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THE SEGMENTED MULTI-THRESHOLD TRANSISTOR:

A SINGLE DEVICE WELL MOSFET STRUCTURE FOR MONOLITHIC SIGNAL CONVERSION

by

© Allan Lloyd Silburt, B.A.Sc.

A thesis submitted to the Faculty of Graduate
Studies and Research in partial fulfillment
of the requirements for the degree of

Master of Engineering

Department of Electronics
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The undersigned recommend to the Faculty of Graduate Studies and Research the acceptance of the thesis:

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ABSTRACT

The Segmented Multi-threshold Transistor (SMT) is a novel Single Device Well MOSFET structure intended for use in data conversion integrated circuits. The device makes use of the back gate bias effect to achieve an array of transistors, each with a unique threshold voltage determined by its mask layout position and the bias conditions on a control element. This thesis investigates the design, fabrication and analysis of an SMT test structure as well as its application to digital to analog (D/A) and analog to digital (A/D) signal conversion circuits.

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LIST OF ABBREVIATIONS

A/D	Analog to Digital
CMOS	Complementary Metal Oxide Silicon
D/A	Digital to Analog
IC	Integrated Circuit
JFET	Junction Field Effect Transistor
MOSBI	Metal oxide Silicon Bipolar
MOSFET	Metal Oxide Silicon field Effect Transistor
OP-AMP	Operational Amplifier
SDW	Single Device Well
SMT	Segmented Multi-threshold Transistor
SOS	Silicon On Sapphire

LIST OF SYMBOLS (cont.)

V_F	Fermi voltage
V_{FB}	flat-band voltage
V_G	gate to source voltage
V_{GN}	n-channel gate to source voltage
V_{GP}	p-channel gate to source voltage
V_T	threshold voltage
$V_T(y)$	threshold voltage as a function of position
V_{TD}	change in threshold voltage due to back gate bias
V_{Teff}	effective threshold voltage
V_{To}	threshold voltage at zero back gate bias
V_w	well potential
V_j	voltage across a junction
V_{ms}	metal-semiconductor voltage
V_o	junction barrier potential
V_s	surface potential
W	n-channel source to drain spacing on the SMT
	channel width on other MOSFETs
x_D	depletion width
y_o	center position of SMT drain segments
y_s	width of SMT surface segments
y	position with respect to the grounded well contact
Z	narrow channel correction factor
ϵ_{ox}	oxide permittivity
ϵ_{si}	silicon permittivity
λ_n	channel length modulation factor (n-channel)
λ_p	channel length modulation factor (p-channel)
μ_n	electron mobility
μ_p	hole mobility

LIST OF SYMBOLS

A_v	voltage gain
a_k	polynomial coefficient of order k
B	square root of the potential between the channel and the well
C_i	input capacitor
C_{ox}	oxide capacitance
C_s	sampling capacitor
E_{ox}	electric field in the oxide
E_{si}	electric field in silicon
I_{DP}	p-channel drain current
I_{DS}	drain current
I_{eff}	effective current
I_p	SDW p-channel drain current
K_n	$\mu_n C_{ox} (W/L)_n$
K_p	$\mu_p C_{ox} (W/L)_p$
KT/q	thermal voltage
L	p-channel gate length, n-channel gate width for the SDW
M	SMT drain segment number
N_{ave}	average impurity concentration
N_{epi}	epitaxial impurity concentration
N_i	intrinsic impurity concentration
N_{sp}	p-type source diffusion impurity concentration
Q_D	depletion charge directly beneath the gate electrode
Q_F	depletion charge in the gate fringe regions
Q_e	total gate depletion charge
Q_{eo}	depletion charge beneath the gate electrode at zero well bias
Q_{ss}	surface state and oxide charge
q	electronic charge
$R_{channel}$	buried channel resistance
R_{series}	well series resistance
R	load resistance
r	correlation coefficient
S	root mean square error
T	series resistance correction factor
t_{ox}	oxide thickness
V_{DD}	drain voltage power supply
V_{DN}	n-channel drain to source voltage
V_{DP}	p-channel drain to source voltage

CHAPTER 1

INTRODUCTION

The purpose of this thesis is to investigate the possible applications and limitations of the Segmented Multi-threshold Transistor (SMT). The SMT is a novel Single Device Well MOSFET structure consisting of a series of surface channel transistors with common gate and source connections and segmented drains. All of the devices are located in a common isolated well as shown in figure 1.1. A voltage gradient is established along the length of the well to cause a range of back gate biases to be applied to each surface transistor. The result is a series of MOSFETs, each with a unique threshold voltage.

The idea was inspired by the Single Device Well MOSFET (SDW) developed at the University of Waterloo by E.Z. Hamdy[1], M. I. Elmasry and Y.A. El-Mansy[2-5]. The SDW is a merged structure consisting of an enhancement type surface MOSFET and a buried depletion MOSFET of opposite carrier polarity sharing the same well and oriented at right angles to each other. In the SDW, the two transistors are inherently coupled together. The gate potential, in general, modulates the conductance of the surface and buried channel, the latter through the variation of the surface depletion layer depth. In addition, current in the buried channel affects the surface transistors via the substrate bias effect. It is the latter property which is exploited in the SMT.

The SDW was modified with the aim of minimizing the coupling between the gate and the buried channel while maximizing the back gate bias effect on the surface transistor. The desired result was a series of surface channel MOSFETs with threshold voltages governed by an independent control element. Experimental results have shown the SMT to have the intended characteristics.

The applications envisioned for the SMT were in Analog to Digital (A/D) and Digital to Analog (D/A) signal conversion. By controlling the threshold voltage of a MOSFET in the above manner it is possible to build comparison circuitry in which the trigger level is dependant on both the Integrated Circuit (IC) mask layout and the bias conditions on

Figure 1.1: SMT test chip layout

Legend: red: P+ diffusion black: N+ diffusion
green: gate oxide blue: metal and contact cuts

the control element. In the case of a parallel or "flash" A/D converter where a large number of comparators are required to achieve a given resolution, the SMT allows the reference voltage divider, which determines the trigger level for each stage, to form a merged structure with the actual comparator circuitry. Thus there is the possibility of a large savings in chip area due to the reduced number of contact holes and interconnect lines in an integrated system.

With these motives in mind, a test structure was developed and integrated which would hopefully exhibit the desired properties. This thesis describes the design and basic evaluation of the SMT test chip and the investigation of its possible applications in monolithic A/D and D/A signal conversion systems.

In chapter two the background theory related to the SDW is developed. Chapter three describes the design, layout and processing of the test structure. In chapter four, the results of static tests on the fabricated devices are presented and a model is described to account for some detailed aspects of its characteristics. Calculations based on this model are then compared with the experimental results.

In chapter five, circuit applications for the SMT are described and the results of some simple A/D and D/A circuits which were breadboarded using the test structure are presented. In addition some design considerations for a fully integrated system are considered and some anticipated difficulties are pointed out. Chapter 6 concludes the thesis and presents some recommendations for further work.

CHAPTER 2 BACKGROUND THEORY ON THE SMT

2.1 INTRODUCTION

This chapter presents the material that forms the background from which the Segmented Multi-threshold Transistor has evolved. This includes a qualitative description of the Single Device Well MOSFET (SDW) as well as theory related to the MOSFET threshold voltage and the substrate bias effect. The operation of the SDW is described briefly and those equations which relate to the SMT are presented. In addition some inadequacies in the SDW theory are discussed.

2.2 THE MOSFET THRESHOLD VOLTAGE AND THE SUBSTRATE BIAS EFFECT

The cross section of a P-type Aluminum gate MOSFET fabricated in an isolated device well is shown in figure 2.1. The threshold voltage of a MOSFET, V_T , is defined as the voltage which must be applied between the gate and source electrodes to induce strong inversion at the semiconductor surface. Strong inversion at the surface is interpreted as the condition where the surface potential is equal to twice the Fermi level, V_F , in the neutral semiconductor below the channel. When this occurs the majority hole concentration at the surface is equal to the majority electron concentration in the bulk.

The gate voltage necessary to induce strong inversion is given by[6]:

$$V_T = V_{FB} - 2V_F - \frac{Q_e}{C_{ox}} \quad (2.1)$$

where:

$$V_F = \frac{KT}{q} \ln \left[\frac{N_{epi}}{N_i} \right]$$

the first term in the above equation represents the voltage on the gate necessary to achieve the flat-band condition. At this point the

Figure 2.1: Cross section of a P-channel aluminum gate MOSFET in an isolated device well.

surface potential, V_s , is equal to that in the neutral well. This flat-band voltage can be broken down into:

$$V_{FB} = V_{ms} + Q_{ss}/C_{ox} \quad (2.2)$$

where Q_{ss} is a lumped quantity representing surface state and oxide charge per unit area and V_{ms} is the metal-semiconductor work function difference.

The third term in equation 2.1 represents the voltage across the oxide capacitance, C_{ox} , necessary to support a depletion charge, Q_e , both of these quantities being expressed per unit area. This can be determined by considering an ideal step junction to be formed between the inversion layer and the well. Assuming a uniform impurity density in the well, the depletion charge is given by:

$$Q_e = [2q\epsilon_{si}N_{epi}(V_s + V_w)]^{1/2} \quad (2.3)$$

Here, the surface potential is measured with respect to the neutral well which may have in turn have an applied voltage, V_w , applied with respect to the source. At the threshold condition, V_s is equal to twice the Fermi potential which, in conjunction with equation 2.1, yields:

$$V_T = V_{FB} - 2V_F - \frac{1}{C_{ox}} [2q\epsilon_{si}N_{epi}(2V_F + V_w)] \quad (2.4)$$

If the threshold voltage for zero well bias is defined as:

$$V_{To} \equiv V_T(V_w=0) = V_{FB} - 2V_F - \frac{Q_{eo}}{C_{ox}} \quad (2.5)$$

where

$$Q_{eo} = [4q\epsilon_{si}N_{epi}V_F]^{1/2}$$

then equation 2.4 can be written as:

$$V_T(V_w) = V_{To} + \frac{Q_{eo}}{C_{ox}} \left[1 - \left(1 + \frac{V_w}{2V_F} \right)^{1/2} \right] \quad (2.6)$$

or

$$\begin{aligned} V_{TD}(V_w) &= V_T - V_{To} \\ &= \frac{Q_{eo}}{C_{ox}} \left[1 - \left(1 + \frac{V_w}{2V_F} \right)^{1/2} \right] \end{aligned} \quad (2.7)$$

In this form the square root dependance of the threshold voltage on well bias can be clearly seen. The extent to which V_T can be modulated is governed by Q_{eo} , C_{ox} and V_F which are all process dependant. The crucial process parameters are the well impurity concentration, N_{epi} , and the gate oxide thickness, t_{ox} , since:

$$C_{ox} = \epsilon_{ox} / t_{ox}$$

where

$$\epsilon_{ox} = \text{oxide permittivity}$$

Thus, a thicker oxide and higher well impurity density will favour a stronger well-bias dependance of V_T . Note that the weaker logarithmic dependance of V_F on N_{epi} is far less significant than the square root dependance of Q_{eo} .

2.3 SDW STRUCTURE

The Single Device Well MOSFET is illustrated in cross-section in figure 2.2[7]. It consists of a surface channel enhancement mode MOSFET stacked on top of a depletion MOSFET of opposite carrier type. The channel of the lower device is formed by the bulk silicon of the device well and is at right angles to the surface channel. Because of the use of the bulk as a current carrying element, the structure can only be fabricated in a technology which can provide the necessary isolation. This restricts it to a mixed MOS/Bipolar (MOSBI) technology, bulk Complementary MOS (CMOS) technology or CMOS Silicon-On-Sapphire (CMOS/SOS). For this thesis, all analysis will be carried out for a P-channel aluminum gate MOSBI technology since this was the only process readily available to the author.

A three dimensional drawing of the SDW is shown in figure 2.3[8]. It is evident that the SDW, although simple to fabricate, presents some problems in analysis because of its three dimensional nature. The perpendicular current flows in the surface and buried channels create inclined and irregularly shaped depletion regions which, for exact analysis, require a 3-dimensional mathematical treatment.

The existence of a depletion region under the surface channel isolates the two currents from direct interaction. However coupling between the two devices results from the modulation of the depletion

Figure 2.2: Cross section of an SDW MOSFET fabricated in MOSBI, bulk CMOS and CMOS/SOS Technologies[6].

region depth and contour due to current flowing in both channels as well as the potential on the gate electrode.

According to Hamdy's analysis[9], the surface channel device behaves as a conventional enhancement MOSFET with an effective threshold voltage which is modified by the potential across the buried channel, V_{DN} . The buried device has a more complex dependence on the terminal voltages. This is illustrated in figure 2.4[10]. The voltage on the gate, V_{GN} , relative to the flat-band voltage, V_{FB} , determines the nature of the buried channel current flow, I_{DN} . With $V_{GN} \gg V_{FB}$, the surface is accumulated and conduction takes place at the surface as well as in the bulk. As V_{GN} approaches V_{FB} a depletion region begins to extend along the surface. This in combination with the depletion region around the well-substrate junction serves to modulate the current in the buried channel. As V_{GN} decreases below V_{FB} , the depletion region increases in depth, pinching off the lower channel in a manner similar to a Junction FET (JFET).

As parts of the surface become strongly inverted conduction begins in the surface device. The depletion region under the inverted part of the channel is then shielded from further dependence on the gate voltage and the depletion depth in this area stays at its maximum value. For $V_{GN} \ll V_{FB}$, the inversion layer covers the entire surface and I_{DN} is no longer influenced by the gate potential.

2.4 SDW THEORY OF OPERATION

In this section some basic equations developed by Hamdy governing SDW behaviour are presented. In particular it is the surface channel device that is of primary concern. The surface transistor is treated by Hamdy as a classical MOSFET with a gradual channel. The effects of the buried channel are taken into account by dividing the width of the surface device into incremental ideal MOSFETS of width dy and integrating the current contribution from each as illustrated in figure 2.5[11]. Each slice is taken to have a threshold voltage which is determined by its position, y , with respect to the buried channel source diffusion.

The $V_T(y)$ relationship is determined by assuming a linear voltage distribution along the buried channel so that the effective substrate

Figure 2.4: Cross section of the buried channel of an SDW MOSFET[9].

Figure 2.5: Top view of the SDW MOSFET showing incremental analysis of the surface device[10].

bias on each slice is given by:

$$V(y) = V_{DN}(y/W) \quad (2.8)$$

Equations 2.6 and 2.7 then become:

$$V_T(y) = V_{To} + \frac{Q_{eo}}{C_{ox}} \left[1 - \left(1 + \frac{V_{DN} y}{2V_F W} \right)^{1/2} \right] \quad (2.9)$$

$$V_{TD}(y) = \frac{Q_{eo}}{C_{ox}} \left[1 - \left(1 + \frac{V_{DN} y}{2V_F W} \right)^{1/2} \right] \quad (2.10)$$

The current in each slice is represented by:

$$dI_p(y) = \frac{\mu_p C_{ox}}{L} \left[(V_{GP} - V_T(y)) V_{DP} - \frac{V_{DP}^2}{2} \right] dy \quad (2.11a)$$

in the triode region, and

$$dI_p(y) = \frac{\mu_p C_{ox}}{2L} [V_{GP} - V_T(y)]^2 dy \quad (2.11b)$$

in the saturation region. The use of these expressions is based on the following commonly made assumptions:

- a) surface potential equal to $2V_F$ everywhere along the slice
- b) no mobile channel charge at or below threshold
- c) a uniform depletion region whose charge is given by equation 2.3.

Integrating the current contributions from each slice the resulting equations are [12]:

$$I_p = \mu_p C_{ox} (W/L)_p \left[(V_{GP} - V_{Teff}) V_{DP} - \frac{V_{DP}^2}{2} \right] \quad (2.12a)$$

$$I_p = \frac{1}{2} \mu_p C_{ox} (W/L)_p [V_{GP} - V_{Teff}]^2 - I_{eff} \quad (2.12b)$$

for the triode and saturation regions respectively where

$$V_{Teff} = V_{To} + \frac{4Q_e V_F}{3C_{ox} V_{DN}} \left[\frac{3V_{DN}}{4V_F} - \left[\left(1 + \frac{V_{DN}}{2V_F} \right)^{3/2} - 1 \right] \right] \quad (2.13a)$$

$$I_{eff} = \mu_p C_{ox} \frac{1}{3} (W/L)_p \left(\frac{2Q_e V_F}{3C_{ox} V_{DN}} \right)^2 \left[\left(1 + \frac{V_{DN}}{2V_F} \right)^{3/2} - 1 \right]^2 - \left(\frac{3V_{DN}}{4V_F} \right)^2 + \frac{9}{8} \left(\frac{V_{DN}}{2V_F} \right)^3 \quad (2.13b)$$

It would appear from these expressions that if V_{DN} were held constant, the surface transistor would have the same characteristics as

a conventional MOSFET with a threshold voltage of V_{Teff} and a saturation current offset by I_{eff} . However, there are several assumptions used in this analysis which limit its accuracy. The first is that the surface transistor makes the transition from the subthreshold region to strong inversion like a typical MOSFET. Because of the positional dependance of the threshold voltage the surface may be only partially inverted over a sizable range of applied gate potential as illustrated in figure 2.4d. Therefore, it is incorrect to integrate equations 2.11a and b over the entire distance from source to drain in this transition region. In fact, the SDW surface transistors have a "soft" turn-on characteristic as the inversion layer spreads across the surface towards the buried channel drain. This gradual transition is further enhanced by the contribution of subthreshold current from the parts of the channel not yet strongly inverted.

This is illustrated in figure 2.6 which shows the drain current versus gate voltage characteristic of the surface device of an SDW structure. Here, the drain voltage of the p-channel transistor was held constant at -100 mV. The characteristics were measured first with a buried drain voltage of 5 Volts while the buried source was grounded. The same procedure was repeated with a potential applied uniformly over the entire well such that the gate voltage matched the previous case at a drain current of 20 microAmps. With a uniform well potential the transistor behaves like a conventional MOSFET with a fixed back-gate bias. It can be seen that the transition out of the subthreshold region is considerably more gradual when a current flows along the buried channel.

In order to measure the threshold voltage, one usually assumes a simple expression for drain current and extrapolates this down to the transition region. When taking such measurements, the voltages are kept as low as possible in order to avoid the effects of the electric field dependance of carrier mobility which influences the slope of the drain current characteristic. However, the soft turn-on of the SDW prevents the use of the low current regime for extrapolation. As a result there is some question about the measurement and possibly the definition of a threshold voltage for the surface device.

Another consequence of the positional dependance of V_T for the

Figure 2.6: I_{DP} versus V_{GP} for a twin SDW structure. Both surface transistors are driven in parallel (effective $W/L = 10$) and $V_{DP} = -0.1$ Volts.

(a) with current flowing along the buried channel,

$V_{DN} = 5.00$ Volts

(b) with uniform well potential, $V_W = 1.58$ Volts

incremental MOSFET slices in equations 2.11a and b is that the saturation voltage is also a function of position. Therefore the transition from the triode to the saturation region should also be gradual. By integrating either 2.11a or 2.11b across the entire surface, the resulting expressions for drain current will not be accurate within this transition.

The assumption that the voltage distribution along the buried channel is linear is also questionable since the profile of the depletion region varies in both of the lateral directions. This can be seen by referring to figure 2.3. Along the length of the lower channel, the shape of the depletion region is dependant on the gate voltage as well as V_{DN} . Along the surface channel length, the depletion depth varies with V_{DP} as in conventional MOSFETs. The constriction in the buried channel that is responsible for the gate modulation of I_{DN} also decreases the conductance along that section of the channel. The narrowness of the constriction is dependant on V_{DN} and V_{GN} up to the point where the entire surface is strongly inverted. The contours in the x-direction will depend on V_{DP} and will differ in shape after the device enters saturation. None of this behaviour is covered in the simple analytical model developed by Hamdy and understandably so in view of the complicated nature of the problem. More accuracy was obtained by Hamdy when modeling the SDW on a computer as a partitioned array of parallel surface channel and series buried channel devices as described in reference 3.

In the present work, the design of the SMT centered on creating a structure in which many of the simplifying assumptions made by Hamdy are justifiable so that a predictable and usable threshold behaviour is obtained. As a preliminary study to determine the feasibility of the SMT concept, an experiment was carried out on the SDW structure shown in figure 2.7[13]. This device was originally intended as a vehicle for investigating SDW differential stages. It consists of two surface transistors of equal dimensions side by side above a long and narrow buried device. The threshold voltages of the two surface MOSFETs were measured as a function of buried channel potential. The experiment was performed first with the buried channel source and drain connected together to provide a uniform well bias and then with a voltage

Figure 2.7: Photomicrograph of the twin SDW structure[13].

gradient along the lower channel.

The threshold voltage was determined by connecting the gate to the drain of the surface device and measuring the drain current at drain voltages of -4, -5 and -6 Volts. This forces the transistor to operate in the saturation region. The threshold voltage can then be determined from the intercept of a linear regression of the square root of I_{DP} onto V_{DP} [14]. This is in accordance with a first order model of the drain current of a MOSFET in which:

$$I_{DP} = \mu_p C_{ox} (W/L)_p [V_{GP} - V_T]^2$$

The results of the experiment are shown in figures 2.8 and 2.9. Also shown in figure 2.8 is a line representing the ideal threshold behaviour predicted by equation 2.6. For the case of uniform well bias (i.e. both well contacts held at the same potential), the characteristic follows equation 2.6 up to a maximum well bias of about 4 volts after which the curve saturates at a maximum threshold voltage of about 2.7 volts. This can be explained by considering the width of the depletion region between the junctions formed by the epitaxial layer with the channel, substrate and P+ drain diffusion. These can be approximated by ideal step junctions in which case their depletion widths are given by:

$$x_D = \left[\frac{2\epsilon_s \epsilon_i}{q N_{epi}} (V_j - V_0) \right]^{1/2} \quad (2.14)$$

where

$$V_0 = \frac{2KT}{q} \ln \left[\frac{N_{epi}}{N_i} \right] \quad \text{for the channel-epi junction}$$

$$V_0 = \frac{KT}{q} \ln \left[\frac{N_{epi} N_{sub}}{N_i^2} \right] \quad \text{for the epi-substrate junction}$$

and

$$V_0 = \frac{KT}{q} \ln \left[\frac{N_{epi} N_{sp}}{N_i^2} \right] \quad \text{for the epi-source junction}$$

The value for V_j in the above equation is the total applied reverse bias across the junction. In the case of the depletion region beneath

Figure 2.8: V_T versus V_W for the twin SDW structure. The line is drawn through points calculated from equation 2.6 for $Q_{eo}/C_{ox} = 0.338$ Volts.

Figure 2.9: V_T versus V_{DN} for the twin SDW structure. The line is drawn through points calculated from equation 2.15 for $Q_{eo}/C_{ox} = 0.338$ Volts.

the channel, it is assumed that the surface is fully inverted. In this case V_j varies from zero, near the P+ source diffusion, to V_{DP} near the drain. For the epi-P+ source junction, V_j is the sum of the magnitudes of V_{DP} and V_{DN} . For the epi-substrate junction, V_j is simply equal to V_{DN} since the substrate is held at ground potential. The specifications for the UW300 chip[15] show an epitaxial layer thickness of 6 microns and a P+ source junction depth of 3.5 microns. The impurity concentration in the epi layer is given as 6 ohm-cm. Using these figures in equation 2.14, a drain voltage of only 0.4 Volts will deplete the entire region below the drain diffusion all the way down to the substrate-epi junction with $V_{DN}=0$. If V_{DP} is made very small, the depletion region extends down to the substrate-epi junction for $V_{DN} > 5$ Volts. Therefore it is not surprising that the back gate bias effect could only be observed for small values of V_{DN} .

When a current is passed along the buried channel by applying V_{DN} to one N+ diffusion and grounding the other, the results of figure 2.9 were obtained. Also shown are the threshold voltages predicted from theory based on a uniform voltage distribution along the buried channel. These points were obtained by integrating equation 2.9 between the limits corresponding to the position and width of each of the two surface transistors so that:

$$\begin{aligned}
 V_{Teff} &= \int_{Y_0 - Y_s/2}^{Y_0 + Y_s/2} V_T(y) dy \\
 &= V_{To} + \frac{Q_{eq}}{C_{ox}} \left[1 - \frac{4V_{FW}}{3V_{DN}Y_s} \left[\left(1 + \frac{V_{DN}(Y_0 + Y_s/2)}{2V_{FW}} \right)^{3/2} \right. \right. \\
 &\quad \left. \left. - \left(1 + \frac{V_{DN}(Y_0 - Y_s/2)}{2V_{FW}} \right)^{3/2} \right] \right] \quad (2.15)
 \end{aligned}$$

where Y_0 is the center position and Y_s is the width of each of the surface channels. Figure 2.9 shows that the measured threshold voltages are below the predicted values for both devices. This would imply that the net well bias over the width of each transistor is less than that predicted by Hamdy's simple analytical model. Therefore a substantial fraction of the voltage drop along the buried channel must

occur very near to the drain terminal due to the pinching which occurs there. It is concluded that the potential distribution along the buried channel of an SDW with the above structure can not be considered linear and accordingly, the characteristics of such a device can depart significantly from the simple analytical relationships presented by Hamdy. Better accuracy could be obtained using the partitioned SDW[3] model on a computer. However, this type of model would be difficult to use in creating an SMT layout since it would not yield an analytic relationship between a desired surface channel threshold voltage and its required layout position.

2.5 CONCLUSIONS

In this chapter the SDW MOSFET has been presented along with some review of its operating characteristics. Particular attention has been given to the substrate bias effect and its influence on the surface device. Using some simple measurements on an SDW structure, it was shown that the simple analytical model for the surface transistor near the threshold point is over-simplified. In addition the assumption of a linear potential distribution along the buried channel does not adequately describe the threshold behaviour of the surface transistor. For more accurate prediction of the threshold voltage of the SDW, the effects of the finite epitaxial layer width must be taken into account since the amount of neutral semiconductor available to form the buried channel vanishes with only moderate applied voltages. This results in a pinched buried channel in which the potential profile differs substantially from the linear distribution assumed by Hamdy in his analysis.

CHAPTER 3

THE SMT TEST STRUCTURE

3.1 INTRODUCTION

The Segmented Multi-threshold Transistor differs from the Single Device Well MOSFET in that the buried channel is designed to behave like a linear resistor and not as an FET. In addition the surface transistor is segmented so that a series of devices all share the same well. Significant alterations to the SDW structure were required in order to optimize the back gate bias effect in the surface transistors while avoiding the non-ideal threshold behaviour described in the previous chapter. In this chapter the design considerations for an SMT test structure are presented with attention given to both layout and processing.

3.2 MODIFICATIONS TO THE SDW STRUCTURE

The SMT test structure layout is shown in figure 1.1. It consists of a segmented P-channel surface transistor with common gate and source electrodes and independent drains. The entire structure is set in a single device well defined by P+ isolating diffusions in an N type epitaxial layer. On either end of the well an N+ diffusion defines the buried channel contact points. Cross sections of the structure are shown in figure 3.1 and 3.2.

The most important difference between the SDW and the SMT is that the latter requires that the buried channel be decoupled from the gate. In the SDW the modulation of the buried channel current, I_{DN} , by the gate will in turn affect the threshold voltage of the surface device. If this occurs, the relationship of the surface transistor threshold voltages to their layout positions will change with the bias conditions on the well and in addition will be sensitive to process variations. In order to minimize the effects of V_G on I_{DN} , the changes in the depletion width under the surface channel regions should be small

Figure 3.1: Cross section of the SMT along the buried channel.

Figure 3.2: Cross section of the SMT along one surface transistor segment.

compared to the thickness of the buried channel. This requires a sufficiently deep and heavily doped well. In addition, by growing thin oxide only in those regions necessary to define a surface MOSFET, the inversion layer is reduced to a series of patches. Thus a large proportion of the area between the N^+ source and drain is covered in thick field oxide under which the depth of the depleted regions (beneath the common gate) is small.

In order to obtain precise and predictable threshold voltages, the well was elongated and minimum width surface devices were used. By reducing the ratio of surface channel width, Y_s , to buried channel length, W , the voltage drop below each of the transistor segments was reduced. For indefinitely narrow transistors equation 2.15 reduces to equation 2.9. This is illustrated in Table 3.1 where the threshold voltages calculated using equation 2.9 and equation 2.15 are shown for $W = 500$ microns and $Y_s = 24$ microns at the eight positions which were later used in the design. The error in equation 2.9 is less than .1% in the worst case which occurs at the segment closest to the grounded side of the well since the gradient of equation 2.9 is largest for small values of Y . Decreasing the ratio of Y_s to W also reduces the soft turn-on effect described in the previous chapter. This provides a crisper threshold which is desirable when the device is used in A/D comparator circuitry.

3.3 SMT DESIGN CONSIDERATIONS

The SMT test structure was designed to suit the metal gate MOS/Bipolar processes at the University of Waterloo and Linear Technology Inc. of Burlington, Ontario. These were the only processes available to the author which could provide the necessary isolated device wells. The structure was confined to one quarter of the 1.9mm x 1.9mm chip, shown in Figure 3.3, which had to include the necessary bonding pads. This, coupled with the fact that the device had to fit in a 16-pin package, resulted in the choice of an 8-segment SMT with a common gate electrode. Another 8-segment SMT with ion-implanted depletion loads was placed on an adjacent quarter of the chip. It should be noted that the decision to use a common gate was simply to save pins and area. It should function equally well with a segmented

Y_0	V_T from eqn.2.9	V_T from eqn.2.15	Error
32	-3.9042	-3.9004	-3.8 mV (0.097%)
69	-4.4380	-4.4363	-1.7 mV (0.038%)
114	-4.9868	-4.9859	-0.9 mV (0.018%)
168	-5.5368	-5.5362	-0.6 mV (0.011%)
229	-6.0413	-6.0409	-0.4 mV (0.007%)
298	-6.5729	-6.5727	-0.2 mV (0.003%)
376	-7.0989	-7.0987	-0.2 mV (0.003%)
461	-7.6264	-7.6262	-0.2 mV (0.003%)

For: $V_{DN} = 15$ Volts, $N_{epi} = 1.255 \times 10^{16}$, $C_{ox} = 43.9 \text{ } \mu\text{F/cm}^2$
 $\gamma_s = 24 \text{ } \mu\text{m}$, $V_{To} = -3.346$ Volts, $V_F = 0.3546$ Volts

Table 3.1: Comparison of threshold voltages calculated using equation 2.9 and 2.15.

Figure 3.3: Photomicrograph of the SMT test structure.

gate, which is necessary in order to properly implement one of the circuits which will be described in chapter 5.

In order to fit into the necessary area the spacing between the N+ well contacts was chosen as 500 microns. Design rules based on 12 micron line widths were used so that the masks would be compatible with the fabrication lines at Linear Technology Inc. and at University of Waterloo since at the time the layout was completed the processing arrangements were still uncertain.

Since it is desirable to control the relationship between V_T and V_{DN} for each surface transistor so that the resulting circuit has a known data conversion characteristic, the inverse of $V_{TD}(y)$ is required. The ratio of Y_S to W is sufficiently small (.024) to justify the use of equation 2.9 or 2.10. Thus, the inverse of equation 2.10 is easily obtained as:

$$y(V_{TD}) = \frac{2V_{FW}}{V_{DN}} \left[\left(1 - \frac{V_{TD}C_{ox}}{Q_{eo}} \right)^2 - 1 \right] \quad (3.1)$$

By substituting the desired list of threshold voltages in the above equation the values for y can be obtained. Since the threshold levels are layout dependant, non-linear A/D or D/A relationships can be easily implemented. This is particularly useful where non-linear conversion schemes are required.

A linear conversion scheme was chosen for the SMT chip to facilitate easy testing and analysis. A set of values for $y(V_T)$ were generated by a computer program and eight suitably spaced threshold levels were chosen. The values of y were rounded off to the nearest micron and used to set the positions of the centers of the surface transistors on the layout.

For these calculations the values for gate oxide thickness and well impurity concentration were fixed arbitrarily at 800 Angstroms and 8.4×10^{15} atoms/cu.cm. respectively. It can be seen by inspection of equation 2.10 that the set of values chosen for y will maintain a linear V_T relationship regardless of Q_{eo} and C_{ox} since these constants appear outside the square root operator. Thus the mask layout is

independent of the process provided N_{epi} can be treated as a constant. Some minor non-linearities could be introduced if a large discrepancy between the actual value of N_{epi} and that used in calculation occurs due to the weak logarithmic dependance of V_F on well impurity level.

The chip layout was made at the University of Waterloo using the WATMASK program. Since this program requires all lines be entered based on their cartesian co-ordinates, it lent itself very well to the precise placement of the surface transistors. After the WATMASK program was complete, the data were shipped to an Aristo flat bed plotter which was used to cut a pattern in rubylith for each mask level. These were optically reduced and then stepped onto the final mask set. A test insert was added to several rows on the mask to permit some simple process evaluations to be performed on the finished wafers.

The minimum resolution imposed by the mask generating equipment in combination with the WATMASK program was one micron. This resulted in a round-off error in the application of equation 3.1. The positions that were chosen for the surface transistors correspond roughly to the relation:

$$V_{TD} = -0.05 - 0.35(M) \quad (3.2)$$

where M is the SMT segment number which can take on an integer value between one and eight. The 50 mV offset in equation 3.2 was required to allow adequate spacing between segment 1 and the well contact diffusion.

Assuming the theory to be completely accurate and attributing all error to y , the actual threshold voltages corresponding to the rounded values of y can be calculated using equation 2.10. If a least squares straight line is fit to the points, the linearity errors introduced by the round-off can then be found by computing the vertical distance from each point to the line. These figures are listed in table 3.2. The worst case error is 3.804 mV for MOSFET number 4 and the root mean square error, S , as defined in appendix A, is 2.82 mV over a 2.85 volt range (0.1%).

It is evident from the layout that the major resolution limit for the SMT imposed by the mask design occurs near the grounded well

<u>MOSFET SEGMENT NUMBER</u>	<u>LINEARITY ERROR</u>
1	-1.28 mV
2	-0.65 mV
3	-1.15 mV
4	+3.80 mV
5	+1.48 mV
6	-0.94 mV
7	+0.84 mV
8	-2.10 mV

Root mean square error: 2.82 mV (0.1% of V_{TD} range)

For r: $V_{dn}=10$ volts, $C_{ox}=43.2$ nF/sq.cm
 $Q_{eo}=44$ nC/sq.cm, $V_f=0.3441$ Volts

Least squares curve fit: $V_{TD}=-0.04774-0.3500(M)$

Table 3.2: Round-off error estimates for the UW700 mask set

contact diffusion. Here, in order to meet the minimum line spacing for the fabrication process, the devices must be separated by a distance six times greater than the mask resolution limit. In a larger scale system the crowding of the surface transistors can be improved by increasing the dimensions of the well. When the well is elongated, the potential gradient along its length is smaller allowing increased threshold resolution to be obtained per unit length of device well. The well can also be made wider so that it holds more than one parallel row of surface transistors. Additional resolution can then be obtained by locating devices in alternate rows at incremental distances from the well contact which are less than the minimum line spacing.

3.4 SMT FABRICATION

Examining equation 2.10 it is obvious that two process parameters, N_{epi} and C_{ox} , are important in determining the threshold behaviour of the SMT. Figure 3.4 shows the effect of substrate resistivity and oxide thickness on the threshold voltage predicted by equation 2.10. From this it can be seen that a high concentration of impurity is desirable since it increases the sensitivity of V_T to substrate bias.

In order to decouple the buried channel from the gate, the penetration of the depletion regions into the well beneath the gate must be small in relation to the epitaxial layer thickness. This will also serve to improve the linearity of the voltage distribution by providing a uniform cross section in the buried channel through which current can flow. These conditions will be met by increasing both the impurity concentration and thickness of the epitaxial film. However, an excessively large N_{epi} would render the SMT incompatible with most standard IC processes. If the epitaxial layer thickness is made too large, problems arise in isolating the device well.

It was desired to test the SMT on epitaxial layers with different impurity concentrations so that the influence of these parameters could be better understood. In particular, a layer with a light impurity density corresponding roughly to that of a CMOS well was required in addition to a sample with a high impurity concentration which would optimize the back-gate bias effect. Unfortunately, due to difficulties in obtaining suitable starting materials, the epitaxial layers could

Figure 3.4: V_{TD} versus V_W for different values of N_{epi} and t_{ox} .

(N_{epi} in atoms/cm³ and t_{ox} in Angstroms)

not be specified arbitrarily. The two samples which were obtained had the following parameters provided by the manufacturer (Semimetals Inc.):

Run	Epitaxial Thickness (microns)	Epitaxial Resistivity (ohm-cm)	Substrate Resistivity (ohm-cm)
1	10-18	0.5-0.7	8-12
2	14.3-15.0	1.75-1.80	10.25-11.3

Relevant data for the rest of the process are summarized in Appendix B. Because of the loose specifications on both the impurity concentration and the thickness of the epi layer and the fact that phosphorous, a relatively fast diffuser, was used to dope the layer, a precise figure for N_{epi} after processing could not be obtained. This will be discussed in more detail in the next chapter. A lap and stain of the finished wafers from run 2 indicated that the substrate-epitaxial layer junction actually moved down to a depth of 21 microns.

In order to provide some insight into the epitaxial layer thickness required to obtain a linear potential distribution, the neutral well which makes up the active portion of the buried channel is approximated by the region shown in dashed lines in figure 3.5. This profile will result in a pessimistic prediction of the potential distribution since it assumes the penetration of gate-induced depletion charge everywhere along the top surface. In fact, the depletion charge under the SMT gate would more closely resemble a series of fingers sticking into the buried channel.

Assuming a gradual channel and a uniform impurity density the buried drain current is given by:

$$I_{\text{DN}} = q\mu_n N_{\text{epi}} L D(y) \frac{dV}{dy} \quad (3.3)$$

where $D(y)$ is the thickness of the channel at any point and L is the channel width. For a uniform current flow we can solve for $V(y)$ for a given set of terminal voltages by integrating $D(y)$ according to:

Figure 3.5: Cross section of the SMT device well showing the approximation to the active portion of the n-channel (dashed line).

$$V(y) = \frac{I_{DN}}{q \mu_n N_{epi} L} \int_0^y \frac{1}{D(y)} dy \quad (3.4)$$

For the situation shown in figure 3.5, $D(y)$ can be approximated by:

$$D(y) = X_{epi} [1 - (y/W)H] \quad (3.5)$$

where

$$H = (X_{D8} + X_{S8})/X_{epi} \quad (3.6)$$

Here, X_{D8} and X_{S8} are the widths of the depletion regions under segment number 8 at the surface and substrate junctions respectively and W is the distance between the edges of the buried channel contacts (see figure 3.5). Substituting this into equation 3.4 the result is:

$$V(y) = - \frac{I_{DN} (W/L)}{q \mu_n N_{epi} X_{epi} H} \ln[1 - (y/W)H] \quad (3.7)$$

Expanding this in a power series:

$$V(y) = - \frac{I_{DN} (W/L)}{q \mu_n N_{epi} X_{epi} H} \left[(y/W) + \frac{H}{2}(y/W)^2 + \frac{H^2}{3}(y/W)^3 + \dots \right] \quad (3.7)$$

From this we can see that in order to obtain a linear potential distribution along the channel, in figure 3.5 the condition $H \ll 2$ must be met.

For a voltage of 15 Volts applied to the buried drain terminal and a gate voltage above the threshold of all of the surface MOSFETs the depletion layer depths can be computed using equation 2.14. This calculation yielded values for H of 0.1 and 0.2 for run 1 and 2 respectively for the epitaxial layer data listed above. This corresponds to a second order term contribution of 10% at $V_{DN} = 15$ Volts at the extreme end of the channel. Therefore, based on this pessimistic analysis of the linearity of the potential distribution along the buried channel, these specifications for the epitaxial layer

were considered adequate for the SMT although some channel constriction effects might be expected on the lightly doped sample.

The fabrications were carried out at the microelectronics lab at the University of Waterloo under the supervision of Mr. R. Grant. The processing sequence was similar to that for standard bipolar circuits with the addition of an extra mask used to define the gate regions and the subsequent thin oxide growth. Aluminum was deposited to form the gate electrode and interconnect lines.

The test insert on the finished wafers contained a large capacitor which was probed in order to perform capacitance versus voltage measurements. From this, values for the flat band potential, surface state charge, oxide capacitance and thickness shown in appendix B were calculated. Unfortunately, there was no contact to the device well on the test insert since it was not intended for a well-isolating process and thus the capacitor could not be biased to gain information about the impurity distribution near the surface. Values for the junction depths were found by lapping and staining pieces of the wafer where possible.

In subsequent chapters individual chips will be referred to by their code number, i.e. UW700-2A-11. Here the UW700 refers to the mask set which was the same for both runs. The "2" refers to the second processing run in which the starting material contained the lightly doped epitaxial layer. A "1" in this position would refer to the first run with the heavily doped epitaxial layer. The "A" indicates that the simple SMT test structure was bonded to the package leads. The chip also contained an SMT with ion implanted load transistors. However, due to difficulties in assessing the results of this processing step, experiments on these devices were not carried out. The last digits in the code number are used to label an individual chip. Although some measurements were made on several dice, those reported in the following chapters were carried out on the same chip for the sake of consistency.

3.5 CONCLUSIONS

In this chapter, the design of an SMT test structure has been presented. Evolving from the SDW, this device required special considerations in order to achieve the desired threshold behaviour. Based on this, the development of the mask set as well as the relevant processing parameters has been described. In addition, some attention has been given to resolution and linearity constraints imposed by feature size limitations in both the mask generation program and the photolithographic process.

The values for the epitaxial layer thickness and impurity level were shown to be important in establishing a predictable threshold voltage characteristic. Two different starting materials were processed with differing epitaxial impurity concentrations. Preliminary calculations indicated that the device on the lightly doped epi layer only marginally satisfies the conditions for a linear potential distribution along the buried channel. Therefore the performance characteristics of the SMT were expected to be closer to ideal for the run with the more heavily doped epitaxial layer.

CHAPTER 4

SMT THRESHOLD VOLTAGE BEHAVIOUR

4.1 INTRODUCTION

This chapter presents the results of static tests on the fabricated SMT structure and attempts to account for some observed second order effects by presenting a more detailed analysis of the threshold voltage measurements. The SMT is first studied with a uniform bias on the entire device well, which is analogous to a conventional MOSFET with back gate bias applied. In this configuration the influence of the fringe charge around the gate electrode and the non-uniform impurity distribution in the well can be analysed. This forms a basis for understanding the device when a current is passed along the buried channel. In this case the resulting non-uniform back gate bias across the width of each surface transistor results in an irregularly shaped depletion region. The effect of this depletion charge distribution on the threshold voltage is considered in some detail. Constrictions in the buried channel caused by the penetration of the space charge layers beneath the surface devices are also shown to play a minor role in explaining the threshold behaviour of the SMT fabricated on the lightly doped epitaxial layer.

4.2 SMT TERMINAL CURRENT BEHAVIOUR

Various aspects of the SMT structure are designed to decouple the buried channel from the gate. This is necessary in order to establish independent control over the threshold voltage of the individual surface transistors. As a preliminary measurement the effect of the gate voltage, V_G , on the buried channel current, I_{DN} , was observed. The channel resistance with zero volts on the gate was 1.30 Kohms for the device with the heavily doped epitaxial layer (UW700-1A-6) and 4.49 Kohms for the device with the lightly doped layer (UW700-2A-11). When the gate voltage was changed from 0 to -15 Volts the channel resistance

changed by 10 ohms and 82 ohms respectively. This was deemed sufficiently small to consider the channel decoupled from the gate. However, as will be shown later, although there is little change in current, the change in potential distribution caused by slight pinching of the lower channel can influence the threshold behaviour of the surface transistors.

The drain current characteristics of a typical surface transistor are shown in figure 4.1a. Here the P-channel drain potential, V_{DP} , was held constant at -100 millivolts while the current was plotted against gate voltage for MOSFET 1. For curve (a) a current corresponding to $V_{DN}=14.97$ Volts flowed along the buried channel whereas for curve (b) a uniform well potential was applied such that the gate voltage and drain current matched curve (a) at 2 microAmps. From this it can be seen that the soft turn-on is less apparent compared with the drain characteristics of the SDW in figure 2.6.

The drain current for all eight surface segments is shown in figure 4.1b. Here, a potential of 6.67 Volts was applied across the buried channel. The displacement in the curves of each of the eight transistors indicates the threshold voltage spread which is induced by the current flowing in the lower device.

4.3 THRESHOLD VOLTAGE MEASUREMENT

The measurement of the MOSFET threshold voltage, although of common necessity in any MOS IC fabrication line, does present some practical problems. Generally speaking, it is not possible to measure the surface potential under the gate directly. Therefore any attempt to define the strong inversion condition in terms of terminal characteristics must make some assumptions about the device's behaviour. Without going into detail on the many MOSFET models that have been reported, generally an increase in accuracy is accompanied by an increase in complexity. The more complex a model is, the more difficult it is likely to be to extract a quantity like the threshold voltage from a simple laboratory measurement. This can also be attributed, in part, to the fact that the threshold voltage itself is a rather vague quantity. Although it is conventionally defined in terms of a precise surface potential condition, this definition is somewhat

Figure 4.1a: I_{DP1} versus V_G for SMT segment 1. (UW700-1A-6)

Aspect ratio: $Y_S/L = 4/3$, $V_{DP1} = -100$ mVolts

(a) with current flowing along the buried channel,
 $V_{DN} = 14.97$ Volts

(b) with uniform well potential, $V_W = 1.034$ Volts

Figure 4.1b: I_{DP} versus V_G for each of the eight SMT drain segments (UW700-1A-6). $V_{DP} = -100$ mVolts, $V_{DN} = 6.67$ Volts. Extrapolated V_G axis intercept shown as dashed lines where $V_G = V_T + V_{DP}/2$.

arbitrary and is used to distinguish the strong inversion region of operation from the weak inversion region which exhibits different terminal current behaviour. In actual fact, the transition between the two regions is smooth and thus the definition of a precise threshold voltage is uncertain. As a result measuring the threshold voltage usually requires the extrapolation of measurements made within one of the transistor's operating regions.

In most industrial fabrication laboratories the threshold is estimated as the gate to source voltage, V_G , necessary to establish a small drain current, usually 1 microAmp. This is often measured with the drain connected to the gate forcing the MOSFET into saturation. Although this quantity will always be somewhat different from an extrapolated threshold voltage, it is sufficient for process monitoring.

A more accurate measurement is usually obtained by extrapolating the drain current, I_{DP} , versus gate voltage characteristic to find the intercept with the V_G axis. It is more convenient to perform these measurements with the gate and drain terminals connected together. In this case, the simple model for drain current mentioned in chapter 2 can be used to deduce the threshold voltage[14]. Here:

$$I_{DP} = \frac{1}{2} \mu_p C_{ox} (W/L)_p (V_G - V_T)^2 \quad (4.1)$$

and the threshold can be determined from the intercept of a best-fit straight line found by a linear regression of the square root of the measured drain currents onto gate voltage.

Equation 4.1 is an approximation which tends to underestimate the current by an amount which depends on the drain voltage at the onset of saturation[16]. Although it approaches the actual current as the gate voltage tends toward V_T , the extrapolation from higher current levels is uncertain. In performing such a measurement on the SMT, the varying depletion region depth caused by the changes in drain voltage could result in some error if this method were used. This suggests the use of a measurement technique in which the drain potential is held constant at a relatively small value. For these reasons, the threshold

voltages for the SMT were determined from measurements of the drain current and gate voltage in the linear region where, according to the first order model,

$$I_{DP} = \mu_p C_{ox} (Y_s/L)_p [V_{DP}(V_G - V_T) - 1/2(V_{DP})^2] \quad (4.2)$$

where Y_s is the width of the surface segments. For these measurements, V_{DP} is held constant at a small value. The threshold voltage can then be obtained from the V_G -axis intercept, V_{int} , of a best fit straight line through the measured points since

$$V_T = V_{int} - 1/2V_{DP}$$

The results of this extrapolation are shown as dashed lines in figure 4.1b.

In practice, rather than determining the threshold voltage graphically, the gate voltage was measured at four drain currents (-0.5, -1.0, -1.5 and -2.0 microAmps) with a four digit voltmeter and a linear regression was performed. The intercept was then determined from this. The correlation coefficient, r , was also computed and in each case was found to differ from one by between 20 and 200 parts per million. The formulas used in the regression analysis are described in appendix A.

4.4 UNIFORM WELL BIAS CHARACTERISTICS

The well bias dependance of a typical surface transistor on the SMT is shown in figure 4.2. This curve shows the half-power behaviour expected for substrate bias dependance of a MOSFET. To gain more information from the data in figure 4.2 it is useful to display the change in threshold voltage with applied bias as a function of the quantity B , which is defined as:

$$B = (2V_F + V_W)^{1/2} \quad (4.3)$$

where V_F is calculated from the manufacturers specified value of well impurity concentration. Equation 2.7 can then be written as:

$$V_{TD} = \frac{Q_{eo}}{C_{ox}} - \frac{[2q\epsilon_{si}N_{epi}]^{1/2}}{C_{ox}} (B) \quad (4.4)$$

From this it is evident that a plot of the measured threshold voltages versus B should form a straight line if equation 4.4 is accurate. If a polynomial in B is fit to the measured data then the presence of any

• Figure 4.2: V_T versus V_W for the SMT with uniform well bias.

second order or higher terms indicates that the threshold voltage is being influenced by factors not considered in equation 4.4.

Figure 4.3 shows the threshold voltage displayed in this manner. It was found that the data correlated very well when fit to a second order polynomial yielding the following results:

$$V_{TD}(B) = 1.2891 - 1.5641(B) + 0.01758(B)^2 \quad \text{with } r^2 = 0.999994$$

$$V_{TD}(B) = 0.5467 - 0.7041(B) + 0.01123(B)^2 \quad \text{with } r^2 = 0.99998$$

for UW700-1A-6 and UW700-2A-11 respectively. Thus, a small but significant second order term is present.

4.4.1 EFFECTS OF THE NON-UNIFORM IMPURITY PROFILE

The most important assumption implied by equation 4.4 is that the epitaxial impurity concentration can be treated as a constant throughout the depletion region. In fact it would be more accurate to say that the figure representing N_{epi} in equation 4.4 is really the average value of the impurity concentration within the depletion region. If the impurity concentration is non-uniform then its average value will change as the depletion depth changes in response to bias voltage on the well. Thus there is more than one voltage dependant quantity within the square root operator in equation 2.4 which contributes to the depletion charge under the gate. A more general expression for the depletion charge in equation 2.1 would be:

$$Q_e = \int_0^{x_D} qN(x) dx \quad (4.5)$$

A minor consequence of having a non-uniform impurity distribution is that the strong inversion condition at the surface is referenced to the Fermi level at the edge of the depletion region. Since this is logarithmically dependant on the impurity concentration at that point, the value for the Fermi potential, V_F required in the threshold voltage equation will be a weak function of bias. This effect will be quite small unless the distribution fluctuates drastically near the depletion boundary. As a result, if an ion implant is used to adjust the zero-bias threshold voltage of the SMT, it must be shallow enough not

Figure 4.3: V_{TD} versus B for the SMT with uniform well bias. A least squares second order polynomial curve has been drawn through each set of points.

to interfere significantly with the impurity profile near the edge of the depletion region. Since a relatively smooth profile is expected for the test structure, the Fermi level will be treated as a constant in all subsequent analysis.

If the non-ideal threshold behaviour is attributed entirely to the well impurity distribution, the threshold data can be used to deduce the impurity profile in the vicinity of the edge of the depletion region. By breaking up the depletion region into elemental charge sheets parallel to the surface with a charge per unit area of:

$$dQ = qN(x)dx \quad (4.6)$$

then the resulting field due to this charge is:

$$dE = dQ/\epsilon_{si} \quad (4.7)$$

which corresponds to an increment in surface potential of

$$dV_s = (x)dE \quad (4.8)$$

Therefore the total potential difference between the surface and the well is:

$$2V_F + V_W = \int_0^{X_D} \frac{qxN(x)}{\epsilon_{si}} dx \quad (4.9)$$

Differentiating equation 4.9 with respect to X_D and treating V_F as a constant we get:

$$\frac{dV_W}{dX_D} = \frac{qN(x)X_D}{\epsilon_{si}} \quad (4.10)$$

The condition of continuity of electric displacement across the silicon/silicon dioxide interface requires:

$$\epsilon_{ox}E_{ox} = \epsilon_{si}E_{si} \quad (4.11)$$

where the fields in the oxide and the semiconductor at the threshold condition are given by:

$$E_{ox} = \frac{V_T - V_{FB} - 2V_F}{t_{ox}} \quad (4.12)$$

$$E_{si} = - \frac{q}{\epsilon_{si}} \int_0^{x_D} N(x) dx \quad (4.13)$$

Substituting these into equation 4.11 and differentiating with respect to V_T we get:

$$\frac{e_{ox}}{t_{ox}} = -qN(x) \frac{dx_D}{dV_T} \quad (4.14)$$

substituting for $N(x_D)$ from equation 4.9 we obtain:

$$\begin{aligned} \frac{dV_T}{dV_W} &= - \frac{t_{ox}}{\epsilon_{ox}} \frac{\epsilon_{si}}{x_D} \\ &= - \frac{C_{ox} x_D}{\epsilon_{si}} \end{aligned} \quad (4.15a)$$

or

$$x_D = - \frac{\epsilon_{si}}{C_{ox} \left[\frac{dV_T}{dV_W} \right]} \quad (4.15b)$$

Differentiating equation 4.14 again with respect to V_T yields:

$$\begin{aligned} \frac{d^2 V_W}{dV_T^2} &= - \frac{C_{ox}}{\epsilon_{si}} \left[\frac{dx_D}{dV_T} \right] \\ &= - \frac{C_{ox}}{\epsilon_{si}} \left[\frac{dx_D}{dV_W} \right] \left[\frac{dV_W}{dV_T} \right] \end{aligned} \quad (4.16)$$

Substituting equations 4.10 and 4.14 into 4.16 and re-arranging the terms we get:

$$N(x_D) = \frac{C_{ox}^2}{q \epsilon_{si} \left[\frac{d^2 V_W}{dV_T^2} \right]} \quad (4.17)$$

Therefore by using equations 4.15b and 4.17 it is possible to determine

the impurity profile (i.e. x_D and $N(x_D)$) within the depletion region from measurements of the threshold voltage at different values of well bias.

A polynomial can be fitted to the data represented as either an absolute threshold voltage, V_T , or as the change in threshold, V_{TD} , due to back gate bias. Since these two terms differ only by a constant (the zero bias threshold voltage), their derivatives will be the same. Since V_{TD} is preferred when analysing the SMT with a voltage gradient along the well this representation for the threshold data will also be used here. For an n-th order polynomial curve fit:

$$V_{TD}(B) = \sum_{k=0}^n a_k B^k \quad (4.18)$$

$$N(x_D) = -\frac{C_{ox}^2}{2q\epsilon_{si}} \frac{\left[\sum_{k=0}^n k a_k B^{k-1} \right]^3}{\sum_{k=0}^n (k-2) k a_k B^{k-1}}$$

and

$$x_D = \frac{-2\epsilon_{si}}{C_{ox} \sum_{k=0}^n k a_k B^{k-2}} \quad (4.20)$$

These expressions can be verified by substituting them into 4.5 which results in:

$$Q_e = -C_{ox} \sum_{k=1}^n a_k B^k \quad (4.21)$$

When this is substituted back into equation 2.1 the original polynomial representation of $V_T(B)$ is obtained. This method of inferring the impurity profile from the measured V_{TD} versus V_W data was used as discussed below.

4.4.2 NARROW CHANNEL EFFECTS

Another second order effect responsible for the introduction of higher order terms in the threshold voltage relationship is due to the presence of depletion charge in the fringes around the edge of the gate region[17] as shown in figure 4.4. This has the effect of increasing the threshold voltage and can be modeled by the splitting the depletion

Figure 4.4: Cross section along the width of a p-channel segment with uniform well bias showing fringing of the depletion charge at the channel edges. Approximation to the depletion charge distribution is shown in dashed lines.

charge into two components such that:

$$V_T = V_{FB} - 2V_F - \frac{1}{C_{ox}}(Q_D + Q_F) \quad (4.22)$$

The depletion charge directly beneath the gate, Q_D , is determined as before from equation 4.5 and the fringe charge, Q_F , is determined separately. Treated in this manner, the fringe charge is represented as an increment in depletion charge which is smeared uniformly beneath the gate region.

A first approximation to the depleted fringe region is to represent it as a quarter cylinder of charge on each side of the gate with a radius equal to the depletion depth below the corner. However this is found to yield an excessively high contribution to the threshold voltage. In fact the fringe regions are probably smaller than this since the edge of the gate does not act as a point source of charge at the silicon surface. However, the cross-sectional area is no doubt dependant on the depletion depth so that the fringe charge can be represented by the rectangular regions shown in figure 4.4. In this case:

$$Q_F = 2[Z(\frac{x_D}{2})(\frac{1}{y_s})]qN_{epi}x_D \quad (4.23)$$

Here Z is dimensionless quantity which could be determined empirically by measuring the threshold voltage of several MOSFETs having different gate widths. Unfortunately such a set of test structures was not fabricated and thus a value for Z could not be obtained though its value should lie between 0 and 1.

If the simple relationship for the depletion depth given in equation 2.14 is substituted into equation 4.23 the result is a fringe contribution to the threshold voltage which is independent of well impurity concentration and directly proportional to well bias voltage. This corresponds to a second order term contribution to the $V_T(B)$ polynomial. However both equation 2.14 and 4.23 treat N_{epi} as a constant. If we take N_{epi} in 4.23 to be the average impurity density then we can write:

$$\begin{aligned}
 N_{ave} &= \frac{1}{X_D} \int_0^{X_D} N(x) dx \\
 &= \frac{Q_D}{qX_D}
 \end{aligned}
 \quad (4.24)$$

where Q_D is as defined in equation 4.5. Therefore equation 4.23 can be written as:

$$Q_F = Z \left(\frac{X_D(B)}{Y_S} \right) Q_D(B) \quad (4.25)$$

where $Q_D(B)$ and $X_D(B)$ are defined by equations 4.20 and 4.21. The resulting threshold equation is:

$$V_T(B) = V_{FB} + 2V_F - \left(1 + \frac{ZX_D(B)}{Y_S} \right) \left(\frac{Q_D(B)}{C_{ox}} \right) \quad (4.26)$$

In order to use equation 4.26 the true impurity distribution must be known. This requires threshold measurements be made on a MOSFET which is wide enough that fringe effects can be ignored. The resulting polynomial coefficients can be used in equations 4.20 and 4.21 to determine Q_D and X_D . Equation 4.26 will then predict the behaviour of a narrow device in the same well. Unfortunately a suitable transistor was not available on the chip and thus it was not possible to determine the profile independently. This, coupled with the fact that a value of Z could not be obtained, meant that the effects of the non-uniform impurity concentration and fringe charge could not be separated.

In order to illustrate the way in which the fringe and impurity grading effects may be separated using the above approach, an arbitrary value of $Z=0.25$ was chosen. Using the polynomial curve obtained from threshold data on the narrow surface transistors for uniform well potential, V_w , and assuming that the coefficients only reflect the non-uniformity of the well impurity, this profile was determined. Then, the fringe contribution to the threshold voltage was calculated using equation 4.25. This figure was subtracted from the measured threshold voltages and a new polynomial was fitted to the data. The fringe contributions were again calculated and the process was repeated until negligible change was observed in the threshold data with the

fringe contributions subtracted. This was deemed to correspond to the accurate separation of fringe and well profile effects for the assumed value of Z .

The measured threshold voltages and those with the calculated fringe contribution subtracted for each iteration are shown in figures 4.5 and 4.6. Using this method convergence was obtained in two iterations for UW700-1A-6 and three iterations for UW700-2A-11. The corresponding impurity profiles for each iteration calculated from equations 4.19 and 4.20 are shown in figures 4.7 and 4.8. From this it can be seen that there is a sharp increase in the impurity density near the surface. It should be noted that for all reasonable values of Z , the calculated impurity profile would exhibit this decrease in concentration with distance and with a steeper gradient than for $Z=0$. The degree of fall of $N(x)$ increases with the value of Z . This effect is likely due to impurity pile-up at the interface during the high temperature processing steps since silicon dioxide has a tendency to repel the phosphorus atoms which were used to dope the epitaxial layer. These results, although not necessarily accurate, may perhaps be considered as typical for this process. Other processes, such as CMOS would also be expected to have non-uniformities in impurity density near the surface as well as in the interior of the well.

The effects of the impurity pile-up and the fringe charge can be seen to compensate one another. As a result their effect on the threshold voltage is not as severe. Since both of these factors were neglected in the design of the masks, some additional error in the threshold voltage for the eight surface devices can be expected. This will be considered in the following section where the impurity distribution and fringe effect assumed here will be used to pursue further analysis of the SMT with a current flowing in the buried channel.

Figure 4.5: V_{TD} versus B for uniform well bias as measured and with the calculated fringe component subtracted for UW700-1A-6. Second order polynomial curves are drawn through each set of points.

Figure 4.6: V_{TD} versus B for uniform well bias as measured and with the calculated fringe component subtracted for UW700-2A-11. Second order polynomial curves are drawn through each set of points.

Figure 4.7: Calculated impurity profile for UW700-1A-6.

Figure 4.8 Calculated impurity profile for UW700-2A-11.

4.5 NON-UNIFORM WELL BIAS CHARACTERISTICS

The threshold voltages of the 8 surface transistors are shown in figures 4.9 and 4.10 for the UW700-1A-6 and UW700-2A-11 respectively. The data are plotted against the MOSFET number, M , which takes on an integer value between 1 and 8 for each of the eight surface transistors. A value of $M=1$ corresponds to the device closest to the grounded side of the buried channel. A best fit straight line has been drawn through each set of points.

It should also be noted in figure 4.9 that for $V_{DN}=0$, the zero bias threshold voltage varies between each surface device. This presumably results from changes in the flat-band voltage due to random fluctuations in surface state and oxide charge. In order to minimize this source of random error when modelling the device it is more useful to work with the change in threshold voltage, V_{TD} , by subtracting the zero bias threshold voltage from each measurement.

The errors contributed by the non-uniform impurity concentration and fringe effects can be seen by referring to table 4.1. Here, the polynomial curve fit to the uniform well bias data was used in conjunction with the mask position of each surface transistor to calculate a threshold voltage assuming a linear potential variation along the well. By fitting a straight line to these calculated points, their departure from a straight line was found by computing the vertical distances from each point to the line. These figures are shown in table 4.1 for $V_{DN}=10$ Volts. Also shown in the table are the departures from a best fit straight line of the corresponding measured threshold voltages with the zero bias threshold voltage subtracted. The bottom line in the table lists the mean square error, S , for each set of points as defined in appendix A. By comparing these figures to table 3.2 it can be seen that the effects of the fringe charge and impurity distribution have increased the non-linearity of the threshold voltages of the SMT. In future designs, some compensation in the layout for the impurity pile-up and fringe charge should be made to improve the accuracy of the device. This would be achieved by making threshold measurements with uniform back gate bias on a MOSFET with similar dimensions to an SMT segment. A polynomial curve fit to data obtained

Figure 4.9: V_T versus M for UW700-1A-6.

A best fit straight line has been drawn through each set of points for $V_{DN} = 0, 2, 4, 6, 8, 10, 12$, and 15 Volts

Figure 4.10: V_T versus M for UW700-2A-11.

A best fit straight line has been drawn through each set of points for $V_{DN} = 0, 2, 4, 6, 8, 10, 12$, and 15 Volts

MOSFET Segment Number	Calculated UW700-1A-6 (mV)	Measured UW700-1A-6 (mV)	Calculated UW700-2A-11 (mV)	Measured UW700-2A-11 (mV)
M=1	-10.16	-24.15	- 9.71	-11.50
M=2	- 2.30	+ 1.61	- 1.06	+ 9.39
M=3	+ 2.18	+12.37	+ 3.47	+ 0.29
M=4	+10.92	+15.03	+ 8.21	+ 4.18
M=5	+ 8.27	+11.89	+ 6.58	+ 1.07
M=6	+ 2.88	+ 2.65	+ 2.72	+ 0.96
M=7	- 0.18	- 3.59	- 1.00	+ 0.86
M=8	-11.60	-15.82	- 9.21	- 5.25
S	8.60 (0.25%)	15.15 (0.44%)	7.20 (0.46%)	9.21 (0.61%)

Table 4.1: SMT threshold voltage errors for $V_{DN} = 10$ Volts

from uniform well bias threshold measurements would then be used in place of equation 2.10 to determine the mask positions of the surface segments of an SMT fabricated within the same process.

In order to examine the threshold voltage behaviour in more detail the data will again be examined as a function of the quantity B . In this case

$$B = [2V_F + V_{DN}(y/W)]^{1/2} \quad (4.27)$$

where y corresponds to the position of the center of each transistor as defined on the mask. Plotting the data against B in this manner implies that the net substrate bias effect on each transistor can be calculated by assuming that

- a) a linear voltage distribution exists along the buried channel and
- b) the depletion region beneath each gate has a profile similar to figure 4.4 with a depth calculated from the well bias below the center of the channel.

If these two assumptions are correct then the positional dependence of the threshold voltage is implicit in B and the data should follow the exact same trend as that for the uniform well bias.

Figures 4.11 and 4.12 show the measured threshold voltages for a buried drain potentials of 4, 8 and 15 Volts superimposed on the measurements for uniform well bias. For the chips with a heavily doped epitaxial layer (UW700-1A-6) the difference between the two sets of data is only perceptible at larger values of B whereas for the lightly doped case (UW700-2A-11) the difference is significant and increases with the well potential. Therefore the conditions in the device depart somewhat from the above assumptions and the resulting error becomes more pronounced as N_{epi} is decreased and V_{DN} is increased. This points to some effect related to the penetration of the depletion regions into the buried channel. Two possibilities were considered. First, the effect on the threshold voltage of the shape of the depletion charge distribution under the surface transistors was investigated. Secondly, the effect of a constriction in the buried channel beneath a surface device was considered.

4.5.1 EFFECTS OF THE DEPLETION CHARGE DISTRIBUTION ON V_T

When a current flows between the buried source and drain, a

Figure 4.11: V_T versus B for uniform well bias and for $V_{DN} = 4, 8$ and 15 Volts (UW700-1A-6). The second order polynomial curve fit to the uniform well bias data is shown as a solid line.

Figure 4.12: V_T versus B for uniform well bias and for $V_{DN} = 4, 8$ and 15 Volts (UW700-2A-11). The second order polynomial curve fit to the uniform well bias data is shown as a solid line.

potential gradient is set up along the lower channel. As a result each surface transistor has a back-gate bias which varies along its width. It was implicitly assumed when designing the layout that this could be approximated by calculating the bias at the center of the gate and assuming a flat depletion region based on this voltage. In fact the depletion cross-section probably resembles that shown in figure 4.13.

In this diagram the grounded side of the well lies off the page to the left at $y=0$ and the center of the transistor is at the point Y_0 . Since the design rules for the process required that the window in the field oxide which defines the gate region be wider than the channel diffusions, the nominal boundaries of the conducting channel, Y_2 and Y_3 , are within the edges of the gate at Y_1 and Y_4 . This ensures a known channel width in spite of small mask misalignments. Unfortunately it also causes some complications in the analysis.

The major differences between this situation and that of the uniform well bias case are due to the different fringe areas on either side of the gate, the graded bottom edge of the depletion region, and the more rapid decay in the depletion boundary to the right of Y_3 . The first two effects are directly as a result of the gradient in well bias whereas the latter is also due to a non-uniform surface potential which exists under the gate.

In order to model the threshold voltage, the depletion charge is split up into four regions as shown in figure 4.13. The fringe charge (Q_1 and Q_4) is represented by rectangles with area proportional to the depletion width at the edges of the gate as in the previous section. The charge under the gate (Q_2 and Q_3) is approximated by two regions with trapezoidal cross-section. The resulting expressions are:

$$Q_1 = Z \frac{x_D(Y_1)}{Y_s} Q_D(Y_1) \quad (4.28)$$

$$Q_2 = \frac{3}{8} Y_s [Q_D(Y_1) + Q_D(Y_3)] \quad (4.29)$$

$$Q_3 = \frac{1}{8} Y_s [Q_D(Y_3) + Q_D(Y_4)] \quad (4.30)$$

$$Q_4 = Z \frac{x_D(Y_4)}{Y_s} Q_D(Y_4) \quad (4.31)$$

where Q_D and X_D are determined from equations 4.18 and 4.19 using the polynomial curve fit with the fringe component removed and setting

$$B = [2V_S + V_{DN}(y/W)]^{1/2} \quad (4.32)$$

Here, the surface potential, V_S , is assumed equal to twice the Fermi level everywhere between Y_1 and Y_3 , although it is as yet unknown at Y_4 .

By assuming that the surface is moderately inverted between Y_3 and Y_4 and that the channel charge is negligible, the surface potential is effectively unclamped from the $2V_F$ condition and varies with the depletion charge. In addition, it is assumed that the measured voltage for the case shown in figure 4.13 corresponds the threshold condition at the point Y_0 in the center of the transistor. Since the gate potential is the same at the points Y_0 and Y_4 then

$$V_{FB} + 2V_F - \frac{Q_D(Y_0)}{C_{ox}} = V_{FB} + 2V_S(Y_4) - \frac{Q_D(Y_4)}{C_{ox}} \quad (4.33)$$

The unknowns in this equation are $V_S(Y_4)$ and the corresponding value of B , as given by equation 4.32. Although it can not be solved analytically a value for $V_S(Y_4)$ can be obtained using iterative techniques.

A plot of the difference in surface potential between the center and edge of the gate versus position for each of the eight transistors on the UW700-2A-11 chip is shown in figure 4.14 for an applied voltage of 15 volts across the buried channel. From this it can be seen that the surface potential variation is most pronounced near the grounded end of the channel and that it differs from $2V_F$ by to less than 10% in the worst case.

With a value for the surface potential at Y_4 the various threshold voltages can now be calculated from:

$$V_T = V_{FB} + 2V_F - \frac{1}{C_{ox}}[Q_1 + Q_2 + Q_3 + Q_4] \quad (4.34)$$

The threshold voltages predicted by equation 4.34 are shown as "x"'s in figure 4.15. It is evident that equation 4.34 differs negligibly from the uniform well bias data. Therefore, although the

Figure 4.14: Change in surface potential at the gate edge, $V_S(Y_4)$, versus segment position for UW700-2A-11.

Figure 4.15: V_{TD} versus B as measured for uniform well bias, $V_{DN} = 15$ volts and for V_{TD} calculated from the detailed model of the depletion charge distribution.

depletion region assumes an assymetrical shape, the total charge contained within it differs very little from that of a transistor in a well biased uniformly to a potential of:

$$V_W = V_{DN}(Y/W) \quad (4.35)$$

Based on this analysis it must be concluded that the difference between the threshold voltage measurements for uniform and non-uniform well bias shown in figures 4.11 and 4.12 are not due to the threshold voltage model but rather to the assumption of a linear voltage distribution along the buried channel. As a result, the possibility of a constriction in the buried channel due to penetration of the gate depletion charge was considered.

4.5.2 EFFECTS OF CONSTRICTION IN THE BURIED CHANNEL V_T

If the conditions in the well are such that the edge of the depletion region formed at the substrate/epitaxial layer junction approaches the depletion region below the channel then the resulting channel constriction will be responsible for a disproportionately large voltage drop. This situation will be most severe for the transistor farthest from the grounded side of the well (MOSFET 8). In addition the effect will be most noticeable for larger bias voltages and lighter impurity levels in the well since these conditions will enhance the depletion layer widths. The crowding of current of current lines near the buried drain contact will further add to this effect. This is in agreement with the measured threshold voltage data.

If it is assumed that the effect of constriction in the channel is only significant at MOSFET 8 then all of the devices will behave as if a series resistance had been added at the ungrounded well contact. This situation is illustrated in figure 4.16. In this case the equivalent well bias for each transistor is:

$$V_{DN} = V_{WT}(Y/W) \quad (4.36)$$

where

$$T = \frac{R_{channel}}{(R_{channel} + R_{series})}$$

Figure 4.16: Cross section of the SMT along the length of the device well showing the channel constriction under the eighth MOSFET segment due to the penetration of the space charge regions.

Using this value of corrected equivalent well bias to calculate B the measured threshold data for $V_{DN} = 15$ Volts and for uniform well bias are shown in figures 4.17 and 4.18. In figure 4.17 for the chip with the heavily doped well a value of $T = 0.99$ corresponding to a series resistance of 13 ohms was used and in figure 4.18 for the device with the lightly doped well a value of $T = 0.95$ corresponding to a series resistance of 225 ohms was used. These values of T were chosen to correct the threshold voltage of segment 8 at $V_{DN} = 15$ Volts. From this it can be seen that with the value of B corrected for a series resistance the data follows the same curve for both uniform and non-uniform well bias.

One might be tempted to explain this observation by attributing the series resistance to the well contact. However the same resistance would also be expected on the other well contact which would have caused an increase in the threshold voltage of the transistors near the grounded end. Since this was not observed, the resistance must be attributed to action near the V_{DN} contact only. In addition, when the threshold voltages are measured with current flowing in the opposite direction along the buried channel, the results indicate a series voltage drop which shifts to the other side of the well.

Therefore the threshold voltage of the SMT with a potential gradient along the lower channel can be characterized by the same polynomial curve fit to the data with a uniform well bias. This is true provided the effective well bias for each transistor is corrected using equation 4.36 to account for a parasitic resistance near the drain of the buried channel. This effect can be attributed to a slight pinching of the buried channel caused by the penetration of depletion charge beneath the gate. This could be eliminated by increasing either the thickness of the impurity concentration of the epitaxial layer. The use of a buried layer to provide a deep, low resistance conducting path in the channel would also reduce the pinching effect.

Figure 4.17: V_{TD} versus B for uniform well bias and for $V_{DN} = 15$ Volts with B corrected for a series resistance of 13 Ohms (UW700-1A-6). A second order polynomial curve fit to the data is shown as a solid line.

Figure 4.18: V_{TD} versus B for uniform well bias and for $V_{DN} = 15$ Volts with B corrected for a series resistance of 225 Ohms (UW700-2A-11). A second order polynomial curve fit to the uniform well bias data is shown as a solid line.

4.6 CONCLUSIONS

This chapter has presented a detailed analysis of the threshold behaviour of the SMT. By looking at the device with the well uniformly biased and as with a voltage gradient along the buried channel it was possible to establish the relative importance of various second order effects. The influence of a non-uniform well impurity profile near the surface and effect of fringe charge around the narrow surface channels was demonstrated. These were shown to contribute to non-linearities in the threshold behaviour of the SMT. In order to increase the accuracy of the threshold voltages, future designs will have to include some compensation for the impurity distribution and narrow channel effects based on prior measurements for a given fabrication process.

Although the depletion charge under the gate region can take on an asymmetrical shape, it was shown that a simple model based on an equivalent uniform well bias adequately describes the threshold behaviour when current flows along the lower channel. It was also shown that, although the current in the buried channel is, virtually unaffected by the gate voltage, the depletion of the well beneath the eighth MOSFET can cause enough of a change in the potential distribution along the channel to be noticeable in the lightly doped samples at high bias levels. This can be represented by a resistance in series with the active channel. Generally, it was found that most of these second order effects were more severe in the samples fabricated on the lightly doped epitaxial layer.

CHAPTER 5

CIRCUIT APPLICATIONS FOR THE SMT

5.1 INTRODUCTION

One of the major goals in the research was to investigate the possible applications of the SMT in integrated data conversion systems. Since the test structure contained only eight surface transistors it was not possible to construct a usable signal conversion system. However the basic circuit building blocks required were demonstrated using the test structure along with other discrete components.

Since all of the circuit configurations which were investigated revolve around the simple inverting amplifier, the first section of this chapter is devoted to aspects of inverter design relating to the SMT threshold voltage. The next two sections present the D/A and A/D test circuits that were breadboarded and the results which were obtained with them. Both of these circuits address the problem of random variation in threshold voltage by performing dynamic voltage comparisons using capacitor switching techniques.

5.2 SMT INVERTER CHARACTERISTICS

A major consideration in designing circuits around the SMT is in making optimum use of the variable threshold voltage of the individual surface transistors. For an inverter this means having its threshold, or toggle point, dependant on the threshold voltage of the appropriate SMT segment. Another consideration is to achieve an inverter with reasonably high gain in its transition region. This is especially important in A/D voltage comparators to ensure crisp switching characteristics.

An inverter is basically a class A amplifying stage which operates over a large signal range. It consists of a driver transistor and a load element. The characteristics of the inverter depend on the type of load and its dimensions with respect to the driver. In modern

integrated circuit technologies, the load can take on various forms. Since the SMT can only be fabricated in a CMOS or a mixed bipolar/MOS process, the range of possible loads is restricted to polysilicon resistors and complementary bipolar or MOS transistors. Since the mixing of bipolar and MOS technologies is relatively uncommon in industry at the present time, the discussions will hinge on a CMOS environment for the SMT.

The circuit diagrams for three inverting amplifier stages are shown in figure 5.1. In each case the driver transistor represents one SMT segment and therefore has a variable threshold voltage. In figure 5.1a the load is connected as a current source by keeping a constant potential on its gate whereas in 5.1b the gate of the load transistor is connected to the input to form an active pull-up as in conventional CMOS logic gates. In both cases the load transistor is an enhancement n-channel transistor. In figure 5.1c the load is a passive polysilicon resistor, R . If we define the inverter toggle point voltage, V_I , to be that where the output voltage, V_O , equals the input voltage, V_G , then this condition can be forced on the circuit by connecting the input and output terminals together, as shown by the dashed lines in figure 5.1. The circuit will then bias itself to the toggle point condition.

Since the SMT will be used as the driver for an array of inverters the effect of the transistor threshold voltage on the toggle point of the inverter is required. A simple analysis of the circuits under these conditions will allow some insight to be gained into the advantages of each of the inverter configurations. When the input and output terminals of the inverters are connected together, the driver transistor is forced into saturation as is the load device in figure 5.1b. If the bias voltage of the current source transistor in figure 5.1a is assumed to be more negative than the toggle point voltage, it too can be considered to be saturated. Under these conditions, the output voltage for the circuits with active loads are entirely determined by feedback if channel length modulation can be neglected. Equating the currents in the driver and load elements the resulting expressions for the toggle points are:

$$V_I = V_{TP} - \left(\frac{2I}{K_p}\right)^{1/2} \quad (5.1)$$

Figure 5.1: Simple inverting amplifier stages.
 (A) current source load
 (B) active pull-up
 (C) resistive load

for the current source load,

$$V_I = \frac{1}{1 + \left(\frac{K_p}{K_n}\right)^{1/2}} [V_{DD} + V_{Tn} + V_{Tp} \left(\frac{K_p}{K_n}\right)^{1/2}] \quad (5.2)$$

for the active pull-up and

$$V_I = V_{Tp} + \frac{1}{RK_p} - \left[\frac{-2}{RK_p} (V_{DD} - V_{Tp} - \frac{1}{2RK_p}) \right]^{1/2} \quad (5.3)$$

for the resistive load. Here,

$$K_p = \mu_p C_{ox} (W/L)_p$$

$$K_n = \mu_n C_{ox} (W/L)_n$$

and I is the bias current flowing in the stage. V_{Tp} and V_{Tn} are the threshold voltages for the p and n channel transistors respectively.

For the resistive load, the toggle point is non-linearly related to threshold voltage of the driver. This is not desirable since the test structure is designed to generate a linear threshold voltage characteristic. In the case of the current source load, the toggle point is directly dependant on the threshold voltage of the driver transistor.

For the active pull-up circuit, the driver's threshold voltage is scaled by the square root of the ratio of the layout dependant parameters K_p and K_n . In this case, in order to achieve the widest possible signal span, K_p must be made very much larger than K_n . This will result in a range approaching that of the SMT threshold voltage. Unfortunately this also results in a very slow rise time for the stage due to the asymmetry of the driver and load transistors. When properly designed (i.e. with $K_p = K_n$), the active pull up circuit can provide the best transient performance of all three inverter configurations. This is one of the reasons for its widespread use in CMOS logic circuits. The result is that in practice, in order to maintain good transient response, use of the active pull-up circuit of figure 5.1b imposes a decrease in analog signal range since K_p and K_n will be of the same order.

To examine the gain of the stage near the toggle point a finite

output resistance for the transistor is introduced by using the following expressions for drain current in saturation:

$$I_{DS} = \frac{K_p}{2}(V_G - V_T)^2(1 + \lambda V_{DS}) \quad (5.4)$$

where λ represents the effects of channel length modulation. The incremental voltage gain, A_v near the toggle point is then:

$$A_v = \frac{(\frac{2K_p}{I})^{1/2}}{\lambda_p + \lambda_n} \quad (5.5)$$

for the current source load,

$$A_v = (2/I)^{1/2} \left[\frac{K_p^{1/2} + K_n^{1/2}}{\lambda_p + \lambda_n} \right] \quad (5.6)$$

for the active pull-up and

$$A_v = 1 - [2RK_p(V_{DD} - V_T - \frac{1}{2}RK_p)]^{1/2} \quad (5.7)$$

for the resistive load. In the first two cases, the gain increases as the D.C. current, I , flowing in the stage decreases. For the circuit of figure 5.1a the gain can be made quite large by adjusting the bias source[18]. For the case of figure 5.1b the same control over gain is generally not possible since decreasing the current must be accomplished via K_p and K_n which also appear in the numerator of equation 5.6. For the resistive load the gain near the toggle point is always less than one since this is near the knee of its voltage transfer curve.

From this analysis it would seem that the current source loaded stage is most desirable since it offers the widest signal range with very high gain. However the active pull-up circuit is generally faster since it can actively swing the output toward both power supply rails. The resistively loaded stage is least desirable because of its non-linear V_T dependance and its low gain near the toggle point. Therefore, in applications where speed is important, a trade-off can be made between analog signal range and response time by using the circuit of figure 5.1b. Where the maximum analog range is of prime concern, the circuit of figure 5.1a is preferred.

The transfer characteristics of an inverter with an SMT driver and a current source load are shown in figure 5.2 and with an active pull-up in figure 5.3. Here, the load device was connected to each of the eight SMT segments in turn while 15 Volts was applied to the buried source terminal. Also shown on the axis is the unity gain line ($V_0 = V_G$). The intersection of each transfer curve with this line defines the toggle-point of the inverter. From this it can be seen that the differing threshold voltage of the SMT segments causes a shift in the inverter transfer characteristics. It should also be noted here that the toggle point does not correspond to the same output voltage for each curve. Because of the finite gain of the circuits, the gate voltage required to establish a fixed output voltage for a family of curves would have a slightly different dependence on threshold voltage than would the toggle point. This must be kept in mind when designing circuits with the SMT.

5.3 D/A CONVERSION CIRCUITS

The simplest form of D/A conversion circuit is shown in figure 5.4. It consists of the eight segment SMT (shown within the dashed line) and a single load. The incoming digital signal is first decoded so that only one of the possible eight lines is at logic one. This is used to select one of the SMT segments via an analog switch. This, in combination with the load, forms inverter in which the input and output terminals have been shorted. The circuit then self-biases itself to its unique toggle point level determined by the threshold voltage of the selected SMT surface transistor. This forms the analog output voltage which is the approximate equivalent of the decoded digital input.

The reference voltage for the conversion is actually the potential applied to the buried source, V_{DN} , since this sets the range of the output voltage. This terminal could also accept an analog signal to form a multiplying D/A converter although the transfer function from the V_{DN} terminal to the output would be non-linear due to the half-power dependence of V_T on well bias.

The analog levels measured to 1 mV accuracy for each of the eight segments are shown for the current source load and active pull-up in figure 5.5a and b for $V_{DN} = 15$ Volts. A least squares linear curve fit

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The analog levels measured to 1 mV accuracy for each of the eight segments are shown for the current source load and active pull-up in figure 5.5a and b for $V_{DN} = 15$ Volts. A least squares linear curve fit

Figure 5.2: Voltage transfer characteristics of the SMT inverter array with current source loads for $V_{DN} = 15$ Volts.
 Drivers: UW700-1A-6 Loads: CD4007 nMOS transistors
 (load current approximately 90 μ A)
 The toggle points of each inverter are represented by the intersections of the transfer curves with the unity gain line.

Figure 5.3: Voltage transfer characteristics for the SMT inverter array with active pull-up loads for $V_{DN} = 15$ Volts (UW700-1A-6)
 Drivers: UW700-1A-6 Loads: CU-011 nMOS transistors
 The toggle points of each inverter are represented by the intersections of the transfer curves with the unity gain line.

Figure 5.4: Simple eight level SMT static D/A converter.

Figure 5.5a: V_I versus M for the simple static D/A converter with current source loads. A best fit straight line has been drawn through each set of points.

Figure 5.5b: V_I versus M for the simple static D/A converter with active pull-up loads. A best fit straight line has been drawn through each set of points.

has been drawn through each set of points. In order to obtain a figure for the linearity of the conversion, the root mean square error, S , was calculated according to the formula in Appendix A. This figure, expressed as a percentage of the toggle point range, gives an indication of the accuracy and usable resolution of the circuit. The resulting values were:

UW700-1A-6 : 8.2 mV (0.20% of V_I range)

UW700-2A-11 : 15.4 mV (0.88% of V_I range)

for the current source loaded inverter and:

UW700-1A-6 : 8.3 mV (0.28% of V_I range)

UW700-2A-11 : 6.8 mV (0.51% of V_I range)

for the active pull-up.

One of the problems in utilizing the SMT in signal conversion is the random fluctuation in threshold voltage between segments. Variations in the range of tens of millivolts are common even between adjacent devices on the same chip [19]. This results in an error which limits the attainable resolution to about six or seven bits. If this error is assumed to be due to effects which have been incorporated into the flat band voltage (i.e. variations in the oxide charge or surface state density) then the change in threshold voltage due to the application of well bias should not be directly affected. Therefore by subtracting the zero bias threshold voltage for each segment, the useful range of the device can be extended. This assumption is borne out by the fact that if the toggle points for the circuit shown in figure 5.4 are measured with V_{DN} set to zero and these values are then subtracted from the data of figure 5.5, the mean square error is reduced noticeably in each case.

A circuit which performs this subtraction dynamically is shown in figure 5.6. Here, the buried source terminal is switched between V_{DN} and ground as clock phase B switches from logic "1" to "0". The resulting waveform on the gate of the SMT is a square wave in which the voltage alternates between the zero bias toggle point and the biased toggle point of the selected segment. The two levels are then subtracted across capacitor C_s .

During clock phase A, the buried source is grounded and C_s stores the difference between the zero bias toggle point and the offset

voltage of the first operational amplifier. During clock phase B, the change in voltage across C_s is transferred to capacitor C_H . The following stage acts as a sample and hold amplifier and is driven by a delayed clock to eliminate the transients at the output terminal. Thus a complete conversion is obtained after one two phase clock cycle. In figure 5.7, oscilloscope recordings of the waveforms at the gate of the SMT (middle trace) and at the output of the first operational amplifier (upper trace) are shown. The lower trace in the photograph shows the voltage at the V_{DN} terminal of the SMT.

The resulting toggle points are shown in figure 5.8a for a CD4007 load n-MOS enhancement load connected as a current source. $V_{DN}=15$ Volts. Note that this circuit has the additional advantage of eliminating the large offset from zero of the threshold levels which could present problems in some applications. The RMS error in these measurements in millivolts and as a percentage of the analog range was:

UW700-1A-6 : 4.1 mV (0.11%)

UW700-2A-11 : 7.0 mV (0.42%)

Although the circuit completes one conversion each clock cycle, the speed is limited because of the use of a current source load for reasons mentioned earlier. At the expense of a smaller analog output range the load was replaced by a polysilicon gate n-MOS transistor (CU-011) fabricated at Carleton University with dimensions similar to the SMT segments and connected as an active pull-up. Although this resulted in more symmetrical charging times, large nodal capacitances associated with the breadboarded circuit prevented any reasonable evaluation of the speed capabilities of the SMT. A fully integrated D/A would have to be constructed for a meaningful measurement of the maximum conversion speed. The ultimate speed limitation for the dynamic circuit is likely to be the rate at which the well can be charged and discharged through the V_{DN} terminal. This will depend greatly on the dimensions, depth and impurity concentration in the well. The resulting threshold levels are shown in figure 5.8b. The RMS error in millivolts and as a percentage of the analog range for these measurements were:

UW700-1A-6 : 4.7 mV (0.17%)

UW700-2A-11 : 3.6 mV (0.28%)

It is worth noting here that the non-linearity errors in these measurements are noticeably improved from those of the threshold

Figure 5.7: Oscilloscope recording of waveforms in the dynamic D/A circuit.
Upper trace: output of the first op-amp (2 Volts/division)
Middle trace: SMT gate (2 Volts/division)
Lower trace: SMT buried channel drain (10 Volts/division)
Horizontal scale: 0.1 μ seconds/division

Figure 5.8a: Dynamic D/A converter output levels (current source loads). A best fit straight line has been drawn through each set of points.

Figure 5.8b: Dynamic D/A converter output levels (active pull-up loads). A best fit straight line has been drawn through each set of points.

voltages shown in table 4.1. Some of the error in the observed threshold voltage is no doubt due to inaccuracies in the measurement and extrapolation procedure. It is then possible that the threshold voltage change due to the application of well bias can be more accurately measured by looking at the toggle point of an inverter. However, since the toggle point levels actually exhibit better linearity than the calculated threshold voltage changes in table 4.1, one must conclude that some compensation for the second order effects described in the previous chapter must be taking place. This may be attributed to the fact that the SMT surface transistors are operating in saturation at the toggle point rather than in the linear region where the threshold measurements were made. Subtle differences between the effective threshold voltage of an SMT surface transistor operating in its saturation or linear region would be lost due to the use of the first order drain current expressions throughout this analysis. However, the net result is that the mean square error in the analog levels of the D/A test circuit actually approach those of table 3.2 which are due to the resolution limits on the mask set. Based on the measurements on the UM700-1A-6 chip, the dynamic D/A converter should be capable of resolving at least 8 bits. The static D/A circuit should also be capable of 8 bit resolution.

5.4 ANALOG TO DIGITAL CONVERSION CIRCUITS

Either of the D/A converter circuits discussed previously could be used to construct a successive approximation A/D converter with the addition of a comparator and some digital counting and control circuitry. However, the applications for the SMT in A/D conversion which were investigated centered on the parallel or flash conversion technique. This is the fastest method of A/D conversion in which an incoming analog signal is simultaneously applied to a series of comparators. Each comparator has a threshold level which differs from its neighbour by an amount corresponding to the least significant binary bit. For an n -bit binary output, 2^n comparators are required whose outputs are then coded into binary form. The speed of such converters is basically that of the response time of the comparators and the encoding logic to a change in the analog input.

In its simplest form, a flash A/D converter implemented with the SMT would consist of an array of inverters as shown in figure 5.9. The incoming signal is fed to the common gate line and the output takes the

Figure 5.9: Simple SMT static A/D converter circuit.

form of a "thermometer code" in which all lines up to a certain point are at logic "1" while the rest are at logic "0". The resulting transfer characteristics would be similar to those of figure 5.2 or 5.3. The encoding of this data into binary form could then be performed by subsequent digital circuitry if required. Since it is difficult to obtain sufficient gain with this circuit to achieve the crisp switching levels necessary for higher resolution the inverters would have to be followed by additional gain stages. Ideally the SMT segment should be incorporated into the input stage of a high gain comparator circuit in such a way as to determine its trigger level. Care must be taken in the design to ensure the correct trigger level dependence on the SMT threshold voltage.

The source terminal of both the buried and surface channel transistors should be connected together in order for the position of the surface elements to result in the intended threshold voltages. The common source voltage could be different than ground providing the substrate voltage is adjusted to maintain well isolation. This would require V_{DN} , the reference, to be applied with respect to an ungrounded potential which could result in increased noise sensitivity. Therefore, in general, the sources of both the surface and buried channels should be held at ground. This restricts the possible circuit configurations for the SMT eliminating, among other things, its use as a driver in a differential stage.

The major difficulty which arises when using the SMT in the comparators of a flash A/D converter is the requirement of each stage for its own load device. The problems resulting from fluctuations in the threshold voltage are now greatly compounded by the addition of another transistor as a source of random error. Therefore subtraction of the zero-bias threshold voltage was essential in the A/D test circuits where discrete load transistors had to be used.

To illustrate this, the toggle points were measured for each of the SMT inverter stages for the circuit of figure 5.9. The load devices were eight n-channel MOSFETs connected as current sources with all gates tied to a common reference voltage. These transistors were taken from three different CD4007 chips selected for their similar

characteristics. The CD4007 is a standard CMOS part which has three individual n and p channel transistors available for discrete connection. The toggle points measured for $V_{DN}=15$ -volts are shown in figure 5.10. The points can be seen to lie in groups of 3, 3, and 2 corresponding to the three CD4007 chips used to form the loads. The resulting RMS errors were:

UW700-1A-6 : 114.5 mV (2.9% of V_i range)

UW700-2A-11 : 66.7 mV (3.8% of V_i range)

When the toggle point with V_{DN} set to zero was subtracted from these measurements the curves shown in figure 5.11 resulted. The RMS errors for this set of points were:

UW700-1A-6 : 16.7 mV (0.43% of V_i range)

UW700-2A-11 : 6.3 mV (0.36% of V_i range)

From this, it is obvious that a significant improvement in the error, due to the random variation in MOSFET parameters can be obtained by concentrating on the change in toggle point with applied bias rather than the absolute value of the toggle point voltage. Since the breadboarded test circuit required the use of discrete load transistors, it was not practical to test a static A/D converter based on the circuit of figure 5.9. Therefore, the tests which were carried out centered on the use of dynamic circuits to provide offset correction for the comparators.

A circuit which compares an incoming signal to the difference in the biased and unbiased inverter threshold levels is illustrated in figure 5.12. For simplicity only two inverters are shown in this diagram. The subtraction is performed across capacitor C_i . During the clock phase A, switches S_1 and S_4 are open while switches S_2 , S_3 and S_5 are closed and capacitor C_i charges up to the zero bias toggle point voltage. During the clock phase B, switches S_1 , S_2 and S_5 are opened while switches S_3 and S_4 are closed. During this time the output rises to the biased toggle point level while the bottom plate of C_i floats at the difference in the biased and unbiased toggle points. The input capacitors for each stage are isolated from each other at this time to prevent their charge from being redistributed. During clock phase C, switches S_1 , S_4 and S_5 are closed and switches S_2 and S_3 are open. The input signal now has the zero-bias toggle point voltage

Figure 5.10: Static A/D converter toggle point voltages for discrete transistor current source loads. A best fit straight line has been drawn through each set of points.

Figure 5.11: Change in toggle point due to the application of voltage to the buried drain terminal for the static A/D converter with current source loads. A best fit straight line has been drawn through each set of points.

Figure 5.12: Offset nulling dynamic SMT comparator circuit.

stored on C_i subtracted from it and the difference appears at the gate of the SMT. Since the inverter had previously been self-biased to its toggle point the amplified signal will unbalance the circuit causing the output to move towards V_{DD} or ground.

For a multiple threshold level circuit switches S_1 and S_2 are shared by all stages whereas capacitor C_i and switches S_3 and S_5 must be replicated for each stage. As a result it is desirable to make C_i as small as possible to minimize its area consumption. Unfortunately, since this capacitor has neither of its terminals grounded during portions of the conversion cycle, the voltage stored on it will be sensitive to the effects of stray capacitances. This is due to the voltage divider action which occurs at floating nodes. Therefore the ratio of the value of C_i to the stray capacitance at its terminals places a limit to the accuracy of the circuit. As a result C_i can not be made arbitrarily small. A similar problem was encountered by Dingwall in his design of a monolithic CMOS A/D converter and prompted the use of Silicon on Sapphire technology to minimize the effects of strays.[20].

The circuit of figure 5.12 is actually quite similar to the comparator stage used by Dingwall and shown in figure 5.13. The major difference is that the latter requires a resistor network to generate the reference level for each stage. According to the author, it is the transient loading of the resistive ladder by the comparator which limits the accuracy of this A/D converter. In the circuit of figure 5.12, the reference voltage, V_{DN} , is fed to the buried channel of the SMT which replaces the resistor network in figure 5.13. Thus the potential divider and the comparator form a merged structure which could potentially simplify and compress the layout of an A/D converter chip. However, an extra clock cycle is required to perform the conversion compared to the two non-overlapping clock cycles required in the circuit of figure 5.13. Ultimately, the speed of the dynamic SMT comparator will be limited by the rate at which the well can be charged and discharged through the V_{DN} terminal. As before, this will depend the impurity concentration, depth and lateral dimensions of the well.

Since the SMT test structure had a common gate electrode for all of the devices, an A/D converter based on the circuit of figure 5.12 could

Figure 5.13: High speed autozeroed CMOS/SOS comparator.
(after Dingwall[20])

not be fully implemented. However it was possible to test its feasibility using the circuit shown in figure 5.14. Here, a jumper is used to connect one SMT inverter section to the rest of the circuit. Although all the other stages are also being driven, the zero bias toggle point stored on capacitor C_i will only correspond to the selected segment. The load devices are silicon gate n-MOS transistors (CU-011) fabricated at Carleton University with dimensions similar to the SMT segments. All of the load transistors were taken from the same wafer and bonded four to a package. The selected inverter drives a standard CMOS D-type flip-flop (CD4013B) from which the digital output corresponding to the SMT segment is taken.

A value of 1nF was used for capacitor C_i in order to minimize the effects of stray capacitances on the breadboard. For this reason the clock frequency was kept low (6.5 KHz) in order to allow the relatively small transistors time to drive the large external node capacitances in the circuit. A fully integrated system would no doubt be capable of operating at much higher speeds.

Figure 5.15 shows oscilloscope recordings of the waveforms at the drain of the selected SMT segment (upper trace) and at the common SMT gate (middle trace). The lower trace shows the clock phase A waveform. The measured threshold levels for each stage are shown in figure 5.16 and 5.17 for the UW700-1A-6 and UW700-2A-11 respectively. Also shown are measurements taken with discrete CD4007 n-MOS load transistors connected as current sources. A slight hysteresis was measurable in all of the comparators. This can be attributed to the CD4013 flip-flop which was found to have 34.5 mV of hysteresis at its Data input. For this reason both "on" and "off" going threshold levels are shown in the graphs. The root mean square error for each set of points in millivolts and as a percentage of the threshold level range was found to be:

UW700-1A-6 "on"	:	11.6 mV	(0.40%)
UW700-1A-6 "off"	:	9.2 mV	(0.32%)
UW700-2A-11 "on"	:	4.4 mV	(0.34%)
UW700-2A-11 "off"	:	4.0 mV	(0.31%)

for the active pull-up loads and:

UW700-1A-6 "on"	:	16.4 mV	(0.43%)
UW700-1A-6 "off"	:	17.6 mV	(0.46%)

Figure 5.14: Offset nulling dynamic A/D test circuit.

Clock waveforms as in figure 5.12

All analog switches: CD4066B

$V_{DD} = -12$ Volts, $V_{DN} = 15$ Volts

Figure 5.15: Oscilloscope recordings of waveforms in the dynamic A/D test circuit.

Upper trace: SMT drain segment (2 Volts/division)

Middle trace: SMT gate (2 Volts/division)

Lower trace: Clock phase A (10 Volts/division)

Horizontal scale: 0.2 μ seconds/division

Figure 5.16: Dynamic A/D converter test circuit threshold levels for both active pull-up and current source loads. (UW700-1A-6) A best fit straight line has been drawn through each set of points.

Figure 5.17: Dynamic A/D converter test circuit threshold levels for both active pull-up and current source loads. (UW700-2A-11) A best fit straight line has been drawn through each set of points.

UW700-2A-11 "on"	:	9.5 mV (0.56%)
UW700-2A-11 "off"	:	7.4 mV (0.44%)

for the current source loads. The voltage transfer function of the circuit for each of the eight segments is shown in figure 5.18. For fixed layout, process and power supply conditions, the major factors limiting the resolution of the SMT A/D converter are the random offset errors (due to threshold voltage, component tolerances, etc.), the non-ideal dependency of V_T on V_{DN} as discussed in chapter 3 and the finite gain of the inverter stages. If the mean square error of the measurements on the SMT test circuits are indicative of these effects combined, a fully integrated offset nulling A/D converter would be capable of 7 bit resolution (UW700-1A-6). An estimate for the simple static A/D converter resolution would be between 5 and 6 bits.

5.5 CONCLUSIONS

In this chapter the applications of the SMT in practical A/D and D/A circuits has been demonstrated. It was found that the major problem of compensating for random variations in threshold voltage could be relieved by subtracting the zero-bias threshold level for each stage. This type of circuit can be implemented using analog switches and capacitors to dynamically remove the offset of an inverter formed by an SMT segment and a load transistor. The resulting A/D and D/A circuits showed good linearity and suggest that the SMT is capable of performing as the heart of a medium resolution monolithic signal conversion system.

The maximum conversion speed attainable with the circuits is heavily dependant on the IC fabrication process which is used. For the dynamic A/D and D/A circuits, the speed is limited by the charging and discharging of the buried channel through the V_{DN} terminal and the SMT inverter's ability to drive the sampling capacitor. The first factor will depend on the lateral dimensions, depth and impurity concentration of the well. The latter will depend on the stray and loading capacitances inherent to the process as well as the dimensions of the SMT segments. At the price of limited resolution, much faster performance is possible with the simpler static A/D and D/A conversion circuits, whose speed is limited only by the transient performance of the individual SMT gain stages.

Figure 5.18: Dynamic A/D converter test circuit voltage transfer characteristics for UW700-1A-6, active pull-up CU-011 loads.

CHAPTER 6

CONCLUDING REMARKS

6.1 SUMMARY

This thesis has investigated the characteristics and potential applications of the Segmented Multi-threshold Transistor. The SMT is a novel MOSFET structure which makes use of the back gate bias effect to achieve an array of transistors with a known distribution of threshold voltages. This is accomplished by establishing a voltage gradient beneath a row of surface MOS transistors in an isolated well such that each device receives a back gate bias which is dependant on its mask position and the bias conditions on the well.

By first studying the behaviour of its parent device, the Single Device Well MOSFET, some basic design criteria were established. In order to obtain a linear potential distribution along the buried channel and to decouple it from the gate electrode, a thicker and more heavily doped well was required compared to that used for the SDW. These conditions permit simplifications to be made in the theory governing the device behaviour. This results in some first order design equations in which the well, which forms the buried channel of the SMT, can be treated as a linear resistor. The back gate bias applied to each surface transistor can then be determined by its position with respect to the well contacts.

With this as a starting point, the design and fabrication of an eight segment SMT test structure was carried out. The devices were fabricated using a metal gate Bipolar/MOS process on two different samples of epitaxial silicon. Measurements on this test structure provided information about the device's behaviour and permitted various second order effects to be identified.

The SMT was first observed with a uniform potential along the buried channel. The data were then studied as a function of B , the square root of the voltage across the junction formed between the surface inversion layer and the well. By fitting a polynomial in B to the data, the effect of non-uniformities in the well impurity profile and

fringing charge around the narrow gate regions was illustrated. A peak in the impurity profile was found at the surface due to the pile-up of the phosphorous impurity atoms. The influence of this on the threshold voltage was somewhat compensated by narrow channel effects. If a Boron doped p-type well were used to fabricate the SMT, the depletion of impurity atoms near the surface would be expected and its effect would add to that of the narrow channel to increase the magnitudes of the threshold voltages. §

When a current was passed along the buried channel, the threshold behaviour changed somewhat from that of the uniform well bias case. Although barely noticeable on the devices fabricated on the more heavily doped epitaxial layer, the effect was considerably more pronounced in the samples with the lighter well impurity concentration. This can be attributed to a slight pinching of the buried channel caused by the penetration of the space charge layer into the well beneath the eighth MOSFET segment. A resistance in series with the ungrounded well contact was found to provide an accurate first order correction for the effect. Including this resistance in the determination of the bias applied to each surface transistor, the threshold behaviour of the SMT devices with a current along the buried channel can be adequately described by the same polynomial in B fit to the data measured with a uniform well bias. Generally, it was found that the non-linearities introduced by these second order effects were more severe for the devices fabricated on the lightly doped epitaxial layer. This is due to the larger depletion regions associated with the lower well impurity concentration.

The basic circuit building block for the SMT is the class A inverting stage in which an SMT segment drives an active load. In a CMOS environment, the load would be a complementary enhancement transistor connected as either a current source or as an active pull-up. The latter can exhibit better transient performance at the expense of an attenuated analog range.

Both the A/D and D/A application circuits make use of the dependance of the toggle point of the inverter on the SMT segment's threshold voltage. In its simplest form the SMT D/A converter consists of a row of analog switches controlled by the decoded digital input and

used to select one SMT drain segment. The drain and common gate are connected to a load which is shared by the entire circuit. The resulting inverter self-biases itself to its unique toggle point which forms the analog output.

In a basic A/D converter, the SMT segments are used as common source drivers for a parallel row of high gain comparators. Although a simple inverter could be used as the comparator, it would have to be cascaded with additional stages to obtain sufficient gain to distinguish between adjacent analog levels. Otherwise, a more complex comparator circuit would be required which derives its toggle point from the SMT segment threshold voltage.

The resolution of data conversion circuits built with the SMT depends on the ratio of the analog range to the minimum usable step size. The analog range will increase with:

- the well impurity concentration
- the gate oxide thickness
- the voltage applied to the buried channel

The minimum usable step size depends on the geometric spacing between the surface devices and the accuracy of the resulting threshold voltages. The factors affecting the minimum step size are:

- the minimum design rule separation of the surface transistors (This limitation may be circumvented by the use of parallel rows of surface transistors in a wider device well as discussed in Chapter 3.)
- the precision of mask digitization and feature placement
- the deviation of the SMT threshold voltages from that assumed when designing the layout
- the random variations in V_T of the SMT segments (and the load devices if more than one load is used in the circuit)

The mean square error of the measurements made on the test circuits indicate the accuracy which was obtained as a percentage of the analog range for this layout and process. With proper system design, this could be translated to usable resolution.

In order to compensate for random variations in the absolute threshold voltage which are inherent in MOS processes, offset nulling circuits were designed which generate their output based on changes in

the threshold voltage when bias is applied to the well. This extends the accuracy of the circuits at the price of a reduction in conversion speed. Since the voltage comparisons are made dynamically using capacitor switching techniques, the clock speed is limited by the time needed to charge the sampling capacitors. Another possible speed limitation is the distributed RC time constant of the buried channel which must be charged and discharged for each comparison. This depends on the well dimensions and impurity concentration and was estimated to be about 4 nanoseconds and 10 nanoseconds for the UW700-1A-6 and UW700-2A-11 chips respectively.

The simpler static SMT circuits based on the absolute threshold voltage can operate much faster since no dynamic comparisons are required. However, based on the mean square error measurements, the static circuits using the UW700-1A-6 chip would be capable of at most 6 bit A/D and 8 bit D/A conversion. The UW700-1A-6 dynamic circuits would be capable of 7 bit A/D and at least 8 bit D/A conversion. The higher resolution of the D/A circuits is due to the fact that in this case, all of the SMT inverter stages share a single load transistor. In addition, the inverters are always operated with 100% feedback between the SMT gate and drain terminals and serve primarily to define the toggle points, not as gain stages. These results were achieved using very simple processing and lithography equipment to fabricate the SMT, and with discrete and small scale integration peripheral components in the breadboarded test circuits. It is possible that even better accuracy could be obtained in a fully integrated system fabricated with finer lithographic capability in a self-aligned silicon gate process. This would allow better definition of the segment positions and better matching and tracking of the components values.

Because of the limited drive capability of the unbuffered SMT transistor segments, it was not possible to determine the maximum conversion speed with the test structure due to the large nodal capacitances associated with the breadboarded circuit. Proper measurement of the maximum conversion speed would require a fully integrated system (or an accurate simulation of it) and would depend heavily on the fabrication process. However, given the maximum master

clock frequency, the proposed offset nulling D/A converter would require one complete cycle of a two phase system clock and the A/D converter would require one cycle of a three phase system clock.

6.2 CONSIDERATIONS FOR FURTHER WORK

A major question which still remains unanswered is whether the use of the SMT would provide any significant improvements over existing monolithic A/D and D/A signal conversion circuits. The major figures of merit for these devices are their speed, resolution, linearity and cost. Since it is not possible to put numbers to any of these parameters for the SMT based on the experiments performed on the test structure, this is the obvious direction for future work. A second SMT design and fabrication will then be required, with the device fabricated in a CMOS well and integrated along with sufficient peripheral circuitry to form working A/D and D/A circuits. Since these differ very little from each other, both could probably be implemented on the same chip. Such a realization of the SMT would allow measurements of the conversion speed to be carried out which would give an indication of its potential performance. In addition, the device should be fabricated using modern process and lithography equipment so that the limits of its analog resolution could be measured. This will require altering of the well dimensions as discussed in Chapter three in order to achieve the minimum analog step size for the process.

Although CMOS/SOS circuitry is capable of very high speeds, it is probably not a practical alternative for fabricating the SMT because of the narrow thickness of the silicon islands which are generally used. In order to successfully fabricate the SMT in a bulk CMOS process, a significant increase would have to be made in the depth and possibly the impurity concentration of the CMOS well. This will require deep implantation of large doses of impurity and subsequent drive-ins to be carried out at the beginning of the processing sequence. A 7 μm deep well with an average impurity density of about 5×10^{16} atoms/cm³ would probably be adequate.

It should be noted that a uniform high impurity concentration need not be maintained throughout the well. As was shown in Chapter 4, a substantial decrease in impurity concentration near the surface was

tolerable. This was partly due to the compensating narrow channel effects. However, the fact that the threshold voltage changes with the total depletion charge, which in turn depends on the integral of the impurity distribution within the space charge region, the effects of a nonuniform impurity profile are much less severe than one might expect. In general, the high impurity concentration desirable for optimizing the substrate bias effect need only be maintained to a depth equal to the depletion layer thickness beneath the surface regions for the maximum applied well potential. This would amount to just under 1.5 microns for a buried channel potential of up to 15 Volts with a well concentration of 1×10^{16} atoms/cm⁻³.

The most important design criterion for the well is to provide a buried channel which is sufficiently wide that the effects of the space charge regions beneath the gate do not significantly alter the desired linear potential distribution along its length. If the impurity concentration is significantly higher near the surface than in the bulk of the well, the current will likely be crowded into the surface region. This will increase the sensitivity of the buried channel current to changes in the gate voltage. The ideal profile would be a retrograde well[21] generated by an implant of high dosage peaked at about 4 to 5 microns. Subsequent drive-in and perhaps an additional implant could be used to enhance the surface concentration to the desired level as well as achieving the necessary junction depth.

6.3 ASSESSMENT OF THE POTENTIAL OF THE SMT

As a result of the work of this thesis, it has been shown the back gate bias effect can be usefully applied to A/D and D/A conversion circuits using the SMT. Measurements on the fabricated test structure have shown that predictable and accurate threshold behaviour can be obtained and that non-linearities imposed by various second order effects can be easily characterized and compensated for in the mask and process design.

One characteristic of an SMT signal conversion chip which might be considered undesirable is the requirement of a reference voltage of opposite polarity to the power supply for the rest of the circuitry. For example, an SMT fabricated in an P-well would require a negative

reference voltage be applied to the buried channel. If the SMT source was at ground potential then the power supply for the rest of the circuit would be positive as would the analog signal range. An alternative to this would be to use the SMT as an active pull-up load rather than the driver in inverter circuit configurations. In this case, the buried channel voltage is of the same polarity but larger than the power supply. Unfortunately, this voltage will be referenced to the power supply rail rather than ground which would make it more susceptible to noise. Therefore, in general, a two polarity power supply would be required for circuits using the SMT.

The power supply range of the SMT is limited by the breakdown voltage of the drain to well diode of the surface transistors (about 60 Volts). However, a more severe limit to the reference voltage, V_{DN} , (and thus the analog range) is imposed by the necessity of avoiding pinching of the buried channel by the depletion regions which would cause the accuracy to suffer. This is the reason for the poorer results obtained with the UW700-2A-11 chip where, as noted in Chapter 4, $V_{DN} = 15$ Volts resulted in noticeable alterations to the potential distribution along the buried channel. It should also be noted that the current flow in the well dissipates power (e.g. 0.2 milliWatts for UW700-1A-6 with $V_{DN} = 15$ Volts). However, this is not likely to be a problem since a full scale system would have an even longer buried channel with a higher resistance.

A potential advantage of the SMT is its efficient use of silicon area due to the merging of the reference potential divider with the active conversion circuitry. Conventional designs require a polysilicon, metal or diffused line to be contacted at the tap positions and then connected to the rest of the circuit. In the SMT, the contact to the reference potential is implicit in the physical location of the segments above the buried channel. This, coupled with the simplicity of circuits needed to implement an A/D or D/A converter, could make it a candidate for use as an analog port on digital signal processing chips. With only minor changes in a conventional CMOS process, the SMT circuits should provide fairly high speed medium resolution A/D or D/A signal conversion, while consuming relatively little die area on an integrated circuit.

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APPENDIX A

REGRESSION FORMULAS

The best fit straight line to the measured data was found using the method of least squares[22]. If equation of the line is:

$$V = \alpha(M) + \beta \quad (A.1)$$

then α and β can be determined from:

$$\alpha = \frac{\sum_{i=1}^n V_i (M_i - \bar{M})}{\sum_{i=1}^n (M_i - \bar{M})^2} \quad \text{where} \quad \bar{M} = \frac{1}{n} \sum_{i=1}^n M_i \quad (A.2)$$

$$\beta = \bar{V} - \alpha \bar{M} \quad \text{where} \quad \bar{V} = \frac{1}{n} \sum_{i=1}^n V_i \quad (A.3)$$

provided the denominator of equation A.2 is not zero. The mean square error, S^2 , for the measured points can be estimated from:

$$S^2 = \frac{1}{n-2} \sum_{i=1}^n [V_i - (\alpha M_i + \beta)]^2 \quad (A.4)$$

APPENDIX B UW700 CHIP SPECIFICATIONS

	<u>UW700-1</u>	<u>UW700-2</u>
Substrate Material	<111> Orientation 8 - 12 ohm-cm (Boron)	<111> Orientation 10.25 - 11.3 ohm-cm (Boron)
Epitaxial Layer	<111> Orientation 0.5 - 0.7 ohm-cm (Phosphorous) * $X_{\text{epi}} = 10 - 18 \mu\text{m}$	<111> Orientation 1.75 - 1.80 ohm-cm (Phosphorous) $X_{\text{epi}} = 21 \pm .3 \mu\text{m}$
Isolation Diffusion	Boron Impurity * $X_j > 18 \mu\text{m}$ (X_j = junction depth)	Boron impurity $X_j = 17 \pm .3 \mu\text{m}$
P+ Diffusion	Boron $X_j = 3.3 \pm .3 \mu\text{m}$ $\rho_s = 175 \pm 5 \text{ oms/sq.}$ (ρ_s = sheet resistance)	Boron $X_j = 3 \pm .3 \mu\text{m}$ $\rho_s = 173 \pm 8 \text{ oms/sq.}$
N+ Diffusion	Phosphorous * $X_j < 2 \mu\text{m}$	Phosphorous * $X_j < 2 \mu\text{m}$
Gate Oxide	Dry Oxidation $t_{\text{ox}} = 79.6 \text{ nm}$ $C_{\text{ox}} = 43.4 \text{ nF/cm}^2$ $V_{\text{FB}} = -0.8 \text{ Volts}$ $Q_{\text{ss}} = 1.5 \times 10^{11} \text{ cm}^{-2}$	Dry Oxidation $t_{\text{ox}} = 87.6 \text{ nm}$ $C_{\text{ox}} = 39.4 \text{ nF/cm}^2$ $V_{\text{FB}} = -0.7 \text{ Volts}$ $Q_{\text{ss}} = 1.1 \times 10^{11} \text{ cm}^{-2}$

(derived from Capacitance vs. Voltage measurements)

(* - estimated from process specifications)

Gate Material	Aluminum Thickness: 1 μm	Aluminum Thickness: 1 μm
Design Rules	6 μm design rules 12 μm minimum spacing 12 μm minimum aluminum line widths 12 μm gate widths 18 μm gate lengths	

The layout of the SMT was designed by the author and digitized using the the WATMASK program. The fabrications were carried out by Mr. R. Grant at the Micro Electronics Laboratory at the University of Waterloo, Waterloo, Ontario, Canada (see figures B.1 and B.2).

Figure B.1: UW700 chip mask layout.

Figure B.2: UW700 chip photomicrograph.

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