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**Voltage Controlled Oscillators and
High Q Copper Inductors**

by

John W. M. Rogers, B. Eng.

**A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment
of the requirements for the degree of**

Master of Engineering

in

Electrical Engineering

Ottawa-Carleton Institute for Electrical Engineering

Department of Electronics

Faculty of Engineering

Carleton University

Ottawa, Canada

August, 1999

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acceptance of the thesis

**Voltage Controlled Oscillators and
High Q Copper Inductors**

submitted by

John W. M. Rogers, B. Eng.

In partial fulfillment of

The requirements for the degree of
Master of Engineering

Dr. Calvin Plett, P.Eng.
Thesis Co-Supervisor

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Ottawa, Canada
1999

Abstract

The increasing demand for portable communications equipment has driven companies to produce transceivers at lower cost. This has led to an intense interest in integrating as many components as possible. One high-speed component that has been particularly hard to integrate with acceptable noise performance is the VCO. This is largely due to the poor quality of on-chip passive components in Si IC technologies.

In this thesis, a technique has been developed to add high Q inductors to conventional silicon integrated circuits as a post-processing step. Plating copper over a low k dielectric layer of polyimide forms the inductors. Inductors with a peak Q as high as 17 at a frequency of 2 GHz have been fabricated.

A design methodology for completely integrated voltage controlled oscillators (VCOs) was also presented. Preliminary VCOs using standard on-chip inductors have a phase noise performance of -103dBc/Hz at 100kHz offset from a 1.9GHz carrier and -94dBc/Hz at 100kHz offset from a 4.7GHz carrier. The results for the 2GHz circuit fall short of meeting the GSM standard for cellular applications of -107dBc/Hz at 100kHz offset by only 4dB.

Finally, some versions of the VCOs were integrated with an on-chip LNA, image reject filter, and mixer to form a completely integrated 2GHz front-end receiver. The receiver has 25dB of conversion gain, a 4.5 dB noise figure and uses 100mW of power from a 3V supply.

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Abbreviations

Å	Angstrom
AC	Alternating Current
Al	Aluminum
BJT	Bipolar Junction Transistor
CAD	Computer Aided Design
Cu	Copper
δ	Skin Depth
DC	Direct Current
EM	Electro Magnetic
F	Noise Factor
FM	Frequency Modulation
f_i	Unity Gain Frequency
GHz	Giga-Hertz
G_m	Transistor Transconductance
K	Boltzmann's Constant
K_{vco}	VCO Gain
IC	Integrated Circuit
μm	Micron or micrometer
NF	Nose Figure
PN	Phase Noise
Q	Quality Factor
r_e	Dynamic Emitter Resistance
RF	Radio Frequency
Si	Silicon
Ti	Titanium
VCO	Voltage Controlled Oscillator

Chapter 1: Introduction

The increasing demand for portable communications equipment has driven companies to try and produce more transceivers at lower cost. This has led to an intense interest in integrating as many components as possible.

One of the high-speed components that has been particularly hard to integrate is the VCO (voltage controlled oscillator). Due to the poor quality of on chip passive components in Si IC technologies it has been very difficult to build integrated VCOs with high levels of performance. Specifically, the low quality factor of on chip inductors, and the poor linearity of on-chip varactors have been the limiting factors determining the phase noise performance level achievable with completely monolithic implementations.

Having poor on chip passives has forced many designers to resort to off chip components in order to achieve acceptable performance levels for many modern cellular standards. This involves many additional and costly design steps including board design with the addition of many extra components. Often the added complexity of bond wires, and transmission lines leads to VCOs with performance inferior to completely integrated designs using much lower quality components.

Key to designing a good on-chip VCO is the availability of high quality inductors and highly linear on chip varactors. To this end many complicated processing, and design techniques have been attempted to improve these devices. However, many of the techniques used are not readily available in standard processes.

1.1 Thesis Goals

There were four main thrusts to this research:

- 1) Develop a new metallization process specifically optimized to produce high quality integrated inductors. Most current Si IC processes build inductors

using an aluminum metal layer in the oxide layer above the substrate. In order to improve the Q of the inductor, the new process developed here will move the metal away from the substrate using a thick layer of polyimide. It will also make use of a copper metal layer instead of an aluminum one. Cu deposited in an electroless process will provide a metal layer with 60% of the resistivity of Al metal of the same thickness.

- 2) A related objective is to explore the optimum design and layout of inductors. As well, design techniques to improve inductors in existing technologies were explored.
- 3) Explore new circuit topologies for building VCOs and develop good design methodologies for designing high performance on-chip VCOs. Techniques for the optimization of VCO designs to yield the best performance were explored.
- 4) After designing and implementing a VCO optimized for high performance, and using high Q inductors, this design was integrated with an on-chip LNA, filter, and mixer to produce a completely integrated RF front end on a single chip.

1.2 Thesis Outline

Chapter 2 of this thesis will describe the metallization process developed for this work. Chapter 3 will discuss inductor layout and design. Chapter 4 will review basic oscillator theory. Chapter 5 will discuss differential oscillator design. Chapter 6 will present the measurements of the inductors and the oscillators. Chapter 7 will summarize the thesis.

Chapter 2: Cu Inductor Process Development

It is very unusual for circuit designers to be able to specify the parameters of the process that they are working in. However, in developing a new metallization process the parameters the process was going to have, within the limits of feasibility now had to be decided.

In this chapter some recent work on copper interconnect will be reviewed. The process specifications for making high Q Cu inductors will be outlined, and the process flow will be described.

2.1 Some Recent Work on Cu Interconnects

To date very few papers have been published concerning post-processed Cu interconnects in Si IC technologies for RF applications. IBM [2] has implemented Cu into the back end of one of their CMOS technologies. The company was the first to show some of the advantages of using this metal, rather than Al in order to build high Q on-chip inductors. This company has built inductors with Qs of up to 17 at the 2 GHz band. This clearly shows that this technology has a dramatic advantage over Al where a comparable inductor would have a Q of 4-6. Other groups have been involved in the development of methods to deposit Cu onto Si. One such group [3] at Cornell University developed the basic solution for electroless Cu plating that formed the basis for the interconnect technology developed in this thesis.

2.2 Process Specifications

When inductors are made in Si technology with Al interconnects, they suffer from the presence of relatively high resistance interconnect structures and lossy substrates,

typically limiting the Q to about 5 at around 2GHz. This causes many high speed RF components, such as voltage controlled oscillators (VCOs) or power amplifiers using on-chip inductors to have limited performance compared to designs using off chip components. The use of off-chip components adds complexity and cost to the design of these circuits, which has led to intense research aimed at improving the performance of on-chip inductors.

In order to improve the performance of on-chip inductors it is necessary to both isolate them from the substrate, and to provide a low resistivity metal to lower the resistance of the metal traces. The process will therefore use a thick layer of polyimide to isolate the inductor from the substrate. This low k (low ϵ_r) dielectric places the inductor further from the substrate reducing eddy currents that degrade Q . Capacitive coupling also is reduced, increasing the self resonance frequency of the structure. An electroless copper plating technique is used to provide low resistance lines. A cross section of the new back end stack is shown in Figure 1.

Figure 1. The process stack for the Cu add on process.

2.3 Setting a Design Goal for the Metal Thickness

As the metal gets thicker the resistance of the traces decreases. However, as the metal line thickness increases, the lithography of the process becomes harder to control. Thick metal lines that are made close to one another also suffer from capacitance between the two adjacent side walls. At high frequencies, another effect comes into play as well.

EM waves suffer attenuation as they enter a conductor, so as the frequency approaches the gigahertz range the distance that they can penetrate becomes comparable to the size of the metal trace. The result is that the current becomes concentrated around the outside of the conductor with very little flowing in the center. The depth at which the EM wave's magnitude is decreased to 36.8% (e^{-1}) of its intensity at surface is called the skin depth of the metal. The skin depth is given by [18]:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \quad (1)$$

where ρ is the resistivity of the material, f is the frequency, and μ is the permeability of the metal. Table 1 shows the skin depth of copper over the band of interest.

Frequency	500MHz	1GHz	2GHz	5GHz	10GHz
Skin Depth	2.956 μm	2.09 μm	1.478 μm	0.935 μm	0.661 μm

Table 1. Skin depth of copper at various frequencies.

Since most of the applications for this technology will lie in the 900MHz to 5GHz band it was decided to try and make the Cu about 3.5 μm thick. Choosing this distance means that the center of the conductor is approximately one skin depth from the surface of the metal, but not much more. Going any thicker will yield little advantage at the frequencies of interest because the center of the conductor will form a “dead zone” where little current will flow anyway.

2.4 Setting a Design Goal for the Polyimide Thickness

The only disadvantages to making the polyimide thicker is that it becomes harder to etch vias to the underlying metal layers and it becomes harder to make the polyimide stick to the surface of the wafer. In all other respects making this layer thicker has no disadvantages. However, after some finite thickness the advantage to making this layer

any thicker will decrease. Thus increased effort has diminishing returns. For example making the polyimide as thick as the oxide underneath will cut the capacitive coupling between the Cu lines and the substrate in half. Doubling the thickness of the polyimide will only drop this capacitive coupling to 1/3 of its original value. As a reasonable goal making the polyimide as thick as the total back end stack underneath (about 5 μm) was decided on.

2.5 Process Flow

The starting material for post processing is a completed wafer of integrated circuits (Figure 2). Pads with openings through the passivation layer to the top-level metal are placed where the copper will later make an electrical connection to the underlying circuits. The first step in the process is to sputter etch away any oxide that might have formed on the exposed pads. Then a thin layer of platinum is sputtered onto the surface of the wafer and patterned so that it coats the pads. The platinum protects the Al pads underneath from etches used later in the process. Next, a layer of polyimide is spun onto the wafer. After it is applied, the wafer is baked to harden the polyimide.

After the polyimide has been applied to the wafer, 1000Å of Al is evaporated onto the surface of the wafer and patterned to form a hard mask for etching vias back to the underlying pads. Vias are then plasma etched through to the Al pads. The Al hard mask is then removed.

Figure 2. Cross section of a wafer at various stages in the process.

After the vias have been opened, a layered structure of Ti (1000Å) and photoresist (PR) is used to define the Cu inductor geometry. The Ti is used as a hard mask for plasma etching trenches into the surface of the polyimide. Once the Ti is patterned, trenches are formed in the polyimide by oxygen plasma etching. These trenches form a plating guide for the Cu. If the Cu is deposited without a plating guide, it tends to grow isotropically. This can lead to unpredictable metal widths, or more seriously shorting of closely spaced lines. A seed layer consisting of an adhesion layer of Ti (300 Å) and a Cu layer (2000 Å) and an Al sealing layer (400Å) is then evaporated onto the surface of the wafer. The seed layers on top of the Ti hard mask are then lifted off by agitating the wafers in an ultra-sonic machine while submerged in acetone leaving seed in only the trenches.

Once the seed is deposited and patterned, the Cu inductor is plated using an electroless solution [3]. The solution consists of 8 g/L of $\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$, 23 g/L of TMAH (used to adjust the pH value), 14 g/L of EDTA, 5 g/L of HCHO, and 10 mL/L of RE610

and 12.5 mL/L of Triton (used as a surfactant). The solution is held at a constant 75° C during plating, and the deposition rate is approximately 170 Å per minute. Patterned films have a measured resistivity of 1.8 $\mu\Omega\text{cm}$. The final wafer is depicted in Figure 3.

Figure 3. Completed wafer with Cu plated into the trenches.

Chapter 3: Inductor Design

Of all the passives built at RF frequencies the one that has been the hardest to model and build is the inductor. In Si technologies, it suffers from proximity to the substrate and from high resistance metals.

In this chapter, the basic theory of inductors will be reviewed including a simple definition for quality factor, and an explanation of the self-resonance frequency. A brief review of some recent work on modeling and building inductors will be given. Advice for the optimal layout of the inductors, as well as some methods for increasing the Q of inductors will be discussed.

3.1 A Simple Model for the Inductor

When describing on-chip inductors it is useful to keep in mind an equivalent circuit model for the structure. Figure 4 shows a circuit model with elements that model many of the non-ideal characteristics of these devices. R_s models the series resistance of the metal traces that the inductor is made out of, $C_{\text{oxide/polyimide}}$ models the capacitance from the traces to the substrate, C_{sub} and R_{sub} model the capacitance and resistance of the substrate and C_{IW} models the inter-winding capacitance between the traces.

Figure 4. A simple model for the Inductor.

3.2 The Quality Factor (Q) of Inductors

The quality factor or Q of a passive circuit element is defined as

$$Q = \frac{|\text{Im}(Z_{11})|}{|\text{Re}(Z_{11})|} \quad (2)$$

The Q of an on chip inductor is affected by many things. At low frequencies, the Q tends to increase with frequency because the losses are relatively constant (mostly due to metal resistance R_s) while the imaginary part of the impedance is increasing linearly with frequency. However, as the frequency increases the inductor starts to generate eddy currents in the substrate through magnetic coupling (this is due to R_{sub}). This loss of energy into the substrate causes the effective resistance to grow. In addition, the skin effect starts to raise the resistance of the metal traces at higher frequencies. Thus most integrated inductors have Qs that rise at low frequencies, then have some peak beyond which the losses make the resistance rise faster than the imaginary part of the impedance and the Q starts to fall off again. Thus, it is easy to see the need for proper optimization such that the inductor has peak performance at the frequency of interest.

3.3 The Self Resonance Frequency of an Inductor

At low frequencies, the inductance of an integrated inductor is more or less constant. However, as the frequency increases the impedance of the parasitic capacitance elements starts to become significant. In fact at some frequency, the impedance of the parasitic elements will cancel that of the inductor and the impedance of the whole structure will go to zero. Thus, the inductor will self resonate. At this point the reactive part of the impedance will be zero. Hence, if the inductance is plotted with respect to frequency, the inductance is nearly constant so at frequencies much lower than the self-resonance frequency. However, as the self-resonance frequency is approached the inductance rises and then abruptly falls to zero. Thus, the inductor has a finite bandwidth over which it can be used. For reliable operation it is necessary to stay well backed off

from self-resonance frequency. Since parasitics increase in proportion to the size of the inductor, the self resonant frequency decreases as the size of the inductor increases. Thus the size of on-chip inductors that can be built is severely limited.

3.4 Recent Work on Inductor Modeling and Layout

Inductors have proved very hard to model and build in Si IC technologies. They have also been a topic of much interest in research over the last few years. Simulators that do exist to simulate their performance are often limited in the geometries that they can handle; for example, Gemcap [4] can only handle square structures. Other more recent simulators like ASITIC [5] can handle arbitrary geometries, however the accuracy of this simulator still is not completely satisfactory as the Q can be as much as 50% optimistic.

Other work has focused on layout considerations. These papers have primarily looked at alternative geometries, or special techniques to enhance the Q of the inductors. A paper from IBM [6] has studied substrate coupling from inductors. This paper also made some conclusions about optimal layout of tiedowns around the inductor to improve the Q. Another paper [7] talks about optimal layout of inductors for use in differential circuits. This paper also claims that using inductors in differential configurations causes the effect of capacitance to the substrate to be reduced. This paper also presents a symmetric differential inductor layout.

Some experiments have involved etching out the substrate around the inductor to reduce the losses [8]. These techniques leave the inductor suspended above an air gap isolating it from the substrate.

3.5 Layout of Spiral Inductors

The goal of any inductor layout is to design a spiral inductor of specified inductance, and with Q optimized for best performance at the frequency of interest. In

order to achieve this, careful layout of the structure is required. The resistance of the metal lines causes the inductor to have a high series resistance limiting its performance at low frequencies, while the proximity of the substrate causes the inductor to generate eddy currents raising the effective resistance at higher frequencies. Large coupling between the inductor and the substrate also causes the structures to have low self-resonance frequencies, placing restrictions on the size of the device that can be built. In order to reduce the series resistance, the line widths should be large; therefore, to obtain a given value of inductance the structure must occupy a greater area, increasing substrate loss. Smaller metal lines mean less substrate loss, but more series resistance. The designer must carefully balance these factors to get the best possible performance at the desired frequency.

Traditionally on-chip inductors have been square as shown in Figure 5. This is because these have been easier to model than more complicated geometries. A square geometry is by no means optimal however. The presence of the ninety-degree bends adds a great deal of unnecessary resistance to the structure. Intuitively it is easy to see that as the structure is made more circular the performance will improve. However, few simulators are able to predict the performance of such structures so the designer is often left with iteration as the only possible design approach.

Figure 5. A square on-chip spiral inductor.

A few of “rules of thumb” can be stated in order to help the designer determine an optimum layout. These rules are based on what changing geometries will do to the values in the equivalent model shown in Figure 4.

- 1) **Line Spacing:** At low frequencies (2 GHz or less) keep the line spacing as tight as possible. At higher frequencies due to coupling between turns, larger spacing may be desirable.
- 2) **Number of turns:** This is typically a third degree of freedom. It is usually best to pick something reasonable (anything less than about 7 can be practical depending on the size of the inductor), and then fine-tune the design by changing the area, and line width.
- 3) **Line Width:** Increasing metal width will reduce the inductance (less turns in a given area) but will decrease the series resistance of the lines at low frequencies. Large inductance area means bigger capacitance, which means lower self resonance. Therefore as W goes up, inductance comes down, and the frequency of Q_{peak} gets lower (and vice versa).

- 4) **Area:** The dimensions of the spiral is the last thing to be adjusted. Bigger areas mean that more eddy currents are present, so it tends to increase high frequency losses. Bigger area means longer spirals, which means more inductance. Therefore as A goes up, inductance goes up, and the frequency of Q_{peak} gets lower (and vice versa).

3.6 The Patterned Ground Shield

Since the inductor tends to stir up eddy currents in the substrate, causing additional losses in the inductor and reducing its performance, one method to reduce this effect is to terminate all the EM fields on a ground plane [19] before they enter the substrate. Unfortunately, eddy currents can flow in a conducting sheet of material easier than they can flow in the substrate. One way to get around this problem is to pattern the ground plane such that it still terminates the EM fields, yet makes it very hard for any eddy currents to start flowing. An example of a patterned ground shield that would work for a square inductor is shown Figure 6. Grooves are cut into the plane perpendicular to the direction of eddy current flow. The ground shield has the disadvantage of adding additional capacitance to the inductor causing its self resonant frequency to drop significantly. For best performance the ground shield should be placed as far away from the inductor as possible while still being above the substrate. In a typical bipolar process the polysilicon layer is a good choice.

Figure 6. Patterned ground shield for a square spiral inductor. Inductor not shown.

3.7 *Isolating the Inductor*

Inductors tend to be extremely large structures, and as such they tend to couple signals into the substrate. Therefore care must be taken to avoid coupling signals in the inductors into other parts of the circuit present on-chip through the substrate. Thus around each inductor a ring of tie downs is added. These tie downs are usually placed at a distance of about five line widths from the outside turn of the inductor. This ring should be connected to a grounding potential so that as little signal as possible passes beyond its boundary into the rest of the substrate. The presence of a patterned ground shield as outlined in the previous section may also have the additional advantage of isolating the inductor from the substrate.

Chapter 4: VCO Circuit Theory

In this chapter, the basic theory of on chip LC VCO design including phase noise considerations will be summarized. Topology choices and device size optimization will be discussed.

4.1 The Ideal LC Resonator

At the core of almost all RF oscillators is an LC resonator or tank that determines the frequency of oscillation, and also often forms part of the feedback mechanism used to obtain sustained oscillations. Thus the analysis of an oscillator begins with the analysis of the LC resonator or tank. Consider the ideal LC tank shown in Figure 7. The transfer function for this circuit is given by:

$$\frac{V_{out}(s)}{I_{in}(s)} = \frac{1}{C} \left(\frac{s}{s^2 + \frac{1}{LC}} \right) \quad (3)$$

Figure 7. An ideal parallel LC resonator.

Figure 8. Pole plot of an undamped LC resonator.

This is an example of an undamped second order system with poles on the $j\omega$ axis as shown in Figure 8. It is useful to find the system's response to an impulse of current. In a real system, this could represent noise. If $i(t) = \delta(t)$ the time domain response of the system can be found.

$$v_{out}(t) = \frac{1}{C} \cos\left(\frac{1}{\sqrt{LC}}t\right) \quad (4)$$

From this equation, it is easy to see that this system's response is a sinusoid whose amplitude is inversely proportional to the value of the capacitance of the tank, and whose frequency is given by:

$$\omega_{osc} = \frac{1}{\sqrt{LC}} \quad (5)$$

4.2 The LC Resonator with Losses

The previous discussion assumes that there are no losses in the circuit. However, in all actual circuits there is some form of resistive losses present in the circuit, which will eventually cause the oscillations to die down to nothing. The LC tank is again considered with the addition of a parallel resistor. Losses can come from many sources in the circuit, however an equivalent parallel resistor as shown in Figure 9 can always replace resistive losses.

Figure 9. An LC resonator with resistive loss.

The transfer function of this circuit is given by:

$$\frac{V_{out}(s)}{I_{in}(s)} = \frac{1}{C} \left(\frac{s}{s^2 + \frac{s}{RC} + \frac{1}{LC}} \right) \quad (6)$$

Now the poles have moved back into the left-hand plane and the system has become underdamped as shown in Figure 10.

Figure 10. The Pole plot of an LC resonator with losses.

The time domain response can again be found when the input is an impulse of current.

This time the voltage is given by:

$$v_{out}(t) = \frac{e^{-\frac{t}{2RC}}}{C} \left(\cos \left(\sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}} t \right) - \sin \left(\sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}} t \right) \right) \quad (7)$$

Now the frequency of oscillation is given by:

$$\omega_{osc} = \sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}} \quad (8)$$

showing that in the case of resonator with losses the frequency is always lower. Note that this is also true even if R is negative. If however $R \gg \sqrt{\frac{L}{4C}}$ as is the case in most RF oscillators even during start up this effect can be ignored. Also, note that once steady state has been reached in a real oscillator, R approaches infinity and this term will go to zero.

4.3 Quality Factor of an LC Resonator

The Q (quality factor) of an LC resonator is a figure of merit used often when dealing with LC tanks and oscillators. It is defined as [20]:

$$Q = 2\pi \left(\frac{E_{\text{Stored / Cycle}}}{E_{\text{Lost / Cycle}}} \right) \quad (9)$$

or in terms of circuit parameters:

$$Q = \omega_o RC = R \sqrt{\frac{C}{L}} \quad (10)$$

Another definition of Q that is particularly useful is:

$$Q = \frac{\omega_o}{2} \left| \frac{d\phi}{d\omega} \right| \quad (11)$$

which can be shown to give the same value in terms of circuit parameters as (9).

4.4 Adding Negative Resistance to the Resonator

The resonator is only half of an oscillator. As can be seen from the previous example in any practical circuit oscillations will die away quickly if something is not added in order to maintain them. Therefore, in order to provide sustained oscillation a feedback loop is introduced which acts to generate a negative resistance. If this parallel negative resistance is smaller than the total losses in the circuit then any noise will result in an oscillation that will grow as opposed to dying away with time. Providing this feedback is usually done in one of three popular ways as shown in Figure 11. (Note that other choices are possible.)

- Using the capacitor to form a feedback loop. This is known as a Colpitts oscillator.
- Using the inductor to form a feedback loop. This is known as a Hartley oscillator.
- Using a transistor in an emitter follower configuration. This is known as the negative resistance oscillator probably because it is the only one where the $-R$ cell is completely separate from the tank.

Note that in each case an amplifier must be added so that the gain around the loop is greater than one so that oscillations can start.

Figure 11. Resonators with feedback. (a) Colpitts Oscillator. (b) Hartley Oscillator. (c) Negative resistance oscillator. Biasing not shown.

4.5 Configuration of the Amplifier

The amplifier shown in Figure 11 is usually made using only one transistor in RF oscillators. The negative resistance oscillator (Figure 12) can be thought of as having either a common collector amplifier where Q_1 forms the feed back, or a common base amplifier where Q_2 forms the feed back. The -Gm oscillator is always used in this configuration for reasons of symmetry when the circuit is made differential. The Colpitts and Hartley oscillators can be made either common base or common collector. Common emitter is usually ruled out because it requires large capacitors and RF chokes that are not usually available in a typical IC technology. It also suffers from the Miller effect because neither the collector nor the base is grounded. These two choices are shown in Figure 13 for the Colpitts configuration.

Figure 12. Negative resistance oscillator. Biasing not shown.

Figure 13. Common base and common collector Colpitts oscillators. Biasing not shown.

Having determined the nature of the amplifier, an expression for the negative resistance of the oscillators can now be derived. Consider first the common base Colpitts configuration with the negative resistance portion of the circuit replaced by its small signal model show in Figure 14. Note that V_{π}' and the current source have both had their polarity reversed for convenience.

Figure 14. Small signal model for the Colpitts common base negative resistance cell.

One equation can be written for V_{π}' in terms of the current flowing through this branch of the circuit.

$$I_i + g_m V_{\pi}' = j\omega C_2 V_{\pi}' + \frac{V_{\pi}'}{r_e} \quad (12)$$

This can be solved for V_{π}' noting that $g_m = 1/r_e$.

$$V_{\pi}' = \frac{I_i}{j\omega C_2} \quad (13)$$

Another equation can be written for V_{ce} .

$$V_{ce} = \frac{I_i + g_m V_{\pi}'}{j\omega C_1} \quad (14)$$

Substituting (13) into (14) gives:

$$V_{ce} = \left(\frac{1}{j\omega C_1} \right) \left(I_i + \frac{g_m I_i}{j\omega C_2} \right) \quad (15)$$

Now using (13) and (15) and solving for $Z_i = V_i/I_i$ with some manipulation:

$$Z_i = \frac{V_i}{I_i} = \frac{V_{\pi}' + V_{ce}}{I_i} = \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} - \frac{g_m}{\omega^2 C_1 C_2} \quad (16)$$

this is just a negative resistor in series with the two capacitors. Thus a necessary condition for oscillation in this oscillator is

$$r_s < \frac{g_m}{\omega^2 C_1 C_2} \quad (17)$$

where r_s is the equivalent series resistance on the resonator. Note that the series negative resistance is maximized for a given fixed total series capacitance when $C_1 = C_2$.

An identical expression to (16) can be derived for the Colpitts common collector circuit. Using a similar analysis, equations can be derived for the Hartley versions of these circuits:

$$Z_i = j\omega(L_1 + L_2) - g_m \omega^2 L_1 L_2 \quad (18)$$

this is just the series combination of the two inductors in series with a negative resistor.

For these two circuits a necessary condition for oscillation is:

$$r_s < g_m \omega^2 L_1 L_2 \quad (19)$$

The analysis of the negative resistance amplifier is somewhat different. The small signal equivalent model for this circuit is shown in Figure 15.

Figure 15. Small signal equivalent model for the negative resistance cell in the negative resistance oscillator.

An expression for the amount of current that flows into the circuit can be written as follows:

$$I_i = \frac{V_i}{r_{e1} + r_{e2}} - g_{m1} V_{\pi 1} - g_{m2} V_{\pi 2} \quad (20)$$

Now if it is assumed that both transistors are biased identically then $g_{m1} = g_{m2}$, $r_{e1} = r_{e2}$, $V_{\pi 1} = V_{\pi 2}$, and the equation can be solved for $Z_i = V_i/I_i$.

$$Z_i = \frac{-2}{g_m} \quad (21)$$

Thus in this circuit a necessary condition for oscillation is that:

$$r_p > \frac{2}{g_m} \quad (22)$$

where r_p is the equivalent parallel resistance of the resonator.

4.6 The Oscillator as a Feedback System

Oscillators can also be thought of as a linear feed back system as shown in Figure 16. The Barkhausen criteria for oscillation are usually applied to this model. First note that [21]:

$$\frac{V_{out}(t)}{n_{in}(t)} = \frac{H_1(s)}{1 - H_1(s)H_2(s)} \quad (23)$$

for the system shown in Figure 16. This system will oscillate provided that $H_1(s)H_2(s)=1$.

Figure 16. Linear model of an oscillator as a feedback control system.

It can be instructive to apply this model to the oscillator circuits discussed above. If the loop is broken at some point, and an analysis is performed then some expressions for open loop gain and equations for the conditions of oscillations can be derived. For the purposes of this discussion, however it is necessary only to show how the model applies to the circuits.

As an example of this type of analysis, let us look at the Colpitts common-base oscillator redrawn with the T-Model for the transistor. It is assumed here for simplicity that any resistance present at the emitter of the transistor is large in parallel with the impedance of C_2 . This may or may not be a valid assumption, but for concept illustration purposes it does not matter. The loop can be broken at the emitter as shown in Figure 17.

Figure 17. Feedback analysis of an oscillator.

Case 1 Output at V_x : Two expressions are written; one for the feed forward gain, and one for the feedback gain.

Feed Forward Gain: In finding the feed forward gain it is necessary to always start at the tank and work forward to the output. In this case V_x is capacitively divided to the emitter voltage V_1 and then the voltage at V_1 controls the current $I = g_m V_1$. This current in turn produces the voltage V_x at the output. It is assumed here that the circuit is operating at resonance and that the LC resonator has an impedance of R_{Tank} .

$$H_1(s) = \frac{V_x}{V_1} \frac{V_1}{V_x} = g_m R_{\text{Tank}} \frac{C_1}{C_1 + C_2} \quad (24)$$

Feed Back Gain: In finding the feedback gain it is necessary to start at the output and work back to the tank. The only thing left here is a wire, which has a transfer function of one:

$$H_2(s) = 1 \quad (25)$$

Case 2 Output at V_1 : Again two expressions are written; one for the feed forward gain, and one for the feed back gain.

Feed Forward Gain: Again it is necessary to start at the tank and work forward to the output. In this case starting from V_x the voltage is fed forward to V_1 (the output) again by a capacitive voltage divider.

$$H_1(s) = \frac{V_1}{V_x} = \frac{C_1}{C_1 + C_2} \quad (26)$$

Feed Back Gain: In finding the feedback gain it is necessary to work backwards again to the tank. From V_1 the voltage is again fed back to V_x by way of the current source.

$$H_2(s) = \frac{V_x}{V_1} = g_m R_{\text{Tank}} \quad (27)$$

4.7 Large Signal Non-Linearity in the Transistor

So far, the discussion of oscillators has assumed that the small signal equivalent model for the transistor is valid. If this were true, then the oscillation amplitude would grow indefinitely, which is not the case. Some non-linearity must be introduced as the signal grows in order to reduce the negative resistance of the oscillator until it just cancels out the losses and the oscillation reaches some steady state value. The source of the non-linearity is the transistor itself.

Presumably the transistor is biased somewhere in the active region. At this operating point, the transistor will have a particular g_m . However, as the voltage swing starts to increase, the transistor will start to enter the saturation region at one end of the swing and the cut-off region at the other end of the voltage swing. Which of these effects starts to happen first depends on where the transistor was biased. If the transistor is biased at a low current, then cut-off non-linearity will appear first, however if the transistor is biased at a high current then it may enter saturation first. Ultimately a combination of both effects will almost certainly be present. The presence of these non-linearities will cause the effective g_m of the device to decrease. Eventually with increasing signal amplitude, the g_m will decrease to the point where it just compensates for the losses in the circuit and the amplitude of the oscillator will stabilize (Figure 18).

Figure 18. I_C vs. V_{BE} curve for a bipolar transistor.

It is the saturation non-linearity that tends to be the “harder” non-linearity, and in most high powered oscillators it will be this effect that will dominate, and reduce the effective g_m the most. This linearity constraint will also put a practical limit on the maximum power that can be obtained from an oscillator. After reaching this limit, increasing the bias current will have very little effect on the output power. Although increasing the current causes the g_m to rise, there is progressively less linear distance from the operating point to where the non-linear region starts.

Looking at the common-base or common-collector Hartley or Colpitts oscillators it can be seen how this effect works on the circuits. In the case of the common base circuit when v_{osc} is at the bottom of its swing v_{ce} tends to be very small causing the base collector junction to be forward biased. This also tends to make v_{be} quite large. These two conditions together cause the transistor to go into saturation. When v_{osc} reaches the top of its swing v_{be} gets very small, and this drives the oscillator into cut-off. A similar argument can be made for the common-collector circuit only it enters cut-off at the bottom of its swing and saturation at the top of its swing.

Figure 19. Oscillator non-linearity illustrated.

Little can be said quantitatively about the large signal amplitude and power produced by an oscillator. As mentioned, increasing the bias current flowing in the tank will increase output power up to a point, beyond which it will have no effect. It is also intuitive to note that as the losses in the resonator are reduced the g_m will have to be further reduced by non-linearity before the oscillator reaches steady state. Thus, we can say that the amplitude of oscillation V_{OSC} is proportional to these two factors at least.

$$V_{OSC} \propto QI_C \quad (28)$$

4.8 Bias Shifting During Start Up

Once the oscillator starts to experience non-linearity then harmonics start to appear. The even ordered harmonics, if present, can cause shifts in bias conditions since they are not symmetric, i.e. they have less negative going swing. Thus they tend to raise the voltage at any node with signal swing on them, and after start up, bias conditions may shift somewhat from what would be predicted by a purely DC analysis.

4.9 Impedance Transformation

Another function of the negative resistance cells of the oscillators is to transform the dynamic emitter resistance to higher value in parallel with the tank. For the common-base and common-collector Hartley and Colpitts oscillators the transformation is carried out by the two passive elements in series. As can be seen in Figure 20 if the T-Model for the transistor is used then for both circuits can be reduced to the case of a resistor in parallel with an imaginary impedance in series with another imaginary impedance. The transformation, using the well-known formula for this network, for the case of the common-base is given by [20]:

$$R_{TankCB} = \left(1 + \frac{Z_1}{Z_2}\right)^2 r_e \quad (29)$$

and in the case of the common-collector is given by:

$$R_{TankCC} = \left(1 + \frac{Z_2}{Z_1}\right)^2 r_e \quad (30)$$

Figure 20. Impedance transformers in the common-base, and common-collector Hartley and Colpitts oscillators.

For the -Gm oscillator, referring back to Figure 15, it is easy to see that in this case, using the T-Model for both transistors gives:

$$R_{\text{Tank-Gm}} = 2r_e \quad (31)$$

This assumes that both transistors are identical.

4.10 Phase Noise in Oscillators

A major challenge in most oscillator designs is meet the phase noise requirements of the system. An ideal oscillator has a frequency response that is a simple impulse at the frequency of oscillation, however real oscillators exhibit “skirts” caused by instantaneous jitter in the phase of the wave form. Noise that causes variations in the phase of the tone (distinct from noise that causes fluctuations in the amplitude of the tone) is referred to as phase noise. The waveform of a real oscillator can be written as:

$$V_{\text{osc}} = A \cos(\omega_o t + \phi_n(t)) \quad (32)$$

where $\phi_n(t)$ is the phase noise of the oscillator. Here amplitude noise is ignored because it is usually of little importance in most system specifications. There are two major sources of phase noise in an oscillator and they will be discussed next.

4.10.1 Noise in the signal path:

In order to derive a formula for phase noise in an oscillator [22] it is necessary to start with the feedback model of an oscillator as shown in Figure 21.

Figure 21. Feedback model of an oscillator used for phase noise modeling.

From control theory, it is known that:

$$\frac{N_{OUT}(s)}{N_{IN}(s)} = \frac{H_1(s)}{1 - H(s)} \quad (33)$$

where $H(s) = H_1(s) H_2(s)$.

$H(s)$ can be written as truncated Taylor series:

$$H(j\omega) \approx H(j\omega_0) + \Delta\omega \frac{dH}{d\omega} \quad (34)$$

Since the conditions of stable oscillation must be satisfied $H(j\omega_0) = 1$. We let $H_1(j\omega_0) = H_1$, where H_1 is a constant determined by circuit parameters.

Now (33) can be re-written using (34) as:

$$\frac{N_{OUT}(s)}{N_{IN}(s)} = \frac{H_1}{-\Delta\omega \frac{dH}{d\omega}} \quad (35)$$

noise power is of interest here so:

$$\left| \frac{N_{OUT}(s)}{N_{IN}(s)} \right|^2 = \frac{|H_1|^2}{(\Delta\omega)^2 \left| \frac{dH}{d\omega} \right|^2} \quad (36)$$

(36) can now be re-written using $H(\omega) = |H| e^{j\phi}$ and the product rule:

$$\frac{dH}{d\omega} = \frac{d|H|}{d\omega} e^{j\phi} + |H| j e^{j\phi} \frac{d\phi}{d\omega} \quad (37)$$

noting that the two terms on the right of (37) are orthogonal:

$$\left| \frac{dH}{d\omega} \right|^2 = \left| \frac{d|H|}{d\omega} \right|^2 + |H|^2 \left| \frac{d\phi}{d\omega} \right|^2 \quad (38)$$

The phase changes at resonance much faster than magnitude, and $|H| \approx 1$ near resonance.

Thus the second term on the right in (38) is dominant, and this equation reduces to:

$$\left| \frac{dH}{d\omega} \right|^2 = \left| \frac{d\phi}{d\omega} \right|^2 \quad (39)$$

now substituting (39) back into (35):

$$\left| \frac{N_{OUT}(s)}{N_{IN}(s)} \right|^2 = \frac{|H_1|^2}{(\Delta\omega)^2 \left| \frac{d\phi}{d\omega} \right|^2} \quad (40)$$

(40) can be re-written again with the help of the definition of Q given in (11):

$$\left| \frac{N_{OUT}(s)}{N_{IN}(s)} \right|^2 = \frac{|H_1|^2 \omega_o^2}{4Q^2 (\Delta\omega)^2} \quad (41)$$

In the special case when the feedback path is unity then $H_1 = H$ and since $|H| = 1$ near resonance (41) reduces to:

$$\left| \frac{N_{OUT}(s)}{N_{IN}(s)} \right|^2 = \frac{\omega_o^2}{4Q^2 (\Delta\omega)^2} \quad (42)$$

Equation (42) forms the noise shaping function for the oscillator. In other words, for a given noise power generated by the transistor amplifier part of the oscillator this equation describes the output noise around the tone.

Phase noise is usually quoted as an absolute noise referenced to the carrier power so (41) should be re-written to give phase noise as:

$$PN = \frac{|N_{OUT}(s)|^2}{2P_s} = \left(\frac{|H_1| \omega_o}{(2Q\Delta\omega)} \right)^2 \left(\frac{|N_{IN}(s)|^2}{2P_s} \right) \quad (43)$$

where P_s is the signal power of the carrier and noting that phase noise is only half the noise present (the other half is amplitude noise and in this approximation AM to PM conversion is ignored). This formula is known as Leeson's equation [23]. The other half is amplitude noise and is of less interest.

The equation can also be re-written to remove the input noise term if the transistor is modeled as a simple amplifier. It is assumed that the amplifier is characterized by its noise factor (F) defined as:

$$F = \frac{N_{TOTAL}}{N_{SOURCE}} \quad (44)$$

where N_{TOTAL} is the total available noise of the amplifier referred to the input, and N_{SOURCE} is the total noise available at the output from the source driving the amplifier. We note also that any resistive source, independent of resistor size $N_{SOURCE} = kT$ where k is Boltzmann's constant and T is the temperature in Kelvin. Now it can be written:

$$|N_{IN}(s)|^2 = FkT \quad (45)$$

Now (43) can be re-written in its final form:

$$PN = \left(\frac{|H_1|_{\omega_o}}{(2Q\Delta\omega)} \right)^2 \left(\frac{FkT}{2P_s} \right) \quad (46)$$

Note that in this derivation it has been assumed that flicker noise is insignificant at the frequencies of interest. This may not always be the case especially in CMOS designs.

It is important to make a few notes here about the interpretation of this formula. Note that in the derivation of this formula that it has been assumed that the noise N_{IN} is injected into the tank. Thus $|H_1|=|H|=1$ at the top of the resonator. However at other points in the loop $|H_1| \neq 1$. For instance in the case of the common-base Colpitts oscillator, when looking at the midpoint between the two capacitors then $|H_1| = C_2/(C_1+C_2)$. A common mistake is to assume that in this circuit the phase noise at this point would be intrinsically worse than at the top of the resonator because the output power is lower by a factor $(C_2/(C_1+C_2))^2$, however the noise is reduced by the same amount leaving the phase noise at the same level at both points in the feedback loop. Note that this is only true up until the thermal noise floor is reached at which point having a stronger signal will influence the phase noise at very large offsets.

4.10.2 Noise in the Control path of a VCO:

So far, the discussion has been of oscillators without a tuning scheme, however most practical designs incorporate some method to change the frequency of the oscillator. These oscillators have a control line where the output frequency is proportional to the voltage on that line:

$$\omega_{osc} = \omega_o + K_{VCO} V_{cont} \quad (47)$$

where K_{VCO} is the gain of the VCO, and V_{cont} is the voltage on the control line. If it is assumed that V_{cont} is a low frequency sine wave of amplitude V_m , and using the narrow band FM approximation, the result is:

$$v_{out}(t) \approx A \cos(\omega_o t) + \frac{A V_m K_{VCO}}{2\Delta\omega} [\cos(\omega_o + \Delta\omega)t - \cos(\omega_o - \Delta\omega)t] \quad (48)$$

where A is the carrier power, and $\Delta\omega$ is the frequency of the controlling signal. Thus if it is assumed that the sine wave is a noise source then the noise power present at $\pm \Delta\omega$ is given by:

$$\text{Noise} = \left(\frac{A V_m K_{VCO}}{2\Delta\omega} \right)^2 \quad (49)$$

If this is converted into phase noise by dividing by the signal power, and if the noise is divided equally into phase and amplitude noise the result is simply:

$$\text{PN} = \frac{1}{2} \left(\frac{V_m K_{VCO}}{2\Delta\omega} \right)^2 \quad (50)$$

Combining (46) and (50) to give the final expression for phase noise completes the discussion of phase noise:

$$\text{PN} = \left(\frac{|H_1| \omega_o}{(2Q\Delta\omega)} \right)^2 \left(\frac{FkT}{2P_s} \right) + \frac{1}{2} \left(\frac{V_m K_{VCO}}{2\Delta\omega} \right)^2 \quad (51)$$

4.11 Some Recent Work On VCO Design

VCO design has been a popular research topic over the last few years. Much work has been done in an effort to better understand their design, and to design circuits with better performance. The following is a summary of some of the work done over the past few years. This is not meant to be a complete list, but rather is meant to give the reader an idea of performance levels typically achieved.

Reference	D.C. Power (mW)	Phase Noise @100 kHz offset	Output Power (dBm)	Frequency (GHz)	Technology
[9]	24	-109 dBc/Hz	Not Reported	1.62-1.8	CMOS
[10]	24	-78 to -87 dBc/Hz	-11.8	10.5-11	SiGe
[11]	54	-92 dBc/Hz	-13.5	2.4	Bipolar
[12]	7.59	-86 dBc/Hz	-24.0	1.66-1.78	CMOS
[13]	40	-105 dBc/Hz	-10.0	1.4-1.54	BiCMOS
[14]	40.5	-105 dBc/Hz	-3.0	0.95-1.1	Bipolar
[14]	43.2	-102 dBc/Hz	-3.0	1.35-1.55	Bipolar
[14]	43.2	-99 dBc/Hz	-3.0	1.95-2.2	Bipolar
[15]	48.6	-102 dBc/Hz	-8.0	1.88-2.03	Bipolar
[16]	33	-86 dBc/Hz	-6.0	1.6-2.0	Bipolar

Table 2. Summary of some recently published VCO specifications.

Reference [9]: This is a -Gm topology. The design uses bond wire inductors which have an extremely high Q. Bond wire inductors are most likely a major reason why this design has such superior noise performance, however this method of implementing inductors has not seen widespread acceptance.

Reference [10]: This is an extremely high frequency oscillator implemented in a high speed SiGe technology. The design is a single ended Colpitts common-emitter topology, which is very unusual for integrated designs. This is one of the few papers that reports a variation in phase noise over the tuning range, however no attempt is made to explain it in the paper.

Reference [11]: This design is a single ended Colpitts common-base topology with emitter follower buffer stage. Although this design has no varactors and therefore no tuning capability, it uses spiral inductors made with three layers of metal which

achieve high Q . This is possible because there are still several microns between the bottom metal and the substrate. This is not usually the case in most technologies.

Reference [12]: This design uses complicated circuitry to linearise the gain of the VCO. Essentially the tuning voltage varies the voltage across the varactors in a non-linear manner so that the C - V_{tune} curve becomes linear.

Reference [13]: This design is a differential Colpitts common collector based oscillator. However, instead of grounding the collector a resistor is placed at that node and the output is taken from there. This provides very good tank isolation, which may have been partially responsible for the good noise performance of this design.

Reference [14]: This design was implemented at three different frequencies. Although from the reference it is hard to determine the exact topology of the oscillator, it obviously shows good performance both in noise and output power.

Reference [15]: This design employs a -Gm topology with transformer coupled feedback, making this an extremely novel design. The paper also boasts an impressively constant gain for the VCO using integrated varactors, but says little about how this was achieved.

Reference [16]: Although this design's performance is not as good as some others, it employs active circuitry to make the varactor characteristic more linear.

4.12 An Example Application for the VCO

An example of an application for the VCO designed in this work could be to use it to form part of a completely integrated receiver like the one presented in [17]. This system, consisting of a completely integrated LNA, mixer, and image reject filter was fabricated in the same technology as the one used for this work. This makes it an ideal candidate to integrate the VCO presented here with this system as the local oscillator reference.

In this chapter, the basic principles of operation of LC oscillators have been reviewed. As well, output power and noise considerations have been discussed. Armed with a good understanding of how these basic circuits work, and how they are affected by noise, the design of differential VCOs will now be undertaken.

Chapter 5: Differential VCO Design

In this chapter, the design of completely integrated differential oscillators will be discussed. Design topology and device sizing will be addressed along with layout considerations.

5.1 Design Goals

The main goal of this design was to minimize the phase noise generated by the VCO. The formula derived in the previous chapter (51) is useful to the designer to identify design trade offs and optimize the circuit for best phase noise performance. The target frequencies for the designs were 1.9GHz, 2.2GHz, and 5GHz. The supply voltage used for these designs was 3.3V. The oscillator will also have to produce sufficient power to adequately drive a Gilbert cell mixer. If the oscillator fails to deliver enough power to the mixer, then the upper quad will not experience complete switching and the mixer noise figure will suffer.

The oscillator was chosen to be differential for a variety of reasons. Differential oscillators can reject common mode noise, they have better power supply noise rejection, are easier to bias on-chip without any ideal grounds available, and are ideal for driving mixers, which usually require a differential input.

5.2 Basic Differential Topologies

The three main oscillators discussed so far can be made into differential circuits. The basic idea is to take two single ended oscillators and place them back to back. Whenever the single ended circuits were previously connected to ground, in the

differential circuit, they are tied together forming an axis of symmetry down the center of the circuit. The basic circuits without biasing are shown in Figure 22.

Figure 22. Basic differential oscillators. Biasing not shown.

5.3 Frequency Tuning

The first task in designing an oscillator is to set the frequency of oscillation, and hence set the value of the total inductance and capacitance in the circuit. To get the unloaded Q as high as possible, as well as increase output swing, it is desirable to make the inductance as large as possible. However, it should be noted that large monolithic

inductors suffer from limited Q . The frequency of oscillation, taking into account transistor parasitics given by:

$$\omega_{osc} \approx \frac{1}{\sqrt{L \left(\frac{C_1 C_2 + C_1 C_\pi}{C_1 + C_2 + C_\pi} + C_\mu \right)}} \quad (52)$$

for the Colpitts oscillators.

$$\omega_{osc} \approx \frac{1}{\sqrt{(C + C_\mu)(L_1 + L_{2eff})}} \quad (53)$$

for the Hartley oscillators, where

$$L_{2eff} = \frac{L_2}{1 - \omega_{osc}^2 C_\pi L_2} \quad (54)$$

and

$$\omega_{osc} \approx \frac{1}{\sqrt{L \left(2C_\mu + \frac{C_\pi}{2} + C \right)}} \quad (55)$$

for the -Gm oscillator. Note that in the case of the -Gm oscillator that the parasitics tend to reduce the frequency of oscillation a bit more than with the Colpitts oscillator.

5.4 Capacitor or Inductor Ratios with Colpitts and Hartley Oscillators

In order to achieve optimal phase noise performance from either of these circuits, the use of capacitors is necessary to transform r_e (the dynamic emitter resistance) to a higher value. This impedance transformation effectively stops this typically low impedance from reducing the Q of the oscillator's LC tank. The impedance transformation is given by:

$$R_{Tank} = 2 \left(1 + \frac{C_2}{C_1} \right)^2 r_e \quad (56)$$

for the Colpitts oscillator, and

$$R_{\text{Tank}} = 2 \left(1 + \frac{L_1}{L_2} \right)^2 r_e \quad (57)$$

for the Hartley oscillator.

Therefore, in order to get the maximum effect of the impedance transformer, it is necessary to make C_2 large and C_1 small in the case of the Colpitts circuit. In the case of the Hartley circuit, it is necessary to make L_1 large and L_2 small. However, if this ratio is made too large then the negative resistance generated by the circuit will not be large enough to compensate for the losses.

The -Gm oscillator is at a disadvantage here because it always presents $2r_e$ to the tank. Thus in high power oscillators that draw a lot of current where this loss may be dominant this circuit will most likely give poorer noise performance.

Since the common-base and common-collector Colpitts and Hartley circuits are so similar, careful simulation is needed to determine which will give better noise performance in a given application. In this work, all experiments were done using the common-base as it showed a marginal phase noise improvement over the common-collector in the technology of interest.

5.5 Sizing of the Transistors

As can be seen from the derivations in the previous chapter one of the sources of phase noise in the circuit is the transistor amplifier. Thus it is desirable to make this device as quiet as possible. There are three major sources of noise in a bipolar transistor; base resistance, collector shot noise, and base shot noise. Since the current controls both base shot noise and collector shot noise, the only one that can be controlled by the size of the device is the base resistance. Since base resistance is inversely proportional to the size on the device, one usually chooses a fairly large transistor. Making the transistor too

large can lead to the parasitics in the device seriously affecting the frequency of oscillation.

5.6 Design and Placement of Varactors

In order for an oscillator to have a voltage controlled frequency there must be an element in that tank that either changes the capacitance or inductance of the tank making the frequency of oscillation change. This function is most commonly done using a diode in reverse bias (commonly referred to as a varactor in this configuration). Placing a tunable reverse bias across a diode causes the length of the depletion region to be lengthened or shortened with the change in reverse bias. This change in length of the depletion region changes the capacitance across the junction. This allows you to build a crude voltage controlled capacitor.

Figure 23. Integrated varactor with parasitic diode.

Diodes in a bipolar process can be realized using either the base-collector or the base-emitter junctions. In the technology used for this work, the most popular option is to make use of the base-collector junction as shown in Figure 23. However, when using this junction there is also a parasitic diode between the collector and the substrate. Unlike the base-collector junction which has a Q greater than 20, this parasitic junction has a low Q due to the low doping of the substrate. This makes it desirable to remove it from the circuit. Placing the varactors in the circuit such that the cathodes are tied together at the

axis of symmetry can do this. Placing two varactors in the oscillators as shown in Figure 24 and Figure 25 effectively ac grounds both sides of the parasitic diodes, and removes them from the differential circuit. Note that of the two, the Hartley oscillator requires a smaller varactor to achieve the same tuning range as the varactor is placed directly in parallel with the tank. However, the Hartley will require a tuning voltage higher than that of the collector voltage, which could lead to some practical problems.

Figure 24. Colpitts common-base with varactor tuning.

Figure 25. Hartley Common-Base with varactor tuning.

5.7 Noise and Linearity in Varactors

When VCO performance is reported, it is typically measured at only one point in the tuning range. However, the phase noise of on-chip designs is not necessarily constant over the tuning range. Unfortunately, on-chip varactors have a highly non-linear C-V curve, and this can make the phase noise over the tuning range very non-uniform. Any noise on the control line can lead to additional phase noise as shown in the previous chapter, and since the varactor is non-linear, K_{VCO} varies over the tuning range. This leads to better than average phase noise at the top of the frequency range (where the varactor is heavily reverse biased) because K_{VCO} is small.

The non-linearity occurs in uniformly doped varactors because as the reverse bias is increased the width of the depletion region changes by a smaller and smaller amount for a given change in voltage. In order to improve the linearity of the varactors the standard base implant can be replaced with a graded doping profile. Thus in the region where it is intrinsically hard to change the depletion width the doping is higher compensating for this effect. The result of using this technique will be a more linear C-V curve, more uniform K_{VCO} , and therefore more uniform phase noise over the tuning range.

To the end of having as little noise as possible on the control line it is also necessary to make R_{Tune} as small as possible without de-coupling to the circuits. Since this resistor is driving an almost perfect open circuit, the noise voltage of this resistor appears at the varactor terminal. The larger the resistor the more noise voltage it places across the varactors causing more phase noise. A better alternative may be to replace the resistor with an inductor here instead.

5.8 Layout of the Varactor

Varactors when used properly can have quite a high Q . However, in order to get the best possible performance from them some care must be taken in their layout. The most important thing is to ensure that the distance the current travels is as short as possible. The further the current has to go the more resistance it encounters and the lower the Q of the device becomes. Thus the best possible design is one with multiple long skinny “fingers” as shown in Figure 26.

Figure 26. Good and bad varactor layouts for best Q performance.

5.9 Biasing of the Circuits

DC currents and voltages must be set for the transistors. As shown in Figure 27 and Figure 28 the base is biased with a simple voltage divider. These resistors were made small enough so that changes in the current flowing into or out of the base would not noticeably affect the bias voltage at this node. However making these resistors too small

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Figure 27. Differential Colpitts common-base with biasing circuitry.

Figure 28. Differential Hartley common-base with biasing.

5.10 Addition of Emitter Degeneration

If sufficient current is driven through the transistors in the circuits depicted in Figure 27 and Figure 28 so that reasonable output power is achieved, the value of r_e is quite small even after it has been transformed to the collector. If steps are not taken, then this resistance will limit the performance of the design. In order to increase the Q of the tank without sacrificing output power, emitter degeneration (R_E) is added to the circuit. This is shown in Figure 29 and Figure 30. Note that after this is done the Q of the tank will most likely be limited by the Q of the inductor. Degeneration will also further increase the linearity of the transistor amplifiers at the cost of adding some additional noise. This allows the signal levels to increase even more before the transistor non-linearity causes saturation although the effective g_m of the transistor is reduced. Care must be taken as the addition of excessive degeneration results in a loop gain of less than one, and oscillations will not start.

5.11 The Addition of Output Buffers

The placement of a 50Ω load either directly across the tank or at the emitter of these circuits would significantly reduce the Q of the circuit. For this reason output buffers with high input impedance have been added to the circuit. They were placed at the emitter instead of at the collector in order to take advantage of the impedance transformation provided by the capacitors since all other things being equal the phase noise should be the same at either point. This buffer also makes the circuit less sensitive to load pull when driving an active load such as the input to a mixer, and gives increased output power. Note that in the case of the common-collector circuit, it is impossible to optimize the capacitor ratio for both the load and r_e . This has led some designers using this circuit to place a resistor at the collector and derive the output from there [10].

Figure 29. Final Colpitts common-base design including output buffers, and biasing.

Figure 30. Final Hartley common-base design with degeneration and output buffers.

Thus the topologies for experimentation have been arrived at, and all components have been sized. At this stage, the only thing left to do was simulate the circuits and then send them for fabrication.

Chapter 6: Results of Experimentation

In this chapter, the results of the various experiments that were run as part of this thesis will be discussed. Many experiments were run to produce low phase noise oscillators and to produce high Q inductors.

6.1 Inductor Experiments Using a Standard Bipolar Process (Al Inductors)

Before the copper process was finished, experiments on VCO design were carried out using standard Al inductors built in the process along with test structures to show the performance of some more exotic structures. All inductors were tested as one port test structures. Measurements were done using the HP 8720A network analyzer. The structures were probed using GGB Industries 40A-GSG-150-P probes, and the network analyzer was calibrated with GGB Industries CS-5 calibration substrate.

Three structures were tested:

- 1) A standard, square 3nH inductor. This inductor had a Q of about 6 at 2 GHz. The results of the measurements done on this inductor are shown Figure 31.
- 2) A 3.5nH octagonal inductor (Figure 32). This inductor was supposed to be a 3nH inductor, but ended up being a little larger than expected. Still it shows improved performance over the square inductor as expected with a Q of about 7 shown in Figure 33.
- 3) A 3nH square inductor with a ground shield (Figure 34). Note that the frequency at which the Q peaks has shifted somewhat due to the presence of additional capacitance from the shield. The self-resonance frequency has also dropped somewhat. However, the Q has increased to a higher value than even the octagonal inductor to have a Q of about 8. Results are shown in Figure 35.

Figure 31. Results for a square 3nH inductor fabricated in the standard bipolar process.

Figure 32. Picture of a 3.5nH octagonal inductor.

Figure 33. Results for a octagonal 3.5nH inductor fabricated in the standard bipolar process.

Figure 34. Picture of a 3nH square inductor with patterned ground shield.

Figure 35. Results for a square 3nH inductor with patterned ground shield fabricated in the standard bipolar process.

6.2 Cu Inductor Testing

To demonstrate the process, a range of experiments was run. Inductors were built as one port test structures on top of blank Si wafers with approximately $3\mu\text{m}$ of oxide on the surface. A typical structure is shown in Figure 36.

Figure 36. Photo micrograph of an inductor test structure.

First, the polyimide thickness was varied for the same thickness of Cu interconnect. Results are shown in Figure 37. Note that the difference in Q is larger at higher frequencies where the effect of the substrate is more important. Thicker polyimide also leads to higher self-resonance frequencies.

Figure 37. Measured inductor L and Q for various thickness of polyimide, and constant Cu thickness of 0.7 μm .

To further demonstrate the advantage of the thicker polyimide a very large inductor was fabricated. This 12 nH structure could not have been made to operate up to 2 GHz using most standard processes because it would have self resonated. It was made using thick polyimide and 2 μm thick copper. A plot of its performance is shown in Figure 38.

Figure 38. A 12nH inductor fabricated over thick polyimide using 2 μ m of Cu.

Figure 39. Simulated inductance and Q for a 3nH inductor using various Cu thickness using ASITIC.

Next, the Cu thickness was varied while the polyimide thickness was held constant. Measured results for inductors fabricated with a Cu thickness from 0.7 μ m up to 3.5 μ m are shown in Figure 40. Simulated results are shown Figure 39 for comparison. Note that making the Cu layer much thicker than 3.5 μ m at frequencies higher than 2 GHz and beyond will have limited effect on performance due to the skin effect. A typical structure made in a standard commercial process and having the same inductance is plotted in Figure 40 for comparison.

Figure 40. Measured inductor L and Q for different Cu thickness.

Note that the measurements do not agree precisely with simulations. The simulator tends to overestimate Q, which is typical for simulation packages. This is due to an underestimation of the magnitude of loss mechanisms probably due to simplifications in the modeling process. The simulations also predict the peak Q at a lower frequency. This may be due to an overestimation of the eddy currents generated by the inductor. Simulators however generally provide accurate trends for the designer with reasonable estimates of performance. Experimentation can then be used to refine designs.

6.3 Oscillator Testing

A range of VCO experiments was performed to characterize performance. All VCOs were tested without packaging using GGB Industries MCW-121-1 and MCW-121-2 eight pin probes. The phase noise of the designs was measured using the HP 4352B VCO/PLL signal analyzer. Output spectrums of the VCOs were observed using the HP 8593E spectrum analyzer. All VCOs built have the schematic shown in Figure 29. Component values can be found in appendix A.

6.3.1 A 1.8 GHz Colpitts common-base VCO with Standard Al Inductors.

Figure 41. Photo micrograph of the VCO.

For the first experiment, a Colpitts common-base topology was chosen as shown in Figure 29 and the circuit was fabricated in Nortel networks NT25 process using standard square on-chip inductors. The inductors were previously discussed in section 6.1.

The layout of the VCO itself is shown in Figure 41. The layout was made as symmetric as possible so that both sides would have the same parasitic capacitance. The inductors were placed apart from the rest of the circuit to insure good performance, and a guard ring of substrate contacts was placed around them.

Calculation of Phase Noise:

From the preceding discussion in section 4.10, it is easy to see how one might go about predicting the phase noise of the VCO. The Q of the oscillator can be calculated, and simulations using SPICE will give accurate predictions of the noise figure of the amplifier and output power of the circuit. V_m can be calculated by summing the noise sources in transistors and resistors present at the terminals of the varactor. Note that this is the noise at f_m modulated to $f_o - f_m$ or $f_o + f_m$. K_{VCO} can be predicted provided a model is available for this device. Such calculations resulted in the predicted values presented in the next section.

The VCO was measured both by wafer probing, and after packaging. It has a tuning range of 90MHz, and a differential output power of -2dBm. This output power is sufficiently high to drive a mixer. Both Q1 and Q2 are biased with 5mA each, and the oscillator was operated from a 3.3volt supply. Phase noise measured for both packaged and unpackaged parts differed by less than 3dB. Plots of frequency vs. tuning voltage and phase noise vs. frequency offset for the packaged VCO are shown in Figure 42 and Figure 43. Note that K_{VCO} decreases from 105MHz/volt down to 5MHz/volt over the tuning range. The phase noise measurements agreed well with values predicted by (6) also shown in Figure 43.

Figure 42. Frequency vs. tuning voltage characteristic.

Figure 43. Phase noise vs. Frequency Offset at 1.8GHz.

A plot of phase noise vs. tuning voltage is shown in Figure 44. This clearly shows that the performance is not uniform over the tuning range. In fact, it varies by as much as 10dB. Calculations using equation (51) also predicted almost the same variation. In addition, in this figure the performance of a VCO with constant K_{VCO} and the same tuning range is predicted. Note that for more than half the tuning range this VCO would

have better phase noise, however the peak performance is reduced. This very clearly demonstrates the effect of the varactor on the phase noise. To further illustrate this point an oscillator was fabricated without varactors. It had a phase noise of -105dBc/Hz at 100kHz offset. A plot of phase noise for this design is shown in Figure 45.

Figure 44. Phase noise at 100kHz offset vs. tuning voltage.

Figure 45. The phase noise of a fixed oscillator.

Phase noise variation over the entire tuning range has been studied. Theoretical calculations and measurements agree very well. A methodology for the design of a completely integrated VCO has been presented. A 1.8GHz VCO was fabricated on a 0.5 μ m bipolar technology with a phase noise of better than -100dBc/Hz at 100kHz offset. In conclusion, the use of linear varactors will lead to more uniform performance levels.

6.3.2 A 1.9 GHz VCO with Improved Performance

In the second submission, the oscillator was redesigned to draw less current, and have a slightly enhanced tuning range. From the first experiment, it is easy to see the importance of low frequency noise. Lowering the current and therefore lowering base shot noise and collector shot noise might help reduce this effect. As well, the resistor in the tuning port was reduced in value. The frequency-tuning characteristic is shown in Figure 46, and the phase noise is shown in Figure 47 and improved phase noise over the tuning band over the previous design is shown in Figure 48.

Figure 46. Frequency vs. tuning voltage characteristic.

Figure 47. Phase noise vs. Frequency Offset at 1.9 GHz.

Figure 48. A comparison of phase noise performance over the tuning range for designs 1 and 2.

6.3.3 A 4.7 GHz Colpitts Common-Base VCO

To push the frequency of oscillation, and to provide an additional point of reference a 4.7GHz VCO was also fabricated using the same topology as the first two

experiments. The nominal phase noise of this design dropped to -94dBc/Hz at 100kHz offset at the top of the tuning range due to increased tuning range and the higher frequency of oscillation. Plots for this oscillator are shown in Figure 49, and Figure 50.

Figure 49. Frequency vs. tuning voltage characteristic.

Figure 50. Phase noise vs. Frequency Offset at 4.7 GHz.

6.4 A Completely Integrated 1.9 GHz Receiver with On-Chip VCO and Filter

Two versions of the VCO were integrated with the completely integrated receiver reported in [17] and shown schematically in Figure 51. For this experiment, the VCO was re-tuned to operate at frequencies around 2.2GHz to accommodate the receiver. In the first version of the receiver the VCO was integrated using standard on-chip inductors, in the second version the VCO had inductors with patterned ground shields. This version of the receiver is shown in Figure 52.

Figure 51. A block level diagram of a superheterodyne receiver with VCO.

Care had to be taken when integrating the VCO with the rest of the circuits. Since the mixer LO input and the VCO output had different bias requirements, a coupling capacitor had to be added in series with VCO output (Figure 53). This capacitor was chosen to be quite large to avoid an unnecessarily high voltage drop across this device. However, making this device large can also lead to coupling of the VCO signal into the substrate through the presence of a parasitic capacitor between the bottom plate of the cap and the substrate. Signal loss was also minimized by adjusting the mixer bias network so as to provide a high input impedance, giving the VCO the luxury of driving an impedance much higher than 50Ω . The entire system is shown in Figure 54.

Figure 52. The completely integrated receiver with VCO using patterned ground shields.

Figure 53. Network used to couple the VCO to the mixer.

Figure 54. Schematic of the entire receiver front-end.

The only component of the receiver that could be tested without packaging was the VCO. It was tested at this stage before the complete system performance was evaluated. The VCO with normal inductors had a phase noise of about -100dBc/Hz at 100kHz offset measured nominally at the top of the tuning range, and an output power of -8.3dBm. The VCO with polyshielded inductors had a phase noise of about -103dBc/Hz at 100kHz offset measured nominally at the top of the tuning range, and an output power of -7.3dBm. This clearly shows that the polyshielded version of the VCO has a higher Q. The output power was slightly reduced because there is a coupling capacitor in series with the load. This capacitor is necessary because the mixer and the VCO output require different bias levels. When the VCO is driving the mixer, this power loss will not be so significant because the mixer has a much higher input resistance than the 50Ω instrument in the lab. The frequency tuning characteristics of the two versions of the VCO are shown in Figure 55. A phase noise plot for the two VCOs is shown in Figure 56.

Figure 55. Frequency vs. tuning voltage characteristic.

Figure 56. Comparison of phase noise of the poly/nonpoly VCOs.

Numerous measurements were also performed on the receivers themselves. Plots of the input matching for the circuit with the ground shielded VCO are shown in Figure 57 and Figure 58. These plots show that the receiver had very good matching with only a small amount of reflection from the input of the LNA. Since S_{11} was better than -10dB

for both versions of the receiver additional improvements in matching would have had little or no effect on the gain. S_{11} was measured using the HP 8720A network analyzer.

Figure 57. Log magnitude plot of the input matching for the receiver.

Figure 58. Smith chart plot of the input matching of the receiver.

The noise figure was measured for both versions of the receiver with the HP 8970B Noise Figure meter. The Noise figure was found to be better for the receiver with

the ground shielded VCO. This version also had better gain. In both cases it is likely due to the stronger LO signal from the VCO.

Table 3 summarizes the figures of merit for the system and compares them against a previous version of the receiver with off-chip VCO producing 0 dBm output power. Note that moving the VCO on-chip did not impact the NF of the receiver, had only a marginal impact on the gain, and helped the LO-IF isolation of the system. The IF output spectrum was measured with the HP 8593E spectrum analyzer. The spectrum for both versions of the receiver are shown in Figure 59 and Figure 60.

From the table, it is easy to see that there are advantages to using ground-shielded inductors for the VCO. The ground shielded VCO had better phase noise, and higher output power which led to better NF for the receiver and higher gain. However it had worse LO to IF isolation. This may have been due to the presence of the ground shield that coupled the LO signal through the ground metal to the other ports. In a redesign of this system the LO leakage may be improved even more if the grounding metal for the VCO and the rest of the circuits are kept separate, and only connected together off-chip. As well the large coupling capacitors between the VCO and the Mixer may have caused the LO signal to leak into the substrate. Future versions of the receiver might use a smaller capacitor to reduce this effect and the substrate could be more firmly grounded around these capacitors.

The current reported in the table does not include the current drawn by the IF output buffers. This current, used in this experiment would however not be necessary in an actual application where the receiver would most likely drive a high impedance.

Figure 59. Differential IF output spectrum for the receiver using only standard inductors.

Figure 60. Differential IF output spectrum for the receiver using polyshielded inductors in the VCO.

	Receiver with Off-Chip VCO	Receiver with VCO	Receiver with shielded VCO
IF Frequency	300MHz	300MHz	300MHz
RF Frequency	1.9GHz	1.9GHz	1.9GHz
VCO Tuning Range	N/a (off chip)	2.09-2.30GHz	2.04-2.24GHz
Notch Tuning	2.34-2.55GHz	2.34-2.55GHz	2.34-2.55GHz
NF @ 1.9GHz	4.5dB	4.8dB	4.5dB
Conversion Gain	28.8dB	24.9dB	25.6dB
VCO Phase Noise	N/a (off chip)	-100dBc/Hz	-103dBc/Hz
S_{11}	-19dB	-10.8dB	-12.5dB
Image Rejection	>65dB	>65dB	>65dB
RF-IF Isolation	32.9 dB	28dB	31dB
LO presence at RF	-61dBm	-61dBm	-58dBm
LO presence at IF	-37.5dBm	-52dBm	-49dBm
Power Supply	3.0 V	3.0 V	3.0 V
DC Current	16.1mA	32.5mA	32.5mA
Package	20TQFP	20TQFP	20TQFP

Table 3. Comparison of Receiver Performance.

6.5 Summary

Thus in this chapter a variety of VCO and inductor experiments have been described. Various techniques for building on-chip inductors have been characterized and reported. VCOs in the 2GHz and 5GHz bands have been built and tested. Finally the VCOs using two different inductors have been integrated with a front-end receiver, and the receiver has been characterized.

Chapter 7: Conclusions

7.1 Summary of Work in this Thesis

In this thesis, a simple post-processing sequence for adding high-Q copper inductors to a conventional silicon integrated circuit has been presented. The inductors have a Q up to three times higher than that available in most standard processes with Al metallization and glass dielectrics. The effect of polyimide as an insulating layer and the effect of low resistance Cu on inductor performance has been studied. High Q inductors will have many advantages for RF circuits. Other techniques for increasing the Q of on-chip inductors without altering the process were also studied. The addition of a patterned ground shield and the use of more circular geometries showed improvement in the performance levels achievable.

Phase noise variation over the entire tuning range in a VCO has been studied. Theoretical calculations and measurements agree very well. A methodology for the design of a completely integrated VCO has been presented. A 1.8GHz VCO was fabricated on a 0.5 μ m bipolar technology with a phase noise of better than -100dBc/Hz at 100kHz offset. It was concluded that the use of linear varactors would lead to more uniform performance levels. This version of the VCO was redesigned to have better phase noise over the entire tuning range and finally had a nominal phase noise of -103dBc/Hz at 100kHz offset. A 4.7GHz VCO was also fabricated in this technology showing that VCOs can run up to at least 1/5 of f_t still having a phase noise of -94dBc/Hz at 100kHz offset.

A completely monolithic front-end receiver has been presented. The receiver has an on-chip image reject filter and a VCO. Two versions of the VCO were integrated with the receiver. One VCO used standard square on-chip inductors while the other used inductors with ground shields. The use of ground shields reduced the phase noise of the

VCO by 3dB. This version of the receiver has 25.6dB of conversion gain and a NF of 4.5 dB.

7.2 Summary of Thesis Contributions

1. A process for developing high Q on-chip inductors has been developed. 3nH inductors with a Q as high as 17 at 2GHz have been fabricated on test wafers.
2. A 2GHz VCO using standard on-chip inductors has been fabricated with a phase noise of -103dBc/Hz at 100kHz offset.
3. A 5GHz VCO using standard on-chip inductors has been fabricated with a phase noise of -94dBc/Hz at 100kHz offset.
4. The effect of varactor non-linearity on the phase noise over the tuning range was explored and equations to describe this effect were developed.
5. Some versions of the VCO used novel ground-shielded inductors showing that the Q of the inductors has a direct impact on the phase noise of the design. This VCO, when integrated with an on-chip LNA, mixer, and image reject filter showed that not only could a VCO be integrated with a receiver, but that it had almost no negative impacts on the receiver performance if the ground- shielded inductors were used.

7.3 Future Work

There is much work left to do in this area that has not been completed due to lack of time. A brief list of what could be done follows:

- 1) A comparison of Hartley and Colpitts based oscillators phase noise. It is the conjecture of the author that the Hartley may have some advantages over Colpitts oscillators. Although they have some very practical implementation problems such as de-coupling capacitors, this may not be quite such a problem as frequencies increase.

- 2) Some work has been done here to explore the maximum frequency an oscillator can be made to function at in a given technology. It would be interesting to see these designs move to much higher frequencies using advanced SiGe technologies.
- 3) At higher frequencies, it might be interesting to compare a straight oscillator to one that has a doubler at the output. For example, a 10GHz oscillator mixed up to 20GHz as compared to a straight 20GHz design to see if one had any performance advantage over the other.
- 4) All work done in this thesis was done using free running VCOs. It would be interesting to try to integrate a complete phase-locked loop on-chip.
- 5) Due to time limitations a VCO using Cu inductors was never finished. It is hoped in the future one can be fabricated and its performance compared to the performance of existing designs.
- 6) The Cu process developed in the course of this thesis has many other possible applications then simply inductors. For example, it could be used to build on-chip transformers and transmission lines.
- 7) Cu has a much higher current carrying capacity then Al. This aspect of the Cu process should be explored and characterized. It may have advantages to power amplifier designers, allowing them to achieve a higher level of integration for their circuits.

7.4 Summary of Publications and Awards

The following is a summary of contributions and awards held by the author as a result of this research:

- 1) Industrial Collaboration Award at MRD-CAN 1998.
- 2) Best Paper Award at the 1999 Micronet Annual Workshop for paper: "Cu Inductors for RF Applications: A Post-Processing Approach"

- 3) Presented a Paper at the 1999 Micronet Annual Workshop entitled: "Design of Integrated VCOs"
- 4) Received the GRIP award for the presentation entitled: "VCOs and High Q Copper Inductors"
- 5) Presented a paper at IITC 1999 entitled: "A High Q On-Chip Inductor Process for Si Integrated Circuits"
- 6) A Second paper is to be presented at BCTM 1999 entitled: "The Effect of Varactor Non-Linearity on the Phase Noise of a Completely Integrated 1.8GHz VCO"
- 7) A third paper is being drafted and has a current working title: "A Completely Integrated 1.9 GHz Receiver With On-Chip VCO and Image Reject Filter"

References

- [1] S.P. Voinigescu, M.C. Maliepaard, J.L. Showell, G.E. Babcock, D. Marchesan, M. Schroter, P. Schvan, and D.L. Hareme, "A scalable high frequency noise model for bipolar transistors with application to optimal transistor sizing for low-noise amplifier design," *IEEE J. Solid-State Circuits*, Vol. 32, pp. 1430-1439, Sept. 1997.
- [2] Daniel C. Edelstein and Joachim N. Burghartz, "Spiral and solenoidal inductor structures on silicon using Cu-damascene interconnects," *International Interconnect Technology Conference*, pp. 18-20, 1998.
- [3] T. Smy, L. Tan, S.K. Dew, M.J. Brett, Y. Shacham-Diamond, and M. Desilva, "Simulation of electroless deposition of Cu thin films for very large scale integration metallization," *Journal of the Electrochemical Society*, vol. 144, No. 6, pp. 2115-2122, June 1997.
- [4] J. R. Long and M. A. Copeland, "The modeling, characterization, and design of monolithic inductors for silicon RF IC's," *IEEE J. Solid-State Circuits*, vol. 32, pp. 357-369, Mar. 1997.
- [5] A. M. Niknejad and R. G. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1470-1481, Oct. 1998.
- [6] A. L. L. Pun, T. Yeung, J. Lau, F. J. R. Clément, and D. K. Su, "Substrate noise coupling through planar spiral inductor," *IEEE J. Solid-State Circuits*, vol. 33, pp. 877-884, June 1998.
- [7] M. Danesh, J.R. Long, R.A. Hadaway, and D.L. Hareme, "A Q-Factor Enhancement Technique for MMIC Inductors," 1998 IEEE Radio Frequency Integrated Circuits Symposium, pp. 217-200.
- [8] D. Hisamoto, S. Tanaka, T. Tanimoto, and S. Kimura, "Suspended SOI structure for advanced 0.1- μm CMOS RF devises," *IEEE Transactions on Electron Devices*, vol. 45, pp. 1039-1046, May 1998.
- [9] Jan Craninckx, and Michel S. J. Steyaert, "A 1.8-GHz CMOS Low-Phase-Noise Voltage-Controlled Oscillator with Prescaler," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1474-1482, Dec. 1995.

- [10] Mehmet Soyuer, Joachim N. Burghartz, Herschel A. Ainspan, Keith A. Jenkins, Peter Xiao, Arvin R. Shahani, Margaret S. Dolan, and David L. Harnage, "An 11-GHz 3-V SiGe Voltage Controlled Oscillator with Integrated Resonator," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1451-1454, Dec. 1997.
- [11] Mehmet Soyuer, Keith A. Jenkins, Joachim N. Burghartz, Herschel A. Ainspan, Frank J. Canora, Saila Ponnappalli, John F. Ewen, and William E. Pence, "A 2.4-GHz Silicon Bipolar Oscillator with Integrated Resonator," *IEEE J. Solid-State Circuits*, vol. 31, pp. 268-270, Feb. 1996.
- [12] B. Razavi, "A 1.8GHz CMOS Voltage-Controlled Oscillator," ISSCC97, pp. 388-389.
- [13] L. Dauphinne, M. Copeland, and P. Schvan, "A Balanced 1.5GHz Voltage Controlled Oscillator with an Integrated LC Resonator," ISSCC97, pp. 390-391.
- [14] B. Jansen, K. Negus, and D. Lee, "Silicon Bipolar VCO Family for 1.1 to 2.2GHz with Fully-Integrated Tank and Tuning Circuits," ISSCC97, pp. 392-393.
- [15] M. Zannoth, B. Kolb, J. Fenk, and R. Weigel, "A Fully Integrated VCO at 2 GHz," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1987-1991, Dec. 1998.
- [16] Wei-Zen Chen, and Jieh-Tsong Wu, "A 2-V 2-GHz BJT Variable Frequency Oscillator," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1406-1410, Sept. 1998.
- [17] J. Macedo, M.A. Copeland, "A 1.9 GHz Silicon Receiver with Monolithic Image Filtering," *IEEE J. Solid-State Circuits*, vol. 33, pp. 378-386, March 1998.
- [18] M. Sadiku, *Elements of Electromagnetics*, Saunders College Publishing 1994.
- [19] C.P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for si-based RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, pp. 743-752, May. 1998.
- [20] Behzad Razavi, *RF Microelectronics*, 1998 Prentice Hall.
- [21] Jack Smith, *Modern Communications Circuits*, 1986 McGraw-Hill.
- [22] B. Razavi, "A Study of Phase Noise in CMOS Oscillators," *IEEE J. Solid-State Circuits*, vol. 31, pp. 331-343, March 1996.

- [23] D.B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proceedings of the IEEE*, Feb. 1966, pp.329-330.

Appendix A

This appendix will give component values for all the oscillators built in this thesis. Values in the tables refer to the following diagram which is the oscillator as it appears in Figure 29.

Figure 29. Final Colpitts common-base design including output buffers, and biasing.

Circuit Element	Value
L	3nH
Q1	20 μ m X 0.5 μ m emitter size
Q2	20 μ m X 0.5 μ m emitter size
Q3	20 μ m X 0.5 μ m emitter size
Q4	20 μ m X 0.5 μ m emitter size
C ₁	4pF
C ₂ /2	1.8pF
C _{var}	1.6-3.5pF
R _{cp}	20 Ω
R _E	20 Ω
R _{tune}	4K Ω
R _{B1}	1K Ω
R _{B2}	2.5K Ω
I ₁	5.3mA
I ₂	5.3mA
I ₃	3.8mA
I ₄	3.8mA

Table 4. Circuit element values for the 1.8GHz oscillator in experiment 1.

Circuit Element	Value
L	3nH
Q1	20 μ m X 0.5 μ m emitter size
Q2	20 μ m X 0.5 μ m emitter size
Q3	20 μ m X 0.5 μ m emitter size
Q4	20 μ m X 0.5 μ m emitter size
C ₁	3.5pF
C ₂ /2	1.4pF
C _{var}	1.6-3.5pF
R _{cp}	20 Ω
R _E	20 Ω
R _{tune}	50 Ω
R _{B1}	1K Ω
R _{B2}	2.5K Ω
I ₁	3.2mA
I ₂	3.2mA
I ₃	2.9mA
I ₄	2.9mA

Table 5. Circuit element values for the 1.9GHz oscillator in experiment 2.

Circuit Element	Value
L	1nH
Q1	20 μ m X 0.5 μ m emitter size
Q2	20 μ m X 0.5 μ m emitter size
Q3	20 μ m X 0.5 μ m emitter size
Q4	20 μ m X 0.5 μ m emitter size
C ₁	1pF
C ₂ /2	0pF
C _{var}	0.9-1.6pF
R _{cp}	20 Ω
R _E	20 Ω
R _{tunc}	50 Ω
R _{B1}	1K Ω
R _{B2}	2.5K Ω
I ₁	5.3mA
I ₂	5.3mA
I ₃	3.8mA
I ₄	3.8mA

Table 6. Circuit element values for the 4.7GHz oscillator in experiment 3.

Circuit Element	Value
L	3nH
Q1	20 μ m X 0.5 μ m emitter size
Q2	20 μ m X 0.5 μ m emitter size
Q3	20 μ m X 0.5 μ m emitter size
Q4	20 μ m X 0.5 μ m emitter size
C ₁	2.4pF
C ₂ /2	0pF
C _{var}	1.6-3.5pF
R _{cp}	20 Ω
R _E	20 Ω
R _{tunc}	50 Ω
R _{B1}	1K Ω
R _{B2}	2.5K Ω
I ₁	3.2mA
I ₂	3.2mA
I ₃	2.9mA
I ₄	2.9mA

Table 7. Circuit element values for the oscillator in the receiver.