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**Investigation of GaAs pHEMT Distributed Amplification
for Broadband Modulator Driver Applications**

by

Qing Xia

A thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfillment of the requirements
for the degree of
Master of Applied Science

Ottawa - Carleton Institute for Electrical Engineering
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Abstract

This thesis investigates GaAs monolithic microwave integrated circuit (MMIC) broadband amplification for potential use in optical modulator driver applications. Two types of distributed amplifiers (DA) are designed and evaluated: one having a conventional topology with cascode gain cells and the other having a matrix topology with common source gain cells. A number of design techniques are utilized in the amplifiers to obtain a high and flat gain as well as a wide bandwidth. These include frequency dependent terminations for the artificial transmission lines, loss compensation by adjusting the negative resistance of the gain cell, and series feedback of the transistors using inductive elements.

A 0.5 - 53 GHz, 5 stage, cascode distributed amplifier based on 0.2 μm GaAs pHEMT technology is designed, fabricated and measured, while a 0.5 - 41 GHz, 2 x 5 stage, matrix distributed amplifier based on the same process is designed and fabricated. Experimental and simulated results are found to be in close agreement.

It is concluded that the conventional topology cascode DA design can provide maximum bandwidth but with limited output voltage swing, whereas the matrix DA topology has the capability of producing larger output voltage swings.

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Contents

Chapter 1. Introduction.....	1
1.1 Motivation.....	1
1.2 Objectives	2
1.3 Thesis Organization	3
 Chapter 2. Overview of GaAs HEMT Technology and Wideband Amplification	4
2.1 Introduction	4
2.2 Overview of AlGaAs/GaAs HEMTs	4
2.2.1 GaAs/AlGaAs HEMT Structure	4
2.2.2 HEMTs Operation	6
2.2.3 AlGaAs/InGaAs/GaAs Pseudomorphemic HEMTs	7
2.3 Comparison of HEMT and Other High Speed Devices	8
2.3.1 Comparison of f_t and f_{max} for Various Transistor Technologies.....	8
2.3.2 Noise Performance	10
2.3.3 Power Performance.....	12
2.4 Philips OMMIC ED02AH Process	13
2.5 Wideband Amplifier Topologies	16
2.5.1 Reactively Matched, Lossy Matched and Feedback Amplifiers	16
2.5.2 Distributed Amplifier	17
2.6 Overview of Distributed Amplification.....	18
 Chapter 3 Distributed Amplifier Theory	22
3.1 Introduction	22
3.2 Image Parameter Method	22
3.2.1 Introduction	22

3.2.2 General Networks	22
3.2.3 L-Section	25
3.2.4 T-Section	26
3.2.5 π -Section	27
3.3 Distributed Amplifier Theory	29
3.3.1 Introduction	29
3.3.2 Artificial Transmission Line for DA	30
3.3.3 Distributed Amplifier Gain	36
3.3.4 Image Impedance Matching	41
3.4 Cascode Distributed Amplifier	42
3.5 Matrix Distributed Amplifier	47
3.6 Conclusion	48
Chapter 4 Distributed Amplifier Design	49
4.1 Introduction	49
4.2 Design of A Cascode Distributed Amplifier	50
4.2.1 Cascode DA Design Objectives	50
4.2.2 Active Device Choice	51
4.2.3 Lumped Element Design of A Cascode DA	54
4.2.4 Microstrip Design for A Cascode Distributed Amplifier	57
4.2.5 Bias and Terminal Matching Circuitry	61
4.2.6 Circuit Optimization	61
4.2.7 MMIC Implementation	68
4.3 Design of A Matrix Distributed Amplifier	73
4.3.1 Matrix DA Design Objectives	73
4.3.2 Active Device Choice	73
4.3.3 Lumped Element Design for A Matrix DA	76
4.3.4 Coplanar Waveguide Design for A Matrix Distributed Amplifier	79
4.3.5 Bias and Terminal Matching Circuitry	80
4.3.6 Circuit Optimization	82

4.3.7 MMIC Implementation	84
4.4 Evaluation of Cascode and Matrix Distributed Amplifiers	86
Chapter 5. Experimental Results.....	88
5.1 Introduction.....	88
5.2 Measurement Setup	88
5.2.1 S-parameter Measurement Setup	88
5.2.2 Output power Measurement Setup	89
5.3 Distributed Amplifier Measurements	90
5.3.1 S-Parameters of the Distributed Amplifier	91
5.3.2 Explanation of Measurement Results	94
5.3.3 Frequency Response Effects Due to Bias	95
5.3.4 Group Delay	96
5.3.5 1-dB Gain Compression.....	97
5.3.6 Output Voltage Swing	99
5.3.7 Comparison with other Amplifier in the literature	99
Chapter 6. Conclusions and Future Work.....	101
6.1 Summary	101
6.2 Future Work	102
References	104
Appendix 1	109

List of Tables

Table 2.1. Comparison of f_t and $f_{\max}$ for various transistor technologies.	9
Table 2.2. Comparison of noise performance of various transistor technologies.	11
Table 2.3. Comparison of various broadband amplifier technologies.	17
Table 4.1: Performance of the cascode and matrix distributed amplifiers.	87
Table 5.1. Performance of reported amplifier based on 0.2 μm GaAs FET.	99

List of Figures

Figure 1.1: Fiber optic transmitter system.	1
Figure 2.1: Conventional HEMT structure.	4
Figure 2.2: Electron velocity versus electric field characteristics for various semiconductors.	9
Figure 2.3: Cross section of ED02AH pHEMT.	14
Figure 2.4: pHEMT small signal equivalent circuit.	15
Figure 2.5 The diagram of a 5 - Section distributed amplifier.	19
Figure 2.6: The circuit diagram of a 5 - section cascode distributed amplifier.	20
Figure 2.7: The circuit diagram of a 2 x 5 matrix distributed amplifier.	21
Figure 3.1: 2 - port Network with Image Impedance.	24
Figure 3.2: Lossless cascade of T - sections forming artificial transmission line.	28
Figure 3.3: The plot of the image impedance, α and β vs. ω for lossless artificial transmission line.	29
Figure 3.4: Equivalent model of a lossy and unilateral pHEMT	32
Figure 3.5: Equivalent model of a distributed amplifier including lossy pHEMT model	32
Figure 3.6: [a] Attenuation on gate line versus normalized frequency.	35
Figure 3.6: [b] Attenuation on drain line versus normalized frequency.	35
Figure 3.7: The plot of the real part of the terminal impedance vs. frequency.	43
Figure 3.8: The equivalent circuit of one cascode cell	45
Figure 4.1: DC I-V curves for 4x15 μm pHEMT device.	52
Figure 4.2: The schematic diagram of one pHEMT cascode cell.	53
Figure 4.3: C_{in} and C_{out} of a cascode cell in Figure 4.2.	53
Figure 4.4: Schematic diagram of a conventional distributed amplifier.	55
Figure 4.5: S-parameters for cascode DA circuit using lumped elements.	56
Figure 4.6: A short length of microstrip line and its equivalent circuit.	57
Figure 4.7: The schematic diagram of the cascode distributed amplifier.	60
Figure 4.8: The equivalent circuit of one cascode cell with	

L_{gate} , C_{gate} , R_{gate} , L_{sd} and L_s	62
Figure 4.9: Effect of the inserted L_{gate} , R_{gate} , C_{gate} , L_{sd} , L_s and L_{dd}	66
Figure 4.10: MMIC layout of the cascode DA.	68
Figure 4.11: Layout of a 60 μm wide pHEMT.....	69
Figure 4.12: Simulated S-parameters of the cascode distributed amplifier.	72
Figure 4.13: Schematic diagram of the matrix distributed amplifier by lumped elements.	74
Figure 4.14: Small signal equivalent circuit of the matrix distributed amplifier.	77
Figure 4.15: Simulation results of the matrix distributed amplifier.	78
Figure 4.16: Schematic diagram of the matrix distributed amplifier.....	81
Figure 4.17: Simulated gain profile with and without L_s (length = 10 μm).	83
Figure 4.18: MMIC layout of the 2 x 5 matrix DA.	84
Figure 4.19: Simulated S-parameters of matrix distributed amplifier.	85
Figure 5.1: Test setup for S-parameters measurement.	88
Figure 5.2: Power measurement setup.	89
Figure 5.3: Microphotograph of the cascode distributed amplifier (2.1 mm x 1.0 mm)	90
Figure 5.4: Frequency characteristics of the distributed amplifier on-chip measurement.	91
Figure 5.5: Comparison between simulated and measured S_{21} of the cascode distributed amplifier at $V_d = 3$ V and $V_g = -0.2$ V.	91
Figure 5.6: Comparison between simulated and measured S_{11} of the cascode distributed amplifier at $V_d = 3$ V and $V_g = -0.2$ V.	92
Figure 5.7: Comparison between simulated and measured S_{22} of the cascode distributed amplifier at $V_d = 3$ V and $V_g = -0.2$ V.....	92
Figure 5.8: Measured $ S_{21} $ for various values of gate bias V_g for cascode distributed amplifier at $V_d = 3$ V.	94
Figure 5.9: Measured $ S_{21} $ for various values of drain bias V_d for cascode distributed amplifier at $V_g = -0.2$ V.	95
Figure 5.10: Calculated group delay as a function of frequency from measured S-parameter of the cascode DA at $V_d = 3$ V and $V_g = -0.2$ V.....	96

Figure 5.11: Measured power performance of the cascode DA at 20 GHz for $V_g=-0.2$ V and $V_d=3$ V.	97
Figure 5.12: Measured 1-dB gain compression point for cascode DA at 10 GHz, 20GHz, 30GHz and 40 GHz.	97

Chapter 1. Introduction

1.1 Motivation

In recent years, wavelength division multiplexing (WDM) and time-division multiplexing (TDM) techniques have been developed to realize high-speed optical networks. 10 Gb/s and 40 Gb/s systems have been widely used in the commercial field. The next generation of optical networks operating above 40 Gb/s are in the research and development phase. A simplified structure of an optical transmitter system is shown in Figure 1.1.

Figure 1.1: Fiber optic transmitter system.

The optical transmitter system usually comprises a laser diode combined with an external electro-optic (EO) modulator. A modulator driver is located at the front-end of the optical transmitter system, whose role is to amplify the output signal of the multiplexer to a higher output voltage, thereby driving the electro-optic modulator. Then, the EO modulator imparts the electrical signal to the light in the form of amplitude modulation. As opti-

cal system speeds increase, a high performance driver is required. This driver must have high flat gain, large output voltage and wide operating bandwidth. Hence, high-speed integrated circuit technology such as monolithic microwave integrated circuit (MMIC) technology can be used to meet this practical application. The aim of this thesis is the design of MMIC distributed amplifiers for potential use as modulator drivers in next-generation optical systems.

1.2 Objectives

An electro-optic modulator with a travelling wave Mach-Zehnder configuration has previously been designed for an optical transmitter system above 40 Gb/s [1]. A large voltage swing must be applied to the modulator in order to achieve acceptable extinction ratios. Therefore, the overall objective of this work is to design, manufacture and measure driver amplifiers in GaAs MMIC technology that combine high output voltage with large bandwidths, as required for next generation optical system. The specific thesis objectives in pursuit of this goal are as follows:

- (a) To design two types of driver amplifiers. One is a conventional topology, cascode gain cell, distributed amplifier configuration based on microstrip technology. Another is a common source gain cell, matrix distributed amplifier configuration based on coplanar waveguide (CPW) technology.
- (b) To optimize and predict the performance-improving mechanisms applicable to each type with the aid of theoretical analysis and CAD tools.
- (c) To evaluate the performances of both types of distributed amplifier (DA) topologies, cascode and matrix DA, in the context of optical modulator driver applications.

1.3 Thesis Organization

This thesis comprises six chapters. Chapter 2 briefly overviews the selected device technology and the principles of distributed amplification. First, the operation of the GaAs HEMT is described and, in order to better understand some of its advantages and disadvantages, performance comparisons of HEMTs to other type microwave transistors are given. Then, basic distributed amplifier theory and topologies are reviewed in this chapter. In Chapter 3, a detailed theoretical analysis is presented that includes the derivation of formulas for the pHEMT-based distributed amplifier. In Chapter 4, a detailed description of the design of the two DAs is given. The layout process and MMIC implementation steps are also discussed in this chapter. In Chapter 5, the measurement apparatus is described along with the experimental performance of the cascode DA. A discussion of the discrepancies between predicted and measured results is presented. Then, the circuit performance of the two different types of distributed amplifier topology is evaluated. Finally, in chapter 6, conclusions are drawn as well as suggestions made for further work.

Chapter 2. Overview of GaAs HEMT Technology and Wideband Amplification

2.1 Introduction

Gallium Arsenide (GaAs) based high electron mobility transistors (HEMTs) are now in widespread use for both low-noise and power amplification. In this chapter, a brief introduction is given to GaAs/AlGaAs HEMTs and MMIC technology. In order to further assess the strengths and limitations of GaAs/AlGaAs HEMTs, a comparison with other traditional microwave transistor technologies is provided. Finally, the Philips ED02AH MMIC process is summarized and wideband amplifier topologies are described.

2.2 Overview of AlGaAs/GaAs HEMTs

2.2.1 GaAs/AlGaAs HEMT Structure

High electron mobility transistors are a field effect device. The cross-section of a HEMT with a selectively doped GaAs-AlGaAs heterojunction structure is shown in Figure 2.1[2].

Figure 2.1: Conventional HEMT structure [2]

In the HEMT, an undoped GaAs layer and an n-doped AlGaAs layer are grown on a semi-insulating GaAs substrate by using molecular-beam epitaxy (MBE) or metalorganic vapor phase epitaxy (MOVPE) technology. The electrons contributed from the n-doped AlGaAs are free to move through the entire crystal until they fall into the lowest energy status allowed them. In the HEMT, the lowest energy states are in the GaAs side of the heterojunction interface. All of the electrons are accumulated in a thin sheet. They are free to move only in the two-dimensional plane of the interface and form a two-dimensional electron gas (2DEG). The undoped AlGaAs spacer layer is introduced to improve the electron mobilities by separating dopant ions from the electron accumulation layer. The density of electrons in the 2DEG is controlled by the voltage on the gate. More positive voltage on the gate increases the electron density and therefore the channel current. When the gate voltage is set to zero, the electron density in the 2DEG can be made zero or nonzero depending on the thickness of the AlGaAs layer, thus resulting respectively in either enhancement mode or depletion mode devices. At room temperature, the low-field mobility of a GaAs HEMT is typically $8,000 \text{ cm}^2/\text{V sec}$ compared to $5,000 \text{ cm}^2/\text{V sec}$ for a GaAs MESFET. Therefore, HEMTs have higher frequency and gain characteristics compared to conventional MESFET. Furthermore, the electron mobility is increased dramatically as temperature is decreased. Hence, HEMTs are sometimes operated at cryogenic temperature for low-noise applications.

A Schottky gate makes contact to the AlGaAs layer. The drain and source ohmic contacts to the HEMT are made via a doped GaAs layer, which is grown on the AlGaAs layer. This structure offers a low parasitic contact resistance.

2.2.2 HEMTs Operation

The I-V characteristic of a HEMT, similarly to that of a GaAs MESFET, has linear and saturated regions. The knee voltage for HEMT saturation appears at lower values of drain-source bias in a HEMT, due to the higher electron mobility. This also decreases the HEMT access resistances as defined on page 15, improving the extrinsic transconductance. In addition, the drain to source current of HEMTs is increased as the gate to source voltage increases. An equation of the transconductance for a HEMT is provided by I. D. Robertson [2].

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{\epsilon_0 \epsilon_r v_{eff}}{h} W \quad (2.1)$$

where $\epsilon_0 \epsilon_r$ is the effective permittivity of AlGaAs donor and spacer layers.

v_{eff} is the effective carrier velocity.

h is the 2DEG to gate separation distance.

W is the device width.

The transconductance of a HEMT depends on the gate-channel separation, effective carrier velocity and the device width. It should be noted that a large device has increased transconductance, but a correspondingly increased gate to source capacitance, thus resulting in no change to the cutoff frequency of the device.

There are two principal figures of merit for the high frequency operation of transistors. The current gain cutoff frequency f_t and the maximum frequency of oscillation f_{max} . The cutoff frequency is defined as the frequency at which the small signal current gain of the transistor falls to unity. On the other hand, the maximum frequency of oscillation is the

frequency at which the unilateral power gain of the transistor becomes unity. The cutoff and maximum oscillation frequency can be expressed as follows [2], in terms of the equivalent circuit elements given on page 15.

$$f_t = \frac{g_m}{2\pi \left[(C_{gs} + C_{gd}) \left(1 + \frac{R_s + R_d}{R_{ds}} \right) + g_m C_{gd} (R_s + R_d) \right]} \quad (2.2)$$

and

$$f_{max} = \frac{f_t}{2 \left(\frac{R_g + R_i + R_s}{R_{ds}} + 2\pi f_t R_g C_{gd} \right)^{1/2}} \quad (2.3)$$

To obtain a high cutoff frequency f_t , a large transconductance as well as low gate capacitance and parasitic resistance are required. Therefore, the transistors should have high effective velocity in the channel, short gate length and low parasitic resistance. Similarly, a large maximum oscillation frequency f_{max} may be obtained by having a high cutoff frequency as well as low gate resistance. Two methods can be utilized to reduce the gate resistance. One uses Tee or mushroom gate structures, which have a small footprint for short gate length but also a large cross-sectional area for small gate resistance. Another method employs multiple gate fingers to reduce the gate resistance.

2.2.3 AlGaAs/InGaAs/GaAs Pseudomorphic HEMTs

A pseudomorphic HEMT (pHEMT) of AlGaAs/InGaAs grown on GaAs has been developed to use InGaAs as the 2DEG channel material instead of GaAs. The principle advantage of the pHEMT is that it has enhanced electron transport in InGaAs compared to GaAs, and improved confinement of carriers in the channel. In addition, the conduction

band discontinuity at the AlGaAs/InGaAs heterojunction is larger than AlGaAs/GaAs case. As a result, the GaAs pHEMT has a higher sheet charge density, higher current density and transconductance. Hence, the pHEMT has a high power gain and large gain-bandwidth product, as required for broadband applications.

2.3 Comparison of HEMT and Other High Speed Devices

Microwave transistors may be characterized by using several different figures of merit. These figures of merit include the current gain cutoff frequency f_t and maximum frequency of oscillation f_{max} , minimum noise figure and the RF output power. The following sections compare these characteristics for various transistor technologies.

2.3.1 Comparison of f_t and f_{max} for Various Transistor Technologies

A summary of the f_t and f_{max} for the various transistors technology is given in Table 2.1. It is clear that III-V devices outperform silicon technologies in high frequency operation, since GaAs material has high low-field electron mobility ($8,000 \text{ cm}^2/\text{Vs}$), which is approximately six times larger than that found in Si. In contrast, wide bandgap semiconductors (SiC and GaN) have relatively low electron mobility, which is around $200\text{-}500 \text{ cm}^2/\text{Vs}$. However, it has very high saturation velocity, typically about $2 \times 10^7 \text{ cm/s}$, which is two times higher than Si (approximately $1 \times 10^7 \text{ cm/s}$) and four higher than for GaAs (approximately $0.5 \times 10^7 \text{ cm/s}$). The electron drift velocity as a function of electric field for GaAs, Si, GaN and SiC is shown in Figure 2.2.

Table 2.1. Comparison of f_t and f_{max} for various transistor technologies

Technology	Feature Size μm	f_t GHz	f_{max} GHz	Ref.
Si bipolar	0.5	50	50	[2]
SiGe HBT	0.12	207	285	[3]
GaAs HBT	1.0	180	280	[2]
InP HBT	1.0	228	270	[2]
GaAs MESFET	0.12	121	160	[4]
GaAs pHEMT	0.1	120	290	[5]
InP HEMT	0.1	160	600	[6]
SiC MESFET	0.5	13.2	42	[7]
GaN HEMT	0.12	110	155	[7]

Figure 2.2: Electron velocity versus electric field characteristics for various semiconductors [7].

Both FET and bipolar devices based on high mobility and velocity materials (e.g. GaAs) may have small gate capacitance, low parasitic resistance and capacitance, and result in higher operating frequency. The GaAs based HEMT and heterojunction bipolar transistor (HBT) process in Table 2.1 offer nearly the highest frequency of operation. Although InP HEMTs show the highest operating frequencies of the various transistors, it still awaits wide commercialization. The main reasons are the low degree of maturity of InP technology and the InP substrates, which are expensive and available only in small diameters.

The heterojunction technology discussed before improves electron mobility, thus increases operating frequency. Hence, the f_t and f_{max} of HEMTs are higher than those of MESFETs. The AlGaIn/GaN based heterojunction device also obtain superior f_t and f_{max} . The SiGe HBT is an improvement of the Si advanced bipolar process. Experimental devices showing f_t and f_{max} of 207 GHz and 285 GHz, respectively, have been reported [3].

2.3.2 Noise Performance

At low frequency, the noise is dominated by trapping effects in the bulk material, at junction interfaces and at the surface of the substrate. These effects combine to give a $1/f$ relation to the noise power spectral density. As the bipolar device is a vertical structure, the current flow in the device is through active junctions which are well shielded from surface and substrate interface. Hence, the $1/f$ noise corner frequency of bipolar devices is at relatively low frequency. In contrast, with FETs, the current flows between surface and gate channel substrate interfaces, which have greater trapping effects and produce larger

1/f noise [8]. A comparison of the noise performance of devices is shown in Table 2.2. The 1/f noise corner frequency of bipolar devices is less than 1 kHz, while that of FETs is approximately 10,000 times higher. Therefore, the low 1/f noise of the bipolar makes it attractive for low phase noise microwave oscillators and mixers.

Table 2.2. Comparison of noise performance of various transistor technologies [2].

Technology	1/f corner frequency	Minimum noise figure	Associated gain
Si bipolar	<1 KHz	1.5 dB@2 GHz	21 dB@2 GHz
SiGe HBT	<1 KHz	0.65 dB@2 GHz	21 dB@2 GHz
GaAs HBT	<1 KHz	0.4 dB@2 GHz	25 dB@2 GHz
GaAs MESFET	>10 MHz	0.8 dB@12 GHz	12 dB@12 GHz
GaAs pHEMT	>10 MHz	0.25 dB@2 GHz 1 dB@18 GHz	16 dB@4 GHz 10 dB@18 GHz
InP HEMT	>10 MHz	0.3 dB@18 GHz	17 dB@18 GHz
GaAs mHEMT		0.4 dB@18 GHz	11.5 dB@18 GHz

Above the 1/f noise corner frequency, the noise is determined by the current shot noise, together with thermal noise from resistors in the current path. Comparing with bipolar transistors, HEMTs offer the best noise performance at high frequency, due to the low internal device resistances and the T-gate technology. Therefore, microwave HEMTs with low noise performance have already been widely used for low-noise amplifications. A GaAs pHEMT with a gate length of $0.15\mu\text{m}$ has been employed in a K-band 3-stage low noise amplifier for on-board receiver modules. The pHEMT provided an excellent low noise figure of 0.9 dB at 35 GHz [9].

2.3.3 Power Performance

HEMTs have been applied for power applications at microwave and millimeter-wave frequencies. The advantages of GaAs HEMTs over GaAs MESFETs for such applications are higher power gain and efficiency. These advantages are due to a high current-gain cutoff frequency resulting from higher electron velocity, which further leads to higher output power. A double heterojunction HEMT has been produced to increase drain current, thus improving power performance. An example with 1 W power at 20 GHz and 40 GHz has been reported [10]. A high-power pHEMT with a gate width of 600 μm provided output power of 24.4 dBm with a power-added efficiency of 57% at 18 GHz [10].

HBTs possess a higher current per effective transistor area, thus have higher power capability than HEMTs. The reason is that HEMTs have a very thin electron channel, so the number of electrons per unit of channel area is lower, and the maximum drain current is also lower. On the contrary, HBTs are a vertical structure. The entire emitter area contributes to current flow, resulting in higher current and power per transistor area. This property of HBTs has led to its usage as a microwave power amplifier. An output power density of 10 mW/ μm^2 emitter area at 10 GHz has been achieved in a GaAs HBT [11]. In addition, amplifiers with HBTs are capable of very high power added efficiencies. At 12 GHz an output power of 1 W with power added efficiency of 72% has been obtained [12].

Wide bandgap semiconductors such as SiC and group III-nitrides have high power density, due to their high breakdown field and high electron saturation velocity. Hence, they are suitable for high power microwave FETs. The SiC MESFET having 2.8 W/mm power density with 12.7% PAE at 1.8 GHz, and the AlGaIn/GaN HEMT having

9.8 W/mm power density with 47% PAE at 8 GHz have been realized [13], [14]. Compared to the wide bandgap FETs, GaAs HEMTs show much lower output power densities (about 0.6 W/mm), and lower breakdown voltage, but can operate at higher frequencies.

2.4 Philips OMMIC ED02AH Process

The OMMIC ED02AH process used in the distributed amplifier fabrication for this thesis is developed by Philips Ltd. for applications up to millimetric frequencies, and for high rate digital circuits for optical links. The transistors are 0.2 μm gate length depletion mode pHEMTs. In addition, in this process, enhancement mode transistors, diodes, implanted and thin-film resistors, Metal-Insulator-Metal (MIM) capacitors, spiral inductors and air bridges can be made. Several backside options are provided by the ED02AH process. A 620 μm thickness GaAs substrate without backside metal and via holes is suitable for coplanar design. On the other hand, a 100 μm thickness GaAs substrate with or without via holes is available for microstrip design.

The ED02AH GaAs pHEMT transistor is based on an AlGaAs-InGaAs-GaAs heterostructure obtained by MOVPE, using an industrial multiwafer system. The cross section of this device is shown in Figure 2.3.

Figure 2.3: Cross section of ED02AH pHEMT [15].

To obtain high maximum available gain and low noise, the multifinger devices can be utilized. The ED02AH process allows gate widths ranging from 10 to 50 μm per finger and up to 8 fingers.

The transistors may be laid out with one or two source grounds. Normally, symmetrical grounding is used to obtain the best performance. The small signal equivalent circuit for the device is shown in Figure 2.4.

Figure 2.4: pHEMT small signal equivalent circuit [15].

where:

C_g , C_d , C_s , L_G , L_D , L_S are the external parasitics of the pHEMT.

R_g , R_s , R_d are the pHEMT access resistances.

C_{gs} , C_{gd} , C_{ds} , R_{ds} , R_{gs} , and g_m are the classical GaAs pHEMT equivalent circuit elements.

g_{gd} (gate drain conductance), g_{gs} (gate source conductance) and R_{gd} (gate drain series resistance) are additional elements useful for a better accuracy under strong reverse gate-drain bias or forward gate-source bias.

2.5 Wideband Amplifier Topologies

An optical modulator driver used to pass high speed random digital data must have a very broad bandwidth. This means the driver should have flat gain over a very broad band. In this section, several popular circuit techniques utilized to implement wide band amplifier are compared.

2.5.1 Reactively Matched, Lossy Matched and Feedback Amplifiers

Reactively matched amplifiers use lossless matching networks to achieve gain compensation. Because of the use of lossless reactive elements, the maximum gain, minimum noise figure, and maximum power output may be achieved within the bounds of Fano's limit for a given FET with a properly designed matching network. The disadvantage of this kind of amplifier is its relatively poor low-frequency match [16].

The lossy matched amplifier adds resistors in their matching networks to provide lossy gain compensation at low frequencies, while maintaining a good input and output match over a broad bandwidth. The advantages of these amplifiers are that they have good gain; good input and output match over a broad bandwidth; small circuit size and can be cascaded. The disadvantages are that they have lower gain than that of reactively matched amplifier due to losses in their matching elements; have lower output power; and have a higher noise figure at low frequencies due to losses in the input and output matching network [16].

Feedback is a very effective technique for extending amplifier bandwidth. In practical amplifiers, the negative feedback from drain to gate of a FET is realized by a series L-

R-C network for ease of layout and biasing. The advantages of feedback amplifiers are that they have small circuit size; broad bandwidth; low gain drift with temperature and have the ability for cascading due to their good input and output match. The disadvantages include poor isolation and lower gain than those of reactively matched amplifiers [16].

2.5.2 Distributed Amplifier

Distributed amplifiers (DA) are widely used to obtain very broad band amplification. The reason is that they are not matched amplifiers, and therefore not subject to Fano's bandwidth limit. The theory of the distributed amplifier will be described in the next sections. The main advantages of DA are that it may provide flat gain over a wide bandwidth. The disadvantages of DA include large area and lower gain. The comparison of various broadband amplifier technologies is shown in Table 2.3.

Table 2.3. Comparison of various broadband amplifier technologies [17].

Amplifier Type	Bandwidth	Gain/device	Comments
Reactive Match	Lowest 1.5 to 2 octaves	Highest	Best power Best noise Large area
Lossy Match	< decade	< decade	Poor noise
Feedback	<=decade	Moderate gain	Small area Poor isolation
Distributed	Highest >decade	Lowest	Largest area

It is known that the optical modulator driver needs an amplifier with flat gain from very low frequency up to V band frequency. Comparing all the above wide band amplifier

technologies, the topology of distributed amplifiers is most suitable for the driver design due to its wide bandwidth characteristics.

2.6 Overview of Distributed Amplification

The distributed amplifier (DA) was first proposed by Percival in 1937 [18], and a detailed theoretical analysis of distributed amplification was given by Ginzton et al. in 1948 [19]. In addition, it is the first time that the term distributed amplifier appeared in the paper. Then, in 1950, Horton et al. gave corrective methods for the design of DA based on well-understood controllable parameters and first reported the experimental result [20]. From then on, in the 1960s, the distributed amplifier was developed rapidly through extensive theoretical research and experiment. The BJT (Bipolar Junction Transistors) was especially used in DA design [21]. In the early 1980s the DA technique became popular when the GaAs MESFETs could be used in a monolithic DA to achieve decade bandwidth microwave amplification [22], [23]. Distributed amplifiers entered a new era when HEMTs became available. An InP coplanar waveguide MMIC distributed amplifier having a gain of 5.5 dB over a frequency range of 5-100 GHz was successfully achieved by Majidi-Ahy et al. in 1990 [24]. Due to its flat gain performance over wide operating bandwidth, distributed amplification is a popular technology utilized for optical modulator drivers in optical transmitter systems [25], [26].

The distributed amplifier is based on the principle of utilizing the input and output capacitance of the transistors combined with the additional inductors to form artificial transmission lines. In this topology, the device transconductance couples the signal from the input transmission line to the output transmission line through each device section.

The devices provide amplification of the signal so that there is overall gain through the amplifier. Ideally, the travelling wave obtains additively superimpose on the output transmission line at each section as it travels toward the output. The cutoff frequencies of the input and output artificial transmission lines limit the amplifier's bandwidth. The schematic of a five stage common-source distributed amplifier having series lumped inductors on the gate and drain lines is shown in Figure 2.5. In practical monolithic microwave distributed amplifiers, the inductance is implemented by a short transmission line, such as microstrip and coplanar waveguide. Distributed amplification is discussed in more detail in the following chapter.

Figure 2.5: The diagram of a 5 - Section distributed amplifier.

A cascode FET arrangement is often used in distributed amplifiers, because this structure can provide high gain, high output resistance and high reverse isolation. In addition, the maximum output voltage swing only if limited by breakdown is higher than for a single FET. A cascode distributed amplifier is shown in Figure 2.6.

Figure 2.6: The circuit diagram of a 5 - section cascode distributed amplifier.

The gain limitation in a distributed amplifier is caused by the limitation on the number of active elements, as will be discussed in the next chapter. Another amplifier topology called a matrix distributed amplifier, which can overcome this limitation, was given by Niclas and Pereira [27].

In this matrix amplifier, the input line is the same as with a distributed amplifier. However, there are more tiers of active elements, and the “output line” of one tier is the input of the next tier. Finally, the output line of the top tier feeds the output of the amplifier. This type of amplifier combines the additive property of distributed amplifiers along with the multiplicative property of cascaded amplifiers. Therefore, this amplifier can maintain the large bandwidth property of the distributed amplifier and also obtain higher gain by adding more devices in its second tier. This matrix structure is quite compact and provides better input and output matching with a lower noise figure and higher gain per

unit area as compared with conventional cascaded multistage amplifiers [28]. Hence, it has relatively lower cost and is particularly suited to monolithic microwave integrated circuits. The configuration of a matrix distributed amplifier with five sections and two tiers is shown in Figure 2.7.

Figure 2.7: The circuit diagram of a 2x5 matrix distributed amplifier.

Chapter 3 Distributed Amplifier Theory

3.1 Introduction

In this chapter, a detailed theoretical analysis of the distributed amplifier (DA) is presented. Since the distributed amplifier can be considered as constant-k filter sections cascaded to form a low pass filter, the image parameter method is introduced in the distributed amplifier analysis. Then, the equations for the DA power gain and line attenuation, specific to the pHEMT device under consideration, are derived and the characteristics of the distributed amplifier are discussed. Finally, both cascode and matrix DAs are described and theoretically analyzed.

3.2 Image Parameter Method

3.2.1 Introduction

A distributed amplifier consists of cascaded identical two-port networks to form an artificial transmission line. The image parameter method is applied for the distributed amplifier analysis due to its relative mathematical simplicity. Hence, the concepts of image impedance and propagation functions of arbitrary networks must be introduced.

3.2.2 General Networks

A two-port network with its image impedance is shown in Figure 3.1(a). The image impedances Z_{i1} and Z_{i2} are defined as the impedances looking into port 1 and 2

respectively when ports 2 and 1 are terminated with Z_{i2} and Z_{i1} , respectively. For a reciprocal two-port, the image impedance is given by [29].

$$Z_{i1} = \sqrt{Z_{sc1} Z_{oc1}} \quad (3.1)$$

$$Z_{i2} = \sqrt{Z_{sc2} Z_{oc2}} \quad (3.2)$$

where Z_{sc1} is the input impedance of port 1 when port 2 is short circuited, and Z_{oc1} is its input impedance when port 2 is open circuited. Z_{i2} is defined similarly for port 2.

The propagation function specifies the transmission properties of the network when the source and load impedances are equal to the image impedances. The ratio V_1/V_2 and I_2/I_1 may be expressed in term of the propagation constant Υ as follows:

$$\frac{V_2}{V_1} = \sqrt{\frac{Z_{i2}}{Z_{i1}}} e^{-\Upsilon} \quad (3.3)$$

$$\frac{I_2}{I_1} = \sqrt{\frac{Z_{i1}}{Z_{i2}}} e^{-\Upsilon} \quad (3.4)$$

If the network is symmetric, Z_{i1} is identical to Z_{i2} . So

$$\frac{V_2}{V_1} = e^{-\Upsilon} \quad (3.5)$$

The propagation constant is defined as $\Upsilon = \alpha + j\beta$, where α is the attenuation, sometimes referred to as the attenuation per section, and β is the phase shift, which is related to the phase velocity. Ragan [29] has shown the propagation constant can be expressed as follow:

Figure 3.1: (a) 2 - port Network with Image Impedance
 (b) L-Section Schematic
 (c) T-Section Schematic
 (d) π -Section Schematic

$$\Upsilon = \tanh^{-1} \sqrt{\frac{Z_{sc1}}{Z_{oc1}}} = \tanh^{-1} \sqrt{\frac{Z_{sc2}}{Z_{oc2}}} \quad (3.6)$$

3.2.3 L-Section

Both the gate line and the drain line of the distributed amplifier are formed by cascading L- sections. Therefore, understanding its propagation constant is necessary. The L-section, also called half-section, is shown on Figure 3.1(b). It is easy to obtain

$$Z_{sc1} = \frac{Z_1}{2} \quad (3.7)$$

$$Z_{oc1} = \frac{Z_1}{2} + 2Z_2 \quad (3.8)$$

$$Z_{sc2} = \frac{1}{\frac{1}{2Z_2} + \frac{2}{Z_1}} \quad (3.9)$$

$$Z_{oc2} = 2Z_2 \quad (3.10)$$

where the parameters Z_1 and Z_2 are the series and shunt arm impedance, respectively. Substituting equation (3.9) and (3.10) into (3.1) and (3.2), the image impedance Z_{i1} and Z_{i2} can be obtained:

$$Z_{i1} = \sqrt{Z_1 Z_2 \left(1 + \frac{Z_1}{4Z_2}\right)} \quad (3.11)$$

and

$$Z_{i2} = \sqrt{\frac{Z_1 Z_2}{1 + \frac{Z_1}{4Z_2}}} \quad (3.12)$$

Inserting equation (3.7) and (3.8) into (3.6), the propagation constant of the L-section is expressed as

$$\gamma_L = \tanh^{-1} \sqrt{\frac{1}{1 + \frac{Z_1}{4Z_2}}} = \frac{1}{2} \cosh^{-1} \left(1 + \frac{Z_1}{2Z_2} \right) \quad (3.13)$$

By substituting equation (3.11) and (3.12) into (3.3), the voltage transfer function of the L-section can be obtained

$$\frac{V_2}{V_1} = \frac{e^{-\gamma_L}}{\sqrt{1 + \frac{Z_1}{4Z_2}}} \quad (3.14)$$

and the reverse transfer function is defined as

$$\frac{V_1}{V_2} = \sqrt{1 + \frac{Z_1}{4Z_2}} e^{-\gamma_L} \quad (3.15)$$

Meanwhile, the current transfer function of the L-section also can be obtained from equation (3.4).

$$\frac{I_2}{I_1} = \sqrt{1 + \frac{Z_1}{4Z_2}} e^{-\gamma_L} \quad (3.16)$$

3.2.4 T-Section

Two identical L-sections can be cascaded to form a T-section, as shown in Figure 3.1 (c). Therefore, the image impedance may be easily obtained. The image impedance of a T-section is given by equation (3.11).

$$Z_{ii} = \sqrt{Z_1 Z_2} \sqrt{\left(1 + \frac{Z_1}{4Z_2} \right)} \quad (3.17)$$

and the voltage transfer function is obtained as

$$\frac{V_2}{V_1} = e^{-\gamma_T} = e^{-2\gamma_L} \quad (3.18)$$

The propagation function may be derived from equation (3.6) as

$$\gamma_T = \cosh^{-1} \left(1 + \frac{Z_1}{2Z_2} \right) \quad (3.19)$$

3.2.5 π -Section

Two identical L-sections can also be transposed and cascaded to form a π -section, as shown in Figure 3.1 (d). The image impedance of a π -section may be obtained from equation (3.12) as

$$Z_{i\pi} = \sqrt{Z_1 Z_2} \sqrt{\left(1 + \frac{Z_1}{4Z_2} \right)^{-1}} \quad (3.20)$$

and the voltage transfer function is

$$\frac{V_2}{V_1} = e^{-\gamma_\pi} = e^{-2\gamma_L} \quad (3.21)$$

The propagation function may be derived from equation (3.6) as

$$\gamma_\pi = \cosh^{-1} \left(1 + \frac{Z_1}{2Z_2} \right) \quad (3.22)$$

It is clear that the propagation constant for both the T-section and π -section are identical.

A lossless lumped element transmission line can be formed by a lossless cascade of T-sections, and is shown in Figure 3.2. The propagation constant and image impedance can be derived from equation (3.17) and (3.19), where $Z_1 = j\omega L$, and $Z_2 = 1/j\omega C$.

Figure 3.2: Lossless cascade of T - sections forming artificial transmission line.

$$\Gamma = \cosh^{-1} \left(1 - \frac{2\omega^2}{\omega_c^2} \right) \quad (3.23)$$

$$Z_i = \sqrt{\frac{L}{C} \left(1 - \left(\frac{\omega}{\omega_c} \right)^2 \right)} \quad (3.24)$$

in which

$$\omega_c = \frac{2}{\sqrt{LC}} \quad (3.25)$$

The above results are only valid when the artificial transmission line is terminated in its image impedance at both ports. Figure 3.3 shows the variation of image impedance of the artificial transmission line as a function of frequency. It is seen that the image impedance is Z_0 and equal to $\sqrt{L/C}$ at low frequency, and decreases to zero at the cutoff frequency ω_c . Thus, an artificial transmission line behaves like an ordinary transmission line well below its cutoff frequency, that is α is equal to zero, and β is a linear function of ω .

Figure 3.3: The plot of the image impedance, α and β vs. ω for lossless artificial transmission line.

3.3 Distributed Amplifier Theory

3.3.1 Introduction

The basic configuration for a distributed amplifier was shown in Figure 2.5, where the input and output capacitances of transistors are combined with lumped inductances to form two artificial transmission lines. The input artificial transmission line is referred to as the gate line, while the output artificial transmission line is referred to as the drain line. These artificial transmission lines are realized by cascading sections terminated by the image impedance. The gate line is coupled to the drain-line by the transconductances of transistors.

The shunt capacitors of the gate and drain line are formed by the intrinsic capacitances C_{gs} and C_{ds} of the device, respectively, and the series lumped inductances are normally replaced by a transmission line in practical high frequency MMIC implementations.

The input signal of the distributed amplifier travels along the gate-line until absorbed by the gate line terminal impedance. Each of the FETs is excited in turn during the signal's travel. FETs amplify the signal and feed a forward travelling wave and a reverse travelling wave onto the drain line. The forward travelling wave outputs at the load, while the reverse travelling wave propagates to the drain dummy load. If the phase velocities of the gate line and drain line are designed to be equal, the forward travelling wave components from each FET will be added at the output. On the other hand, the reverse travelling waves will be cancelled at higher frequencies. The drain dummy load will absorb any unwanted signal.

3.3.2 Artificial Transmission Line for DA

The distributed amplifier is formed as two artificial transmission lines: gate and drain artificial transmission line. The equivalent circuit diagram of a basic distributed amplifier is shown in Figure 3.5 and includes the equivalent pHEMT model of Figure 3.4, where the control voltage V_c is across C_{gs} and R_i . In the section of gate artificial line, the equivalent input circuit of the FET is a series C-R network, C_{gs} and R_i being the input capacitance and resistance of the FET respectively; L_g represents the series inductance. Similarly, in the section of drain artificial line, the equivalent circuit of the FET is a shunt

C-R network, C_{ds} and R_{ds} being the output capacitance and resistance of the FET respectively; and L_d represents the series inductance.

Both the gate- and drain-line attenuation can be derived from the propagation function of the constant-k line from (3.19).

$$\cosh(\alpha + j\beta) = 1 + \frac{Z_1}{2Z_2} \quad (3.26)$$

The Z_1 and Z_2 are the impedances in the series and shunt arms of a section of constant-k line, and $Z_1 = j\omega L_g$; $Z_2 = 1/(j\omega C_{gs}) + R_i$. Hence, the propagation constant of gate line is derived as

$$\cosh(\alpha_g + j\beta_g) = 1 + \frac{j\omega L_g}{2\left(\frac{1}{j\omega C_{gs}} + R_i\right)} = 1 - \frac{\omega^2 L_g C_{gs}}{2(1 + j\omega R_i C_{gs})} \quad (3.27)$$

which can be expanded into real and imaginary parts as:

$$\cosh \alpha_g \cos \beta_g + j \sinh \alpha_g \sin \beta_g = 1 - \frac{2\omega^2/\omega_c^2}{1 + \omega^2/\omega_g^2} + j \frac{2(\omega/\omega_c)^2 \omega/\omega_g}{1 + \omega^2/\omega_g^2} \quad (3.28)$$

where $\gamma_g = \alpha_g + j\beta_g$; $\omega_g = 1/(R_i C_{gs})$ is the gate circuit cutoff frequency, and

$\omega_c = 2/(\sqrt{L_g C_{gs}})$ is the cutoff frequency of the lines. At frequencies well below the cutoff frequency, it may be shown $\cosh \alpha_g$ is close to unity [30]. Thus,

$$\cos \beta_g \approx 1 - \frac{2\omega^2/\omega_c^2}{1 + \omega^2/\omega_g^2} \quad (3.29)$$

then the term of $\sin \beta_g$ can be derived as

Figure 3.4: Lossy and unilateral pHEMT model.

Figure 3.5: Equivalent model of a distributed amplifier including lossy pHEMT model.

- (a) Gate artificial transmission line
 (b) Drain artificial transmission line

$$\begin{aligned}
\sin \beta_g &= \sqrt{1 - \cos^2 \beta_g} \\
&= 2\omega/\omega_c \sqrt{\frac{1}{1 + \omega^2/\omega_g^2} - \frac{\omega^2/\omega_c^2}{(1 + \omega^2/\omega_g^2)^2}}
\end{aligned} \tag{3.30}$$

Since $\sinh \alpha_g = \alpha_g$ for small α_g , the imaginary part of equation (3.28) can be modified as

$$\alpha_g \sin \beta_g = \frac{2(\omega/\omega_c)^2 \omega/\omega_g}{1 + \omega^2/\omega_g^2} \tag{3.31}$$

Substitute (3.30) to (3.31), the attenuation of gate line is expressed as

$$\begin{aligned}
\alpha_g &\approx \frac{2(\omega/\omega_c)^2 \omega/\omega_g}{1 + \omega^2/\omega_g^2} \left(2\omega/\omega_c \sqrt{\frac{1}{1 + \omega^2/\omega_g^2} - \frac{\omega^2/\omega_c^2}{(1 + \omega^2/\omega_g^2)^2}} \right)^{-1} \\
&= \frac{(\omega_c/\omega_g)(\omega/\omega_c)^2}{\sqrt{1 - (1 - \omega_c^2/\omega_g^2)(\omega^2/\omega_c^2)}} \quad [\text{nepers/section}]
\end{aligned} \tag{3.32}$$

Now we derive the attenuation factor of the drain line. From drain line in Figure 3.6 and the equation (3.26)

$$\begin{aligned}
\cosh(\alpha_d + j\beta_d) &= \cosh \alpha_d \cos \beta_d + j \sinh \alpha_d \sin \beta_d = 1 + \frac{Z_1}{2Z_2} \\
&= 1 + \frac{j\omega L_d(1/R_{ds} + j\omega C_{ds})}{2} = 1 - \frac{2\omega^2}{\omega_c^2} + j\frac{2\omega\omega_d}{\omega_c^2}
\end{aligned} \tag{3.33}$$

where $Z_1 = j\omega L_d$, $Z_2 = 1/[(1/R_{ds}) + j\omega C_{ds}]$, $\omega_d = 1/(R_{ds}C_{ds})$ and

$\omega_c = 2/\sqrt{L_d C_{ds}}$. So the imaginary part from equation (3.33) is expressed as

$$\sinh \alpha_d \sin \beta_d = \frac{2\omega\omega_d}{\omega_c^2} \quad (3.34)$$

Since $\sinh \alpha_d \approx \alpha_d$ for small α_d , thus

$$\alpha_d \sin \beta_d = \frac{2\omega\omega_d}{\omega_c^2} \quad (3.35)$$

Meanwhile, within the passband, $\cosh \alpha_d$ is close to unity, the imaginary part of equation (3.33) can be expressed as

$$\cos \beta_d = 1 - \frac{2\omega^2}{\omega_c^2} \quad (3.36)$$

then,

$$\sin \beta_d = \sqrt{1 - \cos^2 \beta_d} = \frac{2\omega}{\omega_c} \sqrt{1 - \frac{\omega^2}{\omega_c^2}} \quad (3.37)$$

substitute equation (3.37) into (3.35), the attenuation factor of the drain line is derived as

$$\alpha_d \approx \frac{2\omega\omega_d}{\omega_c^2 \sin \beta_d} = \frac{\omega_d/\omega_c}{\sqrt{1 - \omega^2/\omega_c^2}} \quad [\text{nepers/section}] \quad (3.38)$$

The attenuation vs. frequency on the gate and drain lines for different ω_c/ω_g or ω_d/ω_c values are shown in Figure 3.6 (a) and (b).

In Figure 3.6, both the gate and drain line attenuations increase with frequency, as well as the ω_c/ω_g and ω_d/ω_c , respectively. And the ω_g and ω_d are affected by the parameters of R_i and R_{ds} respectively. It is clear from equation (3.32) and (3.38) that the gate line loss is proportional to the R_i , and the drain line loss is inversely proportional to the R_{ds} . Therefore, the larger R_{ds} and smaller R_i should be chosen to reduce the line's

(a)

(b)

Figure 3.6: (a) Attenuation on gate line versus normalized frequency.
 (b) Attenuation on drain line versus normalized frequency.

attenuation. In addition, gate line attenuation is more sensitive to frequency than drain line attenuation and thus it has more impact on limiting the upper frequency of the distributed amplifier. Furthermore, the attenuation of the drain line, unlike that on the gate line, exists at low frequency. Therefore, low frequency gain of the DA is affected primarily by the drain line while the high frequency gain is affected by both line attenuations.

3.3.3 Distributed Amplifier Gain

An input wave propagating along the gate line, via the k th FET, to the output on the drain line has been shown in Figure 3.5. The voltage at k th FET's gate may be expressed as

$$V_{gk} = V_{g1} [\exp(-(k-1)\Upsilon_g l_g)] \quad (3.39)$$

where $\Upsilon_g = \alpha_g + j\beta_g$ is the gate line propagation constant converted to per meter quantity, l_g is the gate line length between any two FETs. V_{g1} is the voltage across the first gate, and can be derived from equation (3.14).

$$V_{g1} = \frac{V_{in} \exp(-\Upsilon_g l_g / 2)}{\sqrt{1 + \frac{Z_{g1}}{4Z_{g2}}}} \quad (3.40)$$

where V_{in} is the voltage of the input signal wave, Z_{g1} and Z_{g2} are the gate series and shunt arm impedances, respectively. Substituting equation (3.40) into (3.39), the voltage of k th gate is obtained.

$$V_{gk} = \frac{V_{in} \exp[-(2k-1)\Upsilon_g l_g / 2]}{\sqrt{1 + \frac{Z_{g1}}{4Z_{g2}}}} \quad (3.41)$$

For the pHEMT model, the current contributed from k th FET to the drain line is $g_m V_{gk}$, and then is divided into two parts that go forward and backward along the drain line.

The drain current across n -th FET, I_{dn} , can be expressed as:

$$I_{dn} = \frac{g_m}{2} \sum_{k=1}^n V_{gk} \exp[-(n-k)\Upsilon_d l_d] \quad (3.42)$$

where l_d is the drain line length between any two FETs.

From equation (3.16), the total forward part current appearing on the drain load can be derived as

$$I_0 = \frac{I_{dn} \exp(-\Upsilon_d l_d / 2)}{\sqrt{1 + \frac{Z_{d1}}{4Z_{d2}}}} \quad (3.43)$$

where Z_{d1} and Z_{d2} are the drain series and shunt arm impedances respectively, Therefore, the total current on the load can be derived as:

$$\begin{aligned} I_0 &= \frac{g_m}{2 \sqrt{1 + \frac{Z_{d1}}{4Z_{d2}}}} \sum_{k=1}^n V_{gk} \exp[-(2n-2k+1)\Upsilon_d l_d / 2] \\ &= \frac{g_m V_{in}}{2 \sqrt{1 + \frac{Z_{d1}}{4Z_{d2}}} \sqrt{1 + \frac{Z_{g1}}{4Z_{g2}}}} \sum_{k=1}^n \exp\{ -[(2k-1)\Upsilon_g l_g + (2n-2k+1)\Upsilon_d l_d] / 2 \} \end{aligned} \quad (3.44)$$

The total current equation (3.44) can be simplified as (see Appendix 1)

$$I_0 = \frac{g_m V_{in} \exp[-n(\Upsilon_g l_g + \Upsilon_d l_d)/2] \sinh[n(\Upsilon_d l_d - \Upsilon_g l_g)/2]}{2 \sqrt{1 + \frac{Z_{d1}}{4Z_{d2}}} \sqrt{1 + \frac{Z_{g1}}{4Z_{g2}}} \sinh[(\Upsilon_d l_d - \Upsilon_g l_g)/2]} \quad (3.45)$$

Since the output power is $\frac{1}{2} I_0^2 Z_{dL}$, and the input power is $\frac{1}{2} V_{in}^2 / Z_{gL}$, Where Z_{gL} and Z_{dL} are the terminal L-section image impedances of the gate and drain lines as defined in (3.11), and is

$$Z_{gL} = \sqrt{Z_{g1} Z_{g2} \left(1 + \frac{Z_{g1}}{4Z_{g2}}\right)} \quad (3.46)$$

$$Z_{dL} = \sqrt{Z_{d1} Z_{d2} \left(1 + \frac{Z_{d1}}{4Z_{d2}}\right)} \quad (3.47)$$

If the gate line phase shift per section $\phi_g = \beta_g l_g$ is equal to the drain line phase shift per section $\phi_d = \beta_d l_d$, thus $\Upsilon_g l_g + \Upsilon_d l_d = \alpha_g l_g + \alpha_d l_d + j2\phi$, $\Upsilon_d l_d - \Upsilon_g l_g = \alpha_d l_d - \alpha_g l_g$, where $\phi = \phi_g = \phi_d$. Therefore, the operating power gain is obtained.

$$\begin{aligned} G &= \frac{I_0^2 Z_{dL}}{V_{in}^2 / Z_{gL}} \\ &= \frac{g_m^2}{4} \frac{\sqrt{\frac{Z_{g1} Z_{g2}}{1 + \frac{Z_{g1}}{4Z_{g2}}}} \sqrt{\frac{Z_{d1} Z_{d2}}{1 + \frac{Z_{d1}}{4Z_{d2}}}} \frac{\sinh^2[n(\Upsilon_d l_d - \Upsilon_g l_g)/2]}{\sinh^2[(\Upsilon_d l_d - \Upsilon_g l_g)/2]} \exp[-n(\Upsilon_g l_g + \Upsilon_d l_d)]}{Z_{0G} Z_{0D} \frac{\sinh^2[n(\Upsilon_d l_d - \Upsilon_g l_g)/2]}{\sinh^2[(\Upsilon_d l_d - \Upsilon_g l_g)/2]} \exp[-n(\Upsilon_g l_g + \Upsilon_d l_d)]} \\ &= \frac{g_m^2}{4} Z_{0G} Z_{0D} \frac{\sinh^2[n(\Upsilon_d l_d - \Upsilon_g l_g)/2]}{\sinh^2[(\Upsilon_d l_d - \Upsilon_g l_g)/2]} \exp[-n(\Upsilon_g l_g + \Upsilon_d l_d)] \end{aligned} \quad (3.48)$$

where Z_{0G} and Z_{0D} are the image impedances of the gate and drain lines. Note that the image impedances of the gate and drain lines should be identical for a basic distributed amplifier in order to obtain equal phase shift.

The gain equation (3.48) is valid with three assumptions: i) The unilateral pHEMT model is shown in Figure 3.4. ii) All of the input source, output load, gate and drain line terminations are image impedance matched. iii) The phase shift of gate and drain line are equal.

The series and shunt arm impedances of gate and drain lines are shown in Figure 3.5. So,

$$Z_{g1} = j\omega L_g \quad (3.49)$$

$$Z_{g2} = R_i + \frac{1}{j\omega C_{gs}} \quad (3.50)$$

$$Z_{d1} = j\omega L_d \quad (3.51)$$

and

$$Z_{d2} = \frac{1}{1/R_{ds} + j\omega C_{ds}} \quad (3.52)$$

Normally, the cut-off frequency and the characteristic impedances of the gate and drain lines are equal for the distributed amplifier. Hence, the series gate and drain line inductance L_g and L_d are equal. In addition, the gate and drain capacitance C_{gs} and C_{ds} are equal too. However, in most FETs, the capacitance on the gate is greater than that on the drain. To keep the same value for the two capacitances, a shunt capacitance C_p is added in parallel to C_{ds} , such that

$$C_d = C_{ds} + C_p = C_{gs} \quad (3.53)$$

Where C_d is defined as the effective drain line shunt capacitance. When the amplifier has low loss on both gate and drain lines, the parameters R_i and $1/R_{ds}$ can be neglected in the Z_{oG} and Z_{oD} expressions. Hence, the image impedances of gate and drain lines Z_{oG} and Z_{oD} can be expressed as

$$Z_{0G} = \frac{Z_{0g}}{\sqrt{1 - \left(\frac{\omega}{\omega_c}\right)^2}} \quad (3.54)$$

$$Z_{0D} = \frac{Z_{0d}}{\sqrt{1 - \left(\frac{\omega}{\omega_c}\right)^2}} \quad (3.55)$$

where $Z_{0g} = \sqrt{L_g/C_{gs}}$, $Z_{0d} = \sqrt{L_d/C_d}$ and $\omega_c = 2/\sqrt{L_g C_{gs}} = 2/\sqrt{L_d C_d}$.

Then, the gain equation (3.48) can be simplified as

$$G = \frac{g_m^2 Z_{0g} Z_{0d} \sinh^2[n(\Upsilon_d l_d - \Upsilon_g l_g)/2]}{4 \left[1 - \left(\frac{\omega}{\omega_c}\right)^2\right] \sinh^2[(\Upsilon_d l_d - \Upsilon_g l_g)/2]} \exp[-n(\Upsilon_g l_g + \Upsilon_d l_d)] \quad (3.56)$$

This equation is different from that derived in the classical distributed amplifier paper by Beyer [31] because of the different FET model used in this work. The MESFET model used by Beyer has a control voltage across C_{gs} , so the ratio of the control voltage V_c to the input voltage V_g is $1/(1 + j\omega R_i C_{gs})$, that results in one more product term $[1 + (\omega/\omega_g)^2]^{1/2}$ on the denominator of the gain equation, where $\omega_g = 1/(R_i C_{gs})$. At low frequency, this additional term is close to unity. Hence, both gain expressions are approximately identical. However, at high frequency, this term results in lower gain in [31] than here.

For values of $n\alpha_g l_g \ll 1$, and when drain line losses are neglected compared with gate line loss, $\exp(-n\alpha_g l_g) \approx 1 - n\alpha_g l_g$ and $\exp(-n\alpha_d l_d) \approx 1$ [32], the gain in equation (3.56) can be rewritten

$$G \approx \frac{n^2 g_m^2 Z_{0g} Z_{0d}}{4} \quad (3.57)$$

This power gain is limited by the DA's gate and drain line losses. Therefore, the DA gain cannot be increased indefinitely by adding FETs. An optimum number of stages (n) which maximizes power gain can be derived by differentiating the power gain (3.56) with the n, and equating the resultant expression to zero.

$$n_{opt} = \frac{\ln(\alpha_d^l d / \alpha_g^l g)}{\alpha_d^l d - \alpha_g^l g} \quad (3.58)$$

This expression states that the optimum number of sections depends on the attenuation of gate- and drain-line. This property of DA can be explained as follows. As the signal propagates down the gate line, its amplitude drops due to the gate line attenuation. Similarly, the signal produced by the FETs becomes weaker at the output due to the drain line attenuation. Therefore, when a section is added beyond the optimum number of sections, insufficient signal exists on the drain line to surmount the attenuation of the extra section on the drain line. Thus, the gain begins to decrease with further additions of sections.

3.3.4 Image Impedance Matching

The cascade of constant k filter sections forms an artificial transmission line of image impedance $Z_{i\pi}$. The transmission line needs to be terminated in load impedance of $Z_{i\pi}$ in order that the reflection coefficient is equal to zero. The image impedance of the

π - type constant k filter section can be obtained from equation (3.20). If the input and output L- section are included, then the transmission line needs to be terminated in Z_{0L} rather than $Z_{0\pi}$. The Z_{0L} can be obtained from equation (3.11). By inserting equations (3.49) through (3.52) into (3.11), and let R_i and $1/R_{ds}$ equal zero, the image impedance in the gate- and drain-line can be expressed respectively as:

$$Z_{GT} = Z_{0g} \sqrt{1 - \left(\frac{\omega}{\omega_c}\right)^2} \quad (3.59)$$

$$Z_{DT} = Z_{0d} \sqrt{1 - \left(\frac{\omega}{\omega_c}\right)^2} \quad (3.60)$$

As an example, the plot of the terminal image impedance vs. frequency for a 50Ω characteristic impedance transmission line with $\omega_c = 4.44 \times 10^{11}$ rad is shown in Figure 3.7.

The required matching image impedance decreases as the frequency increases. The impedance is about 50Ω at low frequency, but only about 35Ω at 50 GHz . This property of terminal matching for the artificial transmission line is that Z_{GT} and Z_{DT} vary with frequency.

3.4 Cascode Distributed Amplifier

The cascode arrangement is obtained by cascading the common-source HEMT (CSH) with a common-gate HEMT (CGH). These cascode cells with series lumped inductors form the cascode DA. The simple schematic diagram for this configuration is shown in Figure 2.6. If the transconductances of CSH and CGH in the cascode cell are identical, the

Figure 3.7: The plot of the real part of the terminal impedance vs. frequency for $Z_0 = 50 \Omega$, and $\omega_c = 4.44 \times 10^{11}$ rad.

cascode circuit has the same transconductance as a single CSH circuit, since the current gain of CGH is unity. Therefore, the gain of the cascode DA at low frequency can be approximately expressed by equation (3.57). However, several advantages of using cascode cells in the distributed amplifier exist and are discussed below.

First, the cascode cell has higher output shunt impedance than the common source device. If both of CSH and CGH have same gate width, the output shunt impedance of a cascode cell at low frequency is $(2 + g_m r_{ds})r_{ds}$, which is higher than the r_{ds} of the simple common source device. Meanwhile, it is evident from equation (3.38) that higher shunt output impedance reduces the signal loss on the drain line, so the amplifier performance may be improved.

Secondly, the cascode cell has lower feedback capacitance, which improves isolation and allows millimeter wave design. In addition, the Miller capacitance referred to the input of a CSH stage is equal to the gate-to-drain capacitance C_{gd} multiplied by the voltage gain of the stage, that is, $C_{miller} = C_{gd}(1 - K)$, where K is the voltage gain. For the simple CSH stage the voltage gain is $-g_m r_{ds}$, that can be large; thus, the Miller capacitance is large and substantially reduce the bandwidth of the circuit. For the cascode cell, the voltage gain of the CSH is lower because of the lower impedance from the CGH. The CSH has a load impedance of approximately $1/g_{m2}$, so the voltage gain of the CSH is approximately $-g_{m1}(1/g_{m2})$, that can be approximately minus one while $g_{m1} = g_{m2}$. Therefore, the Miller capacitance can be small, which results in improvement of ω_c/ω_g ratio which affects α_g , and thus expands bandwidth (Figure 3.6).

Thirdly, the cascode configuration has higher voltage swing at the output before HEMT breakdown is reached, because the simple CSH is the inverting output, and the cascode cell has its noninverting CGH output.

As a result of these advantages, the cascode configuration is often used in distributed amplifier to yield a significant improvement in performance with little additional circuit area. However, one limiting factor to be mentioned is that the cascode configuration exhibits negative resistance, which can affect the gain flatness and the stability of the circuit. The equivalent circuit of one cascode cell is shown in Figure 3.8, and the analysis of the negative resistance in a cascode cell is as follows.

We assume that C_{gd} is small enough to neglect, and

Figure 3.8: The equivalent circuit of one cascode cell.

$$\begin{aligned}
 Z_{ds1} &= \frac{R_{ds1}(1 - j\omega R_{ds1}C_{ds1})}{1 + \omega^2 R_{ds1}^2 C_{ds1}^2} = R_1 - jX_1 \\
 Z_{gs2} &= R_{gs2} - j/(\omega C_{gs2}) = R_2 - jX_2 \\
 Z_{ds2} &= \frac{R_{ds2}(1 - j\omega R_{ds2}C_{ds2})}{1 + \omega^2 R_{ds2}^2 C_{ds2}^2} = R_3 - jX_3
 \end{aligned} \tag{3.61}$$

So the output impedance of the cascode configuration can be derived from Figure 3.8, the equation (3.62) is obtained.

$$\frac{V_c - V_{out}}{Z_{ds2}} + g_{m2}V_c + i_{out} = 0 \tag{3.62}$$

and

$$V_c = \frac{Z_{ds1}Z_{gs2}}{Z_{ds1} + Z_{gs2}} i_{out} \tag{3.63}$$

so combine equation (3.61), (3.62) and (3.63), we can obtain

$$\begin{aligned}
Z_{out} &= \frac{V_{out}}{i_{out}} = \frac{Z_{ds1}Z_{gs2}}{Z_{ds1} + Z_{gs2}}(1 + g_{m2}Z_{ds2}) + Z_{ds2} \\
&= \frac{R_1R_2 - X_1X_2 - j(R_1X_2 + R_2X_1)}{R_1 + R_2 - j(X_1 + X_2)}[1 + g_{m2}(R_3 - jX_3)] + R_3 - jX_3
\end{aligned} \tag{3.64}$$

If the image product parts is ignored for the small value, the real part of the output impedance Z_{out} may be written as

$$Re(Z_{out}) \approx \frac{[R_1R_2(R_1 + R_2) - X_1X_2(R_1 + R_2) + (X_1 + X_2)(R_1X_2 + R_2X_1)](1 + g_{m2}R_3)}{(R_1 + R_2)^2 + (X_1 + X_2)^2} + R_3 \tag{3.65}$$

It is clear that there is a negative resistance component, which is approximately equal to

$$R_{nr} \approx \frac{X_1X_2(R_1 + R_2)(1 + g_{m2}R_3)}{(R_1 + R_2)^2 + (X_1 + X_2)^2} \tag{3.66}$$

The negative resistance of the cascode configure in equation (3.66) is dependent on parameters of transistors. The generation of the negative resistance can be explained below.

In a conventional cascode configuration, the output impedance of CSH seen from the source terminal of the CGH is capacitive because of the drain-to-source capacitance (C_{ds1}) of the CSH. Hence, a positive feedback circuit is existed, and results in a negative resistance generation in this configuration. This negative resistance can cause gain peak at high end frequency, and degrades the stability of the amplifier around the cutoff frequency. Several techniques discussed in the next chapter are used to suppress the negative resistance and keep the circuit stable.

3.5 Matrix Distributed Amplifier

The concept of the matrix amplifier combines additive property of distributed amplifiers along with the multiplicative property of cascade amplifiers. In this topology, amplifier can maintain wide bandwidth property of distributed amplifier and still obtain high gain by adding more FETs in the second tier of the matrix DA. The configuration of a 2×5 matrix DA is shown in Figure 2.7. In this amplifier, there are two tiers and five sections of FETs. The idle ports of both input (gate) and output (drain) line are terminated with load resistor to provide an adequate return loss. The center line serves as the output line of the first tier and as the input of the second tier. The idle port of the center line are also terminated with load resistors.

The equation of the low frequency power gain for a two-tier matrix amplifier was provided by C. Paoloni [33]

$$A_o = g_{m1} g_{m2} A_n t \quad (3.67)$$

where

$$A_n = \frac{Z_o N \sinh(b) e^{-b}}{4 \sinh(b/N)}$$

$$t = \frac{Z_{oc} R_{ds} / N}{Z_{oc} / 2 + R_{ds} / N}$$

$$b = \frac{N Z_o}{4 R_{ds}}$$

N section number of matrix amplifier

Z_o characteristic impedance of the gate or drain line.

Z_{oc} characteristic impedance of the central line.

g_{m1} , g_{m2} transconductance of the FET's on the first and second rows respectively.

R_{ds} output resistor of the FET's on the input row.

This equation may be used for theoretical forecast during matrix circuit design.

The advantages of the matrix DA include significantly higher gain over wide bandwidth at considerably reduced size, and hence cost less to produce. It may yield a compact circuit with higher gain per unit area than cascades stages of conventional distributed amplifier. Since the gain of a conventional distributed amplifier is limited by the loss on the gate and drain lines, an optimum FET's number is considered in the DA structure. On the contrary, the matrix amplifier topology can overcome this number limitation of FETs by adding more FETs on several tiers. The another advantages include good input/output match, and flexible circuit topology to obtain nice performance. The disadvantage of the matrix DA is a gain ripple at high-end frequency because of the return loss degradation. Several techniques mentioned in the next chapter are used to cancel this effect and keep the gain flat.

3.6 Conclusion

A detailed theoretical analysis with considering FET losses has been presented for a distributed amplifier. It was found that the number of stages that may be used in the DA is limited by the inherent losses on the gate and drain line, and the terminal image impedance is decreased as frequency increases. In addition, the equations of the DA power gain and lines attenuation for the pHEMT model has been successfully derived. Finally, two types of distributed amplifiers, cascode DA and matrix DA, are briefly described and theoretical analyses are performed.

Chapter 4 Distributed Amplifier Design

4.1 Introduction

In the previous chapter we have overviewed several configurations of distributed amplifier that are suitable to form an optical modulator driver. In this chapter, the design of two MMIC distributed amplifiers will be described in detail. The first amplifier employs a cascode gain cell and is based on microstrip technology. The second amplifier is a matrix distributed configuration, and is based on coplanar waveguide technology. Some performance improvement techniques used in these circuits will be presented. The designs were carried out using the HPEEs of Libra microwave circuit CAD and Momentum EM simulator tools [34].

An electro-optic (EO) modulator with travelling wave Mach-Zehnder configuration has been designed for next-generation optical transmitter systems (> 40 Gbps). This modulator has 10.7 V half-wave voltage and a 65 GHz bandwidth. Therefore, a powerful amplifier with 10.7 V peak-to-peak output voltage over this bandwidth is required to drive this EO modulator.

To obtain such an output voltage swing in a $50\ \Omega$ system, the driver amplifier should achieve approximately 25 dBm output power. In addition, a 20 dB to 25 dB power gain for the driver would be desirable. Meanwhile, the amplifier should exhibit a 65 GHz upper-frequency and an 8 KHz low-frequency while maintaining gain flatness over this broad bandwidth [35]. Both the input and the output should be matched to $50\ \Omega$. These

objectives are ideal and cannot be achieved as a single MMIC with the technology available. More realistic objectives will be presented for each distributed amplifier design in the following sections.

4.2 Design of a Cascode Distributed Amplifier

4.2.1 Cascode DA Design Objectives

The modulator driver IC will be fabricated using the Philips foundry process, which is a GaAs 0.2 μm pHEMT technology. The transistor has a threshold voltage of -0.9 V, a drain-gate breakdown voltage of 8 V, and a current gain cutoff frequency f_t of 63 GHz. The maximum allowable MMIC area for this amplifier circuit is $2.2 \times 1.0 \text{ mm}^2$. In addition, this amplifier will not be packaged, so all circuit elements are to be designed on-chip.

The revised objectives consistent with the above limitations are as follows. A power gain of 8 dB is to be realized. The bandwidth of this amplifier is to be maximized, extending as high in frequency as possible for this transistor technology and as low as possible with on-chip capacitors. In addition, the input and output return loss of the amplifier should be greater than 10 dB over the band in a 50Ω system. Under these conditions, output voltage swing is to be maximized. Reducing the gain target to only 8 dB means that a practical implementation would require a preamplifier to obtain more than 20 dB gain overall. Such pre-amplifier stages having less than 15 dB of gain with a moderate output power level are readily achieved.

The design will begin by first choosing an appropriate cascode device size. Then, a distributed amplifier with lumped elements must be designed. Next, the lumped elements in the circuit will be replaced by microstrip equivalents. Meanwhile, the bias and terminal matching circuitry will be considered. Finally, the circuit layout will take place using Philips ED02AH process rules.

4.2.2 Active Device Choice

An important consideration affecting the upper cutoff frequency of a MMIC is the precise size and geometry of the individual transistors. As a first step in the design process, the transistor style which provides the highest $f_{\max}$ is selected. After a careful study of transistors having 1 to 6 fingers with widths in the range $10\ \mu\text{m}$ to $200\ \mu\text{m}$, it was found that a $4 \times 15\ \mu\text{m}$ pHEMT represented the best choice. This device exhibits a $f_{\max}$ of 115 GHz. The DC operating point of the pHEMT is set for class A operation to obtain maximum possible linear voltage and power. Hence, the pHEMT is biased at $V_{\text{ds}} = 3\ \text{V}$ and $I_{\text{ds}} = 0.5I_{\text{DSS}}$. Its DC I-V curves are given in Figure 4.1, showing that $V_{\text{gs}} = -0.2\ \text{V}$ is required. The transconductance of a $4 \times 15\ \mu\text{m}$ pHEMT is 22 mS. The transconductance of one cascode gain cell in the DA will therefore be 22 mS. From evaluation of equation (3.57), the number N of sections for an ideal cascode DA with 8 dB power gain in a $50\ \Omega$ system is 4.6 can be obtained. Hence, a five-stage DA circuit is chosen.

A distributed amplifier can be treated as two artificial transmission lines, which are coupled by the transconductances of the transistors. For a cascode distributed amplifier, the cut-off frequencies of the artificial lines are dependent on the gain cell's input and

Figure 4.1: DC I-V curves for 4x15 μm pHEMT device.

output capacitances. Figure 4.2 shows the schematic diagram of one cascode cell. Both input and output impedances of this cell can be obtained using Libra tool, and the input capacitance may be calculated by the following equation:

$$C_{in} = \frac{-1}{\omega X_{in}} \quad (4.1)$$

where $Z_{in} = R_{in} + jX_{in}$. Output capacitance C_{out} is obtained in an identical manner.

Figure 4.2: The schematic diagram of one pHEMT cascode cell.

The input and output capacitance values for a cascode gain cell are shown in Figure 4.3.

Figure 4.3: C_{in} and C_{out} of a cascode cell in Figure 4.2.

The average value of the input capacitance C_{in} and output capacitance C_{out} are 0.09 pF and 0.03 pF, respectively. As can be seen, the capacitances are not constant with frequency due to the effect of C_{gd} . In addition, the output capacitance is relatively higher at low frequency due to the ω at denominator in equation for output capacitance calculation. Furthermore, the cell's output capacitance is somewhat smaller than its input capacitance. Hence, the cut-off frequency of the amplifier is dominated by the cell's input capacitance. The cut-off frequency f_c of an artificial transmission line may be calculated from

$$f_c = \frac{1}{\pi Z_o C_{in}} = 63 \text{ GHz} \quad (4.2)$$

with Z_o of both the gate and drain lines is set to 50 Ω . Thus, the cut-off frequency of this amplifier will also be approximately 63 GHz. Due to the varying Z_o of artificial transmission lines, the maximum amplifier operating frequency is no more than 86% of the cut-off frequency [32]. As a result, the operating frequency of the amplifier may be estimated to be 54 GHz before considering the losses in these artificial lines.

4.2.3 Lumped Element Design of A Cascode DA

To satisfy the requirement of the equal phase delay per section along the gate and drain line, and to obtain the same 50 Ω characteristic impedance for both lines, C_{in} should be required to be equal to C_{out} , and the inductance on the gate-line L_g should be equal to the inductance on the drain-line L_d . Therefore, a padding capacitance C_p is needed at the output of the pHEMT, whose value is $C_p = C_{in} - C_{out} = 0.06$ pF.

The characteristic impedances of the gate line and drain line represented by Z_{og} and Z_{od} , respectively, are equal to $50\ \Omega$. Hence, both L_g and L_d are obtained from

$$L_g = C_{in} Z_{og}^2 \quad (4.3)$$

$$L_d = (C_{out} + C_p) Z_{od}^2 \quad (4.4)$$

Substituting values of C_{in} , C_{out} and C_p into equation (4.3) and (4.4), lead to

$$L_g = L_d = 0.23\ \text{nH}$$

Finally, the schematic diagram of a conventional distributed amplifier with lumped elements is shown in Figure 4.4. The S-parameter simulation results are shown in Figure 4.5.

Figure 4.4: Schematic diagram of a conventional distributed amplifier.

Figure 4.5: S-parameters for cascode DA circuit using lumped elements.

It is seen the flat gain S_{21} is about 8 dB, with a 3 dB-bandwidth of 46 GHz, and the amplifier's unity gain bandwidth is 62.5 GHz. It is also evident from this figure that S_{21} drops rapidly at high frequency since there is increasing reflection from both the gate and drain artificial transmission lines. A loss compensation technique described in section 4.2.4 will be employed to improve high frequency performance of this amplifier. In addition, both input and output return loss are greater than 10 dB up to 58 GHz, at which point the image impedance of both artificial transmission lines differs significantly from $50\ \Omega$. As a result, the $50\ \Omega$ dummy terminal resistors can no longer provide good matching. To compensate for this, a resistor-capacitor network may be used instead of the simple resistor, as described later.

The output voltage swing of this circuit may be estimated as follows: The I_{DSS} of a $60\text{ }\mu\text{m}$ HEMT is 13 mA. Since the operation point of all devices is located at $0.5I_{DSS}$, the maximum current swing should be around 13 mA, and the peak current is 6.5 mA. For a five-section DA, the total peak current is about 32.5 mA. Hence, the peak voltage is 1.6 V for 50Ω system. Finally, the output voltage swing of the cascode DA is approximately $3.2 V_{pk-pk}$.

4.2.4 Microstrip Design for A Cascode Distributed Amplifier

The inductors in the lumped element design are now realized by “electrically short” high impedance microstrip lines. To consider the microstrip to be electrically short, its length must be less than $\lambda/7$ (where λ is the wavelength in the microstrip line) at the highest frequency of operation [31]. The equivalent circuit of a short, lossless microstrip line is shown in Figure 4.6, consisting of an inductance with two shunt end capacitances.

Figure 4.6: A short length of microstrip line and its equivalent circuit [2].

For short microstrip lengths, the inductance and shunt end capacitances can be calculated as the follows.

$$L = \frac{Z_o l \sqrt{\epsilon_{eff}}}{c} \quad (4.5)$$

$$C = \frac{l \sqrt{\epsilon_{eff}}}{2Z_o c} \quad (4.6)$$

where l is the length of the microstrip, Z_o is the characteristic impedance, c is the velocity in free space and ϵ_{eff} is the effective dielectric constant for the microstrip.

The microstrip has series inductance as well as shunt capacitance, so the total capacitance of the artificial transmission line of the distributed amplifier is increased, resulting in lower bandwidth than that based on ideal inductors. To minimize the reduction of the amplifier bandwidth, a narrow microstrip is chosen to obtain the highest possible inductance with small shunt capacitance. Therefore, the characteristic impedance Z_o should be high.

Different widths for the drain and gate microstrip lines are chosen in this amplifier design for the following reason. The five-section distributed amplifier consumes high current on the drain line, but much lower current on the gate line. Considering the current capacity of microstrip in the ED02AH process, $10 \mu m$ and $20 \mu m$ are the minimum width microstrips chosen to implement the inductors on the gate and drain lines, respectively. Given the $100 \mu m$ GaAs substrate thickness, their characteristic impedances are 94Ω and 80Ω , respectively. The length of the microstrip can now be derived from equation (4.6). Leading to $280 \mu m$ and $320 \mu m$ as the required gain- and drain-lines lengths, respec-

tively, to achieve 0.23 nH inductance. The corresponding parasitic shunt end capacitances are 0.014 pF and 0.019 pF, respectively. The total parasitic capacitance is therefore twice these values. Since the parasitic capacitance value on the drain line (20 μm microstrip width) is larger than for the gate line (10 μm microstrip width), the additional shunt capacitance C_p on the drain line may be reduced by approximately 0.01 pF.

A short length of 20 μm width microstrip (L_{dd}) is added between the drain of the common gate pHEMT and the drain line to implement the small shunt capacitance C_p , and to improve the amplifier's high frequency response. This short microstrip will generate a small inductance, which results in a higher gain bandwidth product, as will be shown in section 4.2.6. The schematic diagram of the microstrip-implemented cascode distributed amplifier is shown in Figure 4.7.

The gain of the amplifier diminishes at high frequency due to reflection and loss effects on the gate and drain artificial transmission lines. In order to obtain a flat gain and high stability over a wide bandwidth, the loss compensation techniques shown in Figure 4.7 is utilized in the cascode DA configuration. First, L_{gate} , C_{gate} and R_{gate} are added to connect the gate of common gate pHEMTs (CGF) to ground [36]. Second, a short microstrip L_s is employed to connect the source of common source pHEMTs (CSF) to ground [36]. Third, a microstrip L_{sd} is added between the source of CGF and the drain of the CSF [37]. The characteristic of all these added components will be discussed in the next section.

Figure 4.7: The schematic diagram of the cascode distributed amplifier.

4.2.5 Bias and Terminal Matching Circuitry

In the cascode DA design, the V_{g1} and V_d DC biases can be applied to the HEMT's through the gate- and drain-line terminals to reduce chip size, as shown in Figure 4.7. Meanwhile, a separate bias line for V_{g2} is provided for the gate of CGF transistors.

To achieve impedance matching over a broad bandwidth, the terminal impedance must be transformed into the artificial line image impedance. Otherwise, the gain response of the amplifier will be not flat. We know from Chapter 3 Figure 3.7 that both the gate and drain image impedances decrease with frequency. Therefore, a frequency dependent impedance matching circuitry composed of RC networks is employed at the gate line and drain line dummy terminals, respectively. The gate line termination consists of three resistors and a capacitor to realize a lower impedance at high frequency to correspond with the image impedance trend. This kind of matching circuitry can obtain a flat gain and good matching characteristic over wide bandwidth [38].

At the drain dummy terminal, two series resistors with two resistors shunted to ground via capacitors form the matching and bias circuitry. Each RC shunt network with the series resistors absorbs unwanted signal over a different frequency range, and the drain line terminating impedance is designed to decrease with increasing frequency. The two series resistors alone match the line impedance at low frequency [39].

4.2.6 Circuit Optimization

From the analysis in chapter 3, the cascode cell has increasing negative output resistance with frequency. This negative resistance, on the one hand, can increase ampli-

fier gain at high frequency by reducing the effect of transmission line loss; on the other hand, large negative resistance may cause gain ripple and circuit instability. The loss compensation technique is utilized here to optimize the circuit. This technique in the practical circuit shown in Figure 4.7 includes five additional elements, L_{gate} , R_{gate} , C_{gate} , L_{sd} and L_s . Careful design using these elements can control the negative resistance effect and optimize the circuit. The equivalent circuit of one cascode cell encompassing the additional elements is shown in Figure 4.8.

Figure 4.8: The equivalent circuit of one cascode cell with L_{gate} , C_{gate} , R_{gate} , L_{sd} and L_s .

The output impedance of the cascode cell may be expressed as:

$$Z_{out} = \frac{[Z_{ds1} + j\omega(L_{sd} + L_s)][Z_{gs2} + R_{gate} + j(\omega L_{gate} - 1/\omega C_{gate})]}{Z_{ds1} + j\omega(L_{sd} + L_s) + Z_{gs2} + R_{gate} + j(\omega L_{gate} - 1/\omega C_{gate})} \cdot (1 + g_{m2}Z_{ds2}) + Z_{ds2} \quad (4.7)$$

and the negative resistance is modified from equation (3.66) to be

$$R'_{nr} = \frac{X'_1 X'_2 (R'_1 + R'_2)(1 + g_{m2}R_3)}{(R'_1 + R'_2)^2 + (X'_1 + X'_2)^2} \quad (4.8)$$

where

$$\begin{aligned} R'_1 &= R_1 \\ X'_1 &= X_1 - \omega L_{sd} - \omega L_s \\ R'_2 &= R_2 + R_{gate} \\ X'_2 &= \frac{X_2 / (\omega C_{gate})}{X_2 + 1 / (\omega C_{gate})} - \omega L_{gate} \end{aligned} \quad (4.9)$$

The functions of the inserted L_{gate} , C_{gate} , R_{gate} , L_{sd} and L_s are discussed below.

1) Effect of L_{gate} :

When L_{gate} is inserted, the term X'_2 is reduced in equation (4.9), which results in increased negative resistance R'_{nr} in equation (4.8). Therefore, the amplifier gain at high frequency can be improved. However, the stability of the amplifier is reduced correspondingly. Figure 4.9(a) shows the gain and the stability factor vs. frequency with and without L_{gate} , where the L_{gate} is realized with a 20 μm length of microstrip line. In this simulation, L_{gate} increases the gain by 1.5 dB at 50 GHz, but the k-factor is reduced.

2) Effect of R_{gate} :

When a small resistor R_{gate} is inserted, from equation (4.9), R_2' is increased to result in lower negative resistance R_{nr}' . Therefore, the stability of the amplifier is increased; on the other hand, the gain at high frequency is reduced. The simulation results are shown in Figure 4.9(b). When R_{gate} is equal to zero and the other parameters are given practical values, a gain ripple at high frequency appears, and the k-factor of the amplifier is below one, which results in instability of the circuit. If a 15 Ω resistor is inserted, the gain ripple of the circuit is cancelled. Correspondingly, the k-factor is increased and the circuit becomes stable.

3) Effect of C_{gate} :

A small capacitor C_{gate} is inserted to adjust negative resistance as well as provide DC blocking. Since C_{gate} is in series with C_{gs2} in Figure 4.9, the term X_2' in equation (4.9) is decreased. So the negative resistance R_{nr}' increases with C_{gate} . Figure 4.9(c) shows the simulation result. A gain ripple appears and the k-factor is below one for C_{gate} larger than 1 pF. When C_{gate} is reduced to 0.3 pF, the gain tends to flatten and the amplifier becomes stable.

4) Effect of L_{sd} :

Since the value of X_1 in equation (4.9) is relatively small, the insertion of L_{sd} changes the X_1' term to a negative value. Therefore, the resistance R_{nr}' in equation (4.8) may become positive, and the amplifier becomes stable. The simulation results are

shown in Figure 4.9 (d). When a $100\ \mu m$ microstrip L_{sd} is inserted, the stability of the amplifier is increased and a flatter gain response is obtained.

5) Effect of L_s

When a short microstrip L_s is inserted, X_1' turns negative for the same reason as with L_{sd} . So the stability of the circuit is increased, and the gain at high frequency is reduced, as shown in Figure 4.9 (e).

As mentioned earlier, the insertion of L_{dd} between the gain cell and the output line is beneficial to the high frequency response. The effect of this element, as obtained from simulation only, is given in Figure 4.9(f).

In conclusion, the above six factors can be adjusted to control negative resistance of the amplifier and improve gain flat and circuit stability at high frequency.

Figure 4.9: Effect of the inserted L_{gate} , R_{gate} , C_{gate} , L_{sd} , L_s and L_{dd} .

Figure 4.9: Effect of the inserted L_{gate} , C_{gate} , R_{gate} , L_{sd} , L_s and L_{dd} .

4.2.7 MMIC Implementation

The cascode DA circuit may now be implemented in MMIC technology using the Philips ED02AH process. During the layout phase, the design is modified again and again to reflect the circuit layout. The final MMIC layout of the cascode DA is shown in Figure 4.10. Each component of the layout is discussed below.

Figure 4.10: MMIC layout of the cascode DA.

HEMT layout: Figure 4.11 shows the layout of the $60\text{ }\mu\text{m}$ HEMTs found in Figure 4.10. This multifinger device structure includes four identical standard HEMT cells. The standard cells are placed side-by-side so that the ohmic contacts of adjacent HEMTs touch. Each cell has a gate width and length of $15\text{ }\mu\text{m}$ by $0.2\text{ }\mu\text{m}$. The gate resistance is

the parallel combination of the four gate strips, providing a lower resistance compared to one long gate strip. Another advantage of this arrangement is that the four HEMT cells share common drain and source terminals so as to provide good area efficiency.

Figure 4.11: Layout of a 60 μm wide pHEMT.

Passive elements: Two types of Metal-Insulator-Metal (MIM) capacitors are available in the ED02AH process. One uses a single Si_3N_4 layer, and another uses a double Si_3N_4 and SiO_2 layer. The Si_3N_4 MIM type is chosen for the larger coupling capacitors at the input, output and terminal circuits, where the precise value is not important. The $\text{Si}_3\text{N}_4 + \text{SiO}_2$ MIM capacitor is employed for RF grounding at the gate of the CGF, since this type of capacitor provides greatest accuracy for small capacitance values. Two types of resistors are employed in the ED02AH process. One uses the GaAs active layer for large resistance values and another uses a thin film metal layer (NiCr) for small values. The

GaAs resistors are chosen for the gate DC bias resistors of the CGF. In addition, since a large current flows on the drain line, and there is a $0.2 \text{ mA}/\mu\text{m}$ width current capacity limitation for the thin film resistor, the two series drain terminal resistors are laid out as GaAs resistors. Other small resistors are realized using thin film resistors.

Interconnects: The gate artificial transmission line interconnects the gates of all common source HEMTs. It is designed as narrow as the design rules allow so as to primarily work as an inductance. Since the associated shunt capacitance reduces the cut-off frequency of the circuit, the narrow microstrip keep this parasitic to a minimum. The drain artificial transmission line interconnects the drains of all common gate HEMTs. The width of drain line is limited by its current capacity. To achieve the minimum chip size, a meander structure is necessary for both gate and drain lines. Normally, tight bends such as square bends or mitered bends have more parasitics than circular bends with large radii. However, the circular bend cannot be realized by the Philips ED02AH process. Hence, a microstrip discontinuity structure is used in the transmission line design. In the cascode DA circuit, two- side chamfered bends are employed to realize the non 90° angle geometries.

Overall circuit layout: All sources of CSFs are connected to a common ground bus that is located close to the gate line. Between each HEMT is a via hole that provides a ground connection for all CSF source contacts. Separate bias pads are provided for the gate bias of CSF, and the gate and drain bias for the CGF, which are correspondingly represented by V_{g1} , V_{g2} and V_d in Figure 4.10. The cross-over of different metal layers is isolated by dielectric layers and an air bridge to reduce the parasitic capacitance. Since the

gate and drain lines do not extend to the edge of the chip, short $50\ \Omega$ microstrip lines are provided for the input and output.

EM simulation: Electromagnetic (EM) simulation is important for MMIC applications above K band, especially for the sections of transmission line containing discontinuities, because HP-EEsof Libra uses lumped element models to represent them. At low microwave frequencies, such models are relatively accurate, but at high frequency they are suspicious. The EM simulation was carried out with HP-EEsof's Momentum tool. In the cascode DA circuit, the EM simulations were done for both the gate and drain lines, since these lines include many discontinuities and coupling effects. In addition, capacitors with more connecting ports than given in the ED02AH library were handled by EM simulation. All of the above EM simulation results were put in the overall circuit simulation as S - parameter blocks.

The final layout size of the cascode DA is 2.1 mm x 1.0 mm. The simulation results for the final circuit as laid out are shown in Figure 4.12. The gain (S_{21}) is 8 dB with a 3 dB bandwidth of 50 GHz. The gain variation is within 1 dB up to 43 GHz. The input and output return losses are greater than 10 dB up to about 40 GHz. The total DC power dissipation is 0.35 W (6 V x 59 mA).

Figure 4.12: Simulated S-parameters of the cascode distributed amplifier.

4.3 Design of a Matrix Distributed Amplifier

4.3.1 Matrix DA Design Objectives

Similarly to the cascode DA design, the matrix DA driver is fabricated using the Philips process, GaAs 0.2 μm pHEMT technology. The available chip area is approximately $2.2 \times 1.0 \text{ mm}^2$. Within this context, the specifications for the matrix DA are as follows: the amplifier's bandwidth is limited to 40 GHz for applications in a OC768 optical transmitter system, with the low-frequency cutoff extending as low as possible with on-chip capacitors. The circuit is to be realized in a coplanar waveguide regime for this separate foundry access. Meanwhile, the driver amplifier's power gain will be made as high as possible. As before, both input and output return losses of the amplifier should be greater than 10 dB in a 50 Ω system, and the output voltage swing is to be maximized.

To satisfy this driver specification, an active device should be chosen first. Then, a matrix DA with lumped elements must be designed. Next, the lumped elements in the circuit will be replaced by CPW equivalents. Meanwhile, the bias and terminal matching circuitry will be considered. Finally, the circuit layout will take place using Philips ED02AH process rules.

4.3.2 Active Device Choice

The basic matrix DA structure is shown in Figure 4.13. To achieve a 40 GHz bandwidth amplifier, a two-row matrix DA configuration with single common source (CS) transistors used as the gain cells is considered. Capacitive coupling is employed in the upper

tier. As has been explained in the cascode DA design, the cut-off frequency of the artificial transmission lines employed must be approximately equal to $f_{\max}/0.86 = 47$ GHz. Therefore, the input capacitance of each gain cell is obtained from equation (4.2) as $C_{\text{in}} = 0.128$ pF. To satisfy this value, a transistor with $4 \times 20 \mu\text{m}$ gate width is chosen. In addition, the DC point of this pHEMT is set for class A operation to obtain maximum possible linear voltage and power. The average output capacitance of a CS gain cell was found to be 0.06 pF.

Figure 4.13: Schematic diagram of the matrix distributed amplifier by lumped elements.

A capacitive coupling technique is employed in the design so that large devices in the output row can be utilized to obtain higher output power. Obviously, a gain ripple appears at high end frequencies. A compensation technique is used in this matrix distributed amplifier as explained later. The largest possible device that can be used is $120\ \mu\text{m}$ to keep its output capacitance within the $0.128\ \text{pF}$ limit required for the artificial transmission line. Thus a $4 \times 30\ \mu\text{m}$ pHEMT is chosen for the gain cells in the upper row. Its input capacitance is $0.18\ \text{pF}$ but will be effectively less with the capacitive coupling technique.

4.3.3 Lumped Element Design for A Matrix DA

The matrix amplifier, assuming a unilateral HEMT model, can be represented by the small signal equivalent circuit shown in Figure 4.14. Since this is a two tier design, the matrix amplifier consists of three artificial transmission lines: gate line, central line, and drain line. These three lines are required to have the same cut-off frequency to obtain the same phase velocity. The characteristic impedances of the gate, central and drain lines are represented by Z_{og} , Z_{oc} and Z_{od} , respectively. The cutoff frequency f_c of each artificial transmission line is limited by the periodic shunt capacitance loading the transmission lines and the characteristic impedances. Ignoring the gate resistance R_{gs1} and R_{gs2} , the capacitive values on the three transmission lines are as follows:

$$\begin{aligned} C_{\text{gateline}} &= C_{gs1} = 0.12\ \text{pF} \\ C_{\text{centralline}} &= C_{ds1} + C_{gs2} = 0.24\ \text{pF} \\ C_{\text{drainline}} &= C_{ds2} = 0.12\ \text{pF} \end{aligned} \tag{4.10}$$

It is seen that the capacitance value on the central line is larger than that on the other two, and is the dominant limitation to the bandwidth of the matrix amplifier. At 0.24

pF the amplifier's bandwidth would fall below 40 GHz; thus, the capacitive coupling technique is employed here. To maximize power gain while reducing total power consumption and chip area, the characteristic impedance of the central transmission line is chosen to be 40Ω . $C_{\text{centralline}}$ from equation (4.2) should therefore be 0.15 pF. To realize this capacitance value, one series capacitor $C_{\text{gate}} (= qC_{\text{gs2}})$ with 0.18 pF value is inserted to connect the gate of the HEMTs on the output row to the center line. The HEMTs on the upper row can now be considered as a modified device having an effective capacitance of $C'_{\text{gs2}} = qC_{\text{gs2}}/(1+q)$ and an effective transconductance of $g'_{m2} = qg_{m2}/(1+q)$ [40]. Thus, the total periodic capacitance with C_{gate} included is $C'_{\text{centralline}} = C'_{\text{gs2}} + C_{\text{ds1}} = 0.15$ pF, which enables a bandwidth of over 40 GHz. Another advantage of this technique is that it can DC isolate the two tiers.

The lumped inductances on the gate and drain lines can be calculated from equation (4.3), and are equal to 0.3 nH. The series inductance on the center line will be 0.24 nH.

Given that the same area is available as for the cascode DA, the matrix DA will employ the same number of gain cells (5) on each of its two tiers. As stated earlier, $80 \mu\text{m}$ and $120 \mu\text{m}$ pHEMTs are the devices used on the first and second row of the matrix amplifier, respectively. Since $G_{m1} = 30$ mS for $80 \mu\text{m}$ HEMTs, $G_{m2} = 45$ mS for $120 \mu\text{m}$ HEMTs, $Z_{\text{og}} = Z_{\text{od}} = 50 \Omega$, $Z_{\text{oc}} = 40 \Omega$ and $R_{\text{ds}} = 337 \Omega$ for $80 \mu\text{m}$ HEMTs, equation (3.67) may be used to obtain a power gain for the ideal matrix amplifier of approximated 11 dB.

Figure 4.14: Small signal equivalent circuit of the matrix distributed amplifier.

From the schematic diagram in Figure 4.13, a short transmission line L_s ($20 \mu m$) is inserted between the HEMT sources and ground to improve the high end gain flatness.

The simulation results are shown in Figure 4.15. The matrix amplifier has 10 dB gain over a 45 GHz, 3 dB bandwidth. The S_{11} and S_{22} magnitudes are less than -10 dB over 40 GHz with the addition of a resistor-capacitor network at the artificial transmission line terminals (discussed in section 4.2.4).

Figure 4.15: Simulation results of the matrix distributed amplifier.

The maximum output voltage swing of this circuit may be estimated as follows:

The I_{DSS} of a $120\ \mu m$ HEMT is 26 mA. Since the operation point of all devices is located at $0.5I_{DSS}$, the maximum current swing should be around 26 mA, and the peak current is 13 mA. For a five - section DA, the total peak current is about 65 mA. Hence, the peak voltage is 3.2 V for $50\ \Omega$ system. Finally, the maximum output voltage swing of the matrix DA is approximately $6.4\ V_{pk-pk}$.

4.3.4 Coplanar Waveguide Design for A Matrix Distributed Amplifier

Coplanar waveguide is chosen as the propagation medium for the matrix distributed amplifier. Compared with microstrip, CPW has the advantages of lower dispersion,

lower radiation losses, lower substrate thickness sensitivity, lower inductance and easier ground plane access.

Similarly to microstrip, to obtain high inductance with minimal parasitic shunt capacitance, the characteristic impedance Z_0 of the CPW should be high. The characteristic impedance of a CPW line can be approximated by [41]

$$Z_0 = \frac{30\pi}{\sqrt{\epsilon_{eff}}} \frac{K'(k)}{K(k)} \quad (4.11)$$

where $\epsilon_{eff} = (\epsilon_r + 1)/2$, $k = W/D$,

W is the signal line width, D is the ground spacing, ϵ_r is the dielectric constant of the substrate ($\epsilon_r = 12.9$ for GaAs substrate); $K(\cdot)$ and $K'(\cdot)$ are the complete elliptic integral of the first kind and its complement, respectively.

For a given substrate, the characteristic impedance Z_0 is only controlled by the parameter k . Because equation (4.11) is a monotonically decreasing function of k , a high Z_0 may be realized by decreasing W or increasing D . However, W can not be too small, since it is limited by the current capacity, fabrication tolerance, and conductor loss. On the other hand, D can not exceed $\lambda/4$ in order to avoid spurious modes, and a large D may also lead to large discontinuities and chip size. Therefore, 65Ω , 54Ω and 54Ω characteristic impedance of the CPW are chosen for the gate line, center line and drain line, respectively. That leads to $W = 10 \mu m$ and $D = 50 \mu m$ for the gate line, $W = 20 \mu m$ and $D = 60 \mu m$ for the center and drain lines. A wider strip is needed on the center and drain lines to satisfy

current tolerances. The schematic diagram of the matrix distributed amplifier showing CPW sections is given in Figure 4.16.

4.3.5 Bias and Terminal Matching Circuitry

Similarly to the cascode distributed amplifier, the DC bias may be applied to the HEMT's through the gate-, center- and drain-line terminations for minimum chip size. In addition, a series biasing is provided through large resistors for the gates of the output row devices.

To achieve broad band impedance matching, a frequency dependent terminating network composed of RC elements is utilized at the gate line, center line and drain line terminals. This kind of circuitry realizes a lower impedance at high frequency, as required.

4.3.6 Circuit Optimization

As discussed earlier, the broad bandwidth of the amplifier is achieved by reducing the input capacitance of the HEMTs on the second row.

Although the DA circuit structure is now fixed, it is important to mention that there are two design techniques to reduce this input capacitance: 1) using capacitive coupling, and 2) using device scaling (smaller device). The capacitive coupling technique causes the input capacitance of the HEMT to be in series with a coupling capacitor so as to reduce the input capacitance, and increase the bandwidth of the amplifier. However, the coupling

Figure 4.16: Schematic diagram of the matrix distributed amplifier.

capacitor creates a voltage division at the gate input, and results in a loss of gain. This requires more device periphery to make up for the lost gain. On the other hand, if the device scaling technique is used, the transistors in the amplifier are scaled to an appropriately small size to obtain a low input capacitance. In the present matrix DA configuration, the coupling capacitive technique was utilized, because a large device periphery improves the 1 dB power compression point of the amplifier and produces higher output voltage. In addition, the output shunt resistance is increased by the large periphery to reduce the attenuation on the output artificial line.

A gain ripple appears at high end frequencies which may be controlled with a short transmission line inserted between the source of devices and ground. The inductance of these short lines forms a negative feedback and results in flatter gain. Figure 4.17 shows the gain flattening effect due to L_s . It is clear that the gain ripple of the matrix DA is improved at the high end of the frequency response. However, the amplifier bandwidth is somewhat reduced, depending on the length of the short lines. Such a gain ripple control technique does not appear to have been previously employed in the literature.

This 2x5 matrix DA includes three artificial transmission lines. Both the input and output lines are terminated by the 50 Ω system impedance. However, the termination of the center line need not be constrained to 50 Ω . Here it is set to 40 Ω to reduce DC power dissipation and chip size, as discussed earlier. This however causes a slight reduction in the gain of the amplifier.

Overall, the matrix DA configuration is rather flexible. Proper synthesis of the above techniques can lead to good bandwidth and gain characteristics for the amplifier.

Figure 4.17: Simulated gain profile with and without L_s (length = $10\ \mu m$).

4.3.7 MMIC Implementation

The matrix DA circuit is implemented in MMIC technology according to the Philips ED02AH process. The circuit layout is shown in Figure 4.18.

Many of the layout features are the same as for the previous cascode DA design and are not repeated here.

Air bridges are used to connect the two CPW ground planes for suppression of the undesired CPW even mode. These bridges were primarily placed at the discontinuities. A $50\ \Omega$ CPW was employed at the amplifier input and output to reach the edge of the chip. Separate bias pads were provided for the gate- and drain-bias of the input and output row HEMTs, respectively, that are correspondingly represented by V_{g1} , V_{g2} , V_{d1} and V_{d2} . EM simulation was done for the gate- and drain-lines as well as for non-standard MIM capacitors. All of the EM simulation results were included in the complete circuit simulation.

Figure 4.18: MMIC layout of the 2x5 matrix DA.

The final size of the matrix DA is 2.2 mm x 1.0 mm. The simulation results for the final circuit as laid out are shown in Figure 4.19. The gain (S21) is 10 dB with a 3 dB bandwidth of 41 GHz. The gain variation is within 1 dB up to 36 GHz. The input and output return losses are greater than 10 dB to beyond 40 GHz, with some degradation at low frequency due to the finite capacitor values in the frequency dependent terminations. The total DC power dissipation is 0.72 W (3 V x 240 mA).

Figure 4.19: Simulated S-parameters of matrix distributed amplifier.

4.4 Evaluation of Cascode and Matrix Distributed Amplifiers

This chapter has shown that both the cascode and matrix DA configurations may be designed to meet the wide bandwidth requirements of an optical modulator driver. Their performance characteristics are summarized in Table 4.1.

Table 4.1: Performance of the cascode and matrix distributed amplifiers

Topology	Gain (dB)	Bandwidth (GHz)	Output voltage swing (V)	DC Power (W)	Area (mm ²)
Cascode DA	8	0.5-53	3.0V	0.35	2.1x1.0
Matrix DA	10	0.5-41	6.4V	0.72	2.2x1.0

The cascode DA has several advantages over the matrix DA. First, the cascode DA has a large shunt output resistance, which reduces the loss on the drain line, and thus expands the bandwidth of the amplifier (see section 3.3.2). Secondly, the cascode DA has small feedback capacitance, which allows a greater bandwidth to be achieved than with the matrix topology. Thirdly, the cascode DA has lower DC power dissipation than the matrix DA, since the latter dissipates significant DC power in the center line termination. However, the chip size for these two types of DA is almost identical.

On the other hand, the matrix DA also has several advantages over the cascode DA. First, the matrix DA configuration is inherently more stable than the cascode DA, because the cascode topology exhibits negative resistance that may result in amplifier instability at the high end frequencies. Although several techniques may be employed to ensure stability, the design of a cascode distributed amplifier requires more care at this level. Secondly, the number of stages in a cascode DA is limited by the loss on the gate- and drain- lines, and thus results in a gain limitation. The matrix topology may overcome this limitation, since the amplifier gain will be increased with the use of additional tiers.

Chapter 5. Experimental Results

5.1 Introduction

This chapter presents test results of the cascode distributed amplifier designed in Chapter 4. The matrix DA has not been tested due to delay in fabrication. The test setup used in the measurement of the electrical performance of the cascode distributed amplifier is first described. Then, the measured S-Parameters, 1dB gain-compression point, output voltage swing and group delay are given. Finally, deviations between measured results and predicted values are explained.

5.2 Measurement Setup

A probe station is employed for the MMIC measurement to secure the chip in place and to provide a stable means of electrically connecting it to the measurement apparatus.

5.2.1 S-parameter Measurement Setup

A network analyzer was used to perform the S-parameter measurements. The measurement apparatus consisted of an HP8510C network analyzer, cabling and probes. The network analyzer is capable of accurately extracting the S-Parameters of the device over the 45 MHz to 65 GHz frequency band. The HP8510C was calibrated up to the probe tips with a OSLT (Open, Short, Load, Through) calibration method. Coplanar waveguide probes with V-connectors were utilized for the RF signals. Such probes provide an

extremely good $50\ \Omega$ characteristic impedance up to the contacting tips, thus minimizing parasitic reflections and mismatching to the device under test (DUT). In addition, six pin DC probes are employed for DC bias. The test setup is shown in Figure 5.1.

Figure 5.1: Test setup for S-parameters measurement.

5.2.2 Output Power Measurement Setup

The output power measurement setup included a Wiltron synthesized sweeper that generates a large RF signal over 10 MHz to 40 GHz. Because of the limited generator signal power and the significant coaxial cable losses at 40 GHz, an extra power amplifier was added to provide increased power at 40 GHz. An HP8565 Spectrum Analyzer was used to measure the output power. Two directional couplers, one with 20 dB coupling and the other with 10 dB coupling, were employed to sense the incident and reflected powers at the amplifier input. The complete output power measurement setup is shown in Figure 5.2.

The power meters were calibrated before testing for accurate measurement. Therefore, the input power to the DUT is the incident power minus both the reflected power and the loss between coupler and DUT. The output power is that power read on the Spectrum Analyzer plus the cable loss between the analyzer and DUT.

Figure 5.2: Power measurement setup.

5.3 Distributed Amplifier Measurements

The fabricated 5- stage cascode distributed MMIC amplifier is shown in Figure 5.3. All the testing was carried out on the 4" wafer at the Communication Research Centre (CRC) in Ottawa.

Figure 5.3: Microphotograph of the cascode distributed amplifier (2.1 mm x 1.0 mm).

5.3.1 S-Parameters of the Distributed Amplifier

The measured S-parameter magnitudes of the cascode distributed amplifier are shown in Figure 5.4. Figure 5.5 to 5.7 combine the simulated and measured results for each S-parameter.

It can be seen from Figure 5.5 that the measured gain is approximately 2 dB lower than expected at 0.5 GHz, but is in very close agreement with the simulated results between 5 GHz and 45 GHz. The 3 dB bandwidth of the gain response is about 53.5 GHz, which is over 3 GHz wider than that of the simulation results. However, the variation of measured gain is ± 1 dB, which is larger than ± 0.5 dB variation in simulation.

Figure 5.4: Frequency characteristics of the distributed amplifier on-chip measurement.

Figure 5.5: Comparison between simulated and measured S_{21} of the cascode distributed amplifier at $V_d = 3$ V and $V_g = -0.2$ V.

Figure 5.6: Comparison between simulated and measured S_{11} of the cascode distributed amplifier at $V_d=3V$ and $V_g=-0.2V$.

Figure 5.7: Comparison between simulated and measured S_{22} of the cascode distributed amplifier at $V_d=3V$ and $V_g=-0.2V$.

Both the measured S_{11} and S_{22} results are similar to the simulated results, as seen in Figure 5.6 and 5.7, respectively. Some difference appears at low frequency for both parameters and around 35 GHz for the S_{22} parameter.

5.3.2 Explanation of Measurement Results

Figure 5.5 shows that the measured amplifier exhibits lower than expected power gain at low frequency. A partial explanation for their difference is that one of the 25Ω series resistor at the drain terminal was actually laid out to be a 20Ω resistor. Subsequent simulations showed a 1 dB drop in gain due to this change. Another possible effect is the modeling accuracy of the three port capacitors used at gate line and drain line terminals, as well as at each common gate device. It is believed that the capacitance of these non-standard structures has been overestimated.

No common gate device model was available for the circuit design. Therefore, in this work, the common gate device model employed for the cascode gain cell was replaced by the common source device model with the gate grounded. Circuit performance may be different from the actual circuit implemented, especially high frequency. The measured S_{21} response shows a 3 dB bandwidth, which is about 3 GHz wider than the simulated results. Hence, future work should include further analysis and comparison of the performance between the common gate device model and the common source device with gate grounded model.

5.3.3 Frequency Response Effects Due to Bias

The effects of gate and drain bias on the S-parameters are illustrated in Figure 5.8 and 5.9, respectively. Gate bias voltages V_g of 0 V, -0.1 V and -0.2 V were selected in Figure 5.8, while the drain voltage V_d is set to 3 V.

Figure 5.8: Measured $|S_{21}|$ for Various Values of Gate Bias V_g for Cascode Distributed Amplifier at $V_d = 3$ V.

As can be seen, the gain is maximized by setting $V_g = 0$ V, and decreases with reverse bias. This is due to the higher transconductance of pHEMT at $V_g = 0$ V, which produces a higher DA gain. Furthermore, the 3 dB bandwidth is almost identical for the various gate bias values. The results of having a drain bias voltage of 2.5 V and 3 V are shown in Figure 5.9, with the gate bias V_g set to -0.2 V. A reduction in gain is observed with a decrease in drain bias. This may be explained by the fact that the higher drain bias voltage causes higher output resistance R_{ds} of the pHEMT. Thus the overall gain is increased through a reduction of the drain line losses (see section 3.3).

Figure 5.9: Measured $|S_{21}|$ for various values of drain bias V_d for cascode distributed amplifier at $V_g = -0.2$ V.

5.3.4 Group Delay

The group delay is desired to be kept low and constant through the driver amplifier pass band to the upper 3 dB frequency region, in order to minimize pulse distortion and timing jitter. The group delay of the cascode DA is shown in Figure 5.10 and is derived from measured S_{21} phase characteristic (with a frequency step of 0.5 GHz). The average group delay is about 45 ps, and deviations in group delay are approximately ± 10 ps up to 53 GHz.

Figure 5.10: Calculated group delay as a function of frequency from measured S-Parameter of the cascode DA at $V_d = 3$ V and $V_g = -0.2$ V.

5.3.5 1-dB Gain Compression

The 1-dB gain compression point is determined by measuring the output power as a function of the input power. The 1-dB gain compression point was obtained at four different frequencies: 10 GHz, 20 GHz, 30 GHz and 40 GHz. Figure 5.11 shows the output power vs. input power of the cascode DA at 20 GHz. The measured output power is about 13.54 dBm. Other output powers at 1 dB gain compression point shown in Figure 5.11 are 13.71 dBm, 13.58 dBm and 13.01 dBm, respectively.

Figure 5.11: Measured power performance of the cascode DA at 20 GHz for $V_g=-0.2$ V and $V_d=3$ V.

Figure 5.12: Measured 1-dB gain compression point for cascode DA at 10 GHz, 20 GHz, 30 GHz and 40 GHz.

5.3.6 Output Voltage Swing

Since the eye diagram of the driver amplifier has not been tested, the output voltage swing of the cascode distributed amplifier is calculated from output power values. Given the $50\ \Omega$ load impedance, the output voltage swings are 3.07 V, 3.01 V, 3.02 V and 2.83 V, respectively at 10 GHz, 20 GHz, 30 GHz and 40 GHz. This compares very well with the $3.2\ V_{pp}$ value estimated in Chapter 4.

5.3.7 Comparison with other Amplifiers in the literature

Generally, it is rather hard to compare the distributed amplifier performances in the literature, since the amplifier performance depends on transistor materials, gate length of FETs, transistor operating point, number of DA stages, and so on. Table 5.1 lists all amplifiers in the literature based on $0.2\ \mu m$ GaAs FET or HEMT technology, along with their main performance characteristics, for comparison with the results of this work.

Table 5.1. Performance of reported amplifier based on $0.2\ \mu m$ GaAs FET or HEMT.

Reference	Gain (dB)	Bandwidth (GHz)	Power dissipation (W)	Output voltage Swing (V)	Area (mm ²)
Cascode DA (Thesis)	8	0.5-53	0.35	3	2.1 x 1.0
Matrix DA (thesis, predicted)	10	0.5-41	0.72	6.4	2.2 x 1.0
[42]	20	6-12	not given	not given	not given
[43]	9	2-52	not given	not given	2 x 2.5
[44]	9	0-44	1	not given	1.5 x 2.5
[45]	not given	0-40	1	3	3 x 2.5
[46]	not given	0-40	1.6	2.9	1 x 1

It is seen that the cascode distributed amplifier developed in this thesis has the widest bandwidth ever reported using commercially available $0.2\mu m$ GaAs technology. In addition, the DC power dissipation is lowest, and the chip size is smaller. This superior performance is mainly attributable to the novel use of six elements (L_{gate} , C_{gate} , R_{gate} , L_{dd} , L_{sd} and L_s) for the loss compensation technique as opposed to at most four employed in previous designs. The predicted output voltage swing of the matrix DA in this thesis is the highest.

Chapter 6. Conclusions and Future Work

6.1 Summary

In this thesis, GaAs pHEMT based MMIC technology was investigated for potential use in a modulator driver applications. Two types of distributed amplifier, a conventional cascode design and a common source matrix design, have been implemented and evaluated.

In Chapter 1, a brief outline of the motivations, objectives, and organization of this thesis has been presented. A brief review of GaAs HEMTs and distributed amplifier technology is provided in Chapter 2. Performance comparisons of HEMTs to various other microwave transistors are also given in this chapter.

To help in the design of these amplifiers, expressions of the power gain and the artificial line's attenuations for pHEMT based DAs were derived in Chapter 3, which have been verified to yield relatively accurate performance predictions.

The detailed design flows for the cascode and matrix DAs are presented in Chapter 4. A cascode DA with 8 dB power gain and over 50 GHz band width was implemented. In this amplifier, a loss compensation technique was found and theoretically verified to optimize the circuit. This technique can expand the amplifier's bandwidth by overcoming the artificial line's loss with the negative resistance of the cascode gain cells. In addition, a 10 dB gain, 41 GHz bandwidth, matrix DA was designed and fabricated. In this amplifier, a gain ripple compensation technique was found to keep the amplifier's gain flat at high end

frequencies. Further, a capacitive coupling technique was employed to allow larger output power from the amplifier. A different transmission line width technique is utilized in both the cascode and matrix DA designs to improve the frequency response as well as reduce chip area.

Performance evaluations for the two types of DA topologies were also given in Chapter 4. The cascode DA has a broad bandwidth, lower artificial line attenuations, and lower DC power dissipation. On the other hand, the matrix DA can overcome the maximum output voltage swing limitation resulting from the use of small devices. In addition, this kind of circuit provides more design flexibility for simultaneously achieving large gain, stability and broad bandwidth.

The test results for the cascode distributed amplifier are presented in Chapter 5, and include measured S-parameters under various bias conditions, group delay, 1-dB gain-compression point and output voltage swing. The measured results were found to be in good agreement with the simulations, except for low frequency performance. Thus, the major objective for this distributed amplifier was accomplished.

The cascode distributed amplifier developed in this thesis has comparable or superior performance to other designs using a similar technology reported in the literature.

6.2 Future Work

This GaAs pHEMT based distributed amplifier was intended for optical modulator driver applications. More work could be done on improving amplifier performance. In

order to be completely applicable to next generation optical systems, the following suggestions are made.

- (a) To verify the common-gate pHEMT model, which is employed in a cascode cell distributed amplifier, so that the amplifier circuit modeling is more accurate at high frequencies.
- (b) To expand the driver amplifier's bandwidth above 65 GHz, a shorter gate length of pHEMT is needed. Currently, 0.15 μm GaAs-based HEMTs are widely employed to form driver amplifiers for 40 Gbps optical systems. Furthermore, the InP-based HEMT can be used instead of GaAs to obtain high circuit performance, since these devices have significantly improved transconductance and f_t , when compared with GaAs HEMT.
- (c) To achieve higher power and higher output voltage, the double heterojunction HEMTs can be utilized, because this type of device can result in a doubling of the sheet carrier concentration in the channel, thus increasing drain-source current for a given device width.
- (d) To obtain higher power gain of a distributed amplifier, more stages in the DA are required. Therefore, a larger circuit area would be needed.
- (e) To improve circuit performance, some new circuit topologies such as cascode cell matrix DAs should be considered and investigated.

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Appendix 1

Simplification of the equation (3.45) for distributed amplifier in section 3.3.3

The right hand summation term of equation (3.45) is

$$\sum_{k=1}^n \exp\{ -[(2k-1)\Upsilon_g l_g + (2n-2k+1)\Upsilon_d l_d]/2 \} \quad (\text{A1-1})$$

The constants are brought out of the summation

$$\exp(-n\Upsilon_d l_d) \exp[(\Upsilon_g l_g - \Upsilon_d l_d)/2] \sum_{k=1}^n \exp[k(\Upsilon_d l_d - \Upsilon_g l_g)] \quad (\text{A1-2})$$

The substitution $\Upsilon = \Upsilon_d l_d - \Upsilon_g l_g$ is submitted into (A1-2) to obtain

$$\exp(-n\Upsilon_d l_d) \exp(-\Upsilon/2) \sum_{k=1}^n \exp[k\Upsilon] \quad (\text{A1-3})$$

Both the numerator and denominator are multiplied by $\exp(\Upsilon) - \exp(-\Upsilon)$, so obtaining

$$\frac{\exp(-n\Upsilon_d l_d) \exp(-\Upsilon/2)}{\exp(\Upsilon) - \exp(-\Upsilon)} \left\{ \sum_{k=1}^n \exp[(k+1)\Upsilon] - \sum_{k=1}^n \exp[(k-1)\Upsilon] \right\} \quad (\text{A1-4})$$

after modifying the summation sign

$$\frac{\exp(-n\Upsilon_d l_d) \exp(-\Upsilon/2)}{\exp(\Upsilon) - \exp(-\Upsilon)} \left(\sum_{k=1}^{n-2} \exp[(k+1)\Upsilon] + \exp(n\Upsilon) + \exp[(n+1)\Upsilon] \right. \\ \left. - \sum_{k=1}^{n-2} \exp[(k+1)\Upsilon] - 1 - \exp(\Upsilon) \right)$$

(A1-5)

the above equation is simplified as

$$\frac{\exp(-n\Upsilon_d l_d) \exp(-\Upsilon/2) \exp(n\Upsilon/2) \exp(\Upsilon/2)}{\exp(\Upsilon) - \exp(-\Upsilon)} \{ [\exp(\Upsilon/2) + \exp(-\Upsilon/2)] [\exp(n\Upsilon/2) - \exp(-n\Upsilon/2)] \}$$

(A1-6)

then both the numerator and denominator are multiplied by $\exp(\Upsilon/2) - \exp(-\Upsilon/2)$, one obtains

$$\frac{\exp(-n\Upsilon_d l_d) \exp(n\Upsilon/2) [\exp(n\Upsilon/2) - \exp(-n\Upsilon/2)]}{\exp(\Upsilon/2) - \exp(-\Upsilon/2)}$$

(A1-7)

Using the mathematical identity

$$\sinh x = \frac{\exp(x) - \exp(-x)}{2}$$

(A1-8)

then, simplifies to

$$\exp[-n(\Upsilon_g l_g + \Upsilon_d l_d)/2] \frac{\sinh[n(\Upsilon_d l_d - \Upsilon_g l_g)/2]}{\sinh[(\Upsilon_d l_d - \Upsilon_g l_g)/2]}$$

(A1-9)