Analysis and Design of Switching DC/DC Converters

by

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Abstract

Present development trends in the area of high-power-density switching converters indicate a strong need for a new class of simulation tools which would allow for a complex approach to the problems of converter analysis and design. Such approach, besides a fast and accurate simulation of the converter switching waveforms, can include an overall analysis of converter behavior in response to changes of operating conditions, a search for extreme values of converter internal variables, a computation of power dissipated on particular devices, a calculation of the converter's efficiency, an ac analysis, a sensitivity analysis and a design optimization. Also, an integration with the other CAD tools, e.g. thermal simulators, is of particular interest.

In the order to better address today's needs of development and practical design, this thesis presents alternative simulation techniques which can be used for the efficient analysis of switching converters. This work is particularly focussed to the area of steady-state analysis. A novel method for determining converter steady-state is presented. A detailed analytical model of the active clamp reset forward converter with synchronous rectifiers is derived. Based on the both, the converter model and steady-state method, an efficient algorithm for simulation of converter switching waveforms is shown. Further, in sense of complex analysis of converter circuits, the "behavioral characterization" of switching converters is introduced and the simulation algorithm is expanded for an inspection of converter critical nodal variables over a large-scale variation of operating conditions such as input voltage, load current and device parameters.

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List of Symbols

T	switching period
f_{sw}	converter switching frequency
D	duty ratio
D'	complement of duty ratio to 1
$d, d(t)$	duty ratio function
V_g	converter input voltage
y, V_{out}	converter output voltage
X_{ss}	average value of the state vector
Y_{ss}	average value of converter output
CCM	continuous conduction mode of operation of switching converter
DCM	discontinuous conduction mode of operation of switching converter
ACR	active clamp reset
SR	synchronous rectifier

Chapter 1

Introduction

1.1. Problem Description

Recent advancements in the area of switching DC/DC converters have been motivated, first of all, by the needs of a new generation of high-speed VLSI chips for low supply voltage and high supply current. These needs introduce changes in architecture of both the particular converter circuit and that of overall power system. While before, a power system of typical telecommunication shelf equipment included a few high output power converters, it is now common to see these being replaced by tens of low output power converters called bricks or PUPS (point of use power supply). Typically, the PUPS converters have to be installed very close to the affiliated chip load while occupying minimum board space and dissipating a minimum amount of power. The PUPS converters have to deliver high currents, preferably in a maximum di/dt rate, while maintaining a tight output voltage regulation. All of this with the guarantee of full performance over a wide range of input-

voltage, load current, ambient conditions and device tolerances, high design reliability, minimum production cost and satisfaction of various environmental and safety standards.

For switching converter designers the variety of the resulting work is challenging. This concerns anything from a simple manufacturing support, through routine design, to research and development oriented to satisfy the demands for new converters, which come on almost a daily basis. Furthermore, the delivery of a product to market with minimum delay ("time to market") has become another important factor which affects the daily professional life of a switching converter designer.

In such a dynamic area, any means and tools which could make the work of switching converter designers more efficient are welcome. In the field of VLSI, the use of commercial simulators such as Spice and Saber for this purpose is crucial. Unfortunately, the experience from the area of switching converters however shows that the use of these tools is very often not straight forward and does not fully satisfy expectations when simulating a switching power circuit. Perhaps the most frequent complaints from switching converter designers in presence relate to the delays caused by the simulation set-up issues, simulation time itself, and problems with computational convergence. Furthermore, the user menu of commercial simulators is of limited use when the simulation object is a switching converter. This, for instance, concerns computation of efficiency, ac analysis and sensitivity analysis.

As the high power density switching converters move closer to the electronic circuitry, thermal behavior of the converter and that of the entire circuit board becomes an issue. Thus, the integration of electrical and thermal simulators becomes highly desirable. This would require further expansion of the commercial simulators in the area of thermal analysis.

In principle it is possible to use commercial simulators for the analysis of the behavior of switching converters. However the fundamental discrepancy between capabilities of commercial simulators and practical simulation needs is given by the both, a computational concept (numerical integration) and overall orientation (preferably to the area on VLSI design) of first named and a highly non-linear operation of the switching converters. Thus, a reliance on the use of commercial simulators for the simulation and analysis of switching power converters may not be the best choice for the future.

As demonstrated in the literature published over the past two decades, simulation algorithms based on analytical methods can greatly outperform commercial simulators. Using these methods, the simulation time can become substantially shorter and the accuracy of obtained results is acceptable. Typically, the state-space approach is applied to formulate the system equations. In literature, these methods are referred to as “fast time-domain” methods. The proficiency of these methods in terms of speed, accuracy and convergence used to be demonstrated by the simulation of converter start-up transient. To achieve steady-state in an even shorter simulation time, a special class of methods referred to as “methods with accelerated convergence into steady-state” can be found in the published literature. These methods, rather than providing a complete and accurate simulation of trajectory of converter internal variables during start-up, focus on minimizing the numbers of iterations performed by the algorithm (and therefore that of the overall computation time) used to achieve steady-state.

Key concerns raised by the analytical methods when applied to the area of switching converters are: the accuracy of models of the switching devices, the derivation of the state-space model for the converter circuit, and the possible convergence problems of the algorithms used. In spite of the difficulties, it seems that a substantial saving in terms of simulation time without sacrificing accuracy is critical and will act to drive research in the area of analytical simulation methods.

1.2. Thesis Objective

This thesis is oriented primarily towards the analysis of the operation of switching converters in steady-state. All of the steps in the development and design of switching converters beginning by the simple simulation of switching waveforms, through the overall characterization of converter variables over large range of input parameters, efficiency and thermal analysis and ending by an ac and sensitivity analysis, are based on the knowledge of converter steady-state. Thus, a search for a new method which determines converter steady-state most efficiently is the first goal of this work.

The active clamp reset forward (ACR) topology with synchronous rectifiers is one of the most popular topologies of switching converters at present. Since an analytical model of this topology has not yet been published, the derivation of an accurate model is the second goal of this work.

In the Fig. 1.1, a picture of the switching converter based on ACR forward topology with synchronous rectifiers is shown. The converter was designed for Nortel Networks and was considered as a leading product in its category at the time. The main tool used in its development were spreadsheet formulas and practically no simulation of the converter switching operation was done. Thus another target of this work is to provide an efficient mean of simulating a converter's switching waveforms.

In literature, typically, a performance of proposed simulation methods uses to be demonstrated showing either start-up trajectory or steady-state waveforms of one or two nodal variables of converter circuit in, typically, nominal operating point. Practical design would significantly benefit, however, from a more complex analysis which includes a characterization of all converter critical internal variables over a range of operating conditions. Due to the need for such analysis, the final goal of this work is to introduce the characterization

of a converter circuit over variations of the parameters such as input voltage, load current and device tolerance.

Fig. 1.1 A DC/DC PUPS converter (magnified 2:5).

1.3. Thesis Contribution

The scope of this work is broad. From the many topics which are dealt with, the most valuable achievements are:

- The derivation of a new steady-state method. In comparison with published analytical methods, the proposed method is more efficient in terms of speed, accuracy and convergence, making it suitable for a large class of switching power converter topologies.

- The derivation of a detailed state-space model of an active clamp reset forward topology with synchronous rectifiers based on real converter circuit.

- The development and implementation of an algorithm for simulation of the switching operation of a practical converter based on the proposed steady-state method and state-space model of the ACR forward converter with synchronous rectifiers. The results of this simulation are compared with the performance of a real converter. A significant agreement between the simulation and behavior of the real converter in steady-state is demonstrated.

- The introduction of the behavioral characterization of switching converters as a tool for converter analysis over large range of operating conditions. Behavioral characterization shows variations of critical internal nodal variables of converter in response to variations of input voltage, load current and device parameters. A simulation algorithm is developed to demonstrate and perform such as analysis on the ACR forward converter with synchronous rectifiers.

1.4. Outline of the Thesis

Chapter 2. Principles of Switching DC/DC Converters: basic terms used in area of switching power converters are explained.

Chapter 3. Time-Domain Analysis of Switching DC/DC Converters: principles, advantages and potential problems of the published methods for simulation of the operation of switching converters are discussed.

Chapter 4. A Novel Method for Computation of Steady-State Response of Switching DC/DC Converters: introduces and evaluates a novel method for computing the steady-state response of switching converter circuits.

Chapter 5. Analysis of Active Clamp Reset Forward Converter with Synchronous Rectifiers in Steady-State: introduces a detailed state-space model of the ACR forward converter with synchronous rectifiers. The model is then used with the steady-state algorithm proposed in Chapter 4. The switching waveforms for the converter in steady-state are simulated and compared with those obtained with a prototype.

Chapter 6. Behavioral Characterization of Switching Converters: introduces the behavioral characterization of switching converters. The need for such as characterization for design of switching converters is explained. The algorithm for the behavioral characterization is presented and implemented on the topology of the ACR forward converter with synchronous rectifiers.

Chapter 7. Conclusions: the results of the thesis are summarized and suggestions for further research are outlined.

Appendix A: procedure of derivation of a state-space model for ideal ACR forward converter with synchronous rectifiers is shown.

Appendix B: state-space model for real ACR forward converter with synchronous rectifiers is derived.

Appendix C: the output equation for the model of the real ACR forward converter with synchronous rectifiers is extended to include a series of the converter's critical internal variables.

Chapter 2

Principles of Switching DC/DC Converters

2.1. Basic Functional Blocks of Switching DC/DC Converters

A switching DC/DC power converter consists of several basic functional blocks: input filter, switching power stage, control, feedback circuit, and output secondary filter. A general block diagram of a switching DC/DC converter is shown in Fig. 2.1.

The core of a switching power converter is its power stage. The purpose of the power stage is to convert a dc voltage V_g to another dc voltage V_{out} . The power stage is built using semiconductor switching elements (typically diodes and transistors) and energy

storage elements (inductors, capacitors, transformers) and, in principle, can be divided further into functional units such as power train, output rectifier and output filter.

A direct consequence of the switching operation of the elements of the power stage is a generation of non-harmonic currents and voltages. Thus, it is normally necessary to include an input filter to reduce the magnitude of their harmonic components to an acceptable level. On the output of the converter, separate output filters (secondary output filters) are, in some applications, needed to further reduce the switching ripple and high-frequency noise.

To meet the specified requirements for output voltage, a feedback regulation loop is typically necessary. Its role is to compensate for changes in input voltage and load current providing requested overall dynamic response.

The switching elements in the power stage are controlled, primarily, by a signal $\delta(t)$ generated by the control block. The rising edge of this signal is synchronized with the internal clock signal. A comparator in the control block senses the signal V_{ea} from the feedback circuit and, depending on mode of control, compares it to either

Fig.2.1 General block diagram of DC/DC switching converter.

a signal from an internal independent ramp generator or a signal derived from the input current of the converter I_{sen} . The output of the comparator controls the falling edge of the signal $\delta(t)$. More details about the operation of DC/DC converters are provided in section 2.3.

2.2. Classification of Switching DC/DC Converters

Architectures of input and output filters and also those of feedback circuits may be common for many types of DC/DC converters. However, the way the power stage elements are connected can vary significantly and is specific for, so called, switching converter topology. Many different DC/DC converter topologies have been developed in the past and different criteria may be used for their classification.

Converter topologies such as boost, buck, buck-boost and sepic are commonly referred to as “basic non-isolated” topologies. All of these topologies involve one switching transistor and one or two inductors, and perform step-down, step-up, inversion, or a combination of these (e.g. inverted step-down). An example of a boost converter topology is provided in Fig.2.2.

“Isolated” converter topologies may be derived from the basic topologies by replacing the inductor with a transformer. For example, an isolated flyback converter can be derived from the boost converter, and forward, double-forward, half-bridge or full-bridge converters can be derived from the buck converter.

Depending on the characteristics of current in the output inductor of the power stage, all of the above converters may either be operating in continuous conduction mode (CCM) or in discontinuous conduction mode (DCM). In CCM mode, the current in the output

inductor is continuous for the duration of the switching cycle. In DCM the current in the output inductor is discontinuous, typically increasing from zero, and then dropping back to zero, where it stays for the remaining part of the switching cycle. (Typical waveforms associated with CCM and DCM modes of operation are shown in Fig.2.3. and Fig.2.4. respectively.)

During the last decade, a large number of resonant converters were introduced. A resonant converter can be derived from a conventional converter (listed above) by adding a resonant L - C network. The main purpose and advantage of the resonant network is to allow for switching at instances when the current or voltage across the switching device is zero. The resulting main benefits are low switching losses and low EMI/EMC noise generation.

With the significant growth in the market demand for a new class of high power density low output voltage converters, the large family of converters with synchronous rectifiers has been introduced. These converters use transistor switches in place of rectifier diodes.

By mode of control, two main classes of converters are recognized: voltage and current mode control. In the case of voltage mode control, the output voltage is sensed, compared with a reference voltage, amplified by an error amplifier and transformed into a pulse width. The transformation to a pulse width is done by comparing the amplified error signal with a signal from internal ramp generator. In the case of current mode control, the sensed and amplified output voltage is compared with a ramp signal derived from the input current. Further details are discussed in section 2.3.

With respect to switching frequency, two type of converters exist: fixed and variable. While fixed frequency converters operate with a strictly defined switching period, the duration of the switching cycle for variable frequency converters is dependent on con-

verter's selected internal variables. The purpose of extending the switching period is to achieve more favorable conditions for operation of the switching devices and, thus, reduce switching losses and EMI/EMC noise.

2.3. Principle of Operation of Switching DC/DC Converters

The principle of operation of switching DC/DC power converters can be explained using the example of a closed-loop boost converter operating with voltage mode control (Fig.2.2.).

The power stage of the converter consists of an inductor L , switch transistor Q , rectifier diode D and filter capacitor C . The components R_L and R_C represent the parasitic resistances of the inductor and filter capacitor respectively. The control unit can be represented by a comparator with a ramp signal present on its non-inverting input. The input and output secondary filters can be omitted from the discussion without any loss on generality.

We will consider diode D and the transistor Q operating as discrete switches. Further, let's assume that the switches have negligible impedance when on, high impedance when off and change their switching state simultaneously. The time needed by these switches to change state may be treated, for purpose of this paragraph, as negligible. Performing a simple analysis, it can be found, that under most conditions the switches operate in anti-phase, i.e. the transistor is on when the diode is off and vice versa. Thus, the state of the switching elements defines two different converter circuits called topologies.

Topology 1, often called on-time topology or on-topology, begins when the switching transistor Q is on and ends when the transistor is off. During on-time, the right side of the inductor L is connected to ground, and the inductor current i_L rises. The diode D is reverse biased and does not allow the capacitor C to discharge through the transistor Q . During this interval, the output current i_o is supplied to the load by capacitor C , causing the voltage across it to decrease. Due to the state of the switches (transistor Q is on and diode D is off), the power stage is practically separated into two independent circuits.

Fig. 2.2 Schematic of a boost converter with voltage mode control.

Topology 2, often called off-time topology or off-topology, begins when the switching transistor Q is switched off. This change introduces a high impedance into the inductor current path V_g - L - GND . The inductor current decreases causing the polarity of the inductor to reverse. Thus, the voltage at the cathode of diode D rises and stabilizes to a value of

the output voltage V_{out} increased by the diode forward drop. The diode is forward biased and is considered on. The inductor current flows partially into capacitor C and partially into the load. The off-time topology, because of the status of the switches (transistor Q is off and diode D is on) behaves as a RLC circuit.

The switches operate with a period T , called the switching period. The duration of the on-time is given by the product dT , where symbol d stands for the duty ratio. Conversely, the duration of the off-time topology equals $(1-d)T$. Typical waveforms of inductor current and capacitor voltage for a boost converter operating in continuous conduction mode (CCM) at steady-state are given in Fig.2.3.

The state of transistor Q depends on the signal $\delta(t)$ which is generated by the comparator in the control circuit. The time when the transistor switches from off to on is known a priori and is defined by the switching frequency. On the other hand, the time when the transistor switches from on to off is not known before hand and depends on the result of comparing the error signal V_{ea} with the ramp V_{ramp} . The state of diode D depends on the voltage present across its electrodes.

If, in the circuit shown in Fig. 2.2., the feedback and control circuits are removed (open loop operation) and the converter is controlled by the transistor gate signal $\delta(t)$ (generated from an external source with both fixed frequency and duty ratio) then the times of switching for transistor Q are known a priori. In such a case the transistor is referred to in literature as an “external switch”. Since the state of the diode D is changed simultaneously with switching of the transistor, the diode can be also considered as an external switch.

As shown in Fig.2.3., the inductor current flows continuously and is not interrupted over the course of the switching period. In literature, this is referred to as a continuous conduction mode (CCM) of operation. The converter can also operate in a mode where the

inductor current flows only for a portion of the switching period. Based on the parameters of the circuit components, or during the converter response to change of the input voltage or load impedance, the inductor current may fall to zero before transistor Q turns back on.

Fig.2.3 Waveforms of boost converter operating in CCM at steady-state.

This causes diode D to turn off. The state of the switches (transistor Q is off and diode D is off) defines a third topology. The converter, in this instance, operates in a mode referred to as discontinuous conduction mode (DCM). The time at which the diode switches from on to off is not known a priori turning the diode into an “internal switch”. Typical waveforms of inductor current and capacitor voltage of a boost converter operating in discontinuous conduction mode at steady-state are shown in Fig.2.4

Fig.2.4 Waveforms of boost converter operating in DCM at steady-state.

In summary, the principle of operation of switching DC/DC converters can be explained using special circuits called topologies. The topology is enforced to the converter through the converter's switches. The switches may change their status in instants a priori known or unknown. In steady-state, the converter's topologies periodically repeat. The circuit assigned to the converter's topology can be treated as linear. The approach to the modeling of the behavior of switching converters as described above is referred in literature to as piecewise linear.

Chapter 3

Time-Domain Analysis of Switching DC/DC Converters

3.1 Introduction

Large number of simulation algorithms for analysis of switching DC/DC power converters in time-domain are presented in literature. Despite the variety of techniques and approaches used, each of published algorithm need to respond to the following fundamental questions: how to model the converter's devices, how to formulate system equations, and how to solve system equations.

As shown in the previous chapters, switching DC/DC converters are complex circuits which consist of several functional blocks and include various components. Typically, the switching converter includes magnetic devices (transformers, inductors, coupled induc-

tors), switching elements (transistors, diodes), VLSI chips (PWM controllers, reference-sources), optocouplers, passive devices (resistors, capacitors), and even many kinds of protective devices (surge suppressors, varistors, etc.).

The major concern of practical design is about the analysis of the operation of the switching converter's power stage. Accordingly, the focus of this work is the same. The power stage of switching converters usually includes passive devices (resistors, capacitors), magnetic devices (transformers, inductors) and switching devices (diodes, transistors). In this chapter very simple models for resistors, capacitors and inductors are used: resistor is modeled as a pure resistance, capacitor model includes capacitance and serial effective resistance and a winding resistance is added in series with inductance to model the inductor. In literature, switching elements of converters use to be almost always modeled as ideal switches (zero or small resistance when on, infinitive resistance when off and zero switching time). This approach is very common when a new simulation algorithm is presented. In some rare cases the switch model is upgraded using parasitic capacitances and inductances ([8], [24]). Higher level models are typically used in coincidence with commercial simulators ([9], [11]). More detailed discussion about models of devices of switching converters is given in Chapter 5.

To formulate system equations, the piecewise linear modeling technique discussed in Chapter 2 is almost exclusively used in literature. Accordingly, each of several switching topologies which occurs within a switching cycle can be considered a linear circuit. Having the converter topologies identified, two major approaches to the formulation of system equations are adopted: modified nodal (MNA) and closed form (state-space approach). The MNA approach leads to the use of numerical integration to solve system equations. The system equations formulated in closed form can be also solved by numerical integration. The particular advantage of the closed form formulation of system equations, however, resides in an efficient use of analytical expression for their solution which is known a priori. This approach leads to the significantly shorter simulation time. For this feature, the

methods based on the closed form formulation of system equations methods use to be referred in literature to as “fast time-domain methods”.

Using any of the method above the time response of a switching converter can be simulated and the converter switching waveforms at steady-state analyzed. In the past decade a special group of methods referred to as “methods with accelerated convergence into steady-state” was developed. The goal of these methods is to determine the converter’s steady-state in the smallest possible number of iterations rather than to accurately simulate the transient response in time-domain.

The principle of simulation algorithms based on the MNA methods is presented in section 3.2. The use of commercial simulators for analysis of switching converters in time-domain is covered by section 3.3. The algorithms based on the closed form formulation of system equations are discussed in section 3.4. The principle and implementation of methods with accelerated convergence into steady-state is explained in section 3.5. The summary and conclusions are presented in section 3.6.

3.2. Time-Domain Algorithms Based on Modified Nodal Analysis

The modified nodal analysis (MNA) method is a general method for formulation of system equations used for analysis of electrical networks. In this section basic steps for development of simulation algorithms for switching converters based on this method are shown. These steps include the formulation of system equations, solution of the system equations and managing of the overall simulation procedure. The details of the derivation of system equations are illustrated using the boost converter from Chapter 2. Advantages

and disadvantages of the MNA method for simulation algorithms are summarized at the end of this chapter.

a) Formulation of model equations

The MNA method for formulation of system equations is based on formulation of a reduced number of nodal equations using Kirchhoff's laws. Its main advantage is that the procedure of derivation of the system matrix M can be relatively easily automatized using known device stamps.

The piecewise linear modelling technique is used for formulation of system equations in following. The number of sets of system equations depends on number of converter topologies which occur within a switching cycle.

Let's substitute the transistor Q and the diode D in boost converter from Fig.2.2 operating in open loop in CCM by the ideal switches. The circuit of the converter, after this substitution, is shown in Fig.3.1.

Fig.3.1 Boost converter operating in open loop.

As discussed in Chapter 2, two circuit topologies are needed to describe behavior of this converter in time-domain: on-time and off-time topology. During the on-time topology the transistor Q is on and the diode D does not conduct. Consequently, the transistor is replaced by a short connection between the inductor and ground and the diode is modeled as an open circuit. The resulting on-time topology circuit and numbering of related nodes is shown in Fig.3.2.

Fig.3.2 On-time topology of boost converter.

The vector of nodal variables x with reference to the Fig.3.2 is:

$$x = [v_1 \ v_2 \ v_3 \ v_4 \ i_L \ i]^T \quad (3.1)$$

The system matrix can be written from Fig.3.2 by inspection:

$$M_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & -1 & 1 \\ 0 & g_L & 0 & 0 & -1 & 0 \\ 0 & 0 & g + g_c & -g_c & 0 & 0 \\ 0 & 0 & -g_c & sC + g_c & 0 & 0 \\ 1 & -1 & 0 & 0 & -sL & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (3.2)$$

Accordingly, the system equation for the on-time topology is:

$$C_1 \dot{x} + G_1 x = b_1 \quad (3.3)$$

where matrices C_1 , G_1 , and the input vector b_1 are defined as follows:

$$C_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & C & 0 & 0 \\ 0 & 0 & 0 & 0 & -L & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, G_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & -1 & 1 \\ 0 & g_L & 0 & 0 & -1 & 0 \\ 0 & 0 & g + g_c & -g_c & 0 & 0 \\ 0 & 0 & -g_c & g_c & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \text{ and } b_1 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ V_g \end{bmatrix} \quad (3.4)$$

During the off-time topology (Fig.3.3) the transistor Q is off and the diode D is on. Therefore the transistor is replaced by an open circuit and the diode by a short circuit connection.

Fig.3.3 Off-time topology of boost converter.

Again, the system matrix for the off-time topology can be written by inspection and comes in the form:

$$M_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & -1 & 1 \\ 0 & g_L & -g_L & 0 & -1 & 0 \\ 0 & -g_L & g + g_L + g_c & -g_c & 0 & 0 \\ 0 & 0 & -g_c & sC + g_c & 0 & 0 \\ 1 & -1 & 0 & 0 & -sL & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (3.5)$$

The system equations for the off-time topology are:

$$C_2 \dot{x} + G_2 x = b_2 \quad (3.6)$$

where the respective system matrices C_2 , G_2 and the input vector b_2 are

$$C_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & C & 0 & 0 \\ 0 & 0 & 0 & 0 & -L & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, G_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & -1 & 1 \\ 0 & g_L & -g_L & 0 & -1 & 0 \\ 0 & -g_L & g + g_L + g_c & -g_c & 0 & 0 \\ 0 & 0 & -g_c & g_c & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \text{ and } b_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ V_g \end{bmatrix} \quad (3.7)$$

The vector of nodal variables is unchanged:

$$x = [v_1 \ v_2 \ v_3 \ v_4 \ i_L \ i]^T \quad (3.8)$$

In general, the system equations for the boost converter are specified by the expression:

$$C_i \dot{x}(t) + G_i x(t) = b_i(t) \quad (3.9)$$

where the index i is equal to 1 or 2 depending on actual converter topology, and system matrices C_i , G_i and input vector b_i are those defined by the expressions (3.4) and (3.7).

b) Solution of the model equations

The system of equations (3.3) and (3.6) can be solved in time-domain using many numerical methods. The examples of such as methods are Euler methods, methods of Runge-Cutta, method of trapezoidal rule or Gear's methods ([5], [7]). As an illustration, the procedure for the derivation of final recursive expression for computation of time-domain response of the boost converter from Fig.3.2, the backward Euler method will now be explained.

The general formula for the backward Euler integration rule is:

$$x(m+1) = x(m) + h\dot{x}(m+1) \quad (3.10)$$

where

$x(m)$ is the vector of nodal variables x in step m , $\dot{x}(m+1)$ is the first derivative of the vector x in step $m+1$, $x(m+1)$ is the vector x in step $m+1$, and h is the integration step.

From the expression (3.10) the derivative of the vector x in step $m+1$ is

$$\dot{x}(m+1) = \frac{x(m+1) - x(m)}{h} \quad (3.11)$$

After the relation (3.11) is implemented into the system equations (3.9) we get

$$C_i \frac{x(m+1) - x(m)}{h} + G_i x(m) = b_i(m+1) \quad (3.12)$$

where the subscript i is equal 1 or 2 depending on the converter topology. After a small rearrangement terms in (3.12) the final recursive expression for solution of system equations is:

$$x(m+1) = \left(\frac{C_i}{h} + G_i \right)^{-1} \left(\frac{C_i}{h} x(m) + b_i(m+1) \right) \quad (3.13)$$

c) Simulation algorithm

To model the overall behavior of switching converter in time-domain the simulation algorithm has to manage the following tasks: initialization of computation, computation of time-domain response of converter's i -th topology, determination of the time of switching from one topology to another and passing the vector of nodal variables at times of switching. The block diagram of a general simulation algorithm is shown in the Fig.3.4.

Fig.3.4 Block diagram of algorithm for simulation of converter time-domain response.

At the initialization step of simulation the system matrices $C_1, C_2, G_1, G_2, b_1, b_2$ can be computed using parameters of converter devices and the vector x can be set to the zero vector. The simulation can start with computing for the on-time topology.

The times of switching, in the case of the boost converter operating in open loop (Fig.3.2), are known a priori. Thus, the changes of topologies happen at known instants T_{1k} and T_{2k} :

$$T_{1k} = (k + d)T \quad (3.14)$$

$$T_{2k} = kT \quad (3.15)$$

where T_{1k} are the times of switching from on-topology to off-topology, T_{2k} are the times of switching from off-topology to on-topology, d is known value of duty ratio, T is switching period, and $k=0, 1, 2, \dots, n$ is the order of the switching period being simulated.

After the last point of solution for the on-time topology is found ($x_1/(k+d)T$), the vector x is passed as a vector of initial conditions for computation of solution for the off-time topology (X_{20}). Similarly, after the last point of solution for the off-time topology is found ($x_2/(k+1)T$), the vector x is passed to for the on-time topology simulation as a vector of initial conditions (X_{10}).

d) Discussion

1. Size of system matrices

In cases when more complex models of converter devices are used (e.g. transistor and diode are modeled as two-value resistors) the circuit from Fig.3.2 expands, new nodes are added and, consequently, the size of the matrix M grows.

2. Discontinuous conduction mode of operation

In Chapter 2 it was shown that the converter from Fig.3.1 can operate also in the discontinuous conduction mode (DCM). In such a case the system description for the third converter topology can be obtained using the same procedure as shown in section a) above.

3. Closed loop simulation

In case of simulation of converter operating with closed feedback control loop the nodes of feedback circuit (e.g. the voltage mode control feedback circuit as shown in Fig. 2.2) need to be added into the converter model. Since the feedback circuit can force the boost converter operating in CCM in steady-state to operate temporarily in DCM mode (e.g. simulating start-up or large transients), the model of the DCM topology should be added into simulation.

4. Selection of integration step

In general, the size of the integration step h has a critical meaning for accuracy, stability and speed of numerical integration. In case of the DC/DC switching converters this parameter can be chosen in relation to the length of the switching period T_{sw} . In simulation of circuits with no parameters causing high-frequency parasitic ringing (e.g. Fig. 3.1) the choice 100 to 200 timesteps per switching period usually guarantees optimal performance of simulation algorithm.

5. Determination of switching times

The implementation of the feedback circuit (Fig.2.2) or modeling the DCM mode of operation (Fig.2.4) introduces problem of determination of switching times. In contrary to the open loop simulation, the times of switching are not known a priori and vary as simulation progress. The problem of determining switching times can be solved using "switching variables" (e.g. [1]). According to the Fig.2.2, the switching variables can be defined as follows:

$$p_1(t) = V_{ea}(t) - V_{ramp}(t) \quad (3.16)$$

$$p_2(t) = i_L(t) \quad (3.17)$$

The values of t for which applies

$$p_1(t) > 0 \quad (3.18)$$

usually define the duration of the on-time topology. The exception is a simulation of converter circuits which includes the maximum duty ratio control and/or the soft-start function. At the switching instants $t=kT+T_1$ the value of the switching variable $p_1(kT+T_1)$ is equal to zero. Similarly, the values of t for which applies

$$p_2(t) > 0 \quad (3.19)$$

usually define the duration of the second converter topology. At the switching instants $t=kT+T_2$ the value of the switching variable $p_2(kT+T_2)$ is equal to zero and the DCM topology begins.

In simulation algorithm the switching variables have to be evaluated after computing for each integration step. If a negative value of the switching variable is encountered the converter topology is updated.

6. Networks with permitted Dirac impulses

In references [1], [2] and [4] methods for networks with ideal switches with allowed discontinuities including Dirac impulses are presented. The proposed algorithms detects the occurrence of the Dirac impulse, updates converter topology, and finds the contribution of the Dirac impulse to the time-domain solution.

3.3 Analysis of Switching DC/DC Converters Using Commercial Simulators

Formulation of system equations of switching converter using the MNA method and implementation of higher level device models of switching components can be generalized and automated using computers. In fact the modified nodal formulation of system equations and methods of numerical integration are used in computational cores of commercial circuit simulation packages such as PSpice or Saber ([7], [9], [10], [11]).

A total replacement of the role of simulator developer by the role of simulator user combined with relatively easy handling of device models and simulation options create the use of commercial simulators attractive also in the area of simulation of switching power converters. The analysis of converter behavior in time-domain involves the creation of converter model and the setting of the simulation profile for, typically, transient analysis. The converter model can be created either by drafting the converter circuit using the input graphic editor of the simulator (Schematic capture) or by creating a circuit netlist. In the first case the netlist is generated automatically before the simulation is initiated. The models of converter's devices are often available in the simulator's libraries and can be modified using part editor programs. A simple example of simulation schematic of the boost converter from section 3.2 as used in PSpice is shown in Fig.3.5. In this case, the higher order models of the transistor Q and diode D are used.

Fig. 3.5 Schematic of boost converter as created in Schematic capture in PSpice.

Discussion

When using commercial circuit simulators (PSpice, Saber) the problems associated with derivation and sizes of system matrices, also modeling the DCM of operation, are in fact hidden from the user. In case of closed loop simulation the nodes of feedback circuit can be added into the converter model.

Even if, at a first glance, the use of the commercial simulators may seem to be simple and straight forward, in reality, this approach may fail in several aspects. The root of the problems comes from the discrepancy between strongly non-linear operation of converters at instants of switching on one side and the nature of computing algorithms used in commercial simulators on the other side. More specifically, the commercial simulators recognize the model of switching converter as one entity and, therefore, use only one set of system equations for simulation. (In contrast, “hand derived” simulation algorithms (as described in section 3.2.) use the piecewise linear approach and handle the instants of switching by updating the systems equations.) Consequently, such a system description includes strong non-linearities or discontinuities and is exposed to sudden and steep changes of nodal variables associated with converter switching. This may cause substantial difficulties in terms of convergence, accuracy and simulation speed. Even further, the

case of simulation of ideal switches may be beyond computing capability of the commercial simulators. More details related to difficulties associated with the use of commercial simulators are discussed in section 3.6.

3.4. Time-Domain Algorithms Based on Closed Form System Equations

The simulation algorithms based on closed form formulation of system equations, (or the state-space or analytical approach, in abbreviation) are, historically, older than those based on the MNA method. Although, in the area of commercial simulation tools, the closed form formulation of system equations was replaced by the MNA method ([3]), the majority of published works in the area of switching converters use the system matrices formulated in closed form. The system equations created using this approach can be solved using both analytical and numerical methods. Similarly to section 3.2, also in this section the basic steps needed for the derivation of system equations and development of simulation algorithms are shown and discussion is provided. The detailed derivation of system equations is shown, again, in the example of a boost converter operating in open loop in CCM mode (Fig.3.1).

a) Formulation of model equations using state variables

As in section 3.2, the piecewise linear technique is used in following. As a general rule, the number of sets of system equations depends on the number of converter topologies within a switching cycle.

A circuit of a switching converter contains typically two kind of energy storage elements: inductors and capacitors. Thus, the state variables are chosen accordingly: inductor currents and voltage across the capacitors.

To derive the state-space model, firstly, the initial equations can be written using Kirchhoff's laws. From those, secondly, the first derivatives of the state variables are found and state matrices are defined. The application of this procedure to the converter shown in Fig.3.1 follows.

The converter from Fig.3.1 includes one inductor L and one capacitor C . Thus the state vector x is defined by the expression:

$$x = \begin{bmatrix} i_L \\ v_C \end{bmatrix} \quad (3.20)$$

For the on-time topology the initial equations are:

$$V_g = R_L i_L + \dot{i}_L L \quad (3.21)$$

$$v_C + i_C R_C + i_C R = 0 \quad (3.22)$$

$$i_C = C \dot{v}_C \quad (3.23)$$

Fig.3.6 On-time topology of boost converter.

The state-space equations are found after substituting for the capacitor current (3.23) in (3.22) and moving the state variables to the left side:

$$\dot{i}_L = -i_L \frac{R_L}{L} + V_g \frac{1}{L} \quad (3.24)$$

$$\dot{v}_C = -v_C \frac{1}{C(R+R_C)} \quad (3.25)$$

what in a matrix form is:

$$\dot{x} = A_1 x + b_1 V_g \quad (3.26)$$

where

$$A_1 = \begin{bmatrix} -\frac{R_L}{L} & 0 \\ 0 & -\frac{1}{C(R+R_C)} \end{bmatrix}, \text{ and } b_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \quad (3.27)$$

The voltage across the load resistor R is the system output y :

$$y = -i_C R \quad (3.28)$$

After substitution for i_C from (3.23) and $\dot{v}_C$ from (3.25) the output is found in form

$$y = v_C \frac{R}{R+R_C} \quad (3.29)$$

or

$$y = c_1^T x \quad (3.30)$$

where

$$c_1^T = \left[0 \quad \frac{R}{R + R_c} \right] \quad (3.31)$$

The initial equations for the off-time topology (Fig.3.7) are as follows

$$V_g = i_L R_L + \dot{i}_L L + i_c R_c + v_c \quad (3.32)$$

$$v_c + i_c R_c - i_o R = 0 \quad (3.33)$$

$$i_o = i_L - i_c \quad (3.34)$$

$$i_c = C \dot{v}_c \quad (3.35)$$

Fig.3.7 Off-time topology of boost converter.

The expression for the state variable $\dot{v}_c$ can be found from equation (3.33) after substitutions for output current and capacitor current from (3.34) and (3.35) respectively in form

$$\dot{v}_c = i_L \frac{R}{C(R_c + R)} - v_c \frac{1}{C(R_c + R)} \quad (3.36)$$

Equation (3.32), after a substitutions for capacitor current (3.35) and derivative of capacitor voltage from (3.36) gives the expression for the second state variable $\dot{i}_L$:

$$\dot{i}_L = -i_L \frac{R_L + R \parallel R_c}{L} - v_c \frac{R}{L(R_c + R)} + V_g \frac{1}{L} \quad (3.37)$$

where the symbol $R \parallel R_c$ means a parallel combination of resistors R and R_c .

The state equations for the off-time topology in a matrix form are:

$$\dot{x} = A_2 x + b_2 V_g \quad (3.38)$$

where

$$A_2 = \begin{bmatrix} \frac{R_L + R \parallel R_c}{L} & -\frac{R}{L(R_c + R)} \\ \frac{R}{C(R_c + R)} & -\frac{1}{C(R_c + R)} \end{bmatrix} \text{ and } b_2 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \quad (3.39)$$

The system output is defined by the expression

$$y = i_o R \quad (3.40)$$

The expression (3.40), after consecutive substitutions for output current (3.34), capacitor current (3.35) and derivative of capacitor voltage (3.36) introduces the output equation in the form:

$$y = \left[R \parallel R_c \frac{R}{R + R_c} \right] \begin{bmatrix} i_L \\ v_c \end{bmatrix} \quad (3.41)$$

or

$$y = c_2^T x \quad (3.42)$$

where

$$c_2^T = \left[R \parallel R_c \frac{R}{R + R_c} \right] \quad (3.43)$$

In general, the state-space model of the boost converter is specified by sets of linear differential equations:

$$\dot{x} = A_i x + b_i v_g \quad (3.44)$$

$$y = c_i^T x + d_i v_g \quad (3.45)$$

where the index i is equal to 1 or 2 depending on actual converter topology. The system matrices A_i , b_i , c_i^T and d_i are defined by expressions (3.27), (3.31), (3.39) and (3.43), x is the vector of state variables or state vector defined by expression (3.20), v_g is the input vector, and y is the converter's output. For the case of the boost converter from Fig.3.1, the matrices d_1 and d_2 are equal to a zero matrix.

b) Solution of model equations using analytical methods

The piecewise linear model of a switching converter in state-space is defined by a set of linear differential time-invariant equations (3.44) and (3.45). The explicit analytical solutions of these equations can be found in literature on classical control theory in the form:

$$x_i(t) = e^{A_i(t-t_{io})}x_i(t_{io}) + \int_{t_{io}}^t e^{A_i(t-\tau)}b_iv_g(\tau)d\tau \quad (3.46)$$

where $i=1,2, \dots, k$, k is a number of converter topologies within switching cycle, t_{io} is the time of beginning of i -th topology and $x_i(t_{io})$ is a vector of initial conditions at the time t_{io} . The matrix $e^{A_i(t-t_{io})}$ is the state transition matrix assigned to the i -th converter topology.

The solution (3.46) can be further simplified by making the two following assumptions. Firstly, the input vector $v_g(\tau)$ is constant during a switching period, which is true in the case of DC/DC converters. Secondly, the time t_{io} can be set to zero since during the simulation over many switching cycles, an extra variable used to be assigned to monitor time. Thus the expression (3.46) becomes

$$x_i(t) = e^{A_it}x_i(0) + \int_0^t e^{A_i(t-\tau)}b_iV_gd\tau \quad (3.47)$$

and, after the integration, the solution is

$$x_i(t) = e^{A_it}x_i(0) + A_i^{-1}[e^{A_it} - I]b_iV_g \quad (3.48)$$

or

$$x_i(t) = \phi_i(t)x_i(0) + A_i^{-1}[\phi_i(t) - I]b_k V_g \quad (3.49)$$

where $x_i(t_{i0}) = x_i(0)$ and $\phi_i(t) = e^{A_i t}$ is the state transition matrix.

After the state vector is found, the converter output y can be computed directly using the equation (3.45).

c) Solution of model equations using methods of numerical integration

Many methods of numerical integration (Euler's methods, trapezoidal rule method, methods of Runge-Kutta or Gear's methods) can be used to solve the system equations defined by expressions (3.44). In the case of the backward Euler algorithm, the general integration formula (similarly to the relation (3.10)) is:

$$x_i(m+1) = x_i(m) + h\dot{x}_i(m+1) \quad (3.50)$$

where

$x_i(m)$ is the state vector x in step m , $x_i(m+1)$ is the state vector x in step $m+1$, $\dot{x}_i(m+1)$ is a first derivative of state vector x in step $m+1$, index i relates the state vector to the i -th converter topology and h is a constant of the integration algorithm.

From the (3.50) the derivative of state vector x_i in step $m+1$ is

$$\dot{x}_i(m+1) = \frac{1}{h}x_i(m+1) - \frac{1}{h}x_i(m) \quad (3.51)$$

After the relation (3.51) is implemented into the state equation (3.44)

$$\frac{1}{h}x_i(m+1) - \frac{1}{h}x_i(m) = A_i x_i(m+1) + b_i v_g(m+1) \quad (3.52)$$

the general integration formula for the i -th converter topology is

$$x_i(m+1) = (I - hA_i)^{-1} [x_i(m) + hb_i v_g(m+1)] \quad (3.53)$$

or

$$x_i(m+1) = (I - hA_i)^{-1} [x_i(m) + hb_i V_g] \quad (3.54)$$

assuming constant input voltage of the magnitude V_g .

d) Simulation algorithm

The block diagram of the algorithm for computation of the response of the switching converter in time-domain for both analytical and numerical methods is similar to that shown in the section 3.2. At the beginning, the state matrices are computed and state vector is set (typically) to the zero vector. At instants of switching T_i the state vector is passed

as a vector of initial conditions for computation of the solution of consequent topology:

$$x_i(T_i) = x_{i+1}(0) \quad (3.55)$$

The substantial difference between the analytical and numerical approach is the fact that the analytical approach allows for computing values of the state vector directly and accurately at instants of switching, removing the need of execution of tens or hundreds of small integration steps as necessarily requested in case of numerical integration.

e) Discussion

1. Size of system matrices

The size of the system matrices depends on the number of state variables which, in turn, is dependent on the complexity of the models of converter devices used (e.g. transistor is modeled as a parallel combination of channel resistance and parasitic capacitance).

2. Discontinuous conduction mode of operation

The third set of state matrices is needed when modeling the discontinuous conduction mode of operation (DCM). The same procedure as shown in section a) above can be used to derive the system description for the third converter topology.

3. Closed loop simulation

Similarly to section 3.2, both the feedback and the DCM topology circuits need to be implemented into the model when simulating the behavior of a converter operating with closed feedback loop.

4. Selection of integration step

In the case of numerical integration the rule for the selection of the integration step is the same as for the MNA methods discussed in section 3.2.

5. Computation of switching times

In the case of only external switches all time intervals T_i are known a priori and the matrix exponentials $\phi_i(t)$ become constant matrices. Therefore the computation of converter time-domain response consists of repeated evaluations of expression (3.49) with updated initial conditions given in (3.55).

In the case of the internal switches, however, the switching variables or boundary conditions respectively have to be defined and incorporated into simulation algorithms.

If the numerical approach is chosen (c), the switching variables need to be defined and evaluated after computation of each timestep of the converter response using the same approach as shown in the section 3.2 ((3.18) and (3.19)). The values of the switching variables can be derived from values of state variables the same way as it was done for the converter output (a)).

In the case of the analytical approach the computation of switching times means the up front determination of time intervals T_i . The boundary conditions have to be defined and the solution of system equations (3.44) have to be found. In the example of the boost converter operating in closed loop in the voltage mode of control (Fig.2.2) the boundary conditions can be defined in the following form:

$$V_{ea}(T_1) - V_{ramp}(T_1) = 0 \quad (3.56)$$

$$i_L(T_2) = 0 \quad (3.57)$$

and rewritten in a general form:

$$0 = c'_i \cdot x_i + d'_i \cdot V_g \quad (3.58)$$

This form of expression of switching variables will be used later in section 3.5.

6. Approximation of the matrix exponential $\phi_i(t)$

The critical step when solving the boundary problem (3.58) is the approximation of the matrix exponential $\phi_i(t)$. In the past, various solutions for this problem were presented. In [17], the matrix exponential was computed using eigenvalue-eigenvector decomposition. A disadvantage of this method is in the handling of matrices with repeated eigenvalues. A very popular method of approximation of matrix exponential has been the Taylor series expansion ([12], [13], [18], [19]). The Chebyshev polynomial expansion to compute the matrix exponential was used in [16] and [20]. Also, a Pade approximation of matrix exponential was presented in [21]. A performance of methods above was evaluated in [21] and, in terms of accuracy and computational speed, the use of Pade approximation was preferred over the Taylor series approximation.

7. Networks with permitted Dirac impulses

In [6] a state-space based method for networks with ideal switches and permitted Dirac impulses was presented.

3.5. Methods of Accelerated Convergence into Steady-State

Several methods of simulation of converter time-domain response were discussed in previous sections. The time-domain simulation, in general, can begin from any converter state and proceed until a steady-state is achieved. Depending on how far the initial operating point is from the steady-state, the simulation procedure can involve possibly hundreds to thousands of switching cycles and may become time consuming. Therefore, with the goal to obtain a steady-state of the converter in very short time, several methods were developed in the past. Instead of the precise simulation of converter time-domain response, these methods compute values of state vector such that the steady-state is achieved within the smallest number of iterations. These methods are referred in literature to as methods with accelerated convergence into steady-state ([25] through [31]). For simplicity reasons these methods are referred to in this work in abbreviation as methods of accelerated convergence or as steady-state methods.

In the following the derivation of the steady-state algorithm for the accelerated convergence is shown, the overall simulation diagram is outlined, and the discussion provided. Advantages and potential problems of these algorithms are summarized at the end of this chapter.

a) Derivation of the algorithm for accelerated convergence

Consider a converter operating in k topology changes within switching cycle. Let's further assume that the converter's model equations in closed form ((3.44) and (3.45)) are known. A trajectory of state vector of this converter in a steady-state is shown in Fig.3.8.

Fig.3.8 Trajectory of state vector of converter in steady-state.

In the steady-state the initial state x_0 at the beginning of the switching cycle is equal to the state at the end of the switching cycle x_k and vice versa. Thus the following applies:

$$x_k - x_0 = 0 \quad (3.59)$$

In the case when the steady-state was not achieved the result of subtraction (3.59) is a non-zero vector. Since any vector x_0 can be chosen as an initial state, the error function

$$F(x_0) = x_k - x_0 \quad (3.60)$$

is continuous and can be approximated in a small neighborhood of x_0 by a first-order Taylor series expansion

$$F(x_0 + \Delta x_0) = F(x_0) + \frac{\partial F(x_0)}{\partial x_0} \Delta x_0 \quad (3.61)$$

where the matrix

$$\frac{\partial F(x_0)}{\partial x_0} = J(x_0) \quad (3.62)$$

is the Jacobian matrix of the error function $F(x_0)$ at the point x_0 .

At steady-state the expression (3.61) is equal to the zero vector and a correction vector Δx_0 from the same expression is

$$\Delta x_0 = -[J(x_0)]^{-1} F(x_0) \quad (3.63)$$

If a value of correction Δx_0 is known, the initial guess x_0 and all following new (corrected) states can be computed using the iterative formula:

$$x_{0new} = x_0 + \Delta x_0 \quad (3.64)$$

The computation of the Jacobian $J(x_0)$ of the error function (3.62) is an essential part of the overall algorithm of accelerated convergence and its derivation is shown in detail in the following.

After the error function (3.60) is substituted into the expression for the Jacobian (3.62), the Jacobian comes in a form

$$J(x_0) = \frac{\partial x_k}{\partial x_0} - I \quad (3.65)$$

Referring to the expression (3.49) from the previous part, the relation between the state vector at the exit of the i -th topology x_i and state at the exit from previous topology x_{i-1} is

$$x_i = \phi_i(T_i)x_{i-1} + A_i^{-1}[\phi_i(T_i) - I]b_iv_g \quad (3.66)$$

Let's define the sensitivity matrix of the i -th topology J_i as follows:

$$J_i = \frac{\partial x_i}{\partial x_{i-1}} \quad (3.67)$$

The meaning of the definition of the Jacobian J_i is that it shows how sensitive the state vector is at the exit of the i -th topology x_i to changes of state vector at the entry to the same topology x_{i-1} .

Now, after the chain rule is applied, the Jacobian matrix $J(x_0)$ is obtained in a form

$$J(x_0) = J_k J_{k-1} \dots J_i \dots J_2 J_1 - I \quad (3.68)$$

The value of J_i results from a partial differentiation of equation (3.66) with respect to x_{i-1} .

It results in

$$\frac{\partial x_i}{\partial x_{i-1}} = \frac{\partial}{\partial x_{i-1}} \{ \phi_i(T_i)x_{i-1} + A_i^{-1}[\phi_i(T_i) - I]b_iv_g \} \quad (3.69)$$

The state transition matrix $\phi_i(T_i)$ is a function of x_{i-1} because T_i is dependent on x_{i-1} through implicit relationship in (3.58). Since only the state transition matrix $\phi_i(T_i)$

depends on changes of the state vector x_{i-1} , applying the partial derivation to the (3.69) yields

$$\frac{\partial x_i}{\partial x_{i-1}} = \phi_i(T_i) \frac{\partial x_{i-1}}{\partial x_{i-1}} + \frac{\partial \phi_i(T_i)}{\partial T_i} x_{i-1} \frac{\partial T_i}{\partial x_{i-1}} + A_i^{-1} \frac{\partial \phi_i(T_i)}{\partial T_i} b_i v_g \cdot \frac{\partial T_i}{\partial x_{i-1}} \quad (3.70)$$

and further implies

$$\frac{\partial x_i}{\partial x_{i-1}} = \phi_i(T_i) + A_i \phi_i(T_i) x_{i-1} \frac{\partial T_i}{\partial x_{i-1}} + \phi_i(T_i) b_i v_g \cdot \frac{\partial T_i}{\partial x_{i-1}} \quad (3.71)$$

The derivative $\frac{\partial T_i}{\partial x_{i-1}}$ from the expression above shows that the time duration of the i -th topology T_i depends on a change of state vector at the entry to the topology x_{i-1} . This term can be derived using the expression (3.58). The expression (3.58), after substitution for the solution of particular topology x_i in (3.66) implies

$$0 = c'_i \cdot \{\phi_i(T_i) x_{i-1} + A_i^{-1} [\phi_i(T_i) - I] b_i v_g\} + d'_i \cdot v_g \quad (3.72)$$

By applying partial differentiation to the (3.72) with respect to x_{i-1} the following is obtained

$$0 = c'_i \cdot \phi_i(T_i) + c'_i \{\phi_i(T_i) [A_i x_{i-1} + b_i v_g]\} \frac{\partial T_i}{\partial x_{i-1}} \quad (3.73)$$

From (3.73) the derivative $\frac{\partial T_i}{\partial x_{i-1}}$ is obtained in a form

$$\frac{\partial T_i}{\partial x_{i-1}} = \frac{-c'_i \phi_i(T_i)}{c'_i \{ \phi_i(T_i) [A_i x_{i-1} + b_i v_g] \}} \quad (3.74)$$

Finally, a computation of the state transition matrix $\phi_i(T_i)$ for each of k -converter topologies is based on a determination of intervals T_i by one-cycle time-domain analysis made from an initial guess. The procedure for computation of the state transition matrices $\phi_i(T_i)$ proposed in [25] is as follows:

Step 1: Carry out an initial simulation in the i -th topology with appropriate x_{i-1} as the initial condition and determine t_i that satisfies (3.58).

Step 2: Set the input vector v_g to null.

Step 3: Set a new index r to 1.

Step 4: Use the r -th column of the identity matrix as the initial state vector to the i -th topology, carry out a simulation in the i -th topology for a time span of t_i . The r -th column of $\phi_i(T_i)$ is equal to the value of the state vector at the end of this simulation.

Step 5: Repeat step 4 for r from 2 to n , filling up the remaining columns in $\phi_i(T_i)$.

Step 6: Reset the input vector v_g to an appropriate value.

After all state transition matrices $\phi_i(T_i)$ are known, the relations (3.74), (3.71) and (3.67) can be computed. Then, the Jacobian matrix $J(x_0)$ is obtained from the expression (3.68) and a correction of steady-state Δx_0 can be computed from the equation (3.64).

b) Simulation algorithm

According to the procedure for derivation of the core equations in section a) above, the overall algorithm for accelerated convergence into steady-state includes an initial guess of the steady-state vector x_0 , one cycle time-domain simulation and comparison of the final state x_k with the entry state x_0 . Depending on the result of comparison, the algorithm terminates or computes the correction to the previous state Δx_0 and repeats the one-cycle time-domain simulation and steady-state verification. The general block diagram of the simulation algorithm is shown in Fig.3.9.

Fig.3.9 General block diagram of the algorithm of accelerated convergence.

c) Discussion

1. System description

Similarly to section 3.4, the size of system matrices depends on the number of state variables included in modelled circuit. Also, the discontinuous conduction mode of operation requires derivation of the third converter topology.

2. Role of time-domain simulation

The one-cycle time domain simulation is a necessary step in the overall algorithm for accelerated convergence into steady-state.

3. Open-loop feedback operation

The algorithm of accelerated convergence was shown for converters operating in closed feedback loop. For converters operating in open feedback loop, the algorithm can be simplified in cases when the expression $\frac{\partial T_i}{\partial x_i - 1}$ is equal to zero.

4. Exit condition from the iteration

The Newton-Raphson iteration is terminated when the error between x_k and x_0 is acceptable. Because different state variables are of essentially different magnitudes, the exit condition is defined as follows:

$$E(x_k) = \frac{F(x_k)}{X_N} \quad (3.75)$$

where the vector X_N is a normalizing vector defined in terms of the expected averages values of state variables in steady-state.

5. Other methods for accelerated convergence into steady-state

The principles of the methods of accelerated convergence into steady-state, i.e. the guess of the steady-state, the computation of correction using the Jacobian of error function and the one-cycle time-domain simulation, are common for several algorithms published in literature. In the above, the system equations were formulated in closed form and the analytical expression for the Jacobian was derived. A method with a numerically computed Jacobian was presented in [28]. In [26 and 27] the MNA method was used for formulation

of system equations and the Jacobian was computed by differentiating the numerical Laplace inversion.

3.6. Summary and Conclusions

Several methods for analysis of switching converters were discussed in this chapter. In this section the advantages and potential problems of these methods in terms of overall implementation issues, simulation speed, accuracy and convergence are discussed.

a) Overall implementation issues

The formulation of system equations using the MNA method is a straight forward procedure also when modeling switching converters. Practically, it consists of the implementation of known stamps of particular elements into a system matrix. Even more complex models of switching devices can be implemented without substantial difficulties. In contrary, the formulation of system equations in closed form (fast time-domain methods, methods of accelerated convergence) may become lengthy and erroneous even for relatively small number of converter devices. An example of derivation procedure for the active clamp reset forward converter with synchronous rectifiers is discussed in Chapter 5 and, finally, shown in detail in Appendix A and Appendix B.

Implementation algorithms which are based on the numerical integration (for both the MNA and closed form system equations) or use the analytical form of solution (closed form system equations) are relatively simple as long as the times of switching are known.

If the times of switching are not known, switching variables have to be defined and evaluated as simulation progress. In the case of numerical integration the determination of the switching times is relatively straight forward and typically consists of evaluation of inequalities of type (3.18) and (3.19). In the case of analytical methods, however, the determination of the switching times means a search for solution of the exponential matrix equations (3.58). This, typically, leads to the approximation of the matrix exponential by a set of non-linear equations followed by Newton-Raphson iteration and represents an essential complication of the simulation algorithm.

In commercial simulators the formulation and solution of system equations is done automatically from the schematic or netlist (which were assigned to the converter circuit by the user). Difficulties begin, however, when simulation suffers from non-convergence problems, timestep control anomalies, and numeric integration errors. Typically, effort is spent in learning how to overcome nonconvergence problems using the option menu of the simulator's package or using the homothopy technique, and deciding whether the simulation output is accurate or erroneous.

b) Simulation speed

As a natural consequence, the algorithms based on the numerical integration will carry on the simulation much more slowly than those based on the fast time-domain methods. For a simple comparison, if the integration sampling is set to 100 samples per switching period ($h = T_{sw}/100$), then the recursive expressions have to be evaluated 100 times in total to simulate one switching period. In contrast, the fast time-domain algorithm needs to compute 2 or 3 values of state vector within the same simulation interval.

The commercial simulators, to speed up the numerical integration, use the timestep control. The timestep control is an algorithm which determines the timepoints where the circuit equations have to be solved. Thus, the integration step h can become smaller at instances with a higher rate of change of the nodal voltages or currents (e.g. instants of switching, areas of parasitic high-frequency ringing). On the other hand, at the instances of moderate variation of nodal variables, the iteration step can become substantially bigger.

Methods of accelerated convergence, as discussed in section 3.5, allow for a very fast determination of converter steady-state. As a necessary step, however, they include one-cycle time-domain simulation (which may need to be repeated several times) which slow the execution of the overall algorithm down.

The time cost in simulation converter steady-state response using numerical integration is, in contrast to fast time-domain algorithms, more evident with circuits with parasitic parameters such as leakage inductance of magnetic devices and parasitic capacitance of switching elements. These parasitic parameters result in high-frequency ringing (ranging typically from 20 to 200 times greater than switching frequency) which is present at instants of switching. Necessarily, the integration step must become significantly smaller (e.g. $h < T_{sw}/10000$) to guarantee both numerical stability and accuracy of simulation. Consequently, the time for simulation of the steady-state response substantially increases. Contrarily, the simulation speed of fast time-domain algorithm should not suffer in this sense since values of state vector need to be found only (and again) at instants of switching. To speed up the numerical integration, the timestep control algorithms can be used, however, the advantage of the fast time-domain methods is quite evident. An example of high-frequency parasitic ringing is shown in Chapter 5 (e.g. figures 5.22, 5.26, 5.30).

c) Accuracy

The fast time-domain methods, given solution for closed form system equations, compute values of state vectors accurately. Some questions may arise, however, in cases when the accuracy of simulation becomes dependent on the accuracy of determination of the switching times (closed loop simulation). The accuracy of the methods with accelerated convergence into steady-state depends on the strictness of the exit condition from the iteration algorithm (3.75) and, as in the case of the fast time-domain methods, on the accuracy of determination of the instants of switching.

The algorithms based on methods of numerical integration, in contrast, introduce several sources of inaccuracies. Firstly, by definition, these methods approximate the exact solution. The amount of error at a given timepoint depends on both the size of the integration step and the integration method itself. Secondly, in algorithms with ideal switches (such as shown in section 3.2), the accuracy of the instant of switching evaluated by the switching function depends on the integration step. To reduce this error, the integration algorithm may include the reduction of the step size and adjustment of the instant of switching going back and forward in the vicinity of time of switching. The associated cost is, however, an even bigger slow down in the simulation.

d) Convergence

Using any of the methods discussed in this chapter, problems of convergence may occur. Depending on a method, the convergence failure may have a different character.

In the case of “hand derived” numerical methods the selection of the integration step is critical, however in many cases not a difficult problem. With the exception of simulation

resonant type of switching converters and that of parasitic high-frequency ringing, nodal variables of converter change during one topology cycle in, more or less linear fashion. Thus, the size of integration step can be chosen with a reference to the length of the switching period. Usually the setting between 100 and 200 timesteps per switching period should guarantee a reliable convergence of simulation.

In terms of convergence, the commercial simulators are exposed to major challenge when simulating the instants of switching. At these instants the behavior of converter switching elements is highly nonlinear and nodal voltages and currents change at very high rate of change. At such events, the behavior of simulator can become controversial. On one side, the nonlinear behavior of switching devices can introduce the problem of model discontinuities and the simulator may try to solve this problem using increased time step. On the other side, however, the commercial simulator essentially reduces the timestep to accommodate the high rate of change of the nodal variables. This risk of convergence failure is even more extreme if higher level models of switching devices are replaced by the ideal switches.

In the area of fast time-domain methods and methods of accelerated convergence the authors admit problems of convergence ([29], [30], [31]). Also practical experiments which were done in course of this work show that the convergence failures can occur at the computation of switching times. Particularly, they are introduced by a wrong initial guess of switching times which consequently causes the Newton-Raphson iteration to fail. A mechanism of such as failures is now shown on example of computation of switching instant which introduces the DCM mode.

As explained in Chapter 2, the time of switching between the second and third converter topology occurs at the instant when the inductor current falls to zero. The analytical form of this condition is defined in equation (3.57) above and its solution requires New-

ton-Raphson iteration method. A waveform of inductor current of converter operating in DCM mode as can occur during a start-up transient is shown in Fig.3.10.

During the transient the inductor current can be continuous and its magnitude can be several times bigger than in steady-state. As shown in Fig.3.10, the converter achieves a steady-state after n switching cycles. At the steady-state the inductor current is discontinuous and the proper initial guess of the time of switching is $T_{ss} = 0.5(T - T_{s1})$. In the area close to the steady-state, such a guess of the time of switching causes no trouble in iteration algorithm. However, the same guess applied in the area of transient, say at the time T_1 , may lead to a failure of Newton-Raphson iteration. Since the hypothetical waveform of inductor current will fall below zero during the sixth switching cycle, the better guess for the switching instant is $T_{tr} \approx 5.5T$. As is seen from Fig 3.10, the value of proper

Fig.3.10 Waveform of inductor current during start-up transient.

initial guess varies as the transient dies out. At the beginning of simulation the value of proper initial guess can be several times bigger than at steady-state, and, in general, may not be so straight forward to predict.

Similar convergence problems may occur in computing of the length of on-time interval in converters which use voltage mode feedback control. In these converters the length of this interval depends on signals V_{ea} and V_{ramp} and is defined by the equation (3.56). The solution of this equation can be even more challenging because the difference $V_{ea}(t) - V_{ramp}(t)$ may not be monotonous within the interval of a guess.

A method of avoiding failure of Newton-Raphson iteration in methods of accelerated convergence due to a mechanism of converter feedback was presented in [30] and [31]. The presented algorithm includes two iteration loops. In the first loop the feedback is disconnected and for a fixed (guessed) value of duty ratio and guessed value of steady-state a new steady-state is found. In the second iteration loop a correction to duty ratio is computed using the Secant method. Since the Secant method works with two values of variable of interest, two initial guesses are needed and corresponding steady-state have to be found in the first iteration loop at the beginning of overall algorithm. A value of duty ratio corrected in the second iteration loop is passed back to the first loop and, finally, a new value of steady-state can be computed.

In a summary, the methods which exhibit higher simulation speed and higher accuracy (fast time-domain, methods of accelerated convergence) are more prone to fail due to convergence problems. Higher reliability in terms of convergence (methods of numerical integration) however slows the simulation down and introduces inaccuracy. Use of commercial simulators essentially reduces overall simulation set-up effort (derivation of system equations and development of overall simulation algorithm) and allows for a simple

implementation of higher level device models, however the cost is a simulation speed and potential issues with convergence. Also, in terms of further simulation goals (analysis of converter steady-state response to variation of operating conditions, efficiency analysis, integration with thermal simulation programs, etc.), the relative loss of control over simulation can be substantial.

Chapter 4

A Novel Method for Computation of Steady-State Response of Switching DC/DC Converters

4.1. Introduction

Several approaches for determining the steady-state response of switching DC/DC converters have been discussed. Among these, the methods of accelerated convergence into steady-state provide a converter's steady-state response in the shortest time. Major problems with the methods, however, reside in the effectiveness of the iterative computation of state vectors assigned to a converter model. This particularly concerns the computational convergency, number of iterations (CPU time) in relation to the requested accuracy and the overall difficulties associated with implementing the algorithms used.

In this chapter a novel method for determining the steady-state response of switching DC/DC converters is presented. The proposed method reduces the problem of the iterative computation of the state vectors of a converter model to that of finding the time intervals related to the operating topologies of the converter as they occur in steady-state. After the time intervals are found, the converter state vectors are computed using the Newton shooting algorithm.

To guarantee the requested level of converter output voltage, the methods with accelerated convergence into steady-state found in literature require the feedback circuit to be incorporated into the model equations of the converter. The particular value of output voltage of the converter is then enforced through the feedback circuit and through the overall computational mechanism of the steady-state algorithm. Contrarily, the proposed method does not require the implementation of a feedback circuit. Instead, the required output voltage is guaranteed by the incorporation of a “source equation” into the steady-state algorithm. The source equation relates a requested level of converter output voltage in steady-state to the length of the time intervals of the particular topologies which occur within the switching period in steady-state. Two approaches for the derivation of the source equation are shown in this chapter. The first uses the state-space averaging method. The second is based on the direct computation of the average value of the converter’s output voltage using analytical expressions for the closed form solution. The same source equation is obtained when using either approach.

The proposed steady-state method, in comparison to the methods of accelerated convergence and the fast time-domain methods published in literature, has better convergence capabilities. In the previous chapter it was shown that these methods are prone to fail in computation of switching times. The switching times are enforced in the converter circuit by the operation of the feedback circuit and by that of the polarity of the current in the output inductor (recall the discontinuous and continuous conduction mode of operation, DCM and CCM). Unfortunately, during transients caused by the guessing of state vectors,

DCM mode may temporarily occur even with converters designed to operate in continuous conduction mode (CCM). Thus, it is possible, for a converter operating in CCM, to be exposed to unwanted hazards. Further, as an addition to the negative role of a feedback circuit in terms of convergence problems in transients (caused by the guessing of state vectors) is, that the one may also act in changing of the converter's operating mode from CCM to DCM or vice versa. Recall that a steady-state guess is a necessary step used in published methods of accelerated convergence. With the proposed method such problems of convergence failures are not relevant since the implementation of the feedback circuit is not requested and operating mode issues are ruled out.

Another important comparison to make is that the proposed method is simpler in terms of model description. This is due to the fact that the state-space approach is used to formulate model equations and that an implementation of feedback is not required (only model equations for open loop circuit are needed). As a result, the converter model is reduced to a minimum number of states and computational algorithm uses matrices of the smallest size.

A significant advantage results from the capability of the method to achieve a convergence in a fast, accurate and reliable manner. This allows the proposed method to be efficiently used in cases when computation has to be repeated for many different "operating points" of the converter without essential time loss and fear of potential convergence failure while algorithm is executing. An operating point of converter can be defined as a vector of input parameters such as input voltage and output load current. Even device tolerances and device temperature characteristics can be included. At each operating point, a simulation and inspection of switching waveforms can be carried out and the extreme values of the converter's internal variables can be found. The practical meaning of such an approach is to be able to search for the extreme values of the converter's nodal voltages, currents, thermal stress, flux densities, etc. which can occur at various, and, in general, unknown combinations of input parameters. Thus, the proposed method allows for the

development of efficient algorithms for thorough circuit analysis and complex characterization of switching converters. Such algorithms may be considered new and could become very demanded CAD tools used in the practical design of switching DC/DC converters.

Key ideas relating to the proposed method are discussed in detail in section 4.2. The mathematical particulars for the implementation of the algorithms and an example of such an algorithm are presented in section 4.3. In section 4.4, the performance of the method in terms of accuracy, speed and convergence to steady-state at a particular operating point is verified. Three topologies of switching converters have been selected for verification. The conclusions are summarized in section 4.5. Further, the method is also used in all simulation algorithms proposed in Chapter 5 and Chapter 6.

4.2. Principles of the Proposed Method

The proposed steady-state method is based on two key ideas. The first idea is the transfer of the steady-state problem of a converter operating in closed loop to the problem of determining the switching times of the converter operating in open loop. Since the switching times divide the switching period into a series of time intervals, the problem can be referred to as a “time interval problem”. The time interval problem will be discussed in section a). The second idea is to solve the time interval problem using a source equation. As mentioned in the introduction, the source equation relates the required level of a converter output voltage in steady-state to the length of the time intervals and, practically, replaces the function of a feedback circuit in steady-state. The meaning and derivation of the source equation using two different approaches is discussed in section b).

a) Transfer of steady-state problem to a time interval problem

Consider a switching converter operating in open loop with two topological modes within the switching cycle. Generalized waveforms of state vector x and output voltage y in steady-state are shown in Fig.4.1.

Fig.4.1 General waveforms of converter in steady-state.

Referring to section 3.4, a piecewise linear model of a converter is defined by the equations

$$\dot{x} = A_i x + b_i V_g \quad (4.1)$$

$$y = c_i^T x + d_i V_g \quad (4.2)$$

where

$$i=1 \text{ holds for time intervals } nT \leq t < (n+D)T \quad (4.3)$$

$$i=2 \text{ holds for time intervals } (n+D)T \leq t < (n+1)T \quad (4.4)$$

$n = 0, 1, 2, \dots$ is the number of switching cycles

The solution to the equations (4.1) is

$$x_1(t) = e^{A_1 t} X_{10} + \int_{nT}^t e^{A_1(t-\tau)} b_1 V_g \delta \tau \quad (4.5)$$

$$x_2(t) = e^{A_2 t} X_{20} + \int_{(n+D)T}^t e^{A_2(t-\tau)} b_2 V_g \delta \tau \quad (4.6)$$

where the discrete instances nT and $(n+D)T$ refer to the beginning of the time interval for the first and second topologies of the converter and the vectors X_{10} and X_{20} are the values of the state vectors at the beginnings of these intervals.

The fundamental idea of Newton's shooting method (as discussed in the section 3.5) is that, in steady-state, the values of the state vector repeat with the same period as the switching. Thus the value of the state vector at the beginning of the switching period nT is the same,

$$x_1(nT) = x_1(n+1)T = X_{10} \quad (4.7)$$

Also, when switching from the on-time to the off-time topology $(n+D)T$, the state vector remains unchanged by definition,

$$x_1((n+D)T) = x_2((n+D)T) = X_{20} \quad (4.8)$$

After the solutions of the closed form equations (4.5) and (4.6) are substituted into both boundary conditions (4.7) and (4.8), the values of state vector X_{10} and X_{20} can be expressed in the form,

$$X_{10} = (I - e^{A_2 T_2} e^{A_1 T_1})^{-1} (e^{A_2 T_2} K_1 + K_2) V_g \quad (4.9)$$

$$X_{20} = e^{A_1 T_1} X_{10} + K_1 V_g \quad (4.10)$$

where,

$$K_i = A_i^{-1} (e^{A_i T_i} - I) b_i \quad \text{for } i=1,2 \quad (4.11)$$

$$T_1 = DT \quad (4.12)$$

$$T_2 = (1-D)T \quad (4.13)$$

Note that the index n in the expressions (4.9) through (4.13) is left out due to the periodic nature of the converter's operation in steady-state.

Values for the output voltage at the switching times can be calculated from equations (4.2), (4.9) through (4.13) and are of the form,

$$y_{10} = c_1^T ((I - e^{A_2 T_2} e^{A_1 T_1})^{-1} (e^{A_2 T_2} K_1 + K_2) V_g) + d_1 V_g \quad (4.14)$$

$$y_{20} = c_2^T (e^{A_1 T_1} ((I - e^{A_2 T_2} e^{A_1 T_1})^{-1} (e^{A_2 T_2} K_1 + K_2) V_g) + K_1 V_g) + d_2 V_g \quad (4.15)$$

Several important conclusions can be made at this point:

1. For a given duty ratio D , the intervals T_1 and T_2 are computed using expressions (4.12) and (4.13). After the time intervals T_1 and T_2 are known, state vector X_{10} can be computed from (4.9). Basically, the steady-state of the converter is determined using the state vector X_{10} and the length of the time intervals T_1 and T_2 . If requested, the value of the state vector X_{20} and those for the output voltage, y_{10} and y_{20} , can be obtained from expressions (4.10), (4.14) and (4.15). After the state-vector X_{10} and the time intervals T_1 , T_2 are known, the waveforms of state variables and that of the output voltage can be simulated and their average values (X_{ss} , Y_{ss}) can be computed.
2. For various values of duty ratio, different values for the time intervals, state vectors and, finally, average values of the output voltage can be found. For switching converters, lower values of duty ratio cause usually lower average values of output voltage.
3. In principle, the correct value for the duty ratio D can be found by an initial random guess followed by consecutive iterative corrections until the error of the average output voltage meets a prespecified criteria. In literature, a procedure such as this is referred to as a "brute force" method.
4. The function of feedback, in the sense of enforcing an operating point on a converter circuit, is practically disabled. In fact, the Newton's shooting algorithm allows the assignment (for given values of time intervals or that of duty ratio) of a steady-state operating point to a converter circuit (including the feedback circuit) rather than having the feedback circuit enforces the operating point (including the output voltage). Even if it is the feedback circuit which sets the duty ratio in a real circuit (to a value such that output voltage meets the predefined value), the Newton shooting algorithm assumes the duty ratio is already set, "taking the need of a feedback circuit away". The duty ratio (or lengths of time intervals) is the input information for Newton's shooting method and has to be determined

before applying the algorithm. On the other hand, the final consequence of the operation of the feedback circuit at steady-state (this is the average value of the output voltage) is known a priori. Thus, the implementation of a feedback circuit into the converter model practically loses its original meaning allowing the converter can be modeled in open loop.

5. Finally, it is the duration of the time intervals T_1 and T_2 at steady-state, rather than a particular circuit technique used for their generation, which practically determines the average value of the output voltage at steady-state. This conclusion has particular meaning since it allows for:

- the elimination of problems with steady-state methods associated with the design (structural stability of closed loop system, dynamic performance of the feedback circuit causing convergence problems for the steady-state algorithm) and implementation of the feedback circuit;
- the elimination of problems resulting from the implementation of various control schemes (voltage mode, current mode) into steady-state algorithms in general. On the other hand the proposed method allows the feedback circuit to be included and evaluated in steady-state.

6. The shooting algorithm can be easily extended to handle more than two topological changes within the switching period.

7. After the duty ratio (or the time intervals) is known, the computation of the steady-state vectors ((4.9) through (4.15)) and average output voltage is simple and straight forward. Any inaccuracy incurred when determining the duty ratio leads to inaccuracy in values for the state vector and for the output voltage. Convergence problems are, at this point, irrelevant.

In summary, it can be concluded that Newton's shooting algorithm applied to a converter's open loop model can be used to determine the steady-state response of the con-

verter operating in closed loop. It is not necessary to include a feedback circuit in the algorithm. Practically, only a correct value for the duty ratio D (or the values of time intervals assigned to the topologies of the converter in steady-state) is needed to compute the steady-state response of the converter.

b) Derivation of the source equation for computation of time intervals

I. Derivation of the source equation using state-space averaging method

The method of state-space averaging was presented for the first time in [32] and [33] and later discussed in many other works ([37], [58], [59], etc.). The purpose of the method is to find an ac solution or to determine a low-frequency model of switching converter. A converter is modelled as a piecewise linear system and system equations are formulated using the state-space approach. The averaged state-space model is obtained by a weighted summation of the state matrices. The weight of the state matrices is determined by the duration of the topology for which the matrices are derived. To obtain the ac solution the averaged state-space model is further perturbed and linearized at an operating point.

As part of the ac solution for a given duty ratio, the dc solution is derived. The steady-state method proposed in this work, and particularly, the first approach to the derivation of the source equation, uses this dc solution in a “backwards” way, i.e. for given dc value of converter output voltage, the duty ratio (and the time intervals) is computed.

The procedure for the derivation of the dc solution using the state-space averaging method for a converter operating with two topological changes at steady-state ((4.1) through (4.4)) will now be described.

The weighted summation of the state matrices is expressed by equations:

$$\dot{x} = dA_1x + d'A_2x + db_1v_g + d'b_2v_g \quad (4.16)$$

$$y = dc_1^Tx + d'c_2^Tx + dd_1v_g + d'd_2v_g \quad (4.17)$$

where $d' = 1 - d$ and d is the value of duty ratio.

The system described by equations (4.16) and (4.17) can be perturbed by introducing a variation of input voltage v_g as $v_g = V_g + \hat{v}_g$, where V_g is dc line input voltage and $\hat{v}_g$ is the superimposed ac perturbation. Also, the duty ratio may change from cycle to cycle and the variations may be expressed as $d = D + \hat{d}$ where D is the steady-state dc duty ratio and $\hat{d}$ is the ac perturbation. The perturbations of both, the input voltage and duty ratio cause a corresponding perturbation in the state vector $x = X_{ss} + \hat{x}$, where again, X_{ss} is the dc component of the state vector and $\hat{x}$ the superimposed ac perturbation. Consequently, the output y contains a dc component Y_{ss} and a deflection $\hat{y}$. The averaged system (4.16) and (4.17) with implemented perturbation is

$$\begin{aligned} \hat{x} = & ((D + \hat{d})A_1 + (1 - D - \hat{d})A_2)(X_{ss} + \hat{x}) + \\ & + ((D + \hat{d})b_1 + (1 - D - \hat{d})b_2)(V_g + \hat{v}_g) \end{aligned} \quad (4.18)$$

$$\begin{aligned} Y_{ss} + \hat{y} = & ((D + \hat{d})c_1^T + (1 - D - \hat{d})c_2^T)(X_{ss} + \hat{x}) + \\ & + ((D + \hat{d})d_1 + (1 - D - \hat{d})d_2)(V_g + \hat{v}_g) \end{aligned} \quad (4.19)$$

From equations (4.18) and (4.19), and after multiplying the terms in parenthesis and separating the dc terms, the dc solution can be obtained

$$Y_{ss} = -(c_1^T D + c_2^T (1-D))(DA_1 + (1-D)A_2)^{-1}(Db_1 + (1-D)b_2)V_g + (Dd_1 + (1-D)d_2)V_g \quad (4.20)$$

Equation (4.20) shows how the steady-state average value of converter output voltage depends on input voltage, load and duty ratio. Recall that the load current is represented by a load resistor which is incorporated into state matrices A_1 and A_2 . The value on the left side of the equation is known and, in closed loop systems, guaranteed by the operation of the feedback circuit. Thus, for given input and load conditions, the equation can be used to determine the duty ratio of a closed loop system.

It should be noted that equation (4.20) is a general expression for any switching converter operating with two topological changes within a switching cycle at steady-state. Thus it can be used for the large class of switching converters of this type.

II. Derivation of the source equation from average value of converter output voltage

A steady-state average value of converter output voltage Y_{ss} is, by definition, equal to:

$$Y_{ss} = \frac{1}{T} \int_0^T y(t) dt \quad (4.21)$$

In the case of a piecewise linear system with two topological changes within a switching period as described by equations (4.1) through (4.4), the average value of output voltage equals

$$Y_{ss} = \frac{1}{T} \left[\int_0^{DT} y_1(t) dt + \int_{DT}^T y_2(t) dt \right] \quad (4.22)$$

After substituting for y_1 and y_2 from (4.2) into equation (4.22), the average output voltage is

$$Y_{ss} = \frac{1}{T} \left[\int_0^{DT} (c_1^T x_1(t) + d_1 V_g) dt + \int_{DT}^T (c_2^T x_2(t) + d_2 V_g) dt \right] \quad (4.23)$$

Since the input voltage V_g is a constant, the average output voltage can be expressed as

$$Y_{ss} = \frac{1}{T} \left[\int_0^{DT} c_1^T x_1(t) dt + d_1 V_g DT + \int_{DT}^T c_2^T x_2(t) dt + d_2 V_g D'T \right] \quad (4.24)$$

where

$$D' = 1 - D \quad (4.25)$$

At steady-state, the average value for the state vector X_{ss} exists. In [32] it was shown that (for piecewise linear systems as described by expression (4.1) through (4.4)) the average value of state vector, after a linear approximation:

$$e^{DA_1 T} \approx I + DA_1 T \text{ and } e^{D'A_2 T} \approx I + D'A_2 T \quad (4.26)$$

can be obtained in a form

$$X_{ss} = -(DA_1 + D'A_2)^{-1} (Db_1 + D'b_2) V_g \quad (4.27)$$

In steady state, after the substitution of the instantaneous value of state vector $x(t)$ by the average value of state vector X_{ss} ((4.27)) at any instance within switching period, the average value of output voltage Y_{ss} from expression (4.24) can be rewritten as

$$Y_{ss} = \frac{1}{T} \left[c_1^T \int_0^{DT} X_{ss} dt + d_1 V_g DT + c_2^T \int_{DT}^T X_{ss} dt + d_2 V_g D'T \right] \quad (4.28)$$

After the integrals from (4.28) are computed, the expression for averaged output voltage, Y_{ss} , becomes

$$Y_{ss} = \frac{1}{T} c_1^T X_{ss} DT + \frac{1}{T} d_1 V_g DT + \frac{1}{T} c_2^T X_{ss} D'T + \frac{1}{T} d_2 V_g D'T \quad (4.29)$$

or

$$Y_{ss} = (c_1^T D + c_2^T D') X_{ss} + (d_1 D + d_2 D') V_g \quad (4.30)$$

The final expression for average value of converter output voltage is obtained by the substitution of expression (4.27) into the equation (4.30)

$$Y_{ss} = -(c_1^T D + c_2^T (1-D)) (DA_1 + (1-D)A_2)^{-1} (Db_1 + (1-D)b_2) V_g + (Dd_1 + (1-D)d_2) V_g \quad (4.31)$$

This expression is identical to the equation (4.20).

Note:

The linear approximation (4.26) is referred to in literature as the “linear ripple condition”. The condition is well satisfied with all non-resonant type converters. Related discussions can be found in several references (e.g. [32], [33]).

4.3. Implementation Particulars of the Proposed Method

An implementation of the proposed method involves following necessary steps:

- a) Selection of device models and formulation of system equations
- b) Derivation of duty ratio from the source equation
- c) Computation of time intervals
- d) Computation of the state vectors and of the output voltage at steady-state

Steps a) through d) are discussed below in detail. After steady-state is determined, the waveforms of the state variables and that of output voltage can be simulated. A general algorithm for determining steady-state and simulating of converter waveforms is discussed in the part e).

a) Selection of device models and formulation of system equations

The selection of device models for a switching converter, as will be discussed in Chapter 5, should be governed by the final goal of simulation algorithm. To verify the proposed method, simple device models with a minimum number of parasitic elements can be

used. This approach will avoid unnecessary difficulties in deriving the overall model equations for converter.

The system equations for the converter have to be formulated using the state-space approach. This approach is required by the principle of Newton's shooting algorithm. Recall that this algorithm uses the analytical expression for solution of model equations expressed in closed form.

b) Derivation of duty ratio from the source equation

The derivation of an analytical expression for the duty ratio D from equation (4.20) (or (4.31)) can be a difficult task since it involves a matrix inversion. Thus, the solution for the duty ratio will be found numerically using the Newton-Raphson iterative algorithm. The error function $F(D)$ results directly from equation (4.20):

$$F(D) = Y_{ss} + (c_2^T + D(c_1^T - c_2^T))(A_2 + D(A_1 - A_2))^{-1}(b_2 + D(b_1 - b_2))V_g - (d_2 + D(d_1 - d_2))V_g \quad (4.32)$$

Let's define substitutions $G(D)$ and $L(D)$ as follows:

$$G(D) = (A_2 + D(A_1 - A_2))^{-1}(b_2 + D(b_1 - b_2)) \quad (4.33)$$

$$L(D) = A_2 + D(A_1 - A_2) \quad (4.34)$$

Thus the Jacobian of the error function $J(D) = \frac{\partial F(D)}{\partial D}$ is

$$J(D) = \frac{\partial}{\partial D} \{ [Y_{ss} + (c_2^T + D(c_1^T - c_2^T))G(D)]V_g - (d_2 + D(d_1 - d_2))V_g \} \quad (4.35)$$

After the partial differentiation of expression (4.35), the Jacobian is

$$J(D) = (c_1^T - c_2^T)G(D)V_g + (c_2^T + D(c_1^T - c_2^T))\frac{\partial}{\partial D}G(D)V_g - (d_1 - d_2)V_g \quad (4.36)$$

The expression $\frac{\partial G(D)}{\partial D}$ from (4.36) can be expressed as

$$\frac{\partial G(D)}{\partial D} = \frac{\partial L^{-1}(D)}{\partial D}(b_2 + D(b_1 - b_2)) + L^{-1}(D)(b_1 - b_2) \quad (4.37)$$

where the expression for $L(D)$ is defined by equation (4.34)

To find the term $\frac{\partial L^{-1}(D)}{\partial D}$ in equation (4.37), let's first set the product of $L(D)$ and its inverse $L^{-1}(D)$ equal to the identity matrix:

$$L(D)L^{-1}(D) = I \quad (4.38)$$

Then, if we differentiate both sides of the equation above, we obtain:

$$\frac{\partial L(D)}{\partial D}L^{-1}(D) + L(D)\frac{\partial L^{-1}(D)}{\partial D} = 0 \quad (4.39)$$

Finally, the expression for $\frac{\partial L^{-1}(D)}{\partial D}$ results from expression (4.39):

$$\frac{\partial L^{-1}(D)}{\partial D} = -L^{-1}(D) \frac{\partial L(D)}{\partial D} L^{-1}(D) \quad (4.40)$$

Following the idea of the Newton-Raphson algorithm, after an initial guess of the duty ratio (D_0), a correction ΔD can be computed by successive computation of equations (4.33), (4.34), (4.37), (4.40), the Jacobian of the error function $J(D)$ (4.36) and the error function $F(D)$ specified by (4.32). The new value for the duty ratio is

$$D_{new} = D_0 + \Delta D = D_0 - \frac{F(D_0)}{J(D_0)} \quad (4.41)$$

As a standard step of the Newton iteration method, the procedure for computing of values ΔD and D_{new} is repeated until the error (computed by (4.32)) is less than a pre-specified value.

c) Computation of time intervals

The computation of the time intervals T_1 and T_2 using expressions (4.12) and (4.13) is straight forward and does not need any further explanation.

d) Computation of values of state vectors and that of converter output voltage at steady-state

The computation of the space vectors X_{10} , X_{20} and those for the output voltage y_{10} , y_{20} at the times of switching at steady-state using expressions (4.9) through (4.13), (4.14) and (4.15) is straight forward.

e) Overall algorithm of the proposed steady-state method

A general block diagram of the algorithm used for the implementation of the proposed method is shown in Fig.4.2. The core of the algorithm is the Newton-Raphson iteration technique which is used to derive the duty ratio according to some predefined accuracy. Typically switching converters are designed to operate at a duty ratio between 0.25 to 0.75. Thus, the initial guess of the duty ratio D_0 can be set to 0.5. The terms needed to correct the initial guess are specified by expressions (4.33), (4.34), (4.37), (4.40), (4.36), (4.32) and (4.41). The state vector X_{10} can be computed using equations (4.9) and (4.11) through (4.13). Note that the value of the error function $F(D_0)$ in the block diagram is directly deviation from the average output voltage found (for a particular D_0 from the specified value Y_{SS}).

In order to verify the proposed method, a simulation of waveforms of the state variables and that of the output voltage (over a small number of switching cycles) should be included in the algorithm. The computation of average value of output voltage from simulated waveform can be added to verify the accuracy of the algorithm.

Fig.4.2 Block diagram of proposed algorithm.

4.4 Verification of the Proposed Method

The proposed method was evaluated on three frequently used topologies of switching converters: the boost, buck and forward. The parameters of the devices used in the convert-

ers were selected such that the converter's performance met the typical specifications which occur in practice.

In order to verify the steady-state of a converter, two conditions, in principle, have to be satisfied. It first needs be shown that the achieved state is really steady-state, and secondly, that the average output voltage matches a predefined value.

To test the first condition, the state variables (and eventually the output voltage) are computed and compared at relevant switching times. This may be done, for instance, at the beginning and at the end of the switching period. At steady-state it is expected that the difference between two compared state vectors is a zero vector. To demonstrate the performance of the proposed method, the values of the state vector and that of the output voltage were computed at the time of switching over four periods of operation. The results are summarized in tables Tab.4.1, Tab.4.3 and Tab.4.5 below.

From the principle of the proposed method it is apparent that an inaccurate computation of the time intervals for a switching cycle may result in an error of the output voltage. Thus, in order to test the second verification criteria, the average output voltage is computed and compared to the predefined value. In the evaluation section, steady-state waveforms of the output voltage simulated over four switching cycles (Fig.4.3, Fig.4.5 and Fig.4.6) are shown. The average output voltages were computed numerically from the simulated waveforms. A division of 1000 timesteps per switching period was used.

To further evaluate the proposed method, the steady-state response of each converter was determined and evaluated for various operating conditions specified by different combinations of input voltage V_g and output current I_{out} . Tables 4.2, 4.4 and 4.6 list the number of iterations (N) needed to achieve steady-state, corresponding duty ratio (D) and average output voltage, Y_{ss} . The criteria for the average output voltage error (the exit condition for the duty ratio iterations) was set to 1mV.

As another method of evaluation, the steady-state waveforms of the output voltage were compared with ones obtained by numerical integration. Numerical integration was applied to models of open loop converter circuits and carried out until the start-up transient died out. The code for simulation was written in Matlab and the Backward-Euler algorithm was used to carry out the numerical integration. To avoid unnecessary complications of simulation algorithms, a “brute force” approach was chosen. Also, to reduce the number of repetitions in a simulation of converter response using this approach, the values of the time intervals obtained by the proposed method were chosen for the first integration cycle. A step size of 1000 samples per switching period was used for the numerical integration. A second simulation cycle (with the duty ratio changed to the next closest value) did not lead to a more accurate value for the output voltage and served only to confirm the validity of the first simulation.

Example 1: Boost converter

The general circuit of a boost converter operating in continuous conduction mode and its state-space model were discussed in Chapters 2 and 3 respectively. The converter was designed for a step up conversion from 5V to 12V. The parameters of the converter's devices are: inductor inductance $L=80\mu\text{H}$, parasitic resistance of the inductor $R_L=0.07\Omega$, output capacitor capacitance $C=47\mu\text{F}$, effective series resistance of the capacitor $R_c=0.05\Omega$, switching frequency $f_{sw} = 200\text{kHz}$.

Waveforms of the output voltage at steady-state obtained by the proposed method and those obtained by B/E numerical integration (at nominal operating point $V_g=5\text{V}$ and $I_{out}=0.5\text{A}$) are presented in the Fig. 4.3. The average output voltage obtained by the proposed method was 11.9996V. The value obtained by numerical integration (for a duty ratio of 0.592 as computed by the proposed method) was 12.0156V. For the next closest duty

ratio (0.591) the resulting steady-state waveform obtained by numerical integration gives an average output voltage of 11.9881V.

The proposed method allows for the very accurate computation of values of the state vector and that of the output voltage at the instances of switching. Thus an average output voltage much closer to the predefined value of 12V can be found. In case of numerical integration, both the values of the state vector and that of the output voltage show in the simulation algorithm in a discrete form and therefore depend on the size of the integration step. The cost for this is accuracy which, consequently, causes a greater discrepancy between the simulated results and predefined values.

For a closer examination of the steady-state waveforms computed by the proposed method, the values of the state vector and of the output voltage at the instances of switching (X_{10} , X_{20} , y_{10} , y_{20}) for the nominal operating point are shown in Tab.4.1. As shown in this table, the accuracy of computation of the steady-state response is very high and, practically, no error is found.

Switching cycle #:	1		2		3		4	
time [us]	0	2.9585	5.0000	7.9595	10.0000	12.9585	15.0000	17.9585
output voltage y [V]	11.9901	12.0244	11.9901	12.0244	11.9901	12.0244	11.9901	12.0244
Space vector X: I _L [A] V _d [V]	1.1337 12.0151	1.3154 11.9837	1.1337 12.0151	1.3154 11.9837	1.1337 12.0151	1.3154 11.9837	1.1337 12.0151	1.3154 11.9837

Tab.4.1 Steady-state values of the state vector and of the output voltage at switching instants.

The steady-state waveforms of the converter were inspected over an input voltage variations of 4V to 6V and a load variation of 0.3A to 0.7A using a step of 0.1V and 0.1A

respectively. The results of the inspection for the selected nine “corner” operating points are summarized in Tab.4.2.

Fig.4.3 Steady-state waveforms of the output voltage of a boost converter obtained by the proposed method (in the middle) and by B/E integration (at the top and bottom for duty ratio 0.592 and 0.591 respectively).

I _{out} [A]:	0.3			0.5			0.7		
Variable:	D [%]	Y _{ss} [V]	N	D [%]	Y _{ss} [V]	N	D [%]	Y _{ss} [V]	N
V _g =4V	67.29	11.9999	5	67.71	11.9999	5	68.15	11.9999	5
V _g =5V	58.83	11.9997	4	59.17	11.9996	4	59.52	11.9997	4
V _g =6V	50.42	12.0004	2	50.70	11.9996	3	50.98	11.9996	3

Tab.4.2 Duty ratio (D), average output voltage (Y_{ss}) and number of iterations (N) at nine operating points.

Example 2: Buck converter

The general circuit of a buck converter is shown in Fig. 4.4.

Fig.4.4 Buck converter.

The state-space model of the converter operating in continuous conduction mode can be derived in the same way as shown for the boost converter in the Chapter 3. The state matrices found for the on-time topology are:

$$A_1 = \begin{bmatrix} \frac{R_L + R \parallel R_c}{L} & -\frac{R}{L(R + R_c)} \\ \frac{R}{C(R + R_c)} & -\frac{1}{C(R + R_c)} \end{bmatrix}, b_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}, c_1^T = \begin{bmatrix} R \parallel R_c & \frac{R}{R + R_c} \end{bmatrix} \quad (4.42)$$

The state matrices found for the off-time topology are:

$$A_2 = \begin{bmatrix} \frac{R_L + R \parallel R_c}{L} & -\frac{R}{L(R + R_c)} \\ \frac{R}{C(R + R_c)} & -\frac{1}{C(R + R_c)} \end{bmatrix}, b_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}, c_2^T = \begin{bmatrix} R \parallel R_c & \frac{R}{R + R_c} \end{bmatrix} \quad (4.43)$$

The buck converter was designed to step the input voltage from 12V down to 5V. The performance of the proposed steady-state method was evaluated for an input voltage variation of 10V to 14V and for a load current variation of 0.5A to 1.5A. The parameters of devices used for the buck converter: inductor inductance $L=10\mu\text{H}$, parasitic resistance of the inductor $R_L=0.05\Omega$, output capacitor capacitance $C=100\mu\text{F}$, effective series resistance of the capacitor $R_c=0.1\Omega$, switching frequency $f_{sw} = 200\text{kHz}$

The steady-state waveforms of the output voltage obtained by both, the proposed method and B/E numerical integration (at nominal operating point $V_g=12\text{V}$ and $I_{out}=1\text{A}$) are shown in the Fig. 4.5. The average output voltage observed when using the proposed method was 5.0000V. The value obtained by numerical integration, with the duty ratio set to 0.420 (as computed by the proposed method) was found to be 4.9893V. For the next closest duty ratio (0.421), the average output voltage was 5.0012V.

The values of the state vector and that of the output voltage at the instances of switching ($X_{10}, X_{20}, y_{10}, y_{20}$) at the nominal operating point are listed in Tab.4.3. The accuracy of the steady-state response computation is very high and represents essentially no error.

Switching cycle #:	1		2		3		4	
time [us]	0	2.1042	5.0000	7.1042	10.0000	12.1042	15.0000	17.1042
output voltage y [V]	4.9274	5.0710	4.9274	5.0710	4.9274	5.0710	4.9274	5.0710
Space vector X:								
$I_L[\text{A}]$	0.2700	1.7329	0.2700	1.7329	0.2700	1.7329	0.2700	1.7329
$V_c[\text{V}]$	4.9990	4.9991	4.9990	4.9991	4.9990	4.9991	4.9990	4.9991

Tab.4.3 Steady-state values of the state vector and of the output voltage at switching instants.

Fig.4.5 Steady-state waveforms of the output voltage of a buck converter obtained by the proposed method and by B/E integration. The bottom curve was obtained by numerical integration with duty ratio equals 0.420. The curve obtained by the proposed method (at the top) merges with that one obtained by numerical integration with duty ratio set to 0.421.

The steady-state waveforms of the converter were inspected over an input voltage variation of 10V to 14V and a load variation of 0.5A to 1.5A with the step of 0.1V and 0.1A respectively. The results of the inspection for selected nine corner operating points are summarized in Tab.4.4.

I _{out} [A]:	0.5			1			1.5		
Variable:	D [%]	Y _{ss} [V]	N	D [%]	Y _{ss} [V]]	N	D [%]	Y _{ss} [V]	N
V _g =10V	50.25	5.0001	2	50.50	5.0000	2	50.75	5.0001	2
V _g =12V	41.88	5.0000	2	42.08	5.0000	2	42.29	5.0000	2
V _g =14V	35.89	5.0000	2	36.07	5.0000	2	36.25	5.0001	2

Tab.4.4 Duty ratio (D), average output voltage (Y_{ss}) and number of iterations (N) at nine operating points.

Example 3: Forward converter

In line with the concept of this thesis, the circuit of the active clamp reset forward converter with synchronous rectifiers was chosen for experimentation. A detailed discussion about the topology, including the derivation of the related state space model, is covered in Chapter 5, Appendix A and Appendix B. The converter demonstrated here was designed to generate an output of 5V for an input voltage range of 38V to 58V and for loads ranging from 1A to 3A. The parameters of the devices selected for this converter were: number of turns on the transformer primary winding $N_p=22$, number turns on the transformer secondary winding $N_s=6$, magnetizing inductance of primary winding $L_m=1\text{mH}$, total parasitic resistance of the primary winding during on-time $R_p=7\text{Ohm}$, output capacitor capacitance $C=40\text{uF}$, effective serial resistance of the capacitor $R_c=0.004\text{Ohm}$, output inductor inductance $L=10\text{uH}$, parasitic resistance of the inductor winding $R_L=0.04\text{Ohm}$, switching frequency $f_{sw} = 200\text{kHz}$.

The steady-state waveforms of the output voltage obtained by both, the proposed method and numerical integration (at nominal operating point $V_g=48\text{V}$ and $I_{out}=2\text{A}$) are

presented in the Fig. 4.6. The average output voltage obtained using the proposed method was 4.9972V. Using numerical integration with a duty ratio of 0.422 (as computed by the proposed method) a value of 5.0012V was obtained. For the next closest duty ratio value, (0.421), the resulting steady-state waveform had an average value of 4.9903V.

The values of the state vector and that of the output voltage at the instances of switching (X_{10} , X_{20} , y_{10} , y_{20}) at the nominal operating point are shown in Tab.4.5. As with the previous examples, the accuracy of the steady-state response computation is very high and, practically, no error is seen.

Fig.4.6 Steady-state waveforms of the output voltage of a forward converter obtained by the proposed method (in the middle) and by B/E integration (at the top and bottom for duty ratio 0.422 and 0.421 respectively).

Switching cycle #:	1		2		3		4	
time [us]	0	2.1080	5.0000	7.1080	10.0000	12.1080	15.0000	17.1080
output voltage y [V]	4.9915	4.9981	4.9915	4.9981	4.9915	4.9981	4.9915	4.9981
Space vector X:								
I_m [A]	-0.0464	0.0467	-0.0464	0.0467	-0.0464	0.0467	-0.0464	0.0467
V_{cr} [V]	79.9608	79.9608	79.9608	79.9608	79.9608	79.9608	79.9608	79.9608
I_L [A]	1.2573	2.7274	1.2573	2.7274	1.2573	2.7274	1.2573	2.7274
V_c [V]	4.9944	4.9952	4.9944	4.9952	4.9944	4.9952	4.9944	4.9952

Tab.4.5 Steady-state values of the state vector and that of the output voltage at switching instants.

The steady-state waveforms of the converter were inspected over an input voltage variations of 38V to 58V and for load currents ranging from 1A to 3A with a step of 2V and 0.2A respectively. The results of the evaluation at the selected nine corner operating points are summarized in Tab.4.6.

Iout [A]:	1			2			3		
Variable:	D [%]	Y_{ss} [V]	N	D [%]	Y_{ss} [V]	N	D [%]	Y_{ss} [V]	N
$V_g=38V$	51.20	4.9969	3	54.49	4.9970	3	58.17	4.9972	4
$V_g=48V$	40.09	4.9972	2	42.16	4.9972	3	44.41	4.9973	3
$V_g=58V$	32.95	4.9976	3	34.38	4.9976	3	35.91	4.9976	3

Tab.4.6 Duty ratio (D), average output voltage (Y_{ss}) and number of iterations (N) at nine operating points.

4.5. Summary and Conclusions

1. As shown in Tables 4.1, 4.3 and 4.5 the computed values of output voltage and those of the state variables do not show any deflections from steady-state from a practical viewpoint. Also the error in the computed average output voltage is negligible and the achieved accuracy highly exceeds the requirements of practical design.
2. The number of iterations needed to calculate the duty ratio (for a particular converter steady-state) is very low (Tab.4.2, Tab.4.4 and Tab.4.6.). Even for a small average output voltage tolerance (1mV), the typical number of iterations needed was less than five. Thus, the CPU time needed to complete the steady-state computation is negligible.
3. The proposed algorithm never failed in finding the steady-state of a converter. The convergence capabilities result from the characteristics of the source equation

$$Y_{ss} = f_{V_g, R}(D) \quad (4.44)$$

specified by expression (4.20). It is possible to show that, for each parameter V_g and R , the function (4.44) is monotonous on the considered duty ratio interval, and that the Newton-Raphson iteration method (4.3 b)) is practically out of risk of failure.

4. The performance of the proposed method was evaluated for the most common topologies of switching converters. The method can also be directly implemented in algorithms for the analysis of isolated flyback type converters, bridge converters (full-bridge topology, half-bridge topology), interleaved converters and converters with secondary current doubler architectures. The proposed method has no restrictions in terms of mode of control (voltage mode, current mode or average mode control).

5. As seen in the results above, the proposed method allows for the determination of a converter's steady-state in a very fast manner and without the risk of convergence failure. Even the computation of a converter's steady state at many operating points for a specified range of input parameters (input voltage, load current and device tolerances, etc.) can be done within a negligible amount of time. This provides a solid basis for the development of algorithms which can perform not only an efficient simulation of switching waveforms but also analysis of the overall converter response to a range of operating conditions. The meaning of such algorithms for practical design is substantial and will be discussed in Chapter 6.

Chapter 5

Analysis of Active Clamp Reset Forward Converter with Synchronous Rectifiers in Steady-State

5.1 Introduction

The active clamp reset (ACR) forward converter with synchronous rectifiers (Fig.5.1) is one of the most popular topologies of switching DC/DC converters used in design practice today. This topology is part of the large group of converters derived from the basic single-ended isolated forward circuit. The particular implementation varies by the mode of control (voltage mode, current mode), the switching mode (fixed or variable switching frequency), the architecture of the secondary side (single-ended, double-ended, centre-tapped), and by the architecture of output rectifier (diode rectifier, self-driven or externally

driven synchronous rectifiers). The method of active clamp reset itself may be implemented using a few different ways such as with primary positive input rail reset, primary negative input rail reset or with secondary side reset. In comparison with other forward converters (R - C - D reset, diode clamp reset and resonant reset), this circuit allows for a more simplified construction of the isolation transformer, reduced voltage stress across the main primary-side switching transistor, wider range of input voltage, and for the optimal generation of the driving waveforms for the synchronous rectifiers. The use of synchronous rectifiers has a particular meaning for the topology since it allows for a significant improvement in converter efficiency and, consequently, higher power conversion density can be achieved.

Despite the significance of the active clamp reset circuit for the practical use, a detailed steady-state analysis of the topology has not yet been published. Published articles are focussed primarily on the area of circuit development and design. In references [43], [52] and [53], the basic design rules for active clamp reset circuits are described and in [44] and [45], comparative analyses of various reset circuits for forward converters are presented.

Fig.5.1 Basic circuit of ACR forward converter with synchronous rectifiers.

Several implementations for the resetting technique which uses the active clamp principle can be found in references [51] and [54]. As well the development of synchronous rectifier schemes is currently of great interest (e.g. [46] through [49] and patent documents [51], [54], [62] etc.). The most significant published work, from a theoretical prospective, can be considered to be paper [50] where a large signal analysis of the topology is presented. The response of the converter (topology with diode rectifier and positive input line reset) to changes in both, input voltage and load current was analyzed with the main focus on the operation of primary-side resonant LC circuit (will be discussed later in this chapter).

In the effort to complete and systemize the knowledge about the topology of ACR forward converter with synchronous rectifiers, this thesis makes several contributions:

- an accurate analytical model of the ACR forward converter with synchronous rectifiers is derived. This model involves the majority of the parasitic parameters present in a real converter circuit. The state-space approach is used to formulate the converter's model equations.
- switching waveforms of the converter are simulated using the analytical model. Typical waveforms for the topology are shown (the drain-to-source and gate-to-source voltage of primary and secondary switching transistors, magnetizing currents of transformer and output filter inductor, output voltage ripple and total primary current) and compared with those obtained by measurement from a prototype.
- in Chapter 6, the characteristic variations of the critical internal variables of the topology, within a specified range of input voltage and load current are shown, and the extreme values of these variables and the conditions at which they occur are found. Examples of these variables are the peak voltage seen by drain of primary switching transistor, peak voltages seen by drains of synchronous rectifiers, peak gate enhancement of synchronous rectifiers in positive and negative directions, peak magnetizing current of transformer and that of inductor, maximum current ripple of the output inductor and maximum output voltage ripple. The analysis of converter critical variables in response to changes of the input voltage

and load current is referred in this work to as behavioral characterization of switching converter. The obtained results are of significant use in practical design.

Finally, this thesis demonstrates a new approach to the analysis switching converter circuits. In published literature, the behavior of switching converters is analyzed predominantly by hand derived formulas. In rare cases, to find out more about the switching operation of a converter, commercial simulators (e.g. [50]) are used. On the other hand, papers which present analytical methods (e.g. [15],[16],[18],[25]) for simulation switching converter focus primarily on the derivation and verification of these methods rather than on their possible application and use in design practice. Here, several programs were developed to simulate and process the data of converter's switching waveforms. These programs are based on the model of the ACR forward converter with synchronous rectifiers and on the steady-state method, both of which are presented in this work. This, in comparison with use of formulas and commercial simulators, allows for a more systematic and efficient approach to the analysis and design of switching converters.

The principles behind the operation of the ACR forward converter with synchronous rectifiers are explained in section 5.2. The procedure for deriving the real converter model is given in section 5.3 and is broken into three parts. The first, in section 5.3.1, the device models used in the topology are discussed. Then, in section 5.3.2, the model of the ideal ACR forward converter is derived and verified. Finally, in section 5.3.3, the circuit of the ideal ACR forward converter is expanded and the model for a real converter is derived. To verify the accuracy of the model of the real converter, critical waveforms of the nodal voltages and currents are simulated and compared with those obtained by measurement on converter prototype.

5.2 Principle of Operation of ACR Forward Converter with Synchronous Rectifiers

In order to simplify the circuit analysis, let's replace transistors Q_f , Q_r , Q_{fs} and Q_{rs} from Fig.5.1 by ideal switches which have infinite conductance when on, infinite resistance when off, and need a negligible time period for the transition from on status to off status and back. Let's assume that the both transistors Q_f and Q_{fs} are simultaneously on or off and the same applies to the transistors Q_r and Q_{rs} (both can be simultaneously on or off). The transistor couples Q_f , Q_{fs} and Q_r , Q_{rs} change their switching status in opposite phase, i.e. Q_f , Q_{fs} are on at the same time when Q_r , Q_{rs} are off and vice versa. Thus only two circuit topologies, on-time and off-time topology, are allowed.

When the on-time topology is valid, transistors Q_f and Q_{fs} are on and transistors Q_r and Q_{rs} are off. This means that the input voltage is applied across the primary winding of transformer T and that the secondary voltage (of magnitude defined by the transformer turn ratio) is applied across the output LC filter. Consequently, the transformer primary current and output inductor current build up and energy is stored in the cores of magnetic devices.

Conversely, when the off-time topology is valid, transistors Q_f and Q_{fs} are off and transistors Q_r and Q_{rs} are on. The fact that Q_{fs} is off means that current does not flow through the secondary winding and that the primary and secondary circuits are practically independent, allowing them to be treated separately. On the primary side, the magnetizing inductance of the transformer primary winding and the capacitance of the reset capacitor create a resonant LC circuit which is connected between the positive and negative input terminals. Thus, the magnetizing current is enabled to flow into the reset capacitor C_r , causing the voltage across the capacitor to increase, and also, to flow in the opposite direc-

tion causing this voltage to decrease. The reverse magnetizing current forces the operating point of the transformer core to move from the first quadrant into the third quadrant of its hysteresis loop. Due to the active role of the reset capacitor in resetting transformer core, this circuit is called the active clamp reset topology. On the secondary side, a parallel R-L-C circuit exists since transistor Q_{rs} is on. The current through the inductor decreases and the energy stored in the inductor decays.

Waveforms of converter variables such as the voltage across the reset capacitor v_{cr} , voltage across the output capacitor v_c , transformer magnetizing current i_m or output inductor current i_L are discussed in greater detail in section 5.3.2.

It should be noted that rectifier transistor Q_{rs} , when on, allows current to flow through inductor L in both directions. Thus the circuit operates, in comparison with a diode rectifier circuit, only in continuous conduction mode and therefore only two topological modes are needed for the overall analysis of the converter.

5.3 Modeling of ACR Forward Converter with Synchronous Rectifiers in State-Space

The introduction of this section is devoted to the discussion of device models used for the ACR forward converter with synchronous rectifiers. Subsequently, the derivation of a model for the converter is carried out in two steps. The first step is (section 5.3.2) to derive the model of an ideal ACR forward converter. The device models are chosen such that the critical behavior of the converter is preserved. To verify the derived model, the response of the model to the input voltage step is simulated. The waveforms of the state variables at steady-state are then discussed and verified using formulas. For the second step (section

5.3.3), the circuit of the real converter is presented and its model is derived. The waveforms of the nodal voltages and currents which are typically needed for practical design are simulated and the results are compared with the performance of a prototype.

5.3.1 Selection of Device Models

a) Models of magnetic devices

The modeling of the magnetic devices used in switching converters is a specific and wide area of power electronics. Precise models of magnetic devices require material and geometry descriptions for both, windings and core. The internal variables of these devices such as the core flux density, magnetizing inductance, leakage inductance, winding capacitance or winding resistance depend on physical dimensions and device architecture and, thus, are functions of space coordinates. In addition, the magnetic devices are exposed (during switching operation) to non-linear high-frequency waveforms of applied voltage or current. This introduces high-frequency effects in windings such as skin effect, eddy currents and proximity effect what has a reverse impact to the device parameters.

Up to the present, for the purposes of simulation and practical design itself, the parameters of magnetic devices have been expressed predominantly in lumped form. Various examples of such models can be found in many publications ([22] and [36] through [40]). The published models vary by both, the architecture and complexity of parameters.

In general, a lumped parameter model of transformer can include the ideal transformer N_p/N_s , the magnetizing inductance of the primary winding L_m , the leakage inductance of the primary and secondary windings L_{lp} and L_{ls} , the resistance of the primary and secondary windings R_{wp} and R_{ws} , the capacitance of the primary and secondary windings

C_{wp} and C_{ws} , the interwinding capacitance C_{iw} and the magnetic reluctance R_m . An example of such model is shown in Fig.5.2.

Fig.5.2 Transformer model with parasitic parameters.

The ratio of the primary to secondary turns N_p/N_s is the main parameter of a transformer. In order to preserve the dynamic properties of the primary side of the ACR forward converter, the magnetizing inductance L_m should be included. The primary winding resistance R_{wp} models a part of the passive ohmic losses of the device and contributes to the damping of the resonant LC circuit on the converter's primary side. The series winding resistance R_{ws} can be ignored in the case of the ideal converter model since the damping of the resonant LC circuit on the converter's secondary side will be assured by both, the winding resistance of the output inductor R_L (discussed below) and the load resistor R . The magnetic reluctance R_m represents the magnetic losses in the transformer core, and will be also ignored in the model of the ideal converter. In the ACR forward topology, a very low leakage inductance of primary and secondary windings, L_{lp} and L_{ls} respectively, is required. In practice, the magnitude of this leakage inductance uses to be well below 1% of the magnetizing inductance and can be omitted from further consideration. Similarly, the small parasitic capacitances of the windings, C_{wp} and C_{ws} , are not critical for steady-state analysis and will not be considered.

The model of the output inductor (Fig.5.3.), as with the transformer model, includes a magnetizing inductance L , a magnetic reluctance R_{mL} , a winding resistance R_L , a leakage inductance L_{lk} and a winding capacitance C_L . For the purpose of modeling the ideal ACR forward converter the parasitic parameters C_L , R_{mL} and L_{li} can be omitted. The winding resistance R_L will be included in the converter model due to its contribution to damping of the output LC filter.

Fig.5.3 Model of output inductor with parasitic parameters.

b) Model of switching MOSFET transistors

The modeling of power MOSFET switching transistors, as with magnetic devices, is a wide and specific area in the theory of switching power converters. In fact, various approaches can be adopted to create a transistor model.

Perhaps the simplest way of the modeling a switching transistor is to replace it with an ideal switch, i.e. a resistor with zero resistance (a short circuit) when closed, and zero admittance (open circuit) when open, and with transitions between either state occurring in zero time. In reality, there is a non-zero voltage drop across the transistor when it is closed, and non-zero current through when it is open. These properties of the switching

transistor can be modeled using a non-linear kind of “two-value resistor” which has a resistance equal to the on-resistance of the MOSFET when it is on and a high resistance such that a current, equivalent to the leakage current, exists when it is off.

The higher order models of MOSFET transistors involve various parasitic parameters resulting from both the silicon and the package design. Examples of such parameters are the terminal resistances R_g , R_s , R_d , the gate-to-source capacitance C_{gs} , the drain-to-gate capacitance C_{dg} , the drain-to-source capacitance C_{ds} , and the inductance of bond wire connections L_g , L_d , L_s . This model (e.g. [9], [35]) is shown in Fig.5.4.

The model for the power MOSFET transistor has a direct influence on performance of the simulation method and should be selected based on the overall goal of the simulation. For instance, using higher level transistor model requires the derivation of higher order model equations, and can introduce problems with the overall system description (e.g. more than two topological changes within switching period) and the computation of the switching times. This can essentially affect the development of simulation algorithm, cause a substantial increase in simulation time and raise convergence issues. Thus, such a complex model may not be the best choice when simulating converter transient response (e.g. converter response to the load step). However, the high order models should be used when simulating high frequency parasitic ringing (which occur at instances of switching) or when accurately determining power dissipated by the switching devices. In this case, the models for the other devices should also include related parasitic parameters (e.g. the capacitances of transformer and inductor windings, inductance of the layout tracks).

This work is primarily focussed on the analysis of the switching operation of converters in steady-state. In well designed, non-resonant type converters, the high frequency parasitic ringing can be more than 100 times higher than the converter’s switching frequency. Also, such a ringing uses to be well damped within a time slice that is 20 to 40 times shorter than is the length of the switching period (figures 5.22, 5.26, 5.30). The magnitude

Fig.5.4 Model of power MOSFET switching transistor with parasitic parameters.

of the highest spikes of the parasitic ringing may have an influence to the selection of converter devices (i.e. due to the maximum device ratings). However, for the above reasons, the impact of the ringing on both the converter's steady-state operating point and the overall shape of the switching waveforms is not considered critical.

As far as this work is concerned, the switching transistors Q_f , Q_r , Q_{fs} and Q_{rs} will be replaced by non-linear two-value resistors. As is seen from the schematic of the converter in Fig.5.1, the on-resistance of the switching transistors Q_f , Q_r , Q_{fs} and Q_{rs} is always in series with the transformer or the output inductor winding resistances. In the case of modeling of the ideal converter, the resistance of the ideal two-value resistors will be set to zero and infinity when in on and off respectively.

c) Model of capacitors

The model of a capacitor, except for the capacitance C itself, can include parasitic parameters such as an effective series resistance R_c , a series inductance L_c and a parallel leakage resistance R_p . For microwave capacitors, a parasitic parallel capacitance C_p can be added to the capacitor model. An example of such a model ([41]) is shown in Fig.5.5.

Fig.5.5 Model of output capacitor with parasitic parameters.

The serial and parallel resonant frequencies caused by the parasitic parameters L_c and C_p , are typically about two decades higher than the converter switching frequency. Also, for a practical consideration, the leakage current caused by the parasitic resistance R_p can be more than 1000 times smaller than the capacitor ripple current. Therefore, the model of the output capacitor needs only include a capacitance C in series with a parasitic resistance R_c .

5.3.2 Model of Ideal Converter

a) Derivation of model for the ideal ACR forward converter with synchronous rectifiers

The ideal circuit of an ACR forward converter with synchronous rectifiers is shown in Fig.5.6. Based on the intention to use this model with the steady-state method presented in Chapter 4, the piecewise linear model technique and the state-space approach are adopted to formulate the model equations.

Fig.5.6 Model of ideal circuit of ACR converter with synchronous rectifiers.

In the course of the converter operation, energy is stored in the form of magnetic flux in the cores of the magnetic devices (transformer, inductor) and as electrical charge for the capacitors (reset capacitor and output capacitor). Accordingly, the current through the magnetizing inductance of transformer i_m , the current through the output inductor i_L , the voltage across the reset capacitor v_{cr} and the voltage across the output capacitor v_c , are chosen as state variables.

In the section 5.2 was shown that the ideal ACR forward converter with synchronous rectifiers practically always operates in continuous conduction mode and two topologies, on-time and off-time, exist. The two topologies will now be discussed.

On-time topology

The circuit for the on-time topology is shown in Fig.5.7. It is important to emphasize that, even though an infinite resistance for transistor Q_r when it is off is assumed, a resistor of large but finite resistance is used instead (in simulation it is set to 1G Ohm). This finite value has a mathematical purpose which is that if the reset capacitor branch stays open, then the characteristic matrix for topology A_I will include a zero row making it to fail computation of matrix inversion A_I^{-1} (e.g. (3.48)).

Fig.5.7 On-time topology of ACR converter with synchronous rectifiers.

The initial equations for the on-time topology on the primary side are

$$v_g = L_m \dot{i}_m + R_{wp} i_{pt} \quad (5.1)$$

where the total primary current of the transformer i_{pt} consists of the magnetizing current i_m and the reflected secondary current i_p

$$i_{pt} = i_m + i_p \quad (5.2)$$

where the primary current i_p reflected from the secondary side is

$$i_p = \frac{N_s}{N_p} i_L \quad (5.3)$$

For the loop including the reset capacitor applies

$$0 = v_{cr} + R_{rpo} \dot{i}_{cr} \quad (5.4)$$

The initial equations for the secondary side are

$$v_s = L \dot{i}_L + R_L i_L + R_C i_C + v_C \quad (5.5)$$

$$v_C + R_C i_C - R i_O = 0 \quad (5.6)$$

$$i_O = i_L - i_C \quad (5.7)$$

$$v_s = \frac{N_s}{N_p} v_p \quad (5.8)$$

$$v_p = v_g - R_{wp} i_{pt} \quad (5.9)$$

where v_p is the voltage applied across the transformer primary winding, v_s is the transformed primary voltage, i_c is the charging current of the output capacitor and i_o is the output load current.

Detailed steps of the derivation procedure are shown in Appendix A. The results of the procedure are

$$\dot{i}_m = -\frac{R_{wp}}{L_m}i_m - \frac{N_s R_{wp}}{N_p L_m}i_L + \frac{1}{L_m}v_g \quad (5.10)$$

$$\dot{v}_{cr} = -\frac{1}{C_r R_{rpo}}v_{cr} \quad (5.11)$$

$$\dot{i}_L = -\frac{N_s R_{wp}}{N_p L}i_m - \frac{R_{son}}{L}i_L - \frac{R}{L(R+R_c)}v_c + \frac{N_s}{N_p} \frac{1}{L}v_g \quad (5.12)$$

$$\dot{v}_c = \frac{R}{C(R+R_c)}i_L - \frac{1}{C(R+R_c)}v_c \quad (5.13)$$

where the resistance of secondary side R_{son} from equation (5.12) is

$$R_{son} = R_L + R \parallel R_c + \frac{N_s^2}{N_p^2}R_{wp} \quad (5.14)$$

and the symbol $R \parallel R_c$ implies a parallel combination of the load resistor R and the effective serial resistance of output capacitor R_c . The state equations in matrix nominal form are

$$\begin{bmatrix} \dot{i}_m \\ \dot{v}_{cr} \\ \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} -\frac{R_{wp}}{L_m} & 0 & -\frac{N_s R_{wp}}{N_p L_m} & 0 \\ 0 & -\frac{1}{C_r R_{rpof}} & 0 & 0 \\ -\frac{N_s R_{wp}}{N_p L} & 0 & -\frac{R_{son}}{L} & -\frac{R}{L(R+R_c)} \\ 0 & 0 & \frac{R}{C(R+R_c)} & -\frac{1}{C(R+R_c)} \end{bmatrix} \begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_m} \\ 0 \\ \frac{N_s}{N_p L} \\ 0 \end{bmatrix} v_g \quad (5.15)$$

or

$$\dot{x} = A_1 x + b_1 v_g \quad (5.16)$$

where the state matrices for the on-time topology A_1 , b_1 and state vector x are

$$A_1 = \begin{bmatrix} -\frac{R_{wp}}{L_m} & 0 & -\frac{N_s R_{wp}}{N_p L_m} & 0 \\ 0 & -\frac{1}{C_r R_{rpof}} & 0 & 0 \\ -\frac{N_s R_{wp}}{N_p L} & 0 & -\frac{R_{son}}{L} & -\frac{R}{L(R+R_c)} \\ 0 & 0 & \frac{R}{C(R+R_c)} & -\frac{1}{C(R+R_c)} \end{bmatrix} \quad b_1 = \begin{bmatrix} \frac{1}{L_m} \\ 0 \\ \frac{N_s}{N_p L} \\ 0 \end{bmatrix} \quad x = \begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} \quad (5.17)$$

Output equation for the on-time topology

Typically, the output of the converter y is represented by the voltage across the load resistor R

$$y = i_o R \quad (5.18)$$

Since $i_o = i_L - i_c$ and $i_c = C\dot{v}_c$ the final expression for the converter output is

$$y = \frac{RR_c}{R+R_c}i_L + \frac{R}{R+R_c}v_c \quad (5.19)$$

which in matrix form is

$$y = \begin{bmatrix} 0 & 0 & R \parallel R_c & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} \quad (5.20)$$

or

$$y = c_1^T X \quad (5.21)$$

where the state vector c_1^T equals

$$c_1^T = \begin{bmatrix} 0 & 0 & R \parallel R_c & \frac{R}{R+R_c} \end{bmatrix} \quad (5.22)$$

The detailed derivation of the output equation (5.20) can be found in Appendix A.

Off-time topology

During the off-time period (Fig.5.8) the converter circuit consists of two independent resonant LC circuits - one on the primary side and the other one on the secondary side.

Note that the operation of the transformer is disabled and the total primary current i_{pt}

Fig.5.8 Off-time topology of ACR forward converter with synchronous rectifiers.

equals to the magnetizing current i_m . The initial equations for the off-time topology on the primary side are

$$v_g = L_m \dot{i}_m + R_{wp} i_m + v_{cr} \quad (5.23)$$

and

$$\dot{v}_{cr} = \frac{1}{C_r} i_m \quad (5.24)$$

The initial equations for the secondary side circuit are

$$0 = L \dot{i}_L + R_L i_L + R_c i_c + v_c \quad (5.25)$$

$$v_c + R_c i_c - R i_o = 0 \quad (5.26)$$

$$i_o = i_L - i_c \quad (5.27)$$

A detailed derivation procedure is provided in Appendix A. The results are

$$\dot{i}_m = -\frac{R_{wp}}{L_m}i_m - \frac{1}{L_m}v_{cr} + \frac{1}{L_m}v_g \quad (5.28)$$

$$\dot{v}_{cr} = \frac{1}{C_r}i_m \quad (5.29)$$

$$\dot{i}_L = -\frac{R_{sof}}{L}i_L - \frac{R}{L(R+R_c)}v_c \quad (5.30)$$

$$\dot{v}_c = \frac{R}{C(R+R_c)}i_L - \frac{1}{C(R+R_c)}v_c \quad (5.31)$$

where the resistance of secondary side R_{sof} in expression (5.30) is

$$R_{sof} = R_L + R \parallel R_c \quad (5.32)$$

The state equations in matrix nominal form are

$$\begin{bmatrix} \dot{i}_m \\ \dot{v}_{cr} \\ \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} -\frac{R_{wp}}{L_m} & -\frac{1}{L_m} & 0 & 0 \\ \frac{1}{C_r} & 0 & 0 & 0 \\ 0 & 0 & -\frac{R_{sof}}{L} & -\frac{R}{L(R+R_c)} \\ 0 & 0 & \frac{R}{C(R+R_c)} & -\frac{1}{C(R+R_c)} \end{bmatrix} \begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_m} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_g \quad (5.33)$$

or

$$\dot{x} = A_2x + b_2v_g \quad (5.34)$$

where the state matrices for the off-time topology A_2 , b_2 and the state vector x are

$$A_2 = \begin{bmatrix} -\frac{R_{wp}}{L_m} - \frac{1}{L_m} & 0 & 0 & 0 \\ \frac{1}{C_r} & 0 & 0 & 0 \\ 0 & 0 & -\frac{R_{sof}}{L} & -\frac{R}{L(R+R_c)} \\ 0 & 0 & \frac{R}{C(R+R_c)} & -\frac{1}{C(R+R_c)} \end{bmatrix} \quad b_2 = \begin{bmatrix} \frac{1}{L_m} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad x = \begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} \quad (5.35)$$

Output equation for the off-time topology

Since significant similarity between the on-time and off-time circuit on secondary side of the converter, the output equation is

$$y = \frac{RR_c}{R+R_c} i_L + \frac{1}{R+R_c} v_c \quad (5.36)$$

which again, in matrix form, is

$$y = \begin{bmatrix} 0 & 0 & R \parallel R_c & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} \quad (5.37)$$

or

$$y = c_2^T X \quad (5.38)$$

where the state vector c_2^T equals

$$c_2^T = \begin{bmatrix} 0 & 0 & R \parallel R_c & \frac{R}{R + R_c} \end{bmatrix} \quad (5.39)$$

The detailed derivation of the output equation (5.37) can be found in Appendix A.

b) Model verification

To verify the model of the ideal ACR forward converter with synchronous rectifiers, both the model's response to the step of input voltage and the waveforms of state-variables in steady-state are inspected.

The device parameters chosen for the simulation, according to the Fig.5.6, are: $N_p=22$, $N_s=6$, $L_m=1\text{mH}$, $R_{wp}=7\text{Ohm}$, $C_r=100\text{nF}$, $R_{rpf}=1\text{GOhm}$, $L=10\text{uH}$, $R_L=0.05\text{Ohm}$, $C=40\text{uF}$, $R_c=0.1\text{Ohm}$. The switching frequency f_{sw} was set to 200kHz. The resistance of the primary winding R_{wp} was intentionally set high such that the transient of the primary resonant circuit dies out after a small number of oscillation periods. The load resistor R was set to 2.5 ohms and the magnitude of the applied input voltage V_g was set to 48V. A duty ratio (D) of 40% was used.

The code for simulation was written in Matlab and the Backward-Euler algorithm was used to compute the transient response. The waveforms of the state variables during start-up transient are shown in Fig. 5.9 and Fig.5.10. As seen in these figures, the transient dies out and the state variables settle down after ~1.5ms.

At steady-state, the waveforms of the state variables (Fig.5.11 through Fig.5.14) are non-harmonic piecewise linear periodic signals. The waveform of the magnetizing current i_m (Fig.5.11) is a triangular curve, symmetric with respect to the time axis. As expected, the positive values of the falling slope of magnetizing current correspond to the rising curve of the voltage across reset capacitor v_{cr} (Fig.5.12) and the negative values of the falling slope correspond to falling curve of this voltage. At steady-state, the integral of the magnetizing current over one switching period is equal to zero which translates into a quasi-steady waveform of voltage across the reset capacitor. Thus, if the negligible fluctuations caused by the small leakage current through the capacitor during on-time are ignored, the voltage across reset capacitor is the same at the beginning of the off-time period as it is at the end. The peak magnetizing current can be verified by the formula

$$I_{mpk} = \frac{1}{2} \left(\frac{V_g - R_{wp} I_L \frac{N_s}{N_p}}{L_m} \right) \frac{D}{f_{sw}} \quad (5.40)$$

The peak current obtained with this formula, $I_{mpk} = 44.3\text{mA}$ (for $I_L \sim 1.93\text{A}$), agrees with the simulated magnetizing current waveform where $I_{mpksim} = 44.6\text{mA}$.

The steady-state magnitude of the voltage across the reset capacitor v_{cr} can be verified using the volt-second balance rule applied to the transformer primary winding. The formula derived comes in the form

$$V_{cr} = V_g + \frac{D}{D'} \left(V_g - R_{wp} I_L \frac{N_s}{N_p} \right) \quad (5.41)$$

and gives an approximate value $\sim 77.54\text{V}$. The simulated waveform validates this with voltage v_{cr} varying from 77.33V to 77.67V . The peak change in voltage v_{cr} can be verified by the formula

$$\Delta V_{cr} = \frac{1}{4C_{rfs}} \frac{D'}{f_{sw}} I_{mpk} \quad (5.42)$$

which yields a value of 332mV. The value from simulation is 334mV.

A rough value for the mean inductor current i_L (Fig.5.13) and output capacitor voltage v_c (Fig.5.14) can be computed using the following equations

$$I_L = \frac{V_c}{R} \quad (5.43)$$

$$V_c = \frac{N_s}{N_p} \left(V_g - R_{wp} I_L \frac{N_s}{N_p} \right) D \quad (5.44)$$

which gives a current of ~1.93A and voltage of ~4.83V. The average inductor current i_L obtained by simulation is 1.9A. The voltage across the output capacitor shows similar agreement with simulated waveforms on which the voltage varies from 4.748V to 4.771V. The sinusoidal shape of the output capacitor voltage waveform comes from the integration of the increasing and decreasing of the inductor current waveform.

An estimate of the peak-to-peak inductor current ripple can be made using the formula

$$\Delta I_L = \left(\frac{N_s}{N_p} \left(V_g - R_{wp} I_L \frac{N_s}{N_p} \right) - V_{out} \right) \frac{D}{L f_{sw}} \quad (5.45)$$

The computed and simulated values are 1.451A and 1.448A respectively. Finally, the voltage ripple across the output capacitor can be found using the formula

$$\Delta v_c = \frac{\Delta I_L}{8Cf_{sw}} \quad (5.46)$$

The computed and simulated values for this are 22.6mV and 22.8mV respectively.

Fig.5.9 Waveforms of reset capacitor voltage v_{cr} (top curve; 100x diminished) and of transformer magnetizing current i_m (bottom curve) at start-up transient.

Fig.5.10 Waveforms of output capacitor voltage v_c (top curve) and of output inductor current i_L (bottom curve) at start-up transient.

Fig.5.11 Steady-state transformer magnetizing current i_m .

Fig. 5.12 Steady-state reset capacitor voltage v_{cr}

Fig. 5.13 Steady-state output inductor current i_L .

Fig. 5.14 Steady-state output capacitor voltage v_c .

5.3.3 Model of Real Converter

a) Circuit of real ACR forward converter with synchronous rectifiers

The circuit of the real ACR forward converter with synchronous rectifiers is shown in Fig. 5.15. In comparison with the ideal circuit from the previous section, the real circuit includes a driving circuit for the synchronous rectifiers (*SR Driver*), a current sensing

device (R_{sense}), and a feedback control circuit (*Control*). Also, more detailed models of magnetic devices are used.

Fig.5.15 Model of real circuit of ACR forward converter with synchronous rectifiers.

The driving circuit for the synchronous rectifiers (*SR Driver*) consists of a transformer tertiary windings (N_{df} and N_{dr}), a generator of internal voltage (diodes D_1 through D_4 and capacitors C_2 through C_5), resistor dividers (R_1 through R_4) and coupling capacitors C_1 and C_6 . The internal voltage generator and the resistor dividers provide a dc bias voltage for gates of synchronous rectifiers. The tertiary windings of the transformer generate driving waveforms for the synchronous rectifiers Q_{fs} and Q_{rs} based on the magnitude and polarity of the primary voltage. These driving waveforms are coupled with gates of synchronous rectifiers through capacitors C_1 and C_6 . The influence of the SR driver circuit to the operation of main energy storage devices is considered negligible. The control circuit is represented by the symbolic block *Control*. At a steady-state, this block generates the

signals d and d' with a pulse-width such that the output voltage is equal to its predefined value. A detailed description of its structure is not essential due to the nature of the steady-state method presented in Chapter 4 and of the overall goal of this work. The resistor R_{sense} is a model of the primary current sensing device. Track connections are modeled by small resistors R_{tp} , R_{tsn} and R_{tsnf} which are placed between nodes where high currents are expected.

b) Derivation of model for the real ACR forward converter with synchronous rectifiers

The procedure for deriving the state-space model for the real converter is similar to the one for the ideal converter. As before, two topological changes per switching period are considered. The state vector also consists of the same elements, namely the transformer primary magnetizing current i_m , the voltage across the reset capacitor v_c , the output inductor magnetizing current i_L and the voltage across the output capacitor v_c .

On-time topology

The on-time circuit is shown in Fig.5.16. Transistors Q_f and Q_{fs} have been replaced by resistors R_{fpon} and R_{fson} of resistances corresponding to their respective on-resistances. The transistors Q_r and Q_{rs} can be modeled as high resistances R_{rpof} and $R_{rs of}$ which are associated with their drain leakage currents. Practically, however, the leakage current through the transistor Q_{rs} is negligible in comparison with the inductor current I_L , and in order to simplify the derivation procedure, it can be omitted.

Fig.5.16 On-time topology of real circuit of ARC forward converter with synchronous rectifiers.

The primary current i_{pt} branches into currents i_{Rfpon} and i_{cr}

$$i_{pt} = i_{Rfpon} + i_{cr} \quad (5.47)$$

Based on values of the off-resistance of the primary reset transistor R_{rpo} , and the typical voltage across the capacitor C_r , the contribution of current i_{cr} to the total current i_{pt} is negligible. Hence,

$$i_{pt} \approx i_{Rfpon} \quad (5.48)$$

Thus, the voltage drop across the main switching transistor Q_f can be approximated by the product of the total primary current i_{pt} and the transistor on-resistance R_{fpon}

$$v_{fon} = R_{fpon} i_{pt} \quad (5.49)$$

Assuming the above, the initial equations for the primary side of the on-topology circuit are

$$v_g = R_{tp} i_{pt} + L_m \dot{i}_m + R_{wp} i_{pt} + R_{fpon} i_{pt} + R_{sense} i_{pt} \quad (5.50)$$

$$i_{pt} = i_{mt} + i_m + i_p \quad (5.51)$$

In practical circuits, the reluctance current in the output inductor is usually less than 1% of the magnetizing current and can be omitted from the total secondary side current reflected to the primary side:

$$i_p = \frac{N_s}{N_p} i_s = \frac{N_s}{N_p} i_L \quad (5.52)$$

$$R_{fpon} i_{pt} = v_{cr} + i_{cr} R_{rpo} \quad (5.53)$$

$$i_{cr} = C_r \dot{v}_{cr} \quad (5.54)$$

The initial equations for the secondary side on-topology circuit are

$$v_s = R_{ws} i_s + L \dot{i}_L + R_L i_s + R_C i_C + v_C + R_{tsn} \dot{i}_s + R_{fson} i_s + R_{tsn} i_s \quad (5.55)$$

$$v_C + R_C i_C - R i_O = 0 \quad (5.56)$$

$$i_O = i_s - i_C \quad (5.57)$$

$$i_s = i_{mL} + i_L \quad (5.58)$$

$$v_s = \frac{N_s}{N_p} v_p \quad (5.59)$$

$$v_p = v_g - i_{pt} (R_{tp} + R_{wp} + R_{fpon} + R_{sense}) \quad (5.60)$$

Output equation for the on-time topology

The goal of this section is to simulate the nodal voltages and currents of critical importance to the design (e.g. component selection, performance characterization). The waveforms of these variables can be derived from the waveforms of state variables via the output equation. The resulting matrices c_1^T , c_2^T , d_1 , and d_2 have sizes which depend on the number of variables of interest and which can be in the order of tens. The incorporation of such large matrices into the steady-state algorithms is not practical and introduces an unnecessary computation. In reality, the only output variable needed to find converter steady-state is the output voltage. The other voltages and currents of interest can be calculated after the steady-state is found. Thus, the procedure for deriving the output equation is similar to the one shown for the ideal converter circuit. The only difference is that for the real converter the branch of the inductor current I_{mL} and that of the transformer current I_{mt} introduce non-zero state matrix d_1 . Details of this derivation are shown in Appendix B. The equations used to compute waveforms of critical converter variables are provided in Appendix C.

Off-time topology

In the off-time circuit (Fig.5.17) the transistors Q_r and Q_{rs} are modeled by resistors R_{rpon} and R_{rson} . Practically always the leakage currents through the transistors Q_f and Q_{sf} are negligible in comparison with the currents flowing through the transistors Q_r and Q_{rs} and, to simplify the derivation procedure, these circuit branches can be omitted. Based on these assumptions the initial equations for the primary side of the off-topology circuit are

$$v_g = R_{tp}i_{pt} + L_m \dot{i}_m + R_{wp}i_{pt} + v_{cr} + R_{rpon}i_{pt} + R_{sense}i_{pt} \quad (5.61)$$

Considering the high channel resistance of the forward rectifier transistor Q_{fs} , the primary current i_{pt} during the off-time period will not include the reflected secondary current. Thus, the total primary current is

$$i_{pt} = i_{mr} + i_m \quad (5.62)$$

Fig.5.17 Off-time topology of real circuit of ACR forward converter with synchronous rectifiers.

The change in voltage across the reset capacitor in off-time is

$$\dot{v}_{cr} = \frac{1}{C_r} i_{pt} \quad (5.63)$$

The initial equations for the secondary side off-time circuit are

$$0 = L\dot{i}_L + R_L i_s + R_C i_C + v_C + R_{tsnf} i_s + R_{rson} i_s \quad (5.64)$$

$$v_C + R_C i_C - R i_O = 0 \quad (5.65)$$

$$i_O = i_s - i_C \quad (5.66)$$

$$i_s = i_{mL} + i_L \quad (5.67)$$

The complete derivation is shown in Appendix B.

Output equation for the off-time topology

The approach for deriving the output equation is the same as for the on-time topology, i.e. only the converter output voltage will be included in the state matrices. The derivation procedure itself is simpler, in contrast with the on-time topology, since the path $V_g - R_{mt} - R_{mL}$ does not exist. This makes state matrix d_2 a zero matrix. Details of this procedure can be found in Appendix B. As before, the equations used to compute waveforms of critical converter variables are listed in Appendix C.

The state-space models for on-time and off-time topologies, in a matrix nominal form, are as follows

$$\begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} = \begin{bmatrix} -\frac{R_{pon} \parallel R_{mt}}{L_m} & 0 & -\frac{N_s R_{pon} \parallel R_{mt}}{N_p L_m} & 0 \\ \frac{1}{C_p R_{pof} R_{pon} + R_{mt}} \frac{R_{pon} R_{mt}}{R_{pon} R_{pon} + R_{mt}} & -\frac{1}{C_p R_{pof}} & \frac{N_s R_{pon} R_{mt}}{N_p R_{pon} + R_{mt}} \frac{1}{C_p R_{pof}} & 0 \\ -\frac{1}{L} \frac{N_s R_{mt} \parallel R_{pon} R_{pon} + R_{mt}}{N_p R_{pon} R_{pon} + R_{mt}} & 0 & -\frac{1}{L} \left(R_{son} \parallel R_{mt} + \frac{N_s^2 R_{mt} \parallel R_{pon}}{N_p^2 R_{pon} R_{pon} + R_{mt}} \right) & -\frac{R_{mt}}{L(R + R_c) R_{pon} + R_{mt}} \\ -\frac{N_s}{N_p} \frac{R}{C(R + R_c) R_{pon} + R_{mt}} & 0 & \frac{R}{C(R + R_c) R_{pon} + R_{mt}} & -\frac{1}{C(R + R_c)} \left(1 + \frac{R^2}{(R + R_c)(R_{pon} + R_{mt})} \right) \end{bmatrix} \begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_m} \frac{R_{mt}}{R_{pon} + R_{mt}} \\ \frac{1}{R_{pon} + R_{mt}} \frac{1}{C_p R_{pof}} \\ \frac{1}{L} \frac{N_s}{N_p} \frac{R_{mt}}{R_{pon} + R_{mt}} \\ \frac{N_s}{N_p} \frac{R}{C(R + R_c) R_{pon} + R_{mt}} \end{bmatrix} v_g$$

$$y = \begin{bmatrix} R \left(\frac{L}{R_{mt}} - a_{31n} - Ca_{41n} \right) & 0 & R \left(1 + \frac{L}{R_{mt}} - a_{33n} - Ca_{43n} \right) & R \left(\frac{L}{R_{mt}} - a_{34n} - Ca_{44n} \right) \end{bmatrix} \begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} + R \left(\frac{L}{R_{mt}} - v_{3n} - Ca_{4n} \right) v_g$$

$$a_{31n} = -\frac{N_s}{N_p} \frac{1}{L} \frac{R_{mt}}{R_{pon} + R_{mt}} R_{mt} \parallel R_{pon} \quad a_{41n} = -\frac{N_s}{N_p} \frac{R}{C(R + R_c) R_{pon} + R_{mt}} \frac{R_{mt} \parallel R_{pon}}{R_{pon} + R_{mt}}$$

$$a_{32n} = 0 \quad a_{42n} = 0$$

$$a_{33n} = \frac{1}{L} \left(R_{mt} \parallel R_{pon} + \left(\frac{N_s}{N_p} \right)^2 \frac{R_{mt}}{R_{mt} + R_{pon}} R_{mt} \parallel R_{pon} \right) \quad a_{43n} = \frac{R}{C(R + R_c) R_{pon} + R_{mt}} \left(\frac{R_{mt}}{R_{pon} + R_{mt}} - \left(\frac{N_s}{N_p} \right)^2 \frac{R_{mt} \parallel R_{pon}}{R_{mt} + R_{pon}} \right)$$

$$a_{34n} = -\frac{R}{R + R_c} \frac{1}{L} \frac{R_{mt}}{R_{pon} + R_{mt}} \quad a_{44n} = -\frac{1}{C(R + R_c)} \left(1 + \frac{R^2}{(R + R_c)(R_{pon} + R_{mt})} \right)$$

$$b_{3n} = \frac{N_s}{N_p} \frac{1}{L} \frac{R_{mt}}{R_{pon} + R_{mt}} \frac{R_{mt}}{R_{pon} + R_{mt}} \quad b_{4n} = \frac{N_s}{N_p} \frac{R}{C(R + R_c) R_{pon} + R_{mt}} \frac{R_{mt}}{R_{pon} + R_{mt}}$$

Tab.5.1 State-space model for on-time topology

$$\begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} = \begin{bmatrix} -\frac{R_{pof} \parallel R_{mt}}{L_m} & -\frac{1}{L_m} \frac{R_{mt}}{R_{pof} + R_{mt}} & 0 & 0 \\ \frac{1}{C_r} \frac{R_{mt}}{R_{pof} + R_{mt}} & -\frac{1}{C_r(R_{pof} + R_{mt})} & 0 & 0 \\ 0 & 0 & -\frac{R_{xof} \parallel R_{mL}}{L} & -\frac{R_{xof} \parallel R_{mL}}{L(R + R_c)R_{sof} + R_{mL}} \\ 0 & 0 & \frac{R}{C(R + R_c)R_{sof} + R_{mL}} & \frac{R_{mL}}{C(R + R_c)} \left(1 + \frac{R}{(R + R_c)(R_{sof} + R_{mL})} \right) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_m} \frac{R_{mt}}{R_{pof} + R_{mt}} \\ \frac{1}{C_r(R_{pof} + R_{mt})} \\ 0 \\ 0 \end{bmatrix} v_g$$

$$y = \begin{bmatrix} 0 & 0 & R \left(1 + \frac{L}{R_{mL}} a_{33f} - C a_{43f} \right) R \left(\frac{L}{R_{mL}} a_{34f} - C a_{44f} \right) \\ i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix}$$

$$\begin{aligned}
 a_{31f} &= 0 & a_{41f} &= 0 \\
 a_{32f} &= 0 & a_{42f} &= 0 \\
 a_{33f} &= -\frac{R_{mL} \parallel R_{xof}}{L} & a_{43f} &= \frac{R}{C(R + R_c)R_{mL} + R_{sof}} \\
 a_{34f} &= -\frac{R}{R + R_c} \frac{1}{L} \frac{R_{mL}}{R_{mL} + R_{sof}} & a_{44f} &= -\frac{1}{C(R + R_c)} \left(1 + \frac{R^2}{(R + R_c)(R_{mL} + R_{sof})} \right) \\
 b_{3f} &= 0 & b_{4f} &= 0
 \end{aligned}$$

Tab.5.2 State-space model for off-time topology

c) Simulation of switching waveforms of prototype circuit

From the many important nodal voltages and currents needed for practical design, only those which best way characterize the ACR forward topology and verify simulation accuracy are chosen for this discussion. Thus, the following waveforms will be analyzed: drain-to-source voltage of main primary switch, drain-to-source voltage and gate-to-source voltage of the rectifier flyback transistor, total primary current, output inductor current, and output voltage ripple. The results from simulation are then compared with the performance of the prototype.

The simulation algorithm (Fig.5.18), thanks to both the state-space model and the steady-state method derived in Chapter 4, does not require significant development effort. The algorithm starts off with the entry of device parameters, input voltage V_g , and output load current I_{out} . Then, the state-space matrices are computed, followed by the determination of the steady-state. Finally, the waveforms of selected converter variables are derived from those of the state variables.

The device parameters used for the simulation were set according to the parameters of devices which were installed on the prototype. The prototype operated with a 214kHz switching frequency and its output was set to 5.05V. The parameters of prototype devices were as follows:

Transformer: $L_m=1\text{mH}$, $N_p=22$, $N_s=6$, $N_{dr}=N_{df}=4$; $R_{wp}=0.2\text{Ohm}$, $R_{ws}=0.04\text{Ohm}$,
 $R_{mt}=40000\text{Ohm}$

Inductor: $L=8\mu\text{H}$, $R_L=0.05\text{Ohm}$, $R_{mL}=800\text{Ohm}$

Output capacitor: $C=40\mu\text{F}$, $R_c=0.008\text{Ohm}$

Reset capacitor: $C_r=47\text{nF}$

Primary side forward transistor Q_f : $R_{fpon}=0.42\text{Ohm}$

Primary side reset transistor Q_r : $R_{rpon}=10\text{Ohm}$, $R_{rpoj}=1\text{E}9\text{Ohm}$

Secondary side transistors Q_{fs} and Q_{rs} respectively: $R_{fson}=R_{rson}=0.045\text{Ohm}$

Primary and secondary track resistances: $R_{tp}=0.01\text{Ohm}$, $R_{tsnj}=0.008\text{Ohm}$, $R_{tsn}=0.021\text{Ohm}$

Sensing resistors: total parallel resistance $R_{sense}=0.138\text{Ohm}$

SR driver devices: $R_1=R_2=10\text{kOhm}$, $R_3=R_4=100\text{kOhm}$, C_1 through C_4 100nF, V_{FD1} through V_{FD4} 0.7V

Fig.5.18 Block diagram for simulation of switching waveforms of real ACR forward converter.

The waveform of the drain-to-source voltage on the primary switch Q_f is one of the most important internal variables monitored during prototype evaluation, verification testing or failure analysis. In fact, the signal carries information about the switching fre-

quency, duty ratio and transformer reset voltage. Furthermore, from this signal, all the nodal waveforms are derived and the overall switching operation of power train can be assumed. From a design standpoint, the magnitude of this voltage has a direct impact on the selection of the switching transistor Q_f . Plots of the drain-to-source voltage across this transistor as obtained by simulation and measurement are shown in Fig.5.19 and Fig.5.20 respectively. The duty ratio achieved by simulation was 40.45%, very close to the value of 41.6% obtained by a measurement. The peak drain-to-source voltage obtained by simulation was 81.2V and by measurement it was 82.0V.

The voltage across primary winding, transferred to the secondary side, is seen between drain and source of the output rectifier transistors. From figures 5.21 and 5.22 is seen that the simulated and measured waveforms of this voltage (for transistor Q_{rs}) are very similar. The moderate slopes visible on the plots correspond to the voltage drops caused by the parasitic resistances in the converter circuit. In Fig.5.22 a parasitic ringing of high frequency is present at the instance of switching. This ringing is caused by parasitic parameters of devices on the secondary side (drain-to-source capacitance of transistor Q_{rs} and leakage inductance of magnetic devices) which were not considered in the model of real converter.

The gate-to-source voltage of the flyback rectifier transistor Q_{rs} is derived from the primary voltage waveform via the auxiliary windings N_{dr} . To ensure the reliable operation of the converter this voltage has to be verified in both, the positive and negative direction. The waveforms the of gate-to-source voltage as obtained by simulation and measurement (Fig.5.23 and Fig.5.24 respectively) are comparable in terms of magnitude and overall shape. On the measured waveform (Fig.5.24), a small undershoot is visible at the instance of transition from off-time to on-time. The irregularity is due to the parasitic device parameters on secondary side (primarily leakage inductance of the driving winding). This is also the source of the slight asymmetry of the curve during off-time.

In practice, the voltage across the sensing resistor R_{sense} (Fig.5.25 and Fig.5.26) has to be investigated. In the case of current mode control, the signal (with coincidence with the feedback signal) determines the end of the on-time period. In the case of the voltage mode control, the signal typically triggers current limit operations. The waveform is used to monitor the reset process of the transformer and to investigate the saturation point of both magnetic devices - transformer and output inductor. From the simulated waveform (Fig.5.25), the peak primary current is 869mA which is slightly above the measured (and computed) value of 840mA (Fig.5.26). Leading and trailing spikes are observable on the measured waveform which are primarily caused by the charging and discharging of the gates of transistors Q_f and Q_s at times of switching. Despite difficulties in taking a reading, simulated and measured values for the total primary current at the start of the switching cycle were roughly equal (253mA vs. 270mA).

The selection of both the resistance and power rating of the current sense resistors in practical design is not a straightforward task. The difficulties come from the fact that more converter variables are involved in the calculation of primary current. The shape of the primary current itself may make the determination of the power rating challenging. Having the current sense waveform simulated, however, makes the design much simpler and accurate. The advantage of an accurate simulation is particularly of great importance in design when board space is at a premium (e.g. high power density converters).

The inspection of the output inductor current (Fig.5.27 and Fig.5.28) is also critical in many aspects of practical design. The maximum value of the current determines the maximum magnetic flux density of the inductor core. The peak-to-peak ripple affects both, the magnetizing losses in the inductor core and the output voltage ripple. The on-time slope of the current significantly affects the on-time slope of the total transformer primary current, which is important in primary current triggered operations. Thus, analysis of the waveform is necessary when selecting the size of output inductor core, calculating the air gap in the core, selecting the current rating of the output rectifier devices, selecting the primary

side current sensing devices, selecting the output capacitors and when estimating the total power dissipation on secondary side. The waveforms of the output inductor current obtained by simulation (Fig.5.27) and measurement (Fig.5.28) are similar in terms of peak magnitudes and overall shape. The maximum inductor current obtained by simulation was 2.928A whereas the value obtained by measurement was 2.978A. The peak-to-peak ripple of the current was 1.85A in the simulation and 1.96A in practice.

The output voltage ripple is one of the target design parameters, typically specified in the data sheet for the converter. The waveforms of the output voltage ripple obtained by simulation and measurement are shown in Fig.5.29 and Fig.5.30 respectively. Again, very good agreement between the overall shape of the waveforms and the peak-to-peak values is seen. The maximum peak-to-peak output voltage ripple was 29.1mV versus 30.4mV as obtained by simulation and measurement. Parasitic ringing at the instances of switching from the on-time to off-time topology and vice versa can be observed on the measured waveform. The ringing is caused mainly by the parasitic parameters of converter devices on the secondary side (leakage inductances of magnetic devices, track inductances, capacitances of switching transistors, capacitance of output inductor winding, etc.).

Fig.5.19 Simulated drain-to-source voltage of the transistor Q_f

Fig.5.20 Measured drain-to-source voltage of the transistor Q_f

Fig.5.21 Simulated drain-to-source voltage of the reset SR transistor Q_{rs} .

Fig.5.22 Measured drain-to-source voltage of the reset SR transistor Q_{rs} .

Fig.5.23 Simulated gate-to-source voltage of the reset SR transistor Q_{rs} .

Fig.5.24 Measured gate-to-source voltage of the reset SR transistor Q_{rs} .

Fig.5.25 Simulated transformer primary winding current i_{pt}
(simulated as a voltage across $R_{sense} = 0.138 \text{ Ohm}$).

Fig.5.26 Measured transformer primary winding current i_{pt} ($R_{sense} = 0.138 \text{ Ohm}$).

Fig.5.27 Simulated output inductor current i_L .

Fig.5.28 Measured output inductor current i_L (0.5A/div).

Fig.5.29 Simulated output voltage v_{out}

Fig.5.30 Measured output voltage v_{out}

5.4 Summary and Conclusions

The Chapter 5 has an application character with a particular focus on the analysis of the active clamp reset forward converter with synchronous rectifiers in steady-state.

The models for particular devices were chosen such that the simulation of converter switching waveforms satisfactorily reflects the operation of the converter at the switching frequency. The model of the ideal converter was derived. Start-up step response was simulated and the accuracy of this model at steady-state was verified. Simulation results well matched expected behavior.

The model of the ideal converter was upgraded into the model of real converter. Using this model, important converter nodal voltages and currents were simulated. The simulation results were compared with the operation of the prototype. Very good agreement between simulation and behavior of the prototype was demonstrated. The computation of waveforms of 17 converter variables over two switching cycles T_{sw} using a timestep $T_{sw}/400$ took approximately 1sec (Intel Pentium III, 600MHz).

The analytical models of the ACR forward converter, except the simulation of switching waveforms, are suitable for a low frequency characterization of the topology (recall the state-space averaging technique in Chapter 4).

In the simulation algorithm, the steady-state method proposed in Chapter 4 was used for determining converter steady-state. The advantages of the method in terms of convergence, speed and accuracy were confirmed.

Chapter 6

Behavioral Characterization of Switching DC/DC Converters in Steady-State

6.1. Introduction

The analysis of switching waveforms of DC/DC converter at a particular operating point was discussed in the previous chapters. The operating point of the converter was determined by the input voltage and load current. Changing the operating point has a substantial impact on the switching waveforms and also affects converter's efficiency, power dissipated on particular devices and converter's dynamics. The operating conditions, aside from the input voltage and load current, can also involve parameters of converter devices and their tolerances, device temperature characteristics, switching frequency and converter output adjustment range. Due to the great importance for practical design, the anal-

ysis of converter response to changes of operating conditions is selected as the topic for this chapter. Here, such analysis is referred to as a “behavioral characterization”.

Although the results of the behavioral characterization, in sense as defined above, have particular meaning for practice, the topic has not yet been presented in literature in a compact form. Often, the meaning of the behavioral characterization has been narrowed down and terms “the stress analysis” or “the worst case analysis” have been used instead. The operating conditions at which “the worst case” occur are set to the boundary conditions using common sense (i.e. minimum input voltage and maximum load current). The magnitudes of variables of interest are computed using formulas commonly used in design practice (e.g. (5.40) through (5.46)). This approach is typical for the very first steps of converter design ([34], [43], [58]). A more systematic approach to this problem is presented in reference [37] where an evaluation of the selected nodal voltages and currents is made at boundary conditions given by both, maximum and minimum values of input voltage and load current. This reference also suggests to use spreadsheet processors to organize overall computing. Elementary calculations are executed using formulas.

This thesis presents a more general approach to the analysis of converter response to a range of operating conditions. The term of the behavioral characterization is defined. The behavioral characterization is carried out using specific functions referred to as “characteristic variables”. The characteristic variables are derived from converter switching waveforms and evaluated at many points within a range of operating conditions. A search for extreme values of characteristic variables as well as for conditions at which they occur is included.

The mathematical formulation of the behavioral characterization problem is given in section 6.2. The section 6.3 discuss alternative solutions and proposes an efficient algorithm for the behavioral characterization of switching converters. This algorithm is based on the steady-state method presented in Chapter 4. The results of implementation of this

algorithm using the circuit of the ACR forward converter with synchronous rectifiers are shown in the experimental part of this chapter (6.4). The summary and conclusions are presented in section 6.5.

6.2. Formulation of the Behavioral Characterization Problem

The behavioral characterization of switching converters presented in this work is carried out using functions referred to as characteristic variables v_i . These functions can be expressed in a general form as follows:

$$v_i = f_i(p_1, p_2, \dots, p_j, \dots, p_m) \quad (6.1)$$

where the index $i=1,2, \dots, n$ stands for, in general, n characteristic variables, the index $j=1,2, \dots, m$ stands for, in general, m input parameters, and all parameters p_j range from predefined minimum p_{jmin} to maximum p_{jmax} .

The characteristic variables are derived from converter switching waveforms. Since the switching waveforms are functions of state variables, the final expressions for characteristic variables can be made using state variables as well.

Any electrical quantity which has an impact on the performance of the converter and is important from a design standpoint can be defined as a characteristic variable. Three types of characteristic variables can be defined:

- characteristic variables which are related to the instantaneous values of switching waveforms

- characteristic variables which define converter nodal ripples
- characteristic variables which describe average or effective values of switching waveforms

Examples of characteristic variables which are related to the instantaneous values of switching waveforms are: the maximum positive gate-to-source voltage of switching transistors during switching cycle, the peak transformer magnetizing current, and the peak core flux density of the output inductor.

In general, a single switching waveform can carry information about the values of several characteristic variables. For example, a set of characteristic variables assigned to the waveform of gate-to-source voltage of switching transistor Q_{rs} shown in Fig.5.23 v_1 , v_2 and v_3 can be defined as follows:

$$v_1 = V_{Qrsgson}(p_1, p_2, \dots, p_m) = \min_{pos}(v_{Qrsgs}(t, p_1, p_2, \dots, p_m)) \quad (6.2)$$

$$v_2 = V_{Qrsgspeak}(p_1, p_2, \dots, p_m) = \max_{pos}(v_{Qrsgs}(t, p_1, p_2, \dots, p_m)) \quad (6.3)$$

$$v_3 = V_{Qrsgsneg}(p_1, p_2, \dots, p_m) = \min_{neg}(v_{Qrsgs}(t, p_1, p_2, \dots, p_m)) \quad (6.4)$$

where the waveform of gate-to-source voltage of the reset transistor $v_{Qrsgs}(t, p_1, p_2, \dots, p_m)$ is defined by the linear combination of state variables (C.4) and (C.10) shown in Appendix C, v_1 is the minimum positive gate-to-source voltage during the transistor's on-time $V_{Qrsgson}$, v_2 is the peak positive gate-to-source voltage during the transistor's on-time $V_{Qrsgspeak}$ and v_3 is the maximum gate-to-source negative voltage during the transistor's off-time $V_{Qrsgsneg}$. The definition of these variables using the plot of the converter's gate-to-source voltage switching waveform is illustrated in Fig 6.1.

As operation conditions change, the switching waveforms of a converter show significant differences. Consequently, the values of the characteristic variables also vary. The

changes in the waveform of the gate-to-source voltage of Q_{rs} in response to changes in input voltage and load current are shown in Fig.6.2.

Fig.6.1. Definition of characteristic variables for the gate-to-source waveform of transistor Q_{rs} (example).

Fig.6.2 Changes of gate-to-source waveform of the transistor Q_{rs} in response to the variation of input voltage and load current.

Examples of characteristic variables which define nodal ripples of converter are: converter output voltage ripple, reflected input current ripple and flux density ripples in cores of magnetic devices. The output voltage ripple, for instance, can be characterized using variable v_4 defined by expression:

$$v_4 = V_{opp}(p_1, p_2, \dots, p_m) = \max(v_{out}(t, p_1, p_2, \dots, p_m)) - \min(v_{out}(t, p_1, p_2, \dots, p_m)) \quad (6.5)$$

where the function $v_{out}(t, p_1, p_2, \dots, p_m)$ is specified by the expressions (B.75) and (B.128) in Appendix B and for the time t applies $t_0 \leq t < t_0 + T$.

Finally, examples of characteristic variables related to average or effective values of switching waveforms are: power dissipated in current sensing resistors v_5 and copper losses in winding of the output inductor v_6 . Related expressions are as follows:

$$v_5 = P_{Rsense}(p_1, p_2, \dots, p_m) = R_{sense} \frac{1}{T} \left(\int_{t_0}^{t_0+T} i_{pt}^2(t, p_1, p_2, \dots, p_m) dt \right) \quad (6.6)$$

$$v_6 = P_{Lw}(p_1, p_2, \dots, p_m) = R_L \frac{1}{T} \left(\int_{t_0}^{t_0+T} i_{Lt}^2(t, p_1, p_2, \dots, p_m) dt \right) \quad (6.7)$$

where currents i_{pt} and i_{Lt} are defined by the expressions (C.6), (C.11), (C.7) and (C.12) respectively in Appendix C and for the time t applies $t_0 \leq t \leq t_0 + T$.

A direct benefit for practical design is seen when the characteristic variables are compared with a set of design restrictions. This can be done in terms of the converter's maximum device ratings (gate-to-source thresholds, gate-to-source and drain-to-source maximum ratings for switching MOSFETs, saturation flux densities of magnetic devices, power rating of current sensing devices, etc.) and also in terms of the converter's performance specification (output voltage ripple, input reflected ripple current, etc.). The set of restrictions can be written in general form as follows:

$$v_i(p_1, p_2, \dots, p_m) > r_i \text{ or } v_j(p_1, p_2, \dots, p_m) < r_j \quad (6.8)$$

where symbols r_i and r_j represent i -th and j -th design restriction.

As an example, in the case of the control of transistor Q_{rs} , the following inequalities must be satisfied for a reliable design:

$$V_{Q_{rs}gson}(V_g, I_{out}) > V_{Q_{rs}sth} \quad (6.9)$$

$$V_{Q_{rs}gspeak}(V_g, I_{out}) < V_{Q_{rs}gh} \quad (6.10)$$

$$0 > V_{Q_{rs}gsneg}(V_g, I_{out}) > V_{Q_{rs}gl} \quad (6.11)$$

for any combination of the input voltage V_g and load current I_{out} from defined ranges (V_{gmin} V_{gmax}) and (I_{outmin} I_{outmax}).

The inequalities (6.9) through (6.11) indicate that for any input voltage and load current, the gate-to-source voltage of the transistor Q_{rs} should be higher than the gate threshold voltage ($V_{Q_{rs}sth}$) and lower than the maximum gate voltage rating ($V_{Q_{rs}gh}$) when the transistor is on. Also, during the transistor's off period, this voltage has to be less than the gate threshold voltage but still higher than the device's maximum negative gate-to-source voltage rating ($V_{Q_{rs}gl}$).

Behavioral characterization does not only show how the important internal variables of switching converter vary in response to changes in operating conditions, but it can also involve a search for their peak values (minimum or maximum) as well as for the conditions at which they occur. This approach is justified by the fact that the maximum (or minimum) values of the different characteristic variables can occur at different and, generally unknown, operating conditions. A general formulation of the problem can be made using the following expressions

$$v_{imax} = \text{Max}(f_i(p_1, p_2, \dots, p_m)) = f_i(o_{iMax}) \quad (6.12)$$

$$v_{jmin} = \text{Min}(f_j(p_1, p_2, \dots, p_m)) = f_j(o_{jMin}) \quad (6.13)$$

where the vectors

$$o_{iMax} = (t_{mx_i}, p_{1mx_i}, p_{2mx_i}, \dots, p_{mmx_i}) \quad (6.14)$$

$$o_{jMin} = (t_{mn_j}, p_{1mn_j}, p_{2mn_j}, \dots, p_{mmn_j}) \quad (6.15)$$

mean operating points where the characteristic variables v_i and v_j give the maximum and minimum value respective.

For example, Fig.6.2 shows that the maximum negative gate-to-source voltage $V_{Qrsg-sneg,max}$ and the maximum positive gate-to-source voltage $V_{Qrsgspeak,max}$ belong to different plots obtained with different operating conditions. Consequently, for practical design, the conditions at which the extreme values of the characteristic variables occur are used for converter device rating evaluations. They are also recommended for a prototype verification and manufacturing tests.

6.3. Solution for the Behavioral Characterization Problem

The behavioral characterization of switching converter can be considered a challenging task if precise analytical expressions for the characteristic variables ((6.1) through (6.7)) and their extremes ((6.12) and (6.13)) are to be found. Major complications come from derivation and further processing (determining of switching times, derivation of Jacobian function, etc.) of equations which accurately describe behavior of switching converter in steady-state as a piecewise linear circuit. This problem can be simplified if a discrete ("point-by-point") approach is adopted. This approach can be viewed as evaluating

the converter's characteristic variables at many operating points. Assuming that converter steady-state associated with the particular operating point can be determined, the evaluation can be done using formulas typically used in design procedure, commercial simulators, and various analytical methods.

The formulas which are used in design procedure (e.g. (5.40) through (5.46)) can provide a relative efficient way for computing of values of characteristic variables. The problems of computational convergence is not relevant because the formulas are derived for converter steady-state. Results can be obtained quickly even for many input parameters and many operating points. Conversely, results obtained using these formulas have an approximative or an "envelope" character, the formulas are very often not known and need to be derived for each new circuit. Typically, difficulties with deriving the formulas are introduced by the implementation of large amounts of parasitic device parameters, by the accurate computation of switching instances (which need to be done also using formulas), and by the complexity of the converter circuit.

The other solution for the behavioral characterization problem is to use commercial simulators. (The general advantages and disadvantages of commercial simulators were discussed in Chapter 3.) Since the built-in commands for determining the steady-state (e.g. bias point calculation) are not applicable for switching converter circuits, the related procedure should involve:

1. simulation of the switching operation in the time-domain at a particular operating point
2. determination of steady-state
3. inspection of simulated waveforms for one switching cycle
4. storage of the values of the characteristic variables
5. repetition of the procedures 1 - 4 for other operating point
6. evaluation (e.g. plot) of the characteristic variables over the specified range of input parameters.

The disadvantages of this approach include the large amount of time consumed by the time-domain simulation, convergence issues, detection of steady-state, and difficulties with repeating procedures 1 - 4 using the set of commands provided by the commercial simulator.

In comparison to the use of formulas and commercial simulators, the analytical methods (fast time-domain methods, steady-state methods) can introduce more options for the behavioral characterization problem. Although the overall procedure of characterization may involve all steps 1 - 6 as specified above, the advantages of the analytical methods are in the short time needed for determining the converter steady-state, satisfactory accuracy and relative programming freedom. Based on these advantages, an efficient algorithm for solving the behavioral characterization problem is proposed below. The problem of determining the steady-state of the converter is solved using the method proposed in Chapter 4. The choice of using this steady-state method is based on the benefits in terms of convergence, speed and accuracy (Chapter 4).

The block diagram of the proposed method (Fig.6.3) includes two nested loops, one for each input parameter p_1 and p_2 (e.g. input voltage and load current). Since the input parameter may cause a change in the converter state-space model (e.g. a change of load current cause changes to the characteristic matrices A_1 and A_2), the model of the converter also has to be adjusted accordingly. After the steady-state is found, waveforms of interest are computed over one switching cycle using a predefined number of samples. From the waveforms, the values of all characteristic variables v_k are found and stored. If detected, the extreme values of the characteristic variables and the associated values of the input parameters are updated. The procedure of setting a new operating point, determining the steady-state, and finding and evaluating the values of the characteristic variables repeats over all the predefined combinations of the input parameters $[p_{1,i}, p_{2,j}]$. The proposed algorithm can easy accommodate more input parameters.

Fig.6.3 Block diagram for behavioral characterization of switching converter using two input parameters.

6.4. Experimental Results

The circuit of the ACR forward converter was chosen for experimentation. The real converter model and the device parameters specified in Chapter 5 were used. The characteristic variables associated with the drain-to-source and gate-to-source waveforms of switching transistors Q_f , Q_{fs} and Q_{rs} , output inductor current I_L , ohmic losses in the inductor winding P_{Lw} and converter output voltage ripple were chosen for the characterization over changes of the input voltage and load current. The range of input voltages was from 27.5V to 70V. The variation of the load current was specified as 0.5A to 3.0A. Also, the behavior of the output voltage ripple over changes to the inductance and capacitance of the output filter was characterized.

Example 1: Simulation of peak drain-to-source voltage across main switching transistor Q_f in response to the variation of input voltage and load current

The typical waveform of the drain-to-source voltage across the main transistor switch Q_f (at given input voltage and output load current) was shown in Fig.5.19 and Fig.5.20 respectively. The maximum peak value of the waveform $V_{Qf,dspeak}$ over a switching period was chosen as a characteristic variable. The behavior of the variable in response to the variation of input voltage and load current is plotted in Fig.6.4. As is seen from the plot, the variable creates a characteristic “saddle” type of surface with a minimum close to the minimum input voltage. However, the voltage grows significantly as the input voltage approaches the specified minimum. The actual maximum peak voltage (108.86V) occurs at 27.5V input voltage and 3A load current. For purposes of the practical design, these conditions would be critical in the selection the drain-to-source voltage rating of the main switch transistor Q_f .

The magnitude of the characteristic variable $V_{Qfdspeak}$ is given by the sum of the input voltage and transformer reset voltage. The characteristic “saddle” type behavior of the variable in response to the variation of input voltage and load current is caused by the variations the transformer reset voltage - the magnitude of this voltage decreases at high input voltages and increases at low input voltages. The “averaging effect” of the addition of the input voltage and reset voltage can be particularly useful in design of internal voltage generators. The resulting output voltage of such a generator over input voltage and load current variations creates, by a definition, a surface similar to the one on Fig.6.4. Since the internal voltage is typically used to power various converter circuits (pwm controllers, feedback circuitry, etc.) it is necessary to know both, the conditions at which the maximums and minimums occur and the magnitudes of these extremes as well.

Fig.6.4 Variation of maximum drain-to-source voltage of primary switch transistor Q_f in response to the variation of input voltage and load current.

The knowledge about the minimum values of the internal voltage is critical, since it does not occur directly at the corners of specified range of input voltage or load current. The derivation of an accurate analytical expression for the curve of minimum internal voltage can be a challenging task. The solution to the problem, however, can be found with relative ease using the simulation algorithm presented in the Fig.6.3. The curve of minimum voltage found using the algorithm is shown in the Fig.6.5.

Fig.6.5 A path of minimum drain-to-source voltage of primary switch transistor Q_f in response to the variation of input voltage and load current.

Example 2: Simulation of peak drain-to-source voltage across secondary switching transistors Q_{rs} and Q_{fs} in response to the variation of input voltage and load current

The waveform of the drain-to-source voltage across the secondary switching transistor Q_{rs} at converter nominal operating point was shown in Fig.5.21 and Fig.5.22 respectively. The maximum peak value of the waveform $V_{Q_{rs}dspeak}$ and also the maximum peak value of the drain-to-source voltage of the forward secondary rectifier transistor $V_{Q_{fs}dspeak}$ over a switching period were chosen as characteristic variables. Their behavior in response to the variations of input voltage and load current is shown in Fig.6.6.

Fig.6.6 Variation of peak drain-to-source voltage of SR transistors Q_{rs} (upper surface at low input voltages) and Q_{fs} in response to the variation of input voltage and load current.

The opposite behavior of these variables is caused by changes in the voltages (input or forward voltage during on-time and reset voltage during off-time) present across transformer primary winding at various input voltage and output load combinations. As we discussed in the example 1, at low inputs, the forward voltage across the transformer primary winding is low and the reset voltage starts to increase. At high inputs, the forward voltage is high and the magnitude of the reset voltage decreases. Thus, the maximum values of the characteristic variable $V_{Q_{fsd}peak}$, in comparison to the maximum values of the characteristic variable $V_{Q_{rds}peak}$, occur at exactly opposite input voltages. For purposes of practical design, these conditions are critical when it comes to selecting the proper drain-to-source rating of the synchronous rectifiers. The maximum values of the characteristic variables obtained by simulation are: $V_{Q_{rds}peak} = 19.11V$ (at $V_g = 70V$ and $I_{out} = 0.5A$) and $V_{Q_{fsd}peak} = 22.19V$ (at $V_g = 27.5V$ and $I_{out} = 3.0A$).

Example 3: Simulation of peak gate-to-source voltage across secondary switching transistors Q_{rs} and Q_{fs} in response to the variation of input voltage and load current

Proper operation of the synchronous rectifiers depends, primarily, on the generation of accurate driving signals applied to the gates of the switching transistors (Q_{rs} and Q_{fs}). The most critical step in the design of the driving circuit for these transistors (shown in Fig.5.15) is the selection of the turns ratio of the transformer. While a sufficient voltage has to be applied to the gates of transistors Q_{rs} and Q_{fs} such that a small channel resistance is assured when they are on, too much voltage introduces significant gate charge losses and raises thermal and efficiency issues. In extreme cases, an excessive magnitude of the voltage can violate the maximum gate-to-source rating resulting in the catastrophic failure of the device. The simulated driving waveforms has a particular sense, since the driving waveforms are not perfect rectangular signals and magnitude of positive and negative gate voltage of both transistors change significantly over variations of input voltage and output current.

An example of the changes in the driving waveforms of the synchronous reset transistor Q_{rs} in response to variation in input voltage and load current was shown in Fig.6.2. The maximum positive ($V_{Q_{rs}gspeakpos}$, $V_{Q_{fs}gspeakpos}$) and the negative peak values ($V_{Q_{rs}gspeakneg}$, $V_{Q_{fs}gspeakneg}$) of the gate-to-source waveform of both synchronous rectifier transistors Q_{rs} and Q_{fs} over the switching period were chosen as the characteristic variables. The variations of these characteristic variables as a result of input voltage and load current changes are shown in Fig.6.7 and Fig.6.8.

Fig.6.7 Variation of maximum and minimum gate-to-source voltage of reset SR transistor Q_{rs} in response to the variation of input voltage and load current.

The positive gate voltage of the secondary forward transistor Q_{fs} and the negative gate voltage of the secondary reset transistor Q_{rs} are derived from the voltage applied across the transformer primary winding when main transistor Q_f is on (on-time topology). Thus, the gates of synchronous rectifier transistors see the input voltage (reduced by the passive voltage drops across parasitic resistances in the primary loop) transformed to the secondary side. Therefore the values of the characteristic variables $V_{Q_{fs}gs_peakpos}$ and $V_{Q_{rs}gs_peakneg}$, in response to the variations of input voltage and load current, create more-less linear surfaces.

Fig.6.8 Variation of maximum and minimum gate-to-source voltage of forward SR transistor Q_{fs} in response to the variation of input voltage and load current.

The negative gate voltage of secondary forward transistor Q_{fs} and the positive gate voltage of secondary reset transistor Q_{rs} are derived from the voltage applied across the transformer primary winding when main transistor Q_f is off (off-time topology). Thus, the gates of the synchronous rectifier transistors see a primary reset voltage transformed to secondary side. Therefore the values of the characteristic variables $V_{Q_{fs}gspeakneg}$ and $V_{Q_{rs}gspeakpos}$, over variations in input voltage and load current, create a hyperbolic surface. The maximum values of these characteristic variables obtained by simulation are: $V_{Q_{fs}gspeakpos} = 10.49V$ ($V_g=70V$, $I_{out}=0.5A$), $V_{Q_{fs}gspeakneg} = -15.34V$ ($V_g=27.5V$, $I_{out}=3A$), $V_{Q_{rs}gspeakpos} = 17.38V$ ($V_g=27.5V$, $I_{out}=3A$) and $V_{Q_{rs}gspeakneg} = -10.41V$ ($V_g=70V$, $I_{out}=0.5A$).

For purposes of practical design, to select the proper number of turns for the driving transformer (N_{df} and N_{dr}), it is necessary to verify the peak positive gate voltage of the secondary forward transistor Q_{fs} at maximum input voltage and minimum load current. The maximum negative gate voltage of the transistor should be verified at minimum input voltage and maximum current. To verify the operating conditions of the secondary reset transistor Q_{rs} , the peak positive gate voltage should be checked at minimum input and maximum load current. The peak negative gate voltage of the transistor should be verified at maximum input voltage and minimum current.

Example 4: Simulation of output inductor current in response to the variation of input voltage and load current

The importance of the analysis of the output inductor current was explained in the previous chapter. In this example the following characteristic variables associated with the waveform of the inductor current (Fig.5.27 or Fig.5.28) are defined: peak output inductor

current I_{Lpeak} , peak-to-peak ripple of the inductor current I_{Lpp} and ohmic losses in inductor winding P_{Lw}

The peak current through the output inductor I_{Lpeak} (Fig.6.9) reaches its maximum value at maximum input voltage and maximum load current. This operating condition is critical for determining the maximum flux density in the inductor core and selecting the proper size of the air gap in the inductor core. The maximum value of the inductor current was 4.14A.

Fig.6.9 Variation of peak output inductor current i_L in response to the variation of input voltage and load current.

The variations in the peak-to-peak output inductor ripple current I_{Ltp} in response to the variation of input voltage and output current are shown in Fig.6.10. The maximum value of the ripple current occurs at maximum input voltage and maximum load current. The magnitude of the ripple current directly translates into maximum thermal core stress, and it also affects the output voltage ripple of the converter. Thus, this condition is critical in terms of the selection of the magnetizing inductance of the inductor and for evaluating the magnetizing losses of the core. The maximum value of the peak-to-peak ripple current obtained by simulation was 2.27A.

Fig.6.10 Variation of peak-to-peak output inductor current ripple in response to the variation of input voltage and load current.

The results of simulation of the ohmic losses in the inductor winding P_{Lw} are shown in Fig. 6.11. As expected, the maximum, 0.47W, occurs at maximum input voltage and maximum load current.

Fig.6.11 Variation of winding losses on output inductor in response to the variation of input voltage and load current.

Example 5: Simulation of converter output voltage ripple in response to the variation of input voltage and load current

The typical waveform of the output ripple voltage was shown in Fig.5.29 and Fig.5.30. In this example, the difference between the maximum and minimum value of the

waveform, V_{outp-p} , is chosen as the characteristic variable. The behavior of this variable at different input voltages and load currents is shown in Fig.6.12. As is seen from the figure, the maximum ripple (34.01mVp-p) occurs at maximum input and maximum load. This is in agreement with the inductor ripple current plot where the maximum occurs at the same conditions. It should be noted, however, that at low input voltages, the maximum output ripple voltage can occur at minimum loads. This paradoxical behavior (in comparison with circuits with diode rectifiers) can be explained by the fact that, at low output currents, the output inductor current can flow in the reverse direction. Thus, the output capacitor is loaded by the both, the load resistance and output inductor. Consequently, the voltage across the capacitor drops more significantly at lower loads.

Fig.6.12 Variation of output voltage peak-to-peak ripple in response to the variation of input voltage and load current.

Example 6: Simulation of converter output voltage ripple in response to the variation of output filter parameters

The simulation of converter output voltage ripple with variations in the inductance and capacitance of the output filter ($V_{out-p-p}(L, C)$) has two principal uses: the performance evaluation and in the design itself. The inductance of the output inductor and capacitance of the output capacitor may vary significantly as a result of temperature changes and depending on manufacturing tolerances. Thus, from the performance evaluation aspect, it is necessary to verify whether the converter meets the specification in the worst case conditions. On the other hand, the different devices which are available on the market translate into different component costs and board space requirements. From a design aspect, consequently, it is useful to know whether more board space should be allocated for a bigger size inductor or whether more capacitors should be installed instead as well as how much which device configuration affect the component cost.

The behavior of the output voltage ripple as a result of variation in inductance (4uH through 12uH) and capacitance (35uF through 45uF) of the output filter (as can be expected at various ambient temperature operating conditions) are plotted in Fig.6.13. As expected, the maximum output voltage ripple (61.5mVp-p) occurs when both, the inductance and capacitance are low.

The simulation of output voltage ripple for different values of L , C and effective serial resistance of the output capacitor R_c (Tab.6.1) also confirmed that:

- increasing the inductance can be more efficient than increasing the capacitance
- effectiveness of increasing the capacitance to reduce the ripple is better with lower values of R_c

No.	R_c [mOhm]	L [μ H]	C [μ F]	V_{pp} [mV]	Delta [%]
1	12	6	35	46.1	reference
2	12	6	45	38.6	16.3
3	12	7.72	35	35.8	22.4
4	4	6	35	41.3	reference
5	4	6	45	32.4	21.5
6	4	7.72	35	32.1	22.3

Table 6.1 Output ripple in response to the variation of output filter parameters.

Fig.6.13 Variation of output voltage peak-to-peak ripple in response to the variation of output filter parameters.

6.5. Summary and Conclusions

In Chapter 6 the problem of the behavioral characterization of switching converters was introduced. The behavioral characterization is defined as an analysis of converter overall steady-state response to a range of operating conditions. The term of characteristic variable was defined. The behavioral characterization was carried out using the characteristic variables.

The meaning of behavioral characterization of switching converters for the practical design was explained. An efficient algorithm for the behavioral characterization of switching converters using the characteristic variables was proposed. Implementation examples involved characterization of the active clamp reset forward converter with synchronous rectifiers.

Simulation speed of the proposed algorithms is of a great importance for design practice. The simulation of 10 characteristic variables at 200 operating points using a timestep $T_{sw}/100$ takes approximately ~23.5sec (Intel Pentium III, 600MHz). Since the design of the switching converter has a strong iterative character, any changes of converter device parameter can be evaluated using the proposed algorithms quickly. Thus, the overall design process can advance with essentially no time loss caused by time consuming and erroneous hand calculations.

In the simulation algorithm, again, the steady-state method proposed in Chapter 4 was used for determining converter steady-state. Similarly to the previous chapters, the advantages of the method in terms of convergence, speed and accuracy were confirmed.

Chapter 7

Conclusions

7.1. Summary

This thesis has been devoted to the steady-state analysis and design of DC/DC switching power converters using the state-space approach with a particular focus on the topology of the active clamp reset forward with synchronous rectifiers.

A review of methods for the analysis of switching power converter circuits published in literature was presented. These methods differ by their proficiency in terms of convergence, accuracy and speed. As a general observation, the faster simulation algorithms lead to convergence issues. Also, these algorithms require formulation of system equations in closed form which may require additional development effort. This particularly applies to circuits with many devices or large number of device parameters. Conversely, the cost for the improved convergence and relative simplicity in formulation of system equations

using algorithms based on the numerical integration is both simulation speed and accuracy. In this thesis a novel method for determining steady-state response of switching converters has been presented. The advantages of this method in terms of speed, convergence, accuracy and simplicity of implementation have been demonstrated.

At present, one of the most popular topology of switching converters is the active clamp reset forward with synchronous rectifiers. In this thesis an accurate state-space model of the topology has been derived. This model involves the majority of the parasitic parameters present in a real converter circuit. Based on the converter model and the novel steady-state method, an efficient algorithm for the simulation of converter switching waveforms has been presented. A significant agreement between simulation results and behavior of converter prototype has been demonstrated and, again, the advantages of the proposed algorithm in terms of speed, convergence and accuracy have been shown.

The simulation of converter switching waveforms, as found in literature, usually includes a start-up trajectory or shows steady-state of one or two nodal variables of converter circuit. The practical design would significantly benefit, however, from a more complex analysis which includes a characterization of all important converter internal variables over a range of operating conditions. To address the problem of such an analysis, the behavioral characterization of switching converters has been introduced. An efficient algorithm for the behavioral characterization has been proposed. The set of input parameters for the behavioral characterization can include input voltage, load current, parameters of converter devices and converter output adjustment range. The circuit of the active clamp reset forward topology with synchronous rectifiers has been characterized using the proposed algorithm.

Simulation programs used in this work are directly applicable to practical design. In fact, converter models and simulation algorithms developed in this work were used in the development of new topologies of switching converters ([54] through [56]).

7.2. Suggestions for Further Research

a) Method for deriving converter state-space model

State-space models of converter circuits were derived using Kirchhoff's first and second laws. This method is not optimal when modeling switching converters with many devices or large number of device parameters. An alternative solution to the problem could be to use graph theory which allows for more systematic approach to generating system equations and is suitable for complex automated algorithms.

b) Thermal stress analysis and calculation of converter efficiency

Algorithms developed in this work can be further expanded to include the computation of power losses on particular devices and the calculation of converter efficiency. Further, as was previously shown, extreme values of different converter variables occur at different input-output conditions. Thus maximum power dissipation of different components may occur at different conditions which may not be known a priori. Thus, the task of performing the overall thermal characterization becomes attractive. To perform the task, the advantage of efficient computation of converter nodal variables over variation of input voltage and output current presented in this work is a definite asset.

c) Switching frequency optimization

Magnetic components and switching devices are the most critical devices of a switching converter in terms of power losses. The mechanism of the losses on these devices is quite complex and depends on switching frequency. The final goal of switching frequency

optimization is to find an operating frequency associated with minimum power losses. The task can be fulfilled by repeated computation of losses at many points of predefined scale of switching frequency. Thus, as above, a fast simulation of converter switching waveforms at many points determined by switching frequency as introduced in this work is a very good starting point.

d) Integration with another simulation tools

The integration of circuit simulators with other simulation packages is a hot topic in the area of simulation of power converters. This is particularly applicable to the integration of electrical simulation with thermal simulation tools. The advantage of fast computation of converter nodal waveforms at steady-state can be followed by a computation of power dissipation on particular converter devices. Then, the results can serve as data entry for thermal simulation. Since device parameters of real converter circuits (track resistance of AgPa hybrid substrates, magnetizing inductance of inductors and transformers, etc.) can significantly vary over specified temperature range, interactive consecutive simulations can be an example of a higher level of integration with thermal simulators.

e) Extension for DCM

The proposed steady-state method is derived for two topology changes within the switching cycle. Thus, the method applies to relatively large family of converters operating in continuous conduction mode (CCM) including those with synchronous rectifiers. To cover even wider class of converters the idea of presented steady-state method can be explored for the class of converter operating in three topology cycles (DCM).

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Appendix A

Derivation of State-Space Model of Ideal ACR Forward Converter with Synchronous Rectifiers

The procedure for deriving the state-space model for an ideal circuit of active clamp forward converter with synchronous rectifiers uses the assumptions specified in section 5.3.2. The symbols used for converter device parameters are those used in Fig 5.6 and Fig.5.7 respectively.

On-time topology

According to the circuit for the on-time topology (Fig.5.5), the second Kirchhoff's law applied to the loop of transformer primary side introduces the equation

$$v_g = L_m \dot{i}_m + R_{wp} i_{pt} \quad (\text{A.1})$$

Since the total primary current is a sum of magnetizing current and reflected secondary current

$$i_{pt} = i_m + i_p \quad (\text{A.2})$$

where the secondary current reflected to the primary side is

$$i_p = \frac{N_s}{N_p} i_L \quad (\text{A.3})$$

equation (A.1) becomes

$$v_g = L_m \dot{i}_m + R_{wp} \left(i_m + \frac{N_s}{N_p} i_L \right) \quad (\text{A.4})$$

$$v_g = L_m \dot{i}_m + R_{wp} i_m + R_{wp} \frac{N_s}{N_p} i_L \quad (\text{A.5})$$

$$\dot{i}_m = -\frac{R_{wp}}{L_m} i_m - \frac{N_s R_{wp}}{N_p L_m} i_L + \frac{1}{L_m} v_g \quad (\text{A.6})$$

At the branch of the reset capacitor

$$0 = v_{cr} + i_{cr} R_{rpof} \quad (\text{A.7})$$

Since

$$i_{cr} = C_r \dot{v}_{cr} \quad (\text{A.8})$$

equation (A.7) becomes

$$0 = v_{cr} + C_r \dot{v}_{cr} R_{rpof} \quad (\text{A.9})$$

and finally

$$\dot{v}_{cr} = -\frac{1}{C_r R_{rpo f}} v_{cr} \quad (\text{A.10})$$

For the load loop on the secondary side the following equation applies

$$v_c + R_c i_c - R i_o = 0 \quad (\text{A.11})$$

Since

$$i_c = C \dot{v}_c \quad (\text{A.12})$$

and

$$i_o = i_L - i_c \quad (\text{A.13})$$

equation (A.11) becomes

$$v_c + R_c C \dot{v}_c - R(i_L - C \dot{v}_c) = 0 \quad (\text{A.14})$$

and

$$v_c + \dot{v}_c C(R + R_c) - R i_L = 0 \quad (\text{A.15})$$

Finally the equation for the second state variables becomes

$$\dot{v}_c = \frac{R}{C(R + R_c)} i_L - \frac{1}{C(R + R_c)} v_c \quad (\text{A.16})$$

For the loop of output inductor the following relationship applies

$$v_s = Li_L + R_L i_L + R_C i_C + v_C \quad (\text{A.17})$$

After a substitution for the capacitor current i_C ((A.12)) the voltage across secondary winding is

$$v_s = Li_L + R_L i_L + R_C C \dot{v}_C + v_C \quad (\text{A.18})$$

With the substitution for the derivative of capacitor voltage $\dot{v}_C$ from (A.16), the expression (A.18) comes in the form

$$v_s = Li_L + R_L i_L + R_C C \left(\frac{R}{C(R + R_C)} i_L - \frac{1}{C(R + R_C)} v_C \right) + v_C \quad (\text{A.19})$$

and therefore

$$v_s = Li_L + R_L i_L + \frac{RR_C}{R + R_C} i_L - \frac{R_C}{R + R_C} v_C + v_C \quad (\text{A.20})$$

Thus

$$v_s = Li_L + \left(R_L + \frac{RR_C}{R + R_C} \right) i_L - \left(\frac{R_C}{R + R_C} - 1 \right) v_C \quad (\text{A.21})$$

and after a substitution

$$R_s = R_L + \frac{RR_c}{R + R_c} \quad (\text{A.22})$$

the expression (A.21) becomes

$$v_s = L\dot{i}_L + R_s i_L + \frac{R}{R + R_c} v_c \quad (\text{A.23})$$

From equation (A.23), the derivative of the inductor current is

$$\dot{i}_L = -\frac{R_s}{L} i_L - \frac{R}{L(R + R_c)} v_c + \frac{1}{L} v_s \quad (\text{A.24})$$

Unknown voltage across the transformer secondary winding v_s in expression (A.24) will be derived in a few following steps. The basic transformation of voltage applies

$$v_s = \frac{N_s}{N_p} v_p \quad (\text{A.25})$$

From the primary loop, the primary voltage v_p is

$$v_p = v_g - i_{pt} R_{wp} \quad (\text{A.26})$$

Since $i_{pt} = i_m + i_p$, the equation above becomes

$$v_p = v_g - (i_m + i_p) R_{wp} \quad (\text{A.27})$$

Since the transformation of current applies

$$i_p = \frac{N_s}{N_p} i_L \quad (\text{A.28})$$

equation (A.27) becomes

$$v_p = v_g - R_{wp} i_m - \frac{N_s}{N_p} R_{wp} i_L \quad (\text{A.29})$$

Finally, the equation for the derivative of inductor current is derived after expressions (A.25) and (A.29) are substituted into expression (A.24):

$$i_L = -\frac{R_s}{L} i_L - \frac{R}{L(R+R_c)} v_c + \frac{N_s}{N_p} \frac{1}{L} \left(v_g - R_{wp} i_m - \frac{N_s}{N_p} R_{wp} i_L \right) \quad (\text{A.30})$$

which becomes after simplifying

$$i_L = -\frac{R_s}{L} i_L - \frac{R}{L(R+R_c)} v_c + \frac{N_s}{N_p} \frac{1}{L} v_g - \frac{N_s}{N_p} \frac{1}{L} R_{wp} i_m - \frac{N_s^2}{N_p^2} \frac{1}{L} R_{wp} i_L \quad (\text{A.31})$$

and finally

$$i_L = -\frac{N_s R_{wp}}{N_p} i_m - \frac{1}{L} \left(R_s + \frac{N_s^2}{N_p^2} R_{wp} \right) i_L - \frac{R}{L(R+R_c)} v_c + \frac{N_s}{N_p} \frac{1}{L} v_g \quad (\text{A.32})$$

or

$$\dot{i}_L = -\frac{N_s R_{wp}}{N_p L} i_m - \frac{R_{son}}{L} i_L - \frac{R}{L(R+R_c)} v_c + \frac{N_s}{N_p L} v_g \quad (\text{A.33})$$

where

$$R_{son} = R_s + \frac{N_s^2}{N_p^2} R_{wp} \quad (\text{A.34})$$

Equations (A.6), (A.10), (A.16) and (A.33) are the desired state equations and the state-space model for the on-time topology can be expressed in matrix nominal form:

$$\begin{bmatrix} \dot{i}_m \\ \dot{v}_{cr} \\ \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} -\frac{R_{wp}}{L_m} & 0 & -\frac{N_s R_{wp}}{N_p L_m} & 0 \\ 0 & -\frac{1}{C_r R_{rpf}} & 0 & 0 \\ -\frac{N_s R_{wp}}{N_p L} & 0 & -\frac{R_{son}}{L} & -\frac{R}{L(R+R_c)} \\ 0 & 0 & \frac{R}{C(R+R_c)} & -\frac{1}{C(R+R_c)} \end{bmatrix} \begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_m} \\ 0 \\ \frac{N_s}{N_p L} \\ 0 \end{bmatrix} v_g \quad (\text{A.35})$$

or

$$\dot{x} = A_1 x + b_1 v_g \quad (\text{A.36})$$

where the state matrices for the on-topology A_1 and b_1 are

$$A_1 = \begin{bmatrix} \frac{R_{wp}}{L_m} & 0 & \frac{N_s R_{wp}}{N_p L_m} & 0 \\ 0 & -\frac{1}{C_r R_{rpf}} & 0 & 0 \\ \frac{N_s R_{wp}}{N_p L} & 0 & \frac{R_{son}}{L} & -\frac{R}{L(R+R_c)} \\ 0 & 0 & \frac{R}{C(R+R_c)} & \frac{1}{C(R+R_c)} \end{bmatrix} \quad b_1 = \begin{bmatrix} \frac{1}{L_m} \\ 0 \\ \frac{N_s}{N_p L} \\ 0 \end{bmatrix} \quad (A.37)$$

Output equation for the on-time topology

Let's consider that the voltage across load resistor R is the desired output y

$$y = i_o R \quad (A.38)$$

After the expressions for the output current

$$i_o = i_L - i_c \quad (A.39)$$

and capacitor current

$$i_c = C \dot{v}_c \quad (A.40)$$

are substituted into equation (A.38), the expression for converter output is

$$y = (i_L - C \dot{v}_c) R \quad (A.41)$$

After a substitution for the derivative of the capacitor voltage $\dot{v}_c$ ((A.16)), the expression for converter output is

$$y = \left(i_L - C \left(\frac{R}{C(R+R_c)} i_L - \frac{1}{C(R+R_c)} v_c \right) \right) R \quad (\text{A.42})$$

After simplification this becomes,

$$y = \left(\left(1 - \frac{R}{R+R_c} \right) i_L + \frac{1}{R+R_c} v_c \right) R \quad (\text{A.43})$$

Finally

$$y = \frac{RR_c}{R+R_c} i_L + \frac{R}{R+R_c} v_c \quad (\text{A.44})$$

The output equation in matrix form is

$$y = \begin{bmatrix} 0 & 0 & R \parallel R_c & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} \quad (\text{A.45})$$

where $R \parallel R_c$ stands for the parallel combination of resistors R and R_c

or

$$y = c_1^T X \quad (\text{A.46})$$

where state vector c_1^T equals

$$c_1^T = \begin{bmatrix} 0 & 0 & R \parallel R_c & \frac{R}{R+R_c} \end{bmatrix} \quad (\text{A.47})$$

Off-time topology

Kirchhoff's first law applied to the primary side of converter circuit from Fig.5.6 introduces the equation

$$v_g = L_m \dot{i}_m + R_{wp} i_m + v_{cr} \quad (\text{A.48})$$

from where the derivative of magnetizing current results in

$$\dot{i}_m = -\frac{R_{wp}}{L_m} i_m - \frac{1}{L_m} v_{cr} + \frac{1}{L_m} v_g \quad (\text{A.49})$$

The state equation for the reset capacitor voltage results directly from Fig.5.6:

$$\dot{v}_{cr} = \frac{1}{C_r} i_m \quad (\text{A.50})$$

For the loop of load current applies the same procedure as for the on-time topology ((A.13) - (A.16)) with the same result as before

$$\dot{v}_c = \frac{R}{C(R+R_c)} i_L - \frac{1}{C(R+R_c)} v_c \quad (\text{A.51})$$

For the inductor loop the following is true:

$$0 = L\dot{i}_L + R_L i_L + R_C i_C + v_C \quad (\text{A.52})$$

After substituting for the capacitor current i_C ((A.12)), the above equation becomes

$$0 = L\dot{i}_L + R_L i_L + R_C \dot{v}_C C + v_C \quad (\text{A.53})$$

Further, after substituting for the derivative of capacitor voltage $\dot{v}_C$ from (A.51)

$$0 = L\dot{i}_L + R_L i_L + R_C C \left(\frac{R}{C(R + R_C)} i_L - \frac{1}{C(R + R_C)} v_C \right) + v_C \quad (\text{A.54})$$

and

$$0 = L\dot{i}_L + R_L i_L + \frac{RR_C}{R + R_C} i_L - \frac{R_C}{R + R_C} v_C + v_C \quad (\text{A.55})$$

Thus

$$0 = L\dot{i}_L + \left(R_L + \frac{RR_C}{R + R_C} \right) i_L - \left(\frac{R_C}{R + R_C} - 1 \right) v_C \quad (\text{A.56})$$

and, finally, the equation for inductor current becomes

$$\dot{i}_L = -\frac{R_{sof}}{L} i_L - \frac{1}{L(R + R_C)} v_C \quad (\text{A.57})$$

where

$$R_{sof} = R_L + \frac{RR_c}{R+R_c} \quad (A.58)$$

Equations (A.49), (A.50), (A.51) and (A.57) are the desired state equations and the state-space model for the off-time topology can be expressed in matrix nominal form as follows:

$$\begin{bmatrix} \dot{i}_m \\ \dot{v}_{cr} \\ \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} \frac{R_{wp}}{L_m} & \frac{1}{L_m} & 0 & 0 \\ \frac{1}{C_r} & 0 & 0 & 0 \\ 0 & 0 & \frac{R_{sof}}{L} & -\frac{R}{L(R+R_c)} \\ 0 & 0 & \frac{R}{C(R+R_c)} & -\frac{1}{C(R+R_c)} \end{bmatrix} \begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_m} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_g \quad (A.59)$$

or

$$\dot{x} = A_2 x + b_2 v_g \quad (A.60)$$

where the state matrices for the off-topology, A_2 and b_2 , are

$$A_2 = \begin{bmatrix} \frac{R_{wp}}{L_m} & \frac{1}{L_m} & 0 & 0 \\ \frac{1}{C_r} & 0 & 0 & 0 \\ 0 & 0 & \frac{R_{sof}}{L} & -\frac{R}{L(R+R_c)} \\ 0 & 0 & \frac{R}{C(R+R_c)} & -\frac{1}{C(R+R_c)} \end{bmatrix} \quad b_2 = \begin{bmatrix} \frac{1}{L_m} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (A.61)$$

Output equation for the off-time topology

Since the load loop is identical with that for the on-time topology, the output equation for the off-time topology equals directly to the relation (A.45):

$$y = c_2^T X \quad (\text{A.62})$$

where the state vector c_2^T equals

$$c_2^T = \left[0 \ 0 \ R \parallel R_c \ \frac{R}{R + R_c} \right] \quad (\text{A.63})$$

Appendix B

Derivation of State-Space Model of Real ACR Forward Converter with Synchronous Rectifiers

The procedure for deriving the state-space model for the real circuit of an active clamp forward converter with synchronous rectifiers uses the assumptions specified in section 5.3.3. The symbols used for converter device parameters are those used in Fig 5.16 and Fig.5.17 respectively.

On-time topology

Kirchhoff's first law applied to the loop of transformer primary side introduces the equation:

$$v_g = R_{tp}i_{pt} + L_m \dot{i}_m + R_{wp}i_{pt} + R_{fpon}i_{pt} + R_{sense}i_{pt} \quad (B.1)$$

where, as discussed in section 5.3.3.

$$i_{pt} = i_{Rfpon} + i_{cr} \equiv i_{Rfpon} \quad (B.2)$$

After a substitution

$$R_{pon} = R_{tp} + R_{wp} + R_{fpon} + R_{sense} \quad (B.3)$$

the equation becomes

$$v_g = L_m \dot{i}_m + R_{pon} i_{pt} \quad (B.4)$$

Total primary current i_{pt} is the sum of the magnetizing current i_m , reflected secondary current i_p , and current i_{mt} which represents losses in magnetic core of the transformer

$$i_{pt} = i_m + i_p + i_{mt} \quad (B.5)$$

Assuming $i_L \gg i_{mL}$, the inductor current i_L reflected the primary side equals

$$i_p = \frac{N_s}{N_p} i_L \quad (B.6)$$

To find a suitable expression for current i_{mt} , let's write an equation for primary voltage v_p in following form

$$v_p = v_g - R_{pon}(i_m + i_p + i_{mt}) \quad (B.7)$$

Then, the current i_{mt} comes in a form

$$i_{mt} = \frac{v_p}{R_{mt}} = \frac{v_g - R_{pon}\left(i_{mt} + \frac{N_s}{N_p} i_L + i_m\right)}{R_{mt}} \quad (B.8)$$

which equals

$$i_{mt} = \frac{1}{R_{mt}} v_g - \frac{R_{pon}}{R_{mt}} i_{mt} - \frac{N_s R_{pon}}{N_p R_{mt}} i_L - \frac{R_{pon}}{R_{mt}} i_m \quad (\text{B.9})$$

After the terms for current i_{mt} are moved to the left side, equation (B.9) can be expressed as:

$$i_{mt} \left(1 + \frac{R_{pon}}{R_{mt}} \right) = \frac{1}{R_{mt}} v_g - \frac{N_s R_{pon}}{N_p R_{mt}} i_L - \frac{R_{pon}}{R_{mt}} i_m \quad (\text{B.10})$$

and

$$i_{mt} \frac{R_{mt} + R_{pon}}{R_{mt}} = \frac{1}{R_{mt}} v_g - \frac{N_s R_{pon}}{N_p R_{mt}} i_L - \frac{R_{pon}}{R_{mt}} i_m \quad (\text{B.11})$$

Finally

$$i_{mt} = \frac{1}{R_{mt} + R_{pon}} v_g - \frac{N_s R_{pon}}{N_p R_{mt} + R_{pon}} i_L - \frac{R_{pon}}{R_{mt} + R_{pon}} i_m \quad (\text{B.12})$$

The total primary current i_{pt} from equation (B.5), after substituting for i_p and i_{mt} from (B.6) and (B.12) respectively, becomes

$$i_{pt} = i_m + \frac{N_s}{N_p} i_L + \frac{1}{R_{mt} + R_{pon}} v_g - \frac{N_s R_{pon}}{N_p R_{mt} + R_{pon}} i_L - \frac{R_{pon}}{R_{mt} + R_{pon}} i_m \quad (\text{B.13})$$

or

$$i_{pt} = \left(1 - \frac{R_{pon}}{R_{mt} + R_{pon}}\right) i_m + \frac{N_s}{N_p} \left(1 - \frac{R_{pon}}{R_{mt} + R_{pon}}\right) i_L + \frac{1}{R_{mt} + R_{pon}} v_g \quad (\text{B.14})$$

Finally

$$i_{pt} = \frac{R_{mt}}{R_{mt} + R_{pon}} i_m + \frac{N_s}{N_p} \frac{R_{mt}}{R_{mt} + R_{pon}} i_L + \frac{1}{R_{mt} + R_{pon}} v_g \quad (\text{B.15})$$

The equation for the transformer magnetizing current i_m can be derived from equation (B.4) after substitution for i_{pt} from expression (B.15)

$$v_g = L_m i_m + R_{pon} \left(\frac{R_{mt}}{R_{mt} + R_{pon}} i_m + \frac{N_s}{N_p} \frac{R_{mt}}{R_{mt} + R_{pon}} i_L + \frac{1}{R_{mt} + R_{pon}} v_g \right) \quad (\text{B.16})$$

and

$$v_g = L_m i_m + \frac{R_{mt} R_{pon}}{R_{mt} + R_{pon}} i_m + \frac{N_s}{N_p} \frac{R_{mt} R_{pon}}{R_{mt} + R_{pon}} i_L + \frac{R_{pon}}{R_{mt} + R_{pon}} v_g \quad (\text{B.17})$$

Thus

$$v_g = L_m i_m + R_{mt} \parallel R_{pon} i_m + \frac{N_s}{N_p} R_{mt} \parallel R_{pon} i_L + \frac{R_{pon}}{R_{mt} + R_{pon}} v_g \quad (\text{B.18})$$

where the symbol $R_{mt} \parallel R_{pon}$ represents the parallel combination of resistors R_{mt} and R_{pon} .

The magnetizing current i_m can now be expressed (from the equation above) as

$$i_m = -\frac{R_{mt} \parallel R_{pon}}{L_m} i_m - \frac{N_s R_{mt} \parallel R_{pon}}{N_p L_m} i_L + \frac{1}{L_m} \left(1 - \frac{R_{pon}}{R_{mt} + R_{pon}} \right) v_g \quad (\text{B.19})$$

Finally, the state equation for the transformer magnetizing current i_m is:

$$\dot{i}_m = -\frac{R_{mt} \parallel R_{pon}}{L_m} i_m - \frac{N_s R_{mt} \parallel R_{pon}}{N_p L_m} i_L + \frac{1}{L_m} \frac{R_{mt}}{R_{mt} + R_{pon}} v_g \quad (\text{B.20})$$

Let's assume the magnitude of the current i_{cr} in comparison with the total current i_{pt} is negligible, $i_{pt} \gg i_{cr}$. Then, Kirchhoff's first law applied to the loop of reset capacitor gives an initial equation for the second state variable v_{cr} in the form

$$R_{fpon} i_{pt} = v_{cr} + i_{cr} R_{rpof} \quad (\text{B.21})$$

which, after making a substitution for the capacitor current i_{cr} :

$$i_{cr} = C_r \dot{v}_{cr} \quad (\text{B.22})$$

gives

$$R_{fpon} i_{pt} = v_{cr} + \dot{v}_{cr} C_r R_{rpof} \quad (\text{B.23})$$

Equation (B.23), after substituting the total primary current i_{pt} from (B.15) becomes

$$R_{fpon} \left(\frac{R_{mt}}{R_{mt} + R_{pon}} i_m + \frac{N_s}{N_p} \frac{R_{mt}}{R_{mt} + R_{pon}} i_L + \frac{1}{R_{mt} + R_{pon}} v_g \right) =$$

$$= v_{cr} + \dot{v}_{cr} C_r R_{rpof} \quad (\text{B.24})$$

After subtracting the reset voltage v_{cr} from both sides of the equation and multiplying the terms in parenthesis, equation (B.24) becomes

$$\dot{v}_{cr} C_r R_{rpof} = \frac{R_{mt} R_{fpon}}{R_{mt} + R_{pon}} i_m - v_{cr} + \frac{N_s}{N_p} \frac{R_{mt} R_{fpon}}{R_{mt} + R_{pon}} i_L + \frac{R_{fpon}}{R_{mt} + R_{pon}} v_g \quad (\text{B.25})$$

which results in the state equation for the reset capacitor voltage v_{cr} in the form:

$$\dot{v}_{cr} = \frac{1}{C_r R_{rpof}} \frac{R_{mt} R_{fpon}}{R_{mt} + R_{pon}} i_m - \frac{1}{C_r R_{rpof}} v_{cr} + \frac{N_s}{N_p} \frac{1}{C_r R_{rpof}} \frac{R_{mt} R_{fpon}}{R_{mt} + R_{pon}} i_L +$$

$$+ \frac{1}{C_r R_{rpof}} \frac{R_{fpon}}{R_{mt} + R_{pon}} v_g \quad (\text{B.26})$$

On the secondary side, for the load loop applies

$$v_c + R_c i_c - R i_o = 0 \quad (\text{B.27})$$

Since

$$i_c = C \dot{v}_c \quad (\text{B.28})$$

and

$$i_o = i_s - i_c \quad (\text{B.29})$$

the equation (B.27) becomes

$$v_c + R_c C \dot{v}_c - R(i_s - C \dot{v}_c) = 0 \quad (\text{B.30})$$

and further

$$v_c + \dot{v}_c C(R + R_c) - R i_s = 0 \quad (\text{B.31})$$

Finally

$$\dot{v}_c = \frac{R}{C(R + R_c)} i_s - \frac{1}{C(R + R_c)} v_c \quad (\text{B.32})$$

Since the total secondary current equals

$$i_s = i_L + i_{mL} \quad (\text{B.33})$$

and

$$L \dot{i}_L = R_{mL} i_{mL} \quad (\text{B.34})$$

then equation (B.33) becomes

$$i_s = i_L + \dot{i}_L \frac{L}{R_{mL}} \quad (\text{B.35})$$

Let's substitute the secondary current i_s in equation (B.32) with equation (B.35):

$$\dot{v}_c = \frac{R}{C(R+R_c)} \left(i_L + \frac{L}{R_{mL}} \dot{i}_L \right) - \frac{1}{C(R+R_c)} v_c \quad (\text{B.36})$$

After multiplication the terms in parenthesis in the equation above, the derivative of the output capacitor voltage v_c equals

$$\dot{v}_c = \frac{R}{C(R+R_c)} i_L + \frac{RL}{R_{mL}C(R+R_c)} \dot{i}_L - \frac{1}{C(R+R_c)} v_c \quad (\text{B.37})$$

Kirchhoff's voltage law applied to the inductor loop gives the equation for transformer secondary voltage in the form

$$v_s = R_{ws}i_s + Li_L + R_Li_s + R_ci_c + v_c + R_{tsnf}i_s + R_{fson}i_s + R_{tsn}i_s \quad (\text{B.38})$$

which, after substituting for the capacitor current i_c and rearranging the terms, becomes

$$v_s = Li_L + i_s(R_{ws} + R_L + R_{tsnf} + R_{fson} + R_{tsn}) + R_c C \dot{v}_c + v_c \quad (\text{B.39})$$

Let's substitute for the sum of the resistances in the secondary loop:

$$R_{son}' = R_{ws} + R_L + R_{tsnf} + R_{fson} + R_{tsn} \quad (\text{B.40})$$

and apply expressions (B.35) and (B.40) to the equation (B.39). Now, the secondary voltage v_s equals

$$v_s = L\dot{i}_L + \left(i_L + \frac{L}{R_{mL}}\dot{i}_L\right)R_{son'} + R_c C\dot{v}_c + v_c \quad (\text{B.41})$$

After a small rearrangement of the terms in the above equation, the secondary voltage v_s is

$$v_s = L\left(1 + \frac{R_{son'}}{R_{mL}}\right)\dot{i}_L + R_{son'}i_L + R_c C\dot{v}_c + v_c \quad (\text{B.42})$$

Equations (B.36) and (B.42) include the first derivatives of the state variables v_c and i_L in theirs and can be used to formulate the final state equations. The state equation for the inductor current i_L will be obtained from expression (B.42) after substituting for the derivative of the capacitor voltage v_c ((B.36))

$$\begin{aligned} v_s = & L\frac{R_{mL} + R_{son'}}{R_{mL}}\dot{i}_L + R_{son'}i_L + v_c + \\ & + R_c C\left(\frac{R}{C(R + R_c)}i_L + \frac{L}{R_{mL}}\frac{R}{C(R + R_c)}\dot{i}_L - \frac{1}{C(R + R_c)}v_c\right) \end{aligned} \quad (\text{B.43})$$

After multiplying the terms in parenthesis, the equation for the secondary voltage becomes

$$v_s = L\frac{R_{mL} + R_{son'}}{R_{mL}}\dot{i}_L + \frac{L}{R_{mL}}\frac{R_c R}{R + R_c}\dot{i}_L + R_{son'}i_L + \frac{R_c R}{R + R_c}i_L + v_c - \frac{R_c}{R + R_c}v_c \quad (\text{B.44})$$

or

$$v_s = \frac{L}{R_{mL}}(R_{mL} + R_{son'} + R \parallel R_c)\dot{i}_L + (R_{son'} + R \parallel R_c)i_L + \left(1 - \frac{R_c}{R + R_c}\right)v_c \quad (\text{B.45})$$

where the symbol $R \parallel R_c$ represents the parallel combination of resistors R and R_c .

After making the following substitution

$$R_{son} = R_{son'} + R \parallel R_c \quad (\text{B.46})$$

equation (B.45) can now be expressed as:

$$v_s = \frac{L}{R_{mL}}(R_{mL} + R_{son})i_L + R_{son}i_L + \frac{R}{R + R_c}v_c \quad (\text{B.47})$$

Thus, the equation for the inductor current i_L is

$$i_L = -\frac{1}{L} \frac{R_{mL}R_{son}}{R_{mL} + R_{son}}i_L - \frac{R}{R + R_c} \frac{1}{L} \frac{R_{mL}}{R_{mL} + R_{son}}v_c + \frac{1}{L} \frac{R_{mL}}{R_{mL} + R_{son}}v_s \quad (\text{B.48})$$

or

$$i_L = -\frac{1}{L} R_{mL} \parallel R_{son} i_L - \frac{1}{L} \frac{R}{R + R_c} \frac{R_{mL}}{R_{mL} + R_{son}} v_c + \frac{1}{L} \frac{R_{mL}}{R_{mL} + R_{son}} v_s \quad (\text{B.49})$$

where the symbol $R_{mL} \parallel R_{son}$ represents the parallel combination of resistors R_{mL} and R_{son} .

The unknown voltage across the transformer secondary winding v_s in expression (B.49) will be derived in the following steps. The basic transformation of voltage applies

$$v_s = \frac{N_s}{N_p} v_p \quad (\text{B.50})$$

The primary voltage v_p , as defined by expression (B.7) is

$$v_p = v_g - R_{pon} i_{pt} \quad (\text{B.51})$$

Equation (B.50), after substituting for the primary voltage v_p and the total primary current i_{pt} from expressions (B.7) and (B.15) respectively, is now expressed as:

$$v_s = \frac{N_s}{N_p} \left(v_g - R_{pon} \left(\frac{R_{mt}}{R_{mt} + R_{pon}} i_m + \frac{N_s}{N_p} \frac{R_{mt}}{R_{mt} + R_{pon}} i_L + \frac{1}{R_{mt} + R_{pon}} v_g \right) \right) \quad (\text{B.52})$$

which, after a small rearrangement of terms in parenthesis, becomes

$$v_s = \frac{N_s}{N_p} \left(v_g - R_{mt} \parallel R_{pon} i_m - \frac{N_s}{N_p} R_{mt} \parallel R_{pon} i_L - \frac{R_{pon}}{R_{mt} + R_{pon}} v_g \right) \quad (\text{B.53})$$

and finally

$$v_s = -\frac{N_s}{N_p} \left(R_{mt} \parallel R_{pon} i_m + \frac{N_s}{N_p} R_{mt} \parallel R_{pon} i_L - \frac{R_{mt}}{R_{mt} + R_{pon}} v_g \right) \quad (\text{B.54})$$

The state equation for the inductor current i_L is found after substituting the secondary voltage v_s ((B.54)) into equation (B.49) as follows:

$$\begin{aligned}
i_L = & -\frac{1}{L}R_{mL} \parallel R_{son}i_L - \frac{1}{L} \frac{R}{R + R_c R_{mL} + R_{son}} \frac{R_{mL}}{R_{mL} + R_{son}} v_c + \\
& + \frac{1}{L} \frac{R_{mL}}{R_{mL} + R_{son}} \left(\frac{N_s}{N_p} \left(-R_{mt} \parallel R_{pon}i_m - \frac{N_s}{N_p} R_{mt} \parallel R_{pon}i_L + \frac{R_{mt}}{R_{mt} + R_{pon}} v_g \right) \right) \quad (B.55)
\end{aligned}$$

which can also be expressed as:

$$\begin{aligned}
i_L = & -\frac{1}{L}R_{mL} \parallel R_{son}i_L - \frac{1}{L} \frac{R}{R + R_c R_{mL} + R_{son}} v_c \frac{N_s}{N_p} \frac{1}{L} \frac{R_{mL}}{R_{mL} + R_{son}} R_{mt} \parallel R_{pon}i_m - \\
& - \left(\frac{N_s}{N_p} \right)^2 \frac{1}{L} \frac{R_{mL}}{R_{mL} + R_{son}} R_{mt} \parallel R_{pon}i_L + \frac{N_s}{N_p} \frac{1}{L} \frac{R_{mL}}{R_{mL} + R_{son}} \frac{R_{mt}}{R_{mt} + R_{pon}} v_g \quad (B.56)
\end{aligned}$$

and, finally, the state equation for the inductor current i_L now becomes

$$\begin{aligned}
i_L = & -\frac{1}{L} \left(R_{mL} \parallel R_{son} + \left(\frac{N_s}{N_p} \right)^2 R_{mt} \parallel R_{pon} \frac{R_{mL}}{R_{mL} + R_{son}} \right) i_L - \\
& - \frac{1}{L} \frac{R}{R + R_c R_{mL} + R_{son}} v_c - \frac{N_s}{N_p} \frac{1}{L} R_{mt} \parallel R_{pon} \frac{R_{mL}}{R_{mL} + R_{son}} i_m + \\
& + \frac{N_s}{N_p} \frac{1}{L} \frac{R_{mt}}{R_{mt} + R_{pon}} \frac{R_{mL}}{R_{mL} + R_{son}} v_g \quad (B.57)
\end{aligned}$$

The state equation for the capacitor voltage v_c will be obtained from expression (B.37) after a substitution for the derivative of the inductor current i_L defined by equation (B.57) in following steps:

$$\begin{aligned}
 \dot{v}_c = & \frac{R}{C(R+R_c)}i_L - \frac{1}{C(R+R_c)}v_c - \\
 & - \frac{RL}{R_{mL}C(R+R_c)}\frac{1}{L}\left(R_{mL}\parallel R_{son} + \left(\frac{N_s}{N_p}\right)^2 R_{mt}\parallel R_{pon}\frac{R_{mL}}{R_{mL}+R_{son}}\right)i_L - \\
 & - \frac{RL}{R_{mL}C(R+R_c)}\frac{1}{LN_pL}\frac{N_s}{1}R_{mt}\parallel R_{pon}\frac{R_{mL}}{R_{mL}+R_{son}}i_m - \\
 & - \frac{RL}{R_{mL}C(R+R_c)}\frac{R}{L(R+R_c)}\frac{R_{mL}}{R_{mL}+R_{son}}v_c + \\
 & + \frac{RL}{R_{mL}C(R+R_c)}\frac{1}{LN_p}\frac{N_s}{1}\frac{R_{mt}}{R_{mt}+R_{pon}}\frac{R_{mL}}{R_{mL}+R_{son}}v_g
 \end{aligned} \tag{B.58}$$

which equals to

$$\begin{aligned}
 \dot{v}_c = & \frac{R}{C(R+R_c)}\left(1 - \frac{R_{son}}{R_{mL}+R_{son}} - \left(\frac{N_s}{N_p}\right)^2 \frac{R_{mt}\parallel R_{pon}}{R_{mL}+R_{son}}\right)i_L - \\
 & - \frac{1}{C(R+R_c)}\left(1 + \frac{R^2}{(R+R_c)(R_{mL}+R_{son})}\right)v_c - \frac{N_s}{N_p}\frac{R}{C(R+R_c)}\frac{R_{mt}\parallel R_{pon}}{R_{mL}+R_{son}}i_m + \\
 & + \frac{N_s}{N_p}\frac{R}{C(R+R_c)}\frac{R_{mt}}{(R_{mt}+R_{pon})(R_{mL}+R_{son})}v_g
 \end{aligned} \tag{B.59}$$

Finally, the state equation for the output capacitor voltage v_c is expressed as:

$$\begin{aligned}
 \dot{v}_c = & -\frac{N_s}{N_p} \frac{R}{C(R+R_c)} \frac{R_{mt} \parallel R_{pon}}{R_{mL} + R_{son}} i_m + \\
 & + \frac{R}{C(R+R_c)} \left(\frac{R_{mL}}{R_{mL} + R_{son}} - \left(\frac{N_s}{N_p} \right)^2 \frac{R_{mt} \parallel R_{pon}}{R_{mL} + R_{son}} \right) i_L - \\
 & - \frac{1}{C(R+R_c)} \left(1 + \frac{R^2}{(R+R_c)(R_{mL} + R_{son})} \right) v_c + \\
 & + \frac{N_s}{N_p} \frac{R}{C(R+R_c)} \frac{R_{mt}}{(R_{mL} + R_{son})(R_{mt} + R_{pon})} v_g
 \end{aligned} \tag{B.60}$$

Output equation for on-time topology

Based on equations (B.57) and (B.60), let's define following expressions:

$$a_{31n} = -\frac{N_s}{N_p} \frac{1}{L} R_{mt} \parallel R_{pon} \frac{R_{mL}}{R_{mL} + R_{son}} \tag{B.61}$$

$$a_{32n} = 0 \tag{B.62}$$

$$a_{33n} = -\frac{1}{L} \left(R_{mL} \parallel R_{son} + \left(\frac{N_s}{N_p} \right)^2 R_{mt} \parallel R_{pon} \frac{R_{mL}}{R_{mL} + R_{son}} \right) \tag{B.63}$$

$$a_{34n} = -\frac{R}{R+R_c} \frac{1}{L} \frac{R_{mL}}{R_{mL} + R_{son}} \tag{B.64}$$

$$b_{3n} = \frac{N_s}{N_p} \frac{1}{L} \frac{R_{mt}}{R_{mt} + R_{pon}} \frac{R_{mL}}{R_{mL} + R_{son}} \tag{B.65}$$

$$a_{41n} = -\frac{N_s}{N_p} \frac{R}{C(R+R_c)} \frac{R_{mt} \parallel R_{pon}}{R_{mL} + R_{son}} \tag{B.66}$$

$$a_{42n} = 0 \tag{B.67}$$

$$a_{43n} = \frac{R}{C(R+R_c)} \left(\frac{R_{mL}}{R_{mL}+R_{son}} - \left(\frac{N_s}{N_p} \right)^2 \frac{R_{mt} \parallel R_{pon}}{R_{mL}+R_{son}} \right) \quad (B.68)$$

$$a_{44n} = -\frac{1}{C(R+R_c)} \left(1 + \frac{R^2}{(R+R_c)(R_{mL}+R_{son})} \right) \quad (B.69)$$

$$b_{4n} = \frac{N_s}{N_p} \frac{R}{C(R+R_c)} \frac{R_{mt}}{(R_{mL}+R_{son})(R_{mt}+R_{pon})} \quad (B.70)$$

Let's consider the voltage across the load resistor R as the desired output y

$$y = i_o R \quad (B.71)$$

The expressions for the output current i_o is:

$$i_o = i_L + i_{mL} - i_c \quad (B.72)$$

The capacitor current i_c ((B.28)) and the inductor reluctance current i_{mL} ((B.34)) are substituted into equation (B.71). The expression for the converter output now has the form

$$y = \left(i_L + i_L \frac{L}{R_{mL}} - C \dot{v}_c \right) R \quad (B.73)$$

After expanding the parenthesis the output equals

$$y = R i_L + \frac{RL}{R_{mL}} \dot{i}_L - RC \dot{v}_c \quad (B.74)$$

After the expressions for the derivative of the inductor current and the output capacitor voltage as specified by equations (B.57) and (B.60) are inserted into the equation above, the converter output is

$$y = Ri_L + \frac{RL}{R_{mL}}(a_{31n}i_m + a_{33n}i_L + a_{34n}v_c + b_{3n}v_g) - RC(a_{41n}i_m + a_{43n}i_L + a_{44n}v_c + b_{4n}v_g) \quad (B.75)$$

which is the same as:

$$y = R\left(\frac{L}{R_{mL}}a_{31n} - Ca_{41n}\right)i_m + R\left(1 + \frac{L}{R_{mL}}a_{33n} - Ca_{43n}\right)i_L + R\left(\frac{L}{R_{mL}}a_{34n} - Ca_{44n}\right)v_c + R\left(\frac{L}{R_{mL}}b_{3n} - Cb_{4n}\right)v_g \quad (B.76)$$

where the terms a_{ij} and b_i are those defined by equations (B.61) through (B.70). The converter output (from the (B.76)), in nominal matrix form, is

$$y = c_1^T X + d_1 v_g \quad (B.77)$$

where the matrix c_1^T equals

$$c_1^T = \left[R\left(\frac{L}{R_{mL}}a_{31n} - Ca_{41n}\right) \ 0 \ R\left(1 + \frac{L}{R_{mL}}a_{33n} - Ca_{43n}\right) \ R\left(\frac{L}{R_{mL}}a_{34n} - Ca_{44n}\right) \right] \quad (B.78)$$

and the matrix d_1 equals

$$d_1 = R\left(\frac{L}{R_{mL}}b_{3n} - Cb_{4n}\right) \quad (B.79)$$

The state-space model for the on-time topology is specified by expressions (B.19), (B.26), (B.57), (B.60), (B.77), (B.78), (B.79) and (B.61) through (B.70).

$$\begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} = \begin{bmatrix} -\frac{R_{pon} \parallel R_{mt}}{L_m} & 0 & -\frac{N_s R_{pon} \parallel R_{mt}}{N_p L_m} & 0 \\ \frac{1}{C_r R_{rpf} R_{pon} + R_{mt}} & -\frac{1}{C_r R_{rpf}} & \frac{N_s R_{pon} R_{mt}}{N_p R_{pon} + R_{mt} C_r R_{rpf}} & 0 \\ -\frac{1}{L} \left(\frac{N_s R_{mt} \parallel R_{pon}}{N_p R_{pon} R_{son} + R_{mt}} \right) & 0 & -\frac{1}{L} \left(\frac{R_{son} \parallel R_{mt}}{R_{pon} R_{son} + R_{mt}} \right) & -\frac{R}{L(R + R_c) R_{son} + R_{mt}} \\ -\frac{N_s}{N_p} \frac{R}{C(R + R_c) R_{son} + R_{mt}} & 0 & \frac{R}{C(R + R_c) R_{son} + R_{mt}} \left(1 + \frac{R^2}{(R + R_c)(R_{son} + R_{mt})} \right) & -\frac{R^2}{C(R + R_c)(R_{son} + R_{mt})} \end{bmatrix} \begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_m} \frac{R_{mt}}{R_{pon} + R_{mt}} \\ \frac{R_{pon}}{R_{pon} + R_{mt} C_r R_{rpf}} \\ \frac{1}{L} \frac{R_{mt}}{R_{pon} R_{son} + R_{mt}} \\ \frac{N_s}{N_p} \frac{R}{C(R + R_c)(R_{pon} + R_{mt})(R_{son} + R_{mt})} \end{bmatrix} v_g$$

$$y = \begin{bmatrix} R \left(\frac{L}{R_{mt}} a_{31n} - C a_{41n} \right) & 0 & R \left(1 + \frac{L}{R_{mt}} a_{33n} - C a_{43n} \right) & R \left(\frac{L}{R_{mt}} a_{34n} - C a_{44n} \right) \end{bmatrix} \begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} + R \left(\frac{L}{R_{mt}} b_{3n} - C b_{4n} \right) v_g$$

$$a_{31n} = -\frac{N_s}{N_p} \frac{1}{L R_{mt}} \frac{R_{mt}}{R_{pon} + R_{mt}} \parallel R_{pon} \quad a_{41n} = -\frac{N_s}{N_p} \frac{R}{C(R + R_c) R_{mt} \parallel R_{pon}}$$

$$a_{32n} = 0 \quad a_{42n} = 0$$

$$a_{33n} = -\frac{1}{L} \left(\frac{R_{mt} \parallel R_{son} + \left(\frac{N_s}{N_p} \right)^2 \frac{R_{mt} \parallel R_{pon}}{R_{mt} + R_{son}} \right) \quad a_{43n} = \frac{R}{C(R + R_c) R_{mt} + R_{son}} - \left(\frac{N_s}{N_p} \right)^2 \frac{R_{mt} \parallel R_{pon}}{R_{mt} + R_{son}}$$

$$a_{34n} = -\frac{R}{R + R_c} \frac{1}{L} \frac{R_{mt}}{R_{mt} + R_{son}} \quad a_{44n} = -\frac{1}{C(R + R_c)} \left(1 + \frac{R^2}{(R + R_c)(R_{mt} + R_{son})} \right)$$

$$b_{3n} = \frac{N_s}{N_p} \frac{1}{L R_{mt} + R_{son}} \frac{R_{mt}}{R_{mt} + R_{pon}} \quad b_{4n} = \frac{N_s}{N_p} \frac{R}{C(R + R_c) R_{mt} + R_{son}} \frac{R_{mt}}{(R_{mt} + R_{son})}$$

State-space model for on-time topology

B.2. Off-time topology

Kirchhoff's first law applied to the loop of the transformer primary side introduces the equation

$$v_g = R_{tp}i_{pt} + L_m \dot{i}_m + R_{wp}i_{pt} + v_{cr} + R_{rpon}i_{pt} + R_{sense}i_{pt} \quad (\text{B.81})$$

The total primary current i_{pt} during the off-time period will not include the reflected secondary current. Thus, the total primary current is equal to the sum of the magnetizing and transformer reluctance currents:

$$i_{pt} = i_{mt} + i_m \quad (\text{B.82})$$

After substituting

$$R_{pof} = R_{tp} + R_{wp} + R_{rpon} + R_{sense} \quad (\text{B.83})$$

into equation (B.81), it now becomes

$$v_g = L_m \dot{i}_m + R_{pof}i_{pt} + v_{cr} \quad (\text{B.84})$$

The expression for the reluctance current i_{mt} can be found similarly, as in section B.1. The particular steps are as follows:

$$v_p = v_g - R_{pof}(i_m + i_{mt}) - v_{cr} \quad (\text{B.85})$$

$$i_{mt} = \frac{v_p}{R_{mt}} = \frac{v_g - R_{pof}(i_{mt} + i_m) - v_{cr}}{R_{mt}} \quad (\text{B.86})$$

$$i_{mt} = \frac{1}{R_{mt}} v_g - \frac{R_{pof}}{R_{mt}} i_{mt} - \frac{R_{pof}}{R_{mt}} i_m - \frac{1}{R_{mt}} v_{cr} \quad (\text{B.87})$$

$$i_{mt} \left(1 + \frac{R_{pof}}{R_{mt}} \right) = i_{rmt} \frac{R_{mt} + R_{pof}}{R_{mt}} = \frac{1}{R_{mt}} v_g - \frac{R_{pof}}{R_{mt}} i_m - \frac{1}{R_{mt}} v_{cr} \quad (\text{B.88})$$

and finally

$$i_{mt} = \frac{1}{R_{mt} + R_{pof}} v_g - \frac{R_{pof}}{R_{mt} + R_{pof}} i_m - \frac{1}{R_{mt} + R_{pof}} v_{cr} \quad (\text{B.89})$$

Equation (B.84), after making a substitution for the total primary current i_{pt} from (B.82) and the reluctance current i_{mt} in (B.89), is expressed as:

$$v_g = L_m i_m + R_{pof} i_m + R_{pof} \left(\frac{1}{R_{mt} + R_{pof}} v_g - \frac{R_{pof}}{R_{mt} + R_{pof}} i_m - \frac{1}{R_{mt} + R_{pof}} v_{cr} \right) + v_{cr} \quad (\text{B.90})$$

The elimination of the derivative of the transformer magnetizing current i_m from the equation above is straight forward and can be done as follows:

$$L_m i_m = v_g - R_{pof} i_m + \frac{R_{pof}^2}{R_{mt} + R_{pof}} i_m + \frac{R_{pof}}{R_{mt} + R_{pof}} v_{cr} - v_{cr} - \frac{R_{pof}}{R_{mt} + R_{pof}} v_g \quad (\text{B.91})$$

$$i_m = \frac{1}{L_m} \left(1 - \frac{R_{pof}}{R_{mt} + R_{pof}} \right) v_g - \frac{R_{pof}}{L_m} \left(1 - \frac{R_{pof}}{R_{mt} + R_{pof}} \right) i_m - \frac{1}{L_m} \left(1 - \frac{R_{pof}}{R_{mt} + R_{pof}} \right) v_{cr} \quad (\text{B.92})$$

$$i_m = \frac{1}{L_m} \frac{R_{mt}}{R_{mt} + R_{pof}} v_g - \frac{1}{L_m} \frac{R_{mt} R_{pof}}{R_{mt} + R_{pof}} i_m - \frac{1}{L_m} \frac{R_{mt}}{R_{mt} + R_{pof}} v_{cr} \quad (\text{B.93})$$

Finally, the state equation for the transformer magnetizing current i_m is

$$i_m = \frac{1}{L_m R_{mt} + R_{pof}} v_g - \frac{R_{mt} \parallel R_{pof}}{L_m} i_m - \frac{1}{L_m R_{mt} + R_{pof}} v_{cr} \quad (\text{B.94})$$

A change of voltage across the reset capacitor in off-time is proportional to the current flowing through it:

$$\dot{v}_{cr} = \frac{1}{C_r} i_{pt} \quad (\text{B.95})$$

Equation (B.95), after substituting for both, the total primary current i_{pt} and the reluctance current i_{mt} given by expressions (B.82) and (B.89) respectively, can be expressed as:

$$\dot{v}_{cr} = \frac{1}{C_r} (i_m + i_{mt}) = \frac{1}{C_r} \left(i_m + \frac{1}{R_{mt} + R_{pof}} v_g - \frac{R_{pof}}{R_{mt} + R_{pof}} i_m - \frac{1}{R_{mt} + R_{pof}} v_{cr} \right) \quad (\text{B.96})$$

which also equals

$$\dot{v}_{cr} = \frac{1}{C_r} \left(1 - \frac{R_{pof}}{R_{mt} + R_{pof}} \right) i_m - \frac{1}{C_r (R_{mt} + R_{pof})} v_{cr} + \frac{1}{C_r (R_{mt} + R_{pof})} v_g \quad (\text{B.97})$$

The state equation for the reset capacitor voltage v_{cr} results from the above equation as:

$$\dot{v}_{cr} = \frac{1}{C_r} \frac{R_{mt}}{R_{mt} + R_{pof}} i_m - \frac{1}{C_r (R_{mt} + R_{pof})} v_{cr} + \frac{1}{C_r (R_{mt} + R_{pof})} v_g \quad (\text{B.98})$$

On the secondary side, Kirchhoff's first law applied to the loop of the output inductor introduces the equation

$$0 = L\dot{i}_L + R_L i_s + R_C i_C + v_C + R_{tsnf} i_s + R_{rson} i_s \quad (\text{B.99})$$

which, after substituting for

$$R_{sof} = R_L + R_{tsnf} + R_{rson} \quad (\text{B.100})$$

gives

$$0 = L\dot{i}_L + R_{sof} i_s + R_C i_C + v_C \quad (\text{B.101})$$

Substituting for the total secondary current i_s given by equation (B.35) and the output capacitor current i_C given by the equation (B.28), equation (B.101) becomes:

$$0 = L\dot{i}_L + R_{sof} \left(i_L + \dot{i}_L \frac{L}{R_{mL}} \right) + R_C C \dot{v}_C + v_C \quad (\text{B.102})$$

which, after the multiplication of the terms in parenthesis becomes

$$0 = L \left(1 + \frac{R_{sof}}{R_{mL}} \right) \dot{i}_L + R_{son} i_L + R_C C \dot{v}_C + v_C \quad (\text{B.103})$$

The expression for the derivative of the output capacitor voltage $\dot{v}_C$ for the off-time topology is, in comparison with the on-time expression ((B.37)), unchanged and equals

$$\dot{v}_c = \frac{R}{C(R+R_c)}i_L + \frac{RL}{R_{mL}C(R+R_c)}i_L - \frac{1}{C(R+R_c)}v_c \quad (\text{B.104})$$

The state equation for the inductor current i_L can be derived from expression (B.103) after plugging-in term $\dot{v}_c$ from equation (B.104)

$$0 = L\left(1 + \frac{R_{sof}}{R_{mL}}\right)i_L + R_{sof}'i_L + R_c C\left(\frac{R}{C(R+R_c)}i_L + \frac{RL}{R_{mL}C(R+R_c)}i_L - \frac{1}{C(R+R_c)}v_c\right) + v_c \quad (\text{B.105})$$

Equation (B.105), after a small rearrangement of terms for the state variables, becomes

$$0 = \frac{L}{R_{mL}}\left(R_{mL} + R_{sof}' + \frac{RR_c}{R+R_c}\right)i_L + \left(R_{sof}' + \frac{RR_c}{R+R_c}\right)i_L + \left(1 - \frac{R_c}{R+R_c}\right)v_c \quad (\text{B.106})$$

After a substitution:

$$R_{sof} = R_{sof}' + R \parallel R_c \quad (\text{B.107})$$

equation (B.106) becomes

$$0 = \frac{L}{R_{mL}}(R_{mL} + R_{sof})i_L + R_{sof}'i_L + \frac{R}{R+R_c}v_c \quad (\text{B.108})$$

which results in the final state equation for the inductor current i_L

$$\dot{i}_L = -\frac{1}{L} \frac{R_{mL}R_{sof}}{R_{mL} + R_{sof}}i_L - \frac{R}{L(R+R_c)} \frac{R_{mL}}{R_{mL} + R_{sof}}v_c \quad (\text{B.109})$$

or

$$i_L = -\frac{R_{mL} \parallel R_{sof}}{L} i_L - \frac{R}{L(R+R_C)} \frac{R_{mL}}{R_{mL} + R_{sof}} v_C \quad (\text{B.110})$$

where the symbol $R_{mL} \parallel R_{sof}$ represents the parallel combination of resistances R_{mL} and R_{sof} .

The state equation for the capacitor voltage v_C can be obtained from expression (B.104) after substituting for the derivative of inductor current i_L (as found in the equation (B.110)) in several straight forward steps

$$\begin{aligned} \dot{v}_C &= \frac{R}{C(R+R_C)} i_L + \frac{RL}{R_{mL}C(R+R_C)} \left(-\frac{R_{mL} \parallel R_{sof}}{L} i_L - \frac{R}{L(R+R_C)} \frac{R_{mL}}{R_{mL} + R_{sof}} v_C \right) - \\ &- \frac{1}{C(R+R_C)} v_C \end{aligned} \quad (\text{B.111})$$

$$\begin{aligned} \dot{v}_C &= \frac{R}{C(R+R_C)} i_L - \frac{RR_{sof}}{C(R+R_C)(R_{mL} + R_{sof})} i_L - \frac{R^2}{C(R+R_C)^2} \frac{1}{R_{mL} + R_{sof}} v_C - \\ &- \frac{1}{C(R+R_C)} v_C \end{aligned} \quad (\text{B.112})$$

$$\dot{v}_C = \frac{R}{C(R+R_C)} \left(1 - \frac{R_{sof}}{R_{mL} + R_{sof}} \right) i_L - \frac{1}{C(R+R_C)} \left(1 + \frac{R^2}{(R+R_C)(R_{mL} + R_{sof})} \right) v_C \quad (\text{B.113})$$

finally resulting in:

$$\dot{v}_c = \frac{R}{C(R+R_c)} \frac{R_{mL}}{R_{mL}+R_{sof}} i_L - \frac{1}{C(R+R_c)} \left(1 + \frac{R^2}{(R+R_c)(R_{mL}+R_{sof})} \right) v_c \quad (\text{B.114})$$

Output equation for off-time topology

With respect to equations (B.110) and (B.114), let's define the following coefficients:

$$a_{31f} = 0 \quad (\text{B.115})$$

$$a_{32f} = 0 \quad (\text{B.116})$$

$$a_{33f} = -\frac{R_{mL} \parallel R_{sof}}{L} \quad (\text{B.117})$$

$$a_{34f} = -\frac{1}{L} \frac{R}{R+R_c} \frac{R_{mL}}{R_{mL}+R_{sof}} \quad (\text{B.118})$$

$$b_{3f} = 0 \quad (\text{B.119})$$

$$a_{41f} = 0 \quad (\text{B.120})$$

$$a_{42f} = 0 \quad (\text{B.121})$$

$$a_{43f} = \frac{R}{C(R+R_c)} \frac{R_{mL}}{R_{mL}+R_{sof}} \quad (\text{B.122})$$

$$a_{44f} = -\frac{1}{C(R+R_c)} \left(1 + \frac{R^2}{(R+R_c)(R_{mL}+R_{sof})} \right) \quad (\text{B.123})$$

$$b_{4f} = 0 \quad (\text{B.124})$$

As for the on-time topology, the voltage across the load resistor R is the desired converter output y

$$y = i_o R \quad (\text{B.125})$$

After making substitutions for currents i_o , i_{mL} and i_c from expressions (B.72), (B.34) and (B.28) respectively, the output equation becomes

$$y = Ri_L + \frac{RL}{R_{mL}}\dot{i}_L - RC\dot{v}_c \quad (\text{B.126})$$

The final form of the output equation is found after making substitutions for the derivatives of the inductor current i_L ((B.110)) and output capacitor voltage v_c ((B.114)) in the equation above

$$y = Ri_L + \frac{RL}{R_{mL}}(a_{33f}\dot{i}_L + a_{34f}v_c) - RC(a_{43f}\dot{i}_L + a_{44f}v_c) \quad (\text{B.127})$$

which after small rearrangement becomes

$$y = R\left(1 + \frac{L}{R_{mL}}a_{33f} - Ca_{43f}\right)\dot{i}_L + R\left(\frac{L}{R_{mL}}a_{34f} - Ca_{44f}\right)v_c \quad (\text{B.128})$$

which, in nominal matrix form, is

$$y = c_2^T X + d_2 v_g \quad (\text{B.129})$$

where the matrix c_2^T equals

$$c_2^T = \left[0 \ 0 \ R\left(1 + \frac{L}{R_{mL}}a_{33f} - Ca_{43f}\right) \ R\left(\frac{L}{R_{mL}}a_{34f} - Ca_{44f}\right) \right] \quad (\text{B.130})$$

and the matrix d_2 is equal to the scalar

$$d_2 = 0 \tag{B.131}$$

The state-space model for the off-time topology is specified by expressions (B.94), (B.98), (B.110), (B.114), (B.129), (B.130), (B.131) and (B.115) through (B.124)

$$\begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} = \begin{bmatrix} \frac{R_{pof} \| R_{mt}}{L_m} - \frac{1}{L_m} \frac{R_{mt}}{R_{pof} + R_{mt}} & 0 & 0 & 0 \\ \frac{1}{C_r} \frac{R_{mt}}{R_{pof} + R_{mt}} - \frac{1}{C_r(R_{pof} + R_{mt})} & 0 & 0 & 0 \\ 0 & -\frac{R_{sof} \| R_{mL}}{L} & \frac{R_{sof} \| R_{mL}}{C(R_{sof} + R_{mL})} & -\frac{R_{sof} \| R_{mL}}{C(R_{sof} + R_{mL})} \left(1 + \frac{R_{sof} \| R_{mL}}{R^2} \right) \\ 0 & \frac{R_{sof} \| R_{mL}}{C(R_{sof} + R_{mL})} & -\frac{R_{sof} \| R_{mL}}{C(R_{sof} + R_{mL})} \left(1 + \frac{R_{sof} \| R_{mL}}{R^2} \right) & \frac{R_{sof} \| R_{mL}}{C(R_{sof} + R_{mL})} \left(1 + \frac{R_{sof} \| R_{mL}}{R^2} \right) \end{bmatrix} \begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_m} \frac{R_{mt}}{R_{pof} + R_{mt}} \\ \frac{1}{C_r(R_{pof} + R_{mt})} \\ 0 \\ 0 \end{bmatrix} v_s$$

$$y = \begin{bmatrix} 0 & 0 & R \left(1 + \frac{L}{R_{mL}} a_{33f} - C a_{43f} \right) R \left(\frac{L}{R_{mL}} a_{34f} - C a_{44f} \right) \end{bmatrix} \begin{bmatrix} i_m \\ v_{cr} \\ i_L \\ v_c \end{bmatrix}$$

$$\begin{aligned}
 a_{31f} &= 0 & a_{41f} &= 0 \\
 a_{32f} &= 0 & a_{42f} &= 0 \\
 a_{33f} &= -\frac{R_{mL} \| R_{sof}}{L} & a_{43f} &= \frac{R}{C(R_{sof} + R_{mL})} \frac{R_{mL}}{R_{sof}} \\
 a_{34f} &= -\frac{R}{R + R_c} \frac{1}{L} \frac{R_{mL}}{R_{mL} + R_{sof}} & a_{44f} &= -\frac{1}{C(R_{sof} + R_{mL})} \left(1 + \frac{R^2}{(R + R_c)(R_{mL} + R_{sof})} \right) \\
 b_{3f} &= 0 & b_{4f} &= 0
 \end{aligned}$$

State-space model for off-time topology

Appendix C

Extension of the Output Equation for the Model of the Real ACR Forward Converter with Synchronous Rectifiers

The symbols used for converter device parameters are those used in Fig 5.15 through Fig.5.17.

C.1. On-time topology

The waveform of the drain-to-source voltage across the main primary transistor:

$$V_{Qfds} = \frac{R_{fpon}R_{mt}}{R_{mt} + R_{pon}}i_m + \frac{N_s}{N_p} \frac{R_{fpon}R_{mt}}{R_{mt} + R_{pon}}i_L + \frac{R_{fpon}}{R_{mt} + R_{pon}}v_g \quad (C.1)$$

The waveform of the drain-to-source voltage of the rectifier flyback transistor is represented by equation:

$$\begin{aligned} V_{Qrsds} = & \frac{N_s}{N_p} R_{mt} \parallel R_{pon} \left(\frac{R_{st}}{R_{mL} + R_{son}} - 1 \right) i_m + \\ & + \left[\left(\frac{N_s}{N_p} \right)^2 R_{mt} \parallel R_{pon} - R_{st} + \frac{R_{son}R_{st}}{R_{mL} + R_{son}} - \left(\frac{N_s}{N_p} \right)^2 R_{mt} \parallel R_{pon} \frac{R_{st}}{R_{mL} + R_{son}} \right] i_L + \\ & + \frac{R_{st}}{R_{mL} + R_{son}} \frac{R}{R + R_c} v_c - \frac{N_s}{N_p} \frac{R_{mt}}{R_{mt} + R_{pon}} \left(1 + \frac{R_{st}}{R_{mL} + R_{son}} \right) v_g \end{aligned} \quad (C.2)$$

where:

$$R_{st} = R_{ws} + R_{tsn} + R_{fson} \quad (C.3)$$

The waveform of the gate-to-source voltage of the rectifier flyback transistor is described by expression:

$$\begin{aligned} V_{Qrs gs} = & \frac{N_s}{N_p} R_{mt} \parallel R_{pon} i_m + \frac{N_{dr} N_s}{N_p^2} R_{mt} \parallel R_{pon} i_L + \left(\frac{1}{R_{mt} + R_{pon}} - \frac{N_{dr}}{N_p} \right) v_g + \\ & + \frac{R_2}{R_2 + R_4} \frac{N_{df}}{N_p} V_{crave} - \frac{R_2}{R_2 + R_4} V_{FD1} - \frac{R_2}{R_2 + R_4} V_{FD2} \end{aligned} \quad (C.4)$$

where the average reset capacitor voltage V_{crave} is computed using the expression:

$$V_{crave} = \frac{1}{2} \left(V_{cr}(n_D + 1) + V_{cr}\left(\frac{n_{T-D} + 1}{2}\right) \right) \quad (C.5)$$

The waveform of the total primary current:

$$i_{mt} = \frac{R_{mt}}{R_{mt} + R_{pon}} i_m + \frac{N_s}{N_p} \frac{R_{mt}}{R_{mt} + R_{pon}} i_L + \frac{1}{R_{mt} + R_{pon}} v_g \quad (C.6)$$

The waveform of the output inductor current i_{Lr} :

$$\begin{aligned}
 i_{Lr} = & -\left(\frac{N_s}{N_p} R_{mt} \parallel R_{pon} \frac{1}{R_{mL} + R_{son}}\right) i_m + \\
 & + \left(1 - \frac{R_{son}}{R_{mL} + R_{son}} + \left(\frac{N_s}{N_p}\right)^2 R_{mt} \parallel R_{pon} \frac{1}{R_{mL} + R_{son}}\right) i_L - \\
 & - \frac{R}{R + R_c} \frac{1}{R_{mL} + R_{son}} v_c + \frac{N_s}{N_p} \frac{R_{mt}}{R_{mt} + R_{pon}} \frac{1}{R_{mL} + R_{son}} v_g
 \end{aligned} \quad (C.7)$$

C.1. Off-time topology

The waveform of the drain-to-source voltage of main primary switch:

$$V_{Qfds} = \left(R_{rpon} - \frac{R_{pof}}{R_{mt} + R_{pof}}\right) i_m + \left(1 - \frac{R_{rpon}}{R_{mt} + R_{pof}}\right) v_{cr} + \frac{R_{rpon}}{R_{mt} + R_{pof}} v_g \quad (C.8)$$

The waveform of the drain-to-source voltage of the rectifier flyback transistor:

$$V_{Qrds} = \frac{R_{rson} R_{mL}}{R_{mL} + R_{sof}} i_L + \frac{R}{R + R_c} \frac{R_{rson}}{R_{mL} + R_{sof}} v_c \quad (C.9)$$

The waveform of the gate-to-source voltage of the rectifier flyback transistor:

$$\begin{aligned}
 V_{Qrsgs} = & \frac{N_{dr}}{N_p} R_{mt} \parallel R_{pof} i_m + \frac{N_{dr}}{N_p} \frac{R_{mt}}{R_{mt} + R_{pof}} v_{cr} - \frac{N_{dr}}{N_p} \frac{R_{mt}}{R_{mt} + R_{pof}} v_g + \\
 & + \frac{R_2}{R_2 + R_4} \frac{N_{df}}{N_p} V_{crave} - \frac{R_2}{R_2 + R_4} V_{FD1} - \frac{R_2}{R_2 + R_4} V_{FD2}
 \end{aligned} \quad (C.10)$$

where the average reset capacitor voltage V_{crave} is defined by expression (C.5).

The waveform of the total primary current:

$$i_{pt} = \frac{R_{mt}}{R_{mt} + R_{pof}} i_m - \frac{R_{mt}}{R_{mt} + R_{pof}} v_{cr} - \frac{1}{R_{mt} + R_{pof}} v_g \quad (C.11)$$

The waveform of the output inductor current i_{Lt} :

$$i_{Lt} = \left(1 - \frac{R_{mL} \parallel R_{sof}}{L}\right) i_L + \frac{R}{L(R + R_c)} \frac{R_{mL}}{R_{mL} + R_{sof}} v_c \quad (C.12)$$