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Integrated SOI Waveguide Schottky Photodetector

By

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A thesis submitted to
The Faculty of Graduate Studies and Research
in partial fulfilment of the degree requirements of

Master of Applied Science

In

Electrical Engineering

Ottawa-Carleton Institute for
Electrical and Computer Engineering

Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Ontario, Canada
January 2010

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ISBN: 978-0-494-68635-5
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ISBN: 978-0-494-68635-5

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Integrated SOI Waveguide Schottky Photodetector

Submitted by **Shuxia Li, B.Sc.**

in partial fulfilment of the requirements for the degree of
Master of Applied Science in Electrical Engineering

Thesis Supervisor

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Carleton University

2010

[ii]

Abstract

Schottky barrier sub-bandgap photodetectors have been produced by depositing thin (~ 10 nm) Ni metal layers over silicon-on-insulator (SOI) rib waveguides defined by the Local Oxidation of Silicon (LOCOS) technique. Absolute responsivities of 0.47 mA/W and 0.18 mA/W were obtained for a 500 μm long photodiode with a rib width of 3 μm at wavelengths of 1310 nm and 1550 nm, respectively. Allowing for the optical insertion loss for light entering the waveguide, the adjusted responsivity is 4.7 mA/W and 1.8 mA/W at 1310 nm and 1550 nm wavelength, respectively. The reverse leakage dark current is just 0.3 nA at 1 V reverse bias. The responsivity is comparable to that obtained in SOI waveguide photodetectors fabricated using the ion implant damage technique, but the reverse leakage current should be far lower. These devices could find application in optical telecommunication and optical sensing applications.

Acknowledgements

There are a number of people who have helped me during my graduate study at Carleton University. First, I would like to express my sincere gratitude to Professor Garry Tarr for his guidance and support, for his valuable advice and encouragement in last two years.

My appreciation should go to Rob Vandusen for his enthusiastic assistance in various aspects of this work. Thanks to Carol Adams and Rick Adams for their help in the Microfabrication Laboratory and to Chris Raum for instructing me in the art of waveguide cleaving.

I also want to thank Professor Pierre Berini of the University of Ottawa for providing access to his Optical Testing Laboratory, for his advice and suggestions on optical measurement. Thanks to his group members Ewa Lisicka-Shzek, Charles Chiu, Asad Khan, Israel De Leon for their help to speed up the optical testing.

I'm grateful to Professor Q.J. Zhang for his guidance and support at the beginning of my study. Thanks to Blazenka Power for her administrative assistance in the department.

Thanks to Lingyun Xiong, Zhanjun Bai, Shaowei Liao, Anthony Singhas, Salia Mirbaha and Ryan Griffin for their helps and friendship during my time at Carleton University.

Finally, this is important thing that my husband and daughter have done for me -- for their perpetual love and optimistic spirit in my life.

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List of Symbols

q	= magnitude of electron charge
E_0	= zero vacuum level of energy
E_F	= equilibrium Fermi level
E_c	= energy level of bottom of the conduction band
E_v	= top of the valence band
E_g	= bandgap or forbidden gap
Φ_m	= metal work function voltage
Φ_s	= semiconductor work function voltage
X_s	= affinity of semiconductor, $E_0 - E_c$
V_{bi}	= built-in voltage
V_a	= applied voltage
W	= depletion layer width
h	= Planck's constant
k	= Boltzman constant
T	= depress Kevin
A^*	= Richardson constant
m^*	= effective mass of electron
ϵ_s	= permittivity of semiconductor

- N_D = density of donors
- N_c = effective density of states per unit energy at E_c
- N = semiconductor doped with donors
- P = semiconductor doped with acceptors
- λ = wavelength
- ν = frequency of light
- $h\nu$ = photon energy
- I_D = dark current
- c = speed of light
- I_p = photogenerated current
- I_s = PN junction diode reverse saturation current

Chapter 1 Introduction

Chapter 1 provides the motivation for the research described in this thesis, and outlines the technical contributions and thesis organization. It also provides a detailed background for the work reported here.

1.1 Optoelectronic Integration

Optoelectronic integrated circuits (OEICs) are becoming increasingly important in applications ranging from telecommunication to environmental and biomedical sensing. Optoelectronics monolithic integration is vital to achieve goals of low cost, very small size, and high reliability in any of these systems. The primary objectives for optoelectronic integration are increased functionality and decreased cost of components [1]. For example, the precise alignment of a single optical fiber to an OEIC that combines many laser transmitters is much simpler than the use of multiple discrete component transmitters connected to many fibers. OEICs may also be able to realize new functionality and obtain higher performance compared to systems built from discrete optical and electronic components.

1.2 SOI Waveguide Technology

OEICs are often made in epitaxial materials grown in the InGaAsP material system to take advantage of the possibility of integrating lasers and photodetectors with electronics and optical waveguides. The InGaAsP system can provide bandgaps corresponding to free-space wavelengths in the range 1.3 - 1.6 μm used in optical telecommunications [2]. However, epitaxial InGaAsP materials are very expensive, and wafer sizes are relatively small. For wavelengths longer than 1.1 μm , including the most important optical communications bands, high purity crystalline silicon is transparent, and therefore suitable for use as an optical waveguide material. To date it has not proven possible to produce efficient light emitters or lasers in silicon. However, the low cost and very large size of silicon substrates combined with the possibility of integrating high-density CMOS digital electronics with optical components has led to much research effort in developing silicon OEICs. A wide range of optical devices, including interferometers, ring resonators and directional couplers have been fabricated in silicon-on-insulator (SOI) waveguide technology [3]. There have also been several demonstrations of optical switches in this technology [4]. Silicon OEICs are usually based on SOI rib waveguides, in which a thin crystalline silicon film is formed over a layer of buried oxide SiO_2 on a thick silicon substrate. The rib is typically formed by a shallow etch into the thin silicon film. SOI waveguides are usually formed by using anisotropic plasma etching (often called “reactive ion etching”) to define the waveguide rib. Recently Rowe *et al.* at Carleton demonstrated that SOI waveguides could be made simply by using the Local Oxidation of Silicon (LOCOS) technique used for device isolation in older CMOS technologies [5].

Aside from its simplicity of implementation, the LOCOS technique provides a nearly planar surface that is ideal for integration with CMOS electronics.

1.3 SOI Waveguide Photodetectors

To take full advantage of the integration of optical devices with complex CMOS logic offered by the SOI platform, it would be highly desirable to have a photodiode capable of detecting light in the 1.3 - 1.6 μm wavelength range that could be integrated with the on chip waveguides. However, the detection of light with photon energies less than the silicon bandgap poses a difficult technological challenge. Telecom systems operating at 1.3 - 1.6 μm usually use *p-n* or *p-i-n* junction photodetectors of InGaAsP alloys, with the alloy composition chosen such that the bandgap is less than the incident photon energy. *p-i-n* photodiodes are used where high speed is required, since in these devices photogeneration takes place in the depletion region, and the electric field at the built-in junction rapidly sweeps photogenerated carriers to the contacts. Epitaxial growth of good quality InGaAsP layers on silicon is effectively impossible due to lattice mismatch, so other photodetection schemes must be sought for SOI waveguides. Recently some success in photodetector integration in SOI has been achieved by forming a *p-i-n* junction centered on the waveguide, and then introducing crystal defects in the junction using a high-energy, high dose silicon implant [6] as shown schematically in Figure 1.1. This technique has provided a responsivity up to 19 mA/W at 1.55 μm wavelength for a 6 mm long Si-based detector. This approach was extended to submicron width waveguides by Geis *et al*, giving high responsivity with broad bandwidth from 10 GHz to 20 GHz [7].

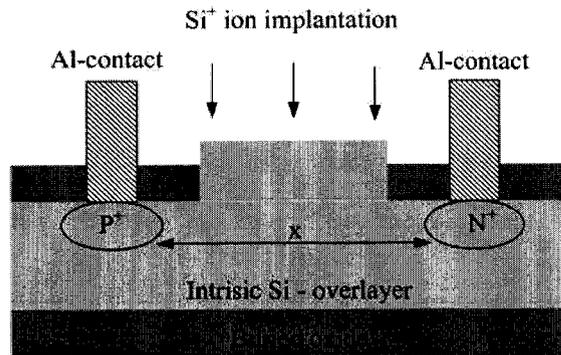


Figure 1.1 Illustration of *p-i-n* waveguide photodetector cross section [6]

There are a number of drawbacks to this implant-damage photodetector approach. The introduction of crystal damage is likely to give a high reverse leakage dark current, and the relatively low responsivity requires the use of long waveguides to obtain reasonable signal currents.

Other research by Vivien *et al.* described a Ge photodetector integrated on SOI waveguide that obtained high responsivity and large bandwidth at 1.55 μm wavelength [8]. Ge photodetectors were integrated in a rib waveguide with the metal–semiconductor–metal (MSM) structure illustrated in Figure 1.2. 1 A/W responsivity and 30 GHz bandwidth were obtained at 1.55 μm wavelength. However, the measured dark current was rather high in comparison with *p-i-n* photodiodes. This may have been caused by low Schottky barrier height of metal/Ge or by Ge/Si layer dislocations.

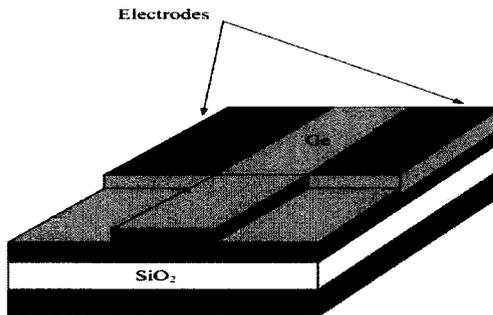


Figure 1.2 Schematic view of MSM waveguide photodetector [8]

Schottky diodes have long been used for sub-bandgap photodetection in silicon. The built-in energy barrier of a metal-semiconductor Schottky diode is less than that of a $p-n$ junction, so that photons with energy less than the bandgap may be capable of exciting electrons over the barrier and giving rise to a photocurrent. Metal silicide Schottky photodetectors on p -silicon substrates are widely used for infrared imaging and RF applications. They have the advantage of response uniformity in large area, high density arrays and compatibility with standard integrated circuit processing techniques. Moreover, the MSM Schottky diode photodetector is very popular for use at telecommunication wavelengths. It is created by depositing metal fingers on the surface of an intrinsic semiconductor crystal. It has the advantage of lower capacitance and easier fabrication compared with the $p-i-n$ photodiode [9].

To date relatively little attention has been given to Schottky diode integration with SOI waveguides. D.-X Xu *et al.* proposed the silicide MSM waveguide photodetectors on SOI substrate shown in Figure 1.3 [10]. The MSM photodetector was made by two metal silicide Schottky junctions. The gap between them is the silicon waveguide. The silicide

sidewalls provided lateral confinement of light and also served as electrodes. The main advantages of this design are high quantum efficiency and high speed. This is because the waveguide structure provides a long optical path length to increase the quantum efficiency at near infrared wavelengths. The electrodes can be made very small to reduce the transit time, facilitating high-speed operation. The drawback is that it cannot obtain high bandwidth and high responsivity at the same time.

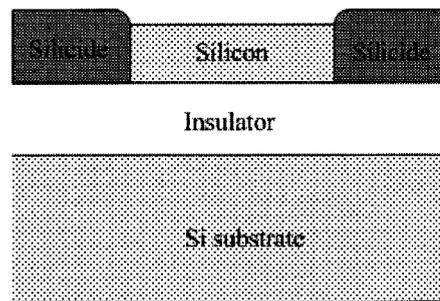


Figure 1.3 Cross-section of silicide waveguide photodetector [10]

Recently Zhu *et al.* reported the integration of Nickel silicide Schottky photodetectors with SOI waveguides formed by reactive ion etching illustrated in Figure 1.4. The Schottky barrier metal was lithographically defined to lie within the top of a 1 μm wide rib. With the sharp rib edges formed by RIE, it was essential that the metal not overlap the rib edge. Overlap would almost certainly have resulted in very high leakage [11]. The actual Schottky barrier consisted of a thin NiSi_2 layer formed on a Ti intermediate layer on the top of the SOI waveguide. The thin NiSi film exhibits good rectifying property on both *p*-type and *n*-type silicon. The titanium layer is beneficial by making NiSi_2 smoother. $\text{NiSi}/p\text{-Si}$ detectors demonstrated dark current of 3.0 nA at room temperature at 1 V reverse bias, with responsivity of 4.6 mA/W at wavelength from 1520

nm to 1620 nm. The drawback of this structure is difficulty of fabrication due to the extremely accurate lithography required to center the Schottky barrier within the narrow waveguide rib.

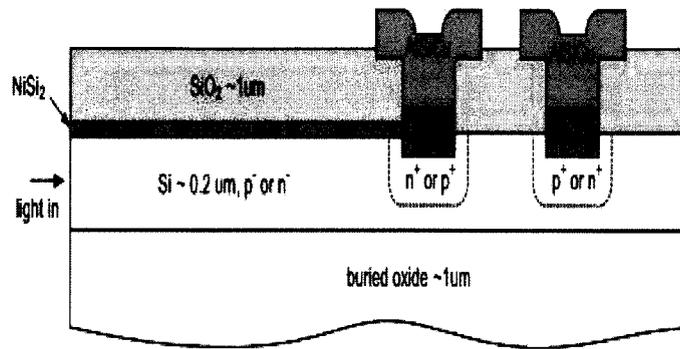


Figure 1.4 Schematic of Nickel silicide Schottky photodetectors [11]

1.4 Thesis Objectives and Contributions

The goal of this project is to demonstrate the first integration of a Schottky barrier sub-bandgap photodetector in LOCOS-defined SOI waveguide technology. The LOCOS technique offers many advantages for the formation of such a device. The surface is inherently nearly planar, so that edge leakage effects are minimized. The Schottky metal can overlap the waveguide, avoiding the need for deep submicron lithography. Integration of the detector output with CMOS electronics would be straightforward. Many issues needed to be considered in completing the project. Waveguide dimensions had to be chosen to give single-mode propagation. Metals providing barrier heights capable of detecting 1.3 - 1.6 μm light, but not give excessive dark current had to be selected. The optical attenuation becomes inevitable when metal is deposited over a waveguide rib. No appropriate simulation software was available here to accurately model this effect. An empirical approach was therefore taken in which a wide range of

metal strip lengths was investigated experimentally such that the loss could be measured. A complete photomask set was designed and made to define the devices, including provision for an ohmic contact to the silicon film. Actual photodetector samples were fabricated in the Carleton Microfabrication Facility. A significant process development effort was required to complete these devices. Issues such as metal adhesion and difficulty in etching noble metal silicide films had to be resolved. After several attempts involving considerable photomask and process refinement working examples using Ni, Pd and Pt barriers were produced. The Ni barriers provided the best performance, and this thesis focuses exclusively on these devices. Optical testing of the devices was carried out in the Professor Berini's Optical Testing Laboratory at the University of Ottawa. Waveguide photodiodes with Ni barriers gave responsivity comparable to that obtained with implant-damaged detectors, but with a low leakage current in reverse bias. The devices appear therefore very promising for integration with CMOS in future silicon OEICs.

1.5 Thesis Organization

This thesis is divided into 7 chapters.

Chapter 1 introduces the goals of this thesis and provides an overview background of previous research work.

Chapter 2 reviews the theory of metal semiconductor contact and the characteristics of a Schottky photodiode. This assists in getting the basic ideas on project design and materials selection for the Schottky diode formation.

Chapter 3 demonstrates the device design and the optical simulation, and optimizes the photodetector geometry for 1.31--1.55 μm wavelength detection.

Chapter 4 describes the fabrication procedure and facilities.

Chapter 5 presents the electrical testing set up and results analysis.

Chapter 6 demonstrates the optical testing set up, the photoresponse measurement, as well as the estimated optical loss.

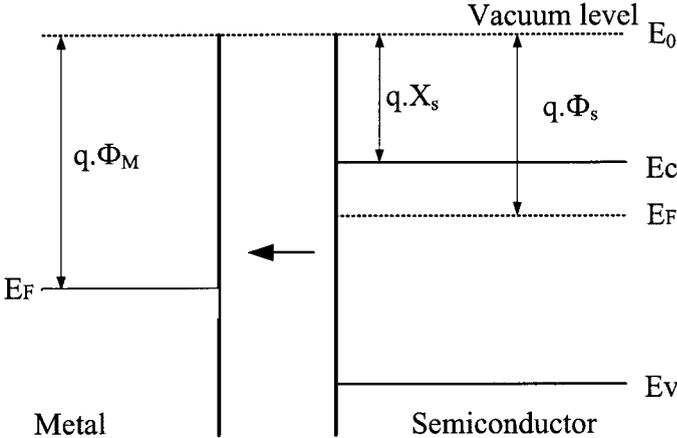
Chapter 7 summarizes the thesis and makes recommendations for future research.

Chapter 2 Background: Metal-Semiconductor Contacts

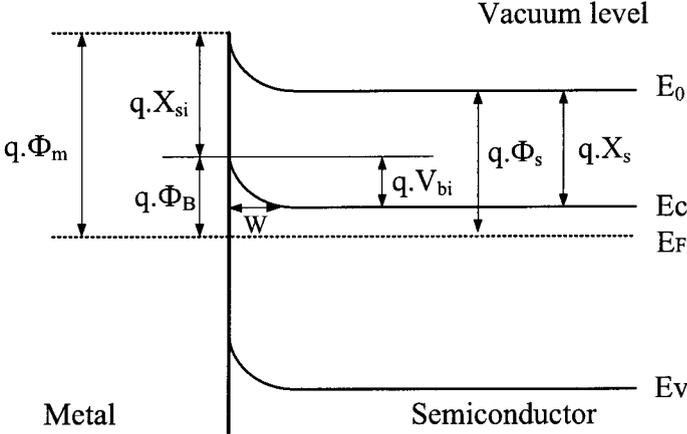
This thesis is heavily dependent on the properties of metal-semiconductor junctions. This chapter is therefore dedicated to a review of the physics of these devices, including barrier formation, current-voltage characteristics and capacitance-voltage characteristics. Then the operational principle and characteristics of a Schottky photodiode will be described.

2.1 Metal – Semiconductor Schottky Contacts

Metal-semiconductor junctions are classified as ohmic contacts or Schottky contacts. A Schottky contact displays a rectifying property allowing current flow in only one direction. The band diagrams of the metal and n -type silicon before making contact are shown in Figure 2.1a. In this case, the work function of semiconductor Φ_s is less than that of the metal Φ_m . E_0 represents the vacuum level which is the energy of free electrons. E_c is the conduction band. E_F indicates the Fermi energy which can be thought of as the average energy of an electron inside the system. $q\Phi_m$ and $q\Phi_s$ is the work function for metal and semiconductor, respectively. Work function is the energy required to move an electron from the Fermi level to vacuum level. In the semiconductor, $q\chi_s$ represents the electron affinity which is the energy required to raise an electron from the bottom of the conduction band to vacuum level.



a) before contact



b) after contact

Figure 2.1 Energy band diagrams of Schottky contact [12]

Figure 2.1b shows a condition of the two materials brought into contact. Since electrons energy in the semiconductor is higher than that in the metal, electrons will flow into the metal from the semiconductor until Fermi levels are aligned and thermal equilibrium is reached. As the result of electrons migration from the semiconductor to the

metal, the semiconductor is charged positively while negative charge resides on the surface of the metal [13]. A depletion layer with a width of W is formed in the semiconductor and an electric field is built up, thus a potential barrier qV_{bi} is established in the semiconductor. This is accompanied by bending the conduction band and the valence band upward in the semiconductor. The electrons from semiconductor moving into the metal must overcome barrier qV_{bi} which is given by equation 2.1 [14]

$$qV_{bi}=q(\Phi_m-\Phi_s) \quad (2.1)$$

In contrast, there is a potential barrier that electrons in the metal must cross over in order to move into the semiconductor, known as the Schottky barrier, whose height $q\Phi_B$ is given in equation 2.2 [14].

$$q\Phi_B=q(\Phi_m-X_s) \quad (2.2)$$

2.1.1 Current-Voltage Characteristics

When forward voltage V_a is applied to the metal-semiconductor junction, the conduction band level in the semiconductor is raised and the depletion region becomes thinner. The barrier in the semiconductor is therefore reduced from V_{bi} to $(V_{bi}-V_a)$. The new energy band diagram is illustrated in Figure 2.2. This bias reduces the electric field and the bending degree of the energy bands in the semiconductor. As the result, more electrons from the silicon will cross the barrier and flow into the metal, while the number of electrons from the metal entering the semiconductor is unchanged.

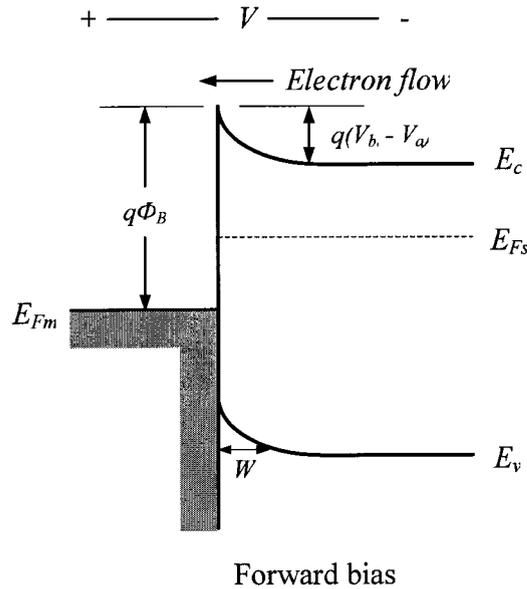


Figure 2.2 Schottky junction with forward bias applied [15]

In other words, the density of the electrons that cross from the semiconductor to the metal is increased by connecting positive bias to the metal, while the density of electrons that cross from the metal to the semiconductor stays at the thermal equilibrium value. The current density J is given by equation 2.3 [16]

$$J = A^* T^2 \exp\left(\frac{-q(\phi_B - V_a)}{kT}\right) \quad (2.3)$$

Where $A^* = \frac{4\pi q m^* k^2}{h^3}$ A^* is the Richardson constant ($120 \text{ A/cm}^2\text{K}^2$), m^* is the effective mass, V_a is applied voltage, T is temperature in Kelvin, k is Boltzmann constant ($1.38 \times 10^{-23} \text{ J/K}$), h is Planck's constant ($6.625 \times 10^{-34} \text{ Js}$).

In contrast, when a reverse bias is applied to the metal-semiconductor junction as shown in figure 2.3, the potential barrier height in the semiconductor will be increased from V_{bi} to $(V_{bi} + V_a)$. The increased barrier reduces the electrons current crossing from

the semiconductor into the metal while the electron flow from the metal to the semiconductor remains the same. As the result, the energy bands in the semiconductor are bent even further and the depletion region W becomes larger. Since the barrier faced by electron in the metal is unchanged, a small reverse bias current therefore will flow from the metal to the semiconductor.

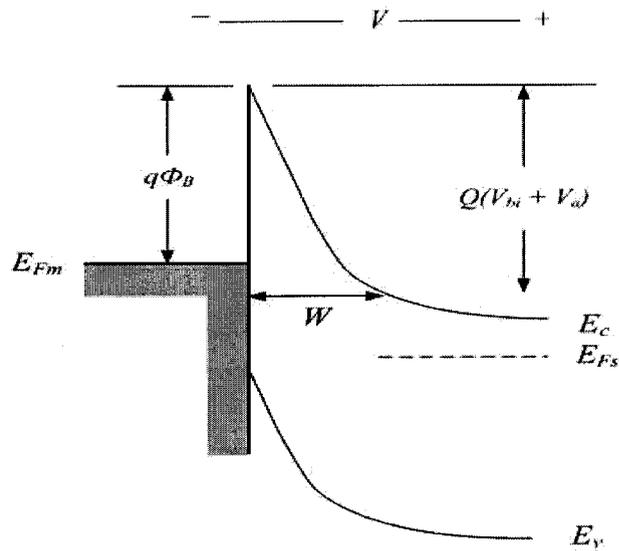


Figure 2.3 Schottky junction with reverse bias applied [15]

According to the thermionic-emission theory, the reverse current should be saturated at the J_0 given by equation 2.4.

$$J_0 = A^* T^2 \exp\left(\frac{-q\phi_B}{kT}\right) \quad (2.4)$$

However, an effect called image force barrier height lowering causes some difference from this ideal condition. The image force lowering reduces the effective barrier height from $q\Phi_m$ by $q\Delta\Phi$ given by equation 2.5.

$$\Delta\phi = \sqrt{\frac{qE}{4\pi\epsilon_s}} \quad (2.5)$$

where the value of electric field near the silicon surface can be estimated by equation 2.6 [11].

$$E = \sqrt{\frac{2qN_D(V_{bi} + V_a)}{\epsilon_s}} \quad (2.6)$$

Therefore, the actual reverse saturation current density J_0 is given in equation 2.7.

$$J_0 = A^*T^2 \exp\left(\frac{-q(\phi_B - \Delta\phi)}{kT}\right) \quad (2.7)$$

The current—voltage characteristic is drawn in Figure 2.4. The current-voltage plot of an ohmic contact is linear and symmetric while that of the Schottky barrier contact is rectifying and has nonsymmetry.

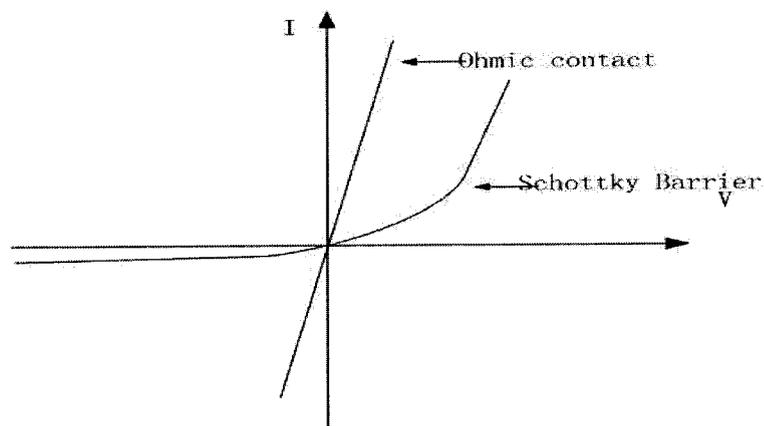


Figure 2.4 Current-Voltage characteristics of Schottky contact and ohmic contact [17]

2.1.2 Capacitance – Voltage Characteristics

When metal and semiconductor are brought into an intimate contact, a capacitance is associated with the depletion region in the metal-semiconductor junction. The junction capacitance is proportional to the interface area of the metal-semiconductor contact. It is also a function of reverse voltage applied across the Schottky diode. When a reverse voltage is applied, the depletion layer will expand and the junction capacitance will decrease. The depletion width W can be expressed by equation 2.8 [14].

$$W = \sqrt{\frac{2\epsilon_s(V_{bi} + V_a)}{qN_D}} \quad (2.8)$$

where N_D is doping level in the semiconductor, V_a is applied voltage. ϵ_s is permittivity of the semiconductor. The corresponding capacitance is obtained in equation 2.9.

$$C = \frac{\epsilon_s}{W} = \sqrt{\frac{q\epsilon_s N_D}{2(V_{bi} + V_a)}} \quad (2.9)$$

2.1.3 Schottky Barrier Height Measurement

The barrier height of metal-semiconductor junction obtained in equation 2.2 is an ideal condition. It is determined by the metal work function and the electron affinity of the semiconductor. In practice, the barrier height may be modified by interface states (energy levels within the forbidden gap of the semiconductor) localized at the metal-semiconductor interface. The Schottky barrier height can be extracted from experimental measurement of current-voltage and capacitance-voltage characteristics. The Schottky barrier height can be calculated from measured I-V data by equation 2.10 [17]:

$$\phi_B = -\left(\frac{kT}{q}\right) \ln\left(\frac{I_s}{SA^*T^2}\right) \quad (2.10)$$

where S is diode area, Φ_B is barrier height, T is temperature in Kelvin, A^* is constant of $8.16Acm^{-2}K^{-2}$, k is Boltzmann constant, q is electron charge, and I_s is the saturation current. I_s is best estimated from the intercept at $V=0$ of the linear region on the semi-logarithmic of I-V plot as shown in the example of Figure 2.5.

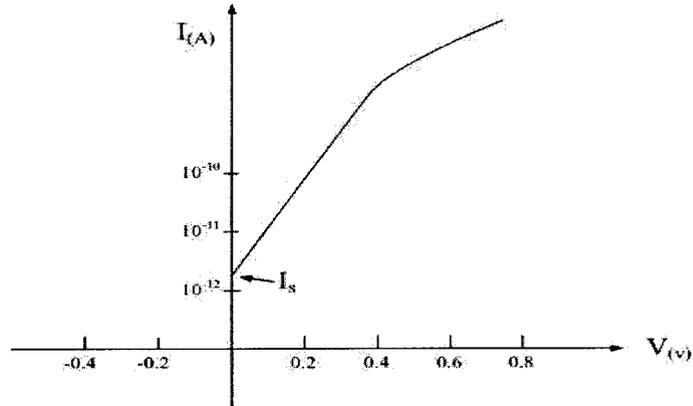


Figure 2.5 Schottky barrier height measured from I--V characteristics [18]

The Schottky barrier height also can be obtained from capacitance-voltage measurement. Rewriting equation 2.9 in 2.11 [14]

$$\frac{1}{C^2} = \frac{2(V_{bi} + V_a)}{q\epsilon_s N_D} \quad (2.11)$$

Assuming N_D is constant throughout the depletion region, we should obtain a straight line by plotting $1/C^2$ versus V_a in Figure 2.6. The barrier height can be obtained by equation 2.12 [19].

$$\Phi_B = \Phi_n + \Phi_i \quad (2.12)$$

where Φ_n is the potential difference between the Fermi level and conduction band edge, the value is given by equation 2.13 [14]

$$\phi_n = \frac{kT}{q} \ln \frac{N_c}{N_D} \quad (2.13)$$

where N_c is effective density-of-states in the conduction band ($2.8 \times 10^{19} \text{cm}^{-3}$ at temperature of 300K). ϕ_n is 0.21V if the doping concentration is 10^{16}cm^{-3} , a typical value for silicon diodes. Φ_i is built-in potential voltage and it can be found from the x-intercept of a plot of $1/C^2 - V$ as shown in Figure 2.6.

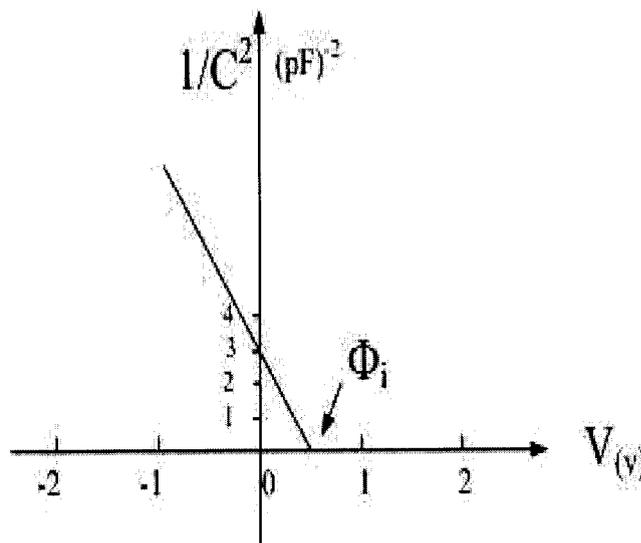
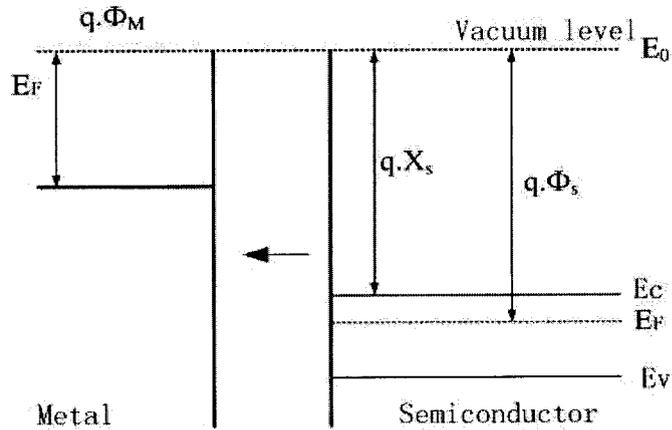


Figure 2.6 Schottky barrier height measured from C--V characteristics [19]

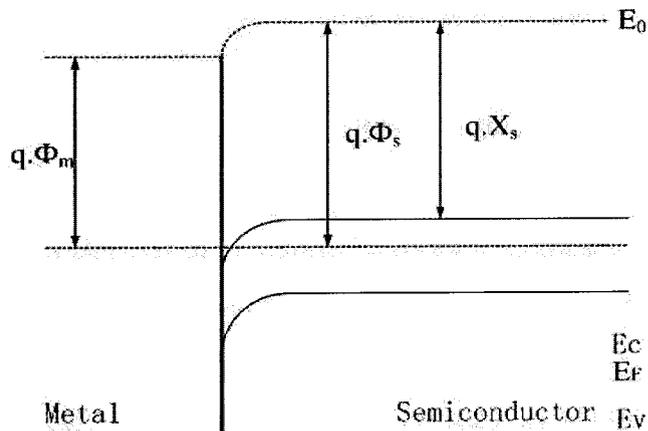
2.2 Metal-Semiconductor Ohmic Contacts

An ohmic contact has linear current-voltage characteristics and easily passes the current in both directions. In addition, the contact should not inject minority carriers and should be stable both electrically and mechanically. The most important property of an ohmic contact is its specific resistance (resistance multiplied by area).

An ohmic contact is formed when the metal work function is smaller than the n -type semiconductor work function with $\Phi_m < \Phi_s$. The contact diagram for the metal and n -type semiconductor is shown in Figure 2.7.



a) before contact



b) after contact

Figure 2.7 Energy band diagrams of idealized ohmic contact [12]

The band diagram for the materials out of contact is drawn in Figure 2.7a, and the equilibrium band diagram is given in Figure 2.7b. Upon intimate contact, electrons flow

from the metal to the semiconductor because of the smaller work function of the metal. As the result, thermal equilibrium is reached and Fermi levels are aligned. Negative charges accumulate on the semiconductor surface and positive charge on the metal surface. In the alignment of Fermi levels, a potential drop equal to $\Phi_m - \Phi_s$ is developed across the semiconductor and energy bands bend downward at the surface of semiconductor. There is no depletion region in the semiconductor so there is no barrier to limit electron flow from the semiconductor to metal.

Comparing the Schottky contact and ohmic contact, we observe that the energy bands bend downward in the ohmic contact while they bend upward in the Schottky contact. The distinguishing difference is that there is no barrier developed in the semiconductor in the ohmic contact while a potential barrier is built in the Schottky contact.

2.3 Operation Principle of Schottky Photodiode

Figure 2.8 shows a schematic of a Schottky barrier photodiode structure.

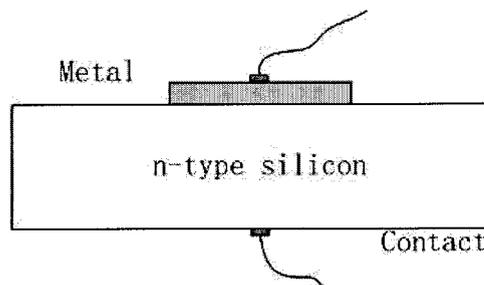


Figure 2.8 Schematic of a Schottky photodiode [20]

The Schottky barrier detector (SBD) generates photocurrent based on the internal photoemission mechanism. If the electrons in the metal absorb sufficient photon energy ($h\nu > q\Phi_B$) from incident light, the photoexcited electrons then cross the Schottky barrier

and are swept across the depletion region at the metal/semiconductor interface. As the result, a photocurrent will flow in the device. The photocurrent generation diagram is shown in Figure 2.9.

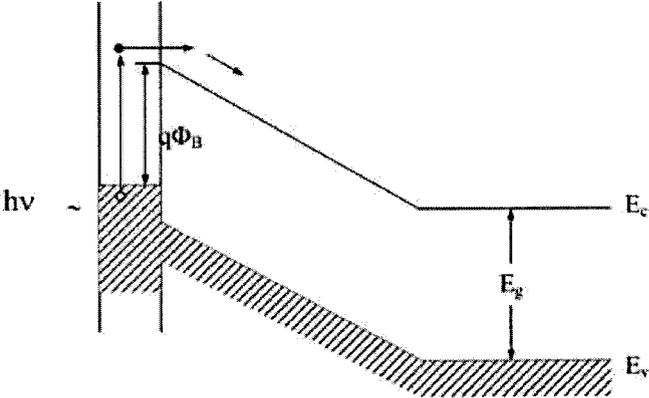


Figure2.9 Diagram illustrating photocurrent generation in reverse bias [16]

2.3.1 Dark Current (I_d) and Photocurrent (I_p)

The dark current and photocurrent are presented in Figure 2.10. The dark current is the leakage current that flows through the photodiode in the absence of light when a reverse bias is applied across the junction. The dark current in Schottky barrier photodetectors is generally attributed to majority carrier transport across the metal-semiconductor interface resulting from thermionic emission of electrons from the metal into the semiconductor [21].

When incident light impinges upon the Schottky barrier diode, in the case of $h\nu > q\Phi_B$, the electrons in the metal can be excited to surmount the Schottky barrier and be collected by the silicon. The total current is the superposition of this photocurrent and the dark current.

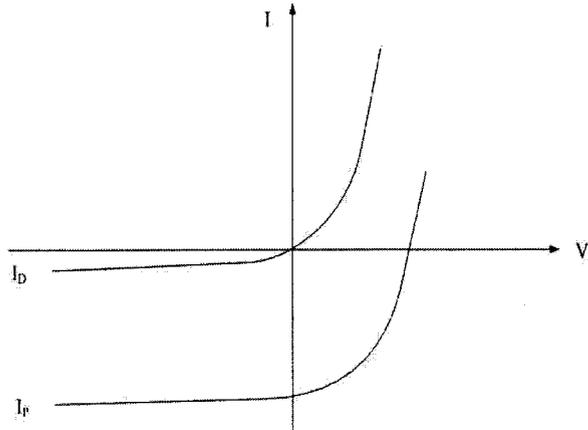


Figure 2.10 Photocurrent and dark current of photodiode [16]

2.3.2 Responsivity and Quantum Efficiency

The responsivity is defined as average current produced by per unit of incident optical power given in equation 2.14 [22]

$$R = \frac{I_p}{P_0} \quad (2.14)$$

where I_p is the photocurrent generated by incident light. P_0 is incident light power.

The quantum efficiency η of a photodiode is the percentage of photons incident on the photodiode that contribute to the photocurrent. If the photodiode operated at 100% quantum efficiency each photon of light striking the detector would result in one electron being added to the photocurrent. The quantum efficiency can be calculated by the formula [22]:

$$\eta = \frac{I_p / q}{P_0 / h\nu} = \frac{Rhc}{q\lambda} \quad (2.15)$$

where R is responsivity (A/W), λ is wavelength of incident light (nm)

Chapter 3 Device Design and Modeling

This chapter presents the design of the integrated waveguide photodetectors. The first consideration is the selection of an SOI geometry which will ensure single-mode propagation with reasonably efficient coupling to single-mode fiber. The next issue is the choice of a Schottky barrier metal which is compatible with standard silicon processing and which will provide photoresponse in the wavelength range of 1.3 – 1.55 μm . The final consideration is the trade-off between the metal thickness or length and the optical loss or photocurrent.

3.1 SOI Waveguide and Modeling

The waveguide in this project is the SOI rib waveguide, in which a uniform layer of SiO_2 is sandwiched between a thick silicon substrate and a thin surface layer of crystalline silicon. The schematic diagram of a rib SOI waveguide is shown in Figure 3.1. Here the thickness of silicon guiding layer is 2.4 μm , and the buried silicon dioxide is about 0.4 μm . The drawn width and height of rib are 4 μm (or 5 μm) and 0.5 μm , respectively. These choices reflected the type of SOI material available at Carleton. The buried SiO_2 has a refractive index of 1.46, and the crystalline silicon layer index is about 3.4. The SOI substrate provides a high index contrast between the silicon core and silicon

dioxide or air in order to confine light in the core layer by total internal reflection. The rib provides additional confinement of the light in horizontal direction.

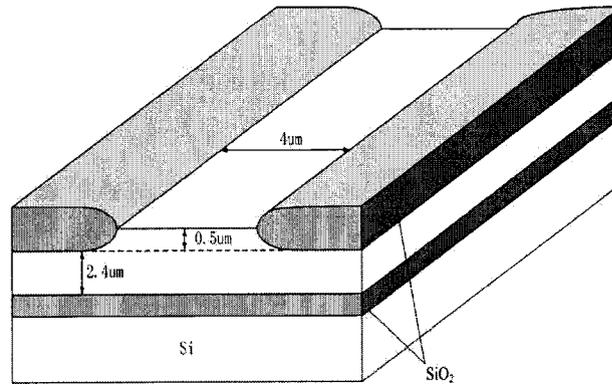


Figure 3.1 Schematic diagram of SOI rib waveguide

Figure 3.1 shows a waveguide defined by the LOCOS process, giving smoothly tapered sidewalls and providing oxide cladding to the left and right of the rib. In early SOI waveguide devices relatively thick silicon was used so that the mode size in the waveguide would be roughly comparable to that in single-mode fiber, giving reasonably efficient coupling to fiber. More recently the trend has been thinner silicon layer so that the device area can be reduced.

The cross section view of the waveguide is illustrated in Figure 3.2. W is the width of rib, H is the height of waveguide rib, h is height of the silicon core. In 1991 Soref *et al.* proposed the following empirical condition for single mode operation [23]:

$$\frac{\omega}{H} \leq 0.3 + \frac{\frac{h}{H}}{\sqrt{1 - (\frac{h}{H})^2}} \quad (3.1)$$

Pogossian *et al.* refined equation (3.1) on the basis of effective index method simulation and experimental results, concluding that the constant 0.3 should be replaced by -0.05, a somewhat more restrictive condition [24].

The dimensions of the waveguide in Figure 3.1 were substituted into equation 3.1, the results showed that the single mode condition is satisfied.

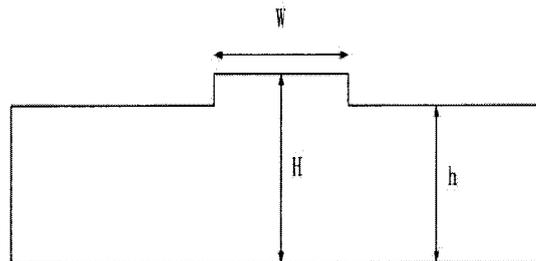


Figure 3.2 Cross section of a SOI rib waveguide

In addition, the single mode propagation in this waveguide was confirmed by optical simulations in Master's student Lynda Rowe's research [5]. The results are quoted here since the waveguides were fabricated using the same mask. In her work, the mode simulation was done both by Apollo Photonic Solutions Suite and the Finite Element Method (FEMLAB). It was found that a single TE mode was confined under the rib at ridge widths of 3 μm and 4 μm . For TM polarization, ridge widths of 3 μm , 4 μm and 5 μm all satisfied the single mode condition.

3.2 Photodetector Design and Simulation

Schottky barrier photodiodes are very attractive for photodetection because their simple structure allows for easy fabrication and integration. Almost all noble metals can be used to form a Schottky photodetector. Most of them have a high Schottky barrier height when

contacting *n*-type silicon. On the other hand, a lower barrier height can be obtained by depositing a metal on a *p*-type substrate. The relation between the barrier height and the cut-off wavelength is shown in equation 3.2 [25]. The cut-off wavelength is the maximum wavelength that will be detected by the Schottky photodiode.

$$\lambda = \frac{1.24}{\phi_b} \quad (3.2)$$

where λ is cut-off wavelength and Φ_B is the corresponding barrier height.

From equation 3.2, it can be seen that for 1.3-1.55 μm wavelength detection, the barrier height should be less than 0.8 eV. The Schottky barrier height of various metals on *n*-type silicon is shown in Table 3.1 [26]. Ni and Ti can be good candidates to form Schottky photodetectors because their barrier height on *n*-type silicon is 0.6 eV or 0.7 eV, corresponding to a cut-off wavelength of approximately 1.77 μm . Moreover, Ni has stable physical and chemical properties, and it will not be dissolved by many of the chemical solutions used during fabrication process [27].

Table 3.1 Schottky barrier height of various silicides on *n*-type silicon

Metal silicide	Schottky barrier height (eV)
TiSi ₂	0.6
NiSi, Ni ₂ Si, NiSi ₂	0.7
Pd ₂ Si	0.74
Pt ₂ Si	0.78
PtSi	0.87

Metal silicide is a thin film formed by solid - state reaction between metal and silicon, which is an attractive candidate for Schottky contacts and ohmic contacts. Based on the barrier heights presented in the Table 3.1, Pt and Pd are also useful if the Schottky barrier height can be controlled properly. In practice, the adhesion of Pt or Pd to silicon oxide is not very good which may cause problems in fabrication.

The Schottky barrier can be controlled by following methods:

1. Arizumi, Hirose and Altaf proposed using the noble metals alloys to make contact on silicon to obtain a linear variation of barrier height with composition [28].
2. Control the properties of the interfacial layer. There are reports that exposure of the semiconductor surface to oxygen before metal evaporation can alter the barrier height.
3. The most effective method is the use of ion implantation doping of the surface region to modify the potential energy barrier in the semiconductor [29].

The structure of the photodetector fabricated here is shown in Figure 3.3. A thin Ni film is deposited on the surface of the left hand waveguide rib to form a Schottky contact. The Ni film is kept very thin in an attempt to minimize absorption of light travelling through the waveguide. Directly contacting such a thin Ni layer is technically difficult, so adjacent to the rib the Ni is overlaid with a thicker Al contact layer. To form an ohmic contact to the silicon, the same aluminum is deposited in a long strip along an adjacent rib. Aluminum has low resistivity and good adhesion to silicon, silicon dioxide and nickel.

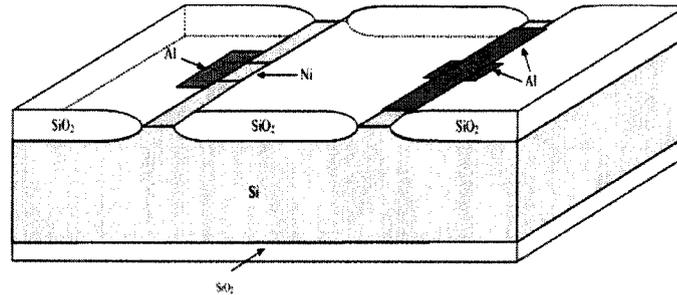


Figure 3.3 Schematic of waveguide photodetector fabricated here

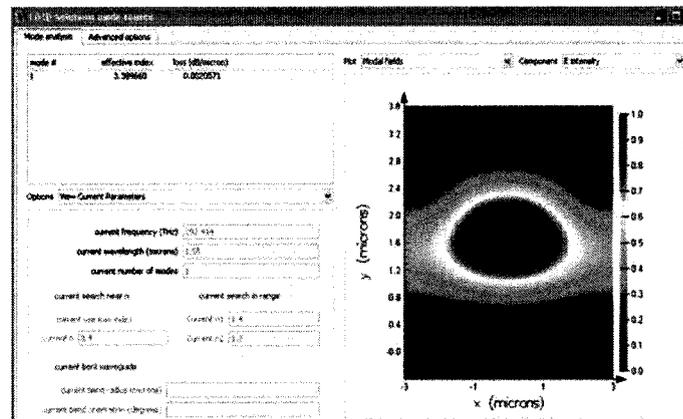
In completing the design of the photodetector structure in Figure 3.3, it is necessary to specify a length for the Schottky contact (the dimension parallel to the rib). If the contact is too short there will be very little photoresponse, but if it is too long the optical loss in the waveguide will be large, which may be undesirable in some applications. An attempt to resolve these issues was made using Finite-Difference-Time-Domain (FDTD) analysis of propagation in the waveguide with a metal overlayer. Commercial FDTD software from Lumerical Solutions was used [30].

The dimension of waveguide modelled is the same as the one given in section 3.1, and the thickness of the metal overlayer is 10 nm. The field intensity profile predicted by the FDTD solutions is shown in Figure 3.4. Interaction between the optical field and the metal layer appears to be small. Optical loss of the waveguide with Ni thin film obtained is 2.1dB/mm at wavelength of 1.55 μm . The optical losses for other metals are listed in Table 3.2.

Table 3.2 Power loss on SOI waveguide with various metals

Metal	Pt	Ni	Ti	TiN
Power loss(dB/mm)	3.3	2.1	2.7	2.2

The FDTD solutions results are suspect since the simulator makes no allowance for plasmon generation in the metal. However, the results do provide at least a starting point for selecting a diode length. Based on the simulation, diodes with length ranging from 10 μm to 1 mm were fabricated, as discussed in the next chapter.

**Figure 3.4 Field intensity profile predicted by FDTD simulation**

Chapter 4 Device Fabrication

The process used to fabricate prototypes of the waveguide photodetector structure designed in Chapter 3 is described in detail in this chapter. All fabrication work was done in the Microelectronics Fabrication Facility at Carleton University.

4.1 Mask Layout

In previous work Master's student K. Ramdas designed a general-purpose photomask to support experiments with SOI waveguide devices. This general-purpose mask is based on an array of 114 waveguide stripes of 3, 4 and 5 μm drawn widths. The waveguides are all 1 cm long and spaced 80 μm apart. The array is repeated on a grid of nine rows and nine columns. The photomask was produced by a commercial supplier to far higher standards of resolution and edge roughness than could be obtained using the in-house mask making equipment at Carleton. To save time and cost, it was therefore decided to use this existing mask as the basis for the present project. New mask layers were designed using the L-edit layout editor to define Schottky barrier metal regions, and Al ohmic contact regions. The additional mask layer were made at Carleton on photographic emulsion plates using a David Mann 1600 pattern generator and Jade AXYL step and repeat camera. The complete layout is shown in Figure 4.1, while a magnified view of a typical single diode is shown in Figure 4.2.

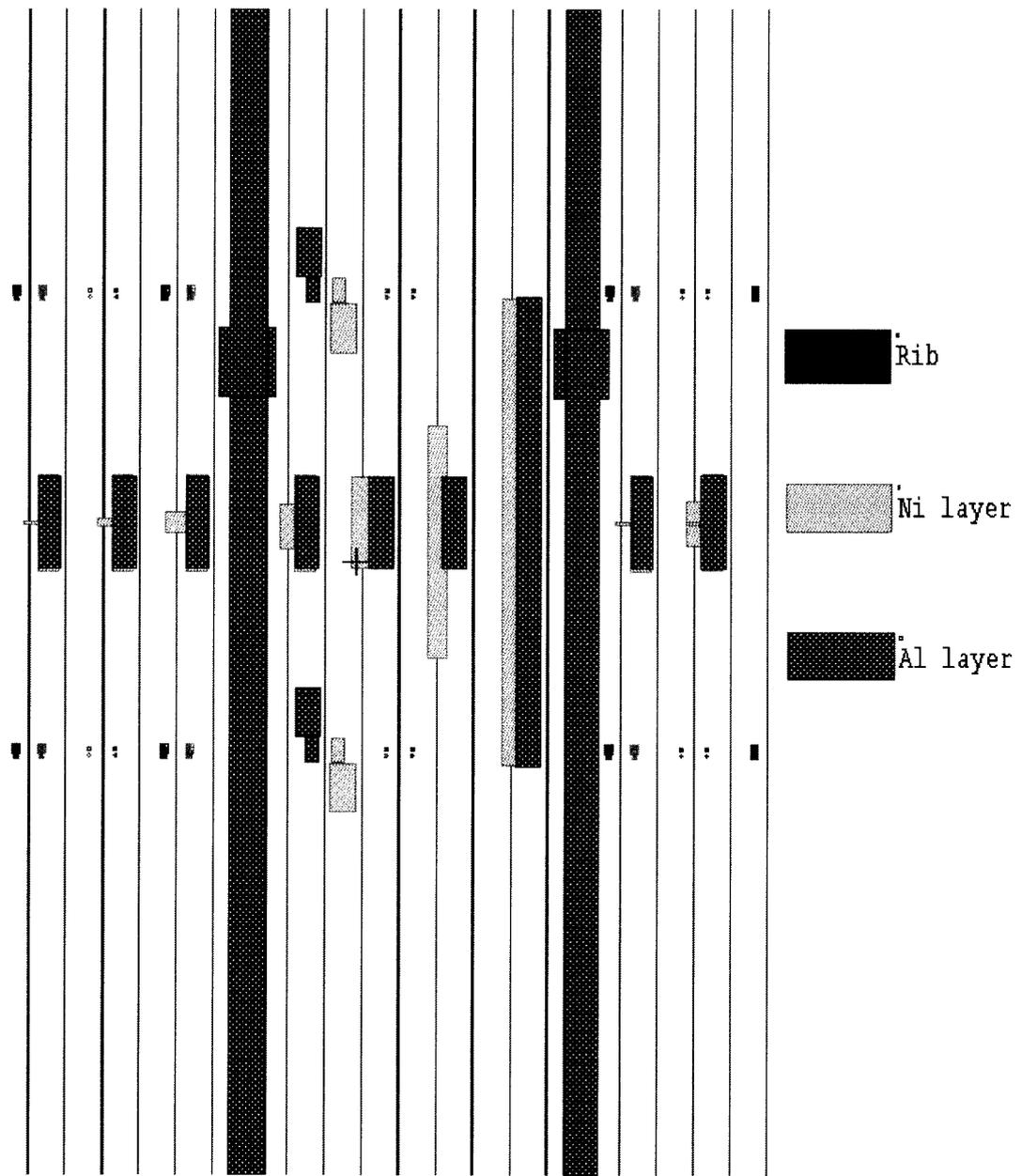


Figure 4.1 Layout of photodiode array

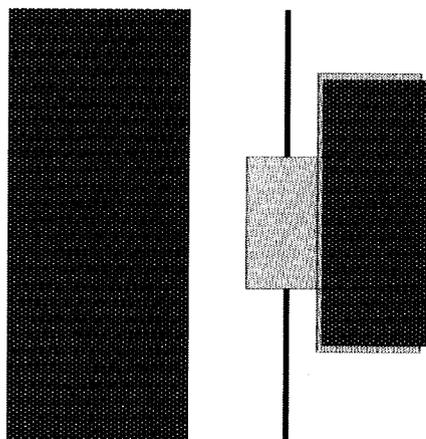


Figure 4.2 Layout of single photodiode, 100 μm length

The red straight lines are rib waveguides. In the LOCOS process these lines mark the nitride mask that protects the silicon from oxidation, leaving thick field oxide everywhere else. The light blue layer defines the Ni Schottky metal. The diode active area is formed where the Ni crosses the rib, with the rest of the Ni region serving as a contact pad. Due to the difficulty encountered in modeling optical absorption in these devices, diodes with lengths ranging from 10 μm to 1 mm were implemented, so that photoresponse and optical absorption could be studied as a function of diode length. The blue layer represents the aluminum ohmic contact to the silicon film, which serves as the substrate for the diodes. In general it is difficult to make low resistance ohmic contact to lightly-doped n-type silicon. Ideally, a phosphorus diffusion or implant should have been used to form a heavily doped n⁺ region under the aluminum to provide a low resistance contact. However, since the current flow through the contacts was anticipated to be small (in the microampere range at most), in the interest of simplicity and to save time contacts were

made directly to the lightly-doped silicon. To minimize total contact resistance, the contacts were made as long as possible (3 mm).

4.2 Substrate Selection

The SOI wafers used here were produced by the Smart-Cut process from SOITEC Corporation. Table 4.1 lists the nominal parameters of this material. Due to the high cost and limited availability of SOI material, devices were also fabricated on standard bulk (non-SOI) 1 – 10 Ωcm *p*-type monitor wafers. The monitor wafers were used as lead wafers to test and develop processes. In general devices prepared on the monitor wafers are electrically functional, but the optical waveguides are not useful due to the lack of an underlying buried oxide layer. Both the SOI wafers and the test wafers are of (100) crystal orientation.

Table 4.1 Nominal parameters of SOI wafer

Parameters	Value
Wafer thickness	500 μm
Silicon layer thickness	3.4 μm
Buried oxide layer thickness	0.4 μm
Silicon layer resistivity	7 Ωcm

The SmartCut process is an efficient method to produce SOI wafers. A thermally oxidized silicon wafer is subjected to a massive hydrogen ion implant and then bonded to a second oxidized wafer. Subsequent annealing 1100 °C causes the bonded wafer pair to

split apart along the peak of the hydrogen implant profile. A final chemical-mechanical polishing process is then used to obtain more uniform and smooth SOI surface [31]. The SmartCut technique can produce Si films of very uniform thickness and high material quality over buried oxide layers of almost any thickness, and has become the standard approach to SOI wafer production for most applications, replacing the earlier Separation by Implanted Oxygen (SIMOX) and bond-and-etch-back (BESOI) methods.

4.3 Process Flow

The primary fabrication process is listed in Table 4.2. The complete, detailed process specification or "run sheet" used in this project is given in Appendix A. The reasons behind the process steps are discussed below.

Table 4.2 The primary fabrication process of Schottky diodes

step	Processing
1	Convert <i>p</i> -silicon to <i>n</i> -silicon using <i>n</i> -well implant
2	Pad oxidation
3	Nitride deposition
4	Waveguide PE, remove nitride and pad oxide, field oxide
5	Schottky metal PE, deposition and lift-off
6	Ohmic contact PE, deposition and lift-off

4.3.1 N-well Implant

Most commercially available SOI material is lightly doped *p*-type. Fabrication of high Schottky barriers on silicon requires the use of lightly-doped *n*-type material. A light phosphorus implant followed by a drive-in diffusion was therefore used to convert the

surface film in the SOI material already available at Carleton from *p*-type to *n*-type. The drive-in is necessary to spread the phosphorus dopant evenly through the silicon film.

A suitable energy and dose for the phosphorus implant and suitable time and temperature for the drive-in were obtained through trial-and-error from SUPREM4 simulation [32]. SUPREM4 indicated a suitable doping profile could be obtained using an implant of $2 \times 10^{12} \text{ cm}^{-2}$ at 50 keV followed by a 30 min drive-in at 1100 °C. The resulting profile, shown in Figure 4.3, has a surface doping slightly greater than 10^{16} cm^{-3} and is relatively flat to a depth of over 1 μm . The first 10 minutes of the drive-in used a dry O_2 ambient to seal the surface and prevent dopant evaporation, while the final 20 minutes were in nitrogen ambient to minimize oxide fixed charge [33].

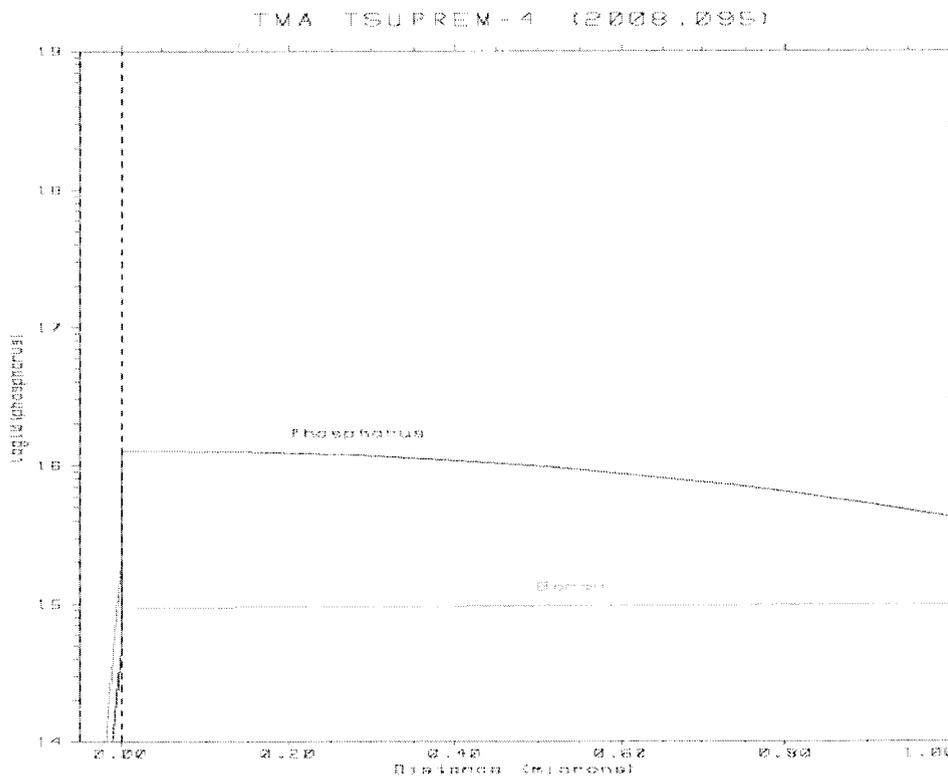


Figure 4.3 Suprem4 simulation of doping profile

4.3.2 Pad Oxidation

The pad oxide serves as a stress relief layer between the silicon substrate and overlying silicon nitride in the LOCOS process. It is required due to the large thermal expansion mismatch between silicon nitride and silicon, and avoids the formation of dislocations in the silicon. Here a 50 nm pad oxide grown in dry O₂ at 1100 °C was used. This thickness was based on the established Carleton ELEC4609 nMOS process. The thickness of oxide was measured by a Nanospec interferometer on a test wafer included in the oxidation cycle.

4.3.3 Nitride Deposition

The nitride layer is used to prevent oxidizing species from reaching the silicon surface. Because oxygen and water vapor diffuse very slowly through nitride, it serves as an oxidation mask in the field oxidation step. Based on the ELEC4609 process, an 80 nm nitride layer was used here. The layer thicknesses satisfy the requirement that the nitride thickness be no more than three times the pad oxide thickness to avoid generating dislocations [33]. The nitride layer was deposited on the pad oxide by a low pressure chemical vapor deposition (LPCVD) process from an NH₃/SiH₂Cl₂ ambient at 820 °C.

4.3.4 Waveguide Formation

Waveguides were patterned using S1811 photoresist and a Karl Suss MA6 mask aligner. After development a 60 s oxygen plasma descum treatment was carried out in a Technics Planar Etch II planar plasma etcher to remove resist residue. The nitride layer was then removed in the same etcher using CF₄/5%O₂ at 0.3 Torr and 100 W RF power. The

photoresist was then ashed in a PlasmaPreen oxygen plasma stripper, and the exposed pad oxide was removed in buffered HF solution. Actual waveguide formation was carried out by field oxidation at 1000 °C. An initial 10 min dry oxidation was used to protect the silicon surface from steam etching. The bulk of the oxidation was then completed in a wet O₂ ambient for 150 min. A 30 min O₂/2%HCl oxidation was then used to reduce stacking faults, followed by 40 min nitrogen ambient anneal to minimize oxide charges. Oxidation provides very smooth sidewalls for the waveguides. The waveguide shape is defined by the “bird’s beak” formed by the lateral diffusion of oxidant under the nitride edges which produces a slowly tapering oxide wedge that merges into the pad oxide.

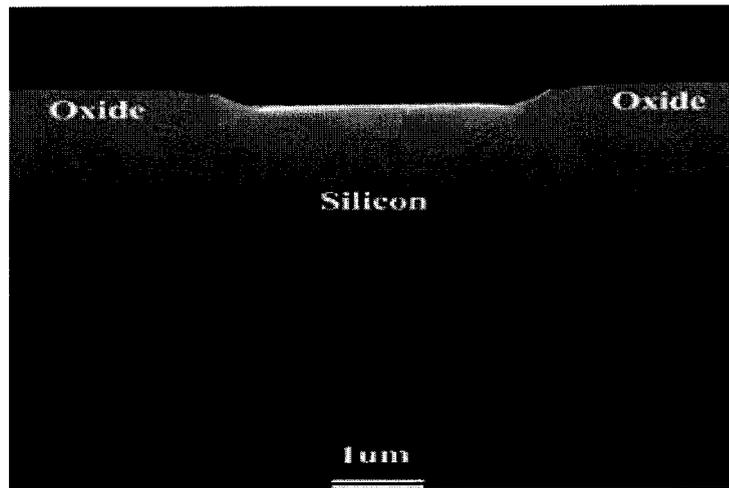


Figure 4.4 SEM picture of SOI waveguide

The top 20-30 nm of the nitride film is converted to SiO₂ during field oxidation. This converted oxide was removed in dilute HF, followed by removal of the remaining nitride and underlying pad oxide using the techniques listed above. Figure 4.4 shows SEM profile of a waveguide obtained from this process. Due to the bird’s beak encroachment

the measured rib widths were 2 μm and 3 μm corresponding to drawn widths of 4 μm and 5 μm .

4.3.5 Metallization

The ohmic contact and Schottky barrier metal layers were both defined by the lift-off technique. This technique depends on a two-layer resist structure. Here the specialized lift-off resist LOR 10B was used for the bottom layer of the stack. The LOR 10B was applied at 1500 RPM giving a thickness of 1.4 μm . It is essential that the height of this layer be greater than the deposited metal thickness. Following a bake at 175 °C for 6 min conventional S1811 resist was applied over the LOR 10B. The S1811 was then exposed and developed. The developer attacks and undercuts the LOR10B, producing a “lip” structure. The lip is critical because it creates a break in the deposited metal film, providing a path for solvent to reach the photoresist. This allows metal in the photoresist covered field regions to be lifted off, while metal contacting the substrate in the windows remains. Here Microposit remover 1165 at 60 °C was used to dissolve the LOR resist.

The metal deposition itself was performed in a cryopumped Balzer BA510 e-beam evaporator. Samples were dipped in 1%HF for 15 seconds followed by rinsing and drying by using nitrogen gas immediately before loading into the evaporator. These steps are essential to minimize the thickness of the native oxide layer in the open windows. The chamber was then pumped down to base pressure of 1×10^{-7} Torr and a Ni film of 10 nm thickness was deposited with an evaporation rate of 0.15 nm/sec. Chamber pressure rose

to approximately 10^{-6} Torr during deposition due to outgassing as the fixturing and shields heated up.

Following formation of the Schottky barrier layer, the 200 nm thick aluminum ohmic contact layer was defined using a similar lift-off process. Figure 4.5 shows an optical microscope view of the completed photodetectors. The white strips are aluminum contact on the substrate and photodiodes. The blue areas are nickel used to form photodiodes on the waveguide ribs.

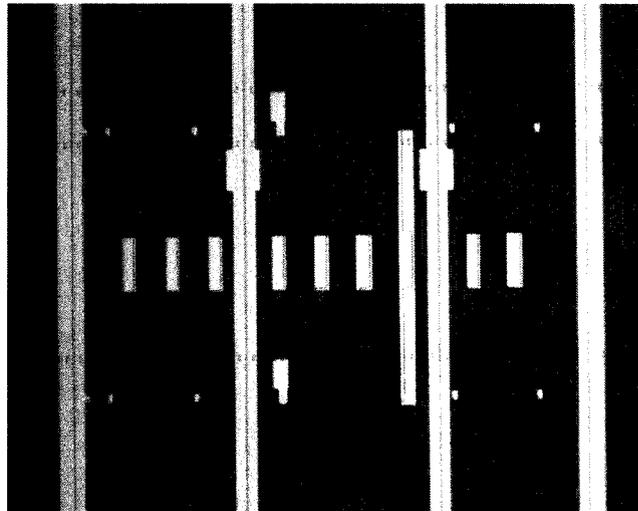


Figure 4.5 Microscope view of fabricated devices

4.4 Edge Facet Formation

In order to “couple” light into the waveguides for optical testing, a smooth, flat edge facet has to be produced perpendicular to the guide. Historically facets have usually been prepared by cleaving or sawing through the waveguide and then polishing the end face. This is a laborious task. At Carleton PhD student C. Raum has had considerable success in producing facets of high optical quality by simply cleaving through the waveguide.

For this project cleaving was used to produce the facets with assistance and guidance from C. Raum. A line was made at the edge of the sample using a sharp diamond scribe. The sample was then placed on a steel fulcrum and flexed with finger pressure causing the cleave line to propagate from the scratch mark through the waveguides. Figure 4.6 shows the resulting cleaved waveguide and edge of the die. For this sample it can be seen that the cleaving did not propagate cleanly near the bottom of the wafer, but the face is nearly perfect at the top surface where the waveguides are located.

Since the wafer used in this project is in (100) orientation, the cleaving exposes a (110) crystal plane, so that an angle of 90° is formed between the surface of the break and the wafer.

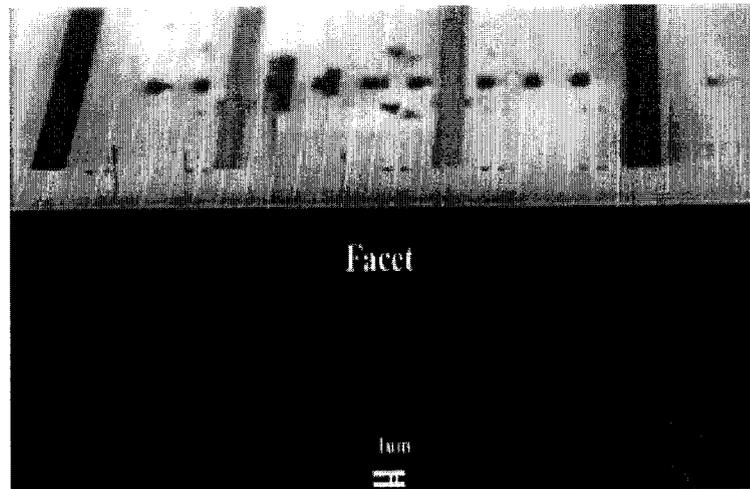


Figure 4.6 SEM image of edge facet of a cleaved wafer

Chapter 5 Results: Electrical Measurement

This chapter presents the results of electrical testing carried out on the nickel-silicon Schottky barrier diodes. Current-voltage and capacitance-voltage characteristics were recorded and analyzed. All measurements were made on the integrated waveguide diodes described in Chapter 4. In retrospect it would have been useful to have made some of the measurements on larger area diodes, such that capacitance could be measured more accurately. Unfortunately, larger devices were not available on the masks used.

5.1 Diode Dark Current-Voltage Characteristics

Dark current-voltage characteristics were measured using a Wentworth wafer prober and Hewlett-Packard 4155 Semiconductor Parameter Analyzer. The prober was enclosed in a light-shielding box during measurements. Typical current-voltage results obtained are shown in Figure 5.1.

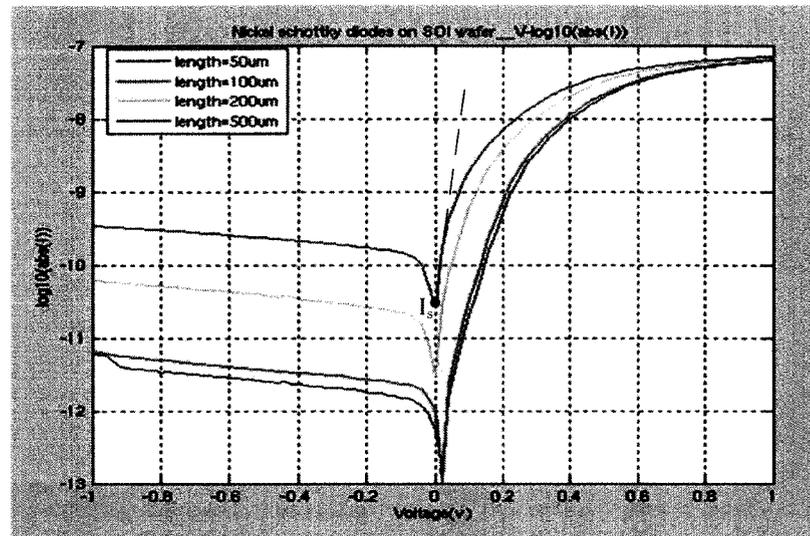


Figure 5.1 Current-Voltage characteristics of the Ni photodiodes

All diodes show rectifying property with relatively low reverse-bias leakage currents. The smallest leakage current which can be resolved with the HP4155 using “long” integration time in this set-up is slightly less than 1 pA. In forward bias the current carried by the diodes is quickly limited by the resistance of the thin metal film.

The barrier height of the photodetector can be computed based on the current-voltage characteristics. From equation 2.10, all the parameters were known except saturation current I_s which can be extracted from these plots. The Schottky barrier is 0.68 eV for 500 μm diode based on the calculation by this method.

5.2 Capacitance Measurement

The capacitance-voltage characteristics of the diodes were measured with a Hewlett - Packard 4280A C-V meter and Wentworth prober. The measurement result of a larger area diode is shown in Figure 5.2.

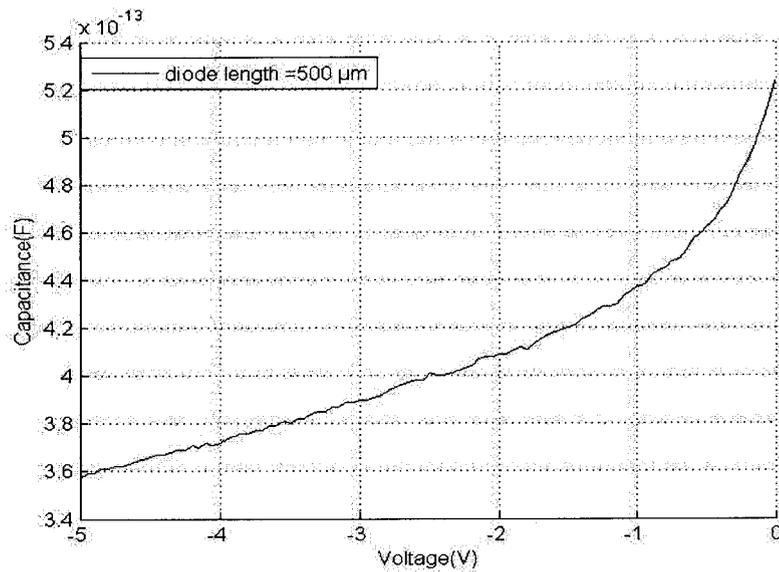


Figure 5.2 Capacitance-Voltage characteristics

The barrier height of the photodiode can also be calculated by capacitance—voltage measurement according to equation 2.12. The built in potential voltage $q\Phi_i$ is 0.5 eV from $1/C^2 - V$ plot in Figure 5.3. Therefore, the barrier height obtained by the C-V measurement is 0.71 eV which is very close to the nominal value of 0.7 eV, and in good agreement with the barrier height extracted from the I-V curve.

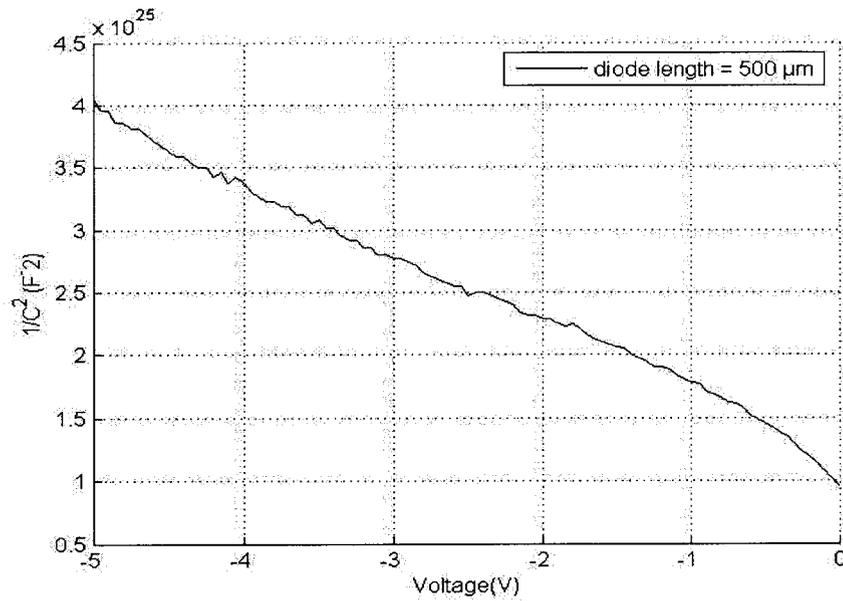


Figure 5.3 Capacitance – Voltage measurement ($1/C^2$ —V)

The doping level N_d can be estimated from the $1/C^2$ —V plot according equation 5.1[18].

$$\frac{\partial C^{-2}}{\partial V} = \frac{2}{\epsilon_s q N_d} \quad (5.1)$$

In this case, $N_d = 1.59 \times 10^{16} \text{ cm}^{-3}$, in reasonably good agreement with the Suprem simulation results shown in Figure 4.3.

Chapter 6 Results: Optical Measurement

This chapter describes the optical testing carried out on the devices fabricated in chapter 4. The experimental setup is described and results, including photoresponse and waveguides insertion losses are presented. All optical measurements were performed in Professor P. Berini's Optical Testing Laboratory at the University of Ottawa.

6.1 Photoresponse Measurement

6.1.1 Experiment Setup

A photograph of the experimental set up for the photoresponse measurement is shown in Figure 6.1. The complete system is mounted on a vibration isolated Newport optical table.

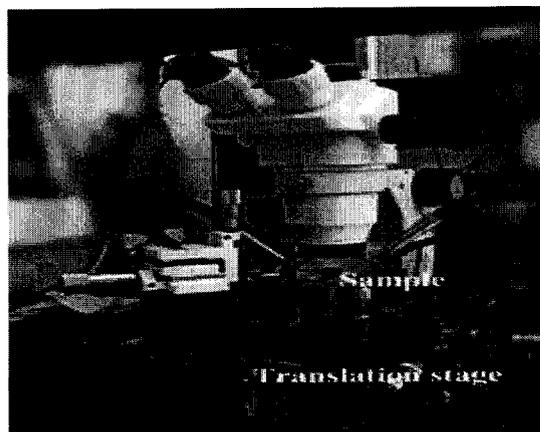


Figure 6.1 Setup used for photoresponse measurements

A tapered PM optical fiber (Oz Optics TPMJ-X-1550-8/125-0.4-10-2.5-14-1) is used to end fire couple 1270 - 1370 nm wavelength laser light provided by an Agilent 8164A lightwave measurement system into the waveguides. The light from the 8164A was passed through a polarizer to ensure that the TM mode of the guide would be excited. The incident light power was measured with an Exfo Pm-1600 High-speed power meter. The tapered fiber was mounted in a brass holder attached to a stage providing x, y, z translation and allowing for the angle of the fiber axis to be changed to align with the waveguide. The x-y position of the fiber and the fiber angle relative to the waveguide were adjusted with the aid of an optical microscope focused on the chip surface. Electrical contact to the anode and cathode of the waveguide diode was made with two probes also mounted on x, y, z translational stages. The diode output current was measured with a Keithley 2400 Sourcemeter. Figure 6.2 shows a magnified view of the chip under test, the input fiber, and the electrical probes. No bias was applied to the diodes during the test (the diodes were operated at photovoltaic mode)

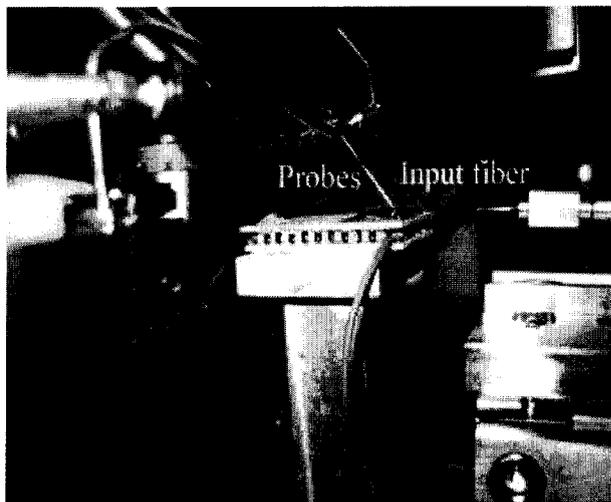


Figure 6.2 Magnified view of photoresponse measurement set-up

Alignment of the input fiber to the waveguide is a difficult and time consuming operation. First, the fiber angular rotation and tilt mounts on the fiber holder were adjusted to make the input fiber parallel with the chip surface and with the waveguides. This was done by raising the fiber above the waveguide and displacing it horizontally over the waveguide, while observing through the microscope. Next, the fiber was moved in the x and y directions in the horizontal plane to bring the fiber tip within about 8 μm of the waveguide under test. Finally, the fiber position was adjusted in the z (vertical) direction to obtain maximum photocurrent. All operations had to be done very carefully in order to avoid collision between the fiber tip and the chip, which might have broken the fiber. Figure 6.3 shows the view through the microscope when the fiber is aligned with a waveguide. The coupling efficiency of light from tapered fiber into waveguide is determined by the overlap integral of the fiber mode (at the waveguide facet) and the waveguide mode. This overlap integral was measured directly by monitoring the photocurrent as the fiber was translated in the vertical direction.

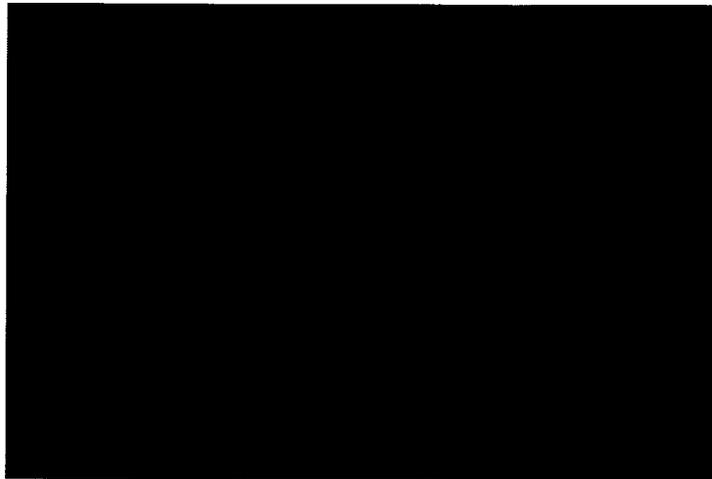


Figure 6.3 View through microscope of fiber aligned with waveguide

6.1.2 Results and Discussion

The photoresponse obtained from waveguides with fabricated widths of 2 μm (drawn width is 4 μm) and 3 μm (drawn width is 5 μm) at the 1310 nm wavelength are listed in Table 6.1. The photocurrent is typically three to six orders of magnitude larger than the dark current.

Table 6.1 Measured responsivity of Ni photodetectors at 1310 nm wavelength

Ni photodetector length (μm)	Responsivity ($\mu\text{A/W}$)	
	Diode width = 2 μm	Diode width = 3 μm
50	28	52
100	50	98
200	110	200
500	320	470

The responsivity computed on the basis of photocurrent versus the incident light power as illustrated in Figure 6.4. The responsivity of devices of various lengths is shown in Figure 6.5. This is a very conservative estimate of photoresponse, since in section 6.2 it will be shown that the coupling loss from the fiber to the waveguide is at least 10 dB. Photoresponse increases linearly with increasing diode length. This demonstrates that the absorption of light by the thin metal overlayer on the waveguide is relatively weak. This is desirable in some applications in that it allows the Schottky photodetector structure to be used without significantly attenuating the light travelling through a waveguide. In

essence the Schottky photodetector can be used as a relatively non-invasive measure of the light power in the waveguide. It is undesirable in that relatively long Schottky diodes must be used to generate a large photocurrent.

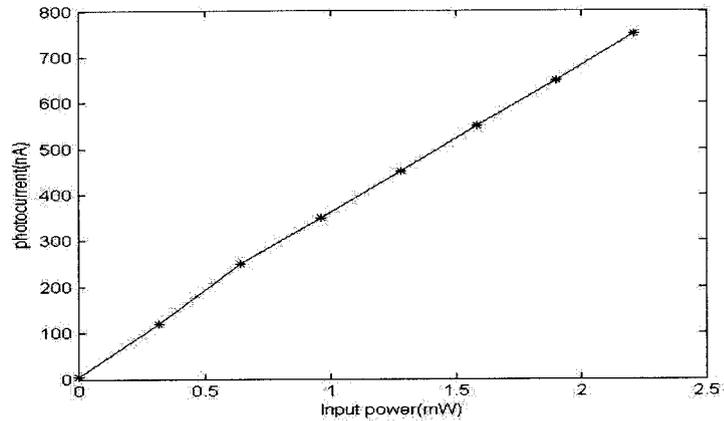


Figure 6.4 Photocurrent versus incident light power of Ni photodetector ($500 \times 2 \mu\text{m}$)

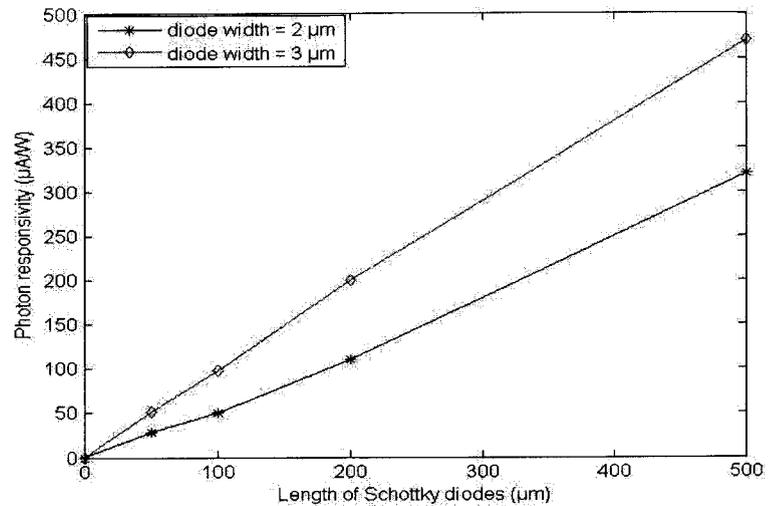


Figure 6.5 Measured responsivity of Ni photodetectors at 1310 nm wavelength

The photoresponse obtained from waveguide with fabricated widths of $3 \mu\text{m}$ at 1550 nm wavelength is listed in Table 6.2. The experimental set-up is the same as that used for

the 1310 nm measurement except the light source was replaced by a tunable external cavity laser. Although there is still measurable photocurrent at 1550 nm wavelength, the currents are relatively small compared to that obtained at 1310 nm wavelength.

Table 6.2 Measured responsivity of Ni photodetectors at 1550 nm wavelength

Length of Ni photodetector (μm)	Responsivity ($\mu\text{A/W}$)
50	10
100	30
200	65
500	180

Photoreponse for a device with area of $500 \mu\text{m} \times 3 \mu\text{m}$ is shown as a function of wavelength in Figure 6.6.

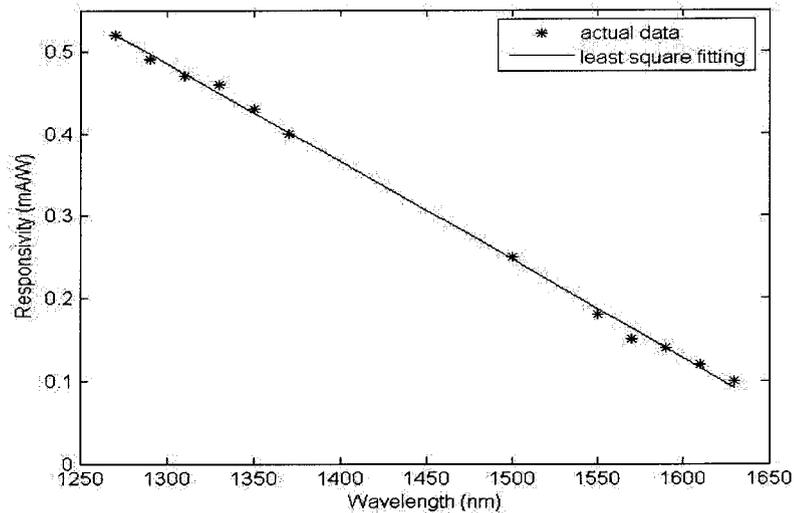


Figure 6.6 Measured responsivity of Ni photodetector at 1310—1640 nm wavelength

The photoresponse clearly drops off rapidly with increasing wavelength. This phenomenon can be explained by relationship of photoresponse and photon energy in the Fowler theory [16]. The square root of the photoresponse increased linearly with increasing photon energy (wavelength decreasing). The barrier height can be obtained from the intercept of the plot on the energy axis in Figure 6.7. The corresponding barrier height is 0.61 ± 0.02 eV from this photoelectric measurement, in reasonable agreement with the barrier height extracted from I-V and C-V curves in chapter 5.

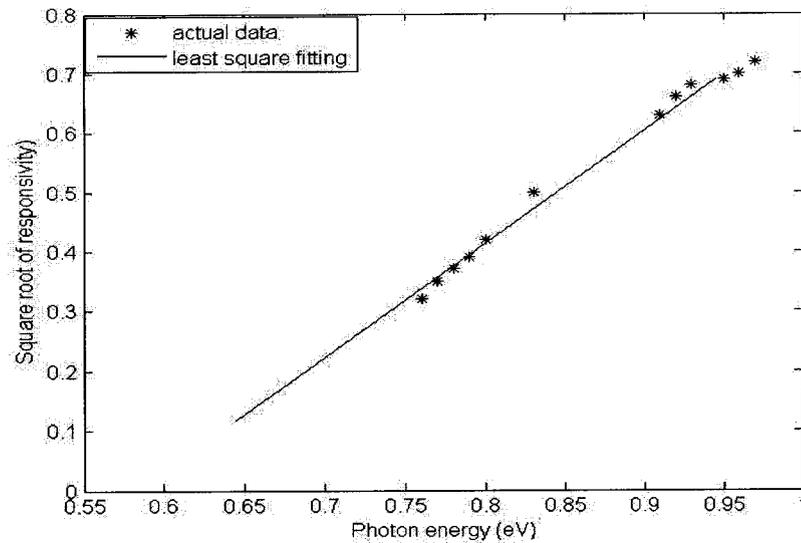


Figure 6.7 Square root of responsivity versus photon energy for Ni diode

For the responsivity measured by butt coupling TE polarized light from same laser source, the value is 50% of that obtained by TM polarized light. This can be explained by the fact that E-field vector of TE mode is parallel to the Schottky metal but TM-polarized light has E-field vector is perpendicular to the Schottky photodetector, so that there was less photocurrent generated by TE polarized light.

6.2 Optical Loss Measurement

6.2.1 Experimental Setup

The setup for optical loss measurement is shown in Figure 6.8. A more detailed view of the key components is given in Figure 6.9. The polarization-maintaining input fiber is mounted in a fiber holder attached to a translation stage providing x, y, z positioning as well as the ability to rotate the fiber in the horizontal x-y plane and control its tilt in the vertical plane. 1310 nm light is supplied to the fiber from an Agilent 8164A source through polarizer. System polarization is adjusted to excite the TM mode in the guide. The set-up differs from that described in section 6.1 in that there is provision to measure the output optical power from the waveguide. This can be done either by butt coupling a tapered fiber to the output, or collecting the output light with a microscope objective focused on a photodiode. A microscope is used to view the alignment of input and output fibers with the waveguide.



Figure 6.8 Optical loss measurement set-up

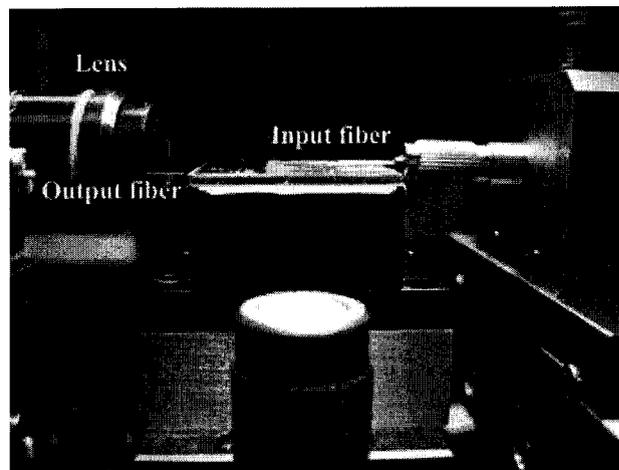


Figure 6.9 Magnified view of optical loss measurement set-up

To use the system, the input fiber was first adjusted in x-y plane to align with the waveguide under test. The objective lens was adjusted simultaneously to provide an image of the output face as shown in Figure 6.10. Once some light is visible in the output, alignment can be further optimized by adjusting the x, y, and z position of the input fiber to maximize the brightness of the image of the waveguide output. Once the brightness of the output waveguide image had been maximized, the output power was measured by bringing the 81635A power sensor close to the lens. Alternatively, in some cases a cleaved fiber was aligned with waveguide output face and the power coupled into the fiber measured with the Agilent 8163A meter. In this experiment, the insertion power loss was measured by the second method since more accurate and consistent results were obtained by this kind of setup.

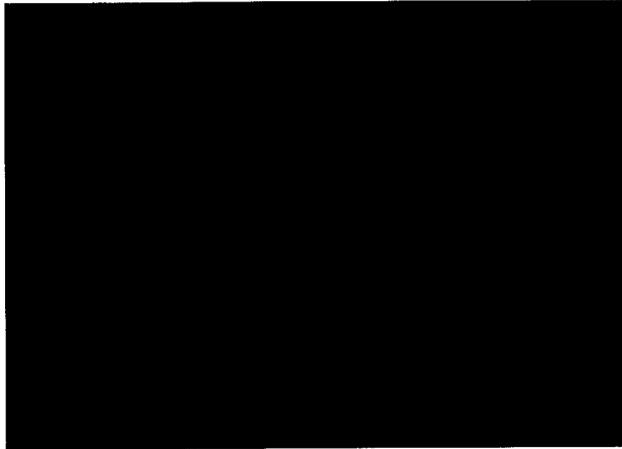


Figure 6.10 Image of waveguide output face showing strong optical coupling into guide

Once one waveguide had been measured, the chip containing the waveguide array was simply displaced with the micrometer controlling the stage to bring the next waveguide into position. This made testing much easier.

6.2.2 Results and Discussion

The maximum output power was measured for reference waveguides without Schottky metal overlayers, and for the Schottky diode photodetectors. The total power loss for transmission from the input fiber through the reference waveguides is 21-23 dB. There are potentially several factors contributing to this loss:

1. Fiber connector
2. Polarizer
3. Reflection at input and output facet: facet imperfections, index mismatch
4. Mode overlap between fiber and waveguide

5. Propagation loss in waveguide: The propagation loss in the reference waveguide was measured by cutback method in Lynda Rowe's research. It is 1 dB/cm at the worst case [5].

The additional power loss due to the Ni film with various lengths was measured on the same setup. It is found that the optical loss due to the 1 mm long metal overlayer is relatively small (less than 2.5 dB). This is an agreement with the observation that the photocurrent is roughly linear with Schottky diodes length in Figure 6.5. However, due to the limited number of Ni samples tested, this result may insufficient for an appropriate evaluation of power loss caused by the photodetector thin film.

Based on the discussion above, the power loss estimated between the input fiber and the waveguide is around 10 dB since other factors are minimum contributors in this experiment. Table 6.3 and 6.4 shows the responsivity calculated by actual light power estimated to have entered in the waveguide. The adjusted responsivity is 10 times larger than the results obtained in the measurement.

Table 6.3 Adjusted responsivity of Ni photodetectors at 1310 nm wavelength

Ni photodetector length (μm)	Responsivity (mA/W)	
	Diode width = 2 μm	Diode width = 3 μm
50	0.28	0.52
100	0.5	0.98
200	1.1	2
500	3.2	4.7

The photoresponse could, of course, be improved by using a longer diode. Indeed, Knights *et al* used diodes of comparable width but up to 6 mm in length. Moreover, since the optical loss caused by the 10 nm metal overlayer is insignificant for the diode lengths reported here, it might be possible to improve the photoresponse by increasing the thickness of the metal layer. This is a topic for future investigation.

Table 6.4 Adjusted responsivity of Ni photodetectors at 1550 nm wavelength

Length of Ni photodetector (μm)	Adjusted responsivity
Width = 3 μm	(mA/W)
50	0.1
100	0.3
200	0.65
500	1.8

Chapter 7 Conclusion and Recommendation

7.1 Conclusion

The monolithic integration of waveguides and photodetectors on a single SOI substrate has many potential applications in optical telecommunication systems and in optical sensing. The SOI planar waveguide platform has proven to be extremely versatile in integrating optical elements [34]. Integration of a simple sub-bandgap photodetector structure with SOI optical devices would greatly enhance the utility of the technology. The goal of this thesis is to design, fabricate, and test a simple Schottky barrier photodetector integrated with SOI optical waveguides.

This thesis began with a review of the literature on SOI waveguide photodetectors. There has been much interest in the sub-bandgap photodetectors fabricated by A. Knights and co-workers using ion implant damage [6]. However, these devices are likely to have high dark leakage current, and the high energy silicon implantation needed in their fabrication is not readily available. One recent report of a Schottky barrier photodetector integrated with SOI waveguides was found in the literature [11]. In this device the Schottky barrier metal was aligned within a 1 μm wide waveguide using advanced stepper photolithography, a technique which is costly and not widely available. In this thesis we have integrated Schottky barrier diodes with SOI waveguides defined using the

LOCOS technique. The smooth surface provided by LOCOS eliminates the need to confine the Schottky metal within the rib, allowing very crude and inexpensive lithography to be used to define the photodetectors. Chapter 2 reviewed the physics of Schottky diode contacts, since understanding the operation of these devices is essential to this project. Chapter 3 reported on the steps taken in designing the waveguides and Schottky contacts. The geometrical constraints for single mode operation of the waveguides were identified. Metals providing suitable Schottky barrier heights to detect light with wavelengths in the range 1.3 - 1.55 μm were selected. FDTD simulation of light propagation in a waveguide with a Schottky barrier metal overlayer was completed to obtain a rough estimate of the attenuation length for light in the waveguide. This was necessary to provide some guidance on the Schottky metal lengths to investigate experimentally. In view of the uncertainty in the FDTD model for the metal, a wide range of Schottky barrier lengths was implemented experimentally. Much effort was made in developing and optimizing the fabrication process for the devices, work which is reported in Chapter 4. Chapter 5 describes preliminary electronic testing of the Schottky diodes. Low leakage current and relatively ideal forward current-voltage characteristics were obtained, making allowance for the high resistance of the thin Schottky metal film. Schottky barrier heights were estimated both from $1/C^2 - V$ data and from the diode saturation current extrapolated from the ideal region of the forward I - V characteristics. Both methods gave a barrier height of approximately 0.7 eV, in good agreement with the literature. Optical test results were reported in chapter 6. For a diode of 3 μm width and 500 μm length, we obtained absolute responsivities of 470 $\mu\text{A/W}$ and 180 $\mu\text{A/W}$ at

wavelengths of 1310 nm and 1550 nm, respectively. This is an extremely conservative estimate of responsivity, making no allowance for coupling loss between the input fiber and the waveguide. Making allowance for such loss of 10 dB on the basis of measurements on reference waveguides reported in chapter 6, the adjusted responsivity would be 4.7 mA/W and 1.8 mA/W at wavelengths of 1310 nm and 1550 nm, respectively. The dark current was just 0.3 nA at 1 V reverse bias. The photocurrent increased linearly with waveguide length in the range 10 μm to 500 μm , indicating that absorption in the 10 nm thick Schottky metal was relatively small. Comparing with the p-i-n implant damage waveguide photodetector developed by Knights's group, Ni Schottky photodetector generated comparable photocurrent in a much smaller diode (0.5 mm length of Ni diode versus 6 mm of p-i-n diode) and used a simpler fabrication process. The dark reverse bias leakage current is also expected to be much lower although Knight's group did not report reverse bias leakage for their devices.

7.2 Future Work

There are many opportunities for future work on Schottky photodetectors integrated with LOCOS-defined SOI waveguides. It would be of interest to test detectors using other metals, including Ti, Pd and Pt. The Ni layers used here were kept very thin to minimize absorption. It would be of interest to determine the extent to which optical loss depends on the metal thickness. Thicker barrier metal layers would offer lower resistance.

It might be possible to use organic materials such as poly-1,4-phenylene vinylene and PCBM (phenyl C61-butyric acid methyl ester) blend films to form polymer heterojunction photodetectors [35, 36] which might provide good photoresponse with

very low optical loss. Comparison of the experimental results obtained here with a full theoretical analysis including plasmon-polariton generation in the thin metal film would be of great interest [37]. Finally, many opportunities exist to explore application of the waveguide photodetectors, even at the level of development reported here. For example, it would be of interest to incorporate a photodetector in an optical biosensor of the kind reported by Densmore *et al.* [38]. In optical telecom, the photodetectors developed here could be used in a channel power leveller [39].

Appendix A: Fabrication run sheet

STARTING MATERIAL: SOITEC SOI 3.4um Si 0.4um buried oxide SL-1, SL-2
Si layer p-type measured as 7 ohm-cm

1. SCREEN OXIDATION

Include test wafer

- a) RCA clean
- b) Oxidation tube temperature 1000°C
 - 5 min preheat O₂
 - 2" every 6 sec push O₂
 - 10 min oxidation dry O₂
 - 40 min anneal N₂
 - 2" every 15 sec pull N₂
 - 10 min cool N₂

Thickness measured on test wafer: 22.6 nm

STORE WAFER SL-2 FOR FUTURE USE, INCLUDE TEST WAFER TOX-1 IN THE FOLLOWING STEPS

2. N-WELL IMPLANT

- a) Ship to Kroko Implant services
- b) Implant 31P+ 50keV 2e12 cm⁻²

3. N-WELL ANNEAL

- a) RCA clean- include new test wafer for use in step 4 below
- b) Oxidation tube temperature 1000°C
 - 5 min preheat N₂
 - 2" every 6 sec push N₂

2" every 15 sec pull	N ₂
10 min cool	N ₂
Target thickness: 1.0μm	thickness measured on test wafer:

8. NITRIDE AND PAD OXIDE REMOVAL

a) Remove converted nitride

Etch in 10% HF until oxide removed from top of nitride

Estimated etch time: 2 min

Actual etch times:

b) Remove nitride (Technics Planar Etch II)

Power: 100 W Source gas: freon/5%O₂ Pressure: 0.3 Torr

Estimated etch time: 1 min 30 sec

Actual etch times:

CUT WAFERS SL-1 AND TOX-1 IN HALF

LABEL HALVES SL-1A, SL-1B, TOX-1A, TOX-1B

STORE PIECES SL1-B, TOX-1B FOR FUTURE USE

CONTINUE WITH PIECES SL-1A, TOX-1A ONLY

9. N-WELL DRIVE

a) Remove pad oxide

Etch in buffered HF or 10% HF until oxide removed from device wells

Estimated etch time: 40 sec

Actual etch times:

b) RCA clean

c) Drive-in tube temperature 1100°C

5 min preheat dry O₂

2" every 6 sec push dry O₂

11 min oxidation dry O₂

24 hour anneal N₂

2" every 15 sec pull N₂

10 min cool N₂

9. CONTACT CLEARING ETCH

Etch in "BD" etchant until bare Si exposed (approximately 1 min)

(Scribe channels will become hydrophobic)

10. SCHOTTKY METAL P.E. Mask CU-290-01

a) Dehydration bake, apply, prebake, expose, develop, postbake, descum LOR photoresist

11. SCHOTTKY METAL DEPOSITION

E-beam evaporation Pt

Target thickness: 10 nm Actual thickness:

12. SCHOTTKY METAL LIFT-OFF

lift-off metal in Microposit 1165 at 65C

rinse 10 min

13. OHMIC METAL P.E. Mask CU-290-01

a) Dehydration bake, apply, prebake, expose, develop, postbake, descum LOR photoresist

Etch in "BD" etchant until bare Si exposed (approximately 1 min)

(Scribe channels will become hydrophobic)

c) Rinse 30 min

14. OHMIC METAL DEPOSITION

E-beam aluminum

Target thickness: 0.5um actual thickness:

15. OHMIC METAL LIFT-OFF

lift-off metal in Microposit 1165 at 65C

rinse 10 min

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