**SUBMICRON CMOS COMPONENTS FOR PLL-
BASED FREQUENCY SYNTHESIS**

by

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**“Submicron CMOS Components for PLL-based
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submitted by Syed Irfan Ahmed, B. Eng.,
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Abstract

This thesis presents the design, the design methodology and the submicron implementation of a PLL-based integer-N frequency synthesizer with an external loop-filter. The synthesizer is implemented in 0.25 μm , TSMC, digital CMOS process. The frequency range is from 10 MHz to 300 MHz and the intended applications of this work are in the areas of Systems-on-Chip, clock generation, networking and audio/video systems. The acquisition time of an integer-N PLL-based synthesizer is primarily affected by the small loop-bandwidth required to improve the spectral purity of the output tone. A novel phase-frequency detector is presented that, in conjunction with the proposed acquisition-aiding methodology, can shorten the acquisition time by a factor of 3.5 compared to an unaided acquisition scenario. To set up the discussion of the proposed acquisition-aiding method, an analysis of the components that make up the total acquisition time is given from control-systems theory and PLL literature. Some acquisition-aiding techniques are compared. The circuits used to achieve such reduction in acquisition times are monolithic, simple and cost-effective. Performance is evaluated for the components and the complete synthesizer. The synthesizer dissipates 14 mW at 230 MHz while operating with a supply voltage of 2.5 V. The successes and failures associated with the three iterations of the design are also reported. Practical tips presented herein can allow a first-time designer to increase the probability of a successful design in the same area.

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Fabrication support is provided by CMC through Taiwan Semiconductor Manufacturing Company Ltd. (TSMC). The technologies, outlined below, are protected by a Non-Disclosure Agreement. Please contact CMC for further information.

- CMOSP35 - TSMC 0.35 μm Mixed-Signal Polycide 3.3 V/5 V 2-poly 4-metal
- CMOSP25 - TSMC 0.25 μm Logic Salicide 2.5 V/3.3 V 1-poly 5-metal
- CMOSP18 - TSMC 0.18 μm Logic Salicide 1.8 V/3.3 V 1-poly 6-metal

CMOSP25 is the primary technology used for this work.

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It has always been a dream to study further and I hope that this is just a beginning.

Table of Contents

Chapter 1: Introduction	1
1.1 Chapter overview	1
1.2 Introduction.....	1
1.3 Focus of the thesis.....	2
1.4 Thesis motivation.....	2
1.5 List of contributions.....	3
1.6 Organization of the thesis	4
Chapter 2: Frequency Synthesis and Phase-Locked Loops	6
2.1 Chapter overview	6
2.2 Definition of an ideal frequency synthesizer	6
2.3 Brief history	6
2.4 Frequency synthesis: Needs and challenges	7
2.5 Basic operations in frequency synthesis	8
2.5.1 Frequency multiplication	8
2.5.2 Frequency division.....	8
2.5.3 Frequency addition and subtraction: mixing.....	9
2.5.4 Frequency filtering	9
2.6 Frequency synthesizer performance criteria	10
2.6.1 Phase noise.....	11
2.7 Frequency synthesis classification	15
2.8 Linearized transfer functions for the integer-N PLL-FS.....	16
2.8.1 Order/type of phase-locked loops	19
2.8.2 Choices available for a loop-filter.....	19

2.8.3	Transfer functions of the 3 rd -order, type-II, PLL-FS	19
2.8.4	Second-order representation of a third-order system.....	23
2.8.5	System-level and circuit parameters for the 2 nd -order loop.....	24
2.8.6	Effect of feedback division ratio on the loop-filter values	25
2.8.7	Acceptable range for the damping coefficient	26
2.8.8	Acceptable range for ω_n as a fraction of f_{ref}	27
2.8.9	Acceptable range for loop-filter resistor, R_2	28
2.8.10	Noise performance and noise transfer functions.....	29
2.8.11	Dynamic loop-response	32
2.9	Publications on CMOS PLL-based synthesizers	33
2.10	Summary	37
Chapter 3: System Design of the PLL-FS		38
3.1	Chapter overview	38
3.2	Fabrication technology and FS architecture	38
3.3	Intended applications	39
3.4	Target specifications.....	39
3.5	System overview of the chosen architecture.....	40
3.6	Acquisition of lock.....	40
3.6.1	Definitions of important terms	41
3.6.2	Pull-in range for the CP-based PLL-FS	41
3.6.3	Hold-in range for the CP-based PLL-FS	41
3.6.4	Lock-range for the CP-based PLL-FS	41
3.6.5	Pull-in time	42
3.6.6	Lock-time.....	42
3.6.7	Total acquisition time.....	42
3.7	Survey of relevant publications on acquisition time	43

3.8	Proposed new PFD/acquisition-aiding mechanism	44
3.9	Phase and frequency detectors	45
3.9.1	Duty-cycle limitation for a dual PFD.....	48
3.9.2	Solution to the duty-cycle problem.....	49
3.9.3	Optional reference feedthrough at $2f_{ref}$	50
3.10	Design procedure for the APFD	50
3.10.1	Arriving at the methodology	51
3.10.2	Design methodology for the Agile-PFD (or APFD).....	53
3.10.3	Reference feedthrough revisited	55
3.10.4	Power dissipation in the three PFDs	56
3.10.5	Maximum operating frequency of a PFD	56
3.10.6	Output characteristics of the three PFDs	57
3.10.7	Deadzone simulation.....	58
3.10.8	Functional simulations	58
3.11	Lock detection overview	61
3.12	New acquisition-aiding methodology - AgileLock.....	62
3.12.1	The reset pulse	63
3.12.2	Stability considerations for the AgileLock	64
3.12.3	Advantages of the AgileLock methodology	65
3.13	PLL-FS system design and practical tips.....	65
3.13.1	Frequency planning.....	66
3.13.2	Initial planning and considerations	67
3.13.3	System design of the PLL-FS	68
3.13.4	Simulating loops with monolithic loop-filters	72
3.13.5	Compensating for loop-parameter variations.....	72
3.14	Test-set for verifying AgileLock.....	73
3.15	Typical second-order step-response equations.....	74

3.16	Methodology for the reduction of acquisition time	74
3.17	Comparison of acquisition techniques	78
3.18	Discussion of the PLL-FS acquisition results	81
3.19	Summary	82
Chapter 4: Circuit Design and Simulation Techniques		83
4.1	Chapter overview	83
4.2	Submicron implementation of the PLL-FS components	83
4.2.1	PFD	84
4.2.2	Chargepump	84
4.2.3	Suitability of loop-filter integration	89
4.2.4	Reference and feedback dividers	92
4.2.5	Voltage-controlled oscillator	95
4.2.6	Rail-to-rail VCO (VCO5)	100
4.2.7	Bandgap reference	103
4.2.8	Lock-detection circuit	104
4.2.9	Acquisition-aiding circuitry	106
4.2.10	Interface circuitry	108
4.3	Simulation techniques	109
4.3.1	General simulations	109
4.3.2	PFD	110
4.3.3	Loop-filter	110
4.3.4	Divider	110
4.3.5	VCO	111
4.3.6	Bandgap reference	112
4.3.7	Lock-detection circuit	113
4.3.8	Acquisition-aiding circuitry	113
4.3.9	Interface circuitry	113

4.4	Summary	114
Chapter 5: Test Setups and Performance Evaluation		115
5.1	Chapter overview	115
5.2	Road-map of the fabricated chips	115
5.2.1	ICECUIR0.....	116
5.2.2	ICECUIR1.....	117
5.2.3	ICECUIR2.....	118
5.2.4	ICFCUIR2.....	119
5.3	Test equipment.....	120
5.4	Printed circuit boards	121
5.5	Test setups	121
5.5.1	Monitoring high-frequency signals off-chip	121
5.5.2	Loop-filter	122
5.5.3	PFD	123
5.5.4	Divider	124
5.5.5	VCO	125
5.5.6	Bandgap reference	126
5.5.7	Detection of lock and measurement of acquisition time.....	127
5.6	Post-layout simulations and measurement results	128
5.6.1	PFD	128
5.6.2	Loop-filter and fractal capacitors.....	130
5.6.3	Divider	131
5.6.4	Post-scalar.....	133
5.6.5	VCO1-VCO5	133
5.6.6	Bandgap reference	144
5.6.7	Lock-detection circuit.....	146
5.6.8	Acquisition-aiding circuitry.....	147

5.6.9	Interface circuitry	147
5.6.10	Full PLL-FS post-layout simulations.....	147
5.6.11	Power dissipation of the PLL-FS	148
5.6.12	Full PLL-FS measurements	149
5.7	Summary	150
Chapter 6: Conclusions		151
6.1	Chapter overview	151
6.2	Conclusions.....	151
6.3	Problem areas.....	152
6.4	Some issues.....	152
6.5	Future research.....	153
6.6	Summary	153
Appendix A: Printed Circuit Boards		154
A.1	Modular approach	154
A.2	PCB-ICECUIR0, PCB-ICECUIR1 and PCB-PLLFS	154
A.3	Modular PCBs.....	156
A.3.1	Power supply filtering	156
A.3.2	Filter PCB	156
A.3.3	RF amplifier PCB.....	157
A.3.4	Bias PCB	157
A.3.5	Reset PCB	157
A.3.6	Signal PCB.....	158
A.3.7	(Input-Output) IO-Panel PCB	158
A.4	Photographs of the modular PCBs.....	159
Appendix B: Chip Level Schematics, Layouts and Pinouts		160

B.1	ICECUIR0.....	160
B.2	ICECUIR1.....	163
B.3	ICECUIR2.....	166
B.4	Details of probe1/probe2 on ICECUIR2.....	167
B.5	Details of probe3 on ICECUIR2.....	168
B.6	Details of probe4 on ICECUIR2.....	169
B.7	Details of probe5 on ICECUIR2.....	170
B.8	Details of probe6 on ICECUIR2.....	171
B.9	Details of probe7 on ICECUIR2.....	172
B.10	Details of probe8 on ICECUIR2.....	173
B.11	Details of probe9 on ICECUIR2.....	174
B.12	Details of probe10 on ICECUIR2.....	175
B.13	ICFCUIR2.....	176
B.14	Floorplan for a typical PLL-FS	177
Appendix C: Component Schematics and Layouts		178
C.1	Phase-frequency detectors	178
C.2	Chargepump and biasing circuitry	181
C.3	VCO1-VCO4	186
C.4	VCO5 (rail-to-rail oscillator)	188
C.5	Dividers (Integer-N and fractional-N)	190
C.6	Lock-detection and acquisition-aiding circuits on ICECUIR1	195
C.7	Bandgap reference	197
C.8	Serial-to-parallel converter.....	198
C.9	On-chip buffer.....	199

C.10	ESD protection module on ICECUIR2.....	199
C.11	APFD (proposed).....	200
C.12	Acquisition-aiding circuitry (proposed).....	201
Appendix D: Frequency Synthesizer Types		202
D.1	Direct Analog Synthesizers (DAS).....	202
D.2	Direct-Digital Frequency Synthesizers (DDFS)	205
D.3	Integer-N loops	209
D.4	Fractional-N loops	210
D.5	Delay-locked loop frequency synthesizer	213
D.6	Hybrid loops.....	214
References		215

List of Figures

Figure 2.1:	An ideal mixing operation in a transceiver	10
Figure 2.2:	Characterization of a noise sideband in the frequency domain	12
Figure 2.3:	Phase noise profile (exaggerated) for a typical signal (dBc/Hz).....	14
Figure 2.4:	Effect of synthesizer phase noise and spurs in a transmitter.....	14
Figure 2.5:	Frequency synthesis classification	15
Figure 2.6:	Linearized s-domain representation of a PLL-FS.....	16
Figure 2.7:	3 rd -order, type-II, CP-based PLL-FS	20
Figure 2.8:	Piece-wise linear Bode plot for $G(s)H(s)$	21
Figure 2.9:	Relationship between ζ and phase margin.....	27
Figure 2.10:	Linear model of a PLL-FS with noise inputs.....	29
Figure 2.11:	Noise transfer functions of a PLL-FS	30
Figure 2.12:	Common phase disturbances at PLL-FS input.....	32
Figure 3.1:	3 rd -order, type-II, CP-based PLL-FS	40
Figure 3.2:	Simplified PFD state-diagram.....	46
Figure 3.3:	Final locked positions with different duty-cycle inputs.....	48
Figure 3.4:	Final locked positions using divide-by-2 flipflops.....	50
Figure 3.5:	Phase-locked condition for PFD-NOR and PFD-NAND	51
Figure 3.6:	PFD-NAND waveforms: f_{ref} lagging f_{div}	52
Figure 3.7:	Truth-table and minimal expressions for APFD design.....	54
Figure 3.8:	Power dissipation in PFD-NAND, PFD-NOR and APFD.....	56
Figure 3.9:	Output characteristics of the three PFDs	57
Figure 3.10:	Deadzone simulation for the APFD	58
Figure 3.11:	Functional waveforms for PFD-NAND, PFD-NOR and the APFD	59

Figure 3.12:	Functional waveforms for the three PFDs (continued).....	60
Figure 3.13:	Typical PFD outputs in the phase-locked state	61
Figure 3.14:	Overview of the AgileLock technique	63
Figure 3.15:	Effect of the reset pulse for small frequency differences.....	64
Figure 3.16:	Frequency-plan using the crystal frequency $f_{ref} = 14.318$ MHz	66
Figure 3.17:	An example PLL-FS design (a) switching (b) loop response	70
Figure 3.18:	Step-response of a second-order control-system parameter [31].....	75
Figure 3.19:	Comparison of results from some acquisition techniques - 1	79
Figure 3.20:	Comparison of results from some acquisition techniques - 2	80
Figure 4.1:	Architectural overview of the chargepump	85
Figure 4.2:	DC characteristics of the chargepump at process corners	86
Figure 4.3:	Artifacts of the misalignment of PFD pulses	87
Figure 4.4:	Clock feedthrough cancellation schemes.....	87
Figure 4.5:	Settling performance of the chargepump	88
Figure 4.6:	Fractal capacitor (concept) and a unit fractal capacitor cell	90
Figure 4.7:	Loop-filter with lumped external inductance	91
Figure 4.8:	Pre-loadable counter module (TFF).....	92
Figure 4.9:	Architectural overview of the presettable divider	93
Figure 4.10:	Multi-modulus divider circuit using re-usable blocks	94
Figure 4.11:	n -stage ring oscillator concept	96
Figure 4.12:	3-stage ring oscillator timing diagram	96
Figure 4.13:	Oscillator spectrums (a) free-running (b) phase-locked	97
Figure 4.14:	Five-stage ring oscillator core.....	98
Figure 4.15:	Linearizing and optimizing the VCO characteristics.....	99
Figure 4.16:	Voltage-to-current converter using (a) PMOS (b) NMOS	101

Figure 4.17:	Complementary V-I converter [73]	101
Figure 4.18:	Advantage of using a rail-to-rail VCO.....	102
Figure 4.19:	Architectural overview of the bandgap reference	103
Figure 4.20:	Lock-Detection Circuit (LDC) on a fabricated chip	105
Figure 4.21:	Acquisition-aiding circuit on a fabricated chip.....	107
Figure 4.22:	Serial-to-parallel converter (basic cell).....	108
Figure 4.23:	Bandgap reference transient settling	112
Figure 4.24:	Test-planning for supplying serial input data.....	114
Figure 5.1:	Configurable NAND gate example	116
Figure 5.2:	All-NMOS source-follower as an output buffer	121
Figure 5.3:	(a) Filter PCB usage (b) Fractal capacitor test setup	122
Figure 5.4:	PFD test setup	123
Figure 5.5:	Divider test setup	124
Figure 5.6:	VCO test setup	125
Figure 5.7:	Bandgap reference test setup	126
Figure 5.8:	Lock detection and acquisition time test setup	127
Figure 5.9:	PFD-NAND functional waveforms at 100 MHz.....	129
Figure 5.10:	S(1,1) measured on the 5-layer capacitor	130
Figure 5.11:	Feedback divider measured results	131
Figure 5.12:	Feedback divider measured results (continued).....	132
Figure 5.13:	Fractional-N divider functional test results.....	132
Figure 5.14:	Post-scalar (a) divide-by-8 (b) power consumption.....	133
Figure 5.15:	VCO1 simulations and measurement results	134
Figure 5.16:	VCO1 measurements (continued).....	135
Figure 5.17:	VCO2 simulations and measurement results	136

Figure 5.18:	VCO2 measurements (continued).....	137
Figure 5.19:	VCO3 simulations and measurement results	138
Figure 5.20:	VCO3 measurements (continued).....	139
Figure 5.21:	VCO4 simulations and measurement results	140
Figure 5.22:	VCO4 measurements (continued).....	141
Figure 5.23:	VCO5 simulations and measurement results	142
Figure 5.24:	Measured duty-cycle variation for VCO1-VCO4	143
Figure 5.25:	Bandgap reference: transient performance	144
Figure 5.26:	Bandgap reference: supply and temperature-dependence.....	145
Figure 5.27:	‘SDOUT5’ output on ‘probe5’-ICECUIR2	147
Figure 5.28:	Closed-loop transient simulation of the PLL-FS	148
Figure 5.29:	Full PLL-FS measurements	149
Figure A.1:	Photographs of the PCBs for testing the fabricated chips.....	155
Figure A.2:	Power supply decoupling circuit.....	156
Figure A.3:	RF amplifier PCB overview	157
Figure A.4:	IO-Panel PCB concept	158
Figure A.5:	Photographs of the modular PCBs.....	159
Figure B.1:	Chip configuration of ICECUIR0	160
Figure B.2:	Chip layout of ICECUIR0	161
Figure B.3:	Chip photomicrograph of ICECUIR0	161
Figure B.4:	Schematic of ICECUIR0.....	162
Figure B.5:	Chip configuration of ICECUIR1	163
Figure B.6:	Chip layout of ICECUIR1	164
Figure B.7:	Chip photomicrograph of ICECUIR1	164
Figure B.8:	Schematic of ICECUIR1.....	165

Figure B.9:	Chip layout of ICECUIR2	166
Figure B.10:	Chip configuration and photomicrograph of ICECUIR2.....	166
Figure B.11:	Pin configuration and layout of probe1/probe2	167
Figure B.12:	Schematic of probe1/probe2	167
Figure B.13:	Pin configuration and layout of probe3.....	168
Figure B.14:	Schematic of probe3	168
Figure B.15:	Pin configuration and layout of probe4.....	169
Figure B.16:	Schematic of probe4	169
Figure B.17:	Pin configuration and layout of probe5.....	170
Figure B.18:	Schematic of probe5	170
Figure B.19:	Pin configuration and layout of probe6.....	171
Figure B.20:	Schematic of probe6	171
Figure B.21:	Pin configuration and layout of probe7.....	172
Figure B.22:	Schematic of probe7	172
Figure B.23:	Pin configuration and layout of probe8.....	173
Figure B.24:	Schematic of probe8	173
Figure B.25:	Pin configuration and layout of probe9.....	174
Figure B.26:	Schematic of probe9	174
Figure B.27:	Pin configuration and layout of probe10.....	175
Figure B.28:	Schematic of probe10	175
Figure B.29:	Chip configuration, layout and photomicrograph of ICFCUIR2	176
Figure B.30:	Schematic of ICFCUIR2.....	176
Figure B.31:	Layout of ICECUIR3 (not fabricated)	177
Figure C.1:	PFD-NAND schematic	178
Figure C.2:	PFD-NAND layout	179

Figure C.3:	PFD-NOR schematic	180
Figure C.4:	PFD-NOR layout (on ICFCUIR2)	180
Figure C.5:	Interconnections of the BG, BGBIAS, CPBIAS and CP blocks	181
Figure C.6:	Schematic of the chargepump	181
Figure C.7:	Schematic of the CPBIAS block	182
Figure C.8:	Layout of the CPBIAS block	182
Figure C.9:	Schematic of the BGBIAS block	183
Figure C.10:	Layout of the BGBIAS block	183
Figure C.11:	Schematic of the charge-removal circuit	184
Figure C.12:	Transmission gate (a) schematic (b) layout	184
Figure C.13:	Layout of the chargepump with the charge-removal circuit	185
Figure C.14:	Schematic of VCO1 - VCO4	186
Figure C.15:	Layout of VCO1 - VCO4	187
Figure C.16:	Schematic of the rail-to-rail bias circuit in VCO5	188
Figure C.17:	Schematic of VCO5 core	188
Figure C.18:	Layout of VCO5 (rail-to-rail VCO)	189
Figure C.19:	Schematic of the T-flipflop (TFF)	190
Figure C.20:	Layout of the T-flipflop (TFF)	190
Figure C.21:	Schematic of the 7-bit programmable FBD and RD	191
Figure C.22:	Layout of the 7-bit programmable FBD and RD	192
Figure C.23:	Schematic of the dual (programmable)-modulus fractional-N divider	193
Figure C.24:	Layout of the dual (programmable)-modulus fractional-N divider	194
Figure C.25:	Layout of the FBD (ICFCUIR2)	194
Figure C.26:	Schematic of LOCKDETECT on ICECUIR1	195
Figure C.27:	Layout of LOCKDETECT on ICECUIR1	195

Figure C.28:	Schematic of LOCKASSIST block on ICECUIR1	196
Figure C.29:	Layout of LOCKASSIST block on ICECUIR1	196
Figure C.30:	Bandgap references (a) schematics (b) layouts.....	197
Figure C.31:	Schematic of the SPC (four stages only)	198
Figure C.32:	Layout of the SPC (four stages only).....	198
Figure C.33:	On-chip buffer (a) schematic (b) layout.....	199
Figure C.34:	ESD protection module (a) schematic (b) layout.....	199
Figure C.35:	APFD schematic overview.....	200
Figure C.36:	Acquisition-aiding circuit interconnections.....	201
Figure C.37:	Lock-detection circuit (improved)	201
Figure D.1:	Multiply-mix-filter method for reference generation.....	202
Figure D.2:	Double-mix approach with drift-cancellation.....	203
Figure D.3:	Decade design for DAS using the same stage.....	204
Figure D.4:	Single DAS stage for the example design: 80 MHz - 200 MHz.....	204
Figure D.5:	DDFS block diagram and functional waveforms.....	206
Figure D.6:	Modulation possibilities in a standard DDFS	209
Figure D.7:	Basic integer-N frequency synthesizer	210
Figure D.8:	Basic concept of a fractional-N loop	211
Figure D.9:	Fractional-N beat-note cancellation.....	212
Figure D.10:	Block diagram of a DLL-based frequency synthesizer.....	214

List of Tables

TABLE 2.1:	Frequency synthesizer performance criteria	10
TABLE 2.2:	Survey of CMOS PLL-based synthesizers.....	33
TABLE 3.1:	Potential low-frequency applications of the PLL-FS.....	39
TABLE 3.2:	Target specifications.....	39
TABLE 3.3:	PFD characterization in literature	51
TABLE 3.4:	Range of system-level parameters and loop-filter values	69
TABLE 3.5:	Chargepump branch-activation calculations	73
TABLE 3.6:	Comparison of acquisition techniques	78
TABLE 4.1:	VCO1-VCO4 major specifications	100
TABLE 4.2:	Process corners.....	109
TABLE 5.1:	Fabricated chips	115
TABLE 5.2:	Details of ICECUIR2 chip contents.....	118
TABLE 5.3:	List of the test equipment.....	120
TABLE 5.4:	VCO1 measured results	135
TABLE 5.5:	VCO2 measured results	137
TABLE 5.6:	VCO3 measured results	139
TABLE 5.7:	VCO4 measured results	141
TABLE 5.8:	VCO5 measured results	143
TABLE 5.9:	Major results for the bandgap reference	146
TABLE 5.10:	Power dissipation of the PLL-FS	148
TABLE D.1:	Generation of 165.436 MHz using the example DAS	205

List of Symbols and Abbreviations

Power supply
Ground
NMOS
PMOS
Inverter
NOR gate
NAND gate
Buffer or amplifier
Library opamp
Thermistor
Resistor
Capacitor
Inductor
Diode
CMOS Vertical-PNP transistor
Any generic PCB
Port/pin (input or output)

D-type latch or D-type static flipflop

RF mixer

RF SMA/SMB connector

Voltage-controlled oscillator

Transmission gate

Nomenclature

b	Ratio of the loop-filter time constants
C_2	Loop-filter (zero) capacitor
C_1	Loop-filter (extra-pole) ripple-smoothing capacitor
D	A general multiplication or division factor
$F(s)$	Loop-filter transfer function (s-domain)
$G(s)$	Forward transfer function of the synthesizer (s-domain)
$G_{OL}(s)$	Open-loop transfer function of the synthesizer
$H(s)$	Feedback transfer function of the synthesizer (s-domain)
I_p	Chargepump current, averaged over many f_{ref} cycles
K_p	PFD gain (A/rad)
K_{vco}	VCO gain (rad/s/V)
K	Loop gain (rad)
L_{eqv}	Lumped series inductance in the PLL-FS loop-filter

M_p	Maximum overshoot of v_{cont} during PLL acquisition
N	Feedback division ratio
$N_{min}, N_{max}, N_{mean}$	Minimum, maximum and mean N values
Q	Post-scalar division ratio
R	Reference division ratio
R_2	Loop-filter (zero) resistor
T_p	Pull-in time
T_S	Settling-time
T_L	Locking-time
T_{acq}	Acquisition time
T_{r1}	Time to go from 10% - 90% of f_v during acquisition
W	The input word for an accumulator
f_{xtal}, ω_{xtal}	Hertzian, angular crystal frequency
f_n, ω_n	Hertzian, angular loop-bandwidth
f_{ref}, ω_{ref}	Hertzian, angular reference frequency
f_{div}	Hertzian frequency at the feedback divider output
f_{vco}, ω_{vco}	Hertzian, angular VCO frequency
f_{out}, ω_{out}	Hertzian, angular frequency output of the synthesizer
f_c, ω_c	Hertzian, angular loop crossover frequency
$f_{max,PFD}$	Maximum operating frequency of the PFD
f_v	Final value of v_{cont} at the end of PLL acquisition
n	Number of VCO stages or general accumulator size
ζ	Damping coefficient of the 2 nd -order loop
$\zeta_{min}, \zeta_{max}, \zeta_{mean}$	Damping coefficients at various N values
$\Phi_i(t)/\Theta_i$	Input excess-phase in the time-domain / s-domain

$\Phi_{out}(t)/\Theta_{out}$	Output excess-phase in the time-domain / s-domain
$\Phi_e(t)/\Theta_e$	Error excess-phase in the time-domain / s-domain
ϕ ,	Phase margin of the PLL-FS open-loop response
ϕ_{max}	Maximum value of phase margin at ω_c
τ_d	Per-stage delay in the ring oscillator
τ_1, τ_2	Time constants of the 2 nd -order loop
t_d	Time-delay through the frequency synthesizer
$u(t)$	Step function
v_{cont}	VCO control voltage
$\Delta\omega$	Initial angular frequency error
$\omega_{n,min}, \omega_{n,max}, \omega_{n,mean}$	Angular loop-bandwidth at various N values
ω_L	Angular lock-range
ω_{fr}	Free-running angular frequency of a VCO
ΔR	Pulse-width of the RESET signal in a PFD

Abbreviations

=PLL=	A behavioral simulator for PLL Design, a software
ALU	Arithmetic Logic Unit
ACI	Adjacent-Channel Interference
AgileLock	An acquisition technique used in this work
AM	Amplitude Modulation
AE	Antenna Errors
APFD	Agile-Phase-Frequency Detector (newly proposed)
APS	Analytical Probe Station
A/V	Audio/Visual, Audio/Video

BCD	Binary-Coded Decimal
BiCMOS.....	Bipolar Complementary-Metal-Oxide-Semiconductor
BG.....	Bandgap reference
BPF.....	BandPass filter
CMOS.....	Complementary-Metal-Oxide-Semiconductor
CMOSP25/CMOSP18 ..	Fabrication technologies (see page iv)
CP.....	Changepump
CQFP	Ceramic Quad Flat Pack, a type of package
DAS	Direct Analog Synthesis (Synthesizer)
DAC, D/A.....	Digital-to-Analog Converter (Conversion)
DC.....	Direct Current
DDFS	Direct-Digital Frequency Synthesis (Synthesizer)
DRC	Design Rule Checker, a tool
DSP.....	Digital Signal Processing
EDA	Electronic Design Automation
ESD.....	Electrostatic Discharge
EMI.....	Electro-Magnetic Interference
FAST.....	A process corner
FBD	Feedback divider
FCC.....	Frequency Control Commission
FIR	Finite Impulse Response
Free-wheeling.....	Requiring no software-controlled initialization sequence
FS	Frequency (synthesis) synthesizer
HSPICE™	A circuit simulator
IC	Integrated circuit

ICECUIR_x, ICFCUIR2. . Fabricated chips

IF. Intermediate Frequency

IIR. Infinite Impulse Response

LAN Local Area Network

LF Loop-filter

LPF Low-Pass Filter

LO. Local Oscillator

LSB. Least Significant Bit

LVS. Layout vs. Schematic, a tool

MOSFET Metal-Oxide-Semiconductor Field Effect Transistor

MSB Most Significant Bit

N.A. Not Available/Not Applicable

NTSC North American Television Standards Committee

OPP. One-Pulse per Push, a circuit

OTA Operational Transconductance Amplifier

PAL. Phase Alternation Line

PCB. Printed Circuit Board

PFD. Phase-Frequency Detector

PD. Power-down

PLL. Phase-Locked Loop

PLL-FS. Phase-Locked Loop based Frequency Synthesizer

PM Phase Margin of the PLL-FS open-loop response

PN. Phase noise

PSD. Power Spectral Density

PSS Periodic Steady State (A tool within Spectre™)

PSRR	Power Supply Rejection Ratio
PVT.....	Process, Voltage and Temperature
RAM.....	Random Access Memory
RD.....	Reference divider
RF	Radio Frequency
RFIC.....	Radio-Frequency Integrated Circuit
RLC	Resistance, Inductance, Capacitance
ROM.....	Read-Only Memory
SC.....	Switched-Capacitor
Spectre [™]	A circuit simulator
SSB.....	Single Sideband
SLOW.....	A process corner
SMA/SMB	Types of RF connectors
TC.....	Temperature Coefficient
TF	Transfer Function
TFF.....	A pre-loadable, T-flipflop based counter module
TYPICAL.....	A process corner
TSPC.....	True Single Phase Clock
VCO	Voltage-controlled oscillator
VLSI.....	Very Large Scale Integration
VTF.....	Voltage-to-Frequency
V-I.....	Voltage to current

1.1 Chapter overview

This chapter provides an introduction and explains the focus of this thesis and the motivation behind this work. Further, it lists the contributions arising from this work and explains the thesis organization.

1.2 Introduction

Complementary-Metal-Oxide-Semiconductor (CMOS) technology is, at the time of this writing, a cheaper alternative to other commercially available IC fabrication processes. RF design has traditionally been done in Bipolar or Gallium Arsenide (GaAs) technologies and SiGe-Bipolar process is also gaining widespread acceptance. Recent advances in CMOS fabrication have achieved an f_{max} greater than 50 GHz. A minimum feature-size of 0.11 μm is commercially available (as of 2001) and there is a growing financial incentive to develop single-chip transceivers, high-speed microprocessors, fiber-optic sub-systems and complex Systems-On-Chip (SoC) using CMOS technology [65][66][67]. RF-CMOS is an area of active research driven primarily by the wireless market. CMOS is the technology of choice for consumer electronics, microprocessors, networking, memories and video clock generators because of its very low power dissipation and cost. The design of large mixed-signal chips is driven by time-to-market and total

cost. This requires an in-depth understanding of the target technology, system architecture, circuit techniques, noise issues and the simulation methods that can optimize performance in a shorter time using behavioral modelling.

1.3 Focus of the thesis

The focus of this thesis document is the fabrication and testing of a submicron integer-N Phase-Locked Loop (PLL) based Frequency Synthesizer (FS) for the low-frequency range. Hereinafter, it is called the PLL-FS. The loop filter (LF) is external due to the general-purpose nature of the chip. One of the targeted applications is a video clock-generator in the 10 MHz to 200 MHz range. The fabrication technology is CMOSP25. The submicron components required to build a general-purpose, cost-effective, and a fast-locking PLL-FS are presented. A novel phase-frequency detector is proposed along with a methodology for reducing the acquisition time that is often the bottleneck for integer-N designs. The test results are shown for the individual components and the complete PLL-FS. This document can be useful for first-time PLL designers as well as the practicing engineer looking for practical FS design tips in a submicron, low-voltage digital CMOS technology. A background on PLL theory is presented later in Chapter 2.

1.4 Thesis motivation

A frequency synthesizer generates the necessary system clocks using an off-chip, high-Q quartz crystal or some other stable frequency reference. It is central to the operation of other on-chip sub-systems. Synthesizers find applications in transceivers, memories, Central Processing Units (CPU), clock and data recovery systems, Digital Signal Processing (DSP) chips, Audio/Visual (A/V) systems and broadband networking chips. In short, any system that requires a clock signal, contains either an external frequency reference or a frequency synthesizer.

PLLs were first introduced in 1932 [26]. The first PLL-based synthesizer was reported around 1970 [2]. Several design variants of the PLL-FS retain the major market share of the frequency synthesizer industry today. A good understanding of PLL-FS design can reduce development costs and time-to-market in addition to improving portability across upcoming CMOS technologies. Essentially an integer-N PLL-FS has five main components. These include:

- Reference divider (RD)
- Phase-frequency detector (PFD) with chargepump (CP)
- Loop-filter (LF)
- Voltage-controlled oscillator (VCO)
- Feedback divider (FBD)

Some non-essential but important accompaniments are:

- Bandgap reference (BG); used to establish clean voltages and bias currents.
- Serial-to-parallel converter (SPC); used to supply data to the PLL-FS.
- Lock-detection circuit (LDC); used to disable the RF output during acquisition.
- Acquisition-aiding circuitry; used to reduce acquisition times.

The input frequency is derived from a high-Q crystal oscillator.

1.5 List of contributions

The contributions arising from this work are as follows:

- A step-by-step methodology for implementing a submicron CMOS, integer-N PLL-FS is presented. The information presented herein can allow a first-time FS designer to design a moderately complex PLL-FS with a higher probability of success. A behavioral simulator is used to simulate and optimize the system-level PLL-FS per-

formance. Simulation methods, circuits, layout techniques and a floorplan are included for a typical PLL-FS.

- The design methodology for a novel PFD, called the Agile-PFD (or APFD) is presented. The APFD works like a conventional PFD for a phase difference of less than $\pm 2\pi$ and provides DC outputs for larger phase and frequency differences. The APFD enhances the acquisition performance of a PLL-FS.
- Various components that make up the total acquisition time are analyzed using relevant literature adopted from control-systems [31] and PLL theory. As a result, a methodology called the “AgileLock” is proposed that reduces the unaided PLL-FS acquisition times by a factor of 3.5. The submicron circuits required to achieve such reduction in acquisition times are monolithic, simple and cost-effective.
- A rail-to-rail configurable VCO is presented that uses the V-I converter circuit from [73]. The core of the VCO is adopted from this work. The rail-to-rail VCO topology allows the use of the entire voltage range in a low-voltage submicron technology. The VCO gain is required at the LF design stage but after fabrication, it can vary almost by a factor of two. The ability to configure the VCO gain during PLL-FS operation can result in a more predictable performance as a passive on-chip LF cannot be modified so easily. The circuitry required to tune the VCO characteristics, using switchable current sources, can be implemented using digital techniques and is not shown for this work.

1.6 Organization of the thesis

There are six chapters in the thesis. These are organized as follows:

Chapter 2 mentions the well-known frequency synthesis techniques and provides a review of PLL-FS concepts. The theory presented in Chapter 2 is later used in Chapter 3 to reduce the acquisition time of a 3rd-order, type-II PLL-FS. The pros and cons of other pop-

ular frequency synthesis architectures are discussed, from the IC-design perspective, in Appendix D for completeness.

Chapter 3 explains the design procedure for the newly proposed APFD and proposes the AgileLock acquisition technique. A second-order step-response treatment is adopted from control-systems literature to better understand various components of the PLL-FS acquisition time. The methodology for reducing acquisition times is proposed and analyzed. An example system-level PLL-FS design is shown using hand calculations and is later optimized using a behavioral simulator. Some acquisition techniques are compared using time-domain simulations and the results thus obtained are presented.

Chapter 4 presents the circuit design of the submicron components in the PLL-FS. Some helpful simulation techniques are also discussed.

Chapter 5 presents the performance-testing results along with the post-layout simulation results for the components and the complete CMOSP25 PLL-FS.

Chapter 6 outlines the conclusions drawn from this work and proposes some future research possibilities.

Appendices contain information about Printed Circuit Boards (PCB), chip layouts, component schematics, pinout diagrams, layout diagrams and a discussion on some popular frequency synthesis architectures.

References cited herein are listed at the end of this thesis document

Frequency Synthesis and Phase-Locked Loops

2.1 Chapter overview

This chapter briefly discusses the frequency synthesis background. To maintain focus on the integer-N PLL-FS, some popular synthesis techniques compatible with monolithic integration are presented in Appendix D, in the interest of completeness. The PLL theory presented here is utilized in Chapter 3 to design a PLL-FS and to reduce its acquisition time. This theory also forms the basis for the component design in Chapter 4. A discussion on PLL-FS acquisition theory is presented later in Chapter 3 to avoid repetition. A survey of the literature on CMOS PLLs is given at the end of this chapter.

2.2 Definition of an ideal frequency synthesizer

An ideal frequency synthesizer is a device that can generate, within its operating range, an arbitrary rational frequency using a frequency reference mechanism. Its output is not affected by time, circuit conditions and environmental variations. It can switch between any two frequencies within its frequency range in zero time using a command interface. The term ‘Frequency Synthesizer’ was first used in 1943 [1].

2.3 Brief history

Human voice is an example of a synthesized sound output and speech-processing remains an active research area. From the early days of mechanical gears when mathemat-

ical tables were used to optimize gear ratios, to the control and miniaturization made possible by PLLs and IC technology and on to the modern day Direct-Digital Frequency Synthesizer (DDFS) and Optical Synthesizers, the field frequency synthesis has continued to use advancing technology. An up-to-date account of historical and mathematical developments in the frequency synthesis domain can be found in [2].

2.4 Frequency synthesis: Needs and challenges

Frequency synthesizers (FS) are an integral part of all communication systems and form basic building-blocks for most data-processing and display systems as well. With hand-held, interactive, power-conscious and light-weight mobile devices characterizing the internet-aware economy, technical advancements in synthesizers are made on a regular basis. From the cost perspective, reducing component count on the PCB is important. Miniaturized components with better Electro-Magnetic Interference (EMI) characteristics reduce cross-talk and Adjacent Channel Interference (ACI). The technical challenges at the chip level are to achieve the following:

- Minimum phase noise (PN) and minimum spurious content in the output tone
- Robustness against Process, Voltage and Temperature (PVT) variations
- Minimum power consumption during normal operation
- Isolation between analog and digital parts
- Reduction of cross-coupling between synthesizers working on the same chip
- Improvement in Power Supply Rejection Ratio (PSRR)
- Reduction of ACI to within Frequency Control Commission (FCC) limits

The VCO is an integral part of the PLL-FS. The design of the VCO is strained by the introduction of lower supply voltages in commercially viable submicron technologies. This necessitates innovative circuit techniques and layout methodologies that are resistant

to PVT variations. Fully differential circuits are used for higher PSRR and noise immunity [70]. Rail-to-rail techniques are employed to increase dynamic range and linearity [73].

PLL-FS retains the major market share of the synthesizer industry [3]. However, the DDFS is very promising in the low-frequency range. Clock recovery applications requiring low PN almost exclusively use some variant of the PLL-FS.

2.5 Basic operations in frequency synthesis

Any periodic waveform can be represented as a Fourier Series, i.e. as a sequence of weighted, harmonically related sine waves. Hence, to generate a frequency, existing sine waves can be manipulated. A sine wave can also be re-constructed mathematically from its samples within the constraints imposed by the Nyquist criterion.

The basic operation of frequency synthesis is nothing more than the step-by-step approximation of real numbers [4]. The circuit operations available for frequency synthesis are multiplication [5], division [7], frequency translation (i.e. mixing) [6][8][9] and filtering [11][12][13].

2.5.1 Frequency multiplication

Multiplication of a sine wave $\sin\omega_1 t$ to generate $\sin D\omega_1 t$, in the presence of small spurious signals results in a $20\log D$ (dB) degradation of the spurious levels, where D is the multiplication factor [3]. Multiplication by a large factor must be carefully examined in any FS implementation. This is especially true for the PLL-FS. Frequency multiplication techniques have been described in [5].

2.5.2 Frequency division

Division of a sine wave $\sin D\omega_1 t$ to generate $\sin\omega_1 t$, results in a $20\log D$ (dB) improvement of the spurious levels, where D is the division factor. Division is employed in multi-loop PLL-FS to improve spurious response [3]. For high frequencies, dynamic

prescalars are used, whereas static dividers are used in the low-frequency range. A good discussion on frequency division techniques can be found in [7].

2.5.3 Frequency addition and subtraction: mixing

Whereas a frequency multiplier generates the harmonics of the same signal, a mixer multiplies two sinusoidal signals (usually called RF and LO), along with their spurious contents. When an information signal $x(t)$ modulates the carrier at the RF port, the mixer translates the spectrum of $x(t)$ to the sum and difference frequencies at the IF port. The output spectrum is at frequencies of $RF \pm LO$ as in Equation (2.1). Subsequent filtering is required to choose one of the spectrums.

$$\sin \omega_1 t \sin \omega_2 t = \frac{1}{2} [\cos(\omega_1 - \omega_2)t - \cos(\omega_1 + \omega_2)t] \quad (2.1)$$

Figure 2.1 shows a typical mixing operation in a transceiver. Multiplication in the time domain is convolution in the frequency domain. A clean synthesizer output reduces the intermodulation terms that are difficult, and often impossible, to filter [6].

2.5.4 Frequency filtering

Filters are devices that act in a frequency-selective manner upon the input signal. Principally described and designed in the frequency domain, they are used to suppress, enhance or isolate the frequencies of interest in the incoming signal.

Filters can be passive (RLC type) or active (opamp-based). For IC realizations, there are two major drawbacks associated with passive filters, namely, large chip-area use and lack of control over absolute values of the passive components. Some popular filter architectures are Switched Capacitor (SC), $g_m - C$, and MOSFET-C filters [13]. The ability to tune the performance of a filter during circuit operation is very desirable in any implementation.

$$S_z(f) = S_x(f) \otimes S_y(f)$$

Figure 2.1: An ideal mixing operation in a transceiver

In the context of FS design, filtering is used either to remove unwanted products from a mixing operation, to control the loop-bandwidth of a PLL-FS, or remove the higher-order harmonics at the output of a DDFS.

2.6 Frequency synthesizer performance criteria

The performance criteria are being summarized in Table 2.1. Further details are available in [14][15][16][17].

TABLE 2.1: Frequency synthesizer performance criteria

#	Criterion	Comment	Units
1	Reference standard	Atomic / crystal, mainly characterized by phase noise and long term stability	ppm
2	Phase noise (PN)	Discussed in Section 2.6.1	dBc/Hz

TABLE 2.1: Frequency synthesizer performance criteria

#	Criterion	Comment	Units
3	Frequency range	Dependent on VCO's tuning range	MHz
4	Frequency resolution	Minimum step-size or channel spacing	MHz
5	Switching speed	Time required to settle within specified tolerance of the final frequency	s
6	Discrete spurious content	Periodic components not related to the carrier. Caused by layout inconsistencies and sub-optimum biasing. Harmonics of the carrier are not included in this definition.	dBc/Hz
7	Power consumption	Inversely proportional to battery life and hence to consumer satisfaction	Watts or dBm
8	Output amplitude flatness	Important for RF synthesizers in order to avoid amplitude-to-phase modulation conversion at the IF port [6].	dBm $\pm$ x dB
9	Output impedance	e.g. 50 Ω for RF applications, 75 Ω for video applications	Ω
10	Interface and control	Can be serial or parallel Uses BCD, hex or binary system and is usually computer-controlled.	N.A.
11	EMI compliance	Shielding is required to maintain compliance with FCC standards.	N.A.

2.6.1 Phase noise

Electrical noise present in nature puts an upper limit on the performance of all electronics and communications systems. To put a meaningful specification on the acceptable PN, the basics have to be revisited.

The mean available thermal noise power per Hz of bandwidth from a resistor at a temperature of T (Kelvin) is given as $N = kT$, Watts per Hz, where $k = 1.38 \times 10^{-23}$ Joules / K and is called the Boltzmann's constant. At a nominal room temperature of 17 °C or 290 K, the noise power density per Hz of bandwidth is thus -174 dBm/Hz. This is taken

as the minimum achievable noise floor for any system [14]. Other sources of noise include shot noise that results from the current due to a large number of independent electrons in semiconductor devices and displays a Gaussian power spectral density (PSD). Power-law noise sources, where $\text{PSD} \propto f^n$, are distributed over a wide range of frequencies. The most important contribution is due to flicker noise. Flicker noise ($1/f$ noise) has a Gaussian distribution and is attributed to contact/surface irregularities and changes in the conductivity of the medium [16]. Flicker noise can be reduced by feedback techniques. The typical frequency domain contributions to a noise sideband are shown in Figure 2.2 [15].

Figure 2.2: Characterization of a noise sideband in the frequency domain

An ideal sine wave, if it existed, would show up as a (Dirac) delta function on an ideal spectrum analyzer. In the real world, a signal is subject to long-term and short-term degradations, both in amplitude and phase. The long-term variations are usually attributed to the reference source in the case of an FS (but not for a VCO) and are generally not a concern during equipment lifetime.

The short-term variations (few signal periods or less) can either be random or non-random. Non-random spurs appear due to mixing, intermodulation, substrate effects, clock-feedthrough, bad circuit design, sub-optimum biasing, improper layout, power supply variations or some other unwanted phenomenon. The challenge for a designer is that many of these spurious signals have to be investigated at the performance-evaluation stage

as simulations cannot generally be performed for all scenarios. Using appropriate techniques and experience, these deterministic spurs can either be removed or suppressed to a reasonable level.

The short-term random variations are present in nature and are called PN. The noise voltage is not measurable as such as the test equipment needs to have a better noise floor than the white noise. Hence the PSD profile close to the carrier is examined with a spectrum analyzer. Consider the instantaneous frequency signal in Equation (2.2);

$$S(t) = \{A_1 + n_1(t)\} \cos[\omega_0 t + \theta(t)] \quad (2.2)$$

where A_1 is the constant amplitude and $n_1(t)$ is the amplitude (AM) noise and is negligible in a well-designed oscillator. It will be ignored in order to simplify the following analysis. The waveform has a center frequency ω_0 , and a phase perturbation given by $\theta(t)$. Treating this phase perturbation as a deterministic sinusoidal phase modulation:

$$\theta(t) = \theta_p \sin \omega_m t = \frac{\Delta f}{f_m} \sin \omega_m t \quad (2.3)$$

where θ_p = peak phase deviation or the modulation index. Assuming $\theta_p \ll 1$ and simplifying, we get [15],

$$S(t) = A_1 \left[\cos \omega_0 t - \frac{\theta_p}{2} \{(\omega_0 + \omega_m)t - (\omega_0 - \omega_m)t\} \right] \quad (2.4)$$

The ideal carrier now has sidebands on either side as shown in Figure 2.3 with an amplitude of $20 \log(\theta_p/2)$ [17]. Due to symmetry, only one sideband is normally depicted in PN specifications and is called Single Sideband (SSB) phase noise. Spectrum analyzers (HP8564E) can calculate this PSD in a bandwidth of 1 Hz at a specified offset from the carrier, denoted by $L(f_m) = \theta_{rms}^2 / 2$. The units for PN at an offset f_m from the carrier are dBc/Hz, i.e., y dB down with respect to the carrier.

Figure 2.3: Phase noise profile (exaggerated) for a typical signal (dBc/Hz)

Intuitively, PN in the frequency domain can be thought of as the cycle-to-cycle jitter in the time domain that changes the instantaneous zero-crossings of an otherwise perfectly (and forever repetitive) sinusoidal signal. Figure 2.4 depicts the effect of PN and discrete spurious content in a transmitter.

Figure 2.4: Effect of synthesizer phase noise and spurs in a transmitter

For radar applications, PN specification is important in the 1 to 10 Hz offset range whereas it is typically specified at an offset of 10 kHz to 1 MHz from the carrier in the case of communications systems.

2.7 Frequency synthesis classification

Figure 2.5 depicts the most important techniques [88] in current use that are amenable to monolithic integration. These are briefly described here and details can be found in [15][16][17][18]. A detailed coverage of DDFS is provided in [2][3]. All-digital PLLs and software PLLs are described in [19]. Discussion on optical frequency synthesis techniques using tuned lasers and optical amplifiers is beyond the scope of this thesis document. A brief background on and outlining current trends in optical synthesizers can be found in [76][77]. A brief description of Direct Analog, Direct-Digital, integer-N, fractional-N, Delay-Locked Loop (DLL) and hybrid loop synthesizers appears in Appendix D. The focus will be maintained on the integer-N synthesizer in order to better understand its acquisition performance in Chapter 3.

Figure 2.5: Frequency synthesis classification

2.8 Linearized transfer functions for the integer- N PLL-FS

The concept of PLLs [26] was considered, for decades, to be a control-systems discipline until the dawn of the IC revolution in the late 1960s. The analysis of PLL-FS, therefore, draws heavily on control-systems theory [31][32][33]. The term ‘Phase-Locked Loop’ is a misnomer because PLLs are actually ‘Frequency-Locked’ and ‘Phase-Tracking’ Loops [74]. In order to analyze a PLL-FS, that is predominantly digital in nature, a transfer function (TF) analysis is required. To this end, continuous operation, linearity and time-invariance have to be assumed. Digital PLLs are sampled-data, non-linear and time-varying feedback control systems with a signal-dependent sampling rate [30], so there are limits where TF analysis breaks down. Figure 2.6 is used to derive the open-loop and closed-loop TFs for the non-unity feedback control system.

$$\Theta_i = \mathcal{L}\{\Phi_i(t)\} \quad \Theta_e = \mathcal{L}\{\Phi_e(t)\} \quad \Theta_{out} = \mathcal{L}\{\Phi_{out}(t)\}$$

Figure 2.6: Linearized s-domain representation of a PLL-FS

The PLL-FS operates on excess phase [87]. If there is no phase perturbation at the input, and the system is locked, there will be no phase perturbation at the VCO output and the system will remain locked in steady-state. Hence, a phase-TF, instead of a voltage-TF, is needed to predict the response of the PLL-FS to various wanted and unwanted stimuli. These stimuli can be introduced at any point within the feedback loop.

As a starting point, the phase-TF of all the recognized sub-systems in the PLL-FS can be derived. After that, control-systems theory can be used to write the overall TFs for the non-unity feedback system. The parameter of interest in a PLL-FS, i.e., phase, changes form within the loop. The output of the PFD is a voltage that after low-pass filtering by the LF drives the VCO. The VCO produces an output frequency that is divided by the FBD and the phase thus produced is compared by the PFD to the reference phase to complete the negative feedback loop.

For the voltage at the output of the PFD, in the Laplace notation, we can write,

$$V_{pfd}(s) = K_p \Theta_e \quad (2.5)$$

where K_p is the PFD gain measured in V/rad.

The LF removes the high-frequency components that can modulate the VCO to produce unwanted sidebands. After the Laplace transformation,

$$V_{cont}(s) = F(s) V_{pfd}(s) \quad (2.6)$$

This time-domain DC voltage drives the VCO and produces an output frequency.

$$\omega_{out} = K_{vco} v_{cont} + \omega_{fr} \quad (2.7)$$

where K_{vco} is the VCO gain (rad/s/V). As phase is the time-integral of frequency, we can integrate both sides to obtain a phase-TF for the excess phase of the VCO only.

$$\int \omega_{out} dt = \Phi_{out}(t) = K_{vco} \int v_{cont} dt \quad (2.8)$$

In the Laplace notation, this excess phase [18] can be represented as,

$$\Theta_{out} = \frac{K_{vco}}{s} V_{cont}(s) \quad (2.9)$$

The feedback divider operation in the s-domain is rather simple.

$$\Theta_{out(divider)} = \frac{\Theta_{out}}{N} \quad (2.10)$$

The forward-TF, $G(s)$, can now be written as follows:

$$G(s) = \frac{\Theta_{out}}{\Theta_e} = \left(\frac{V_{pfd}(s)}{\Theta_e} \right) \left(\frac{V_{cont}(s)}{V_{pfd}(s)} \right) \left(\frac{\Theta_{out}}{V_{cont}(s)} \right) = \frac{K_p F(s) K_{vco}}{s} \quad (2.11)$$

The feedback-TF can be written as:

$$H(s) = \frac{\Theta_{divider}}{\Theta_{out}} = \frac{1}{N} \quad (2.12)$$

Using standard control-systems theory, the open-loop TF can be expressed as:

$$G(s)H(s) = G_{OL}(s) = \frac{\Theta_{out}/N}{\Theta_e} = \frac{K_p K_{vco} F(s)}{Ns} \quad (2.13)$$

The PLL crossover is the frequency where the magnitude of the open-loop TF, i.e. $|G(s)H(s)| = 1$. Adequate phase margin (PM) must be available, when the open-loop gain crosses 0 dB to ensure a stable PLL-FS. This PM depends on the LF architecture and the LF component values. By proper system-level design, the loop-bandwidth and the PM can be optimized for a given application.

The closed-loop TF can be mathematically derived as in [27]. It can also be manipulated algebraically to utilize the open-loop TF, as this knowledge is very useful in the design of PLL-FS.

$$\begin{aligned} \frac{\Theta_{out}}{\Theta_i} &= \frac{N \bullet G(s)H(s)}{1 + G(s)H(s)} = \frac{1}{H(s)} \frac{G(s)H(s)}{1 + G(s)H(s)} = \frac{N \bullet G_{OL}(s)}{1 + G_{OL}(s)} \\ \therefore \frac{\Theta_{out}}{N\Theta_i} &= \frac{K_p K_{vco} F(s)}{Ns + K_p K_{vco} F(s)} \end{aligned} \quad (2.14)$$

Finally the error-TF can be defined in terms of the open-loop TF as:

$$\frac{\Theta_e}{\Theta_i} = 1 - \frac{\Theta_{out}}{N\Theta_i} = \frac{1}{1 + G_{OL}(s)} = \frac{Ns}{Ns + K_p K_{vco} F(s)} \quad (2.15)$$

2.8.1 Order/type of phase-locked loops

The ‘order’ of the loop is the highest power of ‘ s ’ in the denominator of the closed-loop TF. The ‘type’ refers to the number of perfect integrators in the loop. Since the VCO acts as a built-in integrator for the phase response, every loop is at least of type-I. The order can be increased by choosing an appropriate LF architecture. If the LF is active, then the opamp provides an integrating action elevating the loop to type-II. Because of industry prevalence, most of the literature explains 3rd-order, type-II loops.

2.8.2 Choices available for a loop-filter

There are several choices available for the loop filter. These can be analog (active or passive), digital (i.e. FIR, IIR), switched-capacitor (SC), $g_m - C$, and MOSFET-C. The cheapest implementations are always monolithic. Wide variations occur in the fabricated values for passive structures as a result of PVT variations. For low-frequency PLL-FS with small currents in the CP, it is the capacitor size that often determines if the implementation is monolithic or external. An external LF requires at least one bond-pad.

Active filters require pre-filtering to avoid opamp saturation due to current spikes originating from a badly designed CP. In addition, more stability problems occur with higher-order filters due to the phase shift introduced at the loop crossover frequency. The noise contribution of opamps is more than those of passive structures with only a single resistor. Adequate performance can be achieved by using a 2nd-order passive external LF resulting in a 3rd-order, CP-based, type-II PLL-FS. Such a PLL-FS along with the loop filter architecture is shown in Figure 2.7.

2.8.3 Transfer functions of the 3rd-order, type-II, PLL-FS

CP-based loops can deliver type-II operation without the existence of opamps in the LF. This is a particular benefit of using a CP. Also when the loop is tracking near equilibrium the duty-cycle is very small and sideband suppression is substantial [28]. For a

given static phase difference, the *UP* and *DN* pulses from the PFD keep advancing the VCO control voltage in the correct direction. Thus the PFD exhibits a pole at the origin or has ‘infinite pull-in range’ limited only by the VCO tuning range. Resistor R_2 in Figure 2.7 provides a zero in the open-loop TF and prevents oscillation. Capacitor C_1 , that is much smaller than C_2 , reduces the ripple as the current is driven into the LF impedance every cycle. This ripple, if not filtered, causes unacceptable jitter at the VCO output. It should be noted that f_{ref} is the frequency at the input of the PFD, and not of the RD.

Figure 2.7: 3rd-order, type-II, CP-based PLL-FS

From Figure 2.7, the loop-filter's TF, $F(s)$, can be written as:

$$F(s) = \left(\frac{1}{sC_2} + R_2 \right) \parallel \left(\frac{1}{sC_1} \right) \quad (2.16)$$

$$F(s) = \frac{sR_2C_2 + 1}{s^2(C_1C_2R_2) + s(C_1 + C_2)} \quad (2.17)$$

Now, we define two time constants: $\tau_2 = R_2 C_2$ corresponding to the zero-frequency and $\tau_1 = R_2 \left(\frac{C_1 C_2}{C_1 + C_2} \right)$ corresponding to the extra-pole frequency because of C_1 . $F(s)$ can now be written in terms of the loop filter's extra-pole and zero frequencies:

$$F(s) = \frac{(1 + s\tau_2)}{sC_1(1 + s\tau_1)} \cdot \frac{\tau_1}{\tau_2} \quad (2.18)$$

By substituting $F(s)$ into Equation (2.13) the open-loop TF can be expressed in terms of the physical loop parameters.

$$G(s)H(s) = \frac{K_p K_{vco}}{Ns^2 \cdot C_1} \left\{ \frac{(1 + s\tau_2)}{(1 + s\tau_1)} \cdot \frac{\tau_1}{\tau_2} \right\} \quad (2.19)$$

Figure 2.8 shows the piece-wise linear Bode plot for the open-loop TF. At low frequencies, a slope of -40 dB/decade is due to the presence of two integrators in the loop, namely the VCO and the CP. Frequencies $1/\tau_1$ and $1/\tau_2$ are chosen to maximize the phase margin. Also, after the extra-pole frequency, the open-loop gain rolls off at rates

Figure 2.8: Piece-wise linear Bode plot for $G(s)H(s)$

higher than -40 dB/decade because of the presence of parasitic poles in monolithic implementations. In order to find ω_c , we have to substitute $s = j\omega$ in Equation (2.19).

$$G(s)H(s)|_{s=j\omega} = \frac{-K_p K_{vco}}{N\omega^2 \bullet C_1} \left\{ \frac{(1 + j\omega \bullet \tau_2)}{(1 + j\omega \bullet \tau_1)} \bullet \frac{\tau_1}{\tau_2} \right\} \quad (2.20)$$

The phase term can now be written as:

$$\phi(\omega) = \text{atan}(\omega \bullet \tau_2) - \text{atan}(\omega \bullet \tau_1) + 180^\circ \quad (2.21)$$

From Figure 2.8, we observe that in order to maximize the loop-PM (ϕ_{max}) it is necessary to find the loop crossover frequency (ω_c) where the slope of the open-loop phase response becomes zero. After differentiating Equation (2.21), we set the result equal to zero:

$$\frac{d\phi(\omega)}{d\omega} = \frac{\tau_2}{1 + (\omega \bullet \tau_2)^2} - \frac{\tau_1}{1 + (\omega \bullet \tau_1)^2} = 0 \quad (2.22)$$

Upon solving Equation (2.22), we get ω_n in terms of τ_1 and τ_2 .

$$\omega_c = \frac{1}{\sqrt{\tau_1 \bullet \tau_2}} \quad (2.23)$$

Loop crossover frequency (ω_c) is the geometric mean of the angular zero-frequency and the angular extra-pole frequency furnished by C_1 . At this frequency, the open-loop TF crosses 0 dB. Hence the loop should be designed so as to maximize the PM at ω_c . By substituting $\phi(\omega_c) \equiv \phi_{max}$ in Equation (2.21) and using Equation (2.23), we get a quadratic equation in τ_1 that can be solved to get τ_1 and τ_2 in terms of system-level parameters ϕ_{max} and ω_c .

$$\phi_{max} = \phi(\omega_c) = \text{atan}\left(\frac{1}{\omega_c \bullet \tau_1}\right) - \text{atan}(\omega_c \bullet \tau_1) + 180^\circ \quad (2.24)$$

Upon solving Equation (2.24), we get τ_1 :

$$\tau_1 = \frac{\sec(\phi_{max}) - \tan(\phi_{max})}{\omega_c} \quad (2.25)$$

and by substituting τ_1 in Equation (2.23), we get τ_2 :

$$\tau_2 = \frac{1}{\omega_c^2 \bullet \tau_1} \quad (2.26)$$

The LF component values, that will deliver ϕ_{max} and ω_c can now be found.

$$C_1 = \frac{K_p K_{vco}}{N \omega_c^2} \bullet \frac{\tau_1}{\tau_2} \left\{ \frac{\sqrt{1 + (\omega_c \tau_2)^2}}{\sqrt{1 + (\omega_c \tau_1)^2}} \right\}$$

$$R2 = \frac{\tau_2}{C_2} \quad (2.27)$$

$$C_2 = C_1 \left(\frac{\tau_2}{\tau_1} - 1 \right)$$

The foregoing treatment in “Transfer functions of the 3rd-order, type-II, PLL-FS” on page 19 has been adopted from [29][30]. The factor 2π has been omitted to simplify calculations and can easily be inserted later. This method is suitable for CAD simulators. To improve the understanding of the PLL-FS acquisition and noise performance, a 2nd-order treatment is sought for the 3rd-order system. The standard control-systems literature [31][32][33] describes 2nd-order systems in great detail.

2.8.4 Second-order representation of a third-order system

Gardner [28] has defined a parameter $b = 1 + \frac{C_2}{C_1}$, that relates the extra-pole frequency contributed by C_1 in terms of the LF zero-frequency.

$$\frac{1}{\tau_1} = b \bullet \frac{1}{\tau_2} \quad (2.28)$$

Gardner analyzes the system stability in continuous-time and in discrete-time and proves that for $b < 9$, the system becomes unstable. A minimum practical value for ensuring stability and treating the 3rd-order system as a 2nd-order system is thus:

$$C_2 \geq 10C_1 \quad (2.29)$$

Even with wide variations in the absolute tolerances of on-chip passive structures, maintaining this relationship is not difficult and is limited only by the maximum on-chip area allowed for C_2 . With the extra-pole frequency at least an order of a magnitude above ω_c , the dynamic performance of a 3rd-order PLL-FS closely resembles that of a 2nd-order system [31][32][33]. The system-level parameters should now be found in terms of the circuit-level parameters.

2.8.5 System-level and circuit parameters for the 2nd-order loop

The TF of the CP-based PFD can be written as follows:

$$V_{cont}(s) = \left(\frac{I_p}{2\pi}\right) \bullet \Theta_e \bullet F(s) \Rightarrow K_p = \frac{I_p}{2\pi} \quad (2.30)$$

where I_p is the CP current averaged over several reference cycles. The implicit assumption is that v_{cont} does not change much during a reference period and hence, the continuous-time analysis is valid. By substituting K_p from Equation (2.30), and a slightly modified expression for $F(s) = R_2 + 1/sC_2$, (i.e. ignoring C_1) the closed-loop TF in Equation (2.14) can be manipulated and compared with the standard response for a 2nd-order control system [31].

$$\frac{\Theta_{out}}{N\Theta_i} = \frac{\left(\frac{I_p}{2\pi}\right)K_{vco}\left(R_2 + \frac{1}{sC_2}\right)}{Ns + \left(\frac{I_p}{2\pi}\right)K_{vco}\left(R_2 + \frac{1}{sC_2}\right)} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (2.31)$$

The system-level parameters can now be described in terms of the circuit-level parameters as in Equation (2.32). This is a key result that will be used throughout the PLL-FS design procedure.

$$\omega_n = \sqrt{\frac{1}{N} \frac{K_{vco} I_p}{2\pi C_2}} \quad \zeta = \frac{\omega_n \tau_2}{2} \quad (2.32)$$

2.8.6 Effect of feedback division ratio on the loop-filter values

From the system point of view, the factor I_p/N appears in both system-level parameters in Equation (2.32). If the factor I_p/N can be kept within a range that would constrain ω_n and ζ within some theoretical and practical limits, then the performance indicators of the PLL-FS like settling, acquisition time and PN performance can also be kept relatively independent of N , over the operating range of the PLL-FS.

Also by defining $K = I_p K_{vco} R_2 / 2\pi N$, some inter-relationships [28] can be written as in Equation (2.33).

$$\begin{aligned} K &= 2\zeta\omega_n & K\tau_2 &= 4\zeta^2 \\ K/\tau_2 &= \omega_n^2 & \tau_2 &= 2\zeta/\omega_n \end{aligned} \quad (2.33)$$

The VCO gain, K_{vco} , changes with PVT variations and is, in general, not easily controllable without digital techniques [35]. The minimum ω_n is limited by the maximum size of C_2 that can be integrated, lowest realizable I_p and the worst-case acquisition time specified. With an external LF, C_2 cannot be easily switched from one value to another as it would require at least two control signals (increment and decrement). This, in turn, would increase bond-pad area on the chip and external circuitry on the PCB. It would also increase layout and floorplanning difficulty as the PLL-FS is usually embedded in a complex mixed-signal chip. Hence, I_p is the only physical parameter that can be easily employed to control variation in system-level parameters (ω_n and ζ) with a changing

feedback division ratio N . Acceptable theoretical and practical ranges for ω_n and ζ are described next.

2.8.7 Acceptable range for the damping coefficient

The open-loop gain for the 2nd-order system, in terms of the system-level parameters, can be derived from the closed-loop TF [30]. Therefore,

$$G_{OL}(s) = \frac{(\Theta_{out}/N\Theta_i)}{1 - (\Theta_{out}/N\Theta_i)} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2} \quad (2.34)$$

$$\frac{\Theta_{out}}{N\Theta_i} = \frac{G_{OL}(s)}{1 + G_{OL}(s)} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (2.35)$$

Equation (2.34) can be solved [30], to get the open-loop gain and PM as a function of ζ .

$$|G(s)H(s)| = \frac{\sqrt{1 + 4\zeta^2(\omega/\omega_n)^2}}{(\omega/\omega_n)^2}$$

$$\angle\{G(s)H(s)\} = \text{atan}(2\zeta\omega/\omega_n) - 180^\circ$$

$$\phi = \text{atan}\left(2\zeta\sqrt{2\zeta^2 + \sqrt{4\zeta^4 + 1}}\right) \quad (2.36)$$

Hence, if ζ is between 0.5 and 2, the PM is between 51.8° and 85.8° respectively, as shown in Figure 2.9. It should be pointed out that the phase shift contributed by C_1 at ω_c , and time-delays through the PLL-FS would further degrade this PM. Since a practical minimum PM is considered to be 45°, $\zeta_{min} = 0.5$ and $\zeta_{max} = 2.0$ should only be extended after further analysis. As a rule of thumb, $\zeta = 0.9$ represents a practical compromise for optimum noise and settling performance, for a 3rd-order, type-II, CP-based PLL-FS.

Figure 2.9: Relationship between ζ and phase margin

2.8.8 Acceptable range for ω_n as a fraction of f_{ref}

The PFD is usually preceded by an RD, as shown in Figure 2.7, that divides the f_{xtal} to the channel spacing or f_{ref} . The hertzian loop-bandwidth is ideally set at $f_{ref}/100$ and up to a maximum of $f_{ref}/10$ for adequate sideband suppression, the requirement for which is application-dependent [30]. The continuous-time assumption does not hold for larger loop-bandwidths and a discrete-time, z-domain analysis is required. Originally presented by Gardner [28], and improved by Jeong [34] to include the time-delays through the PLL-FS, the stability of a 2nd-order PLL-FS can be summarized as in Inequality (2.37):

$$K\tau_2 \leq \frac{1}{\frac{\pi}{\omega_{ref}\tau_2} \left(1 + \frac{\pi}{\omega_{ref}\tau_2} - \frac{t_d}{\tau_2} \right)} \quad (2.37)$$

where t_d is the time-delay through the PLL-FS. The factor t_d/τ_2 can be ignored if

$$t_d \ll 0.1\tau_2 \quad (2.38)$$

This requires a large enough value for C_2 . For submicron technologies, the typical delays are very small (typically, a few ns) and are usually insignificant.

By making use of the identities presented in Equation (2.33) and setting $t_d = 0$, we can rearrange Inequality (2.37) to get Inequality (2.39) in terms of (ω_{ref}/ω_n) .

$$K\tau_2 \leq \frac{(\omega_{ref}\tau_2)^2}{\pi(\pi + \omega_{ref}\tau_2)} \Rightarrow 4\zeta^2 \leq \frac{(\omega_{ref}/\omega_n)^2(4\zeta^2)}{\pi\{\pi + 2\zeta(\omega_{ref}/\omega_n)\}} \quad (2.39)$$

$$\therefore (\omega_{ref}/\omega_n)^2 - 2\zeta\pi(\omega_{ref}/\omega_n) - \pi^2 \geq 0$$

$$\therefore \left(\frac{\omega_{ref}}{\omega_n}\right) > \frac{\pi}{2}(\zeta + \sqrt{\zeta^2 + 1}) \quad (2.40)$$

Inequality (2.40) (a little different from the one presented in [50]) sets the ratio between ω_{ref} and ω_n , with ζ as parameter, in order to maintain stable PLL-FS operation. To allow for degradation due to the extra pole and other parasitic poles, $(\omega_{ref}/\omega_n) \approx 10$ is taken as a minimum practical value that guarantees stability. For better reduction in sidebands a practical value is $(\omega_{ref}/\omega_n) \approx 20$.

2.8.9 Acceptable range for loop-filter resistor, R_2

The resistor R_2 has to be carefully chosen as it affects many PLL-FS parameters. It is the component in the LF that generates the dominant thermal noise and larger values should thus be avoided, whenever possible. As I_p goes in and out of the LF, it develops an instantaneous voltage $I_p R_2$. This generates, to a first order, frequency excursions on the VCO given by $\Delta\omega_{out} = K_{vco} I_p \theta_e / C_2$. Hence a larger R_2 will result in larger VCO sidebands. Also, the CP leakage current flows through R_2 generating more unpredictable VCO sidebands. Inequality (2.39) can be rearranged to yield Inequality (2.41).

$$\omega_n^2 < \frac{\omega_{ref}^2}{\pi(\pi + \omega_{ref} R_2 C_2)} \quad (2.41)$$

Inequality (2.41) traces a hyperbolic curve [34], where a very small value of R_2 can throw the system into instability due to poor PM. At the same time, it puts an upper

bound on the value of R_2 , as it cannot be increased indefinitely because of the ensuing stability problems and a degradation of acquisition time as a result of a very small loop-bandwidth. A typical range for R_2 can be from 10 k Ω to 40 k Ω , depending on the choice of f_{ref} , the loop-bandwidth and the maximum realizable value of C_2 .

2.8.10 Noise performance and noise transfer functions

Noise can be introduced as a phase disturbance at many points in the loop as shown in Figure 2.10.

Figure 2.10: Linear model of a PLL-FS with noise inputs

A comprehensive chart has been presented in [37] that shows the noise-TFs from various points in the loop to the output. The PLL-FS noise performance can be optimized if the total noise contribution from the PLL-FS components to the output is known.

Rewriting the closed-loop TF for convenience;

$$\frac{\Theta_{out}}{\Theta_i} = \frac{K_p K_{vco} F(s)}{Ns + K_p K_{vco} F(s)} = \frac{N \cdot G_{OL}(s)}{1 + G_{OL}(s)} \quad (2.42)$$

Let the other TFs be denoted by $P_j(s)$ so that by using Mason's rule [31], we get:

$$P_1(s) = \frac{\Theta_{out}}{\Theta_{PFD}} = F(s) \frac{K_{vco}}{s} \left(\frac{1}{1 + G_{OL}(s)} \right) \quad (2.43)$$

$$P_2(s) = \frac{\Theta_{out}}{\Theta_{LF}} = \frac{K_{vco}}{s} \left(\frac{1}{1 + G_{OL}(s)} \right) \quad (2.44)$$

$$P_3(s) = \frac{\Theta_{out}}{\Theta_{VCO}} = \frac{1}{1 + G_{OL}(s)} \quad (2.45)$$

Figure 2.11 shows the various noise-TFs for a typical PLL-FS.

Figure 2.11: Noise transfer functions of a PLL-FS

Equation (2.42) and Equation (2.43) show that any noise from the input crystal source and the CP-based PFD is low-pass filtered. The noise from the crystal oscillator is usually not a concern in PLL-FS design but causes a $20\log N$ (dB) degradation with large FBD ratios. Another source is the static phase offset contributed by the CP leakage currents. This can be kept low using good PFD and CP design techniques. Noise contributions from the RD and the FBD are also included as they appear at the PFD input.

Figure 2.11 shows that increasing K_p can also lower this noise contribution from the PFD and the dividers. This can be achieved by increasing I_p at the cost of increased power dissipation.

Equation (2.44) shows that LF noise is shaped by a bandpass noise-TF, before it reaches the output. The noise introduced by the VCO biasing circuitry can also be referred here. Reduction in K_{vco} minimizes this noise contribution.

Having the same form as the error-TF of the loop, Equation (2.45) shows that any phase contributed by the noise present at the output of the VCO is high-pass filtered. This includes the noise generated by the VCO itself or produced because of substrate and power supply coupling issues. Hence a wider loop-bandwidth would improve the performance of the synthesizer [100]. Fortunately, the noise contribution from the crystal oscillator is exceptionally low and even with low-pass filtering and multiplication by N , does not pose a major design problem. The only disadvantage is that the loop-bandwidth cannot be indefinitely increased and is limited by $(\omega_{ref}/\omega_n) \approx 10$ as shown earlier. Reducing K_{vco} also lowers the sensitivity of the VCO to the noise at its control input, but after ω_n is set, further reduction in K_{vco} should be compensated by an increase in K_p or R_2 to maintain the same loop-bandwidth. Hence, if multiple or programmable VCOs are employed for reduction in K_{vco} , then digital techniques provide a flexible solution to keep the loop-gain constant [35].

A formula for the optimal loop bandwidth is proposed in [39] and relates the external rms jitter, VCO rms jitter and the reference frequency as shown in Equation (2.46).

$$W_{opt} = \frac{1}{NT} \left(\frac{\delta\tau_{1rms}}{\delta\tau_{2rms}} \right) \quad (2.46)$$

where W_{opt} is the optimal PLL bandwidth, $\delta\tau_{1rms}$ is the rms jitter of the internal VCO phase, $\delta\tau_{2rms}$ is the rms jitter of the external input reference, N is the feedback division ratio and $T = 1/f_{ref}$.

2.8.11 Dynamic loop-response

The input signals that are applied or can appear at the inputs of the PLL-FS are the phase-step, the frequency-step and the frequency-ramp. These are mathematically inter-related and are depicted in Figure 2.12 in terms of phase inputs.

Figure 2.12: Common phase disturbances at PLL-FS input

The steady-state error can be found by applying the final-value theorem on the error-TF. The error-TF can be inferred from Equation (2.15) and Equation (2.31).

$$\lim_{t \rightarrow \infty} \Phi_e(t) = \lim_{s \rightarrow 0} s \left(\frac{\Theta_e}{\Theta_i} \right) \Theta_i = \lim_{s \rightarrow 0} s \left(\frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \right) \cdot \Theta_i$$

For a phase-step:
$$\lim_{t \rightarrow \infty} \Phi_e(t) = \lim_{s \rightarrow 0} \left(\frac{s^3}{s^2 + 2\zeta\omega_n s + \omega_n^2} \right) \cdot \frac{\Delta\phi}{s} = 0$$

For a frequency-step:
$$\lim_{t \rightarrow \infty} \Phi_e(t) = \lim_{s \rightarrow 0} \left(\frac{s^3}{s^2 + 2\zeta\omega_n s + \omega_n^2} \right) \cdot \frac{\Delta\omega}{s^2} = 0$$

For a frequency-ramp:
$$\lim_{t \rightarrow \infty} \Phi_e(t) = \lim_{s \rightarrow 0} \left(\frac{s^3}{s^2 + 2\zeta\omega_n s + \omega_n^2} \right) \cdot \frac{\Delta\Omega}{s^3} = \frac{\Delta\Omega}{\omega_n^2}$$

Being a type-II system, the CP-based PLL-FS tracks the phase-step and frequency-step with zero final phase-error [31][32][33]. It has been shown [36] that, for a 3rd-order loop, the angular frequency variation at the PLL-FS input should have a slope less than $[(b-1)/b]\omega_n^2$ if the loop is to remain locked, where b is the ratio between τ_1 and τ_2 as in Equation (2.28).

A frequency-ramp occurs during acquisition or as a test-signal and is seldom unintended in a PLL-FS. It may be generated by a planned sequence of missing pulses in the f_{ref} signal or by changing N continuously so that a PLL-FS is not able to achieve phase-lock. A phase-step is used to analyze noise and power-supply induced phase disturbances, while the PLL-FS is operating in phase-lock. A Butterworth-settling results with $\zeta = 0.707$ for a 2nd-order system. Frequency-step performance is discussed in Chapter 3.

2.9 Publications on CMOS PLL-based synthesizers

Frequency synthesis is an area of active research but a simple comparison between two synthesizers is difficult. The choice of technology, loop architecture, power dissipation, frequency range and phase noise performance are some of the parameters of interest. Table 2.2 lists the frequently quoted performance-metrics of some CMOS PLL-based synthesizers published since 1993. Further, it highlights the focal point of the particular research.

TABLE 2.2: Survey of CMOS PLL-based synthesizers

Reference/ Year	Min. feature size (μm) / Supply voltage (V)	Power dissipation (mW) / Die area (mm^2)	Frequency range (Hz) / VCO type / Phase noise dBc/Hz or p-p jitter (ps)	Application	Focus of the research
[106] / 1993	0.8 μm / 5 V	200 mW / 4.05 mm * 4.05 mm	20 MHz - 40 MHz / Variable- delay line 23 taps / 2.2 ns delay res- olution	Video process- ing	High Stability clock generation +/- 100 ppm

TABLE 2.2: Survey of CMOS PLL-based synthesizers

Reference/ Year	Min. feature size (μm) / Supply voltage (V)	Power dissipation (mW) / Die area (mm^2)	Frequency range (Hz) / VCO type / Phase noise dBc/Hz or p-p jitter (ps)	Application	Focus of the research
[107] / 1993	0.25 μm / 2.5 V	< 100 mW / 1.9 mm * 1.1 mm	75 MHz - 370 MHz / 3-stage differential ring / jitter specs N.A.	CD-ROM, DVD-ROM, A/V applica- tions	Consumer IC, wide locking range, low lock- ing time,
[108] / 1993	0.8 μm / 2.5 - 7 V	N.A. / N.A.	0.3 MHz - 165 MHz / 3-stage ring oscillator / 81 ps pk-pk	Microproces- sors, PC, workstations,	Flexible wide voltage range architecture suited for PCs.
[73] / 1995	0.5 μm / 1.5 - 3 V	25.5 mW @ 622 MHz / N.A.	250 MHz - 640 MHz / Differen- tial ring oscilla- tor / 40 ps pk-pk	Clock genera- tor for multi- media applications	Pre-charge type PFD, 1 GHz oper- ation, rail-to-rail VCO
[109] / 1996	0.5 μm / 3.3 V	9.9 mW / 0.6 mm * 1.3 mm	28 MHz - 380 MHz / source follower VCO / 80 ps pk-pk	Video chip / high-speed data transfer/ (with 600 k transistors)	Noise immunity of 1.0 V pk-to-pk at power rails
[110] / 1996	0.35 μm / 3.3 V	42 mW@ 500 MHz / 1.51 mm * 1.56 mm	110 MHz - 850 MHz / current controlled oscil- lator / 42 ps rms @ 500 MHz	Integration with noisy dig- ital systems	Noise insensitive PLL with a volt- age regulator
[113] / 1996	0.35 μm / 1.0 - 2.2 V	1.2 mW @ 320 MHz / 0.21 mm * 0.21 mm	176 MHz -574 MHz / ring oscil- lator / 150 ps pk- pk rms	2.2 million transistor microproces- sor	Monolithic, low- jitter, and settling time < 60 μs
[102] / 1997	0.18 μm / 0.5 -1.8 V	< 2 mW / 0.48 mm * 0.45 mm	40 MHz -170 MHz / Delay- line/less than 200 ps rms	Multimedia and portable applications	Low-voltage, low- power, novel adaptive-gain VCO
[112] / 1998	0.4 μm / 3.0 V	51 mW / 1.7 mm * 1.9 mm	1800 MHz / LC oscillator / -123 dBc/Hz @ 600 kHz	DCS1800	Monolithic, lin- earized VCO with dual-path loop fil- ter

TABLE 2.2: Survey of CMOS PLL-based synthesizers

Reference/ Year	Min. feature size (μm) / Supply voltage (V)	Power dissipation (mW) / Die area (mm^2)	Frequency range (Hz) / VCO type / Phase noise dBc/Hz or p-p jitter (ps)	Application	Focus of the research
[111] / 1999	0.35 μm / 3.3 V	15 mW / N.A.	896 MHz - 902 MHz / current controlled oscil- lator / -90 dBc/ Hz @ 12.5 kHz	Wireless	Comparison of architectures
[95] / 2000	0.35 μm / 3.3 V	120 mW / 40 mm * 2 mm	435 MHz - 485 MHz / differen- tial ring oscilla- tor / -99 dBc/Hz @100kHz	Clock genera- tor	Fast acquisiton using a Discrimi- nator-Aided Phase Detector (called DAPD)
[100] / 2000	0.35 μm / 3.3V	84.0 mW / 2.2 mm * 1.8 mm	1.38 GHz -1.55 GHz / LC oscil- lator/ -116 dBc/ Hz @ 100 kHz	Multi-stan- dard LO gener- ation for wireless	Wideband PLL architecture to uti- lize low-Q on- chip components
[101] / 2000	0.13 μm / 1.0 -1.8 V	3.9 mW / 0.6 mm * 0.4 mm	1.25 GHz - 2.85 GHz / ring oscil- lator/ p-p 45.8 ps @ 1.0 GHz	Wireless	Low-voltage, low- jitter, novel CP
[103] / 2001	0.5 μm / 3.3V	26 mW / 0.9 mm * 1.8 mm	400 MHz - 485 MHz / Differen- tial Ring Oscilla- tor / -109 dBc/Hz @ 600 kHz	Clock genera- tor for multi- media, microproces- sors	Monolithic, fast- locking, same as [95][46], acquisi- tion time = 260 μs
[104] / 2001	0.25 μm / 2.5 V	55 mW / 1.2 mm * 1.7 mm	2.4 GHz / LC / -133 dBc/Hz @ 3 MHz	Bluetooth™	Monolithic, direct modulation , multi-modulus divider
[96] / 2002	0.35 μm / 3.0 V	60 mW / 2.5 mm * 2.0 mm	0.86 GHz -1.1 GHz, 1.55 GHz - 1.98 GHz / LC / - 104 dBc/Hz @ 100 kHz	PCS, CDMA, cellular	Fully integrated, dual-band, frac- tional-N for wire- less applications

TABLE 2.2: Survey of CMOS PLL-based synthesizers

Reference/ Year	Min. feature size (μm) / Supply voltage (V)	Power dissipation (mW) / Die area (mm^2)	Frequency range (Hz) / VCO type / Phase noise dBc/Hz or p-p jitter (ps)	Application	Focus of the research
[97] / 2002	0.35 μm / 3.3 V	100 mW / N.A.	2.4 GHz - 2.5 GHz / LC / -82 dBc/Hz @ 10 kHz	Industry, Sci- entific and Medicine (ISM)	Hybrid loop, frac- tional-N, LC Oscillator
[98] / 2002	0.35 μm / 3.3 V	109 mW / 1 mm * 1 mm	0.88 GHz - 1.64 GHz / ring / rms 80 ps pk-pk	Wireless	Multi-phase ring oscillator, mono- lithic
[99] / 2002	0.18 μm / 1.8 V	10 mW / N.A.	4.9 GHz - 5.3 GHz / ring oscil- lator/ -121.9 dBc/ Hz @ 10 MHz	Wireless LAN, research	Novel CP to remove ripple on VCO control volt- age, integer-N
[75] / 2002	0.35 μm / 1.8 V	4.59 mW / 0.4 mm * 0.4 mm	103 MHz -1.02 GHz / ring osc/ 110 ps pk-pk @ 33 MHz	Clock genera- tor	Programmable wide-range ring oscillator, novel PFD
[105] / 2002	0.25 μm / 3.3 V	30 mW / N. A.	5.17 GHz - 5.33 GHz / LC tank / -120 dBc/Hz @ 1 MHz	Wireless LAN	Lock time = 3 μs
THIS WORK / 2002	0.25 μm TSMC / 2.5 V	10 mW @ 200 MHz/ active area 1.2 mm * 1.2 mm	50 MHz - 280 MHz / 5-stage ring oscillator / -92 dBc/Hz @ 100 kHz	See Table 3.1	Lock time < 140 μs , novel PFD, novel acquisition technique, and a rail-to-rail VCO

The major conclusion that can be drawn from this chronological literature survey is that the reduction of supply voltages due to the reduction in minimum feature sizes has resulted in more area-efficient and power-conscious systems. After 1998, the majority of PLL-FS applications described in the literature focus on wireless applications. For the successful integration of a PLL-FS with a large digital chip, some form of noise immunity is also desired that goes beyond the simple use of differential logic and utilizes an on-chip voltage regulation mechanism for the critical power supplies.

2.10 Summary

This chapter started with a brief discussion about the evolution and present-day challenges in frequency synthesis. Basic operations required to generate frequencies and the performance criteria necessary to establish a common reference for all frequency synthesis techniques were mentioned. A brief account of some popular frequency synthesis techniques can be found in Appendix D. The background theory relevant to an integer-N, CP-based PLL-FS was presented. This theory forms the basis for the PLL-FS system design in Chapter 3 and for the PLL-FS component design in Chapter 4. A survey of CMOS PLL-based frequency synthesizers was presented from the literature. The applications have emerged and evolved to range from low-frequency consumer products to high-frequency wireless Local Area Networks (LAN).

3.1 Chapter overview

This chapter provides a list of potential applications as well as the specifications for the target system. This is followed by a discussion on PLL-FS acquisition and a survey of relevant literature. The design procedure for a novel PFD is then presented. Various components of the total acquisition time are analyzed using control theory and PLL theory to arrive at a methodology for reducing the acquisition time. An example design of the target PLL-FS is shown using hand calculations. This PLL-FS design is later verified and optimized using a behavioral simulator. This is followed by a comparison of time-domain simulation results from various acquisition techniques.

3.2 Fabrication technology and FS architecture

This work has been done in CMOSP25 technology. If the frequency synthesizer is to be embedded within a large digital chip, then the low-noise DAC required by the fractional-N technique and the significant amount of digital circuitry present in the DDFS render the use of these architectures costly. The PLL-FS architecture shown in Figure 3.1 is chosen because of its simplicity. The general-purpose nature of the chip requires an external LF. A clean analog supply is available for the target system, so a voltage regulator is not shown in this work.

3.3 Intended applications

Table 3.1 summarizes some commercially used frequencies [23][24][25].

TABLE 3.1: Potential low-frequency applications of the PLL-FS

Frequencies (MHz)	Purpose
17.7345, 28.6364, 35.4689	PAL/NTSC television clock sources
74.25, 74.175824	High-Definition Television (HDTV) (1125/60) timebase
48 / 24.576	Intel Graphics™, audio/video
25, 50, 100, 125	Ethernet applications
40 - 167	Video Graphics Array (VGA); modes 1-40
108, 54, 27	TVOUT™ clocks
24.576	Dolby™ AC-3 clock, 48 kHz * 512
25, 50 ... upto 175	Various memory clocks for computers

3.4 Target specifications

Table 3.2 summarizes the target specifications for the clock generator.

TABLE 3.2: Target specifications

Specification	Maximum value	Comments
Technology	0.25 μm , 2.5 V $\pm 10\%$	TSMC 1-poly-5-metal, CMOS process
Short-term jitter	150 ps	No deadzone in the PFD
Frequency range	10 MHz - 200 MHz	As specified in Table 3.1
Power dissipation	< 20 mW @ 200 MHz	< 500 μW in power-down mode
Acquisition time	< 200 μs	Acquisition-aiding circuitry is required
Crystal frequency	14.318 MHz	Variable f_{ref} , minimum $f_{ref} = 2.0$ MHz

the loop component characteristics and the PVT variations. In the absence of an analytical solution, simulations are the only practical alternative [57].

3.6.1 Definitions of important terms

The ‘pull-in’ range is the maximum initial frequency offset, where the PLL-FS will eventually acquire lock but with cycle-slips. The lock-range (locking-range or the ‘lock-in’ range) is the maximum initial frequency offset over which the PLL-FS attains phase-lock without cycle-slips. The ‘hold-in’ range is the maximum range over which the loop operates but if the frequency is slowly changed past this limit, it is thrown out of lock. The foregoing definitions have been adopted from the literature [18][19].

3.6.2 Pull-in range for the CP-based PLL-FS

The CP-based PLL-FS has an infinite pull-in range, practically limited by the VCO tuning range. This means that the CP-based PFD advances the VCO in the correct direction until the frequency acquisition is complete following which a settling and consequently a locking process ensues.

3.6.3 Hold-in range for the CP-based PLL-FS

For a PLL-FS operating in a phase-locked condition, the incoming signal f_{ref} is usually very stable and does not exhibit significant long-term drifts. Thus, the hold-in range is never exceeded under normal operating conditions. If f_{ref} is varied however, then the loop remains locked as long as the rate of change of the angular output frequency does not exceed $[(b-1)/b]\omega_n^2$ as described in Section 2.8.11 where $b = \tau_2/\tau_1$.

3.6.4 Lock-range for the CP-based PLL-FS

Equation (3.1) describes the lock-range as given in [79]:

$$\omega_L = \omega_n \sqrt{4\pi^3} = 11.13\omega_n \quad (3.1)$$

Another version [19] of the lock-range is described in Equation (3.2).

$$\omega_L = 4\pi\zeta\omega_n \quad (3.2)$$

The lock-range changes from $6.28\omega_n$ to $12.56\omega_n$ as ζ changes from 0.5 to 1. For hand calculations, we can assume $\omega_L \approx 10\omega_n$.

3.6.5 Pull-in time

Different books propose different formulas for the pull-in time and usually with different notation [19][84]. The intuitive treatment in [79] is corrected and used here.

$$Q = C_2\Delta V_{cont} = I_{avg}T_p \text{ where } I_{avg} = I_p/2$$

$$\Delta V_{cont} = \frac{\Delta\omega - \omega_L}{K_{vco}} \Rightarrow T_p = \frac{\Delta\omega - \omega_L}{\pi N \omega_n^2} \quad (3.3)$$

where Q is the charge on C_2 , ΔV_{cont} is the voltage change across C_2 required for frequency acquisition, T_p is the pull-in time, $\Delta\omega$ is the initial angular frequency offset, ω_L is the lock-range and ω_n is the loop-bandwidth. This assumes a small resistor R_2 in the LF and an average duty-cycle of 50% for the PFD outputs [79].

3.6.6 Lock-time

The lock-time, T_L , is described by Equation (3.4) [79][19].

$$T_L \approx \frac{2\pi}{\omega_n} = \frac{1}{f_n} \quad (3.4)$$

3.6.7 Total acquisition time

The total acquisition time, T_{acq} , depends on the system-level parameters ω_n and ζ . It also depends on N , because the system-level parameters vary as $1/\sqrt{N}$. It is composed of the three distinct phenomena; the pull-in time, the settling-time and the lock-

time. From the control-systems perspective, the settling-time includes the pull-in time. This is discussed later in conjunction with Figure 3.18 to avoid repetition.

3.7 Survey of relevant publications on acquisition time

Unaided acquisition can be slow for linear PLLs that employ only a phase detection mechanism. On the other hand, a PFD can speed up the acquisition as it has an inherent frequency acquisition capability. Since the inception of PLLs, various techniques have been used to aid the acquisition process. Most of these techniques change the LF components to achieve a wider loop-bandwidth that accelerates the frequency acquisition. Some techniques use memory and digital circuits to aid the acquisition. A summary of the significant acquisition-aiding architectures from the literature is presented here.

- It has been shown that the acquisition time of a 2nd-order loop can be reduced by an order of magnitude if the LF zero resistor is bypassed with two anti-parallel diodes. This is applicable for initial frequency offsets much larger than ω_n [40].
- An ‘Accumulative’ PFD has been described that extends the phase comparison range beyond $\pm 2\pi$, by using 4-bit up/down counters and a low-noise DAC to drive the VCO [78].
- Use of dual detectors providing CP updates at leading as well as trailing edges of the reference signal has been reported. A duty-cycle limitation of 50% is present since the outputs of the two PFDs have been combined using simple AND/OR logic and the detectors have different edge-sensitivities as described later [47].
- Using digital logic, the current count in the FBD can be subtracted from the previous count exactly one reference cycle ago. If the difference is zero or some small number, then the frequency acquisition is deemed complete. The PFD and dividers can be reset so that the phase of the PLL-FS is initialized. This suppresses ringing and improves acquisition time [41][42].

- Storage of the VCO characteristics using a RAM/ROM and consequently switching to a voltage that corresponds closely to the required frequency using a DAC, so that only a phase lock-in is necessary [37], can result in a shorter acquisition time.
- The use of fractional-N techniques employing sigma-delta modulation [22] as well as the use of hybrid-loops with DDFS techniques [17] has been reported.
- Tuning the bandwidth of an ‘adaptive LF’ by adjusting the transconductance of an Operational Transconductance Amplifier (OTA) can reduce the acquisition time by a factor of 9 [43].
- A non-linear PFD beyond phase differences of $\pm\pi$ has been reported. A duty-cycle of 50% is required for PFD inputs [79]. Almost the same principle has been described [95] in conjunction with a change in the LF parameters, but the phase detection range is determined by delay elements.
- A commercial patented method, that is now dominant, was introduced in the early 1990s by Philips Semiconductors (e.g. SA7025 GSM band synthesizer). This uses a fractional-N PLL with dual CPs and digital circuitry to maintain the PM as loop-bandwidth is doubled during acquisition [44].
- Almost similar in implementation is the National Semiconductor’s (e.g. LMX233x) FastLock™ patented scheme implemented in a BiCMOS proprietary technology [46]. It employs circuitry to quadruple the CP current and halves the LF zero-resistor to maintain PM [29][45][46]. This architecture is used in this work as a demonstration, in order to establish its feasibility for a submicron CMOS technology.

3.8 *Proposed new PFD/acquisition-aiding mechanism*

A novel PFD and a simple acquisition-aiding method are presented in this chapter. The key references for the new PFD architecture are [47][79] and those for the acquisi-

tion-aiding method are [41][42]. The proposed APFD architecture has the following advantages:

- It alleviates the PFD input duty-cycle limitation of 50% as in [47][79].
- It produces a DC output (i.e. 100% duty-cycle) for large phase and frequency differences as opposed to a 50% duty-cycle output from a conventional PFD. Hence, the total acquisition time can be reduced for large initial frequency differences.
- The normal operation (phase differences $< \pm 2\pi$) is similar to a conventional PFD, so no additional stability analysis is required as in [79].
- A conventional CP-based PFD has a feedthrough component at f_{ref} that is filtered by the LF. In the newly proposed PFD, this feedthrough can (optionally) be moved to $2f_{ref}$, if the power-budget allows. The feedthrough component at a higher frequency can be filtered more effectively using the same external LF, resulting in further reduction of the VCO sidebands. For a monolithic LF, the absolute variation of the passive components can be accommodated more easily.

The new acquisition-aiding methodology is described later in Chapter 3.

3.9 Phase and frequency detectors

A phase detector is present in every PLL. A PFD, however, imparts an enhanced frequency acquisition capability to the PLL. These phase and frequency detection mechanisms have been widely researched (Refs. in [17][18]) and are mainly characterized according to their phase detection range, maximum operating frequency, output harmonics, power dissipation, duty-cycle dependence and frequency detection capability. The dual D-flipflop PFD and a quad D-flipflop variant for improved frequency acquisition were first proposed by Sharpe [48]. The majority of industrial designs use some variant of the quad D-flipflop PFD. The edge-triggered operation makes its output signals indepen-

dent of the duty-cycle of the inputs [18]. The simplified state diagram [18] for a PFD is shown in Figure 3.2.

Let us assume that the PFD has to output UP and DN signals that drive the CP in the correct direction in Figure 3.1. In general, if $f_{div} > f_{ref}$, then we get more transitions on the f_{div} compared to f_{ref} during any reference period. The state-diagram suggests that the PFD would go to STATE-I and stay there until this is the case. The DN signal is active-high and turns on an NMOS switch in the CP, thereby extracting charge out of C_2 while the PMOS switch remains disabled. This brings v_{cont} down to the required level. A similar sequence of events happens if $f_{div} < f_{ref}$, in which case the active-low UP signal turns on the PMOS switch in the CP and charges C_2 to the required voltage. The NMOS switch remains disabled in this case. STATE-I represents the discharging and STATE-II represents the charging up of C_2 .

Figure 3.2: Simplified PFD state-diagram

The architectural/schematic overview of the two frequently used PFDs is shown in Appendix C (see Figure C.1 and Figure C.3). A power-down (PD) input is provided in each so that it doubles as the reset input. A reset and/or the PD signal would force the PFD outputs in the unasserted state thereby disabling the CP, except for a small leakage current. The NAND version [51] is negative edge-triggered and the NOR version [49][50] is posi-

tive edge-triggered. Hereinafter, the NOR implementation is referred to as the PFD-NOR and the NAND implementation is called the PFD-NAND to avoid confusion.

The RESET circuitry shown in the two PFD implementations uses a four-input NAND (or NOR) gate, whose inputs connect to the outputs of the four latches. To avoid the deadzone problem, a delay can be provided in both the detectors in the RESET branch. This ensures that a minimum-width pulse is available to turn on the switches in the CP completely for the smallest phase difference between the PFD inputs [18]. Otherwise, the VCO would drift until there is significant phase difference before the PFD produces correction pulses that are wide enough to turn on the CP switches. Over a long period of time, the VCO will be modulated by a sub-harmonic of f_{ref} . Since this might very well be within the loop-bandwidth, it cannot be attenuated and will cause significant sidebands at the VCO output. It is an undesirable situation called the ‘backlash’ effect in PLL-FS. The delay inserted to counter this effect is called the ‘anti-backlash pulse-width’ [51].

The global delays through the buffers at the output of the PFDs are optimized to make sure that the *UP* and *DN* signal transitions are fast and aligned. The current spikes can thus be prevented in the CP. The design of each PFD is optimized in conjunction with the CP. An obvious solution seems to be the addition of a transmission gate in the buffer chain to equalize the signal delays. But upon simulation, the very narrow PFD output pulses are visibly distorted by the impedance of the transmission gates. Hence, the use of transmission gates to equalize the global delays is not feasible. In this work, the buffers are considered functionally separate from the PFD, although they are shown together for convenience.

In the literature, the use of dual phase detectors has been proposed [53]. The technique utilizes a ‘Multiplying Phase Detector’ and a standard PFD-NOR type implementation. This increases the acquisition range and injects lower noise during regular data-recovery operation when the ‘Multiplying Phase Detector’ is used alone. Circuit complex-

ity remains a disadvantage although the final outcome is desirable. Another example of a dual-PFD that is a combination of PFD-NAND and PFD-NOR, has been presented but the frequency acquisition and duty-cycle limitations have not been discussed [47].

In this work, an APFD that is a combination of a PFD-NAND and a PFD-NOR is presented with the design methodology for the logic circuitry that can alleviate the duty-cycle limitation as in [47], enhance frequency acquisition performance, and also produce an optional reference component at $2f_{ref}$. This can allow a designer to use an on-chip LF with reduced tolerance requirements for passive on-chip components or increase ω_n for the same ω_{ref} . Hereinafter, it is called the Agile-PFD (APFD). The implementation is amenable to CAD automation and is portable across any technology with a standard digital cell library.

3.9.1 Duty-cycle limitation for a dual PFD

It is clear from Figure 3.1, that a PFD gets its inputs from the RD and the FBD, whose outputs seldom have a 50% duty-cycle. In fact, the PFD receives very short pulses that are dependent on the divider architecture. Since the PFD is an edge-triggered device, there is no potential problem if only one PFD is used. In order to combine a PFD-NAND and a PFD-NOR, a potential problem depicted in Figure 3.3 has to be solved.

Figure 3.3: Final locked positions with different duty-cycle inputs

The PFD-NAND signals a phase-lock when the negative edges of the input signals are aligned. The PFD-NOR signals a phase-lock when positive edges of the input signals are aligned. If the outputs of the two PFDs are combined using a simple AND/OR circuit [47], one of the two PFDs would keep producing correction pulses even when the other signals a phase-lock. As a result, the amplitude of the VCO sideband at f_{ref} would be directly proportional to the difference of the duty-cycles between the two PFD inputs. Hence a phase-lock can never be achieved. The solution is in choosing the edge that has to be aligned, and then develop the APFD design methodology.

3.9.2 *Solution to the duty-cycle problem*

To solve the duty-cycle problem, divide-by-2 flipflops can be used at the two PFD inputs, resulting in similar duty-cycles at each input. The key point are, firstly, to have the same edge-sensitivity for both PFDs and, secondly, to get similar duty-cycles over all PVT variations. The latter requirement can be satisfied by using divide-by-2 flipflops and careful symmetric layout. Nominally, the duty-cycle after the divide-by-2 flipflops would be very close to 50%. As depicted in Figure 3.4, the edge-sensitivity has now been transferred from the PFD implementation to the flipflops and the two PFDs with different edge-sensitivities can now be used without the dilemma depicted in Figure 3.3. For this work, a PFD-NAND is built and tested, and positive edge-triggered divide-by-2 flipflops are being proposed for the APFD only.

Since the input frequencies to the two PFDs are halved and the number of PFDs is doubled, the resulting feedthrough harmonic is still at f_{ref} , if the individual outputs are combined correctly. The power dissipation is slightly increased, as there are two additional static flipflops and some logic, but each of the PFDs is operating at half the frequency. The

major portion of the power (around 64%) is used in the buffers. The area of the APFD is less than doubled as the buffers use most of the area too.

Figure 3.4: Final locked positions using divide-by-2 flipflops

3.9.3 Optional reference feedthrough at $2f_{ref}$

The reference feedthrough during phase-locked state is still at f_{ref} instead of $2f_{ref}$, if a simple AND/OR operation is performed to combine the individual PFD outputs, now at half the input frequency. An extra pulse has, therefore, got to be introduced in the *UP* and *DN* outputs every reference cycle to realize the true advantage of the dual-PFD architecture, i.e., a feedthrough component at $2f_{ref}$. A simple scheme that does not interfere with the RESET pulses being produced by the two PFDs, during a phase-locked state, is presented after the design procedure for the APFD.

3.10 Design procedure for the APFD

Let us proceed with the design of the APFD with two simplifying assumptions, i.e., the *UP* and the *DN* signals are both active-high so that the *UP* signal has to be

replaced with its complement when the design is finished. This makes the design procedure more intuitive and easy to understand. The second assumption is that the divide-by-2 flipflops are present at the individual PFD inputs. Hence, during the phase-locked state the outputs from PFD-NAND and PFD-NOR would look as shown in Figure 3.5. The signals are each at a frequency of $f_{ref}/2$. The signals ($U1$, $D1$) are the (UP , DN) outputs of the PFD-NAND. The signals ($U2$, $D2$) are the (UP , DN) outputs of the PFD-NOR.

Figure 3.5: Phase-locked condition for PFD-NOR and PFD-NAND

3.10.1 Arriving at the methodology

Table 3.3 shows the different measures used to describe the output characteristics

TABLE 3.3: PFD characterization in literature

[Ref]	PFD type	x-axis	y-axis	Comments
[49]	quad latch / NOR	Time-skew (ns)	Error voltage (V)	Includes CP
[50]	quad latch / NOR	Phase difference (ns)	CP output voltage	Includes CP
[51]	quad latch / NAND	Phase difference (ns)	Net output pulse-width (ns)	Axes in time units instead of degrees
[52]	Hogges phase detector	Phase error (rad)	Average output of the detector	Includes CP

of the various PFDs in literature. All of them convey the same information but use differ-

ent units on the x-axis and the y-axis. For simulation purposes, a method similar to [51] is adopted for this work. The idea is to find the number of degrees during every reference period during which a PFD works in the correct direction. This is done by integrating the total useful area under the dominant signal (UP or DN) and subtracting from it the non-useful area under the non-dominant signal. In other words, the correctly utilized percentage of the reference period is to be determined for the input phase difference level.

As shown in Figure 3.6, if f_{ref} lags f_{div} , then the VCO frequency has to be lowered and the active-high DN signal is asserted. As an architectural artifact, the narrow active-low UP pulses are also present. This represents non-useful area as these pulses are driving the CP in the wrong direction, albeit briefly. Hence, the useful phase per reference cycle during which the CP is being driven in the correct direction is the difference of the useful area under the dominant DN waveform and the non-useful area under the non-dominant UP waveform. Also, the initial transient period (shown as exaggerated), where one of the signals is asserted continuously, has to be ignored from this calculation for accurate results. Such a simulation artifact might occur due to the lack of initialization of the latches in the PFD.

Figure 3.6: PFD-NAND waveforms: f_{ref} lagging f_{div}

Assuming no artifacts, Equation (3.5) can be written as follows:

$$UsefulArea = \max(\int DN, \int UP) - \min(\int DN, \int UP)$$

$$TotalArea = SimulationTime \times PulseHeight$$

$$UsefulWork = \frac{UsefulArea}{TotalArea} \quad \text{OR}$$

(3.5)

$$UsefulWork = \frac{UsefulArea}{TotalArea} \times 360^\circ \quad (\text{degrees})$$

The formulas in Equation (3.5) can be employed in real-time, for the case of the APFD, only if the composite *UP* and *DN* signals are somehow available from the dual-PFD combination that drive the CP in the correct direction. Otherwise, to integrate the useful areas from several pulses and subtracting the non-useful areas from other pulses sounds like a complex analog and perhaps an off-line operation; and it indeed is. This new methodology presented next is portable, repeatable and technology-independent. Its implementation requires a digital cell library.

3.10.2 Design methodology for the Agile-PFD (or APFD)

By definition, both PFDs work in the correct direction for a major part of each reference cycle depending on the input phase difference. Hence if the *UP* signal is the dominant signal, it is asserted more often than the *DN* signal and vice versa. If we employ '*m*' PFDs, then we have '*m*' *UP* signals and '*m*' *DN* signals. Out of these, if the total number of asserted *UP* signals is more than the total number of asserted *DN* signals at any time, then an *UPWINS* signal can be generated to reflect this condition. A *DNWINS* signal can provide an equivalent indication, in case the reverse is true. Hence, we require a combinatorial 'Voting Circuit'. It is important to realize that when the asserted *UP* and *DN* signals are equal in number, it may or may not be the phase-locked state. An *INSTLOCK* signal may provide only an 'instantaneous' indication of the lock. This signal has to undergo fur-

ther processing before a stable phase-lock condition can be declared. Figure 3.7 shows the logic design process for the APFD.

PFD-NAND		PFD-NOR		VOTING CIRCUIT OUTPUTS		
$U1$	$D1$	$U2$	$D2$	$DNWINS$	$UPWINS$	$INSTLOCK$
0	0	0	0	0	0	1
0	0	0	1	1	0	0
0	0	1	0	0	1	0
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	1	0	0
0	1	1	0	x	x	0
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	x	x	0
1	0	1	0	0	1	0
1	0	1	1	0	1	0
1	1	0	0	0	0	1
1	1	0	1	1	0	0
1	1	1	0	0	1	0
1	1	1	1	x	x	0

$$DNWINS = D1\overline{U1} + D2\overline{U2}$$

$$UPWINS = \overline{D1}U1 + \overline{D2}U2$$

$$INSTLOCK = \overline{UPWINS + DNWINS}$$

Translated to the real active-low UP outputs, we get

$$DNWINS = D1U1 + D2U2$$

$$UPWINS = \overline{D1}\overline{U1} + \overline{D2}\overline{U2}$$

$$INSTLOCK = \overline{UPWINS + DNWINS}$$

Figure 3.7: Truth-table and minimal expressions for APFD design

From this point forward, the UP signal is treated as an active-low signal and the DN signal is treated as an active-high signal. This is consistent with the actual circuit implementation shown in Figure C.35, “APFD schematic overview,” on page 200.

The first temptation is to group the *UP* and *DN* outputs from different PFDs in adjacent columns, if only to accomplish easy reading. There is no theoretical difficulty. At the time of implementation and later during operation, however, the signal-delays through the two PFDs are, in general, not equal. The *UP* and the *DN* pulses from the same PFD are always better matched. Moreover, during phase-locked condition, the pulses *U1* and *U2* never appear together due to different edge-sensitivities. The second temptation is to get a simpler logic circuit by using ‘don’t care’ states while ignoring that the instantaneous phase-lock condition may appear in any cycle for small phase differences, albeit briefly.

Based on these logical equations, we need to find a way to achieve an average output that reflects the true phase difference. For the instantaneous phase-locked condition signalled by *INSTLOCK*, we can perform a logical AND on the two active-low *UP* signals and a logical OR on the two active-high *DN* signals, to preserve their active polarity, and gate them to the output. While the *INSTLOCK* signal is inactive, we can assert one and only one of the outputs (either *UP* or *DN*) based on which of the *UPWINS* or *DNWINS* signal is active. The proposed logical equations ascertain that the APFD outputs never short the supply to the ground in the CP, except for the brief RESET pulses from the individual PFDs. These brief RESET pulses can be removed [75] to allow a more smooth v_{cont} .

3.10.3 Reference feedthrough revisited

In order to translate the reference feedthrough to $2f_{ref}$, we can use another PFD-NAND and connect both of its inputs to the f_{ref} signal, so that it outputs pulses that are always in lock and inherently stable. Since the divide-by-2 flipflops are positive edge-triggered, and the PFD-NAND is a negative edge-triggered device, the *UP* and *DN* pulses from this additional PFD-NAND do not overlap with the existing pulses in the phase-locked condition. Also, since the RD and FBD outputs are gated using their input frequencies and f_{ref} is always lower than f_{div} because of the loop architecture, the unequal

duty-cycles make sure that there are no glitches in the phase-locked condition. This extra PFD-NAND is active during a stable phase-lock, that is defined later. Figure C.35 shows the implementation of the $2f_{ref}$ option in the APFD.

3.10.4 Power dissipation in the three PFDs

The TYPICAL simulations for power dissipation show an increase of 42% if an APFD is used compared to a PFD-NAND or a PFD-NOR that have similar power dissipation profiles. The $2f_{ref}$ option, however, is 70% more expensive than the simple APFD.

Figure 3.8: Power dissipation in PFD-NAND, PFD-NOR and APFD

3.10.5 Maximum operating frequency of a PFD

A proposed estimate [49] is $f_{max, PFD} = (14 \times GateDelay)^{-1}$ for a PFD-NOR that will roughly translate to about 350 MHz for PFD-NOR and PFD-NAND. Since the input frequencies have been halved, the same applies to the APFD with a little added degradation through the ‘Voting Circuit’. Another estimate found in the literature [85] is given in Equation (3.6), where ΔR is the width of the RESET pulse in a typical PFD.

$$f_{max, PFD} = \frac{1}{2\Delta R} \quad (3.6)$$

For the APFD, the RESET pulses are smeared out a little bit more as they are passed through logic gates. The worst-case RESET pulse width is 1 ns for this work, and it translates to a maximum operating frequency of 500 MHz. This estimate is rather relaxed. For 50% duty-cycle PFD outputs, the on-time would be 1 ns for a 500 MHz pulse. This means that the RESET pulse is on half the time. Hence a more practical estimate is one-fourth of this value or $f_{max,PFD} = 1/(8\Delta R)$. Since a PFD is usually not used at such high frequencies, this is not an issue. For high-frequency operation, dynamic PFD architectures are used [73][86]. It has also been suggested [94] that using the PFD at the highest possible frequencies reduces the in-band PN plateau in PLL-FS design. A typical PN specification for a CMOS PFD is -115 dBc/Hz at a frequency offset of 100 kHz.

3.10.6 Output characteristics of the three PFDs

The output characteristics of the PFD-NAND and PFD-NOR are well known [50][51]. They are being presented in Figure 3.9 (a) for reference and comparison.

Figure 3.9: Output characteristics of the three PFDs

The agility in frequency detection should be used sensibly. In general, $\pm\pi$ is considered as the average phase difference between the two inputs. For applications where the phase difference is often more than this value, the system can be thrown into the frequency acquisition mode, albeit briefly. If such functionality is not required, then the use of the APFD is not recommended. The advantage of this enhanced frequency acquisition will

become apparent later when a comparison of acquisition techniques is presented for different acquisition-aiding scenarios in Figure 3.19 and Figure 3.20.

3.10.7 Deadzone simulation

Ideally, the PFD deadzone is measured in the closed-loop configuration. Practically, the PLL-FS jitter can be roughly divided into two parts, i.e., that due to the PFD's deadzone and that from the other components in the PLL-FS. Figure 3.10 shows the simulated deadzone in the phase-locked condition for the APFD assuming an ideal CP.

Figure 3.10: Deadzone simulation for the APFD

3.10.8 Functional simulations

The functional waveforms for the three PFDs are shown in Figure 3.11 and Figure 3.12. The outputs are (UP1, DN1) for the PFD-NAND, (UP2, DN2) for the PFD-NOR and (UP3, DN3) for the APFD. The PFD inputs are (REF, OSC) and denote the (f_{ref}, f_{div}) respectively as in Figure 3.1. The APFD operation is not duty-cycle dependent and looks similar to that of the PFD-NOR for small phase differences as positive divide-by-2 flipflops have been used. Hence, no further stability analysis is required for small phase differences. The frequency acquisition performance is enhanced to 100% for a phase difference of more than 2π and for frequency differences. Power-down operation is also depicted where the CP is disabled except for the flow of a small leakage current.

(UP1,DN1) = PFD-NAND (UP2,DN2)=PFD-NOR (UP3,DN3)=APFD
 ALIGNED NEGATIVE EDGES OF THE INPUT SIGNALS

(a) Negative edges aligned

(UP1,DN1) = PFD-NAND (UP2,DN2)=PFD-NOR (UP3,DN3)=APFD
 ALIGNED POSITIVE EDGES OF THE INPUT SIGNALS

(b) Positive edges aligned

(UP1,DN1) = PFD-NAND (UP2,DN2)=PFD-NOR (UP3,DN3)=APFD
 PHASE DIFFERENCE 160 DEGREES - REF LEADING

(c) Reference leading oscillator

(UP1,DN1) = PFD-NAND (UP2,DN2)=PFD-NOR (UP3,DN3)=APFD
 PHASE DIFFERENCE 160 DEGREES - OSC LEADING

(d) Oscillator leading reference

Figure 3.11: Functional waveforms for PFD-NAND, PFD-NOR and the APFD

(e) Lower reference frequency

(f) Lower oscillator frequency

(g) Power-down operation

(h) $2f_{ref}$ operation (optional)

Figure 3.12: Functional waveforms for the three PFDs (continued)

3.11 Lock detection overview

The VCO cannot jump between two arbitrary frequencies; e.g. f_1 and f_2 , without going through all the frequencies in between. Such a transition can pollute the RF spectrum. For this reason, the output has to be turned off, while the PLL-FS is switching between channels. In order to accomplish this, a Lock-Detection Circuit (LDC) has to be present in the PLL-FS that disables the output during acquisition until a stable phase-lock is detected. For low-frequency integer-N synthesizers, the LDC might be used, for instance, to enable the enhanced acquisition capability or to switch to a different phase detector to achieve a low-noise operation during phase-locked state. The LDC can deliver out-of-lock information that can be used to change the loop-bandwidth of the PLL-FS.

The definition of phase-lock depends on the application. The most popular method has been proposed by Gardner [63]. In this method, cycle-slips are detected. A cycle-slip occurs when two consecutive edges are applied to one of the inputs of the PFD. Other, less-used definitions, along with a general discussion can be found in [64]. There are many occasions when a ‘near-locked’ condition is also useful to detect and cycle-slipping is by no means the standard or the only definition of an unlocked state.

The information about phase-lock can be derived by comparing the outputs of a PFD in the phase-locked state as shown in Figure 3.13. A simple XOR gate can be used to

Figure 3.13: Typical PFD outputs in the phase-locked state

compare the two signals. If the output is a logical ‘1’, then the signals are different and a ‘LOCK’ signal can be generated. If the output is a logical ‘0’, then one of the pulses is

wider than it should be, thereby indicating a phase difference. The 'LOCK' signal does not provide an accurate indication of phase-lock over time. It can only signal the unlocked state as it happens, or indicate that there is a phase difference or a frequency difference.

The key point is to filter the 'LOCK' or *INSTLOCK* signal using an LPF, and to wait for a certain time, before declaring a more stable indication of phase-lock, i.e., the 'CLEANLOCK' signal. This 'CLEANLOCK' signal can then be used to control the acquisition-aiding circuitry. The circuit-level details are described later in Chapter 4.

3.12 New acquisition-aiding methodology - *AgileLock*

Whereas the patented methodology described in [46] reduces the acquisition time by a factor of 2, it requires an analog pad on-chip and an extra resistor on the PCB in case of an external LF. Further analysis of stability has to be done and simulations have to be performed for the extreme cases of frequency switching.

The newly proposed AgileLock methodology shown in Figure 3.14 has two components. First, the newly proposed APFD is used with enhanced current in the CP. This reduces the total acquisition time as described later. The overshoot during the acquisition is optionally reduced using a previous scheme proposed in [42]. In that work, a reset pulse is applied to the PFD, RD and FBD, when the frequency acquisition is deemed complete. This removes the ringing and allows faster settling. This method is exact but it requires a noisy digital ALU that can inject a lot of noise within the loop bandwidth. The power consumption is another drawback. This kind of ALU can be synthesized very easily using digital logic, but it can occupy a significant area compared to the rest of the chip. The new method does not require the exact determination of the point when frequency acquisition is complete, rather it relies on a simple calculation of the pull-in time and the application of a reset pulse to the RD, FBD and the PFD. This reduces ringing, but does not remove it completely. The information on when to apply the reset pulse can be stored in terms of the

reference cycles, just like the divider-combinations are stored in a RAM. Hence, the circuitry required for the exact determination of the pull-in time can be avoided.

Figure 3.14: Overview of the AgileLock technique

3.12.1 The reset pulse

Resetting the PLL-FS is only advantageous, during and towards the end of the pull-in phase as shown in Figure 3.14. Especially with the APFD, the transition back into the frequency acquisition mode mostly requires three reference cycles or less, so not much time is lost. However, this should not be continued after the final frequency has been reached, as the settling process can be affected in unpredictable ways.

During the period immediately following the PLL-FS frequency switching command, the frequency difference between the PFD inputs is large. Hence the acquisition can continue smoothly at 100% efficiency for an APFD. This should be further checked at some close-in frequency difference conditions as shown in Figure 3.15. It can be seen that

because of the enhanced frequency detection capability of the APFD for any phase difference that exceeds $\pm 2\pi$, the APFD works rather smoothly during frequency acquisition.

Figure 3.15: Effect of the reset pulse for small frequency differences

The ‘CLEANLOCK’ signal is used to trigger four times the normal current in the CP resulting in a faster acquisition. After the phase-lock is achieved, the CP returns to the normal low-current mode. The circuit implementation is shown in Figure C.36.

3.12.2 Stability considerations for the AgileLock

By referring to Figure 2.8 and [50], it is evident that $\omega_n \leq \omega_c$. If the loop is designed with ω_n in mind, then quadrupling I_p during PLL-FS acquisition doubles ω_n and should only improve the PM. If the calculations are initially done to optimize the LF component values at ω_c , then the PM degrades a little. Hence there is no apparent need for changing the LF bandwidth during acquisition to maintain stability as suggested in [46][95][103]. Moreover, by examining Equation (2.40), it can be calculated that if $\zeta_{min} = 0.5$, then $f_{ref}/f_n = 2.54$ is the condition required for stability. Usually the PLL-FS is designed to prevent further degradation of ζ below 0.5 and the ratio f_{ref}/f_n

is maintained at 20, while the minimum acceptable value is 10. Hence, there are no stability concerns for a 3rd-order, type-II, CP-based PLL-FS, using the AgileLock methodology.

3.12.3 Advantages of the AgileLock methodology

- Circuit complexity and cost is minimal and no external or specialized on-chip components are required.
- It is technology-independent and requires a digital cell library for implementation.
- It uses an already tested concept in conjunction with the newly designed APFD to implement a very simple but effective acquisition-aiding mechanism.
- Since the ringing is reduced, it allows greater utilization of the VCO tuning range resulting in a smaller K_{vco} . This improves the PN performance of the PLL-FS.
- Since the acquisition-aiding circuitry is free-wheeling, i.e., it requires no initialization sequences for the enhanced current during acquisition, the start-up time of the PLL-FS is also improved. The reset pulse is not free-wheeling at this time and would require the same circuitry as in [42] to eliminate ringing completely. The ringing can be reduced by a judicious choice of the reset instant, stored in a RAM.

3.13 PLL-FS system design and practical tips

If an external crystal oscillator is already present, then it is desirable to formulate a frequency-plan around that oscillator. In our target system, the crystal oscillator is running at 14.31818 MHz with a nominal accuracy of 70 ppm. The output frequency is related to the input frequency in Figure 3.1 as described by Equation (3.7):

$$f_{out} = \left\{ \frac{(N+2)}{(R+2) \times Q} \right\} f_{xtal} \quad (3.7)$$

With the chosen divider architecture, division is performed by $(N+2)$ instead of N , where N, R and Q have their usual meanings. The post-scalar can divide by 1/2/4/8 and is

controlled by a two-bit interface. Since the specified VCO tuning range is 80 MHz - 200 MHz, a division by 8 at the output provides a minimum of 10 MHz.

3.13.1 Frequency planning

For variable N and R , the valid combinations required to achieve all the outputs are determined as shown in Figure 3.16. A spreadsheet might prove very useful here.

Figure 3.16: Frequency-plan using the crystal frequency $f_{ref} = 14.318$ MHz

Sometimes the frequency to be generated is more accurately reached by going to a higher reference/output frequency first and then by dividing down using the post-scalar. With a fixed f_{ref} , this step is simplified. This might also be done to improve PN or acquisition performance for a required combination. Storing the (N, R, Q) combinations in a RAM is an efficient way of switching between channels. The length of the FBD can now be calculated based on the minimum f_{ref} . For this design, we choose a minimum f_{ref} of 2 MHz and a hertzian loop-bandwidth of $f_{ref}/20 = 100$ kHz. Hence, in order to achieve frequencies from 80 MHz to 200 MHz, we need an FBD ratio of $N_{min} = 40$ and $N_{max} = 100$, that is achievable using a 7-bit presettable divider.

3.13.2 *Initial planning and considerations*

The design methodology will be presented step-by-step to allow more probability of success for first-time designers in an already chosen submicron CMOS technology.

- Choose a package, as the synthesizer is likely to be packaged for testing. Wafer-probed designs are severely limited by the number of probing-pads. The selection of a package allows one to calculate the bond-wire length and package parasitics. This may be more relevant for RF applications.
- If the LF is external, then the die area can be pre-estimated to find the length of the bond-wire for a given package and its cavity size. This can be used in calculations, in addition to the package parasitics.
- If the LF is monolithic, then it is a good idea to test some capacitance structures separately before putting them on the final chip. This will allow accurate prediction of die area and top-metal jumpers can be used to fine-tune the passive elements, if required. Once fabricated, the passive structures are not very flexible.
- Choose the ESD protection structures for the input pads. The best source of information on ESD issues is the fabrication facility as they have a wealth of experience from customer feedback. Also investigate the effects of antenna errors on fabricated chips from technical support. These things cannot be simulated, so experience already gained at the fabrication source is essential.
- Identify the testing requirements, and choose a testing/floorplanning/layout strategy based on it.

For instance, if cross-talk between two or more synthesizers is to be measured, then one can switch a synthesizer between extreme division ratios by using only one test signal tied to all the divider inputs in a pre-defined 'test-mode'. If one wants to measure the PN of the synthesizer with several VCOs and PFD options, then it might be a good

idea to have different on-chip VCOs and PFD options that can be enabled one at a time, possibly using laser surgery. In general, it is a good idea to have layout redundancy and top-metal configuration jumpers for commercial and academic designs alike.

- If the chip-area is limited or if there are too many unknowns, consider sending all the components out as wafer-probed designs for the first run. This allows accurate characterization without package parasitics and usually improves the final design.
- Once the input signals and the testing strategy are confirmed, a chip floorplan is used to make a bonding diagram, so that the PCB design work can proceed in parallel.

If it is an extended project where several synthesizers have to be tested, then it is a good idea to make a modular PCB that can be re-used. Chip floorplanning is necessary for an organized bonding diagram. It also allows a designer to maintain better isolation between analog, digital and RF sections on a large chip and streamlines the PCB design process. If pins can be spared, consider separate multiple pins for digital, analog and buffer supplies. The ground pins can be shared, if required [120].

- Calculate the power dissipation expected in the analog, digital, buffer and RF sections. The supply and ground lines have to be sized accordingly and slotted in the direction of the current flow, if required by the Design Rule Checker (DRC).
- If it is a large digital chip, determine the peak in-rush current and take that into account while designing for the external decoupling capacitors.
- Determine if a separate analog supply is available for the target system, else design differential cells for better PSRR and consider a voltage regulator/bandgap reference option for the analog supply.

3.13.3 System design of the PLL-FS

The system design refers to the calculation of LF parameters that, in turn, determine the system-level parameters ω_n , ζ and T_{acq} . The parameters ω_n and ζ vary with

N approximately as $1/\sqrt{N}$. Equation (3.8) proposed in [19] can be used to find optimum ranges for these parameters.

$$\frac{\zeta_{max}}{\zeta_{min}} = \frac{\omega_{n,max}}{\omega_{n,min}} = \sqrt{\frac{N_{max}}{N_{min}}}$$

$$N_{mean} = \sqrt{N_{min}N_{max}} \quad (3.8)$$

The next step is to use K_{vco} to determine ω_n and ζ . At the time of initial design, however, the VCO probably does not exist. Hence, if the LF is monolithic and the value of K_{vco} is found to be different after fabrication, from the one used for initial calculations, then the monolithic LF might not provide optimum performance. For an external LF, this is not an issue as the LF component values can be changed easily. This circular design procedure is inevitable and hence parameters from an existing VCO (fabricated later, see Chapter 5), i.e., VCO2, are being used in Equation (3.9) for initial design.

The value of K_{vco2} is approximately calculated as follows for VCO2:

$$K_{vco2} = \frac{2\pi(280\text{MHz} - 30\text{MHz})}{2.0\text{V} - 0.5\text{V}} = 1047 \cdot 10^6 \frac{\text{rad}}{\text{s} \cdot \text{V}} \quad (3.9)$$

Making use of Equation (2.32), Equation (2.33), Equation (3.8) and the values of ω_n and ζ already calculated in Table 3.4, we can calculate the values of C_2 and C_1 . Calculation of R_2 was verified using a behavioral simulator to achieve a reasonable PM.

TABLE 3.4: Range of system-level parameters and loop-filter values

N	ζ	ω_n	C_2	C_1	R_2
40	0.894	$2\pi * 126 \text{ kHz}$	169 pF	16pF	34.09 k Ω
64	0.707	$2\pi * 100 \text{ kHz}$	65.0 pF	6pF	34.62 k Ω
100	0.565	$2\pi * 79 \text{ kHz}$	22.8 pF	2pF	34.49 k Ω

Since C_2 cannot change easily unless this is built into the design, its nominal value at $N_{mean} = 64$ is chosen for the calculation of R_2 after τ_2 is calculated. For the PM, we use Equation (2.21) and fix C_1 and C_2 at 65 pF and 6 pF respectively. The PM is roughly calculated as 44° . This will result in some ringing and hence, a new design iteration must be done, the optimum goal being 60° . The pull-in time is directly affected by C_2 as there is a fixed I_p available to charge C_2 ($I_p = 10 \mu\text{A}$ for this work).

Assuming that for a conventional PFD, the CP phase-utilization is only 50% while there is a 2x frequency difference, the pull-in time evaluates to $13.8 \mu\text{s}$ whereas the behavioral simulator shows a value of around $9 \mu\text{s}$. The ringing seen in Figure 3.17 (a) suggests $\zeta \approx 0.5$ as calculated in Table 3.4. The settling-time is reported at $30 \mu\text{s}$. The start-up time is around $13 \mu\text{s}$. The open-loop response Bode plot shows a phase margin of 50° that also agrees with hand calculations. The ringing increases at larger N values, as ω_n varies with $1/\sqrt{N}$, as pointed out earlier. It can also be noticed from Figure 3.17 (b), that as the open-loop response crosses the 0 dB point at ω_c , the PM is not at its peak. So doubling ω_n on the log-scale will result in the point at which the PM is calculated (i.e. ω_c) to move from the left side of the phase-plot curvature to the right side, if nothing else changes.

Figure 3.17: An example PLL-FS design (a) switching (b) loop response

The design iterations have been performed using a third-party behavioral PLL simulator called the ‘=PLL=’ [80]. It was selected because it was used in [37]. Figure 3.17

shows the simulation using the behavioral simulator ‘=PLL=’. A typical simulation time is around 5 seconds on a Pentium™ 333 MHz computer with 64 MB of RAM.

According to [81], the timing jitter, σ_{rms} due to supply and substrate voltage injection V_m , can be calculated for a single FM source at frequency f_o , as follows:

$$\sigma_{rms} = \frac{K_{vco} V_m \omega_{ref}}{\sqrt{2} \cdot f_o^3} \quad (3.10)$$

For an expected rms jitter of 50 ps, $f_o = 200$ MHz, $K_{vco} = 166$ MHz/V (units as used in the paper) and $\omega_{ref} = 2\pi(14.318)$ Mrad/s, a perturbation amplitude on the supply of 37 mV is tolerable. This points out the need for an on-chip voltage regulator that is not shown for this work. The size of the external decoupling capacitors would also include the calculation in Equation (3.10), but it will be dominated by the current spiking due to the digital circuitry in case of a large digital chip. Separate power pads and a clean power supply were available for the analog circuitry in our case.

The noise floors of various components, as proposed in ‘=PLL=’, have been chosen as -115 dBc/Hz for the PFD and -120 dBc/Hz for the dividers. These could not be independently verified by simulation but the measured values shown in Chapter 5 are typically worse than expected of a typical of CMOS design. It is suspected that the PN measurement system is not accurate enough for close-in measurements.

The PLL-FS is a synthesizer that acts like a frequency multiplier. Hence it multiplies the noise power in the PFD and FBD. A large N should, therefore, be avoided. For a division ratio of 64 and 100, the PN degradation is $20\log 64 = 36$ (dB) and $20\log 100 = 40$ (dB), respectively. The VCO is the major noise contributor outside ω_n . This effect can be reduced by increasing ω_n , a requirement that is in conflict with the low-pass noise-TF for the PFD and the FBD, and also limited by the $\omega_{ref}/\omega_n \approx 10$ constraint as pointed out earlier in Chapter 2.

3.13.4 *Simulating loops with monolithic loop-filters*

Simulating loops with monolithic LFs, requires the determination of the worst-case loop-parameters and the worst-case LF component values. Let us assume that the process is constant. The worst-case divider ratios would then be the extreme numbers for N and R as calculated during the frequency planning stage. The FAST and SLOW (process corners described in Table 4.2) values for the LF components should be calculated at the very least, if not the BEST and WORST corners (See “Simulation techniques” on page 109). The following simulations would then be performed.

- FAST process values for LF and all the loop parameters, lowest N , lowest R .
- SLOW process values for LF and all the loop parameters, lowest N , lowest R .
- FAST process values for LF and all the loop parameters, highest N , highest R .
- SLOW process values for LF and all the loop parameters, highest N , highest R .

Hence, complete characterization of a monolithic PLL-FS requires time and manpower. In the absence of accurate behavioral models it is cumbersome to attempt this at the circuit level. An example showing the optimization of the LF using behavioral phase-domain models appears in [82].

3.13.5 *Compensating for loop-parameter variations*

There are four identical branches in the CP shown in Figure C.6, that can be enabled as we increase N in order to keep I_p/N relatively constant. A typical calculation is shown in Table 3.5. These branch-activation sequences can be stored in a RAM along

with the N, R and Q combinations. Also, since the noise from the PFD, CP and FBD is divided by the PFD gain, it is advantageous to increase I_p , if the power budget allows.

TABLE 3.5: Chargepump branch-activation calculations

N	I_p (μA)	I_p/N	K_{vco} , (Mrad/s/V)	$K = \frac{K_{vco}R_2}{2\pi} \cdot \frac{I_p}{N}$	$I_{p, required}$ (μA)
40	10	0.25 μ	1047	1.41 Mrad/s	10.0 μA
64	16	0.25 μ	900	1.21 Mrad/s	18.6 μA
100	25	0.25 μ	650	0.87 Mrad/s	40.1 μA
128	32	0.25 μ	500	0.67 Mrad/s	66.7 μA

Since K_{vco} normally flattens at end of the range, I_p might also be used to compensate for a reduction in K , in order to keep ω_n and ζ relatively constant throughout the operating frequency range of the PLL-FS. The selection can be made using little additional logic circuitry if the calculation proceeds in powers of 2, i.e. $N = 1, 2, 4, 8, \dots$. Identical current sources reduce the potential I_p mismatch. For this work, the variation in ω_n and ζ is not critical because of the small FBD ratios, so three additional CP branches are used to enhance the acquisition performance instead.

3.14 Test-set for verifying AgileLock

To verify AgileLock operation and to compare it with the patented technique [46], the PLL-FS presented as the example design is simulated at the transistor level, under TYPICAL conditions, using the following six test conditions.

- **Case (a):** Full PLL-FS with a PFD-NAND. No acquisition aiding is present.
- **Case (b):** Full PLL-FS with the patented technique (as implemented in ICECUIR1, described in Chapter 4). The current is enhanced during acquisition from 10 μA to 40 μA to improve the acquisition time and the resistor R_2 is halved as in [46].

- **Case (c):** Full PLL-FS with the APFD, $I_p = 10 \mu\text{A}$, no acquisition aiding.
- **Case (d):** Full PLL-FS with the APFD, AgileLock, $I_p = 10 \mu\text{A}$, ringing suppression attempted through five reset pulses applied to the RD, FBD and the APFD.
- **Case (e):** Full PLL-FS with a PFD-NAND, $I_p = 40 \mu\text{A}$ during acquisition. No change to the LF and no ringing suppression attempted.
- **Case (f):** Same as Case (e), except uses the APFD.

3.15 Typical second-order step-response equations

A typical 2nd-order step-response, that explains the various acquisition time components applicable to the PLL-FS, is shown in Figure 3.18. This figure is adopted from [31] along with some equations. The relevant definitions from PLL theory are superimposed on Figure 3.18. It can be seen that there are three distinct phenomena that can be manipulated in order to reduce the total acquisition time; namely pull-in time, settling-time and lock-time.

3.16 Methodology for the reduction of acquisition time

By doubling ω_n , the pull-in time T_p reduces by 4^+ as it varies inversely with ω_n^2 , and also because ω_L appears in the numerator in Equation (3.3) and is subtracted from $\Delta\omega$. If the LF is not changed, then τ_2 does not change, and hence doubling ω_n doubles ζ , as pointed out in Equation (2.32). The settling-time, T_S , that varies inversely with both ω_n and ζ , is therefore, reduced by a factor of 4 (see Figure 3.18). The lock-range, ω_L is doubled and the lock-time is reduced by 2^+ as it is inversely related to ω_n as shown in Equation (3.4). Hence, an improvement factor of 3 to 4 is expected for the total acquisition time, T_{acq} . The calculations following Figure 3.18 show the procedure.

$$v_{cont}(t) = 1 - \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t} \sin\left(\frac{\omega_n t}{\sqrt{1-\zeta^2}} + \theta\right)$$

Comments

- The image is not drawn to scale.
- The pull-in time (T_p) is a non-linear phenomenon and is not exactly described by $v_{cont}(t)$ above.

$$T_p = \frac{\Delta\omega - \omega_L}{\pi N \omega_n^2} \quad T_L = 2\pi / \omega_n$$

$$e^{-\zeta\omega_n T_S} < 0.005 \Rightarrow T_S = \frac{5.29}{\zeta\omega_n} \quad \therefore T_S \approx 4-5 \text{ time constants assuming } \omega_L \text{ is } 0.5\% \text{ of the operating frequency range.}$$

- The lock-time (T_L) corresponds to the lock-range, ω_L only. There are no cycle-slips within T_L .
- There is no cycle-slipping after $v_{cont}(t)$ response enters the lock-range.
- T_p is directly related to the size of C_2 and can be reduced depending on available I_p .
- T_L can be reduced by increasing ω_n .
- T_S can be reduced by increasing ω_n and ζ .

Figure 3.18: Step-response of a second-order control-system parameter [31]

Pull-in time calculations:

$$T_p = \frac{\Delta\omega - \omega_L}{\pi N \omega_n^2} = \frac{\{(286.36 - 114.54) \times 10^6 - 11.13(79 \times 10^3)\} 2\pi}{\pi(100)(2\pi(79) \times 10^3)^2}$$

$$T_p = 13.88 \mu s \quad (\text{For normal mode})$$

$$T_p = \frac{\Delta\omega - \omega_L}{\pi N \omega_n^2} = 3.3 \mu s \quad (\text{For enhanced-current Mode})$$

Settling-time and lock-time calculations:

$$e^{-\zeta \omega_n T_S} < 0.005 \Rightarrow T_S = \frac{5.29}{\zeta \omega_n} \text{ assuming } \omega_L \text{ is } 0.5\% \text{ of maximum frequency}$$

$$\therefore T_S \approx 4 - 5 \text{ time constants}$$

$$\therefore T_S = 26.6 \mu s \text{ for } \zeta = 0.5 \text{ and } \omega_n = 2\pi(79) \text{ kHz}$$

$$T_L = 1/f_n = 12.66 \mu s$$

$$T_{acq} = T_S + T_L = 39.25 \mu s \quad (\text{For normal mode})$$

$$\text{For double } \omega_n, T_S = 5.26 \mu s (\zeta=1), T_L = 6.25 \mu s$$

$$T_{acq} = T_S + T_L = 11.51 \mu s \quad (\text{For enhanced-current mode})$$

Overshoot calculations adopted from [31]:

$$f_v = 2.00 \text{ V corresponding to } 286 \text{ MHz for VCO}_2,$$

$$\text{Overshoot} = M_p = 1 + e^{\frac{-\zeta \pi}{\sqrt{1-\zeta^2}}} = 1 + 0.16 \text{ or } 16\% = 2.32 \text{ V}$$

Additional helpful formulas adopted from [31]:

$$T_{r1} = \frac{2.16\zeta + 0.60}{\omega_n} \quad \zeta \approx \frac{0.55}{\text{cycles}} \quad T_{peak} = \frac{\pi}{\omega_n \sqrt{1-\zeta^2}}$$

$$\text{Percent Overshoot} = \text{P.O.} = \frac{M_p - f_v}{f_v} \times 100$$

The pull-in time calculations can be used to apply one reset pulse near T_p , as it will prevent excessive overshoot and improve settling behavior. Or one can apply closely spaced reset pulses starting at T_{r1} and ending before T_{peak} as shown in Figure 3.18.

Acquisition is a highly non-linear process and the foregoing calculations cannot be completely verified using the behavioral simulator ‘=PLL=’. Therefore, transistor-level transient simulations are necessary for the verification of the hand-calculated results for the six test cases (See “Test-set for verifying AgileLock” on page 73).

In order to conserve power in the normal operating mode, the quadrupled I_p is terminated as soon as a stable phase-lock is sensed by the LDC. The schematics of the acquisition-aiding circuitry appear in Appendix C (see Figure C.36, “Acquisition-aiding circuit interconnections,” on page 201).

The hand calculations are summarized in Table 3.6 and the results of the circuit-level transient simulations appear in Figure 3.19 and Figure 3.20. At this time, the AgileLock is not free-wheeling and an example simulation (Case (d) in Table 3.6) is included that shows a reduction in overshoot as a result of applying a train of five reset pulses to the PFD, RD and FBD.

3.17 Comparison of acquisition techniques

TABLE 3.6: Comparison of acquisition techniques

Loop-parameters: $R_2 = 34.6 \text{ k}\Omega$, $C_2 = 65 \text{ pF}$, $C_1 = 6.5 \text{ pF}$, $I_p = 10 \text{ }\mu\text{A}$, $\text{VCO} = \text{VCO2}$, $N = 40$ to 100, $f_{ref} = 2.86 \text{ MHz}$, $f_{vco} = 286.3 \text{ MHz}$, 50% duty-cycle output							
	Units	Case (a)	Case (b)	Case (c)	Case (d)	Case (e)	Case (f)
I_p (normal / acquisition mode)	μA	10 / 10	10 / 40	10 / 10	10 / 10	10 / 40	10 / 40
PFD type	N.A.	PFD-NAND	PFD-NAND	APFD	APFD	PFD-NAND	APFD
Changes to the LF during acquisition	N.A.	None	R_2 halved	None	None	None	None
Free-wheeling	N.A.	Yes	No	Yes	No	Yes	Yes
Number of reset pulses	N.A.	None	None	None	5	None	None
$\omega_n = 2\pi f_n$	rad/s	$2\pi.79$ kHz	$2\pi.160$ kHz	$2\pi.79$ kHz	$2\pi.79$ kHz	$2\pi.160$ kHz	$2\pi.160$ kHz
$\zeta, \sim @ N=100$	N.A.	0.55	0.55	0.55	0.55	0.9	0.9
$\zeta, \sim @ N=40$	N.A.	0.95	0.95	0.95	0.95	1.8	1.8
$T_p = T_r$	μs	8.1	2.66	6.6	11.57	0.45	0.47
$T_L = 1/f_n$	μs	12.65	6.25	12.65	12.65	6.25	6.25
$T_S = T_{acq} - T_L$	μs	28.58	15.07	32.01	31.65	5.23	3.87
T_{acq} (simulated)	μs	41.23	21.32	44.66	44.3	11.48 / 16.27	10.12 / 13.9
T_{acq} (theoretical)	μs	39.25	16.25	32.94	$6.6 +$ $12.65 =$ 19.25^+	$1.65 +$ $6.25 +$ $\sim 4 =$ 11.9	$<1.65 +$ $6.25 +$ $\sim 4 =$ 11.9
Overshoot	V	0.29	0.32	0.41	0.15	0.32	0.37
Simulation Time ^a	hr	45	55	49	60	47	49

a. Simulation time is normalized for a typical SunBlade™ 1000/5 GB RAM/40 GB hard-drive/single-user

Case (a)

Case (b)

Case (c)

Figure 3.19: Comparison of results from some acquisition techniques - 1

Case (d)

Case (e)

Case (f)

Figure 3.20: Comparison of results from some acquisition techniques - 2

3.18 Discussion of the PLL-FS acquisition results

It can be seen that the AgileLock is stable without changing the LF parameters as suggested in [46][95][103]. This reduces the cost of an additional bond-pad and PCB design effort in the case of an external LF. It is an easily repeatable and free-wheeling technique that offers a reduction in the unaided acquisition time by a factor of 3.5 (and more if a reset pulse can be applied to the APFD, RD and FBD at the correct time to suppress the ringing). It is evident from Table 3.6, that a significant reduction in acquisition time is possible only by increasing ω_n during acquisition. This does not necessarily have to be accompanied with changes to the LF, if the increase in ω_n is two-fold only. The settling-time for smaller N degrades a little for ‘Case (e)’ and ‘Case (f)’ in Table 3.6, as the damping factor has increased to an estimated 1.8 for $N = 40$. This is a small trade-off for reducing the acquisition time without any complicated circuitry. The PFD-NAND, i.e., a quad-latch version of the conventional PFD is not a bad frequency detector after all. The results will be better for the newly proposed APFD, if the capacitor C_2 is bigger and if the frequency range is 1:5 from minimum to maximum frequency. This foregoing discussion assumes that the ratio $f_{ref}/f_n > 20$, that is usually the minimum acceptable value for adequate VCO sideband suppression. Stability is, therefore, maintained as described earlier. Another comment is that it might not be possible to apply a reset pulse for small frequency jumps as the synthesizer would already be in the overshoot portion of the characteristics in less than a reference cycle. For a PLL-FS with an external LF, a minimum value of C_1 should be at least three times the estimated package and PCB parasitics so as to remain comfortably stable. Typical values might be $C_1 = 40$ pF, $C_2 = 500$ pF and R_2 as required to maintain stability. This will result in a ten-fold degradation of the acquisition time. The example design is acceptable for a PLL-FS with an internal LF with some caution, but not a practically sound alternative for a PLL-FS with an external LF. The acquisition time will be around 120 μ s in such a case, and this has been coarsely verified

using the system simulator '= PLL='. Simulation time will be around 9 days for such a scenario and the circuit-level simulations have, therefore, not been attempted.

3.19 Summary

This chapter presented the design methodology and the logic design equations for the newly proposed Agile-PFD or the APFD.

The concepts and terms relevant to PLL-FS acquisition were reviewed. A survey of the literature on PLL acquisition was presented. An example design for the target chip was shown using hand calculations. The example design was later verified and optimized using a behavioral simulator. Simple formulas were adopted from control-systems literature as well as PLL theory to estimate the pull-in time, the settling-time, and the lock-time for the example PLL-FS design. A new acquisition-aiding methodology, the AgileLock, was presented that can reduce the total acquisition time by a factor of 3.5 in conjunction with the APFD. The circuit complexity to implement this enhancement was found to be minimal, as no change to the LF was required.

A comparison of the results, obtained using transistor-level transient simulations, for various acquisition techniques was presented at the end of the chapter along with a data table summarizing the same. The chapter ended with the conclusions derived from these results.

Circuit Design and Simulation Techniques

4.1 Chapter overview

This chapter provides the details of the submicron implementation of the PLL-FS components. A short section is devoted to simulation techniques and frequently encountered simulation problems. The actual schematics and layouts are present in Appendix C. For reasons of brevity, the relevant post-layout simulations are shown in Chapter 5 alongside of the actual measurement results.

4.2 Submicron implementation of the PLL-FS components

The criteria for selection of component architectures were the proven simplicity, previous success of the architecture in another CMOS technology, and portability across upcoming CMOS technologies. The components designed for this work are all single-ended. If a higher robustness to external noise and power-supply induced variations is desired, a fully differential design approach should be considered.

All components are required to have a power-down (PD) functionality, so while the PLL-FS is not in use, power can be saved. Where and if required, a short pulse at the PD input also doubles as the reset signal for a component.

A key commercial point is that the PLL-FS is usually embedded in a large digital system and is sold as a black-box to potential customers. Hence, due to the generic and

modular nature of the applications, there are usually many configuration inputs that enable or disable the hardware functions based on commercial incentives. For instance, the enhanced acquisition mechanism can be enabled or disabled, or the customers might have the option using different phase detectors or VCOs based on their requirements. The final layout for the die is not always changed except for the top-metal layer, that also contains configuration jumpers. Hence, the functionality that is not sold as options should be ‘free-wheeling’, meaning that software-controlled initialization sequences should be avoided, whenever possible. The architecture of the components should be such that they are able to reset themselves in a couple of reference cycles after a Power-On-Reset or a system-wide PD event.

4.2.1 PFD

The PFD has already been described in detail in Chapter 3. Two small circuit-level details are presented here. First, the power dissipation in the buffers is 64% of the total power used in the PFD-NAND and PFD-NOR. This is used to drive the switches in the CP so that complete switching occurs fast. Second, the global delays through the buffer chain at the PFD outputs are optimized in conjunction with the CP. The effects of these circuit-level issues are discussed in conjunction with the CP implementation, as described next.

4.2.2 Chargepump

A digital PFD [48] is almost always used with a chargepump [28]. The single-ended architectural overview of the CP is shown in Figure 4.1. This architecture is derived from techniques available in the literature. The UP and the DN signals from the PFD along with their complements control the time that the current sources I_{up} and I_{dn} are active during each reference cycle as shown in Figure 3.1. Some enhancements have been attempted to reduce the unnecessary current spikes that result in the presence of spurs at the v_{cont} input. This improves PLL-FS settling behavior and noise performance. These CP

voltage spikes have to be reduced by pre-filtering before they reach the active LF in order to avoid opamp saturation, if that is the preferred LF type.

Figure 4.1: Architectural overview of the chargepump

There is a minimum width pulse inserted every reference cycle in the PFD outputs. This pulse gives ample time to the switches to turn on completely, and prevents any partial or incomplete switching as a result of a very small phase difference. This eliminates the deadzone. In the steady-state, i.e., the phase-locked state, the width of the two pulses is different by the amount corresponding to the leakage current. This is one form of static mismatch that is usually non-dominant. The leakage current is of the order of pA.

Another form of static mismatch appears due to the difference in DC magnitudes between I_{up} and I_{dn} . This happens as v_{cont} approaches the rails, limited by the $v_{d,sat}$ of the devices in the current-mirror. Cascoded current sources can be used to reduce this mis-

match, at the expense of a slightly reduced operating voltage range. For a mixed-signal chip, the SLOW supply voltage corner is usually 10% below the TYPICAL corner and that becomes a major limitation for the dynamic range as opposed to any device design as shown in Figure 4.2. The gate-lengths of the current-mirror devices should at least be twice the minimum feature size to increase their output impedance. For this work, the two currents, I_{up} and I_{dn} are matched near the centre of the operating range with their sum optimized to have small variation as shown in Figure 4.2. This results in a predictable detection of phase-lock over the entire tuning range of the PLL-FS, as the *UP* and *DN* pulses are slightly wider than usual near the supply rails. Most PLL-FS implementations would have a clean analog supply referenced to an on-chip bandgap reference for the critical analog circuits to counter the dynamic range problem. This has not been attempted for this work as a clean supply from separate pads was available elsewhere in the system.

Figure 4.2: DC characteristics of the chargepump at process corners

Dynamic mismatch occurs when there is a difference between the on-time and the off-time of a switch in the CP. Full-swing *UP* and *DN* signals with short rise-times and

fall-times can be used to turn on and turn off the transistors thereby reducing this particular mismatch. This is the function of the large inverter chain at the PFD output.

Misalignment of the *UP* and *DN* pulses can result in sharp spikes that create strong spurs at f_{ref} . This is depicted in Figure 4.3. The magnitudes of these spikes can be up to ten times the normal current levels with a duration of one to two gate-delays. In our case, this would be in the range of 100 ps to 300 ps. Such sharp spikes can be minimized by optimizing the global delays through the inverter chain at the PFD output. The effect of this misalignment on VCO sidebands has been discussed in [37].

Figure 4.3: Artifacts of the misalignment of PFD pulses

Switching in the CP creates a clock feedthrough component because of the presence of parasitic capacitances (C_{gs} and C_{gd}) associated with every MOS transistor. This feedthrough can be reduced by using a similar type of transistor driven with the complement of the signal. One of the two schemes as outlined in Figure 4.4 can be used. Scheme

Figure 4.4: Clock feedthrough cancellation schemes

(a) is used to cancel the clock feedthrough component at the sensitive node and scheme (b) is used for charge cancellation at both nodes [12]. Scheme (a) has been used in Figure 4.1 and it shields the sensitive node, i.e., v_{cont} .

The charge-removal circuit has been adopted from [61]. The unity-gain buffer removes the excess charge from *Node A* and *Node B* in Figure 4.1, so that the transient settling performance of the current sources is improved. Without this circuit, these nodes would effectively be floating. The voltage will become unpredictable because of charge-sharing due to parasitics at these nodes that are not known *apriori*. Every time a switching action occurs, *Node A* and *Node B* will take extra time to charge/discharge before reaching v_{cont} . This causes current transients as shown in Figure 4.5.

Figure 4.5: Settling performance of the chargepump

The use of a fully-differential CP can reduce the dynamic mismatch, as the difference of v_{cont}^+ and v_{cont}^- is used to drive a fully-differential VCO. The positive ripple on one output is cancelled by an equal but opposite ripple on the other.

4.2.3 Suitability of loop-filter integration

There are two major problems with LF integration. The first one is the limitation on the size of C_2 , that can be integrated. The second problem is absolute accuracy of passive components. An issue, that receives lesser attention, is the capability of the extraction tools to successfully extract novel parasitic structures. The area consumed by an on-chip LF is roughly one-half of the total PLL-FS area. With no poly-poly capacitors available in CMOSP25, the obvious choice is to try metal-metal capacitors, in order to determine the upper limit on the size of C_2 that can be integrated in a reasonable area.

In recent years, linear fractal capacitors [56] and ways to achieve maximum capacitance [114] have been explored. The fractal capacitors utilize the vertical as well as lateral flux to achieve almost 2.3 times the capacitance per unit area compared to conventional metal-metal capacitors. Flux-capacitors put this enhancement at 4 for a certain topology. As technology dimensions shrink, and the fabrication processes become more reliable, the lateral capacitance will increase almost certainly every year with gradual improvements expected for vertical capacitance as well.

By definition, however, the fractal is a chaotic structure with no regular shape. In order to gain the fractal advantage, without using any specialized CAD tools to manage this unusual shaped structure, several free WindowsTM-based programs were downloaded from the internet, that could generate a fractal of arbitrary size. By visual inspection, pieces of different sizes were selected that offered the maximum silicon coverage in a given square area for the inter-woven metal strands. These patterns were saved as *.DXF files, a universal CAD format, and later imported in Cadence VirtuosoTM layout to form the unit fractal capacitor cells of 41 fF, 252 fF and 380 fF. Since these structures are not currently recognized as capacitors by major CAD tools, parasitic extractions had to be performed. This is depicted in Figure 4.6.

Such unit capacitors can be put together as a grid-array in a common centroid layout. Two 100 pF capacitors are fabricated for this work. The first one uses four metal layers and the second one uses all five metal layers. As shown in Figure 4.6, the appropriate layers in the unit cell are connected through vias at corners and center in order to reduce the resistance of the long metal tracks. One advantage of these capacitors is their linearity and the low bottom-plate capacitance, if the lower metal layers are not utilized. The disadvantage is the low capacitance per unit area compared to a poly-poly structure.

Figure 4.6: Fractal capacitor (concept) and a unit fractal capacitor cell

The second problem with LF integration is the absolute accuracy of on-chip passive components. This can be off by as much as 20% for poly-poly capacitors. Comments about this have already appeared in conjunction with the discussion on PFDs. A PFD with reference feedthrough at $2f_{ref}$ would be a welcome choice, if the LF is monolithic.

Noise coupling from digital portions of a larger chip necessitates that the on-chip LF be enclosed within its own guard rings. In order to satisfactorily remove unwanted spikes from the VCO input, it has also been proposed [57], that an on-chip C_1 be placed close to the VCO input. For an external LF, additional decoupling has to be provided in the VCO biasing circuitry. Otherwise, the noise coupled from the digital package, directly to

the input of the VCO, can create severe ringing. The noise coupled from the LF has a bandpass noise-TF that peaks around ω_c as shown in Figure 2.11.

Another problem that has to be considered is the possibility of unwanted modulation transferred to the VCO from the second-order RLC circuit that is formed by the capacitor C_2 , resistor R_2 and the equivalent inductance, L_{eqv} , as shown in Figure 4.7. Other sidebands might be introduced at higher frequencies due to C_1 . Hence for an external LF, C_1 has to be recalculated taking L_{eqv} into account.

Figure 4.7: Loop-filter with lumped external inductance

For a generic PLL-FS, one is more likely to encounter an external LF. This is because the passive or the active filter cannot easily be made flexible enough after fabrication to be used in generic applications. But a configurable array of rather small ripple-smoothing capacitors can be provided close to the v_{cont} input. This can provide higher attenuation of ripple, over a wide range of usable frequencies in addition to saving some cost. This discussion is more relevant for GHz range synthesizers where interconnects have to be modelled as transmission lines and the package parasitics can actually be used to improve the performance of the RF circuits, e.g., using a bond-wire as a high-Q inductance for the LC tank VCOs [112].

As the minimum feature sizes shrink for new CMOS technologies, the power requirements are also becoming smaller due to low voltage fabrication processes. If we can re-use the same presettable divider as a building block and put together a fractional-N divider, it can be used at lower frequencies, where a dynamic prescaler is either not required or is difficult to design. Some enhanced functionality can also be realized without having to build a sigma-delta modulator based fractional-N synthesizer. The state-of-the-art is always a fixed prescaler for any given technology, since it is not limited by switching delays and its power dissipation is small because of the dynamic nature of the flipflops used [7]. In our case, the advantage is re-usability and portability. The overview of the fractional-N divider is shown in Figure 4.10.

Figure 4.10: Multi-modulus divider circuit using re-usable blocks

The dividers are all programmable and are labelled as ‘M’, ‘N’ and ‘A’. The dividers ‘M’ and ‘A’ are clocked in parallel. Initially ‘N’ starts at $N+1$. When ‘A’ overflows, ‘N’ is set to divide by N instead of $N+1$ and ‘A’ is inhibited, until ‘M’ overflows, which in turn restarts the whole process. The total division ratio is, therefore, $MN + A$. The minimum achievable division ratio is $N^2 - N$, with no missing channels. ‘M’ should always be programmed to a larger number than ‘A’ to avoid unpredictable operation. The advantage of

this setup is that the modulus can be changed on the fly, e.g. from $7/8$ to $15/16$, using a simple digital circuit, alternating every time the divider output appears. The same circuit can be modified to produce $N/N+2$ or any other required ratio. The speed of this multi-modulus divider is limited by the speed of the 'N' divider and the delay in the 'LOAD' chain. This delay can easily be kept below one clock period.

As shown in Figure D.8, the dual-modulus divider along with a modulus controller can provide fractional-N division. The implicit assumption is that the spurious sidebands as a result of this fractional-N division are outside the loop-bandwidth. This restricts the fractional part, to the range 0.4 to 0.6, without requiring a spur-cancellation mechanism outlined in Figure D.9.

Hence a multi-modulus divider with a superior sideband performance can be realized at lower frequencies without having to use sigma-delta techniques or to design a low-frequency prescaler.

4.2.5 Voltage-controlled oscillator

VCOs form an integral part of the total PLL-FS. The frequency range, loop bandwidth, and ultimately the noise performance of the PLL-FS is determined primarily by the VCO. The following discussion heavily derives from previous work done at the Department of Electronics by Dr. Tadeusz Kwasniewski's students [68][69][70]. There are two broad classifications of oscillators based on the output waveform, i.e., sinusoidal and non-sinusoidal [70]. Those with a greater potential for monolithic integration are the LC-tuned, emitter-coupled multivibrator, and the multi-stage ring oscillators.

High frequency operation coupled with a wide tuning range, make the ring oscillators a good choice for integrated implementations [75]. No external components are required. The basic topology of an n -stage ring oscillator is shown in Figure 4.11.

Each stage has a propagation delay as it is loaded by the next stage and has some parasitic capacitance to ground at its output. An odd number of inverters (at least three) is required to sustain a stable oscillation in the single-ended implementation. For a differential implementation, an even number of stages can be utilized by interchanging the outputs before feeding them back to the input. Assuming a delay of τ_d per inverter stage, the frequency of oscillation is given by Equation (4.1).

$$f = \frac{1}{T} = \frac{1}{2n\tau_d} \quad (4.1)$$

Figure 4.11: n -stage ring oscillator concept

The oscillations happen as the signal travels through the ring every half period with an inversion as shown in Figure 4.12.

Figure 4.12: 3-stage ring oscillator timing diagram

Hence a frequency-dependent phase shift of 180° is present. For a negative feedback system, a phase shift of 180° is present by definition and hence the Barkhausen criterion is satisfied [27] that requires a phase shift equal to an integral multiple of 360° with a gain larger than 1 to be present. The output frequency of the VCO is given by Equation (4.2), where ω_{fr} is the minimum/free-running frequency of oscillation, K_{vco} is the VCO gain factor (in rad/s/V) and v_{cont} is the voltage at the input of the VCO.

$$\omega_{vco} = \omega_{fr} + K_{vco}v_{cont} \quad (4.2)$$

Phase noise concepts have been discussed. [See “Phase noise” on page 11]. The PN performance of ring oscillators is poor compared to LC-tuned oscillators as ring oscillators lack a frequency-selective network. Fortunately, when used within a PLL, the PN characteristics are shaped by the closed-loop TF. Specifically, the PN within the loop-bandwidth is suppressed but takes the same form as that of the free-running oscillator outside the loop-bandwidth. The humps in the spectral response near the loop-bandwidth can

Figure 4.13: Oscillator spectrums (a) free-running (b) phase-locked

be reduced by optimizing the LF parameters [68]. This points out to the need for having a large loop-bandwidth [100]. This is fundamentally limited to less than $1/10^{\text{th}}$ of f_{ref} [28], if a crystal oscillator is used. The loop-bandwidth is further restricted to $1/100^{\text{th}}$ of f_{ref} , if the reference is derived from some other source.

Various delay-cells have been proposed [27][68][69][70]. The first stage delay-cell adopted for this work is a single-ended current-starved inverter with symmetric current sources at both rails controlled by a biasing circuit [34][53]. It is followed by simple inverters in the following four stages as shown in Figure 4.14. Since there is a difference between the mobilities of the NMOS and PMOS transistors, an optimum width ratio is maintained in the ring transistors.

The ring has been designed to oscillate at twice the required frequency and the output is divided by two to get a 50% duty-cycle output [69]. This is important in clock generator applications and also results in the improvement of PN by 6 dB.

Figure 4.14: Five-stage ring oscillator core

Always using symmetric current sources might not be the best idea. Figure 4.15 (a) depicts that by optimizing the size of the PMOS transistor M1, connected to the *PBIAS* node, the linearity of the K_{vco} characteristics is improved. The duty-cycle is less than optimum for a better part of the range but it can be forced to exactly 50% after post-division by 2. The non-linearity in K_{vco} is, in general, not acceptable. Figure 4.15 (b) depicts the influence of a PMOS bias transistor in every delay-cell. The maximum operating frequency is reduced by a factor of two, but the total current consumption is reduced by 30% along with the introduction of severe non-linearities. Moreover, the signal swings at Node

B through Node E in Figure 4.14 are reduced to 0.5-1.6 V range under TYPICAL conditions. Node A swings at 0.6-1.5 V as before. The biasing circuitry has an extra ripple filtering capacitor for reducing disturbances that might be picked up from the package or the substrate and is not shown. The size of this capacitor is determined using simulations done at various points across the tuning range. The only disadvantage of a capacitor in the biasing circuitry is that the VCO becomes a little slow in responding to sudden changes in v_{cont} . But the advantage is that a VCO that resists a change in frequency because of sudden changes in v_{cont} , also resists a similar change due to noise. Four VCOs with the general topology shown in Figure 4.14 are designed, fabricated and tested with the same biasing circuitry but different ring transistor sizes. The PN can be further reduced by putting on-chip inductors in series with transistor M1 and other PMOS biasing transistors. This serves to reduce supply-induced jitter.

Phase noise simulation problems are discussed later in Chapter 4 and the VCO test results appear in Chapter 5.

Figure 4.15: Linearizing and optimizing the VCO characteristics

TABLE 4.1: VCO1-VCO4 major specifications

Name	Size of the ring PMOS Wp/Lp (μm)	Size of the ring NMOS Wn/Ln (μm)	Power (mW) @ Minimum undivided frequency output (MHz)	Power (mW) @ Maximum undivided frequency (MHz) including the bias, buffer and divide-by-2 flipflop	Simulated phase noise (dBc/Hz) @ 100 kHz of the divided output, $v_{cont}=1.5$ V
VCO1	8.5/0.5	4.2/0.5	0.99 mW @ 46.5 MHz	3.31 mW @ 539.1 MHz	-105.3 dBc/Hz
VCO2	8.5/0.4	4.2/0.4	1.10 mW @ 46.9 MHz	3.93 mW @ 680.4 MHz	-107.0 dBc/Hz
VCO3	8.5/0.35	4.2/0.35	1.20 mW @ 46.9 MHz	4.30 mW @ 753.5 MHz	-106.8 dBc/Hz
VCO4	3.0/0.8	1.5/0.8	0.58 mW @ 63.2 MHz	1.82 mW @ 311.2 MHz	-103.8 dBc/Hz

4.2.6 Rail-to-rail VCO (VCO5)

The reduction of power supply voltage with upcoming CMOS technologies puts great pressure on the design of the PLL-FS. Using a V-I converter with either NMOS or PMOS as the only driving transistor to which v_{cont} is connected reduces the operating voltage range for the VCO. Corner simulations indicate a further reduction in this range due to the digital nature of the larger chip that houses the PLL-FS and the VCO. This increases the K_{vco} and degrades the PN performance of the PLL-FS. In this section, a variation based on the rail-to-rail bias circuit design is being presented that has been adopted from [73]. The new VCO has some advantages. It can utilize the full voltage range if a compatible CP is available. The final Voltage-to-Frequency (VTF) characteristics can be easily shifted up or down to counteract any variations due to the process corners. The PN can improve for the same VCO architecture as it is biased at a higher operating current. The only trade-off is the extra power dissipation. Circuit complexity and cost remain minimal, if the current sources are monolithic.

The VCO starts oscillating when v_{cont} goes above the threshold of the NMOS transistor or below that of the PMOS transistor as current is established in the current-starved inverters. The typical characteristics are shown in Figure 4.16.

Figure 4.16: Voltage-to-current converter using (a) PMOS (b) NMOS

The rail-to-rail bias technique [73] uses a PMOS and an NMOS transistor to implement a V-I converter that sums the two currents as shown in Figure 4.17. A slightly modified ring is used for this VCO compared to the one used for VCO1-VCO4.

Figure 4.17: Complementary V-I converter [73]

For testing purposes the resistors depicted as PRES, NRES and MAINRES are external. Appropriate sizes of transistors M3 and M4 can be chosen for the required current level and optimized to make the Voltage-to-Frequency (VTF) characteristics more linear. Cascoded current mirrors and sources can replace simple ones. The resistors can be replaced with switchable current branches controlled by transmission gates to control the VTF characteristics of the VCO. The TYPICAL results in Figure 4.18 show the advantage of using a rail-to-rail VCO. Further simulations and results appear in Chapter 5.

Figure 4.18: Advantage of using a rail-to-rail VCO

4.2.7 Bandgap reference

Bandgap references (BG) appear frequently in analog circuits. They provide a reference (V or I) that is independent of the power supply and process variations and exhibits a well-defined dependence on the temperature. Most process variables depend on the temperature but not only on it. If the circuit is temperature-independent, it is process-independent to a certain extent as well.

The predominant method for realizing a zero temperature-coefficient (TC) makes use of the negative-TC characteristics of the bipolar transistor's base-emitter voltage V_{BE} and the positive-TC achieved using a “Proportional-To-Absolute-Temperature” or a PTAT device. The difference between the base-emitter voltages of two bipolar transistors carrying different currents is a PTAT device [62]. A good discussion on BGs can be found in [13][27] and an overview is shown in Figure 4.19.

Figure 4.19: Architectural overview of the bandgap reference

The BG was not integrated with any fabricated PLL-FS, but was built and tested separately using the Analytical Probe Station (APS). The major problems with such references in a digital CMOS technology are the lack of an extraction capability and the weaker performance of vertical-PNP parasitic structures in an n-well CMOS process. Vertical-NPN is the equivalent type in a p-well process that is less commonly available. The start-up circuit is conspicuously absent from Figure 4.19, and is provided inside the library opamp used in this BG. The opamp determines the settling behavior of the BG as well.

4.2.8 Lock-detection circuit

A simple way to detect and declare a phase-locked condition is shown in Figure 4.20. The operation of the circuit is simple. For a phase-locked condition, the ‘UP’ and ‘DN’ pulses always have opposite logical value within a certain delay tolerance. Consequently, the pulses at the output of the XOR gate are of minimum width and are filtered by the pulse-filtering capacitor, realized using an NMOS and a PMOS transistor. There is no limitation on the architecture of this capacitor. The only requirements are:

- Sufficiently larger than the minimum required value to filter the smeared out pulses from the PFD due to PVT variations in the phase-locked state.
- Able to filter slightly wider pulses at the extremes of the operating voltage range to account for the DC mismatch in I_p , if any.

The need for several long closed-loop transient simulations at the extremes of the voltage range cannot be circumvented here. After the pulse-filter, the signal is cleaned up using two inverters thus providing a ‘LOCK’ signal. A similar ‘LOCK’ signal can also be derived from the *INSTLOCK* signal, but care has to be taken so as not to load the *INSTLOCK* itself, due to the pulse-filter capacitors. Otherwise, its intended function inside the

APFD can be affected. Such a derivation would also include the cycle-slip information as it is inherently provided by the APFD, by way of the *INSTLOCK* signal.

Figure 4.20: Lock-Detection Circuit (LDC) on a fabricated chip

The active-high ‘ENABLE’ signal (not shown here) provides the opportunity to globally enable or disable the entire LDC. Only the ‘LOCK’ signal is made externally available at all times. This can be gated through the ‘PD’ signal so that it is at a logical ‘0’ while the system is powered down. The frequency of the ‘LOCK’ signal provides the out-of-lock information that can be useful for adaptive-PLL applications. The ‘PD’ signal can power the entire circuit down. If a short pulse is applied to the ‘PD’ input, then the divider also reloads the count and re-initializes the lock-detection process. The ‘CLEANLOCK’ is also cleared in a ‘PD’ or a system-wide reset event that can be triggered elsewhere and is not shown.

If the ‘UP’ and ‘DN’ signals shown in Figure 4.20 are indeed in lock, then the ‘LOCK’ signal is at a logical ‘1’, and the same reusable divider (with perhaps a smaller number of flipflops) starts counting the ‘REFIN’ pulses. The key point is to wait for a certain time interval, before declaring a more stable indication of the lock, i.e., the ‘CLEANLOCK’ signal. The inputs to the counter can be derived from the Serial-to-Parallel

converter (SPC) that is described later. The inputs can also be hard-wired or provided as options in the top-metal layer depending on the application. In a digital system, they can also be derived from a data bus.

As a design variation, an array of selectable pulse-filtering capacitors can be integrated. Their size should be some reasonable value that is much smaller than the required size to provide fine steps for the detection of small phase differences. Such capacitors can be enabled or disabled with available signals or top-metal shorts, to provide enhanced functionality and reliable testability.

4.2.9 Acquisition-aiding circuitry

The PLL-FS starts up with zero voltage at the v_{cont} input. It should be able to achieve phase-lock itself over the entire operating range. If the PLL-FS is not self-acquiring, then an acquisition-aiding circuit is employed improve its acquisition performance.

The methodology described here is a patented technique implemented in a BiCMOS technology [46]. The system-level details were available, so an acquisition circuit based on the PLL-FS architecture was implemented as shown in Figure 4.21. This circuit is used as a demonstration to verify the feasibility of the patented method for CMOS technologies. The basic idea is to reduce the LF resistor R_2 , thereby increasing ω_n , but keeping ζ constant. The consequent drop in the PM is compensated by shifting the entire open-loop phase characteristics to a higher frequency. This is done by quadrupling the CP current. An improvement by a factor of around two has been reported in the same work. As described in Chapter 3, the changing of the LF parameters is not necessary in order to ensure stability, although it does help. The total acquisition time is reduced by a factor of

two due to the poor damping at higher N values. This is because the whole argument is centered around maintaining the PM by changing the LF values during acquisition.

Figure 4.21: Acquisition-aiding circuit on a fabricated chip

In conjunction with the LDC described earlier, a lock-assisting circuit was designed as shown in Figure 4.21. The ‘LATCHEN’ signal comes from the SPC and signals the start of the acquisition process. The duration of this signal can be wider than the acquisition time itself. A “ONE PULSE PER PUSH” (OPP) circuit has been borrowed from [58], that produces one pulse as this event happens. The ‘IPUMP4X’ signal becomes high and enables three additional identical branches in the CP raising its current to $40\ \mu\text{A}$. Also, R_2 is bypassed using an open-drain NMOS transistor at the same time. The output resistance of this transistor is kept low so that a parallel combination with $R_2/2$ results in an effective bypass. As the ‘CLEANLOCK’ signal becomes available from the LDC, the second OPP circuit turns off this functionality restoring the PLL-FS to its normal mode of operation.

4.2.10 Interface circuitry

The PLL-FS requires inputs for the RD and FBD in addition to some configuration inputs depending on the application. As part of a large mixed-signal chip, these inputs are available in parallel from the digital section. As a stand-alone system, however, the inputs cannot be provided in parallel as the design becomes pad-limited and inefficient in terms of area. An SPC can reduce the number of pads to three for any number of required inputs. This technique is commercially used [60]. A simple SPC can be realized using a cascade of the basic cells shown in Figure 4.22.

Figure 4.22: Serial-to-parallel converter (basic cell)

The data is clocked serially using the ‘SERIALCLK’ input. After all the ‘SHIFT STAGE’ latches contain data at their inputs, a positive transition at the ‘LATCH’ signal latches the ‘DATA’ to the respective divider inputs or other parts of the chip. The speed of this SPC is very high for submicron CMOS technologies and its power dissipation becomes a concern only if a fast-hopping FS has to be tested.

4.3 Simulation techniques

Simulation cannot replace analysis. However, it is an indispensable vehicle for learning and understanding, as analysis can become difficult especially in the case of a PLL-FS. To simulate the circuit performance reliably, the PVT corners for the CMOS25 process are shown in Table 4.2. Military specifications may require other process corners.

TABLE 4.2: Process corners

Variable	Process corner name		
	FAST	TYPICAL	SLOW
Process model	FAST	TYPICAL	SLOW
Supply voltage	2.75V	2.5 V	2.25V
Temperature (junction)	120 °C	70 °C	-40 °C

These corners are sufficient for simulating digital circuits. For analog design, every parameter of interest has a ‘WORST’, ‘BEST’ or ‘TYPICAL’ value. For instance, the bandwidth of an opamp might be the ‘BEST’ (i.e. largest bandwidth) with the FAST process model but at lower temperatures. So the FAST corner might not be the BEST corner for opamp bandwidth but it could be the BEST corner for the opamp’s slew rate.

4.3.1 General simulations

Every component has to be simulated to determine its performance in the case of various events and operating conditions. In addition, specific simulations might have to be run on every component.

- Functional simulations at process corners to verify correct operation.
- Power dissipation simulations in the normal and PD modes.
- Start-up simulations to make sure that no additional stimuli are required.

- Verification of the PD operation and consequently returning to the normal mode.
- Use of the PD signal as the reset signal.
- Frequency response of the component, if applicable.
- Noise/PN simulations

4.3.2 PFD

Most of the information about PFDs has appeared in Chapter 3. The PFD should be driven with signals having comparable slew-rates to reduce the deadzone. The rise-time and the fall-time of the divider output is optimized as it eventually plays a major role in the power dissipation of the PFD. The effect of this rise-time and fall-time is further reduced by two inverters at each of the PFD inputs.

4.3.3 Loop-filter

Since the LF is external, the major drawbacks are the increased parasitics and the available values of the discrete components. If the LF is monolithic, however, then it has to be simulated not only over the process corners but also the BEST, TYPICAL and WORST corners as determined for its components. The process corners might not be able to fully characterize the best-case and the worst-case LF component values, but they are usually sufficient.

4.3.4 Divider

The necessary post-layout simulations are the functional simulations at the highest operating frequency. The division ratio should be set at minimum and maximum for this purpose. The comprehensive set of simulations for a digital divider can take a long time. Measurement results can be achieved more easily for the divider. Having several on-chip dividers with different division ratios is not a bad idea as it expedites testing.

The power in a static digital divider is given by Equation (4.3) [55], where ‘ C ’ = equivalent load capacitance, ‘ V ’ = supply voltage and ‘ f ’ = operating frequency.

$$P_{divider} = CV^2 f \quad (4.3)$$

4.3.5 VCO

There are a number of issues associated with the VCO PN simulations. The Periodic Steady State (PSS) tool within SpectreS™ is used to simulate the post-layout PN for the VCOs at FAST, SLOW and TYPICAL corners.

The simulation parameters (reltol, vabstol, iabstol) are set at (1e-3, 1e-6, 1e-12) respectively. Changing the parameter iabstol from 1e-12 to 1e-9 improves convergence but provides a value of PN that appears improved by almost 6 dBc/Hz. The stabilization time parameter (defined as ‘tstab’) by SpectreS simulator is chosen so that the initial transients in the oscillator have settled. The frequency of the oscillator is noted after a sufficiently long transient simulation and provided as the initial guess for the fundamental (beat) frequency. This results in a shorter PSS analysis. The ‘traonly’ algorithm is used and accuracy presets have been chosen as ‘moderate’ as they aid convergence. The PN of the divide-by-2 signal is simulated. Another problem is that if a sinusoidal source is introduced [71], let’s say at 10 MHz, then this should be an integral multiple of the initial beat-note frequency provided to the simulator. This results in exorbitant simulation times and is best left until the measurement stage. The final comment is that the PN should be simulated over a range extending one decade above and below the loop bandwidth. In our case, the simulations are performed in the frequency range 10 kHz - 10 MHz. The input voltage, v_{cont} , is set to 1.5 V, that is typically half way down the usable voltage range of the VCO.

The conclusion is that the PN simulation can only be used as an initial guess. The other important simulations are the corner simulations for the VTF characteristics and the power dissipation. More information about some PN simulation bottlenecks can be found in [119].

4.3.6 Bandgap reference

Post-layout extraction could not be performed due to the inability of the extractor tool to recognize vertical-PNP transistors. There were no SpectreS™ simulation models for a vertical-PNP transistor. HSPICE™ models were available for the TYPICAL case only. Since digital CMOS processes are not usually optimized for bipolar parasitic extractions, this effort remains inconclusive until the measurement stage. All the simulation results have been acquired by running 70 μs long simulations and recording the stable voltage at the end. DC simulations proved inaccurate in this case.

The use of different sized vertical-PNP transistors is not recommended in a CMOS reference. The vertical-PNP parameters are more prone to deviation for two reasons. First, they are dependent on the doping profile of the n-well, that is not as well-controlled as the mask-generation process. Secondly, the extended characterization data on vertical-PNP transistors is often not available due to commercial reasons. It is useful to provide fine-stepping top-metal jumper options for the resistor R_2 (Figure 4.19) to tune the final BG voltage, in the absence of an extraction capability. However, this technique is not feasible for mass production.

The settling performance of the BG can be evaluated by applying a pulse through a capacitor at the output [27]. The simulation parameters depend on the application.

Figure 4.23: Bandgap reference transient settling

Simulations and measurements for the BG appear in Chapter 5.

4.3.7 Lock-detection circuit

The lock detection is best tested in the closed-loop configuration but the functionality of the digital circuitry can be tested routinely. The pulse-filter capacitors in the LDC are simulated over process corners to verify correct operation. While simulating the LDC, a low-frequency modulated signal source can be used for more realistic but shorter simulations. The comprehensive simulations are done in conjunction with the acquisition testing.

4.3.8 Acquisition-aiding circuitry

The simulation times can easily become prohibitive for routine PLL-FS acquisition scenarios. Depending on the available computing power, one has to set the simulation tolerance parameters appropriately.

At least two closed-loop simulations are required. The first, with the acquisition aiding circuitry turned off, and the second, with the circuitry turned on. For a boundary simulation, all inputs of the FBD can be switched from a logical '1' to a logical '0' using a low-frequency pulse. Some shortcuts that can be used initially to verify functionality and reduce simulation times are the use of ideal current sources in the CP, a higher reference frequency, use of behavioral models and relaxed simulation parameters.

4.3.9 Interface circuitry

For easier programming, the format of the input serial-data stream has to be planned. An illustration is shown in Figure 4.24. This also means that while the layout of the dividers is in progress, an effort has to be made to make it as compatible as possible with the layout of the SPC. A computer running a customized software routine can come to the rescue but the need for a plan is evident here. A useful thing to do is to provide a

sufficiently long sequence of zeros before by the real data so that the ambiguity in this data transfer operation can be reduced, when the ‘LATCH’ signal is applied.

Figure 4.24: Test-planning for supplying serial input data

4.4 Summary

This chapter presented the circuit-level implementation of the PLL-FS components. Actual schematics and layouts appear in Appendix C. A brief account of some useful simulation techniques was also presented. The simulations required to ensure proper functionality of an integrated PLL-FS were mentioned.

Chapter 5 presents the measured results alongside of the relevant post-layout simulation results for the components and the fabricated chips.

Test Setups and Performance Evaluation

5.1 Chapter overview

This chapter presents a road-map of the fabricated chips, a list of test equipment used, test setups, the post-layout results and the measured results for individual components and the complete PLL-FS. Problems encountered during testing are also mentioned.

5.2 Road-map of the fabricated chips

Table 5.1 shows the major details of the fabricated chips. Details of the PCBs used as test fixtures can be found in Appendix A.

TABLE 5.1: Fabricated chips

Design name	Technology	Area/package type	Year	Test fixture(s)
ICECUIR0	CMOSP25	2.4 mm * 2.4 mm (CQFP44)	Sept 1999	PCB-ICECUIR0
ICFCUIR2	CMOSP18	1389 μ m * 473 μ m (loose dice)	Feb 2000	Analytical Probe Station (APS)
ICECUIR1	CMOSP25	2.4 mm * 2.4 mm (CQFP 44)	May 2000	PCB-ICECUIR1 / PCB-PLLFS
ICECUIR2	CMOSP25	2.8 mm * 2.4 mm (loose dice)	Apr 2001	APS, Modular PCBs

5.2.1 ICECUIR0

This was the first of the fabricated chips with several problems (see B.1 on page 160 for details). The problems encountered are being listed here for the reference of the first-time designer. These are by no means comprehensive or all-inclusive.

- Default digital libraries with gate strengths of 1x, 2x and 4x were present with no possibility of parameter-passing or assignable supplies.

The standard library cells, primarily realized using metal-3, used a generous supply of vias and were suited for digital use only. For this work, a library of configurable and custom-designed gates was realized, primarily in metal-1, with a minimum number of vias. (i.e. after the failure of ICECUIR0). Parameters could be passed and power supplies were assignable to entire blocks (digital, analog and buffer). Therefore, the same library components could be used throughout the whole chip.

Figure 5.1: Configurable NAND gate example

- Output pads were hooked up incorrectly. These pads can only be simulated on the extracted level and did not have an associated schematic. User data on these pads was sketchy as they were meant to be used by automatic synthesis tools.
- The top-level schematic never started out with the layout intricacies in mind and the layout was flattened at the end resulting in many problems. Layout vs. Schematic (LVS) was run on the individual components, but not on the finished chip.

- Parallel divider inputs made the design pad-limited and area-inefficient. The floor-plan was severely constrained due to the FBD and RD inputs coming in from all sides. Digital and analog sections were not well-isolated. Separate pads for analog and digital supplies were not available, as all of the package pins were already assigned.
- Most of the Antenna Errors (AE) were removed but this concept was not well understood at that time. During the early days of CMOS25 and CMOS18, the designs with a certain number of AE were accepted for fabrication.

5.2.2 ICECUIR1

All of the above oversights and deficiencies were removed from ICECUIR1 (see B.2 on page 163 for details). The LVS tool reported complete correspondence. Post-layout simulations were performed on all the components, although the full-chip simulations were done at the schematic level. A separately testable PFD, divider, TSPC flipflop and VCO1-VCO4 were present along with an SPC. A full PLL-FS along with an LDC and acquisition-aiding circuitry was also present. Output buffers were used on all digital outputs for recording sharp pulses, e.g. on the PFD. Two fractal capacitors 100 pF each were also present, along with the SHORT and OPEN de-embedding pads. Due to the previous experience with digital pads, simple analog bonding pads were used (with no ESD protection). As the test results from the first batch of ICECUIR1 that was tested using PCB-ICECUIR1 were inconclusive, five loose dice were sent back for re-bonding. There were only two possibilities. Since all the components cannot fail and the PFD, VCO2 and VCO4 were found operational on 2/5 chips, it was assumed that there was either an ESD problem or some fault with the PCB-ICECUIR1. Since all the inputs (even unconnected ones) were found shorted, with 100 Ω or less measurable with a DC multimeter to ground, it was thought to be an ESD problem. The confluence of PCB-ICECUIR1 supply planes was also thought of as the culprit, but then it was ruled out. The final results were incon-

clusive as to whether the PCB-ICECUIR1 or ESD discharge was the problematic area. Another PCB was populated, but did not prove useful. The chips died before they could be tested.

The re-bonded batch of five chips (originally loose dice) was tested using a less complicated PCB-PLLFS. The first populated board failed for unknown reasons. The first chip had several messed up bond-wires. The second one had a missing bond-wire. The third, fourth and the fifth chips from this re-bonded batch worked on a newly populated PCB-PLLFS. The PCB-PLLFS had series resistors of 50 k Ω - 100 k Ω on all critical bias and data inputs. The PLL-FS operation was partially successful as serial data could not be supplied and because the VCO2 had a bad PN found during stand-alone testing on the ICECUIR2. The problem of the lack of a data-path was traced back to the missing ground connection on one of the buffers joining the ‘SDATA’ input on ICECUIR1 to the SPC. The chip locks to $4f_{ref}$ on start-up and the reset button on the ‘Reset PCB’ brings the synthesizer back to the $2f_{ref}$ mode. The actual reason for this start-up behavior is unknown. However, by supplying a varying f_{ref} , it has been verified that v_{cont} actually corresponds to the correct frequency at the output. Hence, the chip is functional but not controllable.

5.2.3 ICECUIR2

This chip was a combination of separately testable components compatible with the APS mounted 8-pin probe assembly. It was fabricated after the failure of the first batch of ICECUIR1 chips. This was done to characterize the individual components and to rule out the possibility of a non-operational component. Table 5.2 lists the contents on each of the separate APS-compatible structures (see B.3 on page 166 for details).

TABLE 5.2: Details of ICECUIR2 chip contents

Structure name	Details of circuits present	Area (dimensions in μm)
probe1	PFD-NAND, CP 1x, $I_p = 10 \mu\text{A}$, external bias	468 * 1205

TABLE 5.2: Details of ICECUIR2 chip contents

Structure name	Details of circuits present	Area (dimensions in μm)
probe2	PFD-NAND, CP 4x, $I_p = 40 \mu\text{A}$, external bias	468 * 1205
probe3	PFD-NAND, CP 1x $I_p = 10 \mu\text{A}$, with an on-chip BG	607 * 1210
probe4	Fractional-N divider driven using the SPC	545 * 1210
probe5	SPC, 7-bit divider driven using the SPC	534 * 1210
probe6	Divider with fixed inputs; $N = 128, 64, 32, 16$	595 * 1210
probe7	Divider with fixed inputs; $N = 8, 4, 2, 1$	610 * 1210
probe8	Fixed fractional-N, to test the 25 kHz f_{ref} scenario	470 * 1220
probe9	VCO1-VCO4	560 * 1210
probe10	VCO5, to test the rail-to-rail operation	590 * 1173
ICECUIR2	A total of 10 APS-compatible structures	3000 * 2600

5.2.4 ICFCUIR2

This chip was fabricated for comparison of results with CMOSP25 and gaining experience with the, then new, CMOSP18 process. Positive results were obtained, although the chip had 75000 AE at tape-out. This chip housed a PFD-NOR and a digital divider. The clock input was shared between the PFD-NOR and the divider. The divider on ICFCUIR2 was tested using the APS. An on-chip ripple counter was used to increment the divider inputs during testing, thus requiring only one low-frequency probing pad. Antenna Errors were reduced by using p-type diffusion attached to critical nets. The dice were found to be functional, but not very stable, and care had to be exercised during their testing (see B.13 on page 176 for details).

5.3 Test equipment

The instruments used for testing, with their aliased names, appear in Table 5.3.

TABLE 5.3: List of the test equipment

#	Name and function of the test equipment	Alias ^a
1	Summit 9000 - Cascade Microtech - Analytical IC Probe Station	APS
2	HP8131A 500 MHz Pulse Generator	PG
3	SME06 Rhode and Schwarz, Signal generator 5 kHz-6 GHz	SG
4	HP53132A 225 MHz Counter	CO
5	Spectrum Analyzer HP8593E 9 kHz - 26.5 GHz	SA1
6	Spectrum Analyzer HP8564E 30 Hz - 40 GHz with PN option	SA2
7	HP80000 Data Generator 2 GHz	DG
8	Oscilloscope Tektronix TDS684B 4-Channel 1 GHz- 5 Gsamples/s	OS
9	Power Supply Keithley Model 2400 Series Source Meter	PS1
10	Power Supply HP3630A 0-6V/2.5A, 20V/0.5A	PS2
11	Agilent 8720ES 50 MHz - 20 GHz S-Parameter Network Analyzer	SPNA
12	HP5372A Frequency and Time Interval Analyzer	FTIA

a. Except for the APS, these aliases do not appear in the abbreviations list at the beginning of the thesis and are local to Chapter 5 only.

Along with the APS, 3-pin and 8-pin probes were used as shown in the various layout diagrams in Appendix B. The APS is situated inside a wire-mesh Faraday's cage to improve measurement accuracy by reducing extraneous noise. PS1 was used to set precision voltages and currents and PS2 was used to supply power to non-critical test setups. Data can be captured from SPNA, OS and DG using a floppy diskette. Phase Noise has been measured using the HP-8564E PN-firmware option. The HP3048 PN-measurement

system is a more broadband and a sensitive method. Details on how to measure PN can be found in appendix E of [70].

5.4 Printed circuit boards

The details of the PCBs designed can be found in Appendix A. Two key things should be noted in conjunction with the PCB design.

- Professional help produces better results in a shorter time.
- Modular approach saves time as the same PCBs can be re-used.

5.5 Test setups

Test setups are briefly described and are being repeated from various references for convenience only.

5.5.1 Monitoring high-frequency signals off-chip

In order to monitor a high-frequency signal off-chip, it has to be driven using an on-chip buffer. It is possible to divide a high-frequency signal on-chip before measuring it

Figure 5.2: All-NMOS source-follower as an output buffer

off-chip. This improves the PN of the signal, whilst the divider adds some noise of its own. This cannot be done if the short pulses ($t_{period} < 1$ ns) have to be monitored and processed as such, e.g. in the case of a PFD. An NMOS source-follower circuit has been used [7][70] to provide sufficient current to an off-chip RF inverting amplifier. The buffer has its own power supply. Two NMOS transistors have been used as the presence of a large n-well, housing a PMOS transistor, can cause latch-up [70].

The design of the NMOS source-follower buffer should take into account the chip and package parasitics that it has to drive. Typical values of bond-pad capacitance are in the range of 1.5 pF-3 pF. The inductance of the bond-wire depends on its length and a typical value is 1.5 nH. The pin capacitance for a CQFP44 package is around 1 pF. If a PCB-mounted socket is employed to facilitate replacement of dead chips, 1 pF can be added to the above. The inductance of the PCB track depends on the thickness of copper used on the PCB. This estimation is more relevant for GHz range PLL-FS.

5.5.2 Loop-filter

Figure 5.3 shows the ‘Filter PCB’ usage. During simulation, it is trivial to change

Figure 5.3: (a) Filter PCB usage (b) Fractal capacitor test setup

the LF parameters. On a PCB however, the gold-plated component pads deteriorate after a few soldering attempts. For added flexibility during testing, a ‘Filter PCB’ was designed

and fitted with gold-plated SMA connectors. Since several of these boards were available, the LF could be changed by simply changing the PCB. The final testing can be done using a fixed and well-grounded LF close to the package pin.

5.5.3 PFD

The PFD test setup is shown in Figure 5.4. The deadzone can be measured by adding the active-low ‘UP’ and the active-high ‘DN’ pulses with each other and sweeping the phase difference across zero degrees, while monitoring the average output voltage. Ideally, this is a closed-loop measurement. Functional measurements can be made by supplying the inputs using the PG, and monitoring the signals on the OS. The PG has a dual 50 Ω output with the possibility of duty-cycle, amplitude, delay and frequency adjustments.

Comments

- The on-chip buffers are powered using a separate 2.5 V supply.
- Appropriate cables should be used if the DUT is mounted on the APS.
- IO-Panel PCB is used to power the RF amplifiers and the on-chip buffers as shown in Appendix A.

Figure 5.4: PFD test setup

5.5.4 Divider

The characterization of the integer-N and fractional-N dividers, requires the test setup shown in Figure 5.5. The concept is the same as presented in [7].

Comments

- The on-chip buffers are powered using a separate 2.5 V supply.
- Appropriate cables should be used if the DUT is mounted on the APS.
- Spectrum Analyzer and Oscilloscope can be connected simultaneously only if an RF-splitter is used.
- IO-Panel PCB is used to power the RF amplifiers and the on-chip buffers.
- HP80000 drives the SPC when required.
- DC voltmeter is used to measure the self-oscillation voltage and monitor vdd during parametric testing.

Figure 5.5: Divider test setup

5.5.5 VCO

The VCO test setup has been mainly derived from [69][70][71] and is shown in Figure 5.6. PS1 is a versatile instrument with pre-programmed stimuli, General Purpose Instrument Bus (GPIB) interface, and precision current measurement capability.

Comments

- The on-chip buffers are powered using a separate 2.5 V supply.
- Appropriate cables should be used if the DUT is mounted on the APS.
- The IO-panel PCB powers the RF amplifiers, on-chip buffers and the Bias-Tee.
- Spectrum Analyzer and Oscilloscope can be connected simultaneously only if an RF-splitter is used.
- 'Bias PCB' uses a battery input in this case to get a clean VCO control voltage.
- DC Voltmeter is used to monitor the control voltage and the supply voltage during parametric testing

Figure 5.6: VCO test setup

5.5.6 Bandgap reference

The BG test setup requires a power supply and two DC voltmeters. A clean battery-powered supply can be used initially to measure accurate output. Temperature related measurements are not possible at the Carleton University as the temperature-controlled chamber is not available for the APS assembly. However, a heat-gun can be used along with a laboratory thermometer for some coarse measurements. A low-frequency pulse-train can be injected to measure the transient settling performance of the bandgap.

Comments

- The supply can be modulated as shown in the VCO test setup to measure BG's spur performance.
- Short cables should be used if the DUT is mounted on the APS.
- SA2 and PG should not be connected simultaneously in order to avoid damage to SA2.
- 'Bias PCB' uses a battery input to get a clean supply voltage.
- The PG is used to measure the transient settling along with the OS.

Figure 5.7: Bandgap reference test setup

5.5.7 Detection of lock and measurement of acquisition time

The lock detection performance of the PLL-FS is tested with a modulation-domain analyzer similar to the FTIA. The DG is used to switch once or continuously between two desired channels. The frequency acquisition can be directly studied depending on the arming mode of the FTIA. Using the OS, the phase and frequency errors at phase-lock cannot be well-resolved, but continuous switching between two channels can give a good estimate of acquisition time.

Figure 5.8: Lock detection and acquisition time test setup

5.6 *Post-layout simulations and measurement results*

The results are presented in this section for the components and for the full PLL-FS. The measurement results pertaining to ICFCUIR2 are being skipped for reasons of brevity. The PFD-NOR and the divider on ICFCUIR2 are functional, however.

5.6.1 *PFD*

The measurement results for the PFD-NAND at 100 MHz are shown in Figure 5.9. The pulses shown are all inverted and are (from top to bottom) ‘UP’, ‘DN’, ‘REFIN’, ‘OSCIN’ respectively as labelled in Figure C.1. The pulses have been smeared out because of the delays in the on-chip buffer, SMA cables, and the RF amplifier PCB. The results are shown in the following order in Figure 5.9:

- (a) No phase difference - 50% duty cycle
- (b) No phase difference - different duty cycles
- (c) ‘REFIN’ leading ‘OSCIN’
- (d) ‘OSCIN’ leading ‘REFIN’
- (e) ‘REFIN’ at twice the frequency of ‘OSCIN’
- (f) ‘OSCIN’ at twice the frequency of ‘REFIN’

It can be seen that the duty-cycle of the ‘UP’ and the ‘DN’ outputs is 50% for twice the frequency difference between the inputs. This translates to a longer pull-in time for large initial frequency differences. The deadzone has been indirectly measured at 100 ps by taking the difference of the active pulse widths while sweeping the input phase difference in steps of 5 ps. The measurement was not conclusive because of the smeared out signals. A better way to find the deadzone can be to monitor another ‘LOCK’ signal without the pulse-filter capacitors and running a spectral analysis on the same during closed-loop operation, while sweeping the input phase difference.

Figure 5.9: PFD-NAND functional waveforms at 100 MHz

5.6.2 Loop-filter and fractal capacitors

The LF is external, so simulation results do not apply as such. The results are presented in this section for the measurements done on the fractal capacitors using the APS.

First the SPNA was calibrated using the CS-5 calibration substrate for ‘OPEN’, ‘SHORT’ and ‘LOAD’ conditions. Then, four readings were taken off every available die for ‘SHORT’, ‘OPEN’, ‘4-layer’ and ‘5-layer’ capacitor. These readings were de-embedded by a two-step method using the Agilent ADSTTM tool. For more accuracy, a three-step [115], or a four-step [118] method can also be used. Other references on high-frequency measurements are [116][117].

The results are inconclusive on these measurements. The reason is that there were five loose dice available earlier. Later, these were sent for re-bonding after the failure of ICECUIR1. The Cascade microwave probes do not have a profile that can allow direct probing on packaged chips. The original packages were cut open and measurements were made on the dice thus obtained. It is speculated that due to the shocks during this cutting procedure, the lattice structure does not hold very well. Some of the capacitors do behave as capacitors but exact values could not be measured. Figure 5.10 shows the $S(1,1)$ for the 5-layer fractal capacitor that is yet to be de-embedded.

Figure 5.10: $S(1,1)$ measured on the 5-layer capacitor

5.6.3 Divider

The comprehensive simulation and testing of a programmable divider can take a long time. On ‘probe6’ and ‘probe7’ on ICECUIR2 (shown in section B.8 on page 171 and section B.9 on page 172 respectively), enough redundancy is present to enable faster testing with the OS. It should be noted that static dividers work from DC up to a maximum frequency whereas dynamic prescalars have a minimum and maximum range and other amplitude-dependent characteristics [7]. N is the feedback division ratio and the divider divides by $N+2$ because of its architecture. Some measured results appear in Figure 5.11 and Figure 5.12.

Figure 5.11: Feedback divider measured results

The fractional-N divider has been tested on ‘probe4’ and ‘probe8’ on ICECUIR2 (shown in section B.6 on page 169 and section B.10 on page 173 respectively). It operates up to a maximum frequency of 640 MHz and, therefore, can be used in the target design and also in the networking ICs that typically require 622 MHz operation. The functional test results are shown in Figure 5.13.

Figure 5.12: Feedback divider measured results (continued)

Figure 5.13: Fractional-N divider functional test results

5.6.4 Post-scalar

The post-scalar was tested on ‘probe6’ at pin ‘FOUT65’ on ICECUIR2 (see section B.8 on page 171). It works up to a maximum frequency of 1.6 GHz (divide-by-8 operation) as shown in Figure 5.14 (a).

Figure 5.14: Post-scalar (a) divide-by-8 (b) power consumption

5.6.5 VCO1-VCO5

The results of the simulations performed on and the measurement results obtained for VCO1-VCO4 are presented next in the following order:

- (a) Post-layout corner simulations for the PN at $v_{cont} = 1.5$ V
- (b) Measured phase noise at $v_{cont} = 1.5$ V
- (c) Post-layout corner simulations for the VTF characteristics
- (d) Measured VTF characteristics with the supply voltage as parameter
- (e) Post-layout corner simulations for power consumption
- (f) Oscilloscope trace for the VCO waveform at maximum frequency
- (g) PSD of the VCO without modulation on the power supply
- (h) PSD of the VCO with modulation on the power supply

Thereafter, a data table summarizes the measured results for each VCO.

(a)

(b)

(c)

(d)

(e)

(f)

Figure 5.15: VCO1 simulations and measurement results

Figure 5.16: VCO1 measurements (continued)

Table 5.4 summarizes the measurement results for VCO1.

TABLE 5.4: VCO1 measured results

Parameter	Measured value	Comments
Phase noise	-75.5 dBc/Hz @ 100 kHz	Simulated value = -100 dBc/Hz ^a
Voltage range	0.5 V - 2.1 V	As simulated
Tuning range	45 MHz - 230 MHz	As simulated
Power dissipation	3.1 mW @ 489 MHz	As simulated

- a. See [119] for details on what can cause over-estimation of PN when the PSS tool is used within the Spectre™ environment. This particular discrepancy for VCO1 remains unexplained but there is enough indirect evidence to prove that it is not an invalid result or the result of a testing problem. A similar result was measured for an unlocked VCO2 on ICECUR1. The layout of VCO1 was originally used as a template for VCO2-VCO4. Only the ring transistor sizes were changed.

(a)

(b)

(c)

(d)

(e)

(f)

Figure 5.17: VC02 simulations and measurement results

Figure 5.18: VCO2 measurements (continued)

Table 5.5 summarizes the measurement results for VCO2.

TABLE 5.5: VCO2 measured results

Parameter	Measured value	Comments
Phase noise	-74.67 dBc/Hz @ 100 kHz	Simulated - 101 dBc/Hz @ 100 kHz ^a
Voltage range	0.4 V - 2.3 V	As simulated
Tuning range	45 MHz - 330 MHz	As simulated
Power dissipation	3.9 mW @ 660 MHz	As simulated

- a. See [119] for details on what can cause over-estimation of PN when the PSS tool is used within the Spectre™ environment. This particular discrepancy for VCO2 remains unexplained but since it has been measured on ICECUIR1 and on probe9-ICECUIR2, it is not an invalid result or the result of a testing problem. The layout of VCO1 was used as a template for VCO2-VCO4. Only the ring transistor sizes were changed.

(a)

(b)

(c)

(d)

(e)

(f)

Figure 5.19: VC03 simulations and measurement results

Figure 5.20: VCO3 measurements (continued)

Table 5.6 summarizes the measurement results for VCO3.

TABLE 5.6: VCO3 measured results

Parameter	Measured value	Comments
Phase noise	-92.17 dBc/Hz @ 100 kHz	Simulated -101 dBc/Hz @ 100 kHz ^a
Voltage range	0.6 V - 2.0 V	As simulated
Tuning range	55 MHz - 350 MHz	As simulated
Power dissipation	4.5 mW @ 700 MHz	As simulated

- a. See [119] for details on what can cause over-estimation of PN when the PSS tool is used within the Spectre™ environment. This measured result for VCO3 is within 9 dB of the simulated result and is realistic as four VCOs are running at the same time while the test is being conducted at $v_{cont}=1.5$ V. See Figure B.25 for the APS-compatible layout.

Figure 5.21: VCO4 simulations and measurement results

Figure 5.22: VCO4 measurements (continued)

Table 5.7 summarizes the measurement results for VCO4.

TABLE 5.7: VCO4 measured results

Parameter	Measured value	Comments
Phase noise	-87.83 dBc/Hz @ 100 kHz	Simulated -98 dBc/Hz @ 100 kHz ^a
Voltage range	1.0 V - 2.5 V	As simulated
Tuning range	200 MHz - 260 MHz	As simulated
Power dissipation	1.6 mW @ 260 MHz	As simulated

- a. See [119] for details on what can cause over-estimation of PN when the PSS tool is used within the Spectre™ environment. This measured result for VCO4 is within 10 dB of the simulated result and is realistic as four VCOs are running at the same time while the test is being conducted at $v_{cont}=1.5$ V. See Figure B.25 for the APS-compatible layout.

(a) VCO5 (PRES=NRES=10 k Ω)
MAINRES as parameter

(b) VCO5 (PRES=5 k Ω , NRES=1 k Ω)
MAINRES as parameter
(Polynomial trendline added)

(c) Phase noise result for VCO5

(d) Typical VCO5 outputs on 'probe10'

(e) VCO5 spectrum

(f) VCO5 spectrum with modulation

Figure 5.23: VCO5 simulations and measurement results

Table 5.8 summarizes the measurement results for VCO5.

TABLE 5.8: VCO5 measured results

Parameter	Measured value	Comments
Phase noise	-81.67 dBc / Hz	For a typical measured case only. Will change with current selection and VCO control voltage. ^a
Voltage range	0 V - 2.5 V	Rail-to-rail Operation
Tuning range	40 MHz - 640 MHz	Depends on the input bias currents. Maximum frequency is primarily determined by the ring transistor sizes.
Power dissipation	4.1 mW @ 440 MHz	As simulated

- a. This degradation in PN is mainly due to the external resistors namely MAINRES, PRES and NRES. In order to further reduce the PN, on-chip inductors can be used in series with the PMOS bias transistors and the external resistors. This reduces the contribution of power supply jitter toward VCO PN.

The measured variation in duty-cycles for VCO1-VCO4 is shown in Figure 5.24. The solution adopted is a divide-by-2 static flipflop that delivers a 50% duty-cycle output over PVT variations. Further comments about duty-cycle optimization can be found in [68][69]. For the rail-to-rail VCO, i.e., VCO5, the duty-cycle depends on the selection of the individual branch currents.

Figure 5.24: Measured duty-cycle variation for VCO1-VCO4

5.6.6 Bandgap reference

The simulation and measurement results for the transient performance of the BG appear in Figure 5.25.

(a) Start-up transient simulation (vdd as parameter, cout=5 pf)

(b) Start-up time vs. output capacitance

(c) Simulated settling behavior (cout=5 pf)

(d) Measured settling behavior (cout=5 pf)

Figure 5.25: Bandgap reference: transient performance

For systems that frequently go to into the PD mode, a minimum start-up time of $4 \mu\text{s} * 2 = 8 \mu\text{s}$ will ensure stable biasing as the BG transient settling could not be simulated over process corners. A more agile start-up circuit can be used, in which case the perfor-

mance will be limited by the transient settling. Several design improvements can be found in [27].

Power supply and temperature-dependence simulations appear in Figure 5.26. The actual measurements for the temperature-dependence are coarse due to the lack of a temperature-controlled environment for the APS.

(a) Bandgap voltage vs. power supply with temperature as parameter (simulated)

(b) Bandgap voltage vs. power supply (measured at room temperature)

(c) Bandgap voltage vs. temperature with supply voltage as parameter (simulated)

(d) Bandgap voltage vs. temperature (coarse measurement, vdd = 2.5V)

Figure 5.26: Bandgap reference: supply and temperature-dependence

The major results for the BG are summarized in Table 5.9. The discrepancy between simulated and measured results for the BG voltage at TYPICAL voltage and room temperature is thought to be the result of several factors. They include the use of a poly-resistor inside the library opamp to set up the bias currents, different sized vertical-PNP transistors, use of poly-resistors in the BG itself and the offset voltage of the library opamp. The individual contributions from these factors have not been investigated further. The BG is functional although not accurate. A general comment is that the use of n-well resistors could be investigated as the vertical-PNP transistors are also situated inside the n-well. The PVT variations will, to a first order, move the entire BG circuit in the same direction.

TABLE 5.9: Major results for the bandgap reference

Parameter of interest	Simulated value	Measured value
Bandgap voltage (final)	1.256 V (TYPICAL)	1.709 V
Dice-to-dice variation	Not simulated	(max) ± 0.8 mV (6 dice)
Start-up time	4 μ s @ $c_{out} = 5$ pF	4.7 μ s (50 Ω probes)
Settling time	0.3 μ s + 0.7 μ s $\sim$ 1 μ s	1.6 μ s + 1.2 μ s $\sim$ 2.8 μ s
Supply dependence	340 μ V/V, 2.25 V - 2.75 V	curvature (peak @ 1.21 V)
Temperature dependence	94.73 μ V/ $^{\circ}$ C	120 μ V/ $^{\circ}$ C
Power dissipation	172 μ A * 2.5V = 430 μ W	466 μ W

5.6.7 Lock-detection circuit

This could not be tested on the re-bonded ICECUIR1 chips. The SPC was found to be functional on ‘probe5’ (see section B.7 on page 170), but the serial-data could not be sent to the PLL-FS. This was later traced back to the failure of the LVS/DRC tools to detect a soft-substrate connection that would have allowed the data-path to be functional.

5.6.8 Acquisition-aiding circuitry

This could also not be tested for the reasons mentioned above. Simulations have appeared in Chapter 3.

5.6.9 Interface circuitry

The SPC was tested on 'probe5'-ICECUIR2 as shown in Figure B.18. The serial-data ('DATA5') was sent in using the DG at half the frequency of the serial clock ('CLK5'). This was done at several frequencies. The SPC was found to be operational as it controlled a divider as expected. A typical 'SDOUT5' output is shown in Figure 5.27.

Figure 5.27: 'SDOUT5' output on 'probe5'-ICECUIR2

5.6.10 Full PLL-FS post-layout simulations

The closed-loop transient simulations shown in Figure 5.28 run at a rate of approximately 10 μ s per day on an ULTRA-10 Sun-SPARC™ with 1 GB of RAM. The results cannot be indefinitely stored, for reasons of hard-disk space, and are usually stored as abridged text files or a picture files, after post-processing.

As shown in Figure 5.28(a), the duty-cycle of the OSCBY2 signal is 50%. This simulation was performed for the PLL-FS at the extracted level with 9670 circuit components. The post-layout netlist for the ICECUIR1 chip had over 16,000 components and could not be simulated for unknown reasons. Figure 5.28(b) shows that when the switching command is issued at $t = 5 \mu$ s, the VCO control voltage is near its final value because

of the supplied initial condition. This allows the designer to estimate the pull-in time by looking at the slope of the final straight part, without wasting significant time. A good estimate can be made by starting 20% below the final value of v_{cont} because the duty-cycle of the PFD outputs becomes shorter as the final frequency is reached.

Figure 5.28: Closed-loop transient simulation of the PLL-FS

5.6.11 Power dissipation of the PLL-FS

The power dissipation of the total chip is calculated as shown in Table 5.10.

TABLE 5.10: Power dissipation of the PLL-FS

Component	Measured power dissipation (mW)	Comments
CP, BGBIAS, CPBIAS	540 μ W	Indirect measurement on 'probe 2' and 'probe3'
BG	466 μ W	Measured on 'probe3'. Not included on ICECUR1
PFD-NAND	1.1 mW @ 14 MHz	Measured on 'probe1' (64% power in the buffers)
VCO2	3.6 mW @ 200 MHz	Divide-by-2 flipflop not included
Feedback Divider	3.4 mW @ 200 MHz	Measured on 'probe5'

TABLE 5.10: Power dissipation of the PLL-FS

Component	Measured power dissipation (mW)	Comments
Post-scalar	425 μ W @ 200 MHz	Simulated Only
Total	9.065 mW ^a	Measured 13.09 mW ^b

a. This power dissipation can be reduced by using power-conscious logic families in the digital part instead of the static gates. Since it was not the focus of this work, it has not been attempted.

b. Being dissipated in lock-detection and lock-assist circuits, and also some increased power in RD due to a higher f_{ref} .

5.6.12 Full PLL-FS measurements

Figure 5.29 shows the measured results for the re-bonded batch of ICECUIR1 chips tested using the PCB-PLLFS and the modular PCBs (see section A.3 on page 156).

(a) 250 kHz loop-bandwidth

(b) Reference spurs @ 108 MHz

(c) Phase noise plot

(d) Oscilloscope trace

Figure 5.29: Full PLL-FS measurements

The foregoing measurements in Figure 5.29 have been included for the sake of completion. The sub-optimal operation of the PLL-FS was verified by supplying different reference frequencies and measuring the v_{cont} to verify that the VCO2 was indeed functional. Since the VCO2 tested on ICECUIR1 and on ICECUIR2 has a bad PN, the results of these measurements are not practically acceptable. As far as the layout is concerned, VCO1-VCO4 are identical except for the ring transistor sizes. This problem of bad PN remains untraceable. The lack of a data-path is traceable to the LVS problem as described earlier.

5.7 Summary

This chapter presented the measurement results alongside of the relevant post-layout simulation results. The measurements were done to characterize the individual components of the PLL-FS. All the designed components were found to be functional as a result of testing using the APS. Two problems prevented the thorough testing of the PLL-FS. For the first set of chips, it is speculated that it was an ESD/bonding issue. For the second set of chips, it was the failure of the LVS/DRC tools to detect a missing ground connection that prevented the serial data from reaching the divider inputs.

The need for test-planning and communication with the technical support/fabrication engineers are crucial factors for a successful chip design. A time-saving step can be putting proper ESD protection on all inputs. Another precaution can be wire-bonding half the chips for the initial testing phase and getting the loose dice re-bonded in case of a bonding problem.

6.1 Chapter overview

This chapter summarizes the work done and mentions some of the problem areas and issues. Further, it suggests some possibilities for future research.

6.2 Conclusions

In this thesis, the design methodology of a low-cost, fast-locking integer-N PLL-FS has been presented. The synthesizer and its submicron components have been designed and fabricated using the CMOSP25 process. Measured results have been presented for the components and the full PLL-FS. The primary use of such synthesizers is in the area of microprocessors, memories, networking solutions and video clock generation. The design methodology can allow first-time designers to use behavioral simulators and an IC-design environment to arrive at a beta-level PLL-FS without a lot of previous expertise in the synthesizer design area. Practical tips required to fabricate a more predictable, controllable and a repeatable synthesizer, in a submicron CMOS technology, are also included.

The design methodology of a new PFD, i.e., the APFD, has been proposed. The acquisition time is often the bottleneck for an integer-N PLL-FS design. Using the new APFD and the acquisition-aiding methodology proposed herein, the acquisition times can be reduced by a factor of 3.5, whilst the loop-bandwidth remains at a small fraction of

f_{ref} during normal operation. This delivers acceptable VCO sideband performance while meeting the acquisition time specifications. The circuit complexity required to achieve such reduction in acquisition times is minimal.

The PLL-FS consumes 10 mW from a 2.5 V supply at a frequency of 200 MHz. The active die-area estimated on ICECUIR3 is 1.2 mm * 1.2 mm (see “Floorplan for a typical PLL-FS” on page 177). The design was partially testable as the SPC on the fabricated chip was not functioning properly due to an LVS problem. Bonding issues added another dimension to the uncertainty at the performance evaluation stage.

6.3 Problem areas

The guidelines and references from literature presented herein cannot ordinarily be found in one place with such detail. A designer requires the knowledge of the following in order to complete a synthesizer design project from start to finish:

- PLL-FS theory
- System-level, third-party behavioral simulators for PLL-FS design
- A well-supported fabrication technology and the associated design-flows
- Simulators, simulation methods and IC-design environments
- Test planning and test equipment usage
- Layout redundancy and efficient testability of the fabricated chips
- ESD problems, antenna errors and PCB design issues

6.4 Some issues

The cost of designing a chip is the most critical parameter in an industrial setting. This is directly associated with the time-to-market. The actual cost of the fabricated chips is the least expensive part of an IC-design project. Currently, many IC-designers rely on

simulation tools exclusively, to achieve the specifications, as the fabrication technologies get outdated soon. This prevents a deep understanding of the design but is somewhat inevitable as the technologies change at the device level rapidly. Behavioral simulators provide a quick learning method, but not without the relevant literature. A design is more likely to succeed, and be portable to an upcoming technology, if a system-level understanding of the target design is present.

6.5 Future research

The following can be used as some ideas for continuing this work:

- Reliable integration of the loop-filter in a digital CMOS process
- Actual fabrication of the proposed APFD and its deadzone measurement
- A free-wheeling circuit algorithm for the reset pulse in the AgileLock methodology
- Testing the cross-coupling between synthesizers using the new APFD
- A monolithic, fully-differential, fractional-N, low-power synthesizer (1.0 mW or less) in CMOS18 employing an LC-type VCO for enhanced PN performance
- A free-wheeling circuit algorithm for controlling the gain of VCO5
- Multi-band, Multi-VCO, automatically configurable PLL-FS with rail-to-rail operation for low-frequency systems
- A DDS implemented in Verilog™ for low-frequency applications
- An All-Digital synthesizer encoded in Verilog™ for low-frequency applications
- The use of the AgileLock methodology for a wireless GHz range synthesizer

6.6 Summary

This chapter presented the concluding remarks for this thesis document, pointed out some issues and proposed some future research possibilities.

A.1 Modular approach

For testing large chips, many kinds of stimuli and test setups are required. Some of these are regulated supplies, multi-bit data inputs, crystal oscillator inputs, super clean bias voltages and potentiometers for precision external biasing. RF and low-noise amplification might be required to monitor the signals off-chip. Modular and re-usable PCBs save time and are highly recommended for large mixed-signal chips especially during the initial testing phase. If the signal integrity is a critical issue (in the RF range), then there is no choice but to make compact and custom-made PCBs. Some excellent tips on designing PCBs for clock generator ICs appear in [72].

A.2 PCB-ICECUIR0, PCB-ICECUIR1 and PCB-PLLFS

The PCB-ICECUIR0 was simple and functional with the divider inputs in parallel, but ICECUIR0 had little to offer. PCB-ICECUIR1 was too complicated due to the fact all the circuits from a simple bias voltage to the inverting RF amplifiers were put on the same board. There were at least five separate supply planes namely digital_vdd, analog_vdd, buffer_vdd1 for the PLL-FS, buffer_vdd2 for the other testable circuits and a 9V DC-rail (for RF amplifier circuits). It was too difficult to manage especially with unstable chips. From the parasitics point of view, a through-hole socket was used on PCB-ICECUIR0 but

a surface-mounted socket was used on PCB-ICECUIR1. The need for a modular PCB design was evident. Direct soldering of a chip on to the PCB was deemed too risky as populating a new board for every couple of chips was time consuming. The chip cannot be replaced many times as the gold-plated soldering pads deteriorate quickly. A modular and a less complicated PCB-PLLFS was designed to ensure reliable testing. Figure A.1 shows the three main PCBs designed for testing the fabricated chips.

(a) PCB-ICECUIR0

(b) PCB-ICECUIR1

(c) PCB-ICECUIR1 (close-up)

(d) PCB-PLLFS

Figure A.1: Photographs of the PCBs for testing the fabricated chips

A.3 Modular PCBs

In order to test the re-bonded batch of ICECUIR1 chips, modular PCBs were designed. The PCBs are briefly described here and some of the important structures on these PCBs are discussed for reference. PCB-PLLFS as shown in Figure A.1 uses these PCBs for the various inputs it requires.

A.3.1 Power supply filtering

All PCBs contain power supply decoupling as shown in Figure A.2. The two smaller capacitors are also present on each critical bias input near the package pin to provide extra suppression from unwanted coupling with clock signals.

Figure A.2: Power supply decoupling circuit

A.3.2 Filter PCB

This PCB is used to quickly change the LF parameters during testing. For final testing, however, a well-grounded LF near the package is desirable. Using this PCB adds a couple of pF to the LF. Hence, the minimum value of C_1 should be well above the contribution made by the 'Filter PCB' and the package parasitics, in order to get repeatable results. This changes the other LF parameters as well. Typically, $C_1 = 40$ pF, $C_2 = 400$ pF +, and R_2 is as required to maintain stability.

A.3.3 RF amplifier PCB

There is a need to monitor high-frequency signals off-chip to verify component operation. The RF broadband amplifier ERA-1/2/3 SM (DC - 8 GHz) from Minicircuits™ has been used to implement a functionally separate inverting pulse amplifier module shown in Figure A.3. Commercial pulse amplifiers are expensive and often do not meet

Figure A.3: RF amplifier PCB overview

the broadband requirement for the application. An LNA with a similar PCB footprint can be substituted for the RF amplifier, if the design is modular. A PCB with four RF inverting amplifiers was also designed to facilitate the easy measurement of more than one signal.

A.3.4 Bias PCB

The Bias PCB can accept one of three supply inputs in addition to a battery. It is primarily used to establish a clean reference. The other uses can be a custom voltage regulator that provides a fixed or variable bias with current measurement capability.

A.3.5 Reset PCB

This PCB provides a reset pulse using a microprocessor supervisory-circuit (LM372x from National Semiconductor) that provides switch-debouncing. There is a divided output (using HC4040) driven using an external frequency source. The reset signal available from commercial chips can be active-low or active-high. This board provides jumpers and inverters to provide the desired polarity of the reset signal for more flexibility.

A.3.6 Signal PCB

This board provides three crystal oscillators at 10 MHz, 14.318 MHz and 16 MHz using the surface-mount quartz crystal chips from Epson™ (SP636PCE/636PCV crystal oscillators, with a nominal accuracy 70 ppm). These oscillator outputs are at 0-2.5 V, since the Micrel™ voltage regulators (5209-3.0BM) provide the crystals with a regulated voltage of 3V.

A.3.7 (Input-Output) IO-Panel PCB

The IO-Panel PCB has two power rails and can host upto 6 other modular PCBs. It contains power supply filtering, additional SMA supply outlets, external bias potentiometers, blocking capacitors and a 1.25 supply for the bias-tees. It allows the setup of an easily changeable test-bench for use with the APS or another less complicated PCB. This is conceptually depicted in Figure A.4. With this scheme, only the least complicated PCB needs to be designed for the DUT and all the control inputs can be derived from the modular PCBs mounted on the IO-Panel PCB.

Figure A.4: IO-Panel PCB concept

A.4 Photographs of the modular PCBs

(a) Bias PCB

(b) Signal PCB

(c) Reset PCB

(d) Filter PCB

(e) RF amplifier PCB

(f) RF amplifier PCB (4x)

(g) IO-Panel PCB

(h) IO-Panel PCB usage

Figure A.5: Photographs of the modular PCBs

[illegible]

Submicron CMOS Components for PLL-based Frequency Synthesis

Figure B.2: Chip layout of ICECUIR0

(a) Full chip

(b) Pad hook-up problem

Figure B.3: Chip photomicrograph of ICECUIR0

Figure B.4: Schematic of ICECUIR0

B.2 ICECUIR1

Figure B.5: Chip configuration of ICECUIR1

Figure B.6: Chip layout of ICECUIR1

Figure B.7: Chip photomicrograph of ICECUIR1

Figure B.8: Schematic of ICECUR1

B.3 ICECUIR2

Figure B.9: Chip layout of ICECUIR2

Figure B.10: Chip configuration and photomicrograph of ICECUIR2

B.4 Details of probe1/probe2 on ICECUIR2

Figure B.11: Pin configuration and layout of probe1/probe2

This is the master for probe1 and probe2
 probe1 = 1x chargepump / probe2= 4x chargepump

Figure B.12: Schematic of probe1/probe2

B.5 Details of probe3 on ICECUIR2

Figure B.13: Pin configuration and layout of probe3

PDPFD = vss! and FOURXPFD = vss!

1x INTEGRATED CHARGE PUMP WITH NO EXTERNAL RESISTOR
BANDGAP'S OUTPUT BGOUT3 CAN BE CONNECTED TO BG3, IF
THE BANDGAP IS FOUND TO BE FUNCTIONAL

Figure B.14: Schematic of probe3

B.6 Details of probe4 on ICECUIR2

Figure B.15: Pin configuration and layout of probe4

Figure B.16: Schematic of probe4

B.7 Details of probe5 on ICECUIR2

Figure B.17: Pin configuration and layout of probe5

Figure B.18: Schematic of probe5

B.8 Details of probe6 on ICECUIR2

Figure B.19: Pin configuration and layout of probe6

Figure B.20: Schematic of probe6

B.9 Details of probe7 on ICECUIR2

Figure B.21: Pin configuration and layout of probe7

Figure B.22: Schematic of probe7

B.10 Details of probe8 on ICECUIR2

Figure B.23: Pin configuration and layout of probe8

Figure B.24: Schematic of probe8

B.11 Details of probe9 on ICECUIR2

Figure B.25: Pin configuration and layout of probe9

Figure B.26: Schematic of probe9

B.12 Details of probe10 on ICECUIR2

Figure B.27: Pin configuration and layout of probe10

Figure B.28: Schematic of probe10

B.13 ICFCUIR2

Figure B.29: Chip configuration, layout and photomicrograph of ICFCUIR2

Figure B.30: Schematic of ICFCUIR2

B.14 Floorplan for a typical PLL-FS

Figure B.31: Layout of ICECUIR3 (not fabricated)

Figure B.31 shows the layout for a typical PLL-FS. The PCB test fixture (CQFP24-based) will have three ground planes based on the chip floorplan; digital (left half), analog (right half) and the buffer (towards the bottom). The external LF and VCO biasing resistors will be close to the package and firmly connected to the analog ground plane. This was designed as a stand-alone prototype PLL-FS chip with external resistors for the rail-to-rail VCO and external biasing resistor provision (EXTR) in the CP. Extra guard rings around analog parts and off-chip decoupling caps are essential. ESD protection is available on all bond pads. The active area is 1.2 mm * 1.2 mm.

C.1 Phase-frequency detectors

Figure C.1: PFD-NAND schematic

Figure C.2: PFED-NAND layout

Figure C.3: PFD-NOR schematic

Figure C.4: PFD-NOR layout (on ICFCUIR2)

C.2 Chargepump and biasing circuitry

Figure C.5: Interconnections of the BG, BGBIAS, CPBIAS and CP blocks

Figure C.6: Schematic of the chargepump

Figure C.7: Schematic of the CPBIAS block

Figure C.8: Layout of the CPBIAS block

Figure C.9: Schematic of the BGBIAS block

Figure C.10: Layout of the BGBIAS block

Figure C.11: Schematic of the charge-removal circuit

Figure C.12: Transmission gate (a) schematic (b) layout

Figure C.13: Layout of the chargepump with the charge-removal circuit

Figure C.14: Schematic of VCO1 - VCO4

Figure C.15: Layout of VCO1 - VCO4

C.4 VCO5 (rail-to-rail oscillator)

Figure C.16: Schematic of the rail-to-rail bias circuit in VCO5

Figure C.17: Schematic of VCO5 core

Figure C.18: Layout of VCO5 (rail-to-rail VCO)

C.5 Dividers (Integer-N and fractional-N)

Figure C.19: Schematic of the T-flipflop (TFF)

Figure C.20: Layout of the T-flipflop (TFF)

Figure C.21: Schematic of the 7-bit programmable FBD and RD

Figure C.22: Layout of the 7-bit programmable FBD and RD

Figure C.23: Schematic of the dual (programmable)-modulus fractional-N divider

Figure C.24: Layout of the dual (programmable)-modulus fractional-N divider

- * A section of ICFCUIR2 showing the 7-bit presettable divider
- * Uses a ripple counter incrementer circuit to increment divider ratio
- * On the left side are the diffusion areas to reduce antenna errors
- * Tested on the Analytical Probe Station (APS)

Figure C.25: Layout of the FBD (ICFCUIR2)

C.6 Lock-detection and acquisition-aiding circuits on ICECUIR1

Figure C.26: Schematic of LOCKDETECT on ICECUIR1

Figure C.27: Layout of LOCKDETECT on ICECUIR1

Figure C.28: Schematic of LOCKASSIST block on ICECUIR1

Figure C.29: Layout of LOCKASSIST block on ICECUIR1

C.7 Bandgap reference

Figure C.30: Bandgap references (a) schematics (b) layouts

C.8 Serial-to-parallel converter

Figure C.31: Schematic of the SPC (four stages only)

Figure C.32: Layout of the SPC (four stages only)

C.9 On-chip buffer

Figure C.33: On-chip buffer (a) schematic (b) layout

C.10 ESD protection module on ICECUIR2

Figure C.34: ESD protection module (a) schematic (b) layout

C.12 Acquisition-aiding circuitry (proposed)

Figure C.36: Acquisition-aiding circuit interconnections

Figure C.37: Lock-detection circuit (improved)

Frequency Synthesizer Types

D.1 Direct Analog Synthesizers (DAS)

DAS [3][16] utilizes a single reference oscillator, and basic operations thereafter, to produce the desired frequencies. As a very simple example, if 30 MHz and a non-harmonically related frequency of 32.5 MHz have to be generated using a 10 MHz reference, the multiply-mix-filter approach can be used as depicted in Figure D.1.

Figure D.1: Multiply-mix-filter method for reference generation

For harmonically-related frequencies, a comb-generator is used and the desired harmonics are selected using BPFs. An obvious limitation of the above method is the non-ideal TF of the BPF. If harmonics are close together and they cannot be sufficiently filtered, the intermodulation terms from mixing can appear directly on top of the required output frequency. Filtering these terms would be impossible. A crystal-tuned BPF can be employed as a first solution to this problem. Another solution found in commercial instru-

mentation is the ‘double-mix approach’ that cancels the effects of the tuned oscillator on the stability, accuracy and phase noise of the output [16].

In Figure D.2, a second approach is shown in which the input frequency is down-converted. The goal is to use a tuned oscillator to isolate a harmonic from a frequency comb-generator. The only requirement is that the oscillator is tuned so f_{IF} falls in the

Figure D.2: Double-mix approach with drift-cancellation

BPF’s narrow passband. Hence a free-running tuned oscillator can be used to select one frequency at a time and the drift introduced by the oscillator is also cancelled. Cascadable versions of this technique use a more refined ‘triple mix’ approach [16]. Most current DAS architectures use an approach referred to as ‘decades’, wherein the same block can be cascaded for achieving the required resolution [3]. Figure D.3 shows this approach.

As an example, a DAS that can generate frequencies from 80.0 MHz to 200.0 MHz with 100 kHz resolution is presented in Figure D.4, wherein all references can be generated using methods described earlier in this section. It must be pointed out that this represents one of many possible implementations and component availability will probably dictate the final design choices.

Figure D.3: Decade design for DAS using the same stage

Arbitrarily choosing 80 MHz as the input to the first DAS stage, the minimum frequency possible is $(80 + 709 + 10 + 1) = 800$ MHz. The maximum achievable frequency is $(80 + 1809 + 100 + 10) = 1999$ MHz. Upon division by 10, the required frequency range is obtained. The last specified frequency is often not achievable. The resolution of the DAS can be improved by adding similar stages and is convenient for the vendor and the customer alike.

Figure D.4: Single DAS stage for the example design: 80 MHz - 200 MHz

To get further insight into the operation of the example DAS, let's say a frequency of 165.436 MHz is to be generated. Hence, three stages will be required. Starting from the least significant digit required, frequencies of 165.6 MHz, 165.3 MHz and 165.4 MHz will

have to be generated, in this precise order, using the outputs available from the preceding stages. Table D.1 illustrates this procedure.

TABLE D.1: Generation of 165.436 MHz using the example DAS

Stage #	f_{in}	Contributions from the 1st, 2nd and 3rd mixer/BPF stages	$\div 10$
1	80	$80 + 1509 + 60 + 7 = 1656$	165.6
2	165.6	$165.6 + 1409 + 70 + 9 = 1653.6$	165.36
3	165.36	$165.36 + 1409 + 70 + 10 = 1654.36$	165.436

This preliminary system design is far from the finished product. In 1970s and 1980s, it would also have been impractical because of the absence of high-quality affordable RF components in the GHz range. Discrete spurious outputs from each mixer/BPF have to be calculated and BPFs would use drift cancellation circuitry in the individual stages and the reference generation module as described earlier. Such an FS could cost upwards of tens of thousands of dollars using discrete components. The switching speed will depend on the switches and the settling time of the BPFs. Modulation capability is not present but can be easily added as a separate module at the FS output. Power budgets at various points in the DAS have to be calculated to avoid stage saturation while maintaining output amplitude flatness. The PN requirements and frequency offsets between stages put an upper limit on the number of stages that can be cascaded. Shielding of the individual stage modules and the complete DAS would be necessary to ensure EMI compliance. Furthermore, a shielded linear power supply would be required. Hence, this FS technique is primarily limited to high-quality lab instruments and precision applications.

D.2 Direct-Digital Frequency Synthesizers (DDFS)

The heart of this DSP-oriented synthesis technique is the Nyquist Sampling theorem. It states that a signal with no frequency components above f_{max} can be reconstructed

from its samples taken at or above the Nyquist frequency, i.e., $f_{sample} \geq 2f_{max}$. An anti-aliasing filter is used before sampling to reduce the frequency content above f_{max} .

The PLL-FS and DAS techniques manipulate an existing sine waveform to get the required output. In a DDFS, the sine wave samples are generated from mathematical definition. The digital words obtained on a sample-by-sample basis are converted into an analog signal using a low-noise DAC and an LPF. This concept was first proposed in early 1970s [20] but practical realizations gained widespread acceptance in the 1990s. It is now a commercially established technique because of the advances in fabrication, maturity of DSP techniques and a fast evolution of synthesis tools and computers. With the exception of the DAC, everything else has an entirely predictable influence on the DDFS output.

The basic DDFS design contains four distinct blocks shown in Figure D.5; a phase-accumulator, a sine look-up table, a DAC and an LPF [3].

Figure D.5: DDFS block diagram and functional waveforms

An ideal sine wave can be described by $A \sin(\omega t + \phi)$; and therefore, it can be constructed starting with the phase. The phase of a sinusoidal signal goes from 0-359 degrees and then resets back to zero. This can be realized using a counter that can count from 0-359 and then resets itself. The rate at which the counter is clocked will dictate the frequency of the output signal. The problem in frequency synthesis is generation of several frequencies from a single reference. Hence the counter can be replaced by an accumulator that can accept a W -bit input word and can change the rate of phase as desired. By defini-

tion, the rate of change of phase or $\frac{d\phi}{dt}$ is the frequency. Assuming that the accumulator has n -bits and it is clocked at a rate of f_{clk} , the output frequency is given by:

$$f_{out} = 2\pi \frac{d\phi}{dt} = \frac{f_{clk}}{2^n} W \quad (\text{D.1})$$

It is imperative that $W < 2^n - 1$ as it is the Nyquist frequency. In general W is much less than n . The function of the sine look-up table is to change this value of phase into amplitude by passing a ' k '-bit digital word on to the DAC. After conversion and low-pass filtering a sine wave appears at the output of the DDFS.

The obvious advantage of the DDFS techniques is the use of digital techniques that result in repeatability, predictability, portability, controllability and enhanced functionality. No other FS technique demonstrates all these attributes. The DDFS is a digital system and, therefore, all errors are known at all times or can be calculated. An exact prediction can be made about the total spurious output, noise output and all other parameters and therefore the feasibility for a targeted application can be ascertained at the design stage.

The maximum achievable frequency for a DDFS is theoretically $f_{clk}/2$ (the Nyquist frequency). Practical LPFs are used as anti-aliasing filters and this theoretical maximum is somewhat reduced. At higher speeds, the access-time for ROM, accumulator architecture, DAC architecture and LPF, all contribute toward the reduction of the maximum achievable frequency. The minimum generated frequency can be as low as DC. The maximum frequency of operation is limited by the speed of the accumulator, the DAC, and the input frequency.

Frequency resolution depends on the size of the accumulator and for a binary accumulator, it is given by $f_{clk}/2^n$. As a numerical example, with a 200 MHz clock rate and a 24-bit accumulator, the resolution is 11.92 Hz. A 32-bit accumulator delivers a resolution of 0.046 Hz, that is more than required for most applications. Changing the accumulator size comes at the cost of increased die-area and power dissipation but no additional system

design effort. Using other frequency synthesis techniques, such resolutions are not economically achievable.

The switching speed of a DDFS is the sum of the settling-time of the DAC, the settling-time of the LPF and the time it takes for the accumulator to overflow after a change in the input word. Delay through the digital logic and the access-time for the ROM are negligible at low frequencies. Switching speeds below few tens of ns can be achieved.

In a DDFS, the discrete spurious outputs are present due to quantization errors, aliasing and clock leakage. Aliasing cannot be removed close to the Nyquist frequency due to the order of the LPF. The harmonics of the aliased signals are also present. Without careful design, these can mix with the clock to generate undesirable frequency spurs. Higher-order filters are commonly used to suppress these undesired spurs.

A DDFS is comparable to a PLL-FS in terms of the power dissipation and is much superior to a DAS in the same respect. The output flatness depends on the DAC performance and is reasonably well-controlled. A point worth mentioning is that a successful DDFS implementation requires design expertise in the areas of digital, analog, mixed-signal, memory architectures and DSP techniques.

Modulation capability can be added to the DDFS at several points as shown in Figure D.6. Changing the instantaneous phase will give rise to digital-FM modulation. By putting another accumulator before the main accumulator and controlling its overflow using a RAM, an arbitrary non-linear FM modulation can be generated. Adding digital phase modulation reduces to adding or subtracting a digital word at the accumulator output. A 12-bit adder provides $360/2^{12} = 0.088^\circ$ of phase resolution. Amplitude Modulation (AM) can be achieved either digitally by changing the amplitude representation of the ROM output or by varying the reference supply of the DAC using an auxiliary-DAC and control circuitry. Pulse-modulation at the output can be achieved by setting the DAC input to zero while the digital part keeps running and the state of the DDFS is preserved. After

this reset is removed, the phase memory is also preserved. Another possibility it is to reset the accumulator to a 'zero-phase' or any other initial state.

Figure D.6: Modulation possibilities in a standard DDS

Such a diversity in modulation capability is not possible using other FS techniques. Using a combination of above modulation methods, arbitrary waveform shapes can be synthesized, within the frequency range of the DDS. With the advancement of technology and the understanding of this technique, DDS is likely to replace all other synthesis techniques for low-frequency applications where power consumption is small. For higher frequencies, indirect synthesis will continue to be the architecture of choice.

D.3 Integer- N loops

The basic principle of integer- N loops is shown in Figure D.7. This is a logical evolution of the linear-PLL with a divider in the feedback path. The simplified principle of operation is as follows. The VCO generates a frequency f_{vco} that is divided by the divider and fed back to the phase detector. The phase detector compares the phase of this signal with f_{ref} and generates an error signal in the form of pulses. These pulses are sent

through the LPF to extract the DC control voltage required to adjust the VCO frequency. This completes the loop and the VCO locks to an integer multiple of f_{ref} , i.e., Nf_{ref} .

This deceptively simple operation of the loop is not without some inherent drawbacks. The first and most important is that the integer-N loop acts as a frequency multiplier and hence noise present in the reference is degraded by $20\log N$ (dB). On the other hand, the PLL acts as a narrow BPF. Beyond the loop-bandwidth, the PN of the VCO dominates. Hence a clean reference and a VCO with good phase noise are the keys to the design of the integer-N FS.

Figure D.7: Basic integer-N frequency synthesizer

The output frequency resolution is limited to f_{ref} . Lowering f_{ref} results in excessively large settling-times as the loop gets updated infrequently. Also the feedback division ratio N becomes excessive for RF frequencies. The sidebands at the output of the phase detector have to be low-pass filtered, something that becomes difficult with increasing N and lower f_{ref} . There are several practical solutions to these problems. Acquisition-aiding circuitry can be used to speed up the acquisition time of an integer-N loop. A multi-loop FS can be used to improve PN and switching speed [3] in exchange for a more complex design. A technique known as fractional-N synthesis can be used as well.

D.4 Fractional-N loops

Fractional-N loops can generate fractional multiples of the reference frequency by employing additional digital circuitry in the feedback divider [91][92]. Just as in the case

of a DDS, where an arbitrary fractional resolution can be achieved by changing the accumulator input-word, an arbitrary fractional multiple of the reference frequency can be generated by changing the modulus of the feedback divider on the fly. The spurious response of the fractional-N loops is better than a DDS as the output spectrum is limited by the PLL loop-bandwidth [17]. The major difference between the DDS and Fractional-N loops is that sine wave is already present in the case of fractional-N loops (Figure D.8) and only its phase is manipulated [3] whereas a sine wave is mathematically created in the case of a DDS.

Figure D.8: Basic concept of a fractional-N loop

An example of fractional-N operation is as follows: If a divider is forced to divide by $(N+1)$ and N in succession, a frequency of $(N+0.5)f_{ref}$ would be produced by the PLL-FS. The word ‘fractional-N’ is a misnomer as the fractional frequency is achievable only on a time-average basis. By changing the modulus for a different number of reference cycles, any fractional multiple of the reference frequency can be obtained [3][15][16][17].

In general, if the feedback divider ratio is N for n reference periods and $(N+1)$ for m reference periods, then over $(n+m)$ reference periods, the output frequency is given by:

$$f_0 = \left[\frac{\{N \times n\} + \{(N+1) \times m\}}{m+n} \right] f_{ref} = N f_{ref} \left[1 + \frac{m}{(m+n)} \right] \quad (\text{D.2})$$

Hence a fractional part can be realized provided the fractional beat-note can be cancelled. Without appropriate cancellation, as long as the beat-note is outside the loop-

bandwidth, the synthesizer performance is acceptable. A fractional part of roughly 1/3 to 2/3 can be realized in such a case [17]. The notation $N.F$ is used to describe the integer and the fractional parts. The advantage of the fractional-N technique is that the error present at the output is deterministic, similar to that of a DDFS, and the required correction can be calculated.

If the divider ratio is set at $(N+1)$, then the phase-step at the phase detector input is negative as this waveform accumulates phase slower. The reverse is true for division by N . Assuming binary logic, if we break up the real and fractional part as:

$$N \cdot F = N + \frac{W}{2^n} \quad (\text{D.3})$$

To implement $N.F$ requires an n -bit accumulator. W is the input word to this accumulator and resides in the fraction register as shown in Figure D.9.

Figure D.9: Fractional-N beat-note cancellation

It can take on values between 0 and (2^n-1) . Thus, any fraction can be programmed in the fraction register. The accumulator is updated at a frequency of f_{ref} . The overflow from this accumulator can be used as the modulus control signal for the FBD. The contents of the accumulator are precisely known at any time and can be fed to a DAC. After

inversion and addition to the phase detector output with some form of amplitude control, this can remove the sawtooth artifact at the phase detector output. This must be done exactly at the sampling instant as the phase detector generates information on these edges and the accumulator is also being updated only at these instants [3]. Figure D.9 shows the procedure that has been employed by leading test equipment manufacturers.

This method should not be confused with the original ‘Digiphase’ technique [21]. The major difference is that the Digiphase technique accumulates both the fractional and integer portions and therefore does not require a divider in the feedback path [17]. From the RF-design perspective, the use of a dual-modulus prescaler is power efficient and hence the fractional-N technique is widely used.

Another popular technique for beat-note cancellation is the noise-shaping method using over-sampled sigma-delta modulators to control the modulus of the feedback divider [22]. The idea is to push the resulting quantization noise away from DC and the multiples of the clock frequency. Higher order sigma-delta modulators result in better noise-shaping and filtering towards higher frequencies.

D.5 Delay-locked loop frequency synthesizer

Recently, a frequency synthesis technique has been proposed [83] that uses a Delay-Locked Loop (DLL). A DLL is a PLL that uses a Voltage-Controlled Delay Line (VCDL) instead of a VCO. An ‘edge-combiner’ is used to produce an output that is a multiple of the reference frequency and the number of delay stages. The advantage of a DLL-FS is that the cycle-to-cycle jitter does not add up as it does in the ring oscillator. Very flat close-in phase noise profiles can be achieved using this technique. The disadvantage is that the output frequency is fixed by the number of delay stages and so frequency tuning is not possible. The spurs can be placed away from the RF-band by a careful choice of the reference frequency. Figure D.10 shows a simplified block diagram of the DLL-FS concept

from [83].

Figure D.10: Block diagram of a DLL-based frequency synthesizer

D.6 Hybrid loops

Several kinds of hybrid loops have been explored in the past few decades. Multi-loop synthesizers use mixers to achieve better spurious performance and are amenable to integration. Circuit complexity is a disadvantage so they are mostly employed in test instruments where cost is not the main issue. The idea is to use an inner loop with a relatively poor PN performance that is subsequently improved by division in the outer loop. Hybrid loops employ DDFS and fractional-N techniques beyond some simple mixing operation to realize high performance monolithic solutions. DDFS is mainly employed to generate a frequency range for subsequent processing by fractional-N loops. The biggest advantage of a fractional-N loop at the DDFS output in a hybrid architecture, in terms of monolithic implementation, is that no additional anti-aliasing filter is required at the loop output given the narrow-band tracking action of the PLL itself [17].

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