SI-BASED STACKED INDUCTORS FOR BROADBAND CIRCUIT APPLICATIONS

by

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Abstract

An ever increasing demand for high data rate broadband services into the foreseeable future means that CMOS solutions that transmit and receive data at high speeds with low error rates, low cost and low power will be needed. High-speed broadband circuits operating at bit rate of 10Gb/s - 40Gb/s or higher, usually require bandwidth enhancement. One of the most common techniques to implement bandwidth enhancement is inductive peaking however, it has the disadvantage of using large circuit area due to the large size of on chip transmission lines or kit inductors. This will lead to increased size and cost of an IC.

In this thesis, the performance of circuits that use stacked inductors for inductive peaking is compared with the performance that would have been achieved using of on chip transmission lines or kit inductors. Detail stacked spiral inductor design procedures are presented using ASITIC and HFSS modeling programs. The equivalent circuit of the stacked inductor is optimized in ADS using the modified 2-π model for better performance matching. Different on-chip isolation techniques are also studied in order to reduce the unwanted coupling.

Finally, some amplifiers and stacked inductors are fabricated in the IBM 0.13μm CMOS process. Measurement results show that stacked inductors with a T-coil topology achieve up to a 73% bandwidth improvement while reducing the required chip area by 85% or more compared to using planar kit inductors from the manufacturer.

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Abbreviations

AC	Alternating Current
ADS	Advanced Design System
ASITIC	Analysis and Simulation of Spiral Inductors and Transformers for IC
BWER	Bandwidth Extension Ratio
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
EM	Electro Magnetic
FEM	Finite Element Method
FFT	Fast Fourier Transform
GSG	Ground Signal Ground
GSW	Gaussian Side Wall
GTGP	Gaussian Top Ground Plane
HFSS	High Frequency Structural Simulator
ISS	Impedance Standard Substrate
k	Coupling coefficient
LNA	Low Noise Amplifier
M	Mutual inductance
MoM	Method of Moments
PEC	Perfect electric conductor
PGS	Patterned Ground Shielding
Q	Quality Factor
Q_{peak}	Peak Q
RF	Radio Frequency
Si	Silicon
SOC	System-On-Chip
SOLT	Short Open Load Thru
STI	Shallow trench isolation
VCO	Voltage Controlled Oscillator
VNA	Vector Network Analyzer

Chapter 1 Introduction

An ever increasing demand for high data rate broadband services in the foreseeable future means that CMOS solutions that transmit and receive data at high speeds with low error rates, low cost and low power will be needed. CMOS is a viable solution for system-on-Chip (SOC) integration. For these reasons, SOCs that integrate all active and passive components using a low-cost semiconductor manufacturing processes provide a very attractive solution for the rapidly emerging commercial and consumer market of high data rate broadband services [1], [2].

1.1 Motivation for this Work

Wireline devices that operate at bit rate of 10Gb/s - 40Gb/s or higher such as MUX/DEMUX circuits for Ethernet applications demand the design of broadband amplifiers [3], [4], and 40Gb/s optical fiber channels and backplane transmission requires broadband amplification in preamplifiers, drivers, transimpedance amplifiers, etc [5]. Even though CMOS devices can provide a low cost solution for system-on-chip, circuit parasitic capacitance and lossy substrate limit the performance of broadband amplifiers. Thus, a bandwidth extension techniques are necessary to achieve a high data rate operation of 10Gb/s - 40Gb/s or higher. One of the most common techniques used is inductive peaking; however, the need for an on-chip inductor with large area consumption and of transmission lines or kit inductors is a serious disadvantage. For example, the minimum outer diameter of a standard inductor in a 0.13μm CMOS technology is 100μm, this waste of layout area can be minimized by the use of our customized ultra-compact inductors employing a multi-level stacked structure have an outer diameter as low as 10μm to 40μm depending on the desired Quality factor and inductance. The design of an 18 stages active delay line design, using the kit inductors for peaking required about 4 mm^2 of chip area; however, with the use of ultra compact inductor presented here, the chip size can be reduced to 2.5 mm^2. Such compact inductors have a low Q of about 5 to 8, but in a peaking application they are in series with a resistor so Q is irrelevant. An example shown

in Figure 1-1 compares the sizes of the kit inductors and the customized stacked inductors for similar inductances.

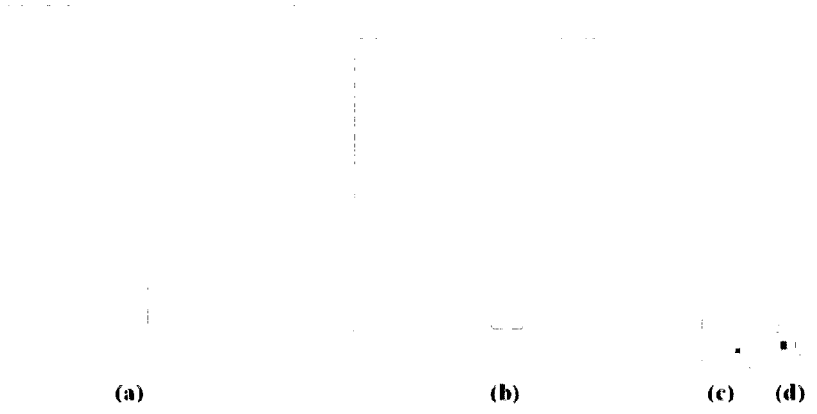


Figure 1-1: Sample layout of inductors, (a) and (b) kit inductors, (c) and (d) stacked inductors

Simulations will be done using HFSS [6], a full 3-D electromagnetic (EM) simulator to explore the inductance, series resistance, Q factor, and coupling efficient when using different isolation techniques. A test chip is designed and manufactured here to study and verify the performance of the stacked inductors simulated with HFSS. Some common source amplifiers will also be tested to explore the bandwidth extension with T-coil inductive peaking topology. An increase in the bandwidth of these amplifiers, compared to standard amplifier architectures, could translate into a reduction in the size and cost of the SOC solution.

1.2 Thesis Outline

Chapter 2 of this thesis will describe on-chip inductor background including the loss mechanisms, e.g. metallic losses, substrate losses, affecting the quality factor of the inductor. This chapter will also discuss Si IC fabrication processes and numerical methods available in EM simulators. Chapter 3 will discuss available on-chip isolation techniques. Chapter 4 will present a customized stacked inductor design flow considerations and layout, including the simulation results using the full 3-D simulator HFSS to explore the inductance parameters such as Q factor, coupling efficient k and mutual inductance M in the presence of various isolation

techniques. Inductor performance variation due to the temperature variation will also be studied. Chapter 5 will review basic inductive peaking theory for amplifiers, and discuss simulation results. Chapter 6 will present the measurements of the inductors and the amplifiers. Chapter 7 will summarize the thesis.

1.3 Thesis Goals

There were four major goals to this research:

1. Provided detail design flow and considerations to build and model stacked inductors based on the understanding of the inductor background information

2. In-depth isolation techniques study, including their advantages and disadvantages

3. Measured some ultra compact stacked inductors that had been fabricated in IBM 0.13μm CMOS process in order to demonstrate the stacked inductor design techniques and model performance.

4. Measured some common source amplifiers that had been fabricated in IBM 0.13μm CMOS process. Used the measurement results to demonstrate that small stacked inductors could be used for inductive peaking amplifiers and provide good bandwidth enhancement while reducing chip area by a huge amount.

Chapter 2 On-chip Inductor Background

Integrating high performance on-chip inductors is still a challenge in modern CMOS technology due to the high conducted of the substrate and the metal losses at high frequencies.

In this chapter, the basic theory of on-chip inductors will be reviewed including the regular planar inductor structure and its parameters. Simple explanations for quality factor, self-resonance frequency, mutual inductance, and coupling coefficient will be given. A brief introduction to the loss mechanisms present in an inductor in a CMOS technology will be given. Finally, the numerical methods in different EM simulators for inductor modeling will be presented.

2.1 Basic Concepts of the On-chip Inductors

On-chip inductors are widely used in CMOS radio frequency (RF) circuits, such as the low-noise amplifiers (LNA), voltage-controlled oscillators (VCO), and power amplifiers. They are usually designed using a spiral structure, as shown in Figure 2-1 [7], which shows a typical layout of an on-chip spiral inductor. Each on-chip spiral inductor can be defined based on its design parameters, including the outer diameter d, the metal width w, the spacing between the wiring metal s, and the number of turn n.

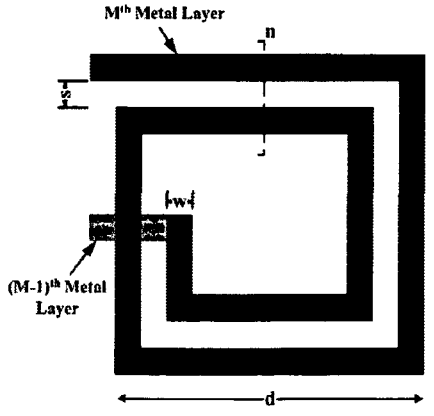


Figure 2-1: Layout and design parameters of an on-chip planar spiral inductor [7]

The main challenge when designing on-chip inductors is to find an area efficient layout that achieves adequate performance in terms of inductance, series resistance, maximum saturation current, coupling coefficient, Q factor, and self-resonance frequency f_{res}.

2.1.1 The Quality Factor of Inductors

For RF circuits design, the quality factor Q of an inductor is one of its most important characteristics since the Q of the inductor significantly affects the performance of the entire system, e.g. the gain/power ratio of the LNA, and the phase noise of the VCO. However, due to the loss mechanisms of the substrate and the thin metal layers in a standard CMOS process, to realize high-Q on-chip spiral inductors is one of the major challenges of CMOS RF research [7]. The quality factor Q of a passive circuit element is defined as

$$Q = \frac{|\mathrm{Im}(Z_{ind})|}{|\mathrm{Re}(Z_{ind})|} \qquad (2.1)$$

The higher the Q factor, the lower the loss of a passive device. Thus, ideal inductors and capacitors have infinite Q whereas practical devices have finite Q. The loss mechanisms of a standard CMOS process will be studied in the next section of this chapter.

2.1.2 Self-resonance of Inductors

Similar to the Q factor, the self-resonance frequency f_{res} is also another important characteristic of on-chip inductors, especially for an inductive peaking implementation for high data rate broadband circuitry. In a peaking application, the inductors are in series with a resistor so Q is irrelevant. An inductor self-resonates at the frequency that its impedance becomes capacitive. In most of cases, the highest useful frequency of an inductor is much smaller than f_{res}, usually only $\frac{1}{3}$ of the f_{res}, because the Q begins to fall off after f_{max}, which is the frequency when the maximum Q occurs, and Q equals zero at f_{res} [7]. In Figure 2-2(a), the f_{res} of the inductor is around 35.69 GHz and its maximum useful frequency is around

12.11 GHz, where there is 10% increase in the inductance compared to the inductance near DC. This inductor has a peak Q of 14.5.

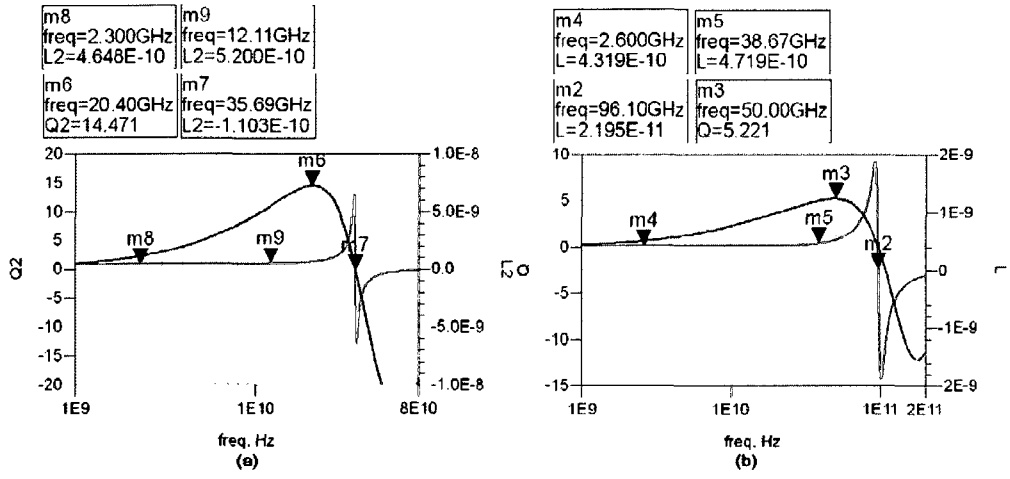


Figure 2-2: (a) an example characteristic of a planar inductor, (b) an example characteristic of a stacked inductor, where for both (a) and (b) the blue curve is the Q and the red curve is the inductance L

Increasing f_{res} is necessary when the frequency bands of the applications are increasing. The planar inductor has large area consumption, and results in long, wide interconnect wires among the passive and active components. Although the inductor's Q factor can be improved using a wider metal width, its f_{res} will be decreased dramatically. Thus, this research is conduced to study the use of 3-D inductors, as shown at Figure 2-3, which can achieve similar inductance compared to a big planar inductor but with much smaller layout area, higher f_{res}, and lower Q. An example of the characteristic of the stacked inductor is shown in Figure 2-2(b), it has similar inductance as Figure 2-2(a), but the f_{res} of the inductor is much higher around 96.1 GHz and its useful bandwidth is 38.67 GHz, however the peak Q factor is only 5.2.

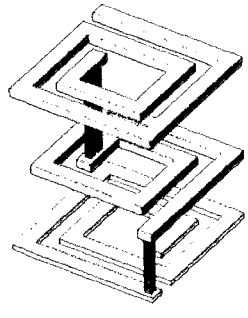


Figure 2-3: Sample 3-D view of a staked square inductor

2.1.3 Mutual Inductance

Mutual inductance, M, occurs between two inductors when one inductor's current changes and that change induces a voltage change in the second inductor. This important property allows transformers to work, but it can also cause unwanted coupling between conductors in a circuit. Mutual inductance can also be related to the inductor's with the coupling coefficient, k. The coupling coefficient is always between 1 and 0. It specifies the relationship between a certain orientations of inductor with arbitrary inductance. So for two nearby inductors with arbitrary inductance and orientations, their mutual inductance and coupling coefficient can be extracted from two-port network Z-parameters obtained from modeling or measurement data as the following [8]:

$$L_1 = \frac{Im(Z_{11})}{\omega} \qquad (2.2)$$

$$L_2 = \frac{Im(Z_{22})}{\omega} \qquad (2.3)$$

$$k = \sqrt{\frac{Im(Z_{12}) \cdot Im(Z_{21})}{Im(Z_{11}) \cdot Im(Z_{22})}} \qquad (2.4)$$

$$M = k\sqrt{L_1 \cdot L_2} \qquad (2.5)$$

2.2 Loss Mechanisms

In CMOS technology, an on-chip inductor suffers from metal and substrate losses [7]. The different loss mechanisms are shown in Figure 2-4 [9] and explained in the following subsections.

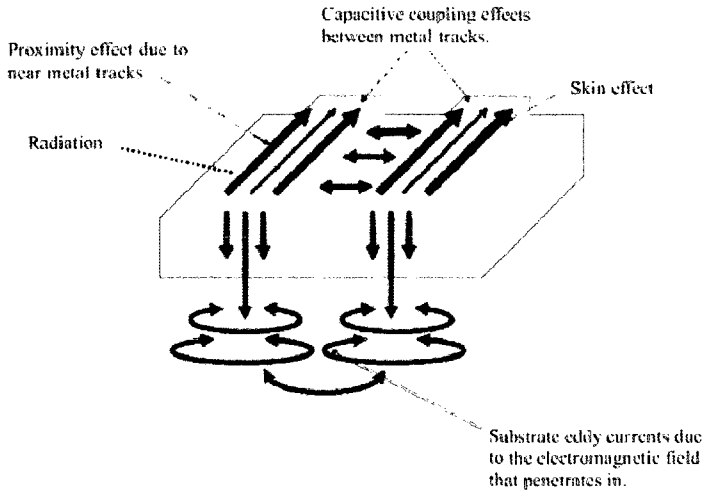


Figure 2-4: Loss mechanisms [9]

2.2.1 Metal Loss

Metal loss results from the current flowing through the series resistance of the inductor. At DC or low frequencies, the series resistance is determined mainly by the sheet resistance and the conductivity of the metal tracks [9]. With the rapid development of CMOS fabrication technologies, typically there are more than 6 metallization layers that can be used. A designer has the ability to make use of one or more metal tracks in parallel to reduce the sheet resistance. On the other hand, using a wider metal line can reduce the ohmic loss resulting in an increase in the capacitive loss and causing a decrease in Q and f_{res} due to the larger metal-to-substrate capacitance [7]. Copper metallization also has been studied as a replacement for aluminum in order to increase the conductivity of the metal tracks and reduce the series resistance of integrated inductors. RF processes like the 0.18μm CMOS process from UMC and the 0.13μm CMOS process from IBM, implement a thick top metal layer with higher conductivity to reduce the resistivity of the metal tracks and increase the quality factor of the integrated inductors [9].

At high frequencies, the current is not evenly distributed throughout the cross section of the metal tracks due to the skin effect and proximity effect (refer to Figure 2-4). In any metal track, the alternating current (AC) tends to be higher where the resistance is minimum;

however, due to the magnetic field that penetrates into the dielectric and substrate, electric fields move the current to the surface and the current is accumulated in the surface of the conductor. Hence, the current density will be less at the centre than the conductor surface [9]. This extra concentration of current at the surface is known as skin effect, causing the effective resistance (AC resistance) of the conductor to increase with frequency. A sample simulation result of current density using Maxwell SV [10] is shown below in Figure 2-5, which the copper track has a 10μm × 4 μm cross section. At higher frequencies, the surface current density is much higher than at the center. On the other hand, the proximity effect also increases the AC resistance of on-chip inductors at high frequencies due to the influence of the magnetic field created by a nearby conductor [11]. A sample simulation result shown in Figure 2-6 explores the proximity effect. In Figure 2-6(a), the AC currents of two nearby conductors are flowing in the same direction; thus, the halves of the conductors in close proximity are cut by more magnetic flux lines than the remote halves. As a result, the current distribution is not even throughout the cross section, and a greater proportion of current is being carried by the remote halves. Conversely if the currents are in opposite directions, the halves in close proximity will carry the greater density of current as shown at Figure 2-6(b). The resulting current crowding is termed the proximity effect, which will significantly increase the AC resistance of the inductor.

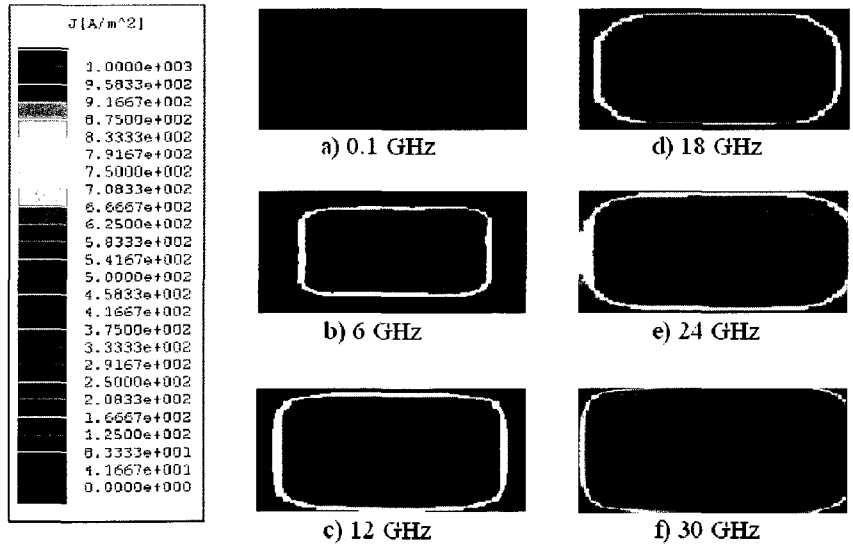


Figure 2-5: Current distribution for a 10μm × 4 μm copper line at different frequencies, a) 0.1GHz, b)6GHz, c) 12GHz, d) 18GHz, e) 24GHz, f) 30GHz

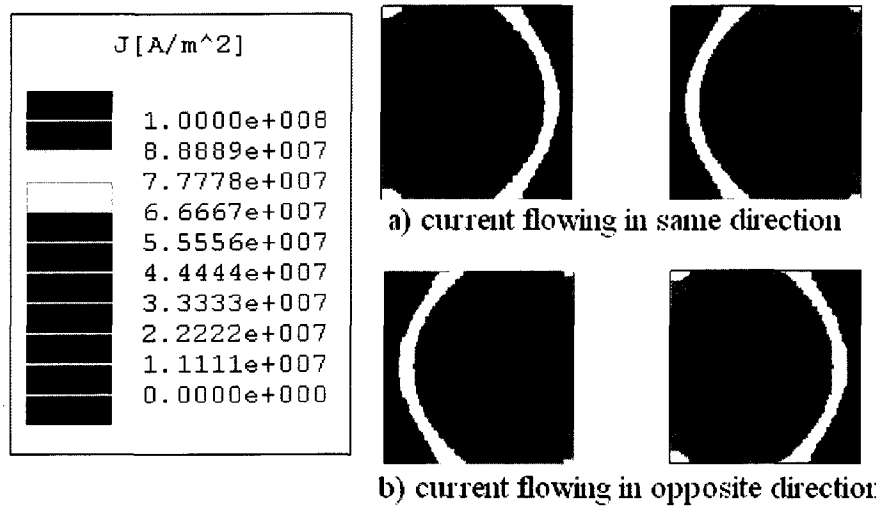


Figure 2-6: Proximity effect, a) current flowing in same direction, b) current flowing in opposite direction

2.2.2 Substrate Loss

The substrate loss also reduces the performance of the on-chip inductors at high frequencies. Typically the substrate resistivity of low-cost commercial CMOS is in the order of 1-2Ω-cm, which is considerably lower than the resistivity of bipolar and BiCMOS processes [12].

The dielectric stack between the different metal layers of an on-chip inductor and the conductive substrate creates parasitic capacitances, as shown in Figure 2-7(a). Having larger parasitic capacitances does not directly reduce the Q factor of the inductor but they do reduce the self-resonance frequency f_{res}, such that the inductor starts behaving like a capacitor rather than an inductor above this frequency. In addition, the displacement currents, as shown in Figure 2-7(b), will couple through these metal-to-substrate parasitic capacitances into the conductive substrate where power is dissipated resulting in capacitive losses [9].

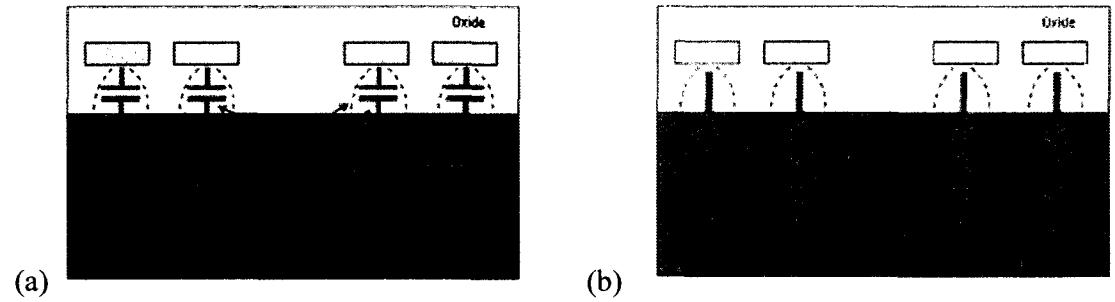


Figure 2-7: (a) Metal-substrate parasitic capacitances, (b) Displacement currents due to the metal-substrate parasitic capacitances [8]

Meanwhile, eddy currents in the substrate and in the inner most inductor turns cause additional power dissipation. A cross section of a circular inductor is shown in Figure 2-8 [12] which shows the magnetic flux generated by the inductor current penetrating into the substrate and the inner most inductor turns and thereby inducing eddy currents. These eddy currents flow in the opposite direction to the current carried by the inductor, resulting in magnetic fields that oppose the change of the original magnetic field due to Lenz's law. Therefore, the ratio between the magnetic flux and the current in the spiral inductor will decrease, resulting in a lower inductance value. In addition, this phenomenon also diminishes the energy in the inductor as the overall magnetic flux decreases; hence, the Q factor of the inductor is lowered. Since CMOS substrates have a low resistivity, the eddy current effect is more significant than in other silicon processes [12].

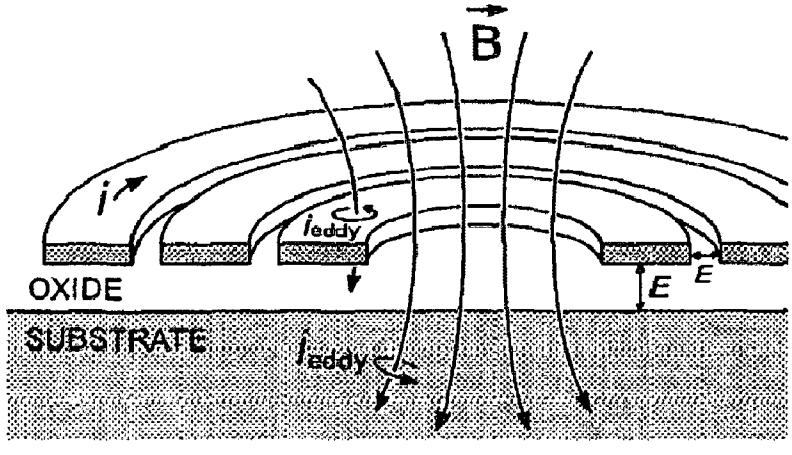


Figure 2-8: Eddy currents [12]

2.3 Fabrication Process Background

The need for high-performance passive elements has become increasingly important because the technology and integration requires high functionality and low cost for different applications. Understanding the IC fabrication process can help to use the features of a technology in order to design high-performance passive elements in a smaller area, with higher Q factor, or higher self-resonance frequency f_{res} for different applications.

With the rapid development of CMOS fabrication technologies, the thickness of the silicon-oxide layer has been increased in order to provide more levels of metallization for higher integration and copper interconnects have been widely implemented to reduce the metal series resistance. Figure 2-9 shows the Cross section view of the IBM-0.13μm CMOS process [13] as an example of an existing technology. The diagram shows 8 levels of metal, including 3 layers of thin metal wiring (M1, M2, and M3), 2 layers of thick metal (MQ and MG), and 3 RF wiring layers (LY, E1, and MA). With the availability of the metallization options, using the thicker top-metal layers can help to design higher Q inductors for lower metal loss. On the other hand, lower level metals, such as M2, M3, MQ and MG, can be used to design 3-D stacked inductors with a smaller area and higher self-resonance frequency f_{res}. Hence, designers have a higher degree of freedoms to develop high performance miniature inductors.

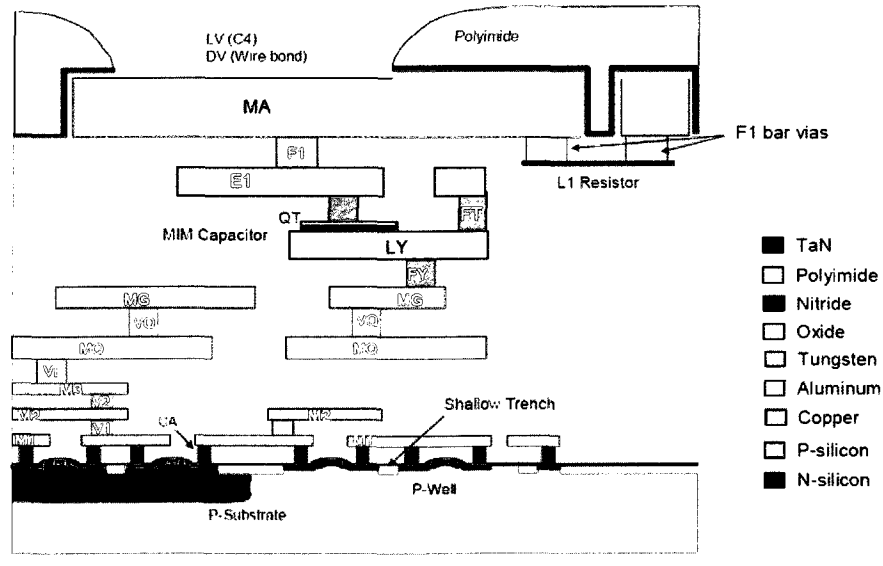


Figure 2-9: Cross section view of IBM-0.13μm CMOS 8 level metallization process [12]

2.4 Numerical Methods in EM Simulators

To explore the performance of inductors, EM simulators are used, such as ADS momentum, Sonnet, and HFSS. These simulators use different computational electromagnetic (CEM) techniques to find solutions to Maxwell's equations for problems specified by a given geometry and material properties. In this case, stacked inductors designed in IBM 0.13μm CMOS technology will be modeled through these simulators and the results will be compared with measurements in a later chapter. Some material properties will not exactly match but the relative performance of the structures should be consistent. Two major electromagnetic computational methods are used by common EM simulator tools such as ADS momentum, Sonnet, and HFSS.

Both Momentum and Sonnet use the Method of Moments (MoM). They are called "2.5-D" simulators because they have fields for three dimensions but the sources or currents of these fields are confined to a two dimensional plane [14]. Momentum uses the form? of MoM that assumes that substrates go to infinity in all directions, and uses an Integral Technique to solve the problem. Sonnet uses a form of MoM that assumes that the problem space is bounded by perfect electric conductor (PEC) walls, and because of this can use FFTs to compute the Green's function integral. The geometries in these two simulators are defined in layers from a planar point of view. The simulator focuses on the metal conductors on each plane and the dielectric stack is defined by thicknesses and electromagnetic properties [15].

On the other hand, HFSS is a fully 3-D simulator that utilizes the Finite Element Method (FEM). Simulators that are fully three dimensional have much more freedom to define the problem in space and are not restricted only to two dimensional planes. It is ideal for waveguides, antennas and other similar, real 3-D structures, such as stacked inductors since the metal thicknesses are different from one level to another. Simulators that are not fully 3-D have difficulty modeling these structures accurately [15].

2.4.1 Methods of Moments

The MoM is probably the most widely used numerical technique in RF CEM for antenna and passive component engineering. In the method of moments, the radiating/scattering structure is replaced by equivalent surface currents. This surface current is discretized into wire segments and/or surface patches, which are the meshes in the simulators. In a more homogeneous area of the structure the divisions can be larger and where large non-uniformities are present, there will be a denser mesh. This process is known as graded or irregular meshing. As an example, Figure 2-10 shows the mesh of a stacked inductor generated by ADS momentum, which is only the surface mesh. When using Momentum in ADS, since the mesh does not define inside the conductor and only on the surface, the metal tracks need to be defined as thick metal in order to explore the skin depth. A matrix equation is then derived, representing the effect of all the meshes on the surfaces of the structure. Then the matrixes are solved by using the free-space Green function. The relevant boundary condition is then applied to the whole Green functions yielding a set of linear equations. The solution of this linear system yields the current on each mesh. The resulting matrix which must be factored or used in an iterative solution scheme is fully populated, with complex valued entries. Typical matrix dimensions range from some hundreds for small antenna problems to several thousand – the upper limit is imposed by computational limitations, either limited memory and/or excessive run-time [16].

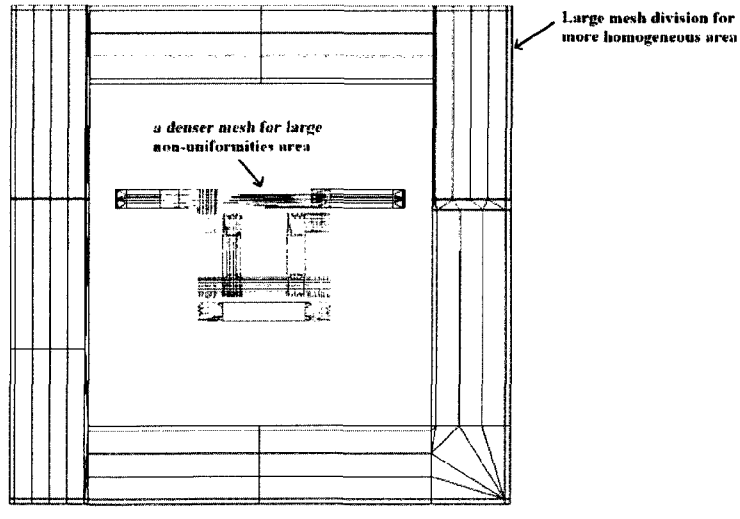


Figure 2-10: An example of a stacked inductor mesh in ADS momentum

Using MoM has several advantages, such as efficient treatment for perfectly or highly conducting surfaces. Only the surface is meshed; no "air region" around the antenna need be meshed. So it is good for patch antennas, planar inductors and inter-digititated capacitors, etc. The MoM automatically incorporates the "radiation condition" – i.e. the correct behavior on the far field effect. This is very important when dealing with radiation or scattering problems, such as antennas, coupling from nearby structures, etc. The MoM uses the current density as a working variable; hence, it is able to derive the expressions of impedance, losses, gain, and radiation patterns, etc for antennas and passive components via numerical integration. Efficient formulations can be derived for stratified media, such as printed circuit boards, microstrips, and printed antennas, etc [16].

On the other hand, there are also some disadvantages with using MoM. First of all, the MoM does not handle electromagnetically penetrable materials as well as differential equation formulations. Thus, if materials are homogeneous, equivalent surface current formulations is a sufficient, but for real 3-D structure, such as stacked inductors, which is constructed with inhomogeneous dielectric materials, equivalent volumetric currents are required to solve the problem faster and more accurately. In addition, the MoM does not scale gracefully with frequency for typical applications requiring a surface mesh. Doubling the frequency can result in an increase in the run-time by 64 times. This is a major problem present in all the computational methods, although the details do vary slightly from method to method. For a MoM volumetric mesh, required by 3-D structure, the scaling of the mesh is much larger; this has limited the application of MoM for 3-D structure EM computation [16].

In conclusion, the MoM is the preferred method for frequency domain radiation and scattering problems involving perfectly or highly conducting wires and/or surfaces. If the problem involves inhomogeneous dielectric materials, it is unlikely to be the best formulation, but if hybridized with the FEM a very efficient formulation can result [16].

2.4.2 Finite Element Method

Unlike MoM, FEM handles inhomogeneous materials and complex 3-D structures; hence, it deals with the problems in more complicated mesh generation rather than in electromagnetic theory [16]. The unknown field of the 3-D object is discretized using a finite element mesh rather than just meshes on the surfaces. An example in Figure 2-11 (number is strange) shows the meshes of a stacked inductor generated by HFSS, which is much more complicated than the meshes on the object's surfaces. Typically, triangular elements are used for surface meshes and tetrahedrons for volumetric meshes as shown in Figure 2-11, although many other types of elements are available. In addition, triangles and tetrahedrons are the simplest geometrical forms with which two-dimensional and three-dimensional regions respectively can be meshed [16].

Using FEM has several advantages. First of all, it is a very straightforward treatment of complex geometries and material in homogeneities. Secondly, it can easily handle the dispersive materials that have frequency-dependent properties. Moreover, potentially it has better frequency scaling than the MoM, although the requirement to mesh a volume rather than a surface will generate a much larger number of unknowns in the problem. It is also a straightforward extension to higher-order basis functions. In a simulator, this option can be enabled to obtain more accurate numerical results at the cost of computational complexity and time. It is also possible to use conformal elements to better approximate curved geometries [16].

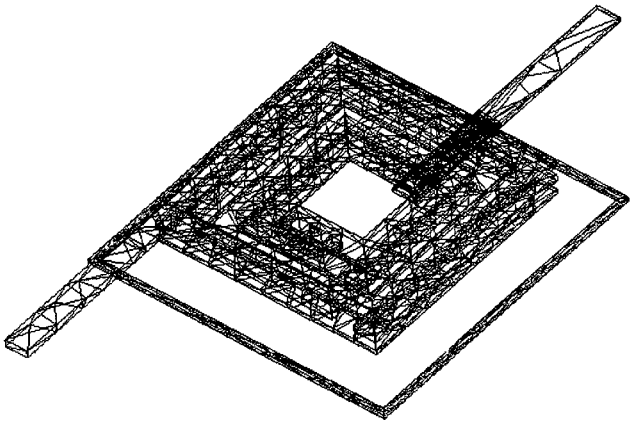


Figure 2-11: An example of stacked inductor mesh in HFSS

On the other hand, there are also some disadvantages with using FEM [24]. It is an inefficient treatment of highly conducting radiators when compared to the MoM due to the requirement to have some mesh between the radiator and the absorber. The FEM meshes can become very complex for large three-dimensional structures; indeed, some designers have reported mesh generation times starting to exceed solution time [16].

In conclusion, the FEM is the preferred method for microwave device and 3-D structures simulation, such as waveguides, antennas, and stacked inductors etc. Using FEM/MoM hybrids, scattering problems involving electromagnetically penetrable media and specialized antenna problems can be accurately and efficiently solved [16].

Chapter 3 On-chip Isolation Techniques

On-chip isolation has significant impact on IC performances due to higher integration levels, higher frequencies, and tighter specifications for present and future products. Higher integration results in more transistors switching, and thus, more noise creation. In addition, it also puts on-chip antennas, inductors, and other noisy and sensitive components together on the same chip that were on separate chips in the past. At higher frequencies noise can couples more easily from place to place through the low resistivity substrate, and isolation provided by wells is reduced. With the tighter specifications of new products and the increased radiations of the circuit components due to coupling at high frequencies, the RF designer must be both knowledgeable and creative to find an effective solution for maximizing on-chip isolation [17].

Understanding of the impact of process technology, grounding effects, guard rings, shielding, and decoupling is necessary to optimize isolation. This section reviews some of the issues of current techniques that affect on-chip isolation. The challenge in addressing this concept is that most of the effects are interdependent [17].

3.1 Shallow Trench Isolation

Shallow trench isolation (STI), also known as the "Box Isolation Technique", is an integrated circuit feature which prevents electrical current leakage between adjacent semiconductor device components. STI has become the standard isolation structure for sub-micron silicon CMOS technologies since 1996, and was first used in 0.25μm CMOS process [18]. STI is created early during the semiconductor device fabrication process, before transistors are formed. As shown in Figure 3-1 [18], the key steps of the STI process involve etching a pattern of trenches in the silicon, depositing one or more dielectric materials, such as silicon dioxide, to fill the trenches, and removing the excess dielectric using a technique such as chemical-mechanical planarization. Hence the devices or groups surround by the higher

resistance trench region can be isolated from other parts of the chip in order to reduce noise or signal coupling through the substrate.

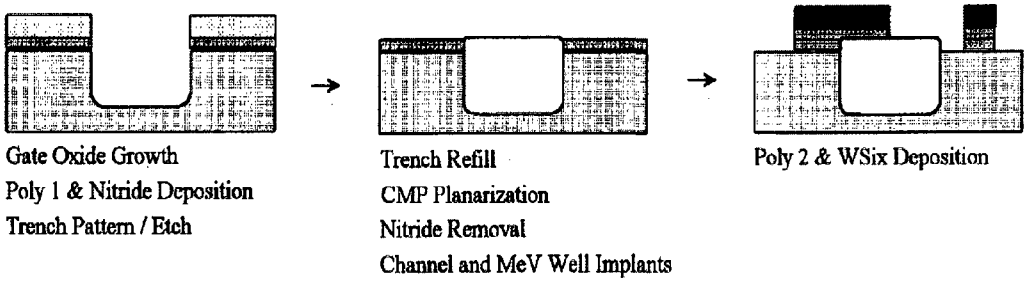


Figure 3-1: Sample process sequence of shallow-trench isolation in 0.25μm CMOS technology [18]

Meanwhile, rather than etch and fill a silicon dioxide region to form the STI, some technologies, such as the IBM-0.13μm CMOS process, use an additional mask to block P-well and N-well implants from the mask region to create regions of high resistivity to form the STI. Figure 3-2 [13] shows the process cross section and mask levels of the additional layer structure to form the STI. The green region is the low-doped region, which creases the p-well implant block shape on the additional lithography mask. As a result, integrating an on-chip inductor above the STI region can reduce the eddy current effect due to the high resistivity. For the kit inductors, this option is always incorporated; however, for customized inductors, designers need to enable this option and use it in order to reduce the eddy current effect.

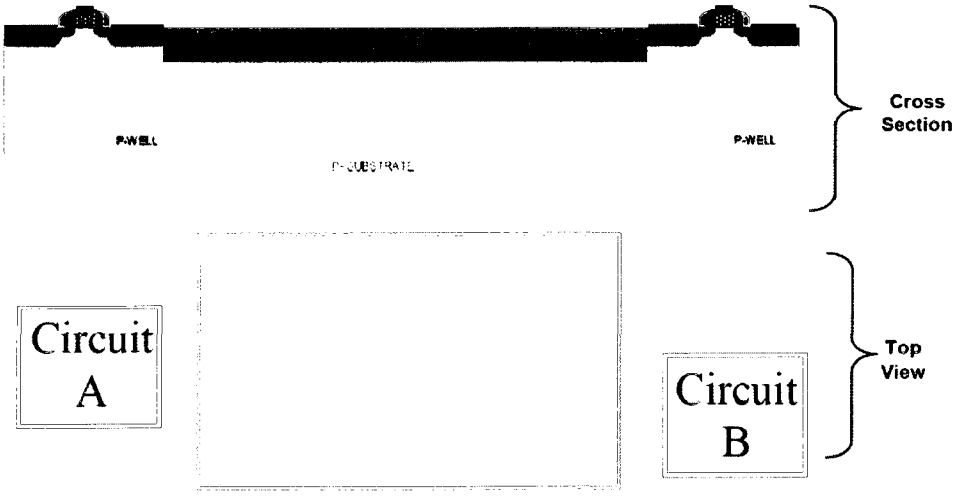


Figure 3-2: Cross section of additional mask to form the STI [13]

3.2 Guard Rings

Digital circuits generate significant switching noise, which is coupled into the substrate through the source/drain junction capacitances, bulk terminals, and wiring. This noise signal can travel through the substrate, where it is introduced into sensitive analog circuits though various paths. This phenomenon is much more severe at high frequencies in that not only the switching noise will couple to the passive components through the low resistive substrate resulting in lower Q factor, but the noise will also radiate from the inductors to the other circuitry on the chip. Thus, guard rings around a sensitive circuit help to decouple noise from the circuit and ensure that noise will couple equally into both sides of a differential design; in addition, guard rings around a noise source provide a low-resistance path to AC ground for the noise and help minimize the amount of noise injected into the substrate [17].

The guard ring technique consists in placing biased P+ or N+ diffusion regions surrounding the core analog/RF circuitry, which is required to connect to a quiet ground. As shown in Figure 3-3, the red rings represent the substrate contacts, which are connected to ground or the negative power supply if the substrate is not at ground. The STI region is shown in green between the two substrate rings. For an inductor, the guard ring is usually placed at a distance of about five line widths away [17]. The efficiency of guard rings depends on the noise frequency and package inductance.

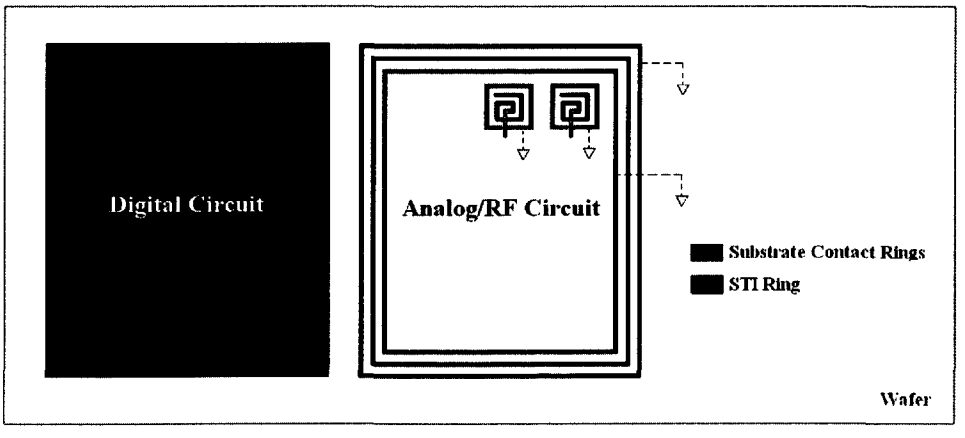


Figure 3-3: Sample guard rings isolation structure

3.3 Guard Ring with Gaussian Side Walls

The traditional planar on-chip inductor is made using top level metals in order to enhance the Q factor. If adding a guard ring using the top level metal to the planar inductor, the routing of the inductor will not be able to use the top level metal and also will make the routing complicated. However, it is unnecessary to add top level metal to reduce the noise and coupling effects. However, for the small stacked inductors, 3-D inductors that are made by low level metals, adding Gaussian side walls (GSW) surround the stacked inductors can help to further reduce their coupling effects, which is extending the idea from guard rings around a noise source to provide a low-resistance path to AC ground for the noise and help minimize the amount of noise injected into the substrate. Since the stacked inductors have multiple levels of metal, Gaussian side walls can provide a more efficient AC ground to different metal levels. Hence, signals will be further isolated from outside. The height of the side walls can be built by stack up the metals from the guard ring and through the vias to one level higher than the inductor top level metal. In simulation, the GSW is simply to copper wall instead of multi-level metals and vias, as shown in Figure 3-4.

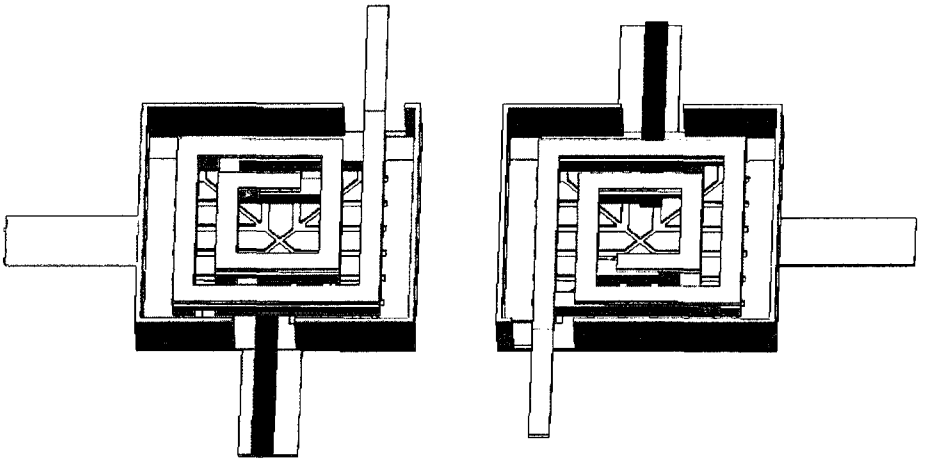


Figure 3-4: Single ended inductors with Gaussian side walls isolation

Base on simulations, this technique has advantages in maximizing the isolation with minimum chip area. However, it still slightly degrades the Q factor and inductance since there are additional parasitic capacitance between the inductor metals and the Gaussian side walls.

3.4 Patterned Ground Shielding

Proper shielding for a sensitive signal line or a passive component is considered an effective analog/RF IC layout technique in order to reduce the noise coupling and substrate losses. The challenge is to determine the appropriate shield layer, bias potential, and layout pattern. Sensitive signal buses are often laid out with AC signal and shield lines to prevent crosstalk through lateral and fringing electric fields (i.e. using a slow wave structure or coplanar wave guide). Hence, in order to isolate the coupling from the signal lines to the substrate, n-well or diffusion layers can be placed under the lines to prevent noise coupling [17].

As mentioned in Section 2.2.2, on-chip inductors usually occupy substantial die area and thus are susceptible to coupling through the substrate. In order to reduce this substrate loss, a shield with low level metal layers or polysilicon layers can be built to block electromagnetic energy from coupling to the substrate. Due to the proximity effect of the inductor and the shield, if a solid metal shield is used, this will also allow the image eddy currents to flow in the shield; hence it will reduce the Q factor. As a result, the ground shield must be patterned, as in the examples shown in Figure 3-5. A patterned ground shield (PGS) only allows shield currents to flow perpendicular to the conductive paths of a spiral inductor, thereby preventing the majority of eddy currents which flow parallel to the device, reducing the substrate losses and enhancing the Q. However, as the distance from the inductor to the ground terminal are reduced, the shielding increases parasitic capacitance; thus causing the inductor's self-resonant frequency to drop significantly. For best performance, the patterned ground shield should be placed far away from the inductor, but remain above the substrate [19]. Typically, using the polysilicon layer will be a better choice than other low level metal layers.

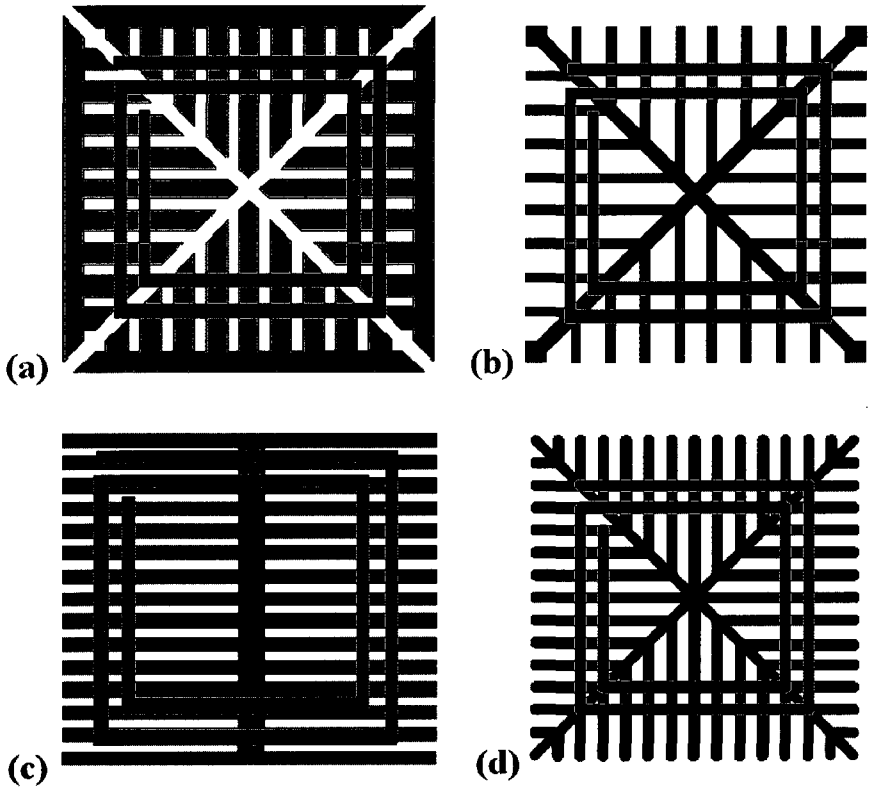


Figure 3-5: Example shapes of patterned ground shield, (a) & (c) Metal-1, (b) & (d) Poly

3.5 Gaussian Top Ground Plane

The traditional planar on-chip inductor is made with top level metals and needs to be "hollow" in order to enhance the Q factor. Hence, in general there is no circuit or wire routing underneath a big planar inductor. However, when building a small stacked inductor using low level metals, it is possible to reduce circuit area by placing wire routing on top of the stacked inductors. Therefore, modeling a stacked inductor using low level metals with a Gaussian top ground plane (GTGP), which can be used to explore the effect of the inductor with metal filled on top or with an AC ground path on top. Figure 3-6 shows two stacked inductors in IBM 0.13μm CMOS technology side by side with MA metals on top and the MA metals are connecting to ground. As the distance D is reduced and the top ground plane MA moves toward the stacked inductor, the coupling coefficient and mutual inductance is reduced by trading off the inductance and the Q factor. By careful modeling, the change in the metal thickness by

using different level metals stacked up for the top ground plane, the unwanted mutual inductance can be dramatically reduced by trading off small amount of the inductor performance. Therefore, modeling stacked inductors with metal filled on top or with AC ground paths on top can also minimize the chip area while maximizing the isolation for desired performance of a design.

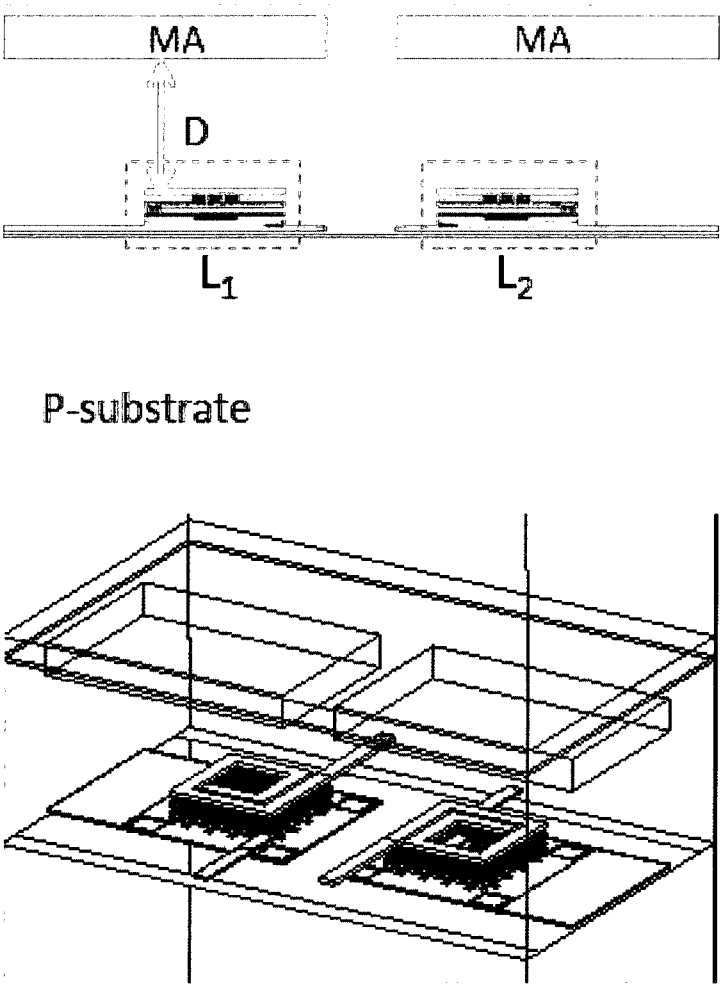


Figure 3-6: example of two stacked inductors with metal ground plane on top (a) 2-D view, (b) 3-D view

Chapter 4 Multispiral Stacked Inductor Design

Since the first stacked spiral inductor was proposed by H. J. Finlay in 1985 [20], many research and development activities had been conducted in order to implement the stacked spiral inductors in different applications by trading off the area, Q factor, and self-resonance frequency f_{res}. The general idea of the stacked inductors is that of multi-level inductors connected in series; hence, strong mutual coupling from the stacked up structure happen to allow the generation of the same inductance in less silicon area as compared to planar inductors.

In broadband high speed circuit design, a larger number of inductors are necessary for bandwidth enhancement. In order to reduce the cost for silicon area, stacked inductors are necessary, and in a peaking application, the inductors are in series with a resistor so Q is irrelevant.

In this chapter, the geometries of stacked inductors will be first discussed for trade-offs between area, Q factor, and self-resonance frequency. After that, the stacked inductor design procedures through the basic modeling in ASITIC. Then the compact equivalent model for simulation will be presented. Finally, different on-chip isolation techniques will be discussed in order to maximize the isolation in the smallest silicon area. The contribution for this chapter is included the new compact stacked inductor design flow and comparison between the stacked inductor simulation and measurement results.

4.1 Geometries of Multispiral Stacked Inductors

4.1.1 General Geometries of Multisprial Stacked Inductor

In general, the geometry of the multispiral stacked inductor could be squared, hexagonal, octagon, circular, etc, depending on the permitted angle between the metal tracks dictated by

the fabrication technology used. As an example, Figure 4-1 shows three inductors with different geometries.

In the same area with the same metal width, spacing, number of turns, and outer dimension, octagonal and circular geometries require less metal length to achieve the same number of turns. Thus series resistance is compressed and Q factor improved. On the other hand, the square shaped inductor will be the most area efficient. For example, for a square area on the wafer, a square shape will utilize 100% of the area, whereas hexagonal, octagonal and circular shapes use 65%, 82.8% and 78.5% respectively [21]. In an inductive peaking application, with the inductor in series with a resistor, having more inductance is more important than having higher Q factor; thus, the square shaped stacked inductor should be used in order to be area efficient with slightly lower self-resonant frequency due to higher parasitic capacitance. Square spirals, which have 90 degree segments, are more commonly found in earlier fabricated circuits due to difficulties in non-Manhattan geometries in design layout tools and fabrication foundries. Square spiral geometry was chosen for the research of this thesis because of the ease of its design.

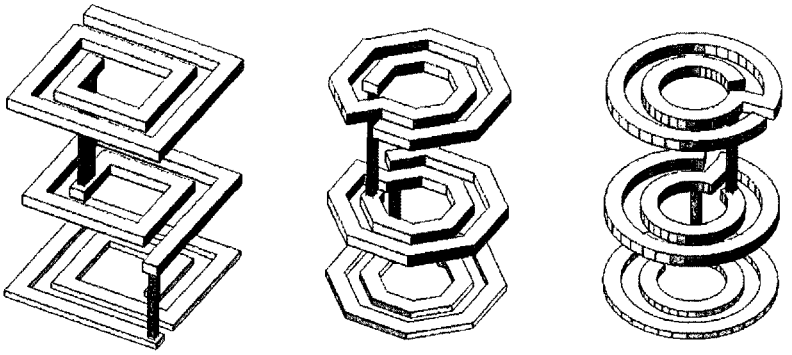


Figure 4-1: Examples of squared, octagonal, and circular multispiral stacked inductors

4.1.2 Square Tapered Multisprial Stacked Inductor

The square tapered geometry is shown in Figure 4-2(a) that has constant spacing but the metal width is tapered continuously in a linear fashion, which is designed to minimize the current constriction at high frequency.

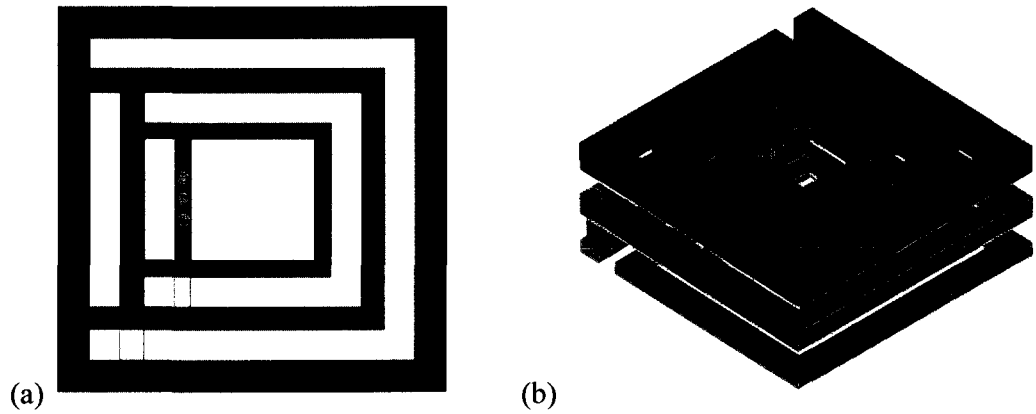


Figure 4-2: (a) top-view and (b) 3-D view of a three-turn tapered stacked inductor

Current crowding due to the skin effect and proximity effect causes non-uniform current flows at high frequency. Since at high frequency current crowding limits the current to the outer edges of the conductors, metal width does not have strong influence on minimizing the metal losses as at low frequency. Moreover, the magnetic field is strongest in the center of a spiral and thus the time-varying magnetic field produces eddy currents of greatest strength in the inner turns [21]. For these two reasons, decreasing the metal width of the inner turns and to effectively move these turns closer to the outer edge can reduce the eddy current effect to the inner turns. Furthermore, tapering can be an effective means of increasing the self-resonance frequency of a device by decreasing the cross-sectional area of the device [21].

4.2 Initial Stacked Inductor Design in ASITIC

4.2.1 Introduction to ASITIC

ASITIC, Analysis and Simulation of Spiral Inductors and Transformers for ICs, is a CAD tool for the RF circuit designer to analyze, model, and optimize passive and interconnect metal structures residing on a lossy conductive substrate. This includes inductors, transformers, capacitors, transmission lines, interconnect, and substrate coupling analysis [22]. ASITIC allows the circuit designer to plan and optimize the layout of a chip in the presence of magnetic and electrical interaction and coupling through the substrate and oxide layers of the IC, such as

eddy current losses due to the conductive substrate, skin effect and proximity effects, or eddy currents in the metallization [22].

ASITIC performs fast 2-D and 3-D method of moment simulations to model the given structure of the passive components. The calculations are performed an order of magnitude faster than general EM analysis tools. As an initial design tool, ASITIC has been demonstrated to be sufficiently accurate to estimate the inductance, Q factor, series resistance, and the self-resonance frequency f_{res} of a planar spiral inductor [23], [24]. For a multispiral stacked inductor, ASITIC can be used to estimate the inductance, which is quite accurate compared to the simulation results in Momentum and HFSS; however, the trend of the Q factor and self-resonance frequency f_{res} are usually over estimated for a 3-D structure. As a result, a 3-D simulator such as HFSS is necessary in order to explore the parasitic in a 3-D environment for more accurate estimation of the stacked inductor performance; and this will be discussed in next section.

4.2.2 Design Considerations using ASITIC

ASITIC uses a technology file that describes the substrate and metal layers of the process [22]. An example of an IBM 0.13μm CMOS technology file for ASITIC is shown in Appendix A. In ASITIC, a stacked inductor can only be designed as a square shaped structure, but this is good enough for an area efficient design. The designers are able to vary the number of stacked layers, the inductor's outer dimension, the metal width, the number of turns, and the spacing between turns, in order to optimize tradeoffs between area, Q factor and self-resonance frequency f_{res}.

The tradeoffs for design considerations on ASITIC can be summarized as:

(1) For a given driving current constrain, minimum metal width that can handle the operating current will be the first consideration for a design that has minimum area and the highest self-resonance frequency.

(2) For a given inductance value, increasing the number of stacked layers will result in more mutual inductance and therefore smaller area, but will increase the series resistance.

(3) Increasing the metal width of the inductor will decrease DC resistance, but will increase area and capacitance; thus, the self-resonance frequency f_{res}.

(4) Increasing the number of turns also increases mutual inductance, and therefore will result in smaller area, but will increase parasitic capacitances due to the larger area overlap to the substrate.

(5) Minimum spacing can be used to provide maximum coupling between the turns resulting in a smaller number of turns for higher inductance, but will increase the metal loss due to the proximity effect. The trade-off of using minimum spacing and smaller turns will depends on decreasing the amount parasitic capacitance between the metal to the substrate and the parasitic capacitance from the turn by turn metal tracks.

Thus, designing a stacked-inductor in ASITIC is an iterative process, but it is much faster than designing in a 3-D EM simulator. As mentioned in section 2.1, in most cases, the highest useful frequency of an inductor is much smaller than f_{res}, usually only 1/3 of the f_{res}, but ASITIC usually will over estimate f_{res} by 30% for a small stacked inductor structure based on simulation comparisons to momentum and HFSS. Designers should be aware of this and design the stacked inductor for high enough f_{res} in this initial estimation.

For inductive peaking applications, inductor area should be minimized and self-resonance frequency f_{res} should be maximized at the expense of slightly higher series resistance. Once the layout of a stacked inductor is created, the layout can be exported in CIF format from ASITIC, and imported into Cadence [34]. The designers can also export the stacked inductor layout from Cadence as a GDS II stream format, and import into ADS layout and HFSS to perform more accurate simulations in order to explore the broadband performance of the stacked inductor. The modeling procedures in ADS and HFSS are shown to Appendix-C.

4.3 Compact Inductor Models

A compact inductor equivalent circuit is necessary for both frequency domain and transient simulations in order to prevent long simulation times associated with the EM simulators while still modeling all the relevant energy loss mechanisms. It is essential to produce successful circuit design since inadequate capacitance modeling of an inductor leads to poor prediction of the self-resonance frequency, f_{res}; in addition, when applied to LC tuned circuits, the center frequencies may shift by 10% or more due to incorrect modeling [25]. Hence, a variety of equivalent circuit have been developed attempting to accurately model all of these concerns.

In ASITIC, once the layout of an inductor is created, it will generate a simple π model of the inductor for a specified frequency, as shown in Figure 4-3. However, this is only a narrow-band model and only valid for a particular frequency. Hence, additional work needs to be done in order to obtain a broadband model of an inductor for circuit design. For low-gigahertz applications, a single π broadband model shown in Figure 4-4 [26] may be sufficient to present the behavior of an on-chip spiral inductor. This model has the advantage of using the minimum possible number of circuit elements to reduce the complexity of the model. In order to create this single π broadband model, many of the narrow-band π models in Figure 4-3 can be generated for different frequencies in ASITIC and then reconstructed in Cadence. Using Spectre's S-parameter analysis, the four S-parameters (S_{11}, S_{21}, S_{12}, S_{22}) can be calculated for each narrow-band model; and then circuit s-parameters can be imported into HSPICE and using the bisection optimization method to curve fit the single π broadband model [27].

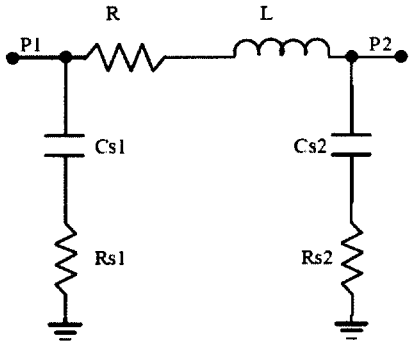


Figure 4-3: ASITIC narrow band inductor model

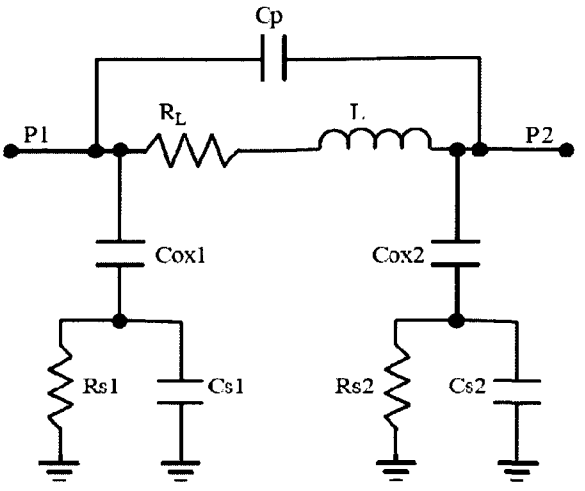


Figure 4-4: Broadband inductor π-model [26]

As the frequencies of application become higher and higher, a single π model is inadequate since half of the capacitance of the inductor in Figure 4-4 is connected to a small-signal ground. Instead, the distributed nature of the spiral structure is better described by the double- π model, as shown in Figure 4-5 [25].

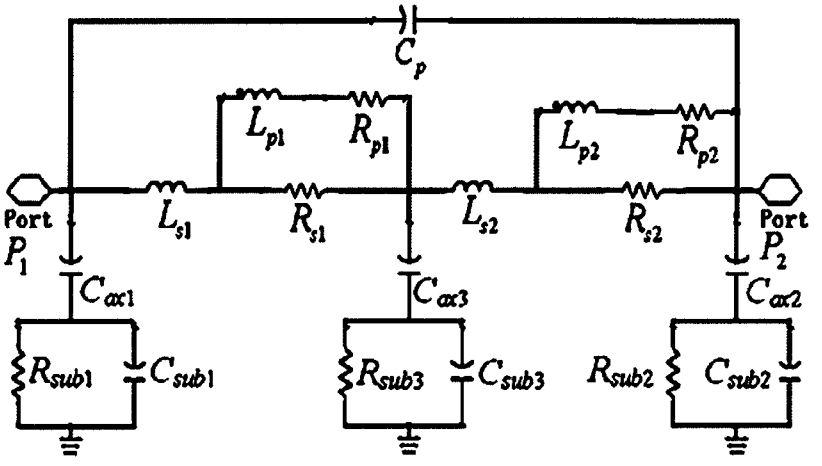


Figure 4-5: Compact double-π model of on-chip inductors [25]

Although the double-π model in Figure 4-5 accounts for better modeling of the behaviors for the on-chip spiral inductor, it is still not sufficiently accurate to capture the strong coupling effect of the multi-level metal stack inductors. A modified double-π model of on-chip inductors from [28], as shown in Figure 4-6, provides a better matched for performance

associate with different types of parasitic effects compared to the original double-π model in Figure 4-6 up to 100GHz.

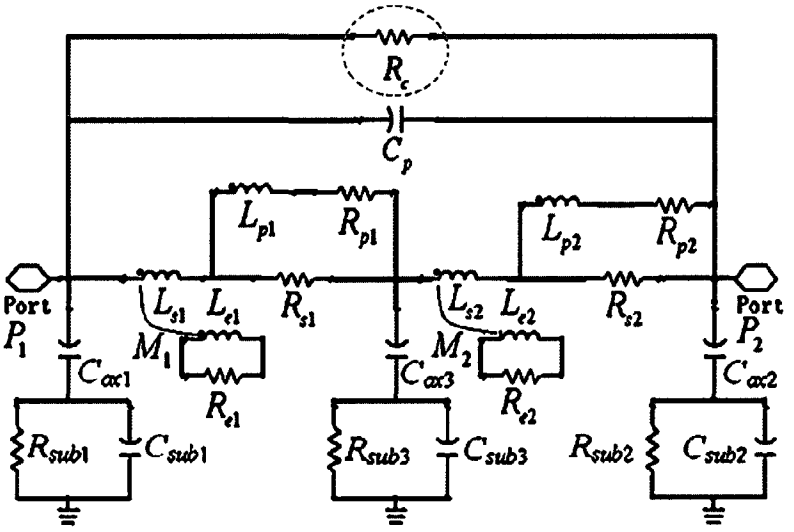


Figure 4-6: Modified double-π model of on-chip inductors [28]

For the model in Figure 4-7, two single loops (L_{e1}, M_1, R_{e1}) and (L_{e2}, M_2, R_{e2}) are used to model the effect of eddy currents induced within the heavily doped substrate for low cost silicon based technologies of CMOS. However, when modeling an inductor in an RF CMOS process with a lightly doped Si-substrate for which such eddy-current effects are normally insignificant and these two loops can be removed. Moreover, two series L-R branches (L_{p1}, R_{p1}) and (L_{p2}, R_{p2}) and two inductors L_{s1} and L_{s2} are employed to model the skin and proximity effects. The three-element C-R-C oxide-substrate models account for the capacitive substrate coupling. C_{ox} in the three-element model denotes the oxide capacitance, which can be partitioned into three parts C_{ox1}, C_{ox2}, and C_{ox3}. The parallel capacitance C_p accounts for the capacitive effects between metal windings and capacitance between each layer of the on-chip inductor. Finally, R_c is added into the conventional double-π model for the conductor loss arising from the magnetic field generated through the substrate return path under high frequency [28].

ADS optimization tools can implement the modified double-π model to do the curve fitting automatically. An example of using this method for the curve fitting for a stacked inductor is

shown in Figure 4-7 and shows that the double-π model results are very close to the simulation results for frequencies up to 100 GHz.

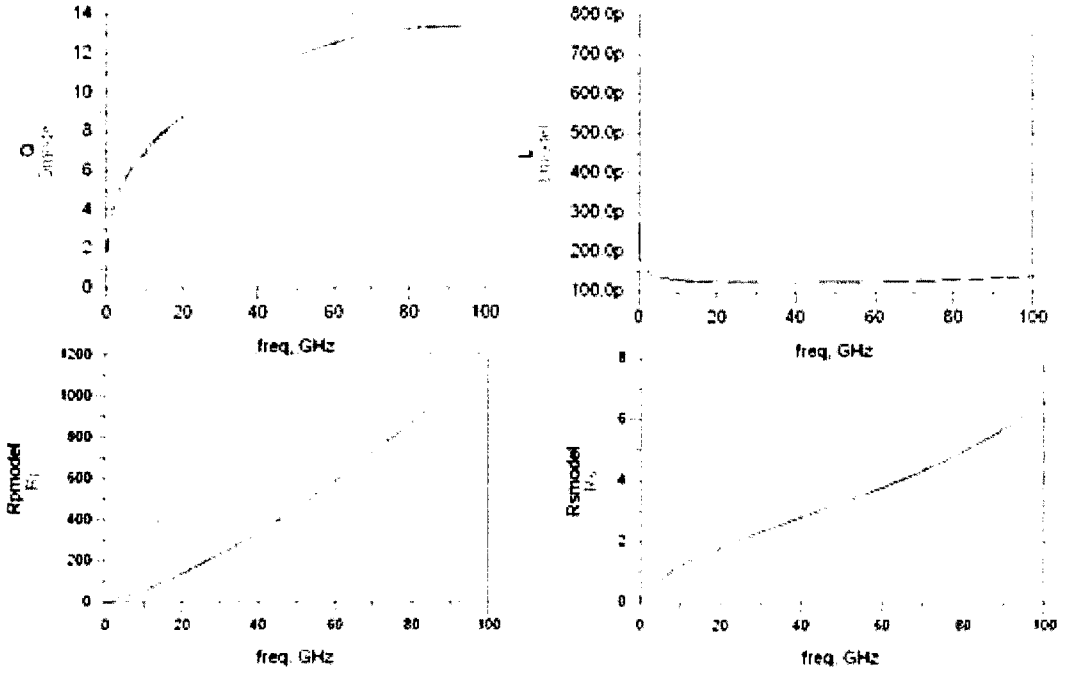


Figure 4-7: Sample stacked inductor broadband model curve fitting results using the modified double-π model of on-chip inductors

4.4 Stacked Inductor Simulation Results

The two stacked inductors implemented in this work's test chip have been simulated using HFSS using different isolation techniques. The simulation results will be presented in this section. Figure 4-8(a) shows the annotated layout of a stacked inductor, which has an inductance value of approximately 248pH, using 4 layers of metal (M5 to M2), with outer dimensions of 9.5μm×9.5μm, 1.5 turns, a trace metal width of 1.9μm, and spacing of 0.6μm; similarly, a second layout of a stacked inductor is shown in Figure 4-8(b), with an inductance value of approximately 430pH, 3 metals stacked layers (M5 to M3), 20μm×20μm outer dimension, 2 turns, 2μm metal width, and 2μm spacing.

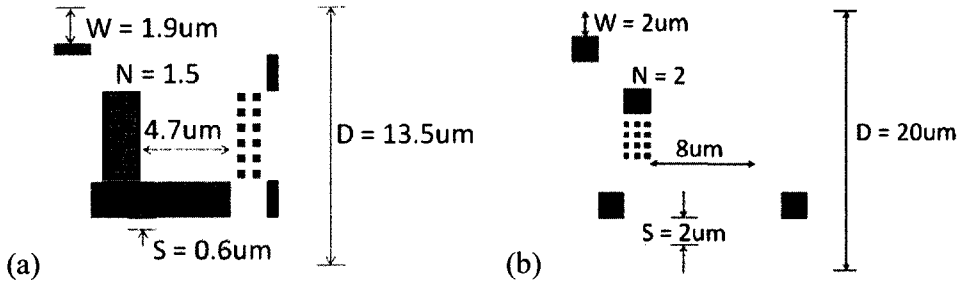


Figure 4-8: Two stacked inductors layout (a) 248pH and (b) 430pH

4.4.1 Two-port Simulation Results in HFSS

Figure 4-9 and 4-10 show the Q and L for the two stacked inductors presented in Figure 4-8 using two-port characterization, including inductors with and without patterned ground shields. Simulation results show that both stacked inductors have larger inductance values when the PGSs are not applied. However, the increasing in Q and the decreasing in L of the stacked inductors are not significant when the PGSs are applied.

The Q factor for the inductors presented here only increases slightly, which may be due to the fact that low level metallization used here is much thinner than the top level metals and the use of narrow metal width. As a result, the series resistance of the inductor increase; hence, reducing the Q factor, but the smaller cross sectional area will also reduce the uneven current distribution due to the skin effect and proximity effect where the center of the conductor is much closer to the surface. In addition, the stacked inductor has a very small center opening comparing to a traditional "hollow" planar inductor, the substrate loss will not be significant for the small stacked inductors.

According to Figure 4-9 and 4-10, the inductances for each set of inductors are almost the same. This is due to the much smaller overlap region of the inductor and the PGS compared to the planar inductors that have much larger overlap area. The inductance values are decreased when PGSs are applied. Specifically, if an M1 PGS is used, the distance between the inductor metal layers is minimized resulting in largest additional parasitic capacitance; hence, decreasing the inductance when compared to inductors that use a poly based PGS.

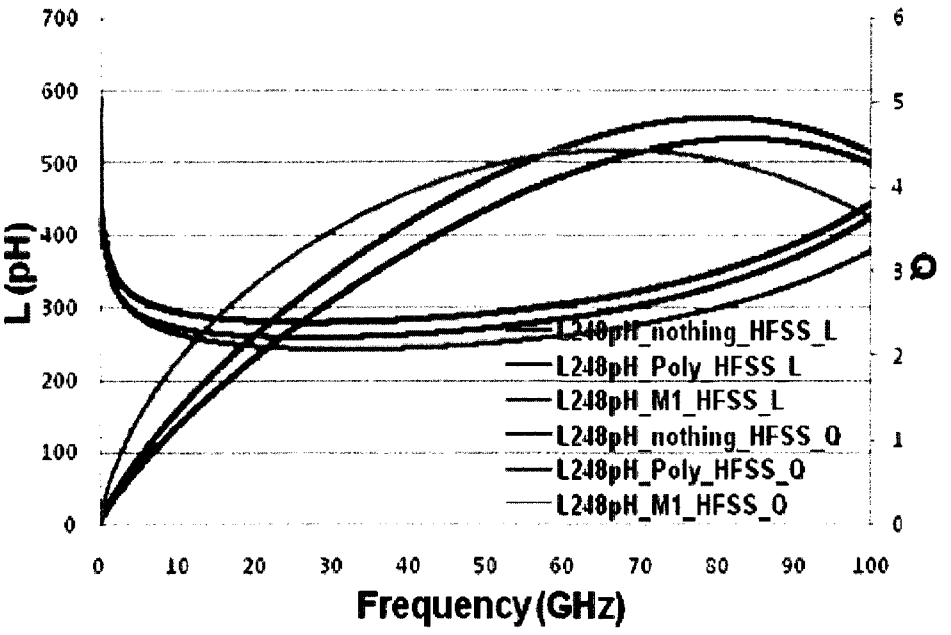


Figure 4-9: Compared the Q and L of the 248pH stacked inductor with M1 or poly PGS

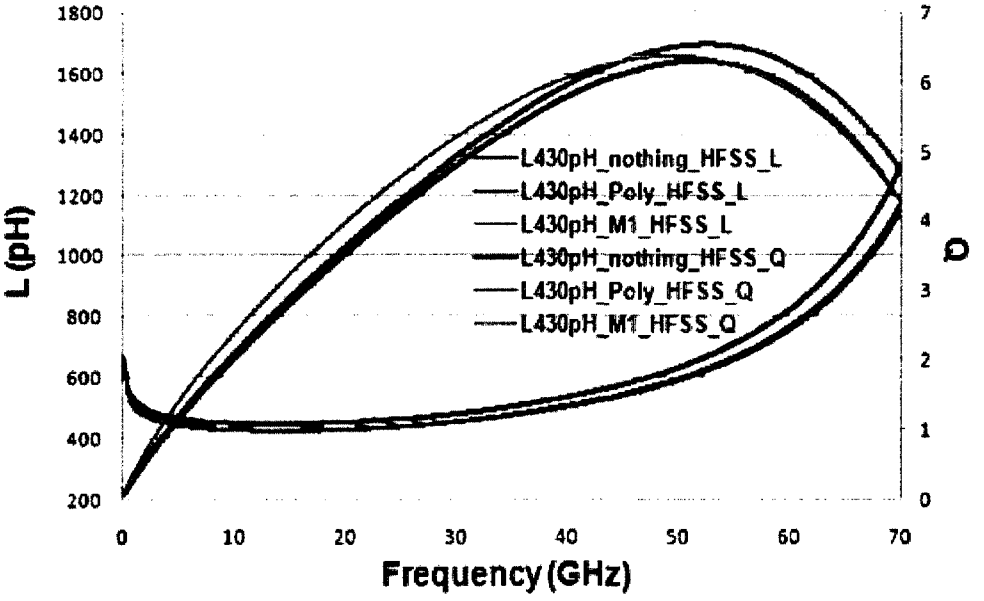


Figure 4-10: Compared the Q and L of the 430pH stacked inductor with M1 or poly PGS

4.4.2 One-port Simulation Results in HFSS

Two identical single ended stacked inductors were placed as shown in Figure 4-11. These inductors were used to explore the coupling effect of stacked inductors with different isolation techniques as mention in Section 3.3 to 3.5. Figure 4-12 to 4-15 compare the Q, L, coupling coefficient k and mutual inductance M of the 430pH stacked inductor with different isolation techniques respectively, including the reference structure (guard ring only), poly PGS, M1 PGS, LY top Gaussian top ground plane, and Gaussian side wall. Table 1 summarizes the performance of the 430pH stacked inductors, including the L, Q_{peak}, self-resonance f_{res}, coupling coefficient k and mutual inductance M.

The summary results show that adding a PGS to the small stacked inductor has no significant effect on the Q factor, which is similar to the two port simulation results. The top available metal ground plane LY, and GSW techniques provide similar isolation performance to reduce coupling effects in the stacked inductor. However, the LY top techniques reduce the Q, L and the self-resonance f_{res} by 10% or more; whereas, the GSW techniques only reduce the Q factor by about 2%, the inductance L and the self-resonance f_{res} is also reduced by about 10%. Therefore, the use of PGS is not necessary recommended for the super compact stacked inductor, and the GSW can be chosen to provide maximum isolation for certain application with no significant effect on the Q, L and the self-resonance f_{res}.

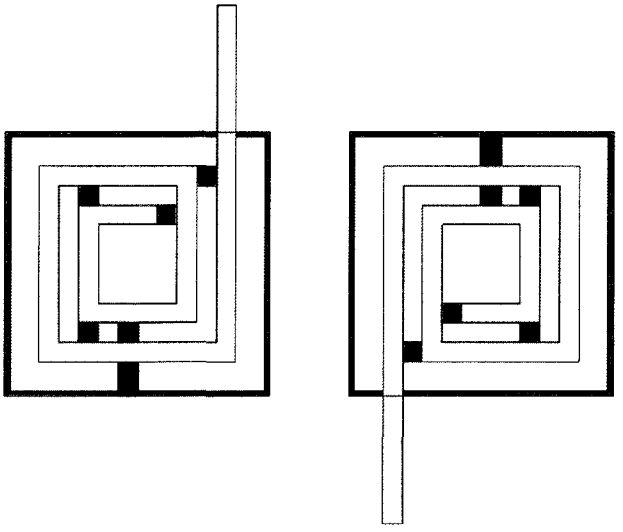


Figure 4-11: Two single ended 430pH stacked inductors place side by side

Table 1: Performance summary of the 430pH stacked inductors with different isolation

Isolation	Nothing	Poly PGS	M1 PGS	LY top	GSW
L(pH) @ 30GHz	417.87	407.74	377.85	368.05	385.83
L (%)	ref	-2.425	-9.578	-11.923	-7.668
f_{res} (GHz)	101	98.8	96.8	91.2	93.8
f_{res} (%)	ref	-2.178	-4.158	-9.703	-7.129
Q_{peak}	6.326	6.571	6.471	5.503	6.176
Q_{peak} (%)	ref	3.870	2.289	-13.014	-2.371
k @ 30GHz	0.04097	0.03917	0.03594	0.02441	0.02244
k (%)	ref	-4.4	-12.3	-40.4	-45
M (pH) @ 30GHz	17.13	15.92	13.57	9.01	8.66
M (%)	ref	-7	-21	-47	-49

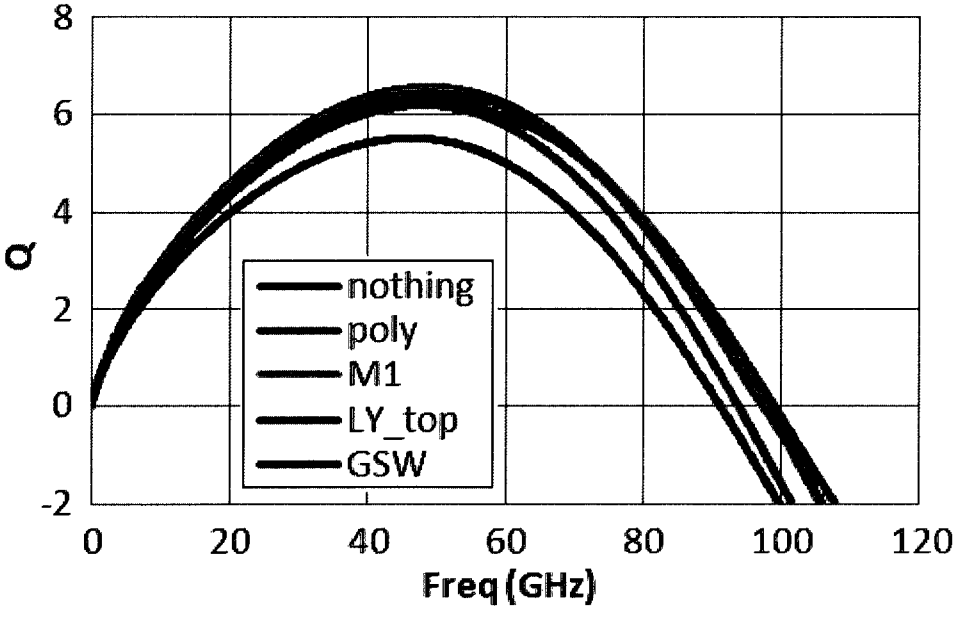


Figure 4-12: Simulated Q of the 430pH stacked inductor with different isolation schemes

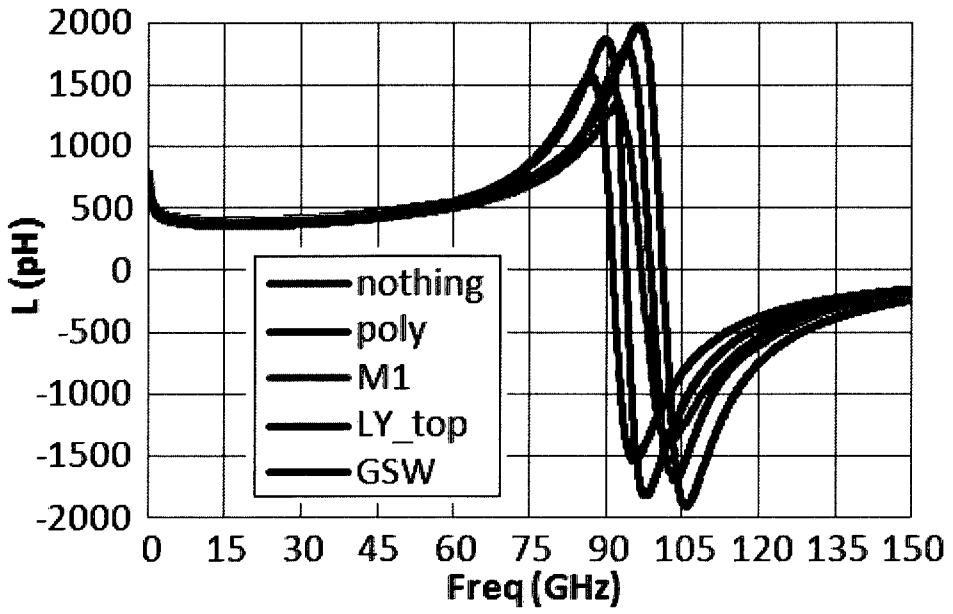


Figure 4-13: Simulated L of the 430pH stacked inductor with different isolation schemes

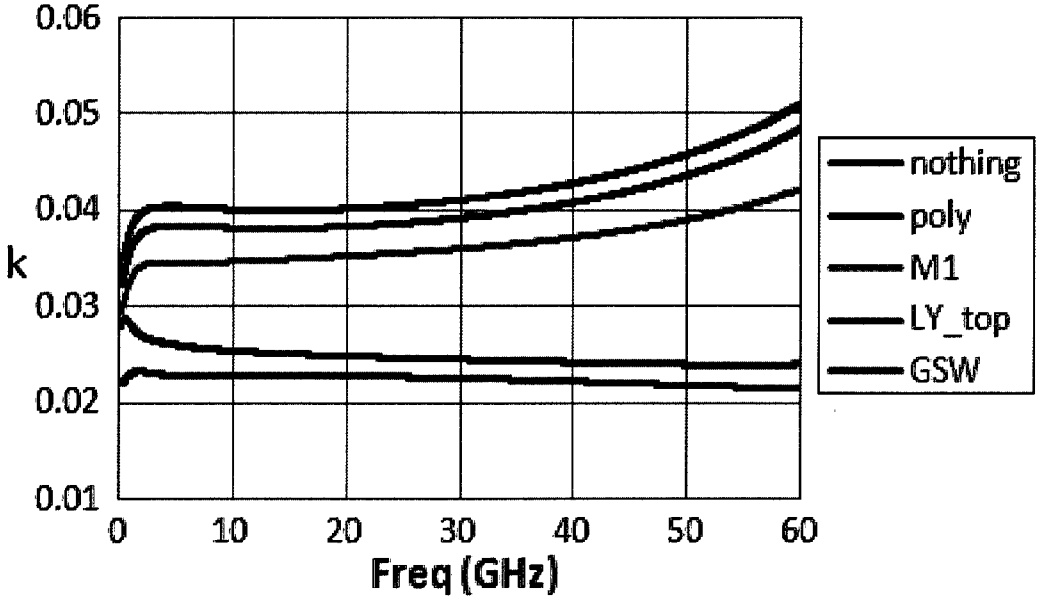


Figure 4-14: Simulated k of the 430pH stacked inductor with different isolation techniques

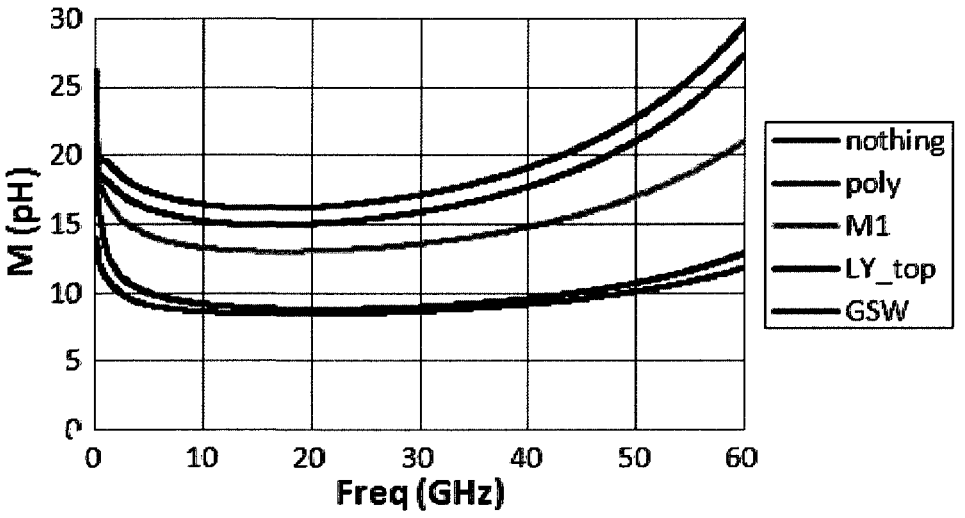


Figure 4-15: Simulated M of the 430pH stacked inductor with different isolation techniques

As mentioned in section 3.5 and Figure 3-6 (a), when the distance D from the GTGP to the inductor is reduced, the coupling coefficient k and mutual inductance M will be reduced by decreasing in the inductance L and the Q factor. Figure 4-16 shows the simulated Q and L of the 430pH stacked inductor with GTGP isolation, which has significant effect on the Q and L by changing the distance D of the top ground plane from the metal LY to top metal MA.

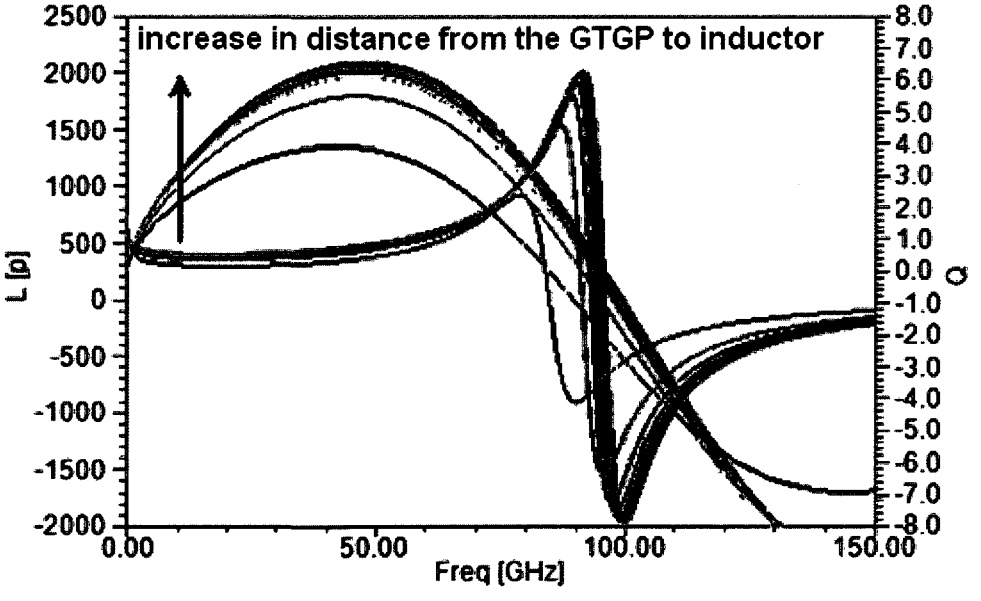


Figure 4-16: Simulated Q and L of the 430pH stacked inductor with GTGP isolation

Figure 4-17 shows that as the top ground plane moves closer to the inductor by reducing the dielectric isolation between these metal layers, the self-resonance frequency, L, and peak Q are also reduced dramatically. On the other hand, the coupling coefficient k and mutual inductance M are reduced by about 47% as shown in Figure 4-18.

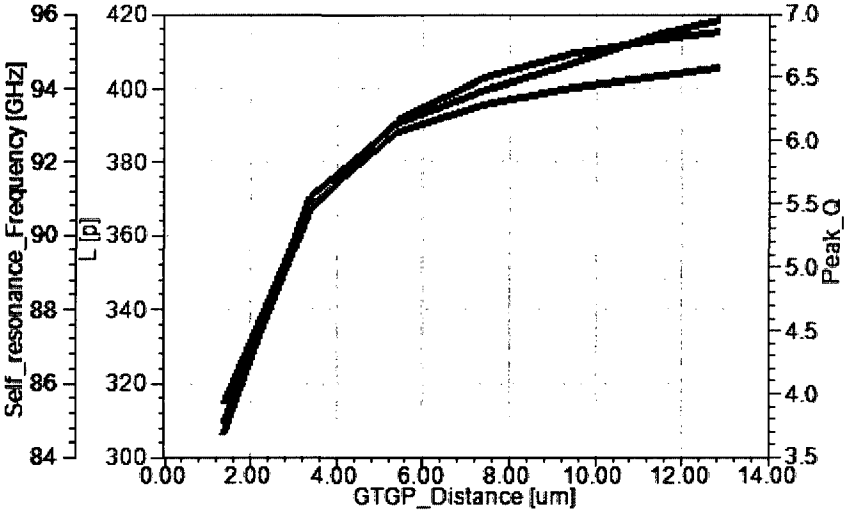


Figure 4-17: Self-resonance frequency, L, and peak Q of the 430pH stacked inductors with GTGP isolation vs. distance of the TGP

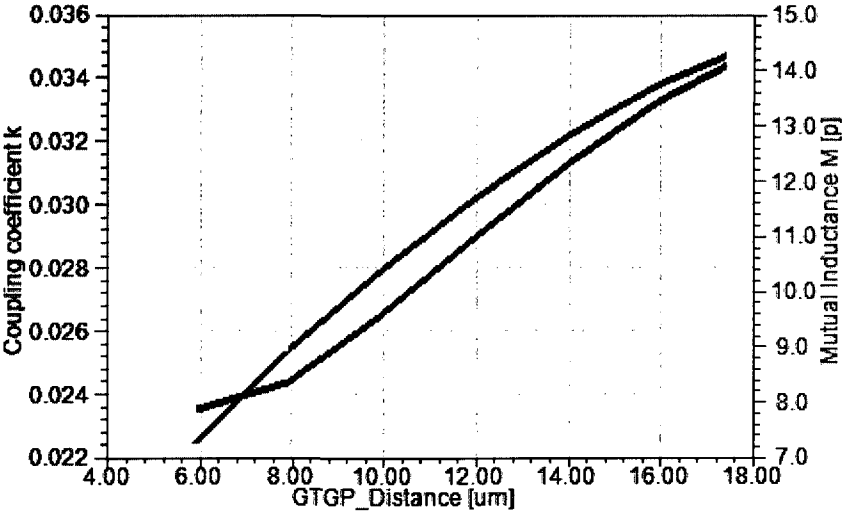


Figure 4-18: Coupling coefficient k and mutual inductance M of the 430pH stacked inductors with GTGP isolation vs. distance of the TGP at 30 GHz

Figure 4-19 shows the simulated Q and L values of the 430pH stacked inductor with GSW isolation that the height of the Gaussian side wall increased from the guard ring to the same height of the stack inductor. As shown in Figure 4-20, the use of GSW isolation has less effect on the Q, L and f_{res} of the stacked inductor compared to the use of GTGP isolation. According to Figure 4-21, the coupling coefficient k and mutual inductance M also can be reduced by about 49% showing that this technique is similar to the GTGP isolation technique.

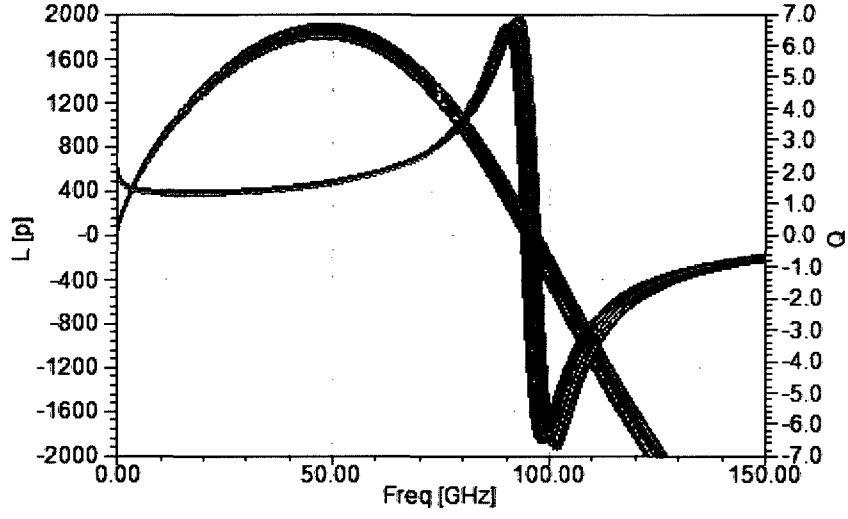


Figure 4-19: Simulated Q and L of the 430pH stacked inductor with GSW isolation

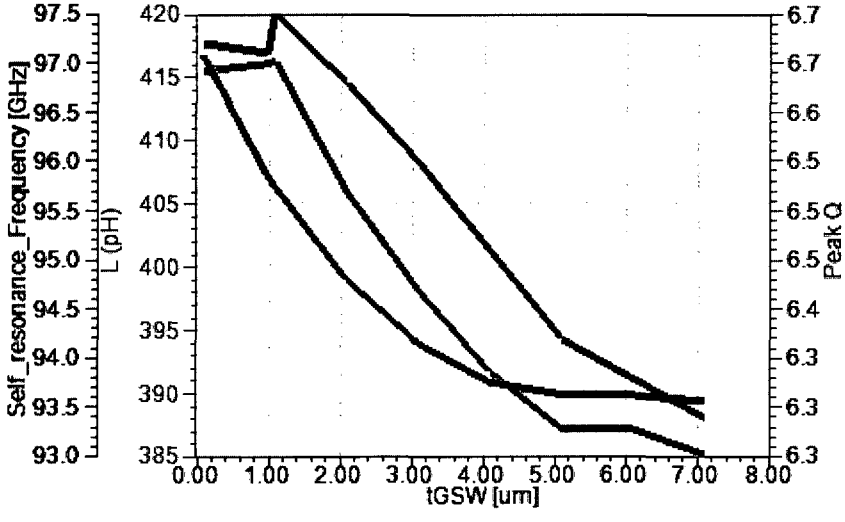


Figure 4-20: Self-resonance frequency, L, and peak Q of the 430pH stacked inductors with GSW isolation vs. thickness of the GSW

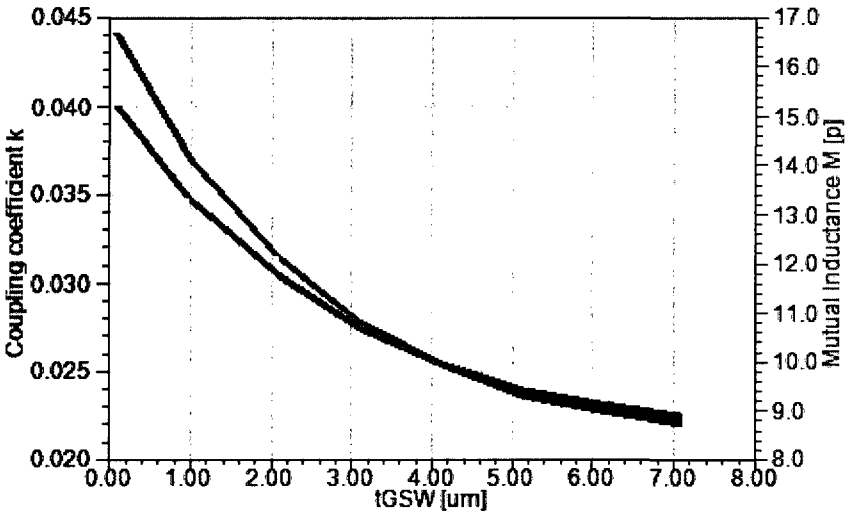


Figure 4-21: Coupling coefficient k and mutual inductance M of the 430pH stacked inductors with GSW isolation vs. distance of the TGP at 30 GHz

4.4.3 Inductor Variation with Temperature

The simulation results shown in Figure 4-22 to 4-27 are valid for temperature variation from -40°C to 100°C where the metal and substrate conductivities have been changed according to their temperature coefficients of conductivity, refer to Appendix F. The corresponding conductivity, as calculated by:

$$\sigma_{T'} = \frac{\sigma_T}{1+\alpha(T-T')} \quad (4.1)$$

Where: $\sigma_{T'}$ is the electrical conductivity at a common temperature, T'

σ_T is the electrical conductivity at a measured temperature, T

α is the temperature compensation slope of the material,

T is the measured absolute temperature,

T' is the common temperature.

The Q factor decreases with an increase in temperature over the frequency range presented here. In contrast, inductance changes little over temperature. The behavior of Q with temperature is caused by the increase in resistivity of the inductor metallization and the conductivity of the substrate.

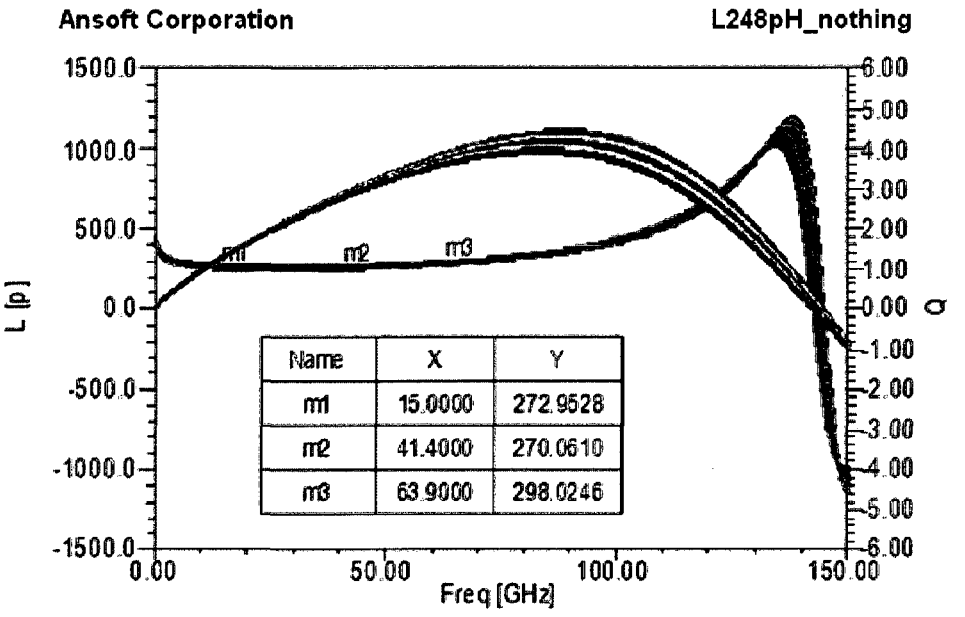


Figure 4-22: Simulated Q and L of the 248pH stacked inductor without PGS vs. Freq with varying temperature

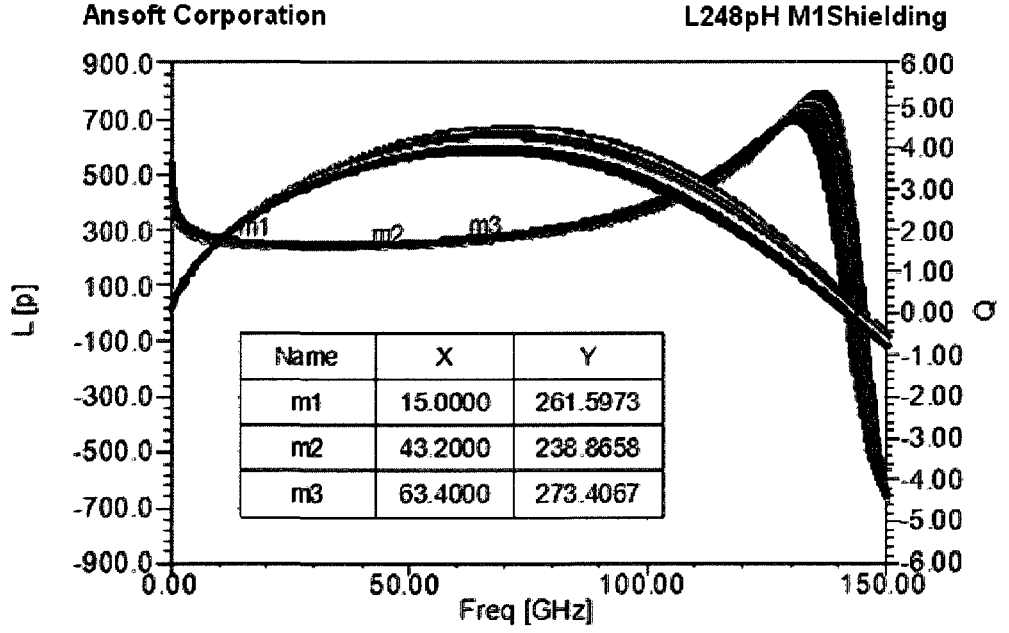


Figure 4-23: Simulated Q and L of the 248pH stacked inductor with M1-PGS vs. Freq with varying temperature

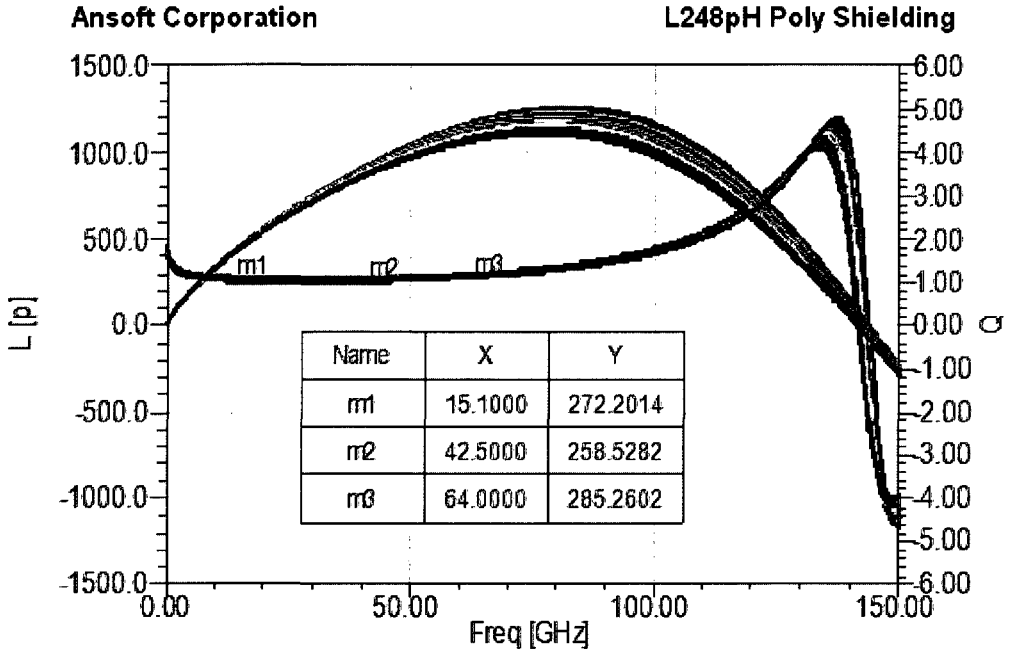


Figure 4-24:: Simulated Q and L of the 248pH stacked inductor with Poly-PGS vs. Freq with varying temperature

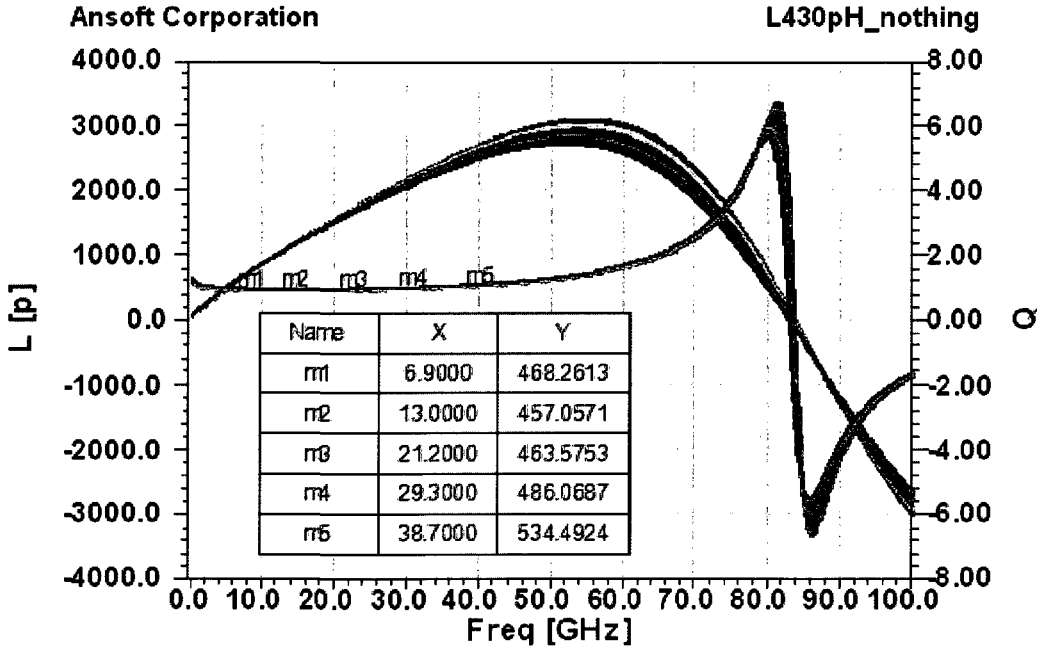


Figure 4-25: Simulated Q and L of the 430pH stacked inductor without PGS vs. Freq with varying temperature

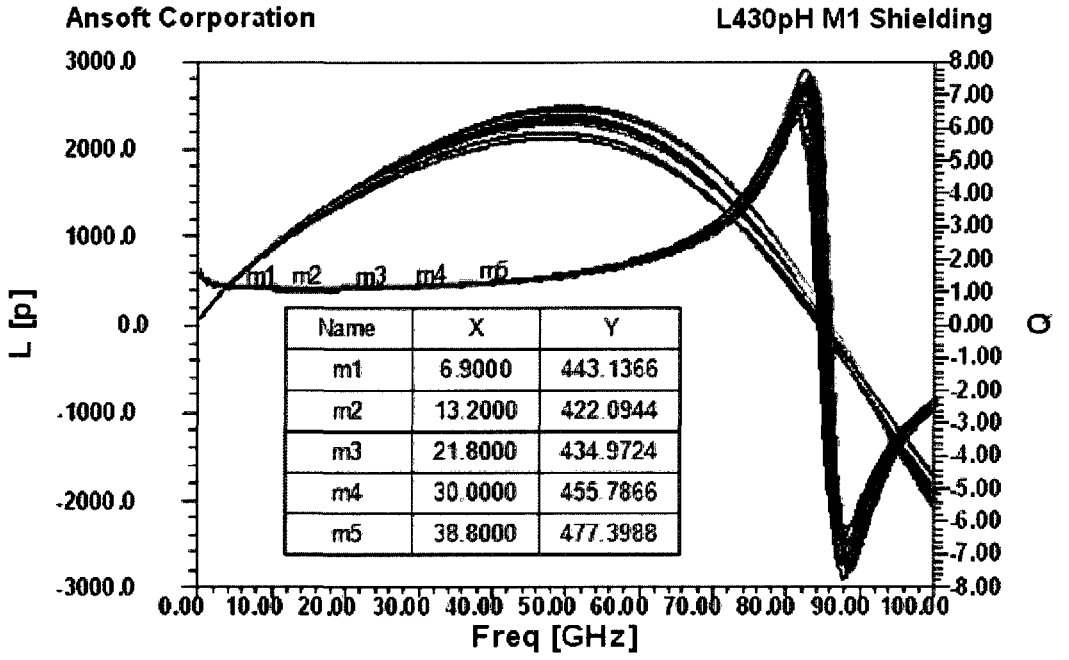


Figure 4-26: Simulated Q and L of the 430pH stacked inductor with M1-PGS vs. Freq with varying temperature

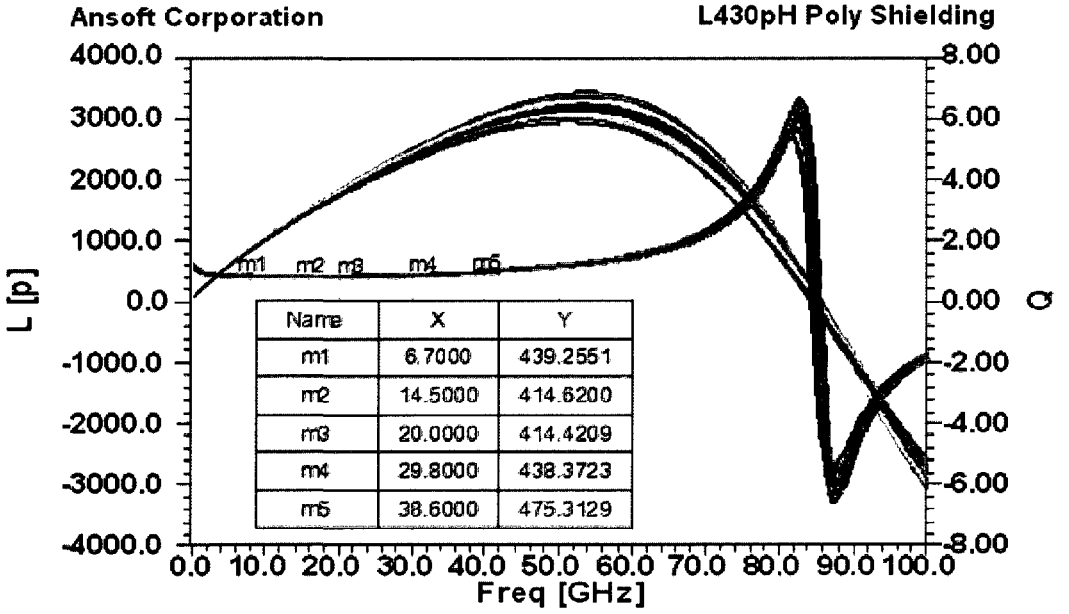


Figure 4-27: Simulated Q and L of the 430pH stacked inductor with Poly-PGS vs. Freq with varying temperature

Figure 4-28 and 4-33 summarizes the self-resonance f_{res}, Q_{peak}, and Q_{peak} frequency of the two stacked inductors vs. the temperature from -40°C to 100°C. Table 2 below summarizes the

variation in percentages based on Figure 4-28 and 4-33, using room temperature 25°C as the reference point. This summary shows consistency in the variation of inductor performance due to temperature effects. The self-resonance f_{res} was not changed significantly (about 1%). The peak Q changed from -9% to 6.7% as shown in Table 2, but its absolute values only changes by less than 1. When these inductors were placed in series with a resistor, the resulting change in Q does not have a significant effect on the amplifier performances. Meanwhile, the peak Q frequency changes around -4% to 3%.

Table 2: Performance summary of stacked inductors with different PGS in percentage for temperature variation from -40°C to 100°C

PGS type	*L*	f_{res}	Q_{peak}	Q_{peak} Freq
No	248pH	-0.5% to 0.6%	-7.7% to 6.1%	-3.5% to 2.6%
Poly	248pH	-1.2% to 0.9%	-6.7% to 5.7%	-3.5% to 2.9%
M1	248pH	-0.8% to 0.9%	-6.7% to 4.2%	-5.1% to 2.9%
No	430pH	-0.9% to 0.7%	-8.5% to 6.7%	-3.0% to 2.2%
Poly	430pH	-0.7% to 0.6%	-8.1% to 6.5%	-3.7% to 1.0%
M1	430pH	-1.0% to 0.8%	-9.2% to 3.9%	-2.6% to 3.2%

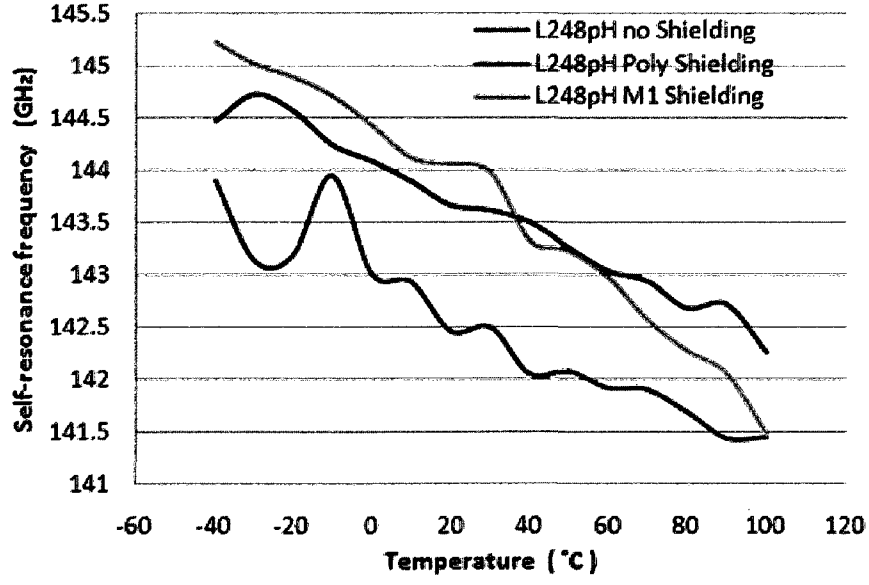


Figure 4-28: Self-resonance frequency of the 248pH stacked inductors vs. temperature

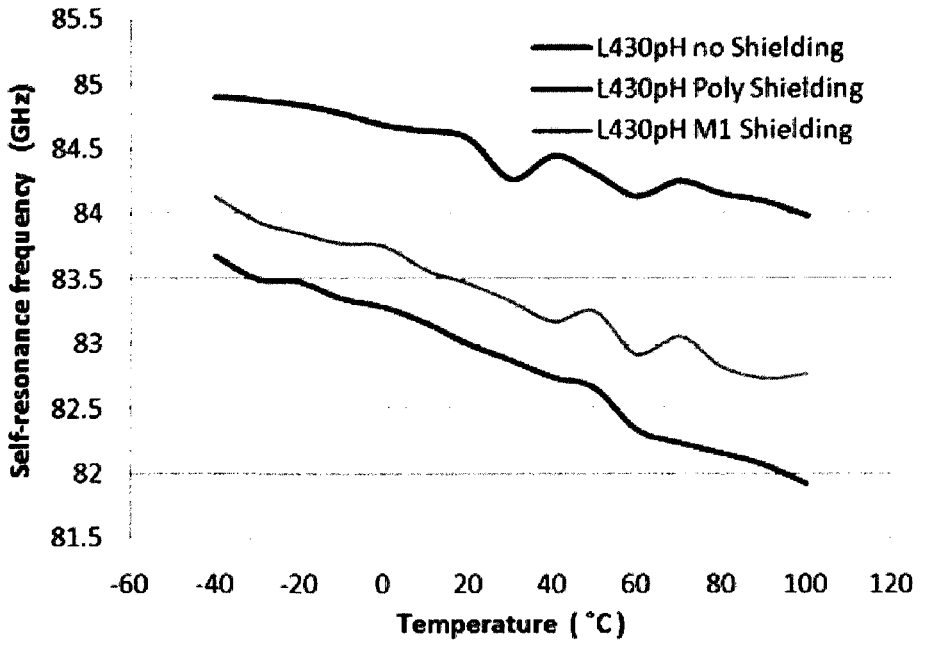


Figure 4-29: Self-resonance frequency of the 430pH stacked inductors vs. temperature

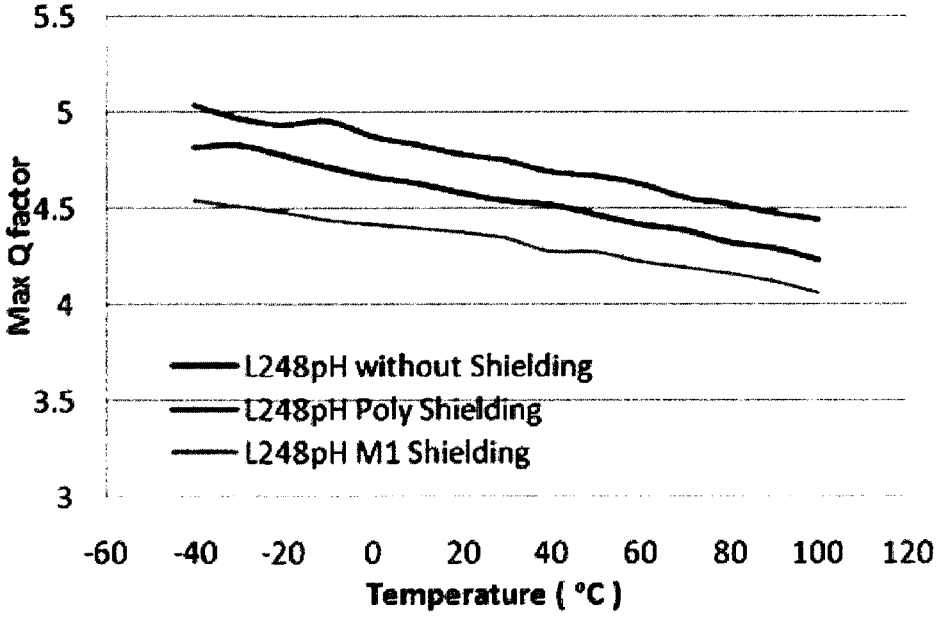


Figure 4-30: Maximum Q factor of the 248pH stacked inductors vs. temperature

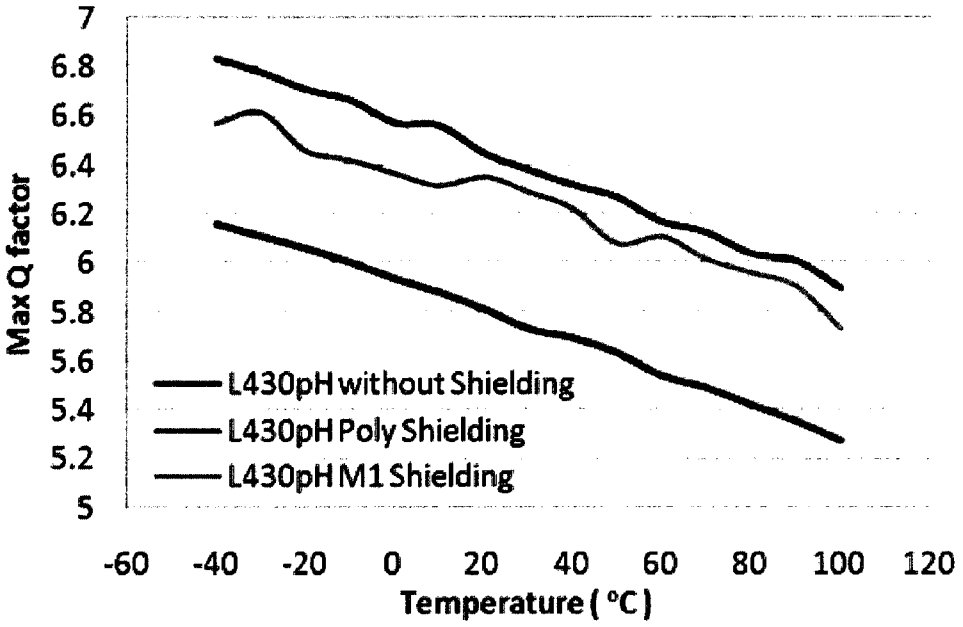


Figure 4-31: Maximum Q factor of the 430pH stacked inductors vs. temperature

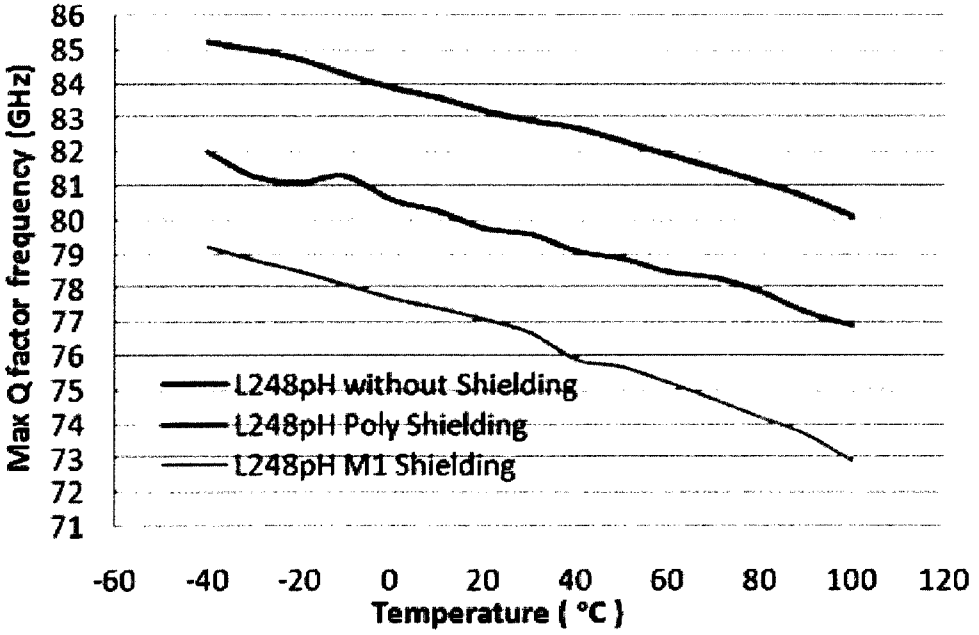


Figure 4-32: Maximum Q factor frequency of the 248pH stacked inductors vs. temperature

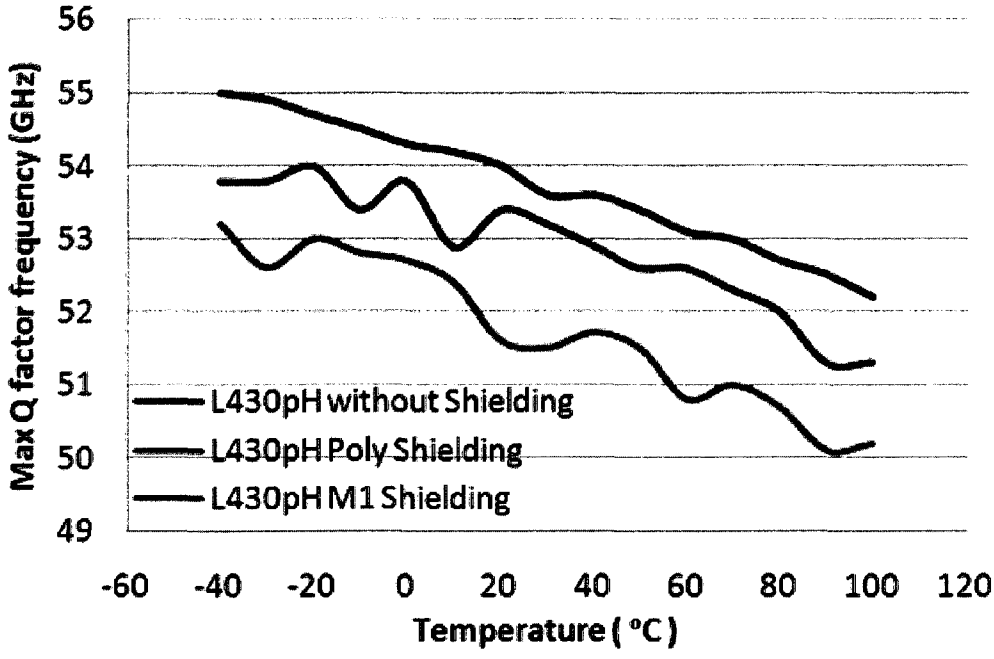


Figure 4-33: Maximum Q factor frequency of the 430pH stacked inductors vs. temperature

In conclusions, the geometries of stacked inductors have been studied in this chapter. The stacked inductor design procedures and considerations through the basic modeling in ASITIC are presented. The coupling effects of various isolation techniques to the stacked inductor have been studied. Simulation results show that adding PGS to the small stacked inductor has no significant effect on the Q factor. Hence, the PGS is not necessary for the super compact stacked inductor. Simulation results also show that the Gaussian side wall technique can be chosen to provide maximum isolation for certain applications and with no significant effect on the Q, L and the self-resonance frequency f_{res}. For the experiment of this thesis, the inductors with different PGS isolations are still chose for fabrication in order to demonstrate the unnecessary use of PGS for small stacked inductors.

Chapter 5 Amplifiers with Inductive Peaking

Inductive peaking is one of the most common techniques for bandwidth enhancement in order to meet the critical requirements of high-speed applications. Inductive peaking allows for larger bandwidths without an increase in the power consumption and design complexity of the circuit. In this chapter, the basic theory of operation of amplifiers with inductive peaking will be summarized, including the choice of topology and their relative bandwidth improvement.

5.1 Common Source Amplifiers

A reference common source (CS) amplifier is shown in Figure 5-1(a) in single stage configuration with a resistive load R and a capacitive load C. In a multi-stage cascade configuration, additional capacitive load C_2 from the next stage is shown in Figure 5-1(b). The power gain of an amplifier is simply the product of the trans-impedance $Z(s)$ and the trans-conductance g_m. Assumed g_m is approximately constant, only trans-impedance is considered hereafter for different peaking techniques [2]. For the common source amplifier in Figure 5-1 (a) and (b), the gain will be,

$$G_P = \frac{I_{out}}{V_{in}} \cdot \frac{V_{out}}{I_{in}} = g_m \cdot Z(s) \qquad (5.1)$$

$$Z(s) = \frac{R}{1+sRC} \qquad where\ C = C_1 + C_2 \qquad (5.2)$$

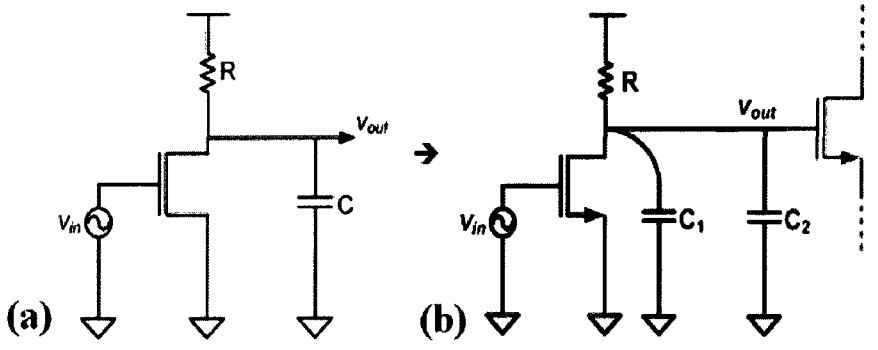


Figure 5-1: (a) single stage CS amplifier, (b) CS amplifier in multi-stage cascade [2]

For a given power constraint, in this type of CS amplifier there are tradeoffs between gain and bandwidth. Figure 5-2 shows the gain and resulting cut-off frequencies when the resistive load R change by $R_3 > R_2 > R_1$ resulting in the gain changed $G_{P3} > G_{P2} > G_{P1}$ and -3dB bandwidth $f_3 < f_2 < f_1$.

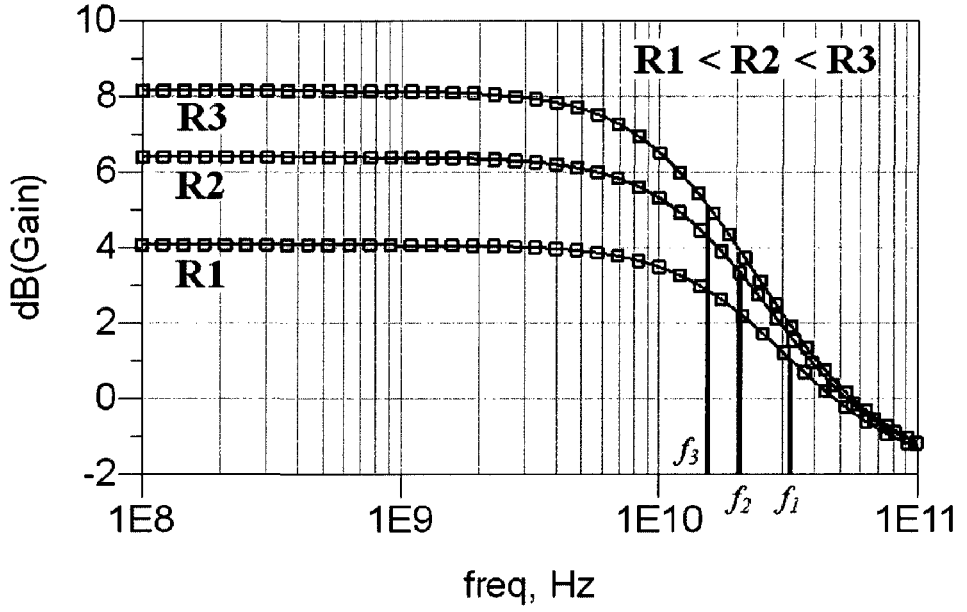


Figure 5-2: Gain and bandwidth tradeoff in CS amplifiers

According to Figure 5-1(b), C_1 and C_2 represent the drain parasitic and load capacitance. This general CS amplifier is widely used in a differential configuration for wireline applications with several stages cascaded to achieve high levels of gain. Thus, C_2 includes the gate capacitance of the next stage. Depending on the desired value of gain, voltage swing, and bias current for a given transistor size in each stage, the ratio $k_c = C_1/(C_1+C_2)$ becomes a design constraint, which typically varies from 0.2-0.5. Hence, a given bandwidth extension technique may not be optimum for all k_c values, and a multi-stage amplifier may achieve superior performance using different bandwidth extension techniques using different k_c values for each stages [2].

5.2 Bridged-shunt Peaking

Shunt peaking is a bandwidth extension technique in which an inductor L connected in series with the load resistor R shunts the output capacitor $C = (C_1+C_2)$, as shown in Figure 5-3 [2]. For the shunt peaking, the trans-impedance will be

$$Z(s) = \frac{V_{out}}{I_{in}} = \left(\frac{1}{sC}\right) || (R + sL) = \frac{R+sL}{1+sRC+s^2LC} \qquad (5.3)$$

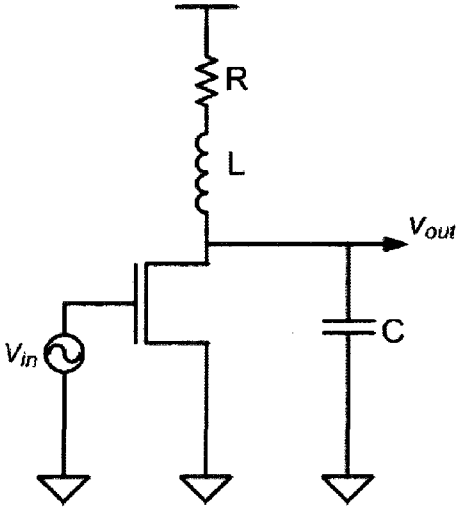


Figure 5-3: A common-source amplifier with shunt peaking [2]

The shunt peaking inductor in Figure 5-3 introduces a zero in $Z(s)$, which increases the trans-impedance with frequency, such that it compensates for the decreasing impedance of C, and thus extends the -3 dB bandwidth [2]. Substituting the -3 dB bandwidth of the reference common-source amplifier, $\omega_0 = \frac{1}{RC}$, and the variable $m = \frac{R^2C}{L}$, into (5.3) and normalizing to the impedance at DC (R) gives

$$Z_N(s) = \frac{1+\frac{s}{m\cdot\omega_0}}{1+\frac{s}{\omega_0}+\frac{s^2}{m\cdot\omega_0^2}} \qquad (5.4)$$

Theoretical simulation results for shunt peaking are shown in Figure 5-4. The maximum bandwidth extension ratio (BWER) of 1.84 occurs when $m = \sqrt{2}$. This extension comes with

1.5dB of peaking. A maximal flat gain is achieved from $m = 1 + \sqrt{2} = 2.414$ but BWER is reduced to 1.72.

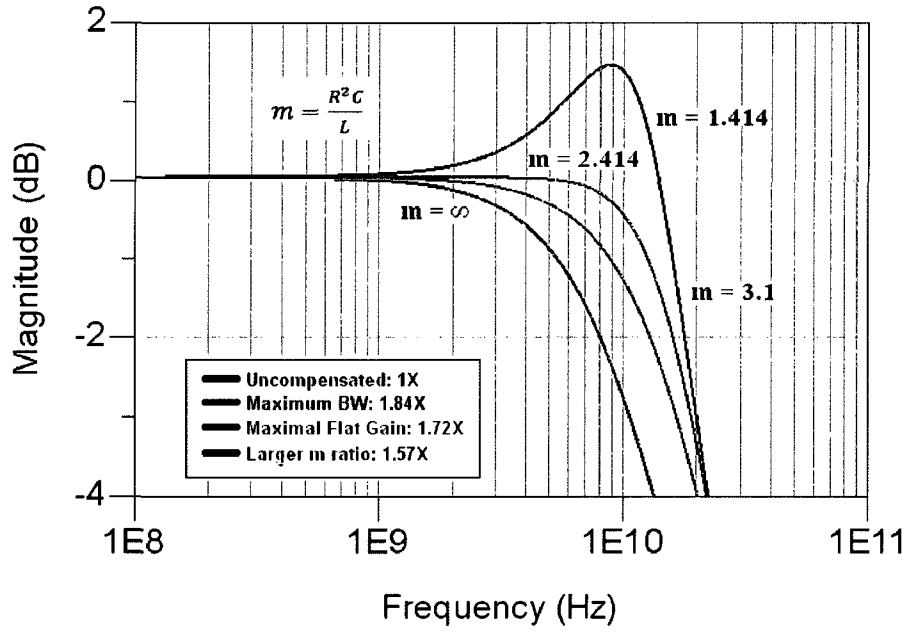


Figure 5-4: Ideal bandwidth improvement with shunt peaking

Although the incerased impedance of the shunt peaking inductor improves the -3dB bandwidth, it also leads to peaking in the response (i.e. 1.5dB peaking when m = 1.414). Hence, techniques for eliminating the peaking with maximum BWER are desired. One possible solution is to add a large enough shunt capacitor with the inductor to remove the peaking but small enough to not significantly alter the gain reponse, which is the bridged-shunt network [2], as shown in Figure 5-5. Its nomailized trans-impedance with $k_B = \frac{C_B}{C}$, $\omega_0 = \frac{1}{RC}$, and $m = \frac{R^2C}{L}$ will be

$$Z_N(s) = \frac{1+\left(\frac{1}{m}\right)\frac{s}{\omega_0}+\left(\frac{k_B}{m}\right)\frac{s^2}{\omega_0^2}}{1+\frac{s}{\omega_0}+\left(\frac{k_B+1}{m}\right)\frac{s^2}{\omega_0^2}+\left(\frac{k_B}{m}\right)\frac{s^3}{\omega_0^3}} \qquad (5.5)$$

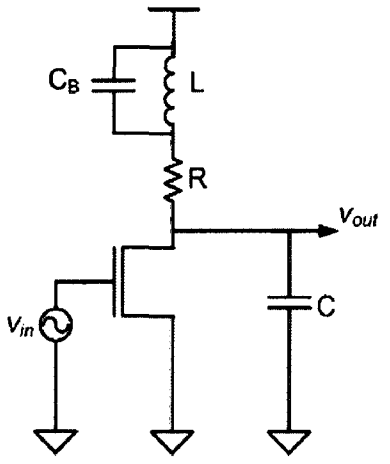


Figure 5-5: A common-source amplifier with bridged-shunt peaking [2]

Compared to (5.4), C_B introduces another pole and zero in $Z_N(s)$. Figure 5-6 shows magnitude responses for the bridged-shunt peaking circuit for several practical values of k_B along with the shunt peaking ($k_B = 0$) and uncompensated cases. When $k_B = 0.11$ and $m = 1.671$, a BWER of 1.84 is achieved with a flat gain response, which is nearly the same bandwidth improvement compared to the shunt peaking design with a maximum BWER of 1.84 but 1.5 dB of peaking; whereas when $k_B = 0.28$ and $m = 1.414$ (same shunt peaking inductance), a BWER of 1.96 is achieved with a flat gain response and is slightly larger than the shunt peaking design with a maximum BWER of 1.84 but 1.5 dB of peaking.

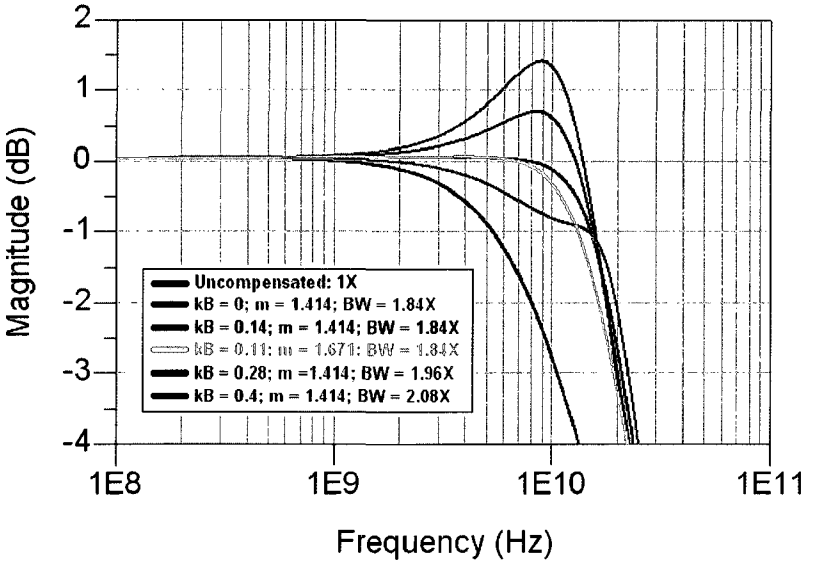


Figure 5-6: Ideal bandwidth improvement with bridged-shunt peaking vs. k_B

As shown in Figure 5-6, compared to shunt peaking with $m = 1.414$, bridged-shunt peaking has the advantage that it uses a larger value of m to achieve same bandwidth improvement with flat gain, which means a smaller inductance with smaller die area and higher self-resonant frequency, etc. In addition, an inductor implemented in silicon has significant shunt parasitic capacitances. By connecting L to the supply in Figure 29, it has the advantage that it incorporates the inductor parasitic as C_B for this topology since there is no pure shunt peaking in practice where $k_B > 0$; if more C_B is required, an additional capacitor can be added. On the other hand, connecting L to the drain adds parasitic capacitance to the load capacitance C and reduces the bandwidth [2].

5.3 Series Peaking

Series peaking is a bandwidth extension technique in which an inductor L connected in series with the output capacitor C shunts the load resistor R, as shown in Figure 5-7 [2]. The normailized trans-impedance for the series peaking with $\omega_0 = \frac{1}{RC}$, and $m = \frac{R^2C}{L}$ will be

$$Z_N(s) = \frac{1}{1+\frac{s}{\omega_O}+\frac{s^2}{m\cdot\omega_O^2}} \qquad (5.6)$$

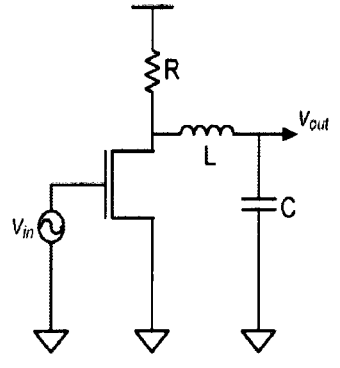


Figure 5-7: A common-source amplifier with series peaking [2]

According to (5.6), series peaking does not add a zero; hence showing inferior performance when compared to shunt peaking where the theoretical maximum flat gain only

has a BWER of 1.41 when $m = 2$. However in practice, drain parasitic C_l can be significant; such that better BWER can be achieved using capacitive slitting where an inductor is inserted to separated the total load capacitance into two constituent components as shown in Figure 5-8 [2]. Then the normalized trans-impedance with $k_C = \frac{C_1}{C}$ for the capacitive splitting topology will be

$$Z_N(s) = \frac{1}{1+\frac{s}{\omega_o}+\left(\frac{1-k_C}{m}\right)\frac{s^2}{\omega_o^2}+\left(\frac{k_C(1-k_C)}{m}\right)\frac{s^3}{\omega_o^3}} \qquad (5.7)$$

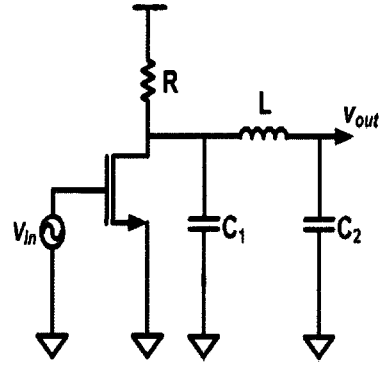


Figure 5-8: A common-source amplifier with series peaking and capacitive splitting [2]

The separation of C_l from C in Figure 5-7, creates another pole, which affects BWER versus k_C as shown in Table 3. As the parasitic capacitance ratio k_C increases, BWER increases to a maximum of 2.68 for $k_C = 0.3$. If the passband peaking ripples that occur for higher values of k_C is acceptable, an even larger BWER is achievable. Figure 5-9 shows the theoretical simulation results of the -3 dB bandwidth improvements for practical k_C values corresponding to Table 3.

Table 3: Series Peaking with Capacitive Splitting Summary

$k_C = C_1/C$	Ripple (dB)	$m = R^2C/L$	BWER
0	0	2	1.41
0.1	0	1.8	1.68
0.2	0	1.8	2.26
0.3	0	2.4	2.68
0.4	1.3	1.9	2.83
	2.45	2.5	3.4
0.5	3.2	1.5	2.74

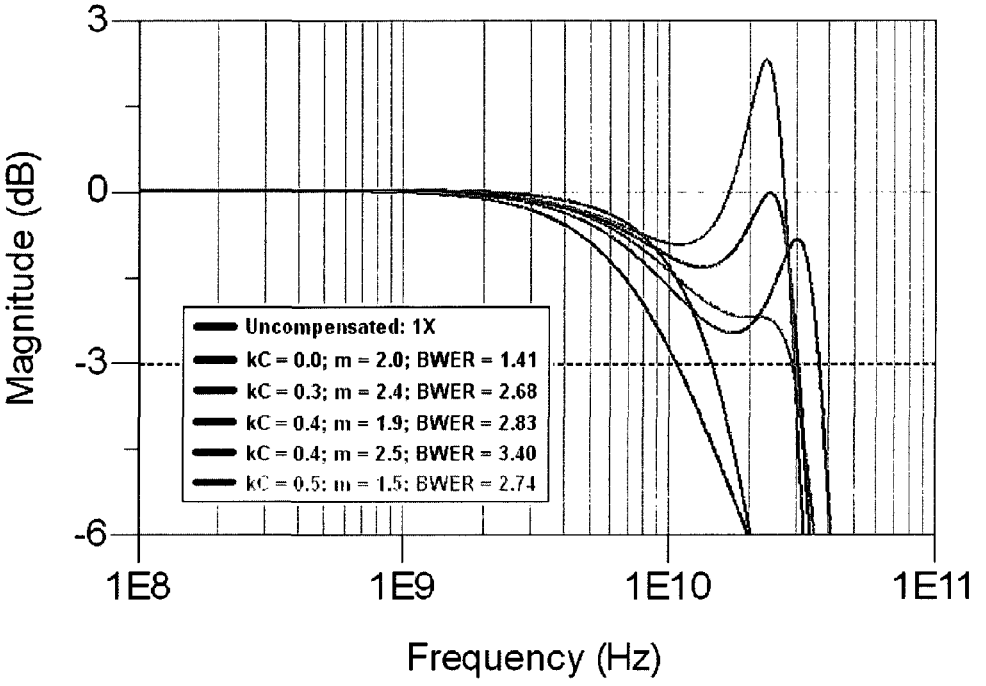


Figure 5-9: Ideal bandwidth improvement with series peaking vs. k_C

5.4 Bridged-shunt-Series Peaking

Bridged-shunt-series peaking technique, as shown in Figure 5-10, combines capacitive splitting of the series peaking network and inductive peaking of the bridged shunt approach. It uses two inductors but provides larger BWER values than its shunt-series peaking counterpart [2]. The normalized trans-impedance of the bridged-shunt-series peaking network is as follows with $\boldsymbol{m_1} = \frac{\boldsymbol{R^2C}}{\boldsymbol{L_1}}$, $\boldsymbol{m_2} = \frac{\boldsymbol{R^2C}}{\boldsymbol{L_2}}$, and k_B, k_C, and $\boldsymbol{\omega_0}$

$$Z_N(s) = \frac{1+\left(\frac{1}{m_1}\right)\frac{s}{\omega_o}+\left(\frac{k_B}{m_1}\right)\frac{s^2}{\omega_o^2}}{1+\frac{s}{\omega_o}+\left(\frac{1+k_B}{m_1}+\frac{1-k_C}{m_2}\right)\frac{s^2}{\omega_o^2}+\left(\frac{k_B}{m_1}+\frac{k_C(1-k_C)}{m_2}\right)\frac{s^3}{\omega_o^3}+\left(\frac{(k_C+k_B)(1-k_C)}{m_1m_2}\right)\frac{s^4}{\omega_o^4}+\left(\frac{k_Ck_B(1-k_C)}{m_1m_2}\right)\frac{s^5}{\omega_o^5}} \quad (5.8)$$

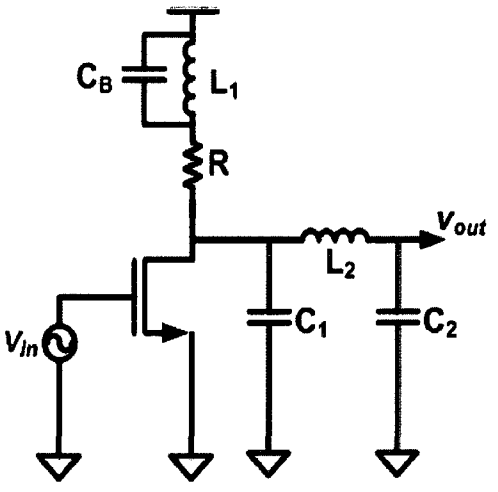


Figure 5-10: A common-source amplifier with bridged-shunt-series peaking network [2]

Table 4 shows results for different k_C and passband ripple values; for k_C = 0.4, a BWER of 4.02 is possible. Figure 5-11 shows bandwidth improvements for several values of k_C corresponding to Table 4. A response having a BWER of 3.78 with almost no gain-peaking is achieved for m_1 = 5 and m_2 = 3, which affords pole-zero cancellation. However, such cancellations require precise component values that are difficult to realize due to distributed parasitic effects and process, voltage, and temperature (PVT) variations [2]. In contrast, C_B in a bridged-shunt-series peaking design adds a degree of freedom to control a zero that mitigates the effects of parasitic and leads to a larger BWER.

Table 4: Bridged-Shunt-Series Peaking Summary

$k_C = C_1/C$	$k_B = C_B/C$	Ripple (dB)	$m_1 = R^2C/L_1$	$m_2 = R^2C/L_2$	BWER
0.4	0.3	0	5	3	3.78
0.4	0.2	2.1	5	4	4.02
0.5	0.2	2.1	4	2	3.58

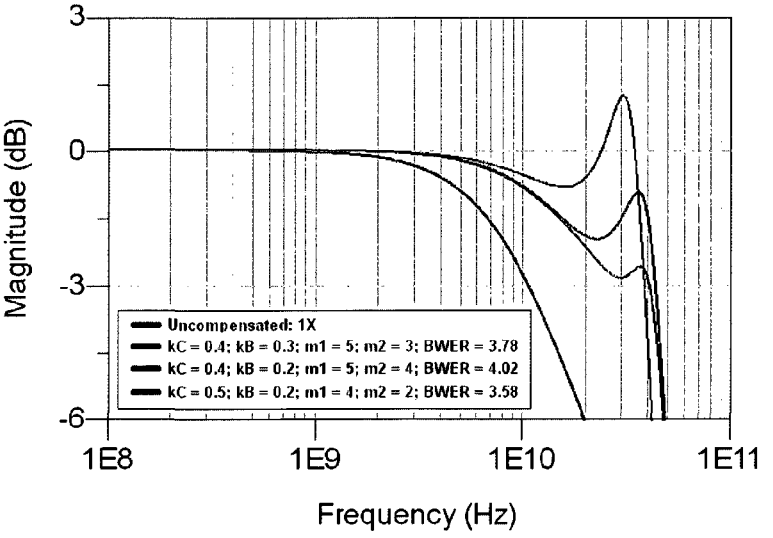


Figure 5-11: Ideal bandwidth improvements with bridged-shunt-series peaking vs. k_C

5.5 Conventional T-coil Peaking

Bridged-shunt-series peaking gives a large BWER for $k_C > 0.3$; however, as the load capacitance increases ($k_C < 0.3$), the capacitive-splitting action of L_2 and the bridging action of C_B become ineffective in achieving a large BWER [2]. Base on literature review, conventional T-coil peaking is a combination of shunt and double series peaking, as shown in Figure 5-12 [29], which can provide better bandwidth extension for the cases of $k_C < 0.3$.

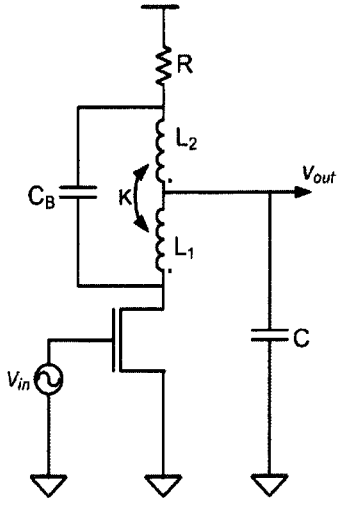


Figure 5-12: A common-source amplifier with conventional T-coil peaking network

The main characteristic of this circuit are the mutually coupled inductors which can be realized by a center tapped coil L and a bridged capacitance C_B. The normalized trans-impedance of the conventional T-coil peaking network is

$$Z_N(s) = \frac{1}{1+\left(\frac{s}{\omega_n}\right)2\zeta+\frac{s^2}{\omega_n^2}} \quad (5.9)$$

The relations between different components of the T-coil amplifier are shown below according to [29]. ζ is the damping factor and is chosen as $\frac{1}{\sqrt{2}}$ to achieve maximum flat pass-band response, also referred as Butterworth response. L_M is the mutual inductance resulting from the coupling between the two halves of the coil L_1 and L_2, where K is the coupling coefficient of the two inductors. C_B is the bridging capacitance, which is used to create parallel resonance and provides further bandwidth improvement. Theoretically, the BWER for maximally flat gain of the conventional T-coil peaking circuit can be achieved for 2.83 [29], as shown in Figure 5-13. The equations for the relations of the components in the T-coil network are

$$L_1 = L_2 = \frac{R^2C}{2} \quad (5.10)$$

$$\omega_n = \frac{1}{R\sqrt{C_B \cdot C}} \quad (5.11)$$

$$\zeta = \frac{1}{4}\sqrt{\frac{C}{C_B}} \quad (5.12)$$

$$C_B = \frac{C}{16\zeta^2} = \frac{C}{4}\left(\frac{1-|K|}{1+|K|}\right) \quad (5.13)$$

$$L_M = \frac{R^2C}{4}\left(\frac{1}{4\zeta^2} - 1\right) = K\sqrt{L_1L_2} \quad (5.14)$$

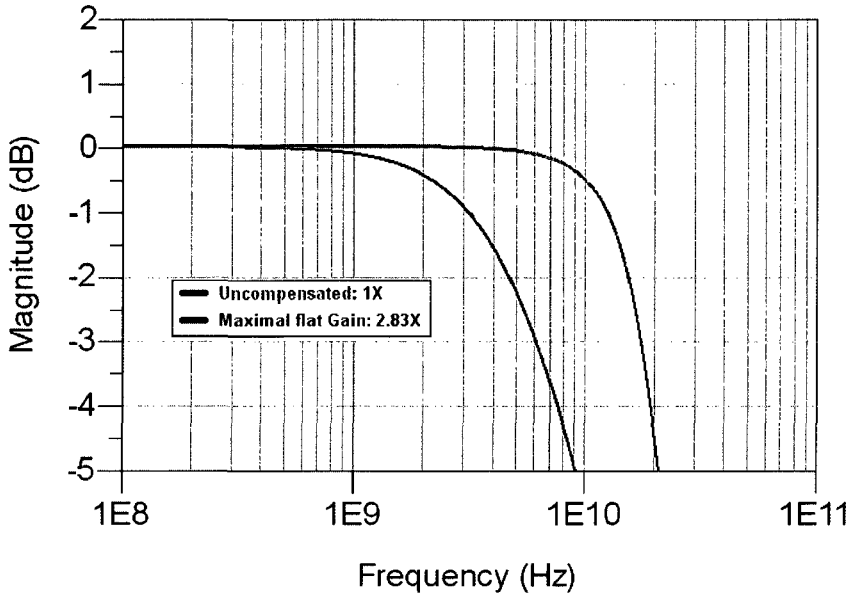


Figure 5-13: Ideal bandwidth improvements with conventional T-coil peaking network

5.6 Asymmetric T-coil Peaking

Modified from conventional T-coil peaking network, asymmetric T-coil peaking technique according to [2], as shown in Figure 5-14(a), can achieve larger BWER than the conventional one. In an asymmetric ($L_1 \neq L_2$) T-coil peaking, the coils will achieve a negative mutual inductance (-M), as shown in Figure 5-14(b), the equivalent small signal network incorporates a T-model of the transformer. As in the bridged-shunt-series peaking, the secondary inductor L_2 induces the capacitive splitting so that the initial charging current flows only to C_1; then the current begins to flow in L_2, which causes a proportional amount of current to flow to C_2. Since the load capacitance C_2 is in series with the –M of the T-coil, this negative magnetic coupling allows for an initial boost in the current flow to C_2; thus, an improvement in rise time and the BWER [2]. The normalized trans-impedance of the asymmetric T-coil peaking network is as follows with $\boldsymbol{m_1 = \frac{R^2C}{L_1}}$, $\boldsymbol{m_2 = \frac{R^2C}{L_2}}$, $\boldsymbol{k_m = M/\sqrt{L_1L_2}}$, k_C, and $\boldsymbol{\omega_0}$ [2]

$$Z_N(s) = \frac{1+\left(\frac{1}{m_1}+\frac{k_m}{\sqrt{m_1m_2}}\right)\frac{s}{\omega_o}}{1+\frac{s}{\omega_o}+\left(\frac{1}{m_1}+\frac{k_C}{m_2}+\frac{2k_Ck_m}{\sqrt{m_1m_2}}\right)\frac{s^2}{\omega_o^2}+\left(\frac{k_C(1-k_C)}{m_2}\right)\frac{s^3}{\omega_o^3}+\left(\frac{k_C(1-k_C)(1-k_m^2)}{m_1m_2}\right)\frac{s^4}{\omega_o^4}} \quad (5.15)$$

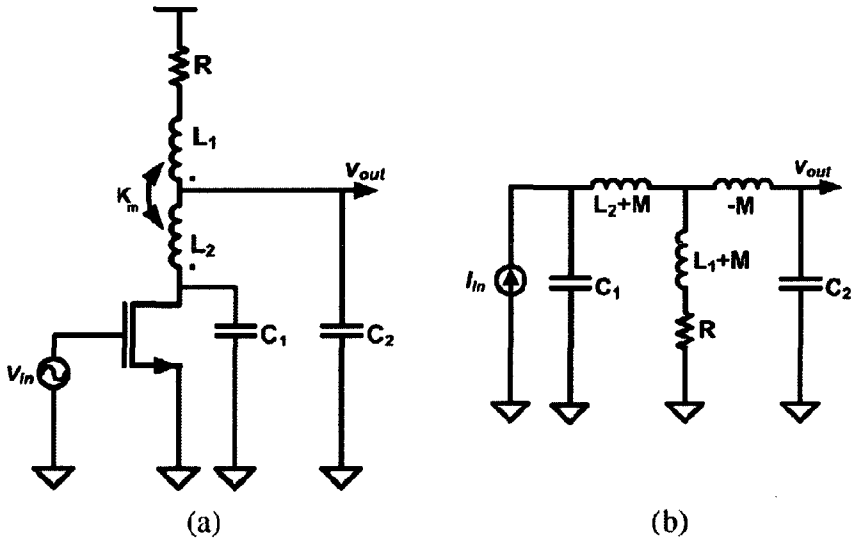


Figure 5-14: (a) A common-source amplifier with asymmetric T-coil peaking network, (b) an equivalent T-coil peaking small signal network [2]

According to [2], employing an asymmetric T-coil and properly using the drain capacitance (C_1) leads to optimum pole-zero locations for a larger BWER than the conventional T-coil network with $L_1 = L_2$, where the theoretical maximum BWER is only 2.83. As shown in Figure 5-15, for different k_C and passband ripples corresponding to Table 5, the BWER can be achieved to over 5 in some cases.

Table 5: Asymmetric T-coil Peaking Summary with capacitive splitting

k_C	k_m	m_1	m_2	Ripple (dB)	BWER
0.05	0.6	4	1.6	1.2	5.15
0.05	0.6	3.5	2	1.8	5.69
0.1	0.5	4.2	2	0	4.5
0.2	0.5	4	2.4	0	4.38
0.2	0.6	5.5	2.4	0	3.7
0.3	0.5	4	2.7	0	4.05

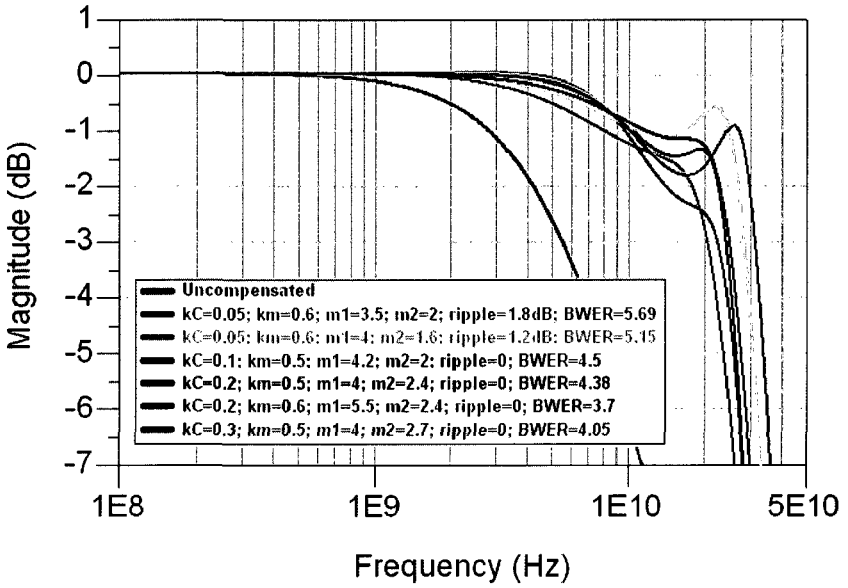


Figure 5-15: General bandwidth improvements with asymmetric T-coil peaking vs. k_C using ideal passive components

5.7 Inductive Peaking using Stacked Inductors

An example of a common source amplifier using customized stacked inductor for conventional t-coil peaking (refer to Figure 5-12) is introduced in this section that is new to save huge amount chip area. The performance will be compared between using the stacked inductor and the kit inductors.

Figure 5-16 to 5-19 compares the characteristics Q and L of the kit and stacked inductors shown in Figure 1-1 before and after the inductor is connected with a series 65Ω resistor for a broadband amplifier design. The simulation results in Figure 5-16 show that in a peaking application, stacked inductors are much more area efficient compared to standard kit inductors, while providing equivalent inductance at higher self-resonance frequency. Since inductors are in series with a resistive load, its Q is irrelevant and showing even higher Q at high frequency as shown in Figure 5-17 and 5-19. Figure 5-20 shows for the t-coil peaking topology, both amplifiers achieve almost the same bandwidth improvement, whether they use stacked or kit inductors, of about 50% while requiring only 15% of the chip area of the planar kit inductors from the manufacturer.

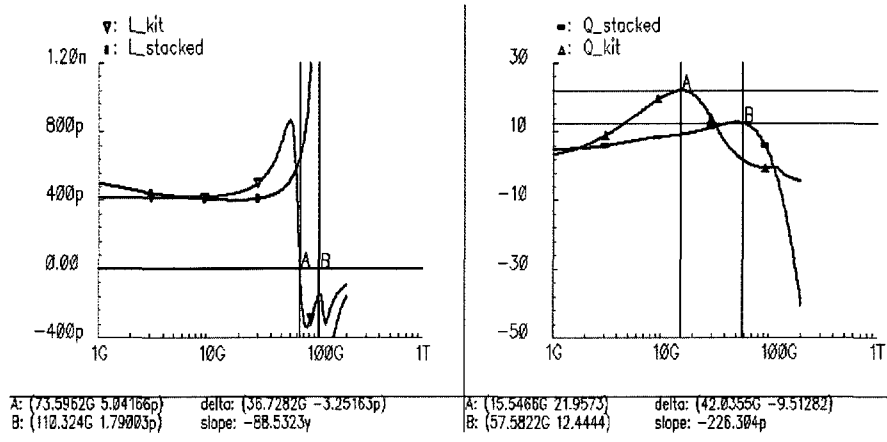


Figure 5-16: Q and L of a 409 pH kit and stacked inductor without load

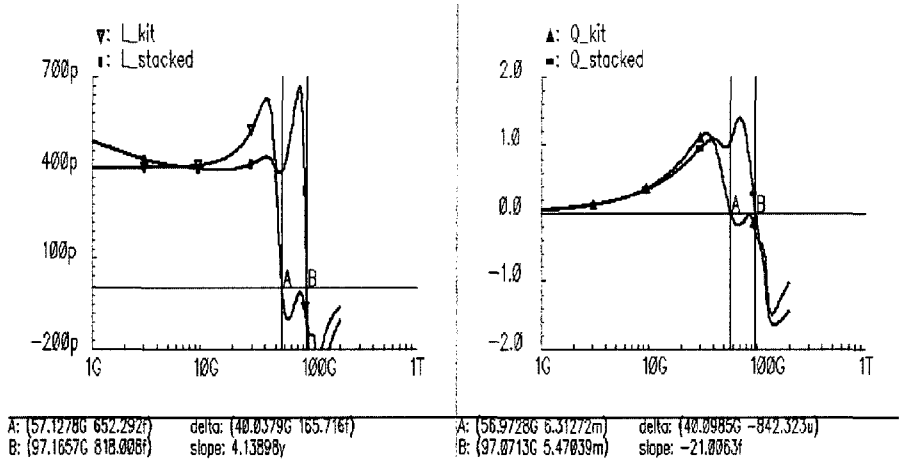


Figure 5-17: Q and L of 409 pH kit and stacked inductors loaded with series 65Ω resistor

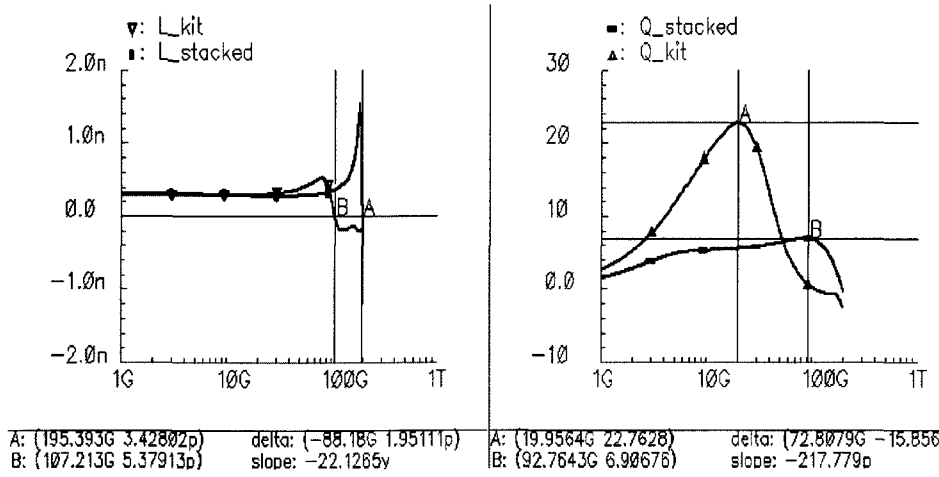


Figure 5-18: Q and L of a 292 pH kit and stacked inductor without load

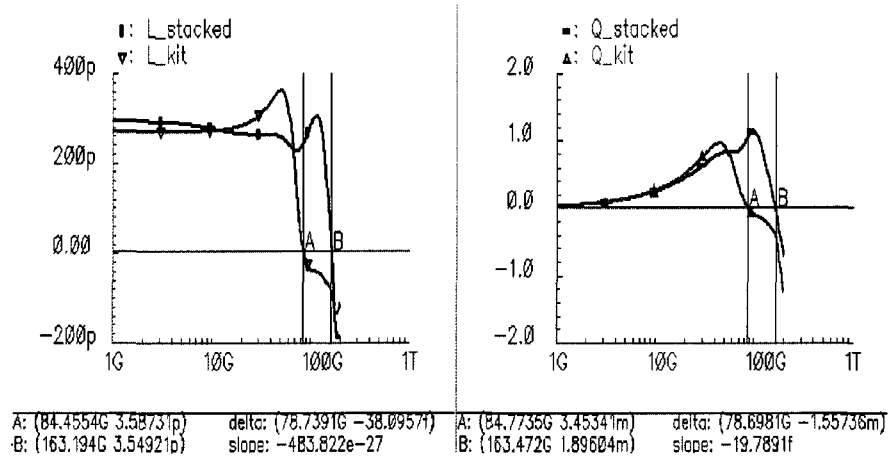


Figure 5-19: Q and L of 292 pH kit and stacked inductors loaded with series 65Ω resistor

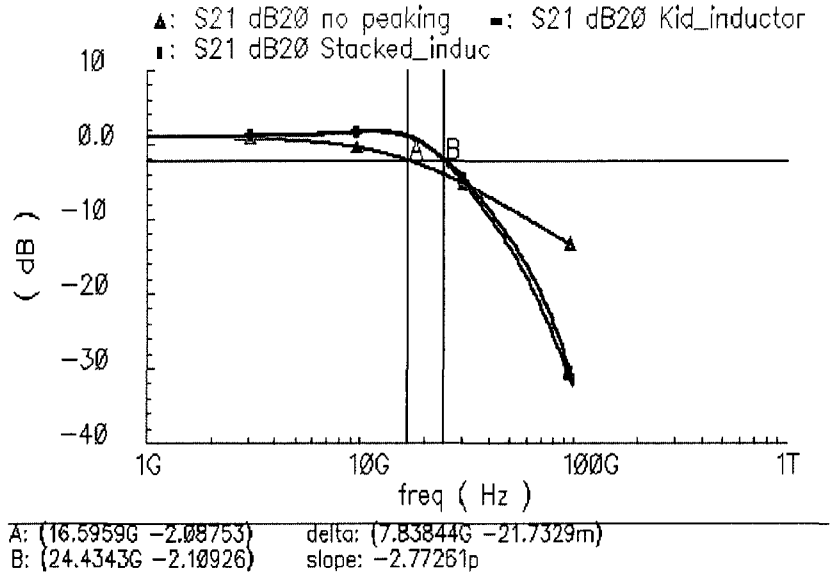


Figure 5-20: 50% bandwidth improvement with T-coil peaking topology

In conclusion, the basic theory of operation of amplifiers with various inductive peaking techniques has been studied. The simulation results from Section 5.1 to 5.6 were based on the use of ideal pass components; therefore, the simulation results are theoretical results. A given bandwidth extension technique may not be optimum for different capacitive load and a multi-stage amplifier may achieve superior performance using different bandwidth extension

techniques for each stages. T-coil peaking topology gives the theoretical maximum bandwidth enhancement over other techniques that have been studied in this chapter. Finally, the design example shows that for the t-coil peaking topology, both amplifiers achieve almost the same bandwidth improvement, whether they use stacked or kit inductors, and the chip area can be reduced by about 85% or more compared to using planar kit inductors from the manufacturer. The results in Figure 5-20 did not show zeros since the simulation frequency only be set up to 100 GHz.

Chapter 6 Inductor and Amplifier Experimental Results

In this chapter, de-embedding methods, measurement results of fabricated inductors and amplifiers with and without inductive peaking will be presented.

6.1 De-embedding Techniques

Due to the difficulty to build probe tips small enough to directly contact on the DUT, on-wafer de-embedding structures become necessary in order to remove the parasitic effects of the test fixture [9]; this is especially important for high-frequency measurement for which the parasitic components of the test fixtures and the probes will dramatically affect the measured results.

6.1.1 De-embedding Structures

Although different de-embedding methods have been studied and presented by numerous researchers, the typical set of test structures required for de-embedding, which are still the same as shown in Figure 6-1 [19], including a short, open, and through structures.

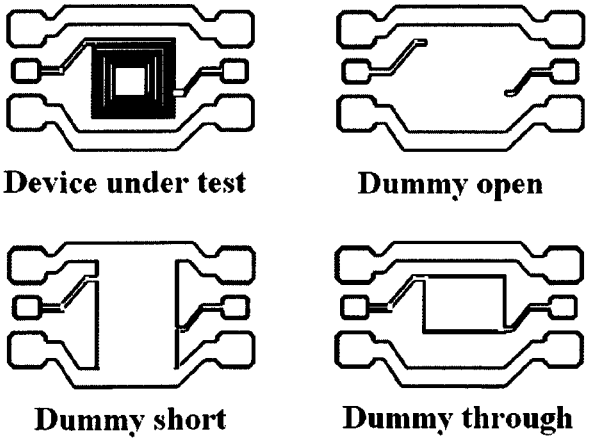


Figure 6-1: Example of de-embedding structures used for on-wafer measurements [19]

6.1.2 De-embedding Methods

After measuring the S-parameters for the above de-embedding structures, some simple calculations can be performed to remove the unwanted parasitic. Figure 6-2 shows a model used for 2-port de-embedding, as described in [31]. For 1-port characterization, the 2-port model was modified so that one side is shorted to ground, resulting in the model shown in Figure 6-3.

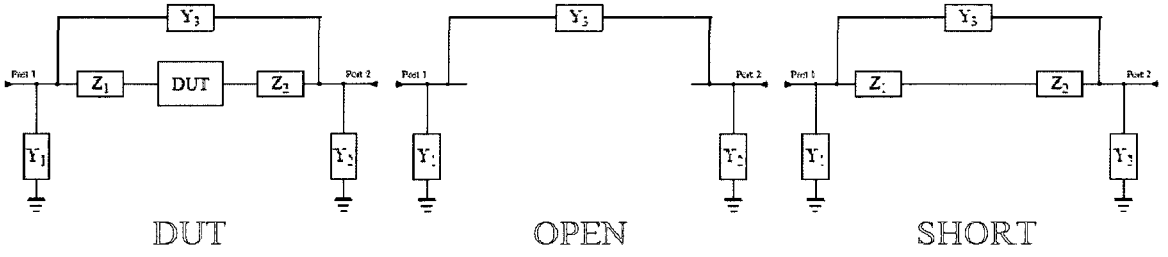


Figure 6-2: Two-port De-embedding Model showing the parasitic components [31]

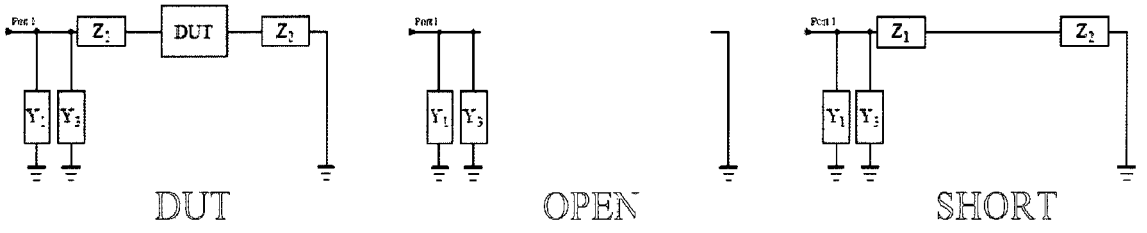


Figure 6-3: One-port De-embedding Model showing the parasitic components [31]

According to the 1-port and 2-port model s in Figure 6-3 and 6-2, two similar equations (6.1) and (6.2) can be used to calculate the necessary parameters for the DUT, which are based on the Short-open and Open-short De-embeddings equations. As an example for the short-open method, based on the measured s-parameters of the open, short, and DUT from the VNA, we can remove the series parasitic from both the embedded DUT and open fixtures by subtracting the Z-parameters of the short; then remove the parallel parasitic from the embedded DUT by subtracting the Y-parameters of the open from the previous step. Finally, the actual DUT characteristics can be obtained by converting Y_{so} to S-parameters.

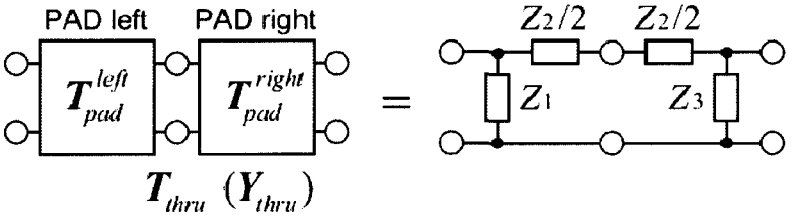
Method-1: Short-open de-embedding [32]

$$Y_{so} = (Z_{meas} - Z_{short})^{-1} - (Z_{open} - Z_{short})^{-1} \quad (6.1)$$

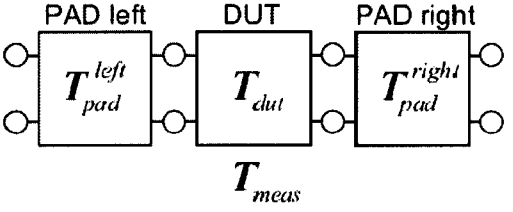
Method-2: Open-short de-embedding [32]

$$Y_{os} = \left((Y_{meas} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1}\right)^{-1} \quad (6.2)$$

The third de-embedding method uses the through structure only [32]. Figure 6-4(a) shows a through and a circuit model; whereas Figure 6-4(b) shows a test pattern with pads and a device under test.



(a) a through and a circuit model



(b) A test pattern with pads and a device under test (DUT)

Figure 6-4: Connections and a circuit model for through only de-embedding [32]

The calculation of this method goes through equation (6.3) – (6.7) as follows. The Y_{thru} matrix of the through structure is [32]

$$Y_{thru} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} \frac{1}{Z_1} + \frac{1}{Z_2} & -\frac{1}{Z_2} \\ -\frac{1}{Z_2} & \frac{1}{Z_3} + \frac{1}{Z_2} \end{bmatrix} \quad (6.3)$$

Since the through property is symmetrical, the Y-matrixes of the left and right pads can be calculated as

$$Y_{pad}^{left} = \begin{bmatrix} Y_{11} - Y_{21} & 2Y_{21} \\ 2Y_{21} & -2Y_{21} \end{bmatrix} = \begin{bmatrix} \frac{1}{Z_1} + \frac{2}{Z_2} & -\frac{2}{Z_2} \\ -\frac{2}{Z_2} & \frac{2}{Z_2} \end{bmatrix} \quad (6.4)$$

$$Y_{pad}^{right} = \begin{bmatrix} -2Y_{12} & 2Y_{12} \\ 2Y_{12} & Y_{22} - Y_{12} \end{bmatrix} = \begin{bmatrix} \frac{2}{Z_2} & -\frac{2}{Z_2} \\ -\frac{2}{Z_2} & \frac{1}{Z_3} + \frac{2}{Z_2} \end{bmatrix} \quad (6.5)$$

Then, the T_{dut} matrix of the DUT can be de-embedded as,

$$Y_{thru} \Rightarrow Y_{pad}^{left},\ Y_{pad}^{right} \Rightarrow T_{pad}^{left},\ T_{pad}^{right} \quad (6.6)$$

$$T_{dut} = T_{pad}^{left^{-1}} \cdot T_{meas} \cdot T_{pad}^{right^{-1}} = T_{pad}^{left^{-1}} \cdot T_{pad}^{left} \cdot T_{dut} \cdot T_{pad}^{right} \cdot T_{pad}^{right^{-1}} \quad (6.7)$$

According to [33], the open-short equation may give negative resistance values for inductors and for passive devices that are not realistic; hence, the short-open technique is preferred. In addition, according to [32], the through only method has better self-consistency and higher accuracy than conventional methods 1 and 2 at higher frequencies; hence, it is better for high frequency de-embedding.

6.2 Results of Experimentation

In this section, the measurement results of the stacked inductors and the amplifiers presented in this thesis will be discussed. Figure 6-5 shows the micrograph of the chip, where a red label GSG area is used for the stacked inductors and a blue label GSG area is used for the amplifiers with inductive peaking and using the stacked inductors.

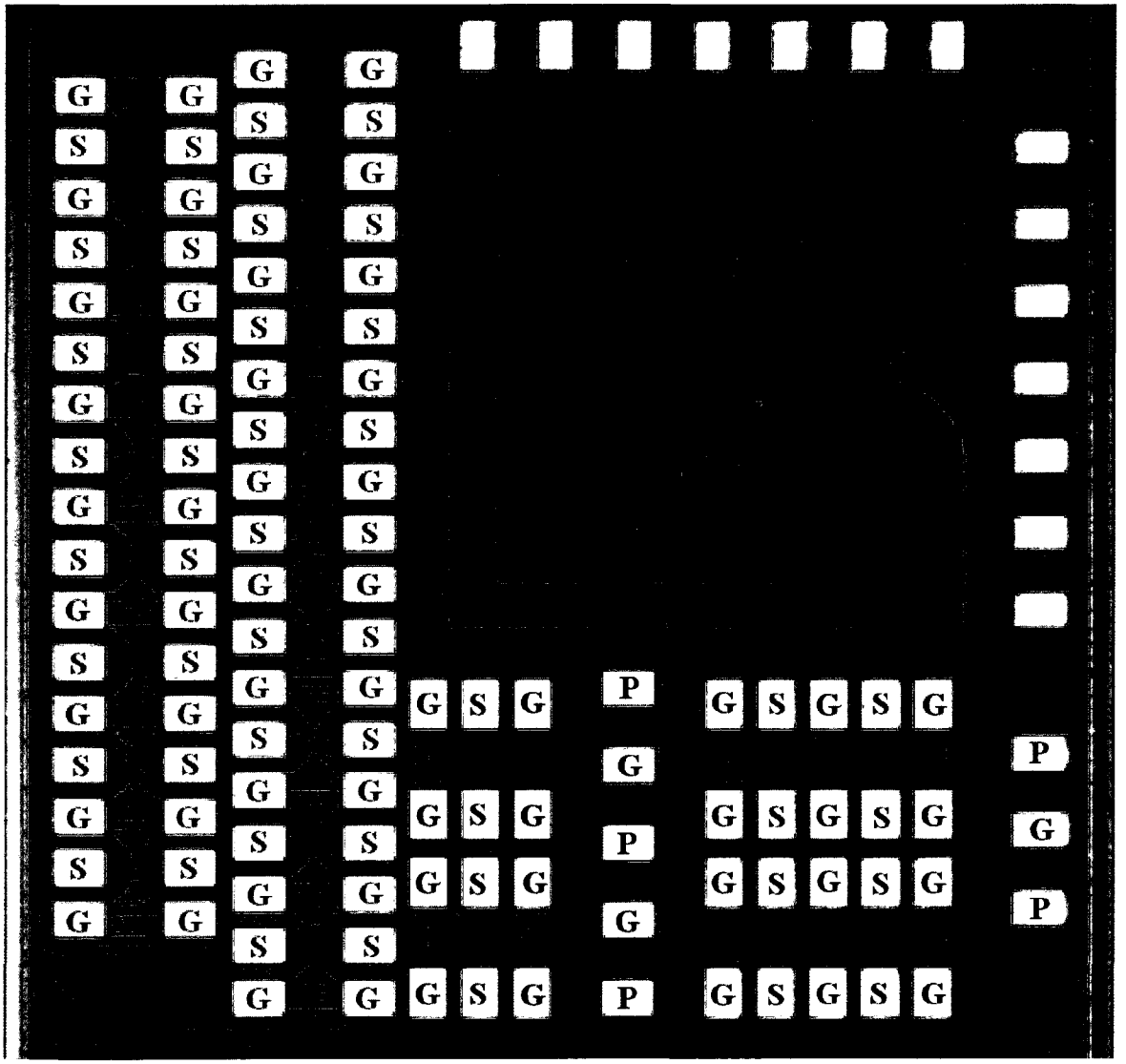


Figure 6-5: Photo of micrograph of the chip for inductors and amplifiers

6.2.1 Two-port Inductor Testing

The two port inductors are measured to explore the effect of patterned ground shielding on the small stacked inductors. The structures were tested, including the 248pH inductor that is made by 4 metals stacked (M5 to M2), 9.5μm×9.5μm outer dimension, 1.5 turns, 1.9μm metal width, and 0.6μm spacing and the 430pH inductor that is made by 3 metals stacked (M5 to M3), 20μm×20μm outer dimension, 2 turns, 2μm metal width, and 2μm spacing as shown in Figure 4-14. Figure 6-6 shows the micrograph of one of the stacked inductor in two port characterization. Each tested structure was measured in 4 chips. Measurements were done using the Agilent E8361A, which has an operating frequency range from 10 MHz to 67 GHz. The structures shown here were probed using GGB Industries 67A-GSG-100-P probes, and the network analyzer was calibrated with GGB industries CS-5 calibration substrate.

Figure 6-6: Example micrograph of the 248pH inductor in two-port characterization

Figure 6-7 to 6-10 and Figure 6-12 to 6-17 compared the simulated and measured Q and L of the 430pH and 248pH stacked inductor with different pattern ground shielding respectively. The measurement results reasonably matched the simulation results. However, there still are difference between the results that may be due to the non-ideal de-embedding structures, the low level auto-metal-fills around and inside the inductor, the skating parasitic causing by the move of the probe across the pad, the simplified via connection in the simulation, and differences between simulation and fabrication models.

In addition, Figure 6-11 and 6-18 compares the measured Q and L for these two stacked inductors with different PGSs respectively. The measurement results show consistency for both inductors when compared to simulation and the small stacked structures with different PGSs have not changed significantly in the L and Q. These results are similar to the simulation in section 4.5.1 that can be explained as the small open center of the inductor and small overlap area that contribute a small additional parasitic. Hence, the effect of the PGS on L and Q is very small. According to the micrograph in Figure 6-6, there are still some low level auto-metal-fills in the center of the inductors. This metal fill can further reduce the magnetic flux that penetrates through the center of the inductor into the substrate and thus reduce the inductance. As mentioned, although the additional parasitic capacitance due to the PGSs is small, the measurement results show that the increase in parasitic capacitance is more compared to the decrease in substrate loss. Hence, the Q factors of the small stacked inductors are decreased when patterned ground shields are placed underneath, as shown in Figure 6-11 and 6-18.

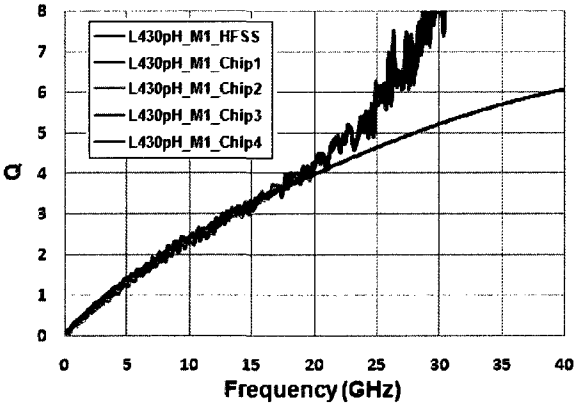


Figure 6-7: Simulated and measured Q of the 430pH inductor with M1 PGS

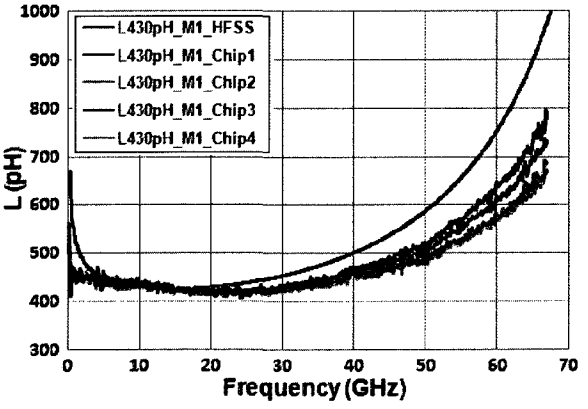


Figure 6-8: Simulated and measured L of the 430pH inductor with M1 PGS

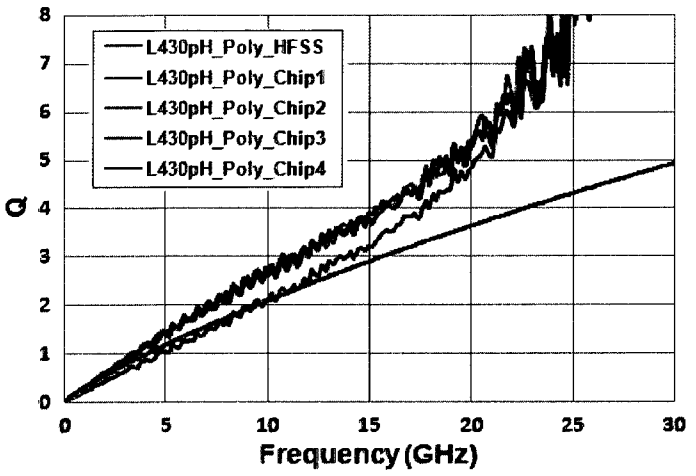


Figure 6-9: Simulated and measured Q of the 430pH inductor with Poly PGS

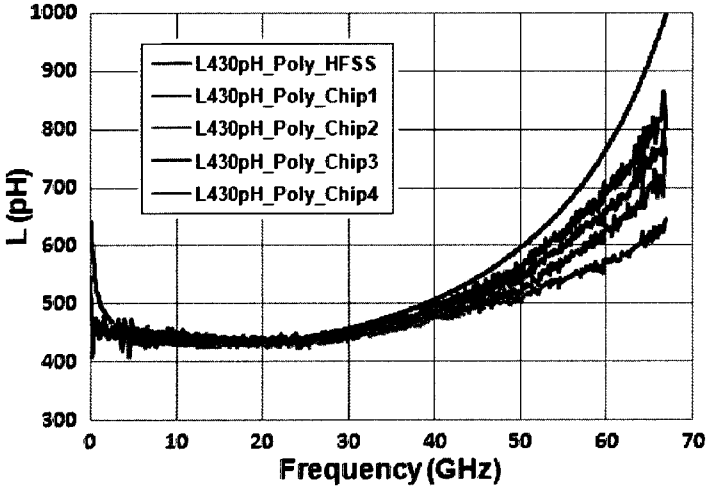


Figure 6-10: Simulated and measured L of the 430pH inductor with Poly PGS

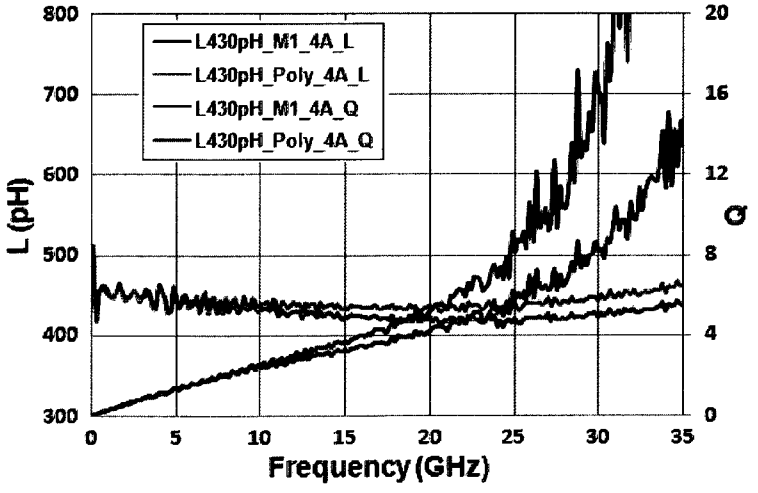


Figure 6-11: the measured Q and L of the 430pH inductor with different PGSs

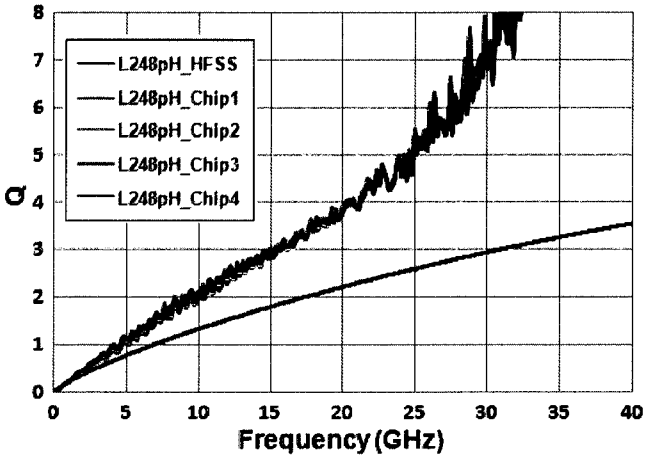


Figure 6-12: Simulated and measured Q of the 248pH inductor without PGS

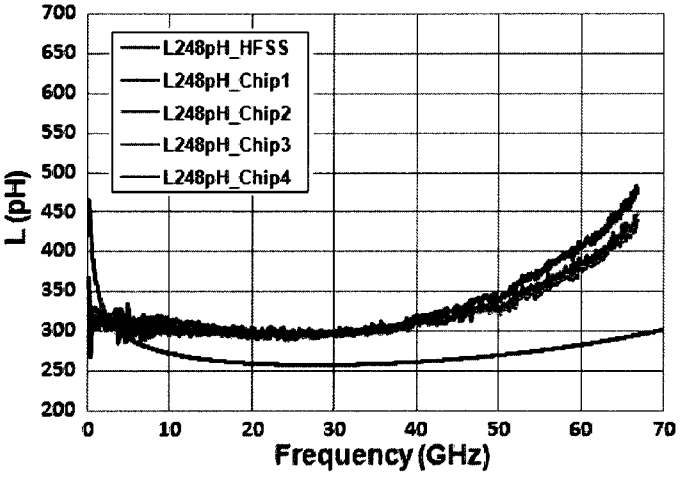


Figure 6-13: Simulated and measured L of the 248pH inductor without PGS

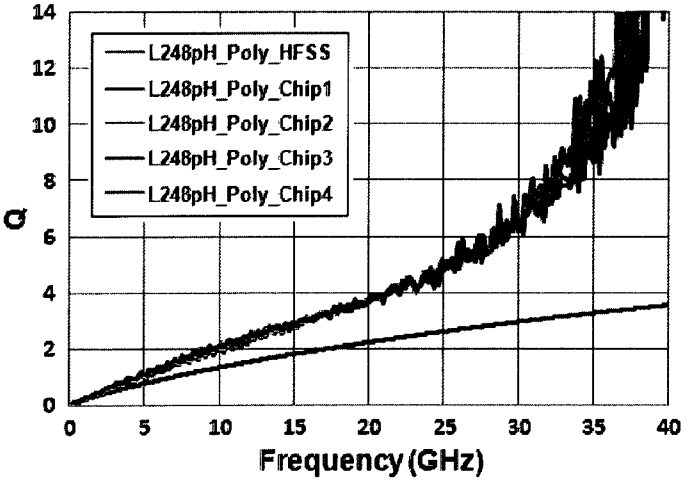


Figure 6-14: Simulated and measured Q of the 248pH inductor with Poly PGS

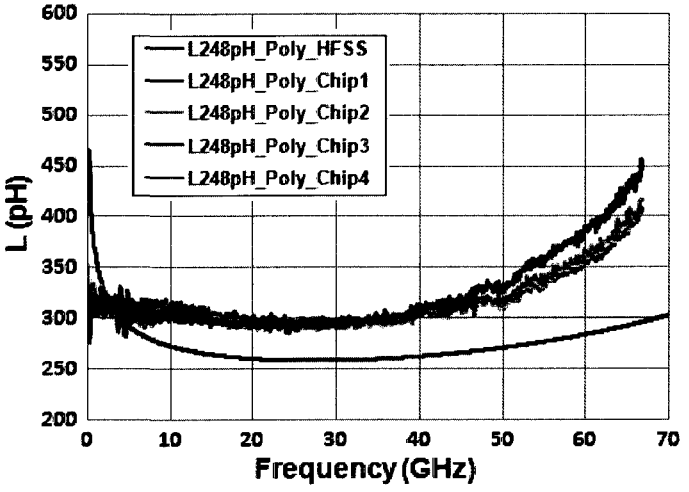


Figure 6-15: Simulated and measured L of the 248pH inductor with Poly PGS

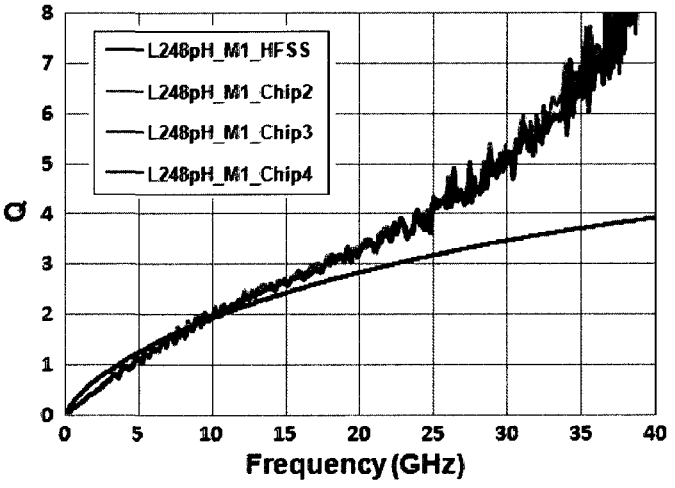


Figure 6-16: Simulated and measured Q of the 248pH inductor with M1 PGS

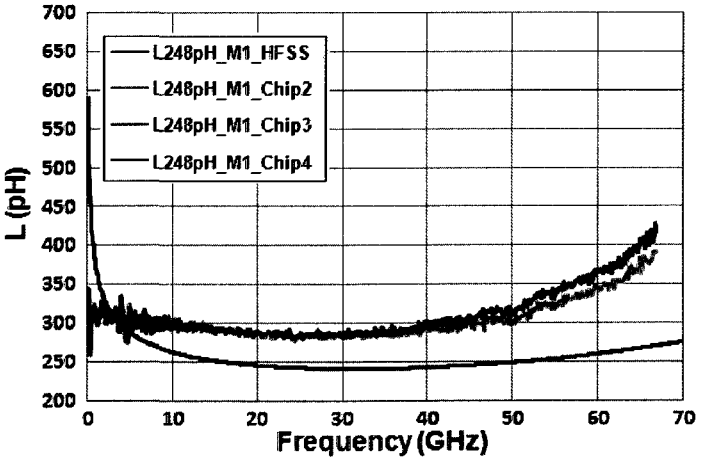


Figure 6-17: Simulated and measured L of the 248pH inductor with M1 PGS

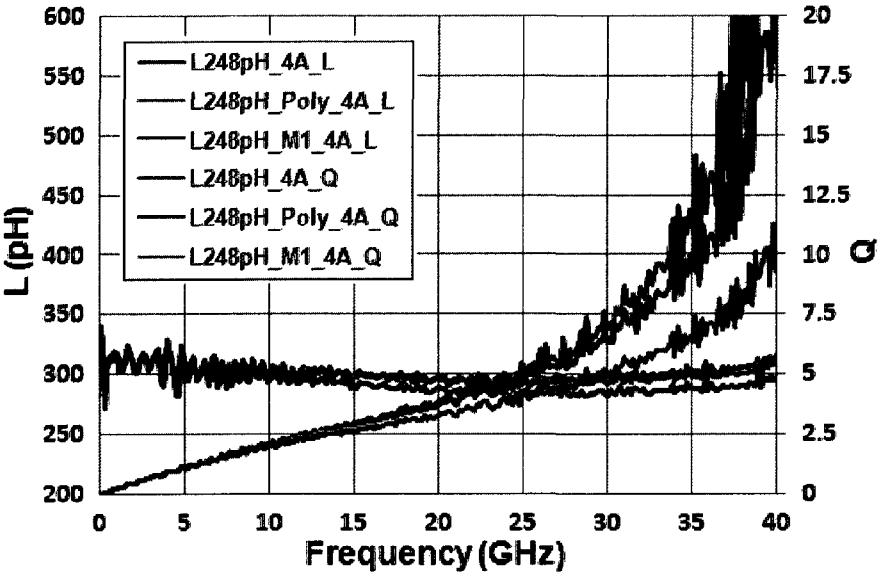


Figure 6-18: the measured Q and L of the 248pH inductor with different PGSs

6.2.2 One-port Inductor Testing

Figure 6-19 shows the micrograph of the 430pH and 248pH single ended stacked inductor pairs. These two stacked inductors have been fabricated with M1 and poly pattern ground shielding underneath to explore the coupling effect. Figures 6-20 to 6-27 show the total inductance L, Q factor, coupling coefficient k, and mutual inductance M of the 430pH and 248pH stacked inductors.

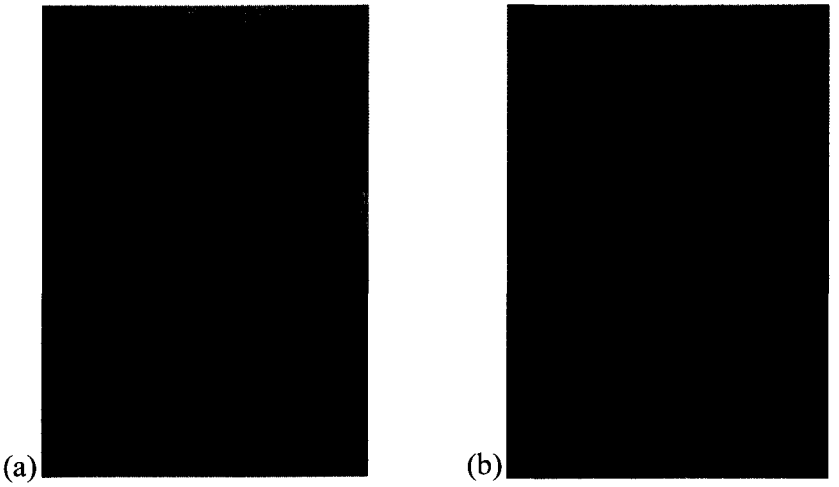


Figure 6-19: Micrograph of two single ended stacked inductor pairs, (a) 430pH and (b) 248pH

According to Figures 6-20 and 6-21, the comparison of the Q factors of both inductors, they show consistently that the pattern ground shields have no significant effect on the Q factors. These are similar to the two port measurement results. Again, it is possibly due to the very small inductor structure and the low level auto-metal-fills, as can be seen in Figure 6-19. These low level auto-metal-fills possibly degraded the performance of the PGS when the center opening of a stacked inductor is small and only about $50\mu m^2$; whereas a regular common planar inductor has center opening about $2500\mu m^2$ or more area. The discrepancies of the Q factor at high frequency could be caused by the non-ideal de-embedding structures.

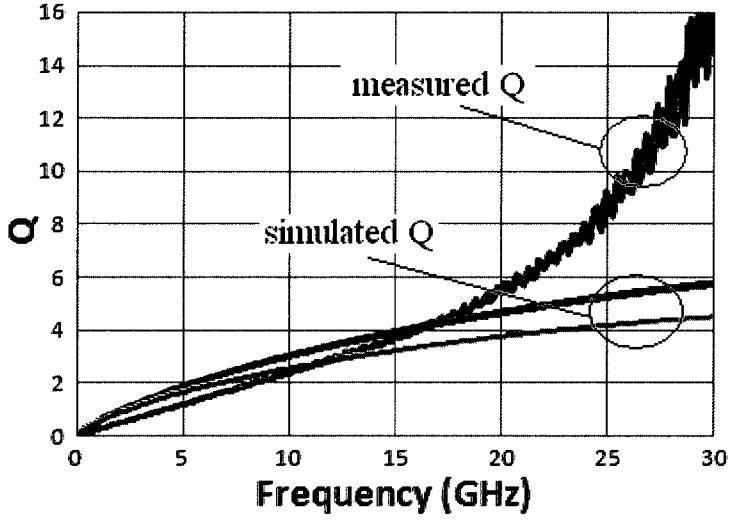


Figure 6-20: Simulated and measured Q of the single ended 430pH stacked inductor

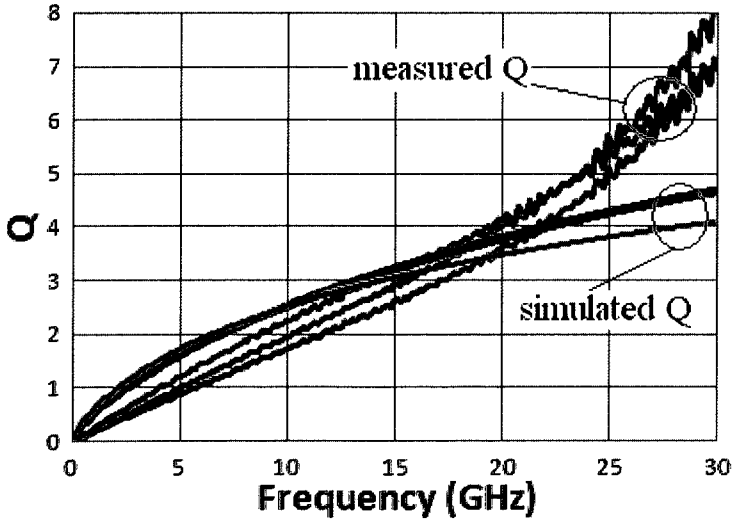


Figure 6-21: Simulated and measured Q of the single ended 248pH stacked inductor

According to Figure 6-22 and 6-23, the comparison of total inductance L for both inductors, they also show consistently that the pattern ground shields have no significant effect on the inductance. In addition, for both inductors, the simulated inductances are about 60pH less than the measured results. The reason for these differences may be due to the increase in coupling coefficient k and the mutual inductance M, as shown in Figure 6-24 and 6-27. The measured results are about double the values of the k and M compared to the simulated results. If the mutual inductances for both inductors are removed, the differences between the simulated and measured self-inductance would be reduced to about 10pH to 20pH, which is reasonably close considering the non-ideal de-embedding structures.

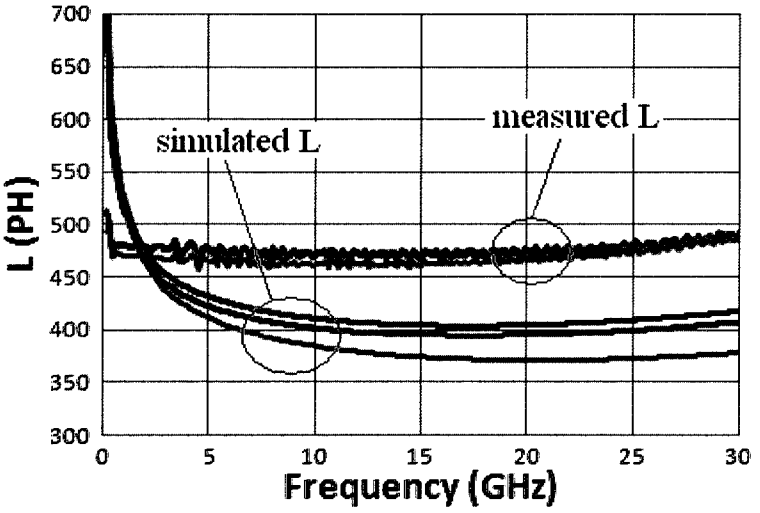


Figure 6-22: Simulated and measured L of the single ended 430pH stacked inductor

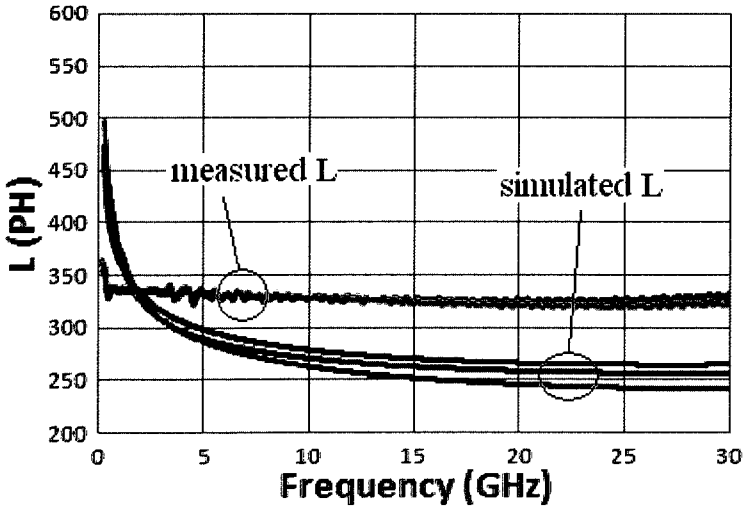


Figure 6-23: Simulated and measured L of the single ended 248pH stacked inductor

According to Figure 6-24 and 6-27, the measured coupling coefficient k and mutual inductance M of both stacked inductors were double or more the simulation results. The measured results also demonstrate that the pattern ground shielding has no significant effect on k and M. Thus, it is necessary to develop different isolation techniques for stacked inductors. The increase in k and M could be due the low level auto-metal-fills. Since the PGSs have no significant effect on the k and M based on the measured results, the signal will couple to another inductor horizontally through the parasitic capacitance between the inductor and the auto-metal-fill rather than vertically through the substrate. This is possible because although the inductors have been separated by more than 6 or 7 times the metal width of the inductors, the physical separation between the inductors is very small, only about 15μm to 20μm; whereas the planar inductors usually have much more separation.

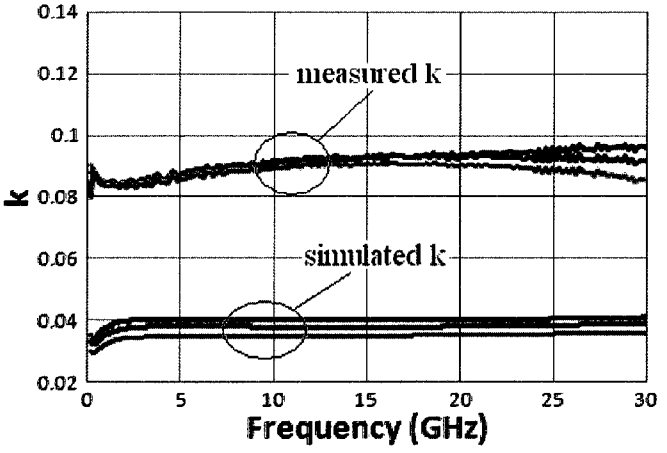


Figure 6-24: Simulated and measured k of the single ended 430pH stacked inductor

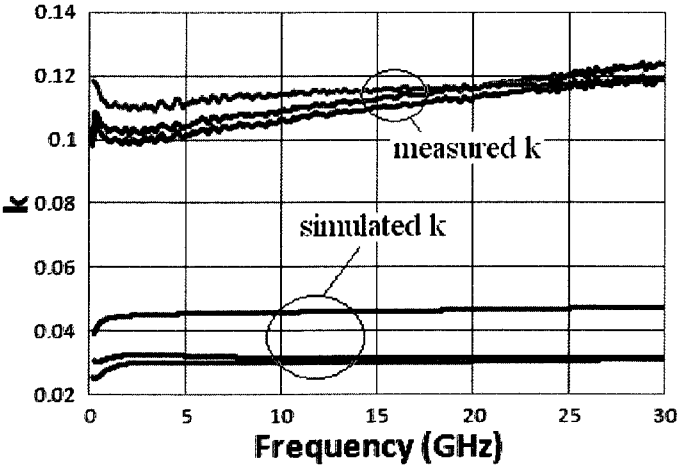


Figure 6-25: Simulated and measured k of the single ended 248pH stacked inductor

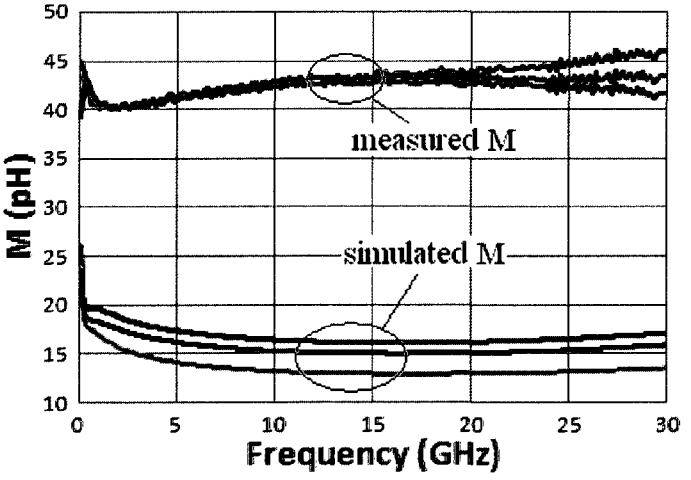


Figure 6-26: Simulated and measured M for the single ended 430pH stacked inductor

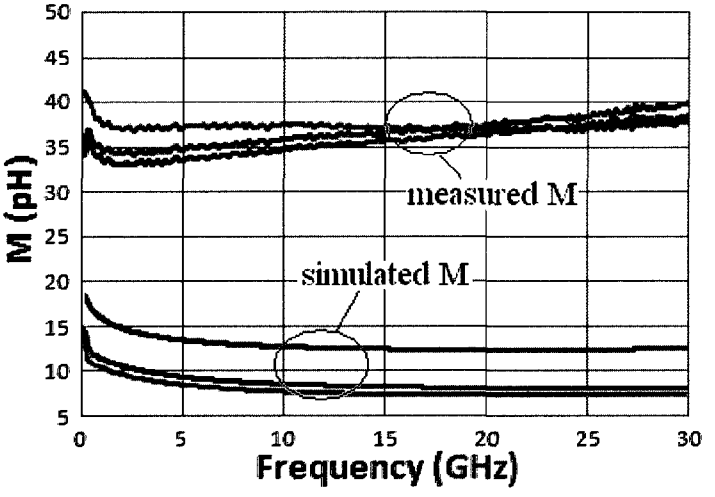


Figure 6-27: Simulated and measured M of the single ended 248pH stacked inductor

All the inductance simulation results are less than the measurement results, this may due to the non-ideal de-embedding structures and the air box that is too small in HFSS for the simulation (the typical need would be 3 times the line width).

6.2.3 Amplifier Testing

The micrograph of the amplifiers with inductive peaking is shown in Figure 6-28. The reference amplifier does not use any peaking technique, and the same amplifier implementing different stacked inductors have also been labeled in Figure 6-28. Table 6 summarizes the

bandwidth, bandwidth improvement and the peaking inductor structures of the first four amplifiers with inductive peaking in Figure 6-29.

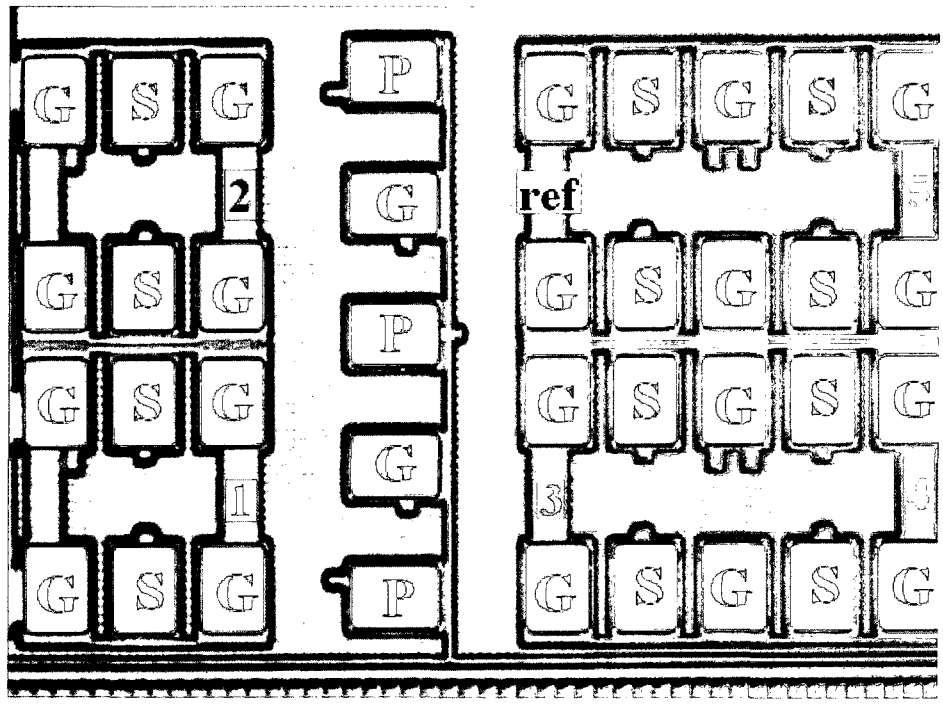


Figure 6-28: The micrograph of the CS amplifiers with inductive peaking

According to Table 6 and the measurement results in Figure 6-29, the reference amplifier has a -3dB bandwidth of approximately 10.65 GHz. The red curve in Figure 6-29 shows that amplifier 1 that uses a 430pH 3 layer stacked inductor with poly PGS producing a -3dB bandwidth about 18.45 GHz, a 73% improvement compared to the reference amplifier while only showing about 1.1dB of gain peaking. The blue curve shows amplifier 2 that uses a 430pH 3 layers stacked inductor with M1 PGS has a -3dB bandwidth of about 17.15 GHz, which corresponds to a 61% improvement while showing 1.1dB of gain peaking; the decrease in bandwidth is mainly due to the reduction in the inductance when using M1 PGS for the inductors. Both amplifiers 1 and 2 used the same structures but with different PGSs stacked inductors for peaking. However, amplifier 3 used smaller outer dimensions for the stacked inductor with one more level of metal and with no PGS; hence, the smaller stacked inductor with 4 layers has a similar inductance of about 420pH and amplifier 3 has flat gain with the same bandwidth improvement as amplifier 2. The green curve in Figure 6-29 shows that

amplifier 4 that uses the 248pH 4 layer stacked inductor without PGS has -3dB bandwidth about 13.5 GHz, which is a 27.7% improvement compared to the reference amplifier. In addition, according to Figure 6-29, the amplifiers using peaking inductors with PGSs have a flat gain in the frequency region from DC to about 1GHz.

Table 6: Inductor structures and bandwidth summary of the CS amplifiers

Amp	Peaking Inductor Structures							BW (GHz)	BW improvement
	L (pH)	D (um)	W (um)	S (um)	N	Layer	PGS		
Ref	---	---	---	---	---	---	---	10.65	Ref
1	430	20	2	2	2	3 to 5	Poly	18.45	73%
2	430	20	2	2	2	3 to 5	M1	17.15	61%
3	420	15	1.6	1.6	1.75	2 to 5	no	17.18	61%
4	248	13.5	1.9	0.6	1.5	2 to 5	no	13.6	27.7%

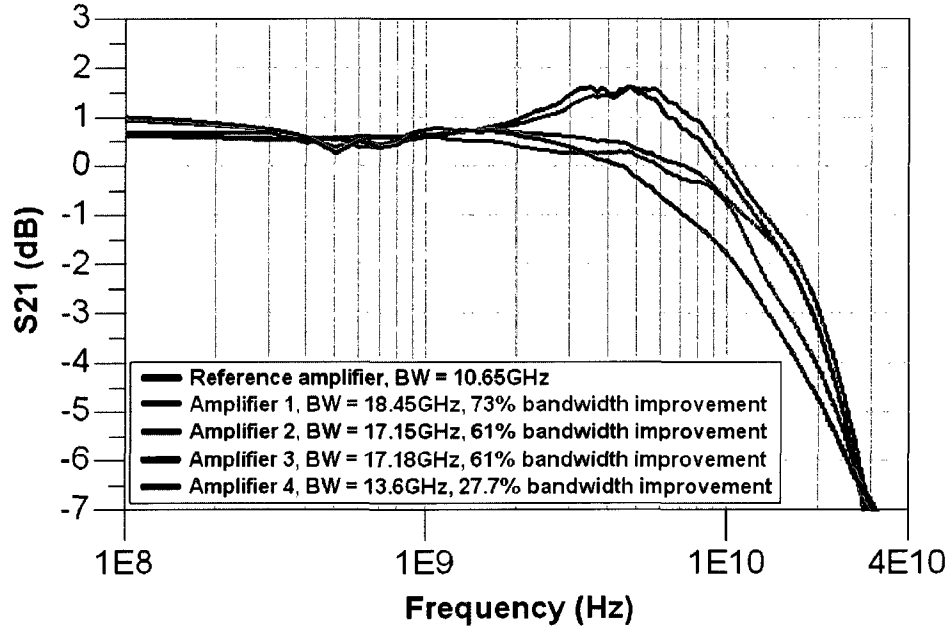


Figure 6-29: The measured S21 of the CS amplifiers with inductive peaking

Amplifier 5 in Figure 6-28 was implemented using a 430pH 3 layer stacked inductor without PGS but with double the ESD protection. Figure 6-30 shows the schematic of the amplifier with the ESD protection. The ESD protection can be defined as an equivalent capacitor connected to ground. According to the measurement results from the previous section, the inductors that implement poly PGS and no PGS have very close Q and L. Thus, the S-

parameter of amplifier 1 using the inductor with poly PGS will be re-simulated with a parallel capacitor (equivalent circuit of the ESD protection) at the input of the amplifier to estimate how much extra parasitic capacitance has been added to amplifier 5 due to the double ESD protection. Once the equivalent capacitance is defined, it can be added to the input of the reference amplifier to predict the reference amplifier bandwidth with double ESD protection. The results are shown in Figure 6-31, where amplifier 5 can improve the bandwidth about 57%.

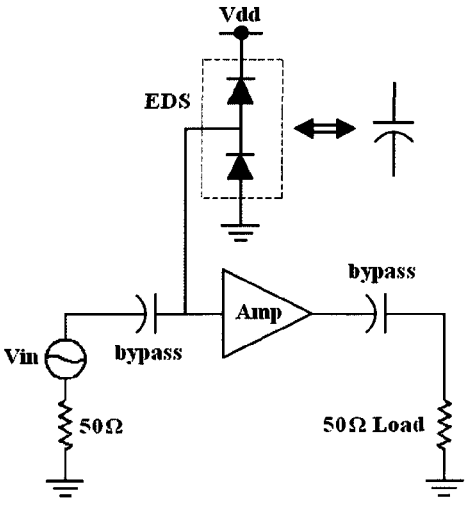


Figure 6-30: schematic of the amplifier with the ESD protection

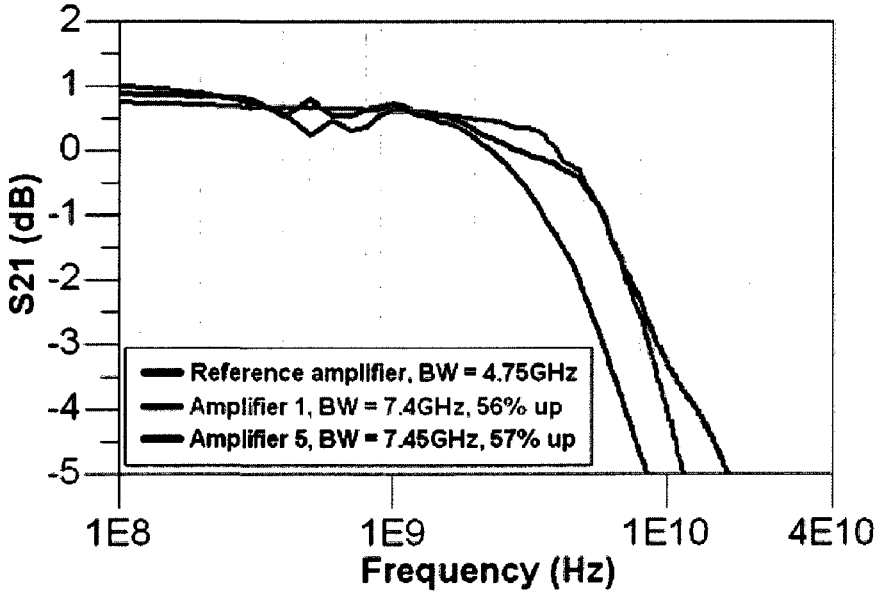


Figure 6-31: The measured S21 of the CS amplifier 5 after redefined the input ESD of the reference amplifier

6.2.4 Problems encounter during Amplifiers Testing

A major problem was encountered during the testing of the amplifier. The Vdd of the reference amplifier and amplifier 3 as shown in Figure 6-28 was found to be shorted to ground by a layout mistake. When applying the simulated DC bias to these two amplifiers, current limiting occurred and the voltmeter showed only 0.23 V for Vdd, not the required 1.2V power supply; hence no measurement results could be obtained initially. The first possible solution is the use of laser trimming technology to disconnect the direct connection from Vdd to ground. However, the measurement results after the laser trimming did not changed. Then, we tried to increase the current limit of the power supply; the voltmeter showed that the voltage at the Vdd was increasing. When Vdd reached about 1.2V, the reference amplifier and amplifier 3 began working reasonably well that the total current reading from Amp-meter was about 216mA.

From this observation, although Vdd was connected to ground with the top level metal MA, this connection is not ideal, which has several ohm resistance as shown in Figure 6-32. The voltage across the R_2 depends on the applied current I_2. When the current is limited, the voltage for Vdd will never research 1.2V. Hence, the amplifiers' supply was too low. As the current was increased, and due to the existence of some resistance between the Vdd and ground, the voltage across the R_2 will increase until Vdd reaches 1.2V. Then Vdd will be high enough for the amplifier to begin operating, but the R_2 theoretical has no effect on the performance of the amplifiers. Thus, the measurement results still can be used to demonstrate the purpose of inductive peaking.

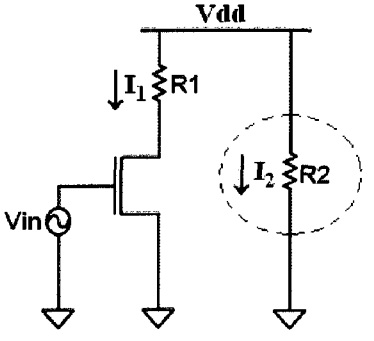


Figure 6-32: schematic of the amplifier with not ideal connection from Vdd to ground

Chapter 7 Conclusions

7.1 Summary of Work in this Thesis

In this thesis, a detail design consideration and procedures for stacked inductors using ASITIC and HFSS modeling programs have been presented. Two new isolation techniques for the small stacked inductor have also been presented. The coupling effects of various isolation techniques to the stacked inductor have been studied. Simulation and measurement results show that adding PGS to the small stacked inductor has no significant effect on the Q factor. Hence, the PGS is not necessary for the super compact stacked inductor. Simulation results also show that the Gaussian side wall technique can be chosen to provide maximum isolation for certain applications and with no significant effect on the Q, L and the self-resonance frequency f_{res}. All the simulation results for inductances are less than the measurement results; this may due to the non-ideal de-embedding structures and the air box that is too small in HFSS for the simulation (the typical need would be 3 times the line width).

The basic theory of amplifiers with various inductive peaking topologies has been studied. Simulation results suggest that using a T-coil inductive peaking topology can achieve the most bandwidth improvement when a large load capacitance is present. Several common source amplifiers that use different stacked inductors for peaking have been fabricated in IBM the 0.13μm CMOS process. Measurement results demonstrated the performance improvement of the stacked inductors for peaking purpose showing that the bandwidth can be improved about 73% while reducing the chip area by about 85% or more compared to using planar kit inductors from the manufacturer.

7.2 Thesis Contributions

The primary contributions of this thesis work are:

1. Using electromagnetic simulations to investigate the performance of small stacked inductors built with low level metals in CMOS technology.
2. Investigated the inductor performance due to temperature variation and techniques for maximum possible isolation.
3. The work done in this thesis can help to understand the flow to build and model stacked inductors in ASITIC, ADS, HFSS, which is technology independent.
4. Several common source amplifiers have been fabricated in IBM 0.13μm CMOS process. It was demonstrated that small stacked inductors can be used for inductive peaking amplifiers and it was proven that good bandwidth enhancement can be achieved while reducing chip area by a huge amount.

7.3 Future Work

Several topics relating to small stacked inductors have not been implemented in the test chip of this thesis, including the isolation effect due to different rotation of inductors, transformers, high coupling effect stacked inductor structures, and the measurement of the two new isolation techniques for the stacked inductor. Hence, one of the possible areas where this work could be extended would involve second design iteration in order to demonstrate the performance of stacked inductor transformers, high coupling structures, and the measurement of the new isolation techniques. In addition, the T-coil peaking topology requires that the inductors have a high coupling effect to provide higher bandwidth improvement. Therefore, there is still potential to further improve the bandwidth by exploring the high coupling effect of stacked inductors structures in a future tape-out.

Since the stacked inductors presented here have been demonstrated to achieve good bandwidth enhancement as peaking inductors when used in common source amplifiers, the next step could be to implement these stacked inductors into wireline circuits that operate at high data rate, such as MUX/DEMUX circuits and equalization circuits. The results obtained from this experiment will be very valuable since most high speed broadband applications require multi-stages circuits with peaking inductors and using small stacked inductors for peaking can reduce the chip area dramatically resulting in a reduction in the cost of fabrication.

References

[1] S. R. Taub and S. A. Alterovitz, "Silicon Techologies adjust to RF Applications," *Microwaves RF*, vol. 33, no. 10, 1994, pp. 60–74, 1994.

[2] S. Shekhar, J. S. Walling, and D. J. Allstot, "Bandwidth Extension Techniques for CMOS Amplifiers," *IEEE Journal of Solid-state Circuits*, vol. 41, no. 11, pp.2424–2439, Nov 2006.

[3] J. Kim, J.-K. Kim, B.-J. Lee, M.-S. Hwang, H.-R. Lee, S.-H. Lee, N. Kim, D.-K. Jeong, and W. Kim, "Circuit techniques for a 40 Gb/s transmitter in 0.13μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig.Tech.Papers*, Feb. 2005, pp. 150–151, 589.

[4] K. Kanda, D. Yamakazi, T. Yamamoto, M. Horinaka, J. Ogawa, H. Tamura, and H. Onodera, "40 Gb/s 4:1 MUX/1:4 DEMUX in 90 nm standard CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech.Papers*, Feb. 2005, pp. 152–153, 590.

[5] S. Galal and B. Razavi, "40 Gb/s amplifier and ESD protection circuit in 0.18μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2389–2396, Dec. 2004.

[6] Ansoft., HFSS - 3D Full-wave Electromagnetic Field Simulation. [Online] http://www.ansoft.com/hfss.

[7] C. C. Tang, C. H. Wu, and S. I. Liu, "Miniature 3-D Inductors in Standard CMOS Process," in *IEEE Journal of Solid-state Circuits*, vol. 37, no. 4, pp.471–480, Apr 2002.

[8] J. Lu, H. Jia, A. Arias, X. Gong, Z. J. Shen, "On-Chip Bondwire Magnetics with Ferrite-Epoxy Glob Coating for power Systems on Chip," in *International Journal of Power Management Electronics*, vol 2008, ID 678415

[9] J. Aguilera, and R. Berenguer, *Design and Test of Integrated Inductors for RF Applications*, Kluwer Academic Publishers, pp.19–21, 39-40, 2004

[10] Ansoft., Maxwell SV, http://www.ansoft.com/maxwellsv/ [Online]

[11] N. A. Talwalkar, "Analysis and Synthesis of On-Chip Spiral Inductors," *IEEE Transactions On Electron Devices*, vol. 52, no. 2, Feb 2005.

[12] Christensen, K. T., "Easy Simulations and Design of On-Chip Inductors in Standard CMOS Processes," *IEEE International Symposium on Circuits and Systems*, pp 360-364, 1998.

[13] IBM Foundry and Manufacturing Services Education, Design Kit Trainning [Online] http://www.ibm.com/chips

[14] Swanson, Daniel G. and Hoefer, Wolfgang J.R., *Microwave Circuit Modeling Using Electromagnetic Field Simulation*, Boston Artech House, 2003. p. 36. 1-58053-308-6.

[15] D. Jack, *Efficient Inductor layout geometries for Radio Frequency Integrated Circuits*, master thesis, 2008, pp. 19-22.

[16] D. B. Davidson, *Computational Electromagnetics for RF and Microwave Engineering*, Cambridge University press, 2005, pp. 7-9, 13-16.

[17] T. Blalack, Y. Leclercq, and C. P. Yue, "On-chip RF isolation techniques," *Bipolar/BiCMOS Circuit and Technology Meeting*, pp. 205-211, Sept 29, 2002

[18] C. Chen, J.W. Chou, W. Lur, and S.W. Sun, "A novel 0.25 μm shallow trench isolation technology," *Electron Devices Meeting*, pp. 837 – 840, Dec. 8-11, 1996

[19] J. Rogers, and C. Plett, *Radio Frequency Integrated Circuit Design,* Boston: Artech House, 2003

[20] M. W. Geen, G. J. Green, R. G. Arnold, J. A. Jenkins, and R. H. Jansen, "Miniature Multilayer Spiral Inductors For GaAs MMICs," *GaAs IC Symposium*, pp. 303-306, 1989.

[21] A. M. Niknejad, and R. G. Meyer, *Design, Simulation and Applications of Inductors and Transformers for Si RF ICs*, Kluwer Academic Publishers, pp. 21–24, 97-98, 2008

[22] A. M. Niknejad, ASITIC, http://rfic.eecs.berkeley.edu/~niknejad/asitic.html [Online]

[23] A. M. Niknejad, "Modeling of Passive Elements with ASITIC," *IEEE RFIC Symposium*, pp. 303-306, 2002.

[24] A. Niknejad and R. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RFIC's," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1470-1481, October 1998.

[25] T.O. Dickson, M.-A. LaCroix, S. Boret, D. Gloria, R. Beerkens, S.P. Voinigescu, "30-100-GHz inductors and transformers for millimeter-wave (Bi)CMOS integrated circuits," *Microwave Theory and Techniques, IEEE Transactions*, vol 53, pp. 123-133, Jan. 2005.

[26] J. R. Long, M. A. Copeland, "The Modeling, Characterization, and Design of Monolithic Inductors for Silicon RF IC's", *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 357-369, March 1997.

[27] L. Travis, *A Delay Cell for 40 Gb/s*, master thesis, 2007, pp. 23-25.

[28] Y. Cao, G. Wang, "A Wideband and Scalable Model of Spiral Inductors Using Space-Mapping Neural Network," *Microwave Theory and Techniques, IEEE Transactions*, vol 55, pp. 2473-2480, Dec. 2007.

[29] P. Staric, W. Margan, *Wideband Amplifiers*, published by Springer, 2006, pp. 2.35-2.50

[30] Cascade microtech, http://www.cmicro.com/products/calibration-tools/impedance-substrate/impedance-standard-substrates [online]

[31] M.C.A.M. Koolen, J.A.M. Geelen, M.P.J.G. Versleijen, "An Improved De-Embedding Technique For On-Wafer High-Frequency Characterization", *IEEE Bipolar Circuits and Technology Meeting*, pp. 188-191, 1991.

[32] Ito. H, Masuv. K, "A simple through-only de-embedding method for on-wafer S-parameter measurements up to 110 GHz", *Microwave Symposium Degest, 2008 IEEE MTT-S International*, 18 June, 2008, page: 383-386

[33] Tiemeijer, Luuk F. and Havens, Ramon J., "A Calibrated Lumped-Element De-Embedding Technique for On-Wafer RF Characterization of High-Quality Inductors and High-Speed Transistors." *IEEE Transactions on Electron Devices*, March 2003, Issue 3, Vol. 50.

[34] Cadence Design Systems. [Online] http://www.cadence.com

[35] Serway, Raymond A. (1998). *Principles of Physics* (2nd ed.). Fort Worth, Texas; London: Saunders College Pub. pp. 602

Appendix A: Sample ASITIC Technology File

The following is the technology file that was written for ASITIC by Travis Lovitt [99], one of the group members who was involved in the initial research of stacked inductors. Due to the non-disclosure agreement of the technology, electrical and physical values have been removed (values replaced with "??"), but the overall structure is still shown.

```
; IBM 8RF_DM (0.13um CMOS) Technology file
; Travis Lovitt, January 2006

; based on the following construction:
; - poly, M1, M2, M3, MQ, MG, LY, E1, MA
; - BF on substrate (no pwell - low conductivity)

<chip>

        chipx = 256 ; dimensions of the chip in x direction
        chipy = 256 ; dimensions of the chip in y direction
        fftx = 512 ; x-fft size (must be a power of 2)
        ffty = 512 ; y-fft size
        TechFile = ibm_8rf_dm.tek
        TechPath = .
        freq = 10 ; frequency of operation
        eddy = 0

<layer> 0               ; substrate layer
        rho = ??        ; resistivity ohm-cm
        t   = ??        ; thickness um
        eps = ??        ; permittivity

<layer> 1               ; STI layer
        rho = ??
        t   = ??
        eps = ??
<layer> 2               ; poly layer
        rho = ??
        t   = ??
        eps = ??

<layer> 3               ; poly to M1 layer
        rho = ??
        t   = ??
        eps = ??

<layer> 4               ; M1 oxide layer
        rho = ??
        t   = ??
        eps = ??

<layer> 5               ; M1 to M2 oxide layer
        rho = ??
        t   = ??
```

```
        eps = ??

<layer> 6               ; M2 oxide layer
        rho = ??
        t   = ??
        eps = ??

<layer> 7               ; M2 to M3 oxide layer
        rho = ??
        t   = ??
        eps = ??

<layer> 8               ; M3 oxide layer
        rho = ??
        t   = ??
        eps = ??

<layer> 9               ; M3 to MQ oxide layer
        rho = ??
        t   = ??
        eps = ??

<layer> 10              ; MQ oxide layer
        rho = ??
        t   = ??
        eps = ??

<layer> 11              ; MQ to MG oxide layer
        rho = ??
        t   = ??
        eps = ??

<layer> 12              ; MG oxide layer
        rho = ??
        t   = ??
        eps = ??

<layer> 13              ; MG to LY oxide layer
        rho = ??
        t   = ??
        eps = ??

<layer> 14              ; LY oxide layer
        rho = ??
        t   = ??
        eps = ??

<layer> 15              ; LY to E1 oxide layer
        rho = ??
        t   = ??
        eps = ??

<layer> 16              ; E1 oxide layer
        rho = ??
        t   = ??
        eps = ??
```

```
<layer> 17              ; E1 to MA oxide layer
        rho = ??
        t   = ??
        eps = ??

<layer> 18              ; MA oxide layer
        rho = ??
        t   = ??
        eps = ??

<layer> 19              ; passivation oxide layer
        rho = ??
        t   = ??
        eps = ??

<layer> 20              ; passivation nitride layer
        rho = ??
        t   = ??
        eps = ??

<layer> 21              ; passivation polyimide layer
        rho = ??
        t   = ??
        eps = ??

<layer> 22              ; air
        rho = ??
        t   = ??
        eps = ??

<metal> 0               ; poly
        layer = 2       ; in which oxide layer
        rsh   = ??      ; sheet resistance mOhm/sq
        t     = ??      ; thickness
        d     = 0       ; distance from bottom of layer
        name = poly
        color = orange

<metal> 1               ; M1
        layer = 4
        rsh = ??
        t = ??
        d = 0
        name = m1
        color = blue

<metal> 2               ; M2
        layer = 6
        rsh = ??
        t = ??
        d = 0
        name = m2
        color = cyan

<metal> 3               ; M3
```

```
        layer = 8
        rsh = ??
        t = ??
        d = 0
        name = m3
        color = pink

<metal> 4               ; MQ
        layer = 10
        rsh = ??
        t = ??
        d = 0
        name = mq
        color = green

<metal> 5               ; MG
        layer = 12
        rsh = ??
        t = ??
        d = 0
        name = mg
        color = yellow

<metal> 6               ; LY
        layer = 14
        rsh = ??
        t = ??
        d = 0
        name = ly
        color = lightbrown

<metal> 7               ; E1
        layer = 16
        rsh = ??
        t = ??
        d = 0
        name = e1
        color = white

<metal> 8               ; MA
        layer = 18
        rsh = ??
        t = ??
        d = 0
        name = ma
        color = red

<via> 0                 ; poly to M1
        top = 1         ; via connects up to this metal layer
        bottom = 0      ; via connects down to this metal layer
        r = ??          ; resistance per via Ohm
        width = ??      ; width of via
        space = ??      ; min spacing between vias
        overplot1 = ??  ; min dist to bottom metal
        overplot2 = ??  ; min dist to top metal
        name = cont
```

```
        color = yellow

<via> 1                 ; M1 to M2
        top = 2         ; via connects up to this metal layer
        bottom = 1      ; via connects down to this metal layer
        r = ??          ; resistance per via Ohm
        width = ??      ; width of via
        space = ??      ; min spacing between vias
        overplot1 = ??  ; min dist to bottom metal
        overplot2 = ??  ; min dist to top metal
        name = v1
        color = lightbrown

<via> 2                 ; M2 to M3
        top = 3
        bottom = 2
        r = ??
        width = ??
        space = ??
        overplot1 = ??
        overplot2 = ??
        name = v2
        color = white

<via> 3                 ; M3 to MQ
        top = 4
        bottom = 3
        r = ??
        width = ??
        space = ??
        overplot1 = .01
        overplot2 = .01
        name = vl
        color = yellow

<via> 4                 ; MQ to MG
        top = 5
        bottom = 4
        r = ??
        width = ??
        space = ??
        overplot1 = ??
        overplot2 = ??
        name = vq
        color = purple

<via> 5                 ; MG to LY
        top = 6
        bottom = 5
        r = ??
        width = ??
        space = ??
        overplot1 = ??
        overplot2 = ??
        name = fy
        color = green
```

```
<via> 6                    ; LY to E1
        top = 7
        bottom = 6
        r = ??
        width = ??
        space = ??
        overplot1 = ??
        overplot2 = ??
        name = ft
        color = white

<via> 7                    ; E1 to MA
        top = 8
        bottom = 7
        r = ??
        width = ??
        space = ??
        overplot1 = ??
        overplot2 = ??
        name = f1
        color = red
```

Appendix B: Matlab Code for De-embedding

```
%% ====================================================================
%% the following code is the short-open de-embedding method
%% GENERAL START
restoredefaultpath
addpath(genpath(pwd))
clear
clc

load SHORT.s2p
load OPEN.s2p
load DUT1.s2p

I=sqrt(-1);

LU1=[]; QU1=[]; SU1FF=[];

for i=1:length(SHORT)

      Freq=SHORT(i,1);

      S11S=SHORT(i,2)+I*SHORT(i,3);
      S21S=SHORT(i,4)+I*SHORT(i,5);
      S12S=SHORT(i,6)+I*SHORT(i,7);
      S22S=SHORT(i,8)+I*SHORT(i,9);
      SS=[S11S,S12S;S21S,S22S]; %% S-parameter of the short structure
      ZS=s2z(SS);

      S11O=OPEN(i,2)+I*OPEN(i,3);
      S21O=OPEN(i,4)+I*OPEN(i,5);
      S12O=OPEN(i,6)+I*OPEN(i,7);
      S22O=OPEN(i,8)+I*OPEN(i,9);
      SO=[S11O,S12O;S21O,S22O]; %% S-parameter of the open structure
      ZO=s2z(SO);


      S11U1=DUT1(i,2)+I*DUT1(i,3);
      S21U1=DUT1(i,4)+I*DUT1(i,5);
      S12U1=DUT1(i,6)+I*DUT1(i,7);
      S22U1=DUT1(i,8)+I*DUT1(i,9);
      SU1=[S11U1,S12U1;S21U1,S22U1]; %% S-parameter of the DUT
      ZU1=s2z(SU1);

      %% Z-parameter of the DUT after de-embedding
      ZU1F=inv(inv(ZU1-ZS)-inv(ZO-ZS));
      SU1F=z2s(ZU1F);  %% Convert the Z-parameter to S-parameter
      Zin1=ZU1F(1,1)-ZU1F(1,2)*ZU1F(2,1)/ZU1F(2,2);

      Q1=imag(Zin1)/real(Zin1); %% Q value for a single frequency
      w=2*pi*Freq;
      L1=imag(Zin1)/w;    %% L value for a single frequency
```

```
      LU1=[LU1; Freq L1]; %% L value for all frequency range

      QU1=[QU1; Freq Q1]; %% Q value for all frequency range

      SU1FF=[SU1FF; Freq real(SU1F(1,1)) imag(SU1F(1,1)) real(SU1F(2,1))
         imag(SU1F(2,1)) real(SU1F(1,2)) imag(SU1F(1,2)) real(SU1F(2,2))
         imag(SU1F(2,2))];
      %% two-port S parameters of the DUT for all frequency range
end
%% ============================================================================


%% ============================================================================
%% the following code is the open-short de-embedding method
%% GENERAL START
restoredefaultpath
addpath(genpath(pwd))
clear
clc

load SHORT.s2p
load OPEN.s2p
load DUT1.s2p

I=sqrt(-1);

LU1=[]; QU1=[]; SU1FF=[];

for i=1:length(SHORT)

      Freq=SHORT(i,1);

      S11S=SHORT(i,2)+I*SHORT(i,3);
      S21S=SHORT(i,4)+I*SHORT(i,5);
      S12S=SHORT(i,6)+I*SHORT(i,7);
      S22S=SHORT(i,8)+I*SHORT(i,9);
      SS=[S11S,S12S;S21S,S22S]; %% S-parameter of the short structure
      YS=s2y(SS);

      S11O=OPEN(i,2)+I*OPEN(i,3);
      S21O=OPEN(i,4)+I*OPEN(i,5);
      S12O=OPEN(i,6)+I*OPEN(i,7);
      S22O=OPEN(i,8)+I*OPEN(i,9);
      SO=[S11O,S12O;S21O,S22O]; %% S-parameter of the open structure
      YO=s2y(SO);


      S11U1=DUT1(i,2)+I*DUT1(i,3);
      S21U1=DUT1(i,4)+I*DUT1(i,5);
      S12U1=DUT1(i,6)+I*DUT1(i,7);
      S22U1=DUT1(i,8)+I*DUT1(i,9);
      SU1=[S11U1,S12U1;S21U1,S22U1]; %% S-parameter of the DUT
      YU1=s2y(SU1);

      %% Z-parameter of the DUT after de-embedding
```

```
      ZU2F=y2z(inv(inv(YU2-YO)-inv(YS-YO)));
      SU1F=z2s(ZU1F);  %% Convert the Z-parameter to S-parameter
      Zin1=ZU1F(1,1)-ZU1F(1,2)*ZU1F(2,1)/ZU1F(2,2);

      Q1=imag(Zin1)/real(Zin1); %% Q value for a single frequency
      w=2*pi*Freq;
      L1=imag(Zin1)/w;    %% L value for a single frequency
      LU1=[LU1; Freq L1]; %% L value for all frequency range

      QU1=[QU1; Freq Q1]; %% Q value for all frequency range

      SU1FF=[SU1FF; Freq real(SU1F(1,1)) imag(SU1F(1,1)) real(SU1F(2,1))
         imag(SU1F(2,1)) real(SU1F(1,2)) imag(SU1F(1,2)) real(SU1F(2,2))
         imag(SU1F(2,2))];
      %% Two-port S parameters of the DUT for all frequency range
end
%% ========================================================================


%% ========================================================================
%% the following code is the through only de-embedding method
%% GENERAL START
restoredefaultpath
addpath(genpath(pwd))
clear
clc

load THROUGH.s2p
load OPEN.s2p
load DUT1.s2p

I=sqrt(-1);

LU1=[]; QU1=[]; SU1FF=[];

for i=1:length(THROUGH)

      Freq=THROUGH(i,1);

      S11=THROUGH(i,2)+I*THROUGH(i,3);
      S21=THROUGH(i,4)+I*THROUGH(i,5);
      S12=THROUGH(i,6)+I*THROUGH(i,7);
      S22=THROUGH(i,8)+I*THROUGH(i,9);
      S=[S11,S12;S21,S22]; %% S-parameter of the through structure
      Y=s2y(S);
      Y11=Y(1,1);Y21=Y(2,1);Y12=Y(1,2);Y22=Y(2,2);
      YL=[Y11-Y21,2*Y21;2*Y21,-2*Y21];
      YR=[-2*Y12,2*Y12;2*Y12,Y22-Y12];
      TL=s2t(y2s(YL)); %% T-matrix of the left half through structure
      TR=s2t(y2s(YR)); %% T-matrix of the right half through structure

      S11U1=DUT1(i,2)+I*DUT1(i,3);
      S21U1=DUT1(i,4)+I*DUT1(i,5);
      S12U1=DUT1(i,6)+I*DUT1(i,7);
      S22U1=DUT1(i,8)+I*DUT1(i,9);
```

```
      SU1=[S11U1,S12U1;S21U1,S22U1]; %% S-parameter of the DUT
      TU1=s2t(SU1);

      SU1F=t2s(TL\TU1/TR); %% S-parameter of the DUT after de-embedding
      ZU1F=s2z(SU1F); %% Convert the S-parameter to Z-parameter
      Zin1=ZU1F(1,1)-ZU1F(1,2)*ZU1F(2,1)/ZU1F(2,2);

      Q1=imag(Zin1)/real(Zin1);  %% Q value for a single frequency
      w=2*pi*Freq;
      L1=imag(Zin1)/w;       %% L value for a single frequency
      LU1=[LU1; Freq L1];    %% L value for all frequencies
      QU1=[QU1; Freq Q1];    %% Q value for all frequencies

      SU1FF=[SU1FF; Freq real(SU1F(1,1)) imag(SU1F(1,1)) real(SU1F(2,1))
         imag(SU1F(2,1)) real(SU1F(1,2)) imag(SU1F(1,2)) real(SU1F(2,2))
         imag(SU1F(2,2))];
      %% Two-port S parameters of the DUT for all frequencies range
end
%% ========================================================================
```

Appendix C: Modeling Inductors in ADS Momentum and HFSS

Modeling Inductors in ADS Momentum and HFSS

Accurately modeling a passive device at microwave frequencies requires EM simulators, such as ADS Momentum or HFSS. Compared to ASITIC, modeling inductors in ADS momentum and HFSS is more time consuming with their huge matrices computations. However, they can simulate more complicated structures including inductors with different isolation techniques and give the broadband s-parameters in order to generate compact inductor models. In this section, the flow to build and model an inductor is described step by step.

- **Modeling in ADS Momentum**

Modeling an inductor in ADS momentum involves four steps: defining the properties of required technology, laying out the passive components, defining the ports, and simulation setup.

The first step is to define the physical parameters of a chosen technology. ADS momentum uses a substrate.slm file as shown in Figure C-1 to define the properties of the dielectric layers and metal layers stacked up and uses a layout.lay file as shown in Figure C-2 to define metal layer mapping and colors for the layout. These two files are essential to create an inductor layout for simulation in momentum and they can be obtained either from the manufacturer or extracted from the technology supplemental documents. The distribution of electromagnetic field of the inductor would be calculated and analyzed. From these analysis and calculations, a set of S parameters will be derived.

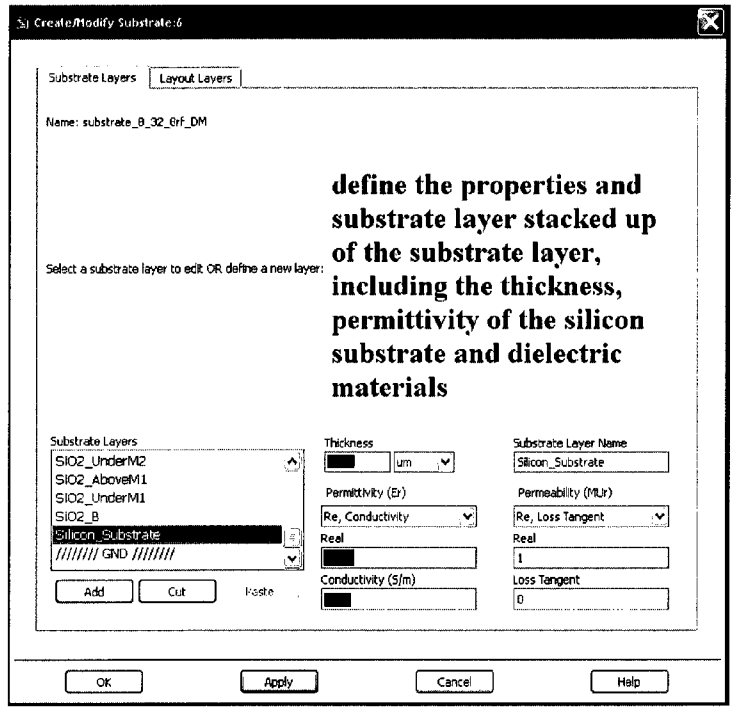


Figure C-1: Example of creating substrate layers stacked up in momentum

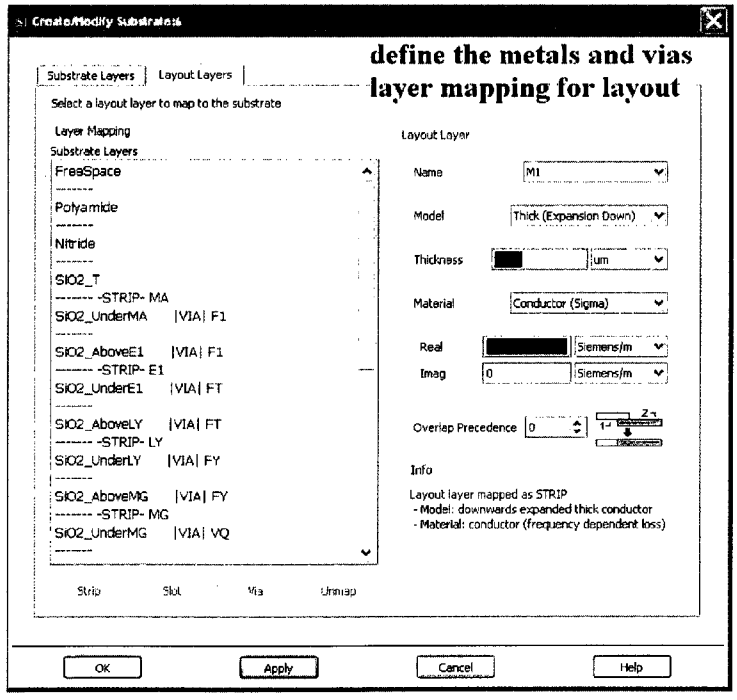
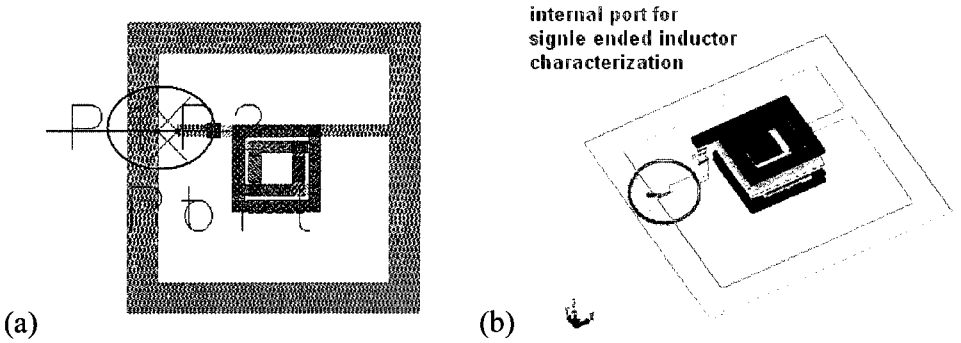


Figure C-2: Example of creating metal layers stacked up in momentum

After defining the properties of the required technology, designers can either import the layout from cadence or manually draw the layout. The ADS layout tool is very similar to cadence virtuoso, but the new version of ADS has a 3-D viewer which can help to visualize the actual structure after layout. Therefore, for complicated passive structures like stacked inductors and some patterned ground shields, designers can do the layout in ADS and then import back to cadence or import to HFSS for 3-D simulation.

The next step is to define the ports for simulation depending on the applications and layout of the inductor. For an inductor with single ended characterization, internal port with a reference ground will be used. The reference ground can be a guard ring or a patterned ground shield connecting to the other end of the inductor, an example of which is shown in Figure C-3. For two ports characterization of an inductor, two internal ports can be used when a guard ring or a pattern ground shield is used as a reference ground, as shown in Figure C-4; otherwise, two single mode ports can be used when the inductor is referenced to the bottom of the substrate, as shown in Figure C-5. For differential mode characterization, the differential mode port can be used, as shown in Figure C-6, where P1 will be the positive side and P2 will be the negative side of the differential port.



(a) (b)

Figure C-3: Single ended inductors structure in ADS (a) 2-D view, (b) 3-D view

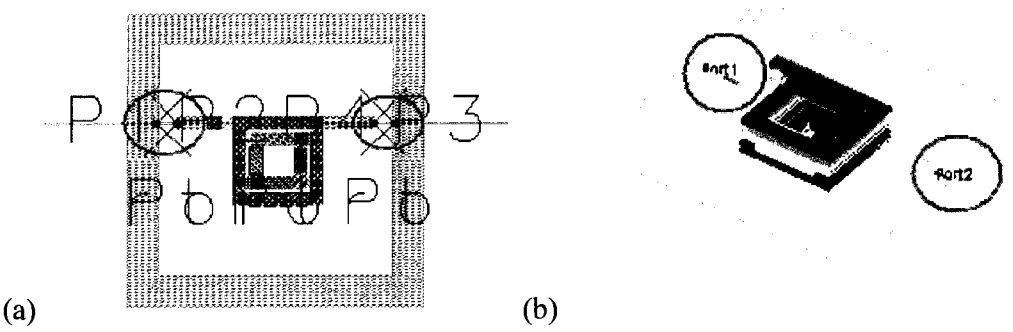


Figure C-4: Two internal ports inductor structure in ADS (a) 2-D view, (b) 3-D view

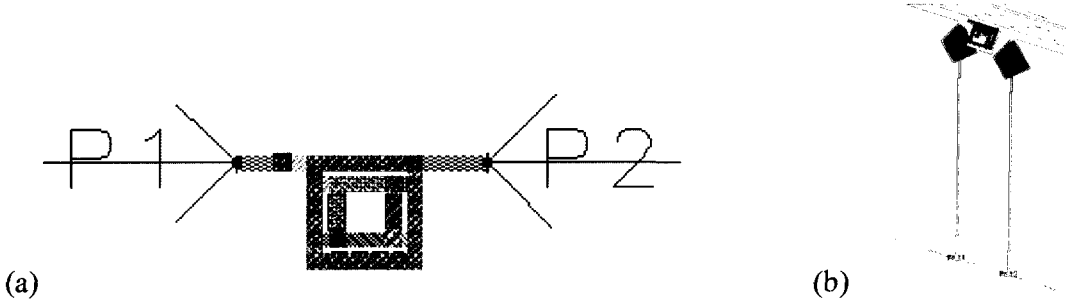


Figure C-5: Two single mode ports inductor structure in ADS (a) 2-D view, (b) 3-D view

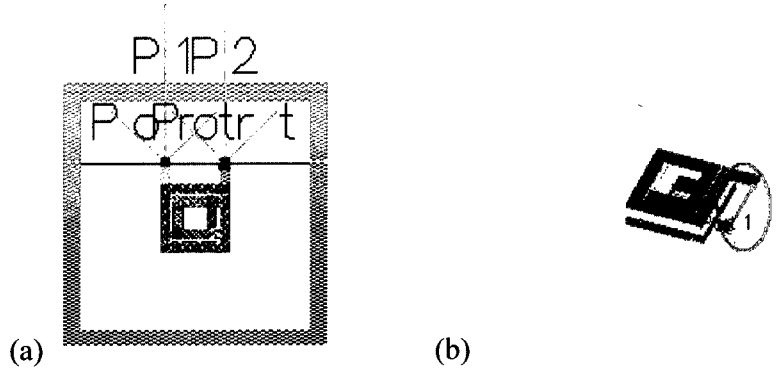


Figure C-6: Differential mode inductor structure in ADS (a) 2-D view, (b) 3-D view

After the port setup, the final step is to choose a method to solve the matrix and define the mesh frequency; then the inductor model can be generated. Depending on the operation frequency of the inductor, the mesh frequency can be chosen in order to reduce the mesh density and simulation time.

- **Modeling in HFSS**

Modeling an inductor in HFSS also involves four steps: defining the properties of materials, making the 3-D structures, defining the ports, and setting up the simulation.

The first step is to define the properties of materials of the chosen technology, including the conductivity of the metal layer, the permittivity and dielectric constant of the oxide layer and substrate layer. Similar to ADS, the properties of the materials can be either extracted from the substrate.slm file from the manufacturer or extracted from the technology supplemental documents. HFSS requires manually assigning the thickness and position of each piece of the layer or generate an automatic file to assign material thickness.

The second step is to construct the 3-D structure. The layout from cadence or ADS can be imported into HFSS as a GDSII file. Figure C-7(a) shows that after importing the GDSII file into HFSS, it will be an unsigned 2-D structure; whereas Figure C-7(b) shows that after assigning the thickness and position of each piece, it will becomes a 3-D structure including the air box for boundary and substrate as shown on the right hand side.

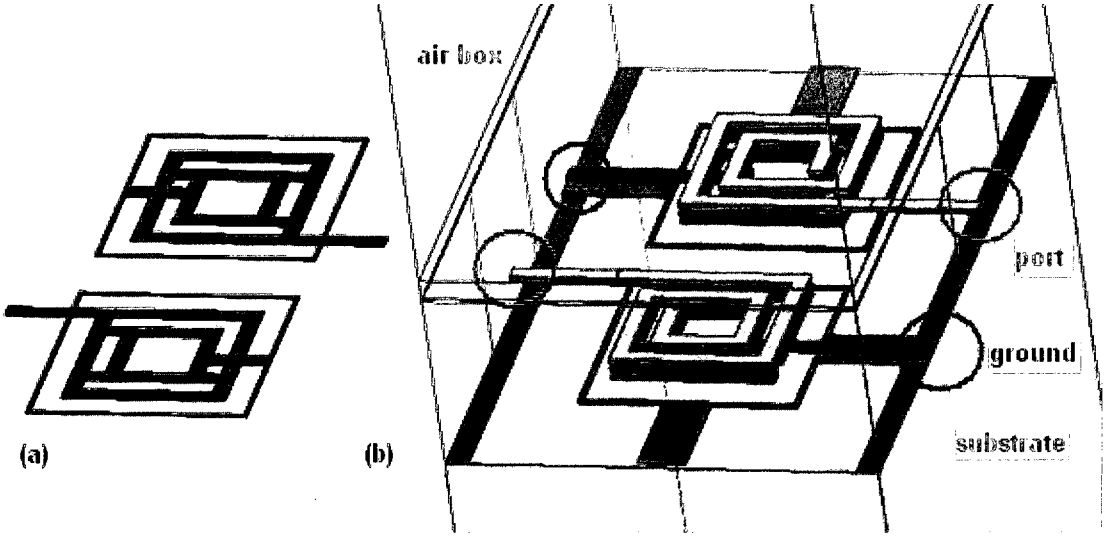


Figure C-7: Single ended inductors structure in HFSS (a) 2-D view, (b) 3-D view

The next step is to define the ports for simulation. These stacked inductors are in single ended configuration and are used to simulate the coupling effect of the inductors. The blue circles in Figure C-7(b) represent the other end of the inductors that are connecting to ground. The two port characterization structure is shown in Figure C-8 where the difference from Figure C-7(b) is that the other end of the inductor also touches a small rectangle, which is defined as the second port of the inductor.

The final step is to configure the solution setup for simulation, including the solution frequency that defines the mesh density, and the sweep type of the simulation that defines the speed of simulation. Other setup steps that help with the convergence of the simulation will be based on the experience of using HFSS. Finally, the stacked inductor 3-D model in HFSS is ready for the simulation to begin.

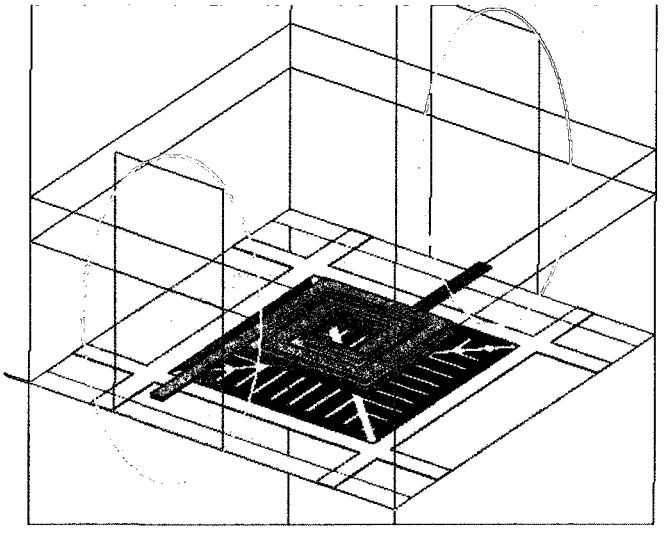


Figure C-8: Two wave-ports inductor characterization structure in HFSS

Appendix D: On-wafer Measurement Preparation

In order to perform on-wafer probing to characterize the inductors, several microwave measuring equipment is required, including a Vector Network Analyzer (VNA), microwave measuring probes, on-wafer calibration kits, and a probe station.

- **Vector Network Analyzer**

A VNA is an instrument used to analyze the scattering parameters (S-parameters) of electrical networks base on the reflection methods [9]. It measures both amplitude and phase properties, so it also call a gain-phase meter. As shown in Figure 6-1, using a switch, the VNA applied a RF reference signal to either port 1 or port 2 of the DUT. Hence, it allows both forward and reverse measurements on the DUT, which are needed to characterize all four S-parameters. Often internal attenuators are available, such that the measuring accuracy and reliability can be improved for a large range of device characteristics [9]. The VNA that used for this measurement is Agilent E8361A, which has operating frequency range from 10 MHz to 67 GHz.

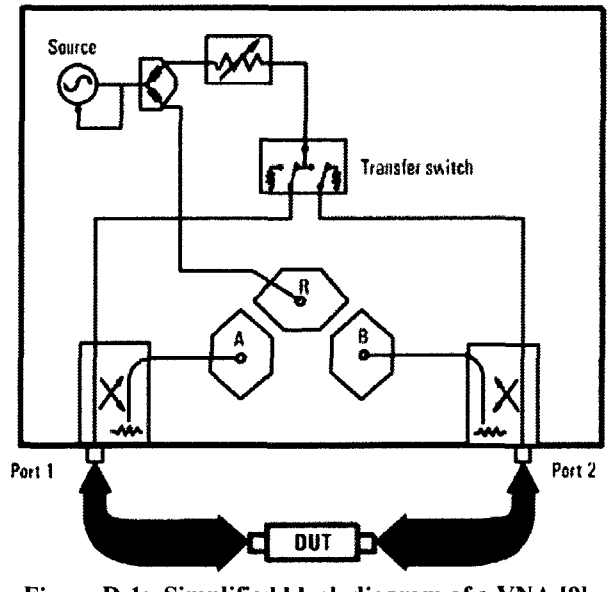


Figure D-1: Simplified block diagram of a VNA [9]

- **Probes**

The probes can be viewed as an adapter to launch a RF signal from the coaxial cable to the contact pads placed on the chip. In order to transmit the signal, at least two conductors, the "signal" conductor and the "ground" conductor are required. Three types of probes are shown in Figure 6-2, which are ground-signal-ground (GSG), ground-signal (GS), and signal ground (SG).

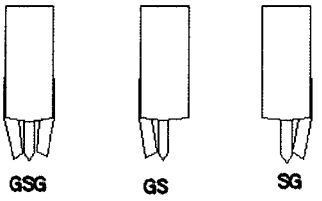


Figure D-2: Three types of RF probes, GSG, GS, and SG

GSG is the most common type of RF probe, which is similar to a coplanar waveguide. A GSG probe provides a balanced configuration as shown in Figure 6-3(a), which consists of two ground tips that shield the signal tip. This structure can tightly control the fields around the signal tip so that the electric fields from the signal (S) will stop at the ground (G) tips and the magnetic fields between S and G will cancel [9]. On the other hand, the GS or SG probes provides an unbalanced configuration as shown in Figure 6-3(b), which can reduces the die area by eliminating one ground tip; however, this results in less shielding of the signal tip, and this can result in crosstalk problems. Therefore, if area is not a constrain, GSG probe should be used for more accurate measurements [9].

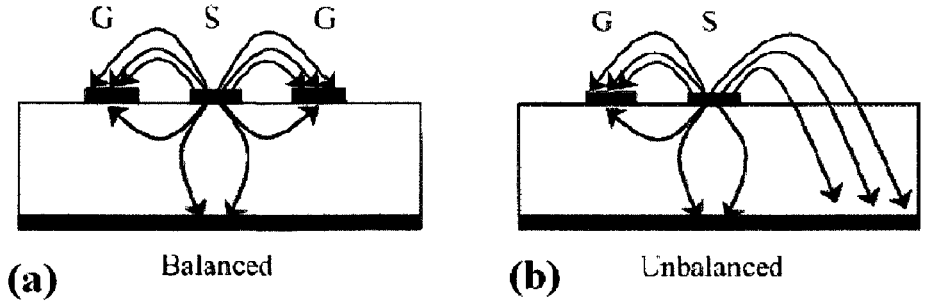


Figure D-3: (a) balanced and (b) unbalanced electric field pattern of RF probe [14]

In addition, in order to perform accurate measurements, the probe needs to be planar. Figure 6-4 shows planar and non-planar tips referred to a calibration reference plane: the dotted line. Poor planarization of the probe may present large measurement errors. For example, if two 100Ω resistors are placed in parallel, the equivalent resistance should be 50Ω. However, if one of the ground tips does not touch the pad as shown in Figure 6-4, the measured load will only be one 100Ω resistor [9]. Thus, the planarity of the probes always needs to be checked before any on-wafer measurements are performed. The planarity of the probe can be checked by watching the scratches left on the substrate metalized contact field as shown in Figure 6-5. Proper scratch depth and width can indicate whether the probe tips are on the same plane or not [9].

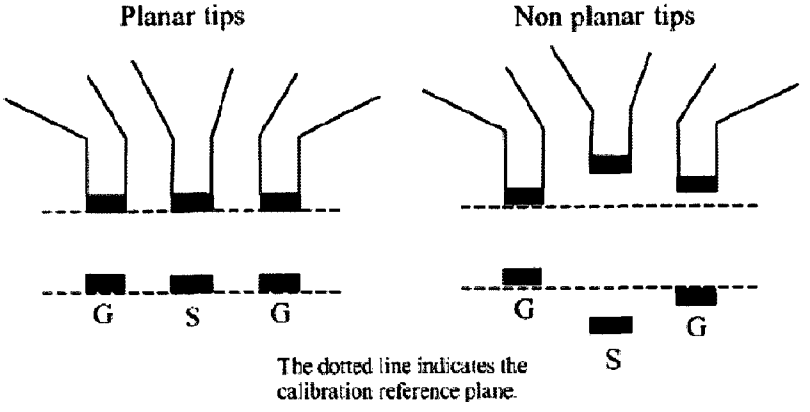


Figure D-4: Planarization of probes [9]

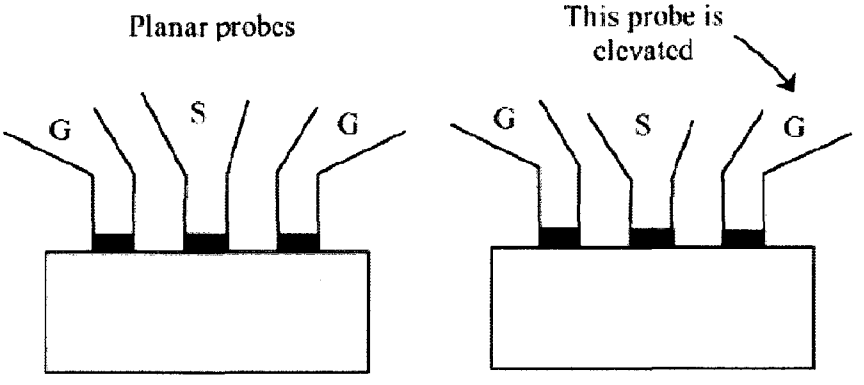


Figure D-5: Checking of the probe tip planarity [9]

- **On-wafer Calibration Kits**

In order to calibrate the VNA up to the probe tips, an on-water calibration kits is required, which is known as the Impedance Standard Substrate (ISS). They are available for different configurations depending on the type of probes and calibration methods. The ISSs are usually made from low loss alumina substrate with high dielectric constant and they use gold for metal contacts to provide low resistance and oxidation [9]. Figure 6-6 shows an ISS from Cascade Microtech [30], which is available for 100-250μm pitch GSG probes with a SOLT (Short-Open-Load-Thru) calibration standard. The SOLT calibration standard shown in Figure 6-7 contains: trimmed 50Ω load resistors (two 100Ω resistors in parallel), shorts and thru lines. The open is usually implemented by lifting the probes high into the air [30].

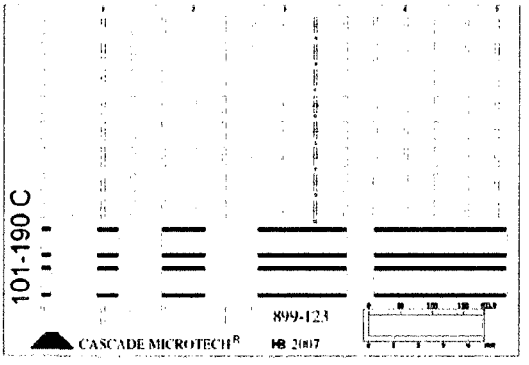


Figure D-6: An impedance standard substrate for GSG configuration [30]

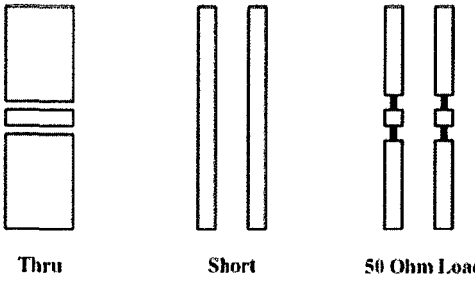


Figure D-7: Thru, short, and 50 Ω load structures on the ISS [30]

- **Probe Station**

A suitable probe station is also important for on-wafer measurement. An automatic probe stations can provide the highest degree of probing repeatability and reliability of the calibration.

However, it is expensive and usually used by IC manufacturers only. As a result, manual probe stations, as shown in Figure 6-8, are the most widely used in research labs and small companies [9].

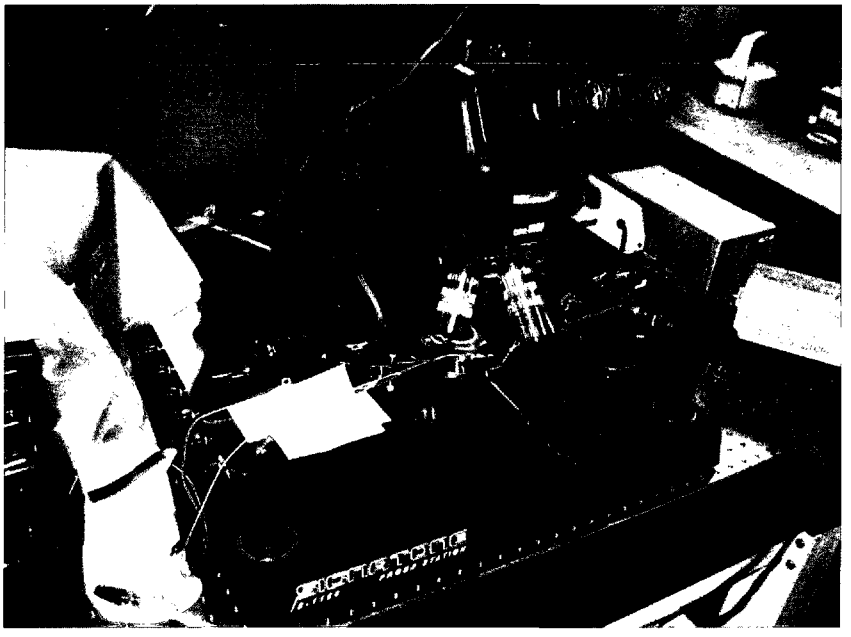


Figure D-8: An example of a manual probe station

The general technique of using a probe station may include the following [9]: stably mounts the device under test, accurately locate the probe in the x, y and z axes, adjust the planarity of the probes, using a microscope to view the very small measuring environment. For more advanced measuring requirements, a probe station can also provide shielding of the measuring environment by using a microchamber, thermal control of the measuring environment, and it can maintain the stability and avoid undesired vibrations by using a anti-vibration table.

SOLT Calibration

After selecting the appropriate test equipments for on-wafer measurement as shown in previous section, the next step is to perform an on-wafer calibration using the probes and the ISS before doing actual measurements, in order to obtain accurate results.The SOLT calibration

procedures involve going through a series of standard steps such as: measuring the short standard, measuring the open standard, measuring the load standard, and measuring the thru standard. The isolation measurement is usually omitted [9].

- **Measuring the Short Standard**

Figure 6-9 shows a Cascade ISS short standard, which is implemented as a 50μm Au metallization line. As mention in section 6.1.2, it is very important that the probes have been planarized properly and the overtravel has been accurately adjusted using the alignment marks; otherwise, the parasitic capacitance of the standard may change, and that will have an impact on the measuring accuracy [9].

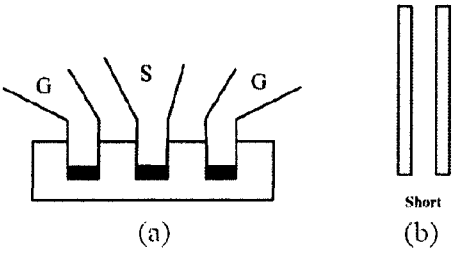


Figure D-9: ISS short standard [9]

- **Measuring the Open Standard**

Usually, an open standard is synthesized by raising the probes into the air a minimum distance of 250μm above the ISS surface. Figure 6-10 shows a Cascade ISS open standard as an alternative.

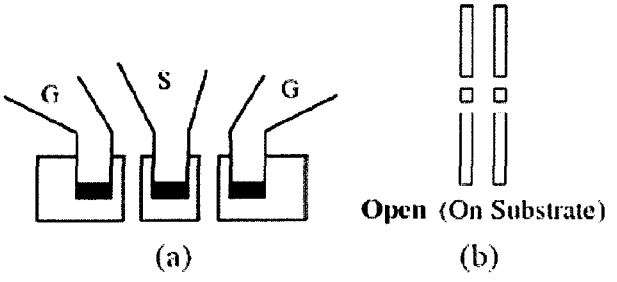


Figure D-10: ISS open standard [9]

- **Measuring the Load Standard**

Figure 6-11 shows a Cascade ISS load standard, which is implemented with two high-precision 100Ω resistors in parallel. The resistors are laser trimmed such that they have a very constant resistance versus frequency. As discussed for the short standard, planarity and overtravel are critical issues for the load standard [9].

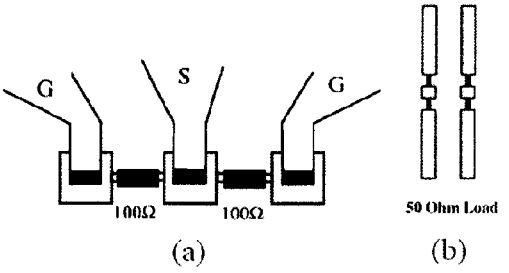


Figure D-11: ISS load standard [9]

- **Measuring the Thru Standard**

Figure 6-12 shows a Cascade ISS thru standard. The probe alignment is more sensitive than the other standards (short, open and load), which should be very accurate including the distance between the probes.

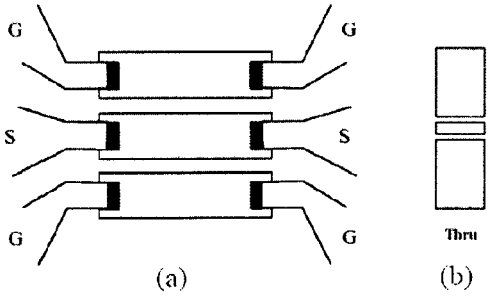


Figure D-12: ISS thru standard [9]

Appendix E: Layout of the test chip

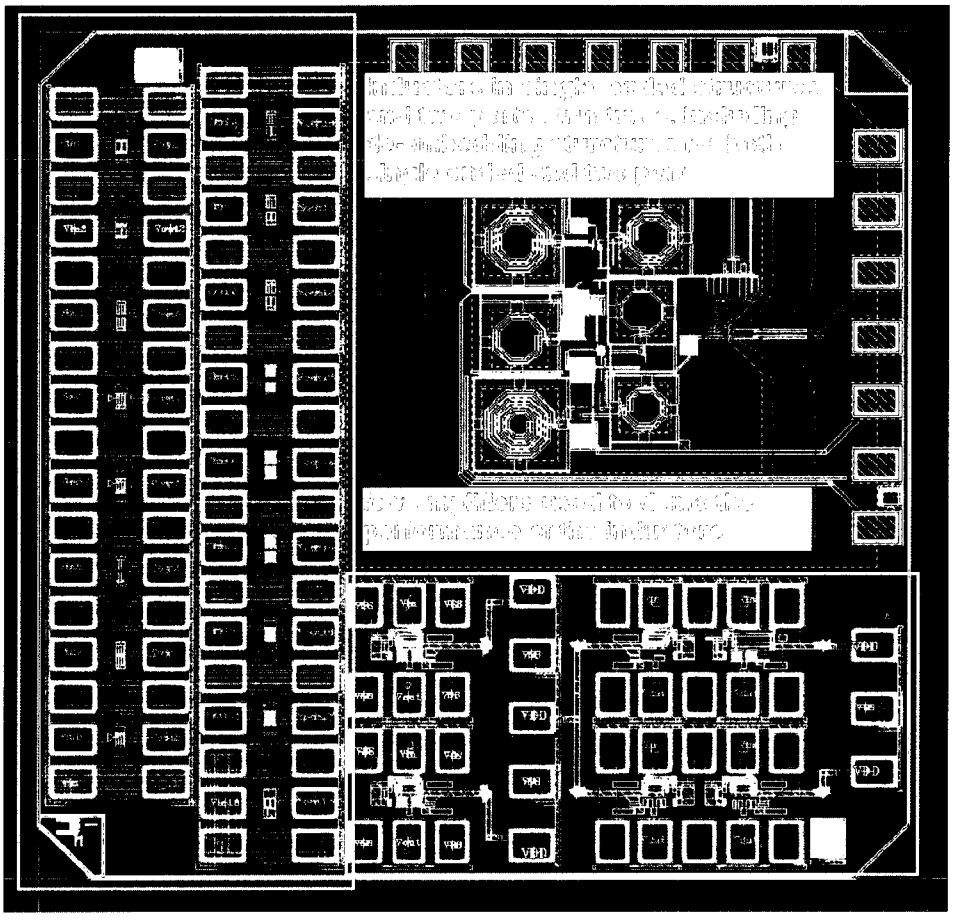


Figure E-1: Layout of the chip for this thesis

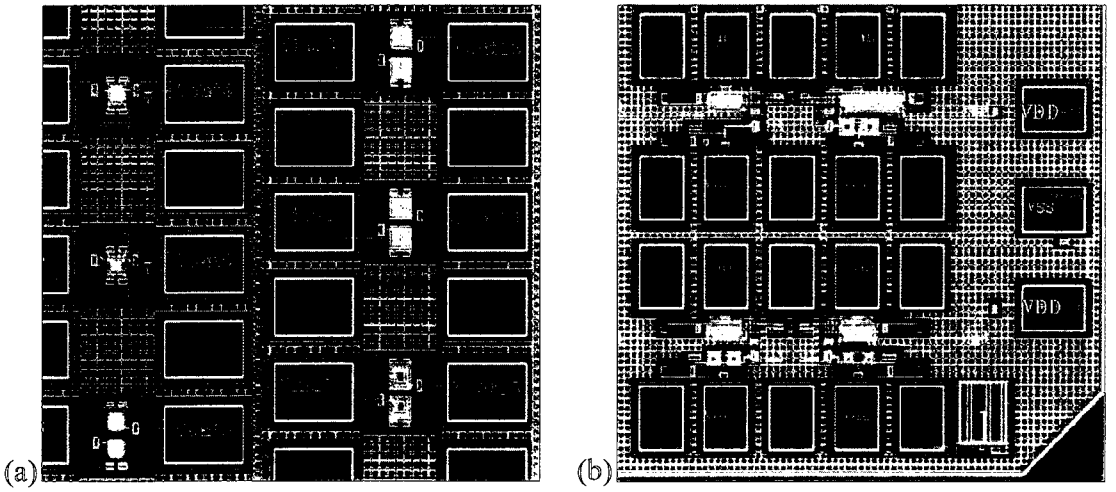


Figure E-2: Zoom in view of the layout, (a) stacked inductors and (b) amplifiers

Appendix F: Material Temperature Coefficients

Table 7: Material Temperature Coefficients [35]

Material	Resistivity (Ω·m) at 20 °C	Temperature coefficient [K^{-1}]
Silver	1.59×10^{-8}	0.003819
Copper	1.72×10^{-8}	0.004041
Gold	2.44×10^{-8}	0.003715
Aluminum	2.82×10^{-8}	0.004308
Calcium	$3.36\text{x}10^{-8}$	?
Tungsten	5.60×10^{-8}	0.004403
Zinc	5.90×10^{-8}	0.003847
Nickel	6.99×10^{-8}	0.005866
Iron	1.0×10^{-7}	0.005671
Tin	1.09×10^{-7}	0.0045
Platinum	1.06×10^{-7}	0.003729
Lead	2.2×10^{-7}	0.0039
Manganin	4.82×10^{-7}	0.000002
Constantan	4.9×10^{-7}	0.000 008
Mercury	9.8×10^{-7}	0.0009
Nichrome	1.10×10^{-6}	0.00017
Carbon	3.5×10^{-5}	−0.0005
Germanium	4.6×10^{-1}	−0.048
Silicon	6.40×10^{2}	−0.075
Glass	10^{10} to 10^{14}	?
Hard rubber	approx. 10^{13}	?
Sulfur	10^{15}	?
Paraffin	10^{17}	?
Quartz (fused)	7.5×10^{17}	?
PET	10^{20}	?
Teflon	10^{22} to 10^{24}	?