A 2.4GHz Fully Differential RF Sampling Front End in 0.18 μm CMOS Process

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The information used in this thesis comes in part from the research program of Dr. Tad Kwasniewski and his associates in the VLSI in Communications group. The research results appearing in this thesis represent an integral part of the ongoing research program. All research results in this thesis including tables, graphs and figures but excluding the narrative portions of the thesis are effectively incorporated into the research program and can be used by Dr. Kwasniewski and his associates for educational and research purpose, including publication in open literature with appropriate credits. The matters intellectural property may be pursued cooperatively with Carleton University and Dr. Kwasniewski and where and when appropriate.

Abstract

Analog front end is the most critical part of the whole wireless receiver. Sensitivity and selectivity are the primary concerns in receiver design. Wireless communication standards have become more complicated due to the lack of globally harmonized spectrum allocation. This has motivated researchers to look for multi-band multi-standard solution for wireless front end. More efficient technologies need to be employed to meet this goal.

In this thesis a novel front-end circuit based on direct RF sampling method was analyzed and modelled. This front end not only significantly reduces noise-folding effect compared with sub-sampling technique, but also achieves great selectivity right at the mixer level to partially select the channel. The selectivity is digitally controlled by the LO clock frequency, decimation ratio and capacitance ratio. Simulation results show that multi-tap direct-sampling (MTDSM) can provide 30dB attenuation for adjacent channel.

The design of a 2.4GHz fully differential RF sampling front end is presented. This front end consists of a low-noise amplifier (LNA), a transconductance amplifier (TA), a multi-tap direct-sampling (MTDSM) and a digital-controlled unit (DCU). All the blocks are fully differential. The circuits are fabricated in 0.18um CMOS process.

The measurement results showed that LNA and DCU work properly but MTDSM part failed due to long trace between the DCU and MTDSM which means sampling switches could not be turned on or off completely. This failure could be fixed by careful layout.

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Table of Contents

List of Tables

List of Figures

List of Abbreviations

WLAN	Wireless Local Area Network
UWB	Ultra Wideband
CDMA	Code Division Multiple Access
WCDMA	Wideband Code Division Multiple Access
GSM	Global System of Mobile Communications
GPRS	General Package Radio Service
UCLA	University of California at Los Angels
TI	Texas Instrument
SDR	Software-Defined Radio
ADC	Analog-to-Digital Converter
SDRX	Software-Defined Receiver
LO	Local Oscillator
DSP	Digital Signal Processing
LNA	Low Noise Amplifier
TA	Transconductance Amplifier
DCU	Digital-Controlled Unit
CMC	Canadian Microelectronics Corporation
RF	Radio Frequency
IF	Intermediate Frequency
SAW	Surface Acoustic Waveform
IR	Image Rejection

PLL	Phase-Locked Loop
SNR	Signal-to-Noise Ratio
FSK	Frequency Shift Keying
IP3	Third Intercept Point
IP2	Second Intercept Point
FCC	Federal Communications Commissions
CT	Continuous Time
WIS	Windowed Integration Sampler
MTDSM	Multi-Tap Direct-Sampling Mixer
PSD	Power Spectrum Density
NF	Noise Figure
LNTA	Low-noise Transconductance Amplifier
CMOS	Complementary Metal Oxide Semiconductor
MOS	Metal Oxide Semiconductor
MOSFET	MOS Field Effect Transistor
NMOS	N-channel MOSFET
PMOS	P-channel MOSFET
CG	Common Gate
CS	Common Source
CML	Current Mode Logical
DFF	D Flip-flop
CFP	Ceramic Float Package

PCB	Printed Circuit Board
MUX	Multiplexer
NFA	Noise Figure Analyzer
I/O	Input/Output

CHAPTER 1

Introduction

1.1 Thesis motivation

The wireless industry has enjoyed explosive growth over the past two decades. Various radio access technologies have been developed and implemented to provide wireless connectivity service for years. Cellular phone technology (GSM, GPRS, WCDMA, etc.) offers long-range voice, data and even video transfer. Wireless local area network (WLAN: 802.11a/b/g) provides home and office radio connectivity. Bluetooth and ultra wideband (UWB) are used for short-range connectivity. Wireless communication standards become complicated due to the lack of globally harmonized spectrum allocation. For example, there are four carrier frequencies (850, 900, 1800 and 1900MHz) for GSM (Global System for Mobile Communications) all over the world. Therefore many wireless communication standards are implemented by adopting different carrier frequencies, channel bandwidths and modulation schemes. This has motivated the industry to look for multi-band multi-standard devices to enable anywhere anytime connectivity[1].

Most people believe that the ultimate solution is software-defined radio (SDR) which uses a single radio to cover many communication channels[2]. However, to cover all major standards from 800MHz to 5GHz, a 12-bit and 10GHz sample rate analog-to-

digital converter (ADC) is needed for an ideal software-defined receiver (SDRX). This ADC is estimated to consume 500W power, therefore this approach still remains impractical in the near future [1]. Recently, important technology breakthroughs in SDRX, such as the software-defined radio multi-band receiver of University of California at Los Angeles (UCLA) [1], and the fully integrated quad-band GSM/GPRS receiver of Texas Instruments (TI) [3], solve this problem in a similar way[13].

The TI solution uses direct RF sampling mixer to sample the RF input signal as it is down-converted, down-sampled, filtered and converted from analog to digital with a discrete-time sigma-delta ADC. In addition, it achieves great selectivity right at the mixer level. Furthermore, the selectivity is digitally controlled by the local oscillator (LO) clock frequency and capacitance ratio, both of which can be precisely controlled in deep submicron CMOS process[4]. This greatly relaxes the stringent dynamic range requirements for the ADC. Moreover, the direct RF sampling mixer pushes analog-to-digital conversion close to the antenna, enabling low-cost and low-power design that exploits sophisticated digital-signal-processing (DSP) algorithms. This avoids analog signal processing influenced by small voltage headroom of the deep-submicron CMOS technologies [5]. The aim of this thesis is to investigate and implement methods for a direct RF sampling front end.

1.2 Thesis contributions

The contributions of this research are outlined as follows:

1. A novel front end circuit based on direct RF sampling method was analyzed and modelled. This front end not only significantly reduces noise-folding effect compared with sub-sampling technique, but also achieves great selectivity right at mixer level to partially select channel.

2. A 2.4GHz direct RF sampling front end was implemented. The circuit includes low noise amplifier (LNA), RF transconductance amplifier (TA), direct RF sampling mixer including charge domain switched capacitor filter and digital-controlled unit (DCU). All building blocks were implemented in differential to reduce common mode noise and sensitivity to package due to parasitic capacitance and inductance.

3. This front end circuit was fabricated in 0.18 μm CMOS technology. Simulation and measurement results confirmed the reported circuit performance and suitability for mobile radio applications.

1.3 Thesis organization

The thesis is organized as follows.

Chapter 1 is the introduction of the thesis including the motivation, contributions and organization of the thesis.

Chapter 2 overviews architectures of wireless transceiver including super heterodyne, low IF and direct conversion.

Chapter 3 explains the fundamentals of design consideration for direct RF sampling front end including brief review of windowed integration sampler, discrete-time transfer function and noise figure consideration.

Chapter 4 presents the implementation of direct RF sampling front end circuit based on 0.18 μm CMOS technology provided by the Canadian Microelectronics Coorporation (CMC). It consists of building blocks including low noise amplifier (LNA), RF transconductance amplifier (TA), direct RF sampling mixer including charge domain switched-capacitor filter and digital-controlled unit (DCU). All the circuits are verified by Spectre/SpectreRF based upon both schematic and post-layout simulation.

Chapter 5 describes the set up of chip test environment and discusses the measurement results.

Chapter 6 draws conclusion of overall research work and provides some suggestion for future work.

CHAPTER 2

Overview of Wireless Receiver Architectures

2.1 Introduction

The recent surge in application of radio-frequency (RF) transceivers has been accompanied with aggressive design goals: low cost, low power dissipation, and small form factor and high-speed data transfer [6]. These goals are driven by both the need for better portability and affordability, and the ever-increasing demand for higher-speed data communications [7]. Most of wireless transceivers used so far are based on the traditional super heterodyne architecture. These transceivers have good performance, but suffer from high production costs and require a relatively large form factor due to expensive surface acoustic waveform (SAW) filters which can not be integrated in silicon. In this section the conventional heterodyne architecture topology is briefly reviewed along with direct conversion and low IF (intermediate frequency) architecture. There exists a corresponding transmitter architecture for each particular receiver architecture, but the transmitter is beyond the scope of this thesis, therefore the following review focuses on receiver structure.

2.2 Conventional Heterodyne Receivers

Most commercial RF transceivers use conventional heterodyne architecture. A general structure of heterodyne receiver is shown in Figure 2.1 [7].

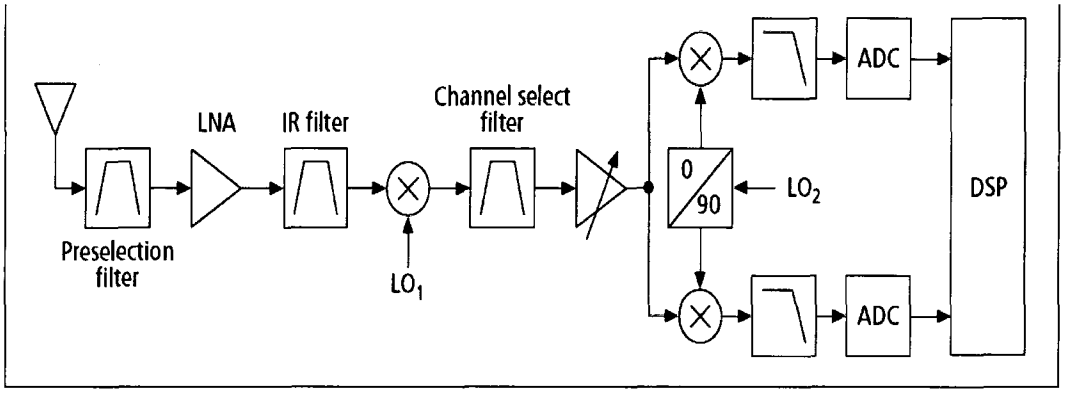


Figure 2.1 :Heterodyne Receiver Architecture[7]

The preselection filter is used to filter out the out-of-band signal and partially reject image band signals. After this filtering, the received RF signal is applied to a low noise amplifier (LNA) which provides sufficient power gain and adds little noise. The image rejection (IR) filter following the LNA further attenuates the signals at the image band. The desired signal at the output of the IR filter is mixed with the output of local oscillator (LO) and downconverted from RF frequency to a fixed intermediate frequency (IF). Since intermediate frequency is fixed, the output frequency of local oscillator changes with the input RF frequency. The local oscillator can be implemented based on phase-locked loop (PLL).

The channel select filter serves to suppress out-of-channel signals and interferers. This IF filter performs desired channel selection and reduces the distortion and dynamic range requirement of the subsequent receiver blocks [19]. The following stage is typically

a programmable-gain IF. The signal can be translated to baseband and demodulated as shown in Figure 2.1, or alternatively further down-converted to lower IF, and then shifted to baseband and demodulated [7].

The principal issue in heterodyne receiver is the tradeoff between image rejection and channel selection. As illustrated in Figure 2.2, the desired band and image band are separated by twice the IF, it is desirable to choose a high IF to reduce the requirement of quality factor (Q) on the IR filter. Furthermore, if the intermediate frequency is set to be high enough that the image can be greatly suppressed by the preselection RF filter, it might be possible to directly connect the output of the LNA to the mixer without including an IR filter [20]. In this case the image can be greatly attenuated whereas interferers nearby IF remain at significant levels, it means that high-Q channel filter is required to remove interferers. On the other hand, if a low IF is chosen, the image corrupts the down-converted signal but channel selection can be done in low IF, this allows employment of high quality channel select filter. Therefore, the choice of intermediate frequency largely depends on the trade-off between image rejection and channel selection. Other factors influencing the choice of IF are availability and the physical size of commercial filters for different frequencies.

From the above analysis on the choice of IF, we know that both the image-rejection filter for low IF receiver and the channel filter for high IF receiver require highly selective transfer functions that are impractical in today's IC technologies [6]. Conventionally, all the filters used in the heterodyne receivers are high-Q discrete component filters, such as surface acoustic wave (SAW) or ceramic filters [7]. Compared to other more integrable receiver architecture like Zero IF or low IF, the heterodyne receiver has supe-

rior performance with respect to selectivity, a measure of a receiver's ability to separate the desired band around the carrier frequency from signals received at other frequencies, and sensitivity, the minimal signal at the receiver input for which there is sufficient signal-to-noise ratio (SNR) at the receiver output [7]. This is achieved with the use of high-Q discrete components [19].

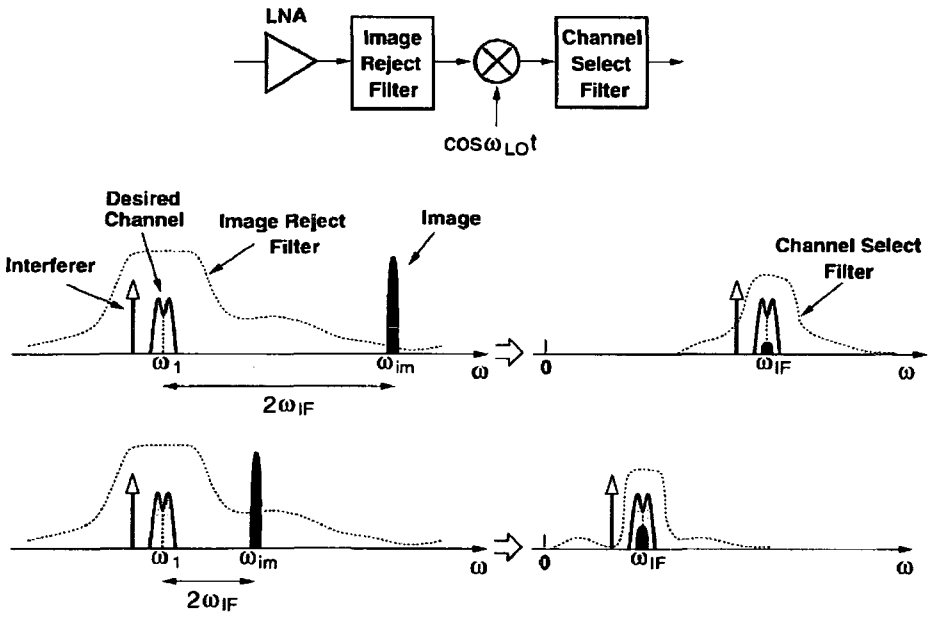


Figure 2.2 :Relationship between IF and bandpass filter[6]

There are some drawbacks to use discrete high-Q components. A major limitation is the low input impedance of off-chip RF filters. This requires a high drive capability for the preceding LNA, inevitably leading to more severe trade-off between gain, noise figure, stability, and power dissipation in the amplifier [20]. Furthermore, it is very difficult and somewhat impractical to design high-Q filters on silicon since integrated inductors

only have moderate Q-factors. In addition, the narrowband discrete-component IF channel-select filter of the heterodyne receiver tailors the particular implementation to a specific standard [19].

2.3 Direct Conversion Architecture

Direct conversion, also known as zero-IF conversion or homodyne, is a natural approach to translate input signal from RF band directly to baseband. Actually direct Conversion architecture was invented many decades ago and has been tried for many times, but never succeeded in the past. In recent years, this architecture becomes more attractive than other ones since this structure has single conversion and high level integration. This architecture is shown in Figure 2.3.

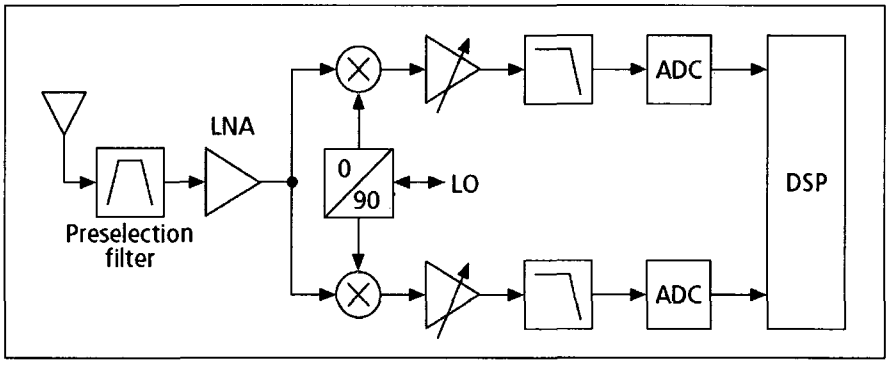


Figure 2.3 :Homodyne Receiver Architecture[7]

The direct conversion receiver downconverts RF band signal of interest directly to baseband and low-pass filtering is employed in the baseband to suppress nearby interferers and select the desired channel. The quadrature downconversion (I and Q channels) is necessary in typical amplitude, phase and frequency vector modulated signals since the

two side-bands of the RF spectrum generally contain different information. Mixing with a real sinusoid would result in irreversible corruption of transmitted information [6]. Note that quadrature downconversion is equivalent to complex mixing.

The homodyne architecture has several fundamental advantages over the heterodyne structure. There is no need for image rejection filter since the intermediary IF stages are removed. Furthermore, the LNA requirement to drive a low impedance is eliminated because of the absence of the bulky off-chip image rejection filters. The functions of channel selection and subsequent amplification are replaced with low pass filtering and baseband amplification which are amenable to monolithic integration.

Despite this suitability for higher levels of integration, a homodyne receiver exhibits a number of issues that either do not exist or not as serious in a heterodyne receiver. We will briefly review some of these issues in the following.

2.3.1 DC offsets

Perhaps the most serious problem is that of DC offsets in the baseband section of the homodyne receiver [21]. The desired signal can be corrupted by these extraneous offset voltages, and more importantly, these offset voltages can saturate the following stages. DC offsets are due to the self-mixing of the local oscillator or the in-band interferer, aside from the usual element mismatch in the signal path.

To better understand the origin and impact of these offsets, consider the received signal path shown in Figure 2.4. Since the isolation between the LO port and the inputs of the mixer and the LNA is not perfect, there must have a finite amount of feedthrough existing from the LO port to the inputs of the LNA and the mixer. This phenomena is

known as LO leakage which arises from capacitive and substrate coupling or through bond-wire coupling if the LO signal is provided externally. The leakage signal appearing at the inputs of the LNA and the mixer is now mixed with the original LO signal and produces a DC component at the output of the mixer. This LO self-mixing can be quite severe, and a time-varying dc-offset occurs when the LO signal leaks out through the antenna, and is radiated and reflected from nearby objects back to the receiver. A similar effect occurs if a large in-band interferer (in the passband of the RF preselection filter) leaks from the LNA output to the mixer LO port and gets multiplied by itself [20]. It should be mentioned here that these dc-offsets also exist in heterodyne receivers, but are mostly eliminated by the IF band-pass filters.

From the above discussion, we know that direct conversion receivers require appropriate methods to remove undesired DC offsets. A simple solution is to use ac-coupling to remove offset in the downconverted signal path. However, since the spectra of all spectrally efficient modulation schemes currently used exhibit significant energy at DC, the signal is corrupted by ac-coupling filters [21]. A better method is to use baseband analog and digital signal processing (DSP) techniques for offset estimation and cancellation [19]. This method can be used in SOC (System-on-chip) solution. However, these techniques add complexity and do not solve the problems associated with flicker noise at low frequencies in CMOS implementations, a significant issue [7]. A possible system solution for the DC offset problem in direct-conversion receivers is to minimize the baseband signal energy near DC by choosing a "DC-free" modulation scheme and use ac-coupling for offset elimination. This approach has been successfully used in pager systems with frequency shift keying (FSK) modulation, despite the spectral inefficiency of FSK [21].

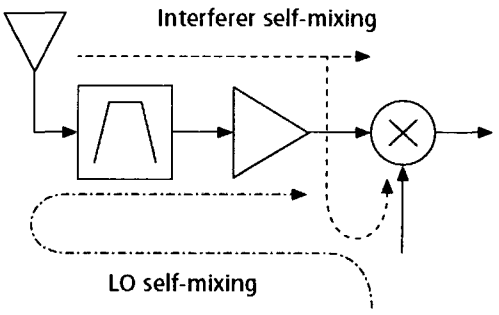


Figure 2.4 :Self-mixing of the LO and interferer in homodyne receiver[7]

2.3.2 I/Q Mismatch

As we know, a homodyne receiver must incorporate quadrature downconversion for most phase and frequency modulation schemes. This requires shifting either the RF signal or the LO output by 90°. Since phase-shifting the RF signal generally entails severe noise-power-gain tradeoff and is especially difficult for the wideband signals used in high-data-rate systems, it is often desirable to shift the LO output. In either case, the errors in the nominal 90° phase shift and mismatches between the amplitudes of the I and Q signal paths corrupt the downconverted signal constellation, therefore increasing the bit error rate [6]. It should be mentioned here that all sections of the circuit in the I and Q signal paths contribute to gain and phase mismatch.

In order to better understand the effect of I/Q mismatch and show convenience of using complex formulation, consider the practical case where the quadrature LO generates the complex signal $x_{LO}(t) = \cos(\omega_{LO}t) - j(1+\varepsilon)\sin(\omega_{LO}t + \theta)$. Here, ε and θ represent LO gain and phase errors [7]. We can rewrite the quadrature LO output as

$$x_{LO}(t) = \frac{1}{2}[1-(1+\varepsilon)e^{j\theta}]e^{j\omega_{LO}t} + \frac{1}{2}[1+(1+\varepsilon)e^{-j\theta}]e^{-j\omega_{LO}t}$$

If we assume there is no LO gain and phase error, the ideal complex LO output should contain only the negative frequency. This can be proven by the following equation:

$$x_{LO}(t) = \cos(\omega_{LO}t) - j(1+\varepsilon)\sin(\omega_{LO}t+\theta) = \cos\omega_{LO}t - j\sin\omega_{LO}t = e^{-j\omega_{LO}t}$$

However, due to gain and phase errors, there is a positive frequency component with a magnitude of $\left|\frac{1}{2}(1-(1+\varepsilon)e^{j\theta})\right|$ based on the above expression. This component causes interfering images and degrades receiver performance. We can separately consider the effects of gain mismatch and phase error. From the above equation, we can obtain that the magnitude of the undesired positive frequency component from gain mismatch is $|\varepsilon|/2$, and for phase mismatch $|\sin(\theta/2)|$, which can be approximated by $|\theta|/2$ when phase error is small. The I/Q mismatch has been a major issue in discrete designs, fortunately it tends to decrease with higher levels of integration in silicon.

2.3.3 Even-Order Distortion

Normally RF receivers are susceptible only to odd-order intermodulation effects. However, even-order distortion also become design issue in direct conversion. As illustrated in Figure 2.5, two strong interferers close to the channel of interest experience a nonlinearity such as $y(t) = \alpha_1 x(t) + \alpha_2 x^2(t)$ in the LNA. If $x(t) = A_1\cos\omega_1 t + A_2\cos\omega_2 t$, then $y(t)$ contains a term: $\alpha_2 A_1 A_2\cos(\omega_1-\omega_2)t$, indi-

cating that two high-frequency interferers generate a low-frequency beat in the presence of even-order distortion. If the mixer is ideal one, this low frequency component will be translated to high frequencies and hence becomes unimportant.

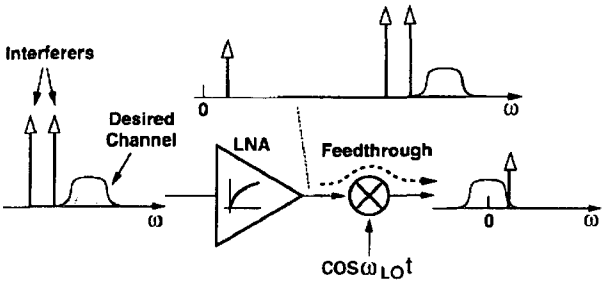


Figure 2.5 :Effect of even-order distortion on interferers[6]

However, mixers exhibit a finite direct feedthrough from the mixer RF input to the mixer IF output due to mismatch in reality. In our illustration here, we have assumed that only the LNA exhibits even-order distortion. In practice, the mixer RF port may also suffer from the same effect, requiring special attention in the design because the signals applied to the mixer are already amplified by the LNA and can create significant distortion [6].

"Second order intercept point" IP2 is used to characterize second-order nonlinearity, IP_2 is defined in the similar way to define the third intercept point (IP_3), two equal-amplitude interferers are applied to the input and their low-frequency beat signal is measured at the output. Plotting the beat signal power versus the input signal power and extrapolating the results yield the IP_2

2.3.4 Flicker Noise

Since a typical gain of LNA together with mixer is roughly 30dB, the amplitude of mixer output signal usually falls in the range of tens of microVolts. The contributed noise from the following stage, e.g., amplifiers and filters, is therefore still critical. In addition, since the downconverted signal is located around DC, the flicker noise of devices has a significant effect on the signal, a severe problem in MOS implementations.

Several techniques can be used to reduce the effect of flick noise. As the stages following the mixer operate at relatively low frequencies, very large devices (several thousand microns wide) can be used to minimize the magnitude of the flicker noise. Moreover, periodic offset cancellation also suppresses low-frequency noise components through correlated double sampling [6]. The effect of flicker noise can also be reduced by increasing the power gain of LNA and mixer.

2.3.5 LO leakage

In addition to introducing dc offsets, leakage of the LO signal to the antenna and radiation from there creates in-band interference for other receivers using the same standard [21]. Each wireless standard and the regulations of the Federal Communications Commission (FCC) impose upper bounds on the amount of in-band LO radiation, typically between -50 and -80 dBm. The issue is less severe in heterodyne and image-reject mixers because their LO frequency usually falls out of the reception band.

The problem of LO leakage becomes less serious as more sections of RF transceivers are fabricated on the same chip. With differential local oscillators, the net coupling to the antenna can approach acceptably low levels [6].

2.4 Low-IF Receiver Architecture

The idea behind the development of the low-IF topologies is to combine the advantages of both heterodyne and homodyne receivers. Among the different low-IF topologies mentioned in [8], a preferred version is shown in Figure 2.6.

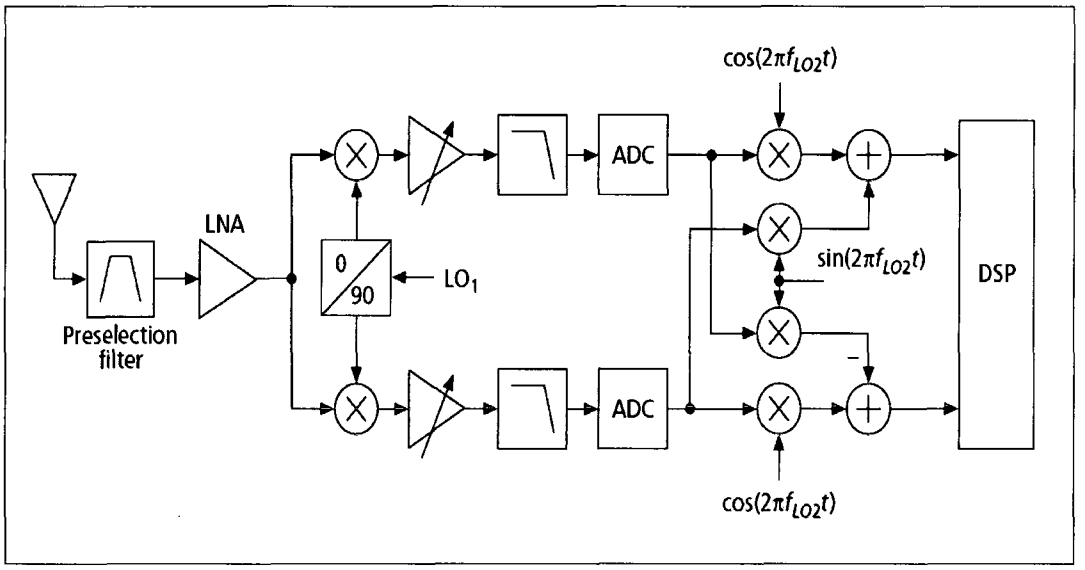


Figure 2.6 :Low-IF Receiver[7]

Typically, IF is chosen as low as one or two times the channel bandwidth in the low-IF receiver. This alleviates the DC offset problem in this architecture compared to homodyne counterpart, because the wanted signal is not located around DC after down-conversion. In addition, in the low-IF topology it is more feasible to sample the low-IF signal with a high resolution analog-to-digital converter (ADC). Another advantage of this low-IF topology is that part of the complex IR mixer is implemented in the digital domain with no gain and phase I/Q mismatches. The I/Q imbalances introduced in the preceding

analog sections can be corrected using adaptive techniques [22]. Therefore, this strategy shifts the hard specification from analog part to the ADCs. Since the performance of integrated ADCs is improving rapidly, this architecture will likely be preferred [8].

It should be mentioned here that digitizing the received signal at the IF stage can also be employed in traditional heterodyne receiver systems. This approach is sometimes called digital IF. In this architecture, the high ADC performance requirements are more challenging to accomplish within a reasonable power dissipation. Despite the advantage of avoiding the I and Q mismatches for typical first IFs in heterodyne receivers, this technique requires a prohibitively fast high-linearity high-dynamic-range ADC, currently limiting its utilization to only base stations [21].

As we know, Nyquist criterion sets the condition for a usable sampling rate for baseband (i.e. lowpass) signals. The minimum sampling frequency in baseband sampling is given by $f_{s,min} = 2f_B$, where f_B is the bandwidth of the baseband signal. The Nyquist criterion ensures that the spectral images of the sampled signal will not overlap in the frequency domain. In addition, since the whole frequency axis will be mapped onto the frequency region [- f_s /2, f_s /2] in the sampling process, limiting of the input bandwidth of a lowpass sampler will prevent signals with frequencies higher than the Nyquist frequency $f_N = f_S$ /2 from folding on top of the desired baseband signal, causing degradation in the signal-to-noise ratio (SNR) of the sampled signal. In a practical radio receiver chain, the input bandwidth of the baseband sampler can be limited by a CT lowpass anti-aliasing filter that simultaneously acts as a channel selection filter prior to A/D conversion[4]. Due to operation at low frequencies, the required stopband attenuation is

usually relatively easy to achieve with integrated filters. If necessary, it is possible to sample the signal at a higher rate than $f_{s,min}$, i.e. to use some amount of oversampling, to further relieve the stopband suppression requirement for the lowpass anti-aliasing filter.

In order to profit to a maximal extent from the benefits of digital signal processing (DSP), the received analog signal should be digitized as early as possible in the receiver chain. However, transferring the A/D interface directly from the baseband to higher frequencies, e.g. to a high IF, by following the Nyquist criterion for lowpass signals would remarkedly increase the band and sampling frequency requirements of the A/D converter. In addition, since the bandwidth of a modulated bandpass signal is usually a fraction of its center frequency, this approach seems highly inefficient, as it is in principle advantageous to use a sampling frequency which is only twice the information bandwidth. Unlike baseband sampling circuits, downconversion circuits based on subsampling take advantage of the spectral aliasing resulting from violation of the Nyquist condition for baseband signals.

CHAPTER 3

Design Consideration of Direct RF Sampling Mixer

3.1 Introduction of Direct RF Sampling Mixer

Sampling mixer is not a brand new idea. We know that subsampling mixer receiver architectures have been demonstrated in the past, they operate at lower IF frequencies[10], [11]. But their noise performance is not as good as traditional mixer because of noise folding and they exhibit sensitivity to clock jitter. Compared with subsampling mixer, direct RF sampling mixer not only operates at RF frequency, but also significantly reduces those effects and achieves great selectivity right at the mixer level to partially select channel. The selectivity is digitally controlled by the LO clock frequency, decimation ratio and capacitance ratio. Decimation ratio and capacitance ratio can be precisely set in deep-submicron CMOS processes.

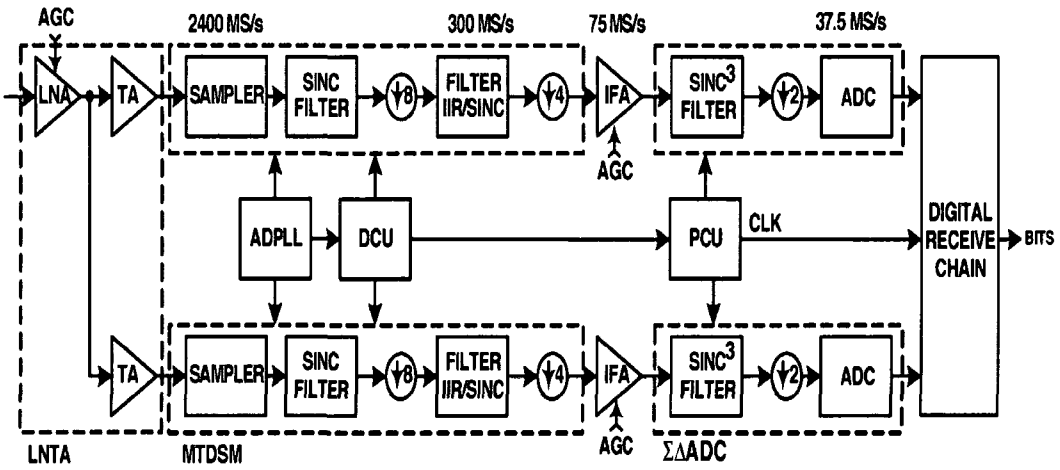


Figure 3.1 :Block diagram of direct RF sampling receiver[4]

The fundamental philosophy of direct RF sampling mixer is to provide all the filtering required by the standard as early as possible. In addition, direct RF sampling technique is quite amenable to migration to the more advanced deep-submicron processes. This approach significantly relaxes the design requirements of the following baseband amplifiers. Hence, the ideas implemented in this architecture can be easily extended to meet tougher standards in deep-submicron digital processes [4].

The architecture of direct RF sampling receiver is shown in figure 3.1. It comprises a RF front-end and baseband back-end followed by the digital receive chain. The analog front-end consists of low noise amplifier (LNA), transconductance amplifier (TA), multi-tap direct-sampling mixer (MTDSM) and digital-controlled unit (DCU). The analog back-end comprises a non-settling IF amplifier followed by a sigma-delta ADC.

All digital clocks are directly derived from the LO, hence, the most dominant current consumption pulses that are present in the clock distribution circuits occur synchronous to the LO. As a result, the coupling to the front-end circuits are either tones at known frequencies or they manifest as DC.

3.2 Brief Review of Windowed Integration Sampler

The core of a direct RF sampling mixer is a charge sampling mixer [12] or windowed integration sampler (WIS) [1]. The transconductor-capacitor (Gm-C) structure of the WIS greatly reduces the influence of the non-linear drain-source resistance of the MOS switch [13].

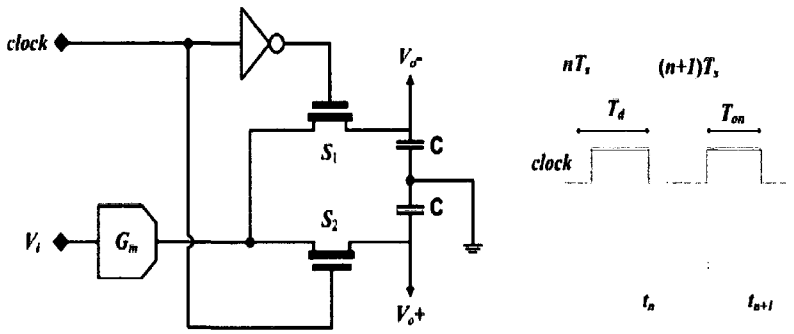


Figure 3.2 :Windowed Integration Sampler[13]

In order to completely switch on or off current source created by transconductor, differential clock signals are used in WIS as shown in Figure 3.2. This structure also gives the transconductor a constant load which is very important for the design of transconductor. The output voltage of WIS is described by the following equation:

$$C\frac{dV_o(t)}{dt} = G_m V_i(t) \tag{1}$$

where G_m is transconductance, $V_i(t)$ is the input voltage and $V_o(t)$ is the output voltage. We can obtain the following equation by integrating both sides of equation (1).

$$x(t_n) = V_o(t_n) - V_o(t_n - T_{on}) = \frac{G_m}{C}\int_{(t_n - T_{on})}^{t_n} V_i(\tau)d\tau \tag{2}$$

where $x(t_n)$ is the signal which is defined as the change of output voltage over one sampling period, T_{on} is integration window width as shown in Figure 3.2. $V_o(t_n)$ is actually the sampled voltage on the sampling capacitor if the capacitor is reset in every sampling period. We can obtain following equation.

$$x(t_n) = \frac{G_m}{C}\int(V_o(t_n) - V_o(t_n - T_{on}))dt \tag{3}$$

Based on equation (3), a linear transfer function from the continuous-time to the sampled discrete-time is described as follow:

$$SH(f) = \frac{G_m}{C}\frac{1 - e^{-j2\pi fT_{on}}}{j2\pi f} = e^{-j2\pi fT_{on}}\frac{G_m T_{on}}{C}\frac{\sin(\pi fT_{on})}{\pi fT_{on}} \tag{4}$$

From equation (4) we know that this transfer function is sinc function. DC gain can be obtained by the following equation.

$$|SH(0)| = \frac{G_m T_{on}}{C} \tag{5}$$

If the input signal is a bandpass signal, it is assumed that bandwidth of signal is much less than carrier frequency. Based on sampling theory, we know that the spectrum of input signal repeats every sampling frequency if we assume no aliasing occurs, the spectrum of output signal equals that of the spectrum of input signal multiplied by sinc function. Actually sinc function helps to remove high frequency components. From equation (5), we can see that the transfer function of WIS can introduce zeros

$$SH(f) = 0 \Rightarrow \left(\frac{\sin(\pi f T_{on})}{\pi f T_{on}} = 0\right) \tag{6}$$

$$(\pi f T_{on} = k\pi) \Rightarrow \left(\frac{\pi f}{2f_{sample}} = k\pi\right) \Rightarrow \left(f_{sample} = \frac{f}{2k}\right) \tag{7}$$

where f is carrier frequency and f_{sample} is the frequency of sampling clock, T_{on} is one half of the sampling period. Based on equation (7), if we try to use sinc function to remove high frequency components, then the relationship between carrier frequency and f_{sample} should following equation:

$$f_{sample} = \frac{f}{N}, \text{ where N is even integer} \tag{8}$$

Here integer N needs to be carefully chosen: since the input signal is normally narrowband, sampling frequency should be much larger compared with the bandwidth of input signal. From above analysis, windowed integration sampler provides embedded anti-aliasing filtering to reduce wideband noise, interferers and blockers before they alias

into the baseband. The sampled signal has a symbol rate of the sampling frequency, thus a lower sampling rate is desirable for back-end digital baseband processor. However, a high sampling frequency is required to reduce noise folding back.

3.3 Direct RF Sampling Mixer

3.3.1 Noise Analysis

The noise sources in a sampling mixer include thermal noise, switching noise and 1/f noise [18]. If we assume that the sampling clock used in the mixer has small phase noise and sharp edges, noise added by the sampling mixer is dominated by thermal noise and the folding-back wideband noise in the input signal. As we know, in conventional sample-and-hold circuits the noise power is kT/C on the sampling capacitor. Since rotating capacitors are reset periodically and noise sources are changing constantly due to switching, noise power expression of RF sampling mixer is very complicated. For simplicity, we assume the noise on the sampling capacitor is still white and the total noise power remains kT/C, the single-sided noise power spectral density (PSD) in the Nyquist band is written as [17]

$$\tilde{V}_{noise}^{2}(f) = \frac{2kT}{Cf_s} \tag{9}$$

The noise PSD is inversely proportional to the sampling frequency. Therefore, a high sampling frequency helps to reduce the noise PDS in the Nyquist band. However, this high sampling frequency results in a high symbol rate, which is very challenging for the design of ADC and the back-end digital circuits. Therefore, decimation is needed before the sampled signals are passed to the ADC. Unfortunately decimation inevitably folds

back wideband noise into the baseband. The direct RF sampling mixer includes embedded notch filter at the frequencies that will alias into baseband. Since the notch filters suppress wideband noise at those frequencies before they alias into baseband, the baseband noise PSD does not increase significantly after decimation [13].

3.3.2 Embedded Filters

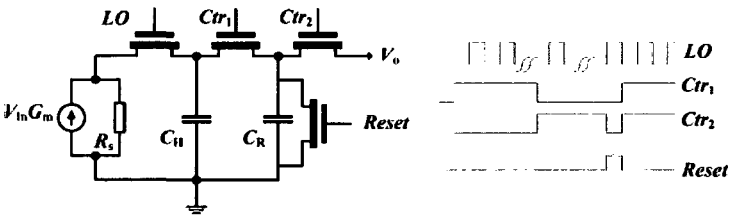


Figure 3.3 :Circuits for Embedded Filtering[13]

The embedded noise-suppressing filter is constructed as shown in Figure 3.3. The history capacitor C_H is large and never reset. There should be at least two rotating capacitors C_R. When one is sharing electrical charge with the history capacitor, the other is sharing charge with the next stage circuits which is reset after sharing charge. When a rotating capacitor is connected to the history capacitor, it has been reset already.

In the direct RF sampling mixer, the number of accumulated samples is the same as the decimation factor N. Assume just before the rotating capacitor is connected, the voltage on the history capacitor is $y(n-N)$. When there is enough time for complete charge sharing, this voltage drops to $\frac{C_H}{C_H+C_R}y(n-N)$

The voltage added to C_H and C_R by the input current is

$$\frac{1}{C_H + C_R} \sum_{k=0}^{N-1} \int_{(N-k)T_s - T_{ON}}^{(N-k)T_s} G_m V_i(t) dt = \sum_{k=0}^{N-1} x(n-k) \tag{10}$$

Based on the assumption of complete charge sharing, the rotating capacitor and the history capacitor have the same voltage $y(n)$ when they separate at the instant nT_s.

$$y(n) = \frac{C_H}{C_H + C_R} y(n-N) + \sum_{k=0}^{N-1} x(n-k) \tag{11}$$

This equation approximately holds for all n if the history capacitor is much bigger than the rotating capacitor. Applying z transform to it, the filter response is derived as

$$H(z) = \frac{Y(z)}{X(z)} = \frac{1}{1 - \frac{C_H}{C_H + C_R} z^{-N}} \cdot \frac{1 - z^{-N}}{1 - z^{-1}} \tag{12}$$

This expression, following those previously published, represents a FIR filter and an IIR filter. When the frequency is very small compared with the sampling frequency, z is approximated as:

$$z^{-N} = e^{-j\omega N T_s} \approx 1 - jNT_s\omega \tag{13}$$

Using the frequency domain approximation, the IIR filter has properties of a single-pole low pass filter. It helps channel selection. In the direct RF sampling mixer, the decimation is performed in two or more stages to alleviate the influence of leakage in the capacitors. When the symbol rate is low enough, an ADC is introduced and more sophisticated DSP algorithms can be applied [13].

Equation (8) shows that the transfer function has zeros at some frequencies ($k\frac{f_s}{N}$, k is not 0, N). Noise near those frequencies is suppressed. The noise aliases into the first Nyquist band after the decimation. But the sum is small and the signal-to-noise ratio (SNR) will not deteriorate significantly due to the notches near the nulls.

3.4 Estimation of the Noise Figure

Sampling mixers suffer from noise folding that wideband noise from the source fold back to baseband or IF band, therefore the noise performance of sampling mixer is not as good as traditional mixer such as Gilbert mixer. The wideband noise is white noise and can be treated as sourced by an equivalent resistor R. If we assume that the input signal has a power spectrum density (PSD) $S(f)$, then the double-side signal-to-noise-ratio (SNR) of the source is

$$SNR_1(f) = \frac{S(f)}{2kTR} \tag{14}$$

From sampling theory, we know that sampling operation moves the spectrum of signal to the baseband with attenuation and folds back the wideband noise to the baseband as well. Because of the embedded FIR/IIR filter, in the frequency band close to DC, the double-side PSD of folding-back noise can be written as

$$V_{noise}{}^2(f) = 2kTR \sum_{k=-\infty}^{\infty} |g(0)|^2 \sin c^2\left(\frac{k\pi}{2}\right) = 4kTR|g(0)|^2 \tag{15}$$

where $g(0)$ is the system transfer function at DC. The signal PSD at the Nyquist band is dependent on the distribution of the input signal. In the narrow band close to DC, the signal power can be written as

$$V_{noise}^2(f) = \frac{4}{\pi^2}|g(0)|^2[S(f+f_o) + S(f-f_o) + 2\rho\sqrt{S(f+f_o)S(f-f_o)}] \quad (16)$$

Where $\rho \in [0, 1]$ is the correlation factor. If the signal has a symmetrical PSD and the correlation factor is zero, the noise figure in a narrow band around DC is

$$NF = 10\log\left(\frac{SNR_{in}}{SNR_{out}}\right) = 10\log\left(\frac{4}{\pi^2}\right) = 3.9dB$$

This matches the minimum noise figure mentioned in [10]. However, if the low-frequency noise has been greatly suppressed by a pre-filter or the correlation factor is 1, the noise figure due to wideband noise folding back can be as good as merely 0.9dB. A noise figure of 2.0dB has been measured for the analog front end.

CHAPTER 4

Design of RF Sampling Front End and Simulation Results

In this chapter, the proposed RF sampling front end building blocks and simulation results will be presented. The front end circuit structure, shown in Figure 4.1, is based on previously published papers about direct RF sampling mixer [3], [4] and [5]. This front end is working at 2.4GHz frequency. The building blocks include a low noise amplifier (LNA), RF transconductance amplifier (TA), multi-tap direct-sampling mixer (MTDSM) and digital-controlled unit (DCU). The frequency synthesizer is not included in this front end, a signal generator will be used to provide local oscillation (LO). In addition, IF amplifier is not included in this front end due to the limitation of chip area.

In order to improve immunity of the common-mode noise, differential topology is employed for all the building blocks. All the circuit blocks discussed here are implemented by using 0.18 μm CMOS technology. Each of them is individually verified by schematic and post-layout simulation.

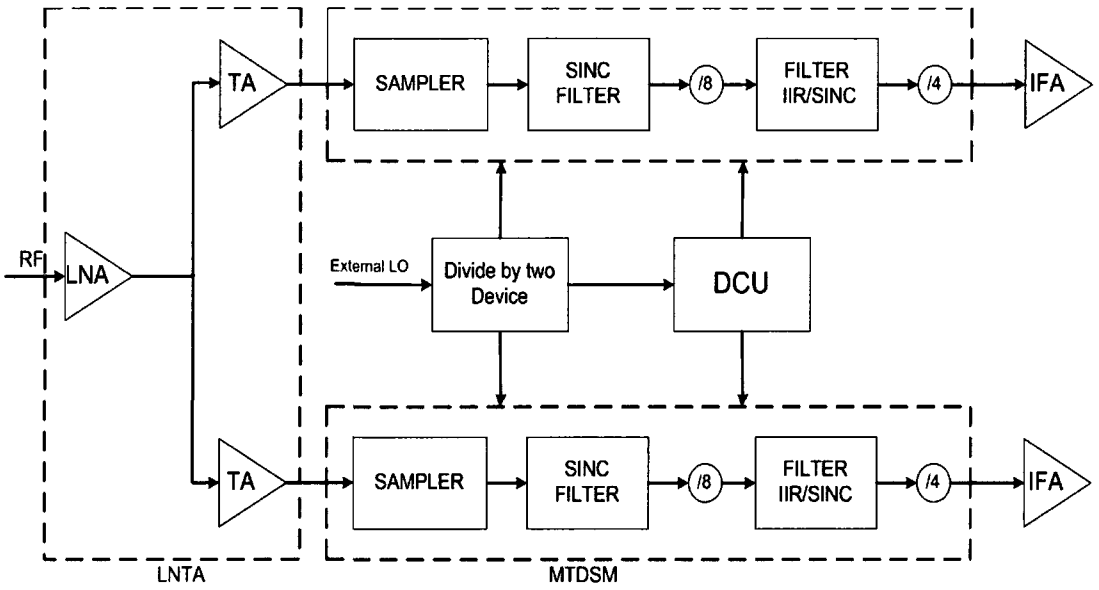


Figure 4.1 :Block Diagram of Direct RF Sampling Front End

The received RF signal is amplified by the low noise amplifier (LNA), and then split into I and Q path since RF signal is a digitally modulated signal. Transconductance amplifier (TA) is used to convert amplified RF signal from voltage domain to current domain. The LNA and TA are designed by conventional RF techniques and they are continuous-time blocks in the receiver. The LNA together with the TA are referred to as low-noise transconductance amplifier (LNTA).

The RF current is then downconverted to a low IF and integrated on a differential sampling capacitor at the LO rate. The positive side together with negative side sample the input signal at the Nyquist rate of the RF carrier. A series of the decimation and filtering functions follow the RF sampling such that any decimation is preceded by the required anti-aliasing filtering. This operation is performed by a multi-tap direct-sampling mixer (MTDSM), shown in Figure 4.2. The MTDSM comprises switched capacitors that

receive timing signals from DCU which generates clocks for the Analog Front End. The main part of the DCU consists of a shift-register whose outputs are "one-hot" constrained as shown in Figure 4.3.

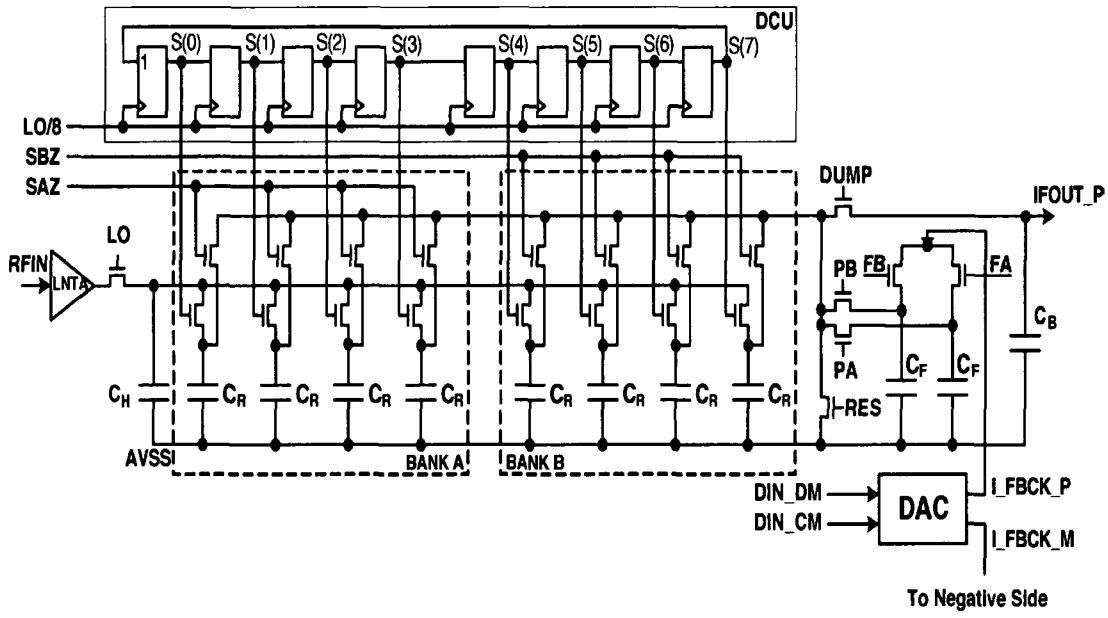


Figure 4.2 :Multi-Tap Direct-sampling Mixer[4]

Two banks of four rotating capacitors C_R are provided with the purpose of sampling the RF input together with a history capacitor (C_H). For eight LO cycles, one out of four rotating capacitors in a bank samples the input together with C_H in parallel, while all four rotating capacitors in the second bank are charge shared with the buffer capacitor C_B . After the charge sharing is completed, the rotating capacitor bank is reset and precharged to a desired voltage by charge-sharing it with a feedback capacitor (C_F). During this time, input RF samples are accumulated on the capacitors in the other bank of rotating capacitors [4].

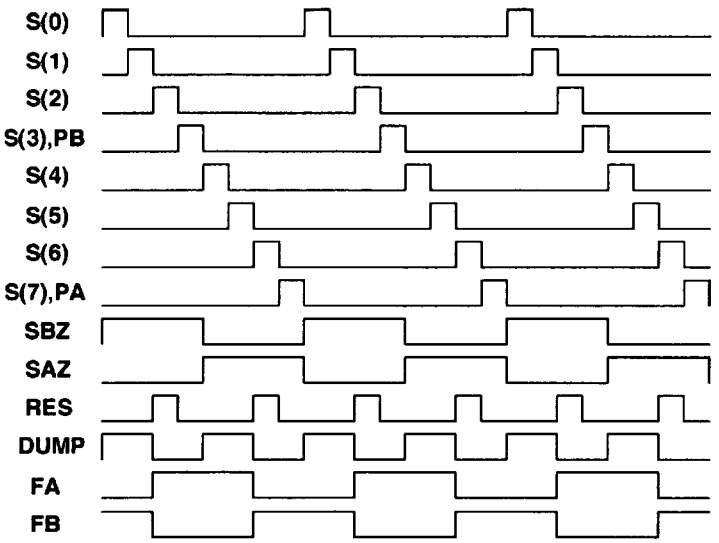


Figure 4.3 :Digital-Controlled Unit Output Signals[4]

4.1 Differential Low Noise Amplifier

The low noise amplifier (LNA) is one of the most important building blocks in the front end of a wireless communication system. LNA is the first stage of receiver and dominates the noise figure of the whole receiver. Besides of low noise, low power consumption, high linearity and chip area are the other key requirements. Because of this situation the design of the LNA is really a challenge. In order to achieve high sensitivity, the LNA is required to have not only low noise figure but also high gain to reduce noise contribution from subsequent circuits and good input matching for maximal power transfer. But gain can not be set too high, otherwise linearity will drop significantly. There is a tradeoff between noise figure, gain and linearity.

4.1.1 LNA Design

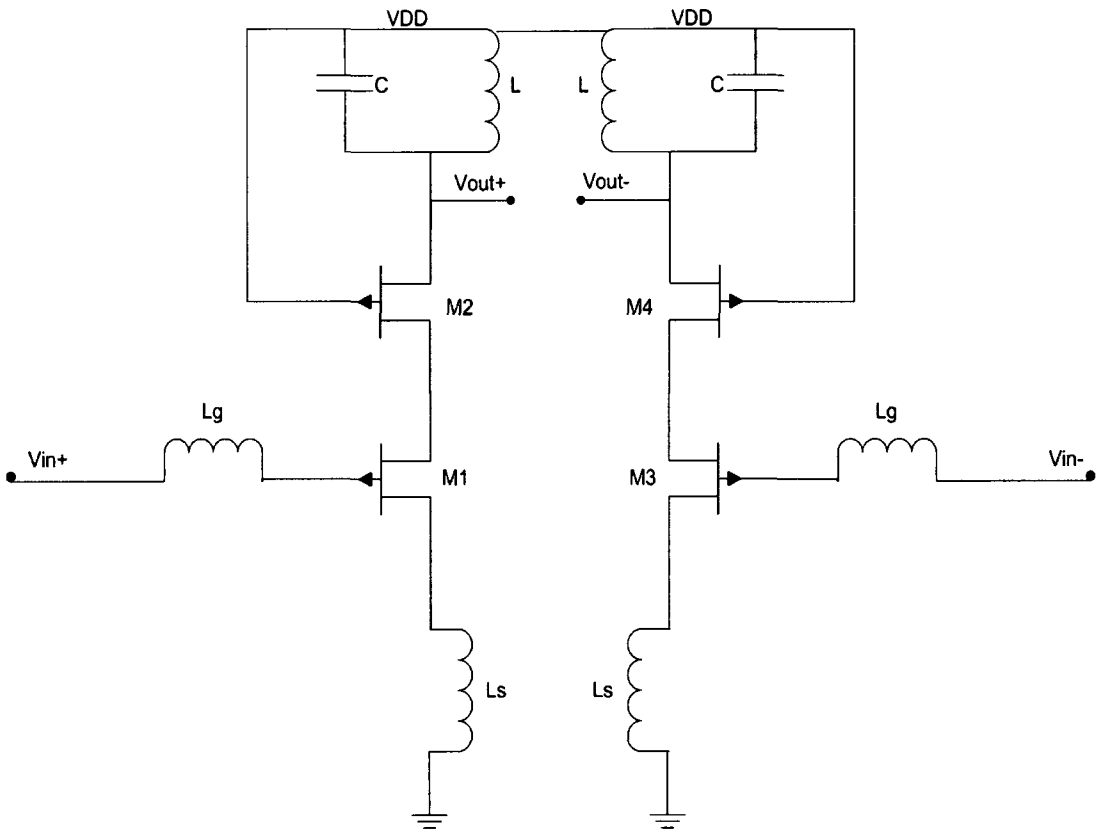


Figure 4.4 :Differential Common Source Inductive Degeneration LNA

There are several types of topologies for an integrated low noise amplifier, like common-gate and common-source structures. A common-source cascade amplifier with inductive degeneration is often preferred for narrow band application because it can satisfy requirements for low noise figure and high power gain simultaneously. Differential structure as shown in figure 4.4 is often used to remove common mode noise. The transistor in common-gate (CG) configuration of the cascode amplifier is used to reduce the Miller effect. As we known, the Miller effect accounts for an increase in the equivalent input capacitance of an inverting voltage amplifier due to amplification of capacitance

between the input and output terminals. This Miller capacitance can be obtained by equation $C_M = C(1 - A_V)$, where A_V is the gain of the common-source amplifier and C is the feedback capacitance C_{gd1}.

From Figure 4.4, we can see that the gain of the common-source (CS) amplifier is $G_{m1}R_L$, where R_L is the output impedance. The input impedance of common-gate (CG) amplifier is $1/G_{m2}$. Therefore, if both transistor M1 and M2 have same G_m, the gain of common-source amplifier decrease to -1 and the Miller capacitance is about $2C_{gd1}$. From the above analysis, we can know that the Miller capacitance is significantly reduced by introduction of common-gate amplifier.

At the output of the cascode amplifier, the overlap capacitance C_{gd2} does not affect the Miller effect since the gate of transistor M2 is AC grounded. Since this C_{gd2} brings capacitance to LC tank. Thus, the capacitor of the LC tank has to be set large enough to make the tank insensitive to C_{gd2}. In addition, with an AC ground at the gate of the cascode amplifier, the output is decoupled from the input and high reverse isolation can be achieved, furthermore LNA stability is also improved.

The use of inductive degeneration results in no additional noise generation since the real part of the input impedance does not correspond to a physical resistor [14]. The source inductor L_s generates a resistive term in the input impedance.

$Z_{in} = \frac{g_{m1}L_s}{C_{gs1}} + j\left(\omega L_g + \omega L_s - \frac{1}{\omega C_{gs1}}\right)$, where L_g and L_s are gate and source inductor respectively, g_{m1} and C_{gs1} denote small signal parameter of transistor M1 (g_{ds1} and C_{gd1} are ignored)

To obtain pure resistive term at the input, gate inductor L_g together with source inductor L_s need to cancel out the admittance due to the gate-source capacitor C_{gs1}. Here, it is assumed that LC tank is in resonance at angular frequency ω_o which is 2.4GHz for this LNA design. To achieve this cancellation and input matching, the source and gate inductances should be set to

$$L_s = \frac{R_s C_{gs}}{g_m}, \qquad L_g = \frac{1}{\omega_o{}^2 C_{gs}} - L_s$$

where R_s is the required input resistance, normally 50.

The noise figure of the whole amplifier excluding noise contribution of transistor M2 can be given as [15].

$F = 1 + \frac{\gamma}{\alpha}\frac{1}{Q}\frac{\omega_o}{\omega_T}\left[1 + \frac{\delta\alpha^2}{k\gamma}(1+Q^2) + 2|C|\sqrt{\frac{\delta\alpha^2}{k\gamma}}\right]$, where $\alpha = \frac{g_m}{g_{d0}}$, γ, δ, C, k are bias dependent transistor parameters and $Q = \frac{1}{\omega_o C_{gs} R_s}$ is the quality factor of the input circuit. From this noise figure equation we can know that noise figure is improved by the factor $(\omega_T/\omega_o)^2$ [15]. In order to simplify noise figure analysis, induced gate noise is ignored. The noise figure of the LNA can be approximated by following equation:

$F \approx 1 + \frac{\kappa g_m R_s}{(\omega_T/\omega_o)^2}$, where κ is bias dependent constant and R_s is source resistance. Taking into account that $\omega_T = g_m/C_{gs}$, we can see that increasing of g_m lowers the noise figure but at the cost of higher power consumption. Since C_{gs} contributes to the noise factor, lowering this capacitance leads to improved noise. The last possibility of noise reduction is reducing the signal source resistance R_s. However, this resistance is fixed, normally. Decreasing the C_{gs} capacitance is done by reducing the size of the transistor. This has an impact on the linearity of the amplifier, and according to input matching requirements, very large inductors L_g should be used that can no longer be placed on chip. Because of this reason the inductor L_g is placed off-chip.

From the above analysis, we can obtain the width and length of transistor M1 to M4, calculate the value of inductance and capacitance for LC tank, find the value of L_g and L_s. The final transistor size and value of inductance and capacitance are shown in table 4.1 and table 4.2

TABLE 4.1: Transistor Size for LNA

Transistor	Width [μ m]	Length [μ m]
M1	240	0.18
M2	240	0.18
M3	240	0.18
M4	240	0.18

TABLE 4.2: Passive Component Value for LNA

Component	Value	Comments
L	2nH	inductance in LC tanK
C	2pF	capacitance in LC tank
L_g	10.26nH	too big, off chip
L_s	0.5717nH	on chip

4.1.2 LNA Simulation Result

The summary of LNA simulation results are shown in the table 4.3 and followed by detailed simulation results in Figure 4.5 through 4.8. All simulation results are obtained by using the spectreRF simulator to simulate the 0.18um CMOS technology design.

TABLE 4.3: LNA Simulation Summary

Parameter	Unit	Specification	Simulation
Power Supply	V	1.8	1.8
Power Gain	dB	20	19.95
Noise Figure	dB	<2.0	1.7
IP3	dBm	as high as possible	-12.8
S11	dB	as low as possible	-40
Z11(Re)	ohm	100	100.72
Z11(Im)	ohm	0	0.503
1dB Compression Point	dBm	as high as possible	-20

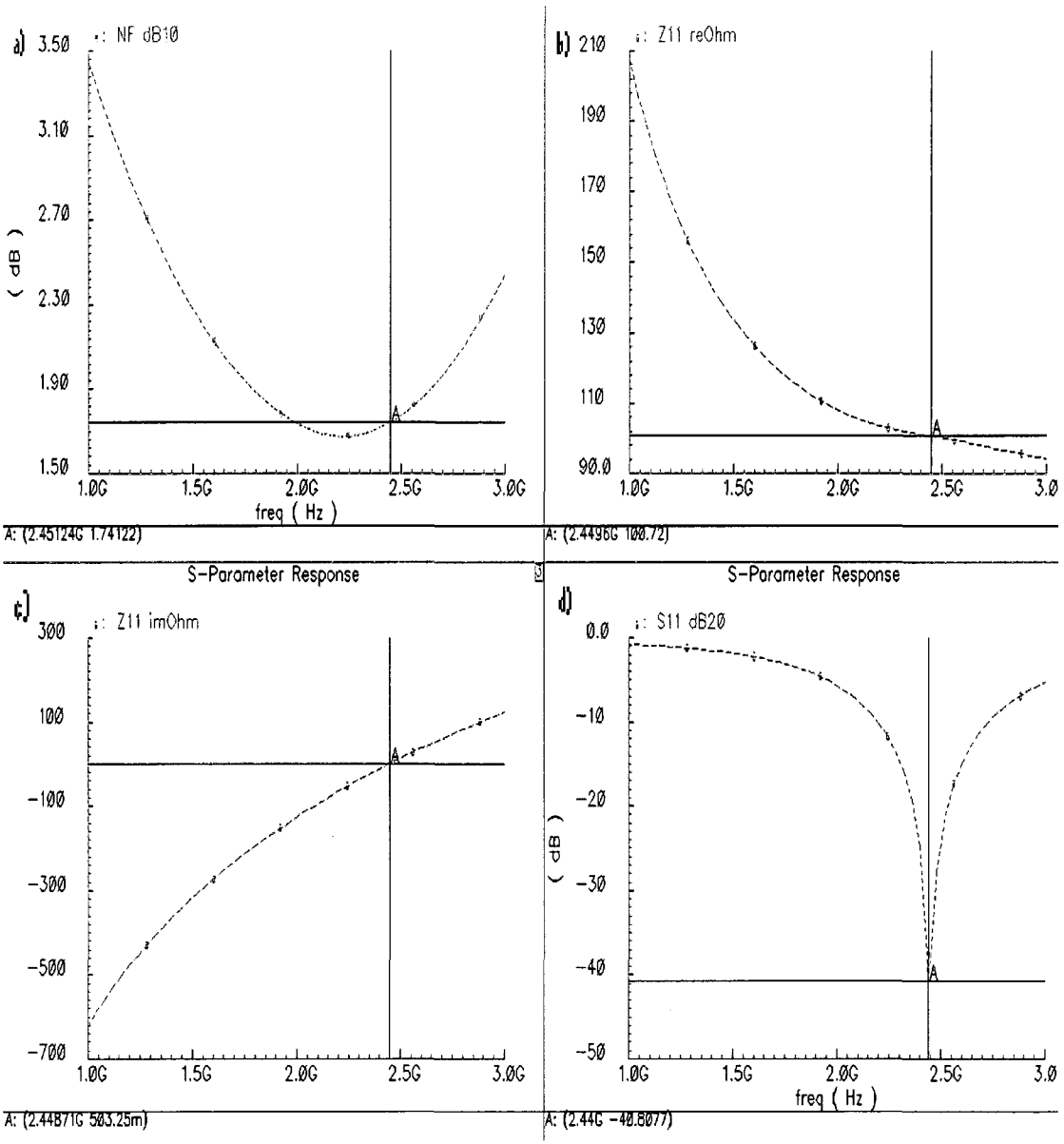


Figure 4.5 :LAN Simulation Result

The simulation of LNA noise figure versus frequency is shown in Figure 4.5a. The real part and imaginary part of input impedance of LNA versus frequency simulation are shown in Figure 4.5b and 4.5c respectively. The simulation of S11 versus frequency is shown in Figure 4.5d.

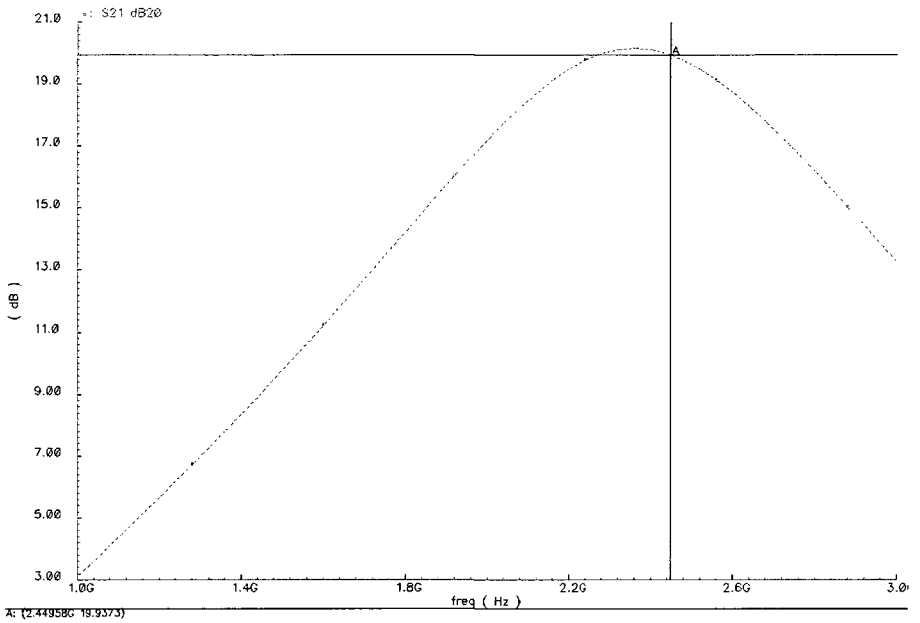


Figure 4.6 :Power Gain Simulation Result

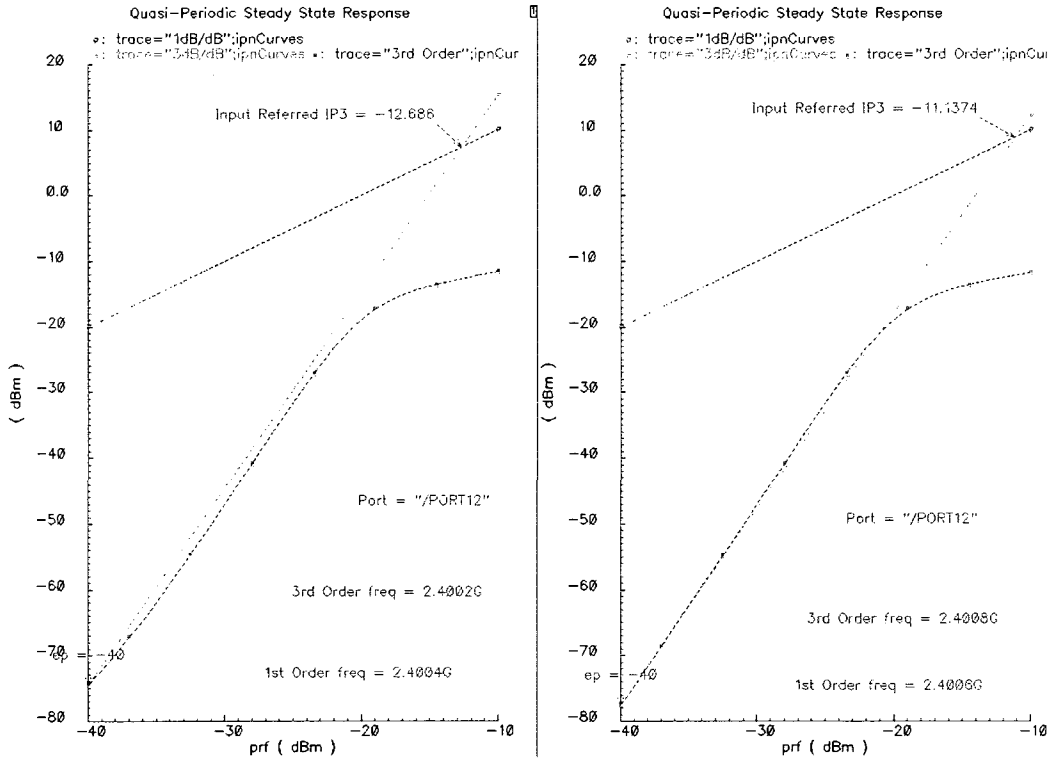


Figure 4.7 :IP3 Simulation Result

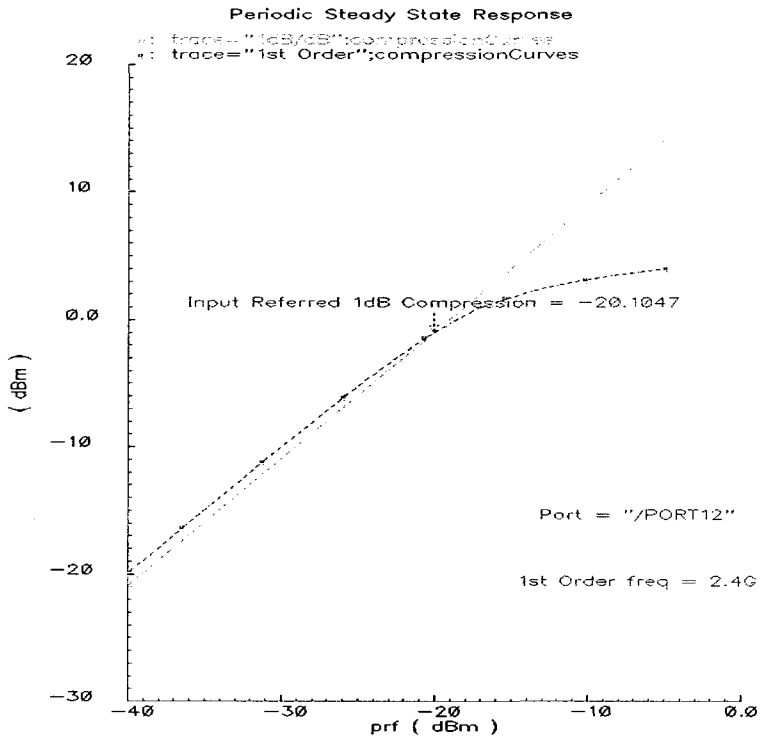


Figure 4.8 :1dB Compression Point Simulation

The simulation of power gain versus frequency is shown in Figure 4.6. IP3 simulation and 1dB compression point simulation are shown in Figure 4.7 and Figure 4.8 respectively. The term "prf" in Figure 4.7 and 4.8 indicates signal input power, the unit of prf is dBm.

4.2 Differential Transconductance Amplifier

The transconductance amplifier is used to translate signal from voltage domain to current domain. In RF sampling front end design, RF signal is converted from voltage to current after signal is amplified by LNA. Since LNA adopts differential structure, consequent TA also uses differential structure.

The most important parameter in TA design is linearity in a high frequency range. Noise performance is also very important since this transconductance amplifier is the second stage following. In order to reduce noise contribution from TA, noise figure needs to be as small as possible.

4.2.1 Transconductance Amplifier Design

The output of a differential transconductance amplifier can be expressed as $i_O(v_1, v_2) = (v_1 - v_2)g_m$ where v_1 and v_2 are the positive and negative input signals of transconductance amplifier. In reality, the transconductance g_m is implemented by MOS transistors which are nonlinear devices. So, we require techniques to linearize the transconductance g_m.

There are three common types of linearization techniques: 1) attenuation: reduce gain to increase linearity, 2) nonlinear terms cancellation, and 3) source degeneration. Among these techniques, source degeneration is often employed. Figure 4.9a and 4.9b illustrate two possible implementations [9]. Although both topologies realize the same transconductance, they present different properties. In figure 4.9a, the noise contribution of the current sink is divided in both branches appearing at the outputs as common-mode noise. For the structure in Figure 4.9b, the noise of each current sink is injected to a single

output, appearing as a differential noise current. On the other hand, the voltage drop at the resistors of Figure 4.9a reduces the common mode swing of the input signals; this is particularly critical for low-voltage applications [9].

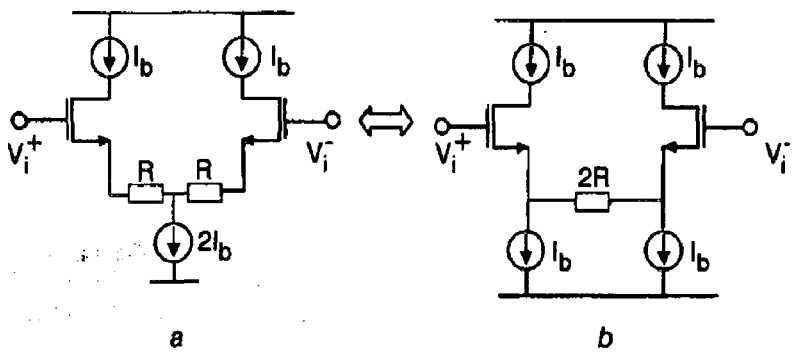


Figure 4.9 :Gm Linearization schemes via source degeneration[9]

Although the noise factor is slightly larger if we use resistor for source degeneration, the linear range is increased. In general, the source degeneration reduces the small-signal transconductance. The differential transconductance amplifier circuit is presented in Figure 4.10.

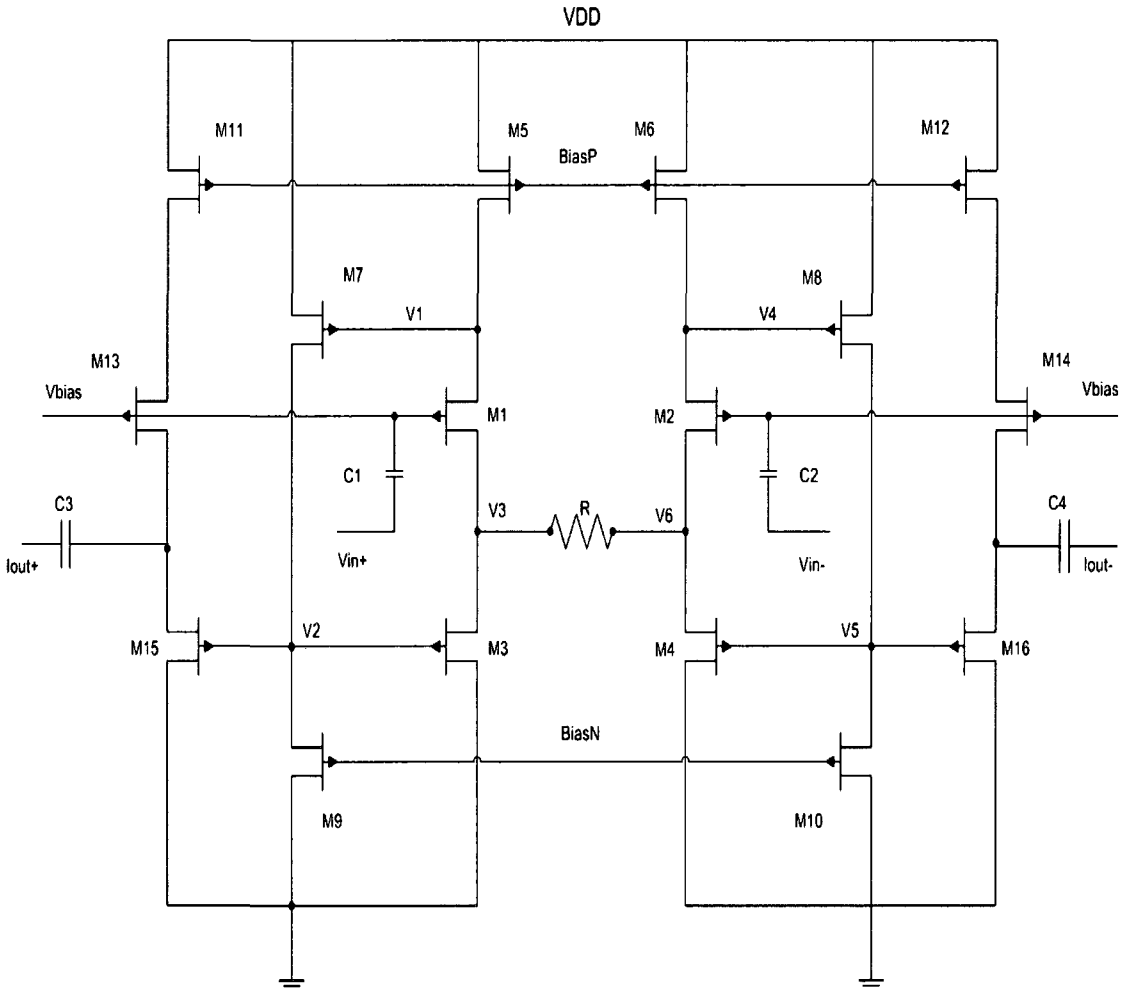


Figure 4.10 :Differential Transconductance Amplifier

Vin+ and Vin- are the differential voltage input signals of transconductance amplifier, Iout+ and Iout- are the current output of transconductance amplifier. Capacitor C1, C2, C3 and C4 are used to couple AC signal and block DC signal. Transistor M1 and M2 serve as input stage, transistor M5, M6, M11 and M12 form current mirror to provide constant current. Transistor M7 and M8 are used as source-follower amplifier, transistor M9 and M10 are used to provide current for M7 and M8 respectively. Transistor M3 and M15 form current mirror, similarly transistor M4 and M16 form current mirror.

When input signal Vin+ and Vin- is applied to transistors M1 and M2, the output of M1 and M2 change with input signals. Since Vin+ and Vin- are differential signals, it is assumed that Vin+ becomes a little bit larger and Vin- becomes a little bit smaller simultaneously. Transistor M1 turns on a little more, then output voltage V1 goes down to keep constant current. Since M7 is source-follower, voltage V2 also drops and the current of M3 will decrease, then voltage V3 increases and keeps V_{gs1} constant. Transistor M1, M7 and M3 form feedback loop to keep the current of M1 constant. Similar analysis can be done for transistor M2, M8 and M4, there is current through resistor R since V3 goes up and V6 goes down. The current of M15 and M16 copy current of M3 and M4 respectively. Finally, the AC coupled differential current output Iout+ and Iout- are obtained.

In addition, the size of transistor M1 and M2 must be carefully chosen since noise figure is also very important parameter for the TA. Techniques used to reduce noise figure for the LNA is also taken for the transconductance amplifier design. The size of transistor is presented in table 4.4

TABLE 4.4: Transistor Size for Transconductance Amplifier

Transistor	Type	Width(μ m)	Length(μ m)
M1, M2	NMOS	80	0.18
M5, M6, M11, M12	PMOS	10	0.20
M3, M4, M7, M8, M9, M10	NMOS	10	0.5

4.2.2 Transconductance Amplifier Simulation Result

The simulation results of transconductance amplifier are shown in figure 4.11 and figure 4.12, the transconductance and noise figure are 5.90mS and 9.51dB respectively.

All simulation results are obtained by using the spectreRF simulator to simulate the 0.18 μm CMOS technology design.

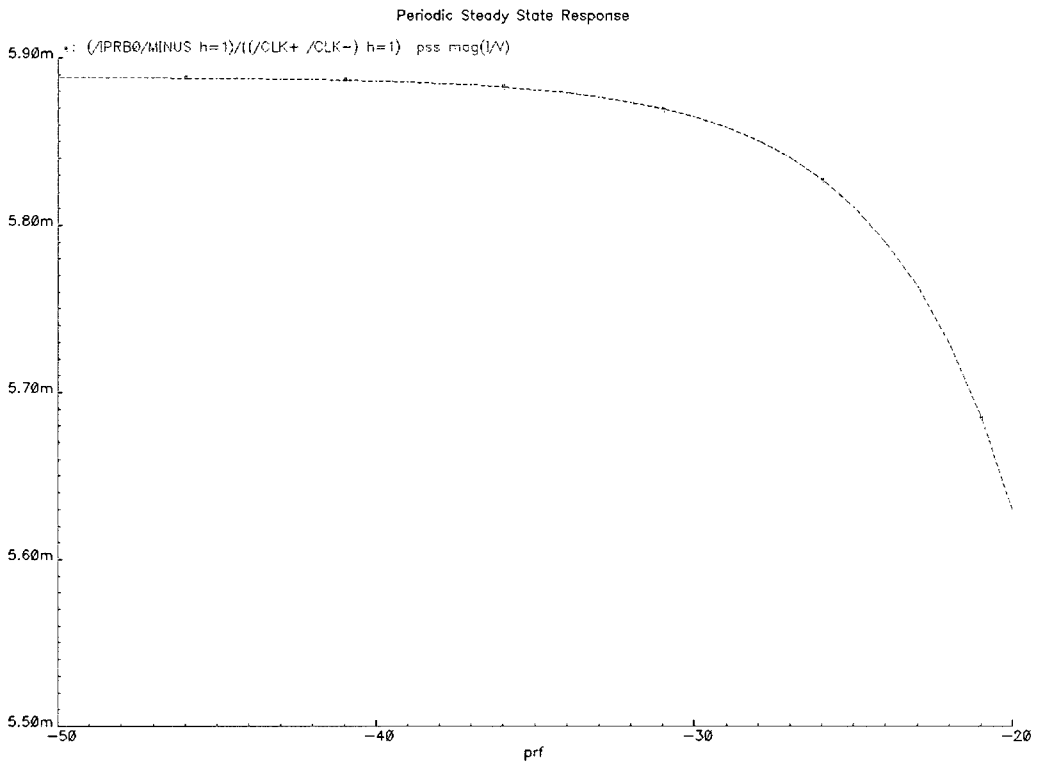


Figure 4.11 :Linearity of Transconductance Amplifier

The simulation of transconductance versus input signal power is shown in Figure 4.11. The term "prf" in Figure 4.11 indicates input signal power, the unit of prf is dBm. The transconductance of transconductance amplifier is 5.90 mS.

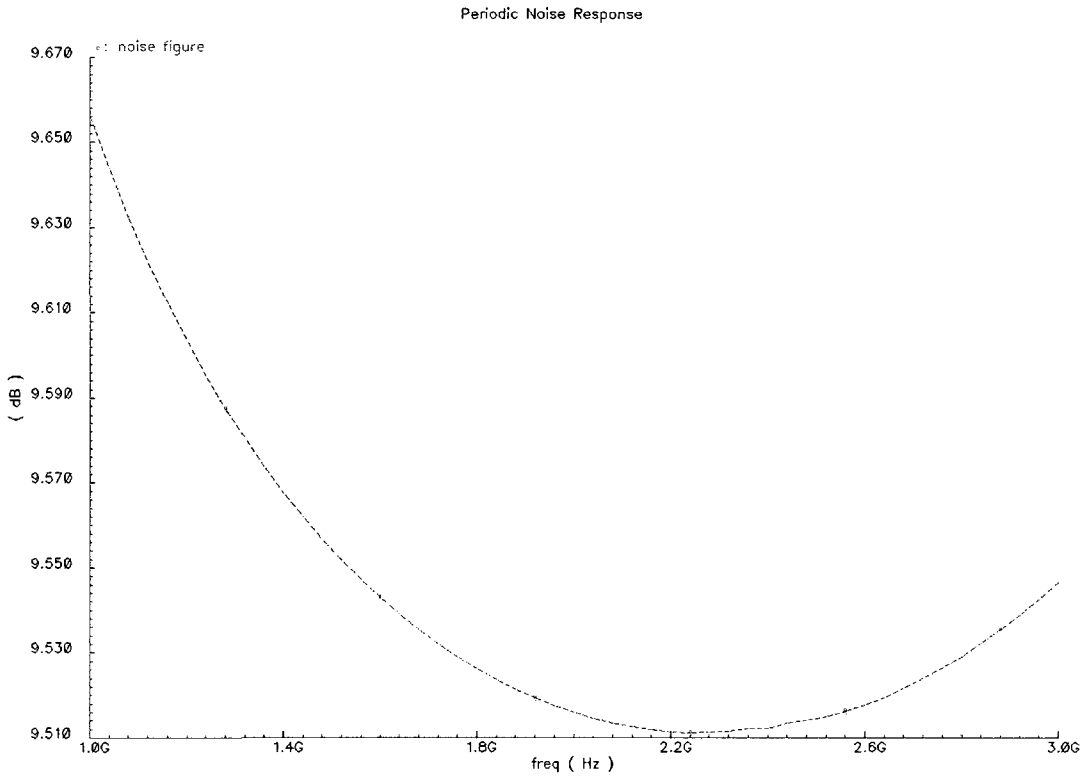


Figure 4.12 :Noise Figure of Transconductance Amplifier

The simulation of noise figure versus frequency for Transconductance Amplifier (TA) is shown in Figure 4.12. Based on the simulation result, noise figure of Transconductance Amplifier is less than 10dB.

4.3 Digital-Controlled Unit

Digital-Controlled Unit (DCU) is used to generate clocks for multi-tap direct-sampling mixer (MTDSM). The main part of the DCU consists of a shift-register whose outputs are "one-hot" signals as shown in Figure 4.3. All the digital-controlled signals are derived from local oscillator (LO). Since there is no LO signal generated from the internal of chip, LO signal is from external signal generator. This external signal can create two

quadrature signals by divider-by-two circuit because there are I and Q two channels for this RF sampling mixer. "One-hot" signals are created by consequent divider-by-eight and 8-bit shift register. The basic building blocks are master-slave D flip-flop and divider-by-two. Divider-by-four and divider-by-eight circuit can be created using basic D flip-flop circuit.

4.3.1 D latch structure

The transistor level schematic of D latch based on current mode logic (CML) structure is shown in figure 4.13. There are two transistor pairs: one is to sample the input data and the other one is to hold the input data. The operation of sample and hold depends on whether the clock is high or low. When the clock is high, the output signals follow the input signals. This is called sample mode. When the clock signal is low, the hold pairs form a positive feedback to maintain the previous state of the output signal. It is also isolate it from the input data. This is called hold mode. The size of transistors was be carefully optimized for the proper operation. The consideration of designing CML circuits includes voltage swing, power consumption and speed.

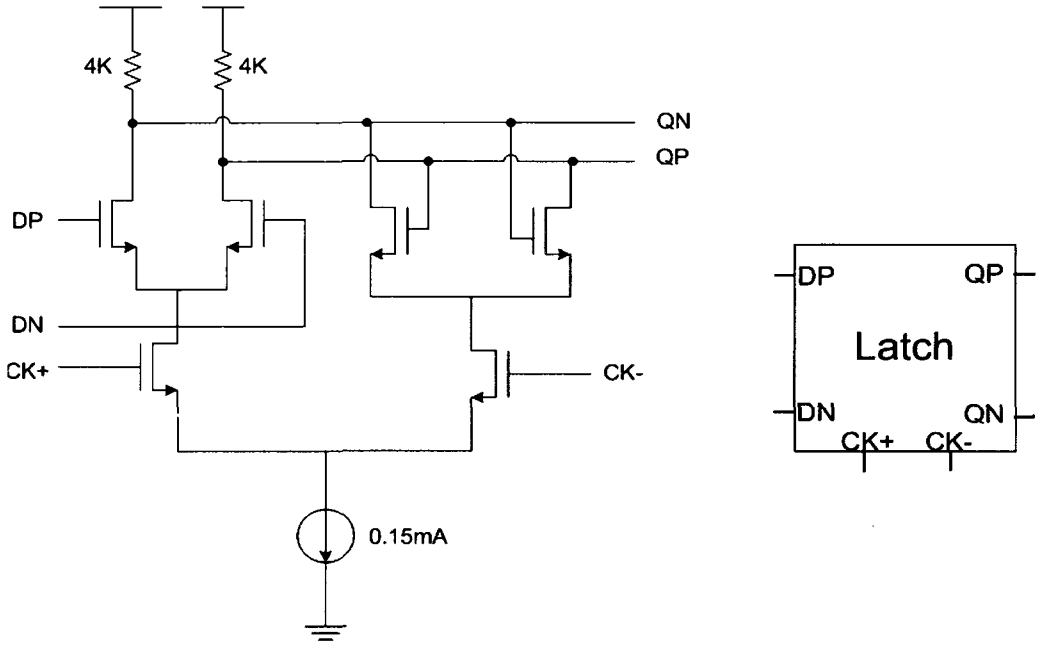


Figure 4.13 :D latch schematic and symbol

4.3.2 D flip-flop (DFF) structure

The D flip-flop (DFF) structure as shown in Figure 4.14 consists of two D latches. When the clock signal (CK) is high, the input data is captured and stored in the first D Latch. When this clock signal (CK) becomes low, the stored data in the first D Latch is transferred to the outputs of the second D Latch, and the outputs will not be affected by the input data until the next clock comes. The CML structure is employed to achieve high speed operation.

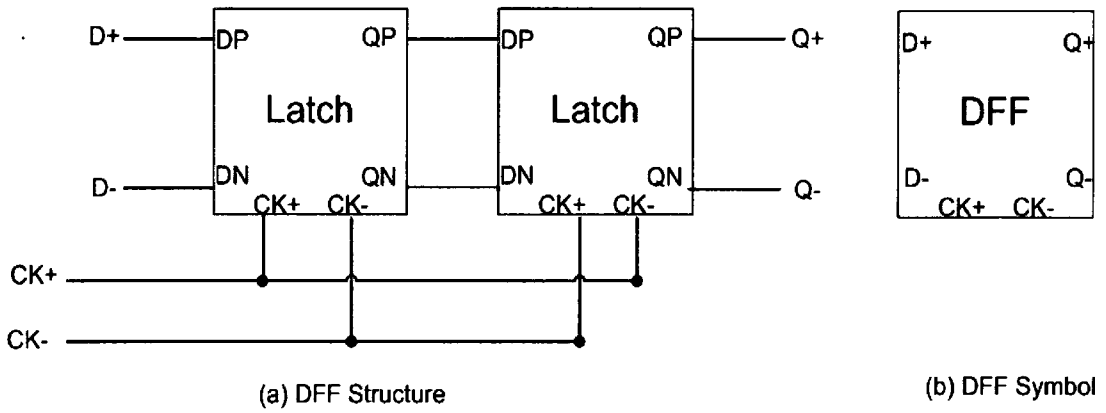


Figure 4.14 :DFF Structure and Symbol

4.3.3 Frequency Divider

As shown in Figure 4.7, there are several frequency dividers in DCU. The block divider-by-2 is used to create quadrature LO signals used for I and Q channels. The block divider-by-8 is used for diving down LO by eight to provide digital control signal for shift register to create "one-hot" signals. In addition the block divider-by-4 is used to create SAZ/SBZ and FA/FB. The basic building for these frequency dividers is D flip-flop. The block diagram of divider-by-2, divider-by-4 and divider-by-8 is presented in Figure 4.15, Figure 4.16 and Figure 4.17 respectively.

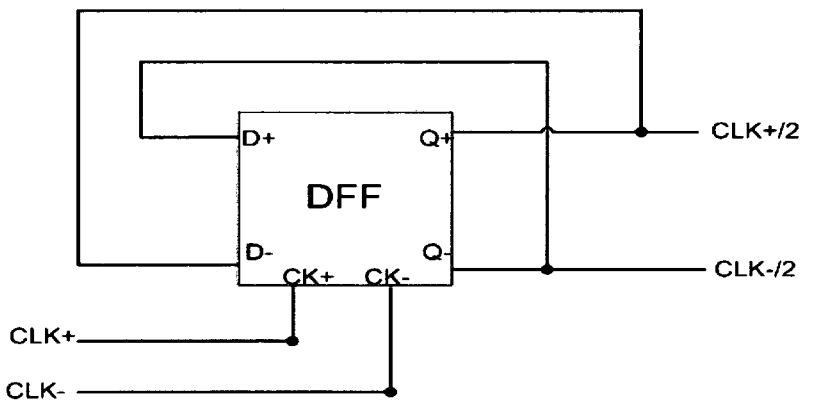


Figure 4.15 :Block diagram of Frequency Divider by 2

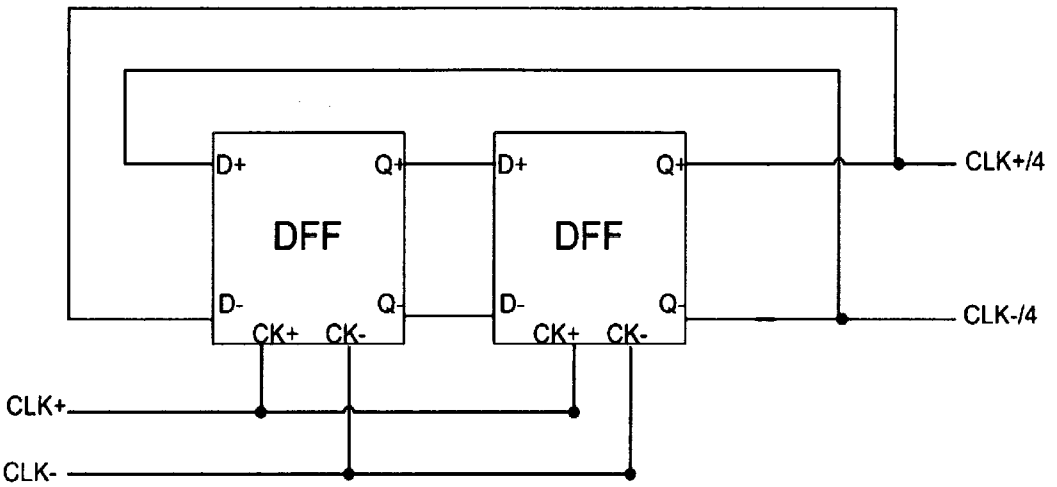


Figure 4.16 :Block Diagram of Frequency Divider by 4

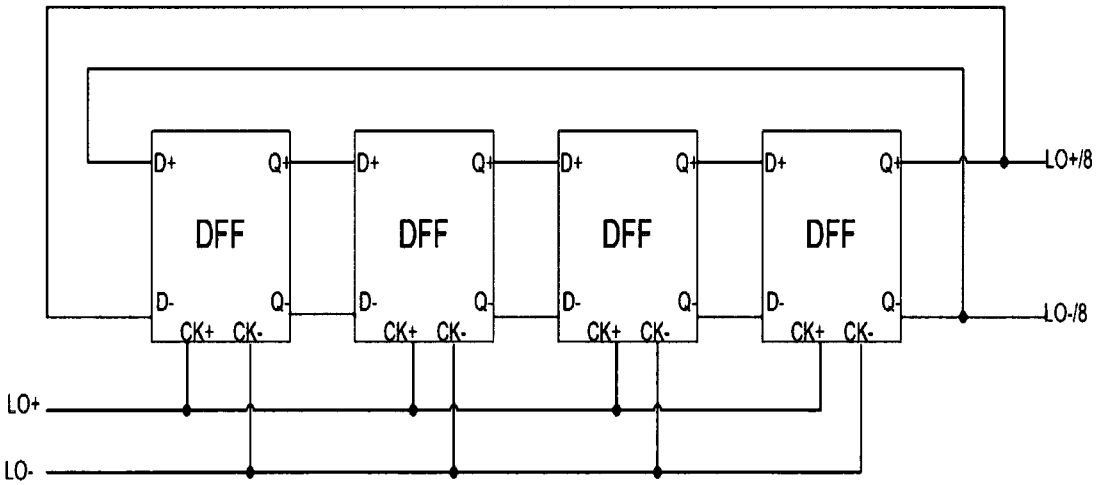
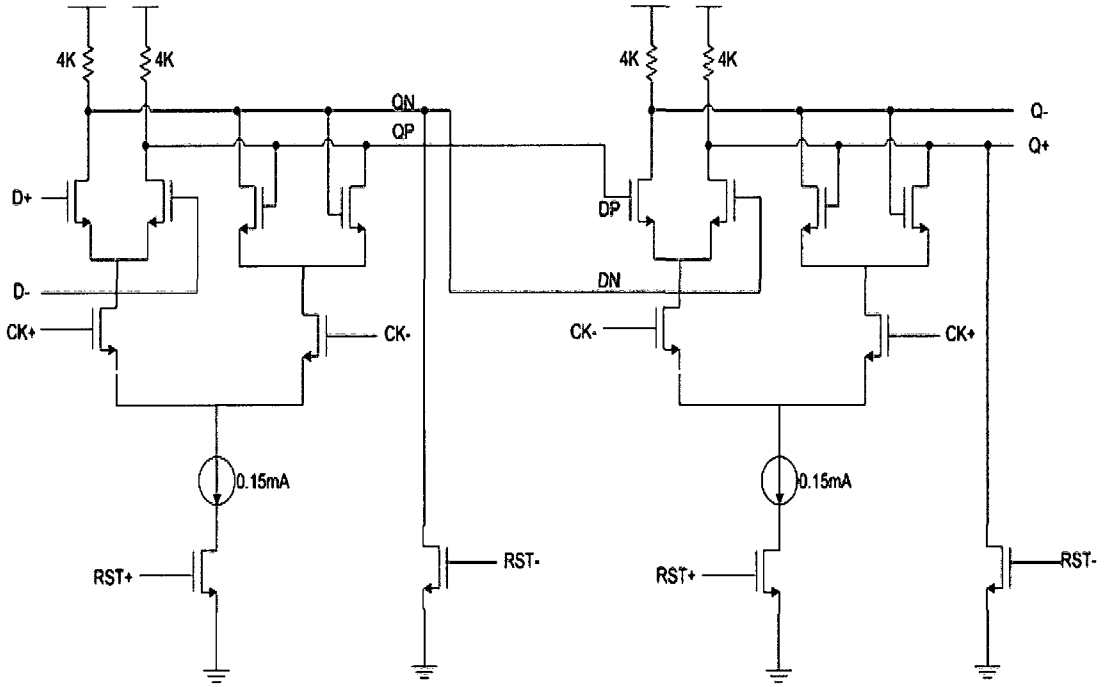


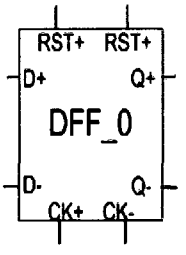
Figure 4.17 :Block Diagram of Frequency Divider by 8

4.3.4 Shift Register

An 8-bit shift register is used for creating 8 "one-hot" control signals to turn on or off rotating capacitors. Since these signals are "one-hot", this means that in the beginning, only one of 8 shift registers should be set to high, others are set to low. Based on this requirement, we need to change basic DFF with initialization high and low. Reset signal is added in the circuit level. There are two building blocks for this shift register: DFF with low initialization as shown in Figure 4.18 and DFF with high initialization as shown in Figure 4.19. The block diagram of 8-bit shift register is presented in Figure 4.20.



(a) Structure of DFF with low initialization



(b) DFF_0 Symbol

Figure 4.18 :Circuit and Symbol of DFF with low initialization

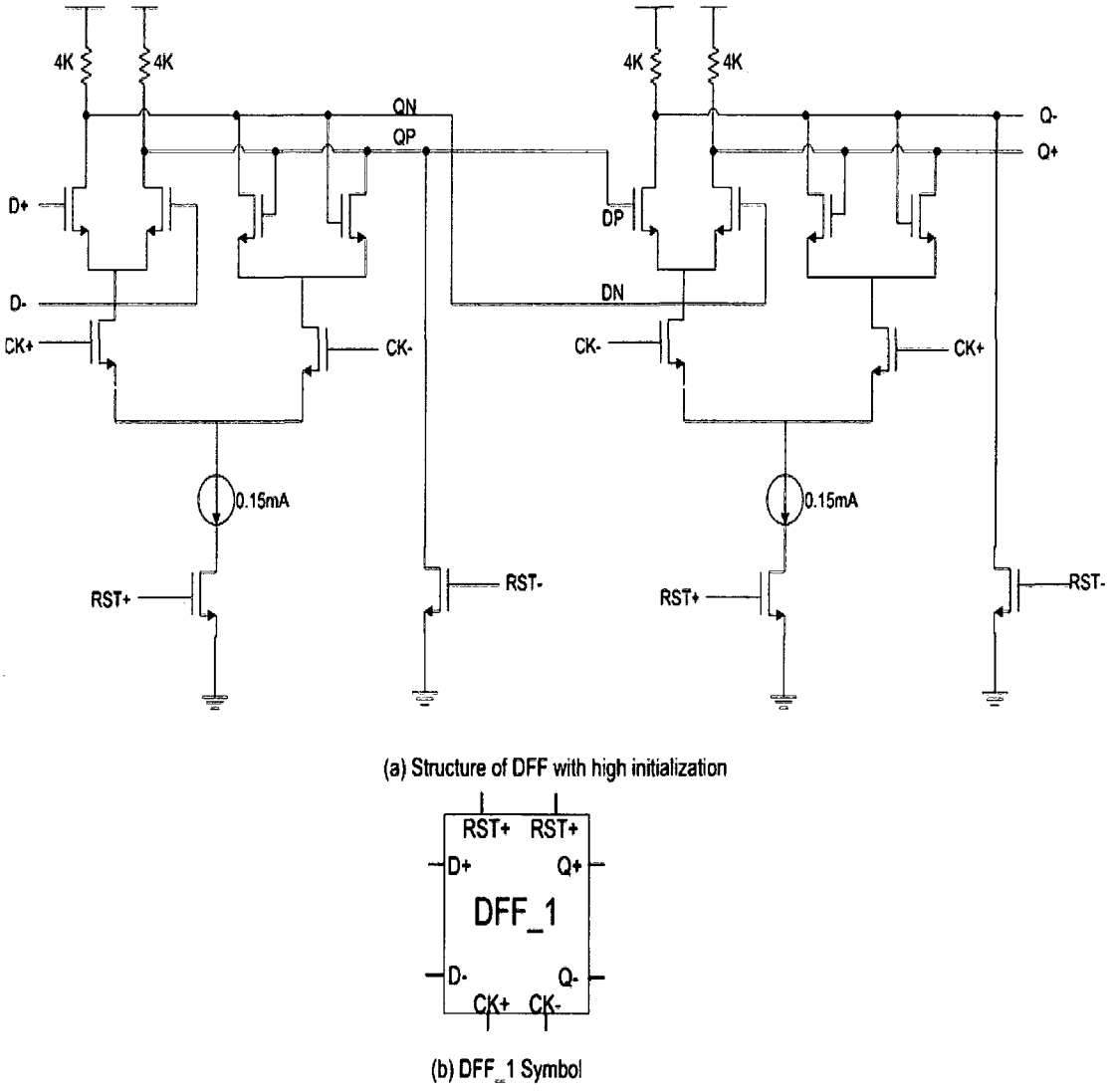


Figure 4.19 :Circuit and Symbol of DFF with high initialization

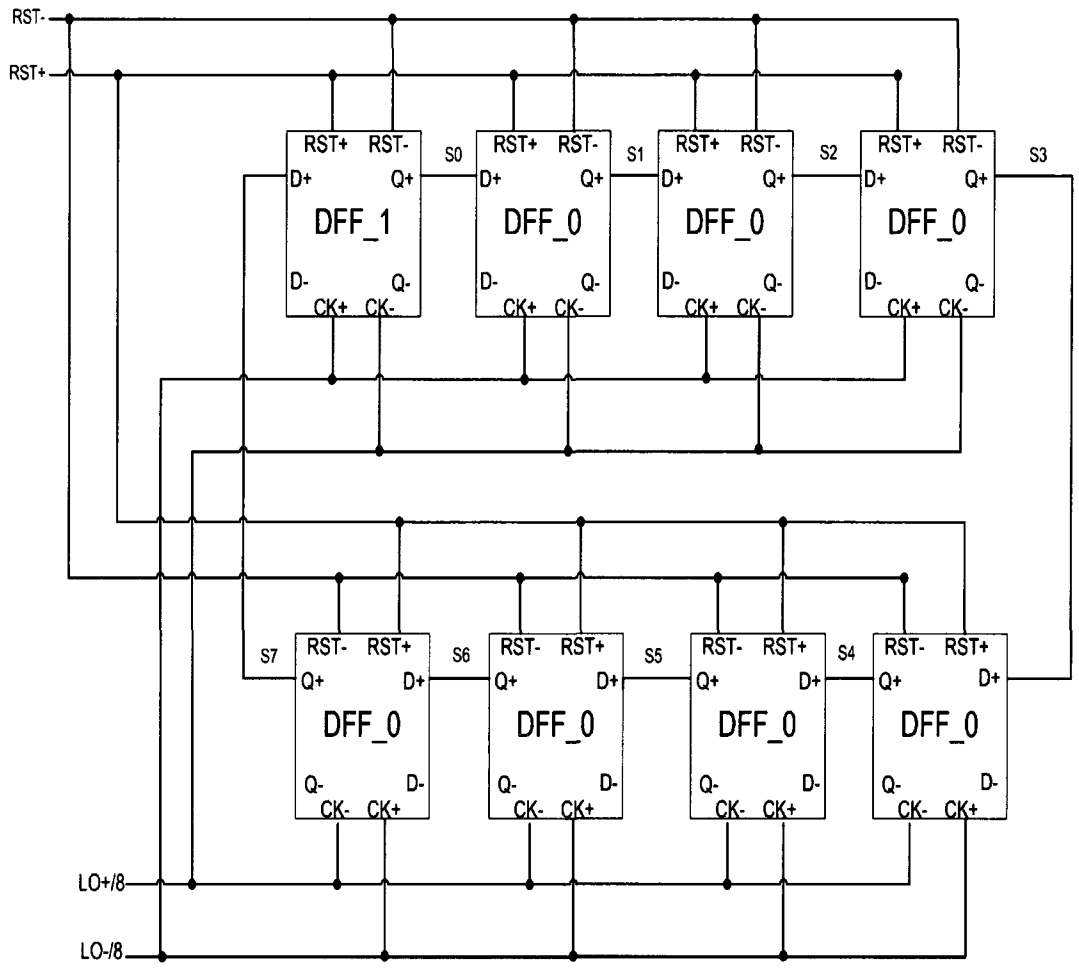


Figure 4.20 :Block Diagram of Shift Register

In addition, DCU signal RES can be created by applying for two output signals of 8-bit shift register S2 and S6 to an OR gate.

4.3.5 DCU Simulation Results

The simulation results of DCU are shown in Figure 4.21 and Figure 4.22. All simulation results are obtained by using the spectreRF simulator to simulate the 0.18um CMOS technology design.

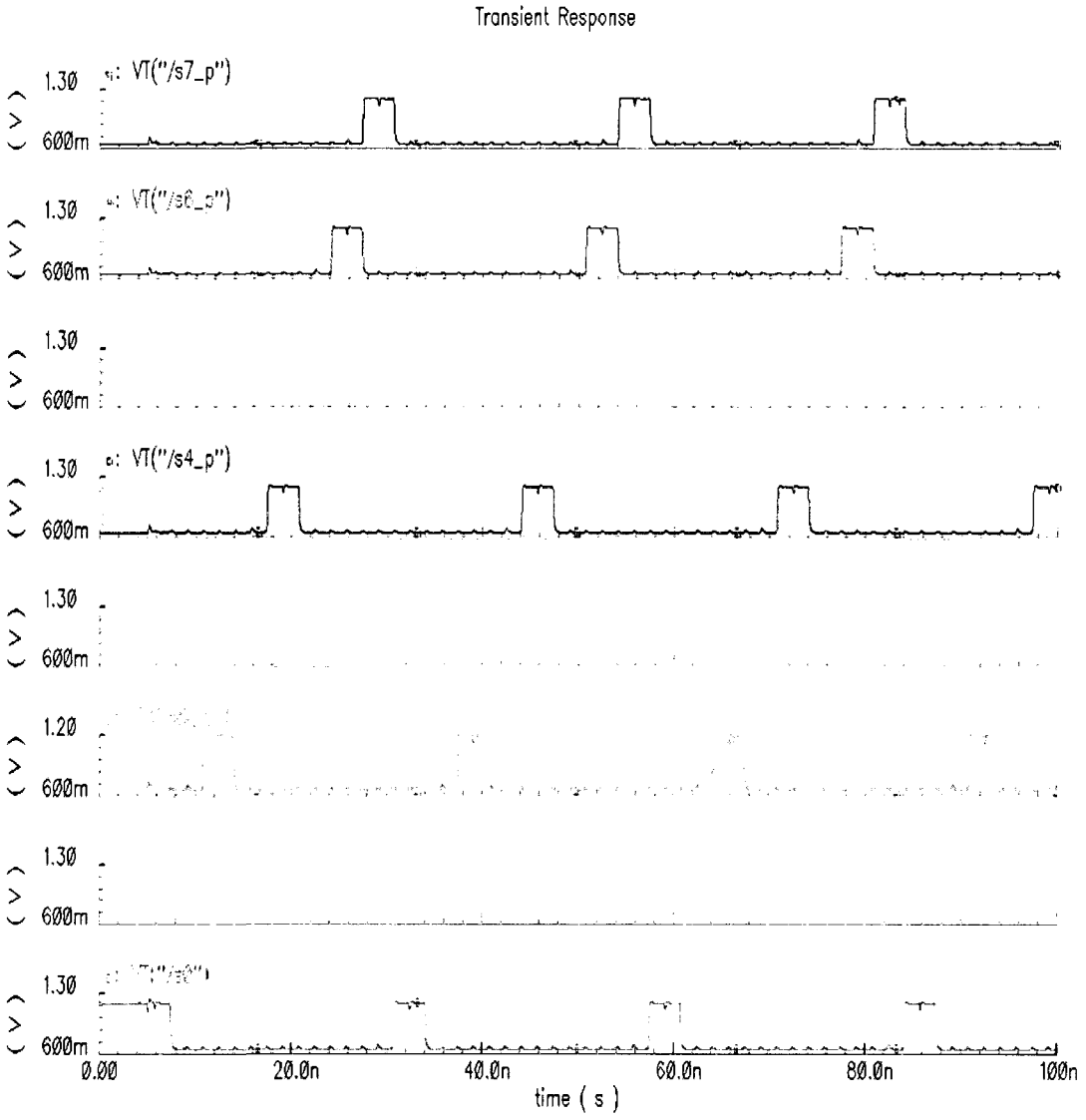


Figure 4.21 :Simulation Results of "one-hot" signals

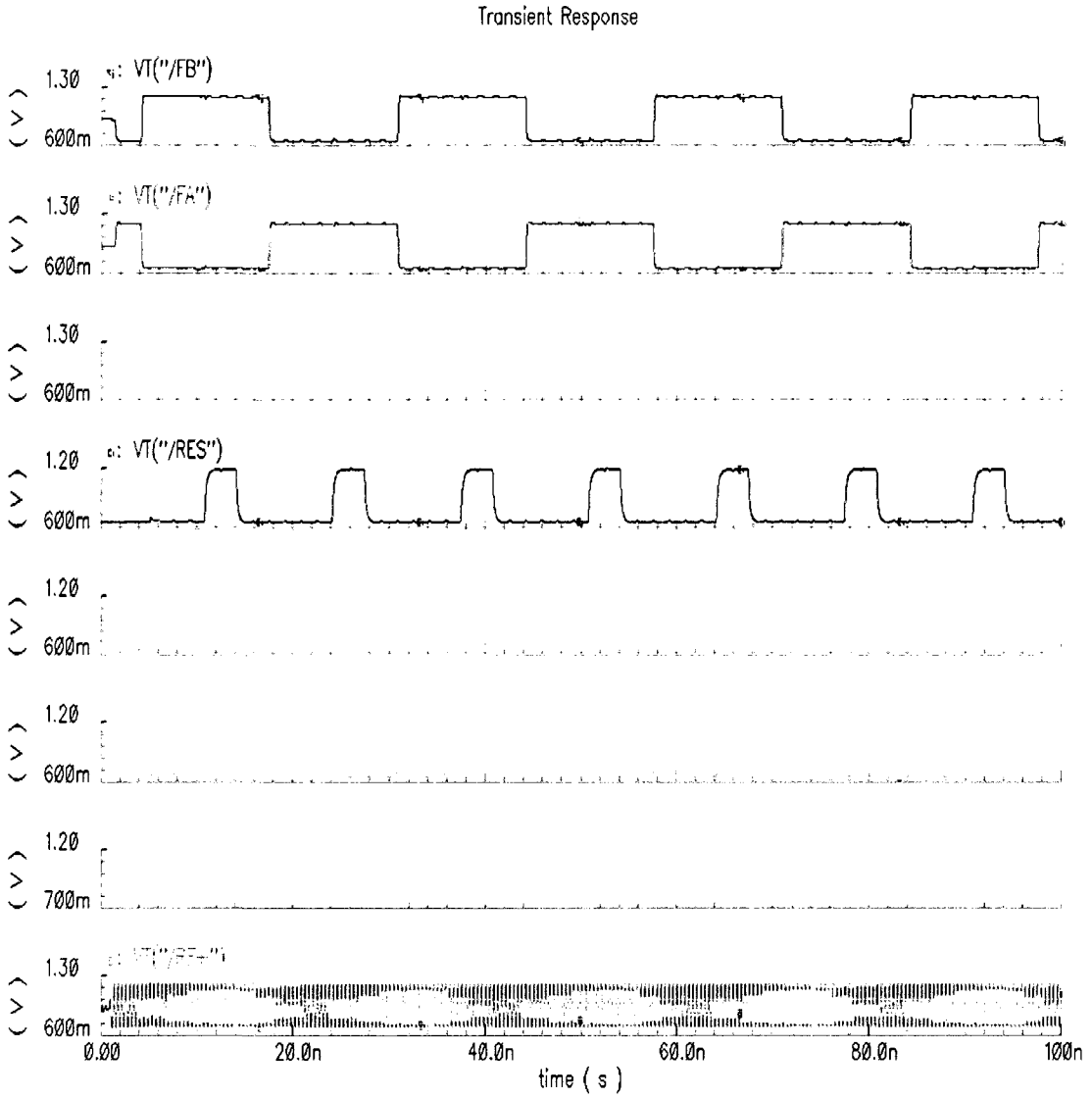


Figure 4.22 :Simulation Results of DCU signals

DCU output signal voltage versus time simulation are shown in Figure 4.21 and Figure 4.22. Based on simulation result in Figure 4.21, 8 DCU output signals from S0 to S7 are "one-hot" signals. Signal SAZ and SBZ have reverse relationship based on simulation result in Figure 4.22, similarly signal FA and FB also have reverse relationship.

4.4 Multi-tap Direct-sampling Mixer

Subsampling mixer architectures have been demonstrated in the past, but they suffer from noise folding and exhibit sensitivity to clock jitter of local oscillator (LO). Multi-tap Direct-sampling mixer is based on direct sampling technique which not only significantly reduces those effects, but also achieves great selectivity right at the mixer level. The selectivity is digitally controlled by the LO clock frequency, decimation ratio and capacitance ratio. In addition, the direct RF sampling technique uses current sampling to simplify the mixer circuit design. The effects of the MOS transistor sizing and settling on the mixer performance are not as relevant here as when using voltage sampling techniques. The charge injection and clock feedthrough simply exhibit themselves as a dc offset, which is removed by the feedback path [6].

4.4.1 MTDSM Design

As shown in Figure 4.2, the MTDSM comprises of switched capacitors that receive control signals from the DCU which generates clocks for MTDSM. There are two banks of rotating capacitors C_R and each bank consists of four C_R. The rotating capacitor is used to sample the RF input signal together with a large history capacitor C_H. For every eight LO cycles, one out of four rotating capacitors in one bank samples the RF input together with C_H, the remaining rotating capacitors in the bank disconnect from C_H. Meanwhile all four rotating capacitors in another bank are charge shared with the buffer capacitor C_B. After the charge sharing is finished, all four rotating capacitors in the bank are reset by discharging and then precharged to a desired voltage by charge-sharing with a feedback capacitor C_F. During this time, input RF samples are accumulated on the capac-

itors in the other bank of rotating capacitors and the history capacitor C_H. Therefore, the transconductance amplifier (TA) experiences a constant load at its output which is equal to C_H plus one C_R.

From the analysis in Chapter 3, one can know that the operation of sampling the input RF signal for eight cycles on C_H and C_R creates a sinc filter. The sinc filter has notches located at integer multiples of f_{LO}/N, where f_{LO} is the frequency of local oscillator and N is decimation ratio. Since f_{LO} is 2.4GHz and N is equal to 8, one can determine the first notch of the sinc filter is 300MHz. The sinc filter can be used as anti-aliasing filter to remove high frequency components and reduces the effect of noise folding. When C_R is disconnected from C_H, charge sharing occurs and each capacitor takes away charge proportional its capacitance. C_H is never discharged and retains a charge in proportion to the ratio α_1, where $\alpha_1 = \frac{C_H}{C_H + C_R}$, C_R stores 1-α_1 of total charge. This creates an IIR filter where the pole is ideally determined by the following equation:

$$f_{c1} = \frac{1}{2\pi}\frac{f_{LO}}{N}\frac{C_R}{C_H + C_R}$$

where f_{LO} is the frequency of local oscillator, N is the decimation ratio. However, the parasitics at the output of LNTA affect this pole and a careful design is required. The DCU timing signals S0 through S7 perform the rotation for sampling operation.

Similarly, the second sinc filter can be found in the readout operation that all the four rotating capacitors C_R in a bank charge-share with C_B. Combining the charge is an accumulation process and creates a sinc filter. The sinc filter has notches located at integer multiples of f_{sample}/N, where f_{sample} is 300MHz and N is decimation ratio 4. The first notch of the second sinc filter is located at 75MHz. Simultaneously, charge splitting of all the four rotating capacitors C_R in one bank from C_B creates an IIR filter whose corner frequency is determined by the equation:

$$f_{c2} = \frac{1}{2\pi}\frac{f_{sample}}{N}\frac{4C_R}{C_B+4C_R}$$

where f_{sample} is 300MHz, N is decimation ratio 4. The readout operation is facilitated by the DUMP signal from the DCU. while SAZ or SBZ perform the combining of charge in a bank. After all four rotating capacitors in a bank are charge-shared with C_B, they are disconnected from capacitor C_B and discharged using the RES signal from the DCU. Following the reset, they are charge-shared with C_F such that the charge is redistributed according to the ratio $C_F/(4C_R+C_F)$.

Since the noise figure of the MTDSM is dominated by the size of C_R, C_R must be carefully chosen to acquire low noise figure. Capacitors C_H and C_B also need to be chosen appropriately to set corner frequency of the first and the second IIR filters. The value of capacitance of C_R, C_H, C_B and C_F are presented in the following table.

TABLE 4.5: Capacitor Value in MTDSM

Capacitor	Value(pF)
C_H	15
C_R	0.45
C_B	15
C_F	15

Since all the switches in MTDSM are implemented by nMos transistors, these are not ideal switches because of a parasitic resistance and capacitance. In order to reduce the parasitic resistance, we need to choose minimal length (0.18 μm) and large width, but parasitic capacitance increases with width and the performance of circuit degrades. In addition, there are charging and discharging operation in MTDSM, transistor width also needs to be chosen carefully to make sure a complete charing and discharing occurs. So, there is trade-off between parasitic resistance, parasitic capacitance, charging and discharging time constant.

All the clocks are derived from the LO, it eliminates clock jitter since all receivers require a mixer switch derived by the LO. Beyond this RF switch, the clock edge control only goes to the extent of ensuring nonoverlap of clocks and settling of signals.

4.4.2 MTDSM Simulation Results

The simulation results of MTDSM is shown in Figure 4.23 and Figure 4.24. All simulation results are obtained by using the spectreRF simulator to simulate the 0.18 um CMOS technology design. Step response simulation result is shown in Figure 4.23. Since the input of MTDSM is current, two ideal current sources were used to simulate two channels with 1MHz frequency spacing. One current source is set to 2.4005GHz, another is set to 2.4015GHz and LO is set to 2.4GHz. The amplitude of both current sources are set to 20 μA. This simulation is used to verify that this mixer circuit is working with great selectivity.

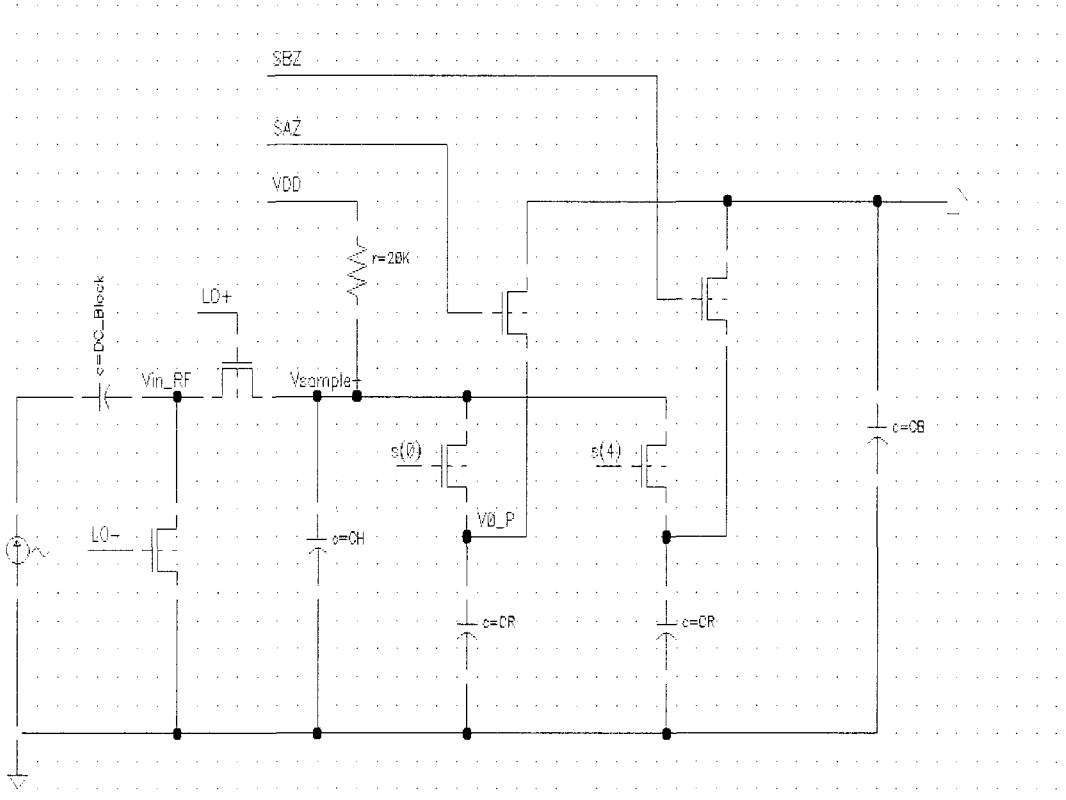


Figure 4.23 :Simplified Schematic of MTDSM

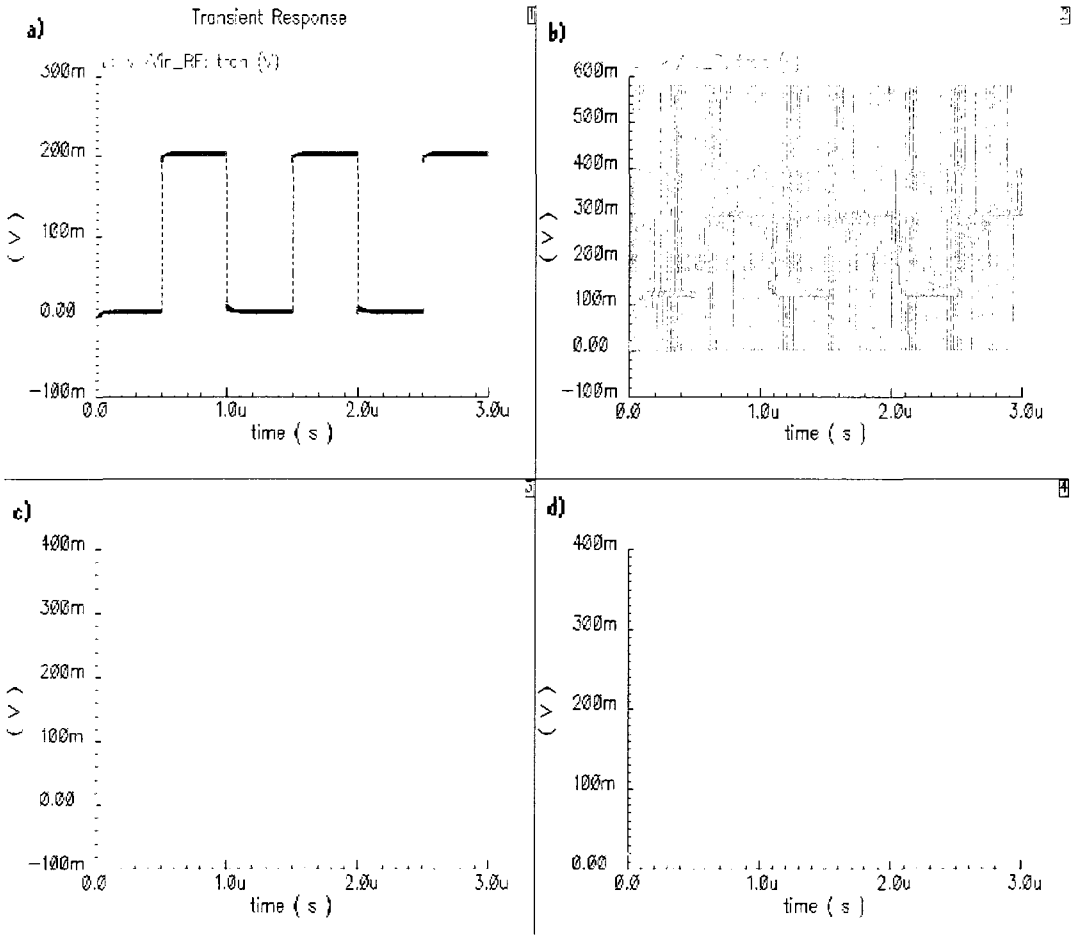


Figure 4.24 :Step Response of MTDSM

The simulation of Vin_RF voltage versus time is shown in Figure 4.24a, V0_P voltage versus time simulation is shown in Figure 4.24b. Vsample+ voltage versus time simulation is shown in Figure 4.24c, the simulation of IFOUT_P voltage versus time is shown in Figure 4.24d. Vin_RF, V0_P, Vsample+ and IFOUT_P can be found in Figure 4.23

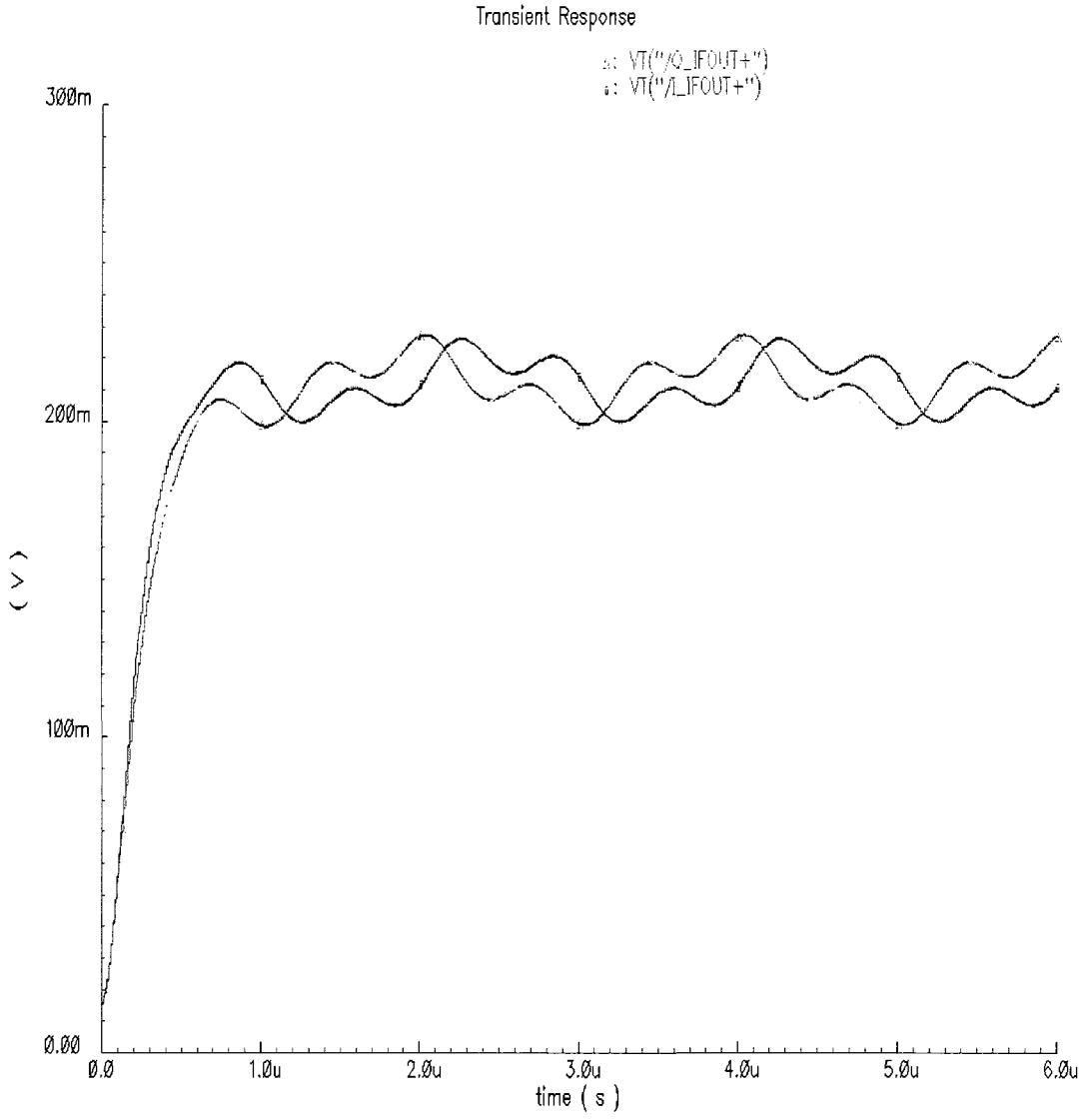


Figure 4.25 :Simulation Result of MTDSM

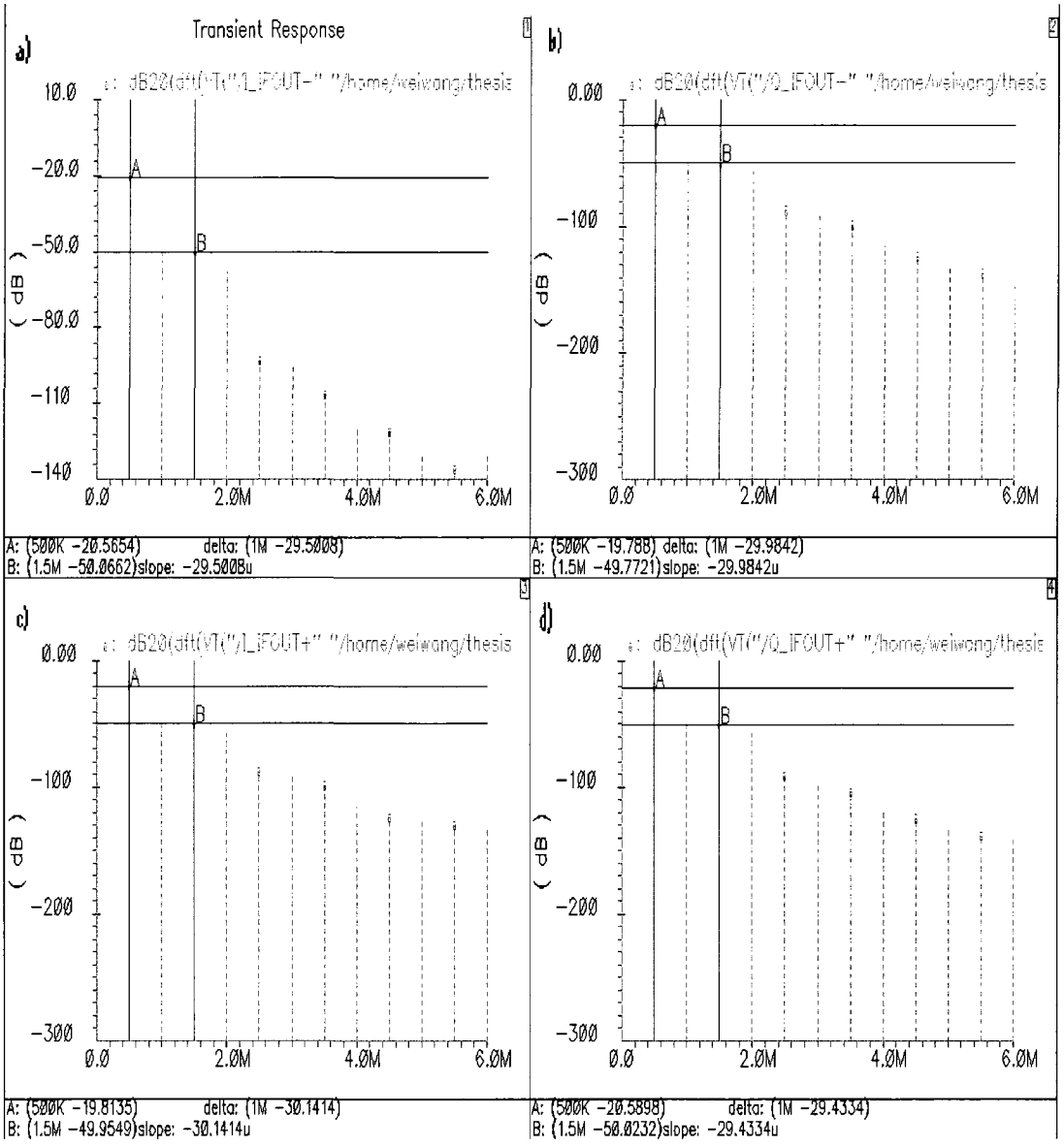


Figure 4.26 :Selectivity Simulation Result of MTDSM

The simulation of IF output voltage of MTDSM versus time is shown in Figure 4.25. MTDSM is implemented in differential and there are I and Q channels in RF front end, so there are four IF output signals: I_IFOUT+, I_IFOUT-, Q_IFOUT+ and Q_IFOUT-. The spectrum of these four IF output signals can be obtained by using DFT. The spectrum of signal I_IFOUT- and I_IFOUT+ are shown in Figure 4.26a and Figure 4.26c respectively. The spectrum of signal Q_IFOUT- and Q_IFOUT+ are shown in Figure 4.26b and Figure 4.26d respectively. Based on the simulation result in Figure 4.26, MTDSM can achieve about 30dB attenuation for adjacent channel, it can be used to partially select channel.

CHAPTER 5 *Layout and Measurement Results*

5.1 Introduction

The chip was fabricated in CMOS 0.18 μm technology and used a 80-pin Ceramic Flat Package (CFP). The test fixture for the 80-pin CFP is provided by the Canadian Microelectronics Corporation (CMC). This chapter describes the chip layout and test bench setup followed by measurement results. Unfortunately this front end design only partially worked. Failure analysis is included in this chapter.

5.2 Layout

The top-level circuit layout is shown in Figure 5.1. Individual layout for each block is shown in Appendix B. The total die area is $1495 \times 995 \mu m^2$. This chip has a total of 46 pads including five RF input pads and two RF output pads. One RF input pad is used for a 4.8GHz input signal (RF±LO) which has twice the frequency of LO clock and two input pads are used for differential LNA input signals (RFIN+ and RFIN-), two other input pads are used for differential TA input signals (TA+ and TA-). Two RF output pads are used to measure the LNA output signals (LNA+ and LNA-). In addition, there are four

output pads used to monitor the mixer output signals (IF+ and IF-) and Digital-Controlled Unit signals (DCU+ and DCU-). By doing this, it is possible to input an RF signal from the LNA and the TA independently.

There are several pads for bias input including LNA and DCU current bias and voltage bias forthe TA. There are five control signal input pads including IQCtrl, Ctrl1, Ctrl2, Ctrl3 and Ctrl4 used to control a DCU signal to be output. IQCtrl is used to control the I or Q channel of the DCU signals to be measured. Control signals Ctrl1, Ctrl2, Ctrl3 and Ctrl4 are used to decide which DCU signal is to be measured. The rest of the pads are used for supply and ground.

The supply and ground for all building blocks including the LNA, TA, mixer and DCU are separated in order to reduce noise coupling from the supply trace. In addition, a guard ring is added for each building block to increase isolation and to further reduce noise coupling.

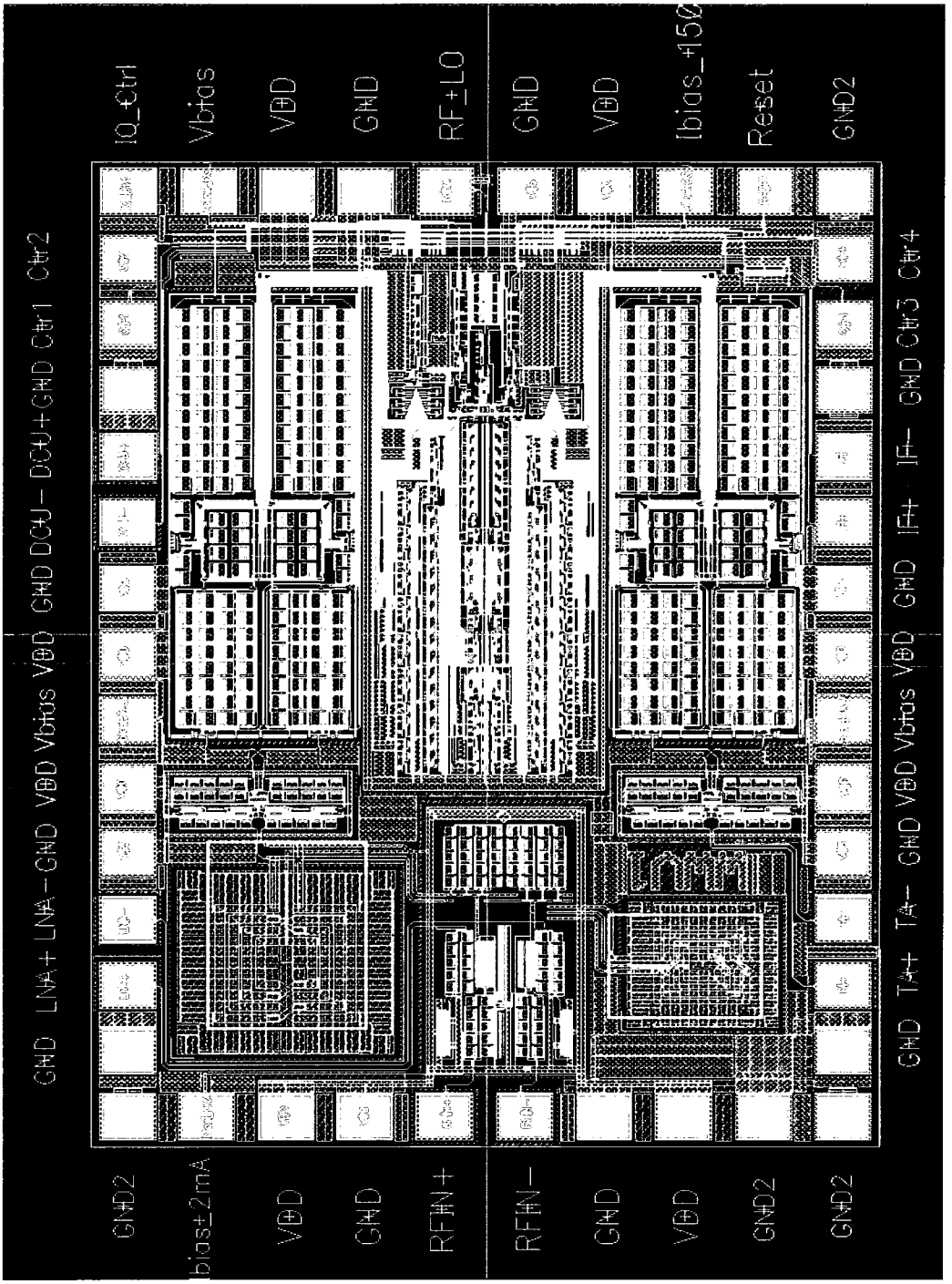


Figure 5.1 :Top Level Layout

5.3 Test Bench Setup

The test bench setup of the Direct RF sampling front end is shown in Figure 5.2 and the chip architecture is shown in Figure 5.3.

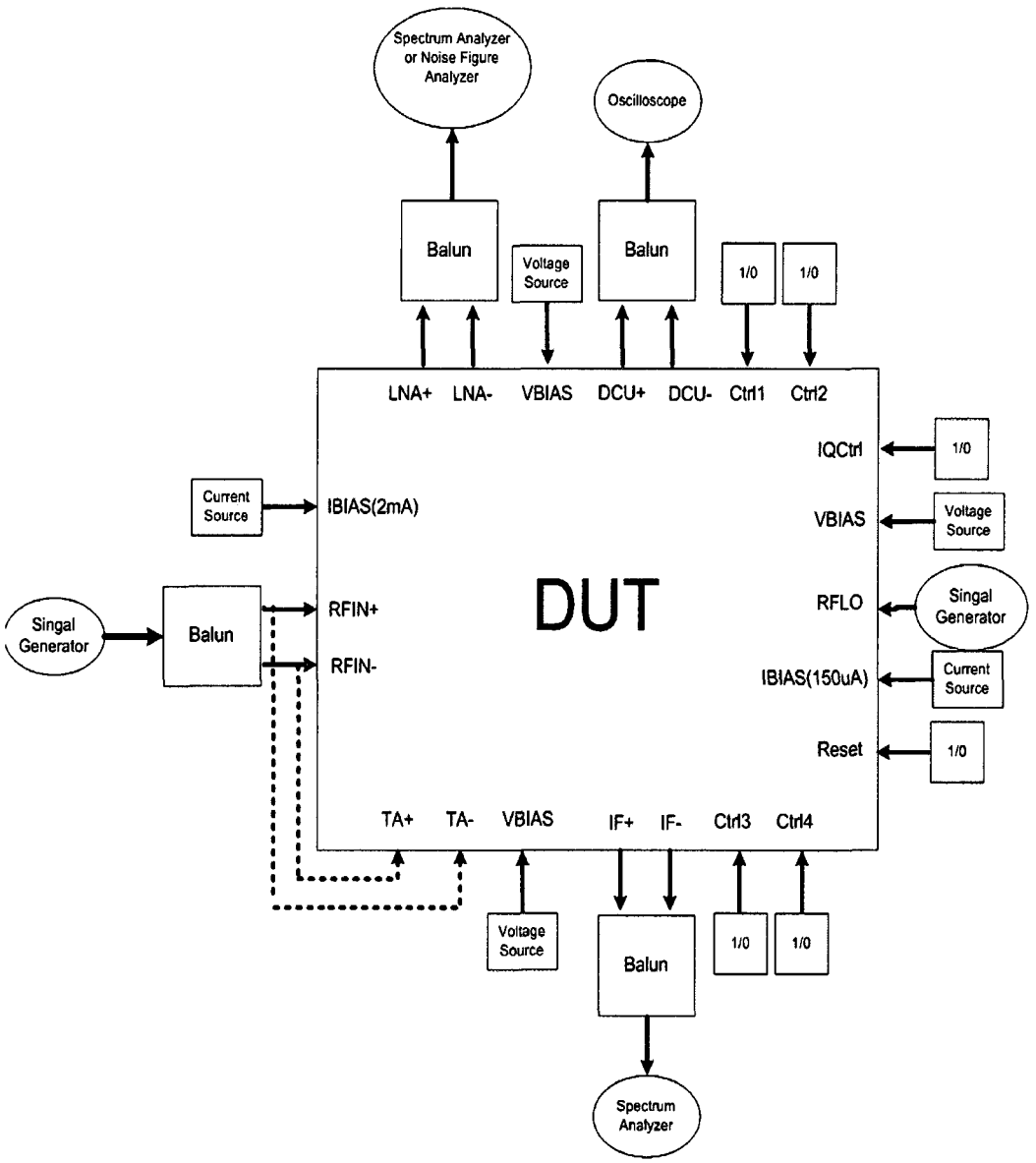


Figure 5.2 :Test Bench Setup

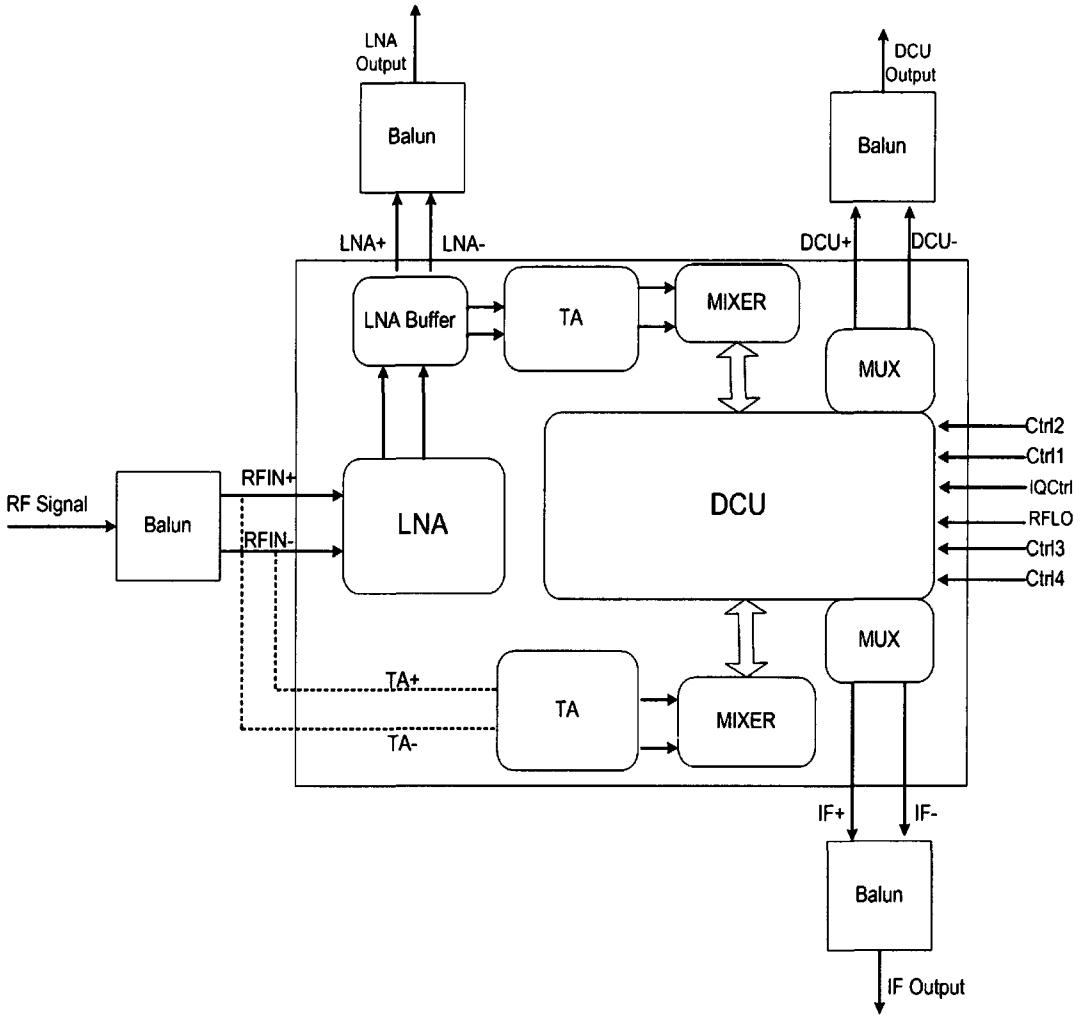


Figure 5.3 :Internal Architecture of Direct RF Sampling Front End

The external DC voltage and current supply provides the DC voltage and current to the chip including the power supply, bias voltage and bias current. The RF generator (ROHDE&SCHWARZ) is used to provide a single-ended RF input signal. A balun is used to translate a single-ended signal to a differential signal which is necessary for the Direct RF sampling front end. The LO signal is created by another signal generator. Five control

signals (IQCtrl and Ctrl1 to Ctrl4) multiplex the output signals due to a shortage of pins on the 80-pin CFP. IQCtrl selects either I or Q DCU signal to be output, the other 4-bits are used to select the DCU digital output to be measured. The Reset signal is used to initialize the 8-bit shift register to create "one-hot" signals. For each block, power supply and ground should be isolated.

5.4 Test Fixture

The test fixture for the 80-pin CFP is shown in Figure 5.4[16]. A clamp is used to fasten the chip to the board with 4 screws. The chip and the clamp must be carefully placed to ensure even pressure on all the pins of the chip and to ensure the successful connection between the chip and the printed circuit board.

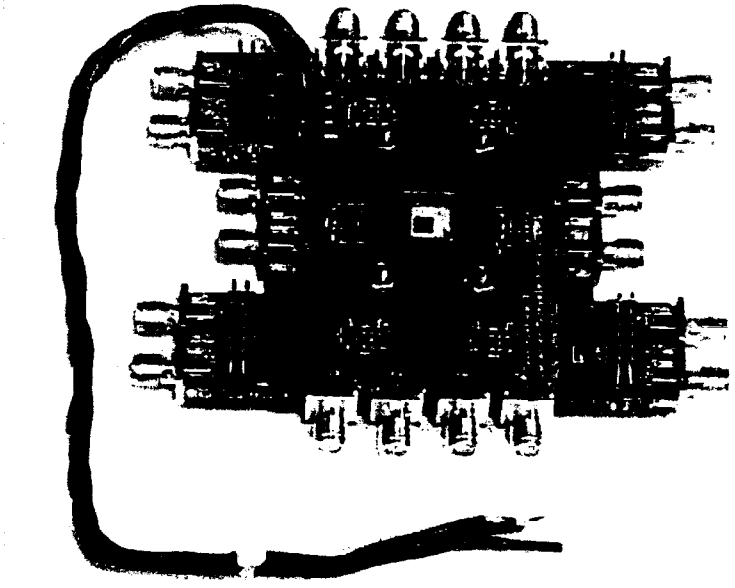


Figure 5.4 :Test Fixture CFP80TF with Clamped chip

5.5 Measurement Result and Analysis

5.5.1 Differential LNA Simulation Results

The first step is to test whether the differential LNA works properly. In order to improve measurement accuracy, cable loss and balun loss are checked first by comparing the difference between the signal generator setting and the measurement result of spectrum analyzer. The working frequency is supposed to be 2.4GHz, but actually power gain is quite low when signal generator is set to this frequency. By sweeping the frequency, maximal power gain is observed at about 2.0GHz, the maximal gain is 14dB which is 6 dB lower than simulation result. The noise figure is measured by noise figure analyzer (NFA). In order to obtain an accurate test result, the NFA needs to be warmed up at least one hour before testing. It must be mentioned here that the uncertainty of test result for the noise figure is 0.02dB. The measured noise figure of the LNA is 3.75dB which is worse than the simulation result of 1.70dB. The following table summarizes the measurement results.

TABLE 5.1: Measurement Summary of LNA

Test	Simulation Result	Measurement Result
Working Frequency(GHz)	2. 4	2. 0
Power Gain(dB)	20	14
Noise Figure(dB)	1. 70	3. 75

There is about 400MHz difference between measurement and simulation result. The possible reasons for this difference are: 1) There is no standard inductor library for 0.18 μm CMOS technology, ASITIC is used to design the inductor, but the model for inductor in ASITIC is not accurate enough. Inductance and parasitic capacitance are not very accurate, 2) The Diva extraction tool may be not accurate enough, the parasitic capacitance in LNA circuit is underestimated, 3) The parasitic capacitance of the interconnection trace is not considered in simulation.

The first reason as to why the power gain is 6dB lower than simulation result is that the quality factor of inductor is optimized for 2.4GHz. The ASITIC simulation result of quality factor is 9.5. With the working frequency set to 2.0GHz during measurement, the quality factor of inductor must be lower than the simulation result. As we know, the impedance of the LC tank at the resonant frequency can be obtained by the equation $Z_{LC\tan k} = Q\omega L$, where $\omega = 2\pi f$. The total impedance of the LC tank drops at a lower working frequency and lower Q, then power gain also drops with lower frequency and lower quality factor. If we assume that Q remains the same, the power gain will drop by 1.58dB when the frequency changes from 2.4GHz to 2.0GHz. The second reason for differing a power gain is that the input matching is optimized for 2.4GHz, but when the frequency changes to 2.0GHz, the matching becomes worse. A final contribution to power gain loss would be that the package together with the pads contribute gain loss due to parasitic inductance and capacitance.

The measured noise figure is 2.05dB higher than the simulation result. The possible reasons are: 1) Post-layout noise figure simulation result is normally higher than schematic simulation result due to the introduction of parasitic resistance after layout. The post-layout simulation result is 0.2dB higher than schematic result. 2) The isolation is not perfect between the LNA and the digital-controlled unit (DCU), this noise coupling boosts noise floor and increases the noise figure. 3) The package and the pads introduce gain loss, this gain loss means a higher noise figure result. 4) The LNA output buffer contributes more noise during measurement compared with the schematic simulation, since the power gain of the LNA is 14dB rather than 20dB. 5) A mismatch between two differential inputs also contribute noise since there is no perfect match between two inputs in practice.

5.5.2 *Differential Transconductance Amplifier*

There is no test output for this building block, but there are two differential inputs for this block. The purpose for adding two RF inputs for the differential transconductance amplifier is to make this chip more measurable. This chip can still be tested even if the LNA does not work properly. There is a shortcoming if the TA is used as an RF input, the input matching is not optimal due to the optimization of noise figure of the TA. Since the LNA works, it is not necessary to use the TA as an RF input.

5.5.3 *Digital Control Unit*

Digital Control Unit is used to produce the local oscillator (LO) and digital control signals for the direct RF sampling mixer. There are a total of 30 output digital signals from the DCU, but there are only two output pads (DCU+ and DCU-) to monitor these digital signals, so a test mux is used to choose which digital signal is to be selected. There are 5 control signals in the mux: IQCtrl used to select a signal for the I or Q channel, the other 4 control signals are used to choose which digital signal is to be selected. The selection of the DCU signal is summarized in Table 5.2.

TABLE 5.2: Summary of Signal Selection

Signal Name	Ctrl4	Ctrl3	Ctrl2	Ctrl1	Frequency relation with LO
S0	0	0	0	1	1/8
S1	0	0	1	0	1/8
S2	0	0	1	1	1/8
S3	0	1	0	0	1/8
S4	0	1	0	1	1/8
S5	0	1	1	0	1/8
S6	0	1	1	1	1/8
S7	1	0	0	0	1/8
SAZ	1	0	0	1	1/32
SBZ	1	0	1	0	1/32
RES	1	0	1	1	1/16
DUMP	1	1	0	0	1/16
FA	1	1	0	1	1/32

TABLE 5.2: **Summary of Signal Selection**

Signal Name	Ctrl4	Ctrl3	Ctrl2	Ctrl1	Frequency relation with LO
FB	1	1	1	0	1/32
L0	1	1	1	1	1

Since the LNA is working at 2.0GHz, the external LO frequency is set to 4.001GHz in order to obtain an IF at 500KHz. Due to the limited number pads for the DCU output, it is impossible to output all digital control signals at the same time to check their logic relationship. So, an oscilloscope was used to check the waveform and the frequency of DCU signals. From the oscilloscope waveforms, it was observed that the frequency of output signal was correct, but the waveform was not as good as expected, especially for the LO signal for the I and Q channels (2.0005GHz).

5.5.4 RF Front End Measurement

To check whether this RF front end works properly, the mixer output signal should be checked by a spectrum analyzer. As we know, low-IF architecture is adopted in this RF front end. The frequency of the IF is 500KHz. In order to obtain this IF, two signal generators are used to generate RF and LO signals with a 500KHz frequency difference.

Since the LNA has maximum gain at 2.0GHz, the frequency of one signal generator is set to 2.0GHz. The frequency of another signal generator is set to 4.001GHz, this external signal passes through a divide-by-2 device on the chip to create LO signals for the I and Q channels. If this front end works properly, one can find this IF signal by using a spectrum analyzer. Actually this IF signal could not be found from the spectrum analyzer. However the high frequency component (such as 4.001GHz, 2.0005GHz) can be found. It therefore appears that the sampling mixer did not work.

After analyzing the test results and comparing with layout/extracted simulation results, there are several possible reasons for failure. 1) The isolation was not good between the analog and digital blocks. 2) After checking the layout, it was found that routing between the LO clock and the RF sampling mixer was too long (over 1000um), there was a large associated parasitic capacitor and resistor. That could be the reason why the LO signals for the I and Q channels were not good and could not turn switch on or off completely, thus the sampling mixer did not work as expected. 3) The LO signal came from a signal generator and it was high frequency(4GHz). When this signal passes through the bond wire and pad, there was strong coupling, but the isolation was not sufficient for this strong signal. That was the reason why the high frequency component can be found in the spectrum. Although there are several possible reasons for failure, the second one must be considered the most important.

In order to prove this analysis, the parasitic capacitance and resistance of two long traces between LO clock and RF sampling mixer must be obtained and then added to the schematic for simulation. These two long traces were completed on top metal 6 with large width (10um) in layout. The extracted parastic resistance and capacitance was 11.6 Ohms and 502fF respectively. Apparently, the parasitic capacitance is quite large. In order to verify the effect of parasitic capacitance and resistance on LO signal, two simulations were run: 1) A transient simulation for the LO without parasitic capacitance and resistance, and 2) a transient simulation for the LO with the parasitic capacitance and resistance. For the second simulation, the parasitic resistance and capacitance were added in

the schematic of the multi-tap direct-sampling mixer(MTDSM) and a transient simulation was run. The two transient simulation results are shown in Figure 5.5 and Figure 5.6 respectively.

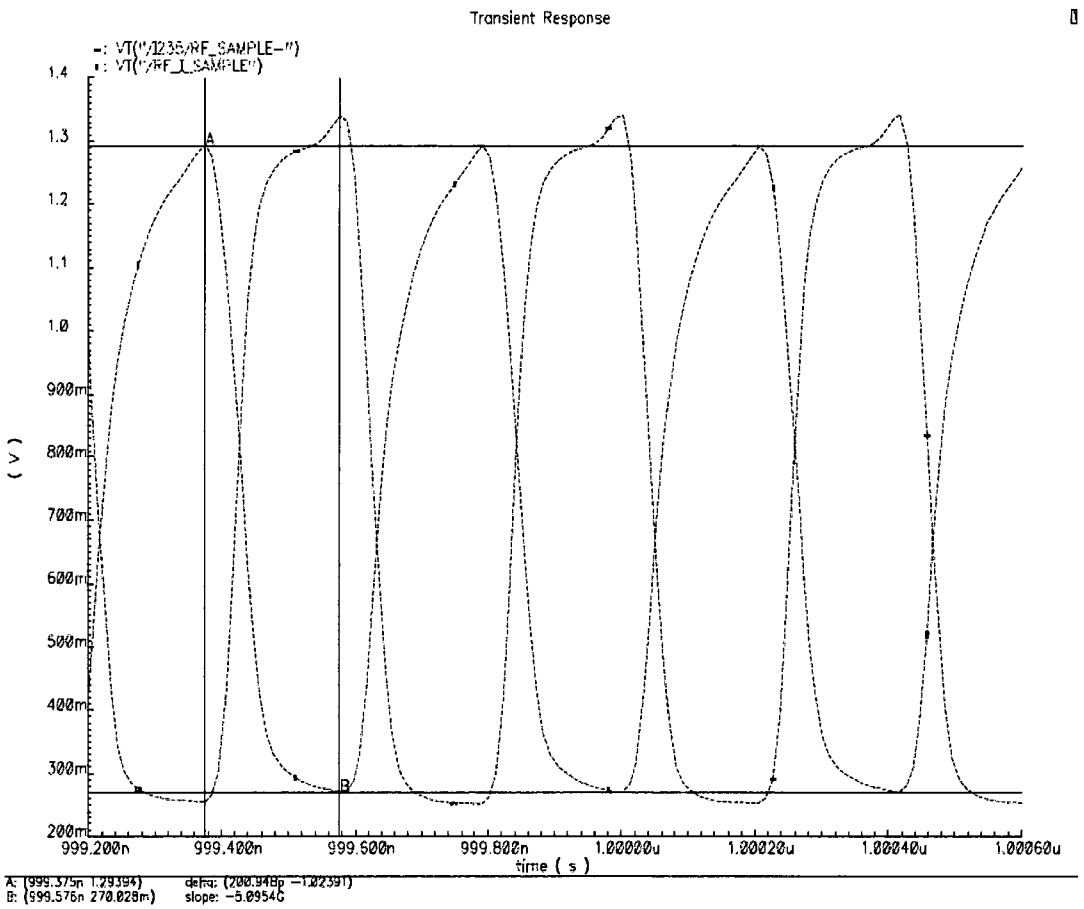


Figure 5.5 :Transient Simulaton for Sampling LO without Parasitic Capacitance

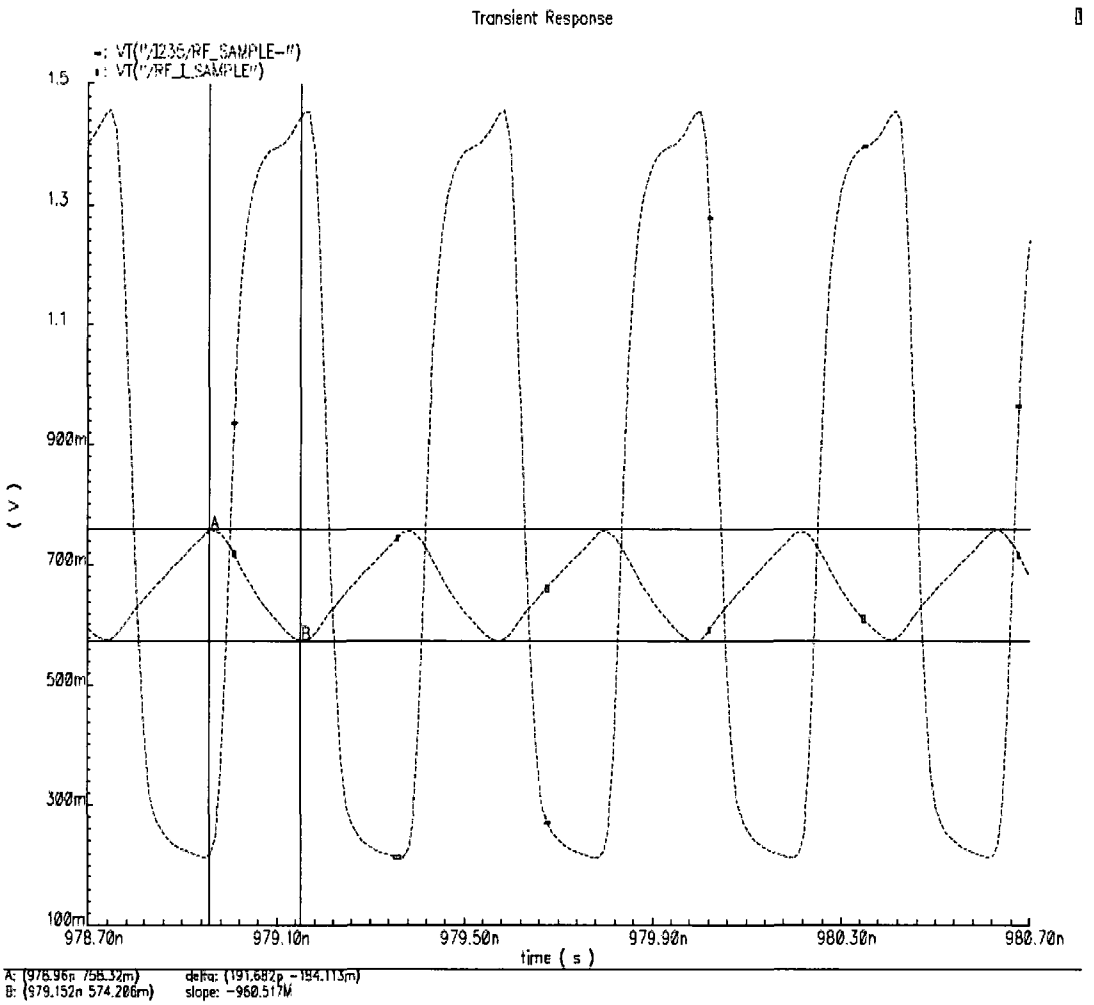


Figure 5.6 :Transient Simulation for Sampling LO with Parasitic Capacitance

Based on the simulation results in Figure 5.5 and Figure 5.6, it can be verified that parasitic capacitance has a large impact on the LO signal. After analyzing the circuit used to generate the LO signals, the reason was found as to why the large parasitic capacitance significantly changed the LO signals. Although a differential structure was used for all building blocks and circuits, there were no differential LO signals for the sampling mixer, actually only one of the differential LO output signals was used to sample the input differential RF signals in the I or Q channel. If parasitic capacitance was loaded on to one diffential LO signal which was used to sample the differential RF input signal and parasitic capacitance was not loaded on to the other LO signal, then the differential structure was changed to an unbalanced structure. The resulting voltage swing of the LO signal diminished dramatically if theassociated parasitic capacitance was large. The voltage swing of the sampling LO without parasitic capacitance was 1.024V based on the simulation result in Figure 5.5. The voltage swing of the sampling LO with parasitic capacitance was 184.11mV based on the simulation result in Figure 5.6. This sampling LO signal definitely can not turn on or off switch completely.

The IF output transient simulation was also rerun to check the effect of the parasitic capacitance. The frequency of the input signal was set to 2.4005GHz and the frequency of the LO was set to 2.4GHz. This simulation was used to verify how well the MTDSM can work with a large parasitic capacitance. After checking the output of the

sampling mixer, 500kHz signal was found at the output of mixer with an attenuated amplitude. The input RF signals and the IF output singal are shown in Figure 5.7 and Figure 5.8 respectively.

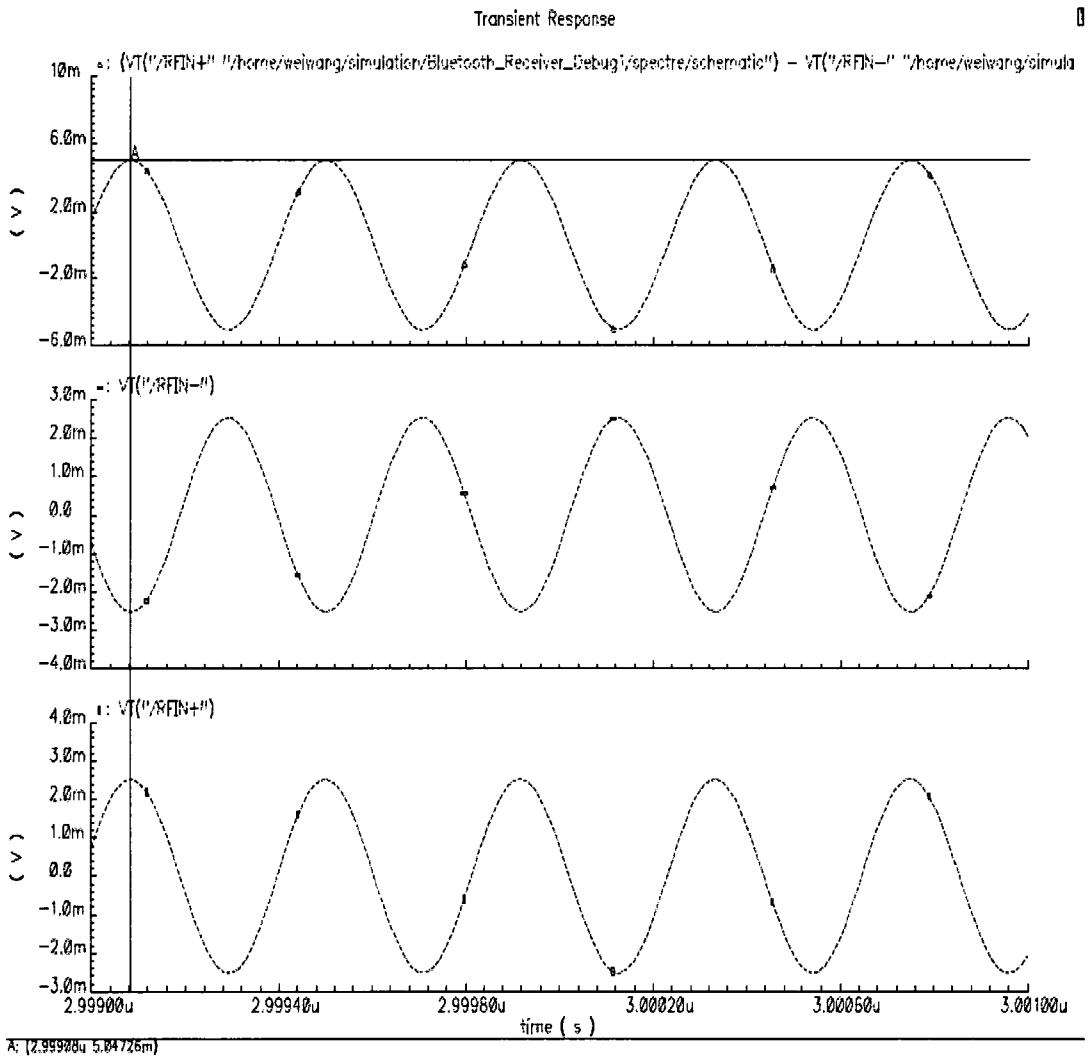


Figure 5.7 :RF Input Signal

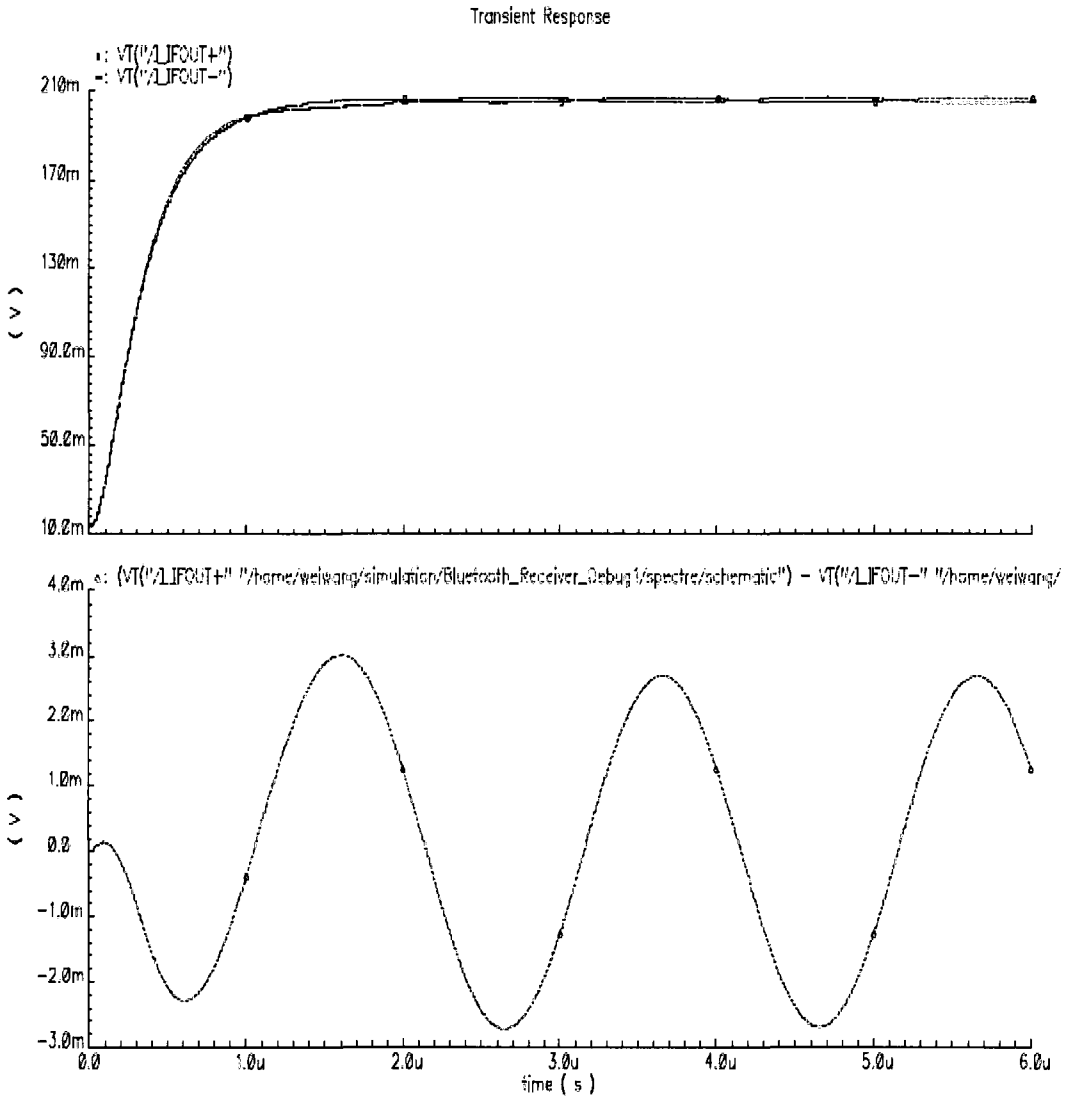


Figure 5.8 :IF Transient Simulation with Parasitic Capacitance

Based on the simulation results in Figure 5.7 and Figure 5.8, it shows that the Multi-tap Direct-sampling mixer(MTDSM) does not work well with a large parasitic capacitance. The MTDSM experiences a large attenuation instead of providing a voltage gain. The attenuation can be calculated on the basis of the simulation result. The peak voltage of input RF signal is 5.0mV. The peak voltage of the RF signal after the LNA increases to 50.0mV as LNA provides a 20dB gain. The peak voltage of the IF output signal is 2.7mV based on the simulation result in Figure 5.8. The attenuation observed was 25.35dB. This proves that a large parasitic capacitance makes the voltage swing of a sampling LO shrink and it therefore can not turn switch on or off completely. Since the frequency of the output IF signal is 500KHz and is very close to DC with respect to the RF input, if DC signal is strong and this IF signal is too weak, it is possible that one can not find the IF signal on the spectrum analyzer.

CHAPTER 6 *Conclusion and Future work*

6.1 Conclusion

The analog front end is the most critical part of the whole wireless receiver. Sensitivity and selectivity are the primary concerns in receiver design. Wireless communication standards become more complicated due to the lack of globally harmonized spectrum allocation. This has motivated researchers to look for multi-band mutli-standard solutions for the wireless front end. More efficient technologies need to be employed to meet this goal.

In Chapter 2 of this document, several architectures of wireless receivers were discussed including conventional heterodyne, zero-IF and low-IF structures. Integration level, power consumption and design issues associated with individual architecture are also presented. The reason why we choose the low-IF structure was explained in this chapter.

In Chapter 3 of this document, a fundamental design consideration of the direct RF sampling front end was discussed. The concept of the Windowed Integrated Sampler (WIS) was introduced and its transfer function was also derived. The details of the direct RF sampling mixer was explained by circuit analysis and the transfer function of a charge domain switched-capacitor filter was presented. The noise performance of a sampling

mixer was also presented, the estimated noise figure was calculated and guidance was given for choice of capacitance in the circuit.

In Chapter 4, the proposed direct RF sampling front end building blocks and simulation results were presented. In order to reduce sensitivity to parasitic capacitance and inductance, a differential structure was used in the circuit design of the LNA, meanwhile inductive source degeneration architecture was used to obtain a low noise figure. Noise performance and linearity are the most important parameters in the design of the transconductance amplifier (TA). Techniques used to improve linearity and reduce the noise figure were also presented. The direct RF sampling mixer circuit was presented in this chapter. The fundamental circuit D flip-flop was discussed for the design of a digital-controlled unit (DCU) with all control signals derived from the LO. A Direct RF sampling front end circuit was fabricated in 0.18 μm CMOS technology.

In Chapter 5, the setup of the chip test environment was described and measurement results are presented. Analysis of measurement results was also presented based on the simulation.

6.2 Future Work

An insufficient number of pins made the test and analysis of the direct RF sampling front end circuit inconvenient. Although we used a 80 pins test fixture, the lack of chip area limited the pin number to 46. In a future design, an 80CFP package with adequate number of pins could be chosen or some probe pins could be used to test and analyze the internal circuits. The best way could be to design a new test board for the chip. Furthermore, the gate inductor of the LNA can be fabricated on the chip if there is enough

space and this can reduce the number of external components and remove the off-chip matching network. In addition, the capacitance ratio can be adjustable if we add more control signals to the circuit. We can then use these control signals to test the performance of the charge domain switched-capacitor filter. The DCU circuit could be optimized to reduce power consumption.

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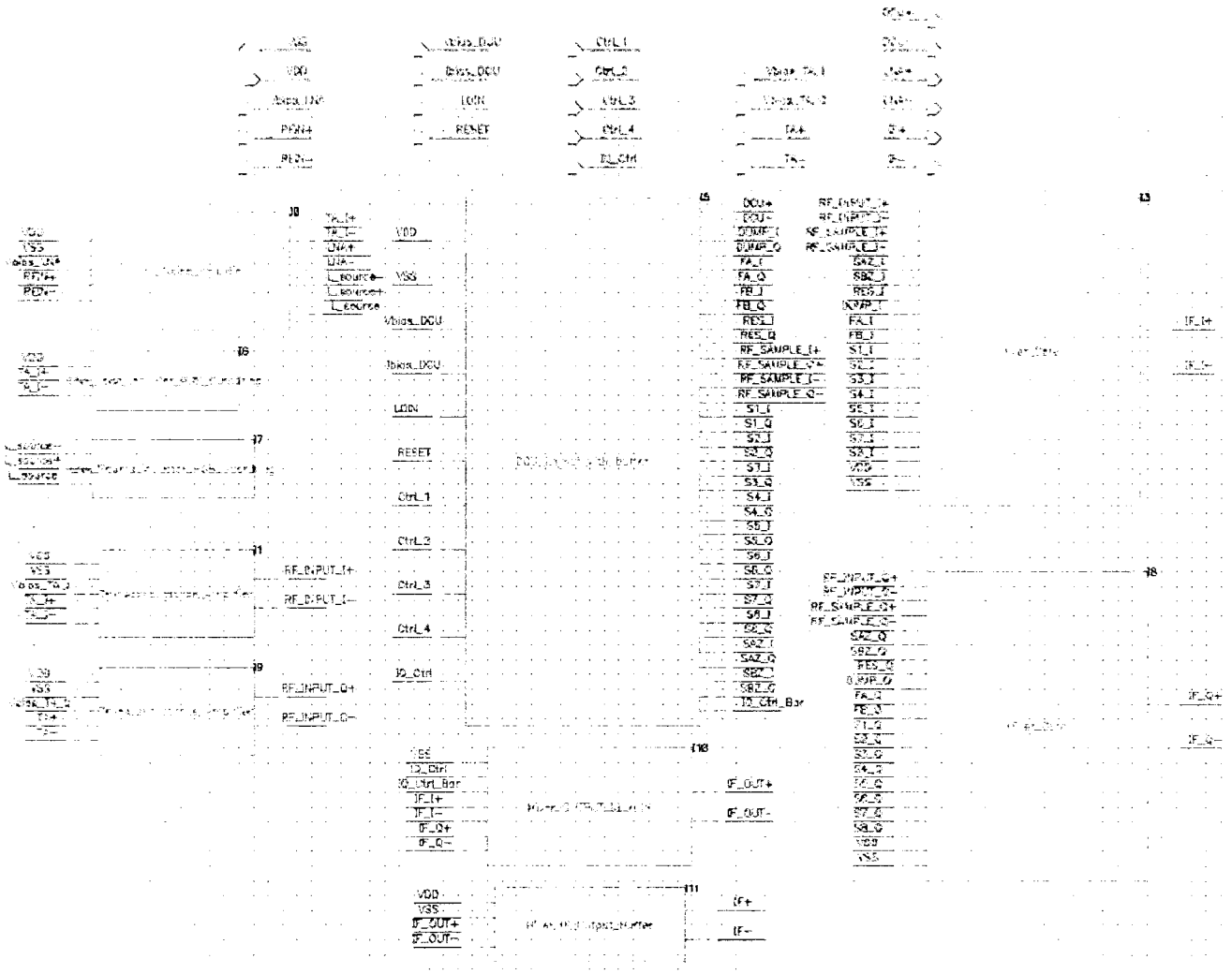
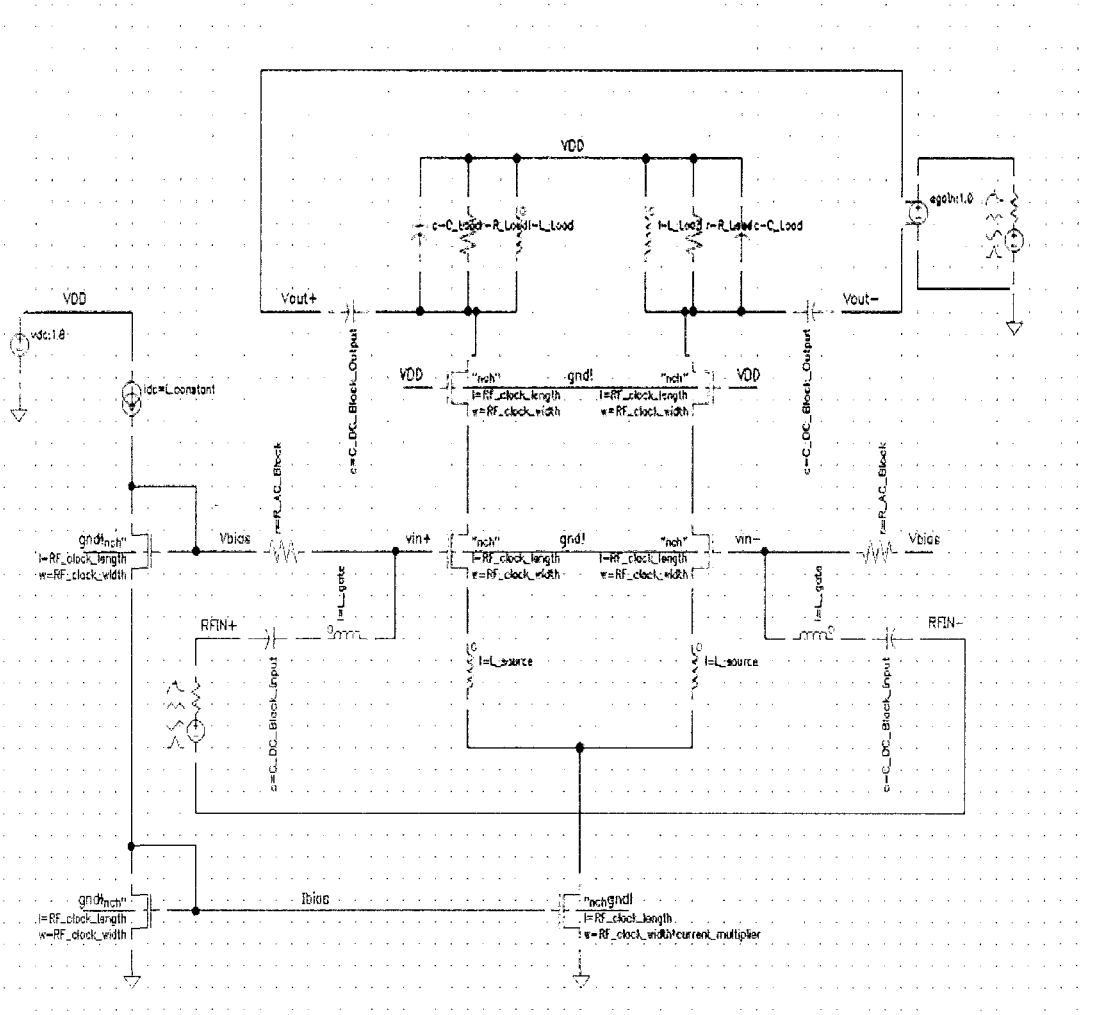
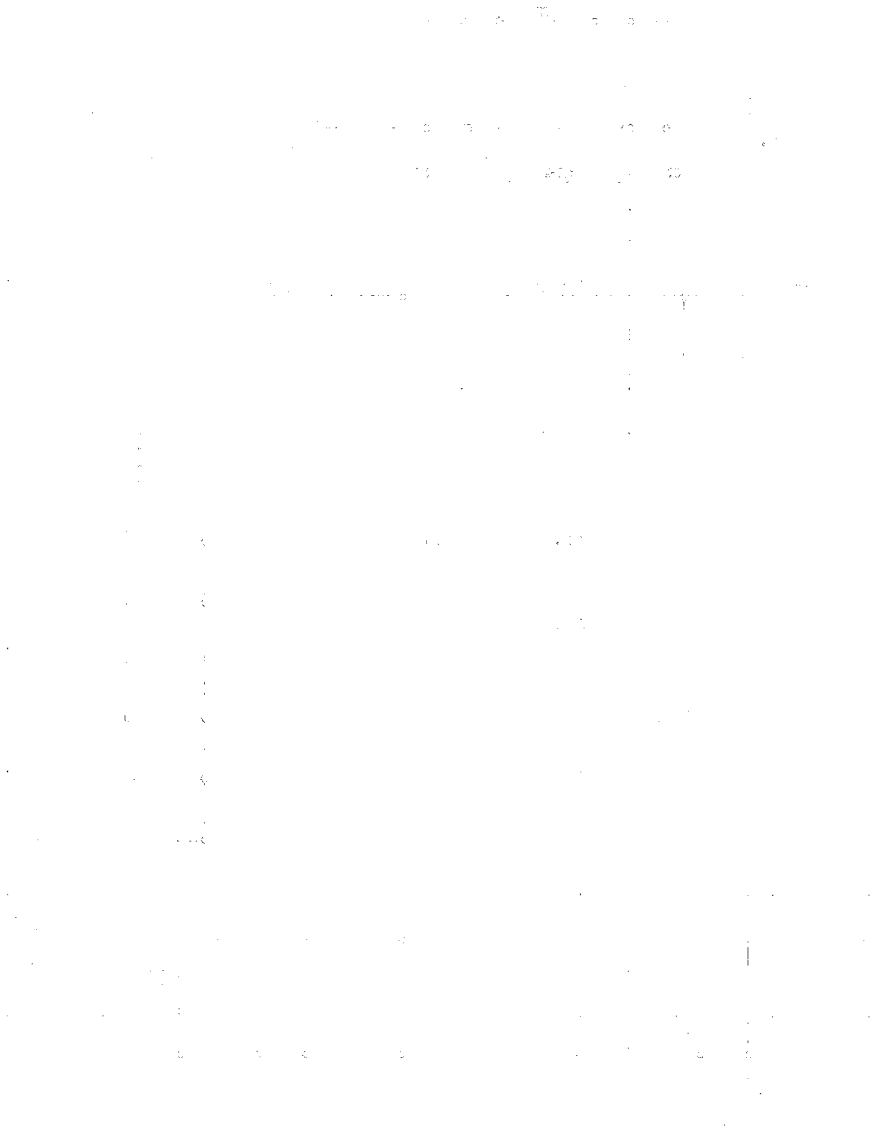
Appendix A: Schematic of Direct RF sampling mixer



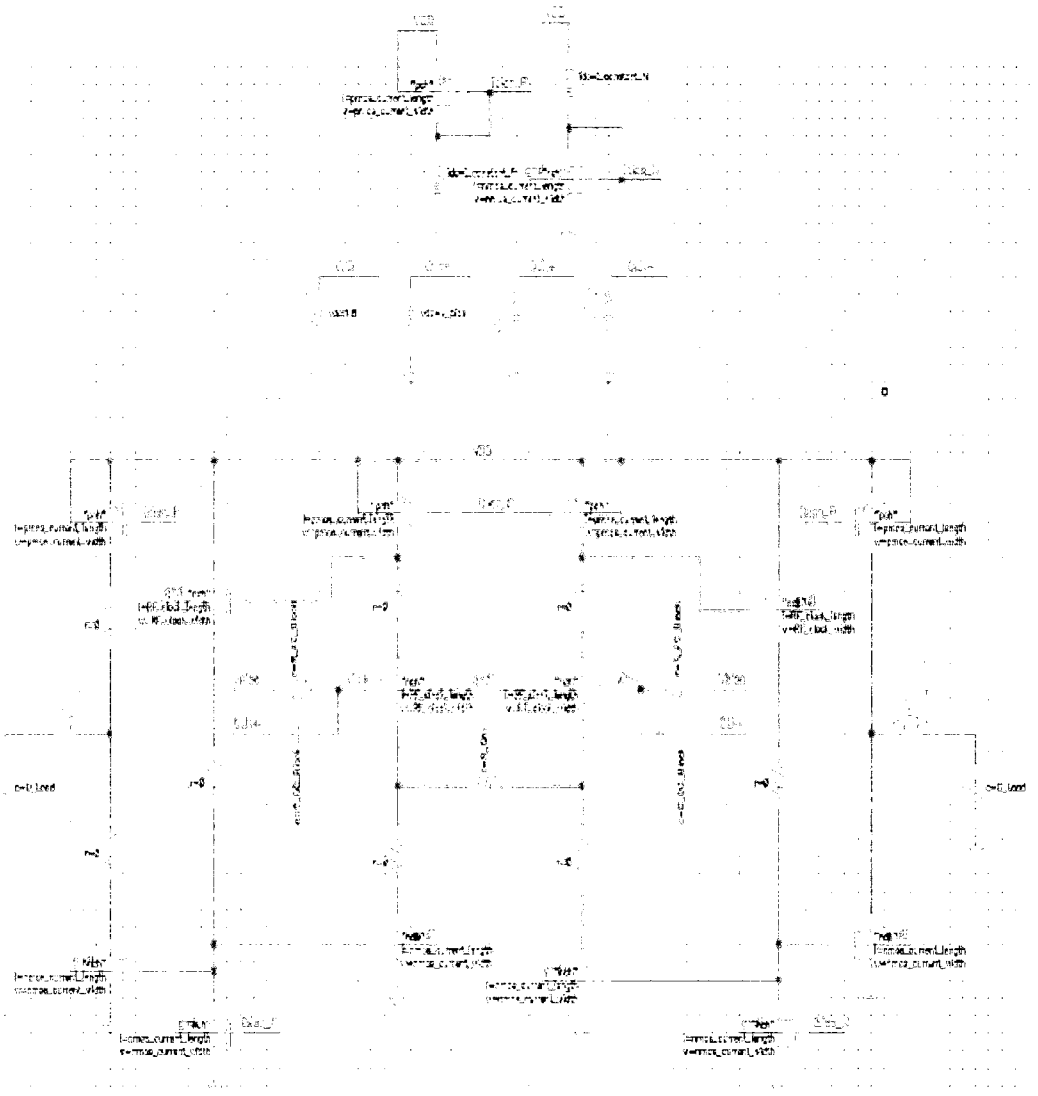
Appendix A.1: Block Diagram of Direct RF Sampling Front End



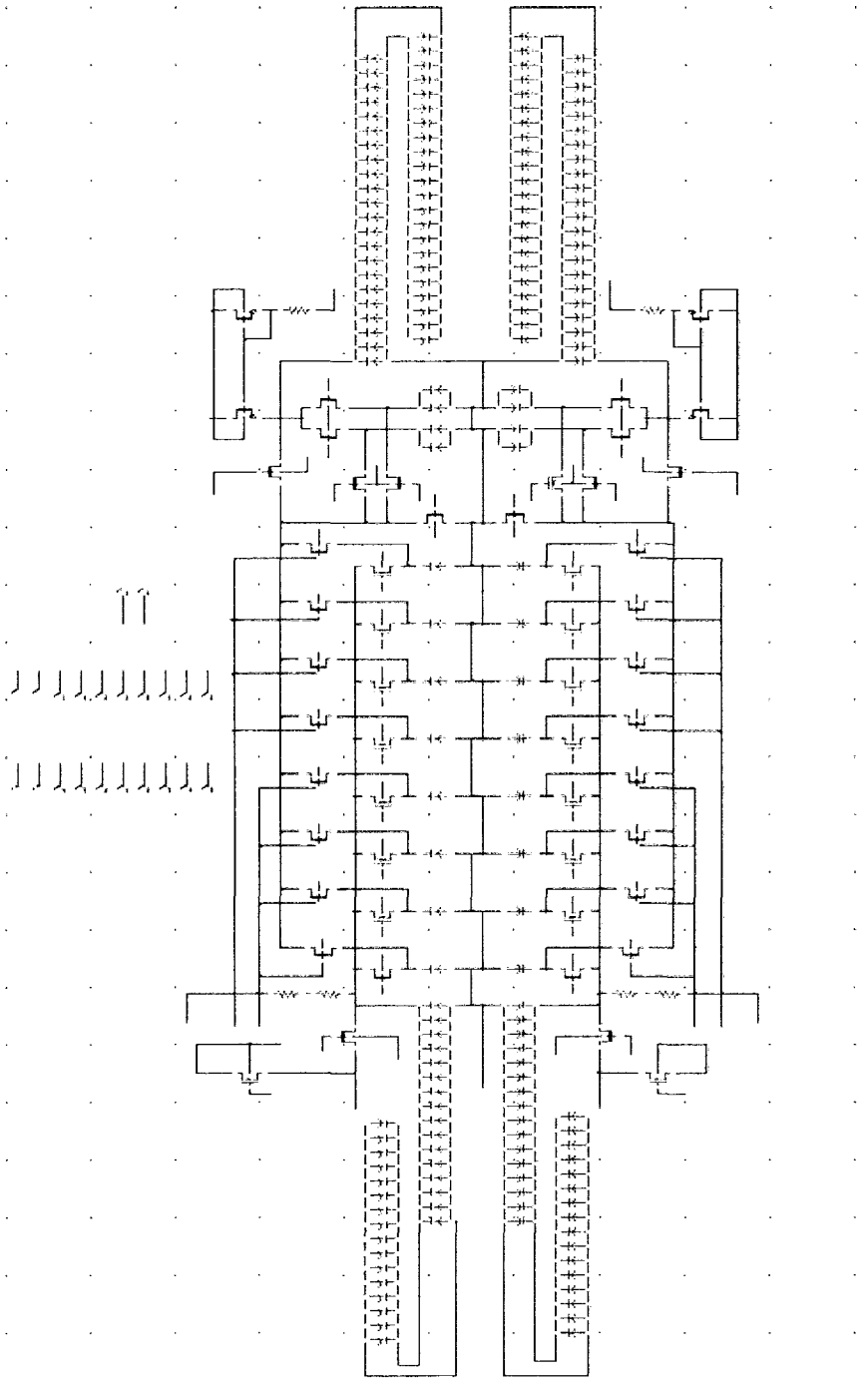
Appendix A.2: Schematic of LNA



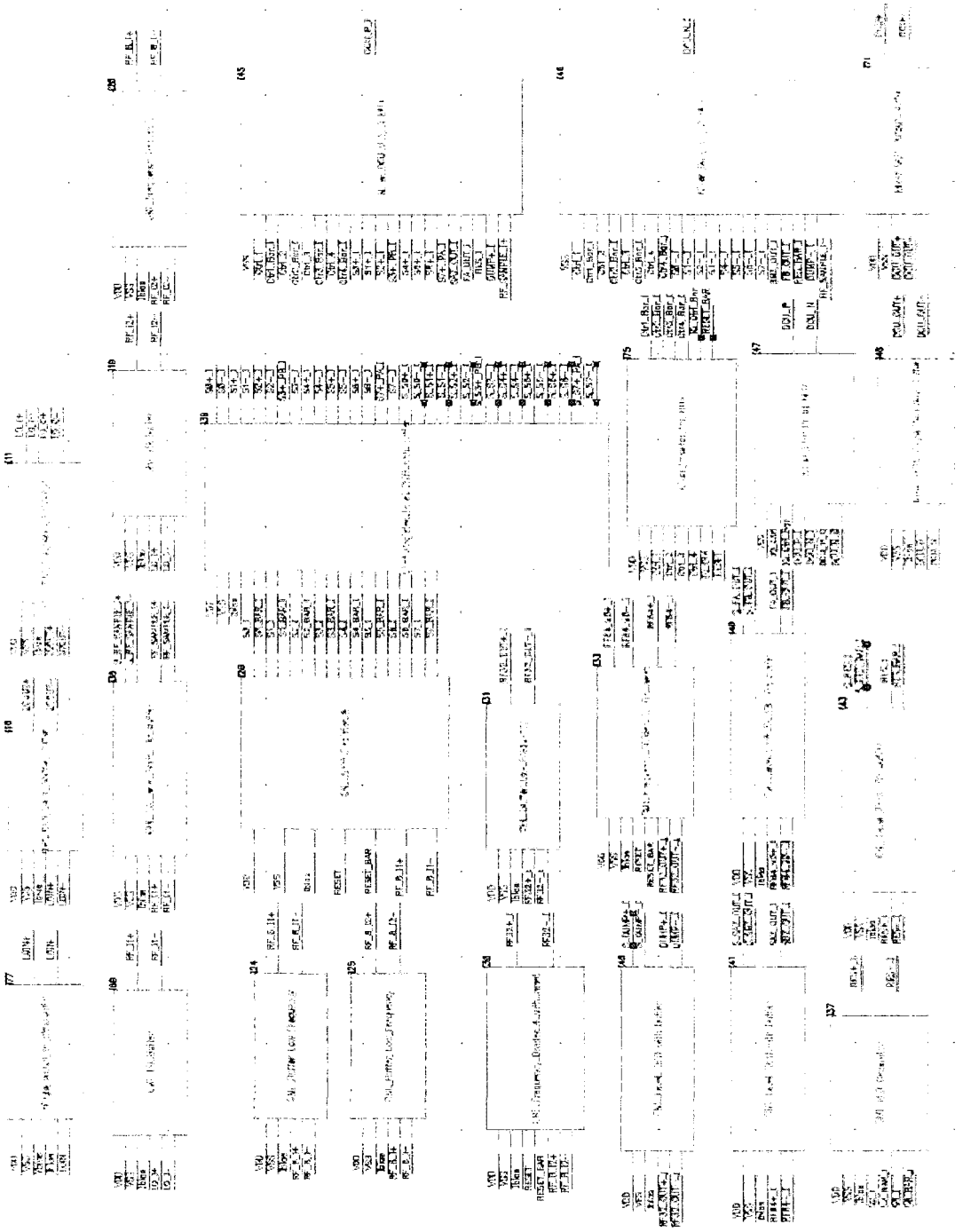
Appendix A.3: Schematic of LNA with package



Appendix A.4: Schematic of Transconductance Amplifier

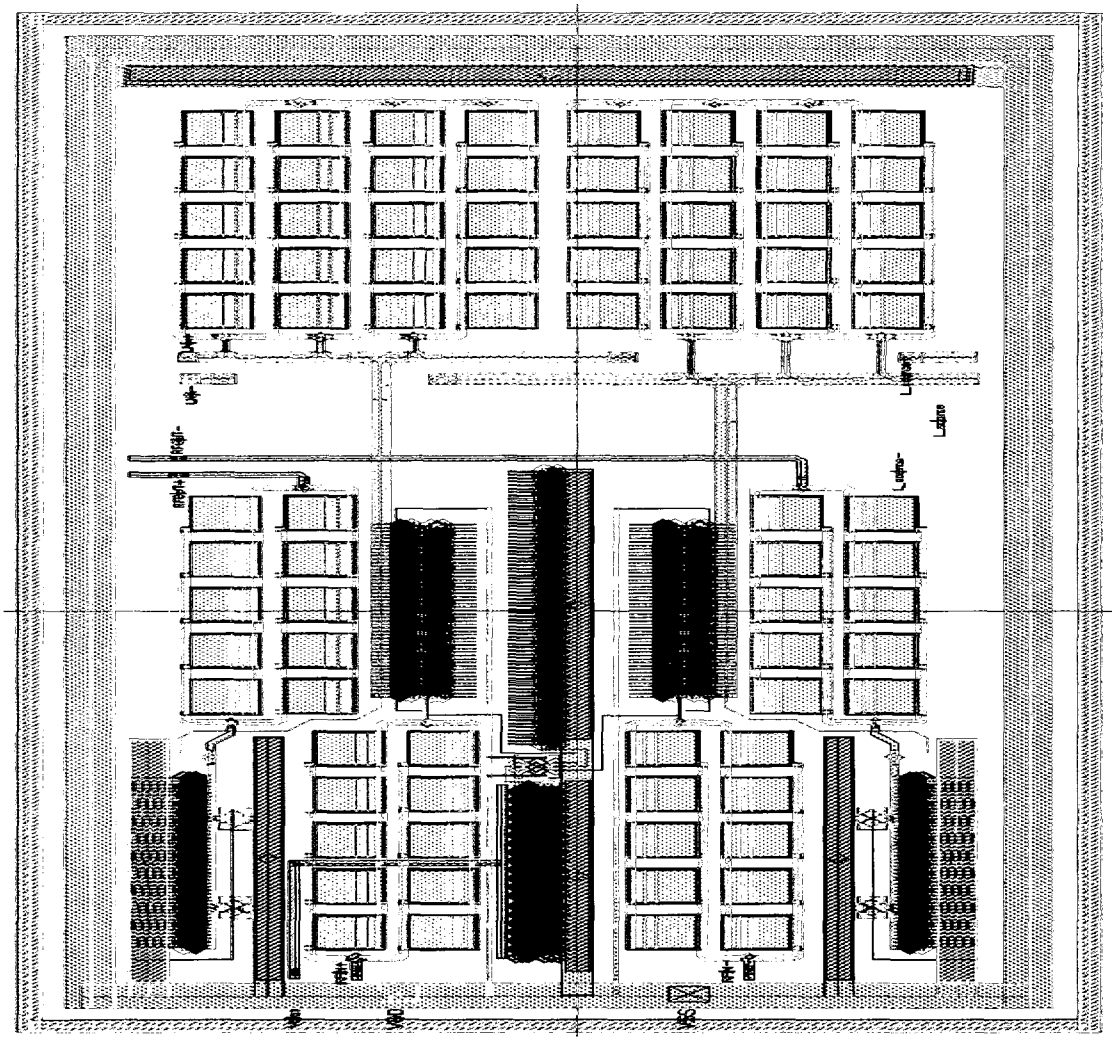


Appendix A.5: Schematic of Mixer

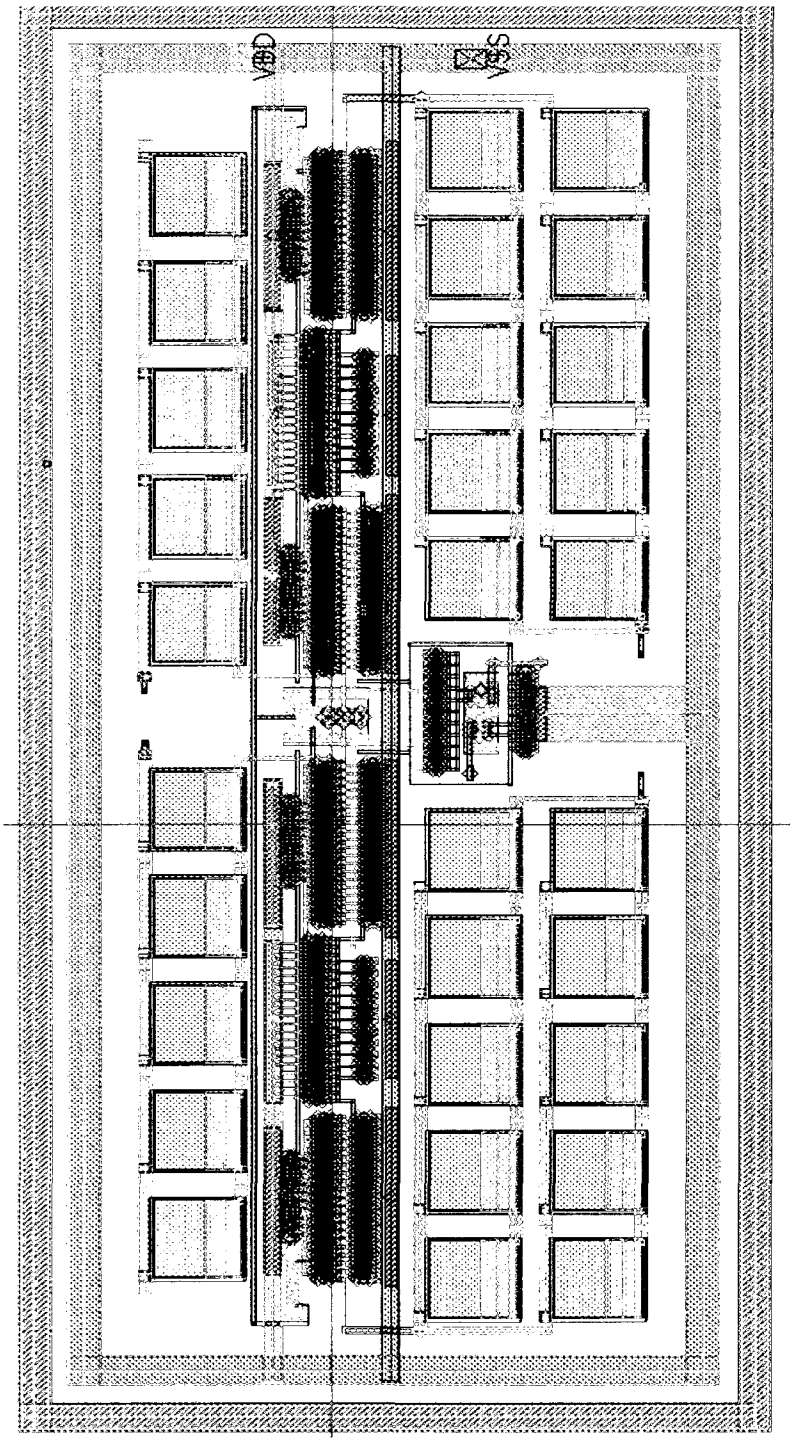


Appendix A.6: Schematic of DCU

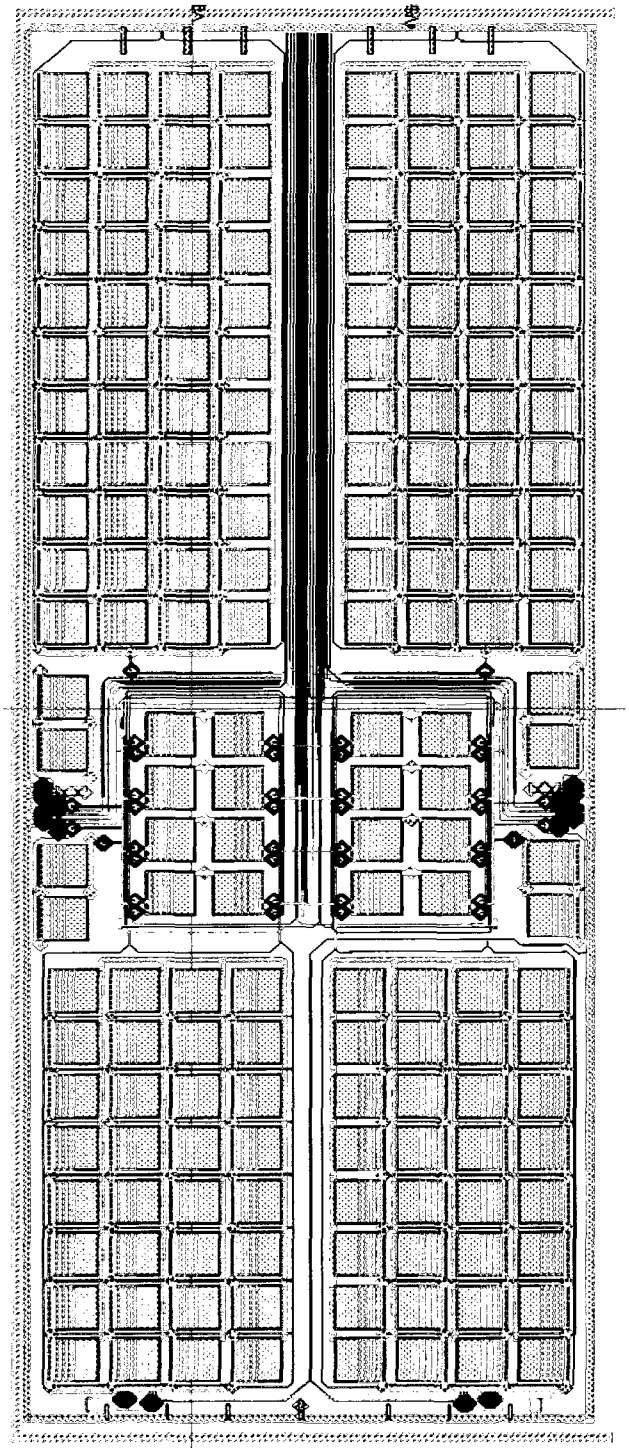
Appendix B: Layout of Direct RF sampling mixer



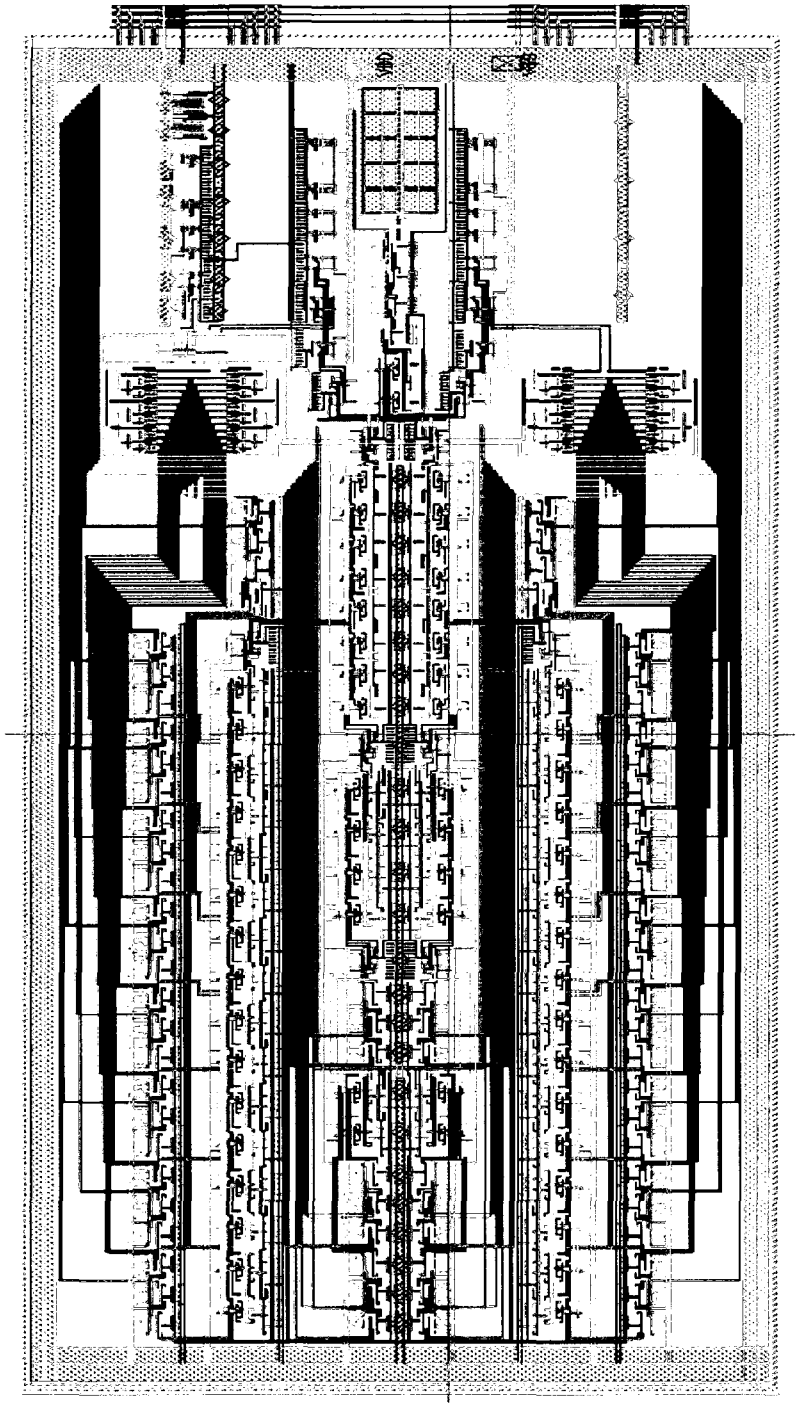
Appendix B.1 Layout of LNA without Inductors



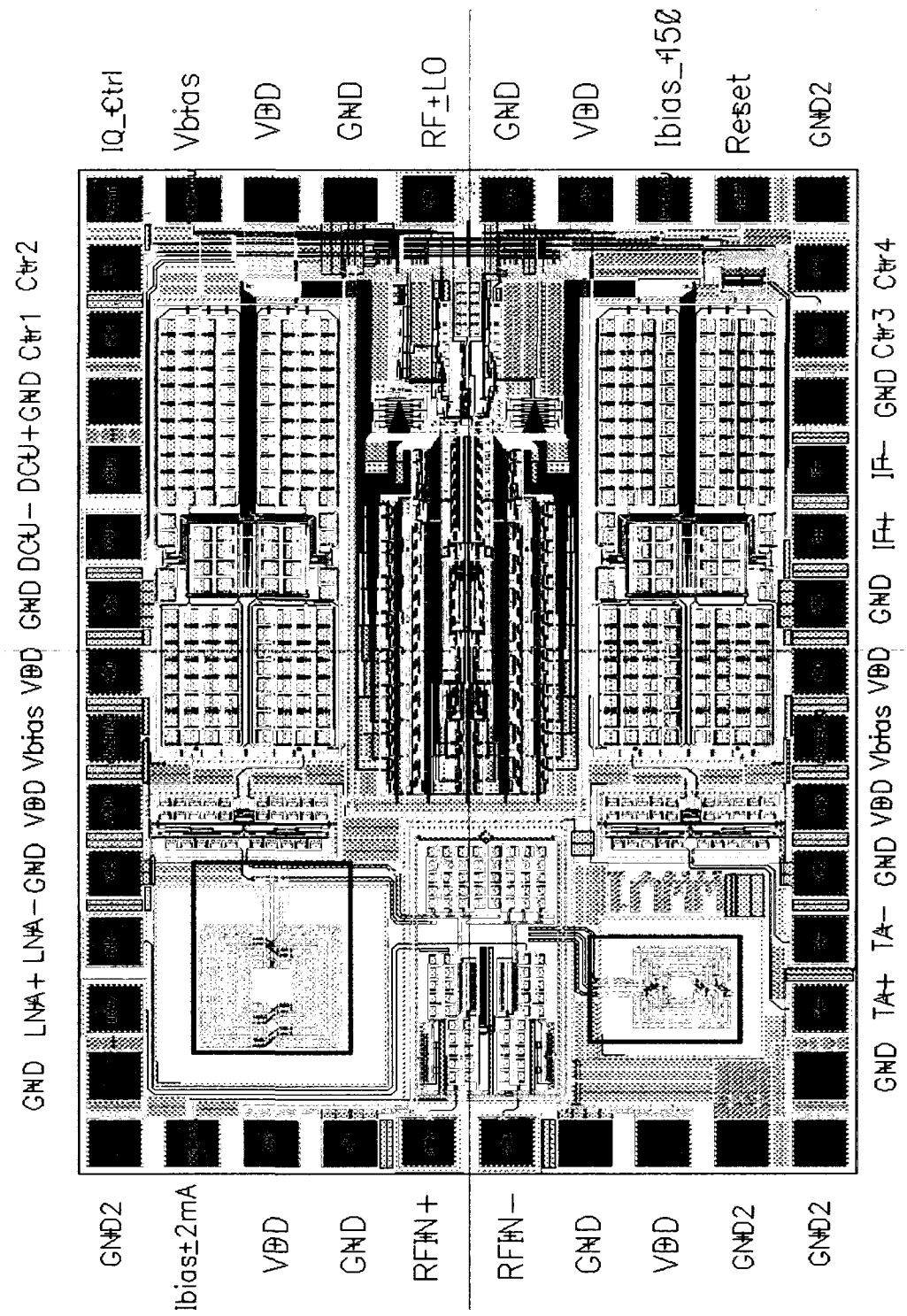
Appendix B.2 Layout of Transconductance Amplifier



Appendix B.3 Layout of Mixer



Appendix B.4 Layout of DCU



Appendix B.5 Layout of Direct RF Sampling Front End