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CMOS ANALOG CUBING CIRCUITS FOR RADIO-OVER-FIBER PREDISTORTION

By
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presented to Carleton University
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Abstract

The practical implementation of an analog cubing function in $0.18\mu\text{m}$ CMOS technology is presented. Analog cubing circuits have analog signal processing applications, such as Radio-over-Fiber predistortion. A literature review of the state-of-the-art revealed a need for CMOS cubing circuits with high gain and bandwidth. The theory and design of the CMOS circuits, which exploit the non-linear and high-frequency characteristics of deep submicron transistors, is presented. Three measures of cubicity, the degree to which a circuit can produce a purely cubic response, were proposed in order to compare the simulated and measured results.

The implemented circuits have measured voltage gains in the range of 1.01 to $31.3V^{-2}$, where the units V^{-2} arise from the cubing nature of the circuit. The direct current draw of the circuits ranged from 4.4mA to 7.2mA . The off-chip test environment prevented high-frequency operation due to capacitive loading and transformer performance issues, but results were observed in the 7 to 100MHz range.

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To Andrew

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Glossary

I_D	Large-signal drain-source current
V_{BIAS}	Input bias voltage
v_{id}	Small-signal differential input
v_i	Small-signal single-ended input
v_{out}	Small-signal differential output
ADS	Agilent Design System
BJT	Bipolar Junction Transistor
CMC	Canadian Microelectronics Corporation
CMOS	Complementary Metal Oxide Semiconductor
ESD	Electrostatic Discharge
FET	Field Effect Transistor
FFT	Fast Fourier Transform
IIP5	Input-referred Fifth-order Intercept Point
JFET	Junction Field Effect Transistor
MIM	Metal Insulator Metal
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PSS	Periodic Steady State
RoF	Radio-over-Fiber

Chapter 1

Introduction

1.1 Motivation

Analog signal processing blocks are attractive for those demanding high-frequency or low-power applications for which digital signal processing is too slow or too power hungry. A variety of such analog signal processing blocks have been reported in the literature [1–4], but their performance degrades significantly at radio frequencies. Improvements in the performance of the reported analog blocks are required for high-frequency applications.

A cubing circuit implementing the mathematical function $f(x) = x^3$ is useful in function approximation blocks [1, 5], frequency multipliers [6], and predistortion blocks [7–9].

One particular application that requires cubing circuits is Radio-over-Fiber Predistortion. Added distortion from laser diodes directly modulated with an analog signal, must be addressed in the cellular base station receiver environment with a predistortion block. Third-order distortion can be generated with the use of analog cubing circuits. The input amplitude to this circuit are expected in the μV to mV range and the frequency response would ideally extended up to the 1GHz range.

1.2 Objective

The objective of this thesis is to describe the theory, design, implementation and testing of CMOS analog cubing circuits required for the Radio-over-Fiber (RoF) predistortion application. As such, the design will be targeted for fabrication in a $0.18\mu\text{m}$ CMOS process to facilitate an integrated solution with other RoF receiver components.

1.3 Thesis Organization

Chapter 2 introduces the RoF predistortion application and conducts a literature review of the state-of-the-art of cubing circuit design. The theory and design of a cubing circuit that is suitable for high frequency operation are described Chapter 3. Simulated operation of the circuit is presented in Chapter 4, including non-ideal matching and parasitic effects. The circuit layout, test setup, and measured results are addressed in Chapter 5. Contribution to research and possibilities for future work will be discussed in Chapter 6.

Chapter 2

Background

Cubing circuits can be used within RF signal processing applications like Radio-over-Fiber (RoF) predistortion. Sections 2.1 and 2.2 discuss the concepts of RoF and predistortion, respectively. A literature review of published cubing circuit designs and results is given in Section 2.3.

2.1 Radio-over-Fiber

Radio-over-Fiber receivers use optical fiber links to distribute RF signals from cellular base stations to the central office. Typically, the components in a non-RoF base station receiver include front end radio frequency, intermediate frequency, base-band and bit-stream components. Large enclosures are required to house the digital signal processing equipment, which increases site installation costs [10, p. 221].

There is on-going research to reduce the need for expensive, digital signal processing base station equipment by instead transmitting radio signals over optical fiber [11–13]. The base station then functions only as a “remote antenna”, leaving the digital signal processing to the central office, and making the base station equipment easier to maintain and upgrade [10, pp. 221-8].

One mechanism for putting “radio over fiber” is laser light intensity modulation. The modulation could be direct or external, by using a modulator. Directly-modulated laser diodes provide a less complex, lower cost solution [13], at the expense of creating additional distortion in the outgoing signal. An example of distortion produced by a Fabry-Perot type laser is illustrated in Figure 2.1, in which the laser diode output of a two-tone test is shown on a lightwave measurement system. The distortion introduced by the laser creates inter-modulation tones on either side of the two large input tones.

Figure 2.1: Laser Diode Output of Two-tone Test on a Lightwave Measurement System.

2.2 Predistortion

Predistortion has previously been used in applications, such as power amplifiers [9, 14, 15] as a linearization method. Recently, predistortion has been used in RoF applications to correct for the distortion introduced by the laser [8, 13, 16–19].

Adaptive predistortion uses the laser's inverse transfer function [19] to counteract added distortion and produce a more linear output. Figure 2.2 illustrates a conceptual predistortion loop that explains the predistortion concept graphically. Ideally, the final optical output response is linear with respect to the RF input.

Figure 2.2: Radio-over-Fiber Predistortion Concept: The RF signal is fed into the predistorter which uses the laser diodes inverse transfer function to add distortion. After the signal is sent through the laser driver and diode, the resultant optical output is linearized. The photo diode observes the distortion at the output and the processor makes adjustments to the predistorter as necessary.

Performance requirements mandate that the predistorter be implemented in analog circuitry (for current CMOS technologies). Analog signal processing offers advantages over digital processing, such as a higher bandwidth, smaller size, and lower power requirements. However, some digital signal processing may be needed to analyze the distortion at the output and generate some analog control signals to correct imperfections in the analog circuitry (i.e. gain errors, device mismatch, and temperature effects).

The predistortion topology of Figure 2.3 was developed in [19, p. 112] by deriving the inverse transfer function of a Distributed Feedback (DFB) laser diode. The circuit is comprised of gain blocks, differentiators, and phase shifters, as well as a splitter, a

summer, a squaring circuit and a cubing circuit (which is used to generate third-order distortion). Section 2.3 will discuss the current state-of-the-art of cubing circuits and the specifications required to evaluate their performance.

Figure 2.3: Predistorter derived from inverse DFB laser diode model [19, p. 112].

2.3 Cubing Circuit Literature Review

The cubing circuits proposed in the literature use a variety of devices to generate cubic responses: diodes [7,9,13,14,20–25], Operational Transconductance Amplifiers (OTA) [5], Junction Field Effect Transistors (JFET) [6], Bipolar Junction Transistors (BJT) [7], and Complementary Metal Oxide Semiconductor (CMOS) transistors [1,8].

The following sections describe the defining properties and specifications of cubing circuits and discuss the devices and topologies that are employed to generate a cubic function. A comparison of the circuit performance characteristics is given in Section 2.3.7.

2.3.1 Cubing Circuit Properties and Specifications

Before evaluating the state-of-the-art of cubing circuits, the specifications by which cubing circuits are judged are described. Where possible, the types of devices and the fabrication process used in the reported literature are indicated. The number of devices within the cubing circuits is also an important evaluation tool, as it can be an indication of the required chip area (several of the designs are fabricated with discrete devices, so this is only a concern if the circuit can be integrated for the desired predistortion application) and power consumption.

An ideal cubing circuit would implement the function: $y = x^3$, or a “cubic monomial” [26, pp. 7-18]. The cubic function is an odd, anti-symmetric, non-linear function. For large inputs ($x > 1$), the ideal circuit would be an amplifier, but for smaller inputs ($x < 1$), it becomes an attenuator. Consider $x = 0.1$, which when cubed becomes: $y = 0.1^3 = 0.001$. To avoid seriously attenuating smaller signals, a gain coefficient of α could be applied to the cubing function: $y = \alpha x^3$.

The transfer function of a voltage cuber is given in Equation 2.3.1, where V_i is the input voltage, V_o is the output voltage, and α is the gain coefficient with units of V^{-2} .

$$V_o(t) = \alpha V_i(t)^3 \quad (2.3.1)$$

The cubic gain (α) can be an important specification of a cubing circuit for certain applications. In the RoF predistortion application introduced in Section 2.2, gain stages are required at the output of the cubing circuit in Figure 2.3 (in the figure, these gain stages are labelled m6, m7 and m8).

Another important specification is the cubicity, or degree to which the cubing term (x^3) can be isolated from other terms (x , x^2 , x^4 , x^5 , etc). To the author’s knowledge, there is no standard method of determining the accuracy of a simulated or measured cubing

response. Most authors in the literature use a graphical comparison to an ideal cubing function, and fit that function to the response to determine the cubing gain. One paper in particular [6] calculated the root-mean-squared (RMS) optimization error of the fitting. A detailed discussion of proposed cubicity measures will be included in Section 3.3.

The time domain behaviour of cubing circuits must also be considered. The ideal response of a cubing circuit (assuming $\alpha = 1$) to a sinusoidal input with amplitude a_1 and angular frequency ω_1 is shown in Equation 2.3.2.

$$(a_1 \sin \omega_1 t)^3 = \frac{3}{4}a_1^3 \sin \omega_1 t - \frac{1}{4}a_1^3 \sin 3\omega_1 t \quad (2.3.2)$$

At the output, there are two tones present: one at the fundamental frequency (ω_1) and the other at its third harmonic ($3\omega_1$). The amplitude at the third harmonic is one third the amplitude at the fundamental. Graphically, the sums of sine terms in Equation 2.3.2 is given by Figure 2.4.

Figure 2.4: Graphical representation: The sum of the sinusoids shown in Figure 2.4(a) ($\frac{3}{4} \sin 2\pi t$ and $\frac{1}{4} \sin 2\pi 3t$) yields the cubic sinusoid of Figure 2.4(b).

In the target RoF application, the modulation frequency for transmission over fiber is in the 1GHz range, because the fiber properties are favourable (i.e. less dispersion) [19].

Therefore, high-speed operation of this circuit is desired. Section 3.3 will also propose a cubicity measure for bandwidth. The published results shown in the following sections simply indicate the operational bandwidth of the circuits.

2.3.2 Diode Cubing Circuits

In predistortion applications [7, 9, 13, 14, 20–24], diodes have been proposed as cubic distortion generators. The standard topology that is used is the anti-parallel structure found in [7, 22–25], and shown here in Figure 2.5.

Figure 2.5: Anti-parallel Diode Predistortion Circuit based on [22, pp. 238].

This topology produces unwanted first, fifth and higher order odd terms. The derivation of the output response found in [22, pp. 237-9] is given in Appendix A.1 (where it was expanded to include fifth-order terms). The final output voltage (V'_{RF}) is shown in Equation 2.3.3 in terms of the input voltage (V_{RF}):

$$V'_{RF} = \frac{R_O V_{RF}}{R_S + R_O + r_1} - \frac{r_3 R_O V_{RF}^3}{(R_S + R_O + r_1)^4} + \frac{(3r_3^2 - (R_S + R_O + r_1)r_5) R_O V_{RF}^5}{(R_S + R_O + r_1)^7} \quad (2.3.3)$$

where R_S is the source resistance, R_O is the output resistance defined in Figure A.1, and r_1 , r_3 , and r_5 are coefficients determined in Appendix A.1 that relate to diode parameters. The unwanted first- and fifth-order terms contribute to a larger error in the pure cubing response and could negatively influence the predistortion effect in the RoF system. In addition to the unwanted odd order terms, diode parameter mismatch within the circuit would cause even order terms to appear at the output.

A typical output response of an anti-parallel diode pair is given in [7] and shown in Figure 2.6. The graph shows the output voltage over a range of input voltages from -0.3V to 0.3V. The cubic fitting curve in Figure 2.6 deviates noticeably from the output response, although no measure of error is reported in [7]. The presence of higher order terms in the transfer function could contribute to the error observed in the output response. The cubic gain of this response was reported as $1.6V^{-2}$. The bandwidth, measured by the generation of third-order distortion, was found to be at least 2.7GHz.

Figure 2.6: Anti-parallel Diode Predistortion Circuit Output Response from [7].

To improve the cubic response of diode circuits, a modified anti-parallel diode circuit was proposed in [9] to improve the suppression of the linear term and another circuit topology was proposed in [27] to improve the suppression of the second-order term. Diodes can be used to generate an exponential characteristic, but consideration of higher order terms (which were neglected within these papers) is useful in order to improve cubing accuracy. More complex diode cubers can be found in patent [20], which involves a diode bridge and patent [21], which involves diode mixers. However, these two patents did not disclose any measured results.

2.3.3 OTA Cubing Circuit

An arbitrary power-law generator based on operational transconductance amplifiers (OTAs) was presented in [5]. A general circuit topology was outlined that is capable of producing an (M/N) th power of the input, where M and N are integers. Results were shown for a squaring, a square-rooting, and a cubing circuit topology.

Figure 2.7: Cube-Law Device Circuit Diagram based on operational transconductance amplifiers (OTAs) presented in [5].

Figure 2.7 shows the cubing circuit topology, which is composed of seven OTAs behaving as voltage controlled current sources. The final expression of the transfer function found in [5] is given by Equation 2.3.4, where g_m represents the transconductance of an OTA and k is the transconductance proportionality constant.

$$V_o = k^2 \frac{g_{mi3}}{g_{mo1}} V_i^3 \quad (2.3.4)$$

The authors of [5] constructed a breadboard circuit of OTAs (made by Intersil, part number: CA3080) to verify the design. The peak-to-peak output voltages are shown versus the peak-to-peak input in Figure 2.8. The input is limited to 0.06V peak-to-peak, or 0.03V peak.

Figure 2.8: Performance of the OTA Cube-Law Circuit presented in [5].

The reported gain for this circuit is $3800V^{-2}$, which is the largest of the cubing circuits reported here. The main disadvantage of this design is the low bandwidth. According to the product data sheets [28] of the OTAs used by [5], the 3dB-down bandwidth is 2MHz.

The authors suggest in the conclusion of their paper that CMOS devices could be used in the arbitrary power-law circuits instead of OTAs to improve dynamic range and accuracy. For the frequency to be improved as well, submicron CMOS devices would be required. However, the non-linear behaviour of submicron CMOS devices would violate the linear transconductance assumptions made in their derivations. This same non-linearity will be exploited in the cuber design proposed in this thesis to extract a cubic response.

As with the diode cubers, device mismatch can cause inaccuracies at the output of the OTA cuber. Mismatch between group i_1 OTAs and group i_2 OTAs causes an asymmetrical bipolar response [5] (meaning that the cubic gain for positive inputs will differ from the cubic gain for negative inputs).

2.3.4 JFET Cubing Circuit

A cubing circuit comprised of Junction Field Effect Transistors (JFETs) was reported in [6]. JFETs operate in a similar manner to depletion MOSFETs, although “the MOSFET has an even higher input resistance. This ... [has] made the JFET virtually obsolete” [29, p. 447]. The cubing circuit presented in [6] is shown in Figure 2.9.

Figure 2.9: Cube-Law Device Circuit Diagram based on Junction Field Effect Transistors (JFETs) presented in [6].

The cubic output response derived in [6] is given by Equation 2.3.5:

$$v_{OUT} \cong \frac{1}{4V_{P1}V_{P3}}v_{IN}^3 \quad (2.3.5)$$

where V_{Pk} is the pinch-off voltage of transistor Q_k .

Assumptions made in the derivations require the input voltage to be small and the resistors to be large so that the JFETs remain in the triode region of operation. Matching

of the JFET pinch-off voltages (V_p) is also a concern. Variations between devices would lead to an output with unwanted terms and a less cubic output.

In [6], the the cubing circuit was implemented with NPDS402 n-channel JFETs and its DC performance is shown in Figure 2.10. The gain of the circuit is $0.271V^{-2}$, which is the lowest of the gains reported here. The input is differential, but the graph plots the peak single-ended input versus the peak output. The input range is $-0.6V$ to $0.6V$.

Figure 2.10: Measured DC Performance of the JFET Cube-Law Circuit presented from [6].

The author fitted an ideal cubing function to the output response of the cubing circuit. The final RMS optimization error was small (1.7%) indicating that the characteristics of the circuit are well approximated by the expression of the output (Equation 2.3.5) with a gain of $0.271V^{-2}$. The author also indicated that this was in reasonable agreement with the calculated gain of the circuit ($0.266V^{-2}$).

The dynamic performance of the JFET cuber illustrated in [6] was limited to only a few kilohertz (3KHz). Typical performance parameters of JFETs given in [29, p. 451] would restrict the bandwidth of this circuit to below 100MHz.

2.3.5 BJT Cubing Circuit

An active cuber (Figure 2.11) comprised of bipolar junction transistors (BJTs) was proposed in [7] for the predistortion of power amplifiers. The circuit exploits the cross-over distortion of a B-class push-pull amplifier. With a proper setting of the bias levels, an odd order non-linear transfer characteristic can be obtained.

Figure 2.11: Circuit Diagram of BJT Cubing Circuit presented in [7].

The transfer characteristic (V_o versus V_i) of Class B amplifiers has “a notch (or dead-band) of $2V_{BE(on)}$ in V_i around $V_i = 0$. This deadband is common in Class B output stages and gives rise to *cross-over* distortion” [30, p. 363]. The transfer characteristic, as illustrated in [30, p. 364], appears to have been distorted by high odd order non-linearities (like third- or fifth- order), but the distortion was not quantitatively described.

Figure 2.12 shows the simulated output response of the push-pull amplifier. The response was fitted to a cubic-law function with a gain of $736V^{-2}$ for an input voltage less than 0.2V. The error between the actual response and the fitted cubic function was not stated in [7]. From visual inspection of Figure 2.12, there is a significant amount of error between the fitted curve and the actual transfer characteristic of the circuit.

Although the circuit suffers from an inaccurate transfer characteristic, it does produce a significant amount of gain and it operates at radio-frequencies (third-order term generation reported up to 2.7GHz [7]).

Figure 2.12: Simulated Transfer Characteristic for BJT Cubing Circuit from [7].

2.3.6 CMOS Cubing Circuits

There were two CMOS cubing circuits found in the reported literature [1,8]. The former was based on a tripling circuit and was fabricated in a $0.8\mu\text{m}$ process and the latter uses a cross-coupled differential pair fabricated in $0.18\mu\text{m}$ (the targeted process for the cubing circuit proposed in this thesis). These two circuits are discussed in detail in the following sections.

CMOS Tripling Circuit

In [1], a tripling circuit was presented which outputs the product of three distinct input voltages: $V_o = V_1 V_2 V_3$. If $V_1 = V_2 = V_3 = V_i$, a tripling circuit becomes a cubing circuit: $V_o = V_i^3$. The design presented in [1] uses a basic cell of four FETs in saturation, as shown in Figure 2.13, to generate an expression for the drain current (I_D) through M4 (Equation 2.3.6).

$$I_D = K(A_1 V_i^4 + A_2 V_i^3 + A_3 V_i^2 + A_4 V_i + A_5) \quad (2.3.6)$$

Figure 2.13: Tripling Circuit Cell Topology from [1].

Equation 2.3.6, which relates I_D to multiple powers of the input voltage V_i , was derived using square-law large signal MOSFET equations in [1]. Appendix A.2 summarizes the values of the coefficients (A_1 to A_5).

A special arrangement of cells with specific input voltage combinations (Figure 2.14) allows the cubing term of Equation 2.3.6 to be isolated and the tripling function of the circuit to be obtained.

Figure 2.14: Tripling Circuit Array of Cells from [1].

Differential inputs to the tripling cells are used to cancel the even order terms in the cell's output current expression (Equation 2.3.6), leaving only the odd order terms. The third-order terms are then isolated from the first-order terms by using an array of cells with specific input voltage combinations, thereby generating a tripling product. The different combinations of inputs are achieved with adding and subtracting circuits, such as the ones suggested by the authors [31, 32].

The output response and the tripler gain, β , (derivation shown in Appendix A.2) are given by:

$$V_{out} = \beta V_1 V_2 V_3 \quad (2.3.7)$$

$$\beta = -48R \left(\frac{1}{2} \mu_n C_{ox} \frac{W_4}{L_4} \right) \left(\frac{W_1/L_1}{W_2/L_2} \right)^2 \left(\frac{1}{V_C - V_{SS} - 2V_T} \right)^2 (V_{SS} + V_T) \quad (2.3.8)$$

With careful selection of the load resistance, R , and the other transistor parameters, which determine the constant β , the output can be related directly to the product of three distinct input voltages. The circuitry of [1] was fabricated in a $0.8\mu\text{m}$ CMOS process with a split supply of $\pm 1.5\text{V}$. The simulated DC response of the tripling circuit (with identical inputs) presented in [1] is shown in Figure 2.15. The cubing gain of the circuit was not stated in the paper, but by inspection of Figure 2.15 the gain is approximately 6V^{-2} . This tripling circuit was shown only to function at low frequencies near baseband (1KHz).

It is crucial to note that the derivation of the output voltage assumes that the devices follow the square-law characteristics of FETs in saturation. Scaling the design to a process with shorter gate lengths (such as $0.18\mu\text{m}$) in order to increase speed could reduce the cubing characteristic of the design, since short-channel devices operate in a non-square law fashion [33, pp. 290-6].

Using the tripling circuit as a cubing circuit results in a solution that is overly complex and includes a large number of transistors (32). The cubing circuit presented in this thesis is primarily based on the concepts developed in [1], but is designed to operate at higher

Figure 2.15: Simulated DC response of the tripler (with identical inputs) with data taken from [1].

frequencies and with a smaller number of transistors. The changes required to implement this improved design are further discussed in Chapter 3.

CMOS Cross-Coupled Differential Pair

A second CMOS cubing circuit was reported in [8]. This design uses the cross-coupled differential pair (CCDP) shown in Figure 2.16 to extract a cubing response.

The derivation of the output response is included in Appendix A.3. The final differential output current ($I_{out} = I_{o+} - I_{o-}$) expressed in terms of the differential input voltage ($v_{id} = v_{in+} - v_{in-}$) is given in Equation 2.3.10.

$$I_{out} = -\sqrt{\frac{(\mu_n C_{ox})^3}{64 (W/L)_{M1-M2} I_{bias1}}} \left(\left(\frac{W}{L} \right)_{M1-M2}^2 - \left(\frac{W}{L} \right)_{M3-M4}^2 \right) v_{id}^3 \quad (2.3.9)$$

If the circuit diagram of Figure 2.16 were to include load resistors at the output, the

Figure 2.16: Cross-Coupled Differential Pair Cubing Circuit from [8].

output current could be converted to an output voltage:

$$V_{out} = R \sqrt{\frac{(\mu_n C_{ox})^3}{64 (W/L)_{M1-M2} I_{bias1}}} \left(\left(\frac{W}{L} \right)_{M1-M2}^2 - \left(\frac{W}{L} \right)_{M3-M4}^2 \right) (v_{id}^3) \quad (2.3.10)$$

Gain results were not reported in [8], nor were the device sizes stated, which would have facilitated the calculation of the expected gain. The operational bandwidth of the cubing circuit was not explicitly stated; although, the bandwidth of the predistorter described in [8] was limited to 90MHz.

One advantage of this design over the CMOS design presented previously (Section 2.3.6) is the significant reduction in transistors. The total transistor count for this circuit is eight (M1-M4 plus four for the current mirrors), whereas the CMOS circuit in [1] has at least 32. The power consumption would also be reduced due to the reduction in the number of transistors and technology scaling. The frequency response was also greatly improved over the previous design (90MHz instead of 1KHz).

However, this cross-coupled differential pair (CCDP) circuit is subject to the same effects of the square-law device assumption as the tripling circuit. The derivation of the differential pair output current, presented in Appendix A.3, assumes the devices

follow square-law behaviour (Equations A.3.1 and A.3.2). This assumption limits the applicability of the CCDP design to submicron channel length devices, which do not operate in a purely square law fashion [34], but that would be required for high-frequency operation [33].

In addition, several other assumptions made in the derivation of the output response reported in [8] and presented in Appendix A.3 are cause for concern. The derivation of the current in a differential pair uses a Taylor series expansion of a square root function (Equation A.3.11), but ignores higher order terms that could certainly contribute to the inaccuracy of the cubic output. Another assumption is also made concerning device sizes and biasing (Equation A.3.18) that requires precision control of the bias currents in order to cancel the first-order term at the output. Process variations within the fabricated design could lead to device mismatch, which in turn would contribute to the inaccuracy of the final output. Mismatch is a concern for most differential designs and will be discussed in detail in Section 3.4.

2.3.7 Summary of Published Cubing Circuit Results

A summary of the device, gain, maximum input and bandwidth information of the cubing circuits reported in the literature is given in Table 2.1. The maximum input is reported as the maximum peak single-ended input voltage.

Ref.	Device	Manufacturer & Part #, or Process	Cubing Gain (V^{-2})	Maximum Input (V)	Bandwidth
[7]	Diode	Schottky HSMS-2822	1.6	0.3	1.3 to 2.7GHz
[5]	OTA	Intersil CA3080	3800	0.03	up to 10KHz
[6]	JFET	Nat'l Semi. NPDS402	0.271	0.6	up to 3KHz
[7]	BJT	Phillips BFE-520	736	0.2	1.3 to 2.7GHz
[1]	CMOS	0.8 μ m	≈ 6	0.4	up to 1KHz
[8]	CMOS	0.18 μ m	N/M	N/M	up to 90MHz

Table 2.1: Performance of Published Cubic Circuits (N/M = Not Mentioned).

The circuit with the highest gain ($3800V^{-2}$) is the OTA cuber reported in [5]. The highest maximum input voltage (0.6V) was reported in [6] for the JFET cuber. The circuits with the highest bandwidths are the diode and BJT cubers reported in [7]. There is a definite trade-off between input range and gain: the smaller the input range, the larger the gain that can be achieved. Figure 2.17 illustrates this relationship.

Figure 2.17: Comparison of published cubing circuit designs.

The error was not quantitatively discussed in most of the papers and hence was not included in the table. By inspection of the figures included in the literature review (Figures 2.6, 2.8, 2.10, 2.12 and 2.15), the circuits with the largest deviation from an ideal cubing response are the diode and BJT cubers. The pn junctions which form diodes and BJTs have an exponential transfer characteristic containing many odd order non-linearities. The higher order non-linearities (fifth, seventh, etc.) would account for the inaccuracies of the responses indicated in Figures 2.6 and 2.12.

Since the cubing circuit designs with the highest bandwidth have the worst error and the designs with the highest gain cannot be easily integrated (the OTA circuit assumes linear transconductance, which would be difficult to achieve with submicron CMOS devices), there is potential for an improved cubing circuit design.

2.4 Chapter Summary

Radio-over-Fiber is mentioned as a cost-effective solution for delivering cellular traffic to the central office via optical fiber. Directly-modulated laser diodes are used to implement this solution. Predistortion is a means of counteracting added distortion from lasers that in the end results in a more linear output. An example of an analog predistorter was given and was shown to require a cubing circuit to generate third-order distortion.

A literature review of cubing circuits was provided, which indicated that cuber specifications such as gain, accuracy, input voltage range and bandwidth are important design goals. Examples of cubers constructed from diodes, OTAs, JFETs, BJT's and MOSFETs were given. A comparison of the published results indicated that these cubers are insufficient for the target RoF predistortion application and there is potential for improved cubing circuit designs.

Chapter 3

Cubing Circuit Theory and Design

The theory and design of a CMOS cubing circuit intended for use in a RoF predistorter will be presented in this section. The theory is based on the tripling circuit design presented previously in Section 2.3.6. A description of the design techniques employed to improve the response will be provided, followed by a discussion of the effects of mismatch within the design. Design parameter selection, input impedance, and expected gain will also be addressed.

The notation used in this chapter and the remainder of this thesis to describe the cubing circuit inputs and outputs is as follows: v_i will represent the input signal voltage (be it DC or time domain), the input bias voltage is given as V_{BIAS} (its presence on any circuit diagram is implied, and the circuitry required to generate this voltage will be discussed later in Section 5.2), v_{id} will represent the differential input voltage, and v_{out} will represent the differential output voltage.

3.1 Cubing Circuit Theory

The tripling circuit in [1] can be used as a cubing circuit. However, the following subsections discuss the simplifications and design techniques applied to this design that were

used to create a high-speed, precision, analog cubing circuit. The deep submicron CMOS technology chosen for RoF application allows for high frequency operation, but requires careful consideration of the non-square-law operation of the MOSFET devices [34]. This will be addressed specifically in Section 3.1.3.

3.1.1 Simplifying the Tripling Circuit

Since a cubing circuit is effectively a tripling circuit with identical input voltages, the design of the tripling circuit presented in [1] can be greatly simplified. The paper suggested letting $V_1 = V_2 = V_3$, indicating that fewer adding and subtracting cells are required to generate the different input combinations for the array. However, it can also be shown that by using additional techniques, fewer than eight cells are required and the total number of transistors can be greatly reduced. The simplification suggested in [1] will be discussed first, followed by an analysis of the additional techniques.

By simplifying the tripling circuit output voltage equation with $v_i = V_1 = V_2 = V_3$ as suggested in [1], fewer adding circuits are required (two instead of eight since only $3v_i$ and $-3v_i$ need to be generated with adding circuits). The simplified cubing circuit topology is shown in Figure 3.1.

3.1.2 Design Technique #1

The first of the techniques used to simplify the initial cubing circuit design takes advantage of the method for isolating the third-order term from the first-order term. As shown in Appendix A.2, the sum of the input voltages as first-order terms must be zero in order to eliminate the linear terms at the output. Instead of $(3v_i - v_i - v_i - v_i = 0)$ it is possible to achieve a cubing result with only three input combinations $(2v_i - v_i - v_i = 0)$. The modified topology is shown in Figure 3.2. The major advantage is the reduction in the

Figure 3.1: Initial Cubing Circuit Topology based on [1].

total number of transistors within the cuber (24 instead of 32). Consequently, the power dissipation is reduced and the layout is smaller. The one disadvantage is that the cubing gain is reduced since the voltage tripling contributes to the gain of the circuit (as shown in the derivation of [1] in Appendix A.2). When the voltage tripling is reduced to voltage doubling a decrease in gain by a factor of four can be expected (tripling gain: $3^3-1-1-1=24$, doubling gain: $2^3-1-1=6$).

Figure 3.2: Simplified Cubing Circuit Topology (using Design Technique #1).

3.1.3 Design Technique #2

A second technique used to improve the cubing circuit design was discovered during simulation. To improve the maximum operation frequency, the transistor lengths were reduced to $0.18\mu\text{m}$ (the minimum allowable gate length in the chosen process). With such short channel devices, the square law model is no longer accurate and direct substitution of circuit parameters into this model does not yield useful results. However, “any nonlinear transfer function can be written as a series expansion of power terms unless the system contains memory, in which case a Volterra series is required” [35, p. 23], but Volterra series analysis can be more complicated [36]. Therefore the non-linearity in the large-signal current through one short channel transistor can be more easily modeled as the weighted sum of multiple powers of the input voltage, as in a Taylor series given by:

$$I_D = a_0 + a_1v_i + a_2v_i^2 + a_3v_i^3 + a_4v_i^4 + a_5v_i^5 + \dots \quad (3.1.1)$$

where I_D is the large signal drain-source current, v_i is the small signal input voltage, and the a_n 's are the Taylor series coefficients. The first coefficient, a_0 , represents the large-signal current component and the remaining coefficients represent small-signal currents, which when added give the overall large-signal drain-source current (I_D). Equation 3.1.1 implies that a single transistor can generate the tripling cell's current expression, instead of the four that were previously required. As before, the even order powers can be canceled using differentially paired transistors. Higher, odd order powers of v_i (e.g. $\{v_i^5, v_i^7, v_i^9, \dots\}$) are negligible compared to v_i^3 for small v_i . The desired cubic term can be isolated by using the same method as the tripling circuit: an analog adder configuration of transistors with specific input voltage combinations to cancel the first-order terms (e.g. $2v_i - v_i - v_i = 0$). The simplified topology is shown in Figure 3.3.

The split supply ($\pm 1.5\text{V}$) used in [1] was replaced with the single supply (1.8V) used

Figure 3.3: Simplified Cubing Circuit Topology (using Design Technique #2).

in the CMOS $0.18\mu\text{m}$ process. All six cubing transistors (M1 to M6) are biased identically (V_{BIAS}), so that the even order and linear terms cancel correctly.

If the v_{out+} and v_{out-} nodes of this new circuit had not been switched from their positions in Figure 3.2, the cubing output would have been inverted since each cell of the tripler contains an inverting stage (M1 and M3 in Figure 2.13).

The main advantages of this design are a reduced transistor count (which implies a smaller layout area and reduced power dissipation) and a topology that allows each transistor to have its bulk and source terminals to be connected to the same potential to avoid complications from the body effect (e.g. increased threshold voltage). In the tripling cell of Figure 2.13, the bulk of M3 should be connected to its source to reduce the body effect. A CMOS process with deep-N-wells or p-wells would be required.

3.1.4 Design Technique #3

This technique serves to improve the gain of the transfer characteristic. The cubing circuit can be configured to amplify the output by adding a current mirror that sinks current

from both the v_{out+} and v_{out-} branches, as shown in Figure 3.4. The current source (I_{ref}) would be located off-chip.

Figure 3.4: Final Cubing Circuit Topology (using Design Technique #3).

In the previous circuit, if the device sizes were increased, the DC current was also increased. With the presence of a current sink to regulate the current, the output gain of the cubing circuit could be increased without increasing the DC current, thereby improving the gain adjustability of the cubing circuit output.

The trade-off is that the cubing transistors are now affected by the body effect since their bulk and source contacts are no longer at the same potential. The gate bias voltage can be increased to offset the increase in the threshold voltage caused by the body effect.

3.2 Cubing Gain Calculation Method

The method proposed for calculating the expected gain of the cubing circuit is based on the method shown in the tripling circuit [1] (Appendix A.2). This proposed method

expands on the concept of using a Taylor series equation to define MOSFET behaviour that was introduced in Section 3.1.3.

With the devices all having deep submicron channel lengths, the square-law model for MOS transistors is no longer appropriate to predict the drain current [34]. This cubing gain calculation method requires that fifth-order Taylor series polynomials (like the one shown in Equation 3.1.1) be fitted to the current responses of each of the six cubing transistors of Figure 3.4.

The DC current responses should be obtained while the transistors are operating within the circuit, to ensure that all non-linear effects are observed. Even though there are four separate inputs (v_i , $-v_i$, $2v_i$ and $-2v_i$), all of the responses are fitted to the input v_i for simplicity and ease of computation. The responses of the six cubing transistors (M1 to M6) are assumed to have the following form:

$$I_{M1} = a_{0,M1} + a_{1,M1}v_i + a_{2,M1}v_i^2 + a_{3,M1}v_i^3 + a_{4,M1}v_i^4 + a_{5,M1}v_i^5 \quad (3.2.1)$$

$$I_{M2} = a_{0,M2} + a_{1,M2}v_i + a_{2,M2}v_i^2 + a_{3,M2}v_i^3 + a_{4,M2}v_i^4 + a_{5,M2}v_i^5 \quad (3.2.2)$$

$$I_{M3} = a_{0,M3} + a_{1,M3}v_i + a_{2,M3}v_i^2 + a_{3,M3}v_i^3 + a_{4,M3}v_i^4 + a_{5,M3}v_i^5 \quad (3.2.3)$$

$$I_{M4} = a_{0,M4} + a_{1,M4}v_i + a_{2,M4}v_i^2 + a_{3,M4}v_i^3 + a_{4,M4}v_i^4 + a_{5,M4}v_i^5 \quad (3.2.4)$$

$$I_{M5} = a_{0,M5} + a_{1,M5}v_i + a_{2,M5}v_i^2 + a_{3,M5}v_i^3 + a_{4,M5}v_i^4 + a_{5,M5}v_i^5 \quad (3.2.5)$$

$$I_{M6} = a_{0,M6} + a_{1,M6}v_i + a_{2,M6}v_i^2 + a_{3,M6}v_i^3 + a_{4,M6}v_i^4 + a_{5,M6}v_i^5 \quad (3.2.6)$$

Several assumptions can be made concerning the relationship between the coefficients, such as identical bias conditions, input voltage conditions, and device sizing. The simplifications made based on these assumptions will be discussed next.

Since all of the transistors have the same dimensions and DC bias, the following assumption can be made:

$$I_{Mx}(v_i = 0) = a_0 = a_{0,M1} = a_{0,M2} = a_{0,M3} = a_{0,M4} = a_{0,M5} = a_{0,M6} \quad (3.2.7)$$

Transistors M2 and M3 have the same input ($-v_i$), therefore, $I_{M2} = I_{M3}$. By the same logic $I_{M5} = I_{M6}$ since M5 and M6 have the same input (v_i).

The differential nature of the circuit leads to another simplifying assumption. Since M1 and M4 have differential inputs, their odd order coefficients would be equal with opposite signs, but their even order coefficients would be equal with the same sign. Equations 3.2.8 and 3.2.9 state this assumption:

$$a_{x,M1} = -a_{x,M4}, x = \{odd : 1, 3, 5\} \quad (3.2.8)$$

$$a_{x,M1} = a_{x,M4}, x = \{even : 2, 4\} \quad (3.2.9)$$

The same can be inferred about the differential nature of M2 and M5:

$$a_{x,M2} = -a_{x,M5}, x = \{odd : 1, 3, 5\} \quad (3.2.10)$$

$$a_{x,M2} = a_{x,M5}, x = \{even : 2, 4\} \quad (3.2.11)$$

After incorporating the previously stated assumptions, the models become:

$$I_{M1} = a_0 + a_{1,M1}v_i + a_{2,M1}v_i^2 + a_{3,M1}v_i^3 + a_{4,M1}v_i^4 + a_{5,M1}v_i^5 \quad (3.2.12)$$

$$I_{M2} = a_0 + a_{1,M2}v_i + a_{2,M2}v_i^2 + a_{3,M2}v_i^3 + a_{4,M2}v_i^4 + a_{5,M2}v_i^5 \quad (3.2.13)$$

$$I_{M3} = a_0 + a_{1,M2}v_i + a_{2,M2}v_i^2 + a_{3,M2}v_i^3 + a_{4,M2}v_i^4 + a_{5,M2}v_i^5 \quad (3.2.14)$$

$$I_{M4} = a_0 - a_{1,M1}v_i + a_{2,M1}v_i^2 - a_{3,M1}v_i^3 + a_{4,M1}v_i^4 - a_{5,M1}v_i^5 \quad (3.2.15)$$

$$I_{M5} = a_0 - a_{1,M2}v_i + a_{2,M2}v_i^2 - a_{3,M2}v_i^3 + a_{4,M2}v_i^4 - a_{5,M2}v_i^5 \quad (3.2.16)$$

$$I_{M6} = a_0 - a_{1,M2}v_i + a_{2,M2}v_i^2 - a_{3,M2}v_i^3 + a_{4,M2}v_i^4 - a_{5,M2}v_i^5 \quad (3.2.17)$$

The current through each of the load resistors is found by summing the branch currents:

$$I_{out+} = I_{M1} + I_{M2} + I_{M3} \quad (3.2.18)$$

$$= 3a_0 + (a_{1,M1} + 2a_{1,M2})v_i + (a_{2,M1} + 2a_{2,M2})v_i^2 + (a_{3,M1} + 2a_{3,M2})v_i^3 + (a_{4,M1} + 2a_{4,M2})v_i^4 + (a_{5,M1} + 2a_{5,M2})v_i^5 \quad (3.2.19)$$

$$I_{out-} = I_{M4} + I_{M5} + I_{M6} \quad (3.2.20)$$

$$= 3a_0 - (a_{1,M1} + 2a_{1,M2})v_i + (a_{2,M1} + 2a_{2,M2})v_i^2 - (a_{3,M1} + 2a_{3,M2})v_i^3 + (a_{4,M1} + 2a_{4,M2})v_i^4 - (a_{5,M1} + 2a_{5,M2})v_i^5 \quad (3.2.21)$$

The differential output voltage (v_{out}) of Figure 3.4 is related to the branch currents (I_{out+} and I_{out-}) as follows:

$$v_{out} = v_{out+} - v_{out-} \quad (3.2.22)$$

$$v_{out} = (V_{DD} - RI_{out+}) - (V_{DD} - RI_{out-}) \quad (3.2.23)$$

$$v_{out} = -R(I_{out+} - I_{out-}) \quad (3.2.24)$$

Substituting Equations 3.2.19 and 3.2.21 into Equation 3.2.24 yields:

$$v_{out} = -2R(a_{1,M1} + 2a_{1,M2})v_i - 2R(a_{3,M1} + 2a_{3,M2})v_i^3 - 2R(a_{5,M1} + 2a_{5,M2})v_i^5 \quad (3.2.25)$$

The relationship between the input (v_i) and the differential input voltage (v_{id}) is given by: $v_{id} = 2v_i$. Substituting this into Equation 3.2.25 yields:

$$v_{out} = -R(a_{1,M1} + 2a_{1,M2})v_{id} - \frac{R}{4}(a_{3,M1} + 2a_{3,M2})v_{id}^3 - \frac{R}{16}(a_{5,M1} + 2a_{5,M2})v_{id}^5 \quad (3.2.26)$$

The linear term of Equation 3.2.26 ($R(a_{1,M1} + 2a_{1,M2})v_{id}$) contains two linear coefficients, $a_{1,M1}$ and $a_{1,M2}$ from Equations 3.2.1 (transistor M1) and 3.2.2 (transistor M2), respectively.

From Figure 3.4, the input voltage of M1 is $2v_i$ and the input voltage of M2 is $-v_i$. Although transistor M1 has an input twice as large as M2, the current expression for M1 (Equation 3.2.1) was fitted to v_i . Therefore, the linear coefficient $a_{1,M1}$ contains a factor of two that corresponds to the voltage doubling.

Similarly, the current expression for M2 (Equation 3.2.2) was fitted to v_i and not to its input $-v_i$. Therefore, the linear coefficient $a_{1,M2}$ will be negative.

Ideally, the following condition holds and the linear term will be cancelled.

$$\frac{1}{2}a_{1,M1} = -a_{1,M2} \quad (3.2.27)$$

Thus, only the third- and fifth-order terms in Equation 3.2.26 remain:

$$v_{out} = -\frac{R}{4}(a_{3,M1} + 2a_{3,M2})v_{id}^3 - \frac{R}{16}(a_{5,M1} + 2a_{5,M2})v_{id}^5 \quad (3.2.28)$$

Unfortunately, the value of the coefficients and hence the gain cannot be easily calculated from transistor parameters. As mentioned previously in Section 3.1, the $0.18\mu m$ CMOS technology chosen for the RoF application allows for high frequency operation, but the deep submicron devices operate in a non-square-law manner [34]. Simulations and curve fittings are required to determine the value of the coefficients. This task will be undertaken in Section 4.1.2.

3.3 Evaluation of Cubicity

As mentioned briefly in Section 2.3.1, measures of cubicity (the degree to which a circuit can produce a purely cubic response) are required. There are graphical measures, such as plotting the absolute difference between the output and an ideal cubic response, or obtaining a polynomial curve-fitting of the output. These graphical methods will both be undertaken in the simulation results in Chapter 4.

Four numerical measures of cubicity will also be used in this thesis. The first proposed measure, cubic polynomial proportionality, uses the coefficients of a polynomial fitted to a DC output response to relate the magnitude of the third-order term to the total magnitude of all the polynomial terms. The second measure is the R^2 coefficient of determination from linear regression analysis that is used to describe the “goodness of fit” of the DC circuit response to an ideal model. The third measure, cubic bandwidth, provides a performance measure of cubing circuit frequency behaviour. The last measure, fifth-order input-referred intercept point (IIP5), will be used to evaluate the amount of unwanted, fifth-order distortion present in the output of the circuit.

3.3.1 Cubic Polynomial Proportionality (PP³)

The polynomial resulting from the calculated gain expression or the graphical curve-fitting method allows the magnitude of the cubic gain to be compared to gain arising from other ordered power terms in the expression. For an n^{th} degree polynomial as given in Equation 3.3.1, the Cubic Polynomial Proportionality (PP³) for a given input voltage (v_{id}) is given by Equation 3.3.2.

$$v_{out} = \alpha_0 + \alpha_1 v_{id} + \alpha_2 v_{id}^2 + \alpha_3 v_{id}^3 + \alpha_4 v_{id}^4 + \cdots + \alpha_n v_{id}^n \quad (3.3.1)$$

$$PP^3(v_{id}, n) = \frac{|\alpha_3 v_{id}^3|}{|\alpha_1 v_{id}| + |\alpha_2 v_{id}^2| + |\alpha_3 v_{id}^3| + |\alpha_4 v_{id}^4| + \cdots + |\alpha_n v_{id}^n|} \quad (3.3.2)$$

The cubic gain α is equivalent to α_3 . The dependence of PP³ on v_{id} is needed since the dominance of certain terms in the v_{out} polynomial depends on the magnitude of v_{id} . As a percentage, this performance measure conveys how well the gain of the cuber overcomes the gain of other power terms in the circuit response (a perfect cuber would have a PP³ of 100%). The α_0 term of Equation 3.3.1 was not included in the denominator of Equation 3.3.2, because DC offset terms can be removed (i.e with coupling capacitors,

level-shifters, or operational amplifier based subtractor circuits). In addition to PP³, it is also possible to compute the individual percentage contributions of other power terms by changing the numerator accordingly in Equation 3.3.2 (i.e. the quadratic contribution (PP²) would have $|\alpha_2 v_{id}^2|$ as the numerator, the quintic contribution (PP⁵) would have $|\alpha_5 v_{id}^5|$, etc). These percentages will be evaluated and compared in the simulations of Section 4.1.2.

3.3.2 Goodness of Fit: R^2

The “goodness of fit” between the circuit response and the response of an ideal model can be achieved using regression. A common criterion used in linear regression modelling to determine the best fit is the condition of least squares [37–40]. The graphical curve-fitting shown in the simulations of Chapter 4 employs the least squares criterion to determine the coefficients of the polynomial that best fits the simulated data. While the least squares criterion can be used for evaluating the coefficients of non-linear models, it is ill-advised for determining tests of significance [39, pp. 325-9], as discussed next*.

The main problem with using the least squares criterion on a non-linear response (like $y = \alpha x^3$) is that “the magnitude of the deviations from the model depend on the magnitude of y ” [40, p. 14]. Texts [37–40] on the subject of regression analysis suggest applying a normalizing transformation on y to remove this dependence. In [39, pp. 397-8], an example is given where a power relationship is linearized by applying a logarithmic transformation. For the log transform to work, the y variable must be positive [38, pp. 15-16] which limits its applicability to the proposed cubing circuit design.

*The use of the least-squares criterion in the polynomial fitting for the PP measures is a problem since fitting errors for smaller input amplitudes are insignificant when compared to fitting errors for larger amplitudes due to the non-linearity of the circuit. However, the polynomials that were fitted to the simulated and measured results were visually confirmed to be accurate except for inputs close to $v_{id} = 0$.

Fortunately, “knowledge of how error variance fluctuates with the mean response can often suggest a transformation” [37, p. 177]. Since the response is expected to be cubic, a cube root transformation can be applied to the non-linear model to linearize it:

$$y = \alpha x^3 \quad (3.3.3)$$

$$\sqrt[3]{y} = \sqrt[3]{\alpha} x \quad (3.3.4)$$

$$y^* = \alpha^* x^* \quad (3.3.5)$$

where y^* is the transformed dependent variable, α^* is the transformed gain and x^* is the transformed independent variable.

Now that the non-linear model has been transformed to a linear model with a slope of α^* ($\alpha^* = \sqrt[3]{\alpha}$) and an intercept of zero, linear regression analysis (and the least squares criterion) can be applied to determine the gain of the response and a measure of the “goodness of fit”.

As an aside, during the application of this method it was observed that if the dependent variable was not dominantly cubic (due to severe device mismatch as will be discussed in Section 3.4 and 4.1.5), the cube root transform is no longer valid. If the dependent variable is only slightly affected (by other order terms: first-order, second-order, etc), this is manifested as a non-zero intercept in the linear regression model.

Statistical analysis reference texts [37–41] report the coefficient of determination, R^2 , as a measure of how well a linear response has been fitted. The value of R^2 is:

$$R^2 = \frac{\sum (y_i)^2 - n\bar{y}^2}{\sum (y_i^*)^2 - n\bar{y}^2} \quad (3.3.6)$$

where y_i is the data corresponding to the model, y_i^* represents the cube root transformed measurement or simulation data, n is the sample size of the measured or simulated data, and $\bar{y}$ is the mean of the transformed data. R^2 is limited in range to between 0 and 1.

As stated in [39, pp. 9-10], the value of R^2 can be interpreted as the proportion of the variation in the dependent variable that is “explained” by its linear relationship with the independent variable.

In summary, several performance measures have been proposed that can be used to evaluate the cubicity of cubing circuits, including the polynomial proportionalities (PP^1 , PP^2 , PP^3 , etc.), as well as R^2 and α^* from the cube root transformation (α^* when cubed equals the gain α). These can be used along with the graphical methods (absolute difference and polynomial curve-fitting) to evaluate cubicity.

3.3.3 Cubic Bandwidth

This measure of cubicity determines the bandwidth over which the circuit response maintains its cubic properties. Equation 2.3.2 states that the response of a cubing circuit to a sinusoidal input has two tones present: one at the fundamental frequency (ω) and the other at its third harmonic (3ω), where the amplitude at the fundamental is three times larger than the amplitude at the third harmonic and there is a 180 degree phase difference between the fundamental and the third harmonic. A bandwidth measurement is required that takes these inherent properties of time domain cubing responses into account.

The proposed method is to gather a series of steady-state responses over different input frequencies and convert them into their component tones (through periodic steady state analysis of simulated data or fast fourier transforms of measured data). The fundamental and third-order tones can then be plotted versus the input frequency. A perfect cuber would have tones with a constant magnitude over frequency, and the fundamental tone would be three times larger than the third-order tone. The bandwidth over which the cuber maintains the ratio of three and 180 degree phase shift between the fundamental and third-order tones is proposed as a measure of cubicity.

The difficulty in using this measure is that the cubicity of the circuit varies with input amplitude. So it is possible to get different bandwidth results with different inputs. This will be further explored in the simulation results of Chapter 4.

3.3.4 Fifth-order Input-referred Intercept Point (IIP5)

Linear amplifier designers use input referred intercept points (like third-order: IIP3 and fifth-order: IIP5) to evaluate the linearity of their circuits and quantify the amount of harmonic distortion. The question for the cubing circuit designer is what measures should be used when evaluating the cubicity of a cubing circuit (the degree to which a circuit can produce a purely cubic response).

Referring back to the sine cubed expression in Equation 2.3.2, the magnitudes of the linear and third-order harmonic terms are both known to increase at a cubic rate. In addition, their magnitudes are related by a factor of three. Plotting the magnitudes of the linear and third-order terms of a cubing circuit on a log-log scale, as the amplitude a_1 is increased, would yield two parallel lines, both with a slope of three with the linear terms all being three times as large as the cubic terms.

Since the lines are parallel, the IIP3 of the cubing circuit is inherently infinite. While this measure does prove that the cubing circuit is functioning correctly, it does not give any indication of the amount of unwanted harmonic distortion in the circuit. For this purpose, other harmonic distortion measures (like fifth-order: IIP5) can be used to determine the amount of unwanted distortion in the cubic output.

One important consideration when using the IIP5 measure is that the fifth-order harmonic of the input must be within the bandwidth of the circuit. An alternative would be to consider two-tone IIP5 measurements, but careful analysis of the non-linear effects of the cubing circuit are required.

3.4 Parameter Mismatch and Variation Discussion

One of the factors expected to reduce the cubicity of the measured results of the cubing circuits is mismatch. Fabrication process tolerances and variations create problems for circuit designers since device sizes and device parameters of the fabricated chip can deviate from the ones used in simulation. Component mismatch can occur when a parameter value of one device deviates from the value of its matched device in a differential pair. Parameter variation occurs when both components from a matched pair deviate identically from their ideal design parameter values.

In addition, test setups used to evaluate the circuit can create problems by providing non-ideal inputs. In the case of the cubing circuit, this could mean input signals that are not completely differential (v_i and $-v_i$) or that are not ideally doubled (v_i and $2v_i$). Given that the accurate isolation of the cubing function depends on differential circuitry to eliminate even order terms, unwanted distortion terms present in the output caused by the reaction of the circuit to non-ideal inputs should be expected. Non-ideal input voltage doubling is also expected to distort the output since the cubing circuit's cancellation of first-order terms depends on combining linear current terms so that the sum is zero.

Mathematical derivations of the cubing circuit output in the presence of mismatch and variation would be challenging and lengthy. The derivations also require prior knowledge of how the Taylor series coefficients are affected when the operating points of each transistor changes. Instead, simulations were used to determine the effects of mismatch and variation, and the results are discussed in Section 4.1.5. Six cases of mismatch and variation were examined that could significantly affect the output of the cubing circuit.

- Load resistor mismatch: one load resistor deviates from its intended value by ΔR
- Load resistor variation: both resistors deviate by ΔR

- Transistor mismatch: a parameter value (width, length, etc) of one transistor deviates from the value of the other cubing transistors
- Transistor variation: all cubing transistors (M1 to M6) incur the same deviation
- Non-ideal differential input voltages: the required input combination for the circuit ($v_i, -v_i, 2v_i$ and $-2v_i$) is no longer differential by a small amount ϵ , but the voltage doubling is still present ($v_i, -\frac{1}{2}(1 + \epsilon)v_i, 2(1 + \epsilon)v_i$ and $-2v_i$)
- Non-ideal voltage doubling: the required input combination no longer has correct voltage doubling, but it is still differential (i.e. $v_i, -v_i, (1 + \epsilon)v_i$ and $-2(1 + \epsilon)v_i$)

Having signals that are not differential or having device mismatch will allow even order terms to appear at the output. Parameter variation will lead to a change in the cubicity of the circuit. In addition, having input signals that are not doubled as required will allow first-order terms to appear at the output, because the voltage doubling enables isolation of the cubing terms from the linear terms.

3.5 Input Impedance

Another important design consideration is the method by which the input signals will be delivered to the circuit. An input network designed to accomplish this task is described in Section 5.2.2. For this input network to effectively transfer voltage to the cubing transistors, the input impedance of those transistors is assumed to be large.

The theoretical calculation of the input impedance is complicated by the non-linearity of the circuit and the limitations of the linear approximation of the transconductance, g_m . In both [33, pp. 284-97] and [42, pp. 172-177], the input impedance of a single MOSFET in saturation is shown to be dominated by the gate-to-source capacitance, C_{gs} , and the gate-to-drain capacitance, C_{gd} . This capacitive input impedance of the transistors should be sufficiently large for the frequencies of interest.

Given the small size of the transistors used in the design, it is the parasitic capacitances of the input bonding pads that will dominate the input impedance of the fabricated design. This will be further examined in the time domain simulations in Section 4.3.3.

3.6 Circuit Design

This section will focus on the design specifics of the cubing circuit introduced in Section 3.1.4, including design criteria, device parameters, and biasing requirements.

3.6.1 Design Criteria

The chosen $0.18\mu\text{m}$ CMOS technology is a single polysilicon, six metal, salicide CMOS process, manufactured by TSMC (Taiwan Semiconductor Manufacturing Company) [43], with the design kit being provided through CMC (Canadian Microelectronics Corporation). The supply voltage for the $0.18\mu\text{m}$ CMOS technology is 1.8V . As a guideline, inputs for the cubing circuit were assumed to be limited to several hundreds of mV's. In practice, the input to the cubing circuit will be on the order of hundreds of μV 's.

3.6.2 Cubing Circuit Component Parameters

The square-law model of MOSFETs that describes their I-V characteristics is given by the following equation from [44, p. 96]:

$$I_D = \frac{\beta}{2} (V_{GS} - V_{TH})^2 \quad (3.6.1)$$

where I_D is the large-signal drain-source current, β is the transconductance parameter, V_{GS} is the gate to source voltage and V_{TH} is the threshold voltage.

Since this square-law model does not provide any indication of the cubing properties of short channel devices, parameterized simulations (that make use of the more complex

BSIM3 model) were used to determine the component values such as transistor widths and resistor values. The transistor lengths of the cubing transistors (M1-M6 of Figure 3.4) were reduced to $0.18\mu\text{m}$ to increase the maximum operating frequency of the circuit.

The current mirror transistors were designed to provide the required current sink. It is common practice ([29, pp. 403-405] and [44, pp. 427-429]) in the design of CMOS current mirrors to use long channel devices to avoid the effects of channel length modulation, which can be defined in terms of the drain-to-source voltage V_{DS} , the gate-to-source voltage V_{GS} , and the threshold voltage V_{TH} :

The voltage difference between the drain and the near end of the channel lies across a short depletion region often called the *pinch-off region*. As V_{DS} becomes larger than V_{eff} [$V_{GS} - V_{TH}$], this depletion region surrounding the drain junction increases its width ... [which] decreases the effective channel length ... [and] increases the drain current, resulting in what is commonly referred to as channel length modulation. [45, p. 25]

To avoid channel modulation effects, “a general design rule is to set the length of the MOSFETs used in analog applications to two to five times the minimum drawn gate length” [44, p. 428]. In following this design rule, the length of the current mirror transistors (M7 and M8) were chosen to be $1\mu\text{m}$, a little over five times the minimum channel length of $0.18\mu\text{m}$.

The component values of Figure 3.4 are listed in Table 3.1.

Component	Width (μm)	Length (μm)	Multiplicity
M1-M6	2.06	0.18	8
M7	7.75	1.00	20
M8	7.75	1.00	100
R	3.00	24.63	12

Table 3.1: Component values for the Saturation Cubing Circuit.

The load resistors (R) are each comprised of twelve polysilicon resistors connected in parallel. Each one has a nominal resistance of $2400\ \Omega$, when combined the load resistance in each differential branch of the circuit is approximately 200Ω .

The supply (V_{DD}) is 1.8V and the shared bias (V_{BIAS}) for the input transistors (M1-M6) is 1.5V. The reference current is 1.2mA which, when fed through the current mirror ratio of 1:5, becomes 6mA.

3.7 Other Cubing Circuit Designs

Two other cubing circuit designs were fabricated: one identical in topology to Figure 3.4, but biased partly in the MOSFET sub-threshold region and another design that is biased in the MOSFET triode region, but does not include Design Technique #3 (the current sink). The simulations, layouts, and measurements for these cubers are reported in Appendices B and C. A comparison of design parameters is given in Table 3.2.

Design Parameter	Saturation Cuber	Sub-threshold Cuber	Triode Cuber
Cubing Transistor Width (μm)	16.48	120.00	9.00
Cubing Transistor length (μm)	0.18	0.18	0.18
Current Mirror	Yes	Yes	No
Load Resistor (Ω)	200	300	526
Bias Voltage (V)	1.50	1.05	0.90

Table 3.2: Comparison of design parameters for the three different cubing circuits.

3.8 Chapter Summary

A cubing circuit was introduced that improves upon the design presented in [1], by reducing the transistor count and by reducing the channel length through process scaling. A method for calculating the cubic gain that is based on the Taylor series approximation of the transistor current responses was presented. The effects of mismatched parameters on the output response were discussed. Design parameters of the saturation cuber were compared to those of the sub-threshold and triode cubers.

Chapter 4

Simulation Results

The DC, time domain and Periodic Steady State (PSS) simulations of the cubing circuit design were undertaken with Cadence SpectreRF using the NMOS mixed-signal models for the transistors within the circuit. AC simulations were not attempted since AC simulations linearize the circuit around its operating point and thus are not suitable for simulation of the cubing response.

DC simulations were first run to ensure that the cubing circuit was performing its analog arithmetic function. The cubicity performance measures proposed in Section 3.3 were applied to the simulation results. Component mismatch analyses were also performed to understand the effects of process variations on the expected output.

Time domain analyses were also undertaken with the goal of determining the cubing circuit's highest operating frequency. The anticipated load of the test setup (discussed in more detail in Section 5.2) was included in the simulated model so that the operation of the circuit within a practical testing environment could be determined.

PSS simulations were used to determine the high-frequency characteristics and input impedances of the cubing circuits.

4.1 DC Simulations

The goals of the DC simulations were:

- to observe the cubing properties of short channel transistors in saturation,
- to determine the DC cubicity of the circuit (PP^3 , α , and R^2),
- to estimate the expected direct current draw of the circuit,
- to study the effects of component mismatch, and
- to examine the effects of parasitic resistance on the circuit

4.1.1 Region of Operation

MOSFET transistors are usually biased in the saturation region of operation to take advantage of increased gain (the slope of the I_{DS} versus V_{GS} curve increases with V_{GS}) and lowered gate-to-channel capacitance ($C_{gd} = 0$, due to pinch-off) [33, pp. 395-6]. While linear approximations of saturation transistor operation are often made (like the linear transconductance, g_m), there still exists non-linear behaviour, as will be discussed in the following sections.

The approximate range of input voltages (v_i) within which the transistors of the circuit remain in saturation can be determined from each transistor's operating point. All six transistors are identically sized and biased; however, transistors M1 and M4 from Figure 3.4 have the larger inputs, $2v_i$ and $-2v_i$ respectively, so these two transistors will exit the saturation region before the others. M1's range of saturation range operation was determined from the DC operating point results shown in Table 4.1.

v_i (mV)	$2v_i$ (mV)	V_{th} (V)	V_{GS} (V)	V_{DS} (V)	$V_{GS} - V_{th}$ (V)
-95	-190	0.682	0.682	0.562	0.000
0	0	0.678	0.891	0.593	0.213
200	400	0.698	1.197	0.500	0.499

Table 4.1: Cubing Circuit Region of Operation for transistor M1.

For $v_i = 0V$, M1 is in saturation since the following conditions for saturation operation are met: $V_{GS} \geq V_{th}$ and $V_{DS} \geq V_{GS} - V_{th}$. For $2v_i = 400mV$, M1 is approaching the triode region of operation since $V_{GS} \geq V_{th}$, but $V_{DS} \approx V_{GS} - V_{th}$. When $2v_i = -190mV$, M1 is approaching the sub-threshold region of operation since $V_{GS} \approx V_{th}$, which is the boundary between saturation and sub-threshold operation.

The range within which M1 remains in saturation extends from -190mV to 400mV. Since the inputs of M4 are the inverse of those of M1, the range of saturation operation of M4 extends from -400mV to 190mV. The overlap between these two ranges identifies the input voltages that allow the cubing circuit to remain in saturation are from $v_i = -95mV$ to $v_i = 95mV$, which corresponds to a differential input voltage range of $\pm(v_i - (-v_i)) = \pm 2v_i$, or $\pm 190mV$. In the next section, DC simulation results will demonstrate how these transistors exhibit cubic tendencies, even within the saturation region of operation.

4.1.2 I_D Polynomial Fitting

In Section 3.1.3, it was stated that the behaviour of a short-channel transistor could be modelled with a Taylor series expression, as given in Equation 3.1.1. To demonstrate the application of this model, the short channel transistors of the cubing circuit design (M1, M2, M4 and M5 of Figure 3.4) were simulated and had their I_D versus v_i curves fitted with fifth-order polynomials (within their saturation region of operation) as determined by polynomial fitting in MATLAB*. Curves for M3 and M6 were not shown since they are identical in size, bias and inputs to M2 and M5, respectively.

The I_D versus v_i curves are shown in Figure 4.1. The polynomial equations fitted to these curves are shown in Equations 4.1.1 to 4.1.6. Even though I_{M1} and I_{M4} are fed with $2v_i$ and $-2v_i$, respectively, they are plotted versus v_i for simplicity.

*The 'polyfit' function within MATLAB was used for all polynomial fitting.

$$I_{M1} = 0.0010 + 0.01251v_i + 0.0121v_i^2 - 0.1768v_i^3 + 0.3363v_i^4 - 0.5687v_i^5 \quad (4.1.1)$$

$$I_{M2} = 0.0010 - 0.00625v_i - 0.00596v_i^2 + 0.0427v_i^3 - 0.1653v_i^4 + 1.0393v_i^5 \quad (4.1.2)$$

$$I_{M3} = 0.0010 - 0.00625v_i - 0.00596v_i^2 + 0.0427v_i^3 - 0.1653v_i^4 + 1.0393v_i^5 \quad (4.1.3)$$

$$I_{M4} = 0.0010 - 0.01251v_i + 0.0121v_i^2 + 0.1768v_i^3 + 0.3363v_i^4 + 0.5687v_i^5 \quad (4.1.4)$$

$$I_{M5} = 0.0010 + 0.00625v_i - 0.00596v_i^2 - 0.0427v_i^3 - 0.1653v_i^4 - 1.0393v_i^5 \quad (4.1.5)$$

$$I_{M6} = 0.0010 + 0.00625v_i - 0.00596v_i^2 - 0.0427v_i^3 - 0.1653v_i^4 - 1.0393v_i^5 \quad (4.1.6)$$

Figure 4.1: I_D versus v_i curves for M1, M2, M4 and M5.

Equations 4.1.1 to 4.1.6 reveal the coefficients (a_0 to a_5 of Equation 3.1.1) of each transistor for this specific operating point and range of inputs. (Note: the coefficients are heavily dependent on the bias and the selected range of inputs.) Also note that $I_{M3} = I_{M2}$ and $I_{M6} = I_{M5}$, as expected.

Using the Taylor series method for predicting the gain (Section 3.2), the coefficients of the current expressions (Equations 4.1.1 to 4.1.6) are substituted into Equation 3.2.26 to find the output cubing gain ($\alpha = 4.57V^{-2}$).

$$v_{out} = -\frac{R}{4} (a_{3,M1} + 2a_{3,M2}) v_{id}^3 - \frac{R}{16} (a_{5,M1} + 2a_{5,M2}) v_{id}^5 \quad (4.1.7)$$

$$= -\frac{200}{4} (-0.1768 + 2(0.0427)) v_{id}^3 - \frac{200}{16} (-0.5678 + 2(1.0393)) v_{id}^5 \quad (4.1.8)$$

$$= 4.57v_{id}^3 - 18.9v_{id}^5 \quad (4.1.9)$$

Ideally, the even order terms are cancelled out, as shown in the derivation of the cubing response (Equation 3.2.26); however, the practical implementation of this circuit will have process variations which will prevent the complete cancellation of even order terms. The effect of mismatch on the circuit is further discussed in Section 4.1.5.

Using the coefficients, it is also possible to verify the linear assumption made in the gain calculation method of Section 3.2 (Equation 3.2.27). By design, the linear term should be cancelled in the summation of the branch currents; however, inevitably there are some residuals that remain.

$$\text{Linear term} = -R(a_{1,M1} + 2a_{1,M2}) v_{id} \quad (4.1.10)$$

$$= -R(0.01251 + 2(-0.00625)) v_{id} \quad (4.1.11)$$

$$= -0.002v_{id} \quad (4.1.12)$$

The significance of the unwanted linear and fifth-order terms is indicated in Figure 4.2, which plots the linear (PP¹), cubic (PP³) and quintic (PP⁵) polynomial proportionalities (refer to Section 3.3.1 for the definitions of these cubicity measures) versus the positive differential input voltage v_{id} .

For small input voltages, the output of this cubing circuit will be dominated by the magnitude of the linear term. In fact, the linear proportionality percentage approaches

Figure 4.2: Odd order Polynomial Proportionality percentages of the saturation cuber are shown versus the differential input.

100% for small inputs. This occurs due to the presence of the linear term (Equation 4.1.12) whose gain seems small (0.002) but this gain actually has a significant affect on the output for small inputs. Table 4.2 compares the magnitudes of the linear and cubic terms for several small input voltages.

Polynomial Term	Magnitude at $v_{id}=10\text{mV}$	Magnitude at $v_{id}=20\text{mV}$	Magnitude at $v_{id}=40\text{mV}$
Linear Term (μV)	20	40	80
Cubic Term (μV)	4.75	38	304

Table 4.2: The magnitudes of the linear and cubic polynomial terms for several small input voltages are listed. For small inputs, the linear term is larger than the cubic term, but as v_{id} increases the cubic term increases and dominates the linear term.

Since the presence of even small linear gain terms leads to 100% maximum PP¹, another measure is needed to quantify the amount of linearity in the cubing circuit output. One possibility is to report the input voltage at which the linear term magnitude

equals that of the cubic term. The “Linear Crossover” voltage for this circuit occurs at $v_{id}=20.9\text{mV}$. The linearity of the remaining circuits will be evaluated using this measure.

The cubicity of the circuits will be evaluated using the polynomial proportionality percentages proposed in Section 3.3.1. The maximum cubic (PP^3) percentage indicated in Figure 4.2 is 92.2% and the maximum quintic (PP^5) percentage is 12.9%. Both of these performance measures were determined for v_{id} within the input range of 0 to 190mV.

For larger inputs ($v_{id} > 0.1\text{V}$), the fifth-order term (v_{id}^5) becomes more significant relative to v_{id}^3 and v_{id} , which causes the quintic proportionality percentage to increase. In both cases, the linear and quintic unwanted terms lower the effective gain of the cuber which will be shown graphically in the following section.

4.1.3 Cubing Circuit Output

Figure 4.3 shows the plots of the output voltages (v_{out+} and v_{out-}) versus the input voltage (v_i). The output voltage nodes share the same bias point (1.20V). Taking the difference of these two nodes will result in the final cubing response (v_{out}) as shown in Figure 4.4.

Figure 4.3: Cubing Circuit Output Voltages (v_{out+} and v_{out-}).

Figure 4.4: The Cubing Circuit Differential Output Response (v_{out}) is plotted versus the Differential Input Voltage (v_{id}) and compared to an Ideal Cubing Response with a gain of $4.0V^{-2}$. The Absolute Error Curve indicates the simulated absolute error of the circuit; its axis is on the right side of the plot.

Although Equation 4.1.9 predicts the gain to be $4.57V^{-2}$, the first- and fifth-order terms in this equation serve to reduce the effective cubing gain of the circuit. Hence, Figure 4.4 compares the differential output voltage (v_{out}) to an ideal cubing curve with a gain of $4.0V^{-2}$ versus the differential input voltage (v_{id}). This figure also includes a plot of the absolute error between the simulated and ideal curves.

From Figure 4.4, the output of the cubing circuit is observed to match the ideal curve within the saturation region of operation (where v_{id} is within the range of $-0.19V$ to $0.19V$). Table 4.3 indicates the maximum absolute error for different input voltage ranges within the saturation region.

The differential output response, v_{out} of Figure 4.4, was fitted (over the entire input range v_{id} : $-0.4V$ to $0.4V$) with an eleventh-order polynomial in MATLAB. The polynomial

Input Range of v_{id}	Maximum Absolute Error
-190mV to 190mV	1.4mV
-175mV to 175mV	0.5mV
-155mV to 155mV	0.06mV

Table 4.3: Absolute error voltages are listed for different input voltage ranges.

and coefficients are shown here in Equation 4.1.13:

$$v_{out} = -0.00126v_{id} + 3.93v_{id}^3 + 28.2v_{id}^5 - 1110v_{id}^7 + 7520v_{id}^9 - 16200v_{id}^{11} \quad (4.1.13)$$

In determining the coefficients, all even order terms (up to tenth-order) were discovered to be insignificant. The coefficient of the third-order term ($3.93V^{-2}$) is close to the gain of $4.0V^{-2}$ that was observed in Figure 4.4. The maximum PP³ percentage for this polynomial is 90.4%, a decrease from the predicted value of 92.2%. The maximum PP⁵ percentage increased to 14.9% from the predicted value (12.9%). These changes are due to the inclusion of higher order terms that decrease the influence of the cubic gain at higher input voltages. The linear crossover point is reduced to 17.9mV from 20.9mV. Rounding error in the calculation of the linear term gain (Equation 4.1.12) is the cause of this change.

Linearizing the differential output response (within the input range: v_{id} : -0.19V to 0.19V) with a cube root transformation and applying linear regression analysis revealed the cubic gain to be $\alpha = 3.95V^{-2}$ and the coefficient of determination to be $R^2 = 0.99973$.

4.1.4 Direct Current Draw

Figure 4.5 illustrates the total direct current draw (including the reference current) of the circuit over the expected range of input voltages. Each of the six main transistors (M1 to M6) draw approximately 1mA each, and the current mirror draws 1.2mA for an approximate total of 7.2mA. The current variation is limited to $25\mu A$ over the range of inputs shown.

Figure 4.5: Total Direct Current Draw versus input voltage (v_i).

4.1.5 Parameter Mismatch and Variation Simulations

As noted previously in Section 3.4, this cubing circuit design is susceptible to device mismatch and variation. Mismatched and varied parameters cause the operating points to change, thereby changing the polynomial coefficients (discussed in Section 4.1.2) and preventing the accurate cancellation of even order and linear terms. The effects of device mismatch and variation on the simulation results are discussed in the following subsections. In addition, the effects of non-ideal voltage inputs (non-ideal differential and non-ideal voltage doubled inputs) will also be simulated.

The DC cubicity measures proposed in Section 3.3.1 (polynomial proportionality percentages) and 3.3.2 (cube root transform: “goodness of fit”) are applied to each of the different simulation cases and the results are tabulated in Section 4.1.7.

Resistor Mismatch

Adding a small, ideal resistor (ΔR) in series with one of the load resistors simulates the effect of a mismatch in load resistance. Figure 4.6(a) shows the differential output with no mismatch and compares it to the output simulated with a load mismatch of 10Ω (a 5% increase) and 20Ω (a 10% increase). Since the DC voltage at the v_{out+} and v_{out-} nodes are different when the mismatch is added, there exists a DC offset in the differential output ($v_{out+} - v_{out-}$). With a 5% mismatch, the offset is 25mV, and with a 10% mismatch, the offset is 50mV for the simulated bias currents.

Figure 4.6: Load Resistor Mismatch Simulation Results.

Figure 4.6(b) shows the corresponding error curves with the offsets removed mathematically from the data. (Note: in a time domain simulation, removing the offset would be possible with AC coupling.) The removal of the offsets reveals that the shape of the absolute error curves for the mismatch simulations are different. Since the mismatched load causes the operating points to change, the cubing behaviour of the transistors changes as well, thus affecting the gain of the circuit.

The DC cubicity performance measures were applied to the results and are reported in Table 4.4 of Section 4.1.7. The maximum PP² percentage increases as the mismatch is increased, indicating that the mismatch is introducing unwanted second-order power terms into the output response. The cube root transforms of the results reveal that the gain (α) increases with the mismatch, but the presence of a non-zero intercept in the transformed response reveals the presence of mismatch. The “goodness of fit” performance measure (the coefficient of determination: R^2) decreases as the resistor mismatch is increased.

Resistor Variation

Increasing each load by a small resistance, ΔR , simulates the effect of resistor variation. Figure 4.7(a) shows the differential output with 5% and 10% parameter variation and compares them to the 0% response as well as an ideal response with a gain of $4.0V^{-2}$.

Figure 4.7: Load Resistor Variation Simulation Results.

There is no DC offset in Figure 4.7(a) as there was in Figure 4.6(a), which is to be expected because the DC output levels are now identical and cancel, leaving no offset.

However, the change in operating points will affect the cubing behaviour of the transistors as was noted in the cubicity measures summarized in Table 4.4.

The increase in resistor variation causes an increase in the maximum PP^3 and a decrease in the linear crossover point (indicating less of linear influence on the output). This was offset by an increase in the maximum PP^5 percentage (indicating that the fifth-order polynomial term has greater influence on the output). The cube root transform of the results revealed an increase in the cubic gain, but a decrease in the “goodness of fit” for large variations. The lack of mismatch in this simulation case is indicated by the zero intercepts in Table 4.4.

Transistor Mismatch

In fabricated transistors, differences in channel width, channel length, oxide thickness, etc. between devices can cause mismatch. As an example of transistor mismatch, the widths of M1 (transistor with input $2v_i$) and M2 (transistor with input $-v_i$) were each separately increased by 1%. Larger mismatches in transistor parameters yield significant errors in the output. Through special layout techniques that are described in Section 5.1.1 and the close proximity of the cubing transistors to each other, it is intended that the transistor mismatch in the circuit will be reduced, similar to the work shown in [46].

The simulation results are plotted in Figure 4.8 and compared against an ideal curve (gain= $4.0V^{-2}$) and an output response with no mismatch (0%). DC offsets measuring 1.9mV were removed in the absolute error plot of Figure 4.8(b).

The cubicity measures applied to these two simulation cases are summarized in Table 4.4. In both cases, the transistor mismatch prevents complete cancellation of second-order polynomial terms and allows for greater influence of the linear terms at the output. This is indicated by increased PP^2 maximums and increased linear crossover points.

(a) Effect of Transistor Mismatch on v_{out} (transistors M1 and M2 incur 1% width increase).

(b) Absolute Error Voltage.

Figure 4.8: Transistor Mismatch Simulation Results.

The cube root transform results reveal that the mismatch of transistor M1 causes a more severe change in the cubic gain ($\Delta\alpha = 1.05V^{-2}$) than the mismatch of M2 ($\Delta\alpha = 0.39V^{-2}$). This is understandable, given that M1 is fed with a larger input voltage ($2v_i$). The opposite polarity of the inputs to M1 and M2, $2v_i$ and $-v_i$, respectively, explains why the cubic gain of the M1 mismatch case decreased while the cubic gain of the M2 mismatch case increased. The non-zero intercepts in both cases indicate the presence of mismatch in the output. The “goodness of fit” in the M1 mismatch case is much worse ($R^2=0.91024$) than the M2 case ($R^2=0.99714$) indicating the severity of the mismatch.

Judging from the absolute error plots and the cubicity performance measures, the effects of mismatch in transistor parameters on the cuber performance is more severe than resistor mismatch. There is therefore a justifiable need to pay special attention to the transistor layout.

Transistor Variation

In the next mismatch case, the widths of all transistors (M1 to M6) were simultaneously increased by different amounts (5% and 10%) and plotted. These two cases are compared with the 0% mismatch response and an ideal curve (gain=4) in Figure 4.9(a). The error curves are plotted in Figure 4.9(b).

Figure 4.9: Transistor Variation Simulation Results.

By increasing the widths of all transistors at the same time, no mismatch is created as the operating points are identical (as indicated by the zero values of the PP² percentages and the zero intercept values in Table 4.4).

Increasing the transistor widths decreases the PP⁵ percentages at the output, but the linear cross-over point increases (indicating that the transistors' behaviour is becoming more linear and less influenced by fifth-order power terms).

The cube root transform of the results reveals that the cubic gain increases as the width is increased. A 5% increase in width causes a greater increase in the gain ($\Delta\alpha = 0.29V^{-2}$) than a 5% increase in load resistance ($\Delta\alpha = 0.10V^{-2}$).

Non-ideal Differential Input Voltages

For the circuit to correctly cancel the even order terms of the Taylor series expansion of the transistor behaviour, the input voltages must be: v_i , $-v_i$, $2v_i$ and $-2v_i$. If the input voltages are not completely differential, error will be introduced at the output. To simulate this, the following input voltage combinations were applied to the circuit. They keep the voltage doubling characteristics of the input but introduce varying degrees of non-ideal differential characteristics.

- Case 1%: v_i , $-1.01v_i$, $2.02v_i$ and $-2v_i$
- Case 5%: v_i , $-1.05v_i$, $2.10v_i$ and $-2v_i$
- Case 10%: v_i , $-1.10v_i$, $2.20v_i$ and $-2v_i$

Figure 4.10 shows the effect of non-ideal differential input voltages on the output.

Figure 4.10: Non-ideal Differential Input Voltages Simulation Results.

Figure 4.10(b) shows the corresponding absolute error voltages. The shape of the output response is distorted for negative v_{id} , as observed by the antisymmetric absolute

error curves in Figure 4.10(b). The presence of the non-zero PP² percentages and the non-zero intercepts listed in Table 4.4 indicate the severity of the differential input mismatch. The cube root transform results reveal that the cubic gain for these simulation cases is increased, but the fit is noticeably worse.

Non-Ideal Input Voltage Doubling

For the circuit to correctly cancel the linear terms of the Taylor series expansion of the transistor behaviour, the input voltages must be: v_i , $-v_i$, $2v_i$ and $-2v_i$. If the voltage doubling is not accurate, error will be introduced in the output. To simulate this, the following input voltage combinations were applied to the circuit. They keep the differential voltage characteristics of the input but introduce varying degrees of non-ideal doubling characteristics.

- Case 1%: v_i , $-v_i$, $2.02v_i$ and $-2.02v_i$
- Case 5%: v_i , $-v_i$, $2.10v_i$ and $-2.10v_i$
- Case 10%: v_i , $-v_i$, $2.20v_i$ and $-2.20v_i$

Figure 4.11(a) shows the differential output voltage and the effect of non-ideal input voltage doubling. Figure 4.11(b) shows the corresponding absolute error voltages.

Significant distortion of the cubic output occurs as the severity of the non-ideal voltage doubling is increased. Since the linear terms of the polynomial output expression are no longer being successfully cancelled as a result of the input voltage combinations, the output response becomes more linear than cubic. This is evidenced by the decrease in the maximum PP³ percentage and the increase in the linear crossover point. In the 1% case, the cubic gain is significantly reduced and the fit is noticeably worse. Beyond the 1% case, the cube root transformation is no longer valid since the output is predominantly linear.

Figure 4.11: Non-ideal Input Voltage Doubling Simulation Results.

4.1.6 Parasitics

Parasitic resistances can have a negative effect on the accuracy of the cubing circuit output as they affect the operating points of the transistors, thereby introducing mismatch and changes in cubing behaviour. Figure 4.12 displays the results of a DC simulation of the extracted layout with parasitic resistances. Equation 4.1.14 shows the polynomial results of the curve-fitting of the extracted output response.

$$v_{out} = -0.00220v_{id} + 0.00058v_{id}^2 + 3.98v_{id}^3 - 0.00583v_{id}^4 + 26.8v_{id}^5 - 1100v_{id}^7 + 7480v_{id}^9 - 16200v_{id}^{11} \quad (4.1.14)$$

The maximum PP³ is 87.5%. This is a decrease of 3% from the polynomial fitting done in Section 4.1.3 (90.5%). The presence of the second-order term is an indication of the mismatch that is observed in the error curve of Figure 4.12. Due to this observed mismatch, the cubic gain reported in Table 4.4 is lowered ($3.90V^{-2}$), the coefficient of determination, R^2 , is reduced (0.996699), and a small intercept exists (0.0034) after the cube root transformation.

Figure 4.12: The extracted Cubing Circuit Differential Output Response (v_{out}) is plotted versus the Differential Input Voltage (v_{id}) and compared to an Ideal Cubing Response with a gain of $4.0V^{-2}$. The Absolute Error Curve indicates the precision of the circuit; its axis is on the right side of the plot.

4.1.7 Cubicity Comparison

The DC cubicity measures proposed in Section 3.3.1 (polynomial proportionality percentages) and 3.3.2 (cube root transform “goodness of fit”) are reported in Table 4.4 for each of the previously discussed simulation cases. In addition, the DC results of the sub-threshold (Appendix B) and triode (Appendix C) cubers are also reported in the table.

Table 4.4 lists three polynomial proportionality percentages: quadratic (PP^2), cubic (PP^3), and quintic (PP^5) and the linear crossover point for each simulation case. A perfect cubing circuit would have a cubic percentage of 100%, zero percent for all other proportionality percentages, and a linear crossover point of zero.

Table 4.4 also provides a summary of the cubicity performance measures (α and R^2) determined from the linear regression of the the cube root transformation of the output responses shown in the previous sections. For a perfect cubic response, the intercepts resulting from the linear regression should be zero. If the calculated values for the intercepts were less than 10^{-6} , they are reported in the table as zero as their value has more to do with significant digit error than the presence of an actual intercept. A non-zero intercept value indicates that mismatch has occurred and the cube root transformation method is beginning to fail due to the presence of power terms other than the cube term. The cubicity measures for output responses that caused the transform method to fail are not shown and are indicated by 'F'.

All performance measures of the saturation cuber were calculated using data with the same input range (v_{id} : -0.19V to 0.19V). The input range for the sub-threshold cuber was v_{id} : -0.15V to 0.15V, and the range for the triode cuber it was v_{id} : -0.3V to 0.3V.

By examining the results in Table 4.4, several observations can be made. Only the simulation cases involving mismatch and non-differential inputs cause voltage offsets to appear at the output. These are evidenced by the presence of non-zero PP² percentages in and transform intercepts in Table 4.4. The output voltage offsets are usually accompanied by a decrease in the coefficient of determination (R^2), as the shape of the output is usually distorted by the mismatch.

Increases in transistor widths and resistor values cause increases in cubic gain. In the case of resistor value increases, it was noted that as the maximum PP³ percentages increased, the maximum PP⁵ percentages would also increase, creating a trade-off between cubing gain and the "goodness of fit".

The circuit is shown to be susceptible to non-ideal voltage doubling. Beyond a 1% deviation, the linear terms of the output polynomial expression dominate the cubic terms.

Cuber	Simulation Case	Percent Change	Max. PP ² (%)	Max. PP ³ (%)	Max. PP ⁵ (%)	Linear Crossover (mV)	Cubic Gain α (V^{-2})	Cube Root Transform Intercept	CoD R^2
SAT	Predicted	0	0	92.2	12.9	20.9	-	-	-
SAT	Simulated	0	0	90.4	14.9	17.9	3.95	0	0.99973
SAT	Resistor Mismatch	5	2.77	89.3	15.1	17.5	4.00	-0.00058	0.99971
		10	4.80	88.5	15.3	17.0	4.05	0.00064	0.99961
SAT	Resistor Variation	5	0	90.7	15.5	17.0	4.05	0	0.99984
		10	0	91.1	16.0	15.9	4.13	0	0.99966
SAT	Transistor Mismatch	1(M1)	0.460	72.4	14.2	54.8	2.90	-0.00075	0.91024
		1(M2)	1.09	82.8	14.4	31.8	4.34	0.00014	0.99714
SAT	Transistor Variation	5	0	89.6	7.08	25.0	4.24	0	0.99971
		10	0	89.9	2.38	29.6	4.52	0	0.99973
SAT	Non-Ideal Differential Input Voltages	1	5.81	87.2	14.1	19.1	4.01	-0.0013	0.99973
		5	19.2	78.7	11.0	23.4	4.22	-0.0072	0.99949
		10	26.9	72.7	6.90	28.0	4.46	-0.015	0.99893
SAT	Non-Ideal Input Voltage Doubling	1	0	65.9	12.7	73.7	2.06	0	0.76843
		5	0	48.7	6.32	144.1	F	F	F
		10	0	45.5	0.602	178.8	F	F	F
SAT	Resistive Parasitics	0	0.31	87.5	14.2	23.5	3.90	0.0034	0.99669
SUB	Predicted	0	0	89.3	13.8	22.0	-	-	-
SUB	Simulated	0	0.015	85.2	13.1	29.3	-50.4	0	0.99985
SUB	Resistive Parasitics	0	0.32	78.9	11.3	36.7	-35.5	-0.00697	0.99367
TRI	Predicted	0	0	97.2	3.11	24.0	-	-	-
TRI	Simulated	0	0.24	99.5	0.56	5.1	0.866	0	0.99997
TRI	Resistive Parasitics	0	3.19	97.2	1.20	16.6	1.00	-0.00016	0.99898

Table 4.4: PP percentages and cube root transform results (Cubic Gain, Intercept and Coefficient of Determination (CoD)) are reported for all DC simulations, including those for the Sub-threshold (SUB) and Triode (TRI) cubers. The 'F' indicates that the cube root transformation has failed and the results are therefore not shown. All DC offsets have been removed. All results are determined within each circuit's input range: saturation (v_{id} : $\pm 190\text{mV}$), sub-threshold (v_{id} : $\pm 150\text{mV}$), and triode (v_{id} : $\pm 300\text{mV}$).

This is expected since the voltage doubling is the mechanism within the design that is responsible for cancelling linear behaviour.

In general, the inclusion of extracted resistive parasitics from the layout of the cubing circuits causes a decrease in the gain. The exception is the triode cuber which benefits from an increase in gain, but which is subject to a reduced R^2 value, indicating that the fit has deteriorated.

4.2 Time Domain Simulations

Time domain simulations results are reported in Section 4.2.1. Simulations that take into account extracted parasitic capacitances and the anticipated capacitive loading due to the measurement setup are shown in Section 4.2.2. A comparison between ideal and simulated time domain cubing responses is given in Section 4.2.3. Simulated input phase delay is reported in Section 4.2.4.

4.2.1 Time Domain Response (No Load)

In Figure 4.13(a), multiple time domain differential output response curves (corresponding to a range of inputs with the same amplitude: $v_{id} = 0.18\text{V}$, but different frequencies) are overlaid on a normalized time axis, where T is the period of the waveform. With no load on the circuit, the circuit retains its sine cubed shape up to 1GHz.

Figures 4.13(b) and 4.13(c) show the time domain responses of the v_{out+} and v_{out-} nodes, respectively, under the same testing conditions. Interestingly, changes to the sine cubed shape of the waveform are observed for frequencies as low as 50MHz. The differential nature of the circuit helps to eliminate even order harmonics in v_{out} , however even order harmonics appear in the output nodes v_{out+} and v_{out-} since these nodes do not benefit from differential subtraction.

(a) Time domain v_{out} voltage (no load).

(b) Time domain v_{out+} voltage (no load).

(c) Time domain v_{out-} voltage (no load).

Figure 4.13: Saturation Cuber Time Domain Results (no load): v_{out} , v_{out+} and v_{out-} voltage plots are overlaid on a normalized time axis (where T is the period of the waveform), for a range of input frequencies with the same input amplitude ($v_{id} = 0.18V$).

4.2.2 Time Domain Response (With Load)

In the RoF predistortion application discussed previously in Section 2.2, the cubing circuit would be part of an integrated design and would be loaded with only high-impedance on-chip loads (MOSFET gate capacitances). To test the the cubing performance off-chip in a practical testing environment, the circuit will need to be driven and loaded with off-chip sources and probes. This will most certainly decrease the useful operating bandwidth of the circuit, but should provide proof-of-concept of its operation.

A test bench that models the anticipated loading of the circuit within its testing environment is shown in Figure 4.14. The bondwire and output load models are discussed later in Section 5.2. The gate bias voltages are applied by the ports, V_{DD} is applied by a 1.8V source, and the 1.2mA reference current is delivered using the 953 Ω resistor.

Figure 4.14: The schematic diagram of the test bench used for time domain simulations is shown. The bondwire and output load models are described in Section 5.2.

Figure 4.15 displays the time domain simulated results, which also include extracted parasitic capacitances from the layout (discussed in Section 5.1).

Figure 4.15: Saturation Cuber Time Domain Results (with load): Output response curves are overlaid on a normalized time axis (where T is the period of the waveform), for a range of input frequencies with the same input amplitude ($v_{id} = 0.18V$). The capacitive nature of the load contributes to the degradation of the output response shape at high frequencies ($\geq 100MHz$).

The capacitive nature of the loading at the output acts as a low-pass filter and serves to attenuate high frequencies. Cubed outputs are particularly affected since the third-order term of the output response ($\sin 3\omega_1 t$ of Equation 2.3.2) appears at three times the fundamental frequency. Attenuation of this term results in degradation of the output waveform shapes as the frequency increases ($\geq 100MHz$). Further analysis of the frequency response of this circuit is given in Section 4.3, which reports the PSS simulation results and the cubic bandwidth.

4.2.3 Expected Time Domain Cubing Behaviour

In order to compare the shape of the simulated time domain response with the expected response (Equation 2.3.2), the cubic sinusoid of Equation 4.2.2 was plotted alongside the cubing circuit response to a 1MHz, 0.18V sinusoid input. The result is shown in Figure 4.16. The absolute difference between the two curves is less than 0.8mV over two periods of the waveform.

$$\text{Expected} = \alpha (v_{id} \sin(\omega t))^3 \quad (4.2.1)$$

$$= 4.0 (0.18 \sin(2\pi (1\text{MHz}) t))^3 \quad (4.2.2)$$

Figure 4.16: Saturation Cuber Time Domain Simulation (with anticipated measurement loading): Output response to an input v_{id} with 180mV amplitude and 1MHz frequency. A curve emulating the expected response (Equation 4.2.2) of this circuit is also plotted.

4.2.4 Simulated Input Phase Delay

In the simulation environment, the four input signals ($2v_i$, $-2v_i$, v_i and $-v_i$) are perfectly in phase. However, in a practical testing environment, this is an unrealistic achievement. As will be discussed in Section 5.2.2 of the Implementation and Testing Chapter, transformers are used to generate the differential input signals and they suffer from performance issues such as phase imbalance. Figure 4.17 displays the simulation results for the case where the $2v_i$ signal was out of phase with the other signals by varying degrees.

Figure 4.17: Input Phase Delay (input $2v_i$ leads the other inputs by varying degrees).

Degradation of the sine cubed shape of the waveform occurs as the phase delay is increased. Ideally, when the output is zero, its slope should be zero at that point in time. However, the phase delay prevents the complete isolation of the time domain cubing response and allows linear and even order terms to appear at the output. Phase imbalance introduced by the transformers will be inevitable and the measured results will contain some degradation in their output cubing response at the zero crossings.

4.3 PSS Simulations

For linear circuits, AC analyses are used to determine the frequency response; however, the transistor linearization applied in this method prevents it from being used in circuits that rely on the non-linear behaviour of its devices. Fortunately, the frequency response of non-linear circuits (especially those that involve frequency translation, like cubers) can be determined by a parametric frequency sweep of PSS simulations.

PSS simulations were employed to quantify the cubic bandwidth (Section 4.3.1), to determine the steady-state cubicity by the input referred intercept points (Section 4.3.2), and to verify the input impedance of the circuit (Section 4.3.3).

4.3.1 Cubic Bandwidth

As mentioned in Section 3.3.3, PSS simulations can be used to gather a series of steady-state responses over different input frequencies and convert them into their component tones. The output response of a cubing circuit to a sinusoidal input should have two tones: one at the fundamental and the other at the third harmonic, where the fundamental tone is three times as large as the third harmonic. Figure 4.18 shows the simulated responses (with and without loading) for an input signal with amplitude 0.18V over a range of frequencies. The cubic bandwidth is the frequency range over which the ratio of the fundamental and third-order tones remains at the ideal ratio of three. Figure 4.19 plots the ratio versus the input frequency.

In the unloaded circuit response of Figure 4.18, the fundamental and third-order tone amplitudes remain constant with frequency until they approach 1GHz. The cubic bandwidths of the unloaded and loaded circuit responses are quantified by determining from Figure 4.19 when the ratio of the fundamental and third-order tone amplitudes deviates by 10% from the ideal ratio of three. In the case of the unloaded circuit response, the

Figure 4.18: Saturation Cuber: the fundamental and third-order tones versus input frequency are shown for the simulated (with and without loading).

Figure 4.19: Saturation Cuber: ratio of the fundamental and third-order tones versus input frequency are shown for the simulated (with and without loading).

cubic bandwidth is beyond 1GHz (any simulations of the mixed signal model beyond this frequency are suspect as they do not take into account the distributed gate resistance of the MOSFET [47]). The cubic bandwidth of the loaded circuit response is 100MHz. As anticipated from the time domain plots of Section 4.2.2, the addition of capacitive loading to the circuit decreases the frequency response. The phase difference between the fundamental and third-order tones was also observed. Within the 100MHz bandwidth, the phase difference deviated less than 20 degrees from the ideal difference of 180 degrees.

As mentioned in Section 3.3.3, the bandwidth of the circuit relies on the cubicity of the circuit which changes depending on the input amplitude. PSS simulations were run for several different amplitudes and the fundamental/third-order ratio and phase differences are summarized in Figure 4.20. As expected the input amplitude does have an effect on the bandwidth. In order to compare the simulated results with the measured results of Chapter 5, the bandwidths will be compared at the same input amplitude ($v_{id}=180\text{mV}$).

(a) Fundamental/Third-Order Ratio vs frequency.

(b) Phase Difference vs frequency.

Figure 4.20: Changes in Cubic Bandwidth resulting from changes in input amplitude are examined. Input $v_{id}=250\text{mV}$ is well outside the input range of this circuit, but it illustrates that for larger input amplitudes the fundamental/third-order ratio deviates from the ideal ratio of three. Within the input range, the bandwidth for small inputs is observed to be reduced (36MHz).

Additionally, a trade-off was noted between gain and bandwidth: increases in gain are met with decreases in cubic bandwidth. Table 4.5 reports cubic gain and bandwidth results over a range of bias voltages (for the same input $v_{id}=180\text{mV}$).

V_{BIAS} (V)	Gain (V^{-2})	Bandwidth (MHz)
1.4	4.07	80
1.5	3.91	100
1.6	3.71	110

Table 4.5: Tabulated Results of Bias Voltage (V_{BIAS}) versus Cubic Gain and Bandwidth.

4.3.2 Harmonic Distortion Measures

Figure 4.21 plots the first-, third- and fifth-order harmonics (H1, H3 and H5, respectively) of the output response of the cubing circuit to a 1MHz input over a range of input amplitudes. The even order harmonics were negligible, as would be expected from a differential circuit.

For a range of input amplitudes (approximately 10 to 200mV), the first and third harmonics are parallel with a slope of three (indicating that their amplitudes are cubing correctly, see Equation 2.3.2) and are separated by a constant distance (corresponding to a factor of three, the ideal ratio). For small input amplitudes (less than 10mV), the fundamental tone has a slope of one, indicating that at these amplitudes the response is mainly linear. This confirms what was observed as the linear cross-over point of Section 4.1.2 (Figure 4.2 and Table 4.2).

As explained in Section 3.3.4, the third-order harmonic distortion measure (IIP3) is not an appropriate performance measure for cubing circuits, but the fifth-order (IIP5) is appropriate. Figure 4.21 indicates the IIP5 of this circuit (for a single-tone test) is 1.84V. Unfortunately, none of the authors of the cubing circuit papers reported in the literature

Figure 4.21: Odd order output harmonics are plotted versus input amplitude for a 1MHz input. The cuber is loaded with the anticipated measurement load. The slopes of the first- and fifth-order harmonics are extrapolated to determine the fifth-order input referred intercept point (IIP5): $v_{id}=1.84V$.

review disclosed the IIP5 of their circuits. At the end of this chapter in Section 4.4, the IIP5 results of this cuber will be compared to the IIP5 results of the sub-threshold and triode cubers, reported in Appendix B and Appendix C, respectively.

4.3.3 Input Impedance

As previously stated in Section 3.5, the input impedance of the circuit must be large to allow the input signals to be effectively delivered through the input network (described in Section 5.2.2).

Figure 4.22 plots the input impedance magnitude for two input nodes: $2v_i$ and v_i . The simulation includes the anticipated loading of the measurement test setup and the extracted parasitic capacitances of the layout. (Impedances for inputs $-2v_i$ and $-v_i$ are

not shown since they are identical to inputs $2v_i$ and v_i , respectively.)

Figure 4.22: The magnitude of the input impedance of input nodes $2v_i$ and v_i are shown versus frequency. The anticipated measurement loading and parasitic capacitances are included in the simulation. The negative linear slope indicates that the impedance is mainly capacitive (values indicated on the figure).

The negative slopes of the impedances shown in Figure 4.22 are an indication that the output is mainly capacitive (approximately 1.05pF and 1.35pF for inputs $2v_i$ and v_i , respectively). Up to 100MHz, the impedance of the inputs are greater than $1\text{k}\Omega$, which for the purposes of the input network is sufficiently large. However, as the frequency increases beyond this point, the lowered impedance will start to affect the voltage transfer to the circuit. The amplitude and phase of the input signals will start to degrade beyond this point and affect the cubic output.

4.4 Results Comparison

A summary of the results presented in this chapter is given in Table 4.6. Simulation results for the sub-threshold and triode cubing circuits are also given.

Performance Measure	Units	Saturation Cuber	Sub-threshold Cuber	Triode Cuber
Input Range (v_{id})	V	± 0.19	± 0.15	± 0.3
Gain: Predicted	V^{-2}	4.57	-60.6	0.89
Gain: Graphed	V^{-2}	4.0	-50	0.87
Gain: Polynomial	V^{-2}	3.93	-63.7	0.862
Gain: Polynomial (E-R)	V^{-2}	3.98	-40.9	1.03
Gain: Cube Root Transform	V^{-2}	3.95	-50.4	0.866
Gain: Cube Root Transform (E-R)	V^{-2}	3.90	-35.5	1.00
Total Direct Current Draw	mA	7.18	7.11	5.85
Maximum PP^2 (E-R)	%	0.31	0.32	3.19
Maximum PP^3 (E-R)	%	87.5	78.9	97.3
Maximum PP^5 (E-R)	%	14.2	11.3	1.20
Linear Crossover Point (E-R)	mV	23.5	36.7	16.6
Coeff. of Determination (E-R)	-	0.99669	0.99367	0.99898
Cubic Ratio (E-C)	-	3.09	2.98	2.98
Cubic Bandwidth (E-C)	MHz	100	80	120
IIP5 (E-C)	V	1.84	0.63	1.77

Table 4.6: Simulation Results Comparison for all three cubing circuits: saturation, sub-threshold, and triode. Simulated results do not include parasitics unless indicated by: E-R (simulated with extracted resistors) or E-C (simulated with extracted capacitors). The bandwidth of the saturation cuber was determined for an input of $v_{id}=180\text{mV}$ (Sub-threshold cuber: $v_{id}=130\text{mV}$, and triode cuber $v_{id}=230\text{mV}$).

Drawing comparisons between the cubing circuits is difficult due to the differences between their designs. Recalling the design parameter comparison (Table 3.2 of Section 3.7), each of the cubers is fabricated with different transistor widths and load resistance values. Even the topologies differ, as the cuber biased in triode does not have a current mirror.

Keeping these differences in mind, it is possible to draw some conclusions about each of the designs. The cuber biased in saturation appears as the middle-of-the-road design. It has a moderate input range ($\pm 0.19\text{V}$), gain ($\approx 4V^{-2}$), and cubic bandwidth (100MHz).

The cuber biased in triode seems to have the purest cubic output as it has the highest PP^3 (97.3%), the lowest PP^5 (1.20%), the lowest linear crossover point (16.6mV), and the best fit according to the coefficient of determination R^2 (0.99898). It has the widest input range ($\pm 0.3V$) and highest bandwidth (120MHz), but also the lowest gain (≈ 0.86 to $1.0 V^{-2}$). The higher bandwidth has more to do with the reduced transistor sizes ($9.0\mu m$) and the lack of a current mirror (which would add capacitance) than with the region of operation.

The cuber biased in sub-threshold has a much higher gain (≈ 35 to $60 V^{-2}$), but it comes at the expense of reduced input range ($\pm 0.15V$) and reduced bandwidth (80MHz). The increase in gain is due to the increased non-linearity of the sub-threshold region. It is reasonable to expect that the sub-threshold cuber, based on typical MOSFET characteristics, would have a lower total direct current draw than the saturation cuber. However, the sub-threshold cuber has much larger transistors ($120\mu m$ as compared to $16.48\mu m$ for the saturation cuber). This could also explain the difference in bandwidth, as larger transistors introduce larger capacitances that would limit the frequency response of the circuit. Although, increased capacitance could also be due to the sub-threshold operation.

To better compare results versus the region of operation, the bias voltage of the saturation cuber was lowered from 1.50V to 0.58V to put it primarily in the sub-threshold region of operation. As mentioned in Appendix B.2.2, operating the cubing transistors in sub-threshold causes the cubing gain to be negative. The bias voltage of 0.58V was chosen so that the gain would be the same magnitude but opposite polarity to compare the performance measures. Table 4.7 lists the performance measures for the cubing circuit presented in this chapter biased in saturation and sub-threshold. All DC results were observed over the same input range (v_{id} : $\pm 0.19V$) and the cubic bandwidth results were determined with the same input amplitude ($v_{id} = 180mV$).

Performance Measure	Units	Biased in Saturation	Biased in Sub-threshold
Bias Voltage (V_{BIAS})	V	1.50	0.58
Input Range (v_{id})	V	± 0.19	± 0.19
Direct Current Draw	mA	7.18	3.1
Maximum PP ³	%	90.4	96.5
Maximum PP ⁵	%	14.9	22.5
Linear Crossover Point	mV	17.9	3.9
Gain: Cube Root Transform	V^{-2}	3.95	-3.93
CoD R^2	-	0.99973	0.99994
Cubic Ratio	-	3.09	3.07
Cubic Bandwidth	MHz	100	85
IIP5	V	1.84	0.85

Table 4.7: Simulation Results Comparison for the saturation cuber biased at 1.5V and at 0.58V (which biases it primarily in the sub-threshold region of operation).

As expected, changing the region of operation from saturation to sub-threshold reduced the direct current draw of the design. The non-linear behaviour of the sub-threshold transistors is the cause of the increased Cubic and Quintic Proportionality percentages, and the reduced Linear Crossover point. The disadvantages of operating the cubing transistors in the sub-threshold region are the reduced bandwidth and decreased IIP5.

4.5 Chapter Summary

DC simulations of the cubing circuit design proposed in Section 3.6 were presented. The two DC performance measures, Polynomial Proportionality and Cube Root Transforms, introduced in Sections 3.3.1 and 3.3.2 were applied to the circuit to evaluate its cubicity. Mismatch and variation of circuit parameters and inputs was investigated and found to have significant effects on the output. Time domain and PSS simulations were undertaken to evaluate the frequency response of the circuit. Comparisons to the sub-threshold and triode cubing circuit results were also made.

Chapter 5

Implementation and Testing

Implementation details, test setups and measurement results for the saturation cuber will be reported in this chapter. Section 5.1 discusses the layout implementation details of the design, while Section 5.2 discusses the printed circuit board (PCB) details. The measurement setup and results for the saturation cuber are reported in Section 5.3. A table comparing the results of the sub-threshold and triode results will also be shown.

5.1 Cubing Circuit Layout

The layout was submitted to the Canadian Microelectronics Corporation (CMC) for the 0404CF fabrication run along with designs from two other Masters Degree candidates. The three designs on chip ICFCUCFD shared ground connections in order to reduce ground bond wire inductance. A photograph of the entire chip is shown in Figure 5.1. The cubing circuits are positioned in the lower third of the chip.

The saturation and sub-threshold cubers were fabricated together. They share only the input connections (v_i , $-v_i$, $2v_i$ and $-2v_i$) and ground. Connections for the reference currents, the voltage supplies and the outputs were separate. Figure 5.2 and Table 5.1 illustrate the placement of the two circuits and the pad names.

Figure 5.1: Chip photograph of ICFCUCFD.

Figure 5.2: Chip photograph showing the circuit layout and bonding pad arrangement of both the sub-threshold and saturation cubers.

Pad #	Pad Name	Notes
1, 4, 6, 9, 12, 14, 17	GND	These ground pads are all interconnected, and are shared with the two other designs on the chip.
2, 3	$v_{out-,SUB}, v_{out+,SUB}$	Output pads for sub-threshold cuber.
5, 13	$I_{ref,SUB}, I_{ref,SAT}$	Reference current inputs for the cubers.
7, 8, 10, 11	$v_i, -v_i, 2v_i, -2v_i$	Shared inputs for the cubers.
15, 16	$v_{out-,SAT}, v_{out+,SAT}$	Output pads for saturation cuber.
18, 19	$V_{DD,SAT}$	Supply voltage pads for saturation cuber.
20, 21	$V_{DD,SUB}$	Supply voltage pads for sub-threshold cuber.

Table 5.1: Bonding Pad Configuration for ICFCUCFD.

A close-up view of the layout of the saturation cuber is shown in Figure 5.3. The transistor and resistor placement is indicated in the figure. A layout technique, called common centroid matching, was employed to protect the devices from mismatch due to linear gradients of process parameters. The unconnected “dummy” devices indicated in Figure 5.3 were also used to prevent mismatch. The common centroid technique, the use of “dummy” devices and other layout considerations are discussed in the next section.

Figure 5.3: Saturation cubing circuit layout in a four-metal-layer, single-polysilicon, $0.18\mu\text{m}$ n-well CMOS technology.

5.1.1 Layout Techniques and Considerations

Given the performance degradations due to component mismatch as demonstrated in Section 4.1.5, there is a need for compensatory layout techniques when implementing the cubing circuit.

A popular method of component matching for IC layouts is “common centroid” [48],

which involves special geometric placement of matched components around a center point. This layout technique provides good rejection against linear temperature gradients and gradients of process parameters that generate component mismatch. Given the susceptibility of the cubing circuit to both transistor and resistor mismatch, common centroid matching was used for the layout.

To facilitate layout design, each of the six cubing transistors has a multiplicity factor of eight. The smaller transistors were more easily placed within a common centroid arrangement. Similarly, each of the two load resistors ($R_L = 200\Omega$) were divided into 12 parallel resistors (approx $2.4\text{ K}\Omega$).

In addition to process parameter linear gradients, edge effects occurring during device formation can also generate mismatch. To compensate for edge effects, identical “dummy” devices are placed equidistant from the matched devices around the outer edges of the common centroid arrangement. These devices, which are not connected to the circuit and have all their terminals shorted together, are indicated with the label “dummy” in Figure 5.3.

In this layout, the power and ground signals were routed first to ensure that they were carried on the lowest level metal to avoid parasitic resistances from unnecessary vias. This was done at the expense of additional capacitance to the substrate because via resistance can vary greatly across the chip.

Ground bounce is a term that refers to a voltage increase in the on-chip ground due to transient (or static) current flow through inductive (or resistive) leads [44, pp. 57-9]. There are seven ground pads in this design as labelled in Table 5.1 and Figure 5.2. The inclusion of extra ground pins lowers the overall bond wire resistance and inductance, and decreases the effect of ground bounce on the circuit [49, p. 74]. A similar effect can be observed on the voltage supply, therefore more than one pad and bond wire were allocated

to the two voltage supplies on the chip.

The spacing of devices within the common centroid arrangement was governed by the design rule for metal-metal spacing. In all cases, multiple parallel vias and contacts were used where possible to minimize parasitic resistances.

Care was taken during the design of the layout to account for the current densities present in the metal output traces. Enlarged traces were used to accommodate the expected currents. A guideline of $1\mu\text{m}$ of conductor width for every mA that it carries was applied [44, p. 54]. It is expected that the larger traces will have more parasitic capacitances and may limit the frequency response of the fabricated circuit.

Ten 200fF MIM bypass capacitors were used between V_{DD} and ground to reduce high-frequency noise (this topic will be further discussed in Section 5.2.1). These capacitors were found in the CMC cell library and have an extracted parasitic capacitance of 344fF.

A typical bonding pad size of $100\mu\text{m}$ by $100\mu\text{m}$ [44, p. 45] and a pitch of $150\mu\text{m}$ were chosen, as they allow for enough space for a bonding machine to touch down on each of the pads. The chip-on-board bonding is further discussed in Section 5.2.3.

On-chip electrostatic discharge (ESD) protection for the gates of the cubing transistors was provided by substrate diodes. As stated in [44, p. 67], this protection scheme relies “on a diode becoming forward biased and providing a low-impedance path to pull the excessive charge away from the MOSFET gate”. The disadvantage is that parasitic capacitances of the diodes could increase the capacitance of those input lines and negatively affect the frequency performance of the chip.

5.1.2 Sub-threshold and Triode Cuber Layouts

The layouts of the sub-threshold and triode cubers are discussed in Appendix B.3 and Appendix C.3. A comparison of the layouts is given in Table 5.2.

Layout Parameter	Saturation Cuber	Sub-threshold Cuber	Triode Cuber
Area without pads (mm^2)	0.015	0.0165	0.0081
Area with pads (mm^2)	0.913*	0.913*	0.1925
# of Input Pads	4*	4*	4
# of Output Pads	2	2	2
# of Supply Pads	3	3	1
# of Ground Pads	7*	7*	1

Table 5.2: Comparison of layout for the three different cubing circuits. The * indicates that the saturation and sub-threshold cubers share the pads.

5.2 Printed Circuit Board Design

Given the differential nature of the circuit and the complexity of generating the four inputs ($2v_i$, $-2v_i$, v_i and $-v_i$) to the cubing circuit, testing the fabricated design was done by bonding the chip to a PCB in lieu of wafer-probing. Since the simulations revealed that the predicted capacitive loading limits the frequency response of the circuit, the upper target of bandwidth for the PCB will be 200MHz.

The PCB was designed to support both the saturation and sub-threshold cubers on one board. The triode cuber required its own PCB, which is described in Appendix C.3. Both PCBs were fabricated by CMR Summit Technologies on the same two-layer, 62mil panel with an FR4 substrate.

Figure 5.4 shows the PCB schematic for testing the saturation and sub-threshold cubers, Table 5.3 lists the Bill of Materials (BOM) and Figure 5.5 shows this PCB's layout. A picture of the populated board is shown in Figure 5.6.

5.2.1 Power Supply

To power the cubing circuit, a 1.8V voltage supply, a 1.5V bias voltage supply and a 1.2mA reference current are required. The following subsections go into more detail about how they are supplied to the chip on the PCB.

Figure 5.4: PCB Schematic Diagram.

Component	Ref. Des.	Value	Part Number	Manufacturer
Capacitors	C1, C2, C5, C6	10 μ F	T491B106K010AS	Kemet
	C3, C7	0.01 μ F	GRM188R71H103KA01	Murata
	C4, C8-C13	0.1 μ F	GRM188R71C104KA01	Murata
	C14-C17	100pF	GRM1885C2A101JA01	Murata
Connectors	J1, J2, J5, J6	1x3	22-03-2031	Molex/Waldom
	J3, J7-J10	SMA	142-0701-201	Johnson
	J4	1x2	22-03-2021	Molex/Waldom
Resistors	R1, R2	100 Ω	ERJ-3EKF1000V	Panasonic
	R3	40.2 Ω	ERJ-3EKF40R2V	Panasonic
	R4	200 Ω	ERJ-3EKF2000V	Panasonic
	R5-R8	10K Ω	ERJ-3EKF1002V	Panasonic
	R9, R10	49.9 Ω	ERJ-3EKF49R9V	Panasonic
	R11-R18	0.1 Ω	ERJ-3RSFR10V	Panasonic
Potentiometer	R19	100 Ω	3269-W-1-101	Bourns
CMOS chip	U1	-	ICFCUCFD	TSMC
Ferrite Bead	U2, U3	1K Ω	BLM21AG102SN1D	Murata
Transformer	U4, U5	1:1	T1-1T-KK81	Mini-Circuits
Current Src	U6	-	LM334Z	National Semi.
Diode Array	U7	-	NUP4301MR6T1-D	ON Semi.
Zener Diode	U8, U9	-	DS9502	Maxim-Dallas

Table 5.3: Cubing Circuit PCB Bill of Materials.

(a) Top side.

(b) Bottom side (as seen through the top).

Figure 5.5: Top and bottom sides of PCB Layout are shown.

Figure 5.6: Picture of populated two-layer, 62mil PCB board with an FR4 substrate.

DC Voltage Supply: V_{DD}

The 1.8V supply required by the cubing circuit is provided by a Keithley Sourcemeter (part number: 2400-LV) attached to pin 3 of connector J1. A jumper applied to connector J6 allows the the supply voltage to be connected to either the sub-threshold cuber (by shorting pins 1 and 2) or the saturation cuber (by shorting pins 2 and 3).

It is common practice in PCB design to add bypass capacitors from the power supply to ground in order to reduce ground bounce effects from short-term transient surges of current [49–51]. As stated in [51], many capacitors are placed in parallel to achieve low impedance in the power distribution system for a wide range of high-frequency transient frequencies. Parasitic inductance in capacitor packages cause those capacitors to appear inductive above their self-resonant frequencies. Multiple, parallel capacitances with a range of values are needed to counteract this effect and reduce the impedance at high frequencies. In the schematic of Figure 5.4, capacitors C1-C4, C10 and C12 are employed as bypass capacitors for the power supply.

In addition to the bypass capacitors, ferrite beads are also used in PCB design for high-frequency noise reduction in the power supply.

Ferrite materials are basically nonconductive ceramic materials that differ from other ferromagnetic materials such as iron in that they have low eddy-current losses at frequencies up to hundreds of megahertz. Thus they can be used to provide selective attenuation of high frequency signals that we may wish to suppress. [52, p. 306]

In the schematic of Figure 5.4, the reference designator U2 indicates the ferrite bead placed between the power supply and the IC supply V_{DD} . Further properties and specifications of this part can be found in [53].

ESD protection of the voltage supply lines is provided by zener diodes with voltage snap-back protection: U8 and U9 for the sub-threshold and saturation cubers, respectively.

During normal operation (cathode connected to V_{DD} and anode connected to ground), the DS9502 behaves as a regular diode; however, if an ESD voltage exceeds the trigger voltage (9.0V), the I/V characteristic of the device will “snapback” allowing current to flow, but at a lower voltage [54]. Once device operation falls below the holding levels (5.5V or 30mA), the device will return to normal mode and behave as a zener diode again with only a small leakage current (30nA). C11 and C13 were placed as bypass capacitors for U8 and U9, respectively. Further specifications for these diodes can be found in the product datasheet [54].

DC Bias Voltage Supply: V_{BIAS}

Similar to the 1.8V voltage supply, this 1.5V bias voltage supply is also provided with bypass capacitors (C5 to C8) and a ferrite bead (U3) for noise reduction. The bias voltage is applied to the transistor gates via the center taps of the transformers (U4 and U5). An alternative biasing strategy involves replacing R11 to R14 with coupling capacitors and populating R5 to R8 with bias resistors.

DC Current: I_{ref}

The 1.2mA current reference can be provided on the board with the use of an adjustable current source, U6, (whose operation is described below) or with a lab current source (Keithley Sourcemeter 2400-LV) applied to pin 1 of connector J4. Connector J4 also allows the current of the on-board current source to be measured by applying an ammeter in series. With the use of a jumper, connector J5 allows the reference current (be it on or off-board) to be applied either to the sub-threshold cuber (by shorting pins 1 and 2) or the saturation cuber (by shorting pins 2 and 3).

The current supplied by the on-board current source (U6: part number LM334Z) is made adjustable by a potentiometer (R19). The required resistance value to set the

supply current to 1.2mA was determined from Equation 5.2.1 which was provided in the LM334Z datasheet [55]. A 100Ω potentiometer was selected to provide adjustability in the current reference.

$$R = \frac{227\mu V/^{\circ}K}{I_{ref}} \quad (5.2.1)$$

$$= \frac{67.6mV/298^{\circ}K}{1.2mA} \quad (5.2.2)$$

$$= 56.4\Omega \quad (5.2.3)$$

ESD protection of the current mirror transistors of both the sub-threshold and saturation cubers is provided by U7, which consists of an array of diodes as shown in Figure 5.7 from the product data sheet for NUP4301MR6T1-D [56]. C9 was placed as a bypass capacitor for this IC. Only two of the inputs are used: IO1 is connected to the I_{ref} input of the sub-threshold cuber and IO2 is connected to I_{ref} of the saturation cuber (IO3 and IO4 are not connected). The function of the diodes is to direct harmful ESD transients away from the inputs to the chip.

Figure 5.7: ESD Protection Diode Array Schematic (U7) from product datasheet [56].

5.2.2 Input Circuitry

Since the sinusoidal signal generator (Agilent E8257D) has an internal source resistance of 50Ω, the circuit's input network was designed to have an input impedance close to 50Ω to reduce reflections and maximize the power transfer. The output of a signal generator is fed in through a vertical SMA connector (J3). Two voltage dividers then divide this

signal by four (R1 and R2) and by two (R3 and R4), thus generating two single-ended signals where one is approximately twice as large in amplitude as the other. For example, if the signal generator is set to output $8v_i$, then the voltage dividers produce $4v_i$ and $2v_i$.

Differential signals are generated with PCB surface-mount transformers (U4 and U5). The peak amplitudes of the differential signals are half as large as the input to the transformer. Given the inputs $4v_i$ and $2v_i$, the outputs of the two transformers become the desired inputs to the cubing circuit ($2v_i$, $-2v_i$, v_i and $-v_i$).

The use of transformers within the input network to create differential signals introduces performance issues such as insertion loss, amplitude imbalance, phase imbalance, and limited input bandwidth. The transformers chosen for this design were surface mount RF transformers fabricated by Mini-circuits. The input bandwidth ranges from 80kHz to 200MHz, with the lowest insertion loss occurring in the 200kHz to 80MHz range [57].

The following subsections determine the input impedance of the input circuitry and confirm the voltage division ratios, as well as discuss the choice of widths for the PCB microstrip transmission lines.

Input Network: Impedance Calculations

Since the input impedance of the chip (Z_{chip}) is sufficiently large (Section 4.3.3) and the impedance transformation ratio is 1:1 for transformers U4 and U5, then looking into one of these transformers, only the 50Ω resistive termination (R9 for transformer U4 and R10 for transformer U5) will appear.

The voltage divider resistor values are chosen such that the overall input impedance to the input network is 50Ω and the proper division ratios are achieved. Figure 5.8 illustrates this simplified input network along with the selected values. Equation 5.2.4 confirms the desired input impedance and Equations 5.2.6 and 5.2.7 confirm the division ratios.

Figure 5.8: PCB Input Impedance Network.

$$Z_{IN} = (Z_{IN,vi}) \parallel (Z_{IN,2vi}) = (R_1 + R_2 \parallel R_9) \parallel (R_3 + R_4 \parallel R_{10}) \quad (5.2.4)$$

$$= (133.3\Omega) \parallel (80\Omega) = 50\Omega \quad (5.2.5)$$

$$V_{U4} = \frac{R_2 \parallel R_9}{R_1 + R_2 \parallel R_9} V_S = \frac{33.3}{100 + 33.3} V_S = \frac{1}{4} V_S \quad (5.2.6)$$

$$V_{U5} = \frac{R_4 \parallel R_{10}}{R_3 + R_4 \parallel R_{10}} V_S = \frac{40}{40 + 40} V_S = \frac{1}{2} V_S \quad (5.2.7)$$

Looking back from each of the transformers towards the input, the impedance should also be matched to maximize power transfer and reduce reflections. Equations 5.2.8 and 5.2.11 confirm that these impedances are approximately matched to 50Ω.

$$Z_{U4} = R_2 \parallel (R_1 + Z_S \parallel (R_3 + R_4 \parallel R_{10})) \quad (5.2.8)$$

$$= 100\Omega \parallel (100\Omega + 50\Omega \parallel (40\Omega + 40\Omega)) \quad (5.2.9)$$

$$= 56.7\Omega \quad (5.2.10)$$

$$Z_{U5} = R_4 \parallel (R_3 + Z_S \parallel (R_1 + R_2 \parallel R_9)) \quad (5.2.11)$$

$$= 200\Omega \parallel (40\Omega + 50\Omega \parallel (100\Omega + 33.33\Omega)) \quad (5.2.12)$$

$$= 55.3\Omega \quad (5.2.13)$$

Input Network: PCB Microstrip Widths

As the input frequency increases, parasitic inductance and capacitance of PCB traces degrades performance. The use of microstrip transmission lines and terminating impedances, however, allows for greater input bandwidth and less reflections back into the source equipment. The Agilent Design System (ADS) software package was used to determine appropriate widths for the microstrips, and to observe s-parameter simulations of the input network.

As mentioned previously, the PCB used for testing is a two-layer board with an FR4 substrate. The PCB's substrate and conductor parameters required for the ADS simulations are summarized in Table 5.4.

Parameter	Symbol	Value
Substrate Thickness (mil)	H	57.6
Relative Dielectric Permittivity	Er	4.3
Relative Dielectric Permeability	Mur	*1.0
Conductor Conductivity (S/m)	Cond	*1E50
Cover Height (mil)	Hu	*3.9E34
Conductor Thickness (mil)	T	2
Dielectric Loss Tangent	TanD	0.015
Conductor Surface Roughness (mil)	Rough	*0

Table 5.4: Summary of PCB substrate and conductor parameters for ADS simulation. The * indicates default values within ADS.

The widths required to achieve a specified intrinsic impedance was determined by using the LineCalc tool within ADS. As an example, consider the microstrip leading from the input to R1: the impedance seen looking into R1 ($Z_{IN,vi}$) is approximately 133.3Ω . To reduce reflections, the intrinsic impedance of the line should be matched to $Z_{IN,vi}$. Using the substrate and conductor parameters of Table 5.4 and using a straight line approximation, LineCalc reports that the microstrip width should be approximately 10mil. This narrow microstrip is shown in Figure 5.5(a) between J3 and R1.

Smaller impedances required larger widths, however, the widths suggested by LineCalc were often wider than the component pads to which the microstrip lines were connected. Since the PCB was fabricated on a panel with boards from other researchers, the board parameters could not be changed. The solution was to make the lines as wide as possible and confirm the operation of the input network with ADS s-parameter simulations.

The schematic setup of the input network is shown in Figure 5.9. Unfortunately, no s-parameter data for the transformers U4 and U5 was available from the manufacturer, therefore, the input network was terminated with two 50Ω loads to represent what should be seen at those nodes. The MSUB block shown in the schematic lists the substrate and conductor parameters of the PCB. The MLIN components represent straight line approximations of the microstrip lines. The simulation results are shown in Figure 5.10.

Figure 5.9: This is the ADS Simulation Setup for verification of PCB microstrip widths.

The S_{11} result in Figure 5.10 represents the magnitude of the input reflection looking into the whole input network (Z_{IN}). The reflection is less than -20dB even up to 1GHz. The S_{22} and S_{33} results represent the magnitude of the output reflection at nodes V_{U5} and V_{U4} , respectively, which correspond to terminations #2 and #3 in Figure 5.9. These output reflections are below -20dB up to approximately 200MHz, which is the upper

Figure 5.10: ADS S-Parameter simulation results for PCB microstrips.

target of the PCB bandwidth.

5.2.3 Bonding Information

The chip was mounted with conductive epoxy directly onto the PCB and bond wires were placed by technician Laurent Mouden using the facilities at École Polytechnique in Montréal. The bond wires are aluminum and have a $25\mu\text{m}$ diameter. Using the 0.5nH per mm rule of thumb and estimating the length of the bond wires to be 2mm , the bond wires were modeled as a 1nH inductor. The capacitance of the PCB landing pads and traces were calculated using parallel plate capacitance approximations and found to be approximately 200fF . Capacitance from fringing effects will increase this amount. For the simulations with loads in Chapter 4, each input and output of the circuit had a series 1nH inductor that modeled the bond wire and a shunt 350fF capacitor that modeled the effects of the PCB capacitance.

Figure 5.11: Picture of chip showing bond wires, taken at École Polytechnique in Montréal.

5.2.4 Output Circuitry

The outputs of the circuit require a high-impedance, low-capacitance load. The cubing circuit converts its output cubing current into an output voltage via the load resistors; therefore, adding a low impedance load in parallel at the output would lower the load resistance and reduce the cubing gain. A high-capacitance load would create a low-pass filter that could attenuate the desired third-order harmonics in the cubic output.

Fortunately, a solder-in Agilent probing system that connects to the Agilent 54830 series of oscilloscopes can provide this type of loading. The 1134A is a probe amplifier that allows a differential probe head (2677A) to be connected to the oscilloscope. The input impedance spice model for this probe head (found in [58]) can be reduced to the simplified circuit of Figure 5.12, whose parameters are found in [59, p.18]. This circuit was used as the output load for the simulations of Chapter 4.

As indicated in the PCB schematic (Figure 5.4), coupling capacitors (C16 and C17) and output SMA connectors (J9 and J10) were positioned and routed on the PCB, but were not needed in the populated board. The 1134A and 2677A probing system does not use SMA connections, but instead allows for a solder-in connection. The 2677A probe tips were soldered to the landing pads of where C16 and C17 would have been placed.

Figure 5.12: Input impedance spice model of the Agilent 1130 Series Active Probe.

5.3 Measured Results

The measured results of the three designs (saturation, sub-threshold and triode cubers) were taken in the Azrieli Pavilion at Carleton University. The test setup and lab equipment that was used are shown in Figure 5.13. The DC setup required that adjustable voltage sources be applied directly to the four inputs of the circuit in place of the signal generator. The remainder of this section will summarize the results that were observed.

Figure 5.13: Measurement Test Equipment: V_{DD} and V_{BIAS} were supplied to the board by Keithley Sourcemeters. The input signal was generated by an Agilent E8257D Signal Generator. An Agilent 54830 Oscilloscope with 1134A and 2677A probe attachments were used to test the output.

5.3.1 DC Results

Unfortunately, DC results for the saturation cuber could not be directly obtained. The lack of ESD protection on each pin and the board handling required by the DC test setup caused several chips to fail. Setting up the DC measurements requires that adjustable voltage sources be applied directly to the four inputs. This involves removing an 0603 component from each input on the PCB and then soldering a wire to the landing pad of the 0603 component. The wires are then connected to adjustable voltage sources (Keithley 2602s). Even with proper ESD precautions (straps, tweezers, table mats and floor mats), three different chips suffered ESD events and failed. The failures were characterized by currents being drawn through the transistor gates (in the range of 50 to 300 μ A, or higher in the case of complete failure).

Figure 5.14 shows the differential output voltage of one of the saturation cubing circuits prior to complete failure. During the collection of the data, one or both of the M2 and M3 transistor gates were drawing 60 μ A of current from the voltage source. The measured results were fitted with a fifth-order polynomial and the expression is given in Equation 5.3.1. The output DC offset of 51.4mV was removed from the results shown in Figure 5.14. Prior to failure, the DC offset was observed as only 9mV.

$$v_{out} = -0.0514 - 0.0539v_{id} - 0.203v_{id}^2 + 3.27v_{id}^3 + 0.0273v_{id}^4 - 6.73v_{id}^5 \quad (5.3.1)$$

Interestingly, even with the failure of one transistor, a significant cubing term remains in the polynomial expression. The failure of the transistors with input $-v_i$ means that linear and second-order terms are not cancelled and are fed through to the output. This result is not unlike the non-ideal voltage doubling case (Figure 4.11(a)) observed in the simulation results of Section 4.1.5.

Fortunately, it was only the saturation cuber DC results that were not obtained. Time

domain results for the saturation cuber, as well as DC and time domain results for the sub-threshold and triode cubers were obtained prior to any ESD events. They are reported in subsequent sections and in the appendices.

Figure 5.14: Sub-threshold Cuber: the measured v_{out} response is compared to an ideal response with $\alpha = 4.0V^{-2}$ and an resistive-extracted simulation response. A polynomial was fitted to the measure response and is given in Equation 5.3.1. *The measured response and the polynomial fit are shown without the 51.4mV output DC offset.

As an alternative to true DC results, a time domain ramp function was applied to the circuit at a low frequency (1MHz) that is within the operational bandwidth of the transformers (200kHz to 80MHz), but still provides good transformer performance. The resulting output is a time domain sweep of the input voltages that approximates the DC test.

A disadvantage of using this approach is that the amplitude and phase imbalance of the transformers makes the results look worse than if they were actually taken at DC.

This is evidenced by the results comparison of Table 5.5 where DC results of the sub-threshold cuber can be compared to results obtained from a 1MHz ramp input (albeit from a different chip). The results indicate a significantly larger linear crossover point arising from linear feed-through for the response obtained for the 1MHz ramp input.

Keeping in mind the disadvantages of using the 1MHz ramp input, the remainder of this section will report on the approximate DC results of the saturation cuber that were obtained prior to device failure.

Figure 5.15: Measured v_{out+} and v_{out-} voltages are compared to those from an extracted simulation.

Figure 5.15 shows the measured output voltages at the v_{out+} and v_{out-} nodes of the circuit and compares them to those expected from simulation with extracted resistive parasitics. In the simulation results, the bias point of the outputs was found at 1.202V. The measured results reveal the bias point to be significantly lower 1.086V and 1.095V for v_{out+} and v_{out-} , respectively. The decrease in the bias points is expected to negatively affect the output of the circuit by decreasing the gain.

The differential output response is shown in Figure 5.16. A polynomial was fitted to the measure response and its expression is given in Equation 5.3.2.

$$v_{out} = -0.00820 + 0.0488v_{id} + 0.100v_{id}^2 + 3.15v_{id}^3 - 1.50v_{id}^4 - 18.5v_{id}^5 \quad (5.3.2)$$

The polynomial expression (Equation 5.3.1) determined from the damaged circuit reported a cubic gain (3.27) that is the same order of magnitude as the one observed in Equation 5.3.2. The differences arise in the magnitude and polarity of the other terms.

Figure 5.16: The measured v_{out} response is compared to an ideal response with $\alpha = 4.0V^{-2}$ and an resistive-extracted simulation response.

The DC offset observed in Figure 5.16 and Equation 5.3.2 can be removed mathematically (although in time domain tests, it can be achieved with coupling caps, in the 1MHz ramp input tests no coupling caps were used, so that the DC bias points could be observed). Figure 5.17 plots the fitted polynomial without the DC offset term.

Figure 5.17: The polynomial fit of the measured v_{out} response without the DC offset is compared to an ideal response with $\alpha = 4.0V^{-2}$ and a resistive-extracted simulation response.

The significance of the gain produced by the unwanted terms in Equation 5.3.2 is indicated in Figure 5.18, which plots the Polynomial Proportionality Percentages. The simulated percentages with extracted parasitic resistances (determined from Equation 4.1.14) are also plotted.

The measured polynomial proportionality percentages are summarized in Table 5.5 and compared to simulations. The maximum PP^3 indicated in the figure is 54.0%, which is a significant drop from the value of 87.5%, which was predicted from the resistive-parasitic extracted simulations. The output is greatly affected by the linear term, which causes a significant increase in the Linear Crossover point from 23.5 to 124.3mV. A large part of the increase can be attributed to the transformer amplitude and phase imbalance as previously discussed. Mismatch is also present in the output as evidenced by the presence of the second- and fourth-order terms, which could be caused by transformer

Figure 5.18: Extracted and Measured Polynomial Proportionality Percentages are shown versus the differential input.

amplitude and phase imbalance, as well as device mismatch.

In Figure 5.19, the cube root transformation and linear regression methods are applied to the fitted polynomial to determine the gain and R^2 of the measured result.

The presence of an intercept in the line of best fit to the cube root transformation of the measure output response indicates mismatch. This was expected, given the difference in bias voltages of v_{out+} and v_{out-} that was observed at the output in Figure 5.15.

The direct current draw of the circuit was measured as 7.17mA, and includes the 1.2mA reference current. The simulated value for the current was 7.18mA.

Measured DC Cubicity Comparison

A comparison of the simulated and measured DC cubicity results is given in Table 5.5. Results for the sub-threshold and triode cubing circuits are also summarized in the table.

In general, the measured maximum PP³ percentages reported in Table 5.5 are lower than the simulated values due to device mismatch. This decrease is accompanied by

Figure 5.19: Cube Root Transformation of Measured v_{out} Response (with the DC offset removed) is shown. The gain (α), intercept and R^2 performance measures are reported.

increased PP² percentages and linear crossover points, which are the result of incomplete isolation of the third-order polynomial term. Proportionality measures taken from the time domain data with the 1MHz ramp input reveals that more linearity appears at the output, which provide evidence of linear feed-through caused by transformer amplitude and phase imbalance (as discussed in Section 4.2.4).

The cube root transform results of Table 5.5 are inline with what was observed in the polynomial proportionality results. The measured gains are decreased from those observed in simulation. Larger transform intercepts appear indicating mismatch and consequently the measured coefficients of determination show a decrease in the “goodness of fit”. In comparing the DC results of the sub-threshold cuber and those obtained from the 1MHz ramp input, the time domain results report a better fit. This is the result of the increased number of data points in the time domain results (5,000 as opposed to only 40 for DC).

Cuber	Simulation Case	Max. PP ² (%)	Max. PP ³ (%)	Max. PP ⁵ (%)	Linear Crossover (mV)	Cubic Gain α (V ⁻²)	Cube Root Transform Intercept	CoD R^2
SAT	Predicted	0	92.2	12.9	20.9	-	-	-
SAT	Simulated	0	90.4	14.9	17.9	3.95	0	0.99973
SAT	Resistive Parasitics	0.31	87.5	14.2	23.5	3.90	0.00340	0.99669
SAT	Measured (DC)	-	-	-	-	-	-	-
SAT	Measured (1MHz ramp)	10.7	54.0	19.7	124.3	3.37	0.00187	0.96821
SUB	Predicted	0	89.3	13.8	22.0	-	-	-
SUB	Simulated	0.015	85.2	13.1	29.3	-50.4	0	0.99985
SUB	Resistive Parasitics	0.32	78.9	11.3	36.7	-35.5	-0.00697	0.99367
SUB	Measured (DC)	36.7	65.2	10.2	30.8	-31.3	0.0431	0.92575
SUB	Measured (1MHz ramp)	14.1	60.3	2.88	92.9	-41.7	0.0145	0.96957
TRI	Predicted	0	97.2	3.11	24.0	-	-	-
TRI	Simulated	0.24	99.5	0.56	5.1	0.866	0	0.99997
TRI	Resistive Parasitics	3.19	97.2	1.20	16.6	1.00	-0.00016	0.99898
TRI	Measured (Real DC)	13.0	73.1	17.4	75.2	1.01	0.00380	0.98723

Table 5.5: PP percentages and cube root transform results (Cubic Gain, Intercept and Coefficient of Determination (CoD)) are reported for all DC simulations, including those for the Sub-threshold (SUB) and Triode (TRI) cubers. All DC offsets have been removed. All results are determined within each circuit's input range: saturation (v_{id} : ± 190 mV), sub-threshold (v_{id} : ± 150 mV), and triode (v_{id} : ± 300 mV).

The total simulated and measured DC output bias voltages and current draw of the circuits (including any reference currents) are summarized in Table 5.6. The widths of the cubing circuit transistors are also included in the table, as the large transistors of the sub-threshold cuber explain why it draws nearly as much current as the saturation cuber.

Performance Measure	Units	Saturation Cuber	Sub-threshold Cuber	Triode Cuber
Cubing Transistor Width	μm	16.48	120.00	9.00
Output Bias (Sim)	V	1.202	0.915	0.285
v_{out+} (Meas)	V	1.086	0.736	0.222
v_{out-} (Meas)	V	1.095	0.750	0.228
Current Draw (Sim)	mA	7.18	7.11	5.85
Current Draw (Meas)	mA	7.17	7.01	4.40

Table 5.6: Direct Current Draw and Output Bias Voltages are listed for all three cubing circuits: saturation, sub-threshold, and triode.

The measured output bias voltages were all less than expected from simulations. The largest of the differences was observed in the measured voltages of the saturation cuber, which were as much as 0.179V less than expected. For each circuit, the measured v_{out+} and v_{out-} voltages differed due to device mismatch. The smallest difference was observed for the triode cuber.

The measured currents of the saturation and sub-threshold cubers are inline with what was expected from simulation, however, the triode cuber draws significantly less than expected. The current through the triode cuber is solely determined by the sizing of the cubing transistors, unlike the saturation and sub-threshold cubers which are driven by current mirrors. Therefore process variations could have affected the design causing the total direct current draw and the output bias voltages to be less than expected.

5.3.2 Time Domain Results

The measured time domain results will be evaluated by looking at the output waveform shapes, at the cubic bandwidth and at the harmonic distortion measures.

Output Waveform Shape

Figure 5.20: Saturation Cuber Measured Results: Time domain output response curves are overlaid on a normalized time axis (where T is the period of the waveform), for a range of input frequencies with the same input amplitude ($v_{id} = 0.18V$).

Figure 5.20 displays the shape of the measured output time domain response for a range of input frequencies. As the input frequency increases, the shape of the waveform looks less like sine wave cubed and more like just a sine wave. Figure 5.21 compares the measured response at 1MHz to the expected ($\text{gain}=4.0V^{-2}$) and simulated responses. The peak magnitude of the measured response is larger and the shape differs significantly from what was expected from simulations.

The distorted shape of the output response is an effect of the linear feed-through caused

Figure 5.21: Saturation Cuber Measured Time Domain Result is compared to the expected and simulated results of Figure 4.16. Responses to an input v_{id} with 180mV amplitude and 1MHz frequency are shown.

by device mismatch and transformer performance issues that were previously discussed. The sub-threshold and triode cuber time domain responses (reported in Appendix B.3.3) were also observed to have distorted outputs from the linear feed-through.

Of the three cubing circuits, the triode cuber is least affected by the effects of mismatch and transformer performance. Its output appears more cubic in nature and looks similar to the phase delay simulations of Figure 4.17. Perhaps the smaller transistors and smaller input capacitance of the triode cuber chip are a contributing factor in the reduced linear feed-through.

Cubic Bandwidth

The steady-state responses of the circuit to a range of different input frequencies were recorded. Fast Fourier Transforms (FFTs) were applied to determine the cubic bandwidth

of the circuit, as proposed in Section 3.3.3. Figure 5.22 plots the fundamental and third-order tones of the FFT versus the input frequency, and Figure 5.23 plots the ratio of the tones to determine the bandwidth. Comparisons to simulated results are included.

Figure 5.22: Saturation Cuber: the fundamental and third-order tones versus input frequency are shown for the simulated (with and without the anticipated measurement loading) and measured results.

In the measured results of Figure 5.22, the magnitude of the fundamental tone is significantly larger than what was expected from simulation, even though the third-order tone appears to track well with the simulations. The increase in the magnitude of the fundamental is a result of increased dominance of the linear term in the output's polynomial expression (Figure 5.18). This could be caused by device mismatch (consider the increased linear crossover points of the transistor mismatch cases listed in Table 4.4 Section 4.1.7), by transformer amplitude imbalance (consider the increased linear crossover points of the non-ideal differential and doubling cases listed in Table 4.4 Section 4.1.7) or by transformer phase imbalance (as discussed in Section 4.2.4).

Figure 5.23: Saturation Cuber: ratio of the fundamental and third-order tones versus input frequency are shown for the simulated (with and without the anticipated measurement loading) and measured results.

The increase of the fundamental magnitude with frequency is further evidence that some of the increase is due to transformer amplitude and phase imbalance, as the amplitude and phase characteristics of the transformer change with frequency. Increased linearity caused by device mismatch would not be significantly related to frequency, unless the mismatch was severe enough to affect the capacitance of the device.

The change in the fundamental tone magnitude causes the cubic ratio to increase to 6.63 instead of the simulated ratio of 3.09, as shown in Figure 5.23. The simulated cubic bandwidth in Section 4.3.1 was determined by finding the input frequencies for which the cubic ratio was within 10% from the ideal ratio of three (between 2.7 and 3.3). Since the measured cubic ratio is beyond this 10% criteria, the bandwidth was determined by averaging the ratio over the first five measurements and determining the frequencies over which the ratio stayed within 10% of that average. Using this criteria, the bandwidth is

7MHz, much less than the 100MHz that was anticipated from simulation.

Probable causes for the reduced bandwidth are increased parasitic capacitances that were not included in the simulations or transformer performance issues. Given the sensitivity of the circuit to non-ideal input amplitudes and phase delays (as discussed in Sections 4.1.5 and 4.2.4, respectively), transformer amplitude and phase imbalances are a significant contributing factor in the reduced measured bandwidth. Although phase imbalance data was not provided by the manufacturer of the transformers used to test the circuit, amplitude versus frequency data was provided and is known to vary with frequency. These variations have an undesirable effect on the output of the circuit and serve to reduce the measured bandwidth.

Harmonic Distortion Measures

The steady-state responses of the circuit to a range of different input amplitudes were recorded. FFTs were applied to determine the harmonic distortion measures of the circuit. Five tones (fundamental through to fifth harmonic) and the extrapolated lines to determine IIP5 are shown in Figure 5.24. Comparisons to simulated results under the same conditions are shown in Figure 5.25.

The first thing to note in Figure 5.24 is that the slope of the fundamental tone is not the ideal slope of three that would indicate a proper cubic function, but instead the slope is 1.86. This is a further indication that the fundamental tone is being dominated by linear feed-through, especially at small input amplitudes where the slope is closer to one (1.20).

The third-order tone has a slope closer to three as expected (3.26). Second- and fourth-order harmonics were present and are noted on the graph. They appear to be small and only affect the output at small input amplitudes. The measured IIP5 of 0.48V

Figure 5.24: Saturation Cuber: steady-state amplitude sweep measured results for a 1MHz input frequency are shown. IIP5 is shown.

is significantly less than the simulated value of 1.84V. The decrease can be attributed to the decreased slope of the fundamental tone.

The comparison of the measured tones to the simulated tones in Figure 5.25 reveals that the measured third- and fifth-order tones follow the same trends as what was expected from simulation. It is only the fundamental tone that differs significantly, but less so for larger amplitudes. At larger amplitudes, the effects of linear feed-through are reduced (a larger slope is observed), as the cubing term begins to dominate the linear term. Analogous to this effect is the linear crossover point observed in the measured results of Figure 5.18, which is the point where the cubing term becomes proportionally larger than the linear term. In Figure 5.18, this point occurred for an input of 124.3mV. Around the same point in Figure 5.24, the slope can be seen to increase before the output saturates for input voltages beyond its range of operation.

Figure 5.25: Saturation Cuber: steady state amplitude sweep measured results for a 1MHz input frequency are shown.

Time Domain Results Summary

A comparison of the simulated and measured time domain results is given in Table 5.7. Measurement results for the sub-threshold and triode cubing circuits (reported in Appendix B.3 and Appendix C.3, respectively) are also summarized in the table.

The measured cubic ratios (fundamental/third-order tone ratios) are all greater than anticipated. As previously mentioned, this can be attributed to incomplete cancellation of the linear term in the output polynomial expression caused by device mismatch and transformer performance issues (amplitude and phase imbalance).

As previously explained, the bandwidth of the saturation cuber as well as the triode cuber are less than expected. The bandwidth of the sub-threshold cuber, however, is actually larger than the 80MHz that was anticipated. As indicated in Section B.3.3, this result is artificially high because the fundamental tone magnitude begins to decrease

Performance Measure	Units	Saturation Cuber	Sub-threshold Cuber	Triode Cuber
Input Range (v_{id})	V	± 0.19	± 0.15	± 0.3
Cubic Ratio (Sim)	-	3.09	2.98	2.98
Cubic Ratio (Meas)	-	6.63	4.57	3.68
Cubic Bandwidth (Sim)	MHz	100	80	120
Cubic Bandwidth (Meas*)	MHz	7	100	10
IIP5 (Sim)	V	1.84	0.63	1.77
IIP5 (Meas)	V	0.48	0.56	0.63

* Taken as 10% deviation from low frequency values

Table 5.7: Time Domain Results Comparison for all three cubing circuits: saturation, sub-threshold, and triode. Both the simulated and measured bandwidths of the saturation cuber were determined for an input of $v_{id}=180\text{mV}$ (Subthreshold cuber: $v_{id}=130\text{mV}$, and triode cuber $v_{id}=230\text{mV}$).

significantly at lower frequencies (15MHz), but the third-order tone magnitude decreases as well, keeping the cubic ratio relatively constant over a wider range of frequencies.

The measured IIP5 results for all of the cubing circuits are lower than expected. In the case of the saturation and sub-threshold cubers, the decrease is due to slope of fundamental being lower than expected. With the triode cuber, the lower IIP5 is caused by decrease in gain observed in the chip used to observe the time domain results.

5.4 Additional Comparisons

5.4.1 Saturation Cuber biased in sub-threshold

As previously mentioned in Section 4.4, the saturation cuber can be biased primarily in the sub-threshold region of operation by reducing the bias voltage from 1.5 to 0.58V (albeit with less gain than the sub-threshold cuber presented in Appendix B). While taking the measurements, it was observed that a bias of 0.58V coincided with the “sweet-spot” discussed in Section B.2.2, where the cubing gain is approximately zero. In order to be able to discern a cubic response at the output, the bias was reduced further to 0.50V.

Measured results at this reduced input bias are shown in Table 5.8.

Performance Measure	Units	Biased in Saturation	Biased in Sub-threshold
Bias Voltage (V_{BIAS})	V	1.50	0.5
Input Range (v_{id})	V	± 0.19	± 0.19
Total Direct Current Draw	mA	7.17	3.24
Maximum PP ^{2*}	%	10.7	15.8
Maximum PP ^{3*}	%	54.0	50.4
Maximum PP ^{5*}	%	19.7	6.39
Linear Crossover Point*	mV	124.3	102.0
Gain: Cube Root Transform*	V^{-2}	3.37	-0.496
CoD R^2 *	-	0.96821	0.3044
Cubic Ratio	-	6.63	2.05
Cubic Bandwidth	MHz	7	75
IIP5	V	0.48	0.75

* These measurements were observed using 1MHz ramp input

Table 5.8: Simulation Results Comparison for the saturation cuber biased at 1.5V and at 0.58V (which biases it primarily in the sub-threshold region of operation). All results are from simulations without extracted parasitics.

One advantage of operating in the sub-threshold region of operation is the significant reduction in current (3.24mA instead of the 7.17mA).

As previously observed, the saturation cuber biased at 1.5V is affected by increased linearity (Cubic ratio = 6.63), but with a reduced bias of 0.5V the circuit is affected by reduced linearity (Cubic ratio = 2.05). This is evident in Figure 5.26, which compares the time domain response of the saturation cuber at the two different biases.

The reason for the reduction in the cubic ratio for the cuber biased in sub-threshold is that the cubing gain is now negative, but the linear feed-through present at the input still has the same polarity. In this case the linear feed-through serves to reduce the magnitude of the fundamental tone.

Interestingly, both this sub-threshold cuber and the one presented in Appendix B have large reported bandwidths. This is due to the fact that both of their fundamental

Figure 5.26: Time domain response of saturation cuber to 1MHz input, for two different bias voltages: 1.5V and 0.5V (which puts it in the sub-threshold region of operation).

and third-order tones decrease with frequency at the same rate, keeping the cubing ratio within 10% over a wider range of input frequencies.

5.4.2 Comparison to Published Cubing Circuits

Figure 5.27 compares the measured gain and input range of the cubing circuits presented in this thesis to the published designs detailed in Section 2.3. A graph plotting the gain versus power consumption would have been a better comparison (across different technologies), but a lack of published results prevented this. For example, the CMOS cuber in [1] uses a 3V supply and has at least 32 transistors drawing current, indicating that it would have higher power consumption than the cubing circuits presented here. Figure 5.27 does illustrate that cubing gain is achievable even when the technology has been scaled down. The measured cubing gain of the sub-threshold cuber ($31.3V^{-2}$) is in fact larger than the published cubing gain ($\approx 6V^{-2}$) of the $0.8\mu m$ CMOS cuber [1].

Figure 5.27: Literature review comparison of cubing gain versus maximum input voltage to measured results of saturation, sub-threshold and triode cubers. A comparison of gain to power consumption was not possible due to a lack of published results.

The bandwidth results of the cubing circuits presented in this thesis are less than expected but they compare well to the other CMOS circuits reported in Section 2.3. The frequency response of the $0.8\mu\text{m}$ CMOS cuber in [1] was only reported up to 1KHz. The frequency response of the $0.18\mu\text{m}$ CMOS cuber reported in [8] was not given, but it was shown to operate within a predistorter with a 90MHz bandwidth.

5.5 Chapter Summary

The layout techniques used to prepare the cubing circuit design presented in Chapter 3 for fabrication were presented. The test setup, including the printed circuit board used to interface the design, was described. Measured DC (using the 1MHz ramp approximation) and time domain results of the saturation cuber were compared against the simulation results of Chapter 4. The measured results were also compared against the measured results of the sub-threshold and triode cubers, reported in Appendices B.3 and C.3.

Chapter 6

Conclusion

This thesis has presented three CMOS analog cubing circuits, for possible use in analog signal processing applications such as Radio-over-Fiber Predistortion. A literature review of the state-of-the-art revealed a need for CMOS cubing circuits with high gain and bandwidth.

Three cubing circuits, each with MOSFETs biased in a different region of operation (saturation, sub-threshold and triode), were designed and fabricated in $0.18\mu\text{m}$ CMOS technology. The non-linear properties and high-frequency operation of deep submicron transistors were exploited to produce a time domain cubic response.

Two measures of DC cubicity (Polynomial Proportionality and Cube Root Transforms) were proposed in order to compare the simulated and measured results. The triode cuber has the highest measured cubic polynomial proportionality ($\text{PP}^3 = 73.1\%$). The sub-threshold cuber has the highest measured gain (31.3V^{-2}), as determined by the cube root transform method. Device mismatch was observed to introduce unwanted linear and even order terms in the output response that decrease the cubicity of the design.

Time domain steady-state cubicity was assessed with harmonic IIP5 measures and by the proposed Cubic Bandwidth method. The saturation cuber had the highest simulated

IIP5 (1.84V), but the lowest measured result (0.48V) due to linear feed-through and reduced cubicity, which is caused by device mismatch and transformer performance issues.

The linear feed-through along with the increased capacitance of the testing environment has a negative effect on the measured bandwidths of the circuit. The capacitance of the bond pads and probe load reduced the simulated bandwidth of the circuits from the 1 GHz range to the 100MHz range. The measured bandwidths were much less due to transformer amplitude and phase imbalances (saturation cuber: 7MHz, sub-threshold cuber: 100MHz, and triode cuber: 10MHz). The bandwidth of the sub-threshold cuber is higher than expected because the fundamental and third-order tones decrease in magnitude at the same rate. In an integrated system, like the RoF predistorter, these circuits should operate at higher frequencies.

6.1 Research Contributions

The contribution to research, shown in this thesis, is a CMOS circuit design that reduces the number of transistors and chip area required, and a design that also has the potential to work in the GHz range of frequency. The integration of the circuit into $0.18\mu\text{m}$ CMOS technology allowed for a simplified topology (since single transistors exhibited cubing behaviour) and an increase in operating frequency due to technology scaling. The design also allows for operation in the saturation, sub-threshold, or triode region of MOSFET operation.

6.2 Future Work

There are several areas of research that could be pursued to improve the designs proposed in this thesis. For example, an output buffer could be used to reduce the capacitive loading

at the output and allow the design to be better interfaced with the testing environment. The reduced capacitance would increase the measured bandwidths of the designs.

Another design modification that could be researched is the replacement of the load resistors with adjustable PMOS loads. Such a replacement could allow for gain adjustability and provide some protection against mismatch if each PMOS transistor had a separate control line. Disadvantages of this design would include increased area (due to extra I/O pads) and increased capacitance of the PMOS transistors over the polysilicon resistors.

Adjustable loads and biases along with some additional detection circuitry could be used to create a self-calibrating circuit. The self-calibration would adjust for process mismatch and variations. In an RoF predistortion circuit, adjustability and self-calibration would also prove quite useful in the presence of temperature variations and laser aging.

The design could be significantly improved if an alternate method of cancelling the linear term was found and the voltage doubling inputs ($2v_i$ and $-2v_i$) were not required. This could significantly improve the response of the output to amplitude and phase imbalance of the inputs. One possibility is to use the cross-coupled differential pair topology of [8] with careful selection of reference currents and transistor sizings. Another advantage of removing the need for voltage doubling is the reduction in the number of inputs. Not only does this reduce the area required for bonding pads, but it reduces the complexity of the input network. In this case, the circuit could be tested via wafer probing instead of on a PCB and higher frequency measurements could be obtained.

At the outset of this thesis, time domain noise analysis was not possible. Future work in the area of cubing circuit design should consider noise analysis (none of the published papers reported on noise). This is especially important in circuits dealing with low gain or small inputs (an example of a noisy output is in the triode cuber time domain results of Figure C.29).

Improvements could also be made to some of the cubicity measures used in this thesis. Both the polynomial proportionality and bandwidth measures are dependent on input amplitude. Better comparisons between circuits could be achieved if those measures could somehow be normalized or calculated differently to take the reliance on input amplitude into account. Additionally, IIP5 measurements could be taken at higher frequencies if two-tone instead of single-tone tests were used. Single-tone tests require that the harmonics appear in band, which is difficult to achieve at higher frequencies.

Alternative applications for the cubing circuit could also be explored. Some suggestions include predistorters for other transmission circuits, or third-order distortion correction circuits for mixers, amplifiers, etc. Another possible use for cubing circuits is in arbitrary waveform generation in analog signal processing systems. In combination with other power circuits (linear amplifiers, squarers, etc), the cubing circuit can be used to generate Taylor series approximations of any desired function (without memory).

Appendix A

Literature Review Derivations

A.1 Derivation of Anti-parallel Diode Circuit Output

From the derivation shown in [22, pp. 237-9], the anti-parallel diode circuit of Figure 2.5 can be replaced with the equivalent circuit shown in Figure A.1. Since the DC current bias charges the two capacitors to sufficiently large voltages, the capacitors can be modelled as voltage sources. Equation A.1.1 gives the current flow through the output resistor R_o :

$$I = I_S \exp((V_b + V_N)/NV_T) - I_S \exp((V_b - V_N)/NV_T) \quad (\text{A.1.1})$$

$$= I_S \exp(V_b/NV_T) [\exp(V_N/NV_T) - \exp(-V_N/NV_T)] \quad (\text{A.1.2})$$

$$= I_S \exp(V_b/NV_T) [2 \sinh(V_N/NV_T)] \quad (\text{A.1.3})$$

$$= 2I_B \sinh(V_N/NV_T) \quad (\text{A.1.4})$$

where I_S is the reverse saturation current, V_T is the thermal voltage, N is the number of diodes in each branch, V_N and V_b are defined in Figure A.1, and $I_B = I_S \exp(V_b/NV_T)$.

Solving for V_N gives Equation A.1.5, which can be expressed as a power series expansion of $\sinh^{-1}$ (Equation A.1.7). In [22, pp. 238], the series is only expanded to the

Figure A.1: Equivalent Anti-parallel Diode Predistortion Circuit [22, pp. 238].

third-order; whereas, here it is expanded to the fifth-order for higher order term comparison.

$$V_N = NV_T \sinh^{-1} \left(\frac{I}{2I_B} \right) \quad (\text{A.1.5})$$

$$= \frac{NV_T}{2I_B} I - \frac{NV_T}{48I_B^3} I^3 + \frac{3NV_T}{1280I_B^5} I^5 + \dots \quad (\text{A.1.6})$$

$$= r_1 I + r_3 I^3 + r_5 I^5 + \dots \quad (\text{A.1.7})$$

The input V_{RF} can be defined in terms of Equation A.1.7, and the current I through the source and output resistors (R_S and R_O , respectively):

$$V_{RF} = R_S I + (r_1 I + r_3 I^3 + r_5 I^5 + \dots) + R_O I \quad (\text{A.1.8})$$

$$= (R_S + R_O + r_1) I + r_3 I^3 + r_5 I^5 + \dots \quad (\text{A.1.9})$$

Using Series Reversion coefficients [60, p. 15] (expanded to include the fifth-order term),

Equation A.1.9 can be rewritten to solve for the current, I :

$$I \approx \frac{V_{RF}}{R_S + R_O + r_1} - \frac{r_3 V_{RF}^3}{(R_S + R_O + r_1)^4} + \frac{(3r_3^2 - (R_S + R_O + r_1)r_5) V_{RF}^5}{(R_S + R_O + r_1)^7} \quad (\text{A.1.10})$$

Therefore, the final relation between the input V_{RF} and the output V'_{RF} can be found

from $V'_{RF} = R_O I$ and Equation A.1.10:

$$V'_{RF} = \frac{R_O V_{RF}}{R_S + R_O + r_1} - \frac{r_3 R_O V_{RF}^3}{(R_S + R_O + r_1)^4} + \frac{(3r_3^2 - (R_S + R_O + r_1)r_5) R_O V_{RF}^5}{(R_S + R_O + r_1)^7} \quad (\text{A.1.11})$$

A.2 Derivation of Tripling Circuit Output

The following analysis of the output equations of the tripling circuit is a summary of the derivation presented in [1]. The variables used in the analysis are shown in Figures 2.13 and 2.14. The output voltage of the tripling circuit is given by:

$$V_{out} = V_{out+} - V_{out-} = R((I_1 + I_2 + I_3 + I_4) - (I_5 + I_6 + I_7 + I_8)) \quad (\text{A.2.1})$$

Where each of the eight currents (I_1 to I_8) represents the I_D current going into a tripling cell as described in Figure 2.13. The equation for I_D is derived in [1] and is given by the following equation (where K_4 is the transconductance parameter for M4):

$$I_D = K_4(A_1 V_i^4 + A_2 V_i^3 + A_3 V_i^2 + A_4 V_i + A_5) \quad (\text{A.2.2})$$

The coefficients (A_1 to A_5) were determined in [1] by developing an expression for the gate voltage of M4 (through current conservation between M1, M2 and M3) and substituting it into the drain current expression for M4. The coefficients (assuming M2 and M3 are sized identically and the gate of M3 is connected to VDD) are:

$$A_1 = \left(\frac{W_1}{L_1}\right)^2 \left(\frac{L_2}{W_2}\right)^2 \frac{1}{4(V_{DD} - V_{SS} - 2V_T)^2} \quad (\text{A.2.3})$$

$$A_2 = \left(\frac{W_1}{L_1}\right)^2 \left(\frac{L_2}{W_2}\right)^2 \frac{-(V_{SS} + V_T)}{(V_{DD} - V_{SS} - 2V_T)^2} \quad (\text{A.2.4})$$

$$A_3 = \left(\frac{W_1}{L_1}\right)^2 \left(\frac{L_2}{W_2}\right)^2 \left(\frac{3(V_{SS} + V_T)^2}{2(V_{DD} - V_{SS} - 2V_T)^2} \right) - \left(\frac{W_1}{L_1}\right) \left(\frac{L_2}{W_2}\right) \left(\frac{1}{2}\right) \quad (\text{A.2.5})$$

$$A_4 = \left(\frac{W_1}{L_1} \cdot \frac{L_2}{W_2} \cdot (V_{SS} + V_T)\right) - \left(\frac{W_1}{L_1}\right)^2 \left(\frac{L_2}{W_2}\right)^2 \frac{1}{(V_{DD} - V_{SS} - 2V_T)^2} \quad (\text{A.2.6})$$

$$A_5 = \left(\frac{V_{DD} - V_{SS} - 2V_T}{2}\right) - \left(\frac{W_1}{L_1}\right) \left(\frac{L_2}{W_2}\right) \frac{(V_{SS} + V_T)^2}{2(V_{DD} - V_{SS} - 2V_T)} \quad (\text{A.2.7})$$

Looking back to Equation A.2.1, it is noted that the differential nature of the output will cancel all even order power terms leaving only the first- and third-order terms for

each of the eight currents. Given the specific input voltage combinations to each of cells that were chosen in [1], it was shown that the first-order terms in both the left branch (I_1 to I_4) and the right branch (I_5 to I_8) would sum to zero, respectively:

$$(V_1+V_2+V_3) + (V_1-V_2-V_3) + (-V_1-V_2+V_3) + (-V_1+V_2-V_3) = 0 \quad (\text{A.2.8})$$

$$(-V_1-V_2-V_3) + (-V_1+V_2+V_3) + (V_1+V_2-V_3) + (V_1-V_2+V_3) = 0 \quad (\text{A.2.9})$$

Thus only the third-order terms in each of the branches remain:

$$(V_1+V_2+V_3)^3 + (V_1-V_2-V_3)^3 + (-V_1-V_2+V_3)^3 + (-V_1+V_2-V_3)^3 = 24V_1V_2V_3 \quad (\text{A.2.10})$$

$$(-V_1-V_2-V_3)^3 + (-V_1+V_2+V_3)^3 + (V_1+V_2-V_3)^3 + (V_1-V_2+V_3)^3 = -24V_1V_2V_3 \quad (\text{A.2.11})$$

The output equation of the tripling circuit is then reduced to:

$$V_{out} = RK_4A_2 (2(24V_1V_2V_3)) = \beta (V_1V_2V_3) \quad (\text{A.2.12})$$

Where β is the tripling factor and when β is expanded it is equivalent to:

$$\beta = -48R \left(\frac{1}{2}\mu_n C_{ox} \frac{W_4}{L_4} \right) \left(\frac{W_1/L_1}{W_2/L_2} \right)^2 \left(\frac{1}{V_C - V_{SS} - 2V_T} \right)^2 (V_{SS} + V_T) \quad (\text{A.2.13})$$

A.3 Derivation of Cross-Coupled Differential Pair (CCDP) Output

The following analysis of the output equations of the CCDP circuit expands on the theory presented in [8]. By using the derivation of the differential output current presented in [29, pp. 528-9], the cubing behaviour of the CCDP circuit can be shown. An analysis of the differential current present in a differential pair will be followed by an examination of the technique that is used to isolate the cubic function.

For the common-source biased differential pair shown in Figure A.2, expressions for the two drain currents (i_{D1} and i_{D2}) are given in Equations A.3.1 and A.3.2, assuming both devices are identically matched, neglecting output resistance, and neglecting the body effect.

Figure A.2: Differential Pair Analysis of Differential Output Current.

$$i_{D1} = \frac{1}{2}K (v_{GS1} - V_{th})^2 \quad (\text{A.3.1})$$

$$i_{D2} = \frac{1}{2}K (v_{GS2} - V_{th})^2 \quad (\text{A.3.2})$$

Equations A.3.1 and A.3.2 can be rewritten as:

$$\sqrt{i_{D1}} = \sqrt{\frac{K}{2}} (v_{GS1} - V_{th}) \quad (\text{A.3.3})$$

$$\sqrt{i_{D2}} = \sqrt{\frac{K}{2}} (v_{GS2} - V_{th}) \quad (\text{A.3.4})$$

Taking the difference of these two equations and substituting $v_{GS1} - v_{GS2} = v_{id}$, where v_{id} is the differential input voltage, gives:

$$\sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{\frac{K}{2}} (v_{id}) \quad (\text{A.3.5})$$

The constraint imposed by the current sink, I_{bias} , is given by:

$$i_{D1} + i_{D2} = I_{bias} \quad (\text{A.3.6})$$

Equations A.3.5 and A.3.6 are two equations with two unknowns, i_{D1} and i_{D2} , and can be solved together to yield:

$$i_{D1} = \frac{I_{bias}}{2} + \sqrt{KI_{bias}} \left(\frac{v_{id}}{2} \right) \sqrt{1 - \frac{Kv_{id}^2}{4I_{bias}}} \quad (A.3.7)$$

$$i_{D2} = \frac{I_{bias}}{2} - \sqrt{KI_{bias}} \left(\frac{v_{id}}{2} \right) \sqrt{1 - \frac{Kv_{id}^2}{4I_{bias}}} \quad (A.3.8)$$

To determine the differential output current, i_{diff} , of the differential pair, the drain current equations (A.3.7 and A.3.8) were subtracted:

$$i_{diff} = i_{D1} - i_{D2} \quad (A.3.9)$$

$$i_{diff} = \sqrt{KI_{bias}} (v_{id}) \sqrt{1 - \frac{Kv_{id}^2}{I_{bias}}} \quad (A.3.10)$$

In the analysis presented in [8], Equation A.3.10 was simplified to Equation A.3.12 using the Taylor series expansion in Equation A.3.11 (assuming that x is small and ignoring higher order terms):

$$\sqrt{1 - x^2} = 1 - \frac{x^2}{2} + \dots \quad (A.3.11)$$

$$i_{diff} = \sqrt{KI_{bias}} (v_{id}) - \frac{1}{8} \sqrt{\frac{K^3}{I_{bias}}} (v_{id}^3) \quad (A.3.12)$$

The output current, I_{out} , defined by the currents labelled in Figure 2.16, can be related to the differential currents of the two differential pairs (M1-M2 and M3-M4):

$$I_{out} = I_{o+} - I_{o-} \quad (A.3.13)$$

$$= I_{o1+} + I_{o2-} - (I_{o2+} + I_{o1-}) \quad (A.3.14)$$

$$= I_{o1+} - I_{o1-} - (I_{o2+} - I_{o2-}) \quad (A.3.15)$$

$$= I_{diff,M1-M2} - I_{diff,M3-M4} \quad (A.3.16)$$

Substituting the expression for differential currents (Equation A.3.12) into Equation A.3.13 yields:

$$I_{out} = \left(\sqrt{K_{M1,M2} I_{bias1}} - \sqrt{K_{M3,M4} I_{bias2}} \right) (v_{id}) - \frac{1}{8} \left(\sqrt{\frac{K_{M1,M2}^3}{I_{bias1}}} - \sqrt{\frac{K_{M3,M4}^3}{I_{bias2}}} \right) (v_{id}^3) \quad (\text{A.3.17})$$

where M1 and M2 of Figure 2.16 are biased with I_{bias1} and have $K_{M1,M2} = \mu_n C_{ox} \left(\frac{W}{L} \right)_{M1,M2}$, and M3 and M4 are biased with I_{bias2} and have $K_{M3,M4} = \mu_n C_{ox} \left(\frac{W}{L} \right)_{M3,M4}$.

To isolate the cubic term of Equation A.3.17, careful selection of the device sizes and biases is required. The following condition ensures that the linear component is cancelled:

$$\left(\frac{W}{L} \right)_{M1,M2} I_{bias1} = \left(\frac{W}{L} \right)_{M3,M4} I_{bias2} \quad (\text{A.3.18})$$

Thus, with some simplification, the cubic transfer function becomes:

$$I_{out} = -\frac{1}{8} \left(\sqrt{\frac{K_{M1,M2}^3}{I_{bias1}}} - \sqrt{\frac{K_{M3,M4}^3}{I_{bias2}}} \right) (v_{id}^3) \quad (\text{A.3.19})$$

$$= -\sqrt{\frac{(\mu_n C_{ox})^3}{64 (W/L)_{M1,M2} I_{bias1}}} \left(\left(\frac{W}{L} \right)_{M1,M2}^2 - \left(\frac{W}{L} \right)_{M3,M4}^2 \right) (v_{id}^3) \quad (\text{A.3.20})$$

Appendix B

Sub-Threshold Cubing Circuit

Cubing gain can also be achieved outside the region of saturation, as will be shown with the design, simulation and measurement results of this cuber.

B.1 Sub-Threshold Cuber Design

This cubing circuit is identical in topology to the cuber presented earlier in this thesis (Figure 3.4); however, the parameters of the cubing transistors (M1 to M6) have been changed to the ones shown in Table B.1. In the interests of reducing the layout design time, the same current mirror transistors (M7 and M8) are employed for this cuber, as for the saturation cuber. The reference current (I_{ref}) remains at 1.2mA. The load resistances (R) were made larger by decreasing the multiplicity of the parallel resistor cells used in the layout of the saturation cuber from 12 to 8 ($2397\Omega/8 \approx 300\Omega$). The bias voltage (V_{BIAS}) is 1.05V.

As will be shown in the simulation and measurement results that follow, this circuit achieves a higher cubing gain, which is due to the increased non-linearity in this region of operation and the increased widths of the cubing circuit transistors. An adverse effect of increasing the transistor size is the corresponding increase in device capacitance which

Component	Width (μm)	Length (μm)	Multiplicity
M1-M6	7.5	0.18	16
M7	7.75	1.00	20
M8	7.75	1.00	100
R	3.00	24.63	8

Table B.1: Component values for Sub-Threshold Cubing Circuit.

will limit the frequency response of the circuit.

B.2 Sub-Threshold Cuber Simulation Results

The same set of simulations (DC, Time Domain and PSS) that were applied to the saturation cuber will also be applied to this design.

B.2.1 DC: Region of Operation

As will be shown later, by biasing this cubing circuit so that some input voltages cause it to go into the sub-threshold region of operation, it can produce more cubic gain than the cuber biased entirely in saturation. Repeating the same procedure reported in Section 4.1.1, the DC operating point information of transistor M1 for various input voltages is reported in Table B.2.

v_i (mV)	$2v_i$ (mV)	V_{th} (V)	V_{GS} (V)	V_{DS} (V)	$V_{GS} - V_{th}$ (V)
-75	-150	0.6288	0.4446	0.5379	-0.1842
-10	-20	0.6192	0.6195	0.5043	0.0003
0	0	0.619	0.6405	0.5052	0.0215
75	150	0.630	0.7446	0.3740	0.1146

Table B.2: Sub-threshold Cubing Circuit Region of Operation for transistor M1.

For an input voltage ($2v_i$) of -20mV or less, M1 enters the sub-threshold region of operation. It can be shown that M4 would enter sub-threshold region for an input of 20mV since M1 and M4 form a differential pair. Therefore, for only a small range v_i of

between -10mV and 10mV, all transistors in this cuber are in saturation. Beyond this range, at least one transistor will be in the sub-threshold region of operation.

The maximum input range was determined by observing the cubing behaviour of the circuit, which was found to diminish beyond $v_i = \pm 75\text{mV}$ (or $2v_i = \pm 150\text{mV}$).

B.2.2 DC: Polynomial Fitting

As was done in Section 4.1.2, four of the cubing transistors (M1, M2, M4 and M5 of Figure 3.4) had their simulated I_d versus v_i curves fitted with fifth-order polynomials (within the expected input range), determined by polynomial fitting in MATLAB. Curves for M3 and M6 were not shown since they are identical in size, bias and inputs to M2 and M5, respectively.

The I_d versus v_i curves are shown in Figure B.1. The polynomial equations fitted to these curves are shown in Equations B.2.1 to B.2.6. Even though I_{M1} and I_{M4} are fed with $2v_i$ and $-2v_i$, respectfully, they are plotted versus v_i for simplicity.

$$I_{M1} = 0.00099 + 0.0307v_i + 0.1648v_i^2 - 2.7530v_i^3 - 11.808v_i^4 + 172.90v_i^5 \quad (\text{B.2.1})$$

$$I_{M2} = 0.00098 - 0.0154v_i - 0.0811v_i^2 + 1.7804v_i^3 + 5.8571v_i^4 - 98.148v_i^5 \quad (\text{B.2.2})$$

$$I_{M3} = 0.00098 - 0.0154v_i - 0.0811v_i^2 + 1.7804v_i^3 + 5.8571v_i^4 - 98.148v_i^5 \quad (\text{B.2.3})$$

$$I_{M4} = 0.00099 - 0.0307v_i + 0.1648v_i^2 + 2.7530v_i^3 - 11.808v_i^4 - 172.90v_i^5 \quad (\text{B.2.4})$$

$$I_{M5} = 0.00098 + 0.0154v_i - 0.0811v_i^2 - 1.7804v_i^3 + 5.8571v_i^4 + 98.148v_i^5 \quad (\text{B.2.5})$$

$$I_{M6} = 0.00098 + 0.0154v_i - 0.0811v_i^2 - 1.7804v_i^3 + 5.8571v_i^4 + 98.148v_i^5 \quad (\text{B.2.6})$$

Equations B.2.1 to B.2.6 reveal the coefficients (a_0 to a_5 of Equation 3.1.1) of each transistor for this specific operating point and range of inputs. (Note: the coefficients are heavily dependent on the bias and the selected range of inputs). Also note that $I_{M3} = I_{M2}$ and $I_{M6} = I_{M5}$, as expected.

Figure B.1: Sub-threshold: I_d versus v_i curves for M1, M2, M4 and M5.

Using the Taylor series method for predicting the gain (Section 3.2), the coefficients of the current expressions (Equations B.2.1 to B.2.6) are substituted into Equation 3.2.26 to find the output cubing gain ($\alpha = -60.6V^{-2}$).

$$v_{out} = -\frac{R}{4} (a_{3,M1} + 2a_{3,M2}) v_{id}^3 - \frac{R}{16} (a_{5,M1} + 2a_{5,M2}) v_{id}^5 \quad (B.2.7)$$

$$= -\frac{300}{4} (-2.7530 + 2(1.7804)) v_{id}^3 - \frac{300}{16} (172.90 + 2(-98.148)) v_{id}^5 \quad (B.2.8)$$

$$= -60.6v_{id}^3 + 439v_{id}^5 \quad (B.2.9)$$

This cubing gain is larger than the gain predicted for the saturation cuber, but the sub-threshold cuber's gain is negative. The transistor currents versus v_i shown in Figure B.1 show a more non-linear characteristic than the currents of the saturation cuber shown in Figure 4.1, which explains the increase in gain.

The change in sign is an interesting phenomenon that indicates there is a operating point of the transistor where the cubing term of the polynomial is reduced to zero. There

is a recently published paper [61] that recognizes a “sweet-spot” in MOSFET amplifier design where there is a significant peaking of the amplifier’s third-order intercept point and increased linearity. While this is certainly an important discovery for amplifier designers, this “sweet spot” is certainly of no help to cubing circuit designers who seek to exploit the cubic behaviour of MOSFETs.

The linear assumption made in the gain calculation method of Section 3.2 (Equation 3.2.27) indicates that the linear term should cancel, but evaluation of the linear term reveals that some linear gain exists:

$$\text{Linear term} = -R(a_{1,M1} + 2a_{1,M2})v_{id} \quad (\text{B.2.10})$$

$$= -300(0.0307 + 2(-0.0154))v_{id} \quad (\text{B.2.11})$$

$$= 0.03v_{id} \quad (\text{B.2.12})$$

The significance of the unwanted linear and fifth-order terms is indicated in Figure B.2, which plots the linear, cubic and quintic proportionality percentages.

The maximum cubic contribution (PP^3) indicated in the figure is 89.3%, which is almost 3% less than the saturation cuber. The unwanted linear and fifth-order terms lower the effective gain of the cuber, which will be shown graphically in the following section.

B.2.3 DC: Cubing Circuit Output

Figure B.3 shows the plots of the output voltages (v_{out+} and v_{out-}) versus the input voltage (v_i). The output voltage nodes share the same bias point (0.915V). Taking the difference of these two nodes will result in the final cubing response of the circuit (v_{out}), shown in Figure B.4.

Although Equation B.2.9 predicts the gain to be $-60.6V^{-2}$, the first- and fifth-order

Figure B.2: Odd order term Polynomial Proportionality percentages of the sub-threshold cuber are shown versus the differential input.

Figure B.3: Sub-threshold Cuber: Output Voltages (v_{out+} and v_{out-}).

terms in this equation serve to reduce the effective cubing gain of the circuit. Hence, Figure B.4 compares the differential output voltage (v_{out}) to an ideal cubing curve with a gain of $-50V^{-2}$, versus the differential input voltage (v_{id}). This figure also includes a plot of the absolute error between the simulated and ideal curves. Table B.3 indicates the maximum absolute error for different input voltage ranges.

Figure B.4: Sub-threshold Cuber: Differential Output Response (v_{out}) is plotted versus the Differential Input Voltage (v_{id}) and compared to an Ideal Cubing Response with a gain of $-50V^{-2}$. The Absolute Error Curve indicates the precision of the circuit; its axis is on the right side of the plot.

Input Range of v_{id}	Maximum Absolute Error
-0.150V to 0.150V	4.8mV
-0.125V to 0.125V	3.1mV
-0.100V to 0.100V	1.9mV

Table B.3: Sub-threshold Cuber: Absolute error voltage comparison for different input voltage ranges.

The differential output response, v_{out} of Figure B.4, was fitted (over the entire input range v_{id} : -0.3V to 0.3V) with an eleventh-order polynomial in MATLAB. The polynomial and coefficients are shown here in Equation B.2.13:

$$v_{out} = 0.0551v_{id} - 63.7v_{id}^3 + 477v_{id}^5 + 6880v_{id}^7 - 122000v_{id}^9 + 532000v_{id}^{11} \quad (\text{B.2.13})$$

In determining the coefficients, all even order terms (up to tenth-order) were discovered to be insignificant. The coefficient of the third-order term ($-63.7V^{-2}$) is close to the gain of $60.6V^{-2}$ that was predicted from the gain calculation, but larger than the gain of $50V^{-2}$ that was observed in Figure B.4. The maximum PP³ is 85.2%. The decrease from the predicted value (89.3%) is due to the inclusion of higher order terms that decrease the influence of the cubic gain at higher input voltages.

Linearizing the differential output response (within the input range: v_{id} : -0.15V to 0.15V) with a cube root transformation and applying linear regression analysis revealed the cubic gain to be $\alpha = -50.4V^{-2}$ and the coefficient of determination to be $R^2 = 0.99985$.

These cubicity performance measures are summarized and compared to those of other circuits in Table 4.4.

B.2.4 DC: Total Direct Current Draw

Figure B.5 illustrates the total direct current draw (including the reference current) of the circuit over the expected range of input voltages. The total current at $v_i = 0$ (7.105mA) is slightly less for this cuber than the total current reported for the saturation cuber (7.182mA). The current variation is limited to $50\mu\text{A}$ over the range of inputs shown.

B.2.5 DC: Parasitics

Even at DC, parasitic resistances can have a negative effect on the accuracy of the cubing circuit output. In this case, the cubing gain observed in the plot changes from $-50V^{-2}$ to

Figure B.5: Sub-threshold Cuber: Total Direct Current Draw versus input voltage (v_i).

$-37.5V^{-2}$. Figure B.6 displays the results of a DC simulation of the extracted layout with parasitic resistances. A polynomial fitted to the output response of the extracted circuit (Equation B.2.14) also reveals a decrease in the cubic gain ($-40.9V^{-2}$) from the cubic gain observed in the polynomial of Equation B.2.13 (-63.7).

$$v_{out} = 0.0552v_{id} - 40.9v_{id}^3 + 319v_{id}^5 + 20200v_{id}^7 - 234000v_{id}^9 + 907000v_{id}^{11} \quad (\text{B.2.14})$$

The maximum PP³ for the extracted response is 79.1%. This is a decrease of over 6% from the polynomial fitting done in Section B.2.3 (85.2%). This is due to the decrease in cubing gain magnitude that was observed in Figure B.6 and the increase in the magnitude of the seventh-order term of Equation B.2.14. No significant even order terms were observed in the polynomial fitting, just as there is no mismatch or asymmetry observed in the error curve of Figure B.6.

Linearizing the extracted differential output response (within the input range: v_{id} :

Figure B.6: Sub-threshold Cuber Extracted: Differential Output Response (v_{out}) is plotted versus the Differential Input Voltage (v_{id}) and compared to an Ideal Cubing Response with a gain of $-37.5V^{-2}$. The Absolute Error Curve indicates the precision of the circuit; its axis is on the right side of the plot.

$-0.15V$ to $0.15V$) with a cube root transformation and applying linear regression analysis revealed the cubic gain to be $\alpha = -35.5V^{-2}$ and the coefficient of determination to be $R^2 = 0.99367$.

B.2.6 Time Domain: Simulated Response (No Load)

The same time domain simulations that were presented for the saturation cuber will be repeated for the sub-threshold cuber.

In Figure B.7(a), multiple time domain differential output response curves (corresponding to a range of inputs with the same amplitude: $v_{id} = 0.13V$, but different frequencies) are overlaid on a normalized time axis, where T is the period of the waveform.

It is observed that for frequencies greater than 100MHz, there is a noticeable degradation in the sine cubed shape of the output waveform.

Figures B.7(b) and B.7(c) show the time domain responses of the v_{out+} and v_{out-} nodes, respectively, under the same testing conditions. Degradation of the output waveform shapes is noted for frequencies greater than 20MHz.

B.2.7 Time Domain: Simulated Response with Load

Figure B.8 shows the time domain simulated results, which include extracted parasitic capacitances from the layout (discussed in Section B.3.1) and the anticipated loading of the measurement setup (previously detailed in Section 5.2). Degradation of the shape of the output response was noted as the input frequency increases ($\geq 50\text{MHz}$). The lowered frequency response of this circuit when compared to the saturation cuber is due to the increased size of the cubing transistors as well as the inherent properties of sub-threshold transistors which make them more capacitive.

B.2.8 Time Domain: Expected Cubing Behaviour

In order to compare the shape of the simulated time domain response with the expected response, the cubic sinusoid of Equation B.2.16 was plotted along side the cubing circuit response to a 1MHz, 0.13V sinusoid input. The result is shown in Figure B.9. The absolute difference between the two curves is less than 2.5mV over two periods of the waveform.

$$\text{Expected} = \alpha (v_{id} \sin(\omega t))^3 \quad (\text{B.2.15})$$

$$= -50 (0.13 \sin(2\pi (1\text{MHz}) t))^3 \quad (\text{B.2.16})$$

(a) Time domain v_{out} voltage (no load). (b) Time domain v_{out+} voltage (no load). (c) Time domain v_{out-} voltage (no load).

Figure B.7: Sub-threshold Cuber Time Domain Results (no load): v_{out} , v_{out+} and v_{out-} voltage plots are overlaid on a normalized time axis (where T is the period of the waveform), for a range of input frequencies with the same input amplitude ($v_{id} = 0.13V$).

Figure B.8: Sub-threshold Cuber Time Domain Results (with anticipated measurement loading): Output response curves are overlaid on a normalized time axis (where T is the period of the waveform), for a range of input frequencies with the same input amplitude ($v_{id} = 0.13V$). Distortion of the waveform due to the load capacitance is noted at frequencies greater than 50MHz.

B.2.9 PSS: Cubic Bandwidth

Figure B.10 shows the fundamental and third-order tones of the simulated output responses (with and without loading) for an input signal with amplitude 0.13V over a range of frequencies. The cubic bandwidth is the frequency range over which the ratio of the fundamental and third-order tones remains at the ideal ratio of three. Figure B.11 plots this ratio versus the input frequency.

In the unloaded circuit response of Figure B.10, the fundamental and third-order tone amplitudes remain constant with frequency until they approach 100MHz. The cubic bandwidths of the unloaded and loaded circuit responses are quantified by determining from Figure B.11 when the ratio of the fundamental and third-order tone amplitudes

Figure B.9: Sub-threshold Cuber Time Domain Result (with anticipated measurement loading): Output response to an input v_{id} with 130mV amplitude and 1MHz frequency. A curve emulating the expected response (Equation B.2.16) of this circuit is also plotted.

deviates by 10% from the ideal ratio of three (the simulated ratio at low frequencies is 2.98). In the case of the unloaded circuit response, the cubic bandwidth is 250MHz. The cubic bandwidth of the loaded circuit response is 80MHz. As anticipated from the time domain plots of Section B.2.7, the addition of capacitive loading to the circuit decreases the frequency response. Within the 80MHz bandwidth, the phase difference deviated less than 20 degrees from the ideal difference of 180 degrees.

The trade-off that was noted between gain and bandwidth for the saturation cuber exists for this cuber as well: increases in gain are met with decreases in cubic bandwidth. Table B.4 reports cubic gain and bandwidth results over a range of bias voltages.

Figure B.10: Sub-threshold Cuber: the fundamental and third-order tones versus input frequency are shown for the simulated results (with and without loading).

Figure B.11: Sub-threshold Cuber: ratio of the fundamental and third-order tones versus input frequency are shown for the simulated results (with and without loading).

V_{BIAS} (V)	Gain (V^{-2})	Bandwidth (MHz)
0.95	54.1	75
1.05	50.8	80
1.15	46.4	85

Table B.4: Sub-threshold Cuber: Tabulated Results of Bias Voltage (V_{BIAS}) versus Cubic Gain and Bandwidth.

B.2.10 PSS: Output Harmonics

Figure B.12 plots the first-, third- and fifth-order harmonics (H1, H3 and H5, respectively) of the output response of the cubing circuit to a 1MHz input over a range of input amplitudes. As with the saturation cuber, this cubing circuit also displays linear tendencies for small amplitudes (fundamental tone has a slope of one for amplitudes less than 3mV).

Figure B.12 indicates the IIP5 for this circuit is 0.63V.

Figure B.12: Odd order output harmonics are plotted versus input amplitude for a 1MHz input. The cuber is loaded with the anticipated measurement load. The slopes of the first- and fifth-order harmonics are extrapolated to determine the fifth-order input referred intercept point (IIP5): $v_{id}=0.63V$.

B.2.11 PSS: Input Impedance

The simulation results of the input impedance of the sub-threshold cuber are nearly identical to those of the saturation cuber (which is expected since the two circuits share the same input traces on-chip). This is indicative of the degree to which the parasitic capacitances of the bond pads and input network dominate the gate capacitances of the MOSFETs used in the cubing circuits, as previously discussed in Section 3.5.

B.3 Implementation and Testing

Implementation details, and measurement results for the sub-threshold cuber will be reported in this section. Section B.3.1 discusses the layout implementation details of the design, while Section B.3.2 describes the sub-threshold operation of the printed circuit board (PCB) previously discussed in Section 5.2. The measurement results are reported in Section B.3.3.

B.3.1 Sub-threshold Cubing Circuit Layout

As previously mentioned, this design was integrated with the saturation cuber as they share ground pads and inputs. The layout of the sub-threshold cuber is shown in Figure B.13. The transistor, resistor and dummy placement is indicated in the figure. The common centroid matching technique, described in Section 5.1.1, was also applied to this design.

The same layout techniques that were applied to the saturation cuber were also applied to the sub-threshold cuber. The sub-threshold cuber has its own current reference, output and power supply pads. An array of ten 200fF bypass capacitors was also added between V_{DD} and ground (not shown in Figure B.13, but visible in Figure 5.2).

Figure B.13: Sub-Threshold cubing circuit layout in a four-metal-layer, single-polysilicon, $0.18\mu\text{m}$ n-well CMOS technology.

B.3.2 Printed Circuit Board Design

The PCB described in Section 5.2 was designed to support both the saturation and sub-threshold cubers. The only differences are the placement of two jumpers, the output connections, and the bias voltage setting. Connector J6 should have pins 1 and 2 shorted with a jumper to provide V_{DD} , and J5 should have also have pins 1 and 2 shorted to provide I_{ref}). The 2677A probe should be connected to the landing pads of capacitors C14 and C15 (as indicated in Figure 5.4 capacitors C14 and C15 and connectors J7 and J8 should not be populated on the PCB). The bias voltage applied to pin 3 of connector J2 should be 1.05V.

B.3.3 Measurement Setup and Results

The same DC and time domain test setup that was discussed in Section 5.3 was used to test this cubing circuit. The following sub-sections will report the DC and time domain behaviour of the circuit. Unfortunately, it was not possible to get both DC and time domain results from the same chip, as the DC measurements proved to be difficult to obtain due to the lack of ESD protection. Differences between the two chips that were measured may account for some of the gain differences observed between the DC and time domain results. (Approximate DC results obtained from a 1MHz ramp input were recorded and are included in Table 5.5 for comparison.)

DC Measurement Results

Figure B.14 shows the measured output voltages at the v_{out+} and v_{out-} nodes of the circuit and compares them to those expected from simulation with extracted resistive parasitics. In the simulation results, the bias point of the outputs was found at 0.915V. The measured results reveal the bias point to be significantly lower 0.736V and 0.750V for v_{out+} and v_{out-} , respectively. The mismatch in the bias points is expected to negatively affect the output of the circuit.

The differential output response is shown in Figure B.15. The polynomial expression fitted to the out put response is given in Equation B.3.1.

$$v_{out} = -0.0127 + 0.0408v_{id} + 1.56v_{id}^2 - 42.9v_{id}^3 - 27.9v_{id}^4 + 298v_{id}^5 \quad (\text{B.3.1})$$

The DC offset observed in Figure B.15 and Equation B.3.1 can be removed artificially (although in time domain tests, it can be achieved with coupling caps). This is shown in Figure B.16, where the polynomial is re-plotted without the DC offset term.

Figure B.14: Sub-threshold Cuber: Measured v_{out+} and v_{out-} voltages are compared to those from an extracted simulation.

Figure B.15: Sub-threshold Cuber: the measured v_{out} response is compared to an ideal response with $\alpha = -35.5V^{-2}$ and an resistive-extracted simulation response. A polynomial was fitted to the measure response and is given in Equation B.3.1.

Figure B.16: Sub-threshold Cuber: the polynomial fit of the measured v_{out} response without the DC offset is compared to an ideal response with $\alpha = -35.5V^{-2}$ and a resistive-extracted simulation response.

In Figure B.16, it is observed that the gain is smaller than expected for positive v_{id} , but larger than expected for negative v_{id} . This is caused by device mismatch, as evidenced by the difference in output bias voltages observed in Figure B.14.

The significance of the gain produced by the unwanted terms in Equation B.3.1 is indicated in Figure B.17, which plots the Polynomial Proportionality Percentages. The DC offset term has been removed from Equation B.3.1 under the assumption that this term could be removed by coupling capacitors for time domain inputs.

The maximum PP^3 indicated in the figure is 65.2%, which is a significant drop from the value of 89.3%, which was predicted from the gain calculation. The magnitude of the second-order term dominates the output in Figure B.17 for small voltages and the fifth-order term dominates the output for larger values of v_{id} . The existence of the second and fourth-order terms is due to the mismatch previously observed.

Figure B.17: Polynomial Proportionality Percentages of the sub-threshold cuber measured results are shown versus the differential input.

The cube root transformation and linear regression methods can be applied to the fitted polynomial to determine the gain and R^2 of the measured result. The result of the transformation and the line of least squares fit is shown in Figure B.18.

The presence of an intercept in the line of best fit to the cube root transformation of the measure output response indicates mismatch. Which was expected, given the difference in bias voltages of v_{out+} and v_{out-} that was observed at the output in Figure B.14.

The current draw of the circuit was also measured. Figure B.19 plots the measured and simulated current draw of the sub-threshold cuber. The measured current follows the same shape of the simulated current, but it is approximately 0.1mA lower than predicted.

Figure B.18: Sub-threshold Cuber: Cube Root Transformation of Measured v_{out} Response (without DC offset) is shown. The gain (α), intercept and R^2 measures are reported.

Figure B.19: Sub-threshold Cuber: Measured vs. Simulated Direct Current Draw.

Time Domain Measurement Results

The measured time domain results will be evaluated by looking at the output waveform shapes, the cubic bandwidth and the harmonic distortion measures.

Figure B.20 displays the time domain shape of the measured output response over frequency. As the input frequency increases the shape of the waveform becomes less cubic and more non-linear. Figure B.21 compares the measured response at 1MHz to the expected ($\text{gain} = -50V^{-2}$) and simulated responses. The positive values of the output track well with what was expected, but the output response below zero differs significantly. This confirms the mismatch that was seen in the DC response in Figure B.16, which observed different gains for positive and negative v_{id} . The degradation in the waveform shape around the zero crossing is the result of linear feed-through caused by transformer amplitude and phase imbalance.

Figure B.20: Sub-threshold Cuber Measured Results: Output response curves are overlaid on a normalized time axis (where T is the period of the waveform), for a range of input frequencies with the same input amplitude ($v_{id} = 0.13V$).

Figure B.21: Sub-threshold Cuber measured results are compared to the expected and simulated results of Figure B.9. Responses to an input v_{id} with 130mV amplitude and 1MHz frequency are shown.

The cubic bandwidth of this circuit was determined by the same method as for the saturation cuber as discussed in Section 5.3.2. Figure B.22 plots the fundamental and third-order tones of the FFT versus the input frequency, and Figure B.23 plots the ratio of the tones to determine the bandwidth. Comparisons to simulated results are included in both figures.

The magnitude of the third-order tone plotted in Figure B.22 is less than was expected from simulation, which caused the cubic ratio to be larger than the ideal ratio of three. The measured ratio was 4.57 instead of the 2.98 expected from simulations. Using the 10% criteria that was previously discussed, the measured cubic bandwidth is 100MHz, which is somewhat larger than the 80MHz that was expected. A look at the tones in Figure B.22 reveals the cause. Although the fundamental tone magnitude begins to decrease significantly at lower frequencies (15MHz), the third-order tone magnitude

Figure B.22: Sub-threshold Cuber: the fundamental and third-order tones versus input frequency are shown for the simulated (with and without loading) and measured results.

Figure B.23: Sub-threshold Cuber: ratio of the fundamental and third-order tones versus input frequency are shown for the simulated (with and without loading) and measured results.

decreases as well, keeping the cubic ratio relatively constant and artificially increasing the cubic bandwidth of the circuit.

Harmonic distortion measures were taken using the same method as for the saturation cuber. FFTs were applied to a series of steady-state responses that were taken at different input amplitudes. Five tones (fundamental through to fifth harmonic) and the extrapolated lines to determine IIP5 are shown in Figure B.24. Comparisons to simulated results under the same conditions are shown in Figure B.25.

Figure B.24: Sub-threshold Cuber: time domain amplitude sweep measured results for a 1MHz input frequency are shown. IIP5 is shown.

The first thing to note with this cubing circuit (and the saturation cubing circuit) is that the slope of the fundamental tone is not three as expected but 2.17. Given this reduced slope value and the presence of a large second-order tone (especially at smaller amplitudes), the fundamental tone is being greatly affected by linear feed-through and device mismatch in the circuit that was previously discussed. However, the slope of the

Figure B.25: Sub-threshold Cuber: time domain amplitude sweep measured results for a 1MHz input frequency are shown.

third-order tone is close to three as expected (3.31). The measured IIP5 of 0.56V is slightly less than the simulated value of 0.63V. The decrease can be attributed to the decreased slope of the fundamental tone.

The comparison of the measured tones to the simulated tones in Figure B.25 reveals that the measured third- and fifth-order tones follow somewhat closely to what was expected from simulation. It is only the fundamental tone that differs significantly, but less so for larger amplitudes. As with the saturation cuber, the effect of the linear feed-through is decreased for larger amplitudes as the cubing term becomes increasingly dominant.

The DC and time domain results of the sub-threshold cubing circuit are summarized in the tables of Section 5.3.1 and 5.3.2, and compared to the other cubing circuits discussed in this thesis.

Appendix C

Triode Cubing Circuit

Just as a cubing response can be obtained with MOSFETs biased in the saturation and sub-threshold regions of operation, it can also be achieved for transistors in the triode region as will be shown in this appendix. This was the first of the three cubing circuits to be designed and was made in a previous CMC fabrication run. It produces less gain than the other two designs, but it provided an initial proof of concept.

C.1 Triode Cuber Design

The topology of this circuit is given in Figure 3.3, which does not employ the current mirror that was used in the design of the sub-threshold and saturation cubers. The input bias voltage (V_{BIAS}) is 0.9V. The parameters of the cubing transistors (M1 to M6) and the load resistors (R) are given in Table C.1. The load resistors are each comprised of six larger resistors (3154Ω) combined in parallel to produce the desired resistance (526Ω). By dividing up the desired resistance into parallel components, a common centroid arrangement of the resistors in the layout is made possible. The layout of the circuit is discussed later in Section C.3.

Component	Width (μm)	Length (μm)	Multiplicity
M1-M6	2.25	0.18	4
R	0.55	6.1	6

Table C.1: Component values for Triode Cubing Circuit.

C.2 Triode Cuber Simulation Results

The same set of simulations (DC, Time Domain and PSS) that were applied to the saturation and sub-threshold cubers will also be applied to this design.

C.2.1 DC: Region of Operation

Repeating the same procedure reported in Section 4.1.1, the DC operating point information of transistor M1 for various input voltages is reported in Table C.2.

v_i (mV)	$2v_i$ (mV)	V_{th} (V)	V_{GS} (V)	V_{DS} (V)	$V_{GS} - V_{th}$ (V)
-150	-300	0.528	0.600	0.2462	0.072
-55	-110	0.528	0.790	0.2632	0.262
0	0	0.528	0.900	0.2637	0.372
150	300	0.5281	1.200	0.2693	0.6719

Table C.2: Triode Cubing Circuit Region of Operation for transistor M1.

For an input voltage ($2v_i$) of -110mV or less, transistor M1 is in saturation, however as the input voltage is increased, M1 enters the triode region of operation since $V_{DS} \leq V_{GS} - V_{th}$. Since M1 and M4 form a differential pair, transistor M4 is in triode for inputs -300mV to 110mV. Therefore, at all times, at least one transistor will be in the triode region of operation.

The maximum input range was determined by observing the cubing behaviour of the circuit, which was found to diminish beyond $v_i = \pm 150\text{mV}$ (or $2v_i = \pm 300\text{mV}$).

C.2.2 DC: Polynomial Fitting

As was done in Section 4.1.2, four of the cubing transistors (M_1 , M_2 , M_4 and M_5 of Figure 3.3) had their simulated I_d versus v_i curves fitted with fifth-order polynomials (within the expected input range), determined by polynomial fitting in MATLAB. Curves for M_3 and M_6 were not shown since they are identical in size, bias and inputs to M_2 and M_5 , respectively.

The I_d versus v_i curves are shown in Figure C.1. The polynomial equations fitted to these curves are shown in Equations C.2.1 to C.2.6. Even though I_{M_1} and I_{M_4} are fed with $2v_i$ and $-2v_i$, respectively, they are plotted versus v_i for simplicity.

Figure C.1: Triode: I_d versus v_i curves for M_1 , M_2 , M_4 and M_5 .

$$I_{M1} = 0.00097 + 0.006519v_i - 0.00017v_i^2 - 0.01959v_i^3 + 0.1014v_i^4 - 0.2625v_i^5 \quad (\text{C.2.1})$$

$$I_{M2} = 0.00097 - 0.003259v_i + 0.00004v_i^2 + 0.00640v_i^3 + 0.0372v_i^4 + 0.1361v_i^5 \quad (\text{C.2.2})$$

$$I_{M3} = 0.00097 - 0.003259v_i + 0.00004v_i^2 + 0.00640v_i^3 + 0.0372v_i^4 + 0.1361v_i^5 \quad (\text{C.2.3})$$

$$I_{M4} = 0.00097 - 0.006519v_i - 0.00017v_i^2 + 0.01959v_i^3 + 0.1014v_i^4 + 0.2625v_i^5 \quad (\text{C.2.4})$$

$$I_{M5} = 0.00097 + 0.003259v_i + 0.00004v_i^2 - 0.00640v_i^3 - 0.0372v_i^4 - 0.1361v_i^5 \quad (\text{C.2.5})$$

$$I_{M6} = 0.00097 + 0.003259v_i + 0.00004v_i^2 - 0.00640v_i^3 - 0.0372v_i^4 - 0.1361v_i^5 \quad (\text{C.2.6})$$

Equations C.2.1 to C.2.6 reveal the coefficients (a_0 to a_5 of Equation 3.1.1) of each transistor for this specific operating point and range of inputs. (Note: the coefficients are heavily dependent on the bias and the selected range of inputs). Also note that $I_{M3} = I_{M2}$ and $I_{M6} = I_{M5}$, as expected.

Using the Taylor series method for predicting the gain (Section 3.2), the coefficients of the current expressions (Equations C.2.1 to C.2.6) are substituted into Equation 3.2.26 to find the output cubing gain ($\alpha = 0.89V^{-2}$).

$$v_{out} = -\frac{R}{4} (a_{3,M1} + 2a_{3,M2}) v_{id}^3 - \frac{R}{16} (a_{5,M1} + 2a_{5,M2}) v_{id}^5 \quad (\text{C.2.7})$$

$$= -\frac{526}{4} (-0.01959 + 2(0.00640)) v_{id}^3 - \frac{526}{16} (-0.2625 + 2(0.1361)) v_{id}^5 \quad (\text{C.2.8})$$

$$= 0.89v_{id}^3 - 0.32v_{id}^5 \quad (\text{C.2.9})$$

This cubing gain is smaller than the gain predicted for the saturation and sub-threshold cubers, which is expected because the triode region in general has less gain than the saturation region and it is not as non-linear in behaviour as the sub-threshold region.

The linear assumption made in the gain calculation method of Section 3.2 (Equation 3.2.27) indicates that the linear term should cancel, but evaluation of the linear term

using the coefficients reveals that some linear gain exists:

$$\text{Linear term} = -R(a_{1,M1} + 2a_{1,M2})v_{id} \quad (\text{C.2.10})$$

$$= -526(0.006519 + 2(-0.003259))v_{id} \quad (\text{C.2.11})$$

$$= -0.000526v_{id} \quad (\text{C.2.12})$$

The significance of the unwanted linear and fifth-order terms is indicated in Figure C.2, which plots the linear (PP¹), cubic (PP³) and quintic (PP⁵) proportionality percentages.

Figure C.2: Odd order term Polynomial Proportionality percentages of the triode cuber are shown versus the differential input.

The maximum PP³ indicated in the figure is 97.2%, which is a 5% improvement over the saturation cuber and almost 8% over the sub-threshold cuber. The relatively low fifth-order gain is the cause for this improvement and also allows for a much larger input range ($v_{id} = \pm 300\text{mV}$), as the fifth-order residuals do not have as much of an effect on

the overall cubic output as v_{id} increases.

C.2.3 DC: Cubing Circuit Output

Figure C.3 shows the plots of the output voltages (v_{out+} and v_{out-}) versus the input voltage (v_i). The output voltage nodes share the same bias point (0.264V). Taking the difference of these two nodes will result in the final cubing response of the circuit (v_{out}), shown in Figure C.4.

Figure C.3: Triode Cuber: Output Voltages (v_{out+} and v_{out-}).

Although Equation C.2.9 predicts the gain to be 0.89, the first- and fifth-order terms in this equation serve to reduce the effective cubing gain of the circuit. Hence, Figure C.4 compares the differential output voltage (v_{out}) to an ideal cubing curve with a gain of $0.87V^{-2}$, versus the differential input voltage (v_{id}). This figure also includes a plot of the absolute error between the simulated and ideal curves. Table C.3 indicates the maximum

absolute error for different input voltage ranges.

Figure C.4: Triode Cuber: Differential Output Response (v_{out}) is plotted versus the Differential Input Voltage (v_{id}) and compared to an Ideal Cubing Response with a gain of $0.87V^{-2}$. The Absolute Error Curve indicates the precision of the circuit; its axis is on the right side of the plot.

The differential output response, v_{out} of Figure C.4, was fitted (over the entire input range v_{id} : -0.4V to 0.4V) with an eleventh-order polynomial in MATLAB. The polynomial and coefficients are shown here in Equation C.2.13:

$$v_{out} = 2.24 * 10^{-5}v_{id} + 0.862v_{id}^3 - 0.0683v_{id}^5 + 10.9v_{id}^7 - 157v_{id}^9 + 408v_{id}^{11} \quad (C.2.13)$$

In determining the coefficients, all even order terms (up to tenth-order) were discovered to be insignificant. The coefficient of the third-order term ($0.862V^{-2}$) is close to the gain of $0.89V^{-2}$ that was predicted from the gain calculation, and even closer to the gain of $0.87V^{-2}$ that was observed in Figure C.4. The maximum PP³ percentage is 99.5%. The

Input Range of v_{id}	Maximum Absolute Error
-0.300V to 0.300V	0.359mV
-0.200V to 0.200V	0.019mV
-0.100V to 0.100V	0.006mV

Table C.3: Triode Cuber: Absolute error voltage comparison for different input voltage ranges.

increase from the predicted value (97.2%) is a result of the decrease in the magnitude of the linear term that allows the cubic term to dominate the expression.

Linearizing the differential output response (within the input range: v_{id} : -0.3V to 0.3V) with a cube root transformation and applying linear regression analysis revealed the cubic gain to be $\alpha = 0.866V^{-2}$ and the coefficient of determination to be $R^2 = 0.99997$.

C.2.4 DC: Total Direct Current Draw

Figure C.5 illustrates the total direct current draw of the circuit over the expected range of input voltages. The total current at $v_i = 0$ is 5.845mA, which is much less than the total currents reported for the saturation and sub-threshold cubers, 7.182mA and 7.105mA, respectively. The current variation is limited to 60 μ A over the range of inputs shown.

C.2.5 DC: Parasitics

Even at DC, parasitic resistances can have an effect on the accuracy of the cubing circuit output. In this case, the cubing gain increases from $0.87V^{-2}$ to $1.0V^{-2}$. Figure C.6 displays the results of a DC simulation of the extracted layout with parasitic resistances.

The absolute error graph is not symmetric around $v_{id} = 0$, which indicates that there is some small mismatch present in the extracted layout of the design. A polynomial fitted to the extracted output response (Equation C.2.14) reveals that a second-order term is

Figure C.5: Triode Cuber: Total Direct Current Draw versus input voltage (v_i).

present, which again indicates a mismatch.

$$v_{out} = -2.86 * 10^{-4} v_{id} - 0.00113 v_{id}^2 + 1.03 v_{id}^3 - 0.166 v_{id}^5 + 6.34 v_{id}^7 - 150 v_{id}^9 + 436 v_{id}^{11} \quad (\text{C.2.14})$$

The maximum PP³ for the extracted response is 97.3%. This is a decrease of 2.2% from the polynomial fitting done in Section C.2.3 (99.5%). This is due to the increase in the linear term and the presence of a second-order term in Equation C.2.14. The polynomial proportionality of the higher order terms in Equation C.2.14 are less than 10% over the range of v_{id} from 0 to 0.4V.

Linearizing the extracted differential output response (within the input range: v_{id} : -0.3V to 0.3V) with a cube root transformation and applying linear regression analysis revealed the cubic gain to be $\alpha = 1.00V^{-2}$ and the coefficient of determination to be $R^2 = 0.99898$.

These cubicity performance measures are summarized and compared to those of other

Figure C.6: Triode Cuber Extraction: Differential Output Response (v_{out}) is plotted versus the Differential Input Voltage (v_{id}) and compared to an Ideal Cubing Response with a gain of $1V^{-2}$. The Absolute Error Curve indicates the precision of the circuit; its axis is on the right side of the plot.

circuits in Table 4.4.

C.2.6 Time Domain: Simulated Response (No Load)

The same time domain simulations that were presented for the saturation and sub-threshold cubers will be repeated for the triode cuber.

In Figure C.7(a), multiple time domain differential output response curves (corresponding to a range of inputs with the same amplitude: $v_{id} = 0.23V$, but different frequencies) are overlaid on a normalized time axis, where T is the period of the waveform. It is observed that for frequencies up to 1GHz, there is a no significant degradation in the sine cubed shape of the output waveform.

Figures C.7(b) and C.7(c) show the time domain responses of the v_{out+} and v_{out-} nodes, respectively, under the same testing conditions. Slight degradation of the output waveform shapes is noted for frequencies greater than 200MHz.

C.2.7 Time Domain: Simulated Response (With Load)

Figure C.8 shows the time domain simulated results, which include extracted parasitic capacitances from the layout (discussed in Section C.3.1) and the anticipated loading of the measurement setup (detailed in Section C.3.2). Degradation of the shape of the output response was noted as the input frequency increases ($\geq 100\text{MHz}$).

C.2.8 Time Domain: Expected Cubing Behaviour

In order to compare the shape of the simulated time domain response with the expected response, the cubic sinusoid of Equation C.2.16 was plotted along side the cubing circuit response to a 1MHz, 0.23V sinusoid input. The result is shown in Figure C.9. The absolute difference between the two curves is less than 0.85mV over two periods of the waveform. If the gain of the expected response is reduced to $0.8V^{-2}$, the difference is reduced to $40\mu V$.

$$\text{Expected} = \alpha (v_{id} \sin(\omega t))^3 \quad (\text{C.2.15})$$

$$= 0.87 (0.23 \sin(2\pi (1\text{MHz}) t))^3 \quad (\text{C.2.16})$$

C.2.9 PSS: Frequency Response

Figure C.10 shows the fundamental and third-order tones of the simulated output responses (with and without loading) for an input signal with amplitude 0.13V over a range

(a) Time domain v_{out} voltage (no load). (b) Time domain v_{out+} voltage (no load). (c) Time domain v_{out-} voltage (no load).

Figure C.7: Triode Cuber Time Domain Results (no load): v_{out} , v_{out+} and v_{out-} voltage plots are overlaid on a normalized time axis (where T is the period of the waveform), for a range of input frequencies with the same input amplitude ($v_{id} = 0.23V$).

Figure C.8: Triode Cuber Time Domain Results (with load): Output response curves are overlaid on a normalized time axis (where T is the period of the waveform), for a range of input frequencies with the same input amplitude ($v_{id} = 0.23V$). Significant distortion of the waveform due to the load capacitance is noted at frequencies greater than 100MHz.

of frequencies. The cubic bandwidth is the frequency range over which the ratio of the fundamental and third-order tones remains at the ideal ratio of three. Figure C.11 plots the ratio versus the input frequency.

In the unloaded circuit response of Figure C.10, the fundamental and third-order tone amplitudes remain constant with frequency until they approach 1GHz. The cubic bandwidths of the unloaded and loaded circuit responses are quantified by determining from Figure C.11 when the ratio of the fundamental and third-order tone amplitudes deviates by 10% from the ideal ratio of three. In the case of the unloaded circuit response, the cubic bandwidth is beyond 1GHz (any simulations beyond this frequency are suspect as they do not take into account the distributed gate resistance of the MOSFET [47]). The cubic bandwidth of the loaded circuit response is 120MHz. As anticipated from the time

Figure C.9: Triode Cuber Time Domain Result (with load): Output response to an input v_{id} with 230mV amplitude and 1MHz frequency. A curve emulating the expected response (Equation C.2.16) of this circuit is also plotted.

domain plots of Section C.2.7, the addition of capacitive loading to the circuit decreases the frequency response. Within the 120MHz bandwidth, the phase difference deviated less than 20 degrees from the ideal difference of 180 degrees.

The trade-off that was noted between gain and bandwidth for the saturation and sub-threshold cubers also exists for this cuber: increases in gain are met with decreases in cubic bandwidth. Table C.4 reports cubic gain and bandwidth results over a range of bias voltages.

V_{BIAS} (V)	Gain (V^{-2})	Bandwidth (MHz)
0.875	1.24	90
0.900	0.80	120
0.925	0.46	210

Table C.4: Triode Cuber: Tabulated Results of Bias Voltage (V_{BIAS}) versus Cubic Gain and Bandwidth.

Figure C.10: Triode Cuber: the fundamental and third-order tones versus input frequency are shown for the simulated results (with and without loading).

Figure C.11: Triode Cuber: ratio of the fundamental and third-order tones versus input frequency are shown for the simulated results (with and without loading).

C.2.10 PSS: Output Harmonics

Figure C.12 plots the first-, third- and fifth-order harmonics (H1, H3 and H5, respectively) of the output response of the cubing circuit to a 1MHz input over a range of input amplitudes. As with the saturation and sub-threshold cubers, this cubing circuit also displays linear tendencies for small amplitudes (fundamental tone has a slope of one for amplitudes less than 2mV). Figure C.12 indicates the IIP5 for this circuit is 1.77V.

Figure C.12: Odd order output harmonics are plotted versus input amplitude for a 1MHz input. The cuber is loaded with the anticipated measurement load. The slopes of the first- and fifth-order harmonics are extrapolated to determine the fifth-order input referred intercept point (IIP5): $v_{id}=1.77V$.

C.2.11 PSS: Input Impedance

Figure 4.22 plots the input impedance magnitude for two input nodes: $2v_i$ and v_i . The simulation includes the anticipated loading of the measurement test setup and the extracted parasitic capacitances of the layout. (Impedances for inputs $-2v_i$ and $-v_i$ are not

shown since they are identical to inputs $2v_i$ and v_i , respectively.)

Figure C.13: The magnitude of the input impedance of input nodes $2v_i$ and v_i are shown versus frequency. The anticipated measurement loading and parasitic capacitances are included in the simulation. The negative linear slope indicates that the impedance is mainly capacitive (values indicated on the figure).

The negative slopes of the impedances shown in Figure C.13 are an indication that the output is mainly capacitive (approximately 0.72pF and 0.75pF for inputs $2v_i$ and v_i , respectively). Up to 200MHz, the impedance of the inputs are greater than 1kΩ, which for the purposes of the input network is sufficiently large. However, as the frequency increases beyond this point, the lowered impedance will start to affect the voltage transfer to the circuit. The amplitude and phase of the input signals will start to degrade beyond this point and affect the cubic output.

The simulation results of the input impedance of the triode cuber are similar to those of the saturation and sub-threshold cubers in that the input impedance is predominately capacitive. However, the input impedance of this cuber is somewhat less, which accounts

for the higher bandwidth of this circuit.

C.3 Implementation and Testing

Implementation details, test setups and measurement results for the triode cuber will be reported in this chapter. Section C.3.1 discusses the layout implementation details of the design, while Section C.3.2 describes the printed circuit board (PCB) that was fabricated to test the triode cuber. The measurement setup and results are reported in Section C.3.3.

C.3.1 Triode Cubing Circuit Layout

The layout was submitted to CMC for the 0304CF fabrication run (design name: ICFCUMDK) along with designs from two other Masters Degree candidates. This cubing circuit does not share any pads with the other circuits on the chip and its position in the layout is indicated in Figure 5.1. Dimensions of the chip and of the circuit (including its pads) are indicated on the figure. The pad names and descriptions corresponding to the numbers in the figure are given in Table C.5.

Pad #	Pad Name	Notes
1	GND	Ground Pad
2, 3	v_{out-}, v_{out+}	Output pads for triode cuber.
4	V_{DD}	Supply voltage for triode cuber.
5, 6, 7, 8	$-2v_i, 2v_i, v_i, -v_i$	Inputs pads.

Table C.5: Bonding Pad Configuration for ICFCUMDK.

A close-up view of the layout of the triode cuber is shown in Figure C.15. The transistor, resistor and dummy placement is indicated in the figure. The common centroid matching technique, described in Section 5.1.1, was also applied to this design.

The same layout techniques that were applied to the saturation and sub-threshold cubers were also applied to the triode cuber, with the exception of the bypass caps and

Figure C.14: Picture of ICFCUMDK chip showing the circuit layout and bonding pad arrangement of the triode cuber.

input diodes.

C.3.2 Printed Circuit Board Design

The PCB designed to test the triode cuber was fabricated by CMR Summit Technologies on the same two-layer, 62mil, FR4 substrate panel as the PCB for the saturation and sub-threshold cubers.

Figure C.16 shows the PCB schematic, Table C.6 lists the Bill of Materials and Figure C.17 shows this PCB's layout. A picture of the populated board is shown in Figure C.18.

The power supply components of this PCB are identical to those of the saturation/sub-threshold PCB, except the current-sourcing and ESD protection circuits are not included. This chip was also bonded to the PCB in the same manner as the other chip (as discussed in Section 5.2.3). A picture of the bond wires is included in Figure C.19.

The input and output network components of this PCB are identical to those of the

Figure C.15: Triode cubing circuit layout in a four-metal-layer, single-polysilicon, 0.18μm n-well CMOS technology.

Figure C.16: Triode Cuber: PCB Schematic.

Component	Ref. Des.	Value	Part Number	Manufacturer
Capacitors	C1, C2, C5, C6	10 μ F	T491B106K010AS	Kemet
	C3, C7	0.01 μ F	GRM188R71H103KA01	Murata
	C4, C8, C9	0.1 μ F	GRM188R71C104KA01	Murata
	C10-C11	100pF	GRM1885C2A101JA01	Murata
Connectors	J1, J2	1x3	22-03-2031	Molex/Waldom
	J3, J4, J5	SMA	142-0701-201	Johnson
Resistors	R1, R2	100 Ω	ERJ-3EKF1000V	Panasonic
	R3	40.2 Ω	ERJ-3EKF40R2V	Panasonic
	R4	200 Ω	ERJ-3EKF2000V	Panasonic
	R5-R8	10K Ω	ERJ-3EKF1002V	Panasonic
	R9, R10	49.9 Ω	ERJ-3EKF49R9V	Panasonic
	R11-R18	0.1 Ω	ERJ-3RSFR10V	Panasonic
CMOS chip	U1	-	ICFCUMDK	TSMC
Ferrite Bead	U2, U3	1K Ω	BLM21AG102SN1D	Murata
Transformer	U4, U5	1:1	T1-1T-KK81	Mini-Circuits

Table C.6: Triode Cubing Circuit PCB Bill of Materials.

(a) Top side.

(b) Bottom side (as seen through the top).

Figure C.17: The top and bottom sides of a two-layer, 62mil, PCB Layout for the triode cuber are shown.

Figure C.18: Triode Cuber: Populated PCB board.

Figure C.19: Picture of triode cuber chip showing bond wires, taken at École Polytechnique in Montréal.

PCB discussed in Section 5.2.2 and 5.2.4. The microstrip lengths for the input were different, so additional ADS simulations were run to verify the input impedance of the input network. The test setup is shown in Figure C.20 and the results are shown in Figure C.21. Similar results were achieved: S_{33} and S_{22} less than -20dB up to 200MHz, and S_{11} less than -20dB up to 1GHz.

Figure C.20: This is the simulation setup in ADS used to verify the chosen PCB microstrip widths.

The bonding and output load models discussed in Sections 5.2.3 and 5.2.4 for the saturation and sub-threshold cubers also apply to this circuit. In this case, the 2677A

Figure C.21: ADS S-Parameter simulation results are shown for the triode cuber PCB input network microstrips.

solder-in probe would be connected to the landing pads of capacitors C10 and C11 (as indicated in Figure C.16 capacitors C9 and C10 and connectors J4 and J5 should not be populated on the PCB). The bias voltage applied to this circuit should be 0.9V.

C.3.3 Measurement Setup and Results

The same DC and time domain test setup that was discussed in Section 5.3 was used to test this cubing circuit. The following sub-sections will report the DC and time domain behaviour of the circuit. Unfortunately, it was not possible to get both DC and time domain results from the same chip, as the DC measurements proved to be difficult to obtain due to the lack of ESD protection. Differences between the two chips that were measured may account for some of the gain differences observed between the DC and time domain results.

DC Measurement Results

Figure C.22 shows the measured output voltages at the v_{out+} and v_{out-} nodes of the circuit and compares them to those expected from simulation with extracted resistive parasitics. In the simulation results, the bias point of the outputs was found at 0.285V. The measured results reveal the bias point to be somewhat lower 0.222V and 0.228V for v_{out+} and v_{out-} , respectively. The mismatch in the bias points is expected to negatively affect the output of the circuit.

Figure C.22: Triode Cuber: Measured v_{out+} and v_{out-} voltages are compared to those from an extracted simulation.

The differential output response is shown in Figure C.23.

$$v_{out} = -6.64 * 10^{-3} + 5.84 * 10^{-3}v_{id} + 0.0234v_{id}^2 + 1.03v_{id}^3 - 0.0822v_{id}^4 - 2.81v_{id}^5 \quad (C.3.1)$$

The DC offset could be removed artificially (in the time domain this can be achieved with coupling caps). This is shown in Figure C.24, where the polynomial is re-plotted

Figure C.23: Triode Cuber: the measured v_{out} response is compared to an ideal response with $\alpha = 1V^{-2}$ and an resistive-extracted simulation response. A polynomial was fitted to the measure response. The polynomial expression is given in Equation C.3.1.

without the DC offset term.

The significance of the gain produced by the unwanted terms in Equation C.3.1 is indicated in Figure C.25, which plots the Polynomial Proportionality Percentages. The DC offset term has been removed from Equation C.3.1 under the assumption that this term could be removed by coupling capacitors for time domain inputs.

The maximum PP^3 indicated in the figure is 73.1%, which is a significant drop from the value of 97.2%, which was predicted from the gain calculation. The magnitude of the fifth-order term dominates the output in Figure C.25 for larger values of v_{id} . This is significantly different than the low fifth-order term proportionality percentages that were observed in Figure C.2. The existence of the second- and fourth-order terms is due to the mismatch previously observed. The linear term is also shown to be more dominant in the measured results, another consequence of device mismatch.

Figure C.24: Triode Cuber: the polynomial fit of the measured v_{out} response without the DC offset is compared to an ideal response with $\alpha = 1V^{-2}$ and a resistive-extracted simulation response.

Figure C.25: Polynomial Proportionality Percentages of the triode cuber measured results are shown versus the differential input.

The cube root transformation and linear regression methods can be applied to the fitted polynomial to determine the gain and R^2 of the measured result. The result of the transformation and the line of least squares fit is shown in Figure C.26.

Figure C.26: Triode Cuber: Cube Root Transformation of Measured v_{out} Response (with the DC offset removed) is shown. The gain (α), intercept and R^2 measures are reported.

The presence of an intercept in the line of best fit to the cube root transformation of the measure output response indicates mismatch. Which was expected, given the difference in bias voltages of v_{out+} and v_{out-} that was observed at the output in Figure C.22.

Figure C.27 plots the measured and simulated current draw of the triode cuber. The measured current is significantly lower (4.40mA as compared to 5.85mA). The current of through this circuit is solely determined by the sizing of the cubing transistors, unlike the saturation and sub-threshold cubers which are driven by current mirrors. Therefore process variations could have affected the design causing the total current draw and the output bias voltages to be less than expected.

Figure C.27: Triode Cuber: Measured vs. Simulated Direct Current Draw.

Time Domain Measurement Results

The measured time domain results will be evaluated by looking at the output waveform shapes, the cubic bandwidth and the harmonic distortion measures.

Figure C.28 displays the time domain shape of the measured output response over frequency. As the input frequency increases the shape of the waveform becomes less cubic and more linear. Significant noise is present at the output, even with the oscilloscope averaging feature applied to the measured response. This cuber has the least amount of gain as compared to the other two circuits, and the low amplitude at the output makes it difficult to differentiate the output signal from the noise injected by the active probe (the 1134A and 2677A).

Figure C.29 compares the measured response at 1MHz to the expected ($\text{gain}=0.87V^{-2}$) and simulated responses. Significant loss in gain is observed in the time domain response. Since different chips were used to test the DC and time domain results, this is assumed

Figure C.28: Triode Cuber Measured Results: Output response curves are overlaid on a normalized time axis (where T is the period of the waveform), for a range of input frequencies with the same input amplitude ($v_{id} = 0.23V$).

to be the reason why the DC results show no loss in gain, but the time domain results do. Small changes in device size and bias can cause significant changes in the gain and bandwidth of this cubing circuit. The results of a transformer phase imbalance are observed by the change in the zero crossings of the output response. The change in the zero crossings with frequency is similar to the input phase delay simulation shown in Figure 4.17.

The cubic bandwidth of this circuit was determined by the same method as for the saturation and sub-threshold cubers as discussed in Section 5.3.2. Figure C.30 plots the fundamental and third-order tones of the FFT versus the input frequency, and Figure C.31 plots the ratio of the tones to determine the bandwidth. Comparisons to simulated results are included in both figures.

The magnitudes of both the fundamental and third-order tones is less than expected, which is consistent with the loss of gain observed in Figure C.29. The magnitude of

Figure C.29: Triode Cuber Measured Time Domain Result is compared to the expected and simulated results of Figure C.9. Responses to an input v_{id} with 230mV amplitude and 1MHz frequency are shown.

the fundamental tone increases with frequency, which is consistent with what would be observed with a input phase delay problem. The measured ratio of the fundamental and third-order tones is 3.68, as compared to the simulated ratio of 2.98. This is the lowest measured ratio of all the cubing circuits. Using the 10% bandwidth criteria discussed in Section 5.3.2, the cubic bandwidth of this circuit is 10MHz, which is significantly less than the 120MHz predicted from simulations.

Harmonic distortion measures were taken using the same method as for the saturation and sub-threshold cubers. FFTs were applied to a series of steady-state responses was taken at different input amplitudes. Five tones (fundamental through to fifth harmonic) and the extrapolated lines to determine IIP5 are shown in Figure C.32. Comparisons to simulated results under the same conditions are shown in Figure C.33.

A good indication that this cubing circuit is cubing correctly is that the slopes of the

Figure C.30: Triode Cuber: the fundamental and third-order tones versus input frequency are shown for the simulated (with and without loading) and measured results.

Figure C.31: Triode Cuber: ratio of the fundamental and third-order tones versus input frequency are shown for the simulated (with and without loading) and measured results.

Figure C.32: Triode Cuber: time domain steady-state amplitude sweep measured results for a 1MHz input frequency are shown. IIP5 is shown.

fundamental and third-order tones are both close to the ideal slope of three (3.08 and 3.14, respectively). Unfortunately, only a small range of input amplitudes was plotted, as this cubing circuit does not have a lot of gain and below an input of $0.2V$ v_{id} the response was hidden in the noise. The measured IIP5 of $0.63V$ is significantly less than the simulated value of $1.77V$. The decrease can be attributed to the decrease in gain that was observed in the chip used to test the time domain results.

Another interesting thing to note is that the second- and fourth-order tones are relatively small when compared to the even order tones of the other two circuits. This is an indication that this circuit suffers less from the effects of device mismatch.

The comparison of the measured tones to the simulated tones in Figure C.33 reveals that the measured tones follow the same trends as what was expected from simulation other than the loss of gain.

Figure C.33: Triode Cuber: time domain steady-state amplitude sweep measured results for a 1MHz input frequency are shown.

The DC and time domain results of the triode cubing circuit are summarized in the tables of Section 5.3.1 and 5.3.2, and compared to the other cubing circuits discussed in this thesis.

Previous Work

Published Paper

- F. Shearer and L. MacEachern, “A Precision CMOS Analog Cubing Circuit,” in *Proc. IEEE NorthEast Workshop on Circuits and Systems (NEWCAS)*, Montreal, Canada, June 2004, pp. 281–284.

Presentations

- F. Shearer, “A Precision CMOS Analog Cubing Circuit,” in the TEXPO Research Competition at *The CMC Microsystems Annual Symposium*, Ottawa, Canada, October 2005.
- F. Shearer, “Radio-over-Fiber Receiver Predistortion: Adding and Cubing Circuits,” awarded first place at the *IEEE Eastern Ontario Student Paper Competition*, Ottawa, Canada, March 2003.

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