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Hot-Carrier Induced Degradation
in
Surface pMOSFETs

by

Marinette A. Besson, Ingénieur I.S.T.

A thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfillment of the requirements
for the degree of

Master of Engineering

Ottawa-Carleton Institute for Electrical Engineering

Department of Electronics

Carleton University

Ottawa, Ontario

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Professor N.G. Tarr, Thesis co-supervisor

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ABSTRACT

This Thesis reports the design, fabrication and electrical characterization of surface p-channel transistors with good control of short channel effects down to 0.3 μm effective channel length. Design features included a phosphorus Ldd “halo”, gate oxide thicknesses ranging from 9 to 18 nm and three different types of threshold voltage adjust implants. The process used to fabricate the devices is discussed with emphasis on the difficulty of obtaining a high enough level of boron doping in the polysilicon gate to avoid gate depletion effects, while at the same time not diffusing boron through the gate oxide into the underlying channel. Electrical tests confirming that both criteria were met are presented. The mechanisms of hot-carrier-induced degradation were studied for these devices. The relative impact of trapped hot-electrons and hot-carrier generated interface states were studied by means of detrapping of electrons and measurement of the Gate Induced Drain Leakage (GIDL) current. Stress-induced trapped electrons at the drain end of the gate oxide create an apparent reduction of the effective channel length combined with an increase of the channel resistance. The dependence of the degree of degradation on the stress bias voltages was examined. The maximum shift was not obtained for the same bias conditions for all electrical parameters. The relative impact of gate oxide thickness, and threshold adjust implant profiles on the hot-carrier immunity of the pMOSFETs was studied. Devices with thin gate oxide and devices with the deepest threshold adjust implant profile were found to degrade the least.

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CHAPTER 1

INTRODUCTION

1- 1- Surface pMOSFETs: A Brief Background

The choice between buried-channel N-doped polysilicon gate and surface-channel P-doped polysilicon gate pMOSFETs is an important design consideration for CMOS technologies with channel lengths of 0.5 μm and below. Buried-channel transistors present the advantage of processing simplicity and higher hole mobility compared to surface channel pMOSFETs [1][2] but it becomes increasingly difficult to obtain good turn-off characteristics with such devices as the channel lengths are reduced [2][6][10]. Surface-channel p-doped polysilicon gate pMOSFETs are the most common alternative to buried channel devices. It has been shown that their surface conduction path allows for better gate control over the channel charges, resulting in improved turn-off characteristics [6].

The need to dope the gate polysilicon with boron in a surface pMOSFET leads to difficulties in device fabrication. In particular, it is necessary to implant the gate electrode heavily with boron, and anneal the implant with sufficient thermal budget to diffuse the boron to the gate/oxide interface. However, it is simultaneously necessary to avoid boron penetration through the gate oxide into the underlying channel, leaving only a relatively narrow process “window”. The impact of anneal temperature, the ambient, as well of the gate polysilicon thickness and the form in which the boron is implanted to dope the gate electrode are among the processing parameters that have been studied in the past few years to successfully fabricate p-doped polysilicon gate surface p-channel devices [11][13][19].

Hot-electron device degradation was recognized as the main limitation for MOS scaling more than a decade ago [21]. The subject has received much attention for nMOSFETs[22][23][24][25] but only recently was seen as a possible lifetime limiting factor for pMOSFETs. It has been referred to as “hot-electron-induced-punchthrough” for buried pMOSFETs [28]. After prolonged usage these devices were found to fail due to the degradation of their turn-off characteristics induced by energetic electrons being injected into and trapped in the gate dielectric [27]. The degradation of surface pMOSFETs is usually

slower than that of their buried channel counterparts, and so has received less attention to date in the literature. There is evidence that degradation of surface channel devices may still occur through hot-carrier induced punchthrough. However, the surface conduction path [29][31] and/or the use of boron to dope the gate electrode [36][37] in surface pMOS-FETs is believed to induce additional degradation mechanisms (more detailed references will be given on each of these topics during the course of this work).

1- 2- Thesis Organization

This thesis reports the design, fabrication and electrical characterization of surface p-channel transistor with channel lengths as short as 0.3 μm . Emphasis is placed on resistance to hot-carrier induced degradation, which in turn is heavily dependant on the control of short-channel effects. Chapter 2 discusses design of the test devices, which was carried out with extensive reliance on PREDICT [7], SUPREM [8], and MEDICI [9] numerical simulation. Design features included a phosphorus LDD “halo” which MEDICI simulations indicated would be very beneficial in controlling short-channel effects. Gate oxide thicknesses ranging from 9 to 18 nm and three different types of threshold voltage adjust implants giving different channel doping profile were examined. The fabrication of the transistors is also presented with special emphasis placed on the difficulties associated with gate polysilicon doping with boron. Chapter 3 presents two aspects of device electrical performance: experiments to characterize the quality of the gate electrode doping and evaluation of the performance and short channel control of the devices dependant on the gate oxide thickness and the specifics of the threshold voltage implant. Chapter 4 is devoted to the mechanisms and consequences of hot-carrier-induced degradation of the pMOSFETs produced for this thesis. Results are compared to previous work on the topic. The dependence of device degradation on bias conditions is considered. The relative involvement of trapped hot electrons and interface states creation in degradation is examined. The impact of both these effects on the linear transconductance degradation is studied in detail to illustrate the complexity of the degradation mechanisms in surface pMOSFETs. Finally, conclusions are drawn on the correlation between device structures (particularly the gate oxide thickness and threshold voltage adjust implant profile) and the resistance to hot-carrier-induced degradation. Using knowledge of the undegraded short

channel behavior and hot-carrier-induced degradation mechanisms, possible explanations are given for the dependence of the degradation on structure.

CHAPTER 2

DEVICE DESIGN AND FABRICATION CONSIDERATIONS

Traditionally, in a CMOS process, both n- and p-channel devices are fabricated with an n-doped gate polysilicon electrode. To adjust the threshold voltages, a p- layer is implanted underneath the gate oxide. The counter-doping of the n-well in which the pMOSFET is located creates a buried conduction path. This structure is more sensitive to short channel effects than a surface conduction path due to the longer distance between the gate electrode and the channel charges. To avoid having to counter-dope the channel, the gate work function can be raised either by changing the gate material to a refractory metal [4][5] or by changing the gate dopant type from phosphorus to boron. The latter option can more easily be integrated to an existing process and is the most widely chosen in industry for devices with channel lengths of 0.5 μm and below. It is also the choice made for the devices described in this work. The design choices and expected device performance will be discussed first. The fabrication of the transistors will then be presented with special emphasis on the gate polysilicon doping with boron that makes the device a “surface pMOSFET”.

2- 1- Design Considerations

Three design features were studied: variable gate oxide thickness, three different types of threshold voltage adjust implant profile and a phosphorus halo below the p-LDD region [3].

2- 1- 1- Gate Oxide Thickness

The design included three different gate oxide thicknesses: 18, 13 and 9 nm.

2- 1- 2- Threshold Voltage Adjust Implants

pMOSFETs with three different types of threshold voltage implants were fabricated (Figure 1). One set of transistors had arsenic implanted at 10 keV before the gate oxide was grown to adjust threshold voltages. Due to the thermal budget necessary for gate oxide growth, these devices had the deepest arsenic diffusion and the lowest surface

doping. They will be referred to as the “deep- V_{th} ” devices. Both other device types had arsenic implanted after the gate oxide was grown. Another set of transistors were fabricated with an implant energy of at 21 keV to obtain a very shallow threshold voltage implant and the highest surface doping (referred to as “shallow- V_{th} ”) while the final set of transistors was implanted at 45 keV to obtain an intermediate implant depth and surface doping (referred to as “medium- V_{th} ”).

FIGURE 1. Simulated channel doping profiles of three different types of threshold voltage implants.

2- 1- 3- Phosphorus Halo

The diffusion depth of the source and drain junctions influences the ability of a device to maintain control over short channel effects. However, there is a minimum junction depth necessary to avoid spiking during the silicidation step of a process. An alternative is to maintain a deep source/drain junction and reduce the LDD (Lightly Doped Drain) junction depth to minimize the short channel effects while avoiding problems with the silicidation. The LDD junction depth was kept very shallow in this study through use of a phosphorus halo implant that did not modify the source/drain junction depth (Figure 2). Figure 3 shows the expected source/drain and LDD profiles as predicted by the simulator SUPREM. Table 1 gives the SUPREM and PREDICT junction depths with and without the halo implant. MEDICI simulations showed that the reduction in the LDD junction depth translated into a substantial improvement of the subthreshold characteristics (Figure 4). All devices described here were fabricated with a phosphorus halo that allowed device with controlled short channel effects down to 0.3 μm effective channel length.

FIGURE 2. Schematic cross section of the pMOSFET with phosphorus halo.

FIGURE 3. Simulated Ldd junction depth reduction due to phosphorus halo.

FIGURE 4. Comparison of the simulated subthreshold behavior of pMOSFET's with and without halo implant.

	Junction Depths Without The Halo (nm)	Junction Depths With The Halo (nm)	Junction Depths Reduction (%)
SUPREM			
Source/ Drain	197	197	0
LDD	116	59	65
PREDICT			
Source/ Drain	296	296	0
LDD	127	71	57

Table 1: Simulated source/drain and LDD junction depths.

2- 2- Fabrication

The devices were fabricated using p-type <100> substrate of 15 Ωcm resistivity. The process architecture includes twin-well formation, LOCOS isolation, Ti-Salicide barrier metallization, thermally flowed BPSG, tungsten plugs and one level of metal (aluminum). The main steps of the front end process are presented in table 2. The first of the polysilicon gate doping was implanted after the poly gate deposition, while the second came from the source/drain implant for a total dose of $8.10^{15} \text{ cm}^{-2}$. The LDD junction depth was kept shallow through the use of a phosphorus halo implant. 18 nm of gate oxide was grown, followed by a partial etch of each wafer to obtain 13 and 9 nm gate oxide thicknesses ($18.2 \pm 0.1 \text{ nm}$ $13 \pm 0.6 \text{ nm}$ and $9.4 \pm 0.4 \text{ nm}$ as electrically measured) without an additional mask. Therefore, each wafer is divided in three areas of different gate oxide thicknesses (plus intermediate gate oxide thicknesses on the transition rows).

Process	Conditions	
Nwell	Dose= $8.5 \cdot 10^{12} \text{ cm}^{-2}$ Energy=120 kV	
Well Drive	T = 1125 C Time = 8.5 hours	
Threshold voltage adjust implant (arsenic)	Dose = $1.2 \cdot 10^{12} \text{ cm}^{-2}$ Energy = 10 kev Dose = $1.5 \cdot 10^{12} \text{ cm}^{-2}$ Energy = 21 kev Dose = $1.1 \cdot 10^{12} \text{ cm}^{-2}$ Energy = 45 kev	Before gate oxidation After gate oxidation After gate oxidation
Gate oxide thicknesses	180 A, 130 A, 90A	by hydrofluoric acid etch back
LDD implant (boron)	Dose = $1 \cdot 10^{14} \text{ cm}^{-2}$ Energy = 5 kev	
Halo implant (phosphorus)	Dose = $1 \cdot 10^{13} \text{ cm}^{-2}$ Energy = 50 kev	
Gate polysilicon (boron)	dose = $4 \cdot 10^{15} \text{ cm}^{-2}$ Energy = 10 kev	
source/drain (boron)	Dose = $4 \cdot 10^{15} \text{ cm}^{-2}$ Energy = 10 kev	
RTA	T = 1050 C Time = 10s	

Table 2: Front end processing steps.

2- 2- 1- Boron Diffusion From The Polysilicon Gate To The Channel

The penetration of boron from the polysilicon gate into the channel has been reported as the most critical problem for the fabrication of p^+ doped polysilicon gate pMOSFETs. Previous studies have reported ways to prevent boron penetration and have described its effects on device characteristics [11][13][19]. Undesired boron in devices channels can result in significant positive shifts of the threshold voltage [15]. This has been modeled as a very thin sheet of fully depleted boron creating excess negative charge at the Si/SiO₂ interface [15][18]. Enhanced boron penetration occurs when BF₂ is used as a gate polysilicon dopant rather than elemental boron [15][16][17][18]. The modification of the characteristics would then include not only a positive shift in the flat band voltage, but also degradation of the subthreshold swing, an increase in the electron trapping rate and a decrease in the low field mobility and in the interface trap density. These instabilities in the device characteristics were attributed to enhanced boron penetration due to the presence of fluorine, but not to the fluorine itself. The fluorine is hypothesized to passivate dangling bonds at the Si/SiO₂ interface creating negative charge which prevents the formation of B₂O₃. In the absence of fluorine, the formation of B₂O₃ reduces boron diffusion through gate oxide [17].

Hydrogen has also been held responsible for enhanced boron diffusion when present during or before, high temperature anneals, its effect being to increase the level of electron traps [13][14]. Boron in itself would not act as an electron trap in SiO₂ but would rather act as a catalysis for water related trap formation in SiO₂ [37].

Based on these considerations, choices were made for the fabrication of the pMOSFETs. Elemental boron was used to dope the polysilicon and to form the source and drain junctions. BF₂ allows sharper source/drain junctions to be formed because of its smaller channelling tailing effect when implanted in silicon. However, in regard to the polysilicon doping considerations previously mentioned, elemental boron was a preferred choice. A thickness of 0.35 μm of polysilicon was deemed to be necessary to prevent any bridging of the silicidation from the gate to the source/drain contacts. Therefore, the use of only the source/drain boron implant to dope the polysilicon gate would not have been quite enough to dope the gate polysilicon to solid solubility (10^{21} cm^{-3}). For this reason,

an additional boron implant was performed prior to the polysilicon gate etch. The boron implant energy was kept to a minimum and a thin cap layer of oxide was deposited prior to the source and drain implant to minimize boron channeling. Finally, the high temperature anneal after boron implantation was limited to a 10 s rapid thermal anneal at 1050 °C.

CHAPTER 3

ELECTRICAL CHARACTERIZATION.

3- 1- Gate Polysilicon Doping

To ensure that a sufficient level of doping was presented in the gate polysilicon, MOS capacitors C-V curves were recorded to test for gate depletion. Flat-band voltage shift and Si/SiO₂ interface state densities were measured to test whether boron had diffused from the gate through the gate oxide and into the channel.

3- 1- 1- Flat-Band Voltage Shift

It has been reported that boron diffusing into the channel of a pMOSFET could be represented by “a very shallow, fully-depleted p-type layer close to the SiO₂/Si interface” [15][18]. If boron were to diffuse through the gate oxide, one would expect to find a higher concentration of boron in the channel of transistors with a thin gate oxide rather than those with a thick gate oxide. An electrical method, similar to the one used by F. K. Baker [3][18], based on the model of a thin sheet layer of boron at the SiO₂/Si interface whose concentration varies with the gate oxide thickness was developed to test for boron penetration. It was used to determine if boron diffused through the gate oxide during the fabrication of the devices studied. In [18] the shift in flat band voltage was recorded, while in this study, the shift in gate bias for a given bend bending across the silicon was determined.

High frequency C-V measurements were carried out for devices with different gate oxide thicknesses (from 18 nm to 9 nm). The measured capacitance can be represented by the gate oxide capacitance in series with the channel depletion capacitance (the gate oxide capacitance values were extracted for gate biases that put the channel into accumulation). Both the total and oxide capacitance are known, and therefore the depletion capacitance can be determined:

$$C_d(vg) = \frac{C_{tot}(vg) \cdot C_{ox}}{C_{ox} - C_{tot}(vg)} \quad (EQ 1)$$

C_d , C_{ox} , C_{tot} are the depletion, gate oxide and total capacitances respectively for a given gate to substrate bias. Using the model of channel boron represented by a sheet layer of negative charges at the SiO_2/Si surface for the depleted channel, the gate to substrate bias that corresponds to a given depletion capacitance can be expressed as:

$$V_g = \phi_{ms} + \phi - \left(\frac{Q_f + Q_d(\phi) + Q_b}{C_{ox}} \right) \quad (EQ 2)$$

ϕ_{ms} is the work function difference between the channel Si and the gate polysilicon, ϕ is the band bending at a given gate bias, Q_f is the fixed gate oxide charge, Q_d is the depletion layer charge for a given band bending and Q_b the negative charge introduced by a fully depleted layer of boron at the Si/SiO_2 interface if present. For no boron in the channel $Q_b = 0$ and, for a given value of the depletion capacitance C_d , V_g versus $1/C_{ox}$ should be a straight line. The curve intersects the V_g axis at $(\phi_{ms} + \phi)$ and the slope of the curve is $(Q_f + Q_d(\phi))$. If boron diffused into the channel and formed a very shallow p-type layer fully depleted when a bias that puts the channel in depletion is applied on the gate electrode. One would expect the slope of V_g versus $1/C_{ox}$ to vary with the gate oxide thickness t_{ox} , since different amounts of boron would diffuse into the channel depending on t_{ox} .

V_g was plotted versus $1/C_{ox}$ for a given value of C_d and for each of the three different type of devices (Figure 5). Straight lines could be fitted to each of them with a correlation coefficient equal or superior to 0.998. Therefore this electrical method does not show any evidence of boron diffusion into the channel.

3- 1- 2- Fast Interface States Measurements

The flat-band shift method was described by some as an effective way to determine if boron diffused through the gate oxide but others suspected that this method might not be precise enough [12]. It was found that before any shift in the flat-band voltage could be detected, evidence of enhanced surface states was found due to the presence of boron in the device channel or in high concentration in the gate oxide.

The level of interface states at mid-gap was measured using a method based on the comparison of high and low frequency capacitances [20]. Figure 6 shows the results

FIGURE 5. Gate voltage versus inverse of gate oxide capacitance for a given value of the depletion capacitance.

FIGURE 6. Dependence of level of interface states charges on gate oxide thickness

obtained for gate oxide thicknesses ranging from 9 to 18 nm. An abnormally high level of interface states charges was visible but no systematic dependance on the gate thickness could be found. Neither could a correlation be found with the way the arsenic was implanted to adjust the threshold voltage (i.e., before or after the growth of gate oxide formation). There are two alternative explanations for these results. The first one would be that the high interface states level found is not correlated to the presence of boron and another source of contamination is to be blamed (possibly radiation damage). The alternative interpretation would be that boron is responsible for this high level of interface states but the gate oxide thickness difference would not significantly modify the interface states level. One possible explanation would be boron channeling through the gate oxide [6] since only the second stage of the polysilicon doping implant was done through an oxide cap. The fact that the gate was deposited in a polycrystalline rather than amorphous phase reinforces this explanation. A gate oxide thickness difference of 9 nm (from 18 to 9 nm) would not significantly modify the amount of boron channeling through it.

Ultimately, it might be thought the most certain way to find out about the boron distribution would be to get a SIMS cross section of the device. However, by the nature of the SIMS technique itself, contamination of the channel by the high level of boron in the gate polysilicon occurs and no conclusive results could be obtained so far from that method. From the set of experiments carried out in this work it could only be concluded that the level of boron in the channel (if any) was not high enough to significantly shift the flat-band voltage of the pMOSFETs and was probably due to channeling diffusion rather than channeling.

3- 1- 3- Boron Doped Gate Polysilicon Depletion

One must also determine whether or not depletion of the boron doped polysilicon gate occurs when a negative bias is applied at the gate terminal. To avoid boron diffusion into the channel the tendency is to reduce the gate polysilicon doping concentration and anneal time which can lead to non-degenerated gate polysilicon doping levels and, possibly, important depletion of the gate polysilicon in the saturation region of operation of the transistor. Depletion of the gate polysilicon increases the effective gate oxide thickness for more negative values of the gate bias such that:

$$t_{oxeff} = \epsilon \left[\frac{1}{C_{dchannel}} + \frac{1}{C_{ox}} + \frac{1}{C_{dpoly}} \right] \quad (EQ 3)$$

Where t_{oxeff} is the effective gate oxide thickness, $C_{dchannel}$ is the channel depletion capacitance, C_{ox} the gate oxide capacitance and C_{dpoly} is the polysilicon gate capacitance. Capacitances on p-well were considered so that $C_{dchannel}$ is infinite for gate biases that correspond to the gate polysilicon being in depletion. t_{oxeff} will be greater than its expected value if the depletion capacitance, C_{dpoly} , is not infinite (i.e., the polysilicon gate is depleted). One would expect the effect of the depletion to be more important for thin gate oxide since a given value of C_{dpoly} (given amount of gate polysilicon depletion) corresponds to a higher proportion of t_{oxeff} .

Gate depletion was investigated using the same high frequency C-V measurements referred to in section 3-1-1. P-well capacitors were used so that for negative bias on the gate the channel would be in accumulation while the gate would be in depletion, giving $1/C_{tot} = 1/C_{ox} + 1/C_{dpoly}$. Figure 7 shows that some depletion of the gate polysilicon is visible for gate oxide thicknesses down to 9 nm. In the worse case at $t_{ox} = 8.95$ nm, the effective oxide thickness would be 9.23 nm at $v_g = -5$ V which would correspond to approximately a 3% decrease in the saturation current (the percentage loss in saturation current can be calculated in a first approximation by the ratio of the oxide capacitance to the effective oxide capacitance at -5 V).

FIGURE 7. Gate polysilicon depletion on devices with $T_{ox}=18$ nm and $T_{ox}=9$ nm.

3- 2- Structure Dependent Electrical Performances

The performances of the pMOSFETs with effective channel lengths between $0.2 \mu\text{m}$ and $0.7 \mu\text{m}$ were compared with special emphasis put on their relative short channel control, since this is an important parameter controlling the hot-carrier-induced degradation.

3- 2- 1- Gate Oxide Thickness

The threshold voltage roll-off (Figure 8) clearly shows the improvement in short channel behavior of devices with a gate dielectric thickness reduction: a thinner gate oxide increases the transverse electric field and reduces the source/drain depletion infringement on the channel charge, which improves the gate control of the channel charge. For channel lengths between 0.4 and $0.6 \mu\text{m}$, the subthreshold slope at $V_{ds}=-0.1$ improves by $10.7 \pm 2\%$ when comparing $t_{ox}=18$ nm to $t_{ox}=9$ nm. The improvement in linear transconductance ($V_{ds} = -0.1$ V) of a device with 9 nm compared to a device with 18 nm of gate oxide thicknesses is shown on Figure 9 (devices were fully identical except for their gate oxide thicknesses)

FIGURE 8. Dependence of threshold voltage roll-off on gate oxide thickness

FIGURE 9. Dependence linear transconductance on gate oxide thickness

3- 2- 2- Threshold Voltage Adjust Implants

Figure 10 shows the dependence of the linear transconductance ($V_{ds} = -0.1$ V) on the threshold adjust profile. The best linear transconductance was obtained at any given channel length for devices with the deep threshold voltage implant. Presumably, the lower surface doping ($< 2 \cdot 10^{17} \text{ cm}^{-3}$ according to PREDICT simulation) created a lower coulomb scattering mobility reduction at the surface of the channel than for the other devices. For the "shallow- V_{th} " and "medium- V_{th} " devices, the transconductance values were very similar. The current sourcing was recorded on devices with $L_g = 20 \mu\text{m}$ and $t_{ox} = 18 \text{ nm}$ at $V_{ds} = -3.5 \text{ V}$ and $V_{gs} - V_{th} = -3.5 \text{ V}$ (the gate bias was chosen so as to have the same level of inversion in the channels since different devices had different threshold voltage values). Less than 2% difference in drain current was found between the "deep- V_{th} " and the "shallow- V_{th} " pMOSFETs (4.58 ± 0.013 against $4.51 \pm 0.02 \mu\text{A}/\mu\text{m}$). Except for the superior linear transconductance values of the "deep- V_{th} " devices due to lower surface doping, no significant difference was found between the performances of the different types of devices. It is possible that the Si/SiO₂ interface states (discussed in section 3-1-2) give a mobility reduction which explains the very small difference in performance.

FIGURE 10. Dependence of linear transconductance on threshold voltage implants

FIGURE 11. Dependence of threshold voltage roll-off on threshold voltage implants.

The roll-off of the threshold voltage in the linear region of operation at $V_{ds} = -0.1$ V did not indicate any significant difference between devices (Figure 11). To get a more sensitive description of their relative short channel behaviors, the subthreshold slope was measured at a bias of -3.3 V on the drain (Figure 12). Two regions of the curve must be considered. For the long channel region (0.45 μm and longer), the subthreshold slope of the "shallow- V_{th} " devices is smaller than that of the other devices. The better slope of the devices with a very shallow threshold adjust implant is explained by the better control of the gate on the channel charges. For channel lengths smaller than 0.4 μm , the subthreshold slope dramatically increases due to the loss of gate control on the channel charge. The subthreshold slope degradation of the device with the very shallow arsenic implant occurs at longer channel lengths because the threshold voltage implant does not act as a punch-through stopper and therefore does not prevent sub-surface punchthrough current as effectively as for the other devices. MEDICI simulations of the drain region for the "shallow- V_{th} " and "deep- V_{th} " (Figure 13) show that the lateral diffusion of the LDD of the former type of devices is much less at the surface but more important deeper in the channel where punchthrough current dominates the degradation of the very short channel devices.

FIGURE 12. Dependence of subthreshold slope on threshold voltages implants.

FIGURE 13. Comparison of the lateral Ldd diffusion in the channel for three different types of devices.

CHAPTER 4

HOT-CARRIER-INDUCED DEGRADATION

Hot-carrier-induced degradation primarily results from geometric scaling while keeping the supply voltage constant. The electric field increases in the device to the point where holes and/or electrons gain sufficient energy between collisions to be injected into the gate dielectric resulting in carrier trapping, bulk trap generation or/and fast interface state creation. Carriers which are highly accelerated by the channel electric field are said to be “hot”. The modification of the charge level of the gate oxide due to the injection of carriers changes the device electrical characteristics. Degraded devices do not match their original specifications and this can lead to the failure of a circuit. N- and p-channel transistors do not suffer from the same type of device characteristic instabilities. The following study will concentrate on pMOSFETs with a surface conduction path.

4- 1- Degradation Monitors

4- 1- 1- Substrate and Gate Current

Substrate and gate currents are important monitors of the population of degradation-inducing hot-carriers in MOSFETs. The level of substrate current is directly related to the lateral peak electric field value which determines how energetic channel carriers are. The gate current is related to the type and number of carriers injected into the gate oxide. It is therefore important to look at what creates and influences gate and substrate currents.

4- 1- 1- a- The Substrate Current

The channel conduction of strongly inverted pMOSFETs is caused by holes drifting from the source to the drain. For high negative values of the drain voltage, and therefore high values of the lateral electric field, the channel holes can acquire enough energy to create electron-hole pairs when colliding with the lattice. Since the peak electric field is located near the drain end where the inversion layer is pinched off, the maximum number of collisions will occur at the drain end. The minimum energy required for a hole to create an electron-hole pair, by so called impact ionization, is 1.55 eV. This is more than the

energy required for an electron to create an electron/hole pair, consequently, the substrate current is smaller for pMOSFETs than for nMOSFETs for a given peak field and channel current. The electrons created by impact ionization are for the most part attracted to the positively biased (relative to the drain voltage) substrate terminal, though, under appropriate bias conditions some will contribute to the gate current. Secondary holes are captured by the drain and provide an increased in drain current [23].

As the voltage applied on the gate is swept from zero to high negative values, at a given drain voltage (e.g.: -5.5 V as in Figure 14), the number of channel majority carriers increases while the peak lateral electric field decreases. These two effects explain the bell shape of the substrate current (I_{sub}) versus gate bias curve (chapter 3 of [23]). I_{sub} peaks around -1.5 to -2.5 V bias. It increases as the number of channel carriers increases and then falls off due to the decrease in the electric field value. The impact ionization level is exponentially related to the electric field (page 125 of [23]) according to:

$$\frac{I_{sub}}{I_d} = A (V_{ds} - V_{dsat}) \exp\left(-\frac{E_0}{E_m}\right) \quad (EQ 4)$$

with E_m the peak electric field, E_0 and A are parameters that depend on the type of carrier (electrons or holes). Hence small changes in the electric field have a large effect on the substrate current level.

Due to the dependance of the substrate current on the electric field, gate oxide thickness as well as channel length are expected to modify this value. Figure 14 and Figure 15 show the substrate current at different gate oxide thicknesses and doping profiles measured on the transistors fabricated here. The thinner gate oxides, exhibit higher a substrate current level since the lateral channel electric field increases with gate oxide thickness reduction according to the empirical relation (page 124 of [23]):

$$E_m = (V_{ds} - V_{dsat}) / (0.22 \cdot t_{ox}^{1/3} \cdot x_j^{1/2}) \quad (EQ 5)$$

V_{ds} and V_{dsat} are the drain and saturation voltage, t_{ox} the gate oxide thickness and x_j the junction depth. From this equation it is seen that the reduction of V_{dsat} through the channel length reduction would contribute to increasing E_m , and therefore to increasing

the substrate current. Variations in the channel doping level and shape also modify the substrate current (Figure 15), an effect which will be discussed in section 4-1-1-c. The source/drain junction depth x_j would have an effect as well but this parameter was kept constant in this experiment. The halo described in section 2-1-3 is known to contribute to increasing substrate current [3] (however no device lacking halos were fabricated here for comparison). For the case of pMOSFETs the move from a buried to surface channel design also has an impact on the substrate current amplitude. Surface pMOSFETs like the ones presented in this work are found to generate more substrate current than their buried counterparts [3] due to their highly doped channel (no counter doping and the increased doping of the threshold voltage implant).

The ratio of the substrate current to the source current (I_{sub}/I_s) depends exponentially on the inverse of the peak electric field (as per equation 4) and can be used to detect changes in the peak electric field values induced by gate oxide charge level variations. At the drain end, the local variations in the amount and sign of the bulk or surface gate oxide charges can influence the channel electric field [22][26][30]. Negative charges in excess in the gate oxide in the vicinity of the drain would cause a positive local increment of the flat-band voltage of the pMOSFET, which would allow the transistor to turn ON more easily. The accumulation of positive mobile charges in the channel contributes to increasing the drain junction depletion width which reduces the peak channel electric field. Positive trapped charges in the oxide would have the opposite effect. Therefore, a reduction of I_{sub}/I_s can be interpreted as negative charges being trapped in the gate oxide at the drain end, whereas, an increase in I_{sub}/I_s would be attributed to positive trapped charges. In the following study, both I_{sub} and I_{sub}/I_s will be referred to as monitors of the number of hot-carriers in the channel and variations in the gate oxide charge level. This will be important since as will be described in section 4-2-2, the main effect of degradation due to hot-carriers is a local modification in the level of oxide charges.

4- 1- 1- b- Gate current

The gate current is the result of hot electron injection from the channel into the gate oxide which can occur in both n and p-channel MOSFETs. The gate current can be explained by the “lucky electron” model [23][51] that states that for an electron to be

injected into the gate oxide a series of independent events must take place: 1) the electron must gain enough energy (about 3.1 eV) from the channel field to surmount the Si/SiO₂ barrier 2) it must have its momentum redirected towards the gate electrode 3) it must not lose its energy either through collision in the Si bulk before reaching the gate or in the image potential well. The gate current can be calculated for simulation purposes by considering the probability that these three events will occur. The same principle applies to holes except that they must surmount a Si/SiO₂ barrier increased by the silicon band gap height (1.1 eV) which explains the lower level of hole injection compare to electron injection.

At low gate bias (in absolute value) and sufficiently high drain voltage ($|V_g| < |V_d|/2$) electron injection into the gate oxide of a pMOSFET can occur, since the high lateral electric field at the drain end (high $|V_d|$) generates hot-electrons through impact ionization and the gate oxide transverse electric field near the drain accelerates them towards the gate electrode.

Figure 14 shows the gate current, I_g , recorded on several of the surface pMOSFETs fabricated. It shows that the gate current peaks at low gate bias where the transverse field favors electron injection and that at higher values ($|V_g| = |V_d|$), where the electric field would favor hole injection, no gate current can be detected. In contrast to n-channel devices, p-channel devices exhibit high gate current values that can easily be measured [35]. In the experiments discussed here, the minimum drain bias used was -5.5 V for which the gate current can be determined by direct measurement for transistors with gate lengths up to 0.8 μm for the thickest gate oxide. Figure 14 and Figure 15 show that the dependance of the gate current on the various design parameters follows the same trend as for the substrate current. From Figure 14, one sees that I_g increases as the gate oxide thickness is reduced. This is due to both the increase in the aiding gate oxide field and the increase in the number of hot-carriers due to a higher channel field.

4- 1- 1- c- Substrate And Gate Current Dependence On the Channel Design:

The channel doping profile has a strong impact on both the substrate and gate current amplitude. Table 3a and 3b show the gate and substrate current dependence on the

channel doping profile for devices with 18 nm gate oxide thickness and 0.65 to 0.7 μm channel lengths, measured at $V_{ds}=-6$ V and on 5 μm devices at $V_{ds}=-7$ V measured on different wafers.

Vth implant type	Vth long (V) $V_{ds}=-0.05\text{v}$	Isub/Is (1E-3) at peak Ig	Isub (nA/ μm) at peak Ig	Ig (pA/ μm) at peak Ig	Ig/Is (1E-6) at peak Ig	Ig/Isub (1E-5) at peak Ig
deep-Vth	-0.98	27 ± 3.5	141 ± 24	10 ± 2.3	2.05 ± 0.5	7.5 ± 1.4
shallow-Vth	-1.13	21 ± 3.2	83 ± 20	4.1 ± 0.6	1.25 ± 0.7	2.9 ± 2
medium-Vth	-1.3	33.3 ± 2.7	98 ± 16	4.7 ± 0.24	1.64 ± 0.45	4.9 ± 0.98

Table 3a: Dependence of gate and substrate currents on threshold voltage implants for short channel devices ($l_{eff} = 0.65\text{-}0.7$ μm , $V_{ds} = -6$ V).

Vth implant type	Vth long (V) ($V_{ds}=-0.05\text{v}$)	Ig (pA/ μm) at peak Ig	Isub (nA/ μm) at peak Ig	Isub (nA/ μm) at peak Isub
deep-Vth	-0.98	17.95	71	127
shallow-Vth	-1.13	8.15	42.3	87
medium-Vth	-1.3	12.23	65.5	128.5

Table 3b: Dependence of gate and substrate currents on threshold voltage implants for long channel devices ($l_{eff} = 5$ μm , $V_{ds} = -7$ V).

It appears that the devices with highest V_{th} and intermediate surface doping level (“medium- V_{th} ”) also have the highest substrate to source current ratio, and hence the highest E_m . This result is not surprising since one would expect devices with a highly doped channel to have a high electric field, and therefore more impact ionization per carrier in the channel. However, the devices with a deep arsenic implant, which results in a lower threshold voltage than that of the devices with a shallow one, have a higher rate of impact ionization than their shallow counterparts. Medici simulations of substrate current for two such structures were made and showed the same trend. According to the simulations, more impact ionization (caused by a higher field) takes place in the devices with a deep threshold voltage implant than in the devices with a shallow implant which explains the difference observed in the level of substrate current.

The highest level of gate current was found for the devices with the lowest V_{th} and the deep implant. This can in part be explained by the high substrate current, since the gate

current comes from secondary electrons created by impact ionization. The devices with a deep implant have a high level of gate current compared to the devices with a shallow V_{th} implant because more secondary electrons are available due to a higher impact ionization rate (as previously explained). However, the gate current level is higher for “deep- V_{th} ” devices than for “medium- V_{th} ” devices, whereas their impact ionization rate is lower. A possible explanation would be that a smaller V_{th} causes the gate current to peak at a lower gate bias therefore at a higher gate to drain voltage difference. In other words, the electrons are injected into the gate oxide at the drain end, helped by a higher vertical gate electric field (for devices with 5 μm of channel length the difference in gate current between the “deep- V_{th} ” and “medium- V_{th} ” is still there but smaller). The gate current seems to be monitored by two parameters, the level of secondary electrons in the channel and the vertical energy available for them to surmount the Si/SiO₂ potential and the image potential well. To understand the gate and substrate dependance on the different type of devices we had to consider the shape of the threshold voltage adjust implant as well as the value of the threshold voltage. We will see how these parameters relate to the difference in degradation between different channel profiles.

FIGURE 14. Dependence of substrate and gate current on gate oxide thickness.

FIGURE 15. Dependence of substrate and gate current on threshold adjust profile

4- 1- 2- Oxide Traps And Interface States:

We saw how channel carriers could become hot and gain enough energy to be injected into the gate oxide and give rise to a gate current. A proportion of the carriers injected contributes to the gate current. Some are scattered back into the channel and some do not make it all the way to the gate terminal and so are trapped in the oxide [23][54]. Those injected carriers are usually electrons at $|V_{ds}| > |V_{gs}|$ but could also be holes injected at $|V_{ds}| = |V_{gs}|$ [35][29], but in too small a quantity to be detected as gate current.

The oxide defects introduced by hot-carrier stressing can be divided in two groups. The first type of defects are interface traps or interface states which are localized at the Si/SiO₂ interface. Interface traps can change their charge states by the capture or release of holes or electrons. Their charge level depends on their position with respect to the fermi level. The second type of defects are the fixed oxide traps. They are located more into the

bulk of the oxide and do not exchange mobile carriers with the channel so their charge stays fixed [55]. Carrier traps can either be created or filled during hot-carrier stress.

Hu *et al* [54] proposed a model that could explain the creation of interface states subsequent to hot-carrier stress. The last step of a MOS process is usually a post-metallization anneal at low temperature in hydrogen ambient (e.g. 450° C for the process described here) intended to passivate by bonding to atomic hydrogen the Si dangling bonds introduced during the process. The number of process related interface states is greatly reduced by this passivation step. When an electron is injected at high energy into the gate oxide it can break a Si-H bond which has an energy of only 0.3 eV. The Si⁰ trivalent silicon atom left creates an interface state.

Water related oxide electron traps were found to be enhanced by high level of boron in the gate oxide according to the following model:

Different oxide and interface trap models have been proposed in the literature, some involving two step trap generation processes. Hot hole injection into the gate dielectric is believed to enhanced interface state creation [53][52]. The study of interface states and trap formation is a complex field of microelectronics beyond the scope of this work therefore the physics of the gate oxide defects will not be discussed further and the hot carrier induced defects in the dielectric will simply be seen as positive or negative charges, bias dependant or not (further readings in [41]).

4- 2- Mechanisms Of Hot-Carrier-Induced Degradation In Surface pMOSFETs

4- 2- 1- Bias Of Maximum Degradation

For nMOSFETs the maximum degradation of the device characteristics due to hot carriers takes place at the gate voltage that corresponds to the maximum substrate current. That is because n-channel transistor degradation is mainly due to the formation of interface traps which are created in high number at the peak of substrate current (i.e. highest channel electric field). The situation for pMOSFETs is different. It has been argued by some that the maximum degradation correlates with the peak of the substrate current, ($I_{\text{sub-peak}}$) just as for nMOSFETs, [26][29] and to the peak of the gate current, $I_{\text{g-peak}}$ by others [32][33][35].

To clarify this point three different device types with effective channel lengths between 0.2 and 0.6 μm were stressed for 5000 s at -7 V on the drain and with a gate bias corresponding to the maximum gate current or the maximum substrate current. In both cases the bias conditions put the device in saturation. This was the only stress bias condition studied in this work, even though, it was reported that degradation caused by different mechanisms could be found under different bias conditions (e.g., $V_d = V_g$ [29][35]). The peak linear transconductance g_m ($dI_{\text{ds}} / dV_{\text{gs}}|_{V_{\text{ds}}}$), the extrapolated threshold voltage, V_{th} (intersection of the line of maximum slope with the gate voltage axis in the I_d - V_{gs} plot) and the subthreshold swing S^1 ($d\log I_{\text{ds}} / dV_{\text{gs}}|_{V_{\text{ds}}}$) were recorded at $V_{\text{ds}} = -0.1$ V, as well as the OFF current (drain current at zero volt on the gate and $V_{\text{ds}} = -0.1$ V). Figure 16, Figure 17, Figure 18 and Figure 19 show the percentage of degradation of each of the three former parameters. The level of OFF current before stress is below the noise floor of the instrument used to record these data, therefore, the actual values of the current after stress were plotted rather than the percentage of degradation. Three points can be made from these plots. First, the three former parameters were more degraded when the devices were stressed at $I_{\text{g-peak}}$ than when stressed at $I_{\text{sub-peak}}$. That would mean that devices should be stressed at the gate bias that corresponds to the peak gate current to evaluate the worst

1. The term "swing" is used to describe the inverse of a slope

case degradation in surface pMOSFETs. The second point to be made is that the difference in the degradation level is not dramatically different between the two types of biases. The difference becomes greater than the measurement error only for devices with effective channel lengths smaller than $0.4\ \mu\text{m}$. This corresponds to the observations made by Brassington *et al* [32] that for surface pMOSFETs the maximum degradation of saturated and linear parameters would occur at the peak gate current but the shift of those parameters would still be significant when stressed at the peak substrate current. Finally, the OFF current behaves in a very different way than the other parameters since more leakage current results from the stress at $I_{\text{sub-peak}}$ than the stress at $I_{\text{g-peak}}$. The difference, though small, was very repeatable from die to die and wafer to wafer and will be explained in section 4-2-3-a.

FIGURE 16. Comparison of the linear transconductance shift with devices stressed at maximum gate current or maximum substrate current ($V_{\text{ds}} = -0.1\text{ V}$).

FIGURE 17. Comparison of the threshold voltage shift with devices stressed at maximum gate current or maximum substrate current ($V_{ds} = -0.1 V$).

FIGURE 18. Comparison of the subthreshold slope shift with devices stressed at maximum gate current or maximum substrate current ($V_{ds} = -0.1 V$).

FIGURE 19. OFF current after stress at maximum gate current of maximum substrate current ($V_{ds} = -0.1V$).

Unless explicitly stated otherwise, all stress data reported below will be for the saturation region of operation of the devices: at the gate bias that corresponds to the maximum gate current. Table 4 summarizes the gate to source biases corresponding to the maximum gate current for each type of device with $t_{ox}=18$ nm, -6 V on the drain and effective channel length of 0.65 to 0.7 μm .

Vth implant	deep- V_{th}	shallow- V_{th}	medium- V_{th}
$L_{eff} = [0.65-0.7] \mu m$			
Gate Bias (V) corresponding to the peak I_g	1.42 ± 0.08	1.45 ± 0.15	1.6 ± 0.05

Table 4: Gate biases of the maximum gate current at $V_{ds}=-6$ V and $t_{ox}=18$ nm.

The gate biases at which the maximum gate current occurs change slightly with channel length variations and drain biases (following the same trend as the threshold voltage).

4- 2- 2- Hot-electron trapping

The linear transconductance and current characteristics of a half micron channel length pMOSFET with 18 nm gate oxide thickness stressed in the reverse¹ mode for 10 000 s at -5.5 V on the drain and at -1.2 V on the gate (maximum I_g) are illustrated in Figure 21 and Figure 22. One can see from these figures that peak g_m increases and that the linear current characteristic is shifted to more positive values of the gate voltage. In other words the threshold voltage is smaller in absolute value after degradation. For that reason, at a given gate bias, it appears that degraded pMOSFETs have a higher current sourcing level. The current in saturation also increases with stress, but so does the output resistance. All these observations have in common their resemblance to what, one would expect for a shortening of the channel of the stressed pMOSFETs. That is indeed what studies on buried channel pMOSFETs degradation due to hot-carriers have shown in [22][27][29][35]. The channel electric field peaks in the vicinity of the drain diffusion. Under the bias conditions considered ($V_{gs}=-1.2$ V, $V_{ds}=-5.5$ V), the oxide electric field favors electron injection resulting in a large gate current flow (section 4-1-1-b). Therefore, hot electrons are injected into the gate oxide in the vicinity of the drain where some of them are trapped. Electrons trapped in the gate oxide at the drain end locally modify the surface potential because of the increase in flat-band voltage of the oxide in the area where the negative charges were introduced (Figure 20). If the number of trapped electrons is high, the surface of the degraded part of the channel will tend to always be more inverted than the rest of the channel, effectively acting as an extension of the drain.

The characteristics of the transistor, such as the peak g_m , are now limited by the undegraded part of the channel whose effective length is shorter than that of the initial device. This leads to the observed increase of the peak g_m . From the experimental results obtained in this work on surface pMOSFETs, it appears that the dominant mode of degradation at half micron channel length can be attributed to the reduction of the effective channel length due to hot electrons trapped at the drain end resulting in electrical charac-

1. "reverse" means that the drain and source terminal were interchanged after stress. In other words the stress induced charges trapped in the gate oxide are located at the source end.

teristics degradation due to short channel effects. This corresponds to observations made in previous work on buried pMOSFETs. It is also the dominant degradation mechanism for surface pMOSFETs [29][32][35]. However, a secondary degradation mechanism also exists for surface pMOSFETs that involves stress-induced interface state creation. This will be discussed in the next section.

FIGURE 20. Schematic representation of the inverted channel of a pMOSFET after stress.

FIGURE 21. Shift in the hot-carrier-induced linear transconductance after stress at maximum gate current ($V_{ds} = -0.1\text{ V}$).

FIGURE 22. Shift in the hot-carrier-induced drain current after stress at maximum gate current ($V_{ds} = -0.1\text{ V}$).

4- 2- 3- Interface States

Studies have also focused on pMOSFETs with a surface conduction path to determine if the model previously discussed could fully describe the degradation of transistors with gate polysilicon doped with boron. It was found that surface pMOSFET degradation mechanisms were more complex than the those of their buried counterparts. After stress at low gate bias, the threshold voltage measured in the saturation region of long channel surface pMOSFETs was found to become more negative [29]. These observations were contrary to the shift towards more positive threshold voltage observed in any region of operation for buried pMOSFETs and in the linear region of operation for surface pMOSFETs. This was explained by stress-induced-positive charges closer to the source than the trapped electrons and whose influence on the characteristics was only visible when the drain depletion would screen part of the trapped electrons [29]. Several other studies reported evidence of interface trap creation due to hot-carrier injection which could be detected by charge pumping techniques [25]. At the Si/SiO₂ interface of the nwell of a pMOSFET in inversion, acceptor type interface states in the higher part of the band gap are above the fermi level, therefore empty and neutral and cannot contribute to the electrical characteristics shift observed after stress (Figure 23). On the other hand, donor like interface states that occupy the lower part of the energy band gap are empty, therefore positively charged above the fermi level. This later case corresponds to the inverted channel of a pMOSFET. Hence, both interface states and trapped holes appear as positive charges but the former are bias dependant due to their occupancy dependance on the surface potential, whereas the later are fixed charges independent of the bias conditions [55].

Two types of measurements carried out on the devices fabricated here showed behavior that could not be explained by the simple model of electron trapping at the drain end of the channel. The first evidence of interface state formation during stress was an increase in drain current at zero bias on the gate terminal that was not due to punch-through, but rather to a gate induced drain leakage current (GIDL)[39][40]. The second, more direct, evidence for interface state formation was obtained by detrapping of the injected gate electrons. These measurements are discussed below.

FIGURE 23. Energy band diagram for the channel of a pMOSFET in inversion with fast surface states charges at the Si/SiO₂ interface.

4- 2- 3- a- Gate Induced Drain Leakage (GIDL)

Section 4-2-1 showed that the strongest degradation of all electrical parameters was obtained at gate biases that corresponded to the maximum gate current, except for the OFF current shift that was maximum for stress at $I_{\text{sub-peak}}$. If the stress induced OFF state current were due to bulk punchthrough or drain induced barrier leakage, one would expect it to be highest for devices stressed at $I_{\text{g-peak}}$, since the threshold voltage shift was the greatest for these devices (the absolute value of the threshold voltage is more reduced for devices stressed at $I_{\text{g-peak}}$ than devices stressed at $I_{\text{sub-peak}}$).

To understand the observed OFF state current increase, the source terminal was left floating to insure that no current would come from the source. The drain to substrate current was recorded after stress (100 s at $V_{\text{ds}}=-6$ V, in the same manner than in the previous experiments). To make the GIDL more visible, measurements were made with a slightly positive gate bias (+1 V) to enhance the effect of a positive gate to drain bias without forward biasing the drain to substrate diode. Two regions are visible on the plot of I_{d} versus V_{gd} (Figure 24). At high gate to drain voltages, a drain to substrate current can flow

due to band to band tunneling of carriers along the Si/SiO₂ interface. For high negative values of the drain bias, the GIDL is smaller after stress than before due to the flat-band voltage shift induced by the trapped negative charges [39][40]. This effect corresponds to the channel shortening model and does not explain the observations made on the OFF state current. On the other hand, the GIDL was found to increase significantly after stress in the low range of the drain bias. For low gate to drain biases the field is not high enough for band-to-band tunneling to occur, however the presence of negatively charged acceptor type interface states was found to help electrons tunneling from the valence to the conduction band (the electrons now can tunnel from the valence band to an interface trap then be excited to the conduction band). Figure 24 shows an increase of the GIDL current after stress a low IV_{gdl} bias that can only be explained by acceptor type interface states generated in the drain region during stress.

FIGURE 24 GIDL current before and after stress.

4- 2- 3- b- Hot Electron Detrapping

The presence of interface states (and positive charges) is difficult to detect in surface pMOSFETs because they are screened by trapped electrons which are the dominant cause of degradation. To have direct evidence of interface states visible on the electrical characteristics one would have to suppress the effect of the trapped negative charges. It has been reported that electron detrapping can occur quite easily when an appropriate electric field is applied on the gate of a device (this is one of the arguments given to explain the lower degradation of pMOSFETs by AC stress than would be obtained by DC stress [41]). Here the linear transconductance of a pMOSFET was recorded on an unstressed device, then on a device stressed for 100 s at -6 V on the drain and finally after 500 s under detrapping bias conditions. The detrapping bias conditions consisted in application of a -6 V bias on the gate oxide, with all other terminals grounded. The device was heated to 70 °C to increase the detrapping rate [34]. From Figure 25, one clearly sees that after detrapping, the transconductance characteristic is not back to its original form since the peak of G_m is now lower than it was before stress. The strong increase in peak g_m due to the reduction of the effective channel length disappears after detrapping because the area near the drain is no longer subject to an enhanced inversion; further, the peak is now reduced below its initial value due to the effect of interface states also caused by stressing. This result is similar to nMOSFET degradation which is dominated by stress generated interface states [34]. The effective mobility is reduced due to interface states either because fewer carriers (holes) are available for the conduction, or because of an increase of the surface scattering [22]. The effects observed are consistent with the presence of interface states created by stressing.

These experiments point to the presence of stress induced interface states. No evidence of trapped holes was found; however, they are often associated with the presence of interface states due to their high interface state generation efficiencies.

FIGURE 25. Linear transconductance characteristics after stress and after electron detrapping ($V_{ds} = -0.1$ V).

4- 2- 4- Time Dependence Of The Degradation

Hot-carriers injected into the gate oxide can create electrical characteristics shifts over a long period of time. The time dependence of the degradation has been widely studied for nMOSFETs to find ways of predicting their lifetimes. The lifetime of a device is defined as the time taken for a given electrical parameter to shift by a given percentage under the worst bias conditions. There is an important difference between the time dependence of the degradation for nMOSFETs and pMOSFETs. Several approaches are taken to relate the degradation level with time for nMOSFETs; however, they are all based on a power law dependence of the degradation level with time (i.e.: $D = D_0 t^n$, D the degradation and t the time) [23]. For pMOSFETs the matter is more complicated. The degradation does not have a simple power law dependence with time since a saturation of the degradation occurs [35]. Figure 26 shows this effect, present for all type of pMOSFETs studied here (note the Log scale for the horizontal axis).

The time dependence of the substrate and of the gate current will help explain this saturation phenomenon [30]. Figure 27 shows the time dependence of the gate and substrate current of a pMOSFET subjected to stress. Both the gate and substrate current decrease with time and so does the ratio of the substrate to drain current which is proportional to the channel electric field. Therefore, the degradation leads to a reduction of the source of excitation of the channel carriers which partially explains the saturation observed (we explained in section 4-1-4-a that electrons trapped in the dielectric near the drain reduced the peak electric field). The accumulation of negative charges in the gate oxide creates a local vertical electric field in the gate oxide that tends to repel further injection of negative charges which contributes to the saturation effect (on the other hand, it has been suggested that filling of already existing traps rather than the creation of new ones could explain this saturation of the degradation with time [34][38]).

FIGURE 26. Dependence of the peak linear transconductance degradation on time

FIGURE 27. Time dependance of gate and substrate current of a pMOSFETs under stress

4- 3- Detailed Study Of The Linear Transconductance Degradation

As explained in section 4-2-2, the degradation of pMOSFETs leads to a reduction of effective channel length due to the enhanced channel inversion at the drain end caused by the localized trapping of negative charges in the oxide. Consequently, there is a positive increment in the threshold voltage due to short channel effects and the peak linear transconductance is increased. It was also found in section 4-2-3-b that the increase in the peak g_m value hides an effective decrease of the mobility due to interface states. The transconductance stress-induced shift is more complex than a simple increase in the peak value due to effective channel length reduction.

The observation of the g_m characteristics over a wider range of gate voltage revealed that the degradation does not affect only the peak g_m . Stressed devices showed a more abrupt fall of their transconductance with increased gate bias than non stressed pMOSFETs. Figure 28 illustrates this effect with the characteristics of an unstressed device

compared to its characteristics after 100 s of reverse stress at -6 V on the drain, and to the unstressed characteristics of a second device with a peak transconductance value similar to the one of the stressed device. The reduction of the effective channel length can account for the increase of the peak value of the transconductance but does not explain its faster fall off with increased gate bias. The more dramatic fall of the transconductance with increased gate voltage for the stressed devices than for the unstressed devices could be explained by a higher series resistance in the channel or/and the degradation of the mobility, as discussed below.

FIGURE 28. Stress-induced linear transconductance degradation at high gate bias.

4- 3- 1- Increased Channel Resistance

The detrapping of electrons was used to get a better understanding of this enhanced transconductance degradation at high gate bias. Figure 29 shows the transconductance characteristics first after 100 s of stress at $V_{ds} = -6$ V and then after 500 s of detrapping at $V_{gs} = -6$ V with all the other terminals grounded and the device heated up to 70°C . We see that for $V_{gs} = -3$ to -6 V, the transconductance of the stressed device whose gate negative charges were detrapped is back to its unstressed value whereas at low gate bias the transconductance is reduced presumably due to interface states. This result shows that the transconductance degradation visible in the higher range of gate voltages cannot be attributed to the interface states but rather to the electrons trapped into the gate oxide after stress

FIGURE 29. Recovery of the linear transconductance degradation at high gate bias after detrapping.

Resistances introduced by stress have often been reported for unoptimized LDD nMOSFETs [47] but not very often for pMOSFETs [46]. nMOSFETs with too lightly doped an LDD region could suffer from increased drain depletion due to the accumulation of stress-induced negative charges trapped in the oxide above the LDD. The pMOSFETs studied here have a surface LDD doping of $3 \cdot 10^{19} \text{ cm}^{-3}$ (as obtained by SUPREM simulation) which is a fairly high doping for a LDD diffusion. Moreover, negatively charged trapped carriers above the drain would tend to reduce the width of a p-depleted region rather than increase it. Hence, the mechanism for the increased resistance cannot be the same as for nMOSFETs. As mentioned previously, a pMOSFET whose degradation is dominated by locally trapped electrons can be modeled as two transistors in series [35]. The undegraded part of the channel, which is identical to the initial transistor, except that its effective channel is smaller, is in series with the degraded part of the channel which in turn can be represented as another transistor with a less negative threshold voltage (Figure 30). Since the degraded region of the channel will always be turned on earlier than the rest of the channel, it acts as an extension of the drain (or the source if terminals interchanged after stress) diffusion that would be extremely lightly doped. When the transconductance of the degraded device is compared to the characteristics of an undegraded device with an identical peak g_m (i.e., a device with roughly the same gain), the transconductance of the degraded device falls off much more rapidly with increases of gate bias due to the high resistance introduced by this lightly doped extension of the drain.

FIGURE 30. Schematic representation of the stress-induced increased channel resistance

4- 3- 2- Mobility Reduction

Detrapping showed that the apparent increase in the transconductance peak value of the transconductance hides an effective reduction of the mobility, either due to the reduction of the number of free carriers in the channel or due to the increase in surface scattering. Based on the observations made previously, the relative impact of effective channel reduction, channel resistance increase and mobility reduction was studied in this work, as discussed below.

The empirical effective mobility model $\mu_{\text{eff}} = \mu_0 / (1 + \theta_0(V_{\text{gs}} - V_{\text{T}}))$ [45] where θ_0 is the mobility degradation due to the vertical electric field, μ_0 is the low field mobility and V_{T} the extrapolated threshold voltage, was found to be satisfying for devices fabricated here with a thick gate oxide but did not give good results for the thinner devices. An improved mobility model was subsequently used that gave better results at all gate oxide thicknesses (uses second order term (θ_1) to better describe the effective mobility reduction caused by the vertical electric field). A formula for the drain current was derived with this

mobility model that takes into account the source and drain resistances that cannot be neglected for short channel devices [45].

The mobility model used was:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_0 \cdot (V_{gs} - V_T) + \theta_1 \cdot (V_{gs} - V_T)^2} \quad (EQ 6)$$

This gives the following expression for the drain current [48] which is taken as the basis of the present work:

$$I_{ds} = \beta \cdot \frac{(V_{gs}' - V_{th} - 0.5V_{ds}') V_{ds}'}{1 + \theta_0 (V_{gs}' - V_{th} - 0.5V_{ds}') + \theta_1 \cdot (V_{gs}' - V_{th} - 0.5V_{ds}')^2} \quad (EQ 7)$$

With $V_{gs}' = V_{gs} - R_s I_{ds}$, $V_{ds}' = V_{ds} - R_d I_{ds}$ and $R_t = R_s + R_d$, where R_s and R_d are the resistances introduced by the source and drain respectively. For a device that has not been stressed, the source and drain resistances can be considered equal and $R_s = R_d = R_t / 2$. The gain parameter of a MOSFET of unit width (1 μ m) can be expressed as $\beta = \mu_0 C_{ox} / L_{eff}$ where μ_0 is the low field mobility (cm²/V s), C_{ox} the gate oxide capacitance (in F / cm²) and L_{eff} the effective channel length (in μ m). The threshold voltage V_T , extrapolated from the maximum slope of the I_d - V_g characteristics can be used rather than the intrinsic threshold voltage, V_{th} , by setting $V_T = V_{th} + 0.5V_{ds}$. The equation (7) can be rearranged to get a simpler expression:

$$I_{ds} = \beta \cdot \frac{V_{gt} \cdot V_{ds}}{1 + (\theta_0 + \beta R_t) \cdot V_{gt} + \theta_1 \cdot (V_{gt})^2} \quad (EQ 8)$$

With $V_{gt} = V_{gs} - V_T$. In the following we will let $U = \theta_0 + \beta R_t$.

Equation (8) can be differentiated with respect to the gate voltage to get an expression for the linear transconductance: $g_m = \left[\frac{\partial}{\partial V_{gs}} I_{ds} \right]_{V_{ds}}$

$$g_m = \frac{\beta \cdot V_{ds} \cdot \left[1 - (\theta_1 \cdot (V_{gt})^2) \right]}{\left[(1 + UV_{gt} + \theta_1 \cdot (V_{gt})^2) \right]^2} \quad (\text{EQ 9})$$

Long channel devices ($L_g = 20 \mu\text{m}$) were used to determine the mobility degradation factors, θ_0 and θ_1 , because for the long MOSFETs the source/drain resistance could be neglected compared to the channel resistance. The source/drain resistance was evaluated using an existing extraction program [56] (also used for the effective channel evaluation) based on the linear extrapolation of the channel resistance to $L_{\text{eff}} = 0$. The extracted source/drain resistance was $R_t = 236 \pm 37 \Omega$. Fit of experimental characteristics of long channel devices gave $\theta_0 = 0.15 \text{ V}^{-1}$. However, a discrepancy between the θ_1 coefficient (0.0064 V^{-2}) extracted from the long channel devices ($L_g = 20 \mu\text{m}$) by neglecting the source/drain resistance, and the value (0.0045 V^{-2}) necessary to get a good fit to equation (9) for short channel devices was found. This could be due to a limitation of the mobility model used at high gate bias values and it prevented precise quantitative comparison of the resistance introduced by stress between the different structures.

Figure 31 shows the linear transconductance characteristics of an unstressed device with an effective channel length of $0.41 \mu\text{m}$ and 9 nm thick gate oxide also with the transconductance characteristics obtained from equation (9) using the extracted degradation coefficients (θ_0 and θ_1) and resistance values. Figure 32 shows the calculated linear transconductance characteristics assuming that the only degradation mechanism is a 14% reduction of the effective channel length of the device (i.e., the channel length reduction is calculated by matching of the maximum g_m in a first approximation). In the range of high gate voltages, the analytical expression and the stressed characteristics do not match due to the increase in channel resistance that was not taken into account in the analytical expression. From the characteristics of the transconductance after detrapping (L_{eff} back to

its initial value) it appears that the low field mobility was reduced by 10% (Figure 33) due to the stress. This mobility reduction if not taken into account leads to an underestimate of the effective channel length reduction by comparison of the peak g_m before and after stress (i.e.: 22% reduction of L_{eff} rather than 14%).

FIGURE 31. Analytical expression of transconductance, fit to the experimental data ($V_{ds} = -0.1 V$)

FIGURE 32. Analytically determined transconductance characteristics, adjusted for channel length compared to the experimental data.

FIGURE 33. Analytically determined transconductance characteristics, adjusted for mobility compared to the experimental data.

4- 4- Influence Of The Device Structure On The Degradation Level

4- 4- 1- Oxide Thickness Dependence

Resistance to hot carrier induced degradation was compared for devices with two different gate oxide thicknesses, $t_{ox}=18$ nm or 9 nm. It was found that in the linear region of operation, thinner gate oxide devices degrade less than thicker gate oxide devices. Similar observations were reported for both nMOSFETs [43][44] and buried pMOSFETs [42] but the explanation for such phenomenon was different depending on the type of device. For the nMOSFETs the reduction in mobility due to stress induced interface states was found to be less for devices with thinner gate oxide due to the smaller impact of a given amount of interface states on the mobility for thinner than for thicker gate oxide devices. Buried pMOSFETs with thin gate oxides also showed better immunity to hot-carrier-induced degradation but for a different reason than surface nMOSFETs. It was explained that the thinner the gate oxide, the more the carriers got trapped above the drain rather than above the channel which reduces their impact on the electrical characteristics.

In this experiment, the reverse saturation current and the extrapolated threshold voltage shifts in the linear region of operation were recorded after 100 s of stress at -6 V on the drain on transistors with effective channel lengths between 0.25 and 0.7 μm . Thinner gate oxide devices appeared to be more resistant to the degradation (Figure 34, Figure 35). The difference was more pronounced in the lower range of channel lengths. These observations seemed at first surprising since the channel peak electric field is higher for the devices with the thin gate oxide (and the amount of electrons injected into the gate oxide (see section 4-1-1). From the previous discussion we know that two competing degradation mechanisms take place when surface pMOSFETs are stressed in the saturation region: electron trapping and interface states generation. The electron trapping dominates the shift of the electrical characteristics. The better short channel control of devices with a thin gate oxide explains for their lower degradation level. Different rates of degradation for buried pMOSFETs have been explained by Hiroki *et al* in terms of differences in the location of the electric field peak, and hence differences in the location of trapped hot electrons. We will see that this model could explain the observation made here on the dynamics of the degradation.

FIGURE 34. Influence of the gate oxide thickness on threshold voltage degradation ($V_{ds} = -0.1 \text{ V}$).

FIGURE 35. Influence of the gate oxide thickness on saturation current degradation level ($V_{ds} = V_{gs} = -5 \text{ V}$).

a) Resistance to Short Channel Effects

The unstressed threshold voltage roll-off dependence on the gate oxide thickness (section3-2-1) was explained by the difference in channel charge control by the gate terminal. The very clear superiority of devices with thin gate oxide in controlling the short channel problems with reduced channel length can explain the observed higher resistance to hot-carrier-induced degradation since a given effective channel length reduction will result in less short channel degradation.

b) Detrapping of electrons

It was reported that detrapping of electrons contributed to lowering the level of degradation of pMOSFETs [41]. It was also reported that thin gate oxide made detrapping easier than thicker gate oxide which would explain the lower degradation level of devices with thin gate oxides. To find out if electron detrapping could have influenced the different degradation levels between thin and thick gate oxide, devices were stressed for 100 s at $V_{ds}=-6$ V followed by detrapping for 100 s at $V_{ds}=0$ V and $V_{gs}=-6$ V at room temperature. Not significant detrapping appeared for channel lengths longer than $0.4\text{ }\mu\text{m}$ and for shorter channel lengths no correlation was found between detrapping level and gate oxide thickness. Therefore, detrapping cannot have influenced the degradation level under the conditions of this experiment.

c) Degradation dynamics

The time dependance of the degradation, observed in the form of the saturation current shift, was found to depend on the gate oxide thickness (Figure 36). We see that for all channel lengths, the degradation level of I_{sat} in the first 10 s is higher for $t_{ox}=9$ nm than for $t_{ox}=18$ nm. As the stress time increases the trend inverts and after 10^4 s all devices with thick t_{ox} were more degraded than the ones with thin gate oxide. The same observations were made on the threshold voltage shift by Hiroki et al on buried channel pMOSFETs [42]. The initially higher degradation level for the 9 nm devices can be explained by the higher channel electric field of the device with the thinnest gate oxide. However, after some time the degradation level becomes higher for the 18 nm device than for the 9 nm

device. It was shown by Hiroki et al that the peak electric field location is shifted toward the source due to the increase of negative charges in the gate oxide and that the thicker the gate oxide, the more important the shift of the peak electric field location. In other words, the saturation effect discuss in section 4-2-4 does not occur as fast for the 18 nm device because of the shift in the peak electric field

FIGURE 36. Time dependence of the saturation current increase, for two different gate oxide thicknesses ($V_{ds} = V_{gs} = -5$ V)

4- 4- 2- Threshold Voltage Adjust Implant Dependence

The relative degradation of devices with the three different types of threshold voltage implant was studied. Figure 37 shows the shift of the threshold voltage (in reverse operation) after 100 s of stress at -6 V on the drain, with 18 nm of gate oxide and effective channel lengths between 0.3 μm and 0.7 μm . It appears that devices with the very shallow threshold implant degrade the most and devices with the deepest threshold implant degrade the least. The same trend was observed in the saturation current, and the linear

transconductance at both 18 nm and 9 nm of gate oxide thickness. A number of models were considered to explain the difference in the degradation level: short channel control, location of the charge injection and amount of interface states creation. These are discussed below.

FIGURE 37. Influence of threshold voltage adjust implant on the level of stressed-induced threshold voltage shift

a) Short channel control

The degradation of all three types of devices is dominated by the trapping of electrons in the gate dielectric at the drain end of the channel. The consequence is a reduction of the effective channel length of the device leading to the degradation of the characteristics due to short channel effects. In section 3-2-1 we looked at the relative short channel control of the pMOSFETs depending on their threshold voltage adjust implant profiles. The threshold voltage roll-off did not show a clear superiority of one type of device over the other ones. The subthreshold slope at -3.3 V indicated that the pMOSFETs with the

highest threshold voltage and an intermediate arsenic implant depth (“medium- V_{th} ”) had the structure the most resistant to short channel effects and the “shallow- V_{th} ” the least. Due to the nature of the degradation one would expect that, assuming a similar amount of charges injected into the transistor dielectric, the structure the most resistant to short channel effects would suffer least from the shift of its electrical characteristics. The short channel behavior could contribute to the higher level of degradation of the “shallow- V_{th} ” compare to the other devices but cannot account for the higher degradation level of the “medium- V_{th} ” type of devices compared to the “deep- V_{th} ” type of devices.

b) LDD diffusion shape

The shape of the LDD diffusion at the surface of the channel could also have an impact on the level of the degradation. Figure 38 shows the LDD diffusion at the drain end for both type of devices in the saturation mode of operation. Due to the doping level difference at the surface, the LDD lateral diffusion under the gate at the surface of the channel of the “deep- V_{th} ” devices is 40 nm greater than for the “shallow- V_{th} ” devices. The type of threshold voltage adjust implant influences the overlap of the gate oxide on the LDD diffusion at the surface. It has been shown for nMOSFETs that a wider overlap of the gate dielectric on the LDD diffusion lead to structures more resistant to hot-carrier degradation [49][50]. Assuming that the hot-electrons are injected in the same region of the gate dielectric, the pMOSFETs with less gate to LDD overlap will have a higher proportion of electrons trapped above the channel than the transistors with more overlap that will have higher proportion of electrons trapped above the drain. The larger overlap for the “deep- V_{th} ” than for the “shallow- V_{th} ” devices (40 nm more) allows a larger number of channel charges to be trapped above the drain diffusion rather than above the channel, which could contribute to the lower degradation level. MEDICI simulations of the linear characteristics of “deep- V_{th} ” and “shallow- V_{th} ” pMOSFETs with and without localized negative charges in the gate oxide were made. A uniform level of 10^{18} cm^{-3} of negative charges were introduced in the lowest 10 nm of the gate oxide (10^{12} cm^{-2} [22]) at the source end (the experimental measurements were made with the source and drain interchanged after stress). The charges were located over $0.1 \mu\text{m}$ of the channel centered $0.07 \mu\text{m}$ away from the gate edge for both type of devices which corresponds to 65% of the charges being trapped

above the channel for “shallow- V_{th} ” pMOSFETs against only 25% of them for the “deep- V_{th} ” transistors and 48% for the “medium- V_{th} ”. The simulations showed that the threshold voltage was shifted by 14 mV (1.25% of its initial value) for the “shallow- V_{th} ” devices and by only 2.7 mV (0.3% of the initial value) for the “deep- V_{th} ” and an intermediate 5 mV (0.5%) for the “medium- V_{th} ” devices. It is interesting to observe that this trend in the threshold voltage shift corresponds to the experimental one, which short channel behavior could not fully explain.

FIGURE 38. Comparison of the lateral Ldd diffusion in the channel for three different types of devices.

c) Interface states generation

The last point to be made is related to the creation of interface states. No direct comparison of the level of interface states generated could be done because the high level of electrons trapped would screen their impact on the device characteristics, and only a charge pumping technique would give reliable quantification of the level of interface states being created. At maximum gate current the ratio of the substrate to drain current is higher for “medium- V_{th} ” and “deep- V_{th} ” devices which is indicative of a higher channel electric field for these devices than for the “shallow- V_{th} ” devices. More interface states might therefore be generated and compensate for the trapped electrons for the “medium- V_{th} ” and “deep- V_{th} ” than for the shallow- V_{th} ” devices.

The resistance to short channel effects cannot explain in itself the difference in degradation level of the different types of devices. The variations in gate to LDD overlap from one structure to another was found to be best candidate to explain the relative degradation level; a different proportion of charges would be trapped above the channel and the drain leading to more or less stress-induced characteristic shift. Though, the effect of partial compensation of negative trapped charges by positively charged donor interface states could not be excluded.

CHAPTER 5

CONCLUSION

P-channel MOSFETs with effective channel lengths as short as $0.3\text{ }\mu\text{m}$ showing good control of short channel effects have been designed and fabricated and the mechanisms of degradation due to hot-carrier induced degradation studied. Key features in the design included the use of a surface conduction path structure and the reduction of the LDD junction depth by a phosphorus halo implant. The effects of gate oxide thickness and threshold adjust profile on device performances were also examined.

A major concern in developing the process used to fabricate the devices was obtaining a high, uniform doping level in the gate polysilicon, without allowing boron to penetrate the thin gate oxide and enter the underlying channel. These both goals were successfully achieved as demonstrated by the lack of polysilicon depletion effects in C-V curves up to -5 V gate bias, and by the absence of flat-band voltage shifts. However, a relatively high density of interface states was found in all devices, and this might have been related to boron channeling through the gate polysilicon.

The resistance to short channel effects was found to clearly improve with gate oxide thickness reduction, as did transconductance and current sourcing. Relatively little difference in transconductance and current sourcing was found between devices with deep and shallow threshold voltage implants after allowance was made for variations in threshold voltage. What differences were observed could be explained in terms of increased coulomb scattering due to high doping levels in the channels of devices with shallow V_t adjust implants and may be related to the presence of surface states. The subthreshold slope measured to characterize the resistance to short channel effects for the various structures showed that for surface pMOSFETs a threshold voltage implant as close as possible to the surface might not be the best answer to short channel effect control. The shallow threshold voltage implant did give the lowest subthreshold slope for long channel lengths but failed to act as a punchthrough stopper for the shortest channel lengths leading to premature punchthrough as the channel length decreases compared to structures with more buried threshold voltage implants.

The study of hot-carrier-induced degradation showed that for the surface pMOS-FETs fabricated here, the degradation mechanisms involved both trapped electrons and creation of interface states (both mechanisms have been implicated with degradation in previous studies). Trapping of hot electrons in the gate dielectric during electrical stress results in a local enhancement of channel inversion. The resultant modification in device characteristics can then be described primarily by a reduction in effective channel length. This effect is well-known for buried p-channel devices. However, in contrast to buried pMOSFETs, hot electron trapping is not the only type of degradation taking place in the surface channel devices. Enhanced GIDL observed after stress at low gate to drain bias was explained by the generation of interface states. More direct evidence of these stress induced surface states was seen in the transconductance characteristics after detrapping of the electrons from the gate oxide. The maximum shift in the device characteristics corresponding to an effective channel length reduction due to trapped electrons was found for stressing biases corresponding to the maximum gate current. However, the OFF state current increase after stress was caused by generated interface state and was maximum at bias conditions corresponding to the peak substrate current where the carriers are the most energetic and therefore more likely to create interface states. The behavior of the linear transconductance illustrates the complexity of degradation mechanisms of surface pMOS-FETs. At low gate biases mobility reduction and effective channel reduction have opposing effects on the peak transconductance, while at high gate biases an enhanced resistive effect appears due to trapped electrons rather than hot-carrier generated interface states. To the best of our knowledge, detrapping of stress-induced electrons had never been used to understand the combined effect of trapped electrons and interface states on the linear transconductance degradation after voltage stress. Finally, both the gate oxide thickness and the threshold voltage implants were found to affect the degradation level. Thin gate oxide devices suffer from less degradation mainly due to their better short channel effect control. Short channel control could, however, not fully explain the degradation level dependence on the threshold adjust implant profiles. The gate-to-LDD overlap variations caused by the difference in channel surface doping could have allowed a different proportion of charges to be trapped above the drain or the channel depending on the type of threshold voltage implant used. No work had been done so far on studying the impact of

the threshold voltage adjust profile on the gate-to-LDD overlap and the resulting hot-carrier-induced degradation level. The devices with deepest threshold voltage implant had the lowest surface doping resulting in the greatest gate to LDD overlap. A higher proportion of hot electrons would therefore be trapped above the drain resulting in less degradation of their electrical characteristics. Over all, the most important factor influencing the resistance of a particular device design to hot-carrier induced degradation appears to be the ability to withstand the effect of trapped charges rather than differences in the amount of charge trapped.

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