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Differential Bipolar Stray-Insensitive Quasi-Passive Pipelined Digital-to-Analog Conversion

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the faculty of Graduate Studies and Research
acceptance of the thesis,

Differential Bipolar Stray-Insensitive Quasi-Passive Pipelined Digital-to-Analog Conversion

submitted by
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in partial fulfillment of the requirements
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February 15, 2001

Abstract

Algorithmic Digital-to-Analog Converters (DACs) can offer small and low-power alternatives to other types of DACs for various applications. Despite these main advantages, the traditional designs for these converters are not competitive in terms of linearity, especially at high speed. This work is a thorough study of quasi-passive algorithmic digital-to-analog converters. The existing architectures for these converters are investigated, and the sensitivities that limit their performance are highlighted. Following the review, new concepts in the cyclic DACs are presented. Proposed improvements to the cyclic DAC include the differential bipolar architecture, better sample-and-hold, and digital calibration. Differential bipolar design increases the linearity by one bit and removes the largest nonlinearity from the midrange point. The new digital calibration scheme reduces the effect of capacitor mismatch very efficiently. Subsequently, a stray insensitive quasi-passive pipelined DAC is introduced which greatly boosts the linearity of the converter at high speeds. The novel pipelined DAC architecture is then enhanced with some of the same upgrades applied to the cyclic DAC. Additionally, through the use of multiplexed capacitors in the last stage of the pipelined DAC, the conversion speed can be more than doubled. Experimental findings on the implemented test chips support analytical and simulation results, and prove that the new algorithmic DACs can deliver comparable or better performance at lower power consumption compared to the current-steering DACs.

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List of Abbreviations and Symbols

A/D	Analog-to-digital
AC	Alternating current
ADC	Analog-to-digital converter
α	Transfer-phase duty-cycle
ATE	Automatic test equipment
B_{lp}	Loop bandwidth (rad/s)
BOC	Bank of cyclics
CCA	Complete conversion averaging
CDAC	Cyclic digital-to-analog converter
CMFB	Common-mode feedback
CMRR	Common-mode rejection ratio
CPU	Central processing unit
CT	Continuous time
CTRCF	Continuous-time reconstruction filter
D/A	Digital-to-analog
DAC	Digital-to-analog converter
dBFS	Decibell full-scale
dBr	Decibell to reference
DC	Direct current
DEM	Dynamic element matching

DMT	Discrete multitone
<i>DNL</i>	Differential nonlinearity
DSL	Digital subscriber loop
DSP	Digital signal processing
DT	Discrete time
DUT	Device under test
<i>ENOB</i>	Effective number of bits
EOI	End or identify
$\mathcal{F}\{\cdot\}$	Fourier transform
FIR	Finite impulse response
FISH	FPGA interface for signal handling
FPGA	Field programmable gate array
<i>FS</i>	Full scale
f_s	Sampling frequency
GPIB	General purpose interface bus
GaAs	Gallium Arsenide
IIR	Infinite impulse response
<i>IM3</i>	Third-order intermodulation
<i>IM5</i>	Fifth-order intermodulation
<i>IMD</i>	Intermodulation distortion
<i>INL</i>	Integral nonlinearity
kSps	Kilo samples-per-second
LED	Light emitting diode
<i>LOR</i>	Loss of range
LPF	Low-pass filter
LSB	Least significant bit
MSB	Most significant bit
MSBF	Most-significant-bit first

MSE	Mean square error
MSps	Mega samples-per-second
MTPC	Metal to polycide
<i>MTPR</i>	Multitone power ratio
<i>NBW</i>	Noise-equivalent bandwidth
OSR	Oversampling ratio
PCB	Printed circuit board
PDAC	Pipelined DAC
PLC	Power line cycle
PLL	Phase-locked loop
PTP	Polysilicon to polysilicon
QAM	Quadrature amplitude modulation
QP	Quasi-passive
QPMDTC	Quasi-passive minimum <i>DNL</i> ternary code
$\mathcal{R}$	Conversion rate
RCF	Reconstruction filter
ROM	Read-only memory
$\mathcal{S}$	Number of samples in a test signal
S/H	Sample-and-hold
<i>SFDR</i>	Spurious-free dynamic range
SC	Switched capacitor
SD	Standard deviation
SI	Switched current
Si	Silicon
SiGe	Silicon Germanium
$\Sigma\Delta$	Sigma-delta
$\Sigma\Delta\text{M}$	Sigma-delta modulator
<i>SNDR</i>	Signal to noise-and-distortion ratio

SNR	Signal to noise ratio
Sps	Samples-per-second
$\mathcal{T}$	Settling time
T	Conversion period
THD	Total harmonic distortion
Θ	kT , k is Boltzman constant and T is absolute temperature (here)
VLSI	Very large scale integration
Ω	Continuous-time angular frequency
ω	Discrete-time angular frequency
WILBW	Within loop bandwidth
WOLBW	Without (outside) loop bandwidth

Chapter 1

Introduction

Recent progress in the implementation of complex digital circuits with high operating speed and low power consumption has dramatically increased their application. However, most input devices (sensors), transmission media (twisted pair or coaxial cable, electromagnetic wave, etc.), and output devices (actuators, speakers, video displays, etc.) are analog. Inevitably, a means of converting analog signals to digital and vice versa is required to interface the real world signals and controls to the digital processors.

1.1 Motivation

With ever-increasing speed of digital integrated circuits, comes the urge for increased speed in the analog-to-digital (ADC) and digital-to-analog (DAC) converters. On the other hand, increased performance of digital processors demands higher accuracy (resolution, and linearity) from ADCs and DACs.

More and more electronic products are battery operated and/or miniaturized with high integration density. Battery consumption and heat generation in electronic circuits are major concerns in these cases. For these applications, reduction of power dissipation is the most important goal.

Popularity of electronic merchandise is inversely proportional to their cost, and usually the cost is inversely proportional to the integration level. The latter fact results from the significant price difference between chip-level and board-level manufacturing. Often the cost of packaging silicon chips and board-level assembly exceeds the price of the fabricated silicon itself. As well, highly integrated circuits tend to dissipate less power, and run faster as a result of fewer interface pins and their associated loading. For these reasons, it has become very attractive to integrate data conversion circuits along with the digital circuitry on the same die. Chip area taken by circuits is another major price factor, especially considering that yield drops rapidly as the circuits become larger. This factor is particularly important for highly integrated designs, where many circuit blocks are implemented on the same die.

Conversion speed of the interface circuits is dependent on the fabrication technology, and the architecture. Minimum geometries of the process and its material (e.g. Si, SiGe, or GaAs) determine the technology factor. While, within the same architecture it is possible to improve the speed by using a faster process, the cost difference may be prohibitive. Therefore, it is highly desirable to find architectures that can deliver the required speed with less demand from the technology. Similarly, it is also advantageous to discover DAC architectures that offer the needed linearity (resolution) with relaxed specifications for the fabrication process.

The above issues are some of the key challenges in the field of converter design. It is the intent of this work to find a low-power cost-effective solution to the demand for high-linearity high-speed D/A converters. Algorithmic digital-to-analog converters, despite their good potential as a solution to a broad range of applications, have not been fully developed. Promoting these converters to a practical level through a series of improvements is the goal of this study.

1.2 Digital-to-Analog Conversion System

A general block diagram of a digital-to-analog conversion system is shown in Fig. 1.1. Not all the blocks are explicitly needed for any particular system, but most of the functionality must exist in the path. Some other definitions, may combine some of the shown blocks into one.

Figure 1.1: General block diagram of a DAC system.

DAC Core

The digital input is a discrete-time (DT) and discrete amplitude (digitized) signal. The signal may have been created entirely in a digital system (such as synthesized music) or might have originally come from an analog source (e.g. telephony signals). Regardless of the source, the signal at this point is band-limited to $-\frac{f_s}{2}$ to $\frac{f_s}{2}$ (f_s is the sample rate), with its replicas centred at $\pm n f_s$. The DAC core by itself has the responsibility of converting each digital input sample to a corresponding analog sample.¹ The analog output of the DAC core is still in discrete-time form, in the sense that it is valid (with sufficient accuracy) at a specific time in the sample period (usually the end).

DT LPF

Depending on the DAC architecture, the immediate output of the DAC may have large high-frequency noise (around $\frac{f_s}{2}$) which has to be attenuated before reaching the output of the system. The DT Low-Pass Filter (LPF) provides this function.

¹In case of noise-shaping converters, some correlation between the samples is created in the DAC core (including the modulator) as the samples leave it.

If a DAC does not generate large out-of-band noise, the DT LPF block may not be necessary. Another application of this block is as an augmentation of the digital interpolation function, as will be explained shortly.

DT-to-CT Converter

Conversion from DT to Continuous-Time (CT) usually has to be performed in a separate circuit than the DAC and the DT LPF. The requirement for CT linearity is much more stringent than the DT one, because for a CT signal, the signal value is important at all times, not just at the end of a sample period. Fast transitions at the output exacerbate CT nonlinearity caused by factors such as limited slew-rate. A sufficient, but not necessary, condition for the CT linearity is to have an output which is linearly proportional to the DT input during the entire period. For example, if for a digital input of 0.5, the output at the midpoint of the period is 1 V, for a digital input of 0.25, at the same time point it has to be 0.5 V to satisfy this condition. For a general DAC, or DT LPF, meeting this condition with sufficient accuracy is usually very difficult. If the DT linearity is acceptable, but CT linearity is not maintained, the DAC's AC performance degrades sharply with increasing signal frequency (bandwidth). The usual circuit for a DT-to-CT converter is a highly linearized Sample-and-Hold (S/H).

CTRCF

Finally, a CT Reconstruction Filter (CTRCF) is commonly employed to recondition the signal before delivering it to the output in order to attenuate the images. The images have already been somewhat reduced by the DT-to-CT converter (at least by a first order sinc function), but it may not be sufficient to pass the out-of-band noise specifications for the system. In the time domain, the function of this filter is seen as smoothing the sharp edges of the steps in the output signal to make it better resemble

the intended low-pass signal.

In order to assist the CTRCF in its function, the digital input may be oversampled. With no oversampling, the CTRCF has to have a very sharp and accurate transition from the pass-band to the stop-band to attenuate the images effectively. However, with some degree of oversampling in the digital input signal, there will be a larger transition band to accommodate lower order filters (less power dissipation) and higher tolerance for component variations (especially if implemented on-chip) for the CTRCF. The oversampling in the digital domain is done by interpolation filters, which cannot be ideal either. This means that some residual images are going to be left over by the digital interpolator, which may have to be further minimized by analog filters. This function is more suited to the DT LPF, which tends to have a more precise frequency response (usually based on same component type ratios) compared to the (integrated) CTRCF. This allows for compensation of the baseband droop of the digital signal processor which is another use for the DT LPF block in the system.

1.3 DAC Performance

There are various criteria for assessing the performance of a D/A conversion system. Depending on the application, some criteria are more important than the others [3, Chapter 7]. A review of these metrics is presented in Appendix A. Here, only the important criteria for signal processing applications are reviewed.

Speed

Speed of conversion is mainly expressed in two parameters: rate, and latency.² Conversion rate is the number of samples processed per unit time (usually indicated in samples-per-second or Sps units). Latency is specified as the amount of time that

²Settling time, which is more important for video DACs, does not directly matter in signal processing applications such as audio, and communications

the converter takes to completely process one input sample from the beginning to the end, in other words, input-output delay. For many conversion methods (e.g. current steering DACs), latency is less than or equal to the inverse of the conversion rate, i.e. the samples appear at the output at most one conversion cycle later.

Some data converters have longer delays than $\frac{1}{\text{rate}}$. This is due to the fact that the input data has to be processed in more than one stage in the converter, and different stages can work on different output samples at the same time. One example of this type is the pipelined converter. A pipelined architecture is made of (functionally) similar stages, each one partially processing the data and passing an intermediate value for further steps in the succeeding stages. Since the signal has to pass many stages for a complete conversion, total delay equals the number of stages times the delay of each stage, whereas, the conversion rate is just the inverse of one stage delay. The increased conversion delay of a pipelined converter is not a concern in most applications, such as video processing and communications, while the scheme may take advantage of savings in hardware and power compared to other approaches.

The internal mechanisms of some DACs may require higher clock frequency, and/or multiphase clocks which may impose limitations on some systems. However, there are factors that can mitigate such situations. First, clock frequencies higher than the sampling rate usually exist in the digital part of the system and can be passed on to the DAC. Secondly, the clock frequency can be multiplied to reach the required value in circuits such as a Phase-Locked Loop (PLL). A simpler technique, with little impact on jitter, is also proposed in this thesis that can increase the clock rate by a limited factor.

To facilitate the (re)construction of the analog signal from the digital one (i.e. image rejection by the CTRCF), it is common to oversample, and interpolate the original digital signal before entering the DAC. An Oversampling Ratio (OSR) of 4 to 8 is a practical choice. In this case, the sampling frequency (f_s) should be 8 to 16

times higher than the signal bandwidth (low-pass assumed). Higher OSR increases power dissipation, so excessive increase in OSR should be avoided as much as possible, unless it is needed to reduce the steps at the output to improve the CT linearity of the DAC (especially if no DT-to-CT stage is used).

DC Linearity and Resolution

Among the DC performance factors, linearity is typically the most important. Usually 1% or more gain error and offset may be tolerated, but the linearity has to be well below 0.1%.

Linearity specified in the form of Differential and Integral Nonlinearity (*DNL* and *INL*) is the most important measure of converter accuracy. High *INL* is one indication of high distortion in the output signal. Distortion may appear as harmonics (or intermodulation) of the input signal, or may appear as a spur with no obvious frequency relationship to the signal.

A confusing terminology in the specifications of a DAC is resolution. Resolution strictly means the number of digital input bits that the converter can process, but it is usually mistaken for its linearity. A *true* N -bit resolution DAC, in a common definition, is the one with its *INL* and *DNL* below 0.5 LSB to N bits.³ There are good reasons for having the *implemented* (or *strict*) resolution of a converter higher than its true one. Higher resolution reduces the quantization noise that enters the DAC system, and as a result, improves the Signal-to-Noise Ratio (SNR) at the output. Carrying up to 2 extra bits on top of the true resolution is recommended for this reason.

³Another common terminology is Effective Number Of Bits (*ENOB*), defined as

$$ENOB = \frac{SNDR - 1.76}{6.02}, \quad (1.1)$$

where *SNDR* is the Signal-to-Noise and Distortion Ratio. *ENOB* may be non-integer.

To avoid any confusion, throughout this thesis only the strict definition of resolution is used. Whenever needed, the *linearity* is expressed in terms of bits based on the *true* definition, e.g. a 10-bit linearity means *INL* and *DNL* of less than half of the Full-Scale (*FS*) divided by 1023.

AC Linearity

The quality of the DAC output for a given application can be tested by passing actual signals through the system. However, analysis of these output signals may be too difficult, or sufficient insight may not be obtained from them, hence simplified test signals are quite common. The simplified signals include single tone, two tones, and multitone. The usual metrics for AC performance include Total Harmonic Distortion (*THD*), Intermodulation Distortion (*IMD*), Multitone Power Ratio (*MTPR*), and Spurious-Free Dynamic Range (*SFDR*).

Although DC nonlinearity is the major limitation in the AC performance of the DAC, separate study of the AC characteristics of DACs is still important. At low frequencies, the AC performance is very closely linked to the DC linearity. Depending on the shape of the *INL* versus code plot, *THD* in the order of $-6 \times N$ dB may come out of an *N*-bit *linear* DAC at very low frequencies.

At high signal frequency, DAC outputs exhibit CT linearity limitations in addition to their DC nonlinearity. This behaviour is a direct consequence of poor transient linearity. The exact cause of this impairment is implementation dependent, for example, it may be limited slew rate at the opamp outputs of a voltage DAC, or glitches in a current steering DAC.

1.4 High-Speed High-Linearity DAC Architectures

For the signal bandwidths in the range of 1 MHz, only a few DAC architectures can deliver higher than 80 dB of *SFDR*. In order to achieve such linearity, usually, 12-bit DC linearity or higher is required. It is also very challenging to maintain the CT linearity at that signal bandwidth.

Current steering (Nyquist rate) DACs are by far the fastest D/A converters in terms of conversion rate. When it comes to linearity at high frequency, however, they suffer from transient nonlinearity. For example, *SFDR* for a 14-bit 125 MSps DAC drops from better than 80 dB at 1 MHz signal frequency to about 60 dB at 25 MHz [4]. Therefore, although the conversion rate capability of the DAC is significantly higher than the range of algorithmic DACs in today's technologies, the speed is apparently needed to deliver comparable signal bandwidth.⁴ Other techniques that try to mask the nonlinear transient by using a return-to-zero waveform, create very strong signal images at nf_s that are hard to remove. These converters are sensitive to clock jitter,⁵ and dissipate large amount of power [6, 7].

Oversampling (noise-shaping, or $\Sigma\Delta$) modulator DACs can be either single-bit or multibit. Single-bit modulators have excessive in-band quantization noise with OSR of only 8 (16 MSps for 1 MHz bandwidth).⁶ Even with 4 bits of resolution in noise-shaping DACs, and a fourth-order modulator, it is hard to obtain near 72 dB of *SNR* for the modulator alone at such low oversampling ratios. Multibit modulators also need some dynamic element matching mechanism to avoid detrimental effect

⁴A slower member of the same family cannot deliver better than 73 dB *SFDR* at 1 MHz [5].

⁵Clock jitter modulates the pulse width in these converters (rather than the signal derivative). For example, 50 ps of jitter in a 50% duty-cycle RZ DAC running at 10 MSps causes noise at -60 dBc.

⁶In a study of a 5 V CMOS process (i.e. 0.6- μ m feature size) over the -40°C to $+100^\circ\text{C}$ temperature range, it is found that 20 MSps is practically the maximum clock frequency feasible for switched-capacitor filters with 80 dB linearity.

of element mismatch in their DACs [8]. It is also necessary to use high-order DT filtering to attenuate the out-of-band noise created by these DACs. To deliver high linearity and low-noise performance at high speeds, these switched-capacitor LPFs usually consume a great deal of power.

Algorithmic DACs process the digital input bit-by-bit and combine the results in a procedure which results in a corresponding analog output. The algorithm can be implemented in a cyclic or pipelined structure. The circuit implementation requires some kind of analog memory for storage of intermediate results, so it can use Switched-Capacitor (SC) or switched-current (SI) techniques.

Algorithmic DACs are often mistakenly assumed to be slow. In the cyclic converter, one stage has to process all the digital input bits, one bit per clock cycle, and additionally have a few clock cycles to transfer the charge to a sample-and-hold. This misconception about speed is also supported by the fact that the best cyclic DACs reported to date could not even reach the 1 MSps mark with an 8-bit linearity [9]. However, as will be proven in this thesis, good linearity (better than 13 bits with digital calibration) at speeds higher than 4 MSps can be achieved with cyclic DACs in today's technologies.

The faster versions of the algorithmic DACs (i.e. the pipelined DACs) are more suited for high speed operation. The traditional design, for high linearity, needs an opamp in each pipelined stage, and needs to perform two integrations in each cycle. Therefore, the conversion rate can reach $\frac{1}{2T}$, where T is the settling time for one integration. That allows the pipelined DACs to exceed 25 MSps in rate.

1.5 Quasi-Passive Algorithmic DACs

Quasi-Passive (QP) algorithmic DACs are switched-capacitor algorithmic DACs that do not use amplifiers in the conversion process. In other words, the digital-to-analog

Figure 1.2: Simplified diagram of a quasi-passive cyclic DAC.

conversion is performed entirely by switches and capacitors.

A simplified view of a QP cyclic DAC is shown in Fig. 1.2. The D/A conversion process will be explained in details in Chapter 2, here it is briefly mentioned that the conversion is accomplished entirely in the left-hand switch and capacitor section (the *core*), one bit per clock cycle. At the end of the conversion process, the result is transferred to the S/H, which includes an opamp.

Since the core of the converter consists only of switches and capacitors, settling of the transients is very fast. The S/H transfer phase needs to be longer than the conversion clock phase to accommodate the limited bandwidth of the opamp inside. For example, the conversion may take 12 clock cycles (for 12 bits) and for the next 4 clock cycles (8 clock phases) the charge can be transferred to the S/H, for a total of 16 clock cycles for a full conversion period.

QP algorithmic DACs have three main advantages. First, they are faster than other types that use the opamp inside the loop. In the above example, the opamp can settle 8 times slower than the switches and capacitors. Such a large ratio is not usually necessary from the opamp speed standpoint (opamps are usually only 3 to 4 times slower in settling), but it helps to keep this ratio large in order to save power in the opamp, and this potential for power saving is the second advantage of these DACs. Finally, the QP algorithmic DACs can be less noisy, due to lack of sampled opamp noise in the conversion process. If, for a special application, the output of the DAC has to be delivered to a SC filter (such as DT LPF in Fig. 1.1), the S/H can

be entirely eliminated. In this case, the power dissipation in the core remains as the only analog power consumption, which would be very small.

SC algorithmic DACs, in general, have the potential for the best linearity among all kinds of uncalibrated DACs that rely on matching. That is because matching between capacitors is usually much better than any other integrated element [10, 11, 12]. In both cyclic and pipelined SC DACs, all capacitors are equal (unlike some other architectures with nonunity capacitor ratios), and can therefore take advantage of the best element matching available in integrated circuits.

Despite close to a quarter century history behind the algorithmic DACs [13], these converters have not reached the performance level that can compete with other types of DACs, especially the current steering one. The current implementations lag far behind in terms of conversion rate, signal bandwidth, and linearity. It is the objective of this work to apply enough improvements to the algorithmic architectures to help them favorably compete with other architectures.

1.6 Applications of Algorithmic DACs

Algorithmic DACs can have a variety of applications depending on their speed and linearity level.

For very low signal bandwidth applications (such as audio) the noise shaping modulators are usually more suitable. This is because it is possible to use a high oversampling ratio to suppress baseband noise and allow for large transition bands and simple LPFs.

For very high speed signals (bandwidth greater than 5 MHz, and conversion rate greater than 40 MSps), current steering DACs have the commanding lead. Spending enough current in these DACs can usually deliver the required speed and linearity, although at high frequencies the linearity predictably drops.

In the middle of the speed range, algorithmic DACs can have the right performance coverage. In today's technologies, cyclic DACs can have conversion rates beyond 5 MSps, and pipelined versions can reach 50 MSps. In terms of linearity, these DACs enjoy the best uncalibrated matching accuracy available, and simple digital calibration scheme proposed in this work can further improve that.

Some typical applications for the algorithmic DACs are Digital Subscriber Loop (DSL) transmitters, baseband signal generation for wide-band modulators in communication systems, ultrasound (array) transducer drive, arbitrary waveform generators, and test equipment. A highly suitable use for the cyclic DAC can be the G.lite DSL standard with a signal bandwidth of 552 kHz [14], and for the pipelined DAC the wider band G.dmt with signal frequencies up to 1.104 MHz [15]. The linearity requirement in terms of *MTPR* is in the order of 70 to 80 dB.

1.7 Contributions of This Thesis

The following is a summary of the contributions made in this work in the field of algorithmic D/A conversion, in order of importance.

A new architecture for QP pipelined DAC is proposed to make it stray insensitive, and thereby greatly improve its linearity for high speed operation. Since the stray insensitivity is realized without the use of an opamp in each stage, substantial savings in power dissipation and noise is achieved.

A novel differential bipolar architecture improves the linearity of the original cyclic DAC, and the new pipelined DAC, by one bit. The bipolar technique refers to the use of symmetrical positive and negative references in a sign-magnitude conversion. The new converters have their largest differential and integral nonlinearities situated at the 1/4 and 3/4 range points, and their best performance in the middle of the range. This property by itself is also a significant advantage.

The pipelined DAC is further improved by an additional last stage and multiplexing, which can more than double the conversion speed relative to traditional designs.

A simple digital calibration scheme for reduction of nonlinearity caused by capacitor mismatch is introduced. This scheme is more efficient than previously used methods for algorithmic DACs.

A symmetrical structure is proposed for the cyclic DAC to make digital calibration easier and more efficient, and to take advantage of the parasitic drain-to-source capacitance in a MOS switch. This improves the linearity of the cyclic DAC by as much as an extra bit. Also, by including both capacitors of the cyclic DAC core in charge transfer to the first S/H, the thermal noise power from the core, relative to the signal, is 3 dB lower.

A second S/H circuit is added to the DACs as a DT-to-CT converter to help improve CT linearity. Both S/H stages are thoroughly analyzed for noise. Frequency response of the second S/H with its incomplete settling is also derived.

All of the above ideas have been used in the implementations presented in this thesis, whereas an intermediate architecture between the cyclic and the pipelined DACs, called bank-of-cyclics, remains as a proposal.

A clock multiplier circuit capable of producing accurate duty-cycle waveforms is proposed that can create multi-phase clocks for algorithmic DACs without increasing jitter noticeably.

Application of a first-order $\Sigma\Delta$ modulator in measuring on-chip capacitor ratios provides a very accurate and simple method of evaluating capacitor mismatch.

1.8 Thesis Outline

The thesis organization is as follows. First, a review of the basic algorithmic D/A converters is presented in Chapter 2. The improvements made to the original architec-

tures by others are explained in Chapter 3. Proposed enhancements to the cyclic and the pipelined DACs appear in Chapters 4 and 5 respectively. Some of the side issues, such as the S/H and multiphase clock generation are also covered in these chapters. Implementation methodology for the experiments on the cyclic and pipelined DACs is provided in Chapter 6. The experimental results are reported in Chapter 7, and a conclusion is presented in Chapter 8.

The appendices provide more details on a range of issues related to the main text. Appendix A contains the definitions for the specifications of a D/A converter as applied throughout this thesis. The frequency response and noise analysis of various S/H architectures are derived in Appendices B and C respectively. A simple method for measuring capacitor mismatch is the topic of Appendix D. Finally, Appendix E is a description of the custom FPGA interface that was built to test the implemented DACs.

Chapter 2

Principles of Switched-Capacitor Algorithmic Digital-to-Analog Conversion

Algorithmic D/A conversion is based on a simple step-by-step process. In each step a partial result from the previous step is combined with another part of the multi-bit input word and then passed on to the next step. The scheme is attractive because of savings it offers in terms of circuit size and power.

The cyclic DAC, which is the most economical one, reuses the same hardware in all conversion steps, with the drawback of lower conversion rate. The pipelined architecture increases speed at the expense of larger size. Because of the similarities between these two D/A converter types, the principles of their operation are included in the same chapter.

In this chapter, the conversion algorithm and the simplest implementations are discussed first. Then, the practical limitations of these original ideas are presented to pave the way for the improvements detailed in the following chapters.

2.1 Basic Architecture of Cyclic DAC

The conversion algorithm is common between the cyclic and the pipelined DACs, which is first explained using a flow chart. Next, a specific implementation of the cyclic DAC and its power consumption are analyzed.

2.1.1 The Algorithm

The algorithm for digital-to-analog conversion is the repetitive process shown in Fig. 2.1. The N -bit digital input word is expressed as $b_{N-1}b_{N-2}\cdots b_1b_0$, where each b_n can be 0 or 1. R holds the partial result throughout the conversion, and at the end it will be the analog representation of the digital input. At the initialization phase for each input, R and the bit-counter n are reset to zero. In the first iteration, R is set to the analog value $(b_0V_{\text{ref}})/2$. During the next iteration, $(b_1V_{\text{ref}})/2$ is added to the previous value of R divided by 2. This makes $R = b_1V_{\text{ref}}/2 + b_0V_{\text{ref}}/4$, in other words, R is the analog equivalent of the 2-bit number b_1b_0 . Continuing the process until $n = N$ results in

$$R = b_{N-1}V_{\text{ref}}2^{-1} + b_{N-2}V_{\text{ref}}2^{-2} + \cdots + b_1V_{\text{ref}}2^{-(N-1)} + b_0V_{\text{ref}}2^{-N}, \quad (2.1)$$

or equivalently the output voltage is

$$V_{\text{out}} = V_{\text{ref}} \sum_{n=0}^{N-1} b_n 2^{n-N}. \quad (2.2)$$

The above equation indicates that V_{out} is the analog representative of the digital input word $b_{N-1}b_{N-2}\cdots b_1b_0$. The scale factor V_{ref} is required here to emphasize that V_{out} is an analog value, and its role as a reference voltage will be better explained by the implementation.

Although it is quite possible to convert more than one bit of the input word in each iteration, it will not be considered in this work for two reasons. First of all,

Figure 2.1: Algorithmic D/A conversion flowchart.

multi-bit multi-step converters are usually called “recycling” and not “algorithmic.” However, the main reason for excluding recycling converters from this study is that in the case of pipelined D/A converters (which is the main focus here) they add to the complexity and do not offer any significant advantage.

2.1.2 Switched-Capacitor Cyclic DAC

Switched-capacitor (SC) technique refers to the use of MOSFET switches and capacitors in microelectronic circuits for implementation of various functions, such as filters, modulators, and A/D and D/A converters. The technique became popular mainly because of the accuracy it offers to the integrated filter design [16]. However, there are several other advantages to this technique that make it very suitable for converter design.

Performance of many converter architectures depends very much on the matching accuracy of the circuit elements used in their implementations. Quite often the

mismatch error very closely determines the linearity of the converter. It is known that the integrated circuit element that offers the best matching accuracy for the same area is the capacitor [10, 11, 12]. Therefore, capacitor-based multibit converter architectures can offer the best linearity in the absence of calibration.

Capacitors provide a means of storing analog quantities (as charge or voltage). This function is very useful in the design of some converters, as the process may take many steps before completion and storage of intermediate results is necessary.

Parasitic resistance of the metal interconnections affects the accuracy of the converters that rely on resistor or current source matching. This kind of parasitic is relatively difficult to control or simulate. SC circuits have little sensitivity to these parasitics, since with sufficient settling time, the final voltage on capacitors is independent of switch and metal track resistance.

Examples of switched-capacitor converter architectures are algorithmic converters. SC techniques have been used to implement cyclic D/A converters by using capacitors as storage elements, and MOS transistors as switches for transferring charge between the capacitors [13]. Appropriate digital signals control the switches to implement the algorithm.

The basic SC implementation of the cyclic DAC is illustrated in Fig. 2.2. The timing diagram indicates when each switch is on (closed) or off (open). As with any other SC circuit, the two phases of the control signals (ϕ_1 and ϕ_2) are non-overlapping, i.e. they are never both high at the same time. The switches may be NMOS or CMOS, but these details are not relevant to the operation principles of the circuit and are not considered in this section. Since the DAC consists of only switches and capacitors (no opamps used in the conversion process), this circuit is known as a “quasi-passive” (QP) cyclic DAC. Capacitors C_1 and C_2 are assumed equal, and a digital word of $1 \dots 101$ is used as an example input in the timing diagram.

The partial result R is the voltage across C_2 , which is reset by S_r to zero at the

Figure 2.2: Basic switched-capacitor implementation of the cyclic D/A converter. (a) Schematic. (b) Timing diagram.

beginning of each conversion cycle. In the first phase ϕ_1 of each bit-cycle (i.e. the clock cycle), C_1 is charged to V_{ref} or discharged to zero, by S_1 or S_2 respectively, depending on the value of the current bit b_n . Hence, at the end of ϕ_1 of the n th bit cycle, the voltage across C_1 equals $b_n V_{\text{ref}}$. The conversion starts with b_0 , which is the Least-Significant Bit (LSB), and ends with the Most Significant Bit (MSB), i.e. b_{N-1} . By combining the charges stored in C_1 and C_2 in the second phase using S_3 , and employing the principle of charge conversion in a closed Gaussian surface, we have

$$(C_1 + C_2)V_{C_2}[n] = C_2V_{C_2}[n-1] + C_1b_nV_{\text{ref}}. \quad (2.3)$$

Since $C_1 = C_2 = C$, equation $R = (R + b_n V_{\text{ref}})/2$ is realized. Therefore, at the end of

N th bit-cycle, V_{C_2} is the analog equivalent of the digital input as per V_{out} in Eq. 2.2. This voltage has to be sampled-and-held before S_r closes for the next conversion.

The very simple implementation of the cyclic D/A converter is its main advantage. The number of devices in the circuit is very small, which makes it very economical. The digital section, which provides the control signals to the switches, is also very simple and small. One apparent disadvantage of this converter compared with other designs, such as binary-weighted capacitor-arrays [17, pp. 473-474], is its low speed. At least N clock cycles are needed for an N -bit conversion. This, however, is not necessarily a real disadvantage, because as will be shown later, in practical cases the slowest part of the system is the sample-and-hold, and the improved cyclic converters explained in Chapter 3 may run almost as fast as other charge-redistribution types.

2.1.3 Power Consumption of SC Cyclic DAC

The consumed power of the converter has a few components. The analog-block consumers are the SC DAC core and the S/H section (capacitor charging current from V_{ref} — see Fig. 1.2). Additional power is consumed in the digital control block. Only the dissipation in the DAC core is analyzed here, the other two factors are more implementation specific and will be considered later.

The source of the input power to the cyclic DAC core of Fig. 2.2 is the reference voltage source. In each ϕ_1 phase where the bit value is 1, the source charges the C_1 capacitor for the voltage difference $V_{ref} - R$. Since the value of R from the previous cycle is code and cycle dependent and so is the value of b_n , the exact analysis is not trivial and is highly signal dependent. Through a simple estimation, however, an upper bound can be obtained for this component.

The lowest value of R is zero (assuming V_{ref} is positive). If we assume C_1 should be charged from this lowest value to V_{ref} in every bit-cycle, the amount of energy per

bit taken from V_{ref} is

$$E_{b \text{ max}} = V_{\text{ref}}^2 C, \quad (2.4)$$

where $C = C_1 = C_2$. The energy dissipation for an entire N -bit conversion cycle is then bounded by

$$E_{c \text{ max}} = NV_{\text{ref}}^2 C, \quad (2.5)$$

and the equivalent power dissipation for a conversion time of T is

$$P_{\text{max}} = \frac{1}{T} NV_{\text{ref}}^2 C. \quad (2.6)$$

For example, for $C = 1$ pF, $N = 10$ bits, $V_{\text{ref}} = 1$ V, and $T = 100$ ns (i.e. $f_{\text{clk}} = 10/T = 100$ MHz), $P_{\text{max}} = 100$ μ W.

Despite all the overestimates, power dissipation for a relatively high-speed DAC is fairly low. In the above calculations, the parasitic capacitance of the switches were ignored, but, as will be clear shortly, the above estimate is still virtually an upper bound. A closer upper limit for the power dissipation can be obtained from simulation. Fig. 2.3 displays the simulated normalized input energy to a 10-bit cyclic DAC. The power dissipation is at peak if the DAC is converting only one code for which the energy is maximum, i.e. 682. (Not surprisingly, the decimal code 682 corresponds to the binary code 1010101010.) This maximum normalized energy is approximately 3.78, and hence the associated power is $3.78V_{\text{ref}}^2 C/T$. Again for the above typical values, this results in only about 37.8 μ W. The average power dissipation for all codes is approximately 27.5 μ W. Further simulations show that this peak power grows no faster than the number of bits for higher resolution converters, for example, a similar DAC for 14-bit resolution dissipates only 51.1 μ W at peak (37.5 μ W average). In practice, this small power consumption will be dominated by the S/H power discussed later.

Figure 2.3: Normalized energy dissipation as a function of the input code for a 10-bit cyclic DAC.

2.2 Basic Architecture of Pipelined DAC

The operating principle for the pipelined DAC is the same as the cyclic one. The flowchart is essentially the same as in Fig. 2.1, and the difference is only in the implementation.

It is possible to use separate stages for realizing the $R = (b_n V_{\text{ref}} + R)/2$ operation instead of processing all bits of the digital input word in one stage. In this scheme, as shown in Fig. 2.4, the partial results are pipelined through the stages. This allows the use of the previous stage to operate on the next digital input word, hence, improving the throughput of the converter.

Each stage in the analog section of the pipelined converter consists of a single bit D/A (the multiply node), a divide-by-two summer, and an analog delay element D_a . The digital section is made of a series of shift registers progressively increasing in length from 0 to $N - 1$. Each D_a element could simply be a D-type flip-flop. The analog and digital parts of the converter are clocked from the same clock signal that

Figure 2.4: Block diagram of a pipelined DAC.

synchronizes the digital input.

From the above explanation, the operation of the circuit seems straightforward. It is worth mentioning that in this architecture a new converted data is delivered to the output every clock period T (the same as the delay through D_a and D_d), which is also the same as the input period. Nonetheless, the overall delay for each input sample is NT . This large delay may not be acceptable for some control systems that use the DAC in a feedback loop. For most other applications, however, this extra delay is not a problem. For example, the D/A converter in the DSL modems can have relatively long latency. Furthermore, some pipelined architectures (see Section 2.2.1) use variations of the general scheme to have overlapping operations and thereby reduce the overall conversion delay.

2.2.1 Quasi-Passive Switched-Capacitor Pipelined DAC

The original SC pipelined DAC uses an opamp in each analog stage [2, 18] to perform the required operations. While the use of opamps in the pipelined stages can have

The idea of designing an opampless (or quasi-passive as it is called) switched-capacitor pipelined DAC was introduced in [19] and later explored further in [20, 21]. This method allows realizing high-resolution SC D/A converters, which unlike the binary-weighted capacitor-arrays, use only one capacitor size ($C_{-1} = C_0 = \dots = C_{N-1} = C$), and thereby reduce the circuit size in integrated implementations. Since the pipelined DAC's conversion rate is essentially the same as binary-weighted arrays (both limited by the S/H speed), there is no speed penalty for the saving in the chip area.

The pipelined converter uses a three-phase clock for timing (in [20] three full cycles of an input clock are used instead). The clock phases run continuously (no reset cycle, etc. is needed), and a new digital input word is taken in every clock cycle. Since the

converter operates on $\lceil (N/3) \rceil$ words at the same time (N is the number of resolution bits, and $\lceil \cdot \rceil$ is the integer ceiling function), the digital bits should be distinguished using their sample number: $b_n[m]$ is the n th bit of the m th input word, where the $m - 1$ st word is one sample older than the m th, and so on.

The conversion process for each input begins with the LSB. Depending on the bit value, either $S_{0,1}$ or $S_{0,2}$ is closed during ϕ_1 to charge C_0 to $b_0[m]V_{\text{ref}}$. At the same time, C_{-1} is discharged to 0. In ϕ_2 of the same clock cycle, C_0 shares its charge with C_{-1} through $S_{0,3}$. Since all capacitors are equal, we have $V_{C_0} = (b_0[m]V_{\text{ref}})/2$. During the same ϕ_2 , C_1 is charged to $b_1[m]V_{\text{ref}}$ and is ready to share it with C_0 in the next phase. At the end of ϕ_3 , the voltage across C_1 is $\frac{1}{2}b_1[m]V_{\text{ref}} + \frac{1}{4}b_0[m]V_{\text{ref}}$. It can be shown that, when the charges associated with the input word m reach the output, the voltage across C_{N-1} will be

$$V_{C_{N-1}}[m] = V_{\text{ref}} \sum_{n=0}^{N-1} b_n[m] 2^{n-N}. \quad (2.7)$$

This converter operates on three bits of each input word in the same clock period by staggering their phases. Compared with the general diagram of Fig. 2.4, the overall data delay is reduced to $NT/3$. As a result, the size of the digital section of the converter is also reduced. It should be noted that three charge or discharge operations have to take place in each clock period. Fig. 2.6 shows the register file in the digital section of the QP pipelined DAC. A total of 22 D-type flip-flops are required for a 10 bit converter.

2.2.2 Power Consumption of QP SC Pipelined DAC

The pipelined DAC dissipates power from the reference input voltage similar to the cyclic one. Following the same steps as in the cyclic case, it is clear that the peak energy taken by each sampling capacitor, for each bit, in each cycle is given by Eq. 2.4, and since there are N stages in the pipeline, the total maximum energy is the same

Figure 2.6: Digital section of the quasi-passive pipelined D/A converter.

as Eq. 2.5.

Therefore, the same upper bound on power consumption of Eq. 2.6 applies to the QP pipelined DAC as well.

2.3 Non-ideal Effects

In the analysis of the converters considered so far, idealized models were used. Some practical imperfections cause deviations from these ideal models, which may deteriorate the performance of the converters. Depending on the required accuracy (mainly linearity) for the converters, some action may have to be taken to make them insensitive to these imperfections, or compensate for the error caused by them.

In this section, the effects of various non-ideal factors limiting the accuracy of the converter are discussed. The existing remedies are presented in Chapter 3, and the proposed new ones will be discussed in Chapters 4 and 5.

In some of the following sections, the simulation values of a typical cyclic DAC are used (Fig. 2.7). *The typical DAC* is designed in a 0.35- μm CMOS double-poly

technology. The switch sizes are chosen for a 100 MHz clock frequency for 10-bit resolution. The dummy PMOS transistor M_d is added to have a symmetrical design around C_1 and C_2 (its gate is tied to VDD, so it is always open). For the sake of simplicity, digital control signals are not shown, but it is understood that M_{3p} and M_{3n} have complementary controls to close or open at the same time.

Figure 2.7: Typical 10-bit cyclic DAC in 0.35- μm CMOS technology for 100 MHz clock frequency.

2.3.1 Parasitic Capacitors of Switches

In the simplified analysis of the switched-capacitor algorithmic D/A converters, thus far, the switches were abstract. In MOS technology, switches are made of NMOSFET and/or PMOSFET transistors. Although these transistors have advantages over other analog switches (such as diode bridge [22, Chapter 2]), they are less than perfect. The finite on resistance of these switches and their parasitic capacitors are factors that should be reckoned with in a more accurate analysis.

The main differences between the NMOS and PMOS switch types are control-voltage polarity and suitable source/drain voltage range. While the NMOS switch closes with a high gate-voltage ($V_{GS} > V_{th}$ or $V_{GD} > V_{th}$) the PMOS one is on

with a low gate-voltage ($V_{GS} < V_{th}$ or $V_{GD} < V_{th}$). Since the on resistance of the NMOS transistor in triode region increases as the gate-to-channel voltage drops, these devices are good switches for low source/drain voltages (relative to the power supply voltage); on the contrary PMOS switches are suitable for high channel voltages. Aside from these main differences, NMOS switches are preferable in the midrange voltages because they offer 2 to 3 times higher conductivity for the same size as the PMOS ones (due to higher electron mobility compared with hole mobility [23]).

Even though there are differences between NMOS and PMOS switches, for the purpose of this discussion, they follow the same principles. In other words, they both suffer from finite resistance when closed, and have similar parasitic capacitors. Hence, only the NMOS switch is considered in this and the following sections of this chapter.

An NMOS transistor together with its associated parasitic capacitors is shown in Fig. 2.8 [23]. Depending on the operating region of the transistor, capacitance values vary. Besides, some of the capacitor values depend on the terminal voltages in a given operating region.

Figure 2.8: NMOS transistor and its parasitic capacitors.

Of all these capacitors, C_{DS} is not commonly included in transistor models [23, 16].

Unlike the other parasitic capacitors, this capacitor is not intrinsic in the device, however, as shown in Fig. 2.9, fringing fields between the source and the drain metalization will always effect this capacitance. Although the value of C_{DS} is usually much smaller than the other parasitics, and the capacitor is linear, it can limit the accuracy of the DAC very significantly. (The effect will be further explained in the following sections.)

Figure 2.9: Fringing field creating C_{DS} shown on a simplified cross-section of an NMOS transistor.

The sizes of all parasitic capacitors depend on the technology and the size of the switch itself. As will be discussed later, the switch size is determined by the speed of the converter. Faster converters require larger switches with smaller on-resistance to charge and discharge the capacitors in a shorter time. Therefore, the effect of these parasitics is more important for high-speed DACs.

In the following sections, these parasitic effects are treated one at a time.

2.3.2 Nonlinear Junction Capacitance

Capacitors C_{SB} and C_{DB} represent the reverse biased junction capacitance of source and drain diffusion regions to the bulk (well). Since the bulk has a constant potential,

these two capacitors appear in parallel with the main capacitors of the converter, i.e. C_1 and C_2 (for AC voltages). Unlike the main capacitors, however, these capacitors are highly nonlinear.

The value of the source and drain small-signal junction capacitors can be expressed as [16]

$$C_{sb}(v_{SB}) = \frac{C_{sb0}}{\sqrt{1 + v_{SB}/2\phi_p}}, \text{ and } C_{db}(v_{DB}) = \frac{C_{db0}}{\sqrt{1 + v_{DB}/2\phi_p}}. \quad (2.8)$$

In the above equation, v_{SB} and v_{DB} are source-to-bulk and drain-to-bulk (bias) voltages, and C_{sb0} values correspond to zero bias condition. Constant ϕ_p is a material factor approximately equal to 0.3 V. The large-signal capacitor values can be obtained by first integrating the charge on a given voltage range using

$$Q_{SB} = \int_0^{V_{SB}} C_{sb0}(v_{SB}) dv_{SB}, \quad (2.9)$$

and a similar one for Q_{DB} . Then, $C_{SB} = Q_{SB}/V_{SB}$ yields the large-signal capacitance at a given node voltage.

Fig. 2.10 demonstrates variation with node voltage of the total junction capacitance for all switches on each side of M_3 in the typical cyclic DAC (Fig. 2.7). The large-signal (integrated) capacitance has less variations compared with the small-signal one as a consequence of averaging (integration).

If the switches are laid out symmetrically, and the diffusion capacitors match, the presence of the junction capacitors does not disrupt the addition of charges and the divide-by-two operation (but as will be shown soon, they affect the conversion precision in another way). In other words, if the equations are rewritten in terms of charges instead of voltages, the D/A conversion (to a resulting charge on C_{T2}) is still linear. To show this point, from the principle of charge conservation (C_{T1} and C_{T2} are the total capacitance at nodes N1 and N2 respectively of the cyclic DAC including all parasitics),

$$(C_{T1} + C_{T2})V_{C2}[n] = Q_{C_{T1}}[n] + Q_{C_{T2}}[n] = Q_{C_{T1}}[n-1] + Q_{C_{T2}}[n-1]. \quad (2.10)$$

Figure 2.10: Junction capacitance as a function of terminal-to-bulk bias voltage for the typical cyclic DAC of Fig. 2.7. C_{sb} and C_{SB} represent the small-signal and large-signal capacitance respectively.

Since $C_{T1} = C_{T2}$,

$$Q_{C_{T2}}[n] = \frac{1}{2}(Q_{C_{T1}}[n-1] + Q_{C_{T2}}[n-1]). \quad (2.11)$$

When it comes to sampling the output voltage of the converter, however, the nonlinear capacitance leads to integral nonlinearity for the transfer characteristics. To demonstrate the point, let's assume that for small capacitor nonlinearity, total large-signal capacitance can be approximated by a linear function of the terminal voltage such as

$$C_t = C_{t0} + \alpha V, \quad (2.12)$$

(i.e. first-order capacitor nonlinearity). Then, if Q is the charge on this capacitor, the voltage across it should be found by solving

$$V = \frac{Q}{C_{t0} + \alpha V}, \quad (2.13)$$

which precisely results in

$$V = \frac{-C_{t0} + \sqrt{C_{t0}^2 + 4\alpha Q}}{2\alpha}. \quad (2.14)$$

Clearly, if Q , the charge on the output capacitor in the last step, is a linear function of the input code, the voltage on the output node is not. For the typical example of Fig. 2.7, the simulated integral nonlinearity¹ caused by the nonlinear junction capacitors is shown in Fig. 2.11 for a 10-bit DAC. Maximum *INL* which is larger than 5.8 LSB is rarely acceptable.

Figure 2.11: Simulated integral nonlinearity caused by nonlinear junction capacitors for the typical example of Fig. 2.7 running as a 10-bit DAC with output voltage range of 0 V to 3 V.

One simple way of improving the DAC is to reduce this nonlinearity by partially cancelling the increase in the NMOS junction capacitance with the decrease in that of the PMOS through proper sizing of the devices. This method cannot eliminate the problem though, because the capacitor nonlinearity is not quite first-order, and the

¹See Appendix A for the definition of the performance metrics used throughout this thesis.

process variations can significantly disturb the balance. Better solutions to this issue are considered in Chapter 3.

2.3.3 Charge Injection

Capacitors C_{GS} and C_{GD} in Fig. 2.8 represent the gate-source and gate-drain overlap capacitance, plus the gate-channel capacitance in the triode region. The overlap capacitors are small, constant, and independent of the operating region, so they just slightly increase the total capacitance on each node. The gate-channel capacitor is related to the stored charge in the induced channel when the switch is closed [24]. Immediately after the closure of the switch (when there is still a large voltage difference between the two capacitors) the transistor may enter the saturation region. Following this gross settling, the transistor enters the triode region (small V_{DS}), and hence, the channel charge is determined by

$$Q_{\text{channel}} = C_{\text{ox}}(V_{GS} - V_{th}). \quad (2.15)$$

The capacitance associated with this charge (usually split equally between C_{GS} and C_{GD} in models [16]), is thus nonlinear. The nonlinearity of this capacitance, however, does not have to hurt the integral linearity of the converter (like C_{SB} and C_{DB} do) since all the switches can be turned off before sampling the output voltage (which would require an additional cycle in the timing diagram of Fig. 2.2). Nonetheless, the presence of the channel charge deteriorates the converter's performance in the following ways.

The stored charge in the channel is split between the source and the drain terminals of the switch when it opens. The proportion by which this division occurs depends on many factors including transition time of the gate voltage and impedances seen at the source and drain terminals [25, 26]. So long as layout is symmetrical around the charge splitting switch (S_3 in Fig. 2.2, M_{3p} and M_{3n} in Fig. 2.7), division by two is

still accurate. For other switches, since the capacitors hold the desired voltages when the switches are closed, after opening the switches charge injection creates an error in the voltage across the switch. This inevitably leads to offset (S_2 and insignificantly S_r) and/or gain error (S_1 and S_2) for the converter. In case of the typical converter, this gain error can be as high as 5%, which is also temperature dependent.

Gate control signals to the switches come from digital circuits. These control voltages are tied to the power supplies through digital gates. According to Eq. 2.15, the injected charge is dependent on V_{GS} which is in turn supply voltage dependent. This has two consequences, first, converter gain is dependent on the average supply voltage. Secondly, the circuit has poor supply-noise rejection. This latter issue is an especially important flaw in large mixed-signal systems.

2.3.4 Source-Drain Parasitic Capacitor

As mentioned before, C_{DS} arises from the fringing electrical fields originating from the drain contact and metalization to that of the source. It is the stray capacitance between the source and the drain of M_{3p} and M_{3n} of Fig. 2.7 that, as will be shown shortly, harms the linearity of the DAC. To this capacitance should be added all other stray capacitors that are in parallel, even if they are not in the vicinity of the transistors.

Figure 2.12: Effect of C_{DS} in the operation of the cyclic DAC.

The effect of C_{DS} can be easily established using the simplified diagram of Fig. 2.12. In the first part of this figure, during any ϕ_2 , S_3 (of Fig. 2.2) is closed to share and

split the C_1 and C_2 charges. As a result, C_{DS} is shorted in this phase. In the next ϕ_1 , C_1 is connected to the V_{ref} source or ground for charging or discharging respectively. Since all the capacitors involved are linear (without any loss of generality), based on superposition, the effect of input bits can be considered separately. Hence, it is assumed that the next bit is a zero, and the capacitor is being discharged. In this arrangement, C_{DS} charges up to approximately V_{C_2} of the last phase. More precisely, C_2 shares its charge with C_{DS} . This charge is consequently lost during the next ϕ_2 when C_{DS} is shorted again. In this manner, C_{DS} *steals* a small amount of charge from C_2 in every clock cycle. The relative amount of the stolen charge is approximately proportional to the ratio of C_{DS}/C_2 . In other words, as a result of this charge sharing, the $1/2$ factor in Eq. 2.2 should be modified as

$$V_{out} = V_{ref} \sum_{n=0}^{N-1} b_n (2\beta)^{n-N}, \quad (2.16)$$

where

$$\beta = \frac{C_{DS} + C_2}{C_2}, \quad (2.17)$$

is the *fringe factor*. The fringe factor is normally very close to 1, for the typical example it is around 1.007. This apparently small deviation from ideal, however, can easily limit the differential nonlinearity to less than 7 bits! Since this effect is very similar to capacitor mismatch, it will be further discussed in Section 2.3.6.

A similar effect reduces the accuracy of the pipelined DAC. For example, when capacitors C_{i-1} and C_i are sharing their charges, C_{DS} of $S_{i+1,3}$ takes some of the charge away from them (Fig. 2.5).² This charge is dissipated during the next phase when the switch is closed and C_i and C_{i+1} share their charges.

The source-drain parasitic capacitance can be reduced using careful layout techniques explained in Chapter 6.

²This C_{DS} also transfers some charge proportional to $b_{i+1} V_{ref}$ to C_{i-1} and C_i at this phase, which causes a minor gain error.

2.3.5 Switch On-Resistance

In the ideal model for the algorithmic DACs, switches have no on-resistance, hence the transfer of charge to/from capacitors happens instantly. In practice, due to the finite R_{on} , the transfer of charge is never complete.

When a switch closes between two nodes with very different potentials, for example for charging C_1 from 0 to V_{ref} , MOS transistors go through a large transient operation. During the large transient, transistors exhibit significant variations in R_{on} , or may even start from a saturation state (current source model), such as in the above example. After a short time following closure of a switch, large transients subside, and a fine settling phase during which R_{on} is almost constant begins. For high resolution converters, charge transfer must be almost complete before the switch opens. For a high accuracy transfer, most of the phase time is spent in fine settling. The approximate on-resistance of an NMOS transistor in triode region is given by

$$R_{\text{on}} \approx \frac{1}{k \frac{W}{L} (v_{\text{GS}} - V_{\text{th}})}, \quad (2.18)$$

where W/L is the width/length ratio of the transistor, and k is a process constant [23].

For a given clock period, the settling error is exponentially reduced by decreasing the time-constant $R_{\text{on}}C$, i.e.

$$\Delta V_{\text{final}} = \Delta V_{\text{initial}} e^{-\frac{T}{R_{\text{on}}C}}. \quad (2.19)$$

Therefore, R_{on} has to be minimized by using the smallest transistor length possible, which is limited by the technology feature size (say $0.35 \mu\text{m}$). The R_{on} is maximum for small v_{GS} , which means compared with M_1 , M_2 , and M_r , M_3 is worse off (Fig. 2.7), especially when V_{C_2} is in midrange. The resistance is also higher at hot temperatures, and for slow processes.³

³Slow process refers to a set of worst-case parameters for transistor models (as well as other

It is difficult to calculate exactly what settling accuracy is needed for a given resolution, but a reasonably conservative estimate can be found by requiring the capacitor voltages to settle within 10% of the LSB in the worst case. With this criterion, the settling error will cause less than 1/10 LSB inaccuracy in conversion (e.g. 0.01% for 10 bits). Generally, the converter has to be carefully simulated for the worst case process corner to ensure this condition is met.

2.3.6 Capacitor Mismatch

The accuracy by which an algorithmic DAC performs the conversion is very much dependent on the accuracy of the divide-by-two operation. In a general cyclic DAC, where the divisor is r , the main operation in the flowchart of Fig. 2.1 should be modified to

$$R = \frac{1}{r}(Gb_n V_{\text{ref}} + R), \quad (2.20)$$

where G is a gain factor close to 1 (equal to $r - 1$ for the quasi-passive cyclic DAC). The final conversion result is

$$V_{\text{out}} = G V_{\text{ref}} \sum_{n=0}^{N-1} b_n r^{n-N}. \quad (2.21)$$

One cause for deviation of r in Eq. 2.21 from the desired value of 2 is capacitor mismatch. For the cyclic converter of Fig. 2.2 depending on the *total* capacitance at nodes N1 and N2 (denoted by C_{T1} and C_{T2}) when S_3 is closed, operation in each cycle is modified to

$$V_{C_2}[n] = \frac{C_{T1}}{C_{T1} + C_{T2}} b_n V_{\text{ref}} + \frac{C_{T2}}{C_{T1} + C_{T2}} V_{C_2}[n-1], \quad (2.22)$$

which results in

$$r_{\text{mismatch}} = \frac{C_{T1} + C_{T2}}{C_{T2}}, \quad (2.23)$$

element models) in a given technology that results in the slowest circuits that may be fabricated in that technology. For example, thicker gate oxide and longer gates than nominal make the NMOS and PMOS transistors slower than normal.

and

$$G_{\text{mismatch}} = \frac{C_{T1}}{C_{T2}} = r - 1. \quad (2.24)$$

Further, after including the fringe factor of Section 2.3.4 in the calculations, r can be evaluated as

$$r = \frac{C_{T1} + C_{T2}}{C_{T2}} \frac{C_{T2} + C_{DS}}{C_{T2}}. \quad (2.25)$$

Deviation of r from 2 causes *DNL* and *INL* which are proportional to the error value. Larger discontinuities occur at major code transitions, i.e. when transiting from one code to the next (in increasing order) changes many bits from 1 to 0 simultaneously. The worst point is right at the midrange, when input changes from $011 \dots 11$ to $100 \dots 00$. Fig. 2.13 illustrates the simulated effect of 10% error in r (i.e. 20% mismatch, exaggerated to show better) on the transfer function, *DNL*, and *INL* of a 6-bit cyclic converter. In the simulation, it is assumed that $C_{T1} > C_{T2}$.

Worst case *DNL* (especially for more realistic mismatch values, i.e. less than 1%) approximately equals the error in r (in percentage). For example, if $C_{T1} = 1.002 C_{T2}$ (assuming $C_{DS} \approx 0$ for now), then $r = 2.002$, and $DNL_{\text{max}} \approx 0.1\%$ which is about 0.5 LSB for 9 bits. To prove the point, let's look at the normalized voltage difference between the outputs for codes $011 \dots 11$ and $100 \dots 00$, i.e.

$$\frac{\Delta V_{\text{MSB}}}{G V_{\text{ref}}} = V_{100 \dots 00} - V_{011 \dots 11} = r^{-1} - \sum_{n=0}^{N-2} r^{n-N}. \quad (2.26)$$

The above equation can be rewritten as

$$\frac{\Delta V_{\text{MSB}}}{G V_{\text{ref}}} = r^{-1} - r^{-1} \sum_{m=1}^{\infty} r^{-m} + r^{-N} \sum_{m=1}^{\infty} r^{-m}. \quad (2.27)$$

Using the binomial expansion formula for $a < 1$, i.e.

$$\sum_{m=1}^{\infty} a^m = \frac{a}{1-a}, \quad (2.28)$$

one can rewrite Eq. 2.27 as

$$\frac{\Delta V_{\text{MSB}}}{G V_{\text{ref}}} = r^{-1} - r^{-1} \frac{r^{-1}}{1-r^{-1}} + r^{-N} \frac{r^{-1}}{1-r^{-1}}, \quad (2.29)$$

Figure 2.13: Nonlinearity caused by 20% capacitor mismatch in a 6-bit cyclic DAC.

which may be further modified to

$$\frac{\Delta V_{\text{MSB}}}{G V_{\text{ref}}} = (1 - 2r^{-1}) \frac{r^{-1}}{1 - r^{-1}} + r^{-N} \frac{r^{-1}}{1 - r^{-1}}. \quad (2.30)$$

For r values close to 2, $\frac{r^{-1}}{1 - r^{-1}} \approx 1$, and since r^{-N} is the normalized LSB, Eq. 2.30 results in a midpoint (worst case) normalized DNL value of

$$DNL_{\text{max}} = DNL_{\text{MSB}} \approx 1 - 2r^{-1} \approx \frac{r}{2} - 1. \quad (2.31)$$

Similarly, it can be shown that the second worst differential nonlinearity occurs at 1/4 and 3/4 of the range, whose value is approximately $\frac{r/2 - 1}{2}$, and so on.

One significant negative aspect of the nonlinearity pattern caused by capacitor mismatch, such as the one seen in Fig. 2.13, is that the largest error is right in the middle of the range. The presence of this large discontinuity at the midpoint means that the relative error increases as the signal amplitude decreases. For applications like audio and voice, where the converter is required to have a larger dynamic range than the peak signal-to-noise+distortion ratio (*SNDR*), the nonlinearity pattern of the basic algorithmic converter makes it unsuitable.

Capacitor mismatching is effected by inaccuracies on the edge of the capacitor plates (mainly the top plate), and by variations in the oxide thickness (small-scale and large-scale) [27, 28]. Certain layout techniques can be employed to improve the capacitor matching, such as using square shapes and common centroid topology. The matching accuracy is also process dependent, and thus characteristics should be obtained for the target technology. Some experimental data is available for certain technologies [29, 30, 31, 32, 33].⁴ The precision is improved by increased capacitor size as $C^{-\theta}$ where $\frac{1}{2} < \theta < \frac{3}{4}$ (close to $\frac{1}{2}$ for oxide-thickness dominant, i.e. area dependent, and towards $\frac{3}{4}$ for random-edge dominant, i.e. periphery dependent).⁵

In today's technologies, 0.3% mismatch is typically the best achievable matching for 1 pF capacitors for high yield [33]. Larger capacitors can improve the matching accuracy, however, increasing the capacitor size has other implications, such as increased area, and a rise in power or reduced speed. Although large capacitors reduce the thermal noise as well, the limiting factor for resolution is usually the matching

⁴Unfortunately, no capacitor matching data was available for the TSMC 0.35- μm CMOS, and the 0.6- μm CMOS (used for PDAC) technologies. The special capacitor matching experiments for the TSMC 0.35- μm CMOS, implemented together with the cyclic DACs, are expected to provide some information on this issue.

⁵Assuming fixed-shape capacitor topologies, doubling the capacitor size, double the area, but increases perimeter by $\sqrt{2}$. Therefore, the absolute area dependent mismatch grows by $\sqrt{2}$, whereas the absolute periphery dependent mismatch increases only by $\sqrt[3]{2}$. The normalized (divided by the capacitor value) mismatches are then reduced by $\frac{1}{\sqrt{2}}$ and $\frac{1}{\sqrt[3]{2}}$.

accuracy (except for very low voltage converters — more on noise in Section 2.3.8). Therefore, capacitor matching alone can limit the *DNL* of the cyclic converter to about 9 bits.

The pipelined converter suffers from matching, and C_{DS} similar to the cyclic converter. However, since divide-by-two is executed in different stages, many capacitor matching factors are involved in the conversion. Besides, the coupling through C_{DS} is more complicated because it can cause cross-talk between succeeding input samples. To minimize complexity, let's assume through careful layout C_{DS} is made negligible. For the pipelined converter of Fig. 2.5, the output voltage can be expressed as

$$V_{out} = V_{ref} \sum_{n=0}^{N-1} g_n b_n \prod_{k=n}^{N-1} r_k^{-1}, \quad (2.32)$$

where

$$g_n = \frac{C_{Ti}}{C_{i-1}} \quad (2.33)$$

is the bit gain-modifier, and

$$r_k = \frac{C_{Tk} + C_{Tk-1}}{C_{Tk-1}} \quad (2.34)$$

is the exact divisor between C_{Tk} and C_{Tk-1} .

The effect of the capacitor mismatch in the pipelined converter is different from the cyclic converter in that, for the former, the differential nonlinearity does not exhibit a regular pattern like Fig. 2.13, instead, *DNLs* at major transitions are independent. An example of the simulated nonlinear behaviour of the pipelined converter is shown in Fig. 2.14.

Differential nonlinearity at major code transitions in the pipelined converter is a function of mismatch between the respective capacitor and the binary weighted average of all the other ones to its left (less significant units — see Fig. 2.5). Fig. 2.15 is an overlapped *DNL* plot for 200 Monte Carlo simulations of a 6-bit pipelined DAC with 5% standard deviation in capacitor accuracy. Statistically, the largest nonlinear

Figure 2.14: An example of nonlinearity caused by 10% standard deviation in capacitor accuracy for a 6-bit pipelined DAC.

point is in the middle, in fact on average, the *DNL* at the midpoint is twice as large as the ones at the 1/4 range points.

The distribution of maximum *DNL* and *INL* for 1000 Monte Carlo simulations of a 9-bit pipelined DAC is shown in Fig. 2.16. The figure indicates that, for high yield, 9-bit resolution is a practical limit for linearity in a technology with 0.07% individual capacitor standard deviation (i.e. 0.1% mismatch SD). A similar result can be obtained for the cyclic DAC.

Figure 2.15: Differential nonlinearity caused by 5% standard deviation in capacitor accuracy for a 6-bit pipelined DAC. 200 Monte Carlo simulation results for capacitor mismatch are superimposed.

2.3.7 Capacitor Nonlinearity

Capacitor nonlinearity can arise from penetration of the electric field into the plates. For good conductors, such as metals (with very large number of free charge carriers), the electric field inside the capacitor plates is zero (i.e. the interplate electric field lines terminate on the surface of the plates). With semiconductor plates, however, the electric field partially extends into the plate, increasing the effective distance between the plates, and thereby, reducing the effective capacitance. This phenomenon is significant when at least one of the electrodes is made of silicon. Metal-plate capacitors are very linear, but are usually very large in area (about 30 times larger than silicon plate capacitors of the same value), unless thin inter-metal oxide is available in the process.

The voltage coefficient of capacitance defined as

$$\gamma_V = \frac{1}{C} \frac{\partial C}{\partial V}, \quad (2.35)$$

Figure 2.16: Distribution of the maximum *DNL* and the maximum *INL* caused by 0.07% standard deviation in capacitor accuracy for a 9-bit pipelined DAC (1000 Monte Carlo simulations for capacitor mismatch).

is dependent on the capacitor structure and doping level in the silicon plate(s) [16, p. 88]. For polysilicon-to-polysilicon (PTP) capacitors, if the doping levels are equal, γ_V is very small (less than 10 ppm/V) [27]. The voltage dependence of the metal-to-polycide (MTPC) capacitor is smaller than the PTP ones, but it is more nonlinear (second order effects are worse, as will be seen shortly) [34].⁶

In much the same way as the junction capacitance of the switches, the nonlinearity of the main capacitors affects the integral linearity of the converter. For large switch sizes, junction capacitor nonlinearity usually dominates *INL*, but for very small switch sizes (very slow DACs), it may be the opposite. Besides, for the stray-insensitive DACs (to be discussed in Chapter 3), junction capacitance has no contribution to nonlinearity, but the main capacitor nonlinearity is still effective.

One simple solution that can very effectively cancel out the linear term in the capacitor-voltage relationship is the use of split top-to-bottom capacitors. In this

⁶The voltage coefficient of capacitance for the 0.35- μm CMOS technology used for the main converters in this work is not available, but is believed to be around 100 ppm/V.

method, each main capacitor in the DAC is split into two equal capacitors that are used in parallel by connecting the top plate of one to the bottom plate of the other and vice versa. If γ_V is a voltage-independent constant (i.e. linear CV curve) then

$$C = C_0 + \gamma_V V C_0. \quad (2.36)$$

Using the split top-to-bottom configuration, the total capacitance is

$$C = \frac{C_0}{2} + \gamma_V V C_0 + \frac{C_0}{2} + \gamma_V (-V) C_0 = C_0. \quad (2.37)$$

The quadratic portion of the capacitance nonlinearity, however, is not easily cancelled. For PTP capacitors, this factor is very small (well below 1 ppm/V) [34], and normally does not limit the converter linearity.

2.3.8 Noise

Various noise sources in the converters limit their performance. When a DAC is supplied with an AC input signal, the conversion error in the form of DNL partially turns into noise components (mostly spectral spikes, i.e. spurs) which are added to the input quantization noise and appear at the output. Aside from these noise components, there are also thermal (white), and flicker ($1/f$) noise sources in the converter and the sample-and-hold circuits. The DNL induced noise is signal dependent and related to the matching accuracy etc. which can be improved only by layout techniques or other error correction schemes, and is not considered here.

Switch thermal noise

The thermal noise of the R_{on} of the switches is sampled on the capacitors when the switches open. This happens as the capacitors are charged/discharged by the reference/ground, or when the capacitors share their charge in the next phase. Although the noise voltage from the previous cycle is added to the new one in every cycle, since

the previous noise is divided by two along with the partial result, the overall noise is not expected to grow by the number of cycles. There is no flicker noise contribution in the converter core, since the flicker noise modulates the drain current, and with the proper design of a switched-capacitor circuit the capacitor voltage is settled well before opening the switches and there is negligible current flowing through the switch at that time.

Figure 2.17: Noise sampling mechanism in the input phase (ϕ_1) of a cyclic DAC.

To begin the derivation of the output thermal noise of the cyclic DAC, let's first find the sampled thermal noise of a switch. Fig. 2.17 shows the input section of the cyclic DAC. In ϕ_1 , when the reference voltage is being sampled, switch S is closed and exhibits a resistance R_{on} . The resistance has a thermal noise given by

$$\overline{v_{R_{on}}^2} = 4\Theta R_{on}, \quad (2.38)$$

where the notation $\Theta = kT$ (k is the Boltzman constant, and T is the absolute temperature here) is used to avoid confusion between temperature and the symbol for the conversion cycle T . The low-pass filter formed by R_{on} and C has a noise equivalent-bandwidth of

$$NBW = \int_0^\infty \left| \frac{1}{1 + jR_{on}C\omega} \right|^2 d\omega = \frac{1}{4R_{on}C}, \quad (2.39)$$

in Hz. This is the bandwidth of an ideal LPF (brick wall) which has the same output noise power as the $R_{on}C$ filter with the white input noise. Hence, the total thermal noise across C is

$$\overline{v_C^2} = \frac{\Theta}{C}. \quad (2.40)$$

Since this noise power is independent of R_{on} , the variation of R_{on} during the opening transient does not affect it. Therefore, Eq. 2.40 represents the noise power sampled on C when the switch opens.

Figure 2.18: Noise sampling mechanism in the accumulation phase (ϕ_2) of a cyclic DAC.

The sampled thermal noise of the charge sharing switch in the cyclic DAC (S_3) is best explained using Fig. 2.18. Similar to the above general case, the noise sampled on C_1 and C_2 has a power of

$$\overline{v_{S_3}^2} = \frac{2\Theta}{C}, \quad (2.41)$$

since the equivalent series capacitance is $C/2$. However, only half of the noise voltage is sampled on the integrating capacitor C_2 (noise left on the input capacitor C_1 will be discharged in the next ϕ_1). Thus, the noise power remaining on C_2 from both phases ϕ_1 and ϕ_2 of one clock cycle is

$$\overline{v_{\text{cycle}}^2} = \frac{\Theta}{4C} + \frac{\Theta}{2C} = \frac{3\Theta}{4C}, \quad (2.42)$$

since the noise sources are independent.

In each cycle, the noise left from the previous cycle on C_2 is divided by two (same as the partial result), and added to the new noise. Independence of the noise sources, and their white nature (independence from sample to sample) indicate that various noise components add in power (not voltage). The noise on C_2 at the end of cycle n is

$$\overline{v^2[n]} = \overline{v_{\text{cycle}}^2} + \frac{1}{4}\overline{v^2[n-1]}. \quad (2.43)$$

Recursively, the final noise power across C_2 at the end of conversion is

$$\overline{v_{\text{final}}^2} = \frac{3}{4} \frac{\Theta}{C} \sum_{i=0}^{N-1} \left(\frac{1}{4}\right)^i \approx \frac{\Theta}{C}, \quad (2.44)$$

where in the last step, an approximation to the binomial expansion based on the $N \gg 1$ assumption is used.

For the typical cyclic DAC (Fig. 2.7) with 1 pF capacitors, this is comparable to a 13-bit quantization noise level.

S/H and other noise sources

The noise in the S/H circuit is very much dependent on its architecture and circuit, nevertheless, the sampling process causes all the noise components above the sampling frequency, f_s , to fold back (alias) into the baseband. As a result, the sample-and-hold contributes a very significant amount of noise to the output (usually dominates for high-speed converters). The S/H noise will be discussed in details later.

In addition to the above noise contributors, there is also the noise coupled to the converter through parasitics. This noise component usually originates from the other parts of the integrated circuit, especially from large digital blocks. One main parasitic coupling is through the common substrate of the IC. It is therefore recommended to exercise careful layout techniques to minimize this effect. A circuit solution for effective reduction of this noise is proposed in Chapter 4.

2.3.9 Leakage

All the source/drain junctions in the MOS switches of the converters are reverse biased. Reverse-biased junctions have a small leakage current which can change the stored voltage on a capacitor over time.

The value of the leakage current is estimated at 10 pA/mil² [16, p. 472] at room

temperature. This value roughly doubles for every 10 °C rise in temperature.⁷ For the typical example, the junction area is about 0.3 mil², and the conversion time is 100 ns. This results in a 300 nV drift in the voltage across the 1 pF capacitor. While this leakage is quite negligible at room temperature, for very hot junctions it may become significant.

2.4 Conclusion

In this chapter, basic architectures for algorithmic DACs, especially the switched-capacitor quasi-passive implementations, were studied. The practical limitations to the performance of these DACs due to non-ideal effects have been discussed, and the most important effects have been quantified. In the next chapter, improvements attempting to alleviate some of the shortcomings will be reviewed.

⁷No specification is available for the junction leakage in TSMC's 0.35- μ m CMOS technology.

Chapter 3

Improved Algorithmic DACs

Ever since the original cyclic DAC was proposed, there have been attempts to improve the architecture for higher linearity applications. The non-ideal effects studied in Section 2.3 can limit the linearity of the original cyclic DAC below 7 bits. Some techniques have been proposed that promise to increase this accuracy up to 16 bits.¹ Despite all the improvements, no publication has been found to report even a 10-bit linearity for any algorithmic DAC.

After studying the original algorithmic DACs in the previous chapter, improvements for the algorithmic DACs, mostly suggested and/or implemented by others found in the literature, are studied, and their limitations and drawbacks are discussed. Proposed solutions of this thesis are introduced in the following chapters.

3.1 Stray Insensitive Cyclic DAC

The original cyclic DAC presented in Chapter 2 can be made stray-insensitive by employing an opamp in charge transfer to the capacitors [36, 37, 38]. This is accomplished using the virtual ground node provided by the opamp to prevent the charge

¹Some studies and their associated claims attack only one resolution-limiting factor, so their claims are questionable [35].

stored on the main capacitors from transferring to the parasitics, and vice versa. This type of solution is not desirable, however, because of the speed penalty. If the core of the DAC is made of only switches and capacitors, it can run at much higher clock frequencies at a lower power.

It is possible to maintain the quasi-passive nature of the cyclic DAC, and yet avoid the errors caused by stray capacitors. The idea was proposed by Dias in [1], and later refined and implemented [39, 9].

The basis for the stray-insensitive quasi-passive switched-capacitor cyclic DAC is similar to the stray-insensitive SC integrator [16, p. 278], and is shown in Fig. 3.1. As will be discussed shortly, the sample-and-hold is now a part of the DAC.

The focus in this method is on the amount of charge transferred and shared rather than the node voltages. As explained previously, nonlinear junction capacitors mandate this distinction. Capacitor C_1 is charged to V_{ref} or discharged to ground in every phase 1, depending on the value of the corresponding bit. The parasitic capacitance at node N0 (including source/drain junction capacitors) are charged/discharged at the same time, but since in ϕ_2 this node is grounded, the charge on these parasitics does not contribute to the charge brought to node N1 (now shorted to N2). The only charge added to N1/N2 during ϕ_2 is $-b_n V_{\text{ref}} C_1$ (C_1 includes all the parasitic capacitors that are in parallel with it). The stored charge on C_2 from the previous cycle (0 if this is the first cycle) is added to $-b_n V_{\text{ref}} C_1$ and divided between C_1 and C_2 . At the end of conversion, i.e. in ϕ_2 of the N th clock cycle, the charge on C_1 and C_2 is transferred to the S/H capacitor $C_{\text{S/H}}$. The value of this charge is

$$Q = -2V_{\text{ref}} C \sum_{n=0}^{N-1} b_n 2^{n-N}, \quad (3.1)$$

where $C_1 = C_2 = C$ nominally. Capacitor $C_{\text{S/H}}$ is discharged by S_d just before the charge transfer. By selecting $C_{\text{S/H}} = 2C$, the output voltage at the end of conversion

Figure 3.1: Stray-insensitive quasi-passive switched-capacitor cyclic digital-to-analog converter [1]. (a) Schematic. (b) Timing diagram.

is

$$V_{\text{out}} = V_{\text{ref}} \sum_{n=0}^{N-1} b_n 2^{n-N}, \quad (3.2)$$

as desired.

The schematic of Fig. 3.1 is slightly modified compared with [1] to convey the charges of both C_1 and C_2 to the sample-and-hold. Discharging both C_1 and C_2 , as described above, helps in reducing SC noise (Θ/C) by doubling the effective capacitance and does not require an extra cycle.

It is possible to run the converter part of Fig. 3.1 at a much higher clock frequency than its S/H. To take advantage of this possibility, Dias in [1] suggests to use two sets of C_2 and its associated switches, i.e. the integrating sections, as shown in Fig. 3.2. In this method, at any time, one integrating section participates in the conversion with C_1 while the other one delivers the accumulated charge from the previous conversion to the S/H. Only one capacitor, and three switches (plus the required logic) are added to the circuit to double its overall conversion speed. The sample-and-hold offset is also cancelled in [1] through a special technique. Offset is not usually a very critical specification of the signal processing DACs. Since more offset may be added to the output in the succeeding stages, and because offset cancellation techniques increase the SC (thermal) noise, use of such techniques is not recommended.²

The basis for the conversion is still division-by-two through charge sharing between equal capacitors. Hence, the new architectures still rely on capacitor matching for their accuracy. The matching of capacitance on nodes N1 and N2 in Fig. 3.1, and the ones on nodes N1 and N21/N22 in Fig. 3.2 (including parasitics) remains the main factor in determining the linearity of the converter. Even though the schematic diagrams do not show this point clearly, using dummy transistors and resizing, one has to ensure that the matching is only limited by the random process variations.

²On the plus side, offset cancellation schemes also reduce the flicker noise. Therefore, they may be used if offset and/or low frequency noise are very critical.

Figure 3.2: Stray-insensitive quasi-passive switched-capacitor cyclic digital-to-analog converter with two integrating capacitors [1].

Another matching aspect of the new schemes, that did not exist in the basic design of Section 2.1, is the matching of *impedances* seen at nodes N1 and N2 of Fig. 3.1 (or nodes N1, N21, and N22 of Fig. 3.2). Any mismatch between these impedances can cause unequal distribution of the channel charge in S_5 (or S_{51} and S_{52}) during the opening of the switch (charge injection). The value of the channel charge can be up to 10% of the overall charge or higher, thus even 1% mismatch in distribution can be significant. It may be necessary to add dummy switches in series with C_2 of Fig. 3.1, at the bottom plate, to make the impedances symmetrical.

Charge injection from the switches should be minimized through proper usage of delayed clock phases, and dummy switches. This issue was not suitably explored/implemented in [1, 39, 9] and could be one of the reasons for the poor performance of their converter (barely 7-bit linearity in [9]).

The S/H used in the schematic diagrams of Fig. 3.1 and Fig. 3.2 are resettable,

i.e. the output voltage on them is reset to zero before charging up to its new value. In most practical cases, the final output of the DAC should be a continuous signal, and as such, these frequent reset pulses at the output rate are not acceptable. For those cases, there is a need for a second sample-and-hold after these circuits.

While it is possible (as will be seen later) to design a S/H that does not need to be reset in every cycle, it is almost always necessary to use two S/Hs for the converter. The reason for phase alternation is that the first S/H has to discharge the nonlinear junction capacitance at N_1 , N_2 , etc., and hence cannot have a linear continuous-time output. A second S/H can be designed to avoid charging any nonlinear capacitor and therefore have linear output.

3.2 Stray Insensitive Pipelined DACs

Pipelined DAC configurations which are stray insensitive have also been proposed [2, 18]. These designs use an opamp in every stage of the pipelined converters.

Figure 3.3: Stray-insensitive switched-capacitor building block for the pipelined digital-to-analog converter [2].

Larson [2] uses the circuit of Fig. 3.3 as the building block for his pipelined DAC. In this circuit C_1 is discharged to zero in ϕ_1 , while at the same time C_2 and C_3

are charged to bV_{ref} , and V_{in} respectively. During ϕ_2 , the charges on C_2 and C_3 are transferred to C_1 . Assuming $C_1 = 2C_2 = 2C_3$, this results in

$$V_{\text{sum}} = \frac{1}{2}(V_{\text{in}} + V_{\text{ref}}). \quad (3.3)$$

It should also be noted that the opamp offset is cancelled through this switching scheme.

Figure 3.4: Top-level diagram of the stray-insensitive switched-capacitor pipelined digital-to-analog converter [2].

The complete pipelined DAC according to Larson is shown in Fig. 3.4. The succeeding stages switch their clock phases between Φ_1 and Φ_2 alternatively (N is assumed even in the figure). The reason is that while one stage is performing summation, the next one has to sample its output as V_{in} . The final output yields the overall converted analog signal.

The converter of Fig. 3.4 is fairly large and slow. An opamp is needed in every stage, and two opamps have to settle in series in every clock phase. If the settling time of a single opamp to the desired accuracy is $\mathcal{T}$, then each clock phase has to be

larger than $1.3 \mathcal{T}$.³ Hence, the maximum conversion rate is

$$\mathcal{R}_{\max} = \frac{1}{2.6 \mathcal{T}}. \quad (3.4)$$

3.3 Mismatch Tolerant Cyclic DACs

For all the algorithmic DACs considered in this chapter so far, capacitor mismatch still remains as the most important limiting factor for the linearity of the converters.

In general, various methods of linearity enhancement for D/A converters have been suggested and implemented. While some of these methods are more suitable for other types of converters, a few are particularly attractive for cyclic DACs.

3.3.1 Trim Capacitors

Using small trim capacitors in addition to the main capacitors can compensate for the mismatch [40, 41]. Kobayashi et al. in [40] suggest measuring the capacitor mismatch while trim capacitors are being switched in parallel with one of the main capacitors to find the best combination. When the best matching is found, a register holds the combination to be used during the conversion. The calibration process can take place during any idle interval, although, since the capacitor matching does not change significantly with time, a power-up calibration should be sufficient.

For a 14-bit converter with 1 pF main capacitors, trim capacitors smaller than 100 aF (a = atto = 10^{-18}) are required. Such small capacitors are very hard to design. The method also requires a high precision comparator.

Altogether, this type of error correction requires more precise analog components, and as such, is less favored over other (mostly digital) correction methods.

³The step response of two cascaded first-order stages is given by $1 - (1 + t/\tau)e^{-t/\tau}$. For a settling accuracy of 0.01%, the cascaded stages are 30% slower than each stage alone.

3.3.2 Radix Transformation

As explained in Section 2.3.6, the result of capacitor mismatch and finite C_{DS} can be expressed in a new equation for the output voltage, i.e.

$$V_{out} = G V_{ref} \sum_{n=0}^{N-1} b_n r^{n-N}, \quad (3.5)$$

where r is close, but not equal to 2, and G is the gain modifier (≈ 1). The above equation indicates that the value of bit n in the output is r^{n-N} instead of 2^{n-N} . In other words, the converter operates in *radix- r* number system, and in that sense, it is a linear converter!

If the digital input is transformed from radix-2 to radix- r prior to conversion, then the output will be an accurate analog representation of the input. For this to be possible, first the value of r must be known, secondly, radix transformation should be feasible.

Although variable conversion radix was used in [42] for the purpose of improving relative accuracy in cyclic D/A and A/D converters, the idea was first used by Mannonen in [43] to compensate for matching error. This conversion methodology is a special case of the general class of redundant converters. Redundancy in a D/A converter refers to the overlap of the output values for different input codes, e.g. codes 510 and 513 may produce equal outputs (within the LSB of the converter, of course). A matching code-transformer has to skip the redundant codes in order to produce a linear transfer characteristics.

For a cyclic DAC to be a redundant converter, its radix has to be smaller than 2. One must deliberately mismatch the converter capacitors ($C_2 > C_1$) to ensure that even under worst case ratio errors caused by fabrication, this relationship is maintained. For example, if the worst case capacitor mismatch in the process is known to be 0.4%, it is safe to set $C_2 = 1.005C_1$. The nominal radix is then about 1.995, and can range from 1.991 to 1.999.

To implement the radix transformer, the actual capacitor ratio or the radix has to be measured. It is possible to measure the radix at the package-test step of manufacturing, and store the value in a non-volatile memory on the chip. While this method has the advantage of requiring no calibration circuit on chip, the implementation of non-volatile memory in the technology may not be economical (not to mention the additional test time).

Another approach for radix measurement is to implement a self-calibration scheme on the same chip. The method used in [43] involves the use of an A/D converter for the calibration of the cyclic DAC. This method is particularly attractive if the ADC is already a part of the system function, e.g. in a line-card voice codec. The calibration scheme is fairly complicated and involves solution of a system of linear equations, and according to Mannonen [43], requires a CPU for the calibration. In the correction phase, a lookup table may be enough.

Generally, radix transformers slightly reduce the input range, however, provided that the converter properly saturates at the limits (instead of rolling over), this is normally not an issue for most applications. The amount of reduction in range is similar to the new calibration scheme to be proposed in Chapter 4, so this issue will be discussed in that chapter.

3.3.3 Ternary Code

One of the major issues with the original algorithmic converters is the presence of the largest nonlinearity error in the middle of the range. Such large errors at the midpoint keep the distortion level almost constant regardless of the signal amplitude for the centered inputs. In other words, *SNDR* drops proportional to the signal level, or the converter has equal peak *SNDR* and dynamic range (*DR*).

For many practical applications such as voice and audio, larger *DR* than the *SNDR* is needed. For example, in telephony, 40 dB of peak *SNDR* is satisfactory, whereas

dynamic range in excess of 80 dB is needed from the converter.

There has been some efforts to improve the performance of the cyclic converters by removing the major *DNL* from the midpoint. Kobayashi in [44] explains a scheme for moving the largest error from the midpoint to another location and reducing its size at the same time. The technique uses a ternary number system to achieve the goal.

Kobayashi's ternary digits can take one of three values of -1, 0, and 1. The transformation method is shown by way of an example in Table 3.1. The ternary representation has one fewer digit than the binary one, but it cannot represent the most negative value of the 2's complement code (-16 in the example). Given the fact that the number of ternary code combinations for $N - 1$ digits is 3^{N-1} which is larger than 2^N (except for the trivial case of $N = 2$), some ternary combinations are bound to have equal values. For example, 1c1c and 1011 are both equal to 5 (where "c" stands for -1 for the sake of clarity). The choice of codes has to be made in a way that will optimize the performance of the converter. It can be proven that Kobayashi's choice of the ternary code is optimal in minimizing the largest *DNL* [44].

In implementation, a -1 can be created using a negative reference voltage. Although in this case, one has to carefully match the positive and negative reference voltages. The alternative is to use inverting/noninverting switched-capacitor techniques. These techniques require the use of an opamp in the cyclic DAC loop.

In order to see how the ternary code helps reduce the major nonlinearity at the midpoint, consider the midrange *DNL* for the unsigned binary code (corresponding to the original cyclic DAC) from Eq. 3.5. The step size in transition from code 01...11 to 10...00 is

$$\Delta V_{\text{out}} = G V_{\text{ref}} \left[r^{-1} - (r^{-2} + r^{-3} + \dots + r^{-N+1} + r^{-N}) \right], \quad (3.6)$$

which according to Eq. 2.31 results in the largest *DNL* of about $(1 - 2/r)$ of full-scale.

Value	2's Complement Binary Code					Unsigned Binary Code					Minimum <i>DNL</i> Ternary Code			
	b4	b3	b2	b1	b0	b4	b3	b2	b1	b0	t3	t2	t1	t0
15	0	1	1	1	1	1	1	1	1	1	1	1	1	1
14	0	1	1	1	0	1	1	1	1	0	1	1	1	0
13	0	1	1	0	1	1	1	1	0	1	1	1	1	-1
12	0	1	1	0	0	1	1	1	0	0	1	1	0	0
11	0	1	0	1	1	1	1	0	1	1	1	1	0	-1
10	0	1	0	1	0	1	1	0	1	0	1	1	-1	0
9	0	1	0	0	1	1	1	0	0	1	1	0	1	-1
8	0	1	0	0	0	1	1	0	0	0	1	0	0	0
7	0	0	1	1	1	1	0	1	1	1	1	0	0	-1
6	0	0	1	1	0	1	0	1	1	0	1	0	-1	0
5	0	0	1	0	1	1	0	1	0	1	1	-1	1	-1
4	0	0	1	0	0	1	0	1	0	0	1	-1	0	0
3	0	0	0	1	1	1	0	0	1	1	0	1	0	-1
2	0	0	0	1	0	1	0	0	1	0	0	1	-1	0
1	0	0	0	0	1	1	0	0	0	1	0	0	1	-1
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
-1	1	1	1	1	1	0	1	1	1	1	0	0	0	-1
-2	1	1	1	1	0	0	1	1	1	0	0	0	-1	0
-3	1	1	1	0	1	0	1	1	0	1	0	-1	1	-1
-4	1	1	1	0	0	0	1	1	0	0	0	-1	0	0
-5	1	1	0	1	1	0	1	0	1	1	-1	1	0	-1
-6	1	1	0	1	0	0	1	0	1	0	-1	1	-1	0
-7	1	1	0	0	1	0	1	0	0	1	-1	0	1	-1
-8	1	1	0	0	0	0	1	0	0	0	-1	0	0	0
-9	1	0	1	1	1	0	0	1	1	1	-1	0	0	-1
-10	1	0	1	1	0	0	0	1	1	0	-1	0	-1	0
-11	1	0	1	0	1	0	0	1	0	1	-1	-1	1	-1
-12	1	0	1	0	0	0	0	1	0	0	-1	-1	0	0
-13	1	0	0	1	1	0	0	0	1	1	-1	-1	0	-1
-14	1	0	0	1	0	0	0	0	1	0	-1	-1	-1	0
-15	1	0	0	0	1	0	0	0	0	1	-1	-1	-1	-1
-16	1	0	0	0	0	0	0	0	0	0	-	-	-	-

Table 3.1: Kobayashi's minimum *DNL* ternary code.

This large transitional error is due to the fact that less significant bits incur larger errors than the more significant ones due to the recursive multiplication nature of Eq. 3.5 (i.e. cumulative error in higher powers of r).

The ternary code attempts to use the difference between more significant bits during the transition of the MSB. More specifically, the code transition for the major carry is from $010 \dots 0c$ to $1c0 \dots 00$, for which the error for large N is

$$\Delta V_{\text{out}} \approx G V_{\text{ref}} [(r^{-1} - r^{-2}) - r^{-2}] = G r^{-1} V_{\text{ref}} \left[1 - \frac{2}{r}\right]. \quad (3.7)$$

The ternary code almost doubles the output voltage swing to about $2V_{\text{ref}}$, so the DNL_{max} is reduced to approximately $\frac{1}{4}(1 - 2/r)$ of full-scale. This substantial reduction in the largest differential nonlinearity and moving it from the midpoint by $\pm 1/8$ of the range is shown for a 10-bit cyclic DAC in Fig. 3.5. The plots indicate that there are more large DNL s (relative to the maximum) in the ternary converter than the original one, which suggests that the improvement in the INL may not be as impressive.

The integral nonlinearity of a ternary code cyclic DAC is plotted in Fig. 3.6. Despite much smaller maximum DNL s, accumulation of many of these discontinuities with the same polarity in the same area, results in peak INL values larger than 60% of the original values. This performance will be later revisited among the proposed architectures in Chapter 4.

The cyclic DAC proposed in [44] uses an opamp for the conversion which slows the process, however, quasi-passive implementation of the idea is also possible.

3.3.4 MSB First Method

The flowchart of Fig. 2.1 is not the only algorithmic conversion method. It is also possible to process the digital input starting from its MSB rather than the LSB. The so called *MSB first* (or MSBF) method was introduced by Watanabe [45, 46] and

Figure 3.5: Comparison between differential nonlinearities of the original and Kobayashi's 10-bit cyclic DACs. The errors are caused by 0.4% capacitor mismatch.

later refined by Cauwenberghs [47, 48]. The promise of this newer method is better differential linearity performance.

Cauwenberghs' algorithm is shown in Fig. 3.7. The scheme tries to avoid large *DNL* by modifying the division-by-two step. Instead of accumulating mismatch error by successively dividing the old value of the partial result by the same factor, it divides a *search range* left from the previous step. The search range passed on from one step to the next is updated according to the input bit. This ensures that the error in successive iterations is not cumulative. The conversion tree and an example for the algorithm is shown in Fig. 3.8. The method is similar to the successive approximation A/D conversion algorithm.

It can be shown that, even in the presence of component (resistor or capacitor) mismatch, the *DNL* of the MSBF algorithm is virtually zero for any resolution [47, 48]. The *INL*, however, remains as high, i.e. $0.5 - r^{-1}$. Other non-ideal effects, such as opamp offset (used in the algorithm) can cause both *INL* and *DNL*.

Figure 3.6: Integral nonlinearity of Kobayashi's 10-bit cyclic DAC compared with the original one. The errors are caused by 0.4% capacitor mismatch.

Despite their *DNL* insensitivity to mismatch, MSBF methods are not very attractive. The implementations require multiple opamps in the conversion process, which makes the circuit very large, more noisy, slower, and more power consuming. Three buffers are used in [45, 46], and 2 differential opamps (for a single ended circuit) in [47, 48]. An extra opamp is still needed for the S/H.

3.3.5 Dynamic Element Matching

Error averaging or dynamic-element-matching (DEM) techniques have been very extensively used to partially overcome the limitations in matching accuracy of VLSI components. The general idea is that since component mismatch can cause positive or negative deviation from the ideal performance depending on the value ratios, then by dynamically changing the role of critical components, one can *average out* the effect of mismatch.

Several DEM methods have been proposed for the cyclic DACs, whose brief review

Figure 3.7: Flowchart for the MSB first digital-to-analog conversion algorithm.

follows.

Complete Conversion Averaging

Due to the near perfect symmetry of the nonlinearity plots of the cyclic DACs with capacitor mismatch, it is possible to virtually eliminate the error through double conversion and averaging. In contrast to some other types of DEM techniques, this is a complete conversion averaging method (CCA).

The CCA method was first used by Mycynek [49] for cyclic converters based on resistor dividers and later applied to switched-current DACs by Leenaerts [50] and SC cyclic DACs by Rombouts [51]. The schematic and timing diagrams of this technique are shown in Fig. 3.9. Although the circuit of Fig. 3.9 (the same as that of [51]) is not stray-insensitive, it is possible to make it stray insensitive as well. Two partial

Figure 3.8: Conversion tree for the MSB first digital-to-analog conversion algorithm.

conversions are performed for each digital input word, first time using C_1 as the reference sampling capacitor and C_2 as the integrating one, and the second time vice versa. The average of these two output values is obtained by the S/H, which is then taken and kept by a second sample-and-hold.

Rombouts proves that the CCA method effectively squares the capacitor mismatch error. For example, a 0.4% mismatch can be improved to 16 ppm, equivalent to a 16 bit performance.

The only obvious drawback of this method is its two times increase in conversion time. One other issue is the effect of C_{DS} of S_3 , which can be a significant limiting factor for resolutions higher than 13 bits. Lastly, the S/H leakage for the first output (before the second one is added to it) can reduce the effectiveness of this technique.

Per-Bit Ratio Averaging

The idea of MSBF algorithm and ratio independent division-by-two have been combined to make a precise cyclic D/A converter [52].

The ratio independent divide-by-two is accomplished by storing a small amount of charge proportional to the mismatch between the main capacitors, and using it in the next phase to compensate for the error. The technique uses an opamp in the

Figure 3.9: Complete-conversion-averaging cyclic-DAC. (a) Schematic. (b) Timing diagram

converter for complete charge transfer between capacitors, and can convert one bit per two cycles (four integration phases). The residual effect of mismatch is squared in this design, thereby doubling linearity resolution. Similar ideas have also been published, but they are even more complex and larger in size [53, 54].

As mentioned before, the use of an opamp in the conversion loop reduces conversion rate significantly. Moreover, four integration phases are required in this scheme. Multiple switching phases, especially with the opamp in the loop, also increase the noise substantially. Finally this method does not seem to have any advantages over

the CCA method.

Mean-Square Error Minimization

A quasi-passive cyclic DAC with error averaging on a per-bit basis is introduced in [55], and further explored in [56]. The idea aims at reducing the mean-square error (MSE) of the output, rather than peak integral nonlinearity.

The schematic is the same as Fig. 3.9, but the timing diagram is different. The role of capacitors C_1 and C_2 is selected according to an N -bit sequence generated for each digital input. The conversion time is the same as the original cyclic DAC.

The capacitor selection sequence is generated such that the conversion error caused by mismatch is minimized according to an algorithm. It is claimed that the MSE can be minimized by a factor larger than 10 with a proper choice of algorithm, while the maximum INL remains unchanged. The only penalty in this solution seems to be the extra digital hardware, no estimate of which is available.

Spectral Shaping of Mismatch Error

The mismatch error (noise) can be modulated by some sequence to change its spectrum [35]. The idea of noise shaping, which comes from oversampling modulators, has been widely applied to the component mismatch error in multi-bit oversampling converters.

In contrast to the other solutions, the emphasis here is on improving the overall signal quality as opposed to optimizing performance on a per-sample basis. If the conversion error is varied from one sample to the next in such a way that most of the error (noise) power is made uncorrelated to the signal (randomized) and moved to higher frequencies (close to $f_s/2$), the signal-to-noise+distortion ratio in the band of interest may be increased. For this technique to be effective, some degree of oversampling of the signal is necessary.

The method suggested in [35], uses the same analog circuit as Fig. 3.9, but choice of the sampling capacitor changes for each bit and each sample according to a special scheme. The manner in which the capacitors are chosen is optimized in order to minimize the low frequency noise. The $\Sigma\Delta$ loop proposed for this purpose is a third order noise shaper, and a ROM is used to hold the selection sequence based on the input and the integrated error. The exact design is not revealed, but it is claimed that the converter can achieve a 16 bit *SNR* with oversampling ratio of 16.

The digital control loop seems fairly large, but the need for a low-pass filter may be a more important disadvantage. The converter is suitable for slow signals, since oversampling ratio (say 16) is on top of the number of cycles needed for each conversion (another 16, or 256 total). The idea does not appear to be practical for pipelined converters, since the mismatch error is spread across many stages, and changing the role of capacitors in most pipelined architectures is not possible.

3.4 Conclusion

The enhancements to the basic structures of the algorithmic DACs presented in this chapter address some of the issues with these type of converters. They aim to make algorithmic DACs practical circuits, with some advantages over the other types of D/A converters.

The main advancement in design of the quasi-passive cyclic DAC, so far, is the stray insensitive topology. This is an essential upgrade for this converter, but unfortunately the (less than excellent) implementation examples do not reflect that. However, some other suggested improvements are not very practical, are too slow, and/or dissipate too much of power.

As will be shown in the following chapters, it is possible to improve the performance of the algorithmic DACs even further, and make them viable alternatives for

many applications.

Chapter 4

Advanced Cyclic DAC

The cyclic digital-to-analog converters of Chapter 3 can be further improved. The first major improvement proposed here is the use of a bipolar (sign-magnitude) architecture, through which an extra bit of linearity is obtained. The other enhancements suggested include the use of differential architecture (for better linearity and noise immunity), and a quasi-passive scheme for the minimum *DNL* ternary converter.

Another proposed addition to the cyclic DAC is a digital self-calibration technique which is very efficient for implementation. More details on the circuit implementation will follow in Chapter 6, and some of the detailed derivations are left for appendices.

The improvements are discussed for the cyclic DAC in this chapter, while similar ideas among others are applied to the pipelined converter in the next chapter.

4.1 Differential Bipolar Cyclic DAC

The new architecture aims at reducing mismatch-induced nonlinearity and improving its pattern. In this section, first the idea of bipolar cyclic DAC is introduced, then its shortcoming is analyzed. Finally the fully differential implementation is proposed to address the problem.

4.1.1 Bipolar Cyclic DAC Architecture

A bipolar cyclic DAC is a special case of a ternary converter in which all digits have the same sign. In other words, it is a type of sign-magnitude converter. Fig. 4.1 shows how a bipolar cyclic DAC is made using a conventional CDAC and a reference switch. S_{sign} is toggled according to the sign bit of the input data, i.e. $V_{\text{ref}+}$ is selected for positive inputs and vice versa. The rest of the input bits (i.e. magnitude) are applied to the converter itself. The converter used in this figure can be an original cyclic DAC, or preferably, the stray-insensitive one (Fig. 3.1). The reference voltages are assumed to be symmetrical about GND (i.e. $V_{\text{ref}-} = -V_{\text{ref}+} = -V_{\text{ref}}$).

Figure 4.1: Bipolar cyclic-DAC.

The input-output relationship for this DAC architecture can be written as

$$V_{\text{out}} = s G V_{\text{ref}} \sum_{n=0}^{N-1} b_n r^{n-N}, \quad (4.1)$$

where s is the sign of the digital input (± 1), $b_{N-1}b_{N-2} \dots b_1b_0$ is its magnitude, r is the conversion radix (ideally $r = 2$), and G is the gain modifier (≈ 1). With this convention, the effective number of bits in the input binary number is $N + 1$.

There are two advantages in using this architecture. First, the major *DNL* error is moved away from the midpoint to the $1/4$ and $3/4$ of range points. Secondly, since the output range is effectively doubled, the nonlinearity loses its significance by one bit. To prove these advantages, let's examine the output voltage of the converter for three consecutive codes in the middle of the range,

$$V_{\text{out}}(-1) = -G V_{\text{ref}} r^{-N}, \quad (4.2)$$

$$V_{\text{out}}(0) = 0, \quad (4.3)$$

$$V_{\text{out}}(+1) = +G V_{\text{ref}} r^{-N}. \quad (4.4)$$

The full-scale output voltage is $\pm G V_{\text{ref}} \sum_{n=1}^N r^{-n}$, hence the bipolar output voltage range of the converter is

$$V_{\text{Rout}} = 2G V_{\text{ref}} \sum_{n=1}^N r^{-n} \approx 2G V_{\text{ref}} \frac{r^{-1}}{1 - r^{-1}}. \quad (4.5)$$

The last step results from an approximation to the binomial expansion for large N . The output voltage range is doubled due to bipolar operation. The LSB value for the converter is

$$V_{\text{LSB}} = \frac{V_{\text{Rout}}}{2(2^N - 1)}, \quad (4.6)$$

which for large N can be approximated as

$$V_{\text{LSB}} \approx \frac{V_{\text{Rout}}}{2^{N+1}} \approx 2^{-N} G V_{\text{ref}} \frac{r^{-1}}{1 - r^{-1}}. \quad (4.7)$$

For values of r close to 2, $V_{\text{LSB}} \approx 2^{-N} G V_{\text{ref}}$ which is very close to $V_{\text{out}}(+1)$ as determined by Eq. 4.4. Therefore, the differential nonlinearity is not noticeable in the middle of the range anymore.

These facts are better displayed in the linearity plots of a bipolar cyclic DAC in Fig. 4.2. While the discontinuities have maintained their sizes in LSB (compare with Fig. 2.13), due to the doubled output range, one extra bit of linearity is obtained. The fact that the converter has its best behaviour at the midpoint, makes the dynamic range of the converter virtually independent of its linearity and peak *SDR*. This is a very significant advantage for this converter in many practical applications such as audio and voice.

With this remedy for the mismatch nonlinearity, and with 0.4% worst case mismatch, 10-bit linearity is now within reach. Improving linearity by one bit is a very important gain. To achieve an equivalent improvement by increasing capacitor sizes,

Figure 4.2: Nonlinearity of the bipolar cyclic DAC caused by 20% capacitor mismatch in a 7-bit converter.

one has to notice that matching improves roughly by the square root of the size. Quadrupling capacitor size, to help the linearity by one bit, increases the power dissipation by almost the same factor of 4 (except for the power needed to drive the load which may not change).

4.1.2 Effect of Reference Mismatch

In the analysis and simulation of the bipolar DAC so far, perfect matching of the reference voltages V_{ref-} and V_{ref+} was assumed. A mismatch between these voltages

creates gain (slope) mismatch between the positive and the negative parts of the transfer characteristic. The slope mismatch causes integral nonlinearity like the one shown in Fig. 4.3.

Figure 4.3: Nonlinearity of the bipolar cyclic DAC caused by reference voltage mismatch in a 7-bit converter. $V_{ref-} = -1.2V_{ref+}$.

Large integral nonlinearity of Fig. 4.3 results in even harmonic distortion. For example, a practical value of 0.5% limits the signal-to-distortion ratio to around 59 dB. This factor alone will limit the linearity to about 9 bits. The mismatch in the reference voltages comes from resistor mismatch and offset in the reference block.

With the digital (self) calibration technique, to be introduced later, one may reduce the nonlinearity caused by capacitor mismatch to around the 14-bit level, but the integral nonlinearity resulted from reference mismatch cannot be reduced by that method.

4.1.3 Differential Converter

Differential analog circuits have become increasingly popular in many applications. The main reason for their popularity is their immunity to common-mode noise. In complex analog and mixed signal circuits, significant noise energy may be coupled to any circuit block from the other ones. The most important coupling is through the power supply and reference rails. Other sources of interference include parasitic capacitive and inductive coupling, and coupling through the chip substrate. So long as the coupled noise is symmetrical with respect to the plus and minus sides of a differential circuit, it is effectively attenuated by the symmetry of the circuit. Only a fraction of the noise may appear as common-mode at the output, which will be reduced by the CMRR of succeeding stage.

Another advantage of differential architectures is doubling the signal amplitude while some component noise contributions (such as thermal and flicker noise referred to the input of an opamp) remain essentially the same. Therefore, the signal-to-noise ratio is improved. Differential circuits also tend to be more linear due to cancellation of even harmonics.

A differential implementation of the cyclic DAC is illustrated in Fig. 4.4. The minus side is just a mirror image of the plus side. While they share the same digital input, they use opposite references. The overall output is obtained by subtracting the output of the minus side from that of the plus side before the sample-and-hold block. The S/H is preferably a differential circuit itself.

This differential DAC has a special advantage in addition to the ones mentioned above for general differential analog circuits, which is the virtual cancellation of the reference mismatch error. Although the point seems clear intuitively, a mathematical derivation will help quantifying the effect. Let's assume the inherent gain of the plus and the minus sides of the DAC are G_p and G_m respectively. Ideally $G_p = G_m = 1$,

Figure 4.4: Differential bipolar cyclic-DAC.

but due to capacitor mismatch these gains may have slight errors. The slope of the input/output transfer characteristics of the plus and the minus sides for positive sign is then $G_p V_{\text{ref}+}$ and $G_m V_{\text{ref}-}$ respectively. The overall slope of the converter (after S/H) for positive inputs can be written as

$$S_p = G_p V_{\text{ref}+} - G_m V_{\text{ref}-}. \quad (4.8)$$

Similarly, the negative slope is

$$S_n = G_p V_{\text{ref}-} - G_m V_{\text{ref}+}. \quad (4.9)$$

Ideally $S_p = -S_n$, and no distortion is caused by slope mismatch. The exact slope mismatch is

$$\Delta S = S_p + S_n = (G_p - G_m)(V_{\text{ref}+} + V_{\text{ref}-}). \quad (4.10)$$

This mismatch is less than the single-ended mismatch of $V_{\text{ref}+} + V_{\text{ref}-}$ by $G_p - G_m$. Since G_p and G_m are very close, the effect of reference mismatch has been substantially reduced. Assuming a practical value of 0.5% for gain and reference mismatches, the resultant linearity is better than 16 bits (*THD* of about -105 dB).

Another advantage of the differential architecture for the cyclic DAC is the reduction of the capacitor nonlinearity error. As discussed in 2.3.7, first-order nonlinearity of poly-to-poly capacitors can be eliminated by splitting the capacitors and putting them in parallel top-to-bottom. The differential architecture is a natural method of using this principle. Using identical circuits for the plus and the minus sides means when the top plate of the capacitor is positive with respect to the bottom plate in the plus side, it is negative in the minus side. Therefore, while the plus-side capacitors may become larger by the applied voltage, the minus-side ones will be smaller. Of course this cancellation is effective only for the linear term in the CV relationship (first order nonlinearity), the quadratic term is not helped (the quadratic term is hardly noticeable).

The differential cyclic DAC should have a common-centroid layout [16, p. 476] to help the matching of the capacitors, and thereby improve the linearity of the converter. While it is quite possible to have a common-centroid layout for the single-ended cyclic DAC too, due to the inevitable split in the sampling and integrating capacitors in the differential architecture, this good design practice is naturally enforced.

4.2 Quasi-Passive Minimum *DNL* Ternary Converter

The cyclic converter proposed by Kobayashi in [57, 44] uses an opamp in the conversion loop to achieve stray insensitive divide-by-two and addition. He also uses a sample-and-hold in the conversion loop. As mentioned before, use of opamps in the conversion loop has three major disadvantages: lower speed, higher noise, and higher power consumption.

In the CMOS technology, the highest achievable integration speed for an opamp is usually less than $1/3$ of the settling speed for a switch and capacitor only circuit.

Therefore, cyclic DACs with opamp in the loop are much slower than the quasi-passive ones.

The opamp used in the conversion loop of a cyclic DAC has to be many times faster than the S/H opamp. Especially with the use of two integrating capacitors (section 3.1), or two interleaved cyclic DACs sharing the same S/H (to be introduced in Section 5.8), the S/H has one whole conversion cycle to settle. A conversion cycle has N clock cycles (N is the number of bits), and each cycle has two phases, hence, the opamp in the loop has to settle $2N$ times faster than the S/H (opamp integrates in one phase only, and assuming equal clock phase times). Very short settling time requires very high bandwidth for the opamp in the loop and that means an increase in noise power at the output due to aliasing caused by the sampling mechanism (folding back). Using another S/H in the loop (as per [44]) exacerbates the problem.

Higher speed opamps needed inside the conversion loop dissipate more power, thus, Kobayashi's design is expected to require much more power than the QP CDAC. Instead, the QP CDAC has the advantageous ability of using more power, not for speed (because the speed requirement is very relaxed), but to improve the noise performance.

With these many advantages for the quasi-passive cyclic DACs, a QP scheme for the Minimum DNL Ternary Converter (QPM DTC) is proposed. The analog section of this converter is the same as the quasi-passive bipolar CDAC of Fig. 4.1, the difference is only in the digital controls for the switches. In the QPM DTC scheme, the sign is on a per-digit basis, i.e. if a current digit being processed is a +1, $V_{\text{ref}+}$ is chosen, and if it is -1, $V_{\text{ref}-}$ is used. If the current digit value is 0, the input sampling capacitor is discharged to ground, same as before. As will be discussed in Chapter 6, using complementary transistors, S_{sign} is implemented as a part of the cyclic DAC itself. Similar to the bipolar cyclic DAC, in order to avoid the significant effect of the reference mismatch on linearity, a differential architecture must be used for QPM DTC

as well.

According to simulation, in comparison with bipolar cyclic DAC, for the same matching accuracy, minimum *DNL* ternary converter has a higher *INL* (0.62 LSB versus 0.5 LSB), but a lower *DNL* (0.5 LSB versus 1 LSB).

Figure 4.5: Comparison between the nonlinearity of the quasi-passive minimum *DNL* ternary converter and bipolar cyclic DAC. 10 bit converters with 0.4% capacitor mismatch is assumed.

The QPMDTC method seems superior to the bipolar CDAC, with the exception of higher *INL* and more complicated digital section, however, it may be more sensitive to some parasitics because of frequent switching of the reference voltages during

conversion. Another implementation aspect is the larger settling time required for the minimum *DNL* converter compared with the bipolar one, due to larger transient swings (from $V_{\text{ref}+}$ to $V_{\text{ref}-}$ instead of $V_{\text{ref}+}$ or $V_{\text{ref}-}$ to 0). To achieve the same settling speed, larger switches must be used for the QPMDTC.

4.3 Symmetrical Cyclic DAC

The stray insensitive cyclic DAC of Fig. 3.1 as proposed in [1], is not quite symmetric for charge redistribution between the capacitors. Complete symmetry is possible only if the integrating capacitor has a similar set of switches as the sampling one. Any imbalance between the two sides contributes to mismatch-induced nonlinearity.

To remedy the circuit asymmetry, switches can be added to the integrating capacitor as shown in Fig. 4.6. These extra switches may be only dummies for maximizing the matching accuracy, or depending on the overall architecture, may have other functions as well. When used as dummies, S_{1R} is always open, but S_{2R} which is closed during conversion, may be opened for the S/H phase.

Figure 4.6: Single-ended view of the symmetrical stray-insensitive cyclic digital-to-analog converter.

With all the extra switches added to the circuit, it is possible to implement per-bit and/or complete-conversion averaging schemes discussed in Chapter 3. Another

advantage of these switches is minimizing digital circuitry needed for a calibration scheme introduced later in this chapter.¹

4.4 Sample-and-Hold

At the output of the stray-insensitive cyclic DAC (Fig. 3.1) a sample-and-hold converts the charge stored on node N2 to a voltage across $C_{S/H}$. Although it is possible to design this S/H to avoid the zeroing phase, nonetheless for the reasons that will be discussed shortly, the output of this stage cannot be used as the continuous-time output of a high-linearity DAC. A second sample-and-hold circuit is required to produce a high linearity continuous-time output (Fig. 4.7). In the study of sample-and-hold architectures that follows, the circuits are assessed based on their application in each of the stages, i.e. only for discrete-time performance in the first stage, or both discrete-time and continuous-time behaviour for the second stage.

Figure 4.7: Block diagram of a quasi-passive stray-insensitive algorithmic DAC together with its sample-and-holds indicating Discrete-Time (DT) and Continuous-Time (CT) linearity issues.

Single-Ended Opamp Representation

Throughout this chapter and the rest of this thesis, a simplified single-ended representation of opamps is used in the schematic diagrams. The simplified representation, shown in Fig. 4.8 (a), can represent a single-ended opamp with its positive input grounded, as in Fig. 4.8 (b), or one side of a differential opamp, i.e. Fig. 4.8 (c).

¹This issue will be explained in Section 4.5.2.

Figure 4.8: Simplified single-ended opamp representation. (a) simplified symbol. (b) single-ended equivalent. (c) differential equivalent.

4.4.1 Sample-and-Hold Architectures

The first and the second S/H stages may use different architectures. Various schemes have to be assessed according to their complexity, speed, and noise performance.

First Architecture

The traditional S/H design was shown in Fig. 3.1 [9], and its simplified view is redrawn in Fig. 4.9 which only includes the components relevant to the S/H operation. This scheme uses a switch to discharge the holding capacitor before sampling a new input. Therefore, a reset phase is required in each conversion cycle. If two integrating capacitors are used in the cyclic DAC (as in Fig. 3.2) the transfer and hold phases can be the same.

Use of a reset phase in this architecture is a disadvantage. On the other hand, since the reset switch S_R removes any memory of the past in the S/H, the circuit has a flat discrete-time frequency response. The gain of this S/H design is $\frac{C_S}{C_H}$ and is adjustable.

It is possible to remove only a part of the charge on C_H in the first phase (which will no longer be *reset*) by a simple modification. In order to do so, a discharged capacitor can be placed in parallel with C_H during the first phase, instead of the reset switch S_R [58, p. 395]. This will allow IIR filtering function in the S/H. If this filtering is desired, however, one of the following architectures will be more suitable.

Figure 4.9: Single-ended view of the traditional (first) architecture for a S/H. (a) Schematic. (b) Timing diagram.

Second Architecture

Another sample-and-hold design is shown in Fig. 4.10.² In this design, some of the existing charge on the holding capacitor C_H is *neutralized* by the feedback path, and the charge for a new sample is transferred to it. The inverting block is not actually required in a differential implementation, since the feedback can be taken from the opposite side.

If $C_{FB} = C_H$ the neutralization of the existing charge on C_H from the previous sample is complete and the circuit has no memory (all-pass frequency response). If a low-pass function is desired, $C_{FB} < C_H$ may be chosen. The frequency response of

²The need for delayed clock phases to avoid nonlinearity caused by charge injection is ignored in this diagram as well as all the other ones in this chapter, for the sake of clarity. This issue is discussed in details in Chapter 6.

Figure 4.10: Second architecture for a S/H. (a) Schematic. (b) Timing diagram.

this circuit is derived in a later section.

This architecture has the advantage of no extra (discharge) phase compared with the previous architecture.

If this architecture is used in the second S/H stage, large linear resistors may be placed in series with C_S and C_{FB} in the transfer phase to improve the continuous-time linearity. For the same reason, and also to improve DC gain, a smaller linear resistor may be put in series with C_{FB} during the hold phase as well.

Third Architecture

The last architecture for the sample-and-hold, as shown in Fig. 4.11, was introduced as a *direct transfer SC integrator* [59], and has been used in the past as a discrete-time to continuous-time converter [58, p. 396]. However, its use as a sample-and-hold in

the quasi-passive pipelined DAC, and a detailed analysis of its frequency response and noise are explored here.

Figure 4.11: Third architecture for a S/H. (a) Schematic. (b) Timing diagram.

In this approach, the bottom plate of the sampling capacitor is charged to the input voltage, while its top plate is held at the ground level in the first phase. During the second phase (transfer), the top plate is connected to the input of the opamp which also sits close to the ground level (virtual ground), and the charge on both capacitors is shared by closing another switch between the bottom plates of C_S and C_H . The charge required for changing the voltage on the holding capacitor C_H , is supplied by the sampling capacitor C_S , not by the opamp. The opamp's output only has to provide the required charge difference for the parasitic capacitance at its output, and also drive any (resistive) load.

This method of S/H, similar to the second architecture, does not require a reset phase. Compared with the second design, this architecture does not need the feedback path to reduce the charge existing on the holding capacitor from the previous cycle,

however, it cannot have a flat frequency response.

When this design is used in the second S/H stage, large linear resistors may be added in series with C_S during the transfer phase to improve the continuous-time linearity (Fig. 4.24). The effect of these resistors on the frequency response, noise performance, and linearity of the S/H will be discussed in the following sections.

Other S/H Architectures

Other variations of the S/H architecture can be used to modify its filtering properties. In other words, the two S/H stages can be considered as two stages of an SC filter, and by employing proper feedback and feed-forward paths, the desired response may be obtained. It should be emphasized, however, that the second stage must have a linear continuous-time response, or an additional discrete-time to continuous-time stage will be necessary.

The transfer function of the sample-and-hold architectures, and their noise performance are compared in the following sections.

4.4.2 Sample-and-Hold Frequency Response

The S/H architectures explained in the previous section are essentially switched-capacitor filters. As such, these S/H circuits have certain discrete-time frequency response. Also, when these architectures are used in the second S/H stage, they introduce some continuous-time filtering as well.

The optimal transfer function of the S/H depends on the overall system design in any given application. For example, if attenuation of the residual images leftover after insufficient digital interpolation filtering is desired, a low-pass function in the S/H is preferable. However, Low-pass filtering in the S/Hs is a mixed blessing, because one must also take into account the droop caused by these filters in the bandwidth of interest.

Since the frequency response of the S/H is mainly a function of capacitor ratios, which are relatively accurate, it may be compensated for in the digital domain. For example, in DSL applications, the modulator can be modified easily to preadjust the relative amplitudes of carriers in each bin of the DMT signal to compensate for the S/H droop.

Often a continuous-time LPF follows the D/A to attenuate the image amplitudes around f_s (and its integral multiples). It goes without discussion that the discrete-time response of the S/H *cannot* attenuate those images. It is only the continuous-time filtering effects in the second S/H that helps reducing the images around f_s (and its multiples). The principle CT response of the second S/H is a sinc filter, known as zero-order-hold [60, pp. 123-125]. In this section, only the DT response of the S/H architectures are examined, which are similar for both the first and the second sample-and-hold stages. The frequency response of the DT-to-CT conversion is discussed later.

Another implication of the choice of the S/H transfer function is the output noise, as will be discussed in the next section.

Derivations of all the transfer functions are included in Appendix B. Only the results, and short conclusions are presented in this chapter.

First Architecture

Since the reset switch S_R discharges the holding capacitor before each new sample, this architecture (Fig. 4.9) has a flat frequency response of a single sample delay, i.e. z^{-1} .

Second Architecture

The transfer function for the complete settling assumption at the end of the transfer phase, as derived in Appendix B, is

$$H(z) = \frac{az^{-1}}{1 - (1 - b)z^{-1}}, \quad (4.11)$$

where

$$a = \frac{C_S}{C_H}, \quad (4.12)$$

and

$$b = \frac{C_{FB}}{C_H}. \quad (4.13)$$

The above first-order IIR filter can have a low-pass, a high-pass, or an all-pass magnitude response depending on the values of a and b coefficients. The magnitude of the frequency response of the DT filter in this S/H architecture, for the cases of $C_S = C_{FB} = C_H$, $C_S = C_{FB} = 0.5C_H$, and $C_S = C_{FB} = 1.5C_H$, are shown in Fig. 4.12.

Figure 4.12: Magnitude frequency response of the second S/H architecture for various capacitor ratios. (a) $C_S = C_{FB} = C_H$. (b) $C_S = C_{FB} = 0.5C_H$. (c) $C_S = C_{FB} = 1.5C_H$.

Figure 4.13: Simplified view of the transfer phase for the second S/H architecture. The total resistance in series with C_S and C_{FB} (including any linear resistor added for CT linearity) are represented as R_S and R_{FB} respectively.

With the addition of large linearizing resistors in series with the switches in the second S/H stage (Fig. 4.24), the charge transfer between C_S or C_{FB} and C_H is significantly incomplete. The filter coefficients a and b in Eq. 4.11 should be modified to

$$a' = \frac{(1 - e^{-\frac{\sigma T}{\tau_S}})C_S}{C_H}, \quad (4.14)$$

and

$$b' = \frac{(1 - e^{-\frac{\sigma T}{\tau_{FB}}})C_{FB}}{C_H}, \quad (4.15)$$

respectively. The symbols $\tau_S = R_S C_S$ and $\tau_{FB} = R_{FB} C_{FB}$ represent the time-constant associated with the sampling and the feedback capacitor circuits during the transfer phase as shown in Fig. 4.13. Appendix B contains the detailed study of this matter. Fig. 4.14 shows the effect for a few values of the settling factor $1 - e^{-\frac{\sigma T}{\tau}}$ assuming $\tau = \tau_S = \tau_{FB}$, and $C_S = C_{FB} = 0.5C_H$.

The transfer functions discussed so far are only the discrete-time responses. The effect of DT-to-CT conversion should also be added to them if the architecture is used in the second S/H stage. The detailed treatment of this subject can be found in Appendix B and will be briefly reviewed in a following section on the second S/H

Figure 4.14: Effect of incomplete settling on the magnitude frequency response of the second S/H architecture with $C_S = C_{FB} = 0.5C_H$ and various settling factors.

stage.

Third Architecture

For this scheme (Fig. 4.11), the DT transfer function for complete settling (first S/H stage) according to Appendix B is

$$H(z) = \frac{az^{-1}}{1 + a - z^{-1}}, \quad (4.16)$$

with a as defined in Eq. 4.12. This is a first-order low-pass IIR filter.

Including the effect of finite settling at the end of the transfer phase results in the DT transfer function for the second S/H stage as

$$H(z) = \frac{a(1 - e^{-\alpha T/\tau})z^{-1}}{1 + a - (1 + ae^{-\alpha T/\tau})z^{-1}}, \quad (4.17)$$

in which

$$\tau = R_S \frac{C_H C_S}{C_H + C_S}. \quad (4.18)$$

In this time-constant, R_S is the *total* resistance in series with the sampling capacitor C_S during the transfer phase (including the switches and the linearizing resistors — Fig. 4.24).

Figure 4.15: Magnitude frequency response of the third S/H architecture with $C_S = 2C_H$ and various settling factors $(1 - e^{-\frac{\alpha T}{\tau}})$.

The magnitude of the frequency response of the filter for the case of $C_S = 2C_H$, and various settling factors $(1 - e^{-\frac{\alpha T}{\tau}})$ is shown in Fig. 4.15 (the case of $C_S = C_H$ for this architecture gives the same response as $C_S = C_{FB} = 0.5C_H$ in Fig. 4.14 for the second architecture).

It should be mentioned again that the complete response of the second S/H stage also includes the DT-to-CT transfer function which is discussed in a later section.

4.4.3 S/H Noise

The digital signal arrives at the input of the DAC with its own quantization noise. It is easily proven that for high-resolution converters (even for number of bits larger than 6), and *busy* signals (changing through many quantization levels randomly), the

quantization noise is given by [60]

$$\sigma_q^2 = \frac{\Delta^2}{12}. \quad (4.19)$$

where Δ is the size of the least significant bit (LSB) at the output. This quantization noise is spread over the 0 to $f_s/2$ bandwidth (single-sided frequency axis convention). In quasi-passive algorithmic converters it is relatively easy to add to the number of input bits; in the cyclic design the conversion speed is reduced slightly due to extra cycles, and in the pipelined DAC power dissipation is increased negligibly due to extra stages. Therefore, it is recommended to have the input resolution high enough to make the input quantization noise insignificant relative to the noise and nonlinearity produced in the DAC. Carrying two extra bits is usually sufficient.³

Various noise sources contaminate the output signal of the DAC (see Fig. 4.16). The output of the DAC core arrives at the input of the first S/H together with its own thermal (Θ/C) noise. The first S/H adds its contribution of noise, and then all of that is sampled by the second S/H. The sampling process folds back all the sampled noise power to between 0 and $f_s/2$ (positive-only frequency convention). Up to this point, all the noise is discrete-time (only the sampled values matter), however, the second S/H stage adds some continuous-time noise to the output signal. The noise component of the reference voltages is not attributed to the DAC. The reference noise is usually made very low using heavy low-pass filtering.

Figure 4.16: Noise contributors to the DAC system.

In order to improve the signal-to-noise ratio of the converter, one has to minimize all the significant noise components in the circuit. Hence it is imperative to find

³If the input quantization noise is 4 times smaller than the DAC noise, it increases the overall noise level by only 0.26 dB.

the best architectures for the sample-and-holds to optimize the SNR for the lowest possible power.

Various noise sources in the S/H circuits and their contributions to the output noise are explored in Appendix C. In the following sections the results of Appendix C are reviewed and used for comparison between different architectures.

First Architecture

Only the first S/H stage can use this design (having a reset phase does not allow for an acceptable continuous-time output quality), therefore, only the DT noise performance is analyzed.

Figure 4.17: Schematic for the noise analysis on the first S/H architecture.

The schematic diagram of the circuit including an input referred noise voltage source for the opamp (V_{na}) is shown in Fig. 4.17. The familiar clock phase terminology is used for simplification. Here ϕ_1 represents the reset phase, and ϕ_2 corresponds to the transfer phase. Since, as proven in Appendix C, the circuit has a better performance with only two phases, i.e. without a hold phase (as opposed to the original design [9]), only this case is considered here. In this case, the next S/H stage samples the output during the transfer phase (ϕ_2), which is also the time reference point for the discrete-time signals.

The power spectral density of noise at the output of the stage can be divided in two sections: Within Loop-Bandwidth (WILBW) and Without (outside) Loop-Bandwidth (WOLBW). Within the bandwidth of the feedback loop around the opamp, the opamp can be modeled as ideal and usual switched-capacitor circuit analysis applies. Beyond the loop bandwidth, the feedback loses its effectiveness and in the resulting open-loop circuit the noise has to be considered as referred to the output. The border between the WILBW and WOLBW noise is conveniently set at the -3-dB loop-bandwidth, although this may not be quite accurate in some cases.

The input capacitance of the opamp and the parasitic ones on that node are lumped into C_I . The transfer function for the input referred noise of the opamp (within its loop bandwidth) is found to be

$$\frac{V_{out}(z)}{V_{na}(z)} = \left(1 + \frac{C_S + C_I}{C_H}\right) - \frac{C_I}{C_H} z^{-\alpha}, \quad (4.20)$$

where α is the transfer phase duty cycle. This is a first-order high-pass FIR filter or leaky differentiator. The magnitude response of this transfer function is shown in Fig. 4.18 for a typical case of $\alpha = 0.5$ and $C_S = C_I = C_H$.

If the power of noise outside the loop-bandwidth (WOLBW) at the output of the opamp is significant, it should be integrated from the -3-dB loop-bandwidth to ∞ and distributed over 0 to $f_S/2$ range evenly, in addition to the noise represented by V_{na} and Eq. 4.20.

While in the first look the magnitude of the noise transfer function in Fig. 4.18 seems to be larger at high frequencies, due to the fact that the second S/H stage samples the output of this circuit at f_S (remember this architecture can only be used in the first S/H stage), all the noise power around f_S and its harmonics fold back to the baseband (around 0). Other duty-cycle values may move the peak from f_S .

Two other noise sources contribute to the output noise. The thermal noise of the on-resistance of the reset switch ($\frac{\Theta}{C_H}$) is sampled on C_H when the switch opens, and

Figure 4.18: Magnitude of the transfer function for the input referred noise of the opamp in the first S/H architecture with $\alpha = 0.5$ and $C_S = C_I = C_H$.

remains there to be added to the input sample in the next phase. The thermal noise of the sampling switch S_S goes through the transfer function of the circuit (continuous-time noise) before appearing at the output to be sampled by the next stage. The noise power for this component is:

$$\overline{v_{R_{on}}^2} = 2\pi \frac{C_S}{C_H} \Theta R_{on} B_{lp}, \quad (4.21)$$

where B_{lp} is the -3-dB loop-bandwidth around the opamp, and R_{on} is the series on-resistance of the sampling switch(es). It is clear from Eq. 4.21 that, unlike most SC noise contributors, reducing R_{on} lowers the noise.

All three noise contributors in this circuit are independent, and their powers should be added at the output.

Second Architecture

When used in the first S/H stage, the DT noise of this circuit should be considered. For the second S/H application the CT noise, which includes direct and sampled-and-

held noise, has to be taken into account.

Figure 4.19: Simplified schematic diagram for the discrete-time noise analysis on the second S/H architecture.

Discrete-time noise Fig. 4.19 is the simplified schematic of this architecture for DT noise analysis. This architecture's noise transfer function for the input referred noise of the opamp is derived in Appendix C as

$$\frac{V_{out}(z)}{V_{na}(z)} = \frac{C_H + C_S + C_{FB} + C_I - (C_H + C_I)z^{-\frac{1}{2}}}{C_H - (C_H - C_{FB})z^{-\frac{1}{2}}}. \quad (4.22)$$

assuming a 50% duty cycle for the S/H clock.

The magnitude of the noise transfer function for a typical case of $C_S = C_{FB} = C_I = C_H$ is plotted in Fig. 4.20. The high frequency gain is even larger than the first architecture. Also, as before, one has to keep in mind that the noise around f_s is folded back to the baseband if there is a sampling process after this circuit.

The thermal noise of the switches in the transfer phase appear at the output as a CT noise which is band-limited by the opamp. In the hold phase, however, they are sampled-and-held and the opamp's bandwidth cannot help. For this reason, which is similar to the first architecture, it is better for the next stage to sample the output during the transfer phase.

Figure 4.20: Magnitude of the transfer function for the input referred noise of the opamp in the second S/H architecture with $C_S = C_{FB} = C_l = C_H$.

The CT noise power from the switches at the output during ϕ_2 is

$$\overline{v_{R_{on}}^2} = 2\pi \frac{C_S}{C_H} \Theta R_{onS} B_{lp} + 2\pi \frac{C_{FB}}{C_H} \Theta R_{onFB} B_{lp}, \quad (4.23)$$

where B_{lp} is the loop bandwidth around the opamp, and R_{onS} and R_{onFB} are the resistance in series with C_S and C_{FB} during ϕ_2 respectively.

Assuming $C_{FB} = C_H$, the sampled noise during ϕ_2 is eliminated in the next transfer phase altogether, and only the noise sampled on C_{FB} in ϕ_1 (consisting of switch thermal noise and opamp noise) can be present at the output for the next stage.⁴ This sampled noise is generally shaped by the circuit's transfer function (see Appendix C), but for $C_{FB} = C_H$ it is almost white across 0 to $f_S/2$. The total power of the switch thermal noise is Θ/C_H , to which the output referred noise of the opamp should be added. Formulas for the sampled noise in the case of $C_{FB} \neq C_H$ can be found in Appendix C.

⁴The thermal noise sampled on C_S in ϕ_1 is considered as the noise of the DAC core, and is considered separately.

The overall noise power at the output (analyzed so far) is the sum of the three components, namely the opamp noise, R_{on} noise given by Eq. 4.23, and the sampled thermal noise (Θ/C_H for $C_{FB} = C_H$). On top of these, if the WOLBW noise is substantial, it must be included in the calculations as well. Similar to the first architecture, when this architecture is used in the first S/H stage, there is a direct sampling of this noise at the output by the next stage during the transfer phase. Since the very high frequency out-of-band noise of the opamp is highly undersampled, the samples can be conservatively considered uncorrelated, and the noise powers are added.

Continuous-time noise The second S/H stage provides a continuous-time output for the succeeding stage. Included in this output is the noise of the previous stages received as a DT input (which passes through the same transfer function as the input signal), and the noise of the stage itself which is continuously present at the output. The continuous-time nature of this noise prevents suffering from aliasing of the out-of-band noise due to sampling (which occurs in the previous stage), thereby reducing the noise in the most important frequency range, i.e. the baseband ($< f_s/2$).

There are two kinds of CT noise generated in a S/H, direct and sampled-and-held. The direct noise is the one that reaches the output from its source while it is being generated. The sampled-and-held noise, on the other hand, is the stored (frozen) noise at the output in a clock phase (or a cycle) from a noise sample at a prior time.

The large linearizing resistors used in the second S/H stage are the main contributors to this stage's overall baseband noise. In the second architecture, these resistors are placed in series with both C_S and C_{FB} (at least during ϕ_2) to reduce the speed of transients and help the continuous-time linearity of the opamp. The total resistances in series with C_S and C_{FB} in ϕ_2 are denoted by R_S and R_{FB} respectively.

The thermal noise related to the input sampling capacitor C_S and its associated switches in ϕ_1 (when the output of the first stage is being sampled) is also included

in the CT noise calculations because it applies to the second S/H stage.

The complete analysis of the noise in this architecture for general conditions is relatively involved. Since the main advantage of this architecture compared to the third one is the possibility of a flat frequency response, only this special case is analyzed in Appendix C, and the results are recaptured here. Further, a DC gain of 1 ($C_S = C_{FB} = C_H$) is also assumed here.

The thermal noise of the opamp referred back to its input can be expressed in terms of an imaginary equivalent resistance R_{na} . Because it is very low-pass in nature, the flicker ($1/f$) noise should be treated differently. This noise varies so slowly that the sum of its direct and sampled-and-held components can be viewed through the DT response of the circuit.

The direct noise density due to the opamp at the output can be overestimated as

$$\psi_{dna\theta} = 4 \left[(1 - \alpha) \left(\frac{C_H + C_I}{C_H} \right)^2 + \alpha \left(\frac{3C_H + C_I}{C_H} \right)^2 \right] \Theta R_{na}. \quad (4.24)$$

The density of the sampled-and-held thermal noise of the opamp due to disconnection of C_S at the end of ϕ_2 is given by

$$\psi_{shnaC_S\theta}(f) = \begin{cases} 4\Theta R_{na}(1 - \alpha)^2 \text{sinc}^2\left(\frac{(1-\alpha)f}{f_s}\right) & \frac{1}{4R_S C_S} < \frac{f_s}{2}, \\ 4\Theta R_{na}\left(\frac{1}{2R_S C_S f_s}\right)(1 - \alpha)^2 \text{sinc}^2\left(\frac{(1-\alpha)f}{f_s}\right) & \frac{1}{4R_S C_S} \geq \frac{f_s}{2}, \end{cases} \quad (4.25)$$

and a similar expression can be written for C_{FB} by replacing R_S with R_{FB} .

The flicker noise of the opamp sees a gain of 2 before reaching the output, which is the same as the DT gain of the circuit for the input referred noise of the opamp at DC.

The combined direct and sampled-and-held noise of the resistors at the output has a flat density in the baseband equal to

$$\psi_{br} = 4\Theta R_S + 4\Theta R_{FB}, \quad (4.26)$$

and the sampled-and-held out-of-band noise of the R_S resistor aliased back to the baseband can be approximated as

$$\psi_{\text{sh}R_S}(f) = \begin{cases} 0 & \frac{1}{4R_S C_S} < \frac{f_S}{2}, \\ 4\Theta R_S \left(\frac{1}{2R_S C_S f_S} - 1 \right) (1 - \alpha)^2 \text{sinc}^2 \left(\frac{(1-\alpha)f}{f_S} \right) & \frac{1}{4R_S C_S} \geq \frac{f_S}{2}. \end{cases} \quad (4.27)$$

A similar noise density also comes from R_{FB} .

The thermal noise of the resistors sampled on C_S and C_{FB} at the end of ϕ_1 and transferred to the output in the next phase is

$$\psi_{\text{sh}C}(f) = 4 \frac{\Theta}{f_S C_H} \text{sinc}^2 \left(\frac{f}{f_S} \right). \quad (4.28)$$

Third Architecture

As with the second architecture, the DT and CT noise are considered separately, and are relevant to the first and the second S/H stages respectively.

Figure 4.21: Simplified schematic diagram for the discrete-time noise analysis on the third S/H architecture.

Discrete-time noise Considering Fig. 4.21 as the schematic diagram for this architecture, the transfer function for the input referred noise of the opamp in the third architecture is given by

$$\frac{V_{\text{out}}(z)}{V_{\text{na}}(z)} = \frac{C_H + C_S + C_I - (C_H + C_I)z^{-1}}{C_H + C_S - C_H z^{-1}}. \quad (4.29)$$

The magnitude of this transfer function is plotted in Fig. 4.22 for the case of $C_S = C_I = C_H$. For ease of comparison with the other architectures, the frequency axis extends all the way to f_S (according to Eq. 4.29, the transfer function is symmetrical around $f_S/2$).

Figure 4.22: Magnitude of the transfer function for the input referred noise of the opamp in the third S/H architecture with $C_S = C_I = C_H$.

When this S/H circuit is used in the first S/H stage, the second stage samples the output during the transfer phase. This sample includes the thermal noise of R_{on} for the switches that are closed in ϕ_2 . This noise power is

$$\overline{v_{R_{on}}^2} = 2\pi \left(\frac{C_S}{C_H + C_S} \right)^2 \Theta R_{on} B_{lp}, \quad (4.30)$$

in which B_{lp} is the loop bandwidth (in Hz) around the opamp.

Noise of R_{on} sampled on C_H has a reduced power at the output given by

$$\overline{v_{SC}^2} = \frac{(C_H + C_I)\Theta}{(C_S + 2C_H)(C_S + C_H + C_I)}. \quad (4.31)$$

The complete DT noise is the sum of three noise contributions, i.e. the opamp noise (Eq. 4.29), and the thermal noise given by Eq. 4.30 and Eq. 4.31. As in the

previous two architectures, the WOLBW noise may also have to be taken into account if its value is considerable. Appendix C has the details (Eq. C.7).

Continuous-time noise Following a similar analysis as in the case of the second architecture, the density of the thermal noise of the opamp at the output can be expressed as

$$\psi_{\text{dna}\theta} = 4 \left(\frac{C_H + C_I}{C_H} \right)^2 \Theta R_{\text{na}}, \quad (4.32)$$

in the baseband. The thermal noise density of all the resistors and switches in the baseband can be simplified to

$$\psi_r = \left(\frac{\Theta}{C_S} + \frac{\Theta}{C_{\text{eq}}} \right) \frac{2}{f_S}, \quad (4.33)$$

where C_{eq} is the series combination of C_S and C_H . The gain for the flicker noise to the output is essentially 1.

4.4.4 First S/H Stage

The purpose of the first S/H stage is to transfer the charge resulting from the conversion process to a linear capacitor and thereby create a linearly proportional output voltage. For reasons that will be discussed shortly, this voltage is then resampled-and-held by the second S/H stage to provide a linear continuous-time output for the DAC.

The first S/H can use either of the three architectures presented in the previous sections. All three noise components are smaller at the output of the third S/H architecture compared with the other two architectures. This is easily verified by observing the DT noise performance of the architectures in the previous sections. Given the advantages of lower noise and simplicity, the third architecture is chosen. The low-pass filtering in this architecture, which is very precisely adjustable through capacitor ratios, is also an additional advantage over the first architecture.

Fig. 4.23 shows the single-ended view of the symmetrical cyclic DAC together with the first S/H stage. In the output phase of the cyclic DAC, switches S_5 and S_6 are closed and all other switches are left open. During this phase, the charge stored on the nonlinear capacitance at nodes N2L and N2R is transferred to C_H , C_L , and C_R . Since the latter capacitors are linear (relative to the junction capacitors), the change in the output voltage is proportional to the accumulated charge during the conversion. The total output voltage at the end of this phase is also dependent on the initial voltage across C_H . The response of this discrete-time filter was analyzed in Section 4.4.2.

Figure 4.23: Single-ended view of the cyclic digital-to-analog converter and its first sample-and-hold stage.

As analyzed in Section 2.3.8, the thermal noise power of the switches in the cyclic DAC sampled on the output capacitor (i.e. Θ/C) is inversely proportional to the capacitor size. Using both capacitors in the cyclic DAC to transfer the charge to the S/H (as in Fig. 4.23), reduces the thermal noise power by a factor of 2 (3 dB). This is a new feature compared with the traditional cyclic DACs [9].

In this scheme it is no longer possible to have a second integrating capacitor (as in

Fig. 3.2) to interleave the conversion and S/H operations. However, it is possible to use two separate cyclic DACs sharing the same S/H. In this architecture, while one cyclic core is busy transferring its resultant charge to the S/H, another cyclic core is working on the next conversion. This proposal, called *bank-of-cyclics*, is introduced in Section 5.8, and due to its better symmetry, is more suitable than one cyclic DAC with two integrating capacitors.

If there is sufficient settling time for a complete charge transfer from the nonlinear junction capacitors, the output voltage (step) at the end of the output phase is linearly proportional to the charge resulting from the conversion process. This is the first requirement for a linear S/H. The linearity of the continuous-time output (including the transient) also depends on the transient behaviour of the circuit. Nonlinearity in the form of *INL* (affecting *THD*) may result from poor transient linearity.

It can be shown that the Continuous-Time (CT) output is linear if the area under the output voltage versus time plot (for each sample) is proportional to the input charge. This fact is quite straight forward for the DC performance metrics (i.e. *INL*, and *DNL*). Existence of nonlinear components in the circuit is one strong reason for questioning the CT linearity of the S/H. Among these components are the junction capacitance, and the switch on-resistance. However, the most important nonlinear element in this circuit is the opamp. The opamp is the slowest component of the converter and, for large signals at its input during the transient, it is very nonlinear. The *RC* time-constant of the other nonlinear devices can be made much smaller than the opamp time-constants, consequently, they can have significantly less contribution to the overall nonlinearity.

In the past, simulation accuracy has been limited for switched-capacitor circuits due to the poor charge conservation characteristics of most circuit simulators. Recently, MOS models in HSPICE (level 28) have shown significant improvement which makes it more suitable for these applications. A benchmark simulation error is re-

duced from about 1% to less than 100 ppm.

With the above simulation accuracy, pulse-area mismatches greater than 7% have been observed for the sample-and-hold. Replacing the actual opamp with a linear opamp model reduces the error to about 0.1%. Although it is possible to *linearize* the opamp to some extent, it will not be sufficient even for a high-speed 10-bit DAC.

The main method of improving the transient linearity of the opamp in the S/H, as will be discussed in more detail later for the second S/H, is to slow down the transient. Due to the presence of nonlinear junction capacitance in the transient time-constant, the transient slowdown amplifies the CT nonlinearity caused by the nonlinear junction capacitors. In other words, there is a conflict between improving the CT linearity of the opamp and reducing the CT nonlinearity caused by the junction capacitors. Therefore, a second S/H stage is required to mask the nonlinear transient behaviour of the first one.

Addition of another S/H stage is costly in terms of area, power, and noise. Nonetheless, it is the only way of achieving high linearity at high speed.

Supplementing the S/H circuit with another switched capacitor in parallel with C_H allows the use of larger reference voltages than the output voltage swing of the opamp. This means that with a gain of less than 1 in the first S/H, it is possible to use VSS as $V_{\text{ref-}}$. Alternatively, one can avoid the additional switch and capacitor and use larger references with limited digital signal at the input. Nonetheless, it is recommended to choose the analog ground level for the optimal dynamic range and if, due to lack of sufficient headroom, $V_{\text{ref+}}$ cannot be made high enough, the use of VSS as the $V_{\text{ref-}}$ may be impractical. More details on the implementation issues will follow in Chapter 6.

4.4.5 Second S/H Stage

The performance of this stage is more critical since it provides the continuous-time output of the converter. The architecture may be similar to the first stage with two major differences in the requirements.

The first major difference between the requirements for the second S/H and the first one is the need for a linear continuous-time output. This is usually achieved by avoiding nonlinear transient behaviours such as slewing, which normally implies reducing the speed of transients.

Secondly, the transients in the second S/H do not have to settle very precisely. In the second S/H, charge is transferred between linear capacitors, and incomplete transfer does not result in nonlinearity but rather a minor change in the frequency response of the circuit.

With the above differences in mind, the third S/H architecture is again the most suitable one. Generally, this architecture has the easiest transient condition for the opamp. The opamp does not have to provide the charging current to the capacitors, the charge is transferred from one capacitor directly to the other. The opamp only charges some parasitic capacitors, and provides the current to the (resistive) load. For both S/H architectures, since the top plate of the sampling capacitor is at the ground level in both phases, and except for the minor charge injection imbalance (between the differential sides), the magnitude of the transient at the input of the opamp is very small, and the opamp has its best linearity performance.

In terms of noise, the third architecture has less noise gain for the opamp (Eq. 4.32 vs. Eq. 4.24), especially for the flicker noise (1 V/V vs. 2 V/V). With regards to the resistor noise, however, even though there are two resistors used in the second architecture, and each one has almost the same noise gain to the output as the only resistor in the third architecture, the total resistor thermal noise is not necessarily

more for the former. The reason is that the values of the resistors are chosen to increase the RC time constants to a level that the opamp can handle with high linearity. For equal C_S and C_H , the equivalent time constant in the third architecture is $RC_S/2$ versus RC_S and RC_{FB} in the second one. Therefore, for the same time constants, the resistor value has to be twice as large in the third architecture, and the total thermal noise of the resistors at the output are very close.

The third architecture also has better DC gain accuracy. This is due to the fact that when the feedback capacitor in the second architecture is switched to the output of the opamp (during the hold phase) it drops the output voltage momentarily due to limited output impedance and bandwidth of the opamp. This *glitch towards ground* reduces the average output voltage (DC and baseband signal) and thus causes gain errors that are not precisely controllable. Since the opamp in the second architecture has to charge the feedback capacitor as well, it needs to consume more power too.

With the second architecture, it is possible to have fairly flat frequency response, whereas the third one is always a low-pass filter. However, the high frequency attenuation in the filter is adjustable and precise, which makes it useful in most applications.⁵ Nonetheless, if the very flat response of the second architecture is needed, its other disadvantages may be ignored. However, for the rest of this work, the third architecture is chosen for the second S/H stage.

Now that the architecture has been chosen, improvements can be made to help its continuous-time linearity. Large transients at the input of the S/H opamp can be avoided by having some additional resistors in the third S/H architecture as shown in Fig. 4.24. (As usual, for clarity, only one side of the differential circuit is shown.)

The switched-capacitor noise of the sampling circuit between the first and the second stages of the S/H contributes to the noise in the second stage. This noise

⁵Making the holding capacitor (C_H) in the third architecture very small increases the noise. Therefore, it is not recommended to reduce this capacitor value too much only to help the flatness of the frequency response.

Figure 4.24: Single-ended view of the second sample-and-hold stage.

source was included only in the continuous-time noise analysis of the S/H architectures because it is only a part of the second stage. The power of this noise, Θ/C_S , can only be reduced using larger sampling capacitors (at the cost of increased power dissipation).

Resistor R_1 has the function of band-limiting the input sampling circuit. In the previous stage (i.e. first S/H) the out-of-band noise of the (two stage) opamp may be significant compared with its in-band amount. Since, after sampling, all that noise is spread between 0 and $f_s/2$, it is possible to reduce the noise in this stage by reducing the bandwidth of the sampling switch-capacitor. Although this bandwidth may be reduced just by using a smaller switch (larger R_{on}) it is not the best solution. On-resistance of a MOS switch is more nonlinear, more process dependent, and more temperature dependent compared with linear (polysilicon) resistors. Due to good linearity of these resistors, there is less concern about incomplete settling of the voltage across the sampling capacitor C_S , however, since the transients in the first S/H stage have very large nonlinearities, this settling still has to be relatively accurate compared with the settling of the output of the second stages itself. It is given that the inclusion of R_1 does not reduce the sampled thermal noise on C_S (i.e. Θ/C_S).

Other resistors in the circuit are added to help the CT linearity of the output. In effect, all the resistors during the transfer phase appear “somewhat” in series to reduce

the transient rate of voltage change at the output of the opamp. Due to its limited internal current source supplies, the opamp has a maximum slew-rate. Constant-slope slewing is a major source of CT nonlinearity. To display the point, the area under two step-response waveforms are compared in Fig. 4.25. In this simplified plot, the input for the larger step is twice larger than the smaller one, however $A_2 = \frac{12}{7} A_1$.

Figure 4.25: Effect of slewing on continuous-time nonlinearity.

Beside the opamp, there are two other types of nonlinear elements in the circuit; on-resistance of the switches, and junction capacitors. Large switches with low values of R_{on} reduce the effect of the first nonlinearity type, but due to their large junctions, increase the contribution of the second type.

The minimum value of the total series resistance ($R_1 + R_2 + R_3 + R_4$) is determined by the requirements from the opamp, and their maximum values are limited by the amount of their thermal noise that can be tolerated. Larger resistor values also make the effect of the nonlinear junction capacitors worse. The main reason for distribution of the total series resistance among separate resistors is to allow optimization of the nonlinearity based on the distribution of R_{on} and C_j . They should also protect the output of the opamp from sudden connection of a charged junction or bottom-plate capacitors.

Resistors R_1 and R_2 are the least critical components. These resistors do not charge any nonlinear capacitors. Nodes N2 and N3 are always at the ground level. The only reason for splitting these two resistors is that during the sampling phase only a small portion of the resistance (R_1) is needed for limiting the noise bandwidth (as discussed above).

Resistor R_4 protects the opamp from sudden connection of the junction capacitance on N4, however, its size is limited by the nonlinearity caused by charging of the same junction capacitors. Similarly, R_3 is determined by the junction and bottom-plate capacitors at N1. The remainder from the total resistance required by the opamp is put in R_2 after optimizing all other values.

Excessively large resistor values increase the baseband thermal noise in the second S/H stage. According the analysis of Appendix C, the total time constant, i.e. $R_S \frac{C_S C_H}{C_S + C_H}$, should be kept below $\frac{1}{2f_s}$ to avoid this noise penalty.

The presence of large resistors in series with capacitors, effects a continuous-time low-pass filter. This filter helps in attenuating the signal images around f_s multiples. Because of incomplete settling at the end of the transfer phase due to this large time-constant, the discrete-time transfer function of the S/H architecture has to be slightly modified (see Eq. 4.17).

The complete analysis of the DT-to-CT transfer function is presented in Appendix B, the final result for this transfer function is given by

$$H_{D2C}(\Omega) = \frac{1 - e^{-\alpha T/\tau} e^{-j\Omega\alpha T}}{1 - e^{-\alpha T/\tau}} \left[\frac{-\tau}{1 + j\Omega\tau} (1 - e^{-j\Omega T}) + \frac{1}{j\Omega} (1 - e^{-j\Omega\alpha T}) \right] + \frac{1}{j\Omega} (e^{-j\Omega\alpha T} - e^{-j\Omega T}). \quad (4.34)$$

4.5 Digital Calibration

Digital calibration methods have long been used to improve the accuracy of data converters. Some of the existing schemes for cyclic converters have been discussed in Chapter 3.

Digital calibration is particularly attractive in modern technologies, where fine featured CMOS digital circuits can be used abundantly. Higher speed of operation, and lower power consumption in the new digital circuits make it an easy decision to transfer a lot of design complexity into that part of the system.

After all the improvements made to the cyclic DAC so far, the linearity of the converter still suffers from capacitor mismatch. It is hard to achieve more than 12 bits of linearity without some kind of post-manufacture calibration.

4.5.1 *DNL*-Based Calibration Method

As explained in Chapter 3, radix transformation has been used to correct the error caused by capacitor mismatch. The main issue with this kind of calibration is its complexity. The method suggested in [43] uses an A/D, a CPU, and software for calibration.

In search of a simpler scheme, it is realized from the transfer characteristics of a cyclic DAC that if the major differential nonlinearity breaks are removed from the DAC transfer characteristics, the result will be a very linear DAC. Although there are about as many nonlinear transitions in an algorithmic DAC (with mismatch) as the number of codes, most of the *DNL* values are very small and quite acceptable for a given linearity limit. Discontinuities of the transfer function are larger at more significant bit transitions (excluding sign bit in a bipolar DAC). Depending on the matching accuracy and the required linearity, only a limited number of these break points have to be cured. For this method to work, the *DNL*s have to be negative. In other words, there has to be some redundancy, i.e. the conversion radix in the cyclic DAC must be smaller than 2.

In order to remove a major *DNL* from the transfer characteristics, the value of that *DNL* must be subtracted from the input values on the high side of the transition point. To remove all the major *DNL*s, correction values should be calculated for all the input codes. A correction value for a certain code is equal to the negative of the sum of all major *DNL*s below that code.

An example of the correction value calculation for a unipolar DAC is shown in Fig. 4.26. In this example, only 3 major discontinuities with values larger than 1 LSB

Figure 4.26: Correction values for digital calibration on a 6-bit cyclic DAC with 10% capacitor mismatch.

are to be removed. At the first major transition, i.e. code 16, $DNL \approx -1.5$ LSB. To remove it, a value of 1.5 LSB should be added to the codes higher than 15. Noninteger input codes can only be generated using extra resolution bits; for example in this case using 7 bits in the conversion will allow addition of 1.5 LSB, otherwise, the correction values have to be rounded to the resolution of the DAC. The correction value jumps by about 3 LSBs at the next major transition from 31 to 32, which is the negative of the DNL value at that point. Finally the correction values for inputs higher than 48 are approximately 6 LSBs.

Due to the near perfect symmetry of the bipolar DAC, the correction values are calculated only for one polarity, and applied to the magnitude of the input regardless of the sign. This saves calibration time, and more importantly, required memory.

Figure 4.27: Simulated effect of digital calibration on *DNL* of a 14-bit cyclic DAC (13-bits plus sign) with 0.1% capacitor mismatch.

To demonstrate the application of this concept, a 14-bit cyclic DAC (13 bits plus sign) with 0.1% capacitor mismatch is simulated. Only the 14 largest *DNL* errors are corrected by the calibration method. The *DNL* and *INL* plots of Fig. 4.27 and Fig. 4.28, respectively, indicate very effective reduction of large errors in the uncalibrated converter.

The accuracy of the correction is limited to the tolerance of the A/D converter for measuring *DNL* values. Since each measured *DNL* is the difference between two A/D output values, if the A/D has (at best) ± 0.5 LSB of accuracy for each of those values, the measured *DNL* may have as much as ± 1 LSB of error. For this reason, to reach ± 0.5 LSB of linearity for the calibrated DAC for a given resolution, the calibrating A/D and the DAC itself must run for at least one extra bit of resolution. This subject will be further discussed as a part of the implementation issues.

With the theoretically unlimited linearity available with digital calibration, it is tempting to use this facility excessively. However, some other factors should also be

Figure 4.28: Simulated effect of digital calibration on *INL* of a 14-bit cyclic DAC (13-bits plus sign) with 0.1% capacitor mismatch.

considered in finding a proper limit to the use of this method. First, the linearity of other sections of the converter, especially the continuous-time linearity of the second S/H stage should be examined. There is no use reducing the linearity errors of the DAC core much below the other contributors. For example, if the linearity of the rest of the DAC system is limited to 12 bits (about 80 dB *SFDR*) it is reasonable to try to achieve 14 bits of linearity and resolution in the DAC core. Carrying the extra two bits is also recommended from the noise perspective, as discussed before. Secondly, the size and power dissipation of the calibration logic needed for this method must be considered too. The calibration time may also be a limiting factor in some applications. Finally, the linearity of the converter should always be compared against its noise floor. For most applications, such as DSL, the noise generated by nonlinearity is not distinguishable from the thermal noise. Reducing the thermal noise requires an (almost) inversely proportional increase in the power consumption.

4.5.2 Implementation

To implement this calibration method, the value of major *DNLs* must be measured during a calibration period. Then correction values for various ranges should be calculated and stored in corresponding registers in memory. Finally, during normal operation, the input has to be corrected by the saved correction values.

Figure 4.29: Simplified digital calibration scheme. (a) During calibration period. (b) Normal operation.

A simplified block diagram in Fig. 4.29 shows the calibration scheme. A digital control block provides data and the timing for the sequence of events during the calibration period. This involves generation of the digital codes for both sides of the major discontinuities of the DAC, starting from the first one (closest to zero). Then it decodes the output of the A/D converter, and calculates the output difference minus one LSB, i.e. the *DNL* size for that transition. The absolute value of the first major *DNL* is stored in the first memory location as the correction value for the second

segment of the transfer characteristic, i.e. the values above the transition point.

For example, if only 7 major *DNLs* are to be corrected for a 13-bit DAC (excluding sign), each segment of the input is $\frac{1}{8}$ of the range (1024 LSBs), and the first major transition is from 1023 to 1024. The first correction value, which is the absolute value of the output difference for codes 1023 and 1024 (minus 1 LSB), is stored in the first memory location.

After calibration, the correction values stored in the memory, are available for normal operation. In this mode, first the most significant bits of the digital input determine its segment and the correction value to be fetched from the memory. Then the digital controller adds that value to the input, if the result of the addition falls in a higher segment (than the input itself), the correction value for the next segment has to be fetched and added to the input instead. The decision on the change of segment is simply made if there is a carry from the LSBs to the MSBs during the addition.

The conversion inaccuracy is mainly caused by capacitor mismatch. The mismatch between identically drawn capacitors is virtually independent of temperature, supply voltage, and aging. It is possible to make the *DNL* measurements at the device test phase, and store the correction factors in a non-volatile memory on the chip. This method is particularly attractive if ROM or Flash memory is available in the technology. Otherwise, some kind of self calibration may be employed.

For a self calibrating cyclic DAC, a high precision A/D converter is required to make the *DNL* measurements. Any kind of linear ADC can be used for this purpose. In most systems, such as modems, A/D converters may already exist in the system. However, it is more suitable to have the calibration circuit implemented inside the DAC itself, if it can be made economical (small enough). This way, the DAC will be independent and there will be no need for stringent timing alignments. The proposed method is the use of a high resolution sigma-delta modulator.

First-Order Sigma-Delta Modulator in Second S/H Stage

Sigma-delta modulators can be used as very linear A/D converters without a need for high precision components [58]. Among various architectures, the first-order modulator is the simplest of all, which can also deliver very high accuracy measurements, but at low conversion rates [61, 62, 63].

In the past, first-order $\Sigma\Delta$ modulators have been used in digital calibration of low resolution DACs used in pipelined A/D converters [64]. Recently, the modulator has also been used to digitally calibrate the MSBs of a 14-bit current steering DAC [7].

Figure 4.30: Block diagram of the first-order sigma-delta modulator.

The attractiveness of the first-order $\Sigma\Delta$ as a calibrating A/D converter is in its simplicity and robustness. The block diagram of this converter is shown in Fig. 4.30. The modulator has coarse A/D and D/A converters (in this case single-bit), however through oversampling and noise shaping principles, the low-pass filtered output of the digital decoder delivers high resolution [58]. In the present application, the behaviour and performance of the modulator is best understood in a time-domain analysis contained in [63]. Since all the measurements in the proposed application are relative, unlike [63] there is no need for offset cancellation.

In the new calibration scheme, the calibrating $\Sigma\Delta$ modulator can be implemented as a part of the second S/H stage. The combined circuit is shown in Fig. 4.31 together with its timing diagram. Compared with the S/H alone (Fig. 4.24), the comparator, C_{DAC} , S_1 through S_{12} and their associated control logic are the extra cost for the first-order $\Sigma\Delta$ modulator functionality. The single-bit D/A conversion is accomplished,

(a)

(b)

Figure 4.31: Single-ended view of the second sample-and-hold stage and the sigma-delta modulator embedded in it. (a) Schematic diagram. (b) Timing diagram.

as usual, with a single feedback capacitor C_{DAC} charged selectively by V_{ref} or zero.

In the normal operation mode the S/H circuit runs as before, and the comparator should be turned off to avoid unnecessary power dissipation. For the duration of the calibration period, however, the comparator is powered up and the respective clock phases are also active. In this mode, the charge sharing path through S_3 and S_4 and the resistors is disabled, and the fast integration path through S_5 and S_6 is enabled. Unlike the normal mode, precise settling is required in the calibration mode to ensure sufficient accuracy from the modulator. At the beginning of each calibration measurement, the reset switch S_{12} is closed to discharge C_H . Then the modulator integrates the input, and subtracts the reference or not according to the polarity of the output voltage. This constitutes the classic first-order $\Sigma\Delta$ modulator A/D converter.

According to Robert in [63], it is possible to increase the resolution of the first-order converter, by adding an extra cycle to the operation in which the input is not integrated and only the feedback is subtracted. At the end of that cycle, the output bit D_{out} is not counted like the other bits, but rather appended to the result as the LSB. Although this feature does not require any addition to the circuit of Fig. 4.31, since it requires some extra logic, it is not recommended unless the duration of the calibration period has to be reduced for a given application. The method of decoding for this modulator is explained in the following section on the calibration logic.

The cost of the additional analog circuitry for calibration in the second S/H stage is relatively low. The comparator for the modulator can be a very simple and small design, and its power dissipation can be neglected. The extra switches and the capacitor are also very small compared to the overall size of the circuit. Therefore, the largest impact on size and power dissipation is in the calibration logic.

Calibration Logic

As mentioned at the beginning, digital calibration is possible only if there is redundancy in the DAC, i.e. the conversion radix is smaller than 2. As seen in Chapter 2, the radix is defined as,

$$r = \frac{C_{T1} + C_{T2}}{C_{T2}} \frac{C_{T2} + C_{DS}}{C_{T2}}. \quad (4.35)$$

Using layout techniques explained in Chapter 6, the fringing field capacitance can be made negligible compared with the capacitor mismatch. Assuming perfect symmetry in the drawn layout, the implementation is expected to have a symmetrical distribution of $C_{T1} - C_{T2}$ around 0. However, to guarantee possibility of digital calibration, we must have $C_{T1} < C_{T2}$.

There are two ways to ensure a radix smaller than 2. The first solution is to predistort the drawn layout to make $C_{T1} = C_{T2} - \max(C_{mm})$, where $\max(C_{mm})$ is the worst case capacitor mismatch for identically drawn capacitors. This way, C_{T1} is always smaller than C_{T2} , however, the maximum mismatch is twice as large now. The other possibility is to exchange the role of the capacitors. In this case the new radix will be

$$r' \approx \frac{C_{T2} + C_{T1}}{C_{T1}}, \quad (4.36)$$

which is smaller than 2 if $r > 2$.

From the above two approaches, the second one is preferable because it does not double the maximum mismatch. The efficiency of the digital calibration is dependent upon the matching accuracy. For larger inaccuracies, larger memory is needed to store correction data. As will be seen shortly, doubling capacitor mismatch more than doubles the required memory size.

The block diagram of the calibration logic is shown in Fig. 4.32. The register file (memory) is used to store calibration (correction) data. The M -bit up/down counter, performs as the digital decoder (LPF) for the $\Sigma\Delta$ modulator — to be explored shortly.

Figure 4.32: Block diagram of the calibration logic for the symmetrical cyclic DAC.

The N bit (saturating) adder corrects the input digital codes during the normal operation. The calibration logic functions in two different modes: calibration mode, and normal mode.

Method of decoding $\Sigma\Delta$ modulator output There are minor differences between the decoding method suggested in [63] and the one used here. Since the polarity of the input is known during the calibration (always positive), the traditional method requires a comparison level of $V_{\text{ref}}/2$ for the comparator. However, in the present simplified approach, the comparison level is kept at zero and the output of the integrator swings between $-V_{\text{ref}}$ to $+V_{\text{ref}}$ (or $V_{\text{ref}-}$ to $V_{\text{ref}+}$). This means that the

output voltage of the integrator after 2^N cycles as given by

$$V_{\text{out}}[2^N] = 2^N C_S V_{\text{in}} - C_{\text{DAC}} V_{\text{ref}} \sum_{i=0}^{2^N-1} D_{\text{out}}[i], \quad (4.37)$$

is bound by $\pm V_{\text{ref}}$. This error is equivalent to ± 1 LSB for the A/D converter. The value of D_{out} at the end of the last integration cycle indicates the state of the integrator, e.g. a 1 means $V_{\text{out}} > 0$. By adding this last sample to the summation in Eq. 4.37, the quantized input voltage is defined as

$$V_{\text{in}}^* = 2^{-N} \frac{C_{\text{DAC}}}{C_S} V_{\text{ref}} \sum_{i=0}^{2^N} D_{\text{out}}[i], \quad (4.38)$$

and the quantization error range in the result is reduced to

$$0 < \epsilon_q < \frac{V_{\text{ref}}}{2^N}, \quad (4.39)$$

which is bound by 0 and 1 LSB. Although this range has +0.5 LSB of offset compared with the ideal ± 0.5 LSB range, it is acceptable in this case because all we are interested in is the difference between two A/D measurements as the *DNL* value. Nominally $C_{\text{DAC}} = C_S$ to avoid any need for extra calculations. The matching accuracy of C_{DAC} and C_S is not critical since all the measurements are relative.

In order to approach ± 0.5 LSB of *DNL* error for the calibrated converter, the error in the *DNL* measurement has to be within this range. From the above, the A/D measurement of each *DNL* has ± 1 LSB of accuracy. Therefore, with an N -bit counter, $2^N + 1$ conversion cycles for each level measurement, and an N -bit DAC ($N+1$ including sign) an N -bit linearity bipolar DAC (including sign) may be obtained.⁶ This is the assumed method in all the following discussions.

Calibration mode In this mode, data to the DAC is provided by the state machine, and the sign bit is set to 0, for positive output. Due to the symmetry of the bipolar

⁶Although it is possible to measure the *DNL* values directly to obtain the ± 0.5 LSB of accuracy, due to extra complexity in the analog and digital parts of the circuit, it is avoided here.

DAC, the *DNL* values should be measured for one side only. The second S/H is also put into the $\Sigma\Delta$ mode of operation.

At the beginning of this mode the up/down counter is reset to +1 LSB. Then the state machine performs a test on the relative size of the DAC capacitors by measuring the largest *DNL* for the default setting. After a short settling time, the DAC is run for 2^N cycles while converting code $011 \dots 11$, and the counter is instructed to count up on every 1 bit from the comparator. Afterwards, code $100 \dots 00$ is sent to the DAC and, following some settling time, the counter starts counting down on every 1 at its input. The final result in the counter is the measure of $-DNL$ for the MSB transition. If this value is positive, the capacitor roles are suitable, otherwise, they should be exchanged by flipping the capacitor select output.

After setting the right capacitor roles, the counter is reset to +1 again and the first *DNL* to be corrected is measured (i.e. at the transition between the first and the second segment in the input range). This is the first correction value that should be stored in the memory (discussion on how many of these bits may be nonzero and should be stored in the memory is in a following section). Since it is possible for this difference to be very close to zero (for very well matched capacitors) and the measured value to be slightly negative (due to minute errors) it is very important to ensure that the counter is limited at 0, and is not allowed to roll over.

The second correction value measurement is done without resetting the counter. In this manner the counter actually accumulates the discontinuities as it is supposed to according to Fig. 4.26, and there will be no need for any further calculations. Just before each *DNL* measurement, the counter is advanced by 1 LSB.

Upon concluding the measurement of the correction values for all the $2^L - 1$ major discontinuities, the calibration mode is ended.

Normal mode During normal operation, the proper correction value has to be found in the memory and added to the magnitude of the input. There are two phases in each correction cycle.

In the first phase, MUX1 selects the L MSBs of the input as the read address to the memory to find an estimate of the correction value. Then this value is added to the input. For the most part, the result of the addition should fall within the same segment. For values very close to the upper segment boundary this will not be the case. For these values of input the L MSBs have to be modified to the new segment through MUX1 in the second phase of the correction cycle. Since the segment size is expected to be much larger than the correction values (e.g. $6\% \gg 0.4\%$) there is no chance that addition of the second correction value would change the segment again.

Memory Size

For the digital calibration to be efficient, the amount of memory used must be kept low. On one hand, one must improve the capacitor matching accuracy (using layout techniques) to require fewer and smaller correction values, and on the other hand the memory cells should be used effectively. An estimation of matching accuracy achievable in the application technology is needed before designing the calibration logic (otherwise matching error should be overestimated).

While the measured correction values in the up/down counter have N bits (same as the resolution of the DAC minus sign), most of these bits are expected to be zero, and need not to be stored. For example, in a 14-bit (plus sign) converter with 0.1% worst case capacitor mismatch (similar to the example of Fig. 4.27 and Fig. 4.28, but with one more resolution bit to ensure ± 0.5 LSB maximum nonlinearity), the largest correction value is 24 LSB. Storing a value of 24 requires only 5 bits of memory. Smaller correction values for lower segments, need even fewer memory bits. In this example, the total number of storage bits required in the memory is 29.

Figure 4.33: DNL values that have to be corrected through digital calibration (FS refers to full-scale magnitude).

If the smallest power of 2 which is larger than the absolute value of the largest DNL in LSBs is L , i.e. $\max(|DNL|) < 2^L$, then the next two largest DNL s have absolute values smaller than 2^{L-1} . Likewise, the absolute values of the next 4 largest DNL s are smaller than 2^{L-2} , and so on. According to Fig. 4.33, since the smallest discontinuities that have to be corrected should be larger than 1 LSB, there are only $\sum_{i=0}^{L-1} 2^i$ total correction points, which is equal to $2^L - 1$. In other words, the full range (unipolar) is divided into 2^L segments.

Through mathematical induction, it can be proven that the maximum value of the correction factor at segment j is given by

$$C_{\max}(j) = \sum_{i=1}^{\lfloor \log_2 j \rfloor + 1} (2^i - 1) \left\lfloor \frac{j + 2^{i-1}}{2^i} \right\rfloor, \quad (4.40)$$

where $\lfloor \cdot \rfloor$ is the integer floor function. Since the number of bits required for representing any number m in binary format is $\lfloor \log_2(m) \rfloor + 1$, the total number of bits needed is

$$\begin{aligned} M &= \sum_{j=1}^{2^L-1} \lfloor \log_2(C_{\max}(j)) \rfloor + 1 \\ &= 2^L - 1 + \sum_{j=1}^{2^L-1} \left\lfloor \log_2 \left\{ \sum_{i=1}^{\lfloor \log_2 j \rfloor + 1} (2^i - 1) \left\lfloor \frac{j + 2^{i-1}}{2^i} \right\rfloor \right\} \right\rfloor. \end{aligned} \quad (4.41)$$

From the definition of L it is clear that it represents the number of bits by which the linearity of the DAC is intended to be improved. For example, if 10 bits of accuracy is achievable without calibration, to improve it to 14 bits, $L = 4$ is required. Table 4.1 lists the number of memory bits needed for calibration (M), versus the required enhancement in linearity (L). The growth is very rapid, hence it is shown again that improving the capacitor matching (using special layout techniques etc.), and having a close advance estimate of matching can reduce the circuit size (and power dissipation) significantly. Practically, the enhancement in linearity is limited by other factors and is rarely needed beyond 4 bits.

The parameter K in Fig. 4.32 is the maximum number of bits required to store the correction factors. This number of bits is needed to store the largest correction value, which according to Eq. 4.40 is

$$K = \left\lceil \log_2 \left\{ \sum_{i=1}^{2^L-1} (2^i - 1) \left\lfloor \frac{2^L - 1 + 2^{i-1}}{2^i} \right\rfloor \right\} \right\rceil + 1. \quad (4.42)$$

L (Bits)	M (Bits)
1	1
2	7
3	25
4	73
5	187
6	459
7	1083

Table 4.1: Memory size (M) required in digital calibration for various linearity enhancements (L).

The other elements in the calibration logic which are significant in size are the up/down counter (which can be powered down during normal operation), the state machine (which can be mostly powered down in normal mode), and the multiplex-

ers. The adder is usually needed to perform the 2's complement to sign-magnitude conversion, and already exists in the system.

Calibration Time

The calibration sequence can be initiated on power-up reset, or any power glitch. For each major *DNL* two values have to be measured. For each measurement approximately 2^N samples are needed for the $\Sigma\Delta$ A/D conversion (N is the number of magnitude resolution bits).

If the largest *DNL* before calibration is bound by 2^L , then $2^L - 1$ calibration values have to be measured, and the required number of clock cycles is approximately 2^{N+L+1} . For example, to improve linearity from 10 bits to 14 bits, $N = 14$ and $L = 4$, approximately 0.5 M conversion cycles are needed for calibration.

Loss of Range

It should also be mentioned that the converter redundancy reduces its input range by a small amount proportional to the mismatch. More precisely, the magnitude of the input should not exceed the full scale minus the largest correction value.

From Eq. 4.40, the largest calibration value for the last segment is

$$C_{\max}(2^L - 1) = \sum_{i=1}^{2^L-1} (2^i - 1) \left\lfloor \frac{2^L - 1 + 2^{i-1}}{2^i} \right\rfloor. \quad (4.43)$$

Then the normalized loss of range is

$$\begin{aligned} LOR &= \frac{C_{\max}(2^L - 1)}{2^N} \\ &= 2^{-N} \sum_{i=1}^{2^L-1} (2^i - 1) \left\lfloor \frac{2^L - 1 + 2^{i-1}}{2^i} \right\rfloor. \end{aligned} \quad (4.44)$$

This value is tabulated in Table 4.2 for various target (linearity) resolutions (N bits) and the linearity enhancement (L bits).

N	Linearity Enhancement L						
	1	2	3	4	5	6	7
10	0.000977	0.004883	0.016602	0.047852	0.125977	0.313477	0.750977
11	0.000488	0.002441	0.008301	0.023926	0.062988	0.156738	0.375488
12	0.000244	0.001221	0.004150	0.011963	0.031494	0.078369	0.187744
13	0.000122	0.000610	0.002075	0.005981	0.015747	0.039185	0.093872
14	0.000061	0.000305	0.001038	0.002991	0.007874	0.019592	0.046936
15	0.000031	0.000153	0.000519	0.001495	0.003937	0.009796	0.023468
16	0.000015	0.000076	0.000259	0.000748	0.001968	0.004898	0.011734

Table 4.2: Normalized loss of range due to digital calibration for various target (linear) resolutions (± 1 LSB linearity unipolar, ± 0.5 LSB linearity bipolar) and linearity enhancements (L).

Improving linearity through digital calibration from 10 bits to 14 bits, causes less than 0.3% loss of range. To avoid rollover for input values closer than LOR to the full scale, saturating adders should be used in the calibration system. It should be noted that the DAC gain is also increased by $\frac{1}{1-LOR}$, which can be partially, or fully compensated for.

4.6 Conclusion

The performance of the stray-insensitive quasi-passive cyclic DAC can be greatly improved following the proposals of this chapter. The extra bit of linearity and best performance in the mid-range point, better S/H circuits, and a simple digital calibration method can help improve the performance of the cyclic DAC substantially.

The claims have been supported only by analysis and simulation so far, however, implementations discussed in Chapter 6 will pave the way for an experimental verification in Chapter 7.

In the next chapter, the pipelined DAC will be the target of the proposals for enhancement, some of which are similar to the ones discussed in this chapter for the

cyclic DAC.

Chapter 5

Advanced Pipelined DAC

The quasi-passive pipelined DAC introduced in Chapter 2 and based on [19, 20, 21], has some shortcomings. The limited linearity of the converter is especially important for high speed operation where parasitics are larger due to the larger switch sizes required.

Most of the improvements made to the algorithmic D/A converters by others have been aimed at the cyclic DAC. The main idea of stray-insensitive quasi-passive pipelined DAC has not been reported prior to this work. On top of this main idea, other enhancements based on the discussions on the cyclic DAC in Chapter 4 are also applied to the pipelined DAC here.

5.1 Limitations of Existing QP Pipelined DAC

The nonlinear stray capacitance of the MOS switches used in the original QP pipelined DAC causes integral nonlinearity. Generally, in quasi-passive operation, the resulting charge on the output capacitor is the linear output quantity. In the presence of nonlinear capacitors the output voltage is not linear. The performance limitations are similar to the case of the *typical* cyclic DAC discussed in Chapter 2 (Fig. 2.7). Inevitably, the faster the converter, the larger the switches, and the larger the non-

linearities.

Unlike converters in [19, 20, 21], it is possible to sense the charge stored on the output capacitor (and transfer it to a linear capacitor) to avoid nonlinearity of the output voltage caused by junction capacitance. In this solution, the converter core operates based on the amount of charge, not the voltage. Hence, similar to the case of stray insensitive cyclic DACs, when the charge is transferred to the S/H capacitor, it produces a linear output voltage. There are, however, other problems related to the junction capacitance and the switching scheme that will not be eliminated by this simple technique.

The charge put on each node of the pipelined DAC when they are charged to $b_n V_{\text{ref}}$ is $C_{\text{total}} V_{\text{ref}}$, where C_{total} includes the linear capacitor and all the junction capacitance on that node. When the sampling switch is opened at the end of this phase it also adds some injected charge to the node. Although the injected charge can be reduced using dummy switches (as implemented in [21]), that will add the nonlinear gate capacitance of the dummy switch to the node. Since it is not possible to match the linear capacitor of the sample-and-hold to the total capacitance (including junctions) on each node of the pipelined converter due to process and temperature dependencies, significant gain error results. This gain error is also different for positive and negative reference voltages (due to nonlinearity of the junction and gate capacitors), which reduces the effectiveness of the differential bipolar method.

Therefore, it can be concluded that the simple modification suggested above cannot produce a high performance converter and a more profound change is required.

5.2 Stray Insensitive QP Pipelined DAC

The shortcoming of the traditional QP pipelined DAC is that the charge which is involved in the conversion operation is the sum of the charge on the main capacitor

Figure 5.1: Stray-insensitive quasi-passive pipelined D/A converter. (a) Schematic. (b) Timing diagram.

and the charge on the parasitic capacitors. If the charging of the parasitic capacitors can be avoided, or their charge is removed before any charge sharing operation, the problems created by these parasitics will be solved.

The idea of stray insensitive QP pipelined D-to-A conversion is shown in Fig. 5.1. In this design, the top plate of each main capacitor in the sampling phase is grounded (through $S_{n,1}$) and the bottom plate is charged with the corresponding bit voltage instead (via $S_{n,3}$). In the next phase, when the charge is to be added to the less significant bits, the bottom plate is grounded (by $S_{n,5}$) and only the charge stored on the top plate of C_n is brought into the equation. The charge stored on the parasitics of the bottom plates is dissipated by their grounding switches (i.e. $S_{n,5}$) and do not participate in the conversion process.

The charge sharing with the previous stage, and transfer from one stage to the next, is similar to the original design (Fig. 2.5), and under control of a three phase

clock.

The node voltages throughout the conversion remain nonlinear functions of the input bits (due to junction capacitance of the switches), however, assuming perfect matching of capacitors, the charge remains linear. At the end of each conversion process the charge on the last node is transferred to a linear capacitor of a S/H stage. The output voltage (and hence the gain accuracy) of this circuit depends on the matching between the converter's main capacitors and the S/H capacitor. This matching accuracy is usually better than 0.3%.¹

This architecture solves all the stray capacitance problems of the original design. All these performance enhancements come at the cost of two additional switches per pipelined stage which is much less than the alternative solution, i.e. an opamp included in each stage.

5.3 Differential Bipolar Pipelined DAC

The idea of bipolar conversion can improve the pipelined DAC performance similar to the cyclic DAC. Essentially, an extra bit of resolution, and best linearity in the middle of the range can be obtained using the architecture of Fig. 5.2. A positive or a negative reference voltage is chosen for charging each capacitor based on $s[k] = \pm 1$, the sign of the k th digital input word. The magnitude of the digital input (represented by $b_{N-1} \cdots b_0$) determines the magnitude of the output charge at the end of conversion for each input. As a result, the (statistically) largest *DNL* is moved from the midrange to the 1/4 and 3/4 range points and its amplitude is divided by 2. By a convention similar to the bipolar cyclic DAC, N represents the magnitude resolution, and the overall converter's resolution is $N + 1$, including the sign bit.

To avoid the nonlinearity caused by reference mismatch, a differential implementa-

¹With the third S/H architecture of Chapter 4, the DC gain for the MSB is 1 regardless of capacitor matching, because of the charge sharing method.

Figure 5.2: Bipolar stray-insensitive pipelined DAC.

tion, as shown in Fig. 5.3, is preferred. Similar to the cyclic converter, this balanced circuit also has the advantage of higher noise immunity compared to the original design.

Figure 5.3: Differential bipolar pipelined-DAC.

5.4 Sample-and-Hold

Similar to the cyclic converter, the pipelined DAC needs two stages of sample-and-hold to deliver a linear continuous-time output signal.

Fig. 5.4 shows the single-ended view of the first S/H stage and its connection to the pipelined DAC core. Given the advantages of the third S/H architecture, as analyzed in Chapter 4, it has been chosen for this converter as well. This S/H stage

forces the voltage on the top plate (node) of the capacitor in the last pipelined stage to ground, thereby transferring all the charge stored on that node to the (linear) capacitors C_{N-1} and C_H .

Figure 5.4: First S/H stage in a pipelined DAC.

The second S/H stage is similar to that of the cyclic converter, with only minor timing differences.

5.5 Multiplexed Last Stage

As with the cyclic DAC, one of the main noise sources in the complete pipelined DAC is the first S/H stage. This contribution may be even larger for the pipelined DAC because of the higher speed requirements for this opamp. It is also given that in any CMOS technology the settling time of a network of switches and capacitors (without an opamp) is much smaller than that of an opamp circuit (typically about 3 times). With the help of the pipelined architecture, the conversion rate is greatly improved and the bandwidth of the S/H opamp is the major limiting factor.

The S/H of Fig. 5.4 has to transfer the charge to the linear capacitors in one clock phase. Since a new conversion result is produced every clock cycle, it is possible to

Figure 5.5: Use of multiplexed capacitors in the last stage of the pipelined DAC.

increase the S/H interval to a full clock cycle, thereby reducing the requirement for the opamp bandwidth, and lowering the sampled opamp noise at the output.

The solution, as shown in Fig. 5.5, is to multiplex two capacitors in the last stage of the pipelined converter. Each capacitor in this stage either participates in the conversion by processing the MSB (b_{N-1}), or is connected to the S/H to share its charge with the S/H.

The alternating role of the multiplexed capacitors of Fig. 5.5 is best understood by observing the timing diagram of Fig. 5.6. According to this diagram, the *superphases* Φ_1 and Φ_2 last for a whole clock cycle (T) of the converter. From a single capacitor perspective, the superphases act like the original ϕ_3 , but they are stretched much

Figure 5.6: Timing diagram for the multiplexed last stage of the pipelined DAC, and its first S/H stage.

longer to allow for slower operation of the S/H opamp. From the opamp perspective, there is no difference between the two superphases. As a result, this type of S/H can be called a single-phase architecture.

The most critical challenge in the design of a pipelined DAC, with a multiplexed last stage, is the symmetry of the layout. Since, as discussed before, the total capacitances on the top plate of the pipelined capacitors have to match, all the stages in the pipeline have to be identically drawn (including all the metal routing). However, from the simple diagram of Fig. 5.5, it can be observed that these stages do not match their previous stage ($N - 2$), nor does that stage match all the prior stages (0 to $N - 3$). A solution to this symmetry requirement is explored in Chapter 6.

Another issue with the multiplexed last stages is the capacitor mismatch. In this design, capacitor mismatch mixes with the input signal (modulated by it), which creates *pseudoimages* at $f_S/2$. The pseudoimages are similar to the images around

$\pm nf_S$ in having mirror symmetry, but unlike the images are not caused by DT-to-CT conversion. The amount of charge transferred to the S/H for the same digital input varies between alternating samples. The maximum variation is for the peak input $0.11 \dots 11$. Adding one negligible LSB, the transferred charge in Φ_1 is

$$Q' = V_{\text{ref}}(C_{\text{avg}} + C'_{N-1}) \frac{C'_{N-1}}{C_{N-2} + C'_{N-1}}, \quad (5.1)$$

where C_{avg} is the binary average of C_0 to C_{N-2} . Also, in Φ_2

$$Q'' = V_{\text{ref}}(C_{\text{avg}} + C''_{N-1}) \frac{C''_{N-1}}{C_{N-2} + C''_{N-1}}. \quad (5.2)$$

The ratio of these charges is given by

$$\frac{Q'}{Q''} = \frac{C_{\text{avg}} + C'_{N-1}}{C_{\text{avg}} + C''_{N-1}} \frac{C'_{N-1}}{C''_{N-1}} \frac{C_{N-2} + C''_{N-1}}{C_{N-2} + C'_{N-1}}. \quad (5.3)$$

Since all the capacitors have equal nominal values, let $\frac{C'_{N-1}}{C_{\text{avg}}} = 1 + \delta/2$ and $\frac{C''_{N-1}}{C_{\text{avg}}} = 1 - \delta/2$ (so that δ is the relative mismatch between C'_{N-1} and C''_{N-1}), while $C_{N-2} = C_{\text{avg}}$ (not interested in the effect of C_{N-2} mismatch at this moment). Then, the charge ratios can be written as

$$\frac{Q'}{Q''} = \frac{2 + \delta/2}{2 - \delta/2} \frac{1 + \delta/2}{1 - \delta/2} \frac{2 - \delta/2}{2 + \delta/2} \approx 1 + \delta. \quad (5.4)$$

This means that on top of the peak value there is a pulse train at $f_S/2$ with a relative amplitude of δ . Since the amplitude of the pulse train is dependent on the signal,² the AM modulated signal with pseudoimages around $nf_S/2$ result. These pseudoimages are further attenuated by the low-pass filtering in the first and the second S/H.

The exact analysis of the effect of this capacitor mismatch on an arbitrary signal is cumbersome, however, substantial insight into this effect can be obtained from

²Because of the fact that the MSB has a different mismatch error than the rest of the bits, the amplitude of the pulse train is not linearly proportional to the signal. However, the peak value derived here is always the maximum. Furthermore, the IIR filter in the first sample-and-hold becomes slightly time varying from sample to sample.

simulation. Fig. 5.7 shows the effect on a DMT signal for a capacitor mismatch of 0.1% simulated at high-level in Matlab. The pseudoimage below $f_s/2 = 8.832$ MHz is clearly visible, and the raised noise floor in the baseband due to this nonlinearity is below -90 dBc.

Figure 5.7: Simulated effect of 0.1% capacitor mismatch in the multiplexed last stage of a pipelined DAC at the output of the first S/H stage. Nominally, $C_{N-1} = C_H$ is assumed.

Single-Phase Second S/H

To reduce the speed requirements on the opamp in the second S/H, multiplexed input capacitors can also be used in that stage. Similar to the first S/H stage, this single-phase circuit may also generate pseudoimages at $nf_s/2$ due to mismatch between multiplexed capacitors.³ This effect is more significant in this stage since it is not helped by the low-pass filtering of the first stage.

³The AM modulation in this case is fairly linear.

5.6 Clock Generator

The need for a 3-phase clock for the pipelined converter is usually not easy to accommodate. Some systems do not have a clock generator running higher than the data rate, and the ones that do, usually have it at a power of 2 times the data rate. Including a 3-phase clock generator in the design is the best way to make a versatile pipelined DAC.

One way to generate a 3-phase clock is to multiply the data clock by 3, and then create the phases that are one full cycle wide. The usual method for multiplying a clock frequency is to use a phase-locked loop. Design of a low phase-noise (jitter) PLL is not trivial, and despite all efforts, there is always some additional jitter at the output. The method presented here maintains the synchronization of the critical clock edge in the 3-phase clock with the original one, thereby avoiding any additional jitter that can modulate the output signal.

Figure 5.8: Three-phase clock generator.

The proposed scheme is shown in Fig. 5.8. The basis for this design is the use of feedback loops for generation of clock pulses with desired duty cycles. The circuit is better understood by observing the timing diagram of Fig. 5.9. Shortly after the

rising edge of the input clock, CKIN, flip-flop FF1 is set, and switch S_1 is opened. At this time, the current source I_1 starts to charge C_1 until it reaches the input threshold voltage for IV1, at which time FF1 is reset and P_1 goes back to zero.

Figure 5.9: Timing diagram for the three-phase clock generator.

The amount of source current I_1 determines the rate at which the capacitor is charged to reach V_{THIV1} (the threshold voltage at the input of IV1). The larger the current, the faster the charging and the shorter the pulse width of P_1 . Therefore, the duty-cycle of P_1 is determined by the (inverted) control voltage on the current source (simply a PMOS transistor). The low-pass filter formed by R_1 and C_2 takes the average value of the output voltage at P_1 , which is essentially the duty cycle of that pulse train multiplied by V_{DD} . Through the action of the negative feedback loop, the average value of the output phase P_1 is kept at $V_{DD}/3$, which results in a duty cycle of 1/3 for this clock phase.

Likewise, the duty cycle of Q_2 is maintained at 2/3, which establishes 1/3 duty cycles for (almost) nonoverlapping clock phases P_2 and P_3 . A small amount of overlap between the phases may exist due to minor rising-edge to falling-edge mismatch of the flip-flops and the delay of the AND gate. The output phases of this circuit have to

be further refined by a nonoverlapping phase generator explained in Chapter 6. That generator will also provide delayed clock phases as well as the superphases, needed for single-phase S/Hs.

The precision of the duty cycle for the clock phases is mainly governed by the accuracy of the $V_{DD}/3$ and $2V_{DD}/3$ reference voltages.⁴ These voltages are derived from the power supply with resistor dividers that can have accuracies better than 1%.

To prevent the jitter created in this circuit (on the falling edge of P_1 , both edges of P_2 , and the rising edge of P_3) from increasing the output (analog) noise, the converter has to output samples on the rising edge of P_1 . The timing on this edge is controlled solely by the input clock CKIN, and does not have any significant additional jitter on it.⁵

The same idea can be used to multiply the clock frequency for the cyclic DAC as well. For example, if the maximum clock frequency available in the system is only half of what is needed for a cyclic DAC with suitable conversion rate, this frequency can be multiplied by two using a scheme with 3 similar sections (to produce $\frac{3}{4}$, $\frac{1}{2}$, and $\frac{3}{4}$ duty cycle phases).⁶ Expansion of this method to a higher number of clock phases may be limited by the available timing accuracy (I and C) and power dissipation.

5.7 Digital Calibration

Digital calibration similar to that used in the cyclic converter can be used to linearize the transfer characteristics of the pipelined converter as well. Since more than two capacitors are involved in the conversion algorithm of the pipelined DAC, the *DNL*

⁴Effects of offset and finite gain of the opamp are usually negligible in this circuit.

⁵In the absence of excessive power supply noise, added jitter in digital gates is very negligible since the transition times, especially for on-chip signals, are very short. Power supply noise of the digital section of a DAC has to be kept low and signal-independent. This circuit is not any more sensitive to the power supply noise than any other part of the digital section of a DAC.

⁶Only two sections are needed if original clock is symmetrical.

values are more independent (there are $N + 1$ capacitor values in an N -bit converter). Therefore, if only the capacitor mismatch values were to be stored, more memory elements would be required than in the cyclic case. However, in the *DNL*-based scheme explained in Chapter 4, the correlation between *DNLs* is not considered, hence, the same scheme can be used for the nonmultiplexed pipelined converter. For the pipelined converter with a multiplexed last stage, some changes have to be made to the digital calibration to accommodate the variation of the capacitor mismatch values from sample to sample.

The multiplexing of the last stage alternates the *DNL* values associated with the last capacitor C_{N-1} . The capacitor mismatches (and their related *DNLs*) for all bit transitions prior to the MSB is common between C'_{N-1} and C''_{N-1} . The slight gain variation due to the mismatch between C'_{N-1} and C''_{N-1} during measurement of the calibration values is only a secondary effect. At the MSB and higher up transitions, however, the difference between the *DNL* values for C'_{N-1} and C''_{N-1} requires all calibration values for C'_{N-1} and C''_{N-1} to be measured separately. For example, if for a given matching accuracy and resolution requirement there has to be 15 total calibration values stored for a nonmultiplexed PDAC (i.e. 16 magnitude segments), for a corresponding multiplexed PDAC, $7 + 8 + 8 = 23$ memory locations are needed.

5.7.1 Preskew

Unlike the cyclic DAC (see Section 4.3), it is not practical to exchange the capacitor roles in a pipelined DAC. Therefore, to ensure the ability for calibration, sufficient preskew or redundancy must be built into the pipelined DAC. In this preskew, only the most significant capacitors in the pipelined should be slightly reduced in value, and this reduction has to progressively increase towards the MSB. Following a short review of capacitor matching statistics in the pipelined DAC, the amount of this preskew will be calculated.

Let the normalized (per unit) standard deviation of the value of a unit capacitor from its mean on a given die be σ (e.g. 0.001). Since the value is normalized, by definition, the mean is 1. Then for two unit capacitors, drawn with proper layout techniques,⁷ the normalized standard deviation of mismatch is

$$\sigma_m = \sqrt{\sigma^2 + \sigma^2} = \sqrt{2}\sigma, \quad (5.5)$$

since the capacitors are identically drawn and the random errors in their values are independent. Usually, for a given technology, the value of σ_m is given and σ has to be derived using the above equation.

In a differential DAC, there are two capacitors whose values together, i.e. their sum, determines the mismatch error. Hence, the standard deviation of the value of a (unit) capacitor pair should be found. The nominal capacitor value is doubled, while the standard deviations should be RMS added (independent random variables), therefore normalized (i.e. per unit-pair) standard deviation for the differential pair is given by:

$$\sigma_d = \frac{\sqrt{\sigma^2 + \sigma^2}}{2} = \frac{\sigma}{\sqrt{2}}, \quad (5.6)$$

which is smaller than σ . To calculate the amount of preskew needed for the pipelined DAC, the matching accuracy between one capacitor pair (at $k-1$ position), and a binary weighted average of all the capacitor pairs preceding that ($k-2$ to 0) is needed. The normalized standard deviation of this ratio which is obtained from the weighted sum of the variances of all capacitors, can be estimated by

$$\sigma_{db} = \sqrt{\sigma_d^2 + \left(\frac{1}{4}\sigma_d^2 + \frac{1}{16}\sigma_d^2 + \frac{1}{64}\sigma_d^2 + \cdots + \frac{1}{2^{2(k-1)}}\sigma_d^2\right)} \approx \sqrt{1 + \frac{\frac{1}{4}}{1 - \frac{1}{4}}}\sigma_d \approx 1.155\sigma_d, \quad (5.7)$$

in which the binomial expansion formula for $k \gg 1$ is used.

⁷Proper layout techniques, explained in more details in Chapter 6 are aimed at preventing systematic mismatch in the capacitor values, and thereby leaving only random mismatch errors.

From σ_{db} the (statistical) worst case DNL of an uncalibrated pipelined DAC can be calculated. For example a maximum mismatch of 0.001 corresponds to $DNL_{\max} \approx 0.5$ LSB for 10 bits of resolution.⁸

It is necessary to determine which capacitors have to be preskewed. The capacitor value which is not preskewed may not be calibrated. If the preskew starts from capacitor number k in the pipeline, then the (statistically) worst case DNL which may not be calibrated is due to mismatch between C_{k-1} and the binary average of all previous capacitors. If the worst case value of this mismatch is δ_{db} (say $3\sigma_{db}$), then the worst case uncorrected DNL is $2^{k-1}\delta_{db}$ in LSB, and for this value to be less than or equal to 0.5 LSB,

$$k \leq \log_2 \delta_{db} . \quad (5.8)$$

For example, if $\delta_{db} = 0.1\%$, then $k = 10$ is the largest value allowed, i.e. at least capacitors in positions $k = 10$ and higher have to be preskewed.

To ensure negative DNL at the b_k transition, the preskew value for C_k is $\delta_k = -\delta_{db}$. For the next stage, $k+1$, the same value of preskew is required to deal with the random mismatch, however, in addition to that, a $-\delta_{db}/2$ is also necessary due to the preskew in C_k . In general, the preskew value for capacitor C_{k+j} is

$$\delta_{k+j} = -\delta_{db} + \sum_{i=0}^{j-1} 2^{-i-1} \delta_{k+i} , \quad (5.9)$$

which increases in absolute value towards the MSB. Successive use of the above equation results in values of $-1.5\delta_{db}$, $-2\delta_{db}$, $-2.5\delta_{db}$, etc. as the normalized preskew for capacitors C_{k+1} , C_{k+2} , C_{k+3} , etc. respectively.

With this preskew, the worst case mismatch will be exacerbated, and more memory for calibration data is needed. Basically, the preskew doubles the worst case DNL sizes, which increases the resolution enhancement factor (L) in Table 4.1 by one.

⁸For DC performance only, multiplexing the last stage in the pipelined DAC results in an averaging of the mismatches and improves $DNL_{\max}$ by $\sqrt{2}$.

Figure 5.10: Bank-Of-Cyclics (BOC) digital-to-analog converter.

Likewise, the loss-of-range due to mismatch and calibration is increased as well.

5.8 Bank-of-Cyclics Converter

Cyclic and pipelined quasi-passive converters described so far have considerable similarities. The choice between these architectures depends mainly on the conversion rate requirements.

While the pipelined converter produces a new output in every clock cycle, the cyclic converter needs many clock cycles for its conversion. The sample-and-hold stage of the cyclic converter is only about 3 times slower than the switch and capacitors in charge transfer. Since the number of conversion bits is usually much larger than 2 (equivalent to 4 clock phases for conversion), the same S/H stage can be shared by many cyclic converters.

The Bank-Of-Cyclics (BOC) converter is shown in Fig. 5.10. The M cyclic DAC cores used in this design have time interleaved operations, such that at any given time, only one of them is transferring its resulting charge to the S/H, and all the others are converting the succeeding digital inputs. For example, if 4 cyclic DAC cores are used for 12 bit (plus sign) conversion, the S/H operation takes only 4 clock cycles, and 12 clock cycles are used for the conversion. A BOC converter with a multiplexed S/H

delivers conversion rates that are between a single cyclic and the pipelined DACs.

The effect of mismatch between cyclic converter cores can be analyzed in the same manner as the pipelined DAC with multiplexed last stage, and has a similar peak and spectrum. The pseudoimages in this case appear at nf_s/M .

5.8.1 Economy of Bank-of-Cyclics

Each differential cyclic DAC contains 4 capacitors in the core. An N bit differential bipolar pipelined DAC has $2N$ capacitors. Using the number of capacitors as an indication of the size of the converter core (other factors will be considered later), then for a resolution of N bits, the pipelined converter is $N/2$ times larger than the cyclic. Both converters use roughly 5 switches together with each capacitor.

In the digital section, the cyclic converter requires an N -bit shift register, whereas, the pipelined converter needs $N^2/6 + N/2$ flip-flops.⁹ For example, for $N = 15$, the ratio of flip-flops needed by the pipelined to the cyclic DAC is $45/15 = 3$.

If the proposed simple digital calibration scheme is used, its memory size is larger for the pipelined DAC than the simple cyclic DAC because of preskew, and the doubled last capacitor (multiplexed last stage). For the BOC design, each cyclic core requires a separate memory and the digital control section will be more complicated as well.

The above estimates suggest that, in terms of the circuit size, it is justified to use only a few cyclic converters in the bank. If digital calibration is used, a maximum of two cyclic sections is recommended, whereas without it, up to four converters in the bank may be appropriate.

⁹According to Fig. 2.6, the 3 LSBs have only 3 flip-flops as input registers, the next 3 LSBs have 3 flip-flops as input registers, and 3 others for the pipeline delay, and so on. Generally the number of flip-flops needed is

$$\sum_{i=1}^{N/3} 3i = 3 \frac{\frac{N}{3} + (\frac{N}{3} + 1)}{2} = \frac{N^2}{6} + \frac{N}{2}. \quad (5.10)$$

5.9 Conclusion

Advanced architectures for the pipeline DAC presented in this chapter allow stray insensitive operation in quasi-passive circuits. Also, the addition of the differential bipolar scheme results in an extra bit of linearity and a better nonlinearity pattern.

Multiplexed last stage for the pipelined DAC can increase its conversion rate to more than double, while the optional preskew of the capacitor values in the pipeline makes digital calibration feasible for greater accuracy than what is available from capacitor matching.

These improvements will be put into practice by the implementations of Chapter 6.

Chapter 6

Implementation

In general, an analog circuit concept is only positively proven through implementation and measurement. One too many assumptions or approximations made during the analysis and simulation of the main concept, or one too many parasitic effect neglected in device modeling and circuit simulation may deteriorate the circuit performance to the level that renders it useless. Therefore, careful consideration of all factors in the design and testing of these high-speed and high-resolution converters is a necessity. So far in this work, the analysis and high level simulations have been used to support the ideas. In the present chapter the methodology for implementation of the ideas and their associated challenges are studied. This provides the means for the demanded experimental proof.

The main focus in the implementations in this study has been to prove the concept, rather than presenting a perfectly optimal design. To this end, absolute minimization of some well known factors, such as the thermal noise of the opamp, was not attempted. Nonetheless, the correlation between analysis and simulation on one hand, and the measured data on the other will be verified (Chapter 7).

6.1 Introduction

The purpose of this chapter is to offer a step-by-step approach to the design of QP algorithmic DACs. At the beginning, the system specifications have to be defined. Conversion rate and signal frequency (bandwidth) are the primary requirements, followed by linearity and noise.

The minimum sampling rate for representing a signal in discrete-time domain is twice as large as the signal bandwidth (Nyquist rate). While the Nyquist rate may be a sufficient rate for processing signals in discrete-time domain, in the continuous-time domain, the presence of strong signal images very close to the baseband violates system requirements for out-of-band noise. To facilitate filtering of these images, the digital signal is usually oversampled and interpolated before D/A conversion. Oversampling ratios of 4 and 8 are very common.

Nonlinearity and noise are usually comparable performance factors, since they both represent distortion to the signal. Furthermore, with some modulation schemes, such as Quadrature-Amplitude Modulation (QAM), the very random nature of the signal randomizes the nonlinearity distortion to make it appear like a wide-band noise.

Frequency response is usually less critical since sufficient freedom in DSP allows for substantial compensation.

The next requirement for the design process is the identification of the cost function. With the ever shrinking proportional role and size of the analog sections in modern electronic systems, the chip area is not usually a major concern. Instead, the power consumption of the circuit is commonly considered as the main cost factor to be minimized. The power dissipation in the digital circuitry can be reduced substantially through the use of finer pitch CMOS technologies, and reduced power supply voltage. However, the power dissipation in the analog section is usually not lowered by reducing the process scale (it may even rise). The attention in this case has to be

paid to the topology and circuit optimization.

After the definition phase, workable information from the technology should be collected. The ideal design methodology requires a thorough characterization of the target technology and formulation of the dependencies of power dissipation, linearity, noise, and speed of various blocks on design parameters such as topology and device sizes. The optimization can be addressed by enforcing system constraints on speed, linearity, and noise, while power dissipation of the circuit is minimized. While this methodology can achieve a perfectly optimal design, derivation of all the optimization equations may be too tedious to be practical.

In a more practical approach, the converter is synthesized in an iterative process. The flow is started with an educated guess, and following rough analysis and simulation, the initial design is updated. With a good initial guess and careful analysis, in a few iterations, a near optimal design can be reached.¹ Using this design style, the differential bipolar cyclic and pipelined DACs proposed in Chapters 4 and 5 have been implemented in 0.35- μm and 0.6- μm CMOS technologies respectively. Both processes are double-poly (for their linear capacitance) and triple-metal technologies.

6.2 Design Specifications

Although the D/A converters studied in this thesis are not limited to any specific application, the designs are tailored for DSL applications. These applications require conversion rates from 4.416 MSps to 17.664 MSps, and signal bandwidths from 552 kHz to 1.104 MHz. The linearity and noise performance should be in the range of 10 to 13 bits [14, 15].

Due to lack of capacitor matching data for the target technologies chosen, and also to leave more flexibility for experimenting with digital calibration, the correction

¹That is when further iterations seem to bring little improvement to the design.

circuitry was not implemented on-chip. Based on general capacitor matching expectations, the designs are anticipated to deliver acceptable performance without digital calibration. However, the entire calibration scheme can be added to the design off-chip for both cyclic and pipelined DACs. In the case of the pipelined DAC, on-chip analog circuitry (first order $\Sigma\Delta$ M in the second S/H stage) is included to demonstrate the feasibility of integration. Worst case process variations are also considered in the design and simulation of the DACs.

6.2.1 Cyclic DAC Specifications

The cyclic DAC is slower than the pipelined DAC, hence, it is aimed at the lower end of the conversion rate range, i.e. 4.416 MSps.

In terms of linearity and noise, it is intended to achieve 11-bits in performance. This kind of linearity may be achievable without any digital calibration, which can simplify the circuit. For this to be possible, 0.1% matching accuracy is required for the capacitors.

The conversion resolution is chosen to be 14 bits (13 bits plus sign) to make the relative contribution of the quantization noise negligible. Also, it is intended to experiment on the effectiveness of digital calibration, hence, the number of resolution bits in the conversion are chosen slightly higher than needed. This requires 12.5 cycles for the conversion, to which 3.5 cycles of S/H are appended to make the overall conversion period equal to 16 times the clock period.² This calls for a 70.656 MHz clock frequency, to deliver a 4.416 MSps conversion rate. In a 0.35- μ m CMOS technology, this clock frequency is quite practical.

The cyclic DAC implemented on the test chip will be made flexible for experimentation by having the number of clock cycles for the conversion and the S/H phases

²As a time saving feature, the second phase of the last conversion clock cycle is merged with the sample-and-hold phase, i.e. immediately after the last bit is sampled on the input capacitor, the S/H phase begins and the core capacitors share their charge and transfer it to the S/H at the same time.

programmable. The details will be covered in the control logic section.

For the chosen technology, output swing of 2.5 V (single-ended) is feasible with a 3 V supply, and the analog ground level is set at 1.5 V. Therefore, the largest sine-wave at the differential output is 1.7 V_{RMS}, and the overall noise is to be below 500 μ V_{RMS} in 0 to 2.208 MHz bandwidth before any low-pass filtering, i.e. the baseband noise density has to be under 340 nV/ $\sqrt{\text{Hz}}$.

6.2.2 Pipelined DAC Specifications

The pipelined DAC can deliver higher conversion rates, so it will be designed for 17.6 MSps. Ideally a 3 phase clock should be designed for optimized timing, however, for simplicity of the design, a 4 phase clock is used in this case. In DSL applications 35.2 MHz is usually the system clock frequency. By dividing this clock by two, a 4 phase clock is readily produced. Since there are only three operating phases in a QP pipelined stage, the fourth clock phase will be left as idle. Nonetheless, due to phase interleaving between pipelined stages, all four phases are operating for some stages, and idle for some others.

The symmetry in the timing of the converter helps to reduce some of the parasitic effects. Since bit conversion into a capacitor charge, and charge sharing in divide-by-2 operation occurs in different clock phases for successive bits, parasitic effects for different phases have to be equalized.³ This means that all clock phases have to have equal loading on them, i.e. the number of pipelined stages should be an integral multiple of the clock phases, in this case 4. Thus the reasonable choices for the number of pipelined stages are 12 and 16.

With 12 pipelined stages, a 13-bit resolution (12-bit plus sign) can be achieved. It is expected to obtain a 13-bit performance or better from the pipelined DAC with

³For example, the voltage drop on the reference voltage and power supply rails should not change from phase to phase

digital error correction. Therefore, to have the quantization noise below the linearity level, the number of pipelined stages is set to 16.⁴

The technology for this DAC is 0.6- μm CMOS, running from 5 V power supply. This allows for a (linear) differential output peak voltage of 3 V (i.e. 6 Vppd). Because of unity gain in the chosen third S/H architecture, the reference voltages are set to ± 1.5 V centered at the analog ground (AG) level of 2.1 V.

It is desired to have the thermal noise in the complete converter under a 13-bit level of -78 dB below a full-scale sine-wave. Given 3 V as the peak, the noise power has to be below 260 μV_{RMS} .

6.3 Design Challenges

The principle challenge is to design converter cores with good DC linearity in order to verify the essence of the proposed architectures. In fact, the linearity performance of the converter's core is independent of the signal frequency that it generates. In the core, samples are generated independently and delivered to the first S/H stage.

The (DC) linearity in the core is a function of capacitor matching and certain parasitics such as C_{DS} . These factors can be helped using some layout techniques to be discussed in later sections.

After DC linearity, AC performance, including metrics such as harmonic distortion and *SFDR*, are the most important characteristics. At low frequencies these impairments are tightly linked to the DC linearity (of the core), but at high signal frequencies the performance of the sample-and-holds may dominate. Therefore, after the DAC core, the high speed linearity in the S/Hs, especially the second stage, should receive the attention.

The thermal noise of the circuit is more predictable and easier to control. The noise

⁴With no ambition of building a 17-bit linear DAC.

power is usually inversely proportional to the power dissipation, i.e. 3 dB reduction in noise, requires twice as much power. This relationship holds for individual blocks, and if the noise contribution of separate blocks are optimally assigned, it holds for the entire DAC as well. For example, the thermal noise power from the DAC core is Θ/C , and the power consumption is proportional to C .

As discussed in Chapter 4, there are 3 main noise contributors to the output, namely, thermal noise in the DAC core (Θ/C), sampled thermal noise of the first S/H opamp, and finally thermal noise of switches and resistors in the second S/H stage ($\frac{\Theta}{C_S} + \frac{\Theta}{C_{eq}}$). Since the contribution of the sampling capacitor C_S in the second S/H is relatively larger, it makes sense to use a larger value for this capacitor than the one used in the DAC's core. However, the capacitor size in the core also determines the matching accuracy and its associated linearity (which is improved by larger values). Since these effects were not comparable due to lack of capacitor matching information for the technologies, in the cyclic DAC C_S was made larger (i.e. smaller DAC capacitors for lower linearity requirement compared with the pipelined DAC), and in the pipelined design they were set equal. The opamp noise in the first S/H of the cyclic DAC is the dominant noise source, mainly due to its very large bandwidth (required by short settling time) and high aliasing factor. In the pipelined DAC, the SC thermal noise of the second S/H will be comparable to the opamp noise in the first S/H stage, both of which will be higher than the thermal noise of the core (capacitor size in the core is mainly determined by linearity, i.e. matching).

6.4 DAC Cores

The first step in designing the DAC core is to specify the capacitor size. The size of switches and the logic gates driving them can then be determined based on the capacitor size.

The capacitor size in the core of the DAC determines the matching accuracy, the thermal noise of the core (Θ/C), power consumption in the core (from the reference voltage sources), and power dissipation in the driving logic.

6.4.1 Cyclic Core

The capacitor size in this DAC is mainly chosen for the required matching accuracy. It is expected that with a 1 pF differential unit capacitor, 0.1% matching accuracy can be reached.⁵ Using both capacitors of the core in charge transfer to the first S/H, the effective capacitance for thermal noise calculation is 1 pF, which has $91 \mu V_{\text{RMS}}$ of noise differentially at room temperature. This noise is much less than the overall budget of $500 \mu V_{\text{RMS}}$.

The power taken from each reference voltage source, according to Eq. 2.6, is less than $44.9 \mu W$ ($f_S = 4.416 \text{ MHz}$, $V_{\text{ref}+} = 1.25 \text{ V}$, $C = 0.5 \text{ pF}$, and $N = 13$). The current taken from $V_{\text{ref}+}$ is passed on to the $V_{\text{ref}-}$, so if they are powered by the same supply voltage as the DAC, i.e. 3 V, the total reference power is less than $108 \mu W$, which is negligible. However more power is dissipated in the logic that drives the core (to be simulated later).

The single-ended schematic of the cyclic DAC implemented is similar to the symmetrical DAC of Section 4.3 and is shown in Fig. 6.1. The R_{on} of PMOS switches are about 3 times larger than NMOS ones with the same dimensions (due to lower mobility of holes in silicon). Therefore, for the switches that are connected to the ground level (1.5 V) only NMOS switches are used, and in places where the switch terminals may stay at positive potential, PMOS or complementary transistors are deployed. The switch sizes are determined by simulation for settling ($< 0.01\%$) within 5 ns, which is less than half of the clock period ($\frac{0.5}{70.656 \text{ MHz}} \approx 7 \text{ ns}$) to allow for some non-overlap time between the phases and clock asymmetry.

⁵Unofficial data from the manufacturer of the chip.

Transistor Sizes (W/L)	
M_{1Px}, M_{3P}, M_{5Px}	$30 \mu/0.35 \mu$
M_{2x}, M_{4x}, M_{6x}	$20 \mu/0.35 \mu$
$M_{1Nx}, M_{3Nx}, M_{5Nx}$	$10 \mu/0.35 \mu$

Figure 6.1: Single-ended schematic view of the implemented cyclic DAC. Bulk nodes are connected to respective power supplies.

The switches for transfer of charge to the S/H are also included in this schematic. Due to parasitic couplings (such as capacitance between metal traces), some fluctuations from data bit transitions reach the input of the first S/H opamp, and from there they appear at the output. This cannot cause any extra noise or distortion at the output of the converter since the second S/H stage is disconnected from the first one during the conversion period, hence the path to the output is broken.

In the layout of this circuit, identical cells are used for the plus (top) and minus (bottom) DACs, however, the bottom one is mirrored around the vertical axis to create a common-centroid topology. Empty space is left around the capacitors to reduce the effect of neighbouring topologies on the critical matching accuracy in the core.

Figure 6.2: Connection between the cyclic DAC core and the first S/H.

The connection between the two single-ended DAC cores and the first S/H stage is shown in Fig. 6.2 (the actual implementation uses two single-ended opamps in place of the differential one). Another layout consideration is minimization of the drain-source fringing capacitance in M_{3N} and M_{3P} . The nodes N2L and N2R are shielded in the best possible way by running grounded metal traces in between them and covering the area with higher level metal wherever they come close to each other.

6.4.2 Pipelined Core

For the higher linearity demanded from the pipelined converter, the unit capacitance is chosen as 1 pF. Since in the pipelined DAC only one unit capacitor delivers the charge to the S/H, the thermal noise of the DAC core is the same as the cyclic one above, i.e. $91 \mu V_{RMS}$, which in terms of power is about $\frac{1}{9}$ of the budget for the whole converter.

Size of the unit capacitor affects the power consumption in the first S/H, and logic gates driving the switches in the pipeline (clock phases). Since the pipelined DAC has many more switches than the cyclic DAC, the digital power is a major contributor to

the overall power. Therefore, it is prudent to keep this capacitor as small as possible, limited only by matching requirements for linearity. Due to lack of prior matching data for this technology, the size of this capacitor could not be optimized.

Figure 6.3: Schematic diagram for the single-ended pipelined DAC cell. Bulk nodes are connected to respective power supplies.

The complete schematic diagram of the single-ended pipeline cell is depicted in Fig. 6.3. Aside from switches S_3 (M_{3P} and M_{3N}) and S_7 (M_{7P} and M_{7N}), the rest of the cell is the same as the one proposed in Chapter 5. The switch sizes on the schematic are optimized through simulation for settling in less than 10 ns ($\frac{1}{4}$ of clock period at 17.6 MHz less non-overlap loss).

The role of the extra switches, and the connection between the pipelined stages and the S/H can be better explained using Fig. 6.4. The implemented pipelined DAC takes advantage of multiplexed last stages (15' and 15'') to relax the speed requirements on the opamp. Switch S_7 is responsible for transfer of charge to the

Figure 6.4: Schematic diagram for the implemented differential pipelined DAC with multiplexed last stages.

S/H. Functionally this switch is needed only in the last stages, however, to achieve perfect drawn matching between all stages of the pipeline, they must be included in all other stages and left open all the time.

The other additional switch, i.e. S_3 is required for multiplexing the last stages. Stage 14, has to engage in charge sharing with both stages 15' and 15''. This demands two CMOS switches connected to alternating last stages. Again, for the purpose of matching between stages (here it is even more critical, because these switches are connected to the top plate of the capacitors, which directly determine the divide-by-2 accuracy), this switch must be included in all other stages as well, but left open. The control logic for stages 14, 15' and 15'' are different from other stages to serve their distinctive needs.

The common-centroid topology cannot be used in a pipelined structure, but other layout techniques, such as maintaining sufficient distance between the critically matched unit capacitors and neighbouring structures, and dummies have been used to help the matching accuracy. Also, heavy shielding between top plate nodes

of unit capacitors (terminals of switches S_2 and S_3) is used to avoid the error caused by C_{DS} .

The power consumption of the pipelined core from each reference voltage source, according to Eq. 2.6, is less than $636 \mu\text{W}$ ($f_S = 17.664 \text{ MHz}$, $V_{\text{ref}+} = 1.5 \text{ V}$, $C = 1 \text{ pF}$, and $N = 16$). If the power is considered coming from the same supply voltage as the DAC, i.e. 5 V , the upper bound on DAC core power is less than 2.12 mW . However, more power is dissipated in the logic that drives the core (to be discussed later).

6.5 Control Logic

The digital section of the DACs consists mainly of a non-overlapping phase generator and data registers. To isolate the noise that is generated on the digital supply rails, it is better to isolate the main section of the control logic circuit from the analog side (core and S/Hs). This isolation is best accomplished using separate power supply metal traces, and even better, by having separate supply pads and pins for the digital circuit. This also allows powering some of the digital circuit from a lower supply voltage to save some power. Also, layout techniques should be used to isolate the noise coupled to the substrate by the logic gates from the analog parts. For example, in a P^- -substrate technology N-Well trenches surrounding both the digital and the analog sections of the converter separately, with substrate contacts inside the ring can reduce the substrate coupling.

If separate supplies are used for the digital and the analog sections, the negative supply pins (V_{SS}) should be shorted externally as close to the chip as possible, and decoupling capacitors for those supplies have to be close as well.

On chip, logic controls are buffered, to clean them up from digital noise as much as possible, before entering the analog domain to control switches. The small CMOS buffers used for this purpose are powered from the analog power supply.

The above guidelines, including separate supply pins, were followed in the design of the cyclic and the pipelined DACs.

6.5.1 Cyclic DAC Logic

The simplified top level diagram of the digital section of the cyclic DAC is shown in Fig. 6.5.

Figure 6.5: Top level schematic diagram of the control logic for the cyclic DAC.

The main controller, which is programmable for variable number of conversion bits (2 to 22 plus sign) and variable length of the sample-and-hold transfer phase, generates timing for the sequence of events during operation. During the S/H *transfer* phase of the last conversion period, new parallel data $D\langle 21:0 \rangle$ is loaded into the shift register from the external data generator. At the same time, the sign bit, and the capacitor select bit (to be explained shortly) are also loaded into the parallel register. During the conversion phase, data is shifted bit-by-bit out of the shift register (LSB first) and is sent to the phase generator and gates block. The sign, and the capacitor select bits are also made available to the same block at the same time.

The capacitor select bit, determines which side (left or right) of the cyclic DAC

core acts as the integrating capacitor in this symmetrical circuit. As discussed before (Chapter 4) this feature has multiple advantages. First, it allows choosing the larger capacitor as the integrating one to make the digital calibration scheme possible. Secondly, it is possible to randomize (and perhaps noise shape to some extent) the mismatch error, by changing the selection for different samples (according to some data dependent fashion).

Another advantage of the capacitor selection feature is to optimize the performance of the converter by partially cancelling the effect of capacitor mismatch with that of C_{DS} , in the absence of digital calibration. According to Eq. 2.25, finite C_{DS} always increases the conversion radix, whereas, depending on the relative values of C_{T1} and C_{T2} , mismatch error increases the radix with one choice and reduces it with the other. By selecting the larger capacitor as the integrating one (which is the same choice as for digital calibration) the mismatch error will be partially compensated for by C_{DS} . In fact, by adjusting the nominal value of C_{DS} to half of maximum capacitor mismatch, and the best capacitor selection, an extra bit can be added to the accuracy of the converter.⁶ Optimization of this fringing field capacitance, however, may require difficult 3 dimensional electric field analysis and simulation, or data from a few manufacturing runs. Nonetheless, some improvement in the performance based on this selection is always possible. Both the digital error correction and the capacitor choice can be programmed either at the Automatic Test Equipment (ATE) test phase, or with some self calibration technique. If complete digital calibration is to be used, C_{DS} has to be minimized.

The non-overlapping phase generator uses a circuit similar to the one in [16, p. 517]. The clock phases generated are then gated with proper controls to create the signals that control the switches.

The digital inputs to the converter ($D<21:0>$, sign, and capacitor select) come

⁶It seems that this non-ideality, if used properly, may not be so bad after all!

from an external data generator. The generator provides a new sample (parallel bits) shortly after each rising edge on its clock (gclk from the main controller). More information on the external setup will be provided in Chapter 7.

6.5.2 Pipelined DAC Logic

The logic section of the pipelined DAC is somewhat simpler than the cyclic one due to the lack of programmability. There is no need to program the number of conversion bit to be any less than what the converter can handle (16 bits plus sign), the unused LSBs can be just set to zero. The sample-and-hold phase duration is also set to the clock period by design (multiplexed last stage), which is optimal. The functions in the pipelined DAC logic are the phase generator, and the pipelined shift register.

Figure 6.6: Schematic diagram of a three-phase non-overlapping phase generator for the pipelined DAC (the actual implementation has four phases).

The non-overlapping phase generator for a three phase clock and its timing di-

agram is shown in Fig. 6.6. The basis for this design is the same as the two phase case. The (partially overlapping) input phases, P_1 , P_2 , and P_3 initiate the end of their respective output phase (ϕ_1 , ϕ_2 , and ϕ_3) on their falling edge. Shortly after, the associated delayed phase ends, which lets the next phase to start after another delay. The delay blocks, Delay1 and Delay3, are made of cascaded slow inverters with nominal delays of 0.4 and 1.2 ns respectively. The actual stretch of the delayed phases and the non-overlap gap are adjusted to about 1 ns each (nominally) including other gate propagation delays and gaps between the input phases.

The actual implementation has a four-phase clock, which uses an extension of Fig. 6.6 for phase generation. The three-phase generator is more efficient in timing and can be used together with the three phase clock generator of Chapter 5 (Fig. 5.8). The superphases that last for one whole clock period (used for the S/Hs) are made in a scheme similar to the cyclic DAC phase generator.

The special shift register for effecting the proper pipeline delay for the digital input is very similar to the original one discussed in Chapter 2 (Fig. 2.6). In the implementation of this chapter, the bits have to be delayed four at a time instead of three, because of the four phase clock. Therefore, a total of 40 flip-flops are needed to realize the suitable delay for the magnitude in this design.

6.6 First S/H Stage

The capacitor ratio in the S/H, shapes its frequency response and affects its noise gain. The larger the C_H/C_S ratio, the lower the noise, and the larger the high frequency droop. These relationships have been captured in Chapter 4. For the first S/H, the sampling capacitor C_S is from the DAC core. In both cyclic and pipelined cases, this capacitor is nominally 1 pF. The holding capacitor was chosen as 0.5 pF in the cyclic DAC, and 1 pF in the pipelined one, because the lower conversion rate in the

cyclic DAC increases its in-band droop. The resulting droop from the first S/H stage at 1 MHz for the cyclic DAC is less than 1.4 dB, and for the pipelined DAC is less than 0.27 dB. Having equal capacitor values for the S/H and the pipelined DAC core also improves the matching accuracy between the capacitors (especially when the capacitors are laid out close) to give a more precise frequency response.

According to a normal practice in switched-capacitor circuit design, to avoid signal dependent charge injection, which due to its nonlinearity may introduce distortion, the switches connected at the input of the S/H opamp (M_{6x} in Fig. 6.1, and M_{2x} or M_{3x} in Fig. 6.3) are opened first. The charge injected into the holding capacitors from these switches is constant (because the channel potential of the switch is at the AG level before it opens) and cannot cause distortion. To establish this switching scheme, S/H phases with delayed turn off are made available by the phase generator.

In this S/H stage, a high-gain opamp is demanded to discharge the nonlinear junction capacitors in the DAC core. To ensure that this factor has a negligible contribution to distortion, a loop gain of around 80 dB is required for the CDAC, and around 90 dB is needed for the PDAC. Such a large DC gain is possible either using gain boosting techniques [65] or a two stage design. The advantage of the gain boosting method is higher bandwidth for the opamp, at the expense of smaller output voltage swing, more complexity, and perhaps more power dissipation. With sufficient settling time allocated for the cyclic DAC, and the advent of multiplexed last stage pipelined DAC, there is no need for very high bandwidth opamps. As a result, a two stage opamp architecture is preferred. Two stage opamps are also more flexible in terms of optimization for speed and noise, because the compensation capacitor is different from load.

The output stage of the opamp can operate in class-A or class-AB. The advantage of class-AB over class-A is lower average power dissipation. A wide output swing is needed from the opamp to help the signal-to-noise ratio (mainly because of the

unity gain of the stage). Class-AB designs with wide output swing are usually slow [66]. The main reason is the extra parasitic poles that are introduced by the higher number of nodes, and the complex compensation schemes. These output stages are also less linear than class-A, especially at high frequencies (due to lower bandwidth). In addition to the previous disadvantages, class-AB opamps in general (regardless of the output swing) are less suitable for integration into large ICs. This is a result of their impulsive supply currents that creates extra substrate noise and larger ripples on the power supply rails. Therefore, despite their higher power dissipation, class-A opamps are used for all the S/Hs and the continuous-time reconstruction filter.

The opamp bandwidth for the first S/H stage has to be adjusted carefully. While the speed must be enough to achieve sufficient settling accuracy (less than 0.01% assumed) within the S/H phase, too high bandwidth for the opamp increases the folding factor for out-of-band ($> fs/2$) noise of the opamp into the baseband. Due to process and temperature variations, some overdesign is needed. This will inevitably degrade the noise performance.

6.6.1 Cyclic DAC First S/H

The first S/H in the cyclic DAC consists of the switches that are already included in the DAC core (M_{5xx} and M_{6x}), two single-ended opamps, and two holding capacitors. The connection is shown in Fig. 6.2 in a differential form.

The cyclic DAC is designed using single-ended opamps in place of differential ones. This design is not optimal in terms of noise and power, nonetheless, has some advantages. Aside from ease of implementation, single-ended opamps are faster than differential ones. This is mainly because of lack of a Common-Mode Feedback (CMFB) circuit, which imposes its own stability limitations. Since CMFB is usually slower and has less gain compared with the differential path, the balance (symmetry) in differential opamps is not as good as two single-ended ones. On top of all this, the

two single-ended circuits allow experimenting on a complete single-ended implementation (which may have acceptable performance for some applications), and helps in debugging the chip, should unexpected behaviour occur. For a general application, however, a true differential implementation (like the pipelined DAC in this work) is recommended.

Figure 6.7: Schematic diagram of the single-ended opamp used in the S/H stages of the cyclic DAC.

The opamp is a two-stage design with a single-ended folded cascode in the first stage, displayed in Fig. 6.7. The typical differential cascode has 6 dB higher gain, but that is not required here. The opamp is powered from a 3 V supply, and is biased by the bias voltage generators that drive vbi and vbo pins. The voltages are set by external current sources for flexibility in testing.

For sufficient settling accuracy, each $30\mu/4\mu$ finger of the PMOS transistors biased by the vbi pin should carry $13.6\mu\text{A}$, and each $18.7\mu/1.2\mu$ finger of the PMOS in the output stage delivers $14.7\mu\text{A}$. With these bias conditions, the simulated performance

of the opamp in a differential configuration is summarized in Table 6.1.

Parameter	Value
DC Gain	80 dB
Open-Loop Unity-Gain Bandwidth	30 MHz
Slew Rate	70 V/ μ s
Input Referred Thermal Noise at 1 MHz	46 nV/ $\sqrt{\text{Hz}}$
Output Sampled Noise in Baseband	350 nV/ $\sqrt{\text{Hz}}$
Current Consumption	590 μ A

Table 6.1: Simulated performance of the first S/H stage opamps for the cyclic DAC in a differential configuration.

The disappointing figure in the opamp performance is the noise. There are two components to the sampled output noise, thermal noise within the loop bandwidth of the opamp, and the WOLBW noise.

The input referred noise within the loop bandwidth (0 to 24 MHz) is almost constant with an average of about 50 nV/ $\sqrt{\text{Hz}}$.⁷ The transfer function for this noise is given by Eq. 4.20, and is plotted in Fig. 6.8 for typical values of $C_H = 0.5$ pF, $C_S = 1$ pF, and $C_I = 0.3$ pF. The maximum noise gain is around 1 dB, and its average value across the baseband is below 0.46 dB. With this gain, the differential noise level in the baseband originating from within the loop bandwidth component after folding 11 times is 174 nV/ $\sqrt{\text{Hz}}$.

The WOLBW noise is very large for this opamp due to its small compensation capacitance. In this case the noise in the second stage dominates, and the total noise at the output of the opamp has a typical value of 445 μ V_{RMS} (differential). This noise is very slightly increased by being sampled also on C_H (as explained in Appendix C) and the total noise power from this source as sampled by the next stage, according to Eq. C.43, is $1.021 \times 445 = 454$ μ V_{RMS}. The baseband density of this noise is about

⁷No flicker noise model was available for this technology.

Figure 6.8: Magnitude of the transfer function for the input referred noise of the opamp in the first S/H of the implemented cyclic DAC. Edge of the baseband is marked with the dashed line.

304 nV/ $\sqrt{\text{Hz}}$.

The main reason for large noise from this opamp is the use of PMOS input transistors with low g_m . Enlarging the PMOS transistors for increased g_m reduces the bandwidth (due to their larger parasitic capacitance), unless more power is dissipated. PMOS transistors were used because of their lower flicker noise level, and due to lack of any flicker noise parameter from the technology, it was a conservative approach. Usually, the flicker noise is not a major factor for high-speed DACs, and use of NMOS input transistors allows much less thermal noise from the input transistors, and also much less WOLBW noise from the output stage as well. The reason for reduced WOLBW noise with NMOS input stage is the use of larger compensation capacitance for high g_m NMOS transistors at the input. As discussed at the beginning of this chapter, this design is by no means optimal for low thermal noise performance.

The noise from the on-resistance of the switches according to Eq. C.48 is 9.4 μV_{RMS} for $B_{\text{lp}} = 24 \text{ MHz}$ and $R_{\text{on}} = 2 \times 1000 \Omega$ (factor of 2 for differential), which

is negligible. Finally, the switched-capacitor thermal noise based on Eq. C.51 is $42.9 \mu\text{V}_{\text{RMS}}$ (negligible again). The overall noise from the first S/H is $352 \text{ nV}/\sqrt{\text{Hz}}$, which is entirely dominated by the opamp.

6.6.2 Pipelined DAC First S/H

The connection for the first S/H stage for the pipelined DAC is shown in Fig. 6.4. The capacitor values C_S , C_H , and C_I for this stage are 1 pF, 1 pF and 1.2 pF respectively. The opamp designed for this converter is a fully differential two stage opamp with internal CMFB as shown in Fig. 6.9. The two stage design allows resistive loading for the opamp, which makes it possible for CMFB circuit to use a resistor divider to sense the common-mode output voltage (unlike single-stage opamps).

Figure 6.9: Schematic diagram of the differential opamp used in the pipelined DAC.

Combination of a folded cascode first stage and the second stage results in high DC gain for the opamp which is required for good linearity in charge transfer from the nonlinear junction capacitors. The opamp also features switchable compensation for

operation at 17.664 MSps and 8.832 MSps conversion rates. Unlike the cyclic DAC, there is less flexibility in setting the bias current for the two stages in the opamp, the overall bias is set by the bias cell which sinks 20 μA under nominal conditions.

Parameter	Value
DC Gain	112 dB
Open-Loop Unity-Gain Bandwidth	80 MHz
Slew Rate	62 V/ μs
Input Referred Thermal Noise at 1 MHz	5.7 nV/ $\sqrt{\text{Hz}}$
Output Sampled Noise in Baseband	54 nV/ $\sqrt{\text{Hz}}$
Current Consumption	1.61 mA

Table 6.2: Simulated performance of the first S/H stage opamp for the pipelined DAC.

The performance of the opamp for the first S/H stage is tabulated in Table 6.2. Better results for DC gain, speed, and noise are the consequences of a more elaborate design. However, power dissipation is also significantly higher for this design (higher supply voltage as well as larger current).

The sampled output noise is calculated in a similar manner to the cyclic DAC. For the closed loop bandwidth of 46 MHz and an average gain 0.87 dB in the baseband, the WILBW noise is $42.7 \mu\text{V}_{\text{RMS}}$, and the WOLBW noise from the opamp is found to be $145 \mu\text{V}_{\text{RMS}}$ which after slight increase (according to Eq. C.43) becomes $1.061 \times 145 = 154 \mu\text{V}_{\text{RMS}}$. The overall sampled noise from this opamp is $160 \mu\text{V}_{\text{RMS}}$, or approximately 54 nV/ $\sqrt{\text{Hz}}$.

Another noise contributor in this stage is the on-resistance of the switches which according to Eq. C.48 for total R_{on} of 800 Ω and B_{lp} of 46 MHz is only $8.7 \mu\text{V}_{\text{RMS}}$ differentially. The sampled thermal noise on the capacitors (Eq. C.51) is $43.6 \mu\text{V}_{\text{RMS}}$ (differential). The overall noise from this stage is the sum of opamp, R_{on} , and SC noise, which is approximately $166 \mu\text{V}_{\text{RMS}}$, or 56 nV/ $\sqrt{\text{Hz}}$.

6.7 Second S/H Stage

The essential difference between the second S/H and the first one is the presence of the linearizing resistors. These resistors, as discussed in Chapter 4, are there to relax the slew rate, and bandwidth requirements on the opamps. The total resistance in series with the sampling capacitor C_S in the transfer phase has to be large enough to ensure no slew rate limitation by the opamp. If the largest step size at the output is ΔV_{out} , then the slew rate of the opamp has to be larger than $\Delta V_{\text{out}}/\tau$ to accommodate this step without having any nonlinearity caused by its slew rate limitations.

A study of the intended input signal to the DAC for a given application is needed to determine the maximum value of ΔV_{out} for a given sampling rate. In the case of a Discrete Multitone (DMT) signal used in DSL applications, investigations indicate a maximum step size of less than 0.44% of the peak at the input for the cyclic DAC, and less than 0.22% for the pipelined DAC.⁸ The output step size is further reduced by the first and the second S/H stages' low-pass filtering action. For a conservative design, this filtering function may be ignored and the maximum output step is assumed equal to the input one.

In order to avoid excessive noise accumulation in the baseband, the value of the linearizing resistors should not exceed $\frac{1}{2f_s C_{\text{eq}}}$, where C_{eq} is the series combination of C_S and C_H (see Appendix C for CT noise in the third architecture).

6.7.1 Cyclic DAC Second S/H

This S/H stage uses a 2 pF sampling capacitor and a 0.5 pF holding capacitor. The large value of $a = \frac{C_S}{C_H} = 4$ results in less droop in the baseband by this S/H with the

⁸For the G.Lite case, i.e. 138 kHz to 552 kHz bins, sampling rate of 4.416 MSps is assumed, and for the full rate band of 138 kHz to 1104 kHz, 17.664 MSps is used.

DT frequency response of

$$H(z) = \frac{4z^{-1}}{5 - z^{-1}}, \quad (6.1)$$

(assuming complete settling).

An identical opamp to the first S/H stage is used in this stage, but with different biasing. The transient linearity of the opamp in this stage is improved by increasing the bias current to the input stage, i.e. from $13.6 \mu\text{A}$ to $44 \mu\text{A}$. Since the output stage of this opamp does not deliver charging current to the capacitors, its bias can be cut down to $8.4 \mu\text{A}$.

Parameter	Value
DC Gain (with CTRCF Loading)	74 dB
Open-Loop Unity-Gain Bandwidth	80 MHz
Slew Rate	220 V/ μs
Input Referred Thermal Noise at 1 MHz	24 nV/ $\sqrt{\text{Hz}}$
Current Consumption	670 μA

Table 6.3: Simulated performance of the second S/H stage opamps for the cyclic DAC in a differential configuration.

The performance of the opamp in this stage is listed in Table 6.3. With the improved 240 V/ μs slew rate, and a maximum step size of $0.44 \times 2.5 = 1.1 \text{ V}$, a minimum of 5 ns for $R_S C_{\text{eq}}$ time constant is allowable. However, to have a more robust design, $\tau = 8.6 \text{ ns}$ was chosen with $R_S = 20.6 \text{ k}\Omega$ (excluding switch resistance). The maximum value for R_S , determined by noise performance, is 283 k Ω and is far from being reached.

The input referred thermal noise of the opamp, according to Eq. C.55, sees an effective gain of 1.6 V/V with $C_t = 0.3 \text{ pF}$, hence when referred to the output the noise density is 38.4 nV/ $\sqrt{\text{Hz}}$.

The conservative overestimate for the combined noise of all the switches and R_S as given by Eq. C.60 is 106 nV/ $\sqrt{\text{Hz}}$. After adding the opamp noise, the overall noise

of this stage is $113 \text{ nV}/\sqrt{\text{Hz}}$.

6.7.2 Pipelined DAC Second S/H

This S/H stage has a 1 pF equal sampling and holding capacitors, and uses a similar opamp to the first S/H stage, but with larger bias for driving resistive loads and improved CT linearity using source degeneration resistors for the input differential pair.

Parameter	Value
DC Gain	106 dB
Open-Loop Unity-Gain Bandwidth	99 MHz
Slew Rate	75 V/ μs
Input Referred Thermal Noise at 1 MHz	4.9 nV/ $\sqrt{\text{Hz}}$
Current Consumption	2.45 mA

Table 6.4: Simulated performance of the second S/H stage opamp for the pipelined DAC.

The opamp's simulated characteristics is presented in Table 6.4. With the $75 \text{ V}/\mu\text{s}$ slew rate, and a maximum step size of $0.22 \times 3 = 1.32 \text{ V}$, minimum value for $R_S C_{\text{eq}}$ time constant is 8.8 ns . However to have more margin $\tau = 15 \text{ ns}$ was selected with $R_S = 30 \text{ k}\Omega$ (excluding switch resistance). To avoid degrading the noise performance R_S has to be less than $56.6 \text{ k}\Omega$.

The input referred thermal noise of the opamp after a gain of 2.2 (Eq. C.55) to the output contributes $10.8 \text{ nV}/\sqrt{\text{Hz}}$.

The overall noise of all the switches and R_S according to Eq. C.60 can be approximated to $53 \text{ nV}/\sqrt{\text{Hz}}$, which makes the combined noise of this S/H stage (including the opamp) $54 \text{ nV}/\sqrt{\text{Hz}}$.

A first order $\Sigma\Delta$ modulator is implemented in the second S/H stage of the pipelined DAC according to the schematic diagram of Fig. 4.31. The design is fairly

straight forward. The comparator needed for this design is very simple, as in any $\Sigma\Delta$ A/D converter in general. The schematic diagram of this comparator is shown in Fig. 6.10. The large bias current in the input differential pair provides the speed, and the output is converted to a latched digital control in the D flip-flop. The power consumption of this comparator is not critical either, since it is powered up only during the initial calibration period.

Figure 6.10: Schematic diagram of the comparator in the second S/H stage of the pipelined DAC.

6.8 Continuous-Time Reconstruction Filter

In order to attenuate the images left over by the second S/H, a Continuous-Time Reconstruction Filter (CTRCF) usually follows the DAC. This filter is actually a part of the larger system that the DAC is used in, and not a section of the DAC itself. In fact, the smoothing function of the linearizing resistors in the second S/H stage may ease the requisite response of the CTRCF. Depending on the system requirements, on-chip RC components may or may not be used for this low-pass filter due to their large

variations. In the absence of given system requirements for this filter, a simple second-order Butterworth active RC LPF was implemented on the converter test chips. Low-pass filtering right after the DAC, also relaxes the requirements for very high-speed linearity of the succeeding stages. It is usually much harder to maintain good linearity with (relatively) sharp transitions coming immediately out of the second S/H stage.

6.8.1 CTRCF for Cyclic DAC

Similar to the S/Hs, this stage makes use of two single-ended opamps, rather than a true differential one. Indeed, the opamps are identical to the ones used in the S/Hs, but with different biasing. In a general case, opamps should be optimized for each stage. The circuit is shown in Fig. 6.11.

Figure 6.11: Single-ended schematic diagram of the continuous-time reconstruction filter following the cyclic DAC.

The filter is a modified Sallen-Key design with the opamp inputs at the ground level, hence not requiring large input voltage range for the opamp (unlike the one in [67]). Keeping the inputs of the opamp at the ground level also improves the linearity of the circuit considerably.

The transfer function of this filter is given by

$$H(s) = \frac{-A_{DC}}{1 + \frac{1}{\Omega_0 Q}s + \frac{1}{\Omega_0^2}s^2}, \quad (6.2)$$

where

$$A_{DC} = \frac{R_3}{R_1}, \quad (6.3)$$

$$\Omega_0 = \frac{1}{\sqrt{C_1 C_2 R_2 R_3}}, \quad (6.4)$$

and

$$Q = \frac{R_1 \sqrt{C_1 C_2 R_2 R_3}}{C_2 (R_1 R_2 + R_2 R_3 + R_1 R_3)}. \quad (6.5)$$

Setting $R_3 = R_1 = 2R_2$ and $C_1 = 4C_2$, results in

$$A_{DC} = 1, \quad (6.6)$$

$$\Omega_0 = \frac{\sqrt{2}}{4C_2 R_2}, \quad (6.7)$$

and

$$Q = \frac{1}{\sqrt{2}}, \quad (6.8)$$

which is the transfer function for a second-order Butterworth LPF.

The values used in the implementation were $R_1 = R_3 = 10.36 \text{ k}\Omega$ and $R_2 = 6.2 \text{ k}\Omega$ and $C_1 = 15.64 \text{ pF}$ ⁹ and $C_2 = 3.91 \text{ pF}$. The resulting filter parameters are $A_{DC} = 1$, $\Omega_0 = 15.93 \text{ Mrad/s}$ ($f_0 = 2.53 \text{ MHz}$), and $Q = 0.704$. Slightly lower Q factor helps to reduce the small peaking in the response of the filter close to its cutoff frequency caused by the finite bandwidth of the opamp.

The bias for the input transistors is set to $14.7 \text{ }\mu\text{A}$ for each $30\mu/4\mu$ finger biased by v_{bi} , and $13 \text{ }\mu\text{A}$ for each $18.7\mu/1.2\mu$ PMOS finger in the output stage. With this biasing arrangement, the overall current consumption by the opamp is $660 \text{ }\mu\text{A}$.

The input referred noise of the opamp goes through a gain of 2 to reach the output. The average differential thermal noise density of the opamp at the output is $80 \text{ nV}/\sqrt{\text{Hz}}$. The thermal noise from R_2 resistors also sees a gain of 2 V/V, whereas the others have a gain of 1. Therefore, the total effective differential noise resistance is about $91 \text{ k}\Omega$ which generates a noise density of approximately $39 \text{ nV}/\sqrt{\text{Hz}}$ at

⁹ C_1 was actually made of two 3.91 pF capacitors in parallel differentially.

room temperature. The total baseband noise density from this differential stage is $89 \text{ nV}/\sqrt{\text{Hz}}$, which is negligible compared with the S/H noise.

6.8.2 CTRCF for Pipelined DAC

A fully differential version of the cyclic DAC CTRCF has been included in the pipelined DAC test chip. Use of a fully differential opamp helps reducing noise.

The corresponding resistor values are $R_1 = R_3 = 8 \text{ k}\Omega$ and $R_2 = 4 \text{ k}\Omega$, and the capacitors were both set to 7.03 pF (C_1 is differentially connected). The resulting DC gain is 1, and the cutoff frequency is 2 MHz with $Q = 0.707$.

Since the opamp has to drive larger resistive loads, the bias is boosted and the supply current is increased to 3 mA . The input referred noise of the opamp is $9 \text{ nV}/\sqrt{\text{Hz}}$, which goes through a gain of 2 to the output. The total effective resistance of $64 \text{ k}\Omega$ adds another $32 \text{ nV}/\sqrt{\text{Hz}}$ to a sum of $36.7 \text{ nV}/\sqrt{\text{Hz}}$ for the whole stage.

6.9 Overall Simulated Performance

The simulated performances of the complete DACs are summarized in this section.

6.9.1 Cyclic DAC

Table 6.5 shows a summary of the cyclic DAC simulated performance. Noise in the digital block refers to the quantization noise of a 14-bit digital signal at $f_S = 4.416 \text{ MHz}$.

Again, a significant part of the total power is consumed in the digital section. This dissipation is a combination of simulation and estimation, and can be substantially reduced by optimizing the sizes of digital gates. According to simulation, the flip-flops used are 3 to 4 times faster than needed. About 2.5 mW of the digital power is dissipated in the phase generator and gates, and the rest in the shift registers and

Contributor	Noise (nV/ $\sqrt{\text{Hz}}$)	Power (mW)	Droop at 552 kHz (dB)
Digital	59	5.82	—
DAC Core	61	< 0.11	—
First S/H Stage	352	1.77	1.58
Second S/H Stage	113	2.01	0.96
CTRCF	89	1.98	0.01
Total	390	11.67	2.55

Table 6.5: Simulated performance of the complete differential cyclic DAC.

controller. The capacitive loading of large busses throughout the test chip and the extra logic for programmability, which adds to the power dissipation, is not included here.

Figure 6.12: Magnitude of the frequency response for the cyclic DAC.

Frequency response of the cyclic DAC is shown in Fig. 6.12. Although the droop due to CTRCF is substantially less than the S/Hs, it may not be possible to reduce the cutoff frequency of this filter by much because of its large process variations (unless some kind of post-manufacture calibration is implemented).

Layout Photograph The size of a complete cyclic DAC including its CTRCF is 0.22 mm^2 , and a layout view of an implemented cyclic DAC is shown in Fig. 6.13. A microphotograph of the die with 7 cyclic DACs on it is shown in Fig. 6.14.

Figure 6.13: A layout view of an implemented cyclic DAC.

Figure 6.14: Microphotograph of the implemented cyclic DACs.

6.9.2 Pipelined DAC

Simulated performance of the pipelined converter is shown in Table 6.6. The quantization noise (digital) for a 17-bit resolution at $f_s = 17.664 \text{ MHz}$ is negligible. Power dissipation numbers do not include the comparator in the second S/H, which is powered only during calibration.

More than one third of the total power is consumed by the digital section. The numbers are estimations based on some simulation, because complete simulation of

Contributor	Noise (nV/ $\sqrt{\text{Hz}}$)	Power (mW)	Droop at 1104 kHz (dB)
Digital	4.5	22.5	—
DAC Core	31	< 2.1	—
First S/H Stage	56	8.1	1.15
Second S/H Stage	54	12.3	1.26
CTRCF	37	15.0	0.16
Total	92	60.0	2.57

Table 6.6: Simulated performance of the complete pipelined DAC.

the digital section for a long data sequence with the available tools was impractical. The power consumption in digital section can be reduced through the use of low-power logic cells (especially flip-flops), and lower supply voltage.

Figure 6.15: Magnitude of the frequency response for the pipelined DAC.

The overall frequency response of the pipelined DAC is shown in Fig. 6.15.

Layout Photograph The area taken by a complete pipelined DAC including the CTRCF is 1.1 mm², a layout view of one pipelined DAC is shown in Fig. 6.16. A microphotograph of the test chip including 4 pipelined DACs is shown in Fig. 6.17.

Figure 6.16: A layout view of an implemented pipelined DAC.

Figure 6.17: Microphotograph of the implemented pipelined DACs.

6.10 Conclusion

Cyclic and pipelined DACs have been designed and implemented on silicon to permit experimental verification of the ideas presented in this thesis. The goal of these implementations is to verify the new concepts, as opposed to presenting perfect designs. Nonetheless, the designed circuits have been analyzed and simulated to allow correlation between the expected performance and the measured one. Testing of the fabricated circuits and the results of these measurements are discussed in the next chapter.

Chapter 7

Experimental Results

The cyclic and pipelined DACs designed in Chapter 6, have been fabricated and tested. The metrics of Appendix A are applied to these DACs to evaluate their DC and AC performance. The results of these measurements and analysis are presented in this chapter.

The test setups used for evaluation of the DACs are very critical in providing an accurate view of the converters capabilities. For high-speed high-linearity converters, it is always a challenge to prepare the equipment that can have the required accuracy. The difficulties are more important for the AC measurements.

In this chapter, first the test setups for the DC and the AC measurements are explained, and then the measured characteristics of the cyclic and pipelined DACs are given.

7.1 Test Setup

The test setup includes the evaluation or test board, with the Device Under Test (DUT) mounted on it, and the rest of the equipment surrounding the board that provide power and test signals to the DUT, and also analyze DUTs response.

7.1.1 Test Board

Generally, an evaluation board is required for the converter to be characterized on. The test board design for data converters is particularly critical due to inevitable parasitic couplings.

Proper isolation of the analog and digital sections of the board helps reducing some of the unwanted couplings. In order to separate the noise of the digital impulse currents from the sensitive analog signals, it is advisable to split the ground and power planes of the Printed Circuit Board (PCB) into digital and analog sections. Since the digital and analog supplies are also isolated on the chip, these two planes must be joined very close to the DUT supply pins to allow for a return path for the supply currents of the on-chip digital gates driving analog circuit. Also, in the same neighbourhood, the supply decoupling capacitors should be placed to provide maximum regulation of the power supply voltages.

The differential architecture also improves noise immunity to a great extent. The very same design should be followed on the test board, and as much as possible, throughout the whole test equipment. The differential paths should be close to each other to prevent electromagnetic fields from inducing differential noise. The common-mode noise is substantially reduced by the common-mode rejection of the differential circuits.

The traces on the test board should be kept as short as possible. The transition time on digital signals should not be made too small, because the low output resistance of the drivers mismatches the line impedance of the metal trace (usually around 70 Ω) and multiple reflections that result may cause false data transfer. Alternatively, external termination (damping) resistors may be added to the fast output drivers.

7.1.2 Test Equipment

Few test instruments in today's market have performance close to that of the converters to be tested, let alone performance better enough to yield the accuracy needed for measuring the characteristics of the DUT. This limitation especially makes the AC measurements difficult.

DC Test Equipment

The DC characteristics of the DACs is evaluated by measuring the corresponding DC output levels for all digital input codes. Then, the linearity, gain, and offset can be obtained.

Figure 7.1: Block diagram of the test setup for DC characterization of the DACs.

The setup for measuring DC output voltages of the DACs is shown in Fig. 7.1. Under control of a host workstation and its software, the FPGA Interface for Signal

Handling (FISH — see Appendix E) is programmed to send a sequence of digital codes to the DUT, and the output levels are measured by a voltmeter. The voltmeter has a buffer memory to hold the measured values, and sends a trigger output called “Voltmeter Complete” to the FISH to advance the digital code. In order to reduce the power line noise in the measured voltages, the voltmeter must integrate its input in an integral multiple of the Power Line Cycle (PLC). Only 1 PLC is usually sufficient for the required accuracy. With PLC of 1, about 50 readings can be made in a second, which results in more than 6 minutes of test time for 16k levels (14 bits).

The DUT continuously converts the digital input codes, and receives its clock from a pulse generator. The reference voltage for the DAC is supplied by an external voltage source (Keithley 2400 SourceMeter). Since the test time is more than 6 minutes, very low frequency noise of the voltage source (which cannot be practically removed by filtering) may degrade the measurement accuracy. The voltmeters, however, have been found to have less input referred noise by about two orders of magnitude. Therefore, to compensate for slow reference voltage variations, V_{ref} is simultaneously measured by another voltmeter, and the ratio of the DAC output voltage and V_{ref} is calculated for each sample.

The digital signal to the converter (D<21:0>, sign, and capacitor select) should come from an external data generator. The standard equipment for such functions is a digital pattern generator in a logic analysis system.¹ This instrument takes the clock from the test setup and delivers a new sample. It is also capable of repeating a pattern after reaching its end. There are a few limitations in this equipment that justify the search for a better one. The large unspecified delay in the long cable assembly, requires calibration for different clock frequencies. The amount of available sample memory is limited (in case of HP16522 to less than 256 kSamples). Independent control of device program inputs and the pattern generator is not possible using only

¹For example, HP16522 pattern generator in HP16500 logic analyzer from Hewlett-Packard.

one pattern generator card, despite availability of sufficient number of bits. Also, transfer of data through GPIB for some of these devices is very slow.

AC Test Equipment

Measuring distortion level and signal-to-noise ratio of high-resolution D/A converters requires a large dynamic range from the measuring instrument. For example, if the third harmonic distortion caused by the measurement system is 10 dB below the same harmonic distortion caused by the DUT, it can degrade the measured distortion by as much as 2.4 dB (in the worst case, distortion contributions add in voltage). Flat noise floor of the measuring instrument contributes less significantly and is easier to subtract. As a similar example, 10 dB lower noise floor in the instrument compared with the DUT contributes only about 0.4 dB to the measured *SNR* (independent noise contributions always add in power).

The signal-to-noise ratio and harmonic distortion of the target application is too stringent to be evaluated by off-the-shelf instruments. There is a strong need to build a specialized tester for this purpose. A 16-bit A/D converter from Analog Devices, AD9260, offers a better *SNR* and *THD* than the D/A converters designed in this work. A modified evaluation board for this device together with a FISH board is used as an FFT analyzer. This custom instrument delivers *SFDR* $\approx$ 90 dB and *SNR* $\approx$ 86 dB in a 1.1 MHz bandwidth for full-scale at 1 MHz. Maximum sampling rate for this converter is 20 MHz.

The test setup for AC characterization is shown in Fig. 7.2. A FISH board is used to supply the digital signal to the DUT in a continuous loop. A divided clock frequency runs AD9620EB at an appropriate speed (usually 17.664 MHz) locked to the DUT clock (70.656 MHz or 35.228 MHz). Since both clocks are derived from the same source, the phase noise of the oscillator is cancelled in the system, and if the A/D and D/A cycle times are equal, FFT bins match and no spectral leakage occurs.

Figure 7.2: Block diagram of the test setup for AC characterization of the DACs.

The test signals are generated by the computer software (Matlab) and the results are also analyzed with the same tool.

7.2 Cyclic DACs

The cyclic DACs designed and implemented in CMC's (TSMC) 0.35- μm CMOS technology are tested under the nominal conditions listed in Table 7.1. These conditions have been applied to all DC and AC measurements.

Out of a total of 10 packaged chips, only 8 were functional which have been used for collecting statistics on the performance.

Parameter	Value
Analog and Digital Supply Voltage	3 V
Positive Reference Voltage	2.75 V
Analog Ground Voltage	1.5 V
Negative Reference Voltage	0.25 V
Bias Currents	Same as Simulation
Clock Frequency	70.656 MHz
Magnitude Bits	13
S/H Clock Cycles	4
Total Conversion Clock Cycles	16
Conversion Rate	4.416 MSps
Temperature	Room

Table 7.1: Nominal test conditions for the cyclic DACs.

7.2.1 DC Characteristics

From the DC measurement of all DAC output levels (16383), offset, gain, and DC linearity can be derived.

Distribution of the DC offset and DC gain for the 8 functional devices are shown in Fig. 7.3. Offset is mainly caused by the input offset of the opamps (six single-ended opamps), especially the CTRCF opamps with a gain of 2 for their input offset. The mean value of the offset is 3.8 mV, and its standard deviation is 8.7 mV. The maximum offset is less than 1% of the range. The gain has a mean value of 0.9971 V/V, with a standard deviation of 0.45%.

The DC gain is within 1% of its target. Since the DC gain of the S/Hs is 1 by definition (ignoring the effect of finite DC opamp gain which is less than 0.01% typically), the gain inaccuracy is almost entirely due resistor mismatch in the CTRCF network and the interconnect.

The flexibility of choosing the sampling and integrating capacitors in the cyclic DACs allows optimization of DC linearity performance. The linearity plots for a

Figure 7.3: Distribution of the measured DC offset and gain for the cyclic DACs.

typical cyclic DAC with its left or right capacitors as the sampler are shown in Fig. 7.4 and 7.5 respectively.

From these plots it is apparent that the fringing field capacitor (C_{DS}) helps linearity for the left sampling capacitor, and hurts it for the right sampling capacitor (see Eq. 2.25). In other words, C_{DS} partially compensates for the smaller left sampling capacitor.

The distribution of the *DNL* and *INL* for all samples are shown in Fig. 7.6 and 7.7 for left and right sampling capacitors respectively. From these plots it is visible that the choice of left capacitor for sampling results in a better performance for all devices. This is an indication that the left capacitor is smaller than the right one in all 8 samples. After careful inspection of the layout, it is revealed that there is a minor asymmetry between the parasitic metal-to-metal capacitance of the left and right sides of the cyclic DAC resulting in a systematic mismatch between the sides.

Figure 7.4: DC linearity of a typical cyclic DAC with the sampling capacitor on the left.

Figure 7.5: DC linearity of a typical cyclic DAC with the sampling capacitor on the right.

Figure 7.6: Distribution of DC linearity for the cyclic DACs with the sampling capacitor on the left.

Figure 7.7: Distribution of DC linearity for the cyclic DACs with the sampling capacitor on the right.

7.2.2 AC Characteristics

The signal and noise levels are better explained in dB terms relative to a common reference level. The reference level may also be defined in the digital domain to have an easy correspondence between analog and digital signals.

The reference level, denoted by 0 dBr, in the analog domain is defined as the power of a sine wave with the largest possible magnitude and a DC value of 0. This corresponds to a peak value of $V_{\text{ref}+} - V_{\text{ref}-}$, i.e. 2.5 V for the cyclic DACs.

For a 13-bit plus sign cyclic DAC, the digital 0 dBr amplitude is 111111111111 in binary integer format. For the sake of simplicity, binary point is considered at the left of the MSB for AC signals, which sets the maximum amplitude (very close) to 1 independent of the resolution. Therefore, 0 dBr in digital is the power of a sine wave with the amplitude of 1 regardless of the resolution.

Idle-Channel Noise

With a zero digital input, the output noise power of the cyclic DAC between 100 kHz and 300 kHz is measured to be at -82.2 dBr. For the same bandwidth, the noise power of the measuring system (grounded probe input) stands at -93.6 dBr. The difference of $132 \mu\text{V}_{\text{RMS}}$ which is the contribution of the DUT, when spread over a 200 kHz bandwidth, results in a noise floor of $294 \text{ nV}/\sqrt{\text{Hz}}$. This is not in a very good agreement with the analysis and simulation results as per Table 6.5 ($390 \text{ nV}/\sqrt{\text{Hz}}$). Since most of the noise is contributed by the thermal noise of the devices in the opamps, accuracy of the short channel device models and process variation may be the cause of this difference. The transconductance (g_m) of MOS transistors (hence their thermal noise) is very process dependent and requires accurate modeling. There was also some overestimation in the calculation of noise. Nonetheless, the measured noise is somewhat lower than the initial design specification of $340 \text{ nV}/\sqrt{\text{Hz}}$.

Single-Tone

A typical cyclic DAC with a 0 dBr input at 100 kHz produces the output shown in Fig. 7.8. For a bandwidth of 552 kHz, the *SNR* stands at 76.6 dB, the total-harmonic distortion is at -78.4 dBr, the *SNDR* is 74.4 dB, and *SFDR* = 79.2 dB.

Figure 7.8: Single-tone response of a typical cyclic DAC.

Two-Tone

A typical two-tone response of the cyclic DAC with -6 dBr inputs at 547.7 kHz and 552 kHz is shown in Fig. 7.9. The maximum third order intermodulation distortion, *IM3*, is at -77.4 dBc on this plot. The *IM5* is 3 dB lower at -80.4 dBc.

Multi-Tone

A multi-tone performance of a typical cyclic DAC with an input power of -11.5 dBr and tones spaced at 4.3125 kHz from 138 kHz to 552 kHz with a missing tone at 345 kHz is plotted in Fig. 7.10. The *MTPR* for the missing bin is at 71.6 dBc.

Figure 7.9: Two-tone response of a typical cyclic DAC.

DMT

As proposed in Appendix A, the best performance metric for DSL applications is a finely spaced picket-fence signal that best resembles the actual QAM modulated DMT signal ([14, 15]). With that methodology, the cyclic DACs have been tested, and a typical response is presented in Fig. 7.11.

The total power of noise and distortion in the missing bin at 345 kHz is 65.0 dB below the signal power in the neighbouring bin, i.e. $SNDR_{DMT} = 65.0$ dB for this converter. It is apparent that the thermal noise contributes most of this noise power, because the *MTPR* parameter is higher.

Frequency Response

A typical frequency response of the cyclic DAC is shown in Fig. 7.12. According to this plot, measurement data is in close agreement with the theoretical calculations.

Figure 7.10: Multi-tone response of a typical cyclic DAC with magnified missing bin.

Power Dissipation

The current from the analog power supply is easily measured at 1.9 mA, which is equivalent to 5.7 mW.

A large part of the digital block on the implemented cyclic DACs is shared between 7 DACs. Long digital bus running on the chip increases the power consumption from the digital supply pin. With this fact in mind, the current into the digital power supply at nominal clock frequency is 3 mA. The conservative estimate for the dissipation for one DAC is 2 mA, which results in 6 mW of power. Therefore, power dissipation for the entire converter is under 12 mW (10 mW without the CTRCF).

Digital Calibration

The first-order $\Sigma\Delta$ was not implemented in the second S/H of the cyclic DACs that have been tested, hence, readings from a multimeter have been used to measure the critical output values of the cyclic DACs. The algorithm suggested in Chapter 4 (based on the calculated *DNLs* from multimeter measurements) was used to calibrate (predistort) the digital input to the DACs.

Figure 7.11: Response of a typical cyclic DAC to a fine picket-fence for measuring $SNDR_{DMT}$. The missing bin is magnified.

After digital calibration, the DAC under test (the same one with the above *typical* characteristics) is still programmed for a 13-bit (plus sign) resolution. Only the 7 largest DNL s on the magnitude are treated (8 magnitude segments). The total number of memory bits needed in this example was 12, although larger memory size may be needed in a general implementation.

The DC linearity plots after calibration are shown in Fig. 7.13. The improvement over Fig. 7.4 is significant. A factor of 5 reduction in the maximum DNL and a factor of 3 reduction in maximum INL are results of this calibration.

Since the converter still runs as a 14-bit DAC (including sign), it is not possible to have a better performance than a true 13-bit linearity. Some further improvements have been observed in higher resolution modes, but that requires a change in the conversion rate.

The dynamic performance of the cyclic DAC also serves as a good indication of the effectiveness of the digital calibration scheme. The multi-tone test was repeated for the same DAC after calibration, and the results are recorded in Fig. 7.14.

In comparison with the response before calibration (Fig. 7.10), all the visible

Figure 7.12: Measured frequency response of a typical cyclic DAC in comparison to analysis and simulation.

spurs at the multiples of the DMT bin frequency are now buried under the noise floor. Specifically, the *MTPR* for the missing bin is now higher than 83 dB.

The performance for a fine pitched picket-fence also improves after calibration. Despite the fact that in this implementation most of the overall noise and distortion in the missing DMT bin is contributed by the thermal noise floor, the measured $SNDR_{\text{DMT}}$ after calibration shows an improvement of over 2 dB by standing at 67.1 dB for the same measurement conditions as before calibration.

Figure 7.13: DC linearity of a typical cyclic DAC after digital calibration.

Figure 7.14: Multi-tone response of a typical cyclic DAC after digital calibration with magnified missing bin.

7.3 Pipelined DACs

The nominal test conditions for the pipelined DACs implemented in a 0.6- μm CMOS process are listed in Table 7.2.

Parameter	Value
Analog and Digital Supply Voltage	5 V
Positive Reference Voltage	3.6 V
Analog Ground Voltage	2.1 V
Negative Reference Voltage	0.6 V
Bias Currents	Same as Simulation
Clock Frequency	35.328 MHz
Magnitude Bits	16
Conversion Rate	17.664 MSps
Temperature	Room

Table 7.2: Nominal test conditions for the pipelined DACs.

A total of 18 functional chips have been tested to collect statistics on the performance.

7.3.1 DC Characteristics

DC output voltages have been measured for 16383 levels of all devices. From the collected data, various DC characteristics of the PDACs have been evaluated.

Distribution of the DC offset and DC gain for all 18 functional devices are shown in Fig. 7.15. Offset has an average of -0.15 mV and a standard deviation of 2.6 mV. The maximum offset is 0.2% of the range. The mean value of the DC gain is 0.998 V/V, with a standard deviation of 0.27%. The DC gain is within 0.6% of its nominal value.

The DC linearity characteristics for the a typical pipelined DAC is shown in Fig. 7.16. From these graphs, a maximum *DNL* of 1.4 LSB, and a maximum *INL* of 1.8 LSB is derived for this device.

Figure 7.15: Distribution of the measured DC offset and gain for the pipelined DACs.

The distribution of the *DNL* and *INL* for all 18 devices are shown in Fig. 7.17.

Figure 7.16: DC linearity of a typical pipelined DAC.

Figure 7.17: Distribution of DC linearity for the pipelined DACs at 14-bit resolution.

7.3.2 AC Characteristics

The analog domain reference level (0 dBr) for the pipelined DACs is defined as the power of a sine wave with a peak value of 3.0 V. The digital 0 dBr is the same as the cyclic DAC, i.e. a full scale sine wave.

Idle-Channel Noise

The output noise power of a typical pipelined DAC between 200 kHz and 600 kHz is measured to be at -88.68 dBr with idle input. For the same bandwidth, the measuring system has a noise power of -92.03 dBr. Hence, the DUT contribution is 91.23 dBr, or $58.2 \mu\text{V}_{\text{RMS}}$. The resultant noise density at the output of the pipelined DAC is $92 \text{ nV}/\sqrt{\text{Hz}}$, which is exactly the same as the analysis and simulation value (Table 6.6). Minor overestimations in the analysis must have been balanced by process and modeling inaccuracies.

Single-Tone

A typical single-tone response of the pipelined DAC with a 0 dBr input at 300 kHz is shown in Fig. 7.18. For a bandwidth of 1104 kHz, the *SNR* stands at 84.0 dB, the total-harmonic distortion is at -85.8 dBr, the *SNDR* is 82.1 dB, and *SFDR* = 85.8 dB.

Two-Tone

A typical two-tone response of the pipelined DAC with -6 dBr inputs at 1099.7 kHz and 1104 kHz is shown in Fig. 7.19. The maximum third order intermodulation distortion, *IM3*, is at -83.8 dBc on this plot. The *IM5* is 7 dB lower at -90.8 dBc. At these low levels of distortion, the contribution of the measuring system (expected to be around -90 dB) is not negligible.

Figure 7.18: Single-tone response of a typical pipelined DAC.

Multi-Tone

A typical pipelined DAC tested with a picket-fence input having a 4.3125 kHz pitch, frequency span from 138 kHz to 1104 kHz (a missing bin at 690 kHz), and power of -11.5 dBr, delivers an output spectrum shown in Fig. 7.20. The *MTPR* for this plot is 75.8 dBc.

DMT

The performance of a typical pipelined DAC for a fine-pitched picket-fence input, resembling a DMT signal, is shown in Fig. 7.21. Based on this measurement, the $SNDR_{DMT} = 72.6$ dB for this converter.

Frequency Response

A typical frequency response of the pipelined DAC is shown in Fig. 7.22. Measurement results are fairly close to the theoretical analysis.

Figure 7.19: Two-tone response of a typical pipelined DAC.

Power Dissipation

The overall current from the 5 V power supply is measured at 8.6 mA, which is equivalent to 43 mW, for the DAC alone, and 14.5 mW is dissipated by the CTRCF.

Figure 7.20: Multi-tone response of a typical pipelined DAC with magnified missing bin.

Figure 7.21: Response of a typical pipelined DAC to a fine picket-fence for measuring $SNDR_{DMT}$. The missing bin is magnified.

Figure 7.22: Measured frequency response of a typical pipelined DAC in comparison to analysis and simulation.

Digital Calibration

Using the calibration mode of the second S/H in the pipelined DAC, *DNL* values for a preskewed DAC have been measured. Due to lack of proper synchronization mechanism between the on-chip and off-chip calibration circuitry, one of the capacitors in the multiplexed last stage of the pipelined DAC was disabled for this measurement. Nonetheless, the improvement in the performance achieved through digital calibration can be extended to the multiplexed last stage as well.

From the on-chip sigma-delta modulator, 64k samples for measuring each critical DAC output level (30 total) were collected. The pipelined DAC was run at 8.832 MSps (half the normal rate) to have better settling accuracy in the modulator. The average value of the 64k samples collected for each level yields the digitized level, from which the *DNL* values are obtained by subtraction of the outputs for the adjacent codes. A total of 83 bits of memory was used to hold the correction values in this example.

The effect of digital calibration on DC linearity can be seen from the linearity plots of Fig. 7.23 and Fig. 7.24. These graphs display the linearity performance at 14-bit resolution (including sign). The maximum *DNL* is reduced from 2.24 LSB to 0.63 LSB, and the maximum *INL* is improved from 2.91 LSB to 0.73 LSB.

The effectiveness of digital calibration in an actual application can be seen in the picket fence response of Fig. 7.25 and Fig. 7.26. The *MTPR* is improved from 68 dB to 75 dB according to these measurements after calibration. For most part, the linearity is now limited by the S/Hs, especially because of reduced effective sampling rate (due to disabled multiplexed last stage).

In terms of $SNDR_{DMT}$, the same device indicates an increase from 68.4 dB to 73.3 dB due to digital calibration. Again, at these low-noise and high-linearity levels, the contribution of the measurement system (and its variations) cannot be neglected.

Figure 7.23: Effect of digital calibration on differential nonlinearity of a preskewed pipelined DAC.

Figure 7.24: Effect of digital calibration on integral nonlinearity of a preskewed pipelined DAC.

Figure 7.25: Multi-tone response of a preskewed pipelined DAC before digital calibration.

Figure 7.26: Multi-tone response of a preskewed pipelined DAC after digital calibration (same DAC as Fig. 7.25).

7.4 Conclusion

The cyclic and pipelined DACs proposed and designed in the previous chapters of this thesis have been thoroughly tested after fabrication.

The measurement results support the analysis and simulation predictions on both DAC types. The DC linearity characteristics show behaviours consistent with the expectations, and the limitations due to capacitor matching in the implementation technologies allow very useful range of linearities from 11 to 13 bits for these DACs.

The dynamic performance of the DACs for test cases similar to the actual applications are also acceptable.

Both DC and AC performance of cyclic and pipelined DACs can be significantly improved through the use of the simple self calibration technique proposed earlier in this thesis.

Chapter 8

Conclusions

Throughout this thesis, it has been demonstrated that algorithmic DACs are viable alternatives to other architectures used for high-speed high-resolution D/A conversion.

The improvements proposed and implemented in this work are proven to help the algorithmic DACs' performance achieve the requirements of many practical applications.

8.1 Contributions

The gain in the linearity of the QP cyclic and pipelined DACs due to the differential bipolar architecture is proven through the implementations. This architecture doubles the output range of the converters (relative to their LSB) with a negligible increase in nonlinearity.

The QP cyclic D/A converters proposed and implemented in this work, achieved much better performance than the best previously reported converters [9]. In terms of speed they have passed 4 MSps mark, as compared with 100 kSps, and in regards to linearity, close to 11-bit instead of 7-bit.

The noise performance of the implemented cyclic DACs, is limited by the thermal

noise of the S/H opamp. The design can be optimized without a significant increase in power dissipation. Simulation results indicate that more than 6 dB reduction in the overall thermal noise floor can be gained using an optimized differential opamp.

The linearity of a cyclic DAC is sensitive to the matching between the total capacitance on the sensitive nodes. It is very crucial to have the best possible symmetry in the layout in order to avoid any detrimental effect due to parasitic capacitance mismatch. The implemented cyclic DACs were not optimal in this sense. Most of the nonlinearity seems to be caused by a systematic mismatch in the drawn layout.

The stray-insensitive quasi-passive architecture proposed for the pipelined DAC is capable of reaching high conversion speeds with acceptable linearity. The stray insensitivity, which is very essential for high-speed converters, is achieved without the use of opamps in the pipelined stages.

The previous report on a QP pipelined DAC offers 8-bit linearity for a 333 kSps converter [21]. The new implementation delivers close to 13-bit linearity at 17.6 MSps. A key indicator for capacitor matching accuracy in the 0.6- μm CMOS process used is approximately 0.2% worst case (between two 1 pF capacitors) based on the pipelined DAC linearity measurements. Significantly lower mismatch numbers have been obtained for the 0.35- μm CMOS process used for the cyclic DAC, which proves that as high as 14-bit linearity may be practical for the pipelined DAC without any calibration.

If the linearity performance of the uncalibrated DAC is not satisfactory for an application, significant improvement can be gained through the digital calibration scheme proposed and applied in this thesis. Close to 13-bit and 14-bit linearity levels have been achieved by the cyclic and pipelined DACs respectively. The proposed symmetrical structure for the cyclic DAC makes digital calibration possible without a need for preskew, and results in smaller memory size.

The measured signal-to-noise performance of the implemented DACs are relatively

close to the predicted values from analysis, with some expected margin due to conservative overestimates. The measured frequency responses for both DACs match the analysis results fairly well.

The CT linearity of the output stage, for most part, does not limit the dynamic linearity of the converter, thanks to the deployment of the second S/H stage with very linear CT performance.

Using a first-order sigma-delta modulator for characterizing capacitor matching, capacitor ratios in a 0.35- μm CMOS have been measured. High repeatability and accuracy of this method allows evaluation of the standard deviation for matching between 2 pF capacitors down to 62 ppm. Capacitor matching performance for CMOS technologies, which is very critical for algorithmic converters, is not usually evaluated and/or reported properly. It is advantageous to have test-insert structures based on the proposed method implemented in various technologies to obtain prior knowledge of this important process factor.

8.2 Future Work

The following is a brief list of future enhancements possible for the algorithmic DACs.

Design of a cyclic DAC with an optimal noise performance and perfect symmetry in the layout can help the new cyclic DAC architecture achieve its best capability. Better than 12-bit linearity and SNR should be achievable in the same technology with a better design.

Two to 4 cyclic converters used in a BOC architecture and sharing the same S/H stages can provide a solution between the cyclic and the pipelined DACs in terms of speed and power.

The pipelined DAC should be implemented in finer technologies with higher speed opamps and better capacitor matching. A pipelined DAC implemented in the same

0.35- μm CMOS technology as the cyclic DAC will potentially achieve 14-bit linearity at 50 MSps with no need for digital calibration.

Analog circuitry (first-order $\Sigma\Delta\text{M}$ in the second S/H) for digital calibration should be implemented in a cyclic DAC. Also, with the addition of the corresponding digital circuit, a complete self calibration scheme may be implemented for both cyclic and pipelined DACs.

Same circuit as the capacitor matching experiment can be used to measure capacitor nonlinearity. Increase in the opamp gain (higher than 100 dB) and cancellation of flicker and reference noise should allow very precise measurement of capacitor nonlinearity as well as capacitor matching.

Appendix A

D/A Performance Metrics

Various measures have been used to characterize and compare the performance of different DACs. For the sake of completeness of this thesis, and to avoid any confusion caused by some variations of the metrics definitions among different authors, a set of definitions are presented in this appendix.

The metrics defined in this appendix are more suited for communication signal processing applications of DACs, hence, the list is incomplete for all applications.

The D/A converter performance parameters can be split between static (DC) and dynamic (AC) categories. Both categories are equally important for the characterization and optimization of a DAC design.

A.1 DC Performance

The DC performance of a DAC is a measure of how accurate it can produce individual output levels. Depending on the application, some of these parameters are more important than the others.

Fig. A.1 offers a pictorial definition for the DC metrics of a DAC. The basic characteristics, from which all the parameters are derived is the input-output transfer characteristics. Although in practice this plot is not very useful by itself because of its

Figure A.1: DC characteristics of a general purpose DAC.

too large scale, its derivatives such as *DNL* and *INL* plots are very informative. The figure is for a DAC with positive-only output values, however, similar specifications apply to a DAC with symmetrical output (positive/negative) as well.

It is customary to measure the linearity of the DAC against a line passing through the end points in the input-output characteristic plot (approximation line).¹ The y-intercept of this line is defined as the offset of the converter. If the output of the DAC

¹Another method defines linearity error against the best fit line (in terms of Mean Square Error — *MSE*), but that definition is not used here.

is symmetrical, the offset is at the midrange not at the lower end. The converter gain is the slope of the approximation line. By defining the reference level in digital and analog domains as their Full Scale (FS), nominal value of gain is 1. The (average) Least Significant Bit (LSB) of the converter is defined as the output range divided by $2^N - 1$ (where N is the total number of input bits to the converter, including the sign bit if any), i.e.

$$1 \text{ LSB} = \frac{FS}{2^N - 1}. \quad (\text{A.1})$$

This value is used as a unit for measuring linearity parameters.

Differential Nonlinearity (DNL) is an indication of the accuracy of the output step sizes. There are as many DNL values as the input digital codes (assuming $DNL = 0$ for the first code). For a given code, DNL can be positive or negative, as it is defined as the step size for that code (relative to the immediate previous one) minus 1 LSB,

$$DNL_i = V_i - V_{i-1} - 1\text{LSB}. \quad (\text{A.2})$$

A negative DNL value implies a step size smaller than the LSB. DNL is usually expressed in terms of LSB units, although expression in percentage (“%”) of the FS has also been used.

Integral Nonlinearity (INL) is the measure of deviation of the transfer characteristics from the approximation line. It can also be expressed in the form of a summation of DNL s,

$$INL_i = \sum_{j=0}^i DNL_j. \quad (\text{A.3})$$

Again, INL is also usually specified in LSB units. Both DNL and INL are typically reported in terms of their maxima and minima, for example ± 0.5 LSB.

A.2 Speed

Speed of a DAC is expressed in three different forms: settling time, latency, and conversion rate.

Figure A.2: Timing diagram for speed characteristics of a DAC.

In some DACs there is an inherent delay in the internal circuits before *any* sign of an input change appears at the output. This is the time that the DAC needs to process the digital input before sending it to the output drivers (Fig. A.2). This latency is usually an integral multiple of a clock period used inside the DAC. In some DAC architectures, the output immediately *starts* to move after an alteration in the input code, for those types (e.g. current steering) the latency is zero. However, there is always a finite amount of time that it takes for the output to *reach and stay within certain limits of its final value* after the *start* of the change at the *output*. This settling time is a sign of how closely the output waveform resembles a perfect staircase. A typical value for settling accuracy (δ_s) is 0.1%.

The settling accuracy is mentioned here only to differentiate it from latency, otherwise, for the DAC applications considered in this thesis it is not a critical parameter. In fact, it is usually beneficial to have a slow (and linear) settling at the output to have less energy in the images of the signal at $\pm n f_s$.

The conversion rate is the maximum number of samples per unit time that the

converter can process with *acceptable quality* at the output. This parameter, usually expressed in samples-per-second (Sps) units, has a relatively fuzzy definition. To make the definition sharp, the acceptable quality for the output has to be defined properly before the conversion rate is determined.

For oversampling (noise-shaping) converters, the clock (and therefore input sample rate) is relatively high (usually after some digital interpolation). However, if signals around $f_s/2$ are sent to these converters, they could very well be buried under the quantization noise with a negative *SNR*! For these types of D/A converters, it is more appropriate to assign the conversion rate as twice the signal bandwidth which results in an acceptable *SNR*.

For communication system applications, the input signal frequency (or bandwidth) that the DAC can handle is of greater importance than any of the above speed factors. It is crucial, however, to specify the minimum quality required of the output signal before specifying the maximum bandwidth. The output signal quality for these applications is specified in terms of the metrics of the next section.

A.3 AC Characteristics

Despite all the insight that can be inferred from the DC characteristics of a DAC into its limitations and their causes, the performance that really matters in signal processing applications is the quality of the output for an AC signal. It is sometimes difficult to measure the quality of the output signal with a true input signal for a given application, therefore, special test signals are usually used to verify the capabilities of a converter. These test signals also provide a way of comparing different DACs.

The most common method of measuring the linearity of AC response of a converter is a single-tone test. In a perfectly linear system, response to a single-tone is a pure sine wave of the same frequency. In practical systems, however, nonlinearity and

Figure A.3: AC performance of a DAC.

noise of the converter creates an output spectrum similar to Fig. A.3. In addition to the output tone at f_{in} , there are also its harmonics at nf_{in} (single-sided spectrum), non-harmonically related tones (*nonharmonic spurs*), and noise (white, flicker, or shaped) present at the output. Since the only desirable output is the tone at f_{in} all other spikes in the spectrum, including the harmonics, are called *spur*. The power of a harmonic is denoted by HDx , where x is the harmonic number, e.g. $HD2$, $HD3$ etc. (usually expressed as a ratio to the fundamental in dBc). The ratio of the total power of all harmonics (usually second to the seventh) to the signal power is called the Total Harmonic Distortion (THD).

For most applications, all in-band spurs are equally detrimental, so we define the Spurious-Free Dynamic Range ($SFDR$) as the ratio of the signal power to the power of the largest spur in the signal bandwidth (in dBc). $SFDR$ can also be expressed relative to the full scale sine wave, in which case the unit is dBFS. This latter expression is particularly useful if signals other than single-tone are applied.

The output power in the baseband minus power of the signal and spurs is the

noise power. Aside from the always present thermal noise (which is usually flat), at low frequencies the flicker noise, and at high frequencies shaped quantization noise (oversampling converters) also contribute to the total noise power. The total in-band noise power can be specified in μV_{RMS} units, or relative to the full scale (dBFS). A more common way of indicating the noise, however, is the Signal-to-Noise Ratio (*SNR*), which is the ratio of the powers in dB. Quite often, there are also limits for the out-of-band noise, usually specified for certain size of a sliding window. The ratio of the signal power to everything else in the baseband is denoted by Signal-to-Noise and Distortion Ratio (*SNDR*).²

Figure A.4: Intermodulation distortion definitions.

Single tone measurements for linearity have an important limitation, if the tone frequency is very high (which usually aggravates the AC nonlinearity), the harmonics may be attenuated significantly by the CTRCF, thereby creating the illusion of

²The notation *SINAD* (Signal-to-Noise And Distortion) is also used to represent *SNDR*, but *SNDR* is chosen here because of its consistency with *SNR*.

more linearity than reality. A better test at high frequencies is the intermodulation distortion. In a two tone test (Fig. A.4), the ratio of the (largest) third-order intermodulation spike to the signal spike is denoted by $IM3$ (negative, in dB). The third-order intermodulation products at $2f_{in1} - f_{in2}$ and $2f_{in2} - f_{in1}$ are results of the cubic term in the transfer characteristics of the converter. Similarly, the fifth-order intermodulation distortion ($IM5$) is defined for the fifth-order products.

Figure A.5: Picket fence test and multitone power ratio.

A test signal that is closer to the signals in the actual application than two tones is a multitone (picket fence). Fig. A.5 illustrates an output example for a multitone test. The tone or subcarriers cover the signal bandwidth with the spacing defined by the application, with a missing tone (or tones). The random phase relationship between the subcarriers determines the Peak-to-Average Ratio (PAR , or peak-to-RMS ratio because the average is defined as the RMS value), which is usually between 4 to 6. Multitone Power Ratio ($MTPR$) is defined as the power ratio between a tone and the intermodulation distortion product that fills the empty bin.

For many applications such as DSL, it is desired to know the total amount of noise and distortion per subcarrier in the modulated signal. In these applications the signal is low-pass or bandpass with (almost) flat spectrum in the signal bandwidth. For example, in a Discrete Multitone (DMT) signal, subcarriers spaced at 4.3125 kHz occupy the spectrum from 138 kHz to 1.104 MHz, and the capacity of each subcarrier depends on the ratio of the signal power to the noise and distortion in that subband. Therefore, $SNDR_{DMT}$ may be defined as the signal-to-noise and distortion ratio in each subband. Although it is possible to gain some estimate for this quantity from separate noise, and $MTPR$ measurements, a combined test is more suitable.

Figure A.6: Test system for measuring $SNDR_{DMT}$.

The test system for measuring $SNDR_{DMT}$ is illustrated in Fig. A.6, in which a digital pattern generator and an FFT analyzer are synchronized by a single clock source. The test signal, which will be repeated by the pattern generator at $\frac{f_s}{S}$ rate, is a pseudorandom bandpass (or low-pass) signal with a missing subband and very sharp boundaries. It is virtually impossible to create such a signal with a true modulator, because the signal would not be repetitive, and would have large leakage in its spectral sidebands. The method proposed here uses a minimum FFT bin size (dictated by the common maximum signal length S of the pattern generator and the FFT analyzer) to produce the pseudorandom signal with the desired spectrum. A short sample program

in Matlab that follows demonstrates the principle.

```

samples = 65536; % total number of samples
fs = 4.416e6; % sampling frequency
fftbins = fs/samples; % FFT bin size
scbins = 4312.5 / fftbins; % subcarrier bin size (in FFT bins)

% definition of single-sided magnitude spectrum
mag_ss = [zeros(0.5*scbins, 1); ... % unused half subcarrier
          zeros(31*scbins, 1); ... % first 31 subcarriers nulled
          ones(48*scbins, 1); ... % next 48 subcarriers full power
          zeros(scbins, 1); ... % one empty subcarrier bin
          ones(48*scbins, 1); ... % next 48 subcarriers full power
          zeros(samples/2 - 128.5*scbins - 1, 1)]; % rest is empty

% conjugate symmetry for magnitude
mag = [0; mag_ss; 0; mag_ss(end:-1:1)];

% random phase for single-sided spectrum
phase_ss = randn(samples/2 - 1, 1);
% conjugate symmetry for phase
phase = 1000 * [0; phase_ss; 0; -phase_ss(end:-1:1)];
xf = mag .* (exp(j * phase)); % signal in frequency domain
xt = ifft(xf); % signal in time domain
xr = real(xt); % real part only
xrn = xr / std(xr) / 5.3; % normalized for peak-14.5 dB power

```

An example of a signal generated by the above code is shown in Fig. A.7. The noise leakage in the missing DMT bin and outside the baseband, which is only generated by numerical noise, is very negligible. With an ideal D/A converter under test (and an ideal FFT analyzer) the output sampled signal should be exactly the same (with some delay only). The nonlinearity of the DAC and its noise, however, will increase *the combined noise floor*. The ratio of the signal in a full DMT bin to the combined noise in the empty DMT bin next to it is defined as $SNDR_{DMT}$.

Figure A.7: Time domain and frequency domain views of a test signal for measuring $SNDR_{DMT}$.

Appendix B

Sample-and-Hold Frequency Response

The sample-and-hold architectures explored in Chapter 4 have certain Discrete-Time (DT) and Continuous-Time (CT — important only in a DT-to-CT converter) frequency responses. Detailed derivation and understanding of these responses are essential to the application of these architectures in any system.

In today's complex digital signal processing designs, not only it is relatively easy to compensate for certain non-ideal frequency response of the S/H, but also it is usually desirable to take advantage of these effects.

In this appendix, the DT and CT frequency response of various S/H architectures are derived with no comparison. The assessment of these transfer functions as applied to the DAC system design is included in Chapter 4.

The discrete-time frequency response is dependent on the specific architecture of the S/H and will be treated in separate sections. The response of the DT-to-CT conversion (which applies only to the second and the third architectures) is common for all architectures and is offered in the last section.

B.1 First Architecture

Since in this architecture (Fig. B.1) the reset switch removes any history of the past samples, the current output depends only on the last input sample. Therefore, the transfer function is simply a delay

$$H(z) = \frac{V_{\text{out}}(z)}{V_{\text{in}}(z)} = z^{-1}, \quad (\text{B.1})$$

and has a flat magnitude response.

Figure B.1: Single-ended view of the traditional (first) architecture for a S/H. (a) Schematic. (b) Timing diagram.

Due to the presence of a reset phase in this scheme, it cannot be used in the second S/H stage, hence derivation of its CT response is pointless.

B.2 Second Architecture

Unlike the previous architecture, this architecture can be used in both the first and the second S/H stages. For both stages, the DT behaviour is important and, in the second stage, the CT response should also be considered. In this section the DT transfer functions are derived and the CT effects are referred to Section B.4.

The transfer of charge from the sampling and feedback capacitors to the holding capacitor is never precisely complete. The differential equation governing the transfer of charge through the on-resistance of the switches (also affected by the finite bandwidth of the opamp) guarantees that some residual difference, as small as it may be, remains between C_S and C_{FB} voltages. If the R_{on} of the switches is low enough, and the bandwidth of the opamp is high enough, the residual untransferred charge at the end of the transfer phase is negligible (much more so for the frequency response calculations, rather than linearity concerns). However, in the second S/H stage, due to CT linearity requirements, large resistors are placed in series with some of the switches, and the untransferred amount of charge may be as high as %10.

In this section, first the case of a complete charge transfer is treated, and later a more elaborate transfer function including finite settling accuracy is examined.

To derive the frequency response of the filter, shown again in Fig. B.2, let's begin with the time-domain equations for this architecture. The charge on the holding capacitor C_H at the end of the transfer phase on cycle n is

$$C_H V_{out}[n] = C_H V_{out}[n-1] - C_{FB} V_{out}[n-1] + C_S V_{in}[n-1]. \quad (B.2)$$

In z -domain

$$V_{out}(z) = \frac{C_H - C_{FB}}{C_H} z^{-1} V_{out}(z) + \frac{C_S}{C_H} z^{-1} V_{in}(z). \quad (B.3)$$

Assuming

$$a = \frac{C_S}{C_H}, \quad (B.4)$$

Figure B.2: Second architecture for a S/H. (a) Schematic. (b) Timing diagram.

and

$$b = \frac{C_{FB}}{C_H}, \quad (\text{B.5})$$

the transfer function can be written as

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{az^{-1}}{1 - (1 - b)z^{-1}}, \quad (\text{B.6})$$

which is a first-order IIR filter.

It is evident that if $b = 1$ (i.e. if $C_{FB} = C_H$) the response is a simple delay, and all-pass function is easily obtained. For $b < 1$ the response is low-pass, and conversely, $b > 1$ results in a high-pass frequency response. To maintain a DC gain of 1, one has to keep $a = b$, i.e. $C_{FB} = C_S$.

The effect of incomplete charge transfer can be better evaluated using the simplified diagram of Fig. B.3. For the second S/H stage, resistors R_S and R_{FB} are mainly

Figure B.3: Simplified view of the transfer phase for the second S/H architecture. The total resistance in series with C_S and C_{FB} (including any linear resistor added for CT linearity) are represented as R_S and R_{FB} respectively.

representatives of the series linear resistors added for CT linearity improvements (see Section 4.4.5), nonetheless, they also include R_{on} of the closed switches in series with the capacitors.

With the addition of the large linearizing resistors, large transients at the input of the opamp are eliminated and it is always a good approximation to assume the voltage at the input of the opamp to be at the ground level. With this assumption, and taking the beginning of the transfer phase as the time reference, the voltage on the C_S and C_{FB} are simple exponential functions

$$v_{C_S}(t) = V_{in}[n - 1] \exp\left(-\frac{t}{\tau_S}\right), \quad (\text{B.7})$$

and

$$v_{C_{FB}}(t) = V_{out}[n - 1] \exp\left(-\frac{t}{\tau_{FB}}\right), \quad (\text{B.8})$$

where $\tau_S = R_S C_S$ and $\tau_{FB} = R_{FB} C_{FB}$ are the time constants of the sampling and feedback capacitor-resistors combinations respectively.

At the end of the transfer phase, fractions $\exp\left(-\frac{\alpha T}{\tau_S}\right)$ and $\exp\left(-\frac{\alpha T}{\tau_{FB}}\right)$ of these voltages remain on the respective capacitors. Therefore, the original charge balance

equation should be rewritten as

$$C_H V_{\text{out}}[n] = C_H V_{\text{out}}[n-1] - C_{\text{FB}} \left(1 - e^{-\frac{\alpha T}{\tau_{\text{FB}}}}\right) V_{\text{out}}[n-1] + C_S \left(1 - e^{-\frac{\alpha T}{\tau_S}}\right) V_{\text{in}}[n-1]. \quad (\text{B.9})$$

This leads to

$$H'(z) = \frac{a' z^{-1}}{1 - (1 - b') z^{-1}}, \quad (\text{B.10})$$

for the output voltage, after defining

$$a' = \frac{(1 - e^{-\frac{\alpha T}{\tau_S}}) C_S}{C_H}, \quad (\text{B.11})$$

and

$$b' = \frac{(1 - e^{-\frac{\alpha T}{\tau_{\text{FB}}}}) C_{\text{FB}}}{C_H}. \quad (\text{B.12})$$

The result of incomplete charge transfer, as shown above, is a modification in the filter coefficients with the general shape of the transfer function intact. To avoid excessive DC gain error due to process and temperature variations, the two time constants, τ_S and τ_{FB} should be closely matched.

In the above derivation, it was assumed that the sampling and feedback capacitors were fully charged in the hold period. While this is usually a good assumption for C_S , it may not be the case for C_{FB} . To avoid large transients at the output of the opamp and its associated distortion and gain error¹ when the feedback capacitor switches to the output at the beginning of the hold mode, large resistors may be placed in series with the capacitor in that phase too. To a first order approximation, the b' coefficient of the transfer function has to be modified to

$$b'' = \frac{(1 - e^{-\frac{\alpha T}{\tau_{\text{FB}}}})(1 - e^{-\frac{\alpha T}{\tau_{\text{FBO}}}}) C_{\text{FB}}}{C_H}, \quad (\text{B.13})$$

¹Due to limited bandwidth of opamp, in response to the sudden change of load at the beginning of hold phase (i.e. connection of C_{FB} to the output) the output voltage temporarily drops towards ground. This reduces the average voltage from its desired value, which decreases the DC (low frequency) gain of the stage.

where $\tau_{FBO} = R_{FBO}C_{FB}$ is a new time-constant, and R_{FBO} is the total resistance in series with C_{FB} in the hold phase. This approximation ignores the residual charge leftover from the previous transfer phase on C_{FB} . Deriving more exact equations is cumbersome and usually does not serve any practical purpose.

B.3 Third Architecture

Similar to the second architecture, this scheme is useful for both the first and the second S/H stages. Here the DT response is considered, and the DT-to-CT transfer function can be found in Section B.4.

Figure B.4: Third architecture for a S/H including a potential linearizing resistor. (a) Schematic. (b) Timing diagram.

For this scheme, a general response including the effect of finite settling is evaluated first, then the complete settling response is shown as a special case.

Resistor R_S is the combined series resistance for the input sampling capacitor C_S in the transfer phase, including switches. As long as the opamp bandwidth is not limiting, the settling of the capacitor voltages in this phase is determined by the capacitor values and the series resistance; the opamp merely keeps its input at the ground potential and prevents its input capacitance from taking any of the charge that is being passed around. While this is a good assumption for the second S/H with large linearizing resistors, it is not very accurate for the first S/H stage. Nevertheless, the special case of complete settling, derived later from this analysis, still applies to the first S/H.

The final voltage across C_H for complete settling during the transfer phase is

$$V_{\text{final}} = \frac{1}{C_H + C_S} (C_S V_{\text{in}}[n-1] + C_H V_{\text{out}}[n-1]). \quad (\text{B.14})$$

Using the beginning of the transfer phase as the time reference, the output voltage (same as the voltage across C_H) can be written as

$$\begin{aligned} v_{\text{out}}(t) &= V_{\text{out}}[n-1]e^{-t/\tau} + \frac{1}{C_H + C_S} (C_S V_{\text{in}}[n-1] + C_H V_{\text{out}}[n-1]) (1 - e^{-t/\tau}) \\ &= \left(\frac{C_H}{C_H + C_S} + \frac{C_S}{C_H + C_S} e^{-t/\tau} \right) V_{\text{out}}[n-1] + \\ &\quad \frac{C_S}{C_H + C_S} (1 - e^{-t/\tau}) V_{\text{in}}[n-1]. \end{aligned} \quad (\text{B.15})$$

The time-constant in the above equation is defined as

$$\tau = R_S \frac{C_H C_S}{C_H + C_S}. \quad (\text{B.16})$$

Again, assuming

$$a = \frac{C_S}{C_H}, \quad (\text{B.17})$$

we have

$$\frac{C_S}{C_S + C_H} = \frac{a}{1 + a}, \quad (\text{B.18})$$

and

$$\frac{C_H}{C_S + C_H} = \frac{1}{1 + a}, \quad (\text{B.19})$$

and at the end of the transfer phase ($t = \alpha T$) the output voltage can be written as

$$V_{\text{out}}[n] = \left(\frac{1}{1 + a} + \frac{a}{1 + a} e^{-\alpha T/\tau} \right) V_{\text{out}}[n - 1] + \frac{a}{1 + a} (1 - e^{-\alpha T/\tau}) V_{\text{in}}[n - 1]. \quad (\text{B.20})$$

In z -domain

$$V_{\text{out}}(z) = \left(\frac{1}{1 + a} + \frac{a}{1 + a} e^{-\alpha T/\tau} \right) z^{-1} V_{\text{out}}(z) + \frac{a}{1 + a} (1 - e^{-\alpha T/\tau}) z^{-1} V_{\text{in}}(z), \quad (\text{B.21})$$

which yields the transfer function as

$$H'(z) = \frac{V_{\text{out}}(z)}{V_{\text{in}}(z)} = \frac{a (1 - e^{-\alpha T/\tau}) z^{-1}}{1 + a - (1 + a e^{-\alpha T/\tau}) z^{-1}}. \quad (\text{B.22})$$

This is a first-order IIR low-pass filter with a DC gain of 1.

The filter coefficients of Eq. B.22 are dependent on the settling accuracy (through finite $e^{-\alpha T/\tau}$ terms), which may change over process and temperature. Thus, care must be taken to ensure sufficient accuracy for a given application is obtained.

For the special case of near complete settling (as in the first S/H stage of a QP algorithmic DAC) the transfer function can be simplified to

$$H(z) = \frac{az^{-1}}{1 + a - z^{-1}}. \quad (\text{B.23})$$

B.4 Discrete-Time to Continuous-Time Response

Continuous-time frequency response of the second S/H stage is a transfer function between the discrete-time and the CT signals at the output of the circuit. In other words, the CT transfer function has to be applied to the ideal CT representation of the DT signal at the output of this stage (i.e. the staircase formed by holding the output voltage samples at the end of the transfer phase for the entire cycle), before passing it to the next stage.

Figure B.5: An example of a waveform at the output of a S/H circuit.

Study of the CT frequency response is important because for most applications near exact knowledge of the overall frequency response is required by the system specifications. The simplest example of a DT-to-CT converter is a zero-order hold [60, Chap. 3]. However, due to large linearizing resistors added to the second S/H stage, the real response is not usually close to that of the zero-order hold.

An example waveform at the output of the S/H is shown in Fig. B.5. This example is common to all S/H architectures with two distinct phases. During the transfer phase, charge is being transferred to the holding capacitor, hence, the output voltage is changing. Although, in general, this transient waveform can have many shapes, the output voltage can never completely settle before the end of the transfer phase. In the figure, the dashed lines indicate possible traces of the output waveform transient if it were not stopped by the end of the transfer phase.

The transient behaviour of the S/H circuit during its transfer phase must be kept very linear (i.e. proportional to the input step) in order to have a linear continuous-time output. One way to achieve this is the addition of large linear resistors in series with the input capacitor C_S (C_S and C_{FB} for the second S/H architecture). As explained in the previous section, these resistors will make the output voltage of the opamp very close to a first-order exponential function.

The continuous-time output of the S/H can now be expressed as a convolution of an impulse train representing the discrete-time signal, $V_{out}[n]$, and a unit pulse

representing the DT-to-CT conversion, $h_{\text{D2C}}(t)$, i.e.

$$v_{\text{out}}(t) = \sum_{n=-\infty}^{+\infty} V_{\text{out}}[n] h_{\text{D2C}}(t - nT). \quad (\text{B.24})$$

The unit pulse waveform, as shown in in Fig. B.6, is also the impulse response of DT-to-CT converter. Symbol α stands for the duty cycle of the S/H clock, e.g. for a 50% duty cycle, $\alpha = 0.5$.

Figure B.6: Impulse response of the DT-to-CT transfer function of the S/H (unit pulse).

According to the convolution theorem, the frequency-domain transfer function of the DT-to-CT converter is the Fourier transform of its impulse response, i.e.

$$H_{\text{D2C}}(\Omega) = \mathcal{F}\{h_{\text{D2C}}(t)\} = \int_{-\infty}^{\infty} h_{\text{D2C}}(t) e^{-j\Omega t} dt. \quad (\text{B.25})$$

The impulse response of Fig. B.6 can be expressed as

$$h_{\text{D2C}}(t) = \begin{cases} 0 & t < 0 \\ h_{\text{D2C1}}(t) = \frac{1}{1-e^{-\alpha T/\tau}} (1 - e^{-t/\tau}) & 0 < t < \alpha T, \\ h_{\text{D2C2}}(t) = 1 & \alpha T < t < T, \\ h_{\text{D2C3}}(t) = \frac{1}{1-e^{-\alpha T/\tau}} (e^{-(t-T)/\tau} - e^{-\alpha T/\tau}) & T < t < (1+\alpha)T, \\ 0 & (1+\alpha)T < t, \end{cases} \quad (\text{B.26})$$

where τ is the settling time-constant. For the third architecture, τ is defined in Eq. B.16, and for the second one $\tau = \tau_{\text{FB}} = \tau_{\text{S}}$ is assumed, which is also required

for DC gain accuracy.² To facilitate the derivation of the Fourier transform, the above impulse response is broken into the sum of three nonzero functions $h_{D2C1}(t)$, $h_{D2C2}(t)$, and $h_{D2C3}(t)$ defined in their respective intervals. The first part of the transfer function is

$$\begin{aligned}
 H_{D2C1}(\Omega) &= \mathcal{F}\{h_{D2C1}(t)\} \\
 &= \int_0^{\alpha T} \frac{1}{1 - e^{-\alpha T/\tau}} (1 - e^{-t/\tau}) e^{-j\Omega t} dt, \\
 &= \frac{1}{1 - e^{-\alpha T/\tau}} \int_0^{\alpha T} (e^{-j\Omega t} - e^{-(1+j\Omega\tau)t/\tau}) dt, \\
 &= \frac{1}{1 - e^{-\alpha T/\tau}} \left[\frac{-1}{j\Omega} e^{-j\Omega t} + \frac{\tau}{1 + j\Omega\tau} e^{-(1+j\Omega\tau)t/\tau} \right]_0^{\alpha T} \\
 &= \frac{1}{1 - e^{-\alpha T/\tau}} \left[\frac{1}{j\Omega} (1 - e^{-j\Omega\alpha T}) - \frac{\tau}{1 + j\Omega\tau} (1 - e^{-\alpha T/\tau} e^{-j\Omega\alpha T}) \right].
 \end{aligned} \tag{B.27}$$

The second Fourier transform can be derived as follows

$$\begin{aligned}
 H_{D2C2}(\Omega) &= \mathcal{F}\{h_{D2C2}(t)\} \\
 &= \int_{\alpha T}^T e^{-j\Omega t} dt, \\
 &= \left[\frac{-1}{j\Omega} e^{-j\Omega t} \right]_{\alpha T}^T \\
 &= \frac{1}{j\Omega} (e^{-j\Omega\alpha T} - e^{-j\Omega T}).
 \end{aligned} \tag{B.28}$$

Finally, the last part of the DT-to-CT transfer function is

$$\begin{aligned}
 H_{D2C3}(\Omega) &= \mathcal{F}\{h_{D2C3}(t)\} \\
 &= \int_T^{(1+\alpha)T} \frac{1}{1 - e^{-\alpha T/\tau}} (e^{-(t-T)/\tau} - e^{-\alpha T/\tau}) e^{-j\Omega t} dt, \\
 &= \frac{1}{1 - e^{-\alpha T/\tau}} \int_T^{(1+\alpha)T} (e^{T/\tau} e^{-(1+j\Omega\tau)t/\tau} - e^{-\alpha T/\tau} e^{-j\Omega t}) dt,
 \end{aligned}$$

²The general case of $\tau_{FB} \neq \tau_S$ can be solved in a similar way, but does not seem to serve any practical purpose.

$$\begin{aligned}
&= \frac{1}{1 - e^{-\alpha T/\tau}} \left[\frac{-\tau}{1 + j\Omega\tau} e^{T/\tau} e^{-(1+j\Omega\tau)t/\tau} + \frac{1}{j\Omega} e^{-\alpha T/\tau} e^{-j\Omega t} \right]_T^{(1+\alpha)T} \\
&= \frac{1}{1 - e^{-\alpha T/\tau}} \left[\frac{-\tau}{1 + j\Omega\tau} e^{T/\tau} \left(e^{-(1+\alpha)T/\tau} e^{-j\Omega(1+\alpha)T} - e^{-T/\tau} e^{-j\Omega T} \right) + \right. \\
&\quad \left. \frac{1}{j\Omega} e^{-\alpha T/\tau} \left(e^{-j\Omega(1+\alpha)T} - e^{-j\Omega T} \right) \right] \\
&= \frac{e^{-j\Omega T}}{1 - e^{-\alpha T/\tau}} \left[\frac{\tau}{1 + j\Omega\tau} \left(1 - e^{-\alpha T/\tau} e^{-j\Omega\alpha T} \right) - \frac{1}{j\Omega} e^{-\alpha T/\tau} \left(1 - e^{-j\Omega\alpha T} \right) \right].
\end{aligned} \tag{B.29}$$

The combined transfer function is equal to the sum of the three separate parts.

$$\begin{aligned}
H_{D2C}(\Omega) &= \mathcal{F}\{h_{D2C}(t)\} \\
&= H_{D2C1}(\Omega) + H_{D2C2}(\Omega) + H_{D2C3}(\Omega) \\
&= \frac{1 - e^{-\alpha T/\tau} e^{-j\Omega\alpha T}}{1 - e^{-\alpha T/\tau}} \left[\frac{-\tau}{1 + j\Omega\tau} \left(1 - e^{-j\Omega T} \right) + \frac{1}{j\Omega} \left(1 - e^{-j\Omega\alpha T} \right) \right] + \\
&\quad \frac{1}{j\Omega} \left(e^{-j\Omega\alpha T} - e^{-j\Omega T} \right).
\end{aligned} \tag{B.30}$$

As a special case of $\tau \approx 0$, the above response reduces to

$$H_{ZOH}(\Omega) = \frac{1}{j\Omega} \left(1 - e^{-j\Omega T} \right), \tag{B.31}$$

which is the classic zero-order hold response, usually expressed as $\frac{\sin(\Omega T/2)}{\Omega/2} e^{-j\Omega T/2}$ [60, p. 484]. This may be an acceptable approximation for $\tau < \frac{T}{20}$.

B.4.1 Single-Phase Sample-and-Hold

When the S/H is used with a D/A converter with multiple output capacitors having interleaved functions (e.g. Fig. 3.2 and Fig. 5.5), the second S/H circuit may always be in one mode, i.e. transfer phase. In this case there is no hold phase, and the output is always in exponential settling. If the gap between the S/H clock phases is relatively small enough (say less than 5%), the duty cycle α is close to 1, and there is no significant constant portion in the unit pulse shape of Fig. B.6.

The so called single-phase S/H continuous-time output is a special case of the more general two-phase waveform that has been discussed so far, therefore, the transfer function for this case may be obtained from Eq. B.30 by setting $\alpha = 1$.

$$\begin{aligned}
 H_{\text{D2C1P}}(\Omega) &= \frac{1 - e^{-T/\tau} e^{-j\Omega T}}{1 - e^{-T/\tau}} \left[\frac{-\tau}{1 + j\Omega\tau} (1 - e^{-j\Omega T}) + \frac{1}{j\Omega} (1 - e^{-j\Omega T}) \right] + \\
 &\quad \frac{1}{j\Omega} (e^{-j\Omega T} - e^{-j\Omega T}) \\
 &= \underbrace{\frac{1 - e^{-T/\tau} e^{-j\Omega T}}{1 - e^{-T/\tau}}}_{\text{First Term}} \underbrace{\frac{1 - e^{-j\Omega T}}{j\Omega}}_{\text{Second Term}} \underbrace{\frac{1}{1 + j\Omega\tau}}_{\text{Third Term}}. \tag{B.32}
 \end{aligned}$$

The last term in the above transfer function is that of a first-order low-pass filter with its pole at $\Omega_p = j/\tau$. The middle fraction is a zero-order hold function which is always present in conversion from DT-to-CT.

The first term in the results of Eq. B.32 is a periodic response which is a consequence of separation between the DT and CT functions of the second S/H stage. The assumption of unit height for the impulse response of DT-to-CT converter (Fig. B.6) is based on the inclusion of the effect of finite bandwidth (or finite τ) of the CT response of the S/H on the final value of the output during the transfer phase in the DT frequency response of the S/H. In other words, it is up to the DT response of the S/H to determine what the final value of the output in the transfer phase is, and then the CT response determines how it gets there.

Appendix C

Sample-and-Hold Noise

In quasi-passive algorithmic DACs the sample-and-hold circuits have the largest contribution to the output noise. Proper understanding of this noise power, and its spectrum has an important role in the design and optimization of these types of DACs. A S/H may also be placed at the output of other types of DACs (e.g. $\Sigma\Delta$ M with switched-capacitor RCF, or current steering) to enhance their continuous-time linearity (basically as a discrete-time to continuous-time converter). Therefore, the noise analysis of this appendix is also useful for those applications.

C.1 Introduction

There are two types of noise in the S/H circuits: discrete-time and continuous-time. The DT noise is the value of noise sampled on the output at the end of the charge transfer phase. These values are the only important noise values when the output of the S/H is *sampled* at the end of the transfer phase, which is the case only for the first S/H stage in a QP algorithmic DAC.

The output of the second S/H stage in the QP algorithmic DAC (i.e. the DT-to-CT converter) is used by the following stage continuously (not sampled), therefore, the CT noise voltage (i.e. the noise voltage at all times) at this output is of great

significance, not just the output samples at the end of a certain phase.

It should always be kept in mind that as a result of sampling process all the noise power up to the bandwidth of the circuit aliases back to the baseband (0 to $f_s/2$). In fact, for this very reason, the S/H circuits are the main sources of noise in QP algorithmic DACs.

There have been several publications regarding the noise analysis for switched-capacitor circuits in general. More recent articles aim at automating of the noise analysis [68, 69] which can be included in a general purpose, or a SC simulator. Some older works are more suitable for hand analysis and contain similar examples such as SC integrators [70, 71]. The method of these references is applied to the three S/H architectures considered in this work, with the additional components such as the capacitance at the input of the opamp, which are important in this application. This helps appreciating the relative contribution of each source, and gain some insight into the optimization of the design.

The noise contributors in the S/H are mainly two: the opamp and the switch (plus any series resistance) thermal noise. The opamp noise is separable into two frequency ranges: Within (the feedback) Loop Bandwidth (WILBW) and Without (outside) Loop Bandwidth (WOLBW). For the WILBW noise, the switched-capacitor circuit is analyzed with an ideal opamp model and an input referred noise source. Outside the loop bandwidth of the circuit, the feedback is not effective and the output referred noise is calculated.

A study of the noise performance of the three sample-and-hold architectures introduced in Chapter 4 follows. Except for the first S/H architecture which cannot be used in the second S/H stage (as a DT-to-CT converter), noise in the other architectures is analyzed for both DT and CT performance. Throughout this appendix, the transfer phase for any architecture is denoted by ϕ_1 , and the hold phase is assigned ϕ_2 .

C.2 First S/H Architecture

This traditional design, can be used only for the first S/H stage of a QP algorithmic DAC, since due to lack of a continuous-time output (presence of a reset phase) it cannot be applied to the second S/H stage. Hence, only the discrete-time noise performance of this design is considered.

Transfer Function for Opamp Noise

The schematic diagram of the circuit including a noise source representing the input referred noise of the opamp (V_{na}) is redrawn in Fig. 4.17. The familiar clock phase terminology is used for simplification, hence ϕ_1 is equivalent to the reset phase, and ϕ_2 stands for the transfer phase. In the third phase, i.e. the hold phase, all switches shown are open. Albeit, depending on the implementation (as will be discussed shortly) this third phase may not exist. For the first part of the analysis a two phase clock is assumed, and the time reference is the end of ϕ_2 .

Figure C.1: Simplified schematic diagram for the noise analysis on the first S/H architecture.

The input capacitor C_I is the parallel combination of the input capacitance of the opamp and the parasitics on that node (such as junction capacitance). Since the purpose of this analysis is to find the noise contributions from the S/H components

to V_{out} , the initial charge on the sampling capacitor C_S is assumed zero (the known Θ/C noise of the DAC core is counted separately).

Let's analyze the transfer function for the noise voltage source V_{na} by writing the equation for the charge stored on node N1 during the two phases. The opamp is assumed effective within the frequency range of this analysis, i.e. the derivation applies to the noise within the loop bandwidth of the circuit. The noise outside the opamp bandwidth will be analyzed later.

At the end of ϕ_1 ¹

$$Q_{\text{N1}}[n - \frac{1}{2}] = C_I V_{\text{na}}[n - \frac{1}{2}], \quad (\text{C.1})$$

and at the end of ϕ_2

$$Q_{\text{N1}}[n] = (C_S + C_I) V_{\text{na}}[n] - C_H (V_{\text{out}}[n] - V_{\text{na}}[n]). \quad (\text{C.2})$$

Since C_S was initially discharged, the principle of conservation of charge dictates that $Q_{\text{N1}}[n] = Q_{\text{N1}}[n - \frac{1}{2}]$. Therefore,

$$V_{\text{out}}[n] = \left(1 + \frac{C_S + C_I}{C_H}\right) V_{\text{na}}[n] - \frac{C_I}{C_H} V_{\text{na}}[n - \frac{1}{2}]. \quad (\text{C.3})$$

In z -domain,

$$\frac{V_{\text{out}}(z)}{V_{\text{na}}(z)} = \left(1 + \frac{C_S + C_I}{C_H}\right) - \frac{C_I}{C_H} z^{-\frac{1}{2}}. \quad (\text{C.4})$$

The noise transfer function of Eq. C.4 is a first-order high-pass FIR filter effectively running at twice the sampling rate f_S , but undersampled at f_S .

If the duty cycle of the S/H clock is not 50%, the transfer function has to be modified slightly. For a transfer-phase duty-cycle of α Eq. C.4 should be rewritten as

$$\frac{V_{\text{out}}(z)}{V_{\text{na}}(z)} = \left(1 + \frac{C_S + C_I}{C_H}\right) - \frac{C_I}{C_H} z^{-\alpha}, \quad (\text{C.5})$$

which may move the peak magnitude from f_S .

¹The use of a half sample delay in the following equations assumes a two phase S/H clock with 50% duty cycle. In the general case, the delay should be equal to the duty cycle for the transfer phase. This issue will be revisited shortly.

Noise outside loop bandwidth Opamps usually have some noise power at their output outside their loop bandwidth. If this noise power is significant, the above analysis for WILBW noise is not sufficient to yield a good estimate of the sampled noise at the output of the first S/H stage. In this case, in addition to the noise power shaped by the transfer function of Eq. C.5 and folded back to the baseband, the WOLBW noise power should also be taken into account.

A simple method for considering WOLBW noise is to find the total output referred noise from the -3-dB loop bandwidth to ∞ and distribute it, as usual, between 0 to $f_S/2$. Since the undersampling ratio is very large, a flat distribution of this noise in 0 to $f_S/2$ is a fairly good approximation. In these calculations the band-limiting effect of the on-resistance of the switches in series with the sampling capacitor of the second S/H stage should not be ignored. In fact, it is advantageous to add some series polysilicon resistance (because of better control on its value) to these switches to limit the amount of sampled noise. The WOLBW noise sampled on C_S (and therefore on C_H) is ignored because in the two phase design it occurs after the second stage has already taken its sample, and it will be discharged in the next reset phase before the following sampling at the output.

Switch Thermal Noise

The thermal noise of the reset switch is sampled on the holding capacitor at the end of ϕ_1 . This noise voltage ($\sqrt{\Theta/C_H}$) is then added to the output in the next phase.²

The thermal noise of the on-resistance of the sampling switch S_S , amplified with a gain of C_S/C_H (typically 1) appears at the output as a continuous-time noise. When this noise is sampled by the second S/H, its out-of-band content folds back into the

²In a two-stage opamp, at frequencies higher than the bandwidth of the opamp, the output has a relatively low impedance, and the input is effectively floating (i.e. no virtual ground effect due to lack of gain in the first stage). Then, the effective capacitance seen by R_{on} of the reset switch is somewhat increased by the input capacitance C_I , which reduces the Θ/C noise. Since the effect is minor and very implementation dependent, it is ignored in this analysis.

0 to $f_s/2$ range. Since this noise is band limited by the opamp (more precisely, by the loop-bandwidth for the feedback loop around the opamp), unlike the usual SC noise case, it is advantageous to reduce the on-resistance of the switch to minimize its noise density. The noise power sampled by the next S/H is given by

$$\overline{v_{R_{on}}^2} = 2\pi \left(\frac{C_S}{C_H} \right)^2 \Theta R_{on} B_{lp}, \quad (C.6)$$

where B_{lp} is the loop bandwidth, and $\frac{\pi}{2} B_{lp}$ is its noise-equivalent value. In derivation of the above equation the bandwidth of the switch-and-capacitor, i.e. $\frac{1}{2\pi C_S R_{on}}$ is assumed larger than the loop bandwidth. The noise has an almost flat spectral density,³ and spreads evenly over 0 to $f_s/2$ when sampled. This noise power is sampled by the next stage, only if the sampling happens when S_S is closed, i.e. a two phase scheme. If the output is sampled in the next phase (hold) this continuous-time noise is not present, and instead the sampled noise on C_S and C_H at the end of ϕ_2 (as explained in the following paragraphs) should be taken into account.

Three phase case So far in this noise analysis, it has been assumed that this architecture uses a two phase clock, i.e. the next stage samples the output while ϕ_2 is still on. If according to the original design, a third hold phase exists, and the output is sampled by the next stage during that phase, another switched-capacitor noise component should also be added to the output.

The extra SC noise contribution is a part of the thermal noise of the sampling switch S_S that is sampled on C_H . The detailed derivation of this noise is laborious, but with some approximations sufficient insight may be obtained.

Within the bandwidth of the S/H opamp, its input node is kept at virtual ground. Outside this bandwidth, however, the node voltage at the input is determined by all the other nodes connected to it and their driving impedance. The output node

³This is not an exact statement only because of the use of noise equivalent bandwidth concept, which is a good approximation for $B_{lp} \gg f_s/2$.

of a two-stage opamp⁴ has a low driving impedance (to ground) outside the opamp bandwidth. Since the bandwidth of the opamp is usually much lower than the switch-capacitor circuit ($1/2\pi R_{on}C$), and all the sampled noise is eventually distributed over the 0 to $f_S/2$ bandwidth, the largest contribution to the sampled noise comes from the frequencies above the opamp bandwidth. For these reasons, the circuit model for this noise contributor may be greatly simplified.

The simplified circuit model for the effect of the sampled thermal noise of S_S is shown in Fig. C.2. The thermal noise voltage of the switch resistance is modeled with the noise source V_{nr} . The first step in this analysis is to find the noise voltage sampled on C_S at the end of ϕ_2 .

Figure C.2: Simplified schematic diagram for the noise analysis on the thermal noise of the sampling switch (S_S) in the first S/H architecture.

From the noise source (V_{nr}) point of view, the sampled thermal noise power on the series combination of C_S and $C_H + C_I$ is

$$\overline{v_{nC_{eq}}^2} = \frac{\Theta}{C_{eq}}, \quad (C.7)$$

where C_{eq} is defined here as

$$C_{eq} = \frac{C_S(C_H + C_I)}{C_S + C_H + C_I}. \quad (C.8)$$

Only a fraction of the above noise power appears on C_S . The noise power stored on C_S at the end of this process is

$$\overline{v_{nC_S}^2} = \left(\frac{C_H + C_I}{C_S + C_H + C_I} \right)^2 \frac{\Theta}{C_{eq}}. \quad (C.9)$$

⁴Two stage opamp is required for the second S/H stage, and has advantages for use in the first S/H stage as discussed in Chapter 6.

In the next phase (i.e. after the opamp is settled following the end of ϕ_2 transient) the input of the opamp reaches virtual ground again. In that state, a noise charge with the same amount as the one left on C_S is developed on C_H . Therefore the noise power on C_H (i.e. the output switched-capacitor noise power) is

$$\overline{v_{SC}^2} = \overline{v_{nC_H}^2} = \left(\frac{C_S}{C_H}\right)^2 \overline{v_{nC_S}^2} = \frac{C_S(C_H + C_I)\Theta}{C_H^2(C_S + C_H + C_I)}. \quad (C.10)$$

For a typical set of values, e.g. $C_S = C_I = C_H$, the above output noise component is about 67% (in power) of the thermal noise of the reset switch sampled on C_H . This is a significant rise in the thermal noise.

Since it is quite possible for the next S/H stage to sample the output of this stage when the sampling switch S_S is still closed in the transfer phase, an optimal choice can be made between the two-phase and the three-phase designs. In the two phase scheme, the thermal noise of R_{on} of S_S is continuous-time and band-limited by the opamp, therefore, it can be minimized to a negligible value by using a large switch. However, the sampled noise in a three-phase design is fairly independent of the switch size, and cannot be improved using larger switches. For this reason (and also the simplicity of timing) the two-phase arrangement is recommended for this architecture.

C.3 Second S/H Architecture

This architecture can be used both as the first S/H stage and the DT-to-CT converter. The noise analysis for these two applications are different.

C.3.1 Discrete-Time Noise

The schematic diagram of the second S/H architecture is shown in Fig. C.3. The transfer function for the input referred noise of the opamp, and the thermal noise of the switches are considered separately in the following sections.

Figure C.3: Simplified schematic diagram for the discrete-time noise analysis on the second S/H architecture.

Transfer Function for Opamp Noise

The opamp noise contribution within its loop bandwidth is derived by analyzing the SC network of Fig. C.3. Assuming a 50% duty cycle for the S/H clock, at the end of ϕ_1 , the charge stored on node N1 can be written as

$$Q_{\text{N1}}[n - \frac{1}{2}] = C_{\text{I}}V_{\text{na}}[n - \frac{1}{2}] + C_{\text{H}}(V_{\text{na}}[n - \frac{1}{2}] - V_{\text{out}}[n - \frac{1}{2}]), \quad (\text{C.11})$$

and at the end of ϕ_2

$$Q_{\text{NI}}[n] = (C_{\text{I}} + C_{\text{S}} + C_{\text{FB}})V_{\text{na}}[n] + C_{\text{H}}(V_{\text{na}}[n] - V_{\text{out}}[n]). \quad (\text{C.12})$$

The charge difference between these two phases is the amount delivered by C_{FB} , i.e.

$$Q_{\text{N1}}[n] - Q_{\text{N1}}[n - \frac{1}{2}] = C_{\text{FB}} V_{\text{out}}[n - \frac{1}{2}]. \quad (\text{C.13})$$

Replacing $Q_{N1}[n - \frac{1}{2}]$ and $Q_{N1}[n]$ from the previous equations yields

$$C_H V_{\text{out}}[n] - (C_H - C_{\text{FB}}) V_{\text{out}}[n - \frac{1}{2}] = (C_I + C_S + C_{\text{FB}} + C_H) V_{\text{na}}[n] - (C_I + C_H) V_{\text{na}}[n - \frac{1}{2}], \quad (\text{C.14})$$

that results in

$$\frac{V_{\text{out}}(z)}{V_{\text{na}}(z)} = \frac{C_{\text{I}} + C_{\text{S}} + C_{\text{FB}} + C_{\text{H}} - (C_{\text{I}} + C_{\text{H}})z^{-\frac{1}{2}}}{C_{\text{H}} - (C_{\text{H}} - C_{\text{FB}})z^{-\frac{1}{2}}}. \quad (\text{C.15})$$

in z -domain. A symmetrical S/H clock is assumed in the above equation, otherwise, $z^{-\frac{1}{2}}$ should be replaced with $z^{-\alpha}$, where α is the duty cycle of the transfer phase, as usual. This is a bilinear IIR noise transfer function.

In much the same way as the first S/H architecture, the WOLBW noise of the opamp, if significant, must be added to the above noise. This noise is directly sampled by the next stage (if this is the first S/H stage) at the output. The WOLBW noise is also sampled on C_S , C_{FB} , and C_I at the end of the transfer phase will be totally removed from the next sample if $C_{FB} = C_H$, otherwise a more detailed analysis is required.⁵

The WOLBW noise is also sampled by C_{FB} in the hold phase, and integrated in the next transfer phase. Due to its high undersampling ratio, the samples should be considered uncorrelated⁶ to the output noise in the last transfer phase, and their power should be added to the output after a gain of $\left(\frac{C_{FB}}{C_H}\right)^2$ (simply 1 for $C_{FB} = C_H$).

Switch Thermal Noise

The thermal noise of the switches closed in ϕ_2 appears as CT noise at the output if the next stage takes its sample in this phase. Similar to the first architecture, because this CT noise is band-limited by the opamp rather than the $1/2\pi R_{on}C$, it has a lower power than the sampled noise which exists at the output in ϕ_1 . Therefore, sampling by the succeeding stage should take place in ϕ_2 , and that has been the assumption so far in this section.

There are two components to the switch thermal noise at the output. First, CT thermal noise from the switches that are closed during ϕ_2 . This noise is sampled by the next stage at the f_S rate, and therefore its power up to the bandwidth of the

⁵Since the main advantage of this architecture over the third one is its flat frequency response for the case of $C_{FB} = C_H$, the sampling of the WOLBW noise on C_S , C_{FB} , and C_I at the end of the transfer phase for other cases is not analyzed here.

⁶This is a conservative overestimate, since due to the negative feedback through C_{FB} , any correlation resulting from the low-pass spectral density will reduce the noise power.

opamp folds back to the 0 to $f_S/2$ range. The total noise power contributed by all ϕ_2 switches in this manner is

$$\overline{v_{R_{on}}^2} = 2\pi \left(\frac{C_S}{C_H}\right)^2 \Theta R_{onS} B_{lp} + 2\pi \left(\frac{C_{FB}}{C_H}\right)^2 \Theta R_{onFB} B_{lp}, \quad (C.16)$$

where B_{lp} is the loop bandwidth around the opamp, and R_{onS} and R_{onFB} are the resistance in series with C_S and C_{FB} during ϕ_2 respectively. Applying a similar argument as in the first architecture case, it can be concluded that this noise has an almost flat power spectral density over 0 to $f_S/2$.

The second component of the switch thermal noise is the sampled noise. For both C_S and C_{FB} , noise is sampled at the end of ϕ_1 and ϕ_2 , however, the sampled noise on C_S at the end of ϕ_1 is attributed to the DAC (which is common for all S/H architectures) not to the S/H. The first part of this sampled thermal noise is the noise sampled on C_{FB} at the end of ϕ_1

$$\overline{v_{SC_{FB}}^2} = \frac{\Theta}{C_{FB}}. \quad (C.17)$$

The transfer function for this noise to the output is the similar to the input to the S/H through C_S . As derived in Appendix B, by replacing C_S with C_{FB} in Eq. B.6 this noise transfer function is obtained as

$$\frac{V_{out}(z)}{V_{SC_{FB}}(z)} = \frac{bz^{-1}}{1 - (1-b)z^{-1}}, \quad (C.18)$$

where b is defined as C_{FB}/C_H . Therefore, the power spectral density for this noise at the output is given by

$$\psi_{SC_{FB}}(\omega) = \frac{\Theta}{2\pi C_{FB}} \left| \frac{b}{1 - (1-b)e^{-j\omega}} \right|^2, \quad (C.19)$$

which is flat if $b = 1$.

Following the same argument as in the first architecture case, the noise sampled on the equivalent parallel combination of C_S and C_{FB} at the end of ϕ_2 is

$$\overline{v_{S(C_S+C_{FB})}^2} = \frac{\Theta}{C_{eq}}, \quad (C.20)$$

where C_{eq} here is defined as

$$C_{\text{eq}} = \frac{(C_S + C_{\text{FB}})(C_H + C_I)}{C_S + C_{\text{FB}} + C_H + C_I}. \quad (\text{C.21})$$

Deriving the transfer function of the filter for this sampled noise requires an additional care; this noise is sampled at the end of ϕ_2 at the input, and appears at the output in the next cycle.⁷ The charge transfer equation in this case should be written as

$$C_H V_{\text{out}}[n] = (C_H - C_{\text{FB}}) V_{\text{out}}[n-1] - (C_H - C_{\text{FB}}) \frac{C_S + C_{\text{FB}}}{C_H} V_{S(C_S+C_{\text{FB}})}[n-1], \quad (\text{C.22})$$

which leads to

$$V_{\text{out}}(z) = \frac{(C_H - C_{\text{FB}})z^{-1}}{C_H - (C_H - C_{\text{FB}})z^{-1}} \frac{C_S + C_{\text{FB}}}{C_H} V_{S(C_S+C_{\text{FB}})}(z), \quad (\text{C.23})$$

and the output noise power spectral density is

$$\psi_{S(C_S+C_{\text{FB}})}(\omega) = \frac{\Theta}{2\pi C_{\text{eq}}} \left(\frac{C_S + C_{\text{FB}}}{C_H} \right)^2 \left| \frac{(C_H - C_{\text{FB}})}{C_H - (C_H - C_{\text{FB}})e^{-j\omega}} \right|^2. \quad (\text{C.24})$$

As expected, this noise component is identically zero if $C_{\text{FB}} = C_H$, i.e. if the S/H has a flat frequency response for the input. Generally, the total thermal noise power from the switches is the sum of Eq. C.16, Eq. C.19, and Eq. C.24.

C.3.2 Continuous-Time Noise

For the second S/H stage, where the output is constantly connected to the next stage (probably a CTRCF), the CT noise must be calculated. This noise consists of two types: direct and sampled-and-held.

The direct noise is the one that is present at the output right at the time it is being generated, therefore, there is a *direct* connection between the source and the output.

⁷The thermal noise of these switches in the same ϕ_2 , as they are being sampled, is a CT noise which was considered before.

The sampled-and-held noise is the noise voltage that is stored on a capacitor resulting from a sample taken from the output of a noise source in the past.

For all the analysis in this section, since only the continuous-time noise at the output is of interest, valid approximations for the noise spectra and transfer functions up to $f_S/2$ are used. All the thermal noise powers referred to in this section denote the accumulated power between 0 to $f_S/2$, unless otherwise noted.

As a conservative overestimate, the opamp bandwidth is assumed many times larger than $f_S/2$, which causes aliasing of the undersampled noise. Also, since the linearizing resistors used in the second S/H stage usually create a lower RC bandwidth than the opamp, the usual virtual ground estimate is employed for the analysis of the circuit around the opamp. Lower RC bandwidth also means that the switching circuitry is not effective at the frequencies outside the bandwidth of the opamp, and therefore, the WOLBW noise (if any) is not modulated and/or aliased and remains out-of-band. Thus, with this assumption, the WOLBW noise is not included in the analysis of the CT noise at all.

The very slowly varying $1/f$ or flicker noise (a few kHz bandwidth compared with above 1 MHz sampling rate) has very highly correlated samples, and should be treated differently. In fact, it can be fairly well estimated as an offset at the input of the opamp, and the gain of the S/H for that offset is valid for the flicker noise as well.

Aside from the flicker noise, the rest of the opamp noise (thermal) can be modeled with the thermal noise of an equivalent resistor at its input defined by

$$\overline{v_{na\theta}^2} = 4\Theta R_{na}B, \quad (C.25)$$

for any given bandwidth B .

Direct Noise

There are two sources for the direct noise: the input referred noise of the opamp, and the thermal noise of the switches (and their linear series resistance, if any). From these sources the latter contributes only during ϕ_2 .

Figure C.4: Simplified schematic diagram for the direct noise analysis on the second S/H architecture during ϕ_1 .

According to Fig. C.4, the direct noise at the output during ϕ_1 comes only from the opamp, and is equal to

$$V_{\text{out}} = \frac{C_H + C_I}{C_H} V_{\text{na}}. \quad (\text{C.26})$$

This voltage is present at the output only during the hold phase ϕ_1 , which is equivalent to multiplying it by a pulse train whose value is 1 for this phase, and is zero elsewhere. The effect of this modulation is similar to the one analyzed in [70], and since the opamp bandwidth is usually larger than $f_S/2$, the thermal portion of the output noise power between 0 to $f_S/2$ can be conservatively overestimated by

$$\overline{v_{\text{dna}\theta 1}^2} = (1 - \alpha) \left(\frac{C_H + C_I}{C_H} \right)^2 \overline{v_{\text{na}\theta}^2}, \quad (\text{C.27})$$

where $\overline{v_{\text{na}\theta}^2}$ is the power for the thermal input referred noise of the opamp in 0 to $f_S/2$, i.e. $2\Theta R_{\text{na}} f_S$.

The transfer function for the opamp noise, and the switch thermal noise during ϕ_2 can be derived from Fig. C.5. For the input referred noise of the opamp, the noise

Figure C.5: Simplified schematic diagram for the direct noise analysis on the second S/H architecture during ϕ_2 .

transfer function during this phase is

$$\frac{V_{out}(s)}{V_{na}(s)} = \frac{C_H + C_I}{C_H} + \frac{C_S/C_H}{1 + R_S C_S s} + \frac{C_{FB}/C_H}{1 + R_{FB} C_{FB} s}, \quad (C.28)$$

which has a flat portion and a low-pass portion. Since calculation of the effect of low-pass filtering on autocorrelation function, and thereby the spectrum of the noise can be quite involved, the usual overestimation is applied here and noise is assumed all white with the total power of

$$\overline{v_{dna\theta}^2} = \alpha \left(\frac{C_H + C_S + C_{FB} + C_I}{C_H} \right)^2 \overline{v_{na\theta}^2}. \quad (C.29)$$

This approximation is valid because the bandwidth of the opamp is considered several times larger than $f_S/2$ and noise components can be considered uncorrelated. The total noise power due to the opamp is

$$\overline{v_{dna\theta}^2} = 2 \left[(1 - \alpha) \left(\frac{C_H + C_I}{C_H} \right)^2 + \alpha \left(\frac{C_H + C_S + C_{FB} + C_I}{C_H} \right)^2 \right] \Theta R_{na} f_S. \quad (C.30)$$

The thermal noise of the resistors R_S and R_{FB} are also low-pass filtered. Based on Fig. C.5, these transfer functions are

$$H_{nR_S}(s) = \frac{C_S/C_H}{1 + R_S C_S s}, \quad (C.31)$$

and

$$H_{nR_{FB}}(s) = \frac{C_{FB}/C_H}{1 + R_{FB}C_{FB}s}, \quad (C.32)$$

The resistor noise is usually undersampled, i.e. the noise-equivalent bandwidth ($\pi/2$ times -3-dB bandwidth) is usually larger than half the sampling frequency ($f_s/2$). This means that as a result of modulation (turning noise on and off between phases) fold-over occurs, and the noise around $\pm n f_s$ folds back to the baseband. According to [70], depending on the undersampling ratios (i.e. $\frac{1}{2R_S C_S f_s}$ and $\frac{1}{2R_{FB} C_{FB} f_s}$), the output modulated noise power may be anywhere from α^2 (for no undersampling, ratio = 1) to α (for ratio = ∞) times smaller than the unmodulated thermal noise power. However, that conclusion is based on high undersampling which uncorrelates the samples. In the current application, where the additional linearizing resistors make their noise very low-pass, and therefore more correlated, this assumption leads to an underestimate of the resistor thermal noise.

In fact, it can be seen from the schematic of this circuit, that the baseband portion of the thermal noise across R_S and R_{FB} reaches the output through a similar transfer function as the input to the S/H. For $C_{FB} = C_S = C_H$, the conservative estimate for the thermal noise density of the resistors in the baseband is

$$\psi_{br} = 4\Theta R_S + 4\Theta R_{FB}, \quad (C.33)$$

which includes both the direct and the sampled-and-held parts.

The total direct thermal noise at the output is the sum of Eq. C.30, and Eq. C.33 (with Eq. C.33 also including the sampled-and-held baseband noise of the resistors).

Sampled-and-Held Noise

The sampled-and-held noise consists of the frozen noise voltage of the switch resistors R_S and R_{FB} , and the opamp input referred source V_{na} , at the output at the end of the transfer phase. The noise voltage that appears at the output (in the next hold

phase), is fed back in the next cycle through C_{FB} , and has its own DT and DT-to-CT transfer function according to the results of Appendix B. Since the third sample and hold architecture is superior in performance than this one, except for the lack of a flat frequency response option, only this special case is considered here. This means that $C_{FB} = C_H$ is assumed, and the sampled-and-held noise exists at the output only during the hold phase immediately following the transfer phase the noise was sampled in.

The sampled-and-held part of the opamp noise is the frozen output voltage due to the charge trapped on C_S and C_{FB} at the end of ϕ_2 . This noise is band-limited by the $R_S C_S$ and $R_{FB} C_{FB}$ time constants, since they are slower than the opamp to help its linearity in the second S/H stage. Therefore, the sampled-and-held thermal noise of the opamp due to C_S disconnection is [70]

$$\psi_{\text{shna}C_S\theta}(f) = \begin{cases} 4 \left(\frac{C_S}{C_H} \right)^2 \Theta R_{na} (1 - \alpha)^2 \text{sinc}^2 \left(\frac{(1-\alpha)f}{f_s} \right) & \frac{1}{4R_S C_S} < \frac{f_s}{2}, \\ 4 \left(\frac{C_S}{C_H} \right)^2 \Theta R_{na} \left(\frac{1}{2R_S C_S f_s} \right) (1 - \alpha)^2 \text{sinc}^2 \left(\frac{(1-\alpha)f}{f_s} \right) & \frac{1}{4R_S C_S} \geq \frac{f_s}{2}. \end{cases} \quad (\text{C.34})$$

in which the equivalent resistance is used to represent the thermal noise of the opamp. A similar equation can be written for the noise due to C_{FB} .

According to [70], the sampled-and-held thermal noise density of the R_S at the output can be approximated as

$$\psi_{\text{sh}R_S}(f) = \begin{cases} 0 & \frac{1}{4R_S C_S} < \frac{f_s}{2}, \\ 4 \left(\frac{C_S}{C_H} \right)^2 \Theta R_S \left(\frac{1}{2R_S C_S f_s} - 1 \right) (1 - \alpha)^2 \text{sinc}^2 \left(\frac{(1-\alpha)f}{f_s} \right) & \frac{1}{4R_S C_S} \geq \frac{f_s}{2}, \end{cases} \quad (\text{C.35})$$

where the baseband portion ($f < \frac{1}{f_s}$) is already included in the direct noise equation (Eq. C.33). Also, a similar expression can be written for the thermal noise of R_{FB} .

Finally there is the thermal noise of the switches (and resistors if any) sampled on C_S in the hold phase (ϕ_1) which is added to the input in ϕ_2 . The power of this noise is Θ/C_S and is spread between 0 and $f_s/2$. The noise is held for one whole period

(neglecting the transients for now), therefore, its spectral density is given by

$$\psi_{\text{sh}C_S}(f) = \Theta \frac{C_S}{C_H^2} \frac{2}{f_S} \text{sinc}^2 \left(\frac{f}{f_S} \right). \quad (\text{C.36})$$

Thermal noise of C_{FB} can be written in a similar fashion.

The total sampled-and-held noise power is the sum of all *six* components of Eq. C.34, Eq. C.35, and Eq. C.36 (including the corresponding ones for C_{FB}). The exact frequency response for the sampled-and-held noise sources also includes the effect of incomplete settling and the CT low-pass filtering (which cause droop at the end of baseband — Appendix B). However these effects are minor for noise in the lower part of the baseband and are neglected here.

Flicker Noise

Since the flicker noise of the opamp varies very slowly compared with the sampling frequency f_S , there is no aliasing effect, and the discrete-time and continuous-time values of that at the output are almost exactly equal.

Very accurate gain for the flicker noise referred to the input of the opamp, may be obtained from the DT noise analysis of the previous section. Simply by replacing $z^{-\frac{1}{2}}$ in Eq.C.15 with 1, this gain is obtained as

$$\left(\frac{V_{\text{out}}(z)}{V_{\text{na}}(z)} \right)_{1/f} = \frac{C_S + C_{FB}}{C_{FB}}. \quad (\text{C.37})$$

C.4 Third Architecture

Noise analysis for this architecture, similar to the second one is divided into two parts. The first part is the DT noise analysis which applies to the first S/H stage, whose output is sampled, and the second part of the analysis is for the second S/H stage with a CT output.

C.4.1 Discrete-Time Noise

The noise sources are the input referred noise of the opamp (WILBW), the WOLBW noise referred to the output of the opamp, and the thermal noise of the switches. The analysis is based on the simplified schematic of Fig. C.6.

Figure C.6: Simplified schematic diagram for the discrete-time noise analysis on the third S/H architecture.

Transfer Function for Opamp Noise

The total charge on node N1 at the end of ϕ_2 is given by

$$Q_{N1}[n] = C_I V_{na}[n] + (C_H + C_S)(V_{na}[n] - V_{out}[n]). \quad (C.38)$$

The charge difference on N1 between samples $n - 1$ and n is the amount taken away and dissipated by C_S during ϕ_1 , i.e.

$$Q_{N1}[n] = Q_{N1}[n - 1] - C_S(V_{na}[n - 1] - V_{out}[n - 1]). \quad (C.39)$$

Therefore,

$$\begin{aligned} (C_H + C_S + C_I)V_{na}[n] - (C_H + C_S)V_{out}[n] = \\ (C_H + C_S + C_I)V_{na}[n - 1] - (C_H + C_S)V_{out}[n - 1] - C_S V_{na}[n - 1] + \\ C_S V_{out}[n - 1], \end{aligned} \quad (C.40)$$

and after simplification

$$(C_H + C_S)V_{out}[n] - C_H V_{out}[n-1] = (C_H + C_S + C_I)V_{na}[n] - (C_H + C_I)V_{na}[n-1]. \quad (C.41)$$

The corresponding equation in z -domain yields the noise transfer function as

$$\frac{V_{out}(z)}{V_{na}(z)} = \frac{C_H + C_S + C_I - (C_H + C_I)z^{-1}}{C_H + C_S - C_H z^{-1}}. \quad (C.42)$$

The above derivation applies only to the noise within the loop bandwidth of the opamp, the output referred noise of the opamp outside the -3-dB loop bandwidth (WOLBW) must also be included in the calculations, if it is substantial. This noise is sampled directly by the next stage similar to the first S/H architecture. However, there is also a part that is sampled on C_H as explained below.

Figure C.7: Simplified schematic diagram for analysis of WOLBW noise on the third S/H architecture. The output referred noise source V_{nao} only includes the noise beyond the loop bandwidth.

The sampling of the WOLBW noise is different from that of the input referred noise analyzed before, because the feedback loop around the opamp is not effective for these frequencies. The simplified model is shown in Fig. C.7, in which the output referred noise source for the opamp, V_{nao} only contains the noise beyond the loop bandwidth, but within the noise equivalent bandwidth of C_S and its switches. At the moment of opening the switches at the end of the transfer phase, some noise charge with the value of $\frac{C_S C_I}{C_H + C_S + C_I} V_{nao}$ is stored on C_S . An equivalent charge (with opposite

polarity) is left on the other two capacitor plates on node N1, which will be gradually transferred to C_H , developing an output voltage of $\frac{C_S C_I}{C_H(C_H + C_S + C_I)} V_{\text{nao}}$. In the next transfer phase this charge is divided between C_H and C_S , and the output noise due to this sample is smaller by $\frac{C_H}{C_H + C_S}$ in voltage. Assuming no correlation between samples of V_{nao} (due to high undersampling), the noise power from successive samples should be added up at the output to yield the total output noise caused by this source. After including the noise voltage sampled directly by the next stage we have

$$\begin{aligned}
 \overline{v_{\text{WOLBW}}^2} &= \overline{v_{\text{nao}}^2} + \left[\left(\frac{C_H}{C_H + C_S} \right)^2 + \left(\frac{C_H}{C_H + C_S} \right)^4 + \left(\frac{C_H}{C_H + C_S} \right)^6 + \dots \right] \\
 &\quad \frac{C_S C_I}{C_H(C_H + C_S + C_I)} \overline{v_{\text{nao}}^2} \\
 &= \overline{v_{\text{nao}}^2} + \frac{C_H^2}{C_S^2 + 2C_S C_H} \frac{C_S C_I}{C_H(C_H + C_S + C_I)} \overline{v_{\text{nao}}^2} \\
 &= \left[1 + \frac{C_H C_I}{(C_S + 2C_H)(C_H + C_S + C_I)} \right] \overline{v_{\text{nao}}^2}, \tag{C.43}
 \end{aligned}$$

using binomial expansion.

Switch Thermal Noise

When this S/H circuit is used in the first S/H stage, the second stage samples the output during the transfer phase. The equivalent circuit for this phase is redrawn in Fig. C.8. The R_{on} shown in the figure is the series combination of the on-resistance of the two switches involved.

Assuming a single pole approximation for the opamp gain, it can be written as

$$A(s) = \frac{A_0}{1 + s/\Omega_0}, \tag{C.44}$$

where A_0 is the DC gain, and Ω_0 is the dominant pole of the opamp. Then, using the fact that $A_0 \gg 1$, the transfer function for the resistor noise V_{nr} may be estimated by

$$\frac{V_{\text{out}}}{V_{\text{nr}}} = \frac{C_S A_0}{(C_H + C_S) A_0 + \left(C_H C_S R_{\text{on}} A_0 + \frac{C_H + C_S + C_I}{\Omega_0} \right) s + \frac{(C_H + C_I) C_S R_{\text{on}}}{\Omega_0} s^2} \tag{C.45}$$

Figure C.8: Simplified schematic diagram for the noise analysis on the continuous-time thermal noise of the sampling switches in the third S/H architecture.

For the first S/H, R_{on} is chosen so that $C_S R_{on} < \frac{1}{A_0 \Omega_0}$ (which is the gain-bandwidth product of the opamp), hence, the above transfer function can be simplified to

$$\frac{V_{out}}{V_{nr}} = \frac{\frac{C_S}{C_H + C_S}}{1 + s/B_{lp}}, \quad (C.46)$$

where

$$B_{lp} = \frac{C_H + C_S}{C_H + C_S + C_I} A_0 \Omega_0 \quad (C.47)$$

is the loop bandwidth around the opamp. This low-pass filter has a DC gain of $\frac{C_S}{C_H + C_S}$ (which is always less than 1) and a noise equivalent bandwidth of $B_{lp}/4$, therefore, the total sampled noise power for R_{on} is given by

$$\overline{v_{R_{on}}^2} = \left(\frac{C_S}{C_H + C_S} \right)^2 \Theta R_{on} B_{lp}, \quad (C.48)$$

At the end of the transfer phase, when the respective switches open, their thermal noise is sampled and held on C_H . In an analysis similar to the first architecture (sampled thermal noise in the three phase case) this noise contribution is found to be given by Eq. C.10 for the first S/H stage. In the next transfer phase, the corresponding noise charge is shared between C_S and C_H . Therefore, its noise voltage contribution to the output in the next sample is smaller by $\frac{C_H}{C_H + C_S}$. Since the thermal noise has a white spectrum, i.e. the successive samples are independent, the power of the switched-

capacitor noise at the output is given by

$$\overline{v_{\text{nscout}}^2} = \left[\left(\frac{C_H}{C_H + C_S} \right)^2 + \left(\frac{C_H}{C_H + C_S} \right)^4 + \left(\frac{C_H}{C_H + C_S} \right)^6 + \dots \right] \overline{v_{\text{nCH}}^2}. \quad (\text{C.49})$$

Using binomial expansion formula, the above sum can be written as

$$\overline{v_{\text{SC}}^2} = \frac{C_H^2}{C_S^2 + 2C_S C_H} \overline{v_{\text{nCH}}^2}, \quad (\text{C.50})$$

which after using Eq. C.10 can be simplified to

$$\overline{v_{\text{SC}}^2} = \frac{(C_H + C_I)\Theta}{(C_S + 2C_H)(C_S + C_H + C_I)}. \quad (\text{C.51})$$

Since the noise sources are independent (in case of R_{on} it is white noise), the total DT noise power is the sum of the opamp noise, $\overline{v_{R_{\text{on}}}^2}$, and $\overline{v_{\text{SC}}^2}$.

C.4.2 Continuous-Time Noise

Similar to the second architecture, the direct and sampled-and-held noise for this architecture are analyzed. The noise power of interest is in the 0 to $f_s/2$ band. A separate treatment of the flicker noise, and the special case of the single-phase S/H are also included.

Direct Noise

The direct noise of the opamp is present at the output during both phases, but with different gains. The direct thermal noise of the switches (and resistors) contributes only during the transfer phase ϕ_2 .

The schematic diagram for the hold phase is exactly the same as the second architecture, i.e. Fig. C.4, hence it has a similar gain for the noise source V_{na}

$$V_{\text{out}} = \frac{C_H + C_I}{C_H} V_{\text{na}}. \quad (\text{C.52})$$

Figure C.9: Simplified schematic diagram for the direct noise analysis on the third S/H architecture during ϕ_2 .

During the transfer phase, the circuit changes to that of Fig. C.9. The noise transfer function in this case is

$$\frac{V_{\text{out}}(s)}{V_{\text{na}}(s)} = \frac{C_H + C_S + C_I + R_S C_S (C_H + C_I)s}{C_H + C_S + R_S C_H C_S s}, \quad (\text{C.53})$$

which is a bilinear function with a higher pole frequency than its zero. As a simplifying overestimate, the slight noise reduction at lower frequencies is neglected, and the amount of direct noise from the opamp is approximated as

$$\overline{v_{\text{dna}\theta}^2} = \left(\frac{C_H + C_I}{C_H} \right)^2 \overline{v_{\text{na}\theta}^2}, \quad (\text{C.54})$$

for the thermal noise in the 0 to $f_S/2$ band, and the density of this noise power in the baseband is

$$\psi_{\text{dna}\theta} = 4 \left(\frac{C_H + C_I}{C_H} \right)^2 \Theta R_{\text{na}}. \quad (\text{C.55})$$

The transfer function for the direct resistor noise to the output during the transfer phase is

$$\frac{V_{\text{out}}(s)}{V_{\text{nr}}(s)} = \frac{\frac{C_S}{C_H + C_S}}{1 + s R_S C_{\text{eq}}}, \quad (\text{C.56})$$

where $C_{\text{eq}} = \frac{C_H C_S}{C_H + C_S}$.

The exact analysis of the contribution by the resistor noise in a general case is fairly involved due to complicated correlations between the direct and the sampled-and-held noise components, hence, two simplified cases are considered here. First, if $\frac{1}{2\pi R_S C_{eq}} \gg \frac{f_S}{2}$, the undersampling ratio is very high, therefore [70],

$$\psi_{dr} = 4\alpha \left(\frac{C_S}{C_H + C_S} \right)^2 \Theta R_S. \quad (C.57)$$

In this case, the sampled-and-held noise should be calculated separately and added.

Secondly, if $\frac{1}{2\pi R_S C_{eq}} < \frac{f_S}{2}$, the direct and sampled-and-held noise components are highly correlated and the circuit transfer function for the resistor noise is the same as the input signal. This case is considered in the following section.

Sum of the values from Eq. C.55, and Eq. C.57 yields the total direct thermal noise density in the baseband (Eq. C.57 will be obsolete if Eq. C.60 is used).

Sampled-and-Held Noise

In this architecture, unlike the second one, there is no opamp noise that is sampled on the holding capacitor. The opamp noise that is sampled on the sampling capacitor C_S is discharged in the next hold phase, and does not appear at the output.

Similar to the direct noise analysis, two simplified cases are considered here. First, for $\frac{1}{2\pi R_S C_{eq}} \gg \frac{f_S}{2}$, the noise samples are uncorrelated and their powers should be added. The energy of each sample at the output is $\left(\frac{C_S}{C_H + C_S} \right)^2 \frac{\Theta}{C_{eq}}$, where $C_{eq} = \frac{C_H C_S}{C_H + C_S}$. This energy is present at the output only for the duration of one hold phase, and is later attenuated by the IIR filtering function of the S/H. The overall DT sampled-and-held noise power at the output (prior to DT-to-CT conversion) is

$$\begin{aligned} \overline{v_{shr}^2} &= (1 - \alpha)^2 \left(\frac{C_S}{C_H + C_S} \right)^2 \frac{\Theta}{C_{eq}} + \\ &\quad \left(\frac{C_S}{C_H + C_S} \right)^2 \frac{\Theta}{C_{eq}} \left[\left(\frac{C_H}{C_H + C_S} \right)^2 + \left(\frac{C_H}{C_H + C_S} \right)^4 + \left(\frac{C_H}{C_H + C_S} \right)^6 + \dots \right] \\ &= \left(\frac{C_S}{C_H + C_S} \right)^2 \frac{\Theta}{C_{eq}} \left[(1 - \alpha)^2 + \frac{C_H^2}{C_S^2 + 2C_S C_H} \right], \end{aligned} \quad (C.58)$$

with the help of binomial expansion formula.

In the second case of $\frac{1}{2\pi R_S C_{eq}} < \frac{f_S}{2}$, the high degree of correlation between the direct noise and the noise samples, noise components do not add in power, but in amplitude. A better approach to this case is to write the transfer function for the resistor noise to the output. Since the noise voltage source in series with R_S is also in series with C_S in the transfer phase, the noise voltage source can be equivalently considered at the input to the S/H stage. Therefore, the transfer function of Eq. B.22 applies in this case too, i.e.

$$\frac{V_{out}(z)}{V_{nr}(z)} = \frac{a(1 - e^{-aT/\tau})z^{-1}}{1 + a - (1 + ae^{-aT/\tau})z^{-1}}. \quad (C.59)$$

This low-pass transfer function has a DC gain of 1.

If $\frac{1}{2\pi R_S C_{eq}} \ll \frac{f_S}{2}$, the resistor noise power concentrates in the most important section of the baseband, i.e. the signal bandwidth. The overall power of the resistor noise (limited by the noise equivalent bandwidth of the $R_S C_{eq}$ filter) is Θ/C_{eq} . On the other hand, when $\frac{1}{2\pi R_S C_{eq}} > \frac{f_S}{2}$, some of the out-of-band resistor noise folds back to the baseband and the reduction in the noise floor is not significant. Besides, if R_S is made too small, it cannot improve the CT linearity very much.

As a conservative overestimate, the overall resistor noise (Θ/C_{eq}) is considered spread between 0 and $f_S/2$ before passing through the DT-to-CT response of the S/H. This overestimation is valid only if $\frac{1}{2\pi R_S C_{eq}} \geq \frac{f_S}{2}$, and R_S values larger than $\frac{1}{\pi f_S C_{eq}}$ will increase the output noise.

The thermal noise power sampled on C_S in the hold phase (while sampling the input) should also be added to the sampled-and-held noise. Finally, the output noise is shaped by the DT and DT-to-CT transfer function of the S/H.⁸ However, at the most important frequencies, i.e. $f \ll f_S/2$, the thermal noise at the output is flat and

⁸The direct noise of the opamp and the resistor is shaped only by the CT response of the circuit, but since these represent only a small portion of the overall noise, the entire noise can be considered shaped by the DT response without loss of much accuracy.

its density is given by the sum of Eq. C.55 and

$$\psi_r = \left(\frac{\Theta}{C_S} + \frac{\Theta}{C_{eq}} \right) \frac{2}{f_s}. \quad (\text{C.60})$$

Flicker Noise

Using similar arguments as in the second architecture case, the transfer function for the flicker noise of the opamp to the output can be obtained from Eq. C.42 by replacing z^{-1} with 1, which results in unity.

C.4.3 Single-Phase Sample-and-Hold

The output noise estimate due to the opamp noise for this type of S/H circuit is the same as the two phase case. This is because the best estimate was obtained by assuming of a constant gain for the thermal noise of the opamp to the output regardless of the phase (mixed direct and sampled-and-held noise). Thus, the opamp noise for this circuit can also be obtained from Eq. C.55.

In the single phase S/H, two sets of resistors (R_S) in series with two C_S contribute to the output noise. The alternating exchange of these resistors is analogous to the modulation of their noise by interleaving pulse trains, and due to resistors white noise spectrum (no correlation from sample to sample) this alternation does not affect the amount of noise at the output. Therefore, the thermal noise of the resistors is also the same as the two phase case given by Eq. C.60.

Appendix D

Application of $\Sigma\Delta$ M in Capacitor Matching Measurements

Integrated capacitors have many applications in analog circuits, such as continuous-time and switched-capacitor filters, and data converters. The absolute value of these capacitors changes significantly ($\pm 10\%$ to $\pm 15\%$) by process variations. However, capacitor ratios on the same die, which is much more critical in SC filters and converters, is fairly accurate. The accuracy of capacitor ratios, or the matching accuracy between identically drawn capacitors, is a very crucial process factor in converter design.

Capacitors used in integrated circuit design are usually in the order of 1 pF, with matching accuracies in the order of 0.1%. It is difficult to characterize the capacitor ratios by direct measurement for a couple of reasons. First, the capacitor values are small and the precision is very limited in determining these values. Secondly, if an off-chip measuring instrument is used, parasitics can affect the measured values. It is, therefore, highly desired to design a simple on-chip circuit that can measure capacitor ratios with sufficient accuracy.

D.1 Methodology

To obtain reliable information about the statistical distribution of capacitor ratios, measurement accuracy should be better than 0.01%. Such accuracies are relatively easily obtained in $\Sigma\Delta$ A/D converters.

Figure D.1: Schematic diagram of capacitor matching measurement circuit.

A $\Sigma\Delta$ circuit is shown in Fig. D.1, that is capable of measuring multiple capacitor ratios with high precision. The circuit is essentially a first-order $\Sigma\Delta$ with multiple input capacitors, which are selected through a digital control bus S . Only the capacitor(s) C_x that are activated (by their S_x control set) participate in the conversion process.

Any digital decimation filter may be used to decode the output of the modulator,

but an up/down counter is preferred because of its simplicity and guaranteed accuracy [63]. The input voltage V_{in} can be any value in the input voltage range, however, it is recommended to tie it to one of the reference input voltages $V_{\text{ref}+}$ or $V_{\text{ref}-}$. In this manner, the normalized digital output (to a full scale of 1) yields the ratio C_x/C_I . Since C_I is common among all the capacitors to be measured, capacitor ratios such as C_1/C_2 are easily derived as the ratio of the digital outputs.

In order to avoid any offset error and reduce the effect of flicker noise, it is highly recommend to perform offset cancellation through two consecutive polarized ratio measurement with V_{in} switched from $V_{\text{ref}+}$ to $V_{\text{ref}-}$ (or ground) and subtracting the results.

D.2 Implemented Experiments

The method introduced in this appendix is used in two capacitor matching experiments implemented on the same chip in 0.35- μm CMOS process. The first experiment measures poly-to-poly capacitor matching and is not affected by mismatch between parasitics. The second experiment also includes parasitic capacitors in the measurement.

D.2.1 First Experiment

The aim of this exercise is to evaluate capacitor matching accuracy in a stray insensitive fashion shown in the schematic of Fig. D.1. Four identically drawn capacitors (C_1 to C_4) with x and y axes symmetry are used. A rough layout view of this experiment is demonstrated in Fig. D.2.

Each of the 4 poly-to-poly capacitors has a nominal value of 1 pF, and C_{FB} and C_I , that are broken into two pieces each (for symmetry), are 1.1 pF and 3 pF respectively. The layout of this circuit closely resembles the layout of a cyclic DAC, however, the

Figure D.2: Rough layout of the capacitor matching experiment implemented.

capacitors are twice the size of the capacitors used in the cyclic DACs of this thesis. Because of a single-ended $\Sigma\Delta$ M design, only one opamp is in this circuit which creates some asymmetry in the layout.

The circuit has been run at 3 V supply voltage, nominal bias conditions, and 2.3 MHz clock frequency. 256 k samples have been collected from the output of the modulator after reset for each capacitor under test, for V_{in} at both reference voltages, and then the results were subtracted to cancel the offset. The measurements had repeatability error of less than 50 ppm (equivalent to 50 aF nominally).

The capacitor ratios obtained from the measurements on 8 functional samples of the device indicate individual matching properties of Fig. D.3. From these histograms, it is obvious that despite some effort to create a symmetrical layout (around the capacitors under test), the capacitor values have average variations based on their position. For example, C_1 is the smallest and C_4 is the largest (absolutely, not just on average!).

One classic technique for improving capacitor matching accuracy is the use of the common centroid topology. The effectiveness of this method is observable in Fig. D.4. Here the ratio of sum of two capacitor values to the other two is considered.

Figure D.3: Distribution of individual capacitor ratios between all capacitors of the first matching experiment on 8 devices.

From all the possible combinations of capacitor-pair matching, the common centroid connection (C_1+C_4 versus C_2+C_3) indicates an exceptional improvement in matching accuracy. The standard deviation for this capacitor ratio is less than 62 ppm.

Figure D.4: Distribution of capacitor-pair mismatches for all combinations of the first matching experiment on 8 devices.

D.2.2 Second Experiment

Conversion accuracy in quasi-passive algorithmic DACs depends on the matching of total capacitance on the charge sharing nodes. Although the proportion of the parasitic capacitance to the main one is usually below 20%, if the mismatch between the parasitics is much larger than the main capacitors, it may deteriorate the performance significantly. Therefore, it is crucial to have an estimate about the matching accuracy of the capacitors *including* the stray ones. For this purpose, a *stray sensitive*

switched-capacitor circuit has to be employed.

Figure D.5: Schematic diagram of the capacitor matching experiment which includes parasitics.

The circuit of Fig D.5 is a simple modification of Fig. D.1 which measures capacitor ratios C_{T1}/C_{FB} , C_{T2}/C_{FB} , etc. (C_{Tx} is the total capacitance on the top plate of C_x).

With a layout similar to Fig. D.2, and same testing conditions, the results of this experiment are shown in Fig. D.6 and Fig. D.7. The results are very similar to the first experiment, and again the best matching is obtained by the common centroid method.

Figure D.6: Distribution of individual capacitor ratios between all capacitors of the second matching experiment on 8 devices.

Figure D.7: Distribution of capacitor-pair mismatches for all combinations of the second matching experiment on 8 devices.

Appendix E

FPGA Interface for Signal Handling

E.1 Introduction

Testing analog integrated circuits including A/D and D/A converters, requires a special digital interface to a main controller. The digital interface should not only send the appropriate commands to program the Device Under Test (DUT) in different modes, but also handle the digital signals going to, and coming from the converters. This special interface is on one side connected to a host computer, and on the other side to various ports of a mixed signal chip.

Full functionality of the digital interface can be implemented in a Field Programmable Gate Array (FPGA). The FPGA designs are very flexible, and in today's technology relatively fast. The FPGA Interface for Signal Handling (FISH) is a general purpose interface between a GPIB controller and A/D and D/A converters. The features include:

- GPIB interface for versatility and speed
- Large synchronous static RAM chips for simple and fast interface to a variety of converters

- Independent memory operations for Mem0 and Mem1
- Two extra ports for programming and control of converters
- Very fast and high density FPGAs (optionally up to XC4085XLA)
- FPGA programmability through cable and SPROM
- Optional 3.3 V to 5 V converter for 5 V SPROMs and cable
- TTL compatible 5 V tolerant I/O
- Prototyping area for expansion

E.2 General Description

Block diagram of the FISH is shown in Fig. E.1. The core of the design is an XC4000XLA FPGA from Xilinx in QFP240 package. Except for the GPIB interface buffers, and memories, the rest of the logic is implemented inside the FPGA. The flexibility of the FPGA allows special implementations on the same hardware. For the simple functionality of the FISH, an XC4013XLA (smallest in the family) is more than enough. For more elaborate designs, including some DSP in the FPGA, larger densities can be used. The current hardware design does not allow use of heat-sinks for the FPGA underneath it, but if heat-sinks over the top are sufficient, HQ240 packages may be used.

The GPIB buffers allow bidirectional communication with GPIB with adequate drive and speed. Full GPIB functionality can be implemented, although in the simple implementation of the first FPGA version, some functions such as interrupt request have been left out.

Two memory chips have been used in the design to deliver two independent converters interfaces, Mem0 and Mem1. This feature is handy when two converters on

Figure E.1: Block diagram of the FPGA interface for signal handling (FISH).

the same chip (DUT) are tested. Also, one port can drive a D/A on the DUT while the other one collects data from an A/D converter analyzing the output of the DUT, and so on. Complete independence is achieved through separate data and address ports. The 22-bit width of the address ports allows the use of 4 M sample memories, while the 18-bit wide data ports are enough for most converters (higher resolution ones can use both memories). The memories are of synchronous pipelined Zero Bus Turn-around (ZBT) SRAM which can run at frequencies in excess of 100 MHz. The current FPGA code, however, is not optimized for speed and does not permit higher than 50 MHz. Because of the use of separate power supplies for the memories than the FPGA, 5 V, 3.3 V, or 2.5 V SSRAMs may be used on this board. The FPGA is a 3.3 V-only device.

The memory address is set by a 22-bit counter (inside the FPGA) called Memory Address Pointer (MAP). The counter can only be preset to zero (reset), then it is incremented automatically on every read or write through GPIB or DUT.

The DUT interface ports have 3 groups. Group0 is Port0, Port1, and the lower half of Clocks. This group is more suitably programmed for access to Mem0. To avoid possibility of interference with configuration of the FPGA, it is recommended to use Group0 for interface to D/A converters. (This allows JTAG programming pins, i.e. TDI, TCK, and TMS, to be pulled-up internally, and be held high during configuration.) Group1 is Port3, Port4, and the upper half of Clocks. Finally Group3 consists of two 8 bit ports for slower digital signals intended for control only. The pinout of the ports is designed compatible with HP16500 series logic analyzers, although an adaptor is needed to convert the connector type. The same FPGA pins that go to Port4 and Port5, are available on a 20 pin header beside the prototyping area which makes it suitable for expansion for special designs using wire-wrap technology.

A 50 MHz oscillator runs the main clock to the FPGA, which regulates the timing of various functions. The clock can tolerate 5 V supply, but 3.3 V is recommended.

The switching regulator is designed to provide 5 V supply to run 5 V SPROMs and configuration cables (Xchecker or parallel). If 3.3 V SPROM is used (highly recommended) this supply can be disabled (no power to VCC5 and remove JP25).¹ Also in this case, connect a 3.3 V supply to VCC1, VCC2, and VCC4, and a proper one to VCC3 for the memories (MCM63Z818 is 3.3 V only too). If a 5 V cable is used in this mode, it can be powered from an external 5 V power supply (don't forget to share the grounds as the reference!). If a 5 V supply is needed for SPROM, JP25 should be shorted, and the 3.3 V supply *must* be removed from VCC2 and connected to VCC5 instead. If all this is too confusing, take a look at the schematic, it is really simple! Disabling the switching regulator is also recommended for avoiding its switching noise.

The GPIB address should be set using the micro DIP switch provided. Only addresses from 1 to 30 may be programmed using the rightmost 5 switches (P129 to P133 of the FPGA). An "ON" switch represents a "1" in the respective bit. The settings on these switches is read only upon configuration. It is Ok. to flip them when power is up, but reconfiguration (i.e. cycling power when SPROM is used) is necessary for the new address to become effective.

The FPGA can be programmed either through the cable interface (Xchecker, or parallel) or using a serial PROM. Care must be taken to ensure proper supply voltage is used for these devices. With the on-board 3.3 V to 5 V switching regulator, both options are available. The configuration mode of the FPGA is determined by the state of 3 mode input pins. The useful modes are Master Serial (M0, M1, and M2 grounded through less than 4.7 k Ω – shorts are Ok.) for loading through cables, and Slave Serial (M0, M1, and M2 pulled to VCC1 – open is Ok. with internal pull-ups) for loading from SPROM. The recommended serial PROM for XC4013XLA FPGA is XC17512L which runs from 3.3 V supply (same as FPGA) and has enough capacity

¹Please consult the schematic of this board for understanding detailed instructions.

(any larger one would do too, but will be more expensive).

The Config LED (RED) turns off when the FPGA is properly configured. This takes approximately a second after power up when the SPROM is used. Upon configuration, all internal registers are set to zero. A green LED (Power) indicates live supply for the board.

The optional “Ex Clk” input is used as an active high reset input for the FPGA in version 1 design. The use of this input is not necessary. Upon setting a high (TTL level) on this input (watch the 50 Ω termination on board) all the internal registers of the FPGA are reset to zero (same as after configuration).

E.2.1 Port Pinouts

The pinout of the ports are designed to be similar to the HP16522 pattern generator. However, there are minor differences (refer to HP16522 manual for comparison).

Group0 and Group1 Ports

Port0 and Port1 are the I/O access ports to Mem0 with the pinout of Fig. E.2. The pinout is the same for Group1. Bits 0 to 17 are the memory I/O bits, TCI (Tri-state Control Input) is an input used to tri-state the respective port only when high (internally pulled low).

The Clocks port has the clock input pins for both Group0 and Group1. These clocks are positive edge triggering. There are four reserved pins (RES) on this port which are not programmed in Ver.1.

Group3 Ports

Port4 and Port5 have the pinout of Fig. E.4. Bits 0 to 7 are I/O bits, CLK is an input used to latch data in when the port is programmed as input (see following sections), and STB is a strobe output pulse on every read (for input ports) or write (for output

Figure E.2: Pinout of Port0 through Port3.

Figure E.3: Pinout of Clocks port.

ports).

E.3 GPIB Programming Functions in FPGA Load Version 1

FPGA load determines the functionality of the board and the GPIB interface (if implemented at all). The simple version of the FPGA load, i.e. Version 1, has the following programming modes and format for the GPIB.

Figure E.4: Pinout of Port4 and Port5.

E.3.1 GPIB functions

The only GPIB functions implemented in V1 are write and read. Upon power up (or reconfiguration), the GPIB address is read from the DIP switch settings. Every write to the set GPIB address affects the respective register (defined in the write format later). Every read from the same address returns the value from the register addressed for reading (see the read format section).

E.3.2 Write Format and Addresses

The write command format (with the exception of writing the Read Address Register to be explained later) is shown in Table E.1. The write command starts with the FPGA register address to be written to, which is one byte long. The available write addresses are shown in Table E.2. The next three bytes in the format specify the number of bytes to follow. The bytes that follow will be written to the specified address, and the FISH will be ready to accept new write address. The “Count” is a natural number, i.e. 1 means only one data byte will follow. Count of zero means 16777216 data bytes. Since there is no way of interrupting a write, other than a read (GPIB EOI is not implemented), care must be taken to specify the right number of bytes in Count.

The definitions of the writable registers are in the following subsections. All the writable registers are readable, but some registers are read-only to be presented later (see Table E.4).

Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	...	Byte N+4
Write Address	Count (MSB to LSB)			Data 1	Data 2	...	Data N

Table E.1: GPIB write command format

Write Address (Hexadecimal)	Register Definition
0X10	Read Address Register
0X20	Active LEDs
0X40	Port4 Output Data
0X41	Port4 Status (only 4 MSBs writable)
0X50	Port5 Output Data
0X51	Port5 Status (only 4 MSBs writable)
0X60	Mem0 Data
0X61	Mem0 Stop Address
0X62	Mem0 Control
0X63	Mem0 Status
0X70	Mem1 Data
0X71	Mem1 Stop Address
0X72	Mem1 Control
0X73	Mem1 Status

Table E.2: Writable registers

Read Address Register

This register (RAR) holds the address of the register (or memory) to be read from. Therefore, prior to every read this register should be loaded with the proper address (the write does not have to immediately precede the read).

The format for writing into the RAR is different than the other writes, and is shown in Table E.3.

Byte1	Byte2
0X10	Read Address

Table E.3: Command format for writing to Read Address Register (RAR)

Active LEDs

This register controls the status of two Active LEDs (orange). Bit 0 is for Active 0, and Bit 1 is for Active 1. The rest of the bits are ignored.

Port4 and Port5 Data

Data written to these ports appears on Port4 and Port5 respectively, if the ports are defined as outputs. This feature allows checking for shorts on the outputs automatically.

Port4 and Port5 Status

These registers control the status of Port4 and Port5. Only the 4 MSBs are writable. Bit 7 is the output enable, i.e. the respective port is defined as output when this bit is set to 1.

Bit 5 is for clocked input. If the bit is set, when the port is defined as input (i.e. Bit 7 = 0), data is clocked in on the rising edge of P4CLK or P5CLK respectively. Otherwise, data is latched on the leading edge of P4STB or P5STB respectively.

The strobe pulse is a 60 ns (± 5 ns) active low which appears 40 ns (± 5 ns) after data is available on the output ports. For input ports, the strobe pulse is sent just before each input.

Bits 6 and 4 are reserved for future expansions.

Memory Stop Addresses

Memory Stop Address (MSA) registers specify the address for the last data word in memory. When capturing data (A/D), process can be stopped when the address pointer reaches the MSA. When delivering data (D/A) address pointer can be set to zero (for looping) after it reaches the MSA. The address is three bytes long, with the most significant one written first. It only makes sense to write 3 bytes into this address each time. This stop address is only effective when the memories are under DUT control, otherwise, when GPIB is reading from and writing to the memories, the setting of this register has no effect. Also, this address should not be set to or left at 0 before transferring control to the DUT.

Memory Control

Function of various bits in these registers follows:

Bit 7: Memory under DUT control if 1, else under GPIB control for read/write.

Bit 6: Synchronize clock enable with DUT clock if 1 – use it if clock pulses coming out of DUT are not stoppable by the FISH, otherwise (like using controlled multimeter pulses) leave at 0.

Bit 5: Direction (active high OE for memory) – 1 means memory to FPGA (to DUT), i.e. reading memory.

Bit 4: Repeat if 1 (for D/As), i.e. loop back to address zero after reaching MSA.

Bit 3: Reset counters (and keep them there) if 1.

Bit 2: Enable memory clock, i.e. memory ckeb = 0 if this bit is 1.

Bit 1: DUT ports enabled if 1 (may also need port tri-state control TSC of 0, see below).

Bit 0: DUT port tri-state override. If set to 1, does not care about tri-state control at the port, i.e. output port is always enabled.

Memory Data

Writing to these addresses puts data into the memories, if bit 7 of the respective control register is reset. The memory word is 18-bits wide, so three bytes are needed to hold it. Only the two LSBs of the most significant byte (written first) are used, then the middle byte and least significant bytes should follow. Therefore, for a data block of size N , $3 \times N$ bytes must be written. Data is read back in the same format, but the *first two words* (6 bytes) are pipeline *trash* which should be ignored (read two extra words at the end to compensate). After each word write to a memory data register, address is automatically incremented. To be certain where the data is written to, address pointer should be reset before each block write (bit 3 of memory control register).

E.3.3 Read Format

After specifying the read address (by writing to RAR), any read from the FISH will return one byte of data from the addressed register. It only makes sense to read 3 bytes from MSA registers, and read multiples of 3 bytes from memories. Similar to the write case, memory address is automatically incremented after each word read (3 bytes), and should be reset beforehand.

Some registers in the FPGA are read-only. A list of these registers is presented in Table E.4.

Port4 and Port5 Input Data

Data on Port4 and Port5 pins are always readable, even if these ports are defined as outputs. In order to do this (i.e. if loop-back is desired), since input data needs the

Read-Only Address (Hexadecimal)	Register Definition
0X42	Port4 Input Data
0X52	Port5 Input Data
0X63	Mem0 Status
0X73	Mem1 Status

Table E.4: Read-only registers

clock to latch in, the strobe output should be tied to clock input (STB to CLK), and bit 5 of port status register must be set.

Memory Status

Only bit 7 of this register is meaningful. If this bit is set, it indicates that memory is full, i.e. the MSA is reached.

E.3.4 Program Sequence for ADC Interface

Below is the sequence of steps to be taken for programming the FISH to interface with an A/D converter. Depending on which memory is chosen for this interface (Mem1 recommended) the commands have to be sent to the respective Memory Control Register (MCR).

- Set the desired memory stop address (MSA)
- Send 8'b0s001000 to MCR to set
 - memory under GPIB control
 - synchronize ($s = 1$) or not ($s = 0$) to DUT clock (synchronize for non-stoppable DUT clock)
 - disable memory output (FPGA data to memory)
 - no repeat

- reset address pointer (MAP)
- disable memory clock
- disable DUT ports
- DUT port tristate control active (don't care)
- Send 8'b0s000000 to MCR to set
 - release address pointer (MAP) reset
- Send 8'b1s000100 to MCR to set
 - memory under DUT control
 - enable memory clock

After the above sequence, release the device reset (through Port4/Port5, if necessary) to collect data after about 200 ns. Check the memory status register to find when the memory is full.

Optionally, turn on the proper active LED to indicate that the memory ports are active. It can serve as a verification for the software and hardware, and also function as a warning signal against removing the connection when the ports are active.

After detecting a full memory, perform the following steps to read the memory data into the controller.

- Send 8'b00101000 to MCR to set
 - memory under GPIB control
 - do not synchronize (don't care)
 - enable memory output (FPGA data to memory)
 - no repeat

- reset address pointer (MAP)
 - disable memory clock
 - disable DUT ports
 - DUT port tristate control active (don't care)
- Send 8'b00100100 to MCR to set
 - release address pointer (MAP) reset
 - enable memory clock

Then read stored data from the memory data location.

E.3.5 Program Sequence for DAC Interface

The procedure for sending a digital pattern out of the memory ports (either Group0 or Group1) for interfacing to D/A converters is presented in the following steps.

- Set the desired memory stop address (MSA)
- Send 8'b00001000 to MCR to set
 - memory under GPIB control
 - do not synchronize (don't care)
 - disable memory output (FPGA data to memory)
 - do not repeat pattern
 - reset address pointer (MAP)
 - disable memory clock
 - disable DUT ports
 - do not override DUT tri-state control (don't care)

- Send 8'b00000100 to MCR to set
 - release reset of address pointer (MAP)
 - enable memory clock
- Send the digital signal to the memory data register
- Send 8'b0s1r101g to MCR to set
 - synchronize ($s = 1$) or not ($s = 0$) to DUT clock (synchronize for non-stoppable DUT clock)
 - enable memory output (memory data to FPGA)
 - repeat pattern (if $r = 1$) for repetitive data (looping)
 - reset address pointer (MAP)
 - disable memory clock
 - DUT port tristate control (active if $g = 0$)
- Send 8'b0s1r001g to MCR to set
 - release reset of address pointer (MAP)
- Send 8'b1s11011g to MCR to set
 - memory under DUT control
 - enable memory clock

At the time of the last step, if the clock input from DUT to the FISH is 1, address is advanced by 1 (second data sample appears at the port). Same as the A/D converter case, the active LED may be turned on when the port is active.

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