

Minimizing nMOS Edge Leakage in Fully Depleted Silicon-on-Insulator CMOS using Poly-Buffered LOCOS Isolation

by

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Abstract

A process has been designed, implemented and tested to minimize edge-leakage effects in fully depleted silicon-on-insulator (FD SOI) nMOSFET (nMOS) devices encountered in previous student project SOI CMOS fabrication runs in the Carleton University Microfabrication Laboratory. A layout with test arrays, including enclosed geometry transistors, was designed to perform a test fabrication run. The process uses optimized oxidation steps and Poly-Buffered Local Oxidation of Silicon (PBL) isolation with minimal mask steps and fabrication time. The fabricated test transistors revealed that some subthreshold edge leakage was still present in the nMOS devices.

SEM imaging showed that the field oxide had been almost entirely unintentionally etched away during processing. This reduction in the field oxide thickness creates parasitic edge transistors. Sentaurus simulations imply that if not for this field oxide loss, the fabricated nMOS devices would have had minimal leakage with no kink in the subthreshold curve.

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Chapter 1 Introduction

1.1 Motivation

Thin film silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect transistors (MOSFET) are fascinating devices that offer low junction capacitance and a small back-gate-bias effect when compared to bulk silicon MOSFETs. These advantages lead to devices that can operate from a low-voltage supply and thus enable low-power operation [1]. One major issue that commonly arises with SOI is a high subthreshold leakage current in the nMOSFET devices, which results from a parasitic transistor formed at the edges of the device during isolation.

The Department of Electronics at Carleton University offers a course specific to integrated circuit design and fabrication (ELEC4609). In this course students design digital and analog circuits in a $2.5\mu\text{m}$ fully depleted SOI (FDSOI) CMOS technology. The circuits are then fabricated in Carleton's Microfabrication laboratory, and completed chips are returned for testing before the end of term. This FD SOI process is ideal for this course, as it allows CMOS circuits to be fabricated within a three-week period allowing students the opportunity to design and test circuits within the term. Runs of the process were completed in the winters of 2014 and 2015. Both runs delivered working circuits, but in both cases nMOS transistors demonstrated undesirably high subthreshold leakage.

Extracted device characteristics demonstrated this leakage in the form of a two-part subthreshold curve, which indicated the existence of a parasitic edge transistor [2]. The subthreshold leakage is particularly problematic in view of ELEC4609's extensive use of dynamic logic techniques in which information is stored in the form of charge on the gate-channel capacitance of a MOSFET. Leakage in the pass transistor accessing the capacitor can cause

corruption of the stored information. Subthreshold leakage is also undesirable in switched capacitor filter circuits, which are of interest for future ELEC4609 runs.

The leakage was initially believed to have been caused by boron “suck-out” (also referred to as boron segregation) into the growing field oxide [3, pp. 122, 123] in a poorly designed Local Oxidation of Silicon (LOCOS) isolation process. However, the second run in 2015 showed the problem persisted even with an entirely different mesa isolation technique. This led to the understanding of the importance of both geometry and boron suck-out effects in controlling the leakage.

1.2 Thesis Contributions

Several isolation techniques have been proposed to reduce the SOI subthreshold leakage current [2] [4] [5] [6]. Due to the length of the term for ELEC4609 students and processing limitations at Carleton University, isolation techniques involving field-adjust implants cannot be implemented. The work in this thesis aims at designing an isolation process specific to fabrication techniques at Carleton University that will eliminate the subthreshold leakage current. This is a very challenging goal since it has been shown that edge leakage current is difficult to suppress using LOCOS isolation [5].

Development of this SOI CMOS process was completed using 3D-Sentaurus (by Synopsys) simulations. Processing simulations were completed to minimize edge leakage current through optimization of oxidation times and temperatures, LOCOS techniques to maximize bird's beak sharpness, and variation of nitride and pad oxide thickness. References [5] and [7] investigate the use of Poly-Buffered LOCOS (PBL) to minimize edge leakage current by creating a more narrow bird's beak, allowing a smaller number of electrons to become trapped at the isolation edges to create parallel parasitic transistors in the channel. The process presented in this work defines specific PBL processing steps to fabricate SOI nMOS devices from a CMOS process at Carleton University that prove to minimize the edge leakage issues.

Results from past years' fabrication runs were used as baseline results to improve on. LOCOS and mesa isolation techniques have proven to show effects of edge leakage. The work presented in this thesis specifies a fabrication process utilizing the PBL isolation technique to keep fabrication times for ELEC4609 in the 3-week timeframe and uses minimal photolithography and thus mask steps.

1.3 Outline

Chapter 2 provides background on SOI technology and the SOI nMOS edge leakage issue. Processing details affecting the edge leakage are also discussed, with details specific to oxidation, LOCOS and extended LOCOS, nitride and pad oxide thickness in LOCOS, and Poly-Buffered LOCOS explained. A brief overview of the Sentaurus Semiconductor Device Simulator tool is also included in this chapter.

Chapter 3 describes how the Carleton University SOI CMOS process was simulated using Sentaurus Process, beginning with the implementation of the process flow, and finally discussing the optimization of certain processing steps to minimize the edge leakage issue. A trade-off between optimizing different steps is also discussed to conclude in a fabrication process for an optimized SOI nMOS device specific to Carleton University's Microfabrication Laboratory.

Chapter 4 includes a visual summary of the designed fabrication process, and describes the fabrication of the test devices.

Chapter 5 is a summary of the results from testing and analyzing the fabricated SOI nMOS devices.

Chapter 6 presents the conclusions of the fabrication process specified in this thesis, as well as future work and optimization for future runs.

Chapter 2 Background

Silicon-on-insulator (SOI) has become a technology used for ultra-dense, faster integrated circuits with low power dissipation [8, p. 2]. SOI is, however, sometimes subject to issues with nMOSFET (nMOS) leakage due to a parasitic device formed at the edge of the MOSFETs during isolation. This chapter will detail background on SOI technology, nMOS edge leakage in SOI technology, LOCOS isolation techniques, and processing details that affect this leakage. Finally, an overview of the Sentaurus Process Simulator tool used to design a minimized edge leakage process is presented.

2.1 Silicon-on-Insulator (SOI) Technology

MOSFET devices use only the top part of the silicon bulk wafer as the active region, which leads to undesirable and parasitic effects from the inactive silicon region affecting the devices [8, p. 1]. Such an effect from bulk is the increase in the subthreshold swing from the ideal value of 60mV/decade, which deteriorates the ratio between on- and off-currents. SOI technology is designed using special wafers which have a top layer of thin silicon film, isolated from the bulk silicon wafer by a buried oxide (BOX) which combats these undesirable inactive silicon effects. To discuss SOI technology, a comparison between bulk silicon and SOI CMOS is presented. This outlines the advantages and disadvantages of SOI.

2.1.1 SOI CMOS versus Bulk CMOS Technology

SOI technology becomes desirable over bulk silicon for many reasons. Advantages of SOI include but are not limited to the dielectric isolation, simpler fabrication than bulk silicon, minimized short-channel effects, and reliability to name a few [8, pp. 2-4]. Isolation between devices in SOI is simpler than in bulk CMOS, as the devices are fully electrically isolated in the film using gaps

such as in MESA isolation, or oxide in LOCOS. There is no conduction in the insulating BOX layer, and so device isolation in the film fully isolates the devices from the substrate as well. The isolation differences between bulk and SOI CMOS are illustrated in Figure 2-1.

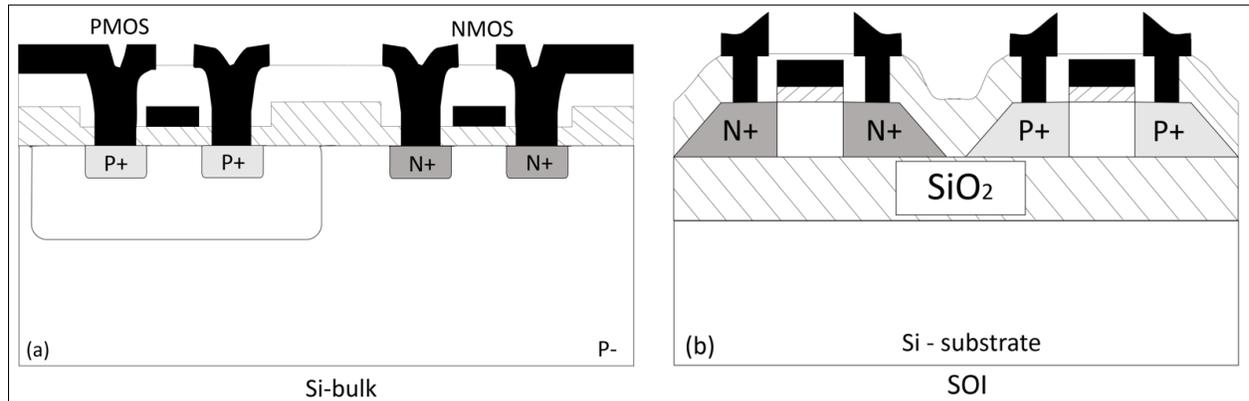


Figure 2-1 – CMOS Isolation in Bulk Silicon versus SOI Technology [8, p. 2]

As charge carriers are completely blocked from flowing between complementary devices, latch-up does not occur in SOI. The source and drain regions in SOI extend down to the insulator. This then significantly reduces parasitic junction capacitances, which will then reduce delays and dynamic power dissipation in devices [8, p. 2].

The absence of wells and inter-device trenches in SOI will reduce the number of processing steps during fabrication. Processing is also simpler as isolation of individual devices is limited only by minimizing packing density and interconnections, not well areas, which makes for denser CMOS circuits. In addition, depletion regions induced by source and drain junctions in bulk silicon impede the gate control over the channel. This causes short-channel effects such as punch-through, drain-induced barrier lowering, degradation of subthreshold swing, threshold voltage roll-off, etc. SOI devices are more immune to short-channel effects as the source/drain depletion regions are restricted in depth to the silicon film thickness and because there is dual-gate control from the front-gate and silicon substrate of the surface potential [8, pp. 3,4]. Also, since the volume

exposed to carrier generation is orders of magnitude smaller than in bulk silicon, SOI has high tolerance to ionizing radiation exposure [8].

Along with all the advantages of SOI, no technology is without its challenges. SOI substrates have uniformity issues, are less readily available than bulk wafers as they must be processed to include a buried oxide and the thin silicon film layer, and can be costly. There are also uncontrollable effects from floating body [8, p. 5] and parasitic nMOS transistors formed at the edge of transistors during isolation. Edge leakage will be discussed in much more detail below. Attention is first turned to floating body effect.

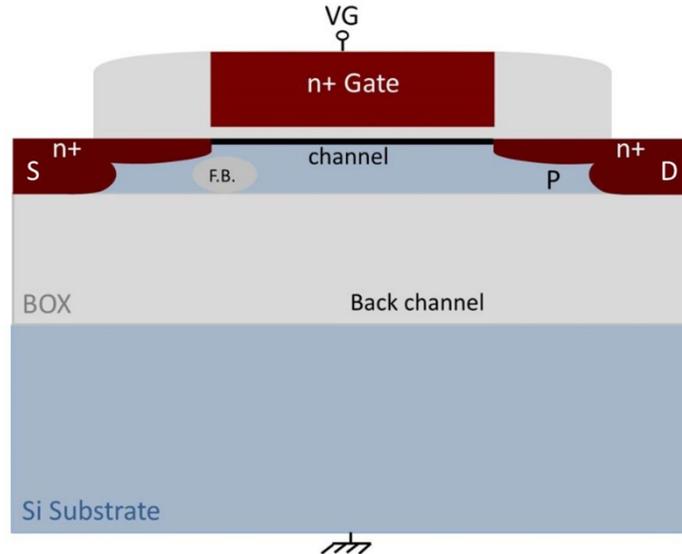


Figure 2-2 – F.B. shows the region where avalanche occurs, leading to the floating body effect in a partially-depleted SOI MOSFET [9]

As shown in Figure 2-2, SOI nMOS devices can have issues with the floating body effect if there is no well or substrate contact. There is a large electric field near the drain when V_{DS} is high compared to V_{GS} and the channel is pinched off (i.e. in saturation), which can cause a weak avalanche producing electrons that enter the drain. Holes are also produced in the avalanche and these are swept into the Si film under the channel and have no place to escape from the film due to the isolating buried oxide layer. This build-up of positive charge under the channel will attract

electrons into the channel effectively lowering the threshold voltage of the device. The floating body effect is worse in nMOS devices as electrons generate new carriers in an avalanche better than holes in a pMOS device, nMOS floating body effects can produce “kinks” in the drain characteristics in both fully- and partially-depleted SOI, described in detail below.

With a higher bias, the self-heating effects of the MOSFET will give a negative resistance in saturation. This compensates for the excess drain current associated with the kink. This is illustrated in Figure 2-3 below, which also illustrates how providing a body contact gives way for excess holes to escape from the film until the drain bias is high and strong substrate currents are reached [10].

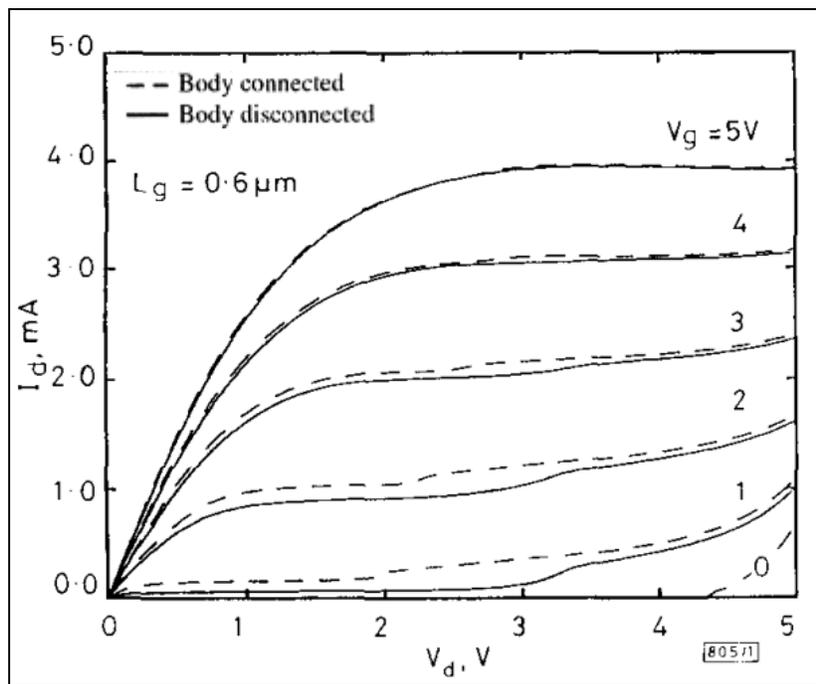


Figure 2-3 – $I_D V_D$ characteristics of an N-channel thin film SIMOX MOSFET; solid line shows body connect, and dashed line shows no body connect [10]

One way around the issue with floating body effect is to use the T-gate device layout. An example of this layout is shown in Figure 2-4. The T-gate provides a drain for the excess holes to the body, as this layout includes a body contact. However, the T-gate layout requires more layout

space, and so this layout is not an ideal solution to eliminate the kink issue in the fully-depleted SOI nMOS devices.

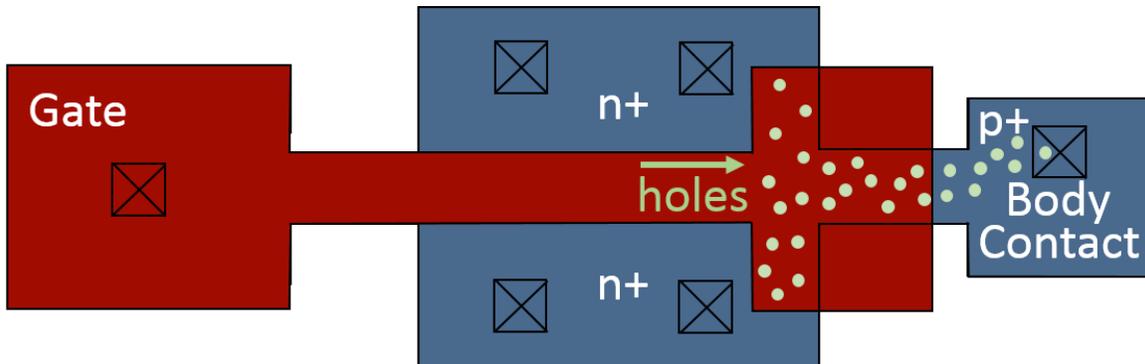


Figure 2-4 – Example of device using T-gate layout

2.2 Partially versus Fully Depleted SOI

SOI CMOS can be designed to have a fully- or partially-depleted channel. SOI MOSFETs have two inversion channels that can be active: a back channel at the Si film-BOX interface and a front channel at the Si film-SiO₂ interface as shown in Figure 2-5 below. A fully-depleted device forms when the depletion region extends through the entire silicon film thickness. There is no possibility of extension of the depletion region with increased gate bias, and this gives a constant depletion charge. The front and back channel surface potentials become interdependent. The resulting excellent coupling between the inversion charge and gate bias offers a device with improved current and subthreshold slope. The channel current depends on both the front and back gate bias [9, p. 4971].

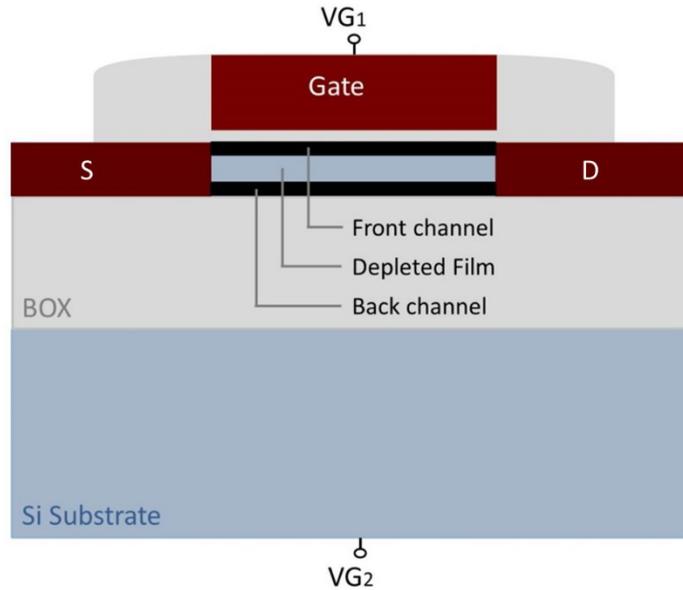


Figure 2-5 – Configuration of a Fully-Depleted n-channel SOI MOSFET [9]

Fully depleted (FD) SOI devices have attracted much attention as low-power and high-performance IC components. The desirable properties of FD SOI devices include suppressed short-channel effects which can allow the use of shorter gates, and a sharp subthreshold slope approaching values as low as 60mV/decade which is ideal in CMOS [11, p. 1872]. However, the threshold voltage of these devices is sensitive to film thickness, which varies across a wafer. This is an uncontrollable consequence of using FD SOI, which can affect circuits that are sensitive to threshold voltage variance [11, p. 1872].

A partially-depleted device forms when the depletion charge does not extend from one interface to the other. In this case, a neutral region remains, which is shown in Figure 2-2. Floating-body effects arise, and the coupling effect between interfaces no longer exists. Majority carriers generated by impact ionization collect in the neutral region, and trigger the kink effect which manifests itself as excess drain current which gives rise to drain current overshoot [9, p. 4971]. As aforementioned, when the depletion region extends (at higher gate bias), self-heating effects of the MOSFET have a negative resistance in saturation which compensates for the excess

drain current associated with the kink [10]. The threshold voltage is lowered by the body potential [9, p. 4971].

2.3 SOI nMOSFET Edge Leakage Issue

SOI CMOS processing has been run three times in the Carleton University Microfabrication Laboratory. The first run was completed in winter of 2014, where a poorly designed LOCOS process was used for device isolation. The field oxidation time and temperature were copied from those used in a traditional bulk nMOS process. They were too long and too high, which resulted in nMOS devices that showed a two-part or “kinked” subthreshold curve. This is shown below in Figure 2-6. A more ideal SOI nMOS subthreshold was produced in Sentaurus and is shown in Figure 2-7, where a device was simulated with the edge etched away. This ensured that no edge effect was present in the subthreshold curve, and thus no kink.

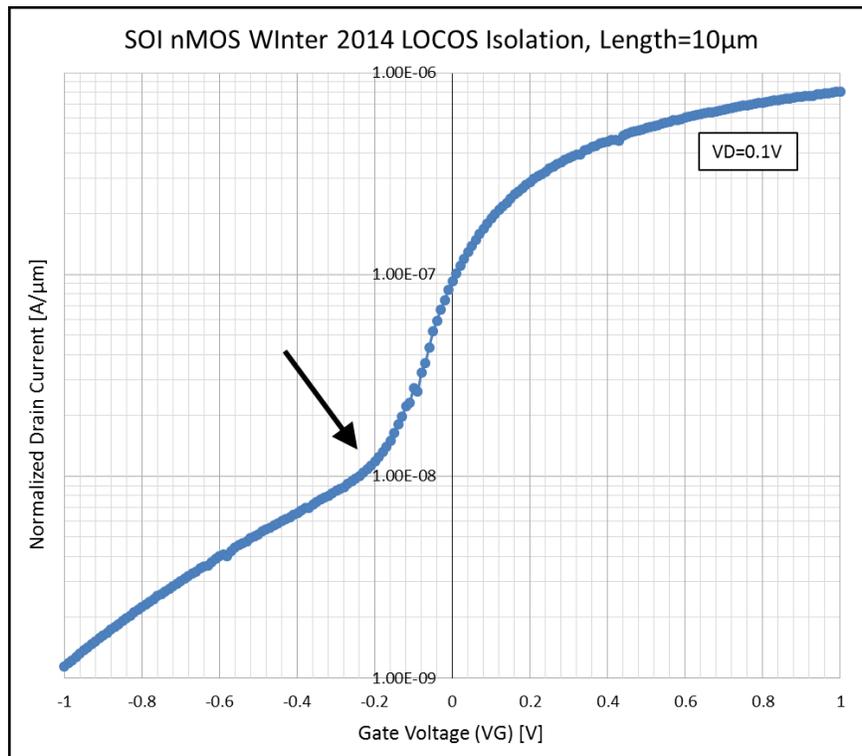


Figure 2-6 – SOI nMOS subthreshold curve showing a kink from Winter 2014 run at Carleton University Microfabrication Laboratory, the kink is indicated by an arrow

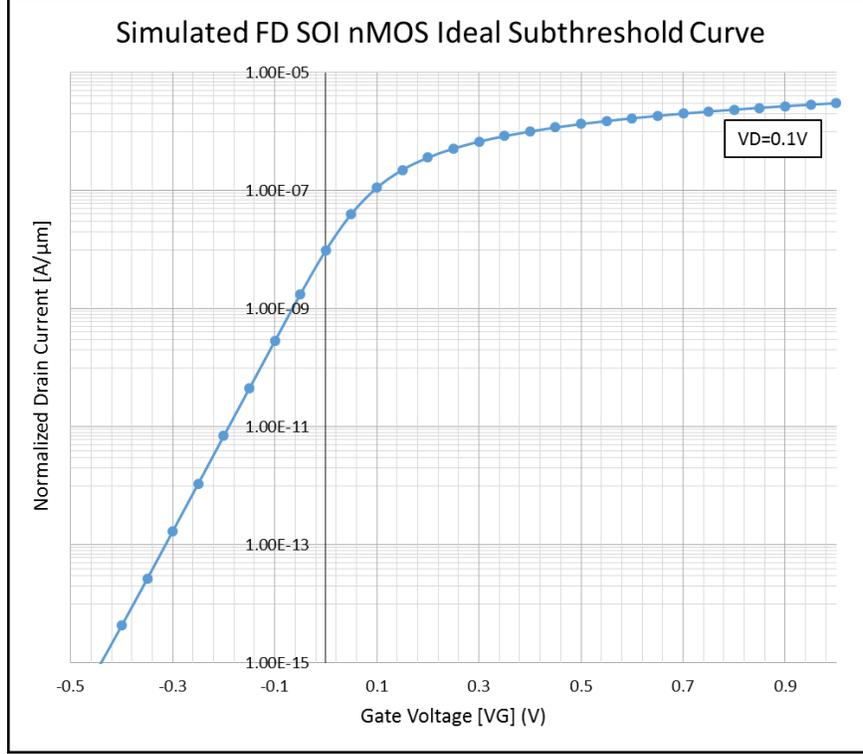


Figure 2-7 – A more ideal SOI nMOS Subthreshold Curve Output from Sentaurus Simulations of Device with No Bird’s Beak (no kink)

During oxidation, heat applied to the wafer will cause the boron in the silicon film to diffuse. Boron will also segregate into the growing oxide [12]. At the edges of the device, the boron will diffuse into the oxide, leaving a lower concentration in the film at these edges. The full equation for SOI nMOS threshold voltage is shown in Equation 2-1 [13], which accounts for effects from the substrate.

Equation 2-1

$$V_{Tn} = V_{FB} + \phi_G - \phi_{si}$$

$$V_{Tn} = V_{FB} + \frac{-\phi_{si} \left(1 + \frac{C_{Si}}{C_{ox1}} + \frac{C_{Si}}{C_{ox2}}\right) - \phi_{s3} \frac{C_{Si}}{C_{ox1}} + \frac{qN_{Si}t_{si}^2}{2\epsilon_{Si}} \frac{C_{Si}}{C_{ox1}} \left(1 + 2 \frac{C_{Si}}{C_{ox2}}\right)}{1 + \frac{C_{Si}}{C_{ox2}}} - \phi_{si}$$

Where,

$$C_{ox1} \equiv \frac{\epsilon_{ox}}{t_{ox1}}, \quad C_{ox2} \equiv \frac{\epsilon_{ox}}{t_{ox2}}, \quad C_{Si} \equiv \frac{\epsilon_{si}}{t_{si}}$$

and,

$$\phi_{s3} = \phi_{sub} + \frac{\epsilon_{si}}{2qN_{sub}} E_0^2$$

$$E_o = -\frac{qN_{sub}t_{Si}}{\epsilon_{Si}}\left(1 + \frac{C_{Si}}{C_{ox2}}\right) + \sqrt{\left[\frac{qN_{sub}t_{Si}}{\epsilon_{Si}}\left(1 + \frac{C_{Si}}{C_{ox2}}\right)\right]^2 - \frac{2qN_{sub}}{\epsilon_{Si}}(\phi_{si} + \phi_{sub}) - \left(\frac{qt_{Si}}{\epsilon_{Si}}\right)^2 N_{Si}N_{sub}}$$

And, for a p-type substrate (as used for this thesis):

$$\phi_{sub} = \frac{kT}{q} \ln\left(\frac{n_i}{N_{sub}}\right)$$

However, it can often be assumed that the buried oxide is thick compared to the silicon film, in which case the substrate does not influence the threshold. Using this assumption, Equation 2-1 is simplified to the form in Equation 2-2 [14, 15]. By observing the equation for nMOS threshold voltage, it can be shown that as the doping concentration, N_A decreases at the edges then the threshold voltage will also decrease.

$$\text{Equation 2-2} \quad V_{Tn} = V_{FB} + 2\phi_B + \Delta V_T = V_{FB} + 2\phi_B + \frac{qN_A t_{Si}}{C_{ox}} = V_{FB} + 2\phi_B + \frac{qN_A t_{Si}}{\epsilon_{ox}} t_{ox}$$

When the boron segregates into the oxide at the edge of the film, parasitic transistors are formed in parallel with the main channel as shown in Figure 2-8. The loss of boron makes the threshold voltage of the edge transistors less than that of the main (center of the channel) transistor. The edge transistor will therefore turn on before the main device, which results in the observed kink in the subthreshold curve. The kink occurs at a lower gate voltage before the turn on of the main channel, showing that this transistor turns on with a lower applied gate voltage.

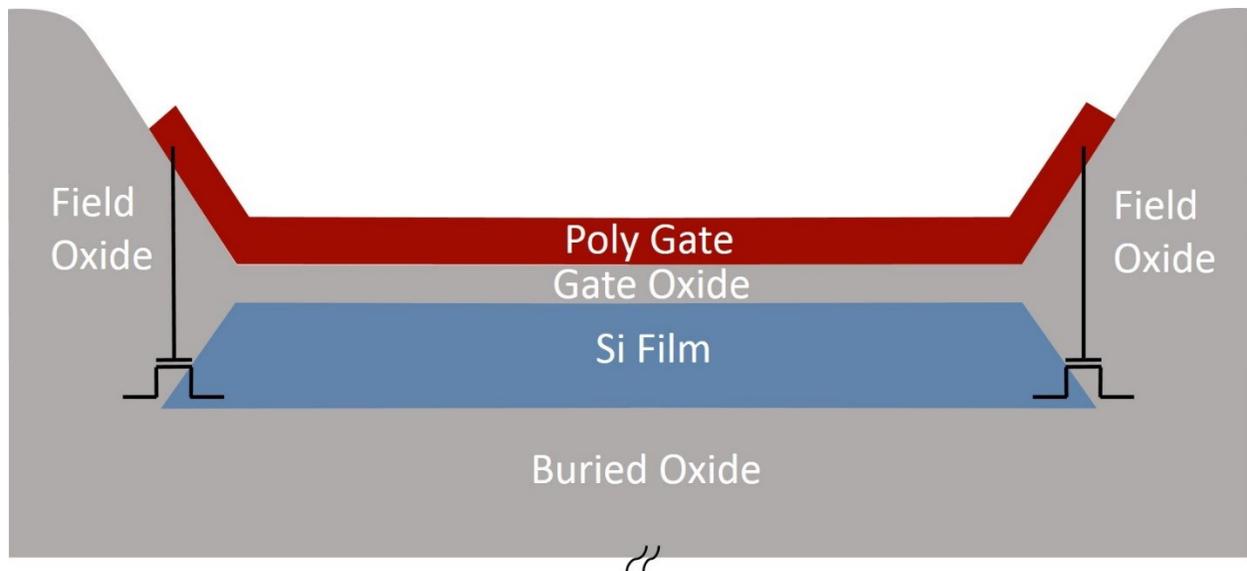


Figure 2-8 – Illustration of location of the parasitic edge transistors formed in the FD SOI nMOS device

In an attempt to avoid boron suck-out into the field oxide, mesa isolation was implemented for the SOI ELEC4609 run in winter 2015. However, subthreshold curves of the SOI nMOS devices continued to show a kink as seen in Figure 2-9. This result was unexpected as there can be no boron loss in the low-temperature mesa process. The results revealed that subthreshold kink may also arise from purely geometrical effects.

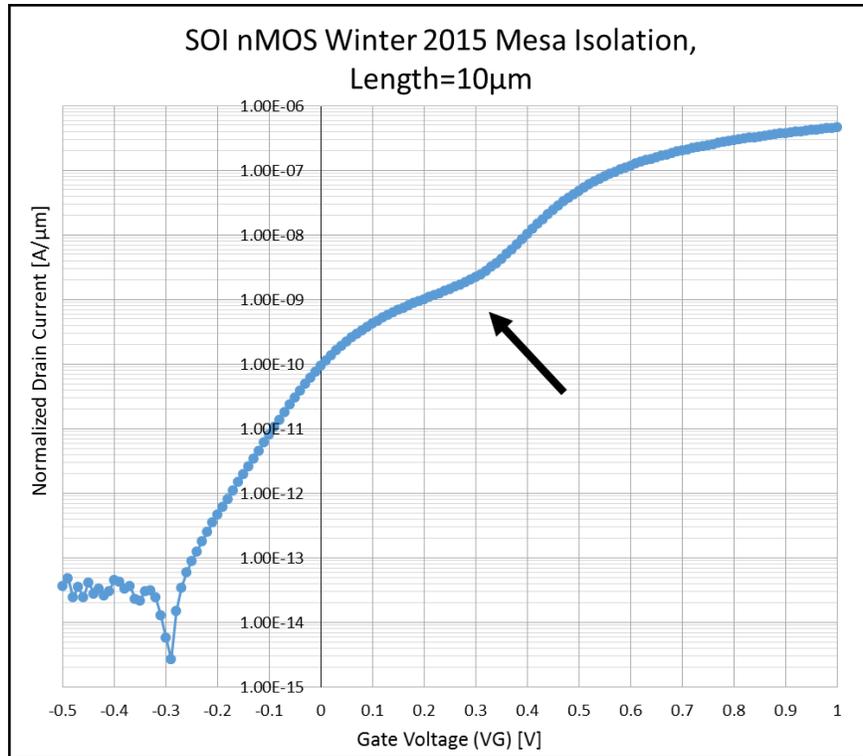


Figure 2-9 – SOI nMOS subthreshold kink from mesa isolated 2015 ELEC4609 run, kink indicated by the arrow

As the mesa isolated run was completed in the Carleton University Microfabrication Laboratory with available equipment, a wet etch was used for isolation which results in a sloped sidewall as illustrated in Figure 2-10. By observing the equation for the threshold voltage shown in Equation 2-2, as t_{si} is reduced on the mesa edge, the threshold voltage will decrease.

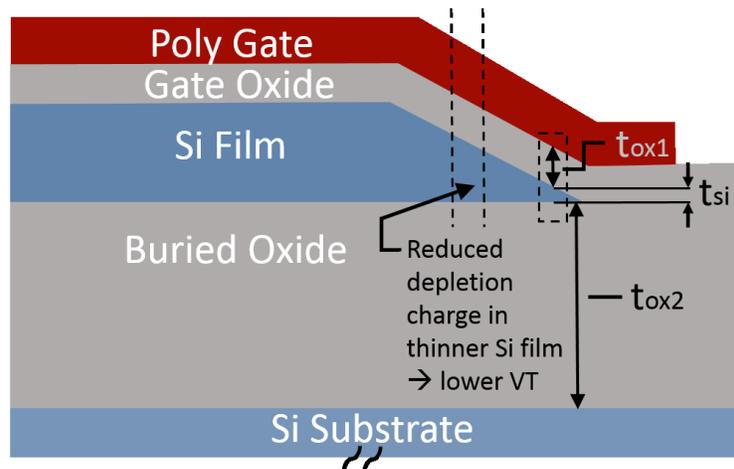


Figure 2-10 – Gate wraparound when using mesa isolation without filling and polishing the isolation spaces created between devices

It is of interest to consider whether subthreshold leakage can arise from geometrical effects in LOCOS isolation. Figure 2-11 shows a cross-section through the channel edge in a LOCOS-isolated device. To a very good approximation, the oxide edge slopes up at the same angle the silicon film edge slopes up.

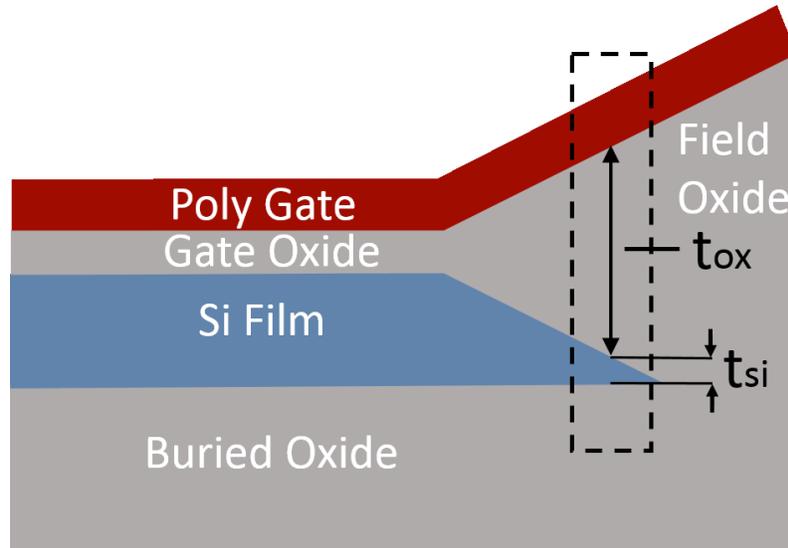


Figure 2-11 – Geometrical effects at the edge of the device in SOI

As a result, moving to the right at the channel edge in Figure 2-11 t_{ox} increases as t_{si} decreases. Using the simple 1-dimensional equation for the threshold shift ΔV_T resulting from doping in the Si film as shown in Equation 2-2, to a crude first approximation, one would therefore expect ΔV_T to remain roughly constant across the channel edge. This suggests that boron segregation is likely to be much more significant than geometrical effects in controlling edge leakage in LOCOS-isolated devices.

Geometry also suggests that it is advantageous to minimize the width of the bird's beak region. With a narrow bird's beak, the total volume of channel edge able to contribute to subthreshold leakage is reduced, as suggested in Figure 2-12.

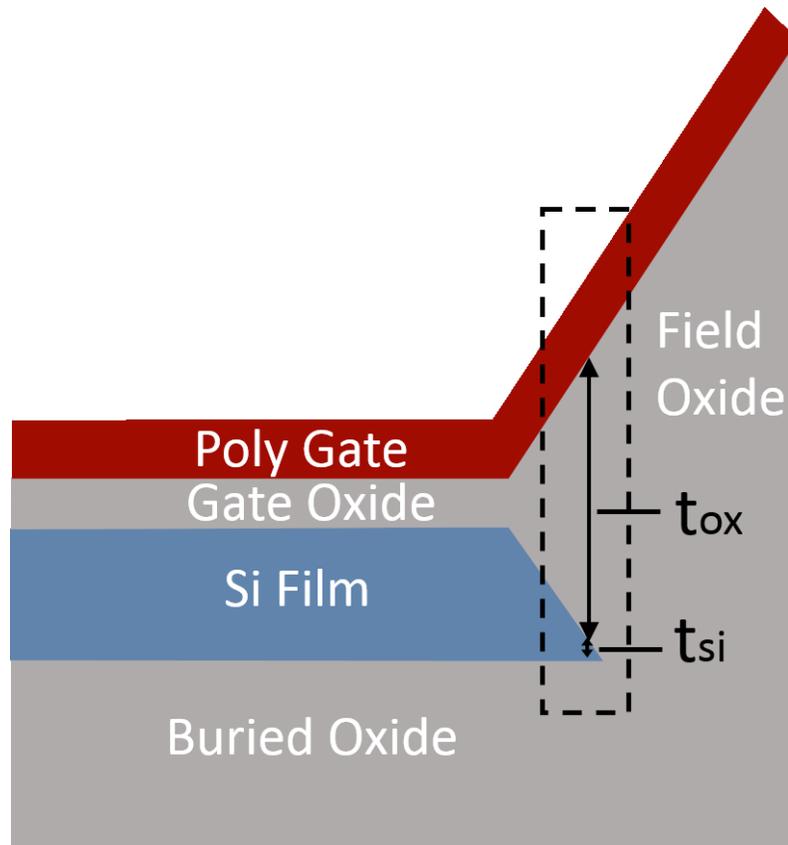


Figure 2-12 – Geometrical effects at the edge of the device in SOI with a sharper bird's beak

2.3.1 Literature Reports of SOI nMOSFET Edge Leakage

Through literature research, it has been found that this two-part subthreshold curve and kink has been a known issue in FD SOI nMOS devices. When LOCOS is used for isolation in FD SOI, a thin silicon tip at the edge of the active channel is formed (bird's beak). This will result in a reduced sidewall threshold voltage, which is referred to as the threshold voltage of the formed parasitic transistor at the edges of the FD SOI nMOS. This appears in the form of a kink in the subthreshold curve [16].

During oxidation, the boron that is introduced during doping diffuses toward, and segregates into the field oxide [16]. The segregation of boron into the field oxide is also referred to as boron suck-out. Typical FD SOI nMOS fabrication uses a massive boron field threshold

adjust implant dose (in the order of 10^{15} cm^{-2}) to maintain an adequate boron doping density at the edge of the active area (in the order of 10^{19} cm^{-3}). This dose has been shown to leave enough boron in the film after field oxidation, which is effective in suppressing the parasitic edge transistor from turning on as illustrated in Figure 2-13 [16].

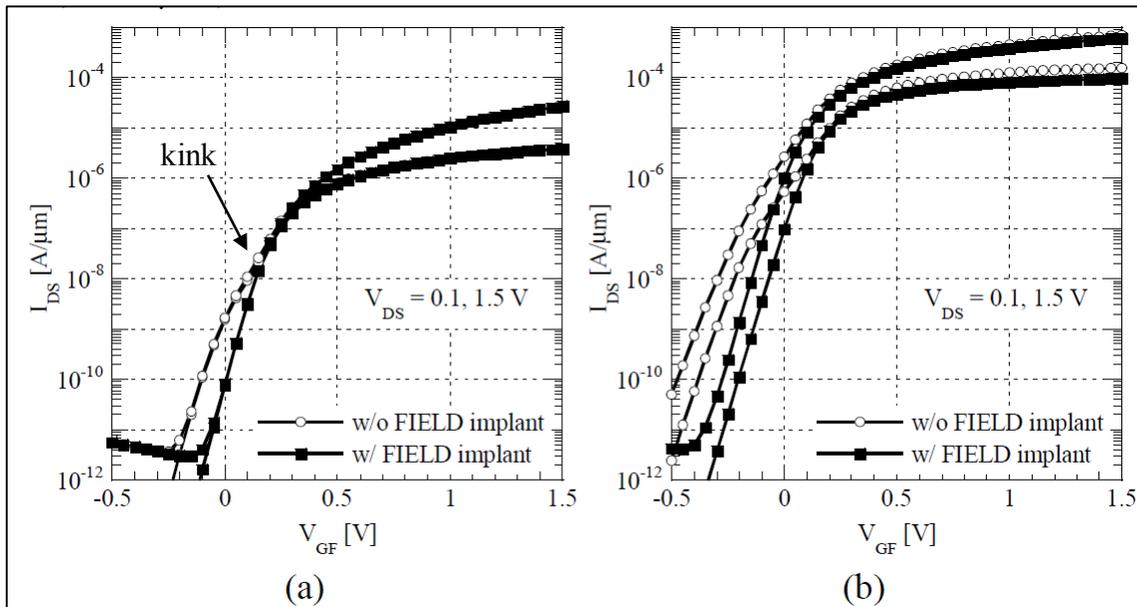


Figure 2-13 – Subthreshold characteristics of a (a) long $10\mu\text{m}$ and short $0.18\mu\text{m}$ FD SOI nMOS transistors with and without a boron field implant [16]

Unfortunately, due to the tight time constraints on the ELEC409 process, use of a field adjust implant is not a viable option. Each implant step currently requires that the wafer batch be shipped to a vendor in Los Angeles. This may incur a time delay of as much as one week.

One other solution that has been presented as a way around the lost boron concentration at the edges of the silicon film during isolation is recessed LOCOS. This technique aims at reducing the sidewall threshold voltage also found as a kink in the subthreshold FD SOI nMOS characteristics. This process also utilizes a boron implantation around the n-channel transistors to help in the boron loss found at the tips of the film (bird's beak) leading to edge leakage currents. This has resulted in much less boron segregation as the oxidation time for field oxide was reduced, a more rounded bird's beak, and an increased threshold voltage of the edge transistors which

eliminated the kink [17]. As this would introduce another implant step, recessed LOCOS was not simple enough for the process designed in this thesis that attempts to isolate using a technique very close to conventional LOCOS for simplicity.

As the mesa isolation did not solve the SOI nMOS edge leakage issue, this thesis seeks other ways to fabricate SOI nMOS devices with minimal or no parasitic transistor effects. As the most common isolation technique used in past ELEC4609 runs was conventional LOCOS, the process designed in this thesis was based around using LOCOS. Literature research suggests that standard LOCOS will always form a parasitic edge transistor in SOI nMOS devices, and so alternative LOCOS techniques were investigated [18] [19].

2.4 LOCOS

LOCAl Oxidation of Silicon (LOCOS) is a technique used to electrically isolate integrated devices from one another with oxide. This process was developed to provide semi-recessed oxide isolation with a relatively planar surface compared to simply etching windows in a uniform field oxide. The oxide is grown locally in areas of the silicon defined by photolithography where no active channels are formed in the field between devices. This allows for nMOS and pMOS devices to be fabricated on the same chip, leading to CMOS circuits where devices are connected through isolated paths [19, pp. 13, 17]. An example of conventional LOCOS is shown in Figure 2-14.

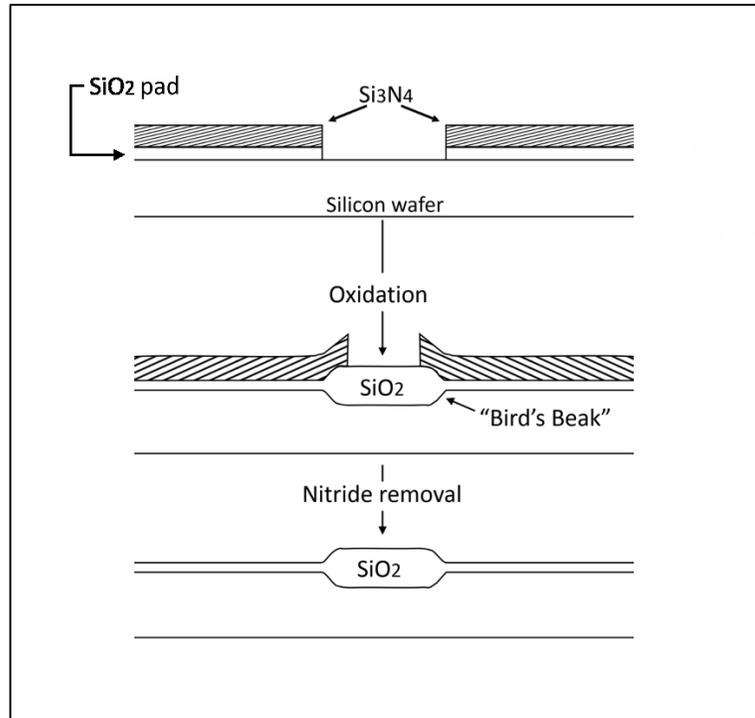


Figure 2-14 – Semi-recessed LOCOS isolation process [19]

The LOCOS process starts with a pad oxide layer that is thermally grown on the surface of the wafer. Silicon nitride is then deposited by LPCVD (low pressure chemical vapour deposition), which functions as an oxidation mask. The active regions are then defined with a photolithographic step, where the applied photoresist is hardened over the areas where active devices will be formed. The nitride layer is dry etched, and the pad oxide can be etched using either a wet or dry chemical process. A channel-stop implant can be performed after this step, but can tend to require high doses of boron (mid 10^{12} - 10^{13} atoms/cm²) for acceptable field threshold voltages that can lead to issues with boron suck-out and oxidation-enhanced diffusion [19, pp. 21-21].

Typically after the nitride and pad oxide layers are etched in the non-active regions, the field oxide is grown locally where field oxide is needed for device isolation. The field oxide is grown using wet oxidation at temperatures around 1000°C for around 2-4 hours for thicknesses of 0.3-1.0µm (necessary for bulk silicon CMOS). It is at this stage that some oxide can diffuse laterally

under the nitride and form a bird's beak by lifting the edges of nitride. This is illustrated in Figure 2-15 below [19, pp. 22-24].

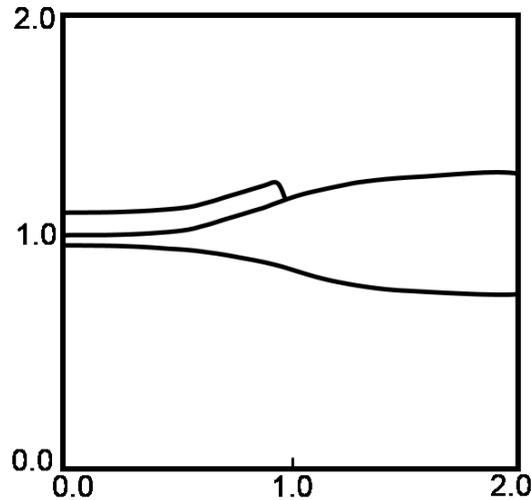


Figure 2-15 – Illustration of bird's beak that forms during semi-recessed LOCOS [19]

The field oxide that diffuses laterally under the nitride forming the bird's beak is illustrated further in Figure 2-16 below. This figure shows that the length of the nitride that lifts is about half the thickness of the grown field oxide. The grown field oxide is semi-recessed into the silicon as shown.

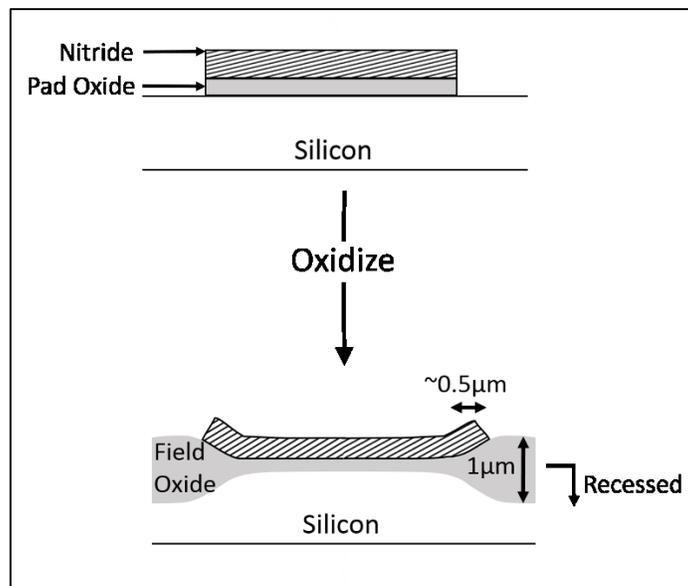


Figure 2-16 –Illustration of semi-recessed LOCOS and bird's beak after field oxidation [19]

The area of silicon under the lifted nitride is affected by the bird's beak effect. Devices are designed to have a certain width, and the bird's beak effect will decrease the width to an effective width of the device. The bird's beak encroaches from all edges of the active device channel as the field oxide surrounds a device. As the widths of devices started to become smaller in design, the bird's beak effect started to have a large impact on the ability to use LOCOS for isolation.

The encroachment could decrease the effective width enough that eventually no current could flow in the device, as shown in Figure 2-17 where there is no longer an effective channel. Equation 2-3 shows the equation for drain current, which shows the decrease of current flow with a decrease in effective width. In an attempt to continue to use LOCOS for isolation as device widths became smaller, modified LOCOS (or extended LOCOS) techniques were developed and are explained in Section 2.4.2. A cross-section example of field oxide encroachment creating the bird's beak effect is shown in Figure 2-18.

Equation 2-3
$$I_D = \frac{W_{eff}}{L} \mu_n C_{ox} \frac{(V_{GS} - V_T)^2}{2} (1 + \lambda V_{DS})$$

As shown in Equation 2-3, the drain current in a MOSFET (here an nMOS device) is affected by many of the device characteristics. Defining the variables in Equation 2-3: I_D is the drain current of the device, W_{eff} is the actual width (not drawn – or set by the mask) of the device after fabrication, L is the length of the device, μ_n is the bulk electron mobility (1350 cm²/V-s), V_{GS} is the gate to source applied voltage, V_T is the threshold voltage of the device, and V_{DS} is the drain to source voltage. C_{ox} is the capacitance per unit gate area of the oxide layer, which is defined as the dielectric/permittivity of the silicon dioxide divided by the thickness of the oxide:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9\epsilon_o}{t_{ox}} = \frac{(3.9)(8.85 \times 10^{-12})}{t_{ox}} = \frac{3.45 \times 10^{-11} F/m}{t_{ox}}$$

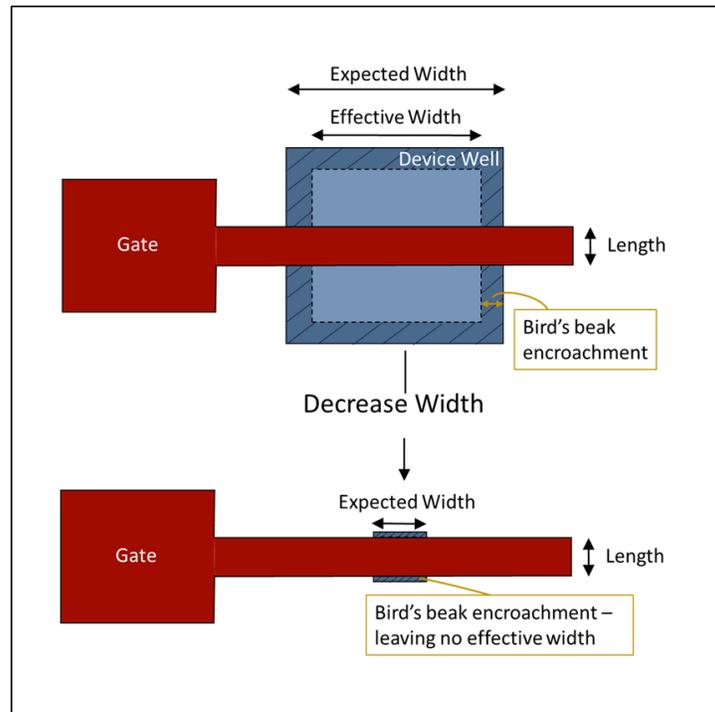


Figure 2-17 – Bird's beak encroachment limiting the effective active channel width

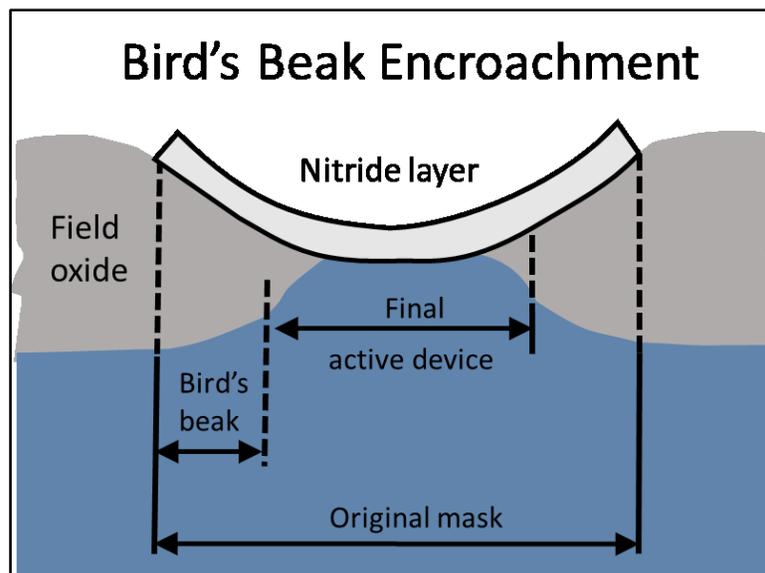


Figure 2-18 – Bird's beak encroachment [19]

2.4.1 Pad Oxide and Nitride Use in LOCOS

Intrinsic stress exists at the Si/SiO₂ interface during field oxidation, which actively influences the process of LOCOS [19]. The stack used in LOCOS for isolation is made of pad oxide and nitride (Si₃N₄). Two different stresses occur in the stack used for LOCOS; compressive stress in the pad

oxide due to expansion during oxidation, and tensile stress in the nitride due to thermal expansion. After oxidation, these unnecessary stresses occur during wafer cooling back to room temperature. If these stresses are high enough, dislocations causing degraded device performance can occur in the crystalline structure of the silicon [20, p. 736].

There is a stress that occurs between the silicon and deposited nitride layer. The function of the pad oxide is to cushion this transition. Generally, less edge force transmits to the silicon from the nitride with a thicker pad oxide. However, if the pad oxide is too thick, the nitride layer's use as an oxidation mask is rendered useless. Lateral oxidation will occur in this case. Thus, it is ideal to only use a minimum pad-oxide thickness that will ensure dislocations are not formed. The optimized thermally-grown pad oxide layer thickness to nitride layer ratio is about one third [19, p. 21].

The nitride layer is deposited on top of the pad oxide, as shown in Figure 2-19. As water vapor and oxygen will only diffuse slowly through silicon nitride, it works well as an oxidation mask to prevent lateral oxidation from the pad oxide. Nitride oxidizes very slowly during the growth of field oxide, where only about a few tens of nanometers of nitride are converted to SiO_2 . Comparatively, silicon oxidizes approximately twenty-five times faster than silicon nitride. These properties of silicon nitride made it perfect for its role in the LOCOS stack. One rule to follow when selecting a nitride thickness is to ensure that it is greater than the thickness that will be converted to SiO_2 during the field oxidation step [19, pp. 21,22].

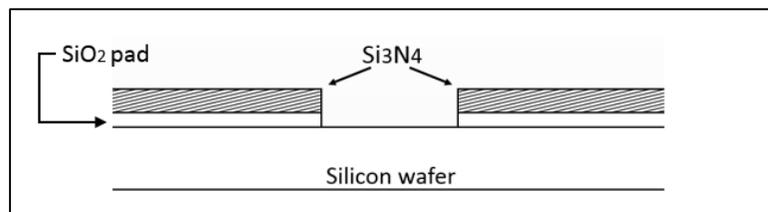


Figure 2-19 – Cross section depicting pad oxide and nitride stack for LOCOS [19]

One drawback of silicon-nitride films is the surface stress due to CVD deposition on silicon (10^7 N/m). A horizontal force acts on the silicon when the stress intrinsic to the nitride film is eliminated. Dislocations causing fabrication defects can arise from this when the stress is larger than the critical stress of silicon. This stress can be alleviated by the viscous flow of the pad oxide [19, p. 22].

The process designed in this thesis utilizes a pad oxide to nitride thickness ratio of $20\text{nm}/160\text{nm}=0.125$. This breaks the optimized ratio, but is effective due to the buffer polysilicon layer. This technique allows for a thinner pad oxide, using the experimental evidence that a thinner pad oxide results in a steeper bird's beak. In doing this, the pad oxide layer is thinned and a poly buffer layer is added on top of the oxide, and beneath a then thicker nitride. This continues to relieve stress from the silicon while decreasing the field oxide encroachment on the active silicon region [19, p. 32]. A cross-section example of field oxide encroachment creating the bird's beak effect is shown in Figure 2-18.

2.4.2 Extended LOCOS

As explained in Section 2.4, issues using conventional LOCOS isolation arose as device geometries reached submicron size. Conventional LOCOS isolation resulted in a bird's beak encroachment that would eliminate the effective width, which created devices with no current flow as shown in Figure 2-17 [19, pp. 13,27,28]. In an attempt to continue to use LOCOS for isolation as device geometries shrunk, extended LOCOS (also referred to as modified LOCOS) techniques were developed to reduce the bird's beak encroachment.

The fully recessed oxide LOCOS process uses a mask to etch down partway into the silicon substrate where the field oxide will be grown. This reduces the bird's beak effect because about

45% of the field oxide growth is downward, and 55% of the growth is upward. This etch helps shape the area where the bird's beak would form as it is etched linearly, as shown in Figure 2-20. However, using this technique causes a bird's head effect in the oxide surround the nitride pads, leading to uneven surface topology [19, pp. 29,30]. In SOI, this technique allows for a shorter field oxidation time as part of the thin film is etched away and so less silicon must be oxidized for isolation. The field oxide then grows downward as far as the buried oxide and then will grow upward filling the small gap from the etch quickly (as it only needs to isolate for a thin film).

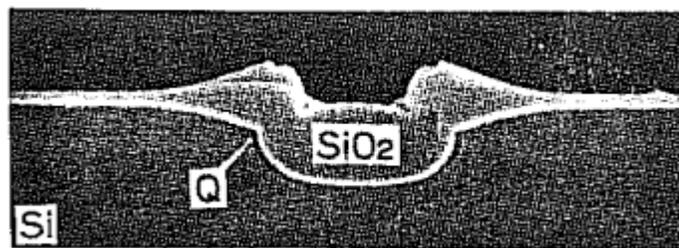


Figure 2-20 – SEM micrograph showing the bird's head (Q) and beak [19, p. 29]

Hewlett-Packard developed a bird's-beak-free isolation technique called Sidewall-masked isolation (SWAMI) in 1982. Limited lateral encroachment allowed for denser circuit design, and allowed for fewer restrictions on field-oxide thickness. This technique also eliminated the Kooi effect (gate-oxide-thinning phenomenon) and improved surface planarity. SWAMI uses the same stack as conventional LOCOS, but then grooves are etched in the silicon to half the designed field-oxide thickness producing recesses of about 60°. The sloped sidewalls reduce stresses contributing to edge effects during field oxidation [19, pp. 39,40].

The Sealed-Interface Local Oxidation (SILO) isolation process reduces the bird's beak length to around 0.2µm by first forming a layer of silicon nitride directly on the surface of the silicon before the deposition of the pad oxide layer [19, p. 33]. The interface of silicon and nitride is sealed, and so lateral diffusion of oxide is prevented, resulting in the short bird's beak. However, if the silicon is not etched, the semi-recessed field oxide will create uneven (step-like) features on

the surface of the wafer. The results from SILO versus conventional LOCOS are shown in Figure 2-21.

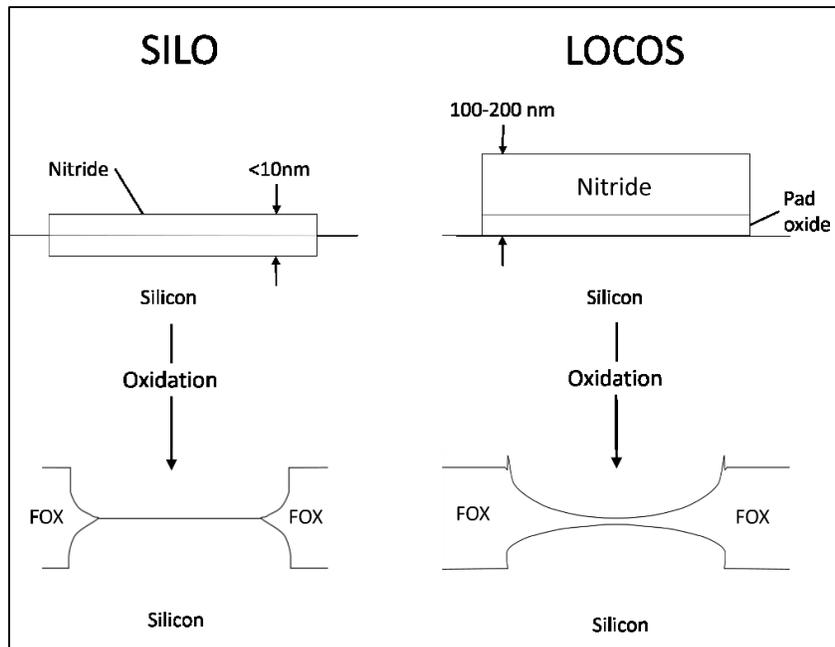


Figure 2-21 – SILO and LOCOS structures before and after field oxidation [19]

A second oxide layer for stress relief is grown, and a second nitride deposition is completed providing conformal coverage of the surface and sidewalls from the silicon recess, and then a CVD oxide is deposited. This structure appears like a silicon mesa where the sidewalls are surrounded by the secondary nitride and oxide. Once the field oxide is grown, the sidewall nitride bends upward from the converted oxide which minimizes the bird's beak effect. However, due to the complexity of SWAMI it is not commonly used, and the depth of the silicon recesses vary depending on position on the wafer which are known issues.

Self-aligned Planar-Oxidation Technology (SPOT) is a semi-recessed LOCOS technique grown under high-pressure oxidation. After the field oxide is grown, it is removed and a second pad oxide is grown on the exposed recessed silicon. A CVD nitride then coats all surfaces. These layers are then etched anisotropically, leaving these layers under the overhanging nitride film, and a second field oxide is grown under high pressure. Fully recessed-oxide (FUROX) isolation is

similar to SPOT, but nitridized oxide is used instead of a pad oxide to seal the silicon surface. This leads to less oxide encroachment into the active device regions [19, pp. 41,42].

For this thesis, a LOCOS isolation technique was to be used that would allow for a quick device turnaround. Poly-buffered LOCOS (PBL) is discussed in Section 2.4.3, where a poly buffer layer is added in between the oxide and nitride in the LOCOS stack. PBL was chosen for this thesis due to the experimental results showing a smaller bird's beak while keeping to a simple process close to conventional LOCOS. This allowed the a simple process for fabrication of the SOI devices in the Carleton University Microfabrication Laboratory that was close to techniques of LOCOS isolation previously completed in the lab. Thus, a simple isolation technique that would give a better bird's beak than conventional LOCOS with minimal thermal budget was ideal.

2.4.3 Poly-Buffered LOCOS (PBL) Compared to Conventional LOCOS

Poly-buffered LOCOS (PBL) is an electrical isolation technique developed as an advanced isolation alternative to conventional LOCOS. PBL is implemented to maintain field thresholds while minimizing field oxide encroachment during field oxidation [7, p. 3815] [19, p. 32]. In SOI technology, conventional LOCOS has also been known to result in a high subthreshold leakage current along the interface of the field oxide/Si film interface in nMOS devices. This leakage occurs from a parasitic edge transistor formed in SOI nMOS devices, and has been shown to be very sensitive to the silicon film thickness. PBL has been proved to also minimize this subthreshold leakage [18, p. 248].

The encroachment and bird's beak effect is minimized using an oxide/poly/nitride stack during LOCOS to protect the active region from field oxidation. Conventional LOCOS uses only an oxide/nitride stack. The poly used in this stack allows for a thinner pad oxide and thicker nitride to be implemented during LOCOS without adding stress to the active regions. Using PBL over

conventional LOCOS reduces the encroachment of oxide into the active silicon from $0.5\mu\text{m}/\text{side}$ to approximately $0.1\mu\text{m}/\text{side}$ [7, p. 3815].

When using LOCOS to isolate devices, the nitride layer acts as a barrier to the field oxide, which in turn protects the active region during field oxidation. In PBL, the added poly layer absorbs stress from the nitride. This is what allows the nitride to be thickened and the oxide thinned in PBL while minimizing the field oxide encroachment. The encroachment, or bird's beak difference when using PBL versus conventional LOCOS is illustrated in Figure 2-22 below. PBL was proven to not introduce degradation in the active region or field interface through tests conducted by Guildi *et. al* in [7].

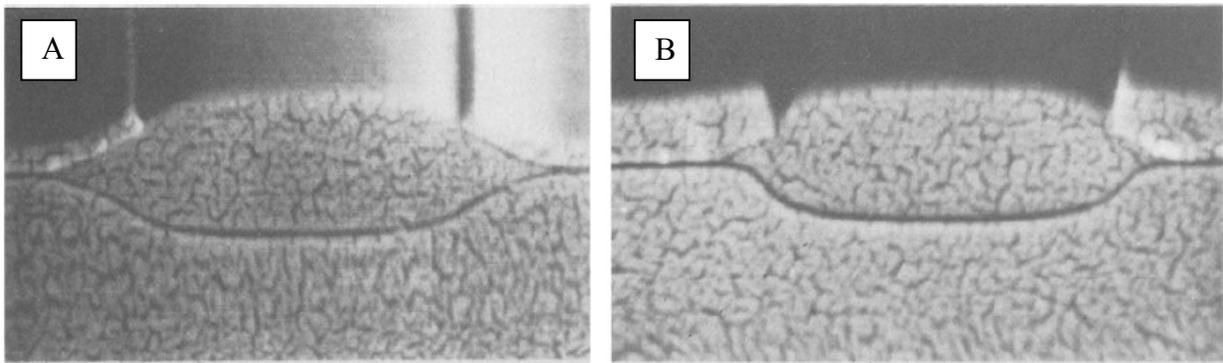


Figure 2-22 – Active region encroachment for (A) conventional LOCOS and (B) poly-buffered LOCOS [21, p. 1993]

PBL has also been proven to minimize the SOI nMOS edge leakage. This edge leakage is discussed in detail in Section 2.3. PBL minimizes this edge leakage as it maximizes the active/field edge slope, which results in decreasing the issue of the silicon region becoming gradually thinner from the bird's beak encroachment. The thinner silicon along the edge can cause a lower threshold voltage, and PBL minimizes this issue [18, p. 248]. PBL also requires a lower thermal budget than conventional LOCOS which helps minimize boron suck-out. The pad oxide can be grown at low

temperatures and for a shorter period of time compared to conventional LOCOS, as the pad oxide for PBL is much thinner than for conventional LOCOS [21].

Founded on the results presented in [7] and [21], PBL was implemented in the process designed for this thesis. Minimizing the thermal budget and thus minimizing the boron suck-out is a key objective. Also, minimizing the bird's beak encroachment is an additional objective as the number of electrons that are able to become trapped in this beak at the edge of the device was also minimized.

The primary issue for SOI nMOS devices is edge leakage, which occurs when the parasitic transistor formed at the edge becomes active before the main channel. In minimizing the boron suck-out creating this parasitic device and electron concentration at the edge, the leakage current through this parasitic edge transistor is minimized which improves the overall SOI nMOS performance and edge leakage. PBL is also ideal for this thesis, as it is simple to implement and does not introduce additional masking layers for photolithography and can be completed with minimal changes to the conventional LOCOS process typically used for ELEC4609 annual runs.

2.5 Discussion of Sentaurus Process Simulator

Sentaurus is a suite of TCAD tools which simulates semiconductor devices from the processing stage to operation and reliability [22, p. 1]. Physical models are used by the Sentaurus simulators to represent the wafer fabrication steps and device operation, which allows the exploration and optimization of semiconductors. As Sentaurus is a very large suite comprising of many different types of simulation tools, this overview will give a general overview of the suite tools used for this thesis. Sentaurus Technology Computer-Aided-Design Tools (TCAD) support both silicon and compound semiconductor technologies, which cover a broad range of semiconductor applications. 2D and 3D device models are created geometrically from rectangles, spheres, polygons, cuboids,

and cylinders, where meshing can be controlled by the user to look for small changes in specific areas of the device [22]. Monte Carlo simulations can be used for very-small transistor analysis.

2.5.1 History of Semiconductor Simulation

Semiconductor process and device simulation is important for the accurate prediction of fabricated device geometries and characteristics [23, pp. 24-1]. This allows designers to cheaply optimize and model devices without needing to do split or multiple fabrication runs. The first process simulators were developed by Stanford University, called Stanford University Process Modeling (SUPREM) which was a 1D simulator. Adding improved models lead to the development of SUPREM II and III, where SUPREM III was commercialized by Technology Modeling Associates Inc. (TMA) in 1979. Later, SUPREM was commercialized by Silvaco and was renamed to ATHENA for 2D process simulation. Silvaco also developed ATLAS for 2D device simulation [23, pp. 24-2].

TMA continued to develop SUPREM, calling the 2D version TSUPREM4. Around 1992, TMA developed a 3D process and device simulator which was not released until after TMA was acquired by Avanti. This simulator was released in 1988 as Taurus. Synopsys acquired Avanti in 2002, and Integrated Systems Engineering (ISE) in 2004. ISE developed a 1D process simulator in 1992 called TESIM, and a 2D process simulator called DIOS. ISE commercialized Florida Object Oriented Process Simulator (FLOOPS) in 2002 [23, pp. 24-2].

Synopsys announced that it would be releasing a new process simulator in 2005. This simulator combined the best features of Taurus and TSUPREM4 into the FLOOPS platform and released it as Sentaurus. Numerous other simulators have also been developed for university and/or commercial use such as ALAMONDE, DADOS, DOPDEES, ICECREM, MicroTec, PROMIS, PROSIM, PREDICT, and TITAN [23, pp. 24-2].

2.5.2 Sentaurus versus Comparable Software

Sentaurus is a complex piece of software used for semiconductor process and device design. This simulator contains a suite of tools that has evolved from the combination of Taurus, TSUPREM4, and FLOOPS by Synopsys. This software is used in industry, and is updated regularly to include new physical models and uses, such as a recent update that includes optoelectronic analysis. Once the user is past the learning curve of such a complex suite of tools, Sentaurus becomes a useful simulator for many different physical and device simulations. When multiple tools of the suite are used in conjunction, a device can be created from processing steps, electrically tested, and have the electrical characteristics extracted to have a full understanding of the device.

Before electrical characterization, a device can be defined by the user with different materials specified in separate regions. This allows for different device geometries to be designed and simulated in Sentaurus. Simulations can be completed in 2D or 3D, which allows for viewing the device at different perspectives where ‘slices’ at any axis can be made to look inside the device. Meshing is also controllable throughout different stages of the device creation. For example, meshing can be set to be coarse in areas of little electrical change (such as in the substrate for SOI), and fine in areas of constant small changes that affect the performance of the device (such as in the bird’s beak for viewing electron concentration).

Complex or simple analyses can also be completed depending on user settings, such as initiating Advanced Calibration or multiple types of recombination. This allows for long or quick simulations, depending on what the user is hoping to obtain from simulations. Advanced calibration was used for this thesis, which is used for accurate process simulation using a selection of models and parameters from basic models to process condition-dependent changes [24]. The Advanced Calibration file contains a set of basic models (such as Si Boron – Transient, Si Dopant-

DiffModel-ChargedPair, etc.) and parameters for the diffusion and reaction equations (such as Si Int ChargeStates). Process condition-dependent changes are called by Sentaurus Process, such as initial conditions after an ion implant [24].

Comparable semiconductor simulators include but are not limited to Minimos by TU Wien (1994), ViennaMOS by TU Wien, PISCES (1989), MEDICI (1993), DAVINCI (1993), and Atlas by Silvaco (1996), and APSYS by Crosslight. Minimos is a general-purpose numerical simulator of semiconductor devices (specifically FETs) in 2D and 3D. This simulator uses only fundamental semiconductor equations, which are solved using Poisson's equation and two carrier continuity equations (for electrons and holes). Relatively simple models are first used for simulation, followed by refinement using more complicated physical mechanisms [25, p. 8]. Downfalls of using Minimos are the lack of advanced calibration models which were important for this thesis, and lack of the ability to simulate SOI in 3D.

ViennaMOS is an open-source GUI-based high-performance semiconductor device and process simulator. This simulator uses a collection of plugins of simulation tools that can be used to build simulation flows. However, this program is currently only a prototype and will be developed to simulate semiconductor device and processing. ViennaMOS can render in 3D and plot in 2D [26].

PISCES was developed at Stanford University, and was later updated and improved by Technology Modeling Associates (TMA). This simulator is used to develop MOS and bipolar integrated circuits. It is considered a powerful 2D device simulator, which models distributions of potential and carrier concentrations. The modelled distributions are used to predict electrical characteristics [25, pp. 8,9]. For this thesis, PISCES was not powerful enough as 3D simulations were important for examining boron suck-out.

MEDICI is the improved version of PISCES by TMA. The improvements allowed users to modify model and material parameters on a region-to-region basis. Arbitrary device geometries are simulated with a non-uniform triangular simulation grid with both planar and nonplanar surfaces. 2D contours and vectors can be produced with MEDICI using data collected from solving semiconductor equations at each node in the simulated device. This data includes device and impurity doping profiles derived from the grid structure [25, p. 9].

DAVINCI is a 3D simulator that will solve 3D distributions of potential and carrier concentrations in a device. This allowed predictions of electrical characteristics with user defined bias conditions. Analysis of minority and majority carrier devices was completed using Poisson's equation and current continuity equations for electrons and holes [25, p. 9].

ATLAS was developed by Silvaco International, and integrates Athena into its simulations [27]. It is similar to Sentaurus with its ability to simulate from the processing stages to electrical characterization and testing. Numerical, physics-based 2D and 3D simulations are used ATLAS to predict electrical behavior of specified semiconductor structures. This simulator provides a user with insight into the physical mechanisms essential to device operation [25, p. 9]. However, the processing simulations can only be completed in 2D, and the output device figures were not as clear and well-defined as Sentaurus' outputs. The grading of material properties and the band discontinuities in the conduction and valence bands are not as well modelled as Sentaurus, although the trapping models of Atlas are extensive [27].

APSYS has good models for devices with multiple different layers, and has good grading of material parameters. However, emphasis has been placed on band structure engineering and quantum mechanical effects. This emphasis is heavily concentrated on the simulation and optimization of applications involving photosensitive or light emitting devices. As this thesis was

based on SOI nMOS devices, this software did not seem fully compatible with the necessary simulations and did not mention process simulation [28].

2.5.3 Meshing

Meshing plays an important role when solving finite-element problems. Computational meshes can lead to a disagreement between experiment result experience and computational results [29]. With a coarse mesh, small changes in results are not calculated correctly, as the change is computed over a large area. With a finer mesh, changes that occur in small areas are calculated with finer detail. However, if meshing is set too fine, then convergence issues come about. When two fine meshes meet at an edge, if the calculated values are different, then the simulation will not converge. It is important to find an optimal mesh that gives enough detail and still converges.

Meshing plays a key role in simulations using Sentaurus. SDevice simulates the device performance by solving multiple, couple physics equations based on the meshing. The finer the mesh, the more complex the solving tools needed. In SProcess, the advanced models for processing steps are combined with mesh generation and the ability to edit generated structures [22]. For this thesis, coarser meshing was used for areas of little change that were not directly affecting the active region of the devices. For example, the silicon substrate and buried oxide had coarse meshing as there was not a large amount of electrical activity in these regions.

Finer meshing was used for areas of high interest where an extensive amount of electrical changes that varied over small regions was present. For example, a fine mesh was set in the silicon film, and an even finer mesh was set at the edge regions where the bird's beak forms. This allowed the boron leakage into the surrounding field oxide to be observed, as well as electron concentration at these edges which was used for optimization of the process.

To determine meshing settings for the different regions, the mesh was initially set fine for the entire device, but was unnecessary for less active regions, and made computational times longer for no benefit to results. Coarser meshes were set for the less active regions. From here, the mesh was refined in the silicon film. A fine mesh was set in the film, and then the mesh was set finer in areas of high interest until the simulations would no longer converge. With finer meshes the simulations take longer to compute, and so the finest meshes were set back to a value that still converged and showed the smallest areas of change that would compute.

2.5.4 Use of SProcess

Sentaurus Process (SProcess) simulates the fabrication process steps in 2D and 3D for silicon process technologies. Parameters used by SProcess have been calibrated with data from equipment vendors, and provides a predictive framework that uses a set of advanced models. This allows users to simulate silicon fabrication processing from nanoscale CMOS to high-voltage power devices. The advanced models include oxidation, diffusion, implantation, and mechanics which are combined with mesh generation and the ability to edit generated structures [22, p. 2].

Users of SProcess can choose to implement advanced implantation and diffusion models, which can be used if fine detail is required. Implant tables implemented by SProcess cover extensive energy ranges (sub-keV to several MeV). Monte Carlo implantation models are efficient and accurate in this tool, which can handle conditions not typically covered well by analytical models. An example of this is sidewall doping of narrow trenches. In addition to this, some of the key important process modules implemented by SProcess include ultrashallow junction formation, high-k/metal gate, and strained silicon [22, p. 2].

As the main point of this thesis is to design a fabrication process that will minimize nMOS edge leakage in SOI devices fabrication at Carleton University, SProcess is a vital tool. The

proposed fabrication process was implemented in SProcess, and this allowed for trial and error optimization of the poly-buffered LOCOS process and the oxidation times and temperatures. This tool allowed the process to be tested and optimized by changing variables in SProcess, where later tools could use the generated structure to test for electrical characteristics.

The structure generated by SProcess allowed for visual optimization of the process for minimizing the bird's beak effect and boron loss at the edges of the devices. This was an exceptional tool to use for visualizing the expected SOI structure, and to view how changes to the process affected the device. Finally, SProcess allowed the processing steps to be broken down into individual steps. This allowed the device to be optimized throughout the process without needing to observe electrical characteristics of a final device, which was useful for understanding the processing of the device and making optimal use of simulation time.

2.5.5 Use of SDevice

Sentaurus Device Editor (SDevice) is a silicon and compound semiconductor device simulator. It simulates the electrical, thermal and optical characteristics of semiconductor devices. Analysis of complex integrated circuit phenomenon such as electrostatic discharge and latch-up can be enabled in SDevice [22, p. 3]. An extensive set of physical models and material parameters support DC, AC, transient, and harmonic balance analysis.

Device performance is simulated by solving multiple coupled physics partial differential equations on a mesh which can be defined automatically or by the user. Voltages and currents can be input into SDevice to calculate electrical characteristics. Physical models used by SDevice during analysis include band structures, Fermi-Dirac statistics, Poisson's equation (continuity equation), band-to-band tunneling, recombination-generation current, drift diffusion current, current, current density, carrier mobility, and velocity saturation [22].

This thesis utilizes the SDevice tool to electrically test the generated SOI structures. Voltages were input to the device terminals using SDevice, which produced an I_D - V_{DS} curve. This curve was used by the SVisual tool to extract electrical characteristics of the SOI devices. The effect of applying voltages to the devices could be viewed using this tool as well. This included produced electric fields, current densities, electron concentrations, recombination areas, etc. The concentration of electrons was important in the design of the SOI devices for this thesis. The concentration at the edges of the devices was minimized by varying process steps in an attempt to minimize the leakage current in the SOI nMOS devices, which could be measured at this stage using SDevice.

2.5.6 Use of SVisual

Sentaurus Visual (SVisual) is a tool that is used to extract different characteristics using the predicted characteristics from SDevice. Input command files can be written to extract different electrical information or create plots for quick visuals. This tool can plot 1D curves (such as current density and characteristic curves), as well as creating cuts along a 2D boundary and plotting data from this area using Tecplot. Quick analysis of device geometry dimensions can be completed by the user, as units are shown along the x- and y-axes. Data can also be exported for plotting in user-chosen tools external to Sentaurus (e.g. Excel) [22].

This thesis utilizes the SVisual tool to extract electrical characteristics of the generated SOI nMOS devices quickly. Command files were written to plot the I_D - V_{DS} curve, and to extract the subthreshold swing and threshold voltage of the generated device. As multiple initial film thicknesses, doping doses, and oxidation times and temperatures were tested at once, SVisual was useful to quickly extract these parameters for immediate comparison of what variances were optimizing the device.

Chapter 3 SOI nMOSFET Simulation

This thesis simulations were completed using Sentaurus. Using Sentaurus Process, the CMOS FD SOI process developed in this thesis was simulated from wafer to device level. The simulations were used to determine approximate boron loss and electron density in different areas of the device. Sentaurus Device was then used to electrically characterize the simulated devices and output characteristic curves.

3.1 Implementation of Process Flow Using Sentaurus Process

The simulated FD SOI process was implemented in separate processing stages in Sentaurus Process. This allowed for optimization of each stage before proceeding in the process. This kept simulation times shorter, as issues were found during each small stage rather than attempting to pinpoint where in the process the device became less optimal. Multiple simulations were also run in parallel with different initial film doping that was available to work with in the fabrication lab, and different pad and field oxidation times. The full simulation file can be found in Appendix A.

The process was split into 9 small simulated process steps as described in Table 3-1 (each simulated process step is referred to as a split from hereon in). An updated device structure and physical characteristics (such as active boron concentration) are output after each split. An example of device structure result after each split is shown in Figure 3-1 to Figure 3-19 below. The process was optimized by assessing the outputs.

This FD SOI process was created to minimize the boron loss during processing, as well as minimizing the bird's beak effect in an attempt to lower the total number of electrons at the edges of the device. Theoretically a lower concentration of active dopant at the edges of the device should decrease the threshold voltage of the formed parasitic device. As such, this process is designed to attempt to have an even distribution of electrons throughout the film, ensuring that the

parasitic edge device does not have a lower threshold than the main channel device and does not turn on first.

Table 3-1 – FD SOI Sentaurus Simulated Process Steps (Splits) and Descriptions

Sentaurus Process Name	Description of Step
SOIWafer	- initialization of wafer geometries and layers
FilmImplant	- growth of mask oxide for implant - implant of boron to silicon film - removal of mask oxide
DeviceIsolation	- growth of pad oxide
PBL	- deposition of polysilicon and nitride for poly-buffered LOCOS stack
LOCOS	- MASK 1: photolithography of PBL stack - etching of nitride, polysilicon, and oxide outside of protected area - growth of field oxide
EtchSiNOx	- etching of the PBL stack (nitride, polysilicon, pad oxide)
PolyGate	- gate oxide growth - deposition of the polysilicon gate - annealing
ToSDevices	- transforms the structure to be 3D by reflecting it in the z-direction
Contacts	- mask used to make thin pseudo source and drain implants for use in electrical characterization - contacts to terminals created to be used in Sentaurus Device

3.2 Physical Device Output from Sentaurus

The following output devices from Sentaurus Process are from wafer 3 and are shown in Figure 3-1 to Figure 3-19. This wafer has an initial film thickness of 116nm and doping of $1.0e12\text{cm}^{-2}$. In the past, the pad oxide thickness was set to 25nm for the ELEC4609 process. To implement poly-buffered LOCOS, the polysilicon and pad oxide in the stack were designed to replace the

25nm pad oxide. As 25nm is very thin to split between two different layers of the stack, 30nm was chosen. The thicknesses were originally designed to be 10nm of pad oxide and 20nm of polysilicon. However, growing such a pad oxide accurately was difficult, and so the pad oxide and polysilicon layers were designed to be 20nm each.

The nitride thickness is designed to be thick for poly-buffered LOCOS. This layer was then designed to be 160nm, which is thick enough to decrease the field oxide encroachment into the silicon film. The polysilicon layer in the LOCOS stack helps relieve stress from a thinner oxide and thicker nitride. Units on the axes in the following figures are measured in microns. The step from the Sentaurus implementation of this process, shown in Appendix A, is indicated in brackets.

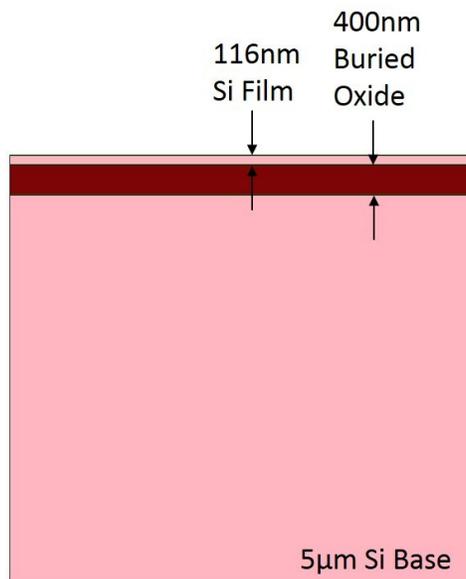


Figure 3-1 – Simulated initial wafer geometry (SOI wafer)

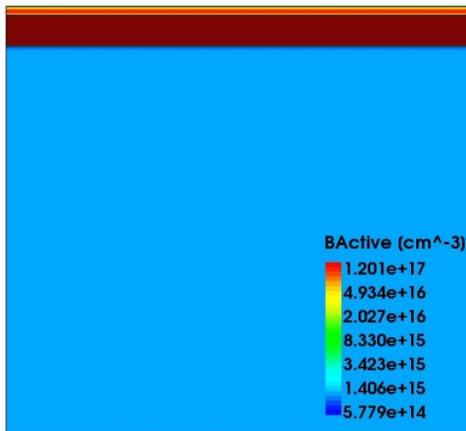


Figure 3-2 – Simulated wafer after boron film implant (FilmImplant)

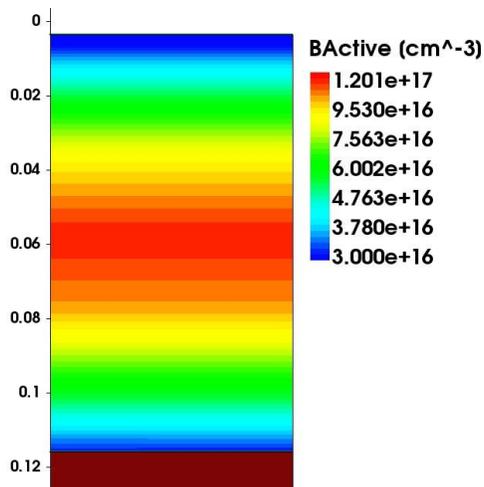


Figure 3-3 – Simulated Si film after boron implant (FilmImplant)

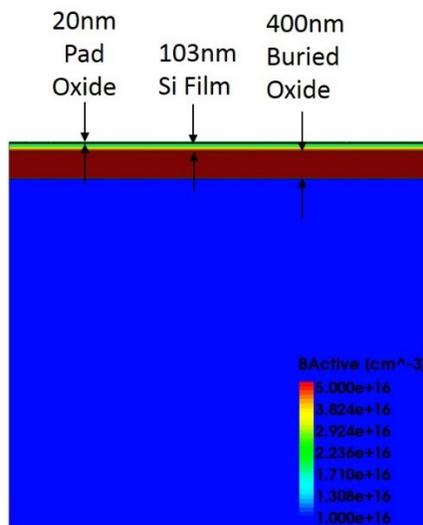


Figure 3-4 – Simulated wafer after pad oxidation (DeviceIsolation)

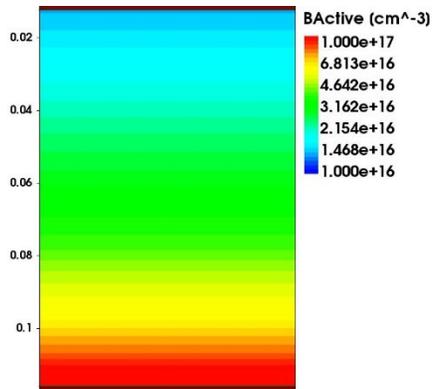


Figure 3-5 – Simulated active boron concentrations in Si film after pad oxidation (DeviceIsolation)

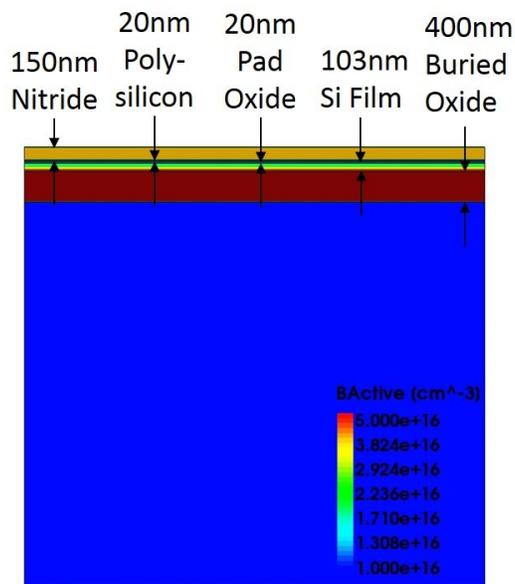


Figure 3-6 – Simulated wafer after polysilicon and nitride poly-buffered LOCOS stack deposition (PBL)

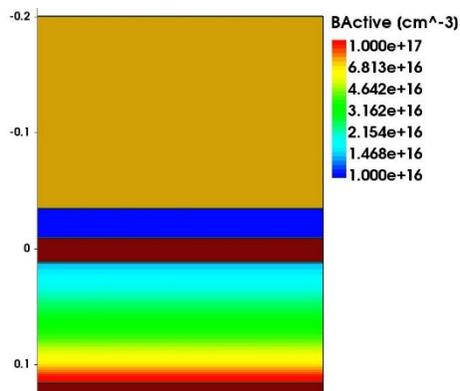


Figure 3-7 – Simulated active boron concentration in Si film after polysilicon and nitride poly-buffered LOCOS stack deposition (PBL)

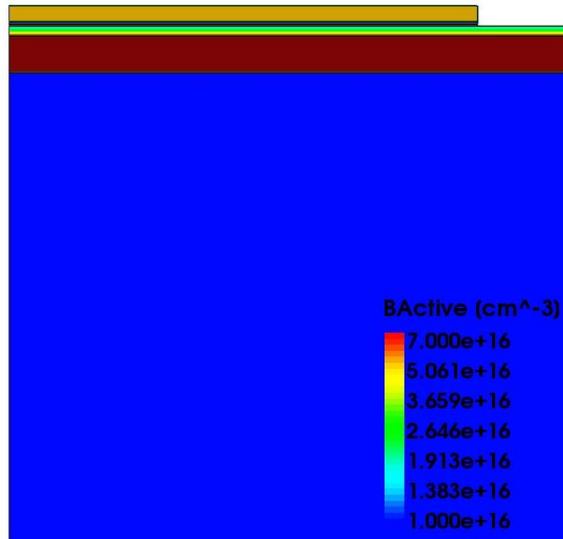


Figure 3-8 – Simulated mask and etch of poly-buffered LOCOS stack for field oxidation (LOCOS)

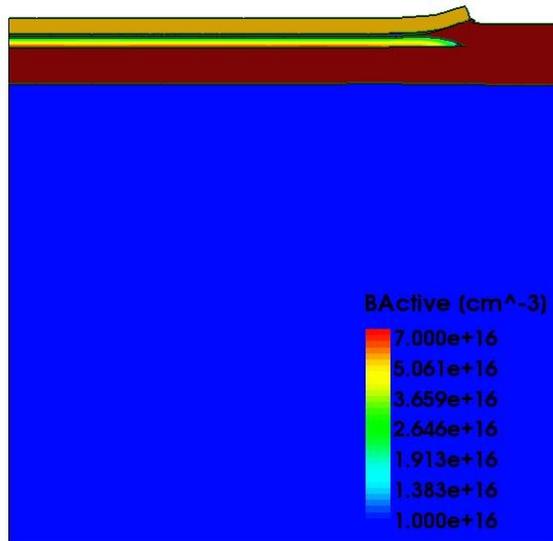


Figure 3-9 – Simulated growth of field oxide during poly-buffered LOCOS (LOCOS)

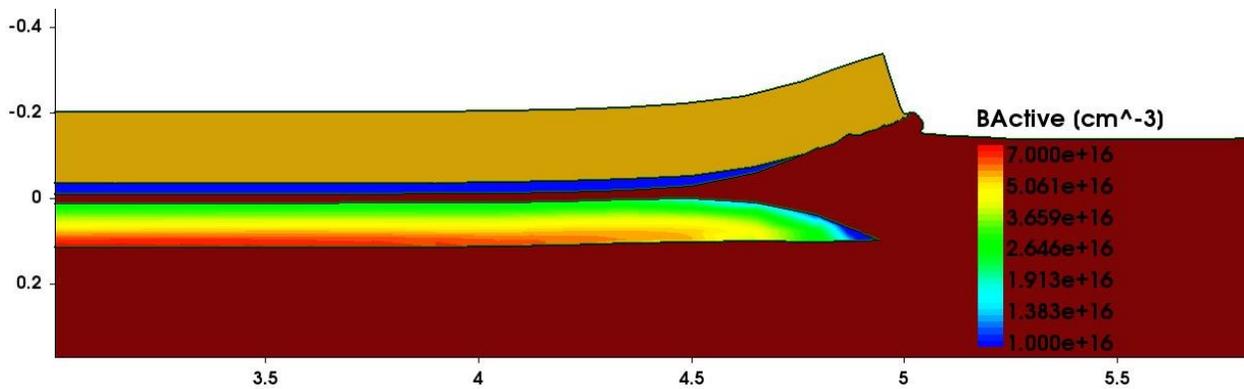


Figure 3-10 – Simulated film edge resultant from field oxidation during PBL, units in μm (LOCOS)

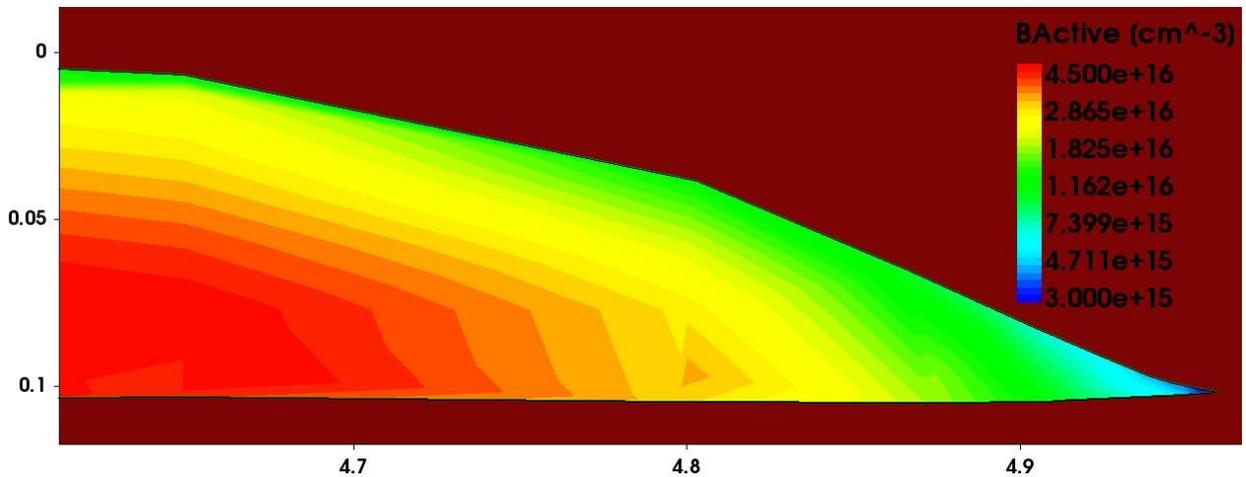


Figure 3-11 – Magnification of simulated film edge after PBL field oxidation (LOCOS)

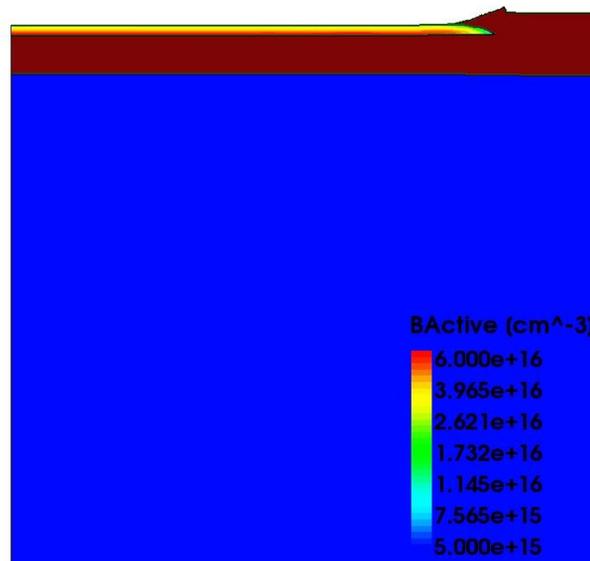


Figure 3-12 – Simulated wafer after etching of poly-buffered LOCOS stack (EtchSiNOx)

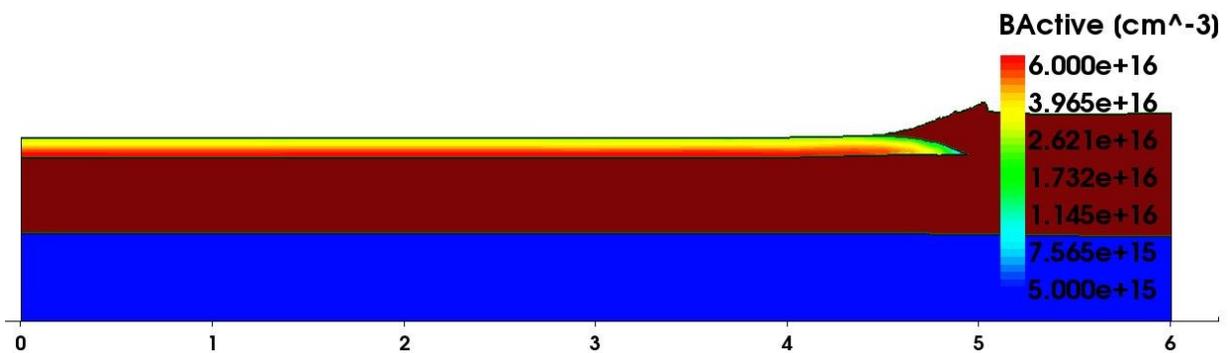


Figure 3-13 – Simulated active boron concentration in film after PBL stack removal (EtchSiNOx)

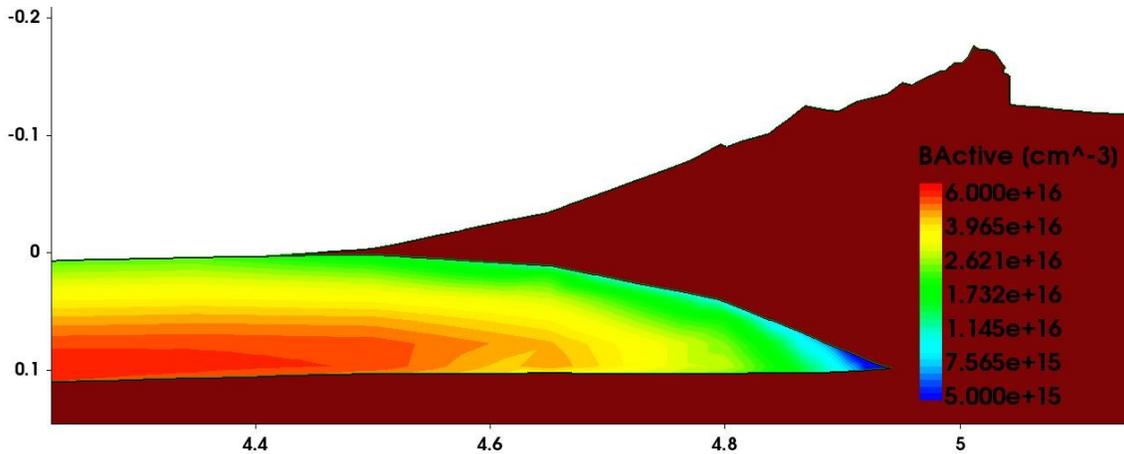


Figure 3-14 – Simulated active boron concentration in film edge after PBL stack removal (EtchSiNOx)

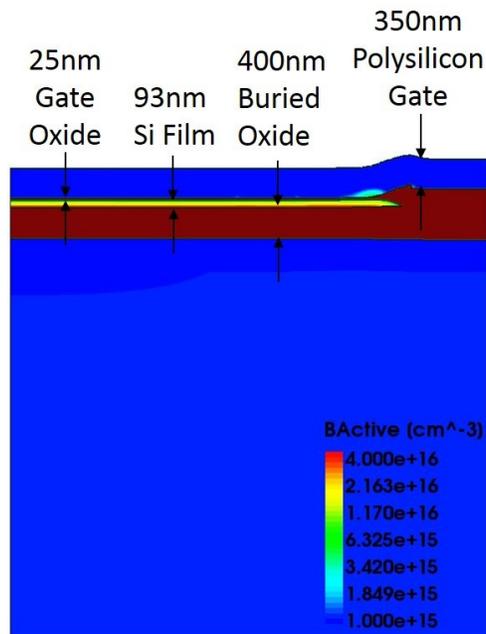


Figure 3-15 – Simulated wafer after growth of gate oxide and deposition of polysilicon gate (PolyGate)

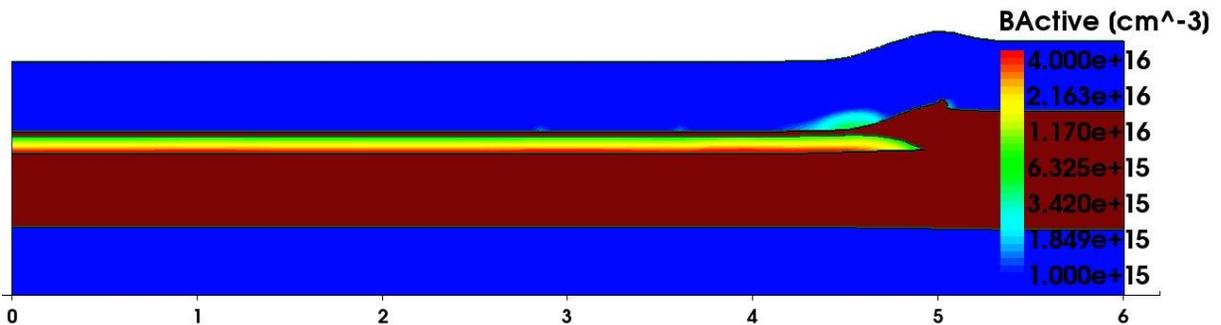


Figure 3-16 – Active boron concentration in simulated film after growth of gate oxide and deposition of polysilicon gate (PolyGate)

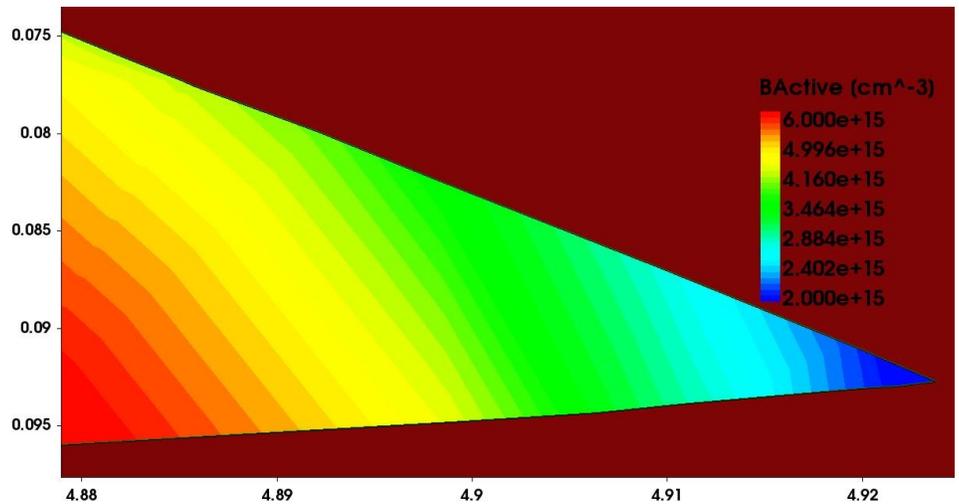


Figure 3-17 – Simulated active boron concentration in film edge after growth of gate oxide and deposition of polysilicon gate (PolyGate)

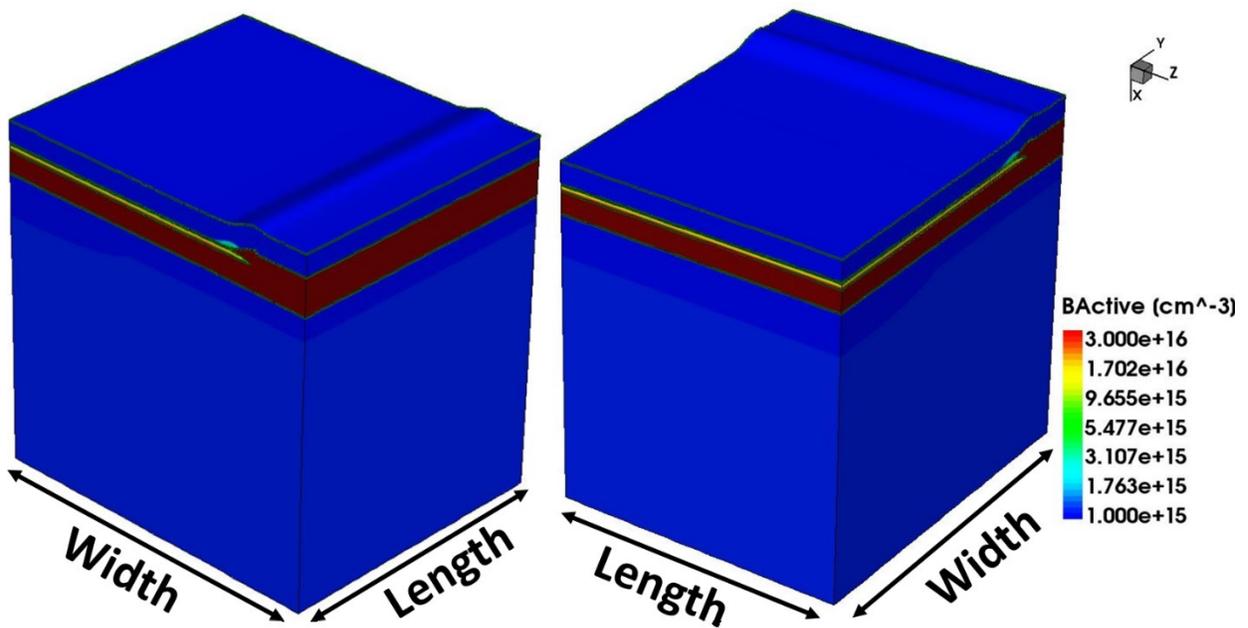


Figure 3-18 – View across the width and length of resultant simulated device after 3D transformation (ToSDevices)

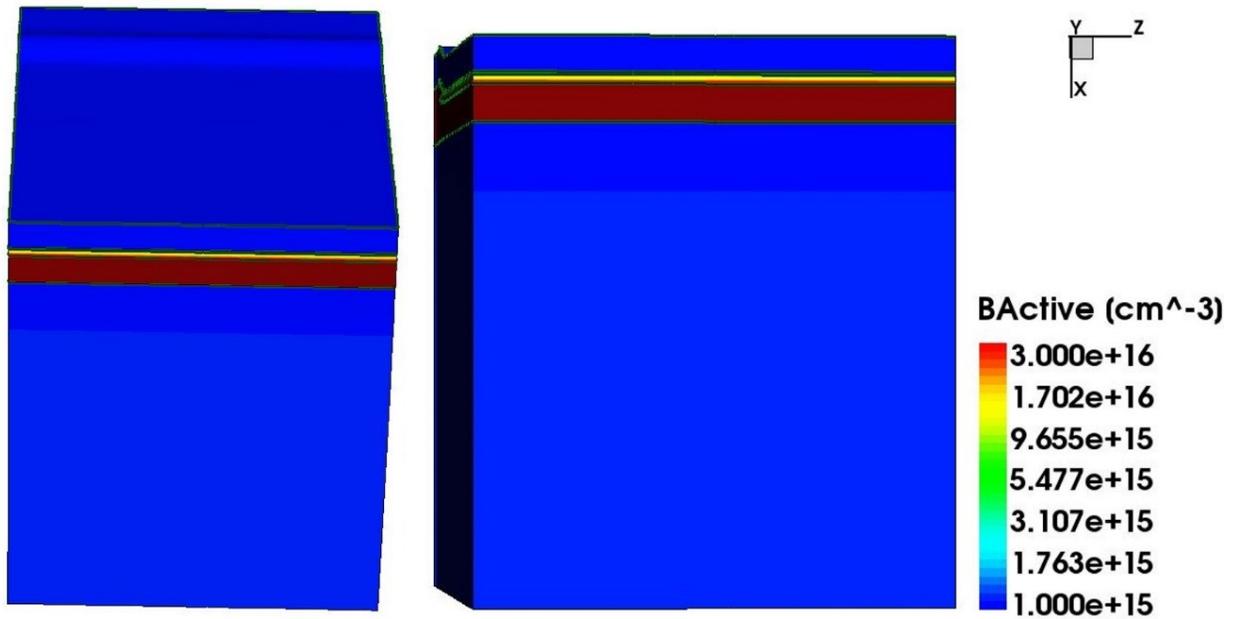


Figure 3-19 – View across the top and front (length) of resultant simulated device after 3D transformation (ToSDevices)

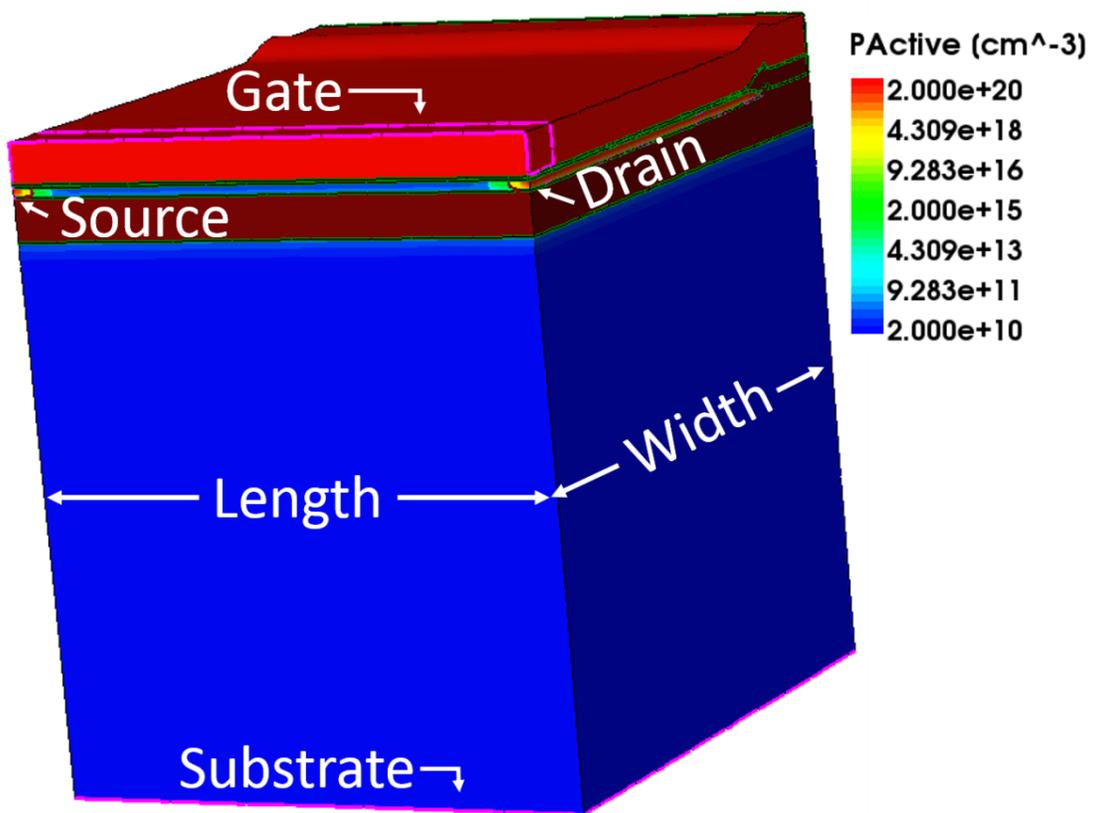


Figure 3-20 – Pseudo thin drain and source contacts created in simulated device by phosphorous doping used only for electrical testing, as well as gate and substrate contacts (Contacts)

3.2.1 Boron Edge Loss Effects

Boron segregates from the silicon film to the surrounding oxide. Simulations have shown that the boron does not only segregate into the field oxide, but also vertically into the pad, buried, and gate oxides during oxidation. This segregation occurs from the high temperatures during oxidation. As boron segregates into the field oxide from the edges of the silicon film, a parasitic transistor is formed at this edge. The parasitic transistors have a lower threshold than the main transistor, which will cause lack of control of the device. This will cause high edge leakage currents, which is a major issue for some circuits.

Simulation outputs shown below illustrate the boron loss into the oxide from the silicon film. When observing just the active boron, Sentaurus will ignore the boron in the oxide as it is considered inactive. To illustrate the boron loss into the surrounding oxide, the total boron was observed. This showed the loss of boron from the silicon film into the oxide. Two examples of the effects of thermal budget are shown below in Figure 3-21 and Figure 3-23. Figure 3-21 shows the boron loss into the oxide with a pad oxidation time of 18 minutes and a gate oxidation time of 28 minutes. Figure 3-23 shows the boron loss with a pad and gate oxidation time of 31 and 45 minutes, respectively.

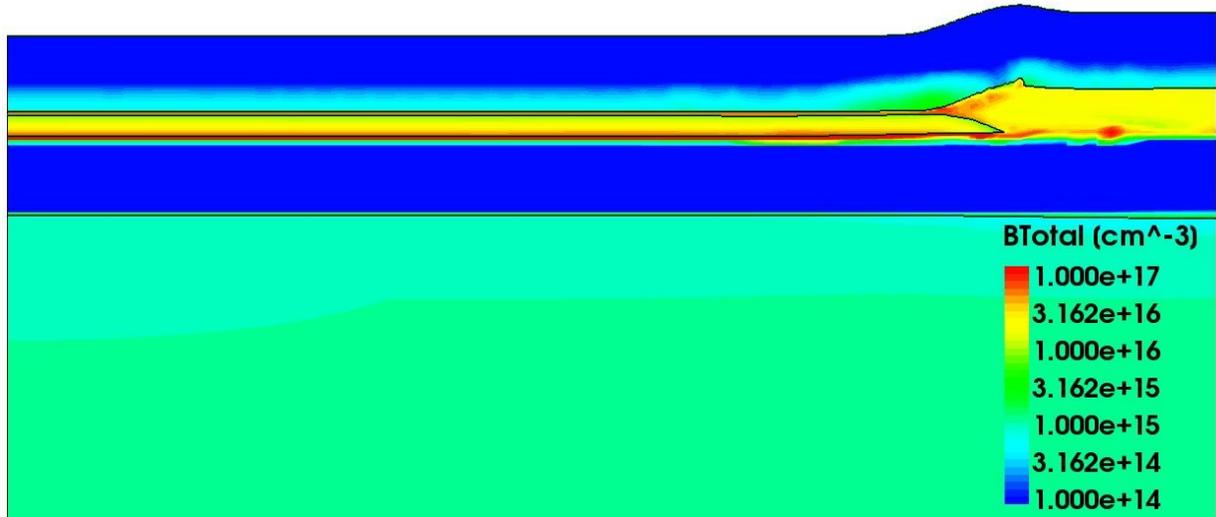


Figure 3-21 – Simulated total boron present in the film and surrounding oxide at the end of the process with a pad oxidation time of 18 minutes and gate oxidation of 28 minutes

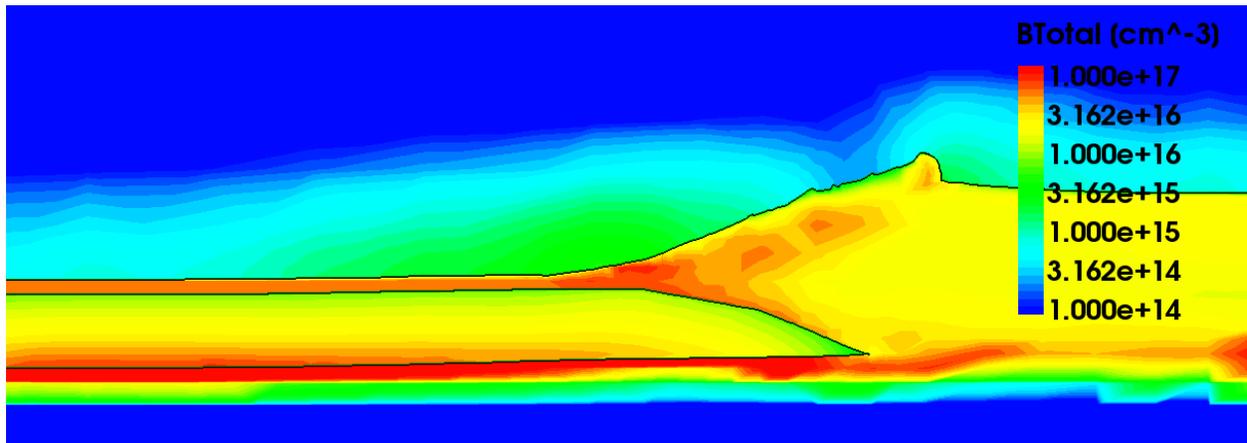


Figure 3-22 – Simulated total boron present at the edge of in the film and surrounding oxide at the end of the process with a pad oxidation time of 18 minutes and gate oxidation of 28 minutes

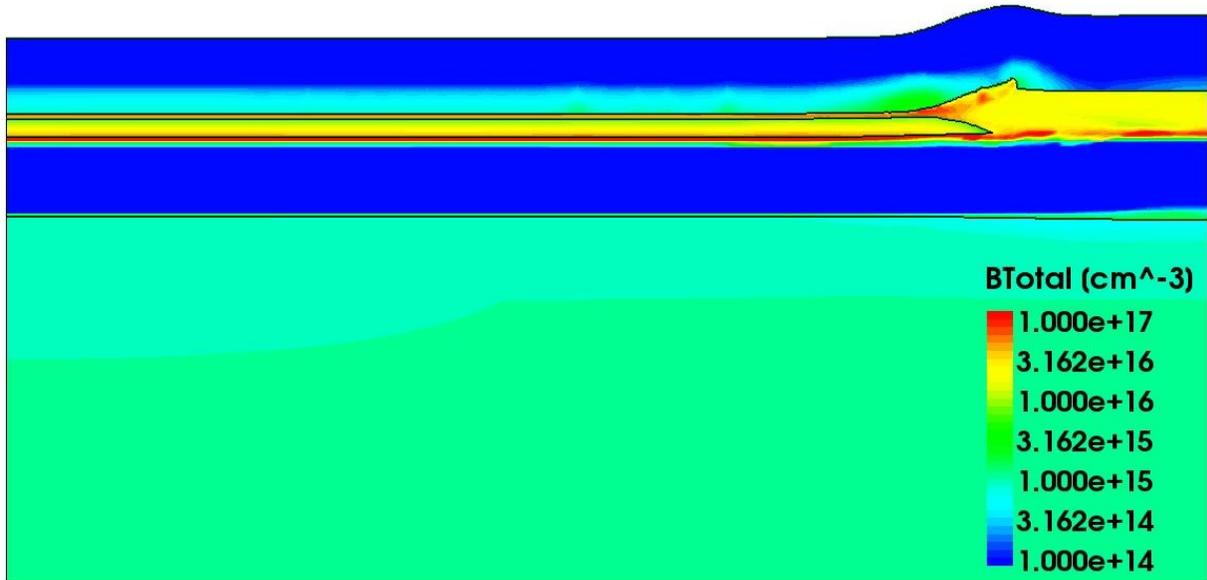


Figure 3-23 – Simulated total boron present in the film and surrounding oxide at the end of the process with a pad oxidation time of 31 minutes and gate oxidation of 45 minutes

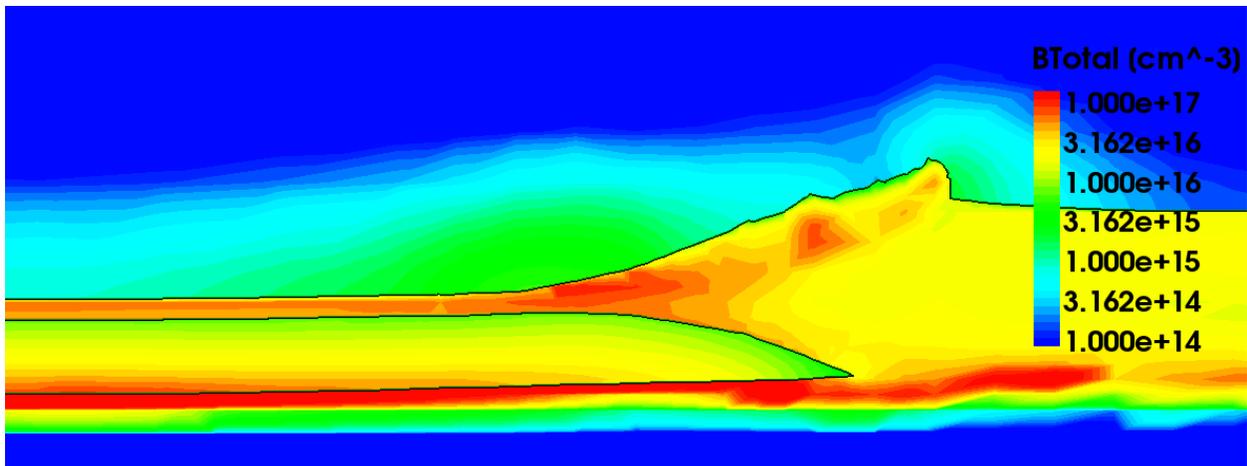


Figure 3-24 – Simulated total boron present in the film and surrounding oxide at the end of the process with a pad oxidation time of 31 minutes and gate oxidation of 45 minutes

As illustrated in Figure 3-24, Figure 3-22, Figure 3-23, and Figure 3-24 there is more boron loss after longer oxidation times. The temperatures were the same for both sets of oxidation times, thus showing how thermal budget affects boron loss. These figures show the loss of boron vertically into the gate and buried oxide layers, as well as into the field oxide. With boron segregating so easily into oxide, it was important to consider thermal budget during the design of

this FD SOI process in order to minimize boron loss. The segregation of boron vertically out of the film was not previously considered, and was a revelation during the design of this process.

Another result of boron loss can be observed in the subthreshold curve. With longer oxidation times leading to more boron loss, the threshold of the device will decrease. For example, in Figure 3-25 the threshold shifted 40mV with small differences in oxidation times.

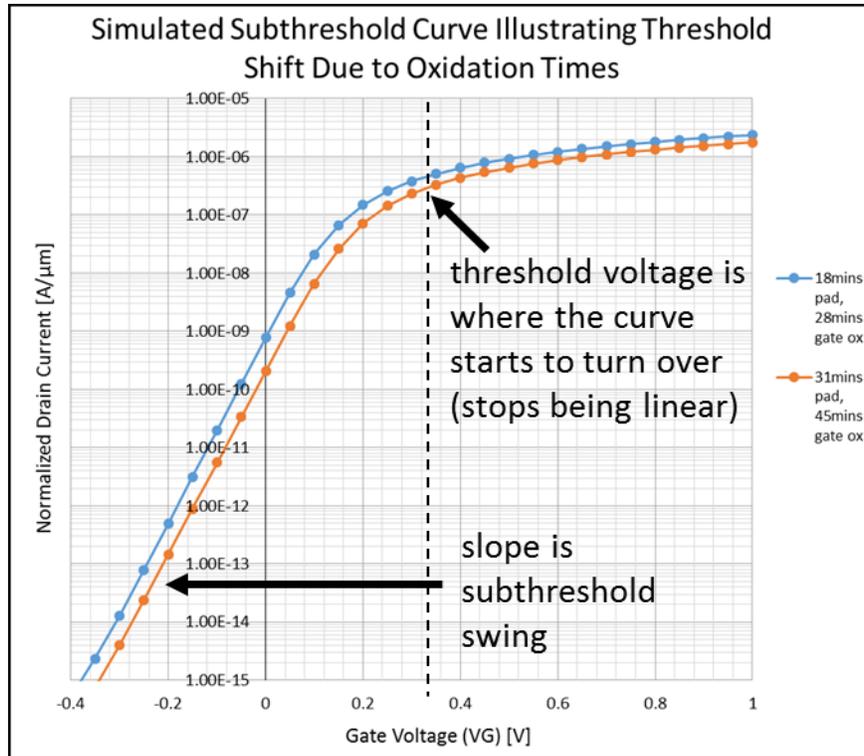


Figure 3-25 – Simulated threshold shift due to varying times during pad and gate oxidation $V_D=0.1V$ (this figure shows $V_T=0.325V$ at dashed line)

3.2.2 Geometrical Effects

Geometrical effects refer to the edge where the active device meets the isolation oxide. Field oxide is grown in areas between active devices for isolation by consuming the silicon film. However, this oxide does not grow isotropically, but rather consumes the film anisotropically. This leads to a pointed tip at the edge of silicon film, which is called the bird’s beak due to the resemblance of the shape to a beak.

Ideally, this edge would be vertical. This would ensure that the gate would have full control over the device, and no electrons could be trapped at the edge leading to higher leakage current. However, this is not possible in LOCOS due to the aforementioned anisotropic growth of oxide in silicon. The process reported in this thesis was designed to not only minimize boron loss, but to also create a steeper and shorter bird's beak. Poly-buffered LOCOS was used to try and produce this steeper edge.

Geometrical effects were explored by simulating LOCOS isolation and observing the electron concentration at the edges of two different devices: one with a bird's beak, and one with the bird's beak etched away having effectively no geometrical effect. Having no geometrical effect means that the boron should ideally be evenly distributed horizontally across the film, as there would be no tapering edge where concentrations would differ. The results are shown in Figure 3-26 and Figure 3-27.

When a bird's beak is formed at the edge of the film, a high concentration of electrons exists at the edge. The density of electrons decreases towards the corner of the edge when observing the density around it in Figure 3-26. The device with no bird's beak shows an even gradient of electron concentration throughout the film, and no large areas of high concentration at the edges. These observations enforced the importance of having as steep an edge as possible.

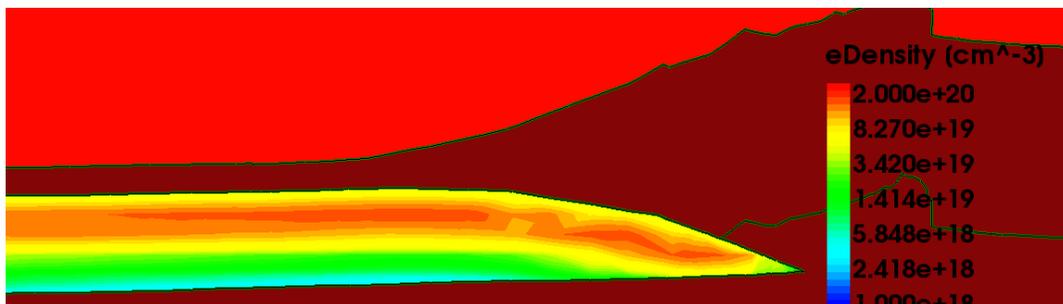


Figure 3-26 – Simulated electron density at the edge of the silicon film with a bird's beak ($V_D=0.1\text{V}$)

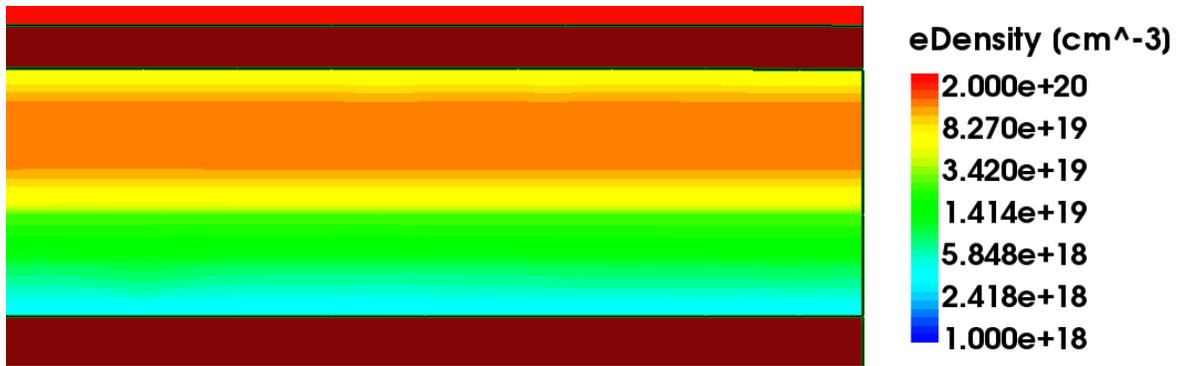


Figure 3-27 – Simulated electron density at the edge of the silicon film with no bird’s beak ($V_D=0.1V$)

The polysilicon layer implemented in the LOCOS stack in poly-buffered LOCOS relieves stress from the nitride layer allowing for a thinner pad oxide. This minimizes the encroachment of the field oxide underneath the LOCOS stack resulting in a shorter bird’s beak [7]. To minimize the geometrical effects in the process designed for this thesis, PBL was used for device isolation. A simulation using conventional LOCOS for this process is shown in Figure 3-28, and a device using PBL is illustrated in Figure 3-29 which shows the shorter bird’s beak using PBL.

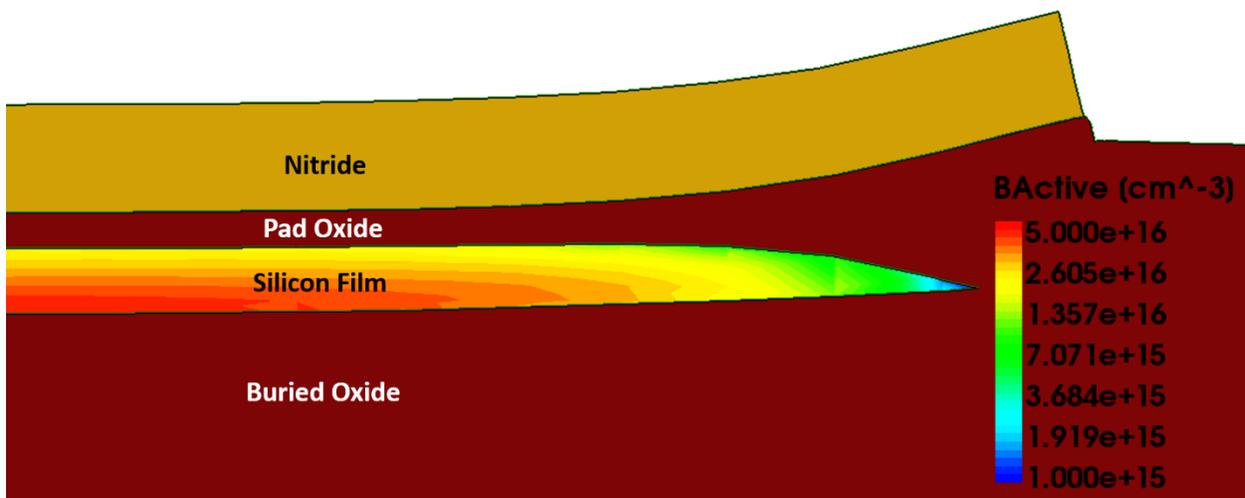


Figure 3-28 – Conventional LOCOS simulation

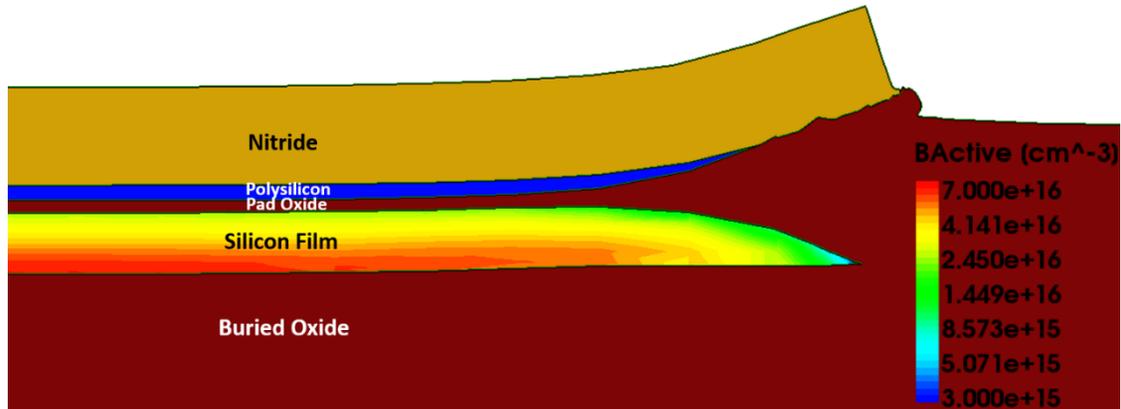


Figure 3-29 – Poly-buffered LOCOS simulation

3.3 Subthreshold I-V Curve Output From Sentaurus

The presence of parasitic edge transistors in fully-depleted SOI nMOS can be observed in the subthreshold curve of the device in the form of a kink. An example of this is shown in Figure 2-6. To determine if parasitic edge transistors are created in the nMOS devices for this FD SOI CMOS process, simulated subthreshold curves were observed. An example of this output curve is shown in Figure 3-30, which was created in Sentaurus by electrically testing the simulated devices.

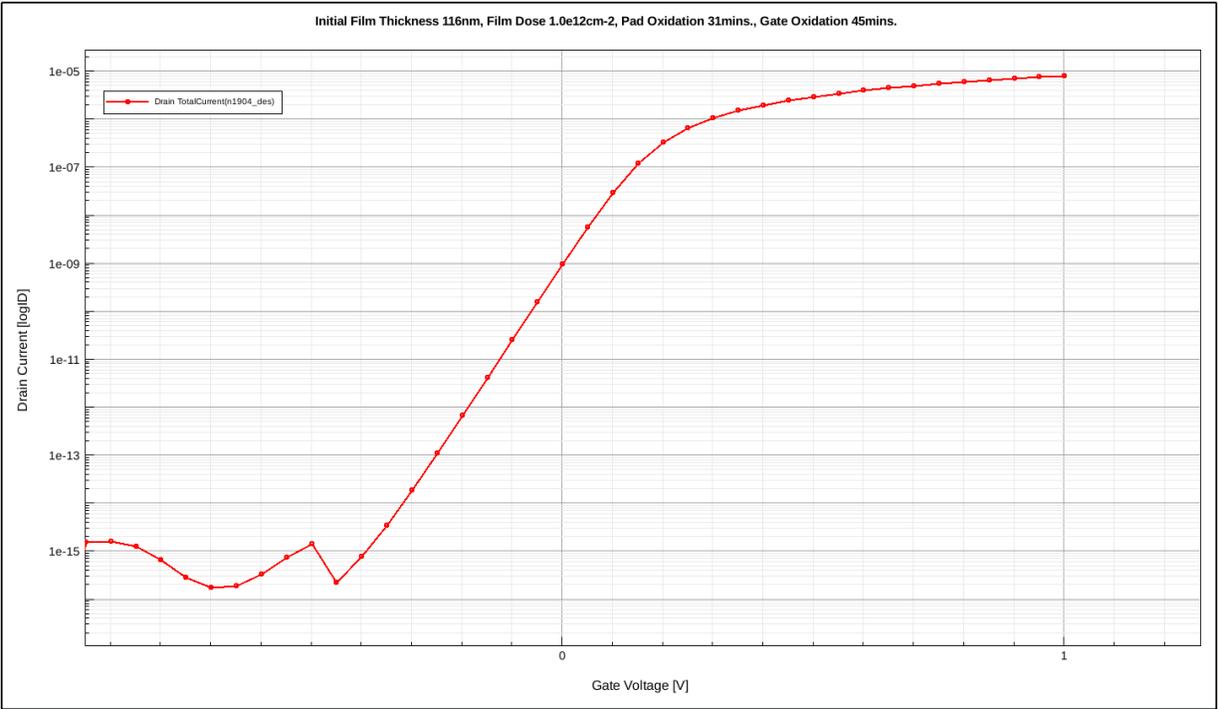


Figure 3-30 – Subthreshold curve created using Sentaurus output data for a simulated FD SOI nMOS device

nMOS devices created in 2014 using an FD SOI process run in the Carleton University Microfabrication Lab revealed kinks in the experimental subthreshold curves as seen in Figure 2-6. To determine if a subthreshold curve with a kink could be simulated, this 2014 process was implemented in Sentaurus. The resultant device showing LOCOS isolation with too long of field oxidation time and too high a temperature is shown in Figure 3-31.

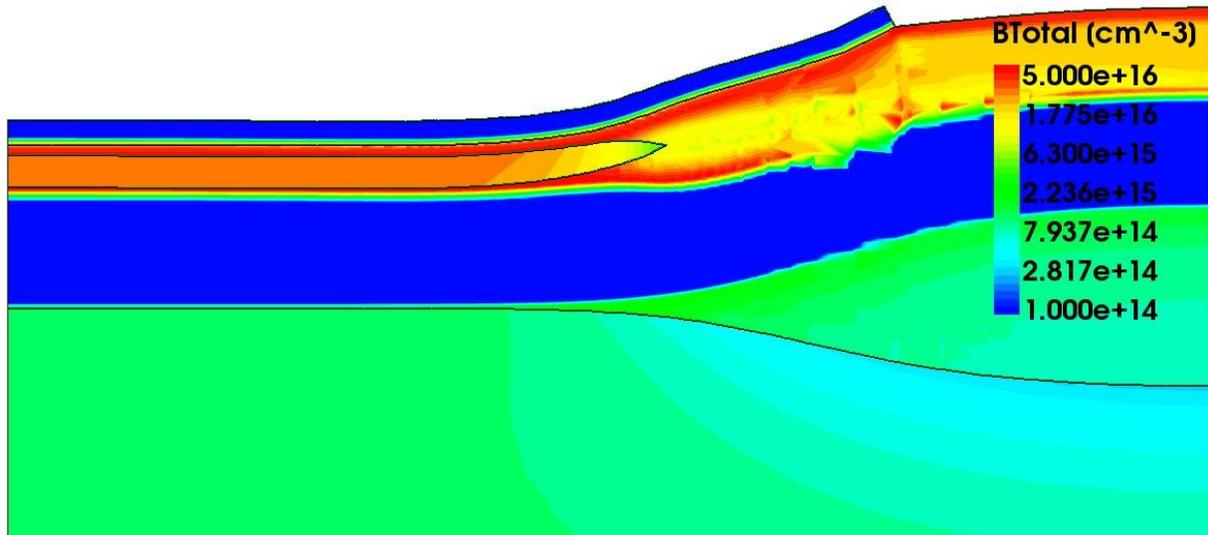


Figure 3-31 – Simulated nMOS device with conventional LOCOS from the 2014 FD SOI CMOS run

The 2014 SOI nMOS device evidently has an extremely high loss of boron into the surround oxide, leaving minimal boron in the Si film. In this case little difference in threshold voltage between the edge and central parts of the device is expected. As show in Figure 3-34, the simulated subthreshold curve indeed does not show two-part behaviour or a “kink.

Simulations were then run with the 2014 SOI process in two different ways: with and without an edge (bird’s beak). It would be expected that the device with and without an edge (such

as in Figure 3-27) would have different threshold voltages showing the effect of the parasitic edge transistor turning on before the main transistor. The resultant plot is shown in Figure 3-32.

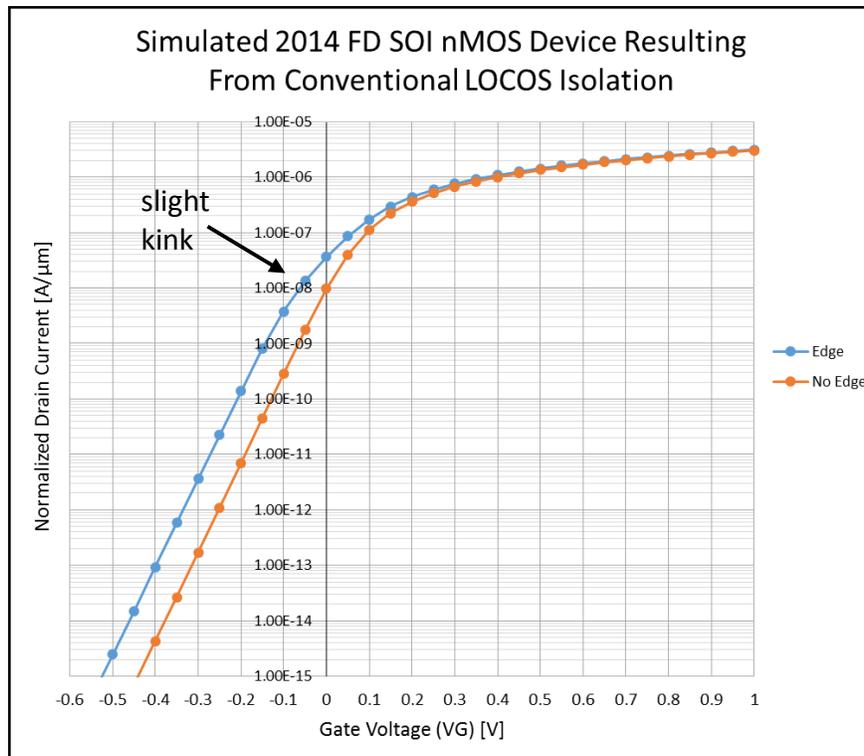


Figure 3-32 – Simulated 2014 FD SOI nMOS Device with and without an edge (bird’s beak)

This figure illustrates that the device with an edge and without an edge have the same low threshold voltage. This suggests that the simulated device has lost almost all of the boron from the Si film, and that the edge transistor has almost the same threshold voltage as the main device. It is suspected that Sentaurus overestimates the boron loss into the surrounding oxide, which would explain why the simulated and experiment results from the 2014 SOI run do not agree.

A small kink can be observed in the device with an edge in Figure 3-32, showing the presence of an edge transistor with a lower threshold voltage than the “main” transistor. Combining these curves to try to illustrate a device with the parasitic edge transistors threshold and “main” transistor threshold does not show this kink, because the edge transistor seems to completely dominate the current flow in this device. This is shown in Figure 3-33.

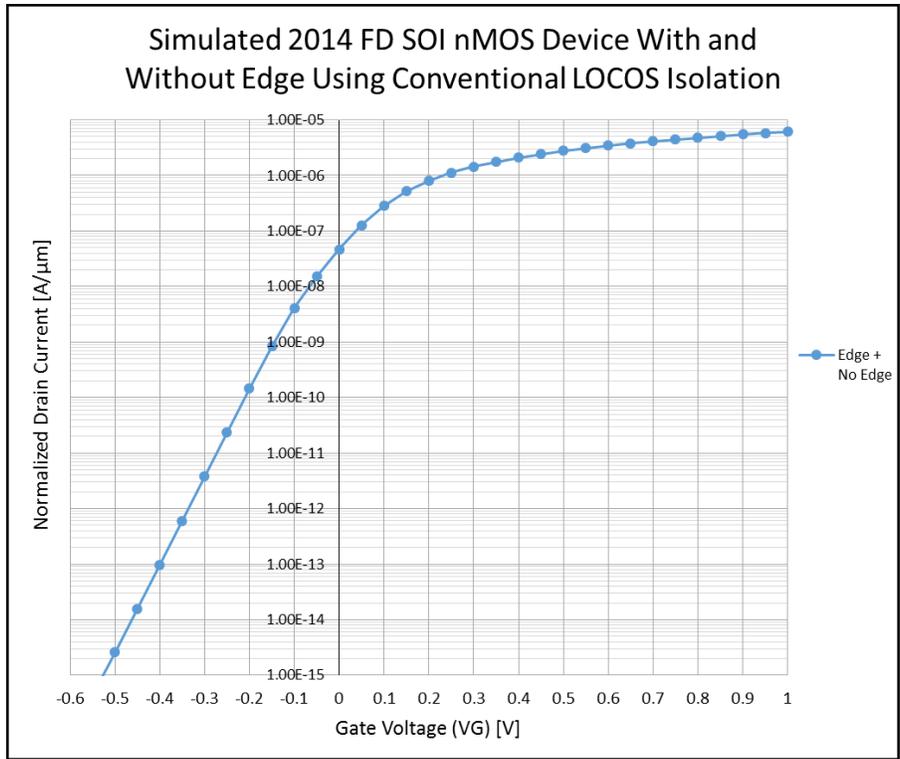


Figure 3-33 – Simulated 2014 FD SOI nMOS device: edge + edgeless device to simulate device with threshold of edge transistor and “main” channel transistor ($V_D=0.1V$)

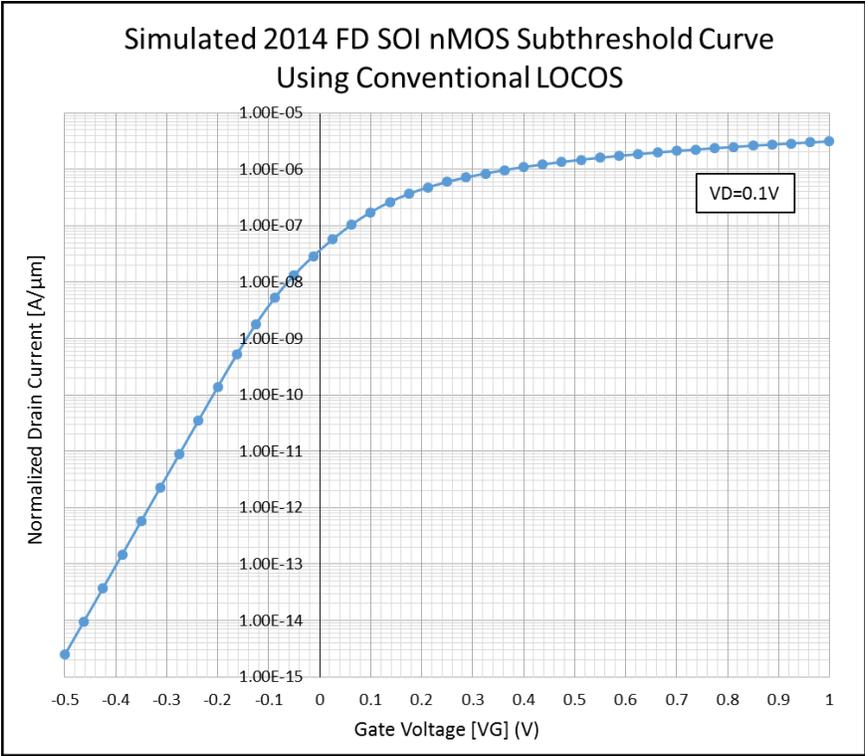


Figure 3-34 – Subthreshold curve from Sentaurus simulation of conventional LOCOS with too long field oxidation time and too high temperature (with silicon film edge)

Figure 3-34 illustrates not only the lack of expected kink from Sentaurus simulations, but also a very low threshold voltage. The threshold voltage around 0.14V is much lower than the expected 0.3V. This low threshold is evidence of massive boron loss in the device.

The mesa isolation SOI run was also implemented in Sentaurus. The mesa device is not subjected to a field oxidation, so it does not suffer from severe boron loss. This simulated curve did show a kink, as shown in Figure 3-35.

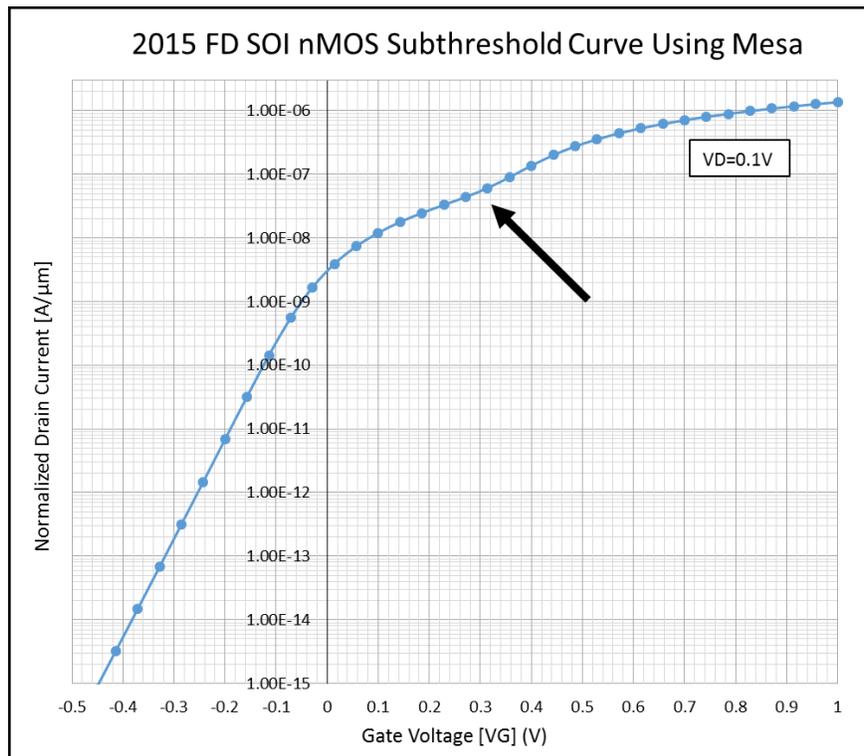


Figure 3-35- Simulated subthreshold curve from device using mesa isolation, kink indicated by the arrow

With this in mind, the process developed for this thesis is expected to be conservative in that the actual boron loss during field oxidation is likely to be less than that simulated here. If the simulated subthreshold curves do not show two-part kinked behaviour, there is strong reason to believe the actual devices will not either.

3.4 Initial Silicon Film Conditions of Present Available SOI Wafers

This FD SOI CMOS process was designed with consideration to starting SOI material already available in the Carleton Microfab. From the past ELEC4609 run, four Smart Cut SOI wafers were available for fabrication of the devices for this thesis. These wafers were all from the same batch, but each wafer had different initial processing in preparation for ELEC4609. The initial conditions of the silicon film in each of these four wafers are detailed in Table 3-2. As this thesis employed these available wafers in order to fabricate the devices at Carleton University expeditiously, simulations were optimized using these four different initial films.

Table 3-2 – Initial SOI Wafer Conditions

SOI Wafer Number	Initial Si Film Doping [cm ⁻²]	Initial Si Film Thickness [nm]
1	1.3e12	114
2	1.2e12	116
3	1.0e12	116
4	1.4e12	110

3.5 Optimized SOI nMOS Device and Process

The process designed for this thesis intended to minimize the nMOS edge leakage discovered in past runs of the FD SOI CMOS process at Carleton University. Two different objectives were made to accomplish this: minimizing boron loss from the silicon film into the surrounding oxide, and shortening the bird's beak. The final optimized process is found in Appendix B: Summer 2015 FD SOI nMOS Run.

Boron loss from the silicon film, specifically at the edges, occurs during oxidation steps. Boron segregates into oxide more easily than it will redistribute evenly in the silicon film. To minimize the boron loss in this process, oxidation times and temperatures and thermal budget were considered. Two types of oxidation were also used: dry and wet oxidation. Both types of oxidation have rates dependent on temperature, but a low temperature was set for the oxidation steps in this

process for minimization of boron loss.

Dry oxidation uses O_2 to oxidize the silicon into SiO_2 . This process is well controlled at an oxidation rate around $<100\text{nm/hr}$. This will result in quality oxide with better material properties than wet oxidation, as the density of the oxide is slightly higher. Dry oxidation is typically used for oxides with thicknesses up to 100nm [30].

Wet oxidation uses H_2O vapor, and will grow much faster than dry oxidation. This type of oxidation will be used for the growth of thicker oxides, such as for electrical isolation or for ensuring higher threshold voltages of parasitic transistors. Wet oxides also have a higher porosity to impurities than dry oxide. As such, this type of oxide is more commonly used when the oxide is not electrically critical, such as field oxide rather than gate oxide [30].

The first oxidation step is the pad oxide grown for the LOCOS stack using dry oxidation. This oxidation step utilizes the lowest temperature that will create a good oxide at atmospheric pressure: 950°C . This is the minimum temperature that SiO_2 will viscously flow which reduces interface roughness [31, p. 171]. A rough interface leads to a lower breakdown voltage and a high defect density. Equipment was not available to oxidize at higher pressures, which would have allowed a quicker oxidation at lower temperatures.

By implementing a poly-buffered LOCOS isolation process, the pad oxide was designed to be only 10nm which results in a shorter oxidation time. PBL also creates a shorter bird's beak, which minimizes the geometrical effects on the device. Oxidation was too difficult to control for such a thin oxide during fabrication at Carleton University. Thus, the pad oxide was redesigned to be 20nm , which still allowed for a short oxidation time. Simulations showed that 31 minutes of dry oxidation at 950°C is expected to grow 20nm of pad oxide.

The second oxidation step is the field oxide grown for isolation using wet oxide. The field

oxidation temperature was designed to be 950°C. The target thickness was designed to be 280nm after finding an optimized field oxidation time. This ensured that the entirety of the 100nm of silicon film would be fully consumed for full device isolation, while only oxidizing for just as long as necessary to isolate which minimized boron loss during this step.

Using Sentaurus, the field oxide time was designed by varying oxidation times. When oxidation time was too short, the field oxide did not fully isolate the device, leaving silicon film between the field and buried oxide seen in Figure 3-36. If the time was too long, the edge of the silicon film would start to bend up as oxide started growing underneath the film, as seen in Figure 3-31. The ideal field oxidation time was found by starting at a time that did not fully isolate the device, and increasing the time just until full isolation. This left a pointed bird's beak tip at the edge as shown in Figure 3-37, and so the time was increased slightly until the corner of the edge was not pointed as shown in Figure 3-29. Simulations showed that 65 minutes of wet oxidation at 950°C is expected to grow 280nm of field oxide for full isolation.

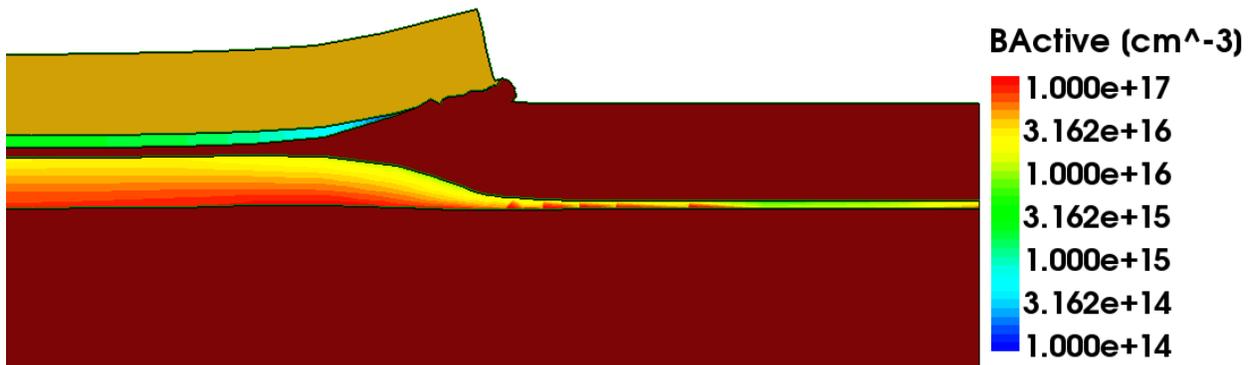


Figure 3-36 – Example of not oxidizing long enough during field oxidation, not isolating the devices

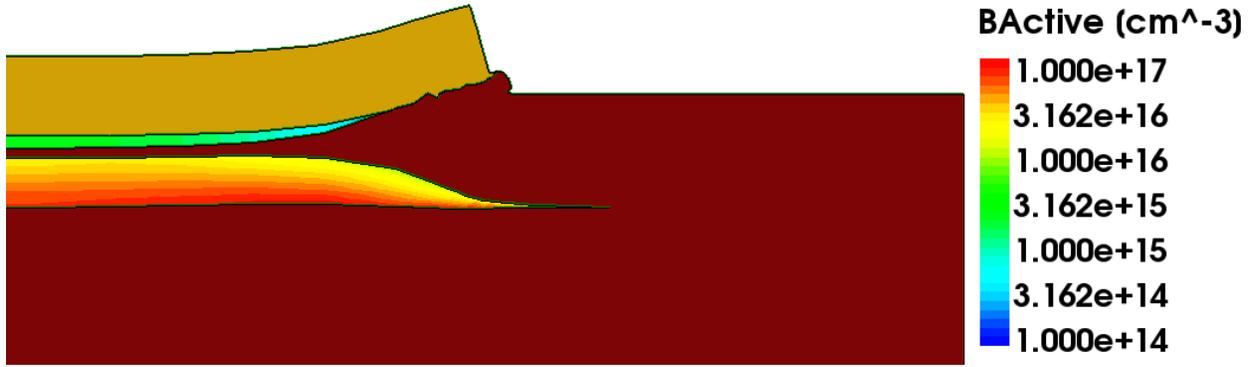


Figure 3-37 – Example of not oxidizing long enough during field oxidation, leaving a pointed tip (bird's beak)

The third and final oxidations step in this process is the gate oxide growth using dry oxidation. Again, the temperature is kept as low as possible at 950°C. A thin gate oxide can lead to a decreased minimum gate length, reasonable threshold voltages, smaller subthreshold swing, better control over the channel (for shorter lengths), and less effects from hot carriers. Equation 3-1 illustrates that minimum gate length is proportional to the oxide thickness and junction depth [32]. For SOI, the junction depth can be assumed to be the silicon film thickness. In order to decrease the minimum gate length, then so too must the oxide thickness.

Equation 3-1
$$L_{min} = T_{ox} \cdot X_j^{\frac{1}{3}} \equiv T_{ox} \cdot T_{Si}^{\frac{1}{3}}$$

The threshold voltage of the device will decrease with an increased oxide thickness (t_{ox}) as shown in Equation 2-2. As drain current will increase with a lower threshold voltage as seen in Equation 3-2, the subthreshold swing will then decrease as shown in Equation 3-3. When the gate oxide is thinner, the gate will be able to control the channel more efficiently. Also, as the gate oxide becomes thinner, the damaged interface region from hot carrier effects is moved into the drain region [33]. This reduces the hot electron effect on the device as the effective damage length in the active channel will be reduced [33].

Equation 3-2
$$I_{D,max} = \frac{W}{L} \mu_n C_{ox} \frac{(V_{DD} - V_T)^2}{2}$$

Equation 3-3

$$S = \frac{\Delta V_{GS}}{\Delta \log_{10}(I_D)}$$

Using this information, a thin gate oxide is ideal. As aforementioned, it is difficult to control dry oxidation for oxides less than 20nm thick in the Carleton University Microfabrication lab without diluted oxygen. Thus, a thin gate oxide of 25nm was designed for this process. Simulations showed that 45 minutes of dry oxidation at 950°C is expected to grow 25nm of gate oxide.

With times and temperatures set for the simulation of the FD SOI CMOS process, the nMOS devices were fully simulated. To set the times for oxidation, simulations of the process were split into subsections. Each subsection was simulated until the desired result was accomplished before continuing to the next step. To optimize the device, it was fully simulated and electrical simulations were completed to extract the subthreshold curve.

The curve was examined, and changes to the process for optimization would be completed. The effect on the threshold voltage after varying times and temperatures in the process was observed by plotting the subthreshold curve before and after changes. Device threshold voltage was designed to be between 0.2-0.4V. This same technique was also used to observe changes in the subthreshold swing, which was designed to be around 60-65mV/decade.

The results from simulations are shown in Table 3-3. The four available starting wafers were all simulated to observe differences due to initial film doping and thickness. This also created available results for comparison to experimental data after fabrication. For all wafers, the resultant threshold voltages and subthreshold swing values are within specification. Some of the threshold voltages were slightly lower than expected, but the optimized process results in most of the device variations to be within design specifications.

Table 3-3 – Results from Sentaurus of the FD SOI nMOS device simulations

SOI Wafer Number	Initial Si Film Doping [cm ⁻²]	Initial Si Film Th. [nm]	Pad Ox. Time [mins.]	Field Ox. Time [mins.]	Final Si Film Th. [nm]	Δ Film Th. [nm]	Threshold Voltage [V]	SS [mV/dec]	Normalized Leakage Current [nA/μm _{width}]
1	1.3e12	114	31	45	91	23	0.306	63.54	0.146
				28	94	20	0.251	63.05	1.363
			18	45	93	21	0.331	63.39	0.063
				28	96	18	0.272	62.68	0.692
2	1.2e12	116	31	45	93	23	0.287	63.52	0.284
				28	95	21	0.235	63.47	2.449
			18	45	95	21	0.308	63.35	0.136
				28	98	18	0.253	62.95	1.341
3	1.0e12	116	31	45	93	23	0.228	64.51	2.018
				28	96	20	0.168	66.95	12.571
			18	45	96	20	0.247	63.93	1.104
				28	98	18	0.203	65.33	7.592
4	1.4e12	110	31	45	87	23	0.314	64.07	0.133
				28	90	20	0.258	63.12	1.069
			18	45	89	21	0.343	63.94	0.052
				28	92	18	0.281	62.73	0.492

Chapter 4 Fabrication of FD SOI nMOS Devices

The fabrication of the fully-depleted silicon-on-insulator nMOS devices was completed in the Carleton University Microfabrication Laboratory. This allowed hands-on fabrication of the devices. The process is designed to use the available equipment and techniques used for the fabrication of ELEC4609 devices.

An abbreviated nMOS only process flow was designed and fabricated. This process did not have a p+, BPSG, contact, or metal layer. The abbreviated flow allowed for a quick fabrication with fewer photolithographic steps, and thus fewer generated mask levels. This also kept the layout design simplified. Probing was executed directly into large pads designed for probing directly into the silicon film.

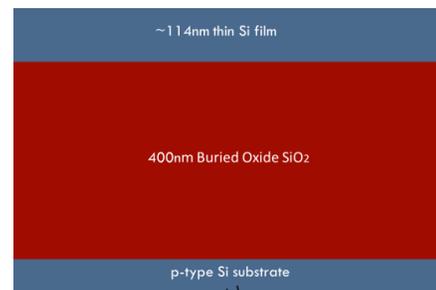
4.1 FD SOI nMOS Process Flow Overview

1. Starting Material

four wafers labelled:
F15-1, F15-2, F15-3, F15-4

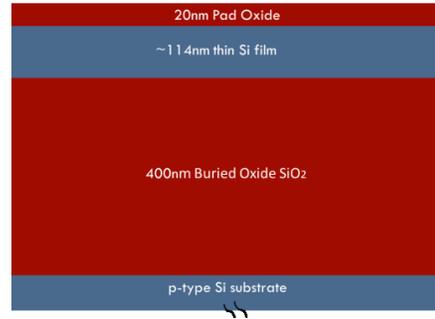
buried Oxide Thickness of 400nm
substrate lightly doped p-type

Wafer F15-	Initial Si Film Doping [cm ⁻²]	Initial Si Film Thickness [nm]
1	1.3e12	114
2	1.2e12	116
3	1.0e12	116
4	1.4e12	110

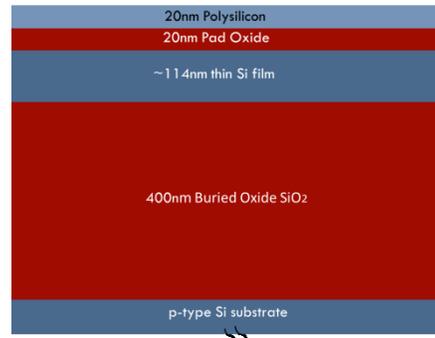


2. Pad oxidation
20nm

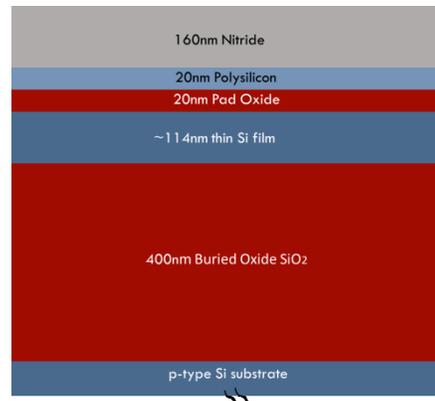
dry oxidation at 950°C for 31 minutes



3. Polysilicon deposition
20nm polysilicon

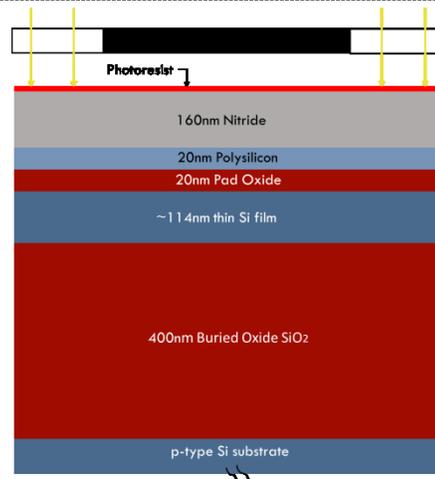


4. Nitride deposition
160nm nitride

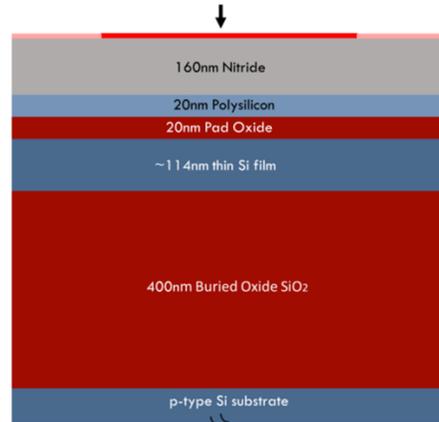


5. Device well **P.E.1**

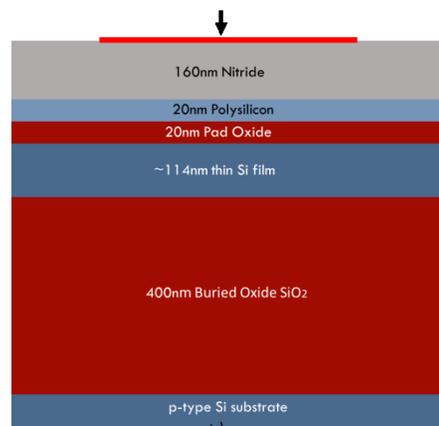
- apply photoresist
- expose to light through mask



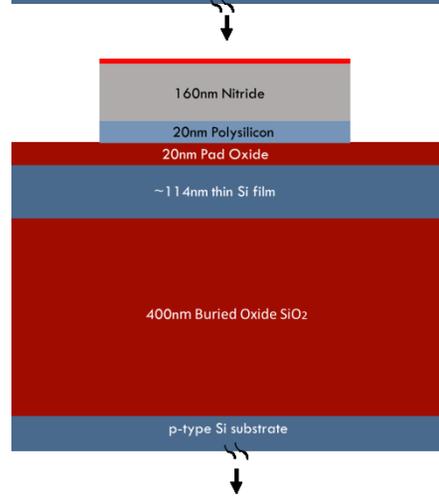
non-exposed photoresist is hardened



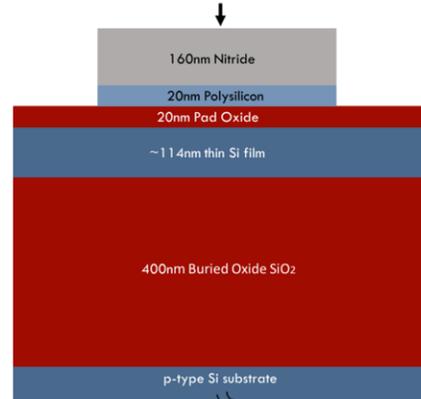
remove photoresist in non-protected areas



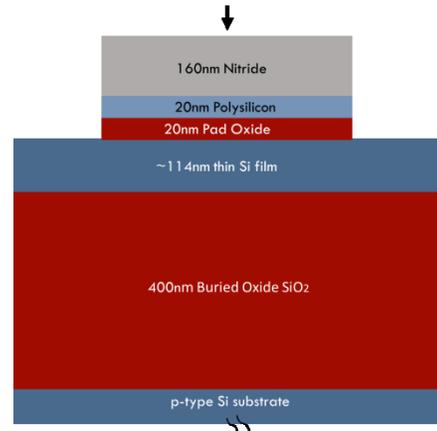
etch nitride and polysilicon in non-protected areas



strip photoresist

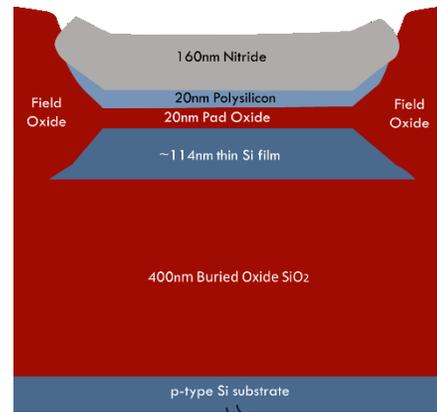


remove 20nm pad oxide



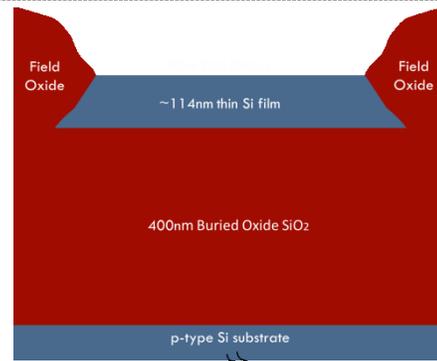
6. Field oxidation

wet oxidation at 950°C for 65minutes
target thickness: 280nm

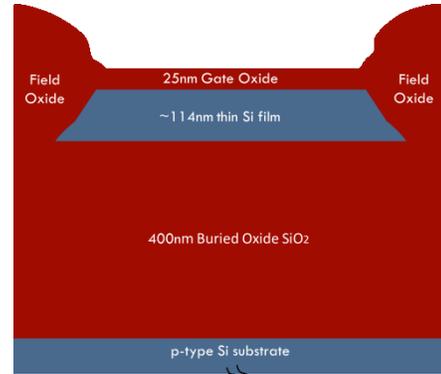


7. Nitride, polysilicon, and pad oxide removal

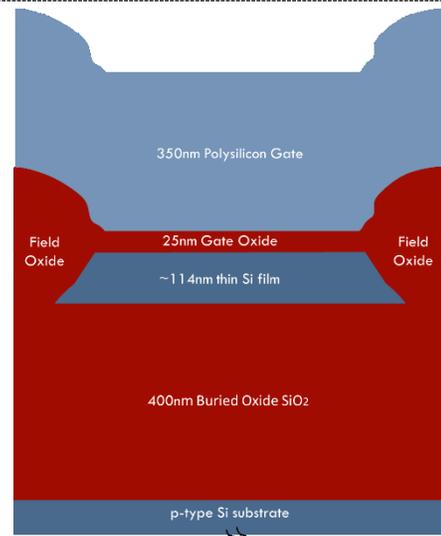
- remove converted nitride
- remove 160nm nitride and 20nm polysilicon
- remove 20nm pad oxide



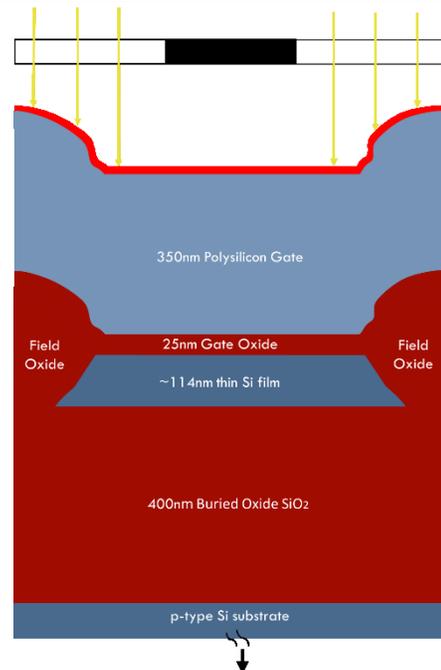
8. Gate oxidation
dry oxidation at 950°C for 45 minutes



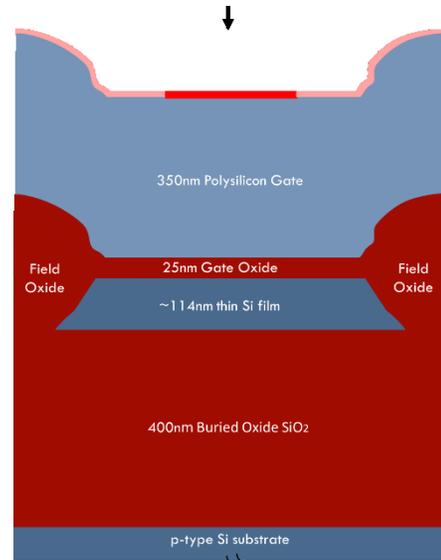
9. Polysilicon gate deposition
350nm



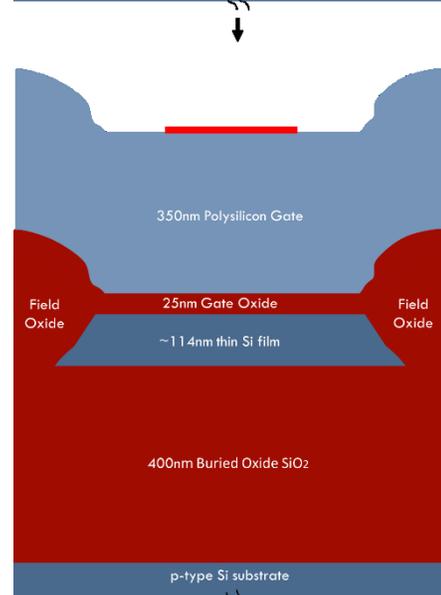
10. Gate P.E. **P.E.2**
- apply photoresist
- expose to light through mask



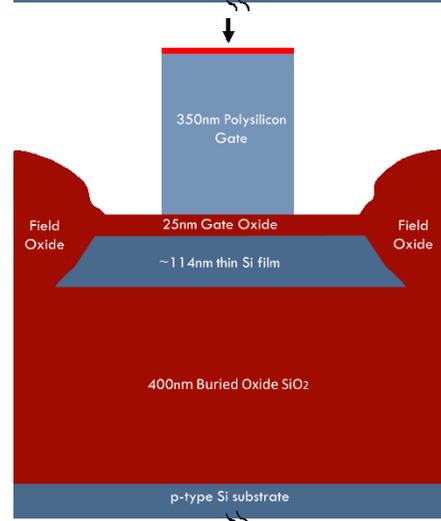
non-exposed photoresist is hardened



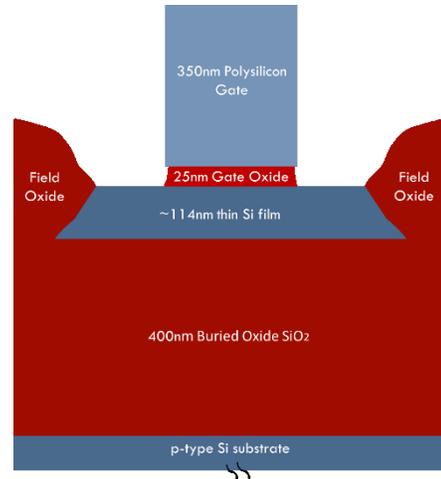
remove photoresist in non-protected areas



- etch polysilicon in non-protected areas
- strip photoresist



11. Source/drain oxide etchback



12. n+ Source/drain diffusion
diffuse phosphorous



4.2 Simulation versus Actual Fabrication Process Specifications

The process specifications for times, temperatures, and thicknesses described in the process flow in Section 4.1 are the values from Sentaurus simulations. During fabrication, the actual times for steps were determined from test runs, temperatures were set by the equipment accuracy, and thicknesses were measured. Table 4-1 summarizes the differences in processing steps between expected and actual values. Some of the columns have a “-” because the layer thickness was input into Sentaurus, where the deposit command did not request a time and temperature.

Table 4-1 – Differences between expected (from simulation) and actual fabrication times, temperatures, and thicknesses

Process Step (refers to run sheet)	Time [minutes]		Temperature [°C]		Thickness [nm]	
	Expected	Actual	Expected	Actual	Expected	Actual (approx.)
2. Pad Oxidation	31	18	950	940	20	19
3. Polysilicon Deposition	-	6.5	-	560	20	25
4. Nitride Deposition	-	26	-	820	160	166
6. Field Oxidation	65	65	950	940	280	284
8. Gate Oxidation	45	28	950	940	25	23
9. Polysilicon Gate Deposition	-	25	-	627	350	376

The dry oxidation time for the pad and gate oxides was very different than expected. The actual times were much lower than Sentaurus predicted which was unexpected. Originally it was assumed that the only issue with Sentaurus simulations were the boron diffusion models. However, the large difference in dry oxidation times does not give high confidence in Sentaurus’ dry oxidation models.

4.4 Test Arrays

To test this process, only nMOS devices were fabricated to confront the parasitic edge leakage in these devices not present in pMOS devices. A secondary intention was to try and fabricate transistor lengths down to $1.25\mu\text{m}$, where the shortest devices have been $2.5\mu\text{m}$ in past runs. Founded on these objectives, test arrays were created with varying widths and lengths. Enclosed geometry transistor arrays were also designed to test for the importance of edge effects. Van derPauw cross structures were created for sheet resistance monitoring for the device well and polysilicon layers. Lastly, the device pads were designed to be between $50\mu\text{m}$ - $100\mu\text{m}$ on a side to allow for direct probing into the device without metal and contact layers.

4.3.1 Basic FD SOI nMOSFET Test Arrays

Three basic FD SOI nMOS test arrays were designed to test this process. Each array had a different width to test narrow and wide devices. Varying lengths were duplicated on each of these three arrays to test for short and long devices. The device sizes in the arrays are found in Table 4-2. The width and length divisions were determined by the available lambda value specific to the mask generation equipment, where lambda was $1.27\mu\text{m}$.

Table 4-2 – Test array designed width and lengths.

Widths [μm]	Lengths [μm]
50.80 10.16 5.08	20.32
	15.24
	10.16
	7.62
	5.08
	3.81
	2.54
	1.27

To test for process variations across the wafers and in different orientations, the arrays were repeated multiple times throughout the die. This also made photolithography yield inconsequential if a few devices did not turn out as the devices were repeated. Finally, the devices were designed with only the device well and polysilicon layers, as probing for electrical characterization could be completed without taking the time to fabricate the contact, BPSG, and metal layers.

The three test arrays are shown in Figure 4-1, Figure 4-2, and Figure 4-3 where the lengths are found labelled underneath the devices. A complete view of the die is shown in Figure 4-4, which illustrates the position of the repeated transistor arrays and Van derPauw structures. Alignment markers for photolithography are also illustrated. The pads were designed to be 100 μm on a side for easier probing.

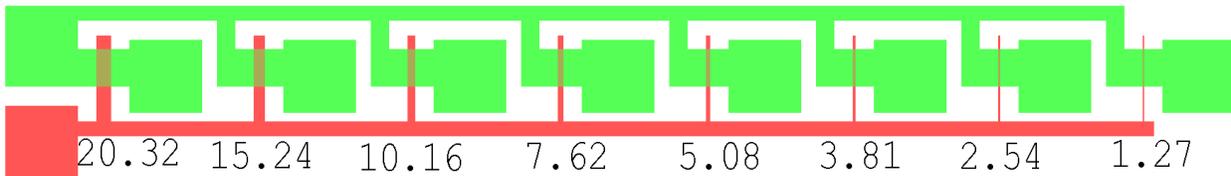


Figure 4-1 – Test array with a width of 50.80 μm

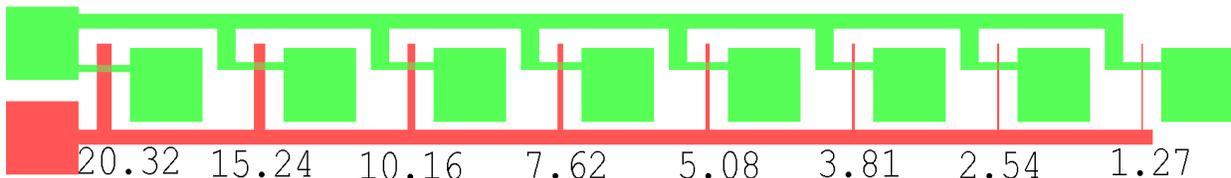


Figure 4-2 – Test array with a width of 10.16 μm

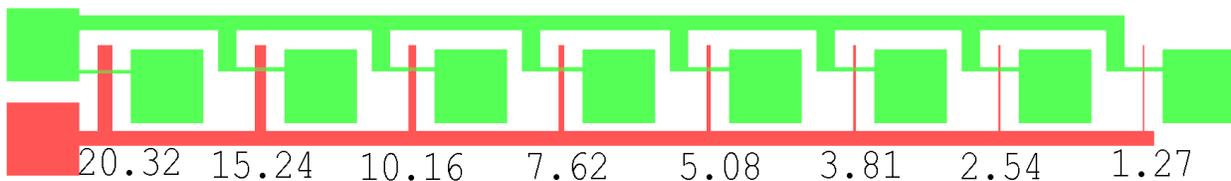


Figure 4-3 – Test array with a width of 5.08 μm



Figure 4-4 – Complete die with repeated test arrays, Van derPauw structures, and alignment markers

4.3.2 Enclosed Geometry Test Arrays

The issue of known leakage paths due to the bird's beak effect in thin gate oxide CMOS technologies is well known. A common approach to eliminate this leakage is to use the enclosed-gate geometry layout. An example of this layout is shown in Figure 4-5. The enclosed geometry layout is not efficient to use for all transistors in a circuit layout. Parametric variance in effective

and minimum widths and lengths, high use of layout area (need to be able to drop a probe into the centre terminal), and a higher input capacitance are some of the downfalls in using this style of device layout [34].

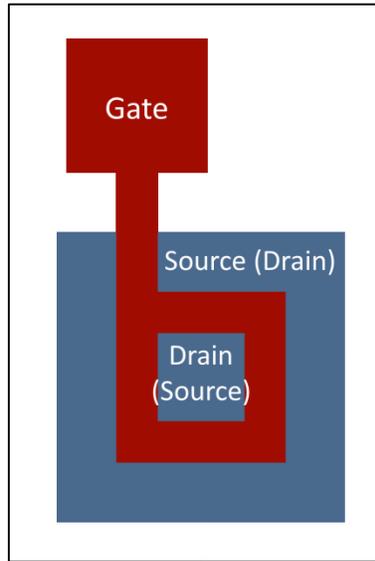


Figure 4-5 – Enclosed-geometry transistor layout

The enclosed geometry transistor theoretically should not be affected by boron loss, as the channel is fully controlled by the gate and there is no edge interfacing with the field oxide. If the kink seen experimentally in past FD SOI runs was due to boron loss at the device edge, then the enclosed geometry transistor should not have a kink. This makes the device a good baseline for what the device characteristics should look like if there was very little or no boron loss into the oxide or other geometrical edge effects. The enclosed geometry transistor test array designed to test in this process is shown in Figure 4-6.

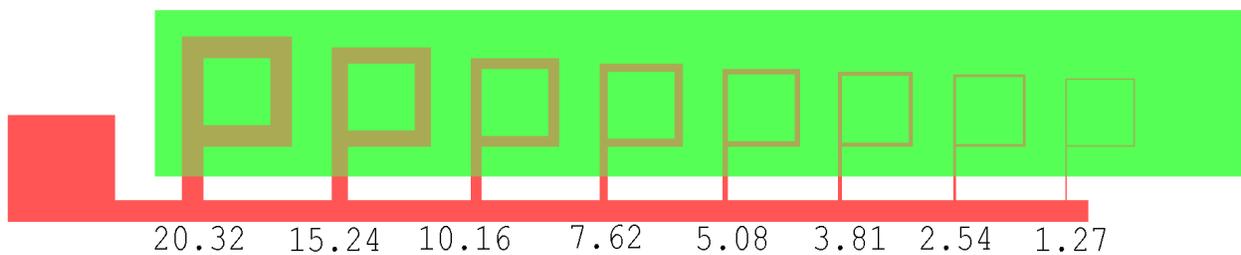


Figure 4-6 – Enclosed geometry test array

Chapter 5 Fabricated nMOSFET Testing and Analysis

Initial electrical testing results are shown in Figure 5-1, which demonstrated that the fully-depleted silicon-on-insulator fabrication run was successful in producing working nMOS transistors. Subthreshold leakage was still present, but was minimized compared to past FD SOI runs in the Carleton University Microfabrication Laboratory. Experimental threshold voltages and subthreshold swing values are within initial design specifications.

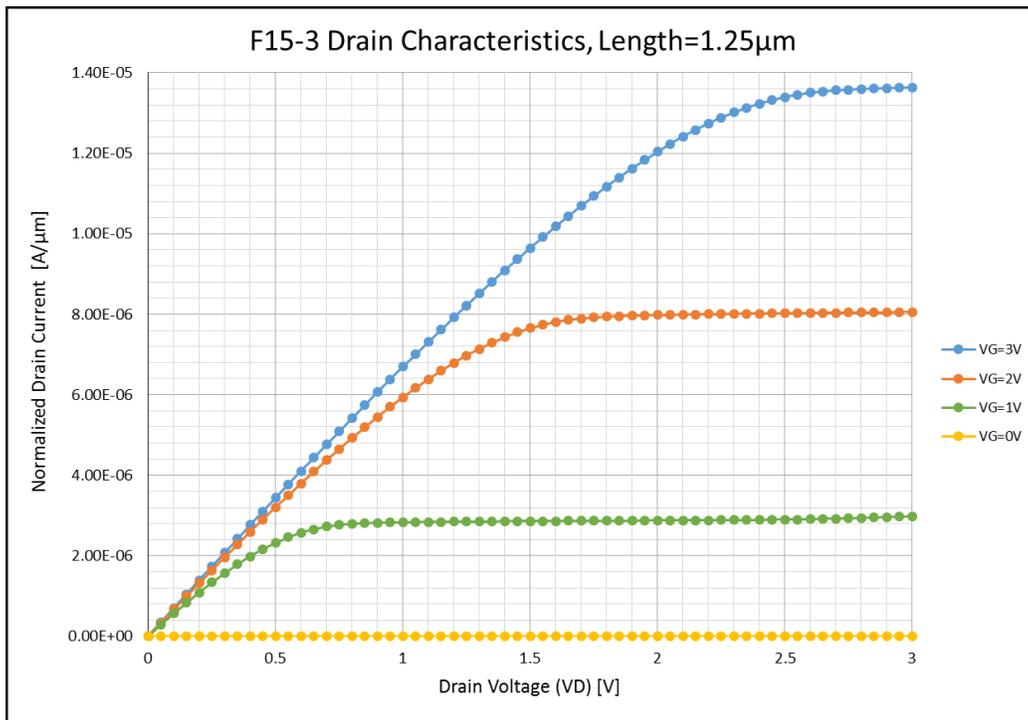


Figure 5-1 – Drain characteristics of a fabricated FD SOI nMOS transistor with no substrate bias

5.1 Enclosed Geometry Results

The enclosed geometry transistors were designed as a baseline for device characteristics without boron loss effects. An experimental subthreshold curve from an enclosed device with a nominal length of 5 µm is shown in Figure 5-2. Many curves were recorded, but all follow the trend of the plotted curve. The electrical characteristics from this data are found in Table 5-1. As expected, these devices did not have a kink in the subthreshold curve.

The threshold voltages found in Table 5-1 were extracted by Sentaurus using the ExtractVTgm function. This function plots the linear I_D vs. V_G characteristic and then extrapolates the curve back to find the V_G axis intercept. This extrapolation is done from the point of maximum transconductance.

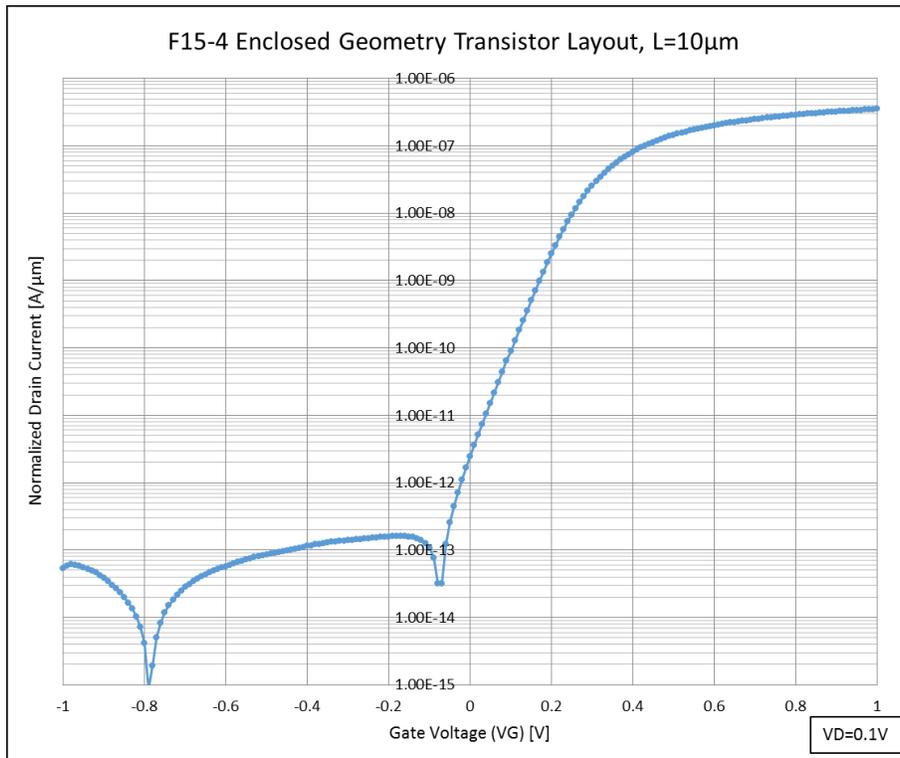


Figure 5-2 – Subthreshold curve from fabricated enclosed geometry nMOS transistor on wafer F15-4 with length of 10μm

Table 5-1 – Electrical characteristics extracted from the fabricated FD SOI nMOS enclosed geometry transistors

Wafer F15-	Nominal Length [μm]	Threshold Voltage [V]	Subthreshold Swing [mV/dec]	Normalized Subthreshold Leakage [nA/ $\mu\text{m}_{\text{width}}$]
1	1.25	0.24	65	0.263
	2.5	0.26	65	0.146
	3.8	0.27	65	0.096
	5	0.28	65	0.070
	7.5	0.29	65	0.049
	10	0.30	65	0.037
	15	0.31	65	0.027
	20	0.32	65	0.020
2	10	0.33	65	0.204
3	10	0.31	65	0.057
	20	0.33	65	0.032
4	7.5	0.29	65	0.004
	10	0.30	65	0.003
	15	0.31	65	0.002
	20	0.32	65	0.001

From the information above in the plot and table, the enclosed geometry transistors prove to serve as a favorable baseline for this FD SOI CMOS process. The subthreshold curve did not show evidence of a kink. The experimental subthreshold swing is nearly ideal for an FD SOI device at 65 mV/dec. The only downfall is that the subthreshold leakage is slightly higher than was anticipated. However, this is a result of the threshold voltage being low, particularly for the lighter film doping. Ideally this leakage would be in the pico- or fempto-amps rather than in the nano-amps (not normalized). Leakage can become a major issue when threshold voltages are already quite low.

5.2 Subthreshold Characteristics: Simulation versus Experimental Results

5.2.1 Subthreshold Characteristic Curves

Subthreshold curves were extracted from the fabricated FD SOI nMOS transistors. All data revealed the presence of a kink. This kink was believed to have resulted from edge boron loss, as there was no kink present in the enclosed geometry curves. Compared to curves from the past run, the kinks were not as severe. This meant that the boron loss, and therefore parasitic edge transistor leakage, has decreased with this newly designed process. An example of the resultant subthreshold curves is shown in Figure 5-3, where all extracted curves not presently shown have similar characteristic patterns.

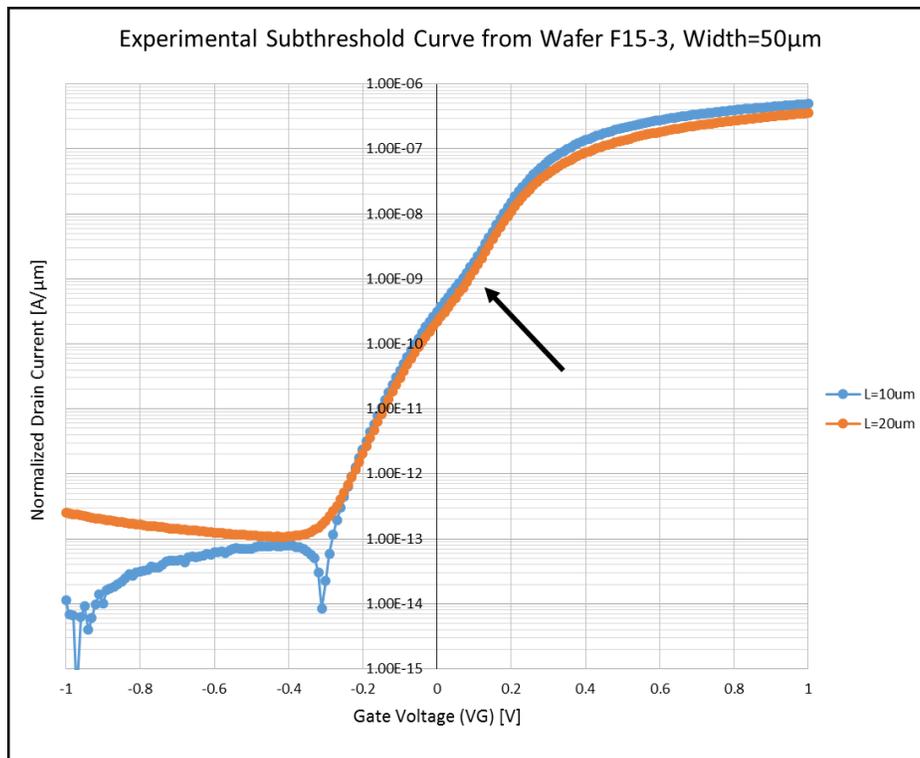


Figure 5-3 – Extracted FD SOI nMOS subthreshold curves from wafer F15-3, kink indicated by the arrow

As the enclosed geometry transistors were a baseline for a fabricated device in this run without boron loss effects, an enclosed geometry versus typical layout device subthreshold curve

was compared. This is shown in Figure 5-4. If there was no edge leakage current, the two curves would overlap. Instead, there is a red arrow indicating an evident sign of leakage current, where this gap would ideally be zero.

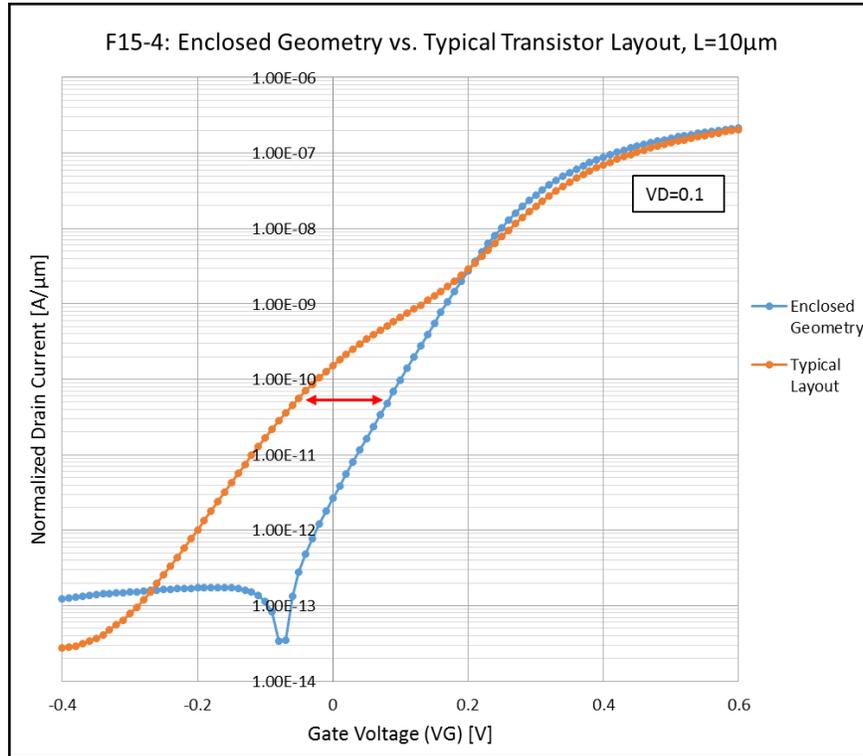


Figure 5-4 – Comparative plot of an enclosed geometry to typical layout device from wafer F15-4, normalized current (subthreshold leakage illustrated by red arrow)

5.2.2 Electrical Characteristics

Electrical characteristics were extracted from the experimental data, where data from all four wafers is found in Appendix C from selected devices. The data presented in the tables below is from wafer F15-4, which has the highest initial dose of boron in the silicon film. This data gives a general overview of the results of this FD SOI CMOS run in an attempt to minimize edge leakage current. The results from this wafer are closest to ideal, and will be used for further comparison and discussion. Table 5-2 is a general summary of the extracted electrical characteristics, and Table 5-3 and Table 5-4 compare the expected (simulated) versus the actual threshold voltages and subthreshold leakage currents.

Table 5-2 – Electrical characteristics extracted from the fabricated FD SOI nMOS devices on wafer F15-4

Nominal Width [μm]	Nominal Length [μm]	Threshold Voltage [V]	Subthreshold Swing [mV/dec]	Normalized Subthreshold Leakage [$\text{nA}/\mu\text{m}_{\text{width}}$]
5	10	0.38	112	1.368
20	5	0.34	92	0.675
	7.5	0.36	88	0.655
	10	0.38	76	0.428
50	1.25	0.31	86	0.666
	2.5	0.33	92	0.468
	3.8	0.34	82	0.508
	10	0.35	88	0.154
	15	0.36	92	0.108
	20	0.37	80	0.073

The results in Table 5-2 above show that the FD SOI nMOS devices had threshold voltages in the design specifications between 0.3-0.4V. Threshold voltages around 0.3V for these nMOS devices was ideal for the full CMOS process where $V_{Tn} = -V_{Tp}$. This relatively low threshold voltage is required to allow both nMOS and pMOS devices to be fabricated using the same boron-doped wells.

The subthreshold swing was much higher than expected, where the ideal value is around 60-65mV/dec. Sentaurus predicted a subthreshold swing value of 63mV/dec for wafer F15-4. The high subthreshold swing values are most likely the result of the parasitic edge transistor distorting the shape of the subthreshold I_D - V_{GS} characteristic. A higher leakage current when $V_G=0V$ results from a high subthreshold swing. The leakage current was also extracted and is shown in Table 5-2. Ideally the leakage current would be around 1pA per micron width, but the actual leakage currents from this run are in the nA range.

Table 5-3 – Comparison of expected vs. experimental threshold voltage data from the fabricated FD SOI nMOS devices on wafer F15-4

Nominal Width [μm]	Nominal Length [μm]	Expected Threshold Voltage [V]	Actual Threshold Voltage [V]	Difference Between Expected vs. Actual [mV]
5	10	0.281	0.38	99
20	5		0.34	39
	7.5		0.36	79
	10		0.38	39
50	1.25		0.31	29
	2.5		0.33	49
	3.8		0.34	59
	10		0.35	59
	15		0.36	79
	20		0.37	89

The results in Table 5-3 show that the actual threshold voltages were slightly higher than expected for this wafer, and are within design specifications. The expected thresholds may be low due to Sentaurus' overestimation of boron loss. It is noted that the threshold voltages of the shorter devices with lengths shorter than $5\mu\text{m}$ are lower than the other devices. This is due to short-channel effects, where the threshold shifts for short devices as shown in Equation 5-1 and Equation 5-2 [35, pp. 5,6]. For SOI, x_j refers to the silicon film depth.

Equation 5-1
$$V_{T0(\text{short-channel})} = V_{T0} - \Delta V_{T0}$$

Equation 5-2
$$V_{T0} = \frac{1}{C_{ox}} \cdot \sqrt{2q\epsilon_{Si}N_A|2\phi_F|} \cdot \frac{x_j}{2L} \cdot \left[\left(\sqrt{1 + \frac{2x_{dB}}{x_j}} - 1 \right) + \left(\sqrt{1 + \frac{2x_{dS}}{x_j}} - 1 \right) \right]$$

These equations show that as the length decreases, so too does the threshold voltage. A longer device will cause this change in threshold voltage to be very small compared to a shorter device. What occurs in a short-channel device to decrease the threshold voltage is due to the electric-field. The charges near the source and drain are terminated on the source and drain rather

than on the gate. The doping underneath the gate will therefore become reduced which in turn reduces the threshold voltage of the shorter device [36].

Table 5-4 – Comparison of expected vs. experimental subthreshold leakage data from the fabricated FD SOI nMOS devices on wafer F15-4

Nominal Width [μm]	Nominal Length [μm]	Expected Normalized Subthreshold Leakage [$\text{nA}/\mu\text{m}_{\text{width}}$]	Actual Normalized Subthreshold Leakage [$\text{nA}/\mu\text{m}_{\text{width}}$]	Difference Between Expected vs. Actual [$\text{nA}/\mu\text{m}_{\text{width}}$]
5	10	0.028	1.368	1.340
20	5	0.172	0.675	0.503
	7.5	0.124	0.655	0.531
	10	0.098	0.428	0.331
50	1.25	0.101	0.666	0.565
	2.5	0.069	0.468	0.399
	3.8	0.054	0.508	0.454
	10	0.025	0.154	0.129
	15	0.017	0.108	0.091
	20	0.013	0.073	0.060

The results in Table 5-4 illustrate the large amount of leakage current in the fabricated devices. The leakage current was expected to be tens to hundred times lower than actual values from simulations. Excess leakage current is due to the parasitic edge transistor, which has evidently formed in the fabricated devices.

Comparing normalized subthreshold leakage of the same lengths for different widths, it would be expected that a shorter device will leak more. The parasitic edge transistor affects a narrower device more than a wide device, as this edge transistor will dominate the device more. It is also expected that longer devices will have less leakage current for this same reason. Both theories prove true in the experimental data.

5.2.3 Cross-Section and Scanning Electron Microscope (SEM) Analysis

A sample from wafer F15-3C was prepared and observed using a SEM. This allowed measurements to be taken of the actual lengths and widths of the devices to be measured. The nominal 50 μ m wide device array was used for measurements. The actual lengths are found in Table 5-5. An example of the SEM images used to measure the actual device sizes is shown in Figure 5-5.

Table 5-5 – Nominal vs. actual lengths measured using a SEM

Nominal Length [μ m]	Actual Length [μ m]
1.25	2.74
2.5	4.00
3.8	5.14
5	6.34
7.5	8.80
10	11.2
15	16.2
20	21.4

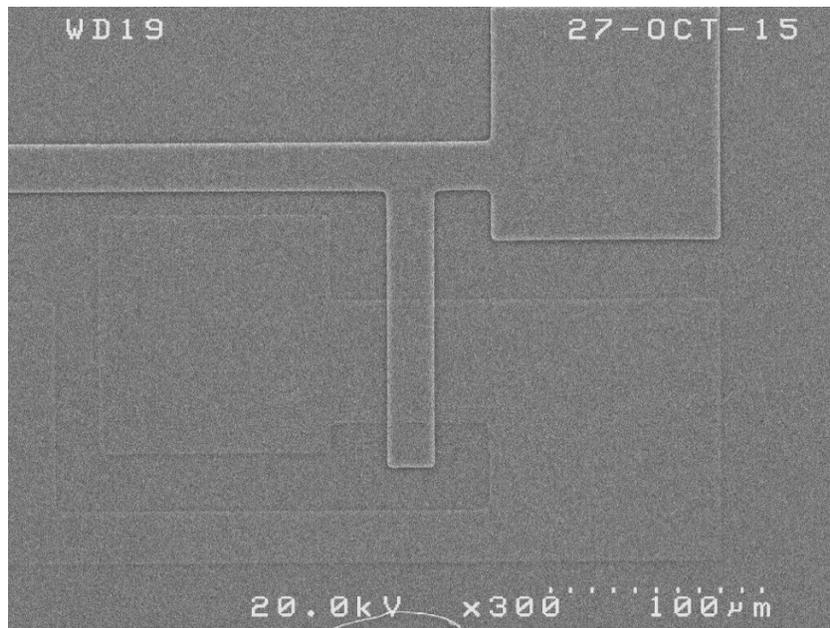


Figure 5-5 – Planar SEM image of nominal 50 μ m wide, 20 μ m long device

Wafer F15-3C was then cross-sectioned, polished and observed using a SEM. Pre-SEM observation, the sample was quickly dipped into a low concentration of BOE (buffered oxide etch)

in order for the oxide to be detected in the SEM. The SEM was used to observe the resultant device (shown in Figure 5-6) and poly-buffered LOCOS bird's beak. An image of this bird's beak is shown in Figure 5-8.

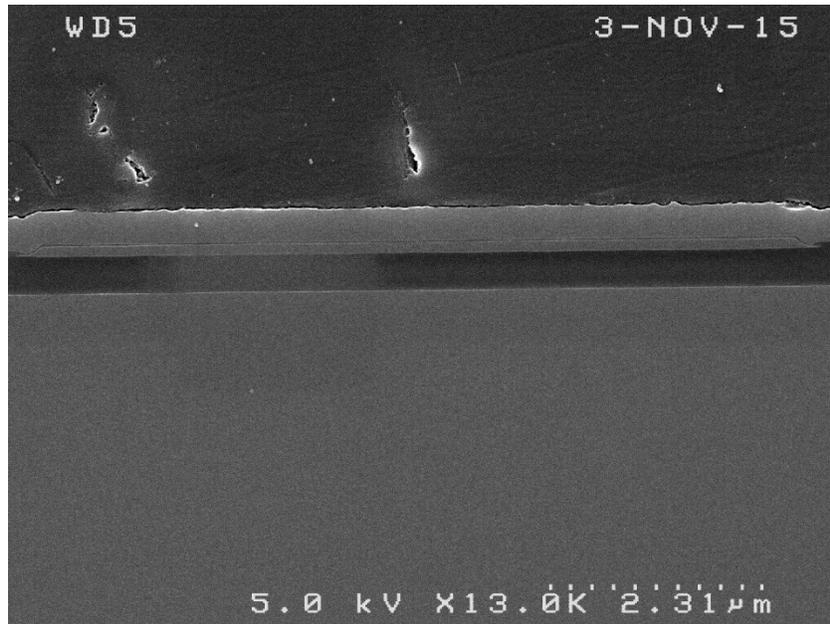


Figure 5-6 – SEM image of full fabricated device looking across the width

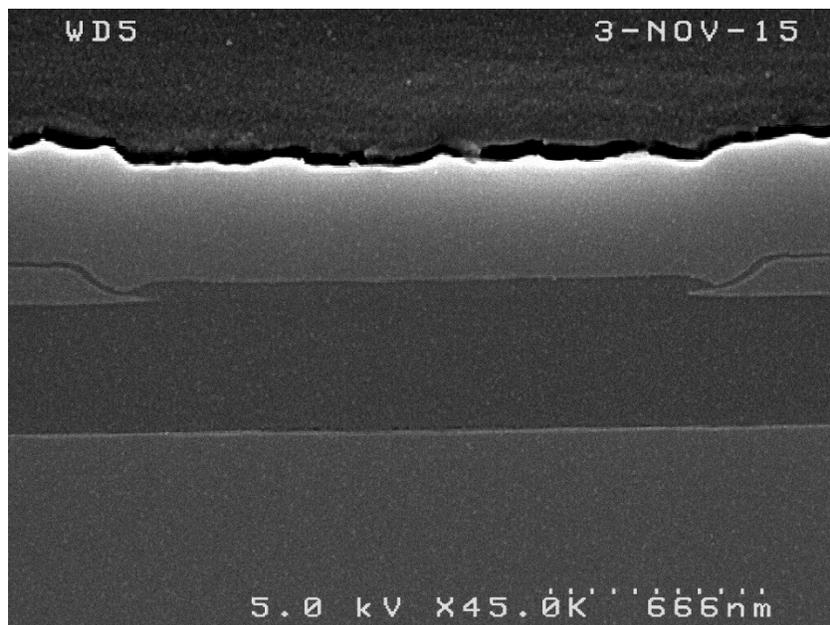


Figure 5-7 – SEM image illustrating an isolation around 1.88µm between devices

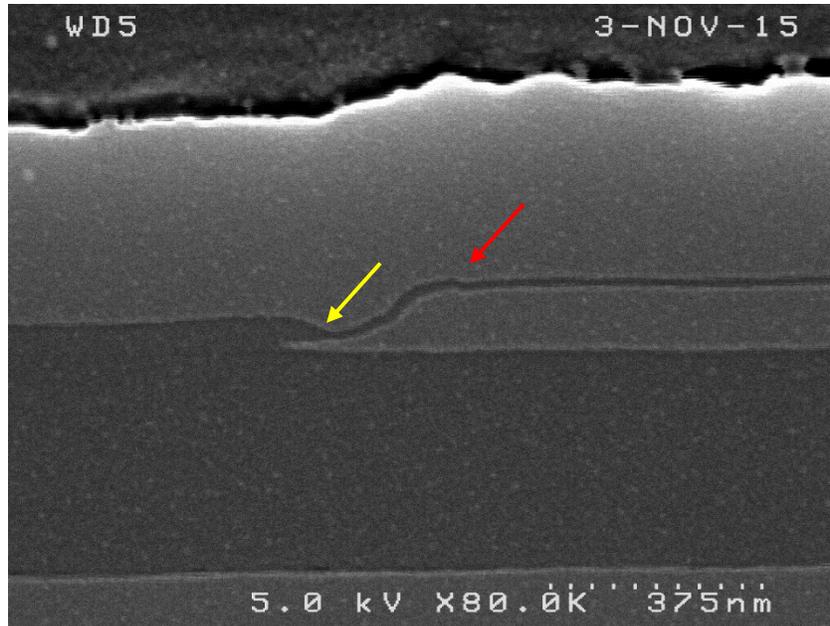


Figure 5-8 – Cross-section view of a fabricated FD SOI nMOS device isolated using PBL

The red arrow indicates a “bird’s crest” which is typical when using PBL. The yellow arrow indicates an effect much like that shown in Figure 3-37. This result illustrates the ‘bend’ in the film where the polysilicon in the LOCOS stack has helped to minimize the field oxide encroachment into the device.

Further observation of Figure 5-8 raised the question of why the polysilicon gate did not rise upward over the field oxide. Measurements were taken to try and determine what was happening in the device, shown in Figure 5-9. This determined that the field oxide had almost been etched away down to the buried oxide layer.

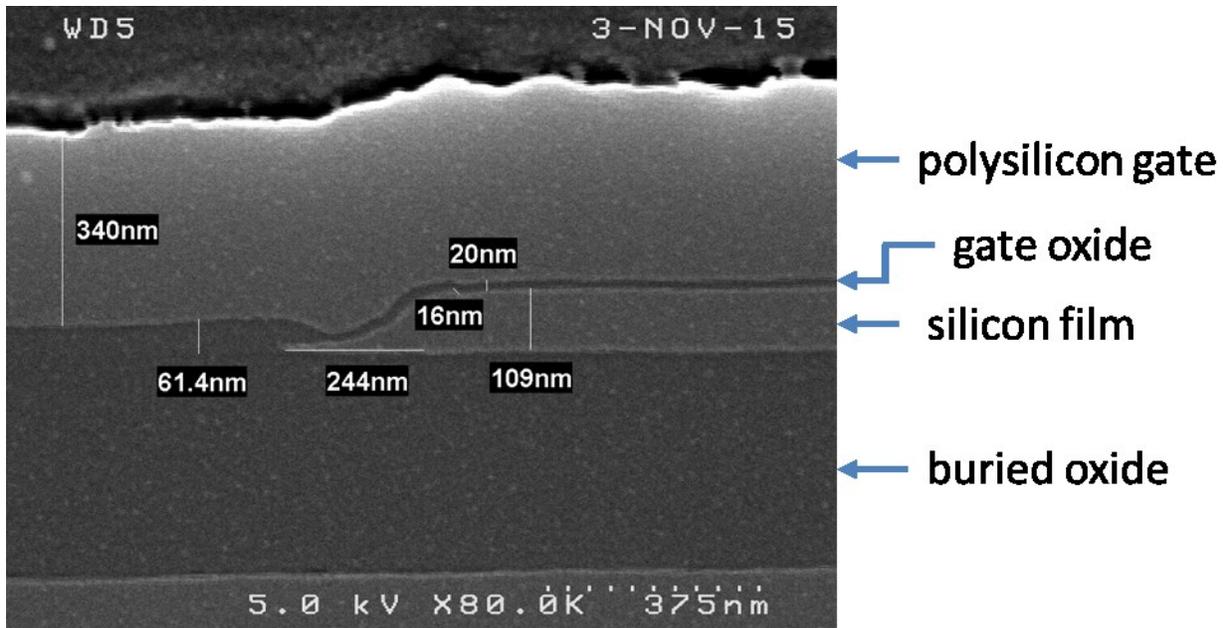


Figure 5-9 – Cross-section view of a fabricated FD SOI nMOS device isolated using PBL with measurements

Figure 5-9 shows the measured thicknesses for the different layers in the device. A comparison of designed versus actual thickness is found in Table 5-6. These results showed that around 120nm of field oxide was unexpectedly etched away during processing. It is also shown that Sentaurus overestimated the amount of consumed silicon film by the end of processing.

Table 5-6 – Designed vs. actual layer thicknesses in the fabricated FD SOI nMOS devices

Device Layer	Designed Thickness [nm]	Actual Thickness [nm]
field oxide	280	61.4
gate oxide	25	20
polysilicon gate	350	340
silicon film	98 (expected from Sentaurus)	109

To determine if this unexpected oxide etch was specific to this run or has occurred in past runs at Carleton University, devices from the first FD SOI run from 2014 were prepared and observed with a SEM. The resultant cross-section is shown in Figure 5-10.

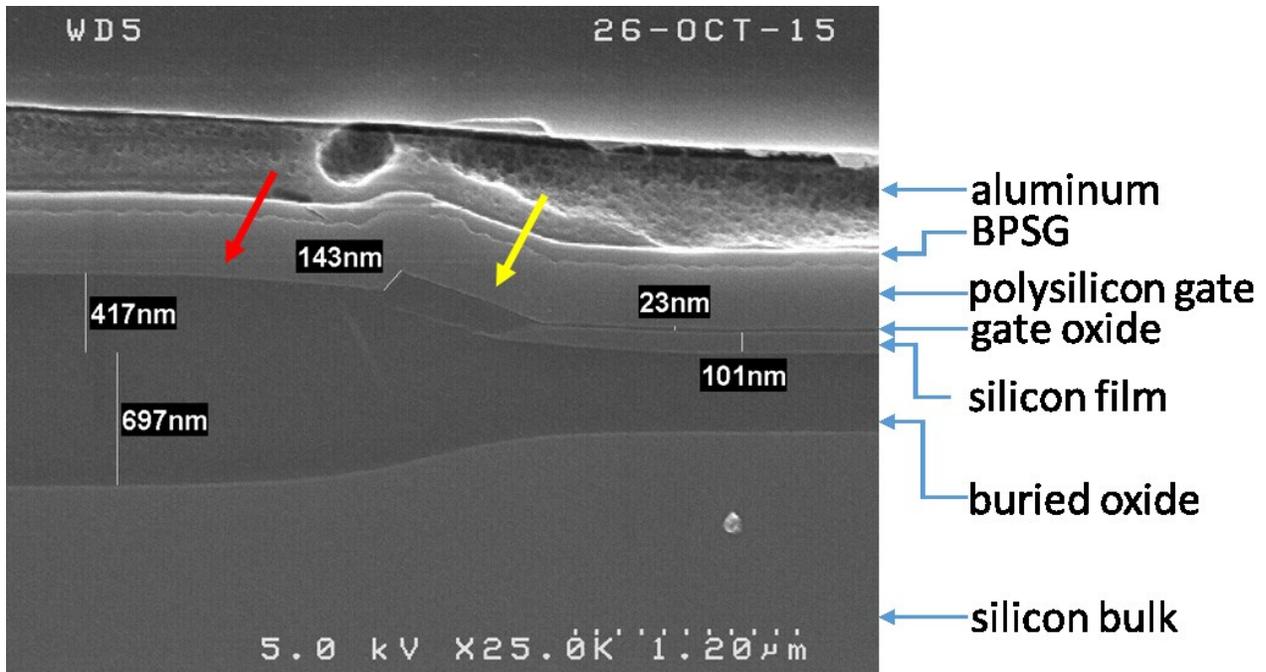


Figure 5-10 – Cross-section view of 2014 FD SOI device illustrating field oxide loss (red arrow)

The red arrow in Figure 5-10 shows the area where 143nm of field oxide has been lost when the LOCOS stack is stripped by a combination of converted nitride etch and nitride removal with the Technics. This is discussed in more detail below. However, the yellow arrow in Figure 5-10 shows a region where the field oxide has been largely protected by the LOCOS stack during the stack strip (at least until the end of the stripping process). This protected area is likely not found in the devices fabricated for this thesis seen in Figure 5-9 because the bird's beak is so narrow that the etching went laterally under the edge of the PBL stack. In the 2014 run, the bird's beak is almost a micron wide, and the lateral etching did not extend this far.

5.3 Discussion of Results

Results reveal that the fabricated FD SOI nMOS devices were successful in minimizing the amount of subthreshold leakage current, but not in eliminating it completely. Threshold voltages are within design specifications of between 0.3 and 0.4V for long channel devices. Full electrical characteristics of selected devices are summarized in tables in Appendix C. The resultant

subthreshold swing values were around 20mV/dec higher than the baseline fabricated enclosed geometry transistors which had an ideal subthreshold swing of 65mV/dec. The subthreshold leakage current was orders of magnitude larger than expected, which is a result of the parasitic edge transistors.

Figure 5-11 illustrates the difference in subthreshold leakage between the PBL and mesa isolated devices. The subthreshold leakage is found by comparing both curves to ideal devices in the form of enclosed geometry for PBL and with a “channel chop” eliminating the edge for the mesa isolated device. The improvement provided by the PBL process is apparent. The “channel chop” shown in Figure 5-12 is an additional fabrication step, where a new mask was produced to etch through the edges of the devices to eliminate the geometrical effect at the edge of the silicon film, thus eliminating the parasitic edge transistors. This is a solution that is not ideal, as it adds a fabrication step and can only be applied to larger devices which have a large enough active channel that the “chop” will still leave enough active device.

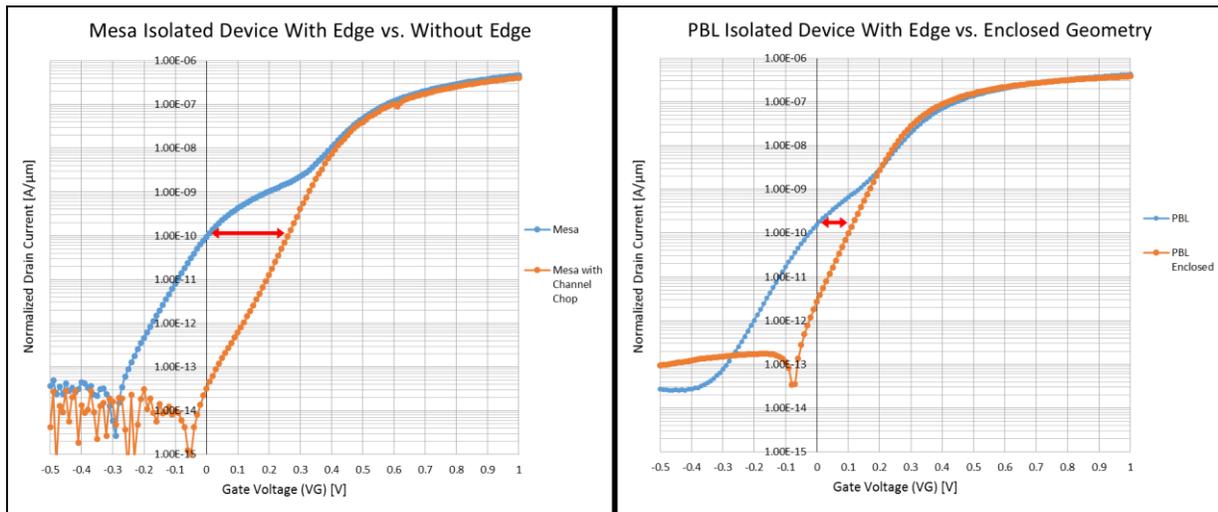


Figure 5-11 – Subthreshold leakage current difference between PBL and mesa devices (leakage shown with red arrow, larger is more leakage)

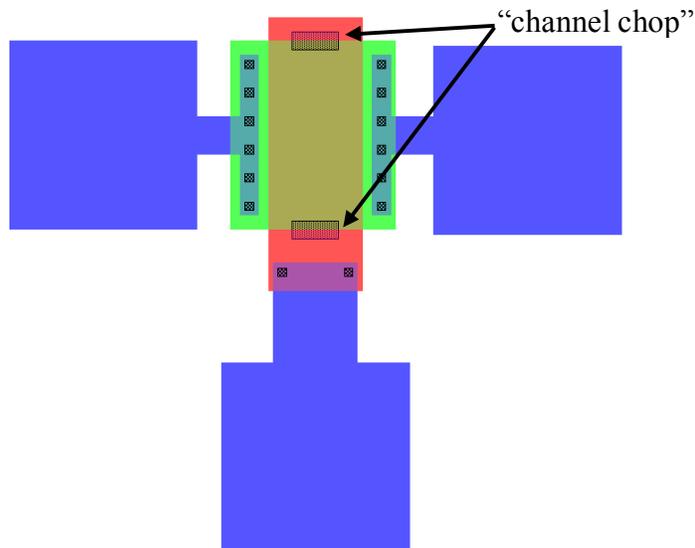


Figure 5-12 – “Channel chop” area to eliminate silicon film edge in mesa isolated devices from winter 2015 run

SEM images of the devices show that the loss of field oxide has led to less than ideal edge geometry. This also leads to an issue with the gate not having a large amount of oxide between it and the edge of the device, where a smaller t_{ox} determines that the parasitic edge transistor will have a lower threshold voltage than the main devices as described by Equation 2-2. This creates the kink seen in the subthreshold curve of the PBL devices, where the kink is evidence of the parasitic edge device turning on. Initially, the field oxide was grown to 284nm, but the final thickness was only 61.4nm. This unexpected loss of field oxide could have occurred in one or both of two different processing steps: stripping of the PBL stack and/or gate oxidation pre-clean.

The PBL stack removal begins with a 2 minute etch in 10% HF solution to remove the oxidized surface of the silicon nitride (so-called “converted nitride) in the device well. This etch is almost certainly excessive and, on the basis of measured etch rates for thermal oxide in 10% HF at 30nm/min, would be expected to remove approximately 60nm of the field oxide. The nitride and polysilicon are removed by etching in CF_4/O_2 plasma in a Technics Planar Etch II planar plasma etcher.

Etchers of this kind in general have poor selectivity; in the case of the process used at Carleton the etch rate for oxide is 24nm/min, polysilicon is 125nm/min, and nitride is 130nm/min (up from the 60nm/min etch rate recorded in 2013 due to changes in equipment behaviour). Thus, the etch rate for oxide is 19.2% of that for polysilicon and 18.5% for nitride. This could have resulted in the loss of an additional 40.6nm for F15-4, 40.6nm for F15-3, 38.6nm for F15-2, and 26.6nm for F15-1 of field oxide after etching through the 160nm of nitride and 20nm of polysilicon. The etch rate for nitride was assumed to be the same as 2013, resulting in too long of an etch in the Technics potentially leading to a loss of field oxide.

Finally, the pad oxide was etched in buffered HF for 5, 10, 20, and 40 seconds for wafers F15-4, F15-3, F15-2, and F15-1, respectively. This large variation in wet etch time was due to differences in remaining oxide thickness described by the dry etch time. Table 5-7 summarizes this point in direct correlation to this run.

Table 5-7 – Etch time differences between wafers in this FD SOI run during PBL stack removal after field oxidation

Wafer	Initial Film Doping [cm-2]	Technics Dry Planar Etch Time to Remove PBL Stack Nitride and Polysilicon (step 7B) [sec]	Wet Etch in 10% HF Time to Remove PBL Stack Pad Oxide (step 7C) [sec]	Total Etch Time [sec]
F15-1	1.3e12	150 (60+60+30)	40	190
F15-2	1.2e12	180 (60+60+60)	20	200
F15-3	1.0e12	185 (60+60+25+25+15)	15	200
F15-4	1.4e12	185 (60+60+15+35+15)	5	190

The buffered oxide etch solution is comprised of a 6:1 volume ratio of 40% ammonium fluoride (NH₄F) in water to 49% HF in water [37]. The etch rate for thermal oxide in buffered HF is 2 nm/sec, so this step could give an additional field oxide loss of 10nm for F15-4, 20nm for F15-

3, 40nm for F15-2, and 80nm for F15-1. In principle, this loss should not affect the critical bird's beak region, since this region is covered by the stack until the very end of the etch process. However, in the PBL process, the bird's beak is deliberately kept narrow, and all the etch processes used are either completely or nearly isotropic. This means etching can proceed laterally into the bird's beak region.

The gate oxidation pre-clean is a standard "RCA clean" [38]. Part of this clean involves the removal of residual oxide by immersion in 1% HF for about 15 seconds at room temperature. The etch rate of 1% HF is around 2-4 nm/min for thermal oxide [38], so a 15 second exposure would only remove around 1nm of oxide. This is far less than the observed field oxide loss.

Overall, the FD SOI CMOS process designed for this thesis was successful. Threshold voltages were within design specifications. The subthreshold swing was higher than expected due to the parasitic edge transistors present in the devices. These parasitic edge transistors also caused a higher leakage current than expected. If the field oxide had not unexpectedly been etched almost completely down to the buried oxide, it is believed that the experimental results would have matched expected results. Thus, this process would have been successful in eliminating the SOI nMOS edge leakage, but instead has simply reduced it.

Chapter 6 Conclusions and Future Work

6.1 Conclusions

The goal of this project was to develop a process capable of producing fully depleted SOI nMOSFETs with sufficient well doping to give threshold voltages of 0.3 to 0.4V but without edge leakage effects, so that the transistors would shut off completely at zero gate bias. The relatively low threshold voltage is required to allow both nMOS and pMOS transistors to use the same boron-doped wells. The process had to be simple enough to be useful in fabrication of designs for the ELEC4609 course. In particular, additional field threshold adjust implants could not be introduced.

Extensive Sentaurus simulations predicted that a carefully designed minimal thermal budget poly-buffered LOCOS isolation could eliminate the two-part nMOS subthreshold kink and edge leakage problems found in previous runs of the Carleton University Microfabrication Laboratory FD SOI process. Comparison of Sentaurus predictions to experimentally measured characteristics from the 2014 LOCOS run devices strongly suggest that Sentaurus overestimates the boron loss during processing. This gave high confidence in this designed process giving even lower boron loss and thus the minimization of subthreshold kink and leakage when implemented experimentally.

The designed process was successful in suppressing subthreshold kinks and edge leakage below the levels achieved in any previous FD SOI CMOS run at Carleton. With appropriate p-well implant dose resultant threshold voltages were within design specifications. Unfortunately, due to the unexpected loss of field oxide, the process did not completely eliminate the subthreshold edge leakage current. The processing step or steps where this field oxide loss occurred is still not known, and will be investigated in the future. This loss of field oxide caused the bird's beak region

to appear more like a mesa edge rather than the desired wedge-shaped field oxide expected from poly-buffered LOCOS. However, the channel edge was sharper than results from past runs using conventional LOCOS isolation, which is an advantage in suppressing subthreshold edge leakage.

6.2 Future Work and Optimization for Future Runs

This process will be re-run in the winter 2015 ELEC4609 run in the Carleton University Microfabrication Laboratory. Precision optical oxide thickness measurement with a Nanometrics NanoSpec/AFT and ellipsometry will be used to monitor field oxide thickness at each step throughout processing so that the sources of field oxide loss can be identified and eliminated. Test structures with very long channel regions will be included to facilitate SEM imaging, which has proven to be extremely useful in identifying the causes of excess edge leakage. The long structures will allow the preparation of SEM samples by simply cleaving along the width of the device near the centre of the gate, avoiding the need for labour intensive polishing.

The simulation and experimental results obtained so far give every reason for confidence that the designed process will eliminate the subthreshold kink and leakage if the field oxide does not get etched away in future runs. The process is simple enough to be implemented within the constraints of ELEC4609 fabrication. This allows for only five mask levels and a single ion implant to achieve full CMOS.

Appendix A:

FD SOI nMOS Sentaurus Process Input File

#Step 1 - Initial SOI Wafer

##-----

#F15-1, 114nm, 1.3e13cm-2

#F15-2, 116nm, 1.2e12cm-2

#F15-3, 116nm, 1.0e12cm-2

#F15-4, 110nm, 1.4e12cm-2

#Initial 2D Grid

#if [string match @SOIWafer@ "1"]

x lines

line x location=0.0<nm> spacing=20<nm> tag=ThinFilmSiTop

line x location=(@film@-2)<nm> spacing=20<nm> tag=BuriedOxideTop

line x location=((@film@-2)+395)<nm> spacing=2.0<um>

tag=SiBaseTop

line x location=((@film@-2)+5395)<nm> spacing=2.0<um>

tag=SiBaseBottom

#Assumed that the Si Base thickness is 5um

#elseif [string match @SOIWafer@ "2"]

x lines

line x location=0.0<nm> spacing=20<nm> tag=ThinFilmSiTop

line x location=(@film@)<nm> spacing=20<nm> tag=BuriedOxideTop

line x location=((@film@)+395)<nm> spacing=2.0<um>

tag=SiBaseTop

line x location=((@film@)+5395)<nm> spacing=2.0<um>

tag=SiBaseBottom

#Assumed that the Si Base thickness is 5um

#elseif [string match @SOIWafer@ "3"]

x lines

line x location=0.0<nm> spacing=20<nm> tag=ThinFilmSiTop

line x location=(@film@)<nm> spacing=20<nm> tag=BuriedOxideTop

line x location=((@film@)+395)<nm> spacing=2.0<um>

tag=SiBaseTop

line x location=((@film@)+5395)<nm> spacing=2.0<um>

tag=SiBaseBottom

#Assumed that the Si Base thickness is 5um

#elseif [string match @SOIWafer@ "4"]

x lines

line x location=0.0<nm> spacing=20<nm> tag=ThinFilmSiTop

```

line x location=(@film@-6)<nm> spacing=20<nm> tag=BuriedOxideTop
line x location=((@film@-6)+395)<nm> spacing=2.0<um>
tag=SiBaseTop
line x location=((@film@-6)+5395)<nm> spacing=2.0<um>
tag=SiBaseBottom
#Assumed that the Si Base thickness is 5um
#endif

# y lines
line y location=0.0<nm> spacing=150<nm> tag=Y_Middle
line y location=6.0<um> spacing=150<nm> tag=Y_Right

#Initial Domains

#Start with SOI wafer with a Si base of unknown depth, followed
#by a 400nm BOX layer of SiO2 and lastly 280nm epitaxial silicon film.

#Si Film
#region Silicon concentration=1e+15<cm-3> field=Boron \
region Silicon concentration=0<cm-3> field=Phosphorus \
xlo=ThinFilmSiTop xhi=BuriedOxideTop ylo=Y_Middle yhi=Y_Right
#SiO2 Insulator
region Oxide xlo=BuriedOxideTop xhi=SiBaseTop ylo=Y_Middle yhi=Y_Right

#Si Base
region Silicon concentration=1e+15<cm-3> field=Boron \
xlo=SiBaseTop xhi=SiBaseBottom ylo=Y_Middle yhi=Y_Right

#Initialize structure
init

# Recommended in all projects
AdvancedCalibration
math coord.ucs

# Recommended for 3D projects
pdbSet Mechanics EtchDepoRelax 0

#mgoals normal.growth.ratio=2.0 min.normal.size=0.002
#June 10: Initializing with finer meshing
#July 3: size was 0.000001 but too small
mgoals normal.growth.ratio=2.0 min.normal.size=0.002
grid remesh

```

```

#Step 2 - Thinning Si Film by Oxidation
##-----
#Fake Deposit to get 2d plots working
  deposit material= {Nitride} type=isotropic time=1 rate= {0.05}
  mask name=FakeMask left=-1 right=2.9<um>
  etch material= {Nitride} type=anisotropic time=1 rate= {0.06} mask=FakeMask
  etch material= {Nitride} type=anisotropic time=1 rate= {0.06}

#split FilmImplant
#####

#Step 3 - Grow Mask Oxide for Implant
##-----
  diffuse O2 temperature=950<C> time=10<min>

  struct tdr=n@node@_S3_PadO2Implant

#Step 4 - Initial Film Implant
##-----
#if [string match @FilmImplant@ "1"]

  implant Boron dose=(@dose@)<cm-2> energy=18<keV>

#elseif [string match @FilmImplant@ "2"]

  implant Boron dose=((@dose@)-(0.1e+12))<cm-2> energy=18<keV>

#elseif [string match @FilmImplant@ "3"]

  implant Boron dose=((@dose@)-(0.2e+12))<cm-2> energy=18<keV>

#elseif [string match @FilmImplant@ "4"]

  implant Boron dose=((@dose@)-(0.4e+12))<cm-2> energy=18<keV>

#endif

#Remove Oxide grown in step 3
  etch material= {Oxide} type=isotropic time=1 rate= {0.1}

  struct tdr=n@node@_S4_InitialFilmImplant

```

```

#split DeviceIsolation
#####
#Step 6 - Pad Oxide Growth
##-----
#if [string match @DeviceIsolation@ "1"]

    diffuse O2 temperature=955<C> time=31<min>

#elseif [string match @DeviceIsolation@ "2"]

    diffuse O2 temperature=955<C> time=18<min>

#endif

#split PBL
#####
#Step 6a - Poly-Buffered LOCOS Polysilicon Deposition
##-----
    deposit material= {PolySilicon} type=isotropic time=1 rate= {0.0255}

#Step 7 - Deposit Silicon Nitride for LOCOS
##-----
    deposit material= {Nitride} type=isotropic time=1 rate= {0.1663}

#split LOCOS
#####
#Step 8 - PE1: Mask and Etch Silicon Nitride for LOCOS
##-----
mask name=LOCOS_Nitride left=-1 right=5<um>
etch material= {Nitride} type=anisotropic time=1 rate= {0.2} mask=LOCOS_Nitride
etch material= {Polysilicon} type=anisotropic time=1 rate= {0.026} mask=LOCOS_Nitride
etch material= {Oxide} type=anisotropic time=1 rate= {0.025} mask=LOCOS_Nitride

    struct tdr=n@node@_S8_Si3N4

#Step 9 - Field Oxide Growth for LOCOS
##-----
    refinebox min= {0.0 1.4} max= {0.25 2.50} \
        xrefine= {0.05} yrefine= {0.05} all add

    grid remesh

    diffuse H2O temperature=950<C> time=65<min>

    struct tdr=n@node@_S9_FieldOxide

```

```

#split EtchSiNOx
#####
#Step 10 - Etch Silicon Nitride and Pad Oxide
##-----
#Global Mesh Settings for automatic meshing in newly generated layers

    #mgoals normal.growth.ratio=2.0 min.normal.size=0.002
    #this left the electrical sims to be 19+ hours...change to 0.02
    mgoals normal.growth.ratio=2.0 min.normal.size=0.02
    grid remesh

#Remove Silicon Nitride
    strip nitride
    struct tdr=n@node@_S10a_IsolationRemoveNitride

#Remove Polysilicon
    etch material= {Polysilicon} type=anisotropic time=1 rate= {0.026}

    struct tdr=n@node@_S10b_IsolationRemovePolysilicon

#Remove Pad Oxide
    etch material= {Oxide} type=anisotropic time=1 rate= {0.025}

    struct tdr=n@node@_S10c_Isolation

#split PolyGate
#####
#Step 11 - Grow Gate Oxide
##-----
#if [string match @PolyGate@ "1"]

    diffuse O2 temperature=955<C> time=45<min>

#elseif [string match @PolyGate@ "2"]

    diffuse O2 temperature=955<C> time=28<min>

#endif
    #ideal gate oxide is 25nm

#Step 12 - Deposit Polysilicon Gate
##-----
deposit material= {PolySilicon} type=isotropic time=1 rate= {0.3765} species=phosphorus
concentration=1e21<cm-3>

```

```

#Step 19 - Anneal MOS Well Implants
##-----
diffuse temperature=900<C> time=10<min>

struct tdr=n@node@_S19_MOSAnneal

#split MOSWell
#####
#Step 19 - Anneal MOS Well Implants
##-----
# diffuse temperature=900<C> time=10<min>

# struct tdr=n@node@_S19_MOSAnneal

#split ToSDevices
#####

#Prepare Structure for Sentaurus Devices
#Transform Half Structure to Full Structure
##-----
#transform sweep back
# z lines
line z location= 0 spacing=200<nm> tag= front
line z location= 2.5<um> spacing=200<nm> tag= back

transform reflect back
struct tdr= n@node@_A

#split Contacts
#####
#Defining Contacts
##-----
mask name=PolyMask left=0 right=6 front=2.495 back=-2.495
mask name=PolyMaskNegative left=0 right=6 front=2.495 back=-2.495 negative

etch material= {Polysilicon} type=anisotropic time=1 rate= {0.425} mask=PolyMask

etch material= {Oxide} type=anisotropic time=1 rate= {0.180} mask=PolyMask
implant Phosphorus dose=1e15<cm-2> energy=20<keV>
diffuse temperature=950<C> time=0.2<min> N2

#Seems like xlo/xhi is actually the y parameters and
#ylo/yhi are actually the x parameters

contact box PolySilicon adjacent.material= Gas \

```

```

        ylo=0 yhi=0.5 xlo=-0.4 xhi=-0.02 zlo=-2.5 zhi=2.5 name="gate"

contact box Silicon adjacent.material= Oxide \
        ylo=0 yhi=5.0 xlo=0.0 xhi=0.2 zlo=2.49 zhi=2.51 name="Drain"

contact box Silicon adjacent.material= Oxide \
        ylo=0 yhi=5.0 xlo=0.0 xhi=0.2 zlo=-2.49 zhi=-2.51 name="Source"

contact bottom name= "backGate"

struct tdr= n@node@_B

#Remeshing for Sentaurus Devices
##-----
struct tdr= n@node@_NoMesh

# remeshing for device simulation
pdbSet Grid SnMesh DelaunayType boxmethod

refinebox interface.mat.pairs= {Silicon Oxide} \
        min= {0.078 -2 0} max= {0.4 2 1} \
        #try min normal size at 0.02?
        min.normal.size= 0.2 normal.growth.ratio= 1.5
grid remesh

struct tdr= n@node@

```

Appendix B:

Summer 2015 FD SOI nMOS Run Sheet

SOI NMOS PROCESS -Aug 14 2015

STARTING MATERIAL: 100mm SOITEC wafer quarters, 280nm Si/400nm BOX Lot 4974-4037
F15-1C, F15-2C, F15-3C, F15-4C
Film already thinned to ~116nm
Film Doping $^{11}\text{B}+$ 18keV dose $1.4\text{e}12\text{cm}^{-2}$
Film Doping $^{11}\text{B}+$ 18keV dose $1.3\text{e}12\text{cm}^{-2}$
Film Doping $^{11}\text{B}+$ 18keV dose $1.2\text{e}12\text{cm}^{-2}$
Film Doping $^{11}\text{B}+$ 18keV dose $1.0\text{e}12\text{cm}^{-2}$
All test wafers are bulk p-type 1-10 Ωcm

Outline:

1. LEVEL ZERO P.E. AND ETCH
2. **PAD OXIDATION 950C 31min dry 20nm**
3. POLYSILICON DEPOSITION
4. NITRIDE DEPOSITION
5. DEVICE WELL P.E.
6. **FIELD OXIDATION 950C 65min wet**
7. NITRIDE, POLYSILICON, AND PAD OXIDE REMOVAL
8. **GATE OXIDATION 950C 45min dry**
9. POLYSILICON GATE DEPOSITION
10. GATE P.E. AND ETCH
11. SOURCE/DRAIN OXIDE ETCHBACK
12. SOURCE/DRAIN DIFFUSION

1. METROLOGY AND SCRIBE CLEARING ETCH Mask CU-325-00

- a) PlasmaPreen condition, HMDS oven,
apply S1811 photoresist, prebake, expose,
develop, postbake, **descum** See appendix A

- b) etch screen oxide
etch in buffered HF until screen oxide removed
estimated etch time: 30 sec

- c) plasma etch Si film (Technics Planar Etch II)
power: 100 W source gas: freon/5%O₂
pressure: 0.3 Torr
estimated etch time: 1 min 50 sec
actual etch times: 1 min 50 sec

- d) Etch buried oxide in buffered HF until substrate exposed (expect hydrophobia)
actual etch times: 5 min

- e) strip PR in PlasmaPreen
actual etch times: 5+5+5 min

2. PAD OXIDATION

Apex recipe# _____ Apex Run# _____

- a) RCA clean

- b) Oxidation tube temperature 950°C (must use this temperature)

5 min preheat	O ₂
2" every 6 sec push	O ₂
31 min oxidation	dry O ₂
2" every 15 sec pull	N ₂
10 min cool	N ₂

include test wafers

target thickness: 20 nm

thickness measured on centre wafer:	F15-1 – 19.6 nm
	F15-2 – 19.1 nm
	F15-3 – 18.8 nm
	F15-4 – 18.9 nm

3. POLYSILICON DEPOSITION Tymcon recipe 0

include test wafer

Deposition

tube temperature: 560°C

deposition time: 6.5 min

target thickness: 20 nm

poly thickness measured on test wafer: avg. 29 nm

4. NITRIDE DEPOSITION

Apex recipe# _____ Apex Run# _____

include test wafer

LPCVD tube temperature: 820°C

deposition time: 26 min

target thickness: 160 nm

actual thickness: ~166 nm

5. DEVICE WELL P.E.**Mask CU-325-01**

- a) PlasmaPreen condition, HMDS oven, apply S1811 photoresist, prebake, expose, develop, postbake, **descum**
(See Appendix A for standard photoresist procedure)

- b) plasma etch nitride and polysilcon (Technics Planar Etch II) (160nm and 20nm)
 - power: 100 W source gas: freon/5%O₂
 - pressure: 0.3 Torr

 - estimated etch time: 60+60 sec

 - actual etch times: F15-1 – 60+60+26 sec
 F15-2 – 60+60+50 sec
 F15-3 – 60+60+30 sec
 F15-4 – 60+60+40 sec

BE EXTREMELY CAREFUL NOT TO OVERETCH AND CUT THROUGH Si FILM

- c) strip PR in PlasmaPreen

- d) remove pad oxide (20nm)
 - etch in buffered HF until pad oxide removed from field regions
 - estimated etch time: 30 sec
 - actual etch time:

6. FIELD OXIDATIONApex recipe# Q0002 Apex Run# _____

include test wafer label as F15-FOXC

- a) RCA clean

- b) Oxidation tube temperature 950°C (must must this temperature)
 - 5 min preheat O₂
 - 2" every 6 sec push O₂
 - 10 min oxidation dry O₂
 - 65 min oxidation O₂ + pyrogenic H₂O
 - 2" every 15 sec pull N₂
 - 10 min cool N₂

target thickness: 280 nm
thickness measured on test wafer: 284 nm

7. NITRIDE, POLYSILICON, AND PAD OXIDE REMOVAL

a) remove converted nitride

etch in 10% HF until oxide removed from top of nitride

estimated etch time: 2 min

actual etch times:

b) remove nitride and polysilicon (Technics Planar Etch II) (160nm and 20nm)

power: 100 W source gas: freon/5%O₂

pressure: 0.3 Torr

estimated etch time: 3 min

actual etch times: F15-1 – 60+60+30 sec

F15-2 – 60+60+60 sec

F15-3 – 60+60+25+25+15 sec

F15-4 – 60+60+15+35+15 sec

BE EXTREMELY CAREFUL NOT TO OVERETCH AND CUT THROUGH Si FILM

c) remove pad oxide (20nm)

etch in buffered HF until
oxide removed from device wells

estimated etch time: 20 sec (to hydrophobia)

actual etch times: F15-1 – 40 sec

F15-2 – 20 sec

F15-3 – 15 sec

F15-4 – 5 sec

8. GATE OXIDATIONApex recipe#Q0047 Apex Run# _____

include test wafer (bare silicon)

a) RCA clean (remove residual screen oxide)

b) Oxidation tube temperature 950°C (must use this temperature)

5 min preheat	O ₂	
2" every 6 sec push	O ₂	
45 min oxidation	O ₂	(actual time 28 min)
20 min anneal	N ₂	
2" every 15 sec pull	N ₂	
10 min cool	N ₂	

target thickness: 25 nm

thickness measured on test wafer: 23nm

9. POLYSILICON GATE DEPOSITION Tymcon recipe 0

include test wafer (Gate oxide)

Deposition

tube temperature: 627°C

deposition time: 25 min

target thickness: 0.35 μm

poly thickness measured on test wafer: 0.376 μm

10. GATE P.E. Mask CU-325-02

- a) PlasmaPreen condition, HMDS oven,
 apply S1811 photoresist, prebake, expose,
 develop, postbake, **descum** See appendix A

- b) plasma etch gate using Technics Planar Etch II planar plasma etcher

 CF₄/O₂ 100 W 0.3 Torr

 estimated etch time: 2 min

 actual etch times:

BE EXTREMELY CAREFUL NOT TO OVERETCH AND CUT THROUGH Si FILM

- c) strip PR in PlasmaPreen

 actual time: 5+5+5 min

11. SOURCE/DRAIN OXIDE ETCHBACK

etch in buffered HF @20°C until Si exposed in source/drain windows

 estimated etch time: 50 sec

 actual etch times: 30 sec (10% HF)

12. N+ SOURCE/DRAIN DIFFUSION Apex recipe#_O0002_Apex Run#_____

a) RCA clean

b) predeposition source: POCl_3 @20°C tube temperature: 950°C

5 min preheat	N_2+O_2
30 sec push	N_2+O_2
5 min warm-up	N_2+O_2
5 min dope	$\text{N}_2+\text{O}_2+\text{N}_2/\text{dopant}$
10 min hold	N_2+O_2
15 sec pull	N_2+O_2
5 min cool	N_2+O_2

c) remove phosphosilicate glass: etch 1 min 50 sec in 1% HF

measure sheet resistance and junction depth on test wafer

sheet resistance:

Appendix C: Extracted Electrical Data from Fabricated FD SOI nMOS Transistors

Summary of electrical characteristics extracted from all fabricated wafers from selected
FD SOI nMOS devices

Wafer F15-	Nominal Width [μm]	Nominal Length [μm]	Threshold Voltage [V]	Subthreshold Swing [mV/dec]	Normalized Subthreshold Leakage [$\text{nA}/\mu\text{m}_{\text{Width}}$]
1	50	1.25	0.22	84	1.128
		2.5	0.30	84	1.024
		3.8	0.31	84	0.604
		5	0.32	80	0.620
		7.5	0.30	84	0.368
		10	0.34	84	0.338
		15	0.35	84	0.218
		20	0.36	80	0.210
2	50	10	0.32	80	0.586
3	5	10	0.34	100	1.123
	50	10	0.32	88	0.318
		20	0.33	84	0.220
4	5	10	0.38	112	1.368
	20	5	0.34	92	0.675
		7.5	0.36	88	0.655
		10	0.38	76	0.428
	50	1.25	0.31	86	0.666
		2.5	0.33	92	0.468
		3.8	0.34	82	0.508
		10	0.35	88	0.154
		15	0.36	92	0.108
20		0.37	80	0.073	

Comparison of expected vs. experimental threshold voltage data extracted from all fabricated wafers from selected FD SOI nMOS devices

Wafer F15-	Nominal Width [μm]	Nominal Length [μm]	Expected Threshold Voltage [V]	Actual Threshold Voltage [V]	Difference Between Expected vs. Actual [mV]
1	50	1.25	0.272	0.22	52
		2.5		0.30	28
		3.8		0.31	38
		5		0.32	48
		7.5		0.30	28
		10		0.34	68
		15		0.35	78
		20		0.36	88
2	50	10	0.253	0.32	67
3	5	10	0.203	0.34	137
	50	10		0.32	117
		20		0.33	127
4	5	10	0.281	0.38	99
	20	5		0.34	39
		7.5		0.36	79
		10		0.38	39
	50	1.25		0.31	29
		2.5		0.33	49
		3.8		0.34	59
		10		0.35	59
		15		0.36	79
		20		0.37	89

Comparison of expected vs. experimental subthreshold leakage data extracted from all fabricated wafers from selected FD SOI nMOS devices

Wafer F15-	Nominal Width [μm]	Nominal Length [μm]	Expected Normalized Subthreshold Leakage [$\text{nA}/\mu\text{mwidth}$]	Actual Normalized Subthreshold Leakage [$\text{nA}/\mu\text{mwidth}$]	Difference Between Expected vs. Actual [$\text{nA}/\mu\text{mwidth}$]
1	50	1.25	0.142	1.128	0.986
		2.5	0.097	1.024	0.927
		3.8	0.076	0.604	0.528
		5	0.061	0.620	0.559
		7.5	0.044	0.368	0.324
		10	0.035	0.338	0.303
		15	0.024	0.218	0.194
		20	0.018	0.210	0.192
2	50	10	0.067	0.586	0.519
3	5	10	0.422	1.123	0.701
	50	10	0.382	0.318	0.064
		20	0.200	0.220	0.020
4	5	10	0.028	1.368	1.340
	20	5	0.172	0.675	0.503
		7.5	0.124	0.655	0.531
		10	0.098	0.428	0.331
	50	1.25	0.101	0.666	0.565
		2.5	0.069	0.468	0.399
		3.8	0.054	0.508	0.454
		10	0.025	0.154	0.129
		15	0.017	0.108	0.091
		20	0.013	0.073	0.060

Comparison of expected vs. experimental subthreshold leakage data extracted from all fabricated wafers from selected FD SOI nMOS devices

Wafer F15-	Nominal Width [μm]	Nominal Length [μm]	Expected Subthreshold Leakage [nA]	Actual Subthreshold Leakage [nA]
1	50	1.25	7.11	56.4
		2.5	4.87	51.2
		3.8	3.79	30.2
		5	3.07	31.0
		7.5	2.21	18.4
		10	1.74	16.9
		15	1.20	10.9
		20	0.91	10.5
2	50	10	3.37	29.3
3	5	10	2.11	6.14
	50	10	19.12	15.9
		20	10.01	11.0
4	5	10	0.14	6.84
	20	5	3.44	13.5
		7.5	2.48	13.1
		10	1.95	8.55
	50	1.25	5.05	33.3
		2.5	3.46	23.4
		3.8	2.69	25.4
		10	1.24	7.68
		15	0.85	5.41
		20	0.65	3.65

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