$\Delta \ln \rho_{\text{eff}} = \frac{1}{\rho_{\text{eff}}} \left(\frac{\partial \rho_{\text{eff}}}{\partial \ln \rho} \right) \Delta \ln \rho$

3

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**High-Frequency BiCMOS
Transconductance Integrators**

by

R. Douglas Beards, B. Eng.

**This thesis is submitted to the
Faculty of Graduate Studies and Research
in partial fulfillment of the requirements
for the degree of
Master of Engineering**

**Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Carleton University
Ottawa, Ontario
Canada
October 1990**

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The undersigned recommend to the Faculty of Graduate Studies and
Research the acceptance of the thesis:

**High-Frequency BiCMOS
Transconductance Integrators**

submitted by R.Douglas Beards in partial fulfillment of the
requirements for the degree of Master of Engineering.

A handwritten signature in cursive script, reading "M.A. Copeland", written over a horizontal line.

Prof. M.A. Copeland
Thesis Supervisor

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Prof. J. Wight
Chairman,
Department of Electronics

October 1990

Abstract

This thesis reports on work that has been done on tunable high-frequency transconductance integrators utilizing a sub-micron BiCMOS technology. A fully-differential integrator has been designed that has both tunable bandwidth and tunable phase compensation. Application of such an integrator to open-loop transconductance filtering in the 10-50 MHz frequency range is explored, and general conclusions concerning analog BiCMOS circuit design are drawn.

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List of Symbols

A_I	current gain
A_v	voltage gain
β	forward current gain of a bipolar transistor
BiCMOS	Bipolar Complementray Metal Oxide Semiconductor - a technology which provides both bipolar and MOS devices
C_c	compensation capacitor
C_{int}	integrating capacitor
f	frequency
f_T	frequency at which the current gain of a transistor is unity
g_m	transconductance
g_o	output or drain conductance
IC	integrated circuit
I_{EE}	tail current in a differential pair
I_s	saturation current of a bipolar transistor
K_p	transconductance factor for MOS transistors, the product of carrier mobility and oxide capacitance
L	gate length of an MOS transistor
M	symbol used to denote an MOS transistor
MHz	megahertz
MOS	Metal Oxide Semiconductor - refers to either a PMOS or NMOS device
OTA	operational transconductance amplifier
p	frequency at which a pole occurs
PSRR	power supply rejection ratio
Q	quality factor (of a filter etc.) Also used to denote a bipolar transistor
R_c	resistor used for compensation

RC	product of resistance and capacitance, yielding a time constant
R_{EE}	emitter degeneration resistance
s	complex frequency variable
SR	slew rate
μ	carrier mobility
UGBW	unity gain bandwidth
V_A	early voltage
VCCS	voltage-controlled current source
VCVS	voltage-controlled voltage source
$v_{o,cm}$	common-mode output voltage
V_{os}	offset voltage
V_T	thermal voltage
V_{th}	threshold voltage
W	gate width of an MOS transistor
ω	a radian frequency
ω_n	natural or resonant frequency
z	frequency at which a transmission zero occurs
λ	channel length modulation factor for an MOS transistor

Chapter 1

Introduction

1.1 Thesis Motivation

In recent years there has been an effort to perform precision signal processing functions monolithically; that is, on a single integrated circuit chip. There are currently two well-developed methods for achieving this. These are with switched-capacitor filtering, and with digital filtering. Both of these methods use sampling actions at the inputs, and so filtering is actually done in discrete time. As a consequence, both anti-alias and smoothing filters are required at the inputs and outputs respectively. In contrast to sampled data techniques, many monolithic continuous-time filtering techniques have been proposed and tried, but none have really stood the test of time and developed into mature techniques.[1] Classical techniques such as active RC filtering, which work well in discrete implementations, simply do not lend themselves to monolithic implementations. This is because it has not been possible to produce precision RC time constants on-chip, in the types of processes that are commonly used today.

The reasons why alternatives to switched-capacitor and digital filtering techniques are still sought can be seen by examining the limitations of these techniques. Switched-capacitor filters are inherently noisy circuits, owing to the high impedance

levels, the presence of many clocked switches, and the effects of aliasing. High-frequency limitations in the switches and op-amps used in the filters severely limit the frequencies of the signals that such filters can process. While careful design along with a thorough understanding of the nature of the limitations can minimize their effects, this tends to push the design of high-frequency, high-performance switched-capacitor filters well beyond the abilities of the average designer. Digital filters tend to be large in area, owing to the additional need for analog-to-digital and digital-to-analog converters, and can be quite power-hungry at high frequencies. The design of the D/A and A/D converters themselves can become the critical design issue, especially where high-speed, low-quantization noise operation is required. Continuous-time filtering techniques on the other hand offer inherently simpler operation and promise small area, low power, and ease of design.

One technique for implementing precision, monolithic, continuous-time filtering that has recently been developed involves the use of the MOS transistor, biased in the linear region, as a voltage-controlled resistor. For small signal swings the transistor behaves as a linear resistor. The value of the resistance can be adjusted by the gate potential of the transistor, usually with an on-chip tuning circuit. These MOS resistors can then be combined with capacitors and op-amps to form active RC filters with high precision.[2]

A second technique is the transconductance filtering approach. With this technique, a precision monolithic RC time constant is obtained using a voltage-controlled current source (VCCS), in place of a resistor, to feed current into the integrating capacitor. This basic integrator can then be used as a building block for more complex filter sections. On-chip tuning techniques can also be applied to this type of filter, where the time constant of the integrator can be adjusted by varying the transconductance of the VCCS.[3] Both of these techniques overcome the earlier-mentioned problem concerning the ability to make a precision RC time constant on-chip.

The latter technique for monolithic continuous-time filtering is the one with which

this thesis is concerned. As will be shown in the next chapter, it is a method that is particularly well-suited to high frequency applications. The crucial design limitation becomes the design of the VCCS, which is typically an operational transconductance amplifier (OTA). A precise unity gain bandwidth and phase margin must be achieved, while other issues common to all signal processing techniques must also be addressed. Recently, the availability of a mixed bipolar and CMOS (BiCMOS) process has provided the designer with an enhanced ability to address these issues.

At present, state-of-the-art monolithic continuous-time high-frequency filtering is being achieved using bipolar processes, and is limited to frequencies around ten megahertz.[4] Newly-emerging technologies such as digital radio will require monolithic filtering capabilities at much higher frequencies, and in a process which is also suitable for high-density digital design. Again, BiCMOS processes appear ideally suited.

1.2 Thesis Objectives

The objective of this thesis is to explore the capabilities of a fine-line BiCMOS process in the design of wideband transconductance integrators for precision monolithic continuous-time filtering. The design considerations of such an integrator will be explored in detail, with an emphasis placed on tunability and phase compensation as means of realizing a precision wideband design. Finally, the objective will be to design and implement an integrator that will provide a quality, high-frequency filtering capability. The work that is presented here represents exploratory research into the area of high-frequency continuous-time filtering using BiCMOS processes, and is not intended to produce a finished, viable design, but rather to open the area for further research.

1.3 Thesis Format

This thesis will present a logical progression through the design process of a tunable, high-frequency, BiCMOS transconductance integrator. In the process, the capabilities of the BiCMOS technology to allow monolithic high-frequency filtering in general are highlighted. The motivation and objectives have already been described. Chapter 2 will describe the concept of open-loop transconductance filtering and will introduce the design considerations for an integrator in the context of a BiCMOS technology. In Chapter 3, possible circuit topologies will be explored, and one will be proposed and justified. Detailed small-signal analysis of the circuit will be presented in Chapter 4, while Chapter 5 will examine the large-signal behaviour of the circuit. Simulation results showing specific performance expectations will be presented in Chapter 6, and finally, Chapter 7 will present the conclusions and recommendations for future work.

Chapter 2

Transconductance Filtering and the BiCMOS Context

2.1 Introduction

Recent advances in the field of telecommunications electronics have placed a greater importance on the need for quality monolithic high-frequency filtering capabilities. The advent of fiber-optic communications networks will vastly increase the speeds at which information can be exchanged. While fiber optics provides a broadband medium for information exchange, designers must be able to provide the circuitry that can process information at the speeds required to fully utilize the available bandwidth. Process development has responded with the introduction of high quality BiCMOS processes which can greatly improve the designers ability to meet the challenge. Circuit design techniques must in turn be adapted to these new processes.

One of the major areas of circuit design which must be improved is that of continuous-time filtering. This chapter explains the principles behind both conventional techniques and transconductance techniques and then looks in depth at the latter techniques which will be shown to have some inherent advantages. A survey will be presented of different approaches to transconductance filtering which have

been reported in the literature, and finally the implications of the availability of a BiCMOS process will be discussed.

2.2 Principles of Transconductance Filtering

2.2.1 Active Filtering

The principles of active filtering can perhaps best be explained with reference to the integrator, which forms the basic building block of many types of active filters. [6] The frequency response of the ideal integrator is that of the $1/f$ response, as shown in Figure 2.1a. The key characteristics are infinite dc gain, a -20dB/decade roll-off indicated by the Laplace transform $1/s$, a constant ninety degree phase shift, and a unity gain bandwidth given by the numerator of the Laplace transform, a . The utility of the integrator as a basic filter building block is illustrated in Figure 2.1b where four integrators and two summing elements are combined to form a second order low pass active filter.

The realization of the integrator generally makes use of the natural integrating action of a capacitor. A current proportional to the input signal is fed into a capacitor, and the resulting voltage across the capacitor is proportional to the time integral of the current. However, the active element which is used varies. In general, it is either a voltage-controlled voltage source (VCVS) or a voltage-controlled current source (VCCS), where the former is commonly known as the operational amplifier or op-amp, and the latter is known as the operational transconductance amplifier or OTA. Integrators based on these two active elements are shown in Figure 2.2.

The integrator shown in Figure 2.2a, based on the VCVS, is the classical active RC integrator. With an ideal op-amp, the negative input to the op-amp is held at virtual ground through feedback, and the resistor then feeds a current proportional to the input voltage into the integrating capacitor. There are two problems with this type of implementation which limit its usefulness in high-frequency monolithic

Figure 2.1: (a) Ideal Integrator Symbol and Frequency Response (b) Realization of a Second Order Lowpass Transfer Function Using Four Ideal Integrators and Two Summers

applications. One concerns the ideality of the resistor, and one the ideality of the op-amp.

In conventional IC fabrication processes, resistors generally exhibit poor linearity and poor absolute accuracy and matching properties. This means that monolithic integrators with accurate and stable gain constants cannot be manufactured directly in the active RC form. A solution to this problem which has been proposed[2] involves the use of appropriately biased MOS transistors in place of resistors. The use of an MOS transistor as a resistor means that the resistance of the device can be tuned on chip by controlling the gate voltage, typically using a phase-locked loop and a precision reference frequency. Additional circuitry is required to linearize the resistance

Figure 2.2: (a) VCVS-Based (Active RC) Realization of an Integrator (b) VCCS-Based (Transconductance) Realization of an Integrator

presented by the MOS transistor.

A second problem concerning the VCVS-based realization involves the ideality of the op-amp. In order for this integrator to work, a large gain must be available to hold the inverting node at virtual ground. This means that the bandwidth of the op-amp must be much greater than the bandwidth of the integrator. Hence, this type of implementation is not particularly well suited to the design of high frequency filters.

The second type of integrator, shown in Figure 2.2b, uses the VCCS as the active element. Here, a transconductance element (such as a simple transistor) is used open-loop to feed the current into the integrating capacitor. The two problems discussed above, associated with the VCVS implementation, are avoided. Tunability is easily achieved, for example by varying the bias current in the transconductance device. More importantly, the active device need not have a bandwidth which is much wider than the integrator bandwidth, as is the case in the VCVS-based implementation. In fact, the bandwidths of the VCCS and the integrator are one and the same. As will be shown in the next section, however, other problems concerning widebanding of the VCCS-based or transconductance integrator must be addressed. A third advantage of the transconductance approach is in component count. The transconductance integrator uses only an active element and a capacitor, while the VCVS-based integrator

Figure 2.3: Frequency Response of a Practical Transconductance Integrator

requires both these components as well as an additional resistor.

The design of the op-amp used in VCVS-based integrator implementations is a highly developed field in both bipolar and MOS technologies. However, because of the relative novelty of the transconductance filtering approach, OTA and transconductance filter design are relatively new fields. While many different approaches have been reported in the literature, [3, 5, 6, 7, 8, 9, 4] to date, no proven and accepted design approach has been developed for practical applications.[1, 10] The next section will look at the design considerations for transconductance integrators, and some of the approaches which have been reported in the literature.

2.2.2 Transconductance Integrators

The transconductance integrator shown in Figure 2.2b will have the frequency response of the ideal integrator only if the VCCS behaves ideally. The response of a practical integrator is shown in Figure 2.3. One potential problem due to non-ideal OTA behaviour is the finite dc gain of the integrator and the associated phase lead near the unity-gain bandwidth (UGBW). A second potential problem is the presence

of non-dominant high frequency poles which will cause excess phase lag near the UGBW. The relative effects of these non-idealities on filter behaviour will of course depend on the type of filter being constructed. However, it can be shown[3, 6] that phase lead at the integrator UGBW will cause a degradation of the quality factor Q of the filter. Conversely, excess phase at the integrator UGBW will cause the filter Q to be enhanced with resultant peaking in the magnitude response and possible oscillation. Depending on the filter being implemented, as little as one half degree of deviation from the ideal ninety degree phase of the integrator UGBW can cause serious degradation of the filter response, particularly in high- Q filters. [3] As one might expect, finite dc gain and non-dominant poles can, to a certain extent, be played off against each other to cancel their respective effects and result in a nearly ideal filter response. That is, phase lead due to finite dc gain can be cancelled by phase lag due to parasitic poles.

A second type of non-ideal effect in integrators is non-linearities which occur for large-signal operation. While this is true for all types of integrator design, it is particularly important in transconductance integrator design. This is because the active elements in these types of integrators are operated open-loop at their UGBW's so that large signal swings may be present at the circuit inputs, in contrast to an op-amp realization where feedback holds the input signal to a very small value.

One of the chief advantages of the transconductance approach to integrator design is the ease of tunability of the integrator UGBW (and hence the associated time constant) via tuning of the transconductance of the OTA. Hence an important design consideration is the tunability of the integrator bandwidth, where it is desired that this be independent of other integrator properties. It is assumed that the desired phase response will be present at the UGBW.

Finally, in addition to the frequency and large-signal response requirements which are particular to OTA design, the design considerations which are common to all types of active device design, such as noise behaviour, slewing characteristics, power supply

rejection (PSR) and common-mode rejection (CMR) must be taken into account. As well, the need for differential inputs to facilitate both inverting and non-inverting integrator design is implicit.

A common approach to the implementation of transconductance integrators is to use a very simple transconductance stage such as a differential pair, in conjunction with the integrating capacitor as shown in Figure 2.4a.[3] The objective of this approach is to avoid the introduction of parasitic high-frequency poles and their associated excess phase. While these poles can not be avoided completely, their effects can be minimized and then compensated for by the phase lead associated with the finite dc gain. Referring to Figure 2.4a, the UGBW of such an integrator can be written from inspection as

$$\omega_o = g_{m(M1,M2)}/2C_{int} \quad (2.1)$$

where, for the MOS differential pair, the transconductance $g_{m(M1,M2)}$ is given by:

$$g_{m(M1,M2)} = \sqrt{K_p(W/L)I_o} \quad (2.2)$$

where K_p is the MOS transconductance factor, and W and L are the width and length respectively of the gate of the MOS transistor. Hence the integrator bandwidth can be easily tuned by varying the tail current I_o in Figure 2.4a.

The simple differential pair implementation of the integrator has some disadvantages as a general purpose integrator. Chief among these are the low dc gain, which causes phase error in the filter response at low frequencies (critical in low pass filter design), and the necessity for a dc level shift (which would cause additional high frequency phase shift) if direct cascading of integrators is required. A different type of OTA implementation that resolves these problems is the folded cascode implementation shown in Figure 2.4b.[9, 11] Equations (2.1) and (2.2) apply equally well to this design, but a higher dc gain can easily be achieved, and no dc level shifting is required when it is desired to cascade integrators. Tuning of the UGBW for this integrator is achieved in a manner similar to that of the differential pair integrator

Figure 2.4: Three Common Approaches to Transconductance Integrator Realization

except that currents in both the differential pair and the cascode stage must be tuned simultaneously to maintain the common mode level, using $V_{control}$, as shown in the Figure.[9]

A third possible configuration for realizing an integrator becomes apparent when one recognizes that the integrator response shown in Figure 2.3 is also the frequency response of a typical two-stage internally compensated op-amp. This approach has in fact been used for integrator realization in the past [6, 8] and is the approach used in this thesis. A simplified schematic of such an integrator, which makes use of the classical pole-splitting technique, is shown in Figure 2.4c. While the two-stage approach appears to represent a regressive step in terms of both complexity and the introduction of extra high frequency parasitic poles, it has a unique property that makes it attractive as an integrator topology but which has not been previously exploited. Specifically, the addition of the nulling resistor R_c in the feedback path allows the zero associated with C_{int} to be tuned as shown in Figure 2.5[12], assuming an appropriate method for varying R_c can be found. The significance of this lies in the fact that a left-hand plane zero adds phase lead to the frequency response, and so the location of the ninety degree phase shift region of the integrator can be adjusted by tuning R_c , and in fact can be extended to higher frequencies. The exact details of this will be considered in later chapters. However, already it can be seen that while the first two integrator implementations allow for tuning of the UGBW, but rely on process control and careful design to ensure a ninety degree phase shift at this frequency, the final implementation using the two stage op-amp allows for both properties to be tuned. A second attractive characteristic of the two-stage approach is the ability to draw on a wealth of knowledge concerning the behaviour of the circuit which has been developed over the years in the general purpose op-amp context. Finally, it is interesting to note that with the two-stage pole-splitting op-amp implementation of the integrator, the OTA and the integrating capacitor can no longer be thought of separately as they have been merged into a single circuit.

Figure 2.5: Movement of the Transmission Zero for the Circuit of Figure 2.4c

While the three transconductance integrator implementations just presented do not represent all the possibilities, they are representative of those which have been reported in the literature, and they illustrate the basic design considerations relevant to such a circuit. The next section of this chapter will examine these and some of the more generic design considerations within the new context of BiCMOS technologies.

2.3 The BiCMOS Context

When designing a transconductance integrator, or indeed any circuit, many design decisions will be influenced by the details of the technology in which it is to be implemented. While many circuit topologies such as the basic two-stage op-amp have analogies in both bipolar and MOS technologies, others, such as the bipolar Gilbert cell are peculiar only to one technology. Design styles also tend to vary between technologies. While the use of resistors as loads is a common practice in bipolar design, the lack of availability of suitable resistor values has resulted in the almost exclusive use of active loads in designs implemented in CMOS technologies.[13] Similarly, while CMOS designs have made use of the availability of complementary

devices in simplifying designs, the lack of availability of a good complementary device in most bipolar technologies has made necessary the development of many techniques which overcome this limitation.[14, 16] In light of these facts, it is apparent that the availability of a mixed bipolar and CMOS or BiCMOS technology will have many implications concerning the choice of a circuit topology for a given application. This section looks at the devices that are available in such a technology and examines some of the implications regarding the design of transconductance integrators.

2.3.1 Devices Available in BiCMOS Technologies

While it is not always the case, many BiCMOS technologies and particularly the one with which this thesis is concerned have evolved from existing CMOS technologies. The main difference from a typical CMOS technology is the addition of a high quality vertical NPN transistor, made possible by including one or more additional processing steps. Complementary PNP transistors and quality precision resistors are generally not available. Capacitors of high quality and precision and both n and p channel MOS transistors with near-micron gate lengths are typically available, as are (typically) both lateral and substrate PNP transistors. The latter types of transistors generally exhibit very poor performance, which falls off rapidly with collector current, and so their use may in most cases be abandoned in favour of the PMOS transistor.

In designing a circuit within a BiCMOS context, the question often arises of whether to use a bipolar or MOS device for a particular transistor. This question may often be answered simply by considering the performance characteristics of the two candidates. This will require careful consideration of other transistors in the circuit, and may even influence the entire topology to be used. As a first step to answering the question however, Table 2.1 compares bipolar and MOS transistors, where it is assumed the devices are operating in their active (high gain) regions, and non-ideal effects are negligible. The equations given there are well known, and their relevance will be discussed subsequently.

Small-Signal Model	<p style="text-align: center;">Bipolar MOS</p>	<p>-MOS has infinite input impedance at dc, while bipolar has finite.</p> <p>-MOS has body effect for $V_{sb} \neq 0$, while bipolar does not.</p>
Output Current	<p>Bipolar: $I_C = I_s \left(1 + \frac{V_{ce}}{V_A}\right) \exp\left(\frac{V_{be}}{V_T}\right) = \beta I_B$</p> <p>MOS: $I_{DS} = \frac{K_p}{2} \frac{W}{L} (V_{gs} - V_{th})^2 (1 + \lambda V_{ds})$</p>	<p>-Bipolar has exponential dependence on bias, while MOS has square-law.</p> <p>-Bipolar depends on bias only, while MOS depends on bias and geometry.</p>
Trans-conductance	<p>Bipolar: $g_m = I_C / V_T$</p> <p>MOS: $g_m = \sqrt{2K_p \frac{W}{L} I_{DS}}$</p>	<p>-For otherwise similar devices, g_m of bipolar typically $\gg g_m$ of MOS.</p> <p>-For bipolar, g_m is fixed for a given bias, while g_m of MOS can be adjusted by bias and geometry.</p>
Output Impedance	<p>Bipolar: $r_o = V_A / I_C$</p> <p>MOS: $r_o = 1 / \lambda V_{DS}$</p>	<p>-V_A typically larger than $1 / \lambda$.</p> <p>-V_A is fixed for a given bias, but λ can be made smaller by increasing gate length.</p>
Intrinsic Gain (voltage)	<p>Bipolar: $g_m r_o = V_A / V_T$</p> <p>MOS: $g_m r_o = \frac{2}{\lambda (V_{gs} - V_{th})}$</p>	<p>-Intrinsic gain is fixed for a given bipolar process, while in MOS, it can be varied by geometry, biasing.</p> <p>-Intrinsic gain typically much larger for bipolar than for MOS.</p>
Unity-Gain Frequency (current)	<p>Bipolar: $2\pi f_T = \frac{g_m}{C_{je} + C_{\mu} + g_m r_F} \approx \frac{\mu V_T}{\omega_b^2}$</p> <p>MOS: $2\pi f_T = \frac{g_m}{C_{gs} + C_{gd}} \approx \frac{\mu (V_{gs} - V_{th})}{L^2}$</p>	<p>-In bipolar case, f_T is approximately fixed for a given process (falls off at high and low currents) while in MOS case, f_T can be adjusted by geometry. In MOS case, high f_T is inconsistent with high $g_m r_o$.</p>
Current Gain	<p>Bipolar: $A_I = \beta_F = \frac{\beta_o}{1 + j\omega \beta_o \frac{C_{\pi} + C_{\mu}}{g_m}}$</p> <p>MOS: $A_I = \frac{1}{j\omega \frac{C_{gs} + C_{gd}}{g_m}}$</p>
Input-Referred Offset (for a differential pair with a resistive load, R)	<p>Bipolar: $V_{OS} = V_T \left(\frac{\Delta R}{R} + \frac{\Delta I_s}{I_s} \right)$</p> <p>MOS: $V_{OS} = \Delta V_{th} + \frac{(V_{gs} - V_{th})}{2} \left[\frac{\Delta(W/L)}{(W/L)} + \frac{\Delta R}{R} \right]$</p>	<p>-Generally, bipolar transistors exhibit better matching than do MOS transistors.</p> <p>-Effects of mismatch are referred back to the input as the ratio I_o / g_m which is smaller for bipolar than for MOS.</p>

Table 2.1: Comparison of Bipolar and MOS Transistor Properties

<p>Noise Models</p>	<p>BJT Noise Model</p> <p>MOSFET Noise Model</p> <p>Equivalent Input-Referred 2-Port Noise Model</p> <p>Bipolar:</p> $\bar{v}_{ni}^2 = 4kT\Delta f \left(r_b + \frac{1}{2g_m} \right)$ $\bar{i}_{ni}^2 = 2q\Delta f \left(I_B + \frac{K_f I_B^4}{2qf} + \frac{I_C}{ \beta(j\omega) ^2} \right)$ <p>MOS:</p> $\bar{v}_{ni}^2 = 4kT\Delta f \left(\frac{2}{3} \frac{1}{g_m} + \frac{K_f I_{DS}^4}{4kTg_m^2 f} \right)$ $i_{ni}^2 = \Delta f \left[2qI_G + \left(\frac{\omega C_{gs}}{g_m} \right)^2 \left(\frac{8kTg_m}{3} + \frac{K_f I_{DS}^4}{f} \right) \right]$	<p>The three main types of noise are:</p> <p>Flicker Noise: Due mainly to capture and emission of carriers in traps associated with defects. Has mean-square noise current of value $\bar{i}_n^2 = K_f I^4 \Delta f / f \quad [A^2]$</p> <p>Shot Noise: Occurs due to dc flow of current across a pn junction. Has mean-square noise current of value $\bar{i}_n^2 = 2qI\Delta f \quad [A^2]$</p> <p>Thermal Noise: Due to random motion of carriers in a resistive element. Has mean-square noise current of value $\bar{i}_n^2 = 4kT\Delta f / R \quad [A^2]$</p> <p>-For comparison purposes (MOS vs. bipolar) it is useful to employ 2-port input-referred noise models, which are valid for any value of source impedance R_S. (Note that the relative effect on the short-circuit output noise current of each noise source depends on the impedance R_S of the source that is driving the transistor.) The equivalent 2-port model can be constructed by solving for an equivalent input noise current $\bar{i}_{ni}^2$ with the input to the transistor open-circuited, and an equivalent input noise voltage $\bar{v}_{ni}^2$ with the input to the transistor short-circuited.</p> <p>-For large values of R_S, the equivalent input noise current is dominant, while for small values of R_S, the equivalent input noise voltage is dominant.</p> <p>-Typically, $\bar{v}_{ni}^2$ is larger for MOS transistors than it is for bipolar transistors because BJT's have a much higher transconductance to current ratio. Thus BJT's generally exhibit lower noise than do MOSFET's when driven by a low-impedance source.</p> <p>-At low frequencies, $\bar{i}_{ni}^2$ is larger for bipolar transistors than it is for MOS transistors because it is then given mainly by the gate leakage current I_G in the case of the MOSFET, and the base current I_B in the case of the BJT. Thus at low frequencies, MOSFET's generally exhibit lower noise than do BJT's, when driven by a high-impedance source.</p>
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Table 2.2: Table 2.1 Continued

When specific process and circuit parameters are substituted in the equations of Table 2.1, the vertical NPN bipolar transistor is seen to give more performance for a given bias current than a MOSFET in almost all respects. Two notable exceptions are the higher input impedance of the MOSFET at dc and the superior low frequency noise performance when driven by a high impedance source, which results from the extremely small gate leakage current. Table 2.1 also shows that in most respects, the performance of a MOSFET can be adjusted by the designer by varying the geometry of the device, even after the current levels are fixed. In general, the BJT's performance is fixed once the current level is fixed.

It can also be seen that while a BJT can be optimized for high f_T and low input-referred voltage noise without compromising gain (simply by increasing the bias current), this is not the case with a MOSFET. Increasing a MOSFET's bias current will increase f_T and decrease the thermal noise component of the input-referred noise voltage component, but will decrease the intrinsic gain and increase the flicker noise component.

With regard to high-frequency performance, it should be noted that the f_T of a device is generally determined by the ratio of the transconductance of the device to the total capacitance at the input to the device. The higher f_T of bipolar transistors as compared with MOS transistors is due mainly to the higher g_m/I ratio that bipolar transistors possess. This results in a situation where, in the bipolar case, a given transconductance can be realized with a much smaller device, and hence one which has much smaller parasitic capacitances.

With these points in mind, it would appear that bipolar transistors should be used almost exclusively. Unfortunately, the need for level shifting and complementary action often requires that PMOS devices be used since no complementary bipolar transistor is generally available. The design goal then is to produce a design which minimizes the need for the use of PMOS transistors, and minimizes the effect that their use has on overall circuit performance. It is worth noting here that some work

Figure 2.6: A Composite Complementary Device

has been reported on the development of composite devices such as the one shown in Figure 2.6 which use NPN and PMOS transistors to produce a quasi-complementary bipolar transistor with performance that exceeds that of an ordinary PMOS transistor, but generally falls short of what could be achieved from a true complementary PNP.[17]

2.3.2 BiCMOS Design Techniques

As was previously mentioned, the selection of a transistor type for a particular device within a BiCMOS design context is often complicated, not just by the particular performance requirements of that device, but also by the interaction with other devices. The need for level shifting also means that some performance compromises may have to be made and/or the topology changed, since a complementary PNP device is not generally available.

As an example of how level shifting requirements can affect performance and topology, consider the simple two-stage uncompensated op-amp shown in Figure 2.7. Figure 2.7a shows a version of the op-amp where an NPN input stage has been chosen, perhaps for low noise performance. Because of this however, the second stage driver must be a PMOS device, and so the bandwidth and gain of the second stage are compromised. Figure 2.7b shows an alternative circuit where the second stage driver

is an NPN device. Here the noise performance of the op-amp is compromised as PMOS devices must be used in the input stage. Finally, Figure 2.7c shows a realization of the op-amp where all driven devices are NPN transistors and so no compromise has been made in either the first or second stages. This has been accomplished however at the expense of an additional level-shifting emitter follower and two diode-connected NPN transistors, which adds to the design complexity, size, and power dissipation of the op-amp.

Further insight into the implications of device selection within a BiCMOS context can be obtained by considering the example of a two-stage op-amp in more detail. This design is covered in an excellent tutorial paper by Gray and Meyer[18] where the design of MOS op-amps is discussed in detail and compared to bipolar design. An example CMOS op-amp is shown in Figure 2.8 along with the corresponding approximate small-signal model. The choice of transistor type for each device will now be considered, with regards to a variety of op-amp performance criteria.

a) Input Impedance

The requirement for input impedance will depend on the application for which the op-amp is required, and specifically how much input current can be tolerated. The design of a general purpose op-amp or one for use in switched-capacitor filters would dictate the use of MOS input devices giving essentially zero input current at dc. Low input-current bipolar op-amps utilize Darlington configurations, emitter degeneration, or base current cancellation schemes to achieve high input impedance. Examples of these techniques are shown in Figure 2.9 along with well known equations for their respective input impedances.[19] Which scheme is actually used, or whether simple MOS input devices are used will depend on the type of application being considered, and on other performance requirements such as noise and offset.

If MOS inputs are used, consideration must be given to the size of devices that are used as this will affect linearity, noise, common-mode input range, and other characteristics. One advantage of using MOS inputs that is particular to OTA design

Figure 2.7: Two-Stage Op-Amp Examples Showing Performance Compromises Associated with Lack of a True Complementary PNP and Hence Need for Level-Shifting

Figure 2.8: Example of Two-Stage Op-Amp Using Pole-Splitting Compensation Technique (a) Circuit Schematic (b) Approximate Small-Signal Model

is the manner in which they lend themselves to tunability. In Section 2.2.2, it was shown how tuning of the UGBW of an integrator can be achieved by varying the bias current in the differential pair of the input stage. When this technique is applied to a simple bipolar input stage without emitter degeneration, Figure 2.9a shows that the input resistance of the OTA will vary in inverse proportion to the bias current. This may have unwanted effects on filter performance. If emitter degeneration is used, the tunability of the OTA is significantly reduced since the transconductance of the differential pair and hence the UGBW of the OTA then depend mainly on the value of the emitter degeneration resistance that is used.

b) DC Gain

The dc gain of the two-stage op-amp can be written as

$$A_v = A_{v1}A_{v2} = \frac{g_{m1}}{g_{o2} + g_{o4}} \frac{g_{m6}}{g_{o6} + g_{o7}} \quad (2.3)$$

where the g_m 's shown are transconductances and the g_o 's are self conductances for the particular transistors according to the subscript numbers. Typical gain values for MOS stages are around fifty per stage and for bipolar are around five hundred per

Figure 2.9: Examples of Bipolar Input Stage Configurations and Associated Input Impedances

Figure 2.10: Illustration of Input-Referred Offset (a) Random Offset (b) Systematic Offset

stage. Thus if a very large dc gain is required, one or both of the stages should use bipolar transconductance elements.

c) Offset Voltage

The input-referred offset voltage of the two-stage op-amp can have two different components. These are the random offset component which occurs due to mismatch between supposedly identical devices (and which was mentioned briefly in Table 2.1) and systematic offset which occurs because of improper design. An example of systematic offset is a mismatch between amplifier stages. Both types are illustrated in Figure 2.10.

In the case of random offset, matching of devices in the input stage is most critical, both because the effect is not divided back by any stage gain and because subsequent stages are often single-ended. It can be shown[18] that the input referred offset is related to mismatch Δ (as defined in Figure 2.10a) in most input stage device parameters by the equation

$$V_{os} = \frac{I}{g_m} \Delta \quad (2.4)$$

where I is the bias current in one side of the differential pair, as shown in Figure

2.10a. In the case of a bipolar differential pair, the ratio I/g_m is a constant, given by

$$\frac{I}{g_m} = \frac{KT}{q} \approx 26mV \quad (2.5a)$$

while in the case of a MOS differential pair, the ratio is given by

$$\frac{I}{g_m} = \frac{V_{gs} - V_{th}}{2} \quad (2.5b)$$

where V_{gs} and V_{th} are the gate-source and threshold voltages respectively of the transistors in the differential pair. This ratio I/g_m is generally much larger than for the bipolar case, being typically on the order of a few hundred millivolts. Thus an amplifier which is required to have low offset voltage should employ a bipolar differential pair in the input stage.

Figure 2.10b depicts the nature of systematic offset voltage. If the quiescent output voltage of the first stage v_{o1} does not equal the quiescent input voltage of the second stage v_{i2} , then an input-referred offset voltage will result, given by

$$V_{os} = \frac{v_{o1} - v_{i2}}{A_{v1}} \quad (2.6)$$

Thus, a large dc gain is required for the first stage in order to minimize the effects of systematic offset. This again implies the need for a bipolar input stage in order to minimize the input-referred offset voltage.

d) Frequency Response

The approximate small-signal model of the two-stage op-amp, shown in Figure 2.8b, can be analyzed to yield the following frequency response information[18]

$$UGBW = \omega_1 = \frac{g_{m1}}{C_c} \quad (2.7a)$$

$$p_1 = \frac{-1}{(1 + g_{m6}R_{o2})C_cR_{o1}} \quad (2.7b)$$

$$p_2 = \frac{-g_{m6}C_c}{C_cC_1 + C_cC_2 + C_1C_2} \approx \frac{-g_{m6}}{C_2} \quad (2.7c)$$

$$z = \frac{g_{m6}}{C_c} \quad (2.7d)$$

Here, C_c is the pole-splitting capacitor, C_1 and C_2 are the sums of all capacitances at the input and output respectively of the second stage, and R_1 and R_2 are the sums of all resistances at the input and output respectively of the second stage. For stable wideband operation, the requirement is that the non-dominant pole p_2 and the zero z be at high enough frequencies relative to the UGBW that an adequate phase margin be obtained. In the case of integrator design, this criteria is even more stringent, requiring a ninety degree phase margin. Obviously, for wideband operation a large second stage transconductance is required, indicating that a bipolar driver would be suitable there.

More insight can be achieved by considering the ratios

$$\left| \frac{p_2}{\omega_1} \right| = \frac{g_{m6}C_c}{g_{m1}C_2} \quad (2.8a)$$

$$\left| \frac{z}{\omega_1} \right| = \frac{g_{m6}}{g_{m1}} \quad (2.8b)$$

From these, it can be seen that the second stage transconductance must also be large relative to the that of the first stage in order to achieve adequate phase margin. This indicates that an MOS differential pair in the first stage would be well matched to the bipolar driver in the second stage. The opposite arrangement would result in possible instability. Other solutions for obtaining adequate phase margin would include a large ratio of currents in the input stage to current in the output stage, the use of emitter degeneration in the input stage, and the use of a nulling resistor in conjunction with C_c (as was discussed in Section 2.2.2).

In Section 2.2.2, it was pointed out that unlike general purpose op-amps, which use feedback to hold signal swings at the input low, OTA's are operated open-loop and so large signal swings may be present at the input. The implication of this is that, assuming a two-stage OTA is used, the second stage of the OTA should indeed be much more wideband than the first stage, or else large signal swings may be present at internal nodes, and the signal may be seriously distorted. This further reinforces the points made above concerning the need for bipolar drivers in the second stage.

A final interesting point to note is that, according to equation 2.7a, the larger the transconductance of the input stage, the larger a value of C_c that will be required to realize a given UGBW. As C_c will typically comprise a large portion of the area of the op-amp, this can be an important consideration. The implication is that a bipolar input stage without emitter degeneration resistors (which themselves consume area) or very low currents, (which implies high thermal noise and deleterious low level effects) will typically require a larger layout area than an MOS input stage because of the inherently higher transconductance of the bipolar transistor. This point has been recognized by bipolar designers in the past, particularly in regard to the design of transconductance integrators which require long time constants [6].

e) Slew Rate

The relationship between slew rate, bias conditions, and frequency response for the two-stage op-amp can be written as

$$SR = \frac{I_{D1}}{g_{m1}} \omega_1 \quad (2.9)$$

Substituting equation (2.5) into (2.9) yields, for the case of bipolar input devices,

$$SR = V_T \omega_1 \quad (2.10a)$$

and for the MOS case,

$$SR = \frac{(V_{gs} - V_{th}) \omega_1}{2} \quad (2.10b)$$

As was seen when offset voltages were considered, the I/g_m ratio of the MOS transistor is much larger than it is for the bipolar transistor, and thus for a given UGBW, the MOS differential pair will give a considerably higher slew rate than the bipolar differential pair, and so should be used for high slew rate amplifier applications. If a bipolar input stage is required for other reasons, emitter degeneration or other transconductance reduction techniques can be used to increase the I/g_m ratio and thus the slew rate.

f) Input Stage Linearity

Figure 2.11: Transfer Characteristics of the MOS and Bipolar Differential Pairs

In addition to slew rate limiting and long time constant realization, another problem associated with the inherently high g_m/I_c ratio of bipolar transistors is the limited input range over which the bipolar differential pair behaves in a linear fashion. It can be shown [20] that the transfer characteristics of the MOS and bipolar differential pairs are as depicted in Figure 2.11. The use of MOS differential pairs allows the linear input range to be extended well beyond what is possible with bipolar differential pairs. However, the linear input range of the bipolar differential pair can also be extended using emitter degeneration to limit the transconductance.

g) Noise

When deriving the equivalent input noise voltage of the two-stage op-amp, only the devices in the first stage need to be considered, since contributions of devices in the second stage are divided back by the (presumably high) gain of the first stage. Also, since each of the transistors in the input stage are driven by typically low impedance sources, the noise current generator associated with each transistor can be neglected. It can then be shown [18] that the equivalent input noise voltage of the

Figure 2.12: Equivalent Input-Referred Noise Voltages for Two Different BiCMOS Input Stages

op-amp is given approximately by

$$\overline{v_{neq}^2} = \overline{v_{ni1}^2} + \overline{v_{ni2}^2} + \frac{g_{m3}}{g_{m1}}(\overline{v_{ni3}^2} + \overline{v_{ni4}^2}) \quad (2.11)$$

where the subscripted noise contributions refer to the respective transistors in the input stage. The important point to note from equation (2.11) is that the noise contributions of M_3 and M_4 are multiplied by the ratio g_{m3}/g_{m1} . The implications of this are illustrated in Figure 2.12. The input stage in (a) has relatively noisy PMOS input devices, whose noise adds directly, and a bipolar current mirror load whose noise adds as g_{m3}/g_{m1} which is typically on the order of 10. Hence the low-noise bipolar devices have their noise contributions amplified. The input stage in Figure 2.12(b) on the other hand makes good use of equation (2.11) to produce a low noise input stage. Here, the low-noise bipolar input devices add their noise directly, while the noisy PMOS devices have their noise attenuated by the ratio g_{m3}/g_{m1} which in this case is typically 0.1. This implementation may, depending on process details, be less noisy than an all-bipolar implementation as long as the ratio g_{m3}/g_{m1} is less than the ratio of the bipolar noise to the MOS noise.

Two final points can be made here regarding the design of low-noise BiCMOS amplifiers. In Figure 2.12, and in general, if MOS devices are required, PMOS transistors should be chosen as they have lower flicker noise than NMOS devices.[21] A second point of importance is that, particularly in the case of OTA design, the assumption that all devices are driven by low impedance sources may not hold true. Cascading of, or feedback around amplifiers with unbuffered outputs (such as OTA's) will produce a situation where the input device(s) is (are) driven by a high impedance source. In this case, the equivalent input noise current sources must be considered, and MOS devices may be the more judicious choice for the input pair (see Table 2.1).

The preceding discussion on the design of a BiCMOS two-stage op-amp has illustrated one very important principle of BiCMOS design. The choice of transistor type for a given device generally depends on many factors, and may influence the entire circuit topology. Performance tradeoffs are almost always involved, and the designer must weigh these carefully. While several specific BiCMOS design principles have been pointed out and will be emphasized later during the discussion of the actual OTA design, the objective was only to illustrate the considerations that are involved, and to demonstrate that bipolar and MOS devices can be combined to yield circuits with performance that exceeds what is possible in either bipolar or CMOS alone. The key advantage of BiCMOS over bipolar design (where vertical PNP's are not available) is that the p-type device in the former offers, in general, greater performance. The key advantage of BiCMOS over CMOS design is that in the former the n-type device offers, in most applications, greater performance. However, in BiCMOS a true complementary device is still not available and so the added design complexities associated with trying to deal with the absence of one are still present. Another advantage of BiCMOS over both bipolar and CMOS design is that in BiCMOS, two completely different device types (bipolar and MOS) are available, giving the designer more flexibility in meeting performance requirements.

In the next chapter, the principles regarding transconductance filtering and BiC-

MOS design techniques will be combined, and a tunable wideband transconductance integrator design will be presented.

Chapter 3

Selection and Rationale of Integrator Topology

3.1 Introduction

In the previous chapter, the rationale behind transconductance filtering as a means for achieving precision high-frequency monolithic continuous-time filtering was explained. Also, the design considerations involved in implementing the basic building block, the transconductance integrator, within a BiCMOS context were presented. This chapter explains the key features of the integrator topology which was selected for implementation in a BiCMOS technology, and the rationale behind the choice. Basic design equations will be presented, leading to a complete design for a BiCMOS transconductance integrator capable of operating in the 10-50 MHz frequency range. This represents an attempt to advance the state of the art, which at present is typified by bipolar designs which operate in the 10MHz range.[4]

3.2 Review of Integrator Requirements

At this point it is useful to briefly review the main performance requirements for a transconductance integrator. The overall objective is to design a circuit which implements, as nearly as possible, the transfer function of an ideal integrator up to relatively high frequencies (i.e.: 10-50 MHz). The precision of the phase and magnitude response near the integrator UGBW is paramount, especially when the integrators are used to implement selective high-Q filters. The objective of obtaining a precise integrator UGBW is readily achievable because of the inherent tunability of the bandwidth of a transconductance integrator. However, to the best of this author's knowledge, no reliable technique has yet been demonstrated for achieving the requisite ninety degrees phase margin, especially at high frequencies.

While an accurate implementation of the frequency response of an ideal integrator is essential, of equal importance is the ability of the integrator to provide quality processing of real signals. This means that a large dynamic range and low signal distortion must be achieved. The former objective can be achieved by keeping noise levels low and maximum allowable signal swings high, while low distortion levels can be achieved by insuring large linear ranges for devices or subcircuits and by keeping mismatches low, slew rates high (and equal), and internal signal swings small. Linearization techniques may also be employed. Finally, the circuit must be designed in such a manner that the effects of loading at the input and output do not greatly affect circuit performance. All of the above requirements should be met while keeping power and area consumption to a minimum. These issues will all be dealt with in more detail as the circuit design is presented.

3.3 The Two-Stage Pole-Splitting Op-Amp as a Tunable Transconductance Integrator

As was mentioned briefly in Chapter 2, the two-stage op-amp configuration which utilizes a pole-splitting compensation scheme was chosen as the basis for the transconductance integrator in this thesis. The main reason for this choice was that this configuration provides a convenient means for compensating excess phase lag associated with parasitic poles through the introduction of a left-hand plane zero in the integrator transfer function. A means of making this phase compensation tunable has been developed, so that a precise ninety degree phase margin can be ensured at the desired integrator UGBW despite the inherent uncertainty regarding the locations of high frequency parasitic poles. This uncertainty arises because parasitic pole locations are in general process and layout dependent. As will be seen, there are also several other advantages to using the two-stage configuration for realizing a transconductance integrator.

Figure 3.1 shows a simplified schematic of the two stage configuration, along with the corresponding approximate small signal model. In the schematic of Figure 3.1a, the input stage of the integrator has been shown as a transconductance element and an associated resistance R_i and capacitance C_i which together form the source impedance of the bipolar output driver, Q_o . The details of the input stage will be dealt with later. Q_o drives an active load M_o (a PMOS current source), as well as a complex load represented by R_L in parallel with C_L . These components would typically represent the input impedance of another similar transconductance integrator. In the small signal model of Figure 3.1b, the load resistance and capacitance have been combined with all other resistances and capacitances at the output node to form R_o and C_o respectively. The compensation resistor R_c and capacitor C_c are connected between the input and output of Q_o . Also, Q_o has been somewhat simplified to the extent that the base-to-collector capacitance C_μ has been omitted. The intrinsic base resistance

Figure 3.1: (a) Simplified Schematic of the Two-Stage Integrator (b) Approximate Small-Signal Model

and capacitance, r_π and C_π respectively, can be lumped in with R_i and C_i if desired.

The circuit diagram of Figure 3.1b has been seen before, in the two-stage op-amp of Figure 2.8, except for the inclusion of the nulling resistor R_c . As would be expected, the transfer functions of the two models are very similar, with the main difference being the location of the zero, and the addition of a third pole. It can be shown [22] that the transfer function of this circuit (with R_c added) is given by

$$\frac{v_o}{v_i} = \frac{A_0(1 - \frac{s}{z_1})}{(1 - \frac{s}{p_1})(1 - \frac{s}{p_2})(1 - \frac{s}{p_3})} \quad (3.1a)$$

where for typical parameter values,

$$A_0 = g_{mi}g_{mo}R_iR_o \quad (3.1b)$$

$$z_1 \approx \frac{-1}{C_c(R_c - \frac{1}{g_{mo}})} \quad (3.1c)$$

Figure 3.2: Pole-Zero Plot for Equation (3.1) for Typical Parameter Values

$$p_1 \approx \frac{-g_{mi}}{A_0 C_c} \quad (3.1d)$$

$$p_2 \approx \frac{-g_{mo}}{C_i + C_o} \quad (3.1e)$$

$$p_3 \approx \frac{-1}{R_c} \left(\frac{1}{C_i} + \frac{1}{C_o} \right) \quad (3.1f)$$

$$UGBW = \omega_1 = \frac{-g_{mi}}{C_c} \quad (3.1g)$$

Of the singularities in equation (3.1), the high frequency parasitic poles p_2 and p_3 contribute phase lag at ω_1 , the integrator UGBW, while the dominant pole p_1 and the left hand plane zero z_1 contribute phase lead at ω_1 . Here it is assumed that $R_c > 1/g_{mo}$ so that z_1 is indeed a left-hand plane zero. A pole-zero plot for equation (3.1) is shown in Figure 3.2, for typical parameter values.

For the typical situation where $R_c \gg 1/g_{mo}$ and $C_o \gg C_i$, equations (3.1c) and (3.1f) can be combined to yield

$$\frac{p_3}{z_1} = \frac{C_c}{C_i} \quad (3.2)$$

Thus even as R_c is varied, the left hand plane zero z_1 will always contribute more phase lead at ω_1 than the phase lag that is contributed by p_3 (as long as $C_c > C_i$). This implies that a value of R_c can always be chosen which will allow z_1 (and to some extent p_1) to compensate p_3 and p_2 (and any other high frequency parasitic poles which may be present), resulting in a precise ninety degree phase margin at

the UGBW of the integrator. Simulations of full integrator circuits using the circuit simulators HSPICE and Scamper have in fact shown this to be the case.

Because of the inherent uncertainties in the values of circuit parameters (and especially resistances such as R_c) due to process and layout variations, this compensation scheme will work best if it is a tunable one. An obvious choice for the tunable element is R_c , since varying R_c only affects the high frequency phase and magnitude responses, and the resistor can be replaced with a tunable transconductance element as is done in the input stages of transconductance integrators.

A modified two-stage integrator which allows for a tunable compensation resistance is shown conceptually in Figure 3.3. In this arrangement, the compensation resistance R_c of Figure 3.1 has been replaced with a diode-connected bipolar transistor, Q_{rc} , and a pair of identical current sources, I_1 and I_2 . The transistor Q_{rc} then acts as a floating resistor with the value of the resistance given by the inverse of the transconductance of Q_{rc} . Thus, the small signal resistance, r_c , is given by

$$r_c = \frac{V_T}{I_{rc}} \quad (3.3)$$

A more detailed investigation of the operation of this tunable resistance will be presented in subsequent chapter.

Since the value of I_{rc} is set by the two identical current sources I_1 and I_2 , the value of the compensation resistance r_c can be tuned by adjusting these two current sources in a complementary fashion. A circuit which achieves this is shown in Figure 3.4. In the circuit of Figure 3.4, a tuning current I_{tune} is injected into the drain-gate of transistor M_{T1} . This current is mirrored to M_{T3} which acts as the lower current source I_2 in Figure 3.3, as well as to M_{T4} (via M_{T2} and M_{T5}) which acts as the upper current source I_1 in Figure 3.3. As long as the transistor pairs M_{T2}, M_{T3} and M_{T4}, M_{T5} are well matched, complementary current tuning will be achieved.

The complete second stage of the integrator is shown in Figure 3.5. Cascode current sources (M_{T6}, M_{T7}) have been added to the tunable complementary current source arrangement to increase the input impedance of the second stage. An emitter

Figure 3.3: Modified Two-Stage Integrator With Compensation Resistor Replaced by a Tunable Transconductance Element

Figure 3.4: Circuit for Providing Complementary Tuning of Current Sources

Figure 3.5: Schematic of Two-Stage Integrator Showing Complete Second Stage

follower circuit (Q_{EF1}, Q_{EF2}) has also been added for level shifting purposes. In the next chapter, it will be shown that the emitter-follower also affects the small-signal behavior of the integrator. With this arrangement, the signal path has been restricted to NPN bipolar transistors only. Thus the circuit should provide good wideband performance, in keeping with the BiCMOS design principles which were described in Chapter 2.

The use of the two-stage op-amp configuration for a transconductance integrator has other advantages besides the tunable compensation ability. One important advantage is that the integrating capacitance (in this case C_c) is internal to the integrator. Recall that in the folded cascode realization of the transconductance integrator, the integrating capacitor is the load capacitor. In that type of realization, variations in load impedance will greatly affect the integrator UGBW and the phase response near that frequency. The available output swing of the folded cascode integrator is also limited because of the cascode devices at the output, whereas in the circuit of Figure 3.3, the output can swing to within a few hundred millivolts of each supply rail. This

means that a higher dynamic range can in general be obtained. Finally, the use of two stages instead of one means that a higher dc gain can in general be obtained, resulting in better integrator performance at low frequencies.

3.4 Input Stage Selection

At this point, the use of a two-stage integrator configuration has been rationalized, and the complete second stage design has been explained. The second stage of the integrator provides a means for allowing tunable phase compensation, ensuring a precise ninety degree phase margin at the UGBW of the integrator. As can be seen from equation (3.1g) however, the UGBW of the integrator is determined by the transconductance of the input stage. Attention will now be given to the selection of an input stage configuration which provides the ability to tune the UGBW of the integrator.

The basic transconductance circuit which is invariably used is the differential pair. The performance of different types of differential pairs were discussed briefly in Section 2.3.2. The MOS differential pair provides a large linear input range, infinite input impedance at dc (regardless of bias), and good transconductance tunability. However, it suffers from a large flicker noise voltage component. The simple bipolar differential pair provides good tunability and low flicker and shot noise, but would require a large compensation (integrating) capacitor or else very low currents (which would increase noise) to achieve a practical integrator UGBW. It also suffers from a limited linear input range, an input impedance which varies with bias, and very poor slew rate performance. Finally, large amounts of emitter degeneration resistance will improve the linear input range, slew rate, and input impedance of the bipolar differential pair, and make the input impedance essentially independent of bias, but thermal noise will increase and most importantly, tunability of transconductance is lost.

Since none of the three basic choices presented above are without their drawbacks, it was felt that an alternative for the input stage should be sought. The configuration which was chosen actually makes use of the heavily degenerated bipolar differential pair, but uses a Gilbert gain cell for tunability. This circuit is shown in Figure 3.6. The principle of operation of this circuit will now be explained.

$$G_m = \frac{g_m}{1 + g_m R_{EE}} \approx \frac{1}{R_{EE}} \quad (3.4)$$
$$I_1 = \frac{I_{EE}}{2} + \frac{v_i}{2R_{EE}} \quad (3.5a)$$

$$I_2 = \frac{I_{EE}}{2} - \frac{v_i}{2R_{EE}} \quad (3.5b)$$

Equation (3.5) shows that the effect of heavy emitter degeneration is in fact a linear voltage to current conversion. It can further be shown [23] that this linear transconductance occurs over the range

$$0 < v_i < I_{EE}R_{EE} \quad (3.6)$$

which can be made relatively large.

The Gilbert cell consisting of transistors Q_3 , Q_4 , Q_5 and Q_6 is a wideband current amplifier, providing linear amplification over a wide range of signal swing. Referring to Figure 3.7, the current gain taken differentially from the collectors of Q_1 and Q_2 to the collectors of Q_3 and Q_4 , can be shown to be [24]

$$A_I \equiv \frac{I_{o2} - I_{o1}}{I_1 - I_2} = \frac{I_{BB}}{I_{EE}} \quad (3.7)$$

and the effective transconductance, $G_{m,eff}$, of the entire input stage is thus

$$G_m = \frac{1}{R_{EE}} \frac{I_{BB}}{I_{EE}} \quad (3.8)$$

Tuning of the effective transconductance of the input stage and thus, according to equation (3.1g), of the integrator UGBW, can be achieved by varying the ratio I_{BB}/I_{EE} . For reasons which will become apparent in the next section, it was decided that tuning should be accomplished in this case by varying the current I_{EE} , as shown in Figure 3.7. While this does vary the intrinsic transconductance of the input pair Q_1, Q_2 , a large emitter degeneration resistance ensures that the input impedance of the input stage is not, to a first order, affected by tuning of the integrator UGBW.

The use of the Gilbert cell as shown in Figure 3.7 also results in a situation where tuning of the integrator UGBW does not affect the slew rate of the integrator. This is because the currents which are available to the second stage during slewing are not varied by tuning, as they would be if a Gilbert cell were not used.

It should also be pointed out that an alternative arrangement of the Gilbert cell exists, where the collectors of the transistor pairs Q_3, Q_4 and Q_5, Q_6 in Figure 3.7 are cross-coupled, resulting in a higher current gain and a situation where none of the

Figure 3.7: Complete Input Stage Configuration Including Circuit for Tuning Integrator UGBW

current in the input stage is wasted. This arrangement was not chosen however as it results in an unduly high output voltage for the first stage.

In summary, the input stage which was chosen allows for a tunable integrator UGBW where tuning does not affect the slew rate or input impedance of the integrator. The input stage is all-bipolar, resulting in low flicker noise and hence extended dynamic range. The stage has a relatively large linear input range, input impedance, and slew rate owing to the use of heavy emitter degeneration. Practical values of the integrator UGBW can be achieved with relatively small values of the compensation (integrating) capacitor.

The load for the input stage has not yet been discussed, nor has level shifting which will be required to interface the first and second stages. These topics will be discussed in the next section, along with the implementation of a doubly-differential design.

3.5 First Stage Loading, Level Shifting, and a Doubly-Differential Design

At this point, both the input and output stages of the transconductance integrator have been defined. What is left to be resolved is the loading for the first stage, and a means of interfacing the first stage to the second. The latter issue is two-fold. First, some level shifting will be required between stages, and second, the input stage is differential in nature while the output stage is single-ended. This implies the need for either a differential to single ended converter, or else a fully or doubly-differential design. In this thesis it was decided that, for reasons which will be given shortly, the integrator design should be doubly-differential. This in turn requires that a common mode stabilization circuit be designed.

3.5.1 Doubly-Differential Integrator Design

Most integrators and op-amps have differential inputs but single-ended outputs, with a differential to single-ended conversion being accomplished internally by some means. A fully-differential integrator is one which accepts a differential signal at the input and provides a differential signal at the output. A doubly-differential integrator has the differential output signal, but has two complete sets of differential inputs. These concepts are illustrated in Figure 3.8, where the standard OTA symbol is used to depict an integrator.

The advantages of using a fully or doubly-differential design are many, but the main one is the high immunity these designs have to power supply noise. This characteristic arises because power supply noise is a common-mode signal. That is to say that (assuming linearity) noise coupled into the circuit from power supply lines would be common to both outputs and so would not be sensed if the output signal is taken differentially. Further to this, the common-mode stabilizing circuit which must be present in a fully or doubly-differential design will act to attenuate power supply

Figure 3.8: Examples of Integrators that are (a) Differential Input, Single-Ended Output, (b) Fully-Differential, and (c) Doubly-Differential

noise (or any other common-mode signal). This characteristic is especially valuable in analog circuits when they must coexist on the same chip with digital circuits, since digital circuits tend to introduce a great deal of noise to power supply lines. Since mixed analog and digital chips are becoming more prevalent, fully or doubly differential designs are becoming more attractive if the dynamic range of analog circuits is to be maintained. Dynamic range is also improved in circuits having differential outputs because the output signal is taken across the two output terminals, and this effectively doubles the available output swing, as compared to the case where the output is taken between one terminal and ground.[18]

The use of a fully or doubly-differential design may, under certain conditions, reduce signal distortion. Banu and Tsividis[2] have demonstrated that in a fully-balanced circuit where a single input signal is applied differentially and the output is taken differentially, all even order harmonics which are introduced due to non-linear behaviour within the circuit will be cancelled out. The cancellation of non-linearities by the use of fully-differential signal paths can be seen intuitively in Figure 3.9. In Figure 3.9, a signal v_{i1} is applied to an inverter circuit, and the differential signal $v_{i2} = -v_{i1}$ is applied to a second identical inverter circuit, as in a fully or doubly-differential design. No output balancing is assumed. In the example, both inverter circuits are exhibiting identical clipping during the positive going swings of their outputs. The

Figure 3.9: Illustration of the Cancellation of Even-Order Non-Linearities by the Use of Fully-Differential Circuitry

two output voltages v_{o1} and v_{o2} both exhibit severe distortion with both even and odd order harmonics being present (evident since neither signal is symmetrical about the time axis). However, the signal $v_{o,diff}$, defined as the difference between v_{o1} and v_{o2} , and which is the relevant signal in a fully or doubly-differential design, will exhibit symmetry about the time axis, and so cancellation of even order harmonics has occurred. The output signal does however contain a common-mode component which would be cancelled to some degree in a circuit which employs output balancing.

A final advantage of using fully or doubly-differential signal paths is that circuits for providing differential to single ended conversion are not necessary. Since these circuits generally contribute both systematic offset and parasitic poles to the transfer function, fully or doubly-differential circuits will exhibit lower input-referred offset and fewer parasitic poles. The latter characteristic implies that a fully or doubly-differential integrator can be made to operate at higher frequencies than an integrator which has a single-ended output.

The main disadvantage of using a fully or doubly-differential circuit is the added design complexity and increased size and power consumption of the circuit. Added design complexity generally arises because a circuit which ensures common-mode stability must be included in the design. Added circuit size and power consumption arise because two complete signal paths must be provided. A realization of the second order low pass transfer function first introduced in Figure 2.1 is shown in Figure 3.10 where two doubly-differential integrators are used.

Hence it has been shown that the advantages of using a doubly-differential circuit design are many, with the only real disadvantage being the added complexity associated with designing the requisite common-mode stabilization circuit. With the doubly-differential design thus rationalized, the remaining aspects of the integrator design can now be described.

Figure 3.10: Realization of Second Order Low-Pass Filter of Figure 2.1 With Two Doubly-Differential Integrators

3.5.2 The Folded Cascode

The first stage loading, and interfacing between the first and second stages can be accomplished with the use of a single sub-circuit. This sub-circuit is the differential folded cascode arrangement illustrated in Figure 3.11. This arrangement also provides a convenient means for incorporating both the doubly-differential circuit and the common-mode stabilization circuit, and provides higher overall dc gain than could be achieved using a standard current mirror load.

Interfacing between the first and second stages of the integrator is accomplished by connecting the outputs from the first stage (the collectors of Q_3 and Q_4 in Figure 3.7) to v_{i1} and v_{i2} in Figure 3.11, while the input to the second stage (the base of transistor Q_{EF1} in Figure 3.5) is connected to v_{o1} or v_{o2} in Figure 3.11. Since a doubly-differential design is required, two complete input stages and two complete second stages are used, as shown in Figure 3.12. The common-mode stabilizing circuit is not shown, but will be added later. For now it will be assumed that the circuit is biased so that the outputs v_o^+ and v_o^- (in Figure 3.12) sit at analog ground when the inputs are all at analog ground.

The operation of the folded cascode arrangement can be explained as follows. Transistors M_{FC1} and M_{FC2} in Figure 3.12 act as current sources, supplying the bias currents to the input stages and to the current sinks Q_{FC1} and Q_{FC2} in Figure 3.12.

Figure 3.11: The Folded Cascode Arrangement

Figure 3.12: Illustration of the Use of the Folded Cascode Arrangement For Interfacing the First And Second Stages in a Doubly Differential Integrator

Figure 3.13: Simplified Schematic of the Two-Stage Integrator Showing Operation of the Circuit

Ideally, input currents to the second stages are zero at the quiescent operating point. The PMOS transistors M_{FC3} and M_{FC4} are common gate cascode devices. Output current from the input stages is fed into the low impedance nodes at the sources of M_{FC3} and M_{FC4} and is "folded over" to the high impedance nodes at the drains of these devices, and from there, out into the second stage inputs. Hence the second stages are driven by high impedance current sources as is required. This action is illustrated in Figure 3.13 which shows a simplified schematic of the entire integrator. Only one input stage is shown, and both the input and output stages are simplified. All devices which operate as current sources or sinks are shown as such.

While the use of PMOS common gate devices in the folded cascode arrangement constitutes an exception to the general BiCMOS design principle of restricting signal paths to NPN BJT's, the benefits in this case outweigh the detrimental effects. The benefits, which have already been described, included accomplishment of the required level shifting and an increased output impedance for the first stage [25] which increases

the dc gain of the integrator. The main disadvantage of their use is the addition of a high-frequency parasitic pole to the integrator transfer function. It can be shown however [18] that the single parasitic pole associated with the use of the folded cascode arrangement is located at the f_T of the cascode devices. Based on typical process and parameter values, this frequency is close to one gigahertz, and so no appreciable effects should be seen below about one hundred megahertz [26]. Finally, it should be noted that it is not possible to use NPN cascode devices, since this would require inverted forms of both the first and second stages and hence a much greater usage of both PMOS and lateral PNP devices.

The final aspect of the integrator design, the common-mode stabilization circuit, will be described next.

3.5.3 Common-Mode Stabilization

The doubly-differential two stage integrator thus far described has no means for ensuring that the common-mode output voltage remains at analog ground, as is desired. The common-mode output voltage, $v_{o,cm}$, is defined as the average of the two differential output voltages v_o^+ and v_o^- as in Figure 3.13. Thus,

$$v_{o,cm} = \frac{v_o^+ + v_o^-}{2} \quad (3.9)$$

The requirement that $v_{o,cm}$ remain at analog ground stems from several performance criteria. The integrator is designed such that a common-mode voltage of zero volts ensures that all devices are biased in their desired (usually active, high gain) operating regimes. A signal-independent common-mode voltage is synonymous with infinite common-mode input rejection and power supply rejection. Analog ground is the midpoint between the power supply rails and thus as the common-mode output voltage it maximizes output swing (and hence dynamic range). Analog ground is the required common-mode output for interfacing between integrators without additional level shifting.

The circuit which is to accomplish the task of keeping $v_{o,cm}$ at analog ground, independent of any input signals to the integrator, is the common-mode stabilization circuit. This task must also be accomplished regardless of process variations which, through their effect on transistor output impedances and other device parameters, will determine the quiescent value of $v_{o,cm}$. More importantly, process variations will affect how hard the common-mode stabilization circuit must work to maintain $v_{o,cm}$ at the desired level under quiescent operating conditions.

From the above description of the tasks which the common-mode stabilization circuit must perform, certain performance criteria can be inferred. The circuit must possess sufficient bandwidth and stability to be able to maintain $v_{o,cm}$ at analog ground in the presence of high frequency common-mode signals (such as power supply noise), and the circuit must possess sufficient operating range (current or voltage) to be able to maintain $v_{o,cm}$ at analog ground in the presence of large signal common-mode inputs and/or large process variations. In addition to these criteria, it is implicit that the common-mode stabilization circuit must operate without adversely affecting the differential operation of the integrator.

Many approaches to the design of common-mode stabilization circuitry have been reported in the literature. Most approaches make use of feedback circuitry, and can be represented by the block diagram in Figure 3.14. Implicit in this diagram is the fact that the differential-output circuit requiring the common-mode stabilization contains some means for controlling the value of $v_{o,cm}$. For example, the value of $v_{o,cm}$ in Figure 3.12 can be controlled by varying the biases V_{b1} or V_{b3} . The feedback implied in Figure 3.14 would however be positive if applied to either V_{b1} or V_{b3} in Figure 3.12 and so an inversion would be required. Similarly, the value of $v_{o,cm}$ could be controlled by controlling the bias current in the inner differential pairs of the Gilbert cells in the input stages (I_{BB} in Figure 3.6). This however would result in a situation where the common-mode stabilization circuit affects the differential operation of the integrator, since varying I_{BB} in Figure 3.6 would also affect the UGBW of the integrator.

Figure 3.14: Block Diagram Showing Conceptual Operation of a Common-Mode Stabilization Circuit

Banu, Khourry, and Tsividis have reported on an approach to the design of common-mode stabilization circuitry which ensures that most of the design criteria are automatically met, with a minimum of design effort or additional circuitry. [27] The basis of the approach is to utilize the existing differential-mode circuitry for the filter component of the common-mode stabilization circuit. By doing so, one ensures (to a certain extent) that the common-mode stabilization circuit has sufficient gain, bandwidth, and stability, since these criteria have already been met for the design of the differential-mode circuit. This approach implies that the fed-back common-mode control signal in Figure 3.14 must be applied at the front end of the circuit requiring common-mode stabilization. This approach has been used for the design of the common-mode stabilization circuit in this thesis, with one important modification. While the bandwidth of the differential-mode circuitry is sufficient for the common-mode circuitry in general-purpose op-amp applications, this is not the case in the design of transconductance integrators. This is because in general-purpose op-amps, the UGBW of the differential-mode circuitry represents the limit of useful operation of the op-amp. In transconductance integrators however, the useful operating range

Figure 3.15: Realization of the Common-Mode Sensing Circuit With Two Equal-Value Resistors

of the integrator extends beyond the UGBW of the differential-mode circuitry. Thus the common-mode stabilization circuitry would possess a bandwidth that exceeds the bandwidth of the differential-mode circuitry. The application of these principles to the doubly-differential transconductance integrator will now be described.

The first component of the common-mode stabilization circuit is the common-mode sensing circuit. The simplest realization of this circuit is a pair of equal-valued resistors, as shown in Figure 3.15. While this function can also be performed using switched-capacitor equivalents or transistor-only schemes, the resistor implementation provides a reasonable compromise between simplicity and performance. Performance is degraded by resistor mismatch, resistor non-linearity, and by the loading of the output stage which is caused by the resistors. Mismatch can be minimized by careful layout of the resistors, while loading of the output stage can be minimized by using large-valued resistors. Linearity of the resistors can be improved by using polysilicon resistors, as opposed to diffused resistors.[28]

The remainder of the necessary common-mode circuitry can be implemented, in accordance with the principles described earlier, as shown in Figure 3.16. The output of the common-mode sensing circuit is fed back to the summing nodes of the folded cascode arrangement via a third, modified input stage formed by transistors

two common-mode sensing resistors in parallel. Similarly, transistor M_{CM1} balances the differential pair by providing a load for Q_{CM1} - Q_{CM2} that is equivalent to the load seen by Q_{CM3} - Q_{CM4} .

The bandwidth of the common-mode stabilization circuit can be made larger than the bandwidth of the differential circuitry by ensuring that the transconductances of Q_{CM1} - Q_{CM4} are larger than the effective transconductances of the differential input stages. A practical limit for the bandwidth of the common-mode stabilization circuit is given by the phase margin requirements for stability (typically forty five degrees - sixty degrees) [29] and can be determined by circuit simulation.

The operating range of the common-mode stabilization circuit is in this case represented by the linear input range of the differential pair formed by Q_{CM1} - Q_{CM4} . Since no emitter degeneration resistance is used, the linear input range is about fifty millivolts, applied differentially (see Figure 2.11). Since $v_{o,cm}$ is applied single-ended, the operating range is approximately doubled to about one hundred millivolts, which was found from simulation to be sufficiently high.

This completes the description of the common-mode stabilization circuit, and of the entire integrator design. The next section will present a summary of the integrator design and rationale. Detailed analysis of the small-signal operation of the circuit will be given in the next two chapters.

3.6 Summary of Integrator Design

A schematic of the complete doubly differential two stage integrator is shown in Figure 3.17. A summary of the attributes of the design is presented below.

- It is based on the classical two-stage op-amp topology with a pole-splitting compensation scheme. This provides the following: high dc gain for accurate low-frequency integrator response, internal integrating capacitor and hence less load sensitivity, wide swing output stage for increased

dynamic range, well-understood circuit behaviour and hence ease of design.

- It utilizes tunable phase compensation through the use of a variable transconductance element (diode-connected BJT) in place of the pole-splitting resistor. This provides the ability to tune the high frequency phase response of the integrator (and by implication, the Q of a filter), and ensure a precise ninety degree phase margin.

- It utilizes bipolar differential pairs with heavy emitter degeneration and Gilbert cells for tuning the transconductance and hence the integrator UGBW. This all-bipolar input stage provides the following attributes: low-noise design for increased dynamic range, high input impedance independent of tuning, large linear input range for increased dynamic range, high slew rate capability independent of tuning, and simplified tuning of integrator UGBW where currents in second stage are not affected.

- It utilizes a folded cascode level-shifting arrangement. This wideband level-shifting scheme increases overall dc gain and facilitates the use of bipolar output drivers in conjunction with an all-bipolar (and hence low-noise) input stage. The folded cascode arrangement also facilitates the implementation of both the doubly-differential design and the common-mode stabilization circuit.

- The use of a doubly-differential design provides the following: increased power supply and common-mode rejection for increased dynamic range, cancellation of non-linearities and hence low distortion, increased output swing for increased dynamic range, less high-frequency parasitic poles due to lack of a differential to single ended converter, reduced input-referred offset.

- It utilizes wideband common-mode stabilization circuit which shares much of the same circuitry as the differential circuit and thus simplifies design.

Chapter 4

AC Small-Signal Analysis

4.1 Introduction

The ability of the modified two-stage op-amp configuration which was described in the previous chapter (or indeed, of any configuration) to provide an accurate integrator response, depends heavily on the high frequency behaviour of the poles and zeros of the transfer function. While the use of tunable elements in the integrator configuration improves the immunity of the circuit to uncertainties regarding pole and zero behaviour, a thorough understanding of the nature of this behaviour is none the less essential. With a thorough understanding comes ease of design, especially in the face of changing process parameters with which the designer will inevitably be met. As will be seen in the next chapter, the large signal performance of the integrator is also dependent on the behaviour of the poles and zeros.

The objective of this chapter is to provide a detailed look at the ac small-signal behaviour of the integrator, with an aim to achieving both intuitive understanding of the integrator behaviour and also useful design equations. Verification of the results which are obtained will be provided through simulation of simplified models. Details regarding the responses of the Gilbert cells and the folded cascode arrangement in the input stage will not be considered since these circuits are both known to be very

Figure 4.1: Use of a Common-Gate (Cascode) PMOS Transistor for Compensation with Improved PSRR

wideband circuits. [24],[18]

4.2 Origin of the Tunable Resistance Method of Compensation

The technique in which a tunable resistance in the feedback path of the second stage is used to provide tunable phase compensation for the integrator was developed from an idea first published by Gray and Meyer [18]. In this and subsequent publications [33], [34] a circuit similar to the one shown in Figure 3.3 was proposed to improve the power supply rejection ratio (PSRR) of CMOS op-amps which utilize the pole-splitting compensation technique. The proposed circuit is shown in Figure 4.1. With this configuration, a common-gate (cascode) PMOS transistor, biased in the saturation region by complementary current sources, is used in place of the standard compensation resistance to improve the negative-supply PSRR of the CMOS op-amp. This technique is referred to as cascode compensation. To the best of this author's knowledge however, no one has yet proposed that this technique be used to provide a means for allowing tunable phase lead compensation.

Figure 4.2: BiCMOS Version of an Operational Amplifier Using the Cascode Compensation Scheme

A BiCMOS version of the circuit shown in Figure 4.1 is shown in Figure 4.2. In this version, the polarity of the cascode compensation transistor is reversed so that only wideband NPN bipolar transistors are used as signal-carrying devices, and small values of the compensation resistance can readily be achieved. The small-signal model of the BiCMOS version is however essentially identical to that of the CMOS version. Not shown in Figure 4.2 are the details of the input stage or the level shifting circuit that is required in the second stage. With the BiCMOS version shown in Figure 4.2, the effective compensation resistance r_c is that seen looking back from the output of the op-amp to the input of the transistor Q_o , [18] and is thus given by the base-emitter diode resistance of Q_c . This is the same result as was obtained from the diode-connected version in the previous chapter, and so the value of r_c is as given by equation (3.3). Thus the configurations shown in Figure 4.1 and Figure 4.2 also offer the ability to tune the frequency response of the op-amp or integrator.

A fundamental difference between the cascode (common-base/common-gate) and the diode-connected compensation scheme described in Chapter 3 relates to the impedance seen looking forward from the input of the driver in the second stage

(the base of Q_o in Figure 4.2) to the output of the second stage. In the diode connected version described in Chapter 3, the value of the compensation resistance is the same in both directions. In the cascode versions illustrated in Figures 4.1 and 4.2, the value of the compensation resistance as seen looking forward from the first stage output is much higher than what is presented looking in the other direction. If one neglects the finite output impedance of Q_c in Figure 4.2 (or M_c in Figure 4.1), the result is a unidirectional compensation resistance. It will be shown that this results in a transmission zero which is strictly a left-hand plane zero.

When the circuit of Figure 4.1 was first published in [18], it was proposed that improved PSRR would arise from the fact that the left-hand side of the capacitor C_c in Figure 4.1 is connected to a virtual ground. While the source of M_c in Figure 4.1 is a low impedance node, it should not be treated as a virtual ground for the purpose of performing a high-frequency small-signal analysis of the circuit. The small-signal analysis was in fact performed based on the virtual ground assumption in [34] giving the somewhat oversimplified result that the transfer function contains only two real poles and no finite zero. In fact, a more exact analysis which will follow shortly will show that the transfer function contains at least three important poles and a finite left-hand plane zero. It can be shown however that under certain conditions, the left-hand plane zero can be made to cancel one of the poles, resulting in the transfer function reported in [34].

While the cascode compensation arrangement was not actually used in the integrator circuit with which this thesis is mainly concerned, much of the analysis which follows will in fact deal with this arrangement. This was done because of the relative novelty of the cascode arrangement, the apparent lack of widespread understanding regarding the behaviour of the circuit, and because of the potential usefulness of such a circuit. The chapter will conclude with a detailed analysis of the diode-connected compensation scheme which was described in Chapter 3.

4.3 AC Small-Signal Analysis of the Cascode Compensation Scheme

This section will explore the small-signal behaviour of the cascode compensation scheme. Different models will be looked at, with an aim to finding a model which accurately predicts the small-signal behaviour of a two stage integrator utilizing the cascode compensation scheme. As will be seen, the inclusion of even a few parasitics in the model will quickly make the resulting design equations very complex. thus the objective will be to develop a model which provides a reasonable tradeoff between complexity and accuracy.

4.3.1 The Complete Small Signal Model

The complete small signal model for a two stage integrator utilizing the cascode compensation scheme is shown in Figure 4.3. this model can be explained with reference to Figure 4.2 which shows the schematic of the integrator. The model in Figure 4.3 is essentially the composite of two hybrid-pi models (one for Q_o and one for Q_c) along with the compensation capacitor C_c , a complex load impedance (R_L in parallel with C_L), and a voltage-to-current converter $g_{m1}v_i$ in parallel with a complex source impedance (R_s in parallel with C_s) to represent the first stage. Parasitic capacitances and resistances associated with the complementary current sources I_{c1} and I_{c2} are also shown.

A cursory inspection of Figure 4.3 quickly reveals that analysis of the complete small-signal model would result in an expression for the transfer function which is very complex and of little practical worth. While one can proceed by progressively simplifying the model in Figure 4.3 until a good compromise between simplicity and accuracy is achieved, an easier approach is to begin with the most highly simplified model and then progressively reduce the number of simplifications. This approach is the one which was used, and the results will now be presented.

Figure 4.3: Complete Small-Signal Model for a Two-Stage Integrator Utilizing the Cascode Compensation Scheme

4.3.2 The Simplest Integrator Model

The simplest model for the integrator is shown in Figure 4.4. This figure actually shows two equivalent representations of the same model, one using a simplified hybrid- π model for Q_c and the other using a simplified “T” model for Q_c . The simplified “T” model in Figure 4.4c clearly shows that the compensation transistor Q_c provides what is nearly, but not quite, a virtual ground connection for the compensation capacitor C_c . The impedance to ac ground seen by C_c is actually $1/g_{mc}$ which can in theory be made to be very small. Doing so however may ultimately conflict with the use of Q_c as a tunable compensation resistance to achieve a flat ninety degree phase response.

Referring to Figure 4.4a, many simplifications have been made as compared with the complete model in Figure 4.3. All resistances have been omitted (with the exception of $r_{\pi c}$) to simplify the resulting transfer function. While this results in inaccurate modeling of the low-frequency behaviour of the circuit, it has very little effect on the prediction of high-frequency behaviour since at high frequencies, capacitive elements generally dominate the circuit behaviour. Resistive elements will be added later for

Figure 4.4: Simplest Model for a Two-Stage Integrator Utilizing the Cascode Compensation Scheme (a) Using Hybrid-Pi Model for Q_c , (b) Using T-Model for Q_c .

low-frequency modeling. The element C_i in Figure 4.4a represents the sum of all capacitance C_i associated with the input stage, the base-emitter capacitance $C_{\pi o}$ associated with Q_o , and the capacitance C_{IC1} associated with the upper complementary current source I_{C1} in Figure 4.2. Likewise, the capacitance C_o in Figure 4.4a represents the sum of all capacitive elements at the collector of Q_o . These include any load capacitance C_L , the collector-substrate capacitance C_{CS_o} associated with Q_o and capacitive elements associated with the PMOS current source which forms the active load for Q_o . The collector-base capacitances $C_{\mu o}$ and $C_{\mu c}$ have been omitted as has the capacitance C_{IC2} associated with the lower complementary current source I_{C2} in Figure 4.3 and the base-emitter capacitance $C_{\pi c}$ associated with Q_c . Finally, the direction of the voltage-controlled current source $g_{mc}v_c$ has been reversed, as has the polarity of the control voltage v_c .

Proceeding with the analysis of the simplified model in Figure 4.4a, one can apply Kirchoff's current law at the nodes labeled 1, 2 and 3 in Figure 4.4a, resulting in the equations

$$g_{m1}v_i + v_2sC_i = g_{mc}v_c \quad (4.1a)$$

$$g_{mc}v_c + v_c/r_{\pi c} + (v_c - v_o)sC_c = 0 \quad (4.1b)$$

$$(v_c - v_o)sC_c = g_{m2}v_2 + v_o sC_o \quad (4.1c)$$

These equations can be solved simultaneously to obtain the overall transfer function of the two-stage integrator

$$\frac{v_o}{v_i} = \frac{g_{mi}}{C_c} \frac{1}{s} \frac{1 + s \frac{C_c}{g_{mc}}}{1 + s \frac{C_i(C_c + C_o)}{g_{mo}C_c} + s^2 \frac{C_iC_o}{g_{mc}g_{mo}}} \quad (4.2a)$$

Equation (4.2a) predicts an ideal integrator response at low frequencies with the gain constant given by g_{mi}/C_c , a high-frequency left-hand plane zero at a frequency $f_z = g_{mc}/2\pi C_c$, and a pair of high-frequency poles which for typical parameter values may be either real or complex conjugates. By comparing the quadratic characteristic equation in (4.2a) with standard second order linear system design equations, one can identify the resonant frequency ω_n and the Q of the pole pair as

$$\omega_n = \sqrt{\frac{g_{mc}g_{mo}}{C_iC_o}} \quad (4.2b)$$

$$Q = \frac{C_c}{C_c + C_o} \sqrt{\frac{C_o g_{mo}}{C_i g_{mc}}} \quad (4.2c)$$

The accuracy of equation (4.2) in predicting the high frequency behaviour of a two-stage integrator using the cascode compensation technique was checked using the circuit simulator HSPICE and process parameters which represent a typical BiCMOS process [35]. The circuit shown in Figure 4.5a was first simulated, and the resultant operating point report from the simulator was used to obtain circuit parameters for the small-signal model which is depicted in Figure 4.5b. Relevant values for the simplified model in Figure 4.4a were then used in equation (4.2) (with the aid of the software package MATLAB) to obtain the predicted magnitude response for the integrator.

The magnitude response predicted by HSPICE and that predicted by equation (4.2a) are shown together in Figure 4.6 for comparison. As expected, the low-frequency response predicted by equation (4.2) is inaccurate because of the omission of all resistive elements from the simplified model. However, Figure 4.6 shows that the high frequency behaviour of the integrator is quite closely modeled by equation (4.2), with only a slight underestimate of the Q of the complex pole pair, and a slight

overestimate of the resonant frequency. These inaccuracies are perhaps outweighed however by the simplicity of the design equations represented by equation (4.2).

4.3.3 Substitution of $C_{\pi c}$ for $r_{\pi c}$

A more accurate model for the cascode-compensated integrator can be obtained, without compromising the simplicity of the design equations, simply by substituting $C_{\pi c}$ for $r_{\pi c}$ in Figure 4.4. This makes intuitive sense because at very high frequencies, $r_{\pi c} \gg 1/\omega C_{\pi c}$ and so $C_{\pi c}$ dominates $r_{\pi c}$.

Substituting $1/SC_{\pi c}$ for $r_{\pi c}$ in equation (4.1) and solving for the transfer function yields

$$\frac{v_o}{v_i} = \frac{g_{mi}}{C_c} \frac{1}{s} \frac{1 + s \frac{C_c + C_{\pi c}}{g_{mc}}}{1 + s \frac{C_i(C_c + C_o)}{g_{mo}C_c} + s^2 \frac{C_i(C_oC_c + C_oC_{\pi c} + C_cC_{\pi c})}{g_{mc}g_{mo}C_c}} \quad (4.3a)$$

$$\omega_n = \sqrt{\frac{g_{mc}g_{mo}C_c}{C_i(C_oC_c + C_oC_{\pi c} + C_cC_{\pi c})}} \quad (4.3b)$$

$$Q = \frac{1}{C_c + C_o} \sqrt{\frac{g_{mo}C_c(C_oC_c + C_oC_{\pi c} + C_cC_{\pi c})}{g_{mc}C_i}} \quad (4.3c)$$

Equation (4.3) shows that $C_{\pi c}$ affects the frequency of the left-hand plan zero as well as the resonant frequency and Q of the complex pole pair. Applying equation (4.3a) to the simplified integrator model in Figure 4.5 results in the magnitude response shown in Figure 4.7. Also shown in Figure 4.7 are the response predicted by equation (4.2a) and that predicted by HSPICE. As can be seen, the use of $C_{\pi c}$ instead of $r_{\pi c}$ in the simplified integrator model of Figure 4.4a results in a slightly more accurate prediction of the high-frequency behaviour. This improvement is achieved without compromising the simplicity of the design equations to any great extent.

4.3.4 Inclusion of r_{bc} with $C_{\pi c}$

Exploratory simulation of the integrator model in Figure 4.5a using HSPICE revealed that the Q of the complex pole pair is highly dependent on the extrinsic base resistance of the bipolar transistors. The larger was the base resistance of the BJT's,

(a)

(b)

Figure 4.5: Model Used for Checking Accuracy of Simplified Small-Signal Models (a) Schematic of Simulation Model Used with HSPICE. Including Parameters Provided by HSPICE (b) Small-Signal Model with Parameters from (a)

Figure 4.6: Magnitude Response of the Simplified Integrator as Predicted by Equation (4.2a) and Compared to the Response Predicted by HSPICE

the higher was the Q predicted by HSPICE. Based on this insight, the simplified small-signal model of the integrator was altered to include the extrinsic base resistance r_{bc} associated with the cascode compensation transistor Q_c . This model is shown in Figure 4.8. Applying Kirchoff's current law at nodes 1, 2 and 3 in Figure 4.8 and solving the three equations simultaneously results in the transfer function

$$\frac{v_o}{v_i} = \frac{g_{m1}}{C_c} \frac{1 + s \frac{C_c + C_{\pi c}}{g_{mc}} + s^2 \frac{C_c C_{\pi c} r_{bc}}{g_{mc}}}{s \left(1 + s \frac{C_1(C_c + C_o)}{g_{m0} C_c} + s^2 \frac{C_1(C_o C_c + C_o C_{\pi c} + C_c C_{\pi c})}{g_{mc} g_{m0} C_c} + s^3 \frac{C_2 C_1 C_{\pi c} r_{bc}}{g_{mc} g_{m0}} \right)} \quad (4.4)$$

As might have been expected, the inclusion of r_{bc} with $C_{\pi c}$ has increased the order of the transfer function. The denominator of equation (4.4) reveals the addition of a fourth pole, while the numerator reveals the addition of a second zero. It can be shown that for the typical parameter values given in Figure 4.5, the numerator of equation

Figure 4.7: Magnitude Response of the Simplified Integrator as Predicted by Equation (4.3a) and Compared to the Response Predicted by HSPICE and to the Response Predicted by Equation (4.2a)

(4.4) predicts two real, distinct left-hand plane zeros, one being at the frequency predicted by the previous model, and a second one being at a much higher frequency. The magnitude response predicted by equation (4.4) is shown in Figure 4.9, along with the response predicted by HSPICE. As can be seen, the result is an overestimation of the Q of the complex pole pair. Since this model still does not accurately predict the high-frequency response of the integrator and is also considerably more complex, it is not thought to be particularly useful.

The insight which was gained from this model can however be used to modify the simplified model described in the previous sub-section in a manner that improves the accuracy of the predictions which result at high frequencies. Since it was found that

Figure 4.8: Simplified Small-Signal Model of the Integrator Including Extrinsic Base Resistance r_{bc} Associated with Q_c

the Q of the complex pole pair is dependent on r_{bc} , one can modify equation (4.3) by including an empirical factor γ which is proportional to the extrinsic base resistance of the BJT's in the process being considered. Equation (4.3) would then be re-written as

$$\frac{v_o}{v_i} = \frac{g_{m1}}{C_c} \frac{1 + s \frac{C_c + C_{\pi c}}{g_{mc}}}{s \left(1 + s \frac{C_1(C_c + C_o)}{\gamma g_{mo} C_c} + s^2 \frac{C_1(C_o C_c + C_o C_{\pi c} + C_c C_{\pi c})}{g_{mc} g_{mo} C_c} \right)} \quad (4.5a)$$

$$\omega_n = \sqrt{\frac{g_{mc} g_{mo} C_c}{C_1(C_o C_c + C_o C_{\pi c} + C_c C_{\pi c})}} \quad (4.5b)$$

$$Q = \frac{\gamma}{C_c + C_o} \sqrt{\frac{g_{mo} C_c (C_o C_c + C_o C_{\pi c} + C_c C_{\pi c})}{g_{mc} C_1}} \quad (4.5c)$$

where γ is proportional to r_{bc} .

4.3.5 Modeling Low Frequency Behaviour

So far, the attempts at modeling the cascode-compensated integrator have focused on the high-frequency behaviour. To this end, most resistive elements have been left out of the simplified model as the high-frequency behaviour is dominated by capacitive elements. In order to model the low-frequency behaviour, it is necessary to include resistive elements at both the input and the output of the integrator. A model which includes these elements is shown in Figure 4.10.

In Figure 4.10 the input resistance R_i is composed of the parallel combination of the source resistance R_s , associated with the input stage, the finite output resistance R_{IC1} of the upper complementary current source I_{C1} , and the intrinsic base resistance

Figure 4.9: Magnitude Response of the Simplified Integrator as Predicted by Equation (4.4) and Compared to the Response Predicted by HSPICE

$r_{\pi o}$ of the output driver Q_o . These elements can all be seen in the complete model shown in Figure 4.3. In a similar fashion, R_o in Figure 4.10 accounts for the parallel combination of all resistive elements at the output of the integrator as seen in the complete model of Figure 4.3. These include the finite output resistance r_{o,Q_o} and r_{o,M_o} of the output driver Q , and the PMOS active load M_o respectively, as well as the resistive component R_L of the load impedance. The rest of the elements in Figure 4.10 are as per the simplified model described in section 4.3.2.

Solving for the transfer function of the model in Figure 4.10, one obtains

$$\frac{v_o}{v_i} = \frac{R_i R_o g_{mi} g_{mo} (1 + s \frac{C_c}{g_{inc}})}{1 + B_1 s + B_2 s^2 + B_3 s^3} \quad (4.6a)$$

Figure 4.10: Simplified Model of the Integrator Including Resistive Elements at the Input and Output

where

$$B_1 = R_i C_i + \frac{C_c}{g_{mc}} + R_o (C_c + C_o) + R_i R_o g_{mo} C_c \quad (4.6b)$$

$$B_2 = R_i C_i \left(\frac{C_c}{g_{mc}} + R_o (C_c + C_o) \right) + \frac{R_o C_c C_o}{g_{mc}} \quad (4.6c)$$

$$B_3 = \frac{R_i R_o C_i C_o C_c}{g_{mc}} \quad (4.6d)$$

The predicted magnitude response given by equation (4.6) is shown in Figure 4.11 along with the response predicted by HSPICE. The basis for comparison is again the model shown in Figure 4.5.

The comparisons shown in Figure 4.11 indicate that inclusion of R_i and R_o in Figure 4.10 provides for very accurate modeling of the low-frequency behaviour of the integrator. Comparing Figure 4.11 to Figure 4.6 reveals that, as expected, modeling of the high-frequency behaviour is not affected by the inclusion of the resistive elements. At the same time however, the design equation represented by equation (4.6) is somewhat more cumbersome to use than those represented by equations (4.2) and (4.3). This situation can be remedied however if one combines the low-frequency information conveyed by equation (4.6) with the high-frequency information conveyed by equations (4.2) and (4.3). The useful information which exists in equation (4.6) is the dc gain A_o of the integrator. Setting $s=0$ in equation (4.6), one finds

$$A_o = R_i R_o g_{mi} g_{mo} \quad (4.7)$$

Figure 4.11: Magnitude Response of the Simplified Integrator as Predicted by Equation (4.6) and Compared to the Response Predicted by HSPICE

In equation (4.2) and (4.3), the UGBW of the integrator is given by the gain constant associated with the $1/s$ term. Thus, the integrator UGBW is given by

$$UGBW = \frac{g_{m1}}{C_c} \quad (4.8)$$

Using the well known relationships

$$\omega_{p1} = \frac{UGBW}{A_o} \quad (4.9)$$

and

$$F(s) = \frac{A_o}{1 + \frac{s}{\omega_{p1}}} \quad (4.10)$$

for a dominant pole system $F(s)$ with dominant pole frequency ω_{p1} , one can then

combine equations (4.7), (4.8), (4.9) and (4.10) to yield the result

$$F(s) = \frac{R_i R_o g_{mi} g_{mo}}{1 + s(R_i R_o g_{mo} C_c)} \quad (4.11)$$

Combining equation (4.11) with the high-frequency pole pair information in equation (4.3) yields the final result

$$\frac{v_o}{v_i} = \frac{R_i R_o g_{mi} g_{mo}}{1 + s(R_i R_o g_{mo} C_c)} \frac{1 + s \frac{C_c + C_{\pi c}}{g_{mc}}}{1 + s \frac{C_i(C_c + C_o)}{g_{mo} C_c} + s^2 \frac{C_i(C_o C_c + C_o C_{\pi c} + C_c C_{\pi c})}{g_{mc} g_{mo} C_c}} \quad (4.12)$$

which contains both the high-frequency and low-frequency information concerning the frequency response of the integrator. Equation (4.3b) and (4.3c) can still be used in conjunction with (4.12).

The magnitude response of the integrator model in Figure 4.5 as predicted by equation (4.12) is shown in Figure 4.12 along with the response predicted by HSPICE. As can be seen, equation (4.12) provides very good modeling of both the high and low-frequency response, while still representing a design equation which is easy to use.

4.3.6 The Cascode-Compensated Integrator as a Two-Pole System

In section 4.2, it was mentioned that a small-signal analysis of the cascode-compensated op-amp in Figure 4.1 has been reported in the literature. [34] The results of this analysis had shown the circuit to possess a simple two-pole transfer function. While the analysis which has just been presented shows that at least three important poles and one finite left-hand plane zero exist, it is instructive to see how the single two-pole result can be arrived at. In fact, it will be shown that this result can be arrived at in two different ways.

If one takes the expression in equation (4.2a) for the integrator transfer function and assumes that the two poles given by the quadratic in the denominator are real and widely spaced, then the quadratic denominator $D(s)$ can be expressed in the

Figure 4.12: Magnitude Response of the Simplified Integrator as Predicted by Equation (4.12) and Compared to the Response Predicted by HSPICE

form

$$D(s) = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) \quad (4.13)$$

where p_1 and p_2 are the two pole frequencies. Multiplying out equation (4.13) gives

$$D(s) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1 p_2} \quad (4.14)$$

Assuming that p_1 is at a much lower frequency than p_2 , equation (4.14) can be rewritten as

$$D(s) \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1 p_2} \quad (4.15)$$

Identifying the terms in 4.15 with those in the quadratic denominator of equation

(4.2a), one obtains the result

$$p_1 \approx \frac{-g_{m0}C_c}{C_1(C_c + C_o)} \quad (4.16a)$$

$$p_1 \approx \frac{-g_{mc}(C_c + C_o)}{C_c C_o} \quad (4.16b)$$

Since the frequency of the left-hand plane zero given by equation (4.2a) is g_{mc}/C_c , one can readily see from equation (4.16b) that for $C_o \gg C_c$, the left-hand plane zero and p_2 will be approximately coincident and will cancel, leaving a simple two-pole transfer function (the two poles being the dominant pole given by equation (4.9) and a high-frequency pole given by equation (4.16a)). The author in [34] has correctly pointed out that this result implies that a cascode-compensated op-amp can drive very large capacitive loads without becoming unstable.

It is interesting to note that the simple two pole result can also be arrived at under a different set of assumptions. If in the small-signal model shown in Figure 4.4b the transconductance of Q_c is made very large, then the result is the model shown in Figure 4.13. In this case, the emitter of Q_c has become a virtual ground for C_c and any current flowing into the emitter of Q_c flows out the collector of Q_c into the base of Q_o . Thus one can see that while feedback does occur, no feed-forward occurs and so the transmission zero has been eliminated. Solving for the transfer function in Figure 4.13, one obtains

$$\frac{v_o}{v_i} = \frac{g_{m1}}{C_c} \frac{1}{s} \frac{1}{1 + s \frac{C_1(C_c + C_o)}{g_{m0}C_c}} \quad (4.17)$$

which is the same result which was obtained for $C_o \gg C_c$.

4.4 The Diode-Connected Tunable Resistance

The tunable compensation scheme just described involving the cascode-connected compensation transistor was originally explored as a candidate for the tunable transconductance integrator. However, it was found that for reasons which will be explained in this section, the diode-connected version is a more suitable one for this application.

Figure 4.13: Simplified Model of the Cascode-Compensated Integrator when the Transconductance of Q_c is Assumed Very Large

In this section, the ac small-signal analysis of the integrator using the diode-connected compensation scheme will be performed, and the results compared to those for the cascode compensation scheme. Implications of the small-signal model on large-signal behaviour in the integrator will also be explored.

4.4.1 AC Small-Signal Analysis of the Diode-Connected Compensation Scheme

A simplified high-frequency, small-signal model of an integrator using the diode-connected compensation scheme is shown in Figure 4.14. This model corresponds to the compensation circuit shown in Figure 3.3, which was used in the integrator topology selected in Chapter 3. From a cursory inspection, it can be seen that the diode connected transistor (represented by the voltage-controlled current source $g_{mc}(v_c - v_2)$ and base-emitter capacitance $C_{\pi c}$) behaves almost exactly like a resistor of value $1/g_{mc}$. The only deviation from this is the presence of the capacitor $C_{\pi c}$ connected across the resistance. For typical process circuit parameters however, the conductance of the voltage-controlled current source is much higher than the conductance of $C_{\pi c}$ for frequencies up to several hundred megahertz. Thus an integrator which utilizes the diode-connected compensation scheme would be expected to show small-signal behaviour which is identical to one using a simple resistor for compensation, up to very high frequencies. This equivalence has in fact been demonstrated

Figure 4.14: Simplified Small-Signal Model of an Integrator Using the Diode-Connected Compensation Scheme

using simulations of integrator circuits which are identical except for the fact that one uses a simple compensation resistance R_c and one uses a diode-connected npn transistor Q_c configured as in Figure 3.3 with $g_{mc} = 1/R_c$.

If one chooses to disregard the base emitter capacitance $C_{\pi c}$ in Figure 4.14, then the small signal model is identical to the one shown in Figure 3.1 with the substitution of $1/g_{mc}$ for R_c . This simplification was used for the initial design of the integrator, as described in Chapter 3. The relevant design equations are those given in equation (3.1), again with the substitution of $1/g_{mc}$ for R_c . It should be pointed out however that the design equations given in equation (3.1) assume three real, widely-spaced poles. For practical process and circuit parameters, the two high-frequency poles given in equation (3.1) may in fact be complex conjugates. A more precise (and more cumbersome) design equation, which can be obtained by solving for the transfer function in Figure 4.14 with $C_{\pi c}$ omitted, is

$$\frac{v_o}{v_i} = \frac{R_i R_o g_{mi} g_{mo}}{1 + s(g_{mo} R_i R_o C_c)} \frac{1 + sC_c(\frac{1}{g_{mc}} - \frac{1}{g_{mo}})}{1 + s \frac{C_i C_o + C_i C_c + C_o C_c}{g_{mo} C_c} + s^2 \frac{C_i C_o}{g_{mc} g_{mo}}} \quad (4.18)$$

The decision to disregard $C_{\pi c}$ in Figure 4.14 is generally a prudent one, as was discussed, assuming that a bipolar transistor is used for the diode-connected compensation transistor Q_c . This is because, as was explained in Chapter 2, bipolar transistors have much smaller parasitic capacitances than do MOS transistors for a given transconductance. However, in the next chapter, it will be shown that for reasons pertaining to large-signal performance, it may actually be desirable to use

a large MOS transistor instead of a bipolar transistor. In this case, the capacitance $C_{\pi c}$ in Figure 4.14 would be replaced by a much larger capacitance representing the sum of the gate-source, gate-bulk, drain-source, and drain-bulk capacitances of the diode-connected MOS transistor. Analysis of the full model in Figure 4.14 would then be prudent. This analysis yields the result

$$\frac{v_o}{v_i} = \frac{g_{m1}}{C_c} \frac{1}{s} \frac{1 + sC_c\left(\frac{1}{g_{mc}} - \frac{1}{g_{mo}}\right) - s^2 \frac{C_c C_{\pi c}}{g_{mo} g_{mc}}}{1 + s\left(\frac{g_{mc} C_c (C_i + C_o) + g_{mo} C_{\pi c} C_c + g_{mc} C_i C_o}{g_{mo} g_{mc} C_c}\right) + s^2 \frac{C_i C_o + C_{\pi c} (C_i + C_o)}{g_{mc} g_{mo}}} \quad (4.19)$$

Equation (4.19) shows that $C_{\pi c}$ affects the high-frequency poles and also introduces a second, high-frequency transmission zero. Assuming that a dominant left-hand plane zero exists (justifiable for $g_{mo} > g_{mc}$ since a left-hand plane zero is seen in equation (4.18)), the numerator in equation (4.19) can be manipulated to reveal the two zero frequencies z_1 and z_2 :

$$z_1 \approx \frac{-1}{C_c\left(\frac{1}{g_{mc}} - \frac{1}{g_{mo}}\right)} \quad (4.20a)$$

$$z_2 \approx \frac{g_{mo} - g_{mc}}{C_{\pi c}} \quad (4.20b)$$

The first zero given by equation (4.20a) is the same as what is found if $C_{\pi c}$ is omitted and is a left-hand plane zero for $g_{mo} > g_{mc}$. The second zero would then be a right-hand plane zero and so would contribute phase lag at high frequencies.

4.4.2 Comparison of the Diode-Connected and Cascode Compensation Schemes

Comparing equations (4.2) and (4.18), two important differences between the small-signal behaviours of integrators using the diode-connected and cascode compensation schemes can be seen. The first difference concerns the nature of the transmission zero in the transfer function. With the cascode compensation scheme, the transmission zero is strictly a left-hand plane zero while in the case of the diode-connected compensation scheme, the transmission zero can be either a left or right-hand plane zero.

A second, more subtle difference between the two compensation schemes concerns the behaviour of the high-frequency poles in the respective integrator transfer functions. Substitution of the parameter values given in Figure 4.5b into equations (4.2) and (4.18) and subsequent analysis reveals that both transfer functions contain complex conjugate pole pairs with equal resonant frequencies. In the case of the cascode-compensated integrator however, the Q of the complex pole pair is approximately twice what it is in the case of the integrator using the diode-connected compensation scheme. The higher Q can cause excessive peaking in the magnitude responses of both the common-mode and difference mode signal paths. This was in fact found to be the case, resulting in the decision to use the diode-connected compensation scheme.

4.4.3 The Transfer Function of the Integrator as a Cascade of Two Stages

In classical text-book treatments of the pole-splitting op-amp/integrator, the two-stage circuit is generally treated as a single gain stage, with no attention given to the internal node where the two stages are joined. In the next chapter, where large signal behaviour of the two-stage integrator will be discussed, it will be shown that the individual frequency response characteristics of the two stages affects the way the integrator distorts large signals. Thus in this section, an approximate analysis will be performed to obtain insight into the frequency response characteristics of the two stages, and specifically, to determine what gain signals at the integrator input experience to the input of the second stage.

Figure 4.15a shows an approximate small-signal model of the two stage integrator using only capacitive feedback for compensation. This model will be dealt with as opposed to the one with both capacitive and resistive feedback, as it simplifies analysis but still shows the general behaviour of the two stages when Miller-compensation is used. In Figure 4.15b, Miller's theorem has been applied to the model in order to un-

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Figure 4.15: Approximate Small-Signal Model of the Two-Stage Integrator (a) as Two Capacitively-Coupled Stages, (b) After application of Miller's Theorem

couple the two stages. Miller's theorem states that a floating admittance Y connected between two nodes V_1 and V_2 , can be represented by two grounded admittances Y_1 and Y_2 at nodes V_1 and V_2 respectively, where the quantities Y , Y_1 , Y_2 , V_1 and V_2 are related by

$$Y_1 = Y(1 - A) \quad (2.21a)$$

$$Y_2 = Y\left(1 - \frac{1}{A}\right) \quad (2.21b)$$

where A is defined as the ratio V_2/V_1 . The criteria for equivalence is that the currents flowing into nodes V_1 and V_2 (and hence the admittances at these nodes) are identical in both cases. This theorem is illustrated in Figure 4.16. In Figure 4.15b, Miller's theorem has been applied to the capacitance C_c , where the factor A in equation (4.21) is the gain A_2 of the second stage of the integrator.

To solve for the two transfer functions $A_2 = v_o/v_2$ and $A_1 = v_2/v_i$ in Figure 4.15b, one proceeds as follows: For the second stage, we have

$$A_2 = -g_{m2}Z_o$$

Figure 4.16: Illustration of Miller's Theorem

where Z_o equals R_o in parallel with C'_o . Thus,

$$A_2 = \frac{-g_{mo}R_o}{1 + sR_o(C_o + C_c(1 - \frac{1}{A_2}))}$$

Solving for A_2 , one obtains

$$A_2 = \frac{-g_{mo}R_o(1 - s\frac{C_c}{g_{mo}})}{1 + sR_o(C_c + C_o)} \quad (2.22a)$$

For the first stage, we have

$$A_1 = -g_{mi}Z_i$$

where Z_i equals R_i in parallel with C'_i . Thus,

$$A_1 = \frac{-g_{mi}R_i}{1 + sR_i(C_i + C_c(1 - A_2))}$$

where A_2 is given by equation (4.22a). Substituting and solving for A_1 , one obtains

$$A_1 = \frac{-g_{mi}R_i(1 + sR_o(C_c + C_o))}{1 + s(R_o(C_c + C_o) + R_i(C_i + C_c g_{mo} R_o)) + s^2(R_i R_o(C_c C_i + C_c C_o + C_o C_i))} \quad (4.22b)$$

If one multiplies equation (4.22a) by (4.22b), the result is the overall transfer function v_o/v_i and is identical to what is obtained using classical approaches. [36]

Thus the two poles of the overall integrator transfer function, as given by equation (2.7), can be identified as being in the transfer function of the first stage. The approximate shapes of the magnitude responses associated with the first and second

Figure 4.17: Approximate Magnitude Responses of the Two Gain Stages and of the Overall Integrator

stages and of the overall integrator are shown in Figure 4.17. An interesting point to note is that the pole in the second stage transfer function corresponds to a zero in the first stage transfer function, and occurs when the Miller-multiplied capacitance at the output of the first stage begins decreasing. This pole-zero combination is not seen in the overall transfer function.

With regard to the large-signal operation of a Miller-compensated integrator, Figure 4.17 shows how much gain signals at the integrator input experience to the input of the second stage. At frequencies near the integrator UGBW, this gain can be significant depending on circuit parameters, causing distortion of the signal. The implications of this phenomena on the large-signal performance of the integrator will be discussed in the next chapter.

4.5 The Emitter-Follower in the Second Stage

In Chapter 3 it was explained how an emitter-follower was required for level shifting purposes in the second stage of the integrator. Because the emitter-follower acts

Figure 4.18: Approximate Small-Signal Model of the Integrator with the Emitter-Follower in Place in the Second Stage

as a very wideband unity-gain buffer, the effect on the high-frequency small-signal performance of the integrator has not been discussed so far. However, two aspects of the emitter-follower behaviour need to be considered. The first concerns the effect that the emitter-follower has on the input resistance of the second stage, and the second concerns the high-frequency behaviour of the emitter-follower.

Figure 4.18 shows the approximate small-signal model for the integrator with the emitter-follower in place in the second stage (see Figure 3.5). The emitter-follower is represented in Figure 4.18 by a simplified hybrid-pi model consisting of intrinsic base resistance $r_{\pi EF}$ and a VCCS of value $g_{mEF}v_{\pi}$. Only capacitive feedback C_c is considered for the sake of simplicity, but the results which will be obtained can be applied to the case where a resistor R_c or a diode-connected transistor Q_c is included in series with C_c .

The effect of the emitter-follower on the input impedance of the second stage, and ultimately, on the dc gain and dominant pole frequency of the integrator can be determined by solving for the transfer function in Figure 4.18 with all capacitors replaced by open circuits. Doing this, one obtains the result

$$\frac{v_o}{v_i} \Big|_{dc} \approx \frac{g_{m1}g_{m2}R_sR_o}{1 + \frac{I_o}{I_{EF}} \frac{g_{m1}R_s}{\beta_{EF}^2}} \quad (4.23)$$

where I_o and I_{EF} are the collector currents in the output driver Q_o and the emitter-follower Q_{EF} respectively. Comparing this result with the result given in equation (4.7) for the dc gain of an integrator without the emitter-follower, one sees that for

large values of β and small values of I_o/I_{EF} , inclusion of the emitter-follower raises the dc gain by approximately R_o/R_i . Since R_o is the relatively high output resistance of the first stage and R_i is the relatively low parallel combination of R_o with the intrinsic base resistance $r_{\pi o}$ of the output driver Q_o , the dc gain of the integrator is raised significantly by the inclusion of the emitter-follower.

The above result can also be arrived at in an intuitive manner. With the inclusion of the emitter follower, the input resistance of the second stage is made so large relative to the output resistance of the first stage that the parallel combination of the two is approximately equal to the output resistance of the first stage. Thus the value R_i which represents the parallel combination of the two resistances in equation (4.7) is replaced by R_o .

An ac analysis of the high-frequency equivalent of Figure 4.18 (ie: with R_s and R_o omitted) reveals that for large values of β , the high-frequency pole-zero behaviour of the integrator is not significantly affected by the inclusion of the emitter-follower. The dominant-pole frequency will however be lowered by the same amount that the dc gain is increased, that is, by approximately R_o/R_i .

If one performs an ac analysis of a more complete model of the integrator however with the emitter-follower in place, the result will be that the transfer function will be seen to contain four important poles. [16]

The root locus for this model is shown in Figure 4.19 with the arrows indicating movement of the poles for increasing g_{mo} . This figure illustrates how, if one attempts to make the integrator very wideband by increasing the current I_o in the output driver too much, the transfer function can contain a pair of underdamped poles. This may lead to peaking or even oscillation. As well, interaction with other poles must be considered. Other types of improper design, including too-small a current in the emitter follower, may also lead to the same problem.

While the result indicated in Figure 4.19 can be achieved by direct hand analysis of a more complete model of the integrator, the resulting equation would be quite

Figure 4.19: Approximate Root Locus for the Integrator with the Emitter-Follower in Place in the Second Stage

cumbersome. A more practical approach is to use computer simulation of the circuit, while being aware of the problems which may arise.

Chapter 5

Large-Signal Behaviour

5.1 Introduction

The previous chapter presented an analysis of the small signal behaviour of the two-stage integrator. While small-signal ac models provide a useful basis for circuit design, careful consideration must also be given to large-signal circuit behaviour. This is necessary because finite signal swings cause device parameters to vary from quiescent values, due to non-linearity, producing variations in the transfer function of the circuit. Finite bias currents and rail voltages in the circuit are another source of non-linear behaviour. While a certain amount of non-linear behaviour will be present for any finite signal level, the degree to which it affects circuit performance can be controlled through careful design. As has been mentioned in previous chapters, large-signal considerations are particularly important in transconductance integrator design since transconductance integrators operate open-loop, without the benefit of feedback to hold signal levels down at the inputs of the integrator.

A complete large-signal analysis of any practical circuit is generally a prohibitively complex undertaking and is best left to circuit simulators such as SPICE. However, potential problems can be spotted in advance and avoided if the designer considers the large-signal behaviour of even highly-simplified models of the circuit that is being

designed.

This chapter will present a brief discussion of the large-signal operation of the integrator topology which has been chosen. Emphasis will be placed on identifying performance limitations which are related to large-signal operation. A complete quantitative analysis is beyond the scope of this thesis, so the discussion which follows will be qualitative in nature, with a few areas being discussed in greater detail.

5.2 Slew Rate Limitations in the Two Stage Integrator

While the transconductance integrator context generally implies that signals are continuous and hence that slew rates would appear to be of little significance, situations may arise where slew rate limitations become important. One such situation is when high-frequency, large-signal inputs are present. A second such situation is when the input signal contains step components. Both of these situations will be discussed, once the origin and nature of slew rate limitations in the chosen integrator topology have been identified.

5.2.1 General Slew Rate Limitations

The origins of slew rate limiting in a two-stage integrator or op-amp can be seen by considering the simple model in Figure 5.1. In this figure, the voltage to current converter in the input stage is capable of supplying a maximum current of value I_i to the compensation (integrating) capacitor C_c . At the same time, the output stage can supply a maximum current of value I_o to the capacitor C_c . As long as I_o is greater than I_i (as is generally the case in well-designed integrators and op-amps [16]), the maximum rate at which the output voltage can change will be determined by the maximum amount of current available from the input stage, and will be given by the

Figure 5.1: Simple Model of the Two-Stage Integrator Showing The Origin of Slew Rate Limitations

well-known voltage-current relationship for a capacitor

$$\left. \frac{dv_o}{dt} \right|_{\max} = \frac{I_i}{C_c} \quad (5.1)$$

Here it is also assumed that parasitic capacitances are negligible compared to C_c so that the maximum slew rate given by equation (5.1) is in fact determined by C_c . Thus it is seen that slew rate limiting occurs when the finite bias currents in the input stage limit the speed at which the output voltage can change.

The maximum value of I_i in equation (5.1) that is available to charge the capacitor C_c can be determined from the simplified model of the integrator shown in Figure 5.2. The biasing levels shown there will be assumed for now, but will be discussed later. If a large step input is applied at v_i as shown in Figure 5.2, then the entire tail current $2I$ in the differential pair will be switched to the device Q_{11} . A current of value I will then be drawn from the integrating capacitor associated with v_o^+ , while an equal current will be supplied to the integrating capacitor associated with v_o^- . Thus it can be seen that v_o^+ will ramp up at the same rate that v_o^- ramps down, and the maximum slew rate for the integrator when the output is taken differentially across the two outputs is thus given by

$$SR = \left. \frac{d(v_o^+ - v_o^-)}{dt} \right|_{\max} = \frac{2I}{C_c} \quad (5.2)$$

Figure 5.2: Simplified Model of the Two-Stage Integrator For Calculating Slew Rate

since equation (5.1) applies to both v_o^+ and v_o^- with $I_i=I$. From symmetry, the same results would be obtained for a large negative step to the inputs.

The bias currents for the folded cascode arrangement which are depicted in Figure 5.2 are the minimum currents necessary for allowing the input stage differential pair to be switched completely one way or the other. In actual fact, it will be shown later that these currents should be increased to minimize distortion in the integrator. Direct application of the biasing scheme depicted in Figure 5.2 to the doubly-differential common-mode stabilized integrator topology which has been selected yields the arrangement which is shown in Figure 5.3. Note that this arrangement allows only one input stage to be over-driven at a time.

It should be emphasized that unless the inputs are actually over-driven so that current in the differential pair is completely switched, the integrator is not being slew rate limited and is in fact operating in an approximately linear fashion. This approximately-linear mode of operation will now be discussed.

Figure 5.4: The Behaviour of the Two-Stage Integrator for Small Step Inputs

sides, one obtains the alternate form of the well known voltage-current relationship for a capacitor

$$v_o = \frac{1}{C_c} \int I_i dt \quad (5.3)$$

Substituting into equation (5.3) the value of I_i depicted in Figure 5.4, one obtains for the positive output

$$v_o^+ = \frac{G_{m,eff}}{2C_c} \int v_i dt \quad (5.4)$$

As with the maximum slew rate in section 5.2.1, the result given by equation (5.4) is doubled when one takes the output differentially. Thus, the differential output voltage is given by

$$(v_o^+ - v_o^-) = \frac{G_{m,eff}}{C_c} \int v_i dt \quad (5.5)$$

which indicates that the required integrating action will occur. As can be seen in Figure 5.4 however, equation (5.5) will only hold until such a time that the output reaches $v_o = A_v v_i$, where A_v is the overall dc gain of the integrator (assuming here that v_i is small enough to keep $v_o = A_v v_i$ within the linear operating range of the integrator, i.e: the devices at the outputs do not saturate). Since both the slope and the final value of the output are known, the period of time Δt over which equation

(5.5) is valid can be found to be

$$\Delta t = \frac{A_v}{G_{m,eff}/C_c} \quad (5.6)$$

Equation (5.6) states that when a voltage step of magnitude less than $I_{EE}R_{EE}$ is applied to the integrator, the output will give a valid result for a period of time equal to the product of the dc gain of the integrator and the time constant of the integrator.

5.2.3 Slew Rate Limiting at High Frequencies

The slew rate limiting which has so far been discussed has in fact involved high frequency signals, since step inputs contain high frequency components. Now the case will be considered when the input is a high-frequency continuous-time signal such as a sinusoidal voltage. It will be shown that if the signal has a large peak amplitude, slew rate limiting will occur along with the associated distortion.

If one considers the integrator being driven by a sinusoidal input such that the integrator is trying to produce an output $v_o(t) = V_p \sin(\omega t)$, then the required rate of change of the output is

$$\frac{dv_o(t)}{dt} = \omega V_p \cos(\omega t) \quad (5.7)$$

which has a maximum value when $\cos(\omega t) = 1$. Thus, one obtains from equation (5.8)

$$\left. \frac{dv_o(t)}{dt} \right|_{max} = \omega V_p \quad (5.8)$$

Setting equations (5.9) and (5.2) to be equal, and rearranging, one obtains the result that the maximum frequency ω_{max} which the integrator can handle without distortion due to slew rate limiting is given by

$$\omega_{max} = \frac{SR}{V_p} \quad (5.9)$$

If one defines V_p to be the maximum allowable output swing of the integrator, then equation (5.10) gives what is referred to as the full-power bandwidth of the integrator. [16] Typically, the full-power bandwidth of the integrator is less than the UGBW,

with the result that the maximum allowable amplitude of signals near the frequency of the integrator UGBW will be limited not by distortion due to device saturation at the output but by the distortion associated with slew rate limiting. It should be noted here that transconductance filters are unusual in that their region of filtering is located near the integrator UGBW. Thus, performance limitations due to full-power bandwidth are particularly important in transconductance integrator design.

5.2.4 Effect of Finite Second Stage Gain

In the derivation of equation (5.1), it was assumed that the second stage of the integrator possessed infinite voltage gain, and thus that the input to the second stage was a true virtual ground. For the case of finite second stage voltage gain, equation (5.1) should be re-written as

$$\frac{dv_o(1 - 1/A_{v2})}{dt} \Big|_{max} = \frac{I_1}{C_c} \quad (5.10)$$

since the voltage across the capacitor in Figure 5.4 is, by inspection, $v_c = v_o(1 - 1/A_{v2})$. If A_{v2} is assumed to be constant, then the equations which were developed from equation (5.1) can be corrected simply by substituting $v_o(1 - 1/A_{v2})$ for v_o . However A_{v2} will in fact vary in a non-linear fashion as a function of v_o . This is an unwanted non-linearity which will cause the magnitudes of the slopes of the output ramp rates to vary from their ideal values.

5.3 Non-Linearities in the Two-Stage Integrator

Slew rate limiting, which was discussed in the previous section, is generally a well-understood phenomena. On the other hand, other forms of non-linear behaviour exist which are more subtle and have generally received little or no coverage in textbooks which deal with circuit design.[30] A rigorous analysis of all forms of non-linear behaviour in the integrator is beyond the scope of this text, but an attempt will now

be made to identify design considerations which are related to such behaviour.

5.3.1 The Nature of Non-Linear Behaviour

The main concern of the circuit designer with regard to non-linear behaviour is that it generates distortion in signals. The discussion which follows will focus on non-linear behaviour which results in amplitude distortion. This type of distortion is also known as harmonic distortion. Figure 5.5 illustrates the nature of non-linear device behaviour which results in amplitude distortion. A device with input signal $x(t)$, which may be a voltage or a current, produces an output $y(t)$ which again may be a voltage or a current. The solid line in Figure 5.5b represents the large-signal transfer characteristic of a linear device, such as an ideal resistor or capacitor. The constant slope of the solid line indicates that $y(t)$ is a scaled replica of $x(t)$ and so does not experience amplitude distortion. The dashed line in Figure 5.5b represents the large-signal transfer characteristic of a non-linear device, such as a bipolar transistor in the common emitter configuration. Since the slope of the dashed line is non-constant, the output signal (which in this case is the collector current) is not a scaled replica of the input signal (the base-emitter voltage) and so amplitude distortion of the signal occurs. In the case of a sinusoidal input voltage, amplitude distortion will manifest itself in the form of harmonics in the output signal. If the magnitudes of the input signal excursions around the quiescent point are kept small however, then the slope of the transfer characteristic is approximately constant and very little distortion occurs. The output signal would then be seen to contain harmonics which are very small relative to the magnitude of the fundamental.[31]

The basic design principle which follows from the above discussion is that in order to reduce signal distortion in the integrator circuit, signal swings at the inputs to non-linear devices such as transistors must be kept small. Where large signal swings must occur (such as at the inputs and outputs of the integrator), linear devices such as resistors and capacitors should be used. Application of this principle to the integrator

Figure 5.5: Illustration of the Nature of Non-Linear Behaviour

Figure 5.6: Simplified Model of the Two-Stage Integrator Showing Key Subcircuits and Considerations for Linear Large-Signal Operation

topology which was chosen will now be considered.

A simplified model of the two-stage integrator is shown in Figure 5.6. The key subcircuits that comprise the integrator are shown (with the exception of the common-mode stabilization circuit) in single ended form. The key considerations for linear, large-signal operation can thus be seen. These are a linear, tunable voltage-to-current conversion in the input stage, linear current steering (level shifting) via the common-gate cascode devices, and linear compensation and amplification in the second stage. Each of these considerations will now be discussed in turn.

5.3.2 Voltage-To-Current Conversion

The large-signal operation of the voltage-to-current conversion subcircuit in the input stage has already been discussed both in this chapter in connection with slew rate limiting, and also in the previous chapter. Since the transconductance integrator is generally operated open-loop, large signal swings at the inputs are inevitable, and so linear large-signal operation of the differential pair is a key design consideration. In this case, large excursions along the diode curves of the differential pair transistors have been avoided through the use of emitter degeneration resistors. With reference to equation (3.4), it can be seen that any large signal swing at the inputs occurs mainly across the emitter degeneration resistance, which is a highly linear device. By equation (3.6), this linear transfer characteristic extends for input signals over the range $-I_{EE}R_{EE}$ to $I_{EE}R_{EE}$, as described in section 5.2. Signals with magnitudes outside of this range will cause severe distortion due to slew rate limiting.

The input stage also contains a Gilbert gain cell for tunable transconductance. This circuit is known to contribute very little to large-signal distortion. [24] The output current from the Gilbert cell is fed to the folded cascode arrangement which performs a level shifting function by steering the signal current to the second stage. Linearity in this subcircuit will now be considered.

5.3.3 Large Signal Current Steering

A simplified model of the current steering arrangement utilizing the folded cascode subcircuit is shown in Figure 5.7. Only one side of the differential arrangement is shown. Non-linear behaviour in this sub circuit will now be considered.

Referring to Figure 5.7, the linear voltage-to-current converter in the input stage, with bias current of I , injects a signal current Δi into the source of the common-gate device M_{FC3} . This device steers the signal current to the input of the second stage. For the common-gate device to accomplish this action, the gate-source voltage of M_{FC3} must change according to the magnitude of the signal current and the transcon-

Figure 5.7: Simplified Model of the Current Steering Arrangement Showing Nature of Non-Linear Behaviour that Occurs There

ductance of M_{FC3} . The well-known voltage-current relationship for the PMOS device was given in Table 2.1, along with the expression for the transconductance. These are repeated here.

$$I_d = \frac{K_p}{2} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) \quad (5.11a)$$

$$g_m = \sqrt{2K_p \frac{W}{L} I_D} \quad (5.11b)$$

According to equation (5.11a), the current injected into the source of the common gate device in Figure 5.7 will result in a change in source voltage proportional to the square root of the magnitude of the signal current. This non-linear behaviour affects other devices which are connected to the source of M_{FC3} either directly or through capacitive coupling. For example, the current $2I$ in the upper current source in Figure 5.7 will be modulated in a non-linear fashion because of the finite output impedance of the current source. This particular example is especially important since the upper current sources generally employ small gate lengths and carry large currents and so, as was seen in Chapter 2, they will have small output impedances.

A potential problem also exists where the source voltage of the common-gate devices may rise high enough to push the upper circuit sources out of saturation.

According to equation (5.11), the magnitude of the resultant Δv 's at the sources of the cascode devices can be reduced by increasing the transconductance of these devices or, equivalently, by decreasing their input impedance. This can be accomplished by increasing the W/L ratio of these devices and/or by increasing the quiescent current through them. The latter solution can also help to avoid a different but related problem associated with large signal operation. In the last section, which dealt with slew rate limiting in the integrator, it was shown that for the bias conditions illustrated in Figure 5.7, overdriving the input stage would result in the current through one or the other of the common-gate devices going to zero. The result would be an effective open circuit and a highly non-linear mode of operation. Thus the bias scheme which was depicted in-full in Figure 5.3 should be altered by increasing the quiescent currents in both the upper current sources and the lower current sinks in the folded cascode arrangement, by equal amounts.

As a final note on non-linear behavior in the current steering circuit, it should be pointed out that non-linearities could be greatly reduced if complementary vertical PNP transistors were available for use as the cascode devices. The high transconductance that is available from these devices would result in a very low impedance at the summing nodes, reducing voltage swings that occur there. At the same time, the parasitic pole that exists because of the cascode devices would be moved to a much higher frequency.

5.3.4 Large Signal Operation in the Second Stages

These are several concerns which must be addressed when considering the large-signal operation of the second stage of the integrator. The output of the integrator (and hence, of the second stage) will necessarily be subject to large signal swings in order to provide a high dynamic range for the integrator. The presence of high gain

in the second stage however may, under appropriate conditions, keep signal swings at the input to the second stage small. Finally, the use of a tunable compensation resistance in the second stage introduces a situation where slew rates internal to the second stage must be considered. These concerns will now be dealt with in turn.

a) Signal Swings at the Output

The output driver arrangement in the chosen integrator topology is a class A, common-emitter configuration. Because of the widespread use of the common-emitter as an output driver, the large-signal performance of this type of configuration has been studied in some detail [32]. A simplified model of the common-emitter stage and the resulting large-signal transfer characteristic are shown in Figure 5.8. The transfer characteristic shows several types of non-linear behaviour. For small signal swings, the transfer curve is an exponential, but is approximately linear and so only mild distortion will occur. If the output swing is too large however, one or both of the output devices M_o and Q_o will be forced out of their high-gain regions and severe distortion will occur. If the load resistance being driven is small, positive swings of the output voltage will be further restricted (as indicated by the dashed line in Figure 5.8) as Q_o will be cut-off before M_o is forced out of the active region. This latter case also corresponds to the situation where a large capacitive load is being driven at high frequencies. In either situation, the departure from the exponential curve is a result of insufficient bias current I_o in the output stage. Thus, distortion due to large swings of the integrator output voltage can be reduced by using large bias currents in the output stage and by having the PMOS device (M_o in Figure 5.8) biased with a small value of $V_{gs} - V_{th}$.

b) Signal Swings at the Input to the Second Stage

An important consideration concerning signal distortion is the magnitude of signal swings which occur at the input to the second stage, since these signals are presented to the base of a common-emitter transistor. Because of the effects of negative feedback around the second stage, the presence of high gain in the second stage of the integrator

Figure 5.8: The Large-Signal Characteristics of the Emitter-Follower Output Driver (a) Simplified Schematic, (b) Transfer Characteristic

will in general result in a situation where the magnitudes of voltage swings at the input to the second stage are kept small. This in turn implies that non-linear devices in the second stage will not experience large signal swings at their inputs, and distortion will be minimized. This beneficial effect has limitations however, as will be shown.

The frequency response of the two-stage integrator can be visualized conceptually as shown in Figure 5.9. This result was derived in the previous chapter. For low-frequency signals, the first stage will provide some voltage amplification v_2/v_1 , resulting in an amplified signal at the input to the second stage. The second stage then provides further amplification of this signal. At some frequency ω_M the voltage gain of the first stage (and likewise of the entire integrator) will begin to roll-off as a result of the Miller-multiplied capacitance that the first stage sees at the input to the second stage. As the magnitude of the first stage gain rolls off, the magnitude of the signal presented to the second stage input is reduced, and the resulting distortion due to exercising diode non-linearities at the second stage input is reduced (however the magnitude at the output of the integrator is also reduced). This behavior continues out to some frequency where the magnitude of the second stage gain v_o/v_i begins to

Figure 5.9: The Frequency Response of the Two-Stage Integrator as a Composite of the Two Individual Frequency Responses

roll-off. At this point the Miller multiplication of the capacitance seen by the first stage begins rolling off, and so the first stage gain levels off, as seen in Figure 5.9.

The important factor to consider here is the gain from the input of the integrator to the input of the second stage *at the intended frequencies of operation*, near the UGBW of the integrator. At these frequencies, it would be desirable to have a large second stage gain and a small first stage gain (the product of the two would of course be approximately unity) so that the signals presented to the input of the second stage would be small, and little distortion would result. Referring to Figure 5.9, this could be achieved in two ways while still maintaining the same overall magnitude response for the integrator. The first involves increasing the frequency at which the gain of the second stage begins to roll off. With reference to the equations presented in the previous two chapters, this could be accomplished (without affecting the overall magnitude response of the integrator) by decreasing the capacitance at the output of the integrator. Since the value of this capacitance is generally determined by the load which must be driven by the integrator however, the designer may not be at liberty to reduce it.

A second means of accomplishing this task is to increase the gain of the second stage by increasing the transconductance of the output driver (increasing the output resistance would be ineffective as the second stage gain would then also begin to roll off sooner). Since this would also lower the input resistance of the second stage (referring to the small-signal models of the previous chapter, $R_i \approx r_{\pi o} = \beta_o/g_{mo}$), the net effect would be to shift the curve $\left|\frac{v_o}{v_2}\right|$ up while lowering the curve $\left|\frac{v_2}{v_i}\right|$ by the same amount. Thus signals near the UGBW of the integrator would receive less gain to the input of the second stage (causing less distortion) with the additional gain being made up by the second stage. Note that this result is not affected by the presence of the emitter-follower in the second stage except that in this case, the gain of the first stage (and of the overall integrator) would be increased at low frequencies.

It is interesting to note that this conclusion regarding minimizing signal distortion at the input to the second stage is consistent with reducing distortion due to cut-off of the output driver (when driving low impedance loads) as well as with widebanding of the integrator.

c) Large-Signal Operation and the Tunable Compensation Resistance

In the previous chapter, it was demonstrated that an appropriately-biased, diode-connected bipolar transistor can be used as a tunable resistance in the compensation network in the second stage of the integrator. However it will now be shown that under large-signal conditions, the tunable resistance can cause distortion of the signal due to non-linear behaviour.

A simplified model of the second stage of the integrator is shown in Figure 5.10. The first stage is represented simply by an ideal current source which injects a signal into the second stage input. Variations in this signal current are reflected directly in variations in the collector current in Q_c . This in turn results in variations in the transconductance of Q_c so that the resistance presented by Q_c to the compensation network varies with signal level. Thus non-linearities and distortion will result for large signal levels. It is interesting to note that this non-linearity results even if

Figure 5.10: Simplified Schematic of the Second Stage of the Integrator Showing Origin of Non-Linear Behaviour in the Tunable Resistance

voltage swings at the input to the second stage are kept small, since the non-linearity results from large *current* variations.

As with the large-signal operation of the folded cascode arrangement in the first stage, the tunable resistance arrangement in the second stage has the potential for exhibiting severe non-linear behaviour. In Figure 5.10, if one sets the value of i_i equal to $-I_c$, then, neglecting base currents, one can see that the entire current from the upper current source will be diverted to the first stage. If this occurs, the transistor Q_c will be cut-off and the second stage will be operating momentarily open-loop. Since the value of I_c is typically much lower than the maximum current that the input stage can draw away from the second stage (i.e: under slew rate limiting conditions) one can say that the maximum *allowable* slew rate of the integrator is determined by the current I_c in the second stage, and the value of the integrating (compensation) capacitor C_c . Thus, one can write with reference to equation (5.2), that the maximum allowable rate of change of the output voltage without slew rate limiting occurring in the second stage is

$$\frac{d(v_o^+ - v_o^-)}{dt} \Big|_{max} = \frac{2I_c}{C_c} \quad (5.12)$$

Likewise, with reference to equation (5.10), one can write that for a given peak magnitude of the output voltage V_p , the full power bandwidth of the integrator is

slew rate limited limited in the second stage to

$$\omega_{max} = \frac{2I_c}{V_p C_c} \quad (5.13)$$

While a potential solution to the slew rate limiting/non-linear behaviour problem in the second stage appears to exist in the form of increasing the value of I_c , practical problems exist with this solution. If a bipolar transistor is used for Q_c , then the value of I_c is fixed by the required value of r_c given by equations (3.3) and (3.1), and by the required tuning of the integrator phase response. As was mentioned earlier, this value of I_c is typically much lower than the maximum amount of current which the first stage can sink from the second stage. Two potential solutions exist for this dilemma, however both of these have further practical problems. The first potential solution involves reducing the bias currents in the input stages of the integrator, so that slew rate limiting would occur in the first stage before it occurs in the second stage. This has the drawback however of reducing the linearity of the input stages as well as increasing noise in the integrator. A second potential solution involves using an MOS transistor for Q_c . If this were done, the value of I_c could be increased beyond the maximum current level that the input stages can sink (equal to one half of the tail current in the inner differential pairs of the Gilbert cells) and the size of the MOS transistor could be adjusted according to equation (5.11b) to give the desired nominal transconductance. However, typical process and device parameters result in required (W/L) ratios for the MOS version of Q_c that are prohibitively large. Simulations have shown that using such large devices results in a situation where parasitic capacitances associated with the large devices cause excessive degradation of the integrator phase response. This solution may however prove workable for low frequency versions of the tunable integrator, since a lower transconductance would then be required for Q_c and hence a smaller MOS device could be used.

Figure 5.11: Illustration of the Generation of a Common-Mode Signal Through the Action of a Non-Linearity on a Purely Differential Signal

5.3.5 Difference-Mode to Common-Mode Conversion

A final aspect of the large-signal behaviour of the integrator which will be considered involves the conversion of non-linear, difference-mode signals into common-mode signals. The mechanism by which this phenomena occurs will be explained, as will the effect on integrator performance.

Figure 5.11 illustrates how, if a purely differential signal is applied to a differential amplifier with a non-linear transfer characteristic, the output of the amplifier can contain both common-mode and difference-mode components if even-order terms are present in the non-linearity. In Figure 5.11a, a non-linear differential amplifier (composed of two identical non-linear single-ended amplifiers) is presented with a purely differential signal, $v_{i1} - v_{i2}$. Figure 5.11b shows the common non-linear transfer characteristic of the two single-ended amplifiers, which are initially biased so that both inputs and both outputs are at zero volts. The purely differential input signal means that both amplifiers exhibit equal but opposite horizontal excursions along their transfer characteristics. However, because of the non-linearity, the resultant vertical excursions along the transfer characteristics are not equal in magnitude and so a common-mode component is generated at the output of the differential amplifier.

The example illustrated in Figure 5.11 is representative of what will occur for instance due to non-linearities in the second stage of the integrator.

The degree to which difference-mode to common-mode conversion occurs depends on the severity of the non-linearity in the transfer characteristic, and the magnitude of the input signals. Thus the techniques for suppressing distortion due to non-linear behaviour which were discussed earlier will apply equally well to the suppression of common-mode components which are generated by non-linearities in the differential circuitry.

Common-mode signals which are introduced to the integrator by any means (i.e. through non-linearities, power supply noise, etc.) will in general be suppressed to some extent by the action of the common-mode stabilization circuit which was described in Chapter 3. The degree to which the common-mode stabilization circuit can suppress common-mode components at the integrator output will depend on both the gain and bandwidth of the common-mode stabilization circuit. As well, the location within the integrator where the common-mode signals originate will be another factor determining the effectiveness of the common-mode stabilization circuit.

Figure 5.12a shows a simplified model of the two stage integrator with the common-mode stabilization circuitry. Three locations where non-linearities in the differential circuitry may cause common-mode components to be generated can be readily identified from the previous discussion. These are in the input stages of the integrator (or alternatively, in the common-gate devices of the folded cascode arrangement), at the inputs to the second stages, and at the outputs of the second stages. Common-mode components which are generated at these three locations will obviously encounter different gains to the common-mode output of the integrator. The last two cases are illustrated in the block diagram of Figure 5.12b where the common-mode components are simply summed into the common-mode signal path either immediately before or after the second stage. The first case described is simply a special case of the second where, depending on the exact location of the non-linearity within the first stage, the

common-mode signal will encounter some additional gain before being summed into the common-mode signal path immediately before the second stage.

If one writes the transfer functions for the common-mode signals depicted in Figure 5.12b, the following simple results are obtained:

$$\frac{V_{o,cm}}{V_{i1,cm}} = \frac{A_2(s)}{1 + A_1(s)A_2(s)} \quad (5.14)$$

$$\frac{V_{o,cm}}{V_{i2,cm}} = \frac{1}{1 + A_1(s)A_2(s)} \quad (5.15)$$

For the case where common-mode components are generated in the first stage, a third gain block $A_3(s)$ can be assumed. The frequency response of this block will be similar in nature to that of the first stage, $A_1(s)$ (being dominated by the Miller capacitance of the second stage), but will typically possess lower dc gain than $A_1(s)$ owing to lower transconductance. Thus one can write that for a common-mode component $V_{i3,cm}$ which is generated in the first stage

$$\frac{V_{o,cm}}{V_{i3,cm}} = \frac{A_2(s)A_3(s)}{1 + A_1(s)A_2(s)} \quad (5.16)$$

The results which are given by equations (5.14) to (5.16) can be interpreted with the aid of Figure 5.12c which shows the typical shapes of the frequency response curves for $A_1(s)$, $A_2(s)$ and $A_3(s)$. This figure is similar to Figure 5.9 since $V_{i,cm}$ and the differential output voltages share essentially the same circuitry. The main difference is that $A_1(s)$ is shifted up to account for the higher first-stage transconductance associated with the common-mode loop.

With reference to equation (5.14) and Figure 5.12c, one can see that at low to medium frequencies where $|A_2(s)|$ is large, common-mode components which are generated at the output of the first stage or the input to the second stage will experience a gain to the output of approximately $1/|A_1(s)|$. At low frequencies, $|A_1(s)| \gg 1$ and so these common-mode components will be attenuated. At intermediate frequencies however (e.g: near the integrator UGBW), $|A_1(s)| \ll 1$, and so these common-mode components will actually be amplified to the output of the integrator. At very high

(a)

(b)

(c)

Figure 5.12: Illustration of the Effect of the Common-Mode Stabilization Circuit on Common-Mode Components Generated by Non-Linearities

frequencies, the gain of the second stage falls off so $|A_2(s)| \ll 1$ and the common-mode signal $V_{i1,cm}$ experiences a gain to the output of approximately $|A_2(s)|$. Hence it is again attenuated.

For common-mode components generated at the output of the integrator (such as might occur if clipping occurs at the output), equation (5.15) and Figure 5.12c predict that up to frequencies near the integrator UGBW, the common-mode components are attenuated by a factor approximately equal to the inverse of the common-mode loop gain. At higher frequencies, this factor becomes asymptotic to 0 dB and the common-mode stabilization loop no longer attenuates these common-mode components.

With reference to equation (5.16) and figure 5.12c, and by comparison to equation (5.14), common-mode components generated in the first stage of the integrator experience the same gain to the output as those generated at the input to the second stage, with an additional gain factor $A_3(s)$. Thus at low to medium frequencies they are attenuated by a factor of approximately $|A_3(s)/A_1(s)|$ and at high frequencies they are attenuated by a factor of approximately $|A_2(s)A_3(s)|$.

The results derived above are summarized in Figure 5.13 which shows the approximate magnitude responses for the various common-mode components. The results indicate that common-mode components generated in the first stage are least damaging since they experience the attenuation due to the Miller capacitance in the second stage. In contrast to this, common-mode components generated at the output of the first stage or the input to the second stage are most damaging since they experience the wideband gain of the second stage but none of the attenuation of the first stage.

While the performance limitations of the common-mode stabilization circuit can be readily identified, as has just been done, the implications of these limitations are not as easily determined. In Chapter 3 it was explained that the common-mode output must be maintained at analog ground to keep active devices in their high-gain regions of operation and to maximize dynamic range and facilitate cascading of integrators. In terms of large-signal distortion however, it was shown in Chapter 3

Figure 5.13: Approximate Magnitude Responses Experienced by Common-Mode Components Generated at Various Points in the Integrator

(see Figure 3.9) that as long as the common-mode output is maintained nominally at analog ground, the difference-mode signal is not affected by common-mode components. Specifically, it can be said that regardless of performance limitations in the common-mode stabilization circuit, the act of taking the output signal differentially will effectively remove even-order harmonics in the differential signal.

Referring to Figure 3.9, which assumes no common-mode stabilization except at dc, if one assumes instead an ideal common-mode stabilization circuit with infinite gain and bandwidth, then it can be readily shown that all common-mode components will be removed from the signals at both of the single ended outputs. The differential signal is not affected. Thus it can be seen that rejection of common-mode components provides suppression of even-order harmonics in the single-ended outputs of the integrator. Since in most applications, signals must eventually be converted to single-ended form, the design of a wideband high-gain common-mode stabilization circuit is important for reducing large-signal distortion.

Chapter 6

Simulation Results and Circuit Implementation

6.1 Introduction

In previous chapters, transconductance filtering has been introduced as a good candidate for achieving quality monolithic filtering at high frequencies. A topology has been selected for a tunable transconductance integrator within a BiCMOS context. Detailed small and large-signal analysis of the integrator has been presented to show expected performance characteristics and limitations and to develop useful design equations.

This chapter will present the results of simulations which were performed for the integrator circuit and compare these to results which are predicted by the simple models developed in earlier chapters. A description of the design process, leading to the layout and fabrication of test circuits, will also be provided. To date, however, no test circuits have been received and no test results could be presented. Testing may however be done at a later date as part of continuing research in the area.

6.1.1 Description of Design Process

Design of the integrator circuit described in this thesis first began as exploratory simulations using the simulator HSPICE at Carleton University with a hypothetical process file provided as part of a graduate course[35]. This process file was intended to be representative of a five volt, one micron BiCMOS technology including NMOS, PMOS and vertical NPN bipolar transistors, as well as resistors, capacitors and a lateral PNP bipolar transistor. The work then continued as part of a research agreement between this author, Carleton University, and Northern Telecom Electronics (NTE).

A new round of simulations at NTE used a proprietary simulator and a process file intended to be representative of an actual sub-micron BiCMOS technology. This technology is similar to the representative technology on which initial simulations were based with regard to the types of devices offered. Initial process files however predicted significant differences in device performance and details concerning the circuit design were adjusted accordingly. These process files were again updated prior to beginning layout of test circuits, and a final round of simulations was performed to determine optimum device sizes.

Layout of test circuits was performed at NTE using the layout editor included in the CADENCE design package and design rules furnished by NTE. The test circuits were included on a test chip fabricated at NTE. Test circuits included a single open-loop integrator, an integrator connected in unity-gain feedback, and a low-pass biquadratic filter similar to the one shown in Figure 3.10. To date, no test circuits have been made available to the author, so details concerning actual circuit performance could not be provided in this thesis. An updated process file has been provided by NTE, which is expected to be more representative of the actual technology. New simulations of the integrator circuit were performed with this update, using the simulator HSPICE. The results of these simulations are presented in the next two sections of this chapter.

6.2 AC Small-Signal Simulation Results

This section will present the results of simulations of the integrator circuit which pertain to the ac small-signal performance of the integrator. These simulations were performed using the level three model type of the circuit simulator HSPICE and a representative process file. Thus a fairly accurate prediction of the integrator performance is expected. One should bear in mind however the well-known limitations of circuit simulator accuracy which are particularly prevalent when one is attempting to model the high-frequency behaviour of devices which employ small geometries.

In addition to the simulation results which will be presented here, results based on the simple models which were developed in earlier chapters will also be presented, where appropriate. As was the case in Chapter 4, the results which are based on simple theory will make use of operating point device parameters which are provided by the simulator.

6.2.1 Difference-Mode Phase and Magnitude Response

The difference-mode phase and magnitude response of the integrator is shown in Figure 6.1. This response corresponds to the simulation conditions shown in Figure 6.2, where it is seen that one set of inputs to the integrator is excited in a fully-differential manner, while the other set of inputs is grounded. Both outputs are loaded with $C_L = 0.5pF$ capacitances, which are intended to represent the input capacitances of a similar integrator which this one might be driving. The common-mode sensing circuit is also shown as this represents a resistive load of $R_L = R = 10K\Omega$. No additional resistive loading is included since the input resistance of a similar integrator would be much greater than $10K\Omega$. The bias conditions internal to the integrator are those shown in Figure 3.17, and correspond to the situation where the integrator phase response has been tuned via I_{RC} to achieve a maximally flat -90 degree phase response over the widest possible frequency range. This tuning was performed with

Figure 6.1: Difference-Mode Phase and Magnitude Response of the Tuned Integrator
the aid of the circuit simulator.

The ac small-signal performance of the integrator as predicted by the simulator is summarized in Table 6.1. The integrator response shows a relatively high dc gain of 70.4 dB and a flat (± 0.5 deg) -90 degree phase response which extends over the range $2\text{ MHz} \leq f \leq 130\text{ MHz}$ with a nominal UGBW of 55 MHz. Values calculated using simple models developed in Chapter 4 and device parameters obtained from simulation results are also shown in Table 6.1. Comparison of the two sets of results reveals that the simple models developed in Chapter 4 tend to overestimate the integrator dc gain and UGBW. As well, the simple models cannot be used reliably to predict the high-frequency phase response of the integrator. This latter deficiency

Figure 6.2: Simulation Conditions for Small-Signal Analysis

results because the simple models predict the locations of only two high-frequency poles and one high-frequency zero in the integrator transfer function, while the simulated response shows that four high frequency poles and one zero are all present near 1 GHz. While this response was in fact predicted in Chapter 4 as a result of the use of an emitter-follower in the second stage of the integrator, a model to predict the actual pole zero behaviour was not developed there because the model would be quite cumbersome to use and of little practical value. This illustrates a fundamental problem with designing high-frequency analog circuits based on low-frequency design techniques. As one attempts to extend the useful operating range of complex analog circuitry such as the integrator described here, the many high-frequency poles and zeros which are inevitably present become more important to the designer, and simple analytical models are no longer sufficient for predicting circuit behaviour. Prediction of the high-frequency behaviour of such circuits requires strong support from circuit simulators.

With regard to inaccuracies in the prediction of integrator UGBW and dc gain, inspection of the simple models developed in Chapter 4 reveals that both inaccuracies

Characteristic	Result From Simulation	Calculated Value
UGBW	55 MHz	68 MHz
Frequency Range over which $-90.5^\circ \leq \phi \leq -89.5^\circ$	2.0 MHz - 130 MHz	—
DC Gain	70.4 dB	73.3 dB

Table 6.1: Summary of the AC Performance Characteristics of the Tuned Integrator as Predicted by Simulation and by Simple Models

likely result from an overestimate of the effective transconductance of the first stage of the integrator. This in turn likely results from failure to account for leakage of the transconductance current to ac ground through the finite output impedances of devices in the first stage.

Despite the deficiencies just described however, the simple models developed in Chapter 4 do provide useful information concerning how the integrator performance is affected by circuit parameters, if not actually providing accurate estimates. Based on the models, a first-pass design of the integrator can be made. Simulation can then be used to fine-tune the integrator design based on insight which is gained from the simple models.

The simulated response shown in Figure 6.1 predicts that the integrator circuit provides a near-ideal response for frequencies between 2 MHz and 130 MHz, with a UGBW of 55 MHz. In accordance with the theory developed in earlier chapters, this indicates that the integrator could be used to achieve filtering in the 50 MHz region. This represents a significant improvement over capabilities which have recently been reported where strictly bipolar designs were used to achieve filtering capabilities in the 10 MHz region [4].

The simulated response shown in Figure 6.1 also predicts an unwanted peaking in the magnitude response at a frequency of about 1 GHz. While this would be unlikely to cause problems in a lowpass or bandpass filter application (where the peaking would then be beyond the useful frequency range of the filter), it could make the integrator unsuitable for realizing highpass filter functions. As well, the peaking could cause potential instability if it were to become large enough to allow the magnitude response to cross 0 dB near where the phase response has reached -180 degrees. It has been found through simulation that this potential problem can be avoided by decreasing the bias currents in the output drivers of the integrator, resulting in a decrease in the amplitude of the peaking. This finding is consistent with the discussion of high-frequency pole behaviour which was presented in Chapter 4. The fact that the behaviour of these high-frequency poles becomes a concern to the designer is symptomatic of the situation where one is attempting to wideband a circuit with many parasitics. As the UGBW of such a circuit is increased, the proximity of the UGBW to parasitic poles and zeros becomes narrower and the parasitics become more important. In the particular case of the integrator response shown in Figure 6.1, increasing the integrator UGBW causes the high-frequency portion of the magnitude response to be shifted up. Thus the magnitude of the peak approaches unity gain and becomes more important for stability reasons.

The individual magnitude responses of the two stages of the integrator, as obtained from simulation, are shown in Figure 6.3. To obtain these results, the gain to the input of the second stage, $|v_2/v_i|$, is calculated directly by the simulator. The gain from the input of the second stage to the output of the integrator, $|v_o/v_2|$, is obtained simply by subtracting $|v_2/v_i|$ from the overall gain. The overall gain of the integrator is also shown in Figure 6.3 for comparison purposes.

In Figure 6.3, it can be seen that the second stage is sufficiently wideband, and the first stage sufficiently narrowband, that over most of the useful high-frequency range of the integrator, inputs to the integrator are attenuated to the input of the second

Figure 6.3: Simulated Difference-Mode Magnitude Responses of the Two Stages of the Integrator, and of the Overall Integrator

stage. This is a desirable situation for reducing signal distortion, as was explained in Chapter 5. The results shown in Figure 6.3 also serve to verify the predictions regarding the common-mode behaviour of the integrator which were discussed in Chapter 5.

6.2.2 Tuning of the Integrator UGBW

The ability to tune the UGBW (and hence the time constant) of the integrator is demonstrated by the simulation results shown in Figure 6.4. This figure shows the difference-mode phase and magnitude response of the integrator for different

Figure 6.4: Simulations Showing Tuning of the Integrator UGBW by Adjusting the Current Ratio in the Gilbert Cell

bias currents in the Gilbert cell of the input stage (tuned via I_{TA} or I_{TB} in Figures 3.17). As can be seen in Figure 6.4, the UGBW of the integrator can be varied over nearly the entire bandwidth defined by the -90 degree phase response. This allows the designer to achieve a precise integrator time constant regardless of variations in loading conditions or process parameters and to achieve a variety of integrator time constants with a single integrator design. This tuning capability can also be used to produce filters with tunable Q's so that filtering characteristics can be adjusted dynamically. The phase responses shown in Figure 6.4 indicate that the integrator phase response must be adjusted each time the integrator UGBW is tuned.

6.2.3 Tuning of the Integrator Phase Response

The ability to achieve a flat -90 degree phase response at high frequencies for the integrator is provided by the tunable phase compensation described in earlier chapters. The position of the high-frequency left-hand plane zero in the integrator transfer function is tuned by adjusting I_{RC} in Figure 3.17. The result of tuning the position of this zero is shown in Figure 6.5. In this figure, it can be seen that by varying the bias current in the diode-connected compensation transistors (Q16 and Q17 in Figure 3.17), the amount of phase lead contributed by the left-hand plane zero near the integrator UGBW can be varied. This allows a flat -90 degree phase response to be achieved at high-frequencies even if the positions of the high frequency poles are unknown or vary as they may in fact do as a result of variations in loading or processing conditions. The positioning of the left-hand plane zero near the high frequency parasitic poles of the integrator also allows the useful frequency range of the integrator to be extended beyond where it could otherwise be if the zero were not present. Finally, it is apparent from Figure 6.5 that fine tuning of the phase response does not affect the integrator time constant. Thus, the two critical aspects of the integrator behaviour, the time constant and the phase response near the UGBW, can be tuned somewhat independently.

6.2.4 Common-Mode Phase and Magnitude Response.

The simulated ac response of the common-mode stabilization circuit for the integrator is shown in Figure 6.6. The performance characteristics of the circuit are summarized in Table 6.2. The transconductance of the differential pair at the front end of the common-mode stabilization circuit was chosen (with the aid of the simulator) such that the dc gain and UGBW of the common-mode circuit would be maximized while still maintaining a safe phase margin. From Table 6.2, this corresponds to an open-loop dc gain of 87.4 dB and a UGBW of 92 MHz giving a phase margin of 71 degrees. While the phase margin is relatively large, it can be seen in

Figure 6.5: Simulations Showing Tuning of the Integrator Phase Response by adjusting the Currents in the Compensation Transistors

Figure 6.5 that the phase rolls off very quickly after the UGBW. Thus, while the bandwidth of the common-mode circuit could be increased to as high as perhaps 800 MHz, this action would put the UGBW dangerously close to the point where the phase lag reaches 180 degree.

Comparing Figure 6.6 to Figure 6.1 one can see that, contrary to what was initially expected, the phase and magnitude response of the common-mode circuit is not simply a vertically-shifted replica of the response of the difference-mode circuit. As was explained in Section 3.5.3, it was initially believed that since the common-mode and difference-mode signals share the same circuitry (with the exception of input stages),

Figure 6.6: Simulation Results Showing Open-Loop Magnitude and Phase Response of the Common-Mode Stabilization Circuit

the small-signal responses of the two signal paths would be vertically scaled replicas of one another. In fact, simulation results revealed that an additional pole was present near the UGBW of the common-mode ac response. Furthermore, simulations revealed that the additional pole appeared to be associated with the common-gate devices in the folded cascode arrangement. The additional pole was effectively removed from the common-mode transfer function by inclusion of the capacitance C_{CM} in Figure 3.17. The common-mode ac response without the capacitor C_{CM} in place is shown in Figure 6.7, where the additional pole can be clearly seen.

The reason why an additional pole is present in the common-mode transfer func-

Characteristic	Result From Simulation
DC Gain	87.4 dB
UGBW	92 MHz
Phase Margin	71°

Table 6.2: Summary of the AC Performance Characteristics of the Common-Mode Stabilization Circuit

tion can be hypothesized from the simplified high-frequency model of the folded cascode arrangement shown in Figure 6.8. In this figure, it can be seen that the gate-source capacitances of the common-gate devices allow high-frequency signals present at the sources of these devices to be coupled directly to their gates. While a common-mode signal which is present at the sources of the common-gate devices will couple directly through the gate-source capacitances to the gates of the common-gate devices, the same is not true for difference-mode signals. This is because under difference mode operation, the source of one cascode device is being pulled up while the source of the other cascode device is being pulled down. Thus no net differential signal is being coupled through to the gates of the cascode devices through their gate-source capacitances. Decoupling the gates of the cascode devices to ac ground via the capacitor C_{CM} appears to eliminate the effect of the common-mode coupling. This explanation has not been verified through small-signal analysis but appears to be supported by the results of circuit simulations.

Figure 6.7: Common-Mode Phase and Magnitude Response of the Common-Mode Stabilization Circuit Without the Inclusion of C_{cm}

6.3 Large Signal Simulation Results

While the ac simulations just presented reveal that the integrator circuit does provide a tunable high-frequency integrator response, the practical usefulness of the circuit inevitably is limited by the ability to process large signals. Analysis presented in Chapter 5 predicts that in particular, the tunable compensation scheme used in the integrator circuit will limit the magnitude of signals that the integrator can deal with. In this section, limitations on the large-signal performance of the integrator will be explored through the results of transient time domain simulations of the integrator circuit.

differentially to the integrator at the unity-gain frequency is given by

$$\frac{V_i}{2} |_{max} = \frac{I_c}{2\pi f_{UGBW} C_c} \quad (6.1)$$

For the integrator with the ac response shown in Figure 6.1, $f_{UGBW} = 55$ MHz, $C_c = 2$ pF, and $I_c = 50$ μ A. The maximum amplitude of signal that can be applied then is given by equation (6.1) as

$$\frac{V_i}{2} |_{max} = 72 \text{ mV}$$

Since the transition to cut-off in a bipolar transistor is in fact a gradual one, it would be expected that distortion due to this type of slew rate limiting would begin occurring for values of $V_i/2$ around 70 mV. This in fact can be seen to be the case in Figures 6.9 and 6.10 which show simulated transient responses of the integrator for values of $V_i/2$ equal to 65 mV and 70 mV respectively, applied to the integrator in the manner indicated in Figure 6.11.

Figure 6.9 shows the sinusoidal signal of peak value $V_i/2 = 65$ mV applied to the positive input of the integrator (the negative input signal is not shown), and the two output waveforms v_o^+ and v_o^- . As can be seen, the outputs are only mildly distorted. The collector current in the diode-connected transistor associated with v_o^- is also shown. As can be seen, the current through this transistor drops to a very low value during positive going swings of v_o^- . In Figure 6.10, the same variables are shown for $V_i/2 = 70$ mV. In this figure, it can be seen that the output waveforms clip during their positive going swings as the collector currents in the diode-connected compensation transistors approach zero. Simulations for larger input signals have revealed that as $V_i/2$ is increased, the minor clipping seen in Figure 6.10 is replaced by sharp spikes on the output signals which grow in time. This indicates that the open circuit in the feedback path which results when equation (6.1) is exceeded causes the integrator to become unstable.

With the exception of the distortion due to slew rate limiting in the tunable compensation circuit, Figures 6.9 and 6.10 show that the integrator is providing

Figure 6.9: Simulated Transient Response of the Integrator for a Sinusoidal Input of Peak Magnitude $V_i/2 = 65mV$

relatively accurate large-signal operation. The input and output signals are 90 degrees out of phase, and of equal amplitude. An additional transient is present however, since the outputs start at $v_o^+ = v_o^- = 0V$ when in fact the -90 degree phase shift should have them starting at $v_o^+ = -v_o^- = -V_i/2$ for the sinusoidal input signal. The resultant differential output signal initially contains a dc component of value V_i . The outputs do converge to their proper values however, with a time constant which is given by the dominant pole frequency of the integrator.

Figure 6.10: Simulated Transient Response of the Integrator for a Sinusoidal Input of Peak Magnitude $V_i/2 = 70\text{mV}$

6.3.2 Distortion In the Fully-Differential Integrator

In previous chapters, it was explained that the use of fully differential signal paths in the integrator causes signal distortion to be reduced. The effect of this can actually be seen in Figure 6.12 which shows the two single-ended output waveforms v_o^+ and v_o^- as well as the differential output voltage ($v_o^+ - v_o^-$) for a 55 MHz differential input signal of 140 mV peak amplitude. Both v_o^+ and v_o^- show relatively severe distortion due in part to the onset of slew rate limiting in the phase compensation circuit. The differential voltage ($v_o^+ - v_o^-$) however shows significantly less distortion, for reasons which were explained in previous chapters. Also shown in Figure 6.12 is the common-

Figure 6.11: Simulation Conditions for Transient Analysis

mode output voltage, which can be seen to be affected by the presence of the nonlinearities in conjunction with the finite gain and bandwidth of the common-mode stabilization circuit.

The degree to which taking the output signal differentially reduces distortion can be seen quantitatively by performing Fourier decomposition of the single-ended and differential output signals. This was done using the circuit simulator HSPICE for a 50 MHz differential input signal with a peak amplitude of 80 mV. The results of the simulations are summarized in Table 6.3 which shows the relative amplitudes of the first five harmonics as well as the total harmonic distortion (THD) present in the single ended and differential output signals. The differential signal is seen to have a THD which is almost an order of magnitude less than the THD in the single-ended outputs. This is seen to be almost entirely due to a drastic reduction in the amplitude of the second harmonic (100 MHz) which results from the output being taken differentially. This is consistent with the discussion which was presented in earlier chapters, and thus the fully-differential integrator is seen to be a low-distortion circuit as compared to a single-ended realization.

Harmonic	Frequency (MHz)	Relative Amplitude	
		v_o^+, v_o^-	$v_o^+ - v_o^-$
1	50	1.000 e -00	1.000 e -00
2	100	6.200 e -02	3.262 e -04
3	150	7.024 e -03	7.026 e -03
4	200	1.745 e -03	1.673 e -04
5	250	4.363 e -04	4.342 e -04
Total Harmonic Distortion (%)		6.242	0.7051

Table 6.3: Results of Fourier Decomposition Obtained From Simulation Comparing Distortion in Differential and Single-Ended Output Signals

Figure 6.12: Simulations Showing Single-Ended, Differential, and Common-Mode Output Signals For Operation Near the Full-Power Bandwidth of the Integrator

Chapter 7

Conclusions and Recommendations

This thesis has been concerned with the design of a wideband monolithic transconductance integrator in the context of a fine-line BiCMOS technology. In the process of designing and analyzing such a circuit, several areas of importance have been explored including BiCMOS analog design techniques, the design of monolithic high-frequency analog circuits in general, and the design of circuits which provide low distortion under large-signal operating conditions. Important conclusions have been drawn in each of these areas. As well, a specific circuit design has been presented which promises to provide a precision monolithic filtering capability in the 50 MHz region. This represents a significant advance over what is currently considered to be state of the art. Test circuits have been laid out and fabricated in an industrial BiCMOS process, but testing was not possible as part of this thesis. It may however be carried out at a later date as part of continuing research in the area of high-frequency monolithic continuous-time filtering.

The integrator design which has been presented makes use of tunable phase lead compensation which simultaneously extends the useful frequency range of the integrator and provides insensitivity of the circuit to loading and process variations. The

tunable compensation circuit which was used however was seen to restrict the amplitude of signals which the integrator can pass without severe distortion or even instability occurring. While a potential solution to this problem has been presented, this solution was deemed to be unsuitable for high-frequency applications. Further work in this area should address the problem of improving the large-signal high-frequency capabilities of such a circuit, as it is felt that tunable phase compensation is a promising technique for increasing the bandwidth of continuous-time filters.

The integrator which was designed also makes use of a fully-differential topology. It has been shown that the use of such a topology can greatly reduce harmonic distortion which occurs as a result of non-linear large signal behaviour. It was shown however that in order to fully realize the benefits of such a circuit, a common-mode stabilization circuit must be designed which possesses sufficient bandwidth. In the case of transconductance integrator design, this bandwidth must be much greater than the bandwidth of the integrator itself and hence the design of the common-mode stabilization circuit can become more difficult as the bandwidth of the integrator is increased. This problem was alleviated to some extent by incorporating the difference-mode circuitry as an integral part of the common-mode stabilization circuit. In this way, the techniques which were employed to increase the integrator bandwidth simultaneously extended the bandwidth of the common-mode stabilization circuit.

The general design philosophy which was used—that of applying low-frequency circuit design techniques to realize a high-frequency circuit—was seen to result in several fundamental problems. One of these problems concerns the ability to model the behaviour of such circuits, and a second related problem concerns the bandwidths which can be achieved using such an approach. Specifically, it was seen that when one attempts to wideband a complex low-frequency circuit such as the pole-splitting op-amp/integrator which was used in this thesis, the many parasitic poles and zeros which are inevitably present in such a circuit become extremely important and can not be simply ignored as they often are in low-frequency design. As a result, the

designer is no longer faced with only a few parasitic poles in the vicinity of the intended bandwidth, but instead faces a large number of parasitics with complex interactions, and is forced to rely more heavily on simulation tools for design. Thus the design process becomes more difficult and time consuming, with simple analytical models becoming less useful. This point was clearly demonstrated with the design of the tunable transconductance integrator which proceeded using simple analytical models which have been shown in the past to be very accurate at low frequencies. These models failed however to predict such phenomena as peaking in the frequency response near the UGBW of the integrator.

The presence of many high-frequency parasitic poles and zeros was also seen to produce an effective limit on the possible bandwidth which can be achieved using low-frequency circuit techniques. This is because the frequencies to which these parasitics can be pushed is ultimately limited by the characteristics of the fabrication process being used, and specifically, by the f_T 's of the active devices in that process. If for example one designs in a process where the f_T 's of the devices are near 1 GHz, then the useful bandwidth of a circuit which contains many parasitics, and is designed by usual low-frequency circuit techniques, will be limited to about 100 MHz. Beyond this point, the phase response of the circuit will begin to fall off very rapidly. This problem can be alleviated to a certain degree by the availability of bipolar transistors possessing high f_T 's, and by the use of phase compensation techniques.

Finally, it has been shown that attempts to build wideband complex circuits developed on the op-amp techniques used here also requires careful attention to the large-signal operation of the circuit. Specifically, slew rate limiting may begin to occur at high frequencies, where devices simply do not possess sufficient current to charge and discharge internal capacitances at the speeds that are required. While this problem can in most cases be remedied simply by increasing bias currents in the circuit and by keeping capacitances small, the design process nonetheless becomes more difficult as the sources of these limitations must be identified in advance by the

designer.

The above conclusions tend to support a move to the use of high-frequency design techniques such as those employed by designers working in GaAs processes. With these techniques, the number of active devices used is kept to a minimum, with the recognition that additional active devices will result in additional parasitics. Such a move however would tend to result in a situation where functionality and signal quality are sacrificed, and so would not support the overall objective of achieving a quality, high-frequency filtering capability. The conclusion which is supported then is that, as required operating frequencies are extended, the design of high-frequency analog circuitry will inevitably become much more complicated and reliant on computer simulation. At the same time, designers must be more prudent with the use of active devices in order to reduce the number of parasitics which are present, and hence to extend the useful frequency range of the circuit being designed, and reduce the complexity of the modeling problem which is associated with the design.

With regard to BiCMOS design in particular, several conclusions can be drawn based on the experience which was obtained during this design exercise. Most importantly perhaps, it was found that because of the higher g_m/I and $g_m/C_{parasitic}$ ratios which are possessed by bipolar transistors, these devices should be used almost exclusively over MOS transistors when wideband circuitry is being designed. As signal-carrying devices, MOS transistors should be used only when their unique properties of infinite input resistance and easily-adjustable (ie: through device geometry) performance characteristics are required.

The ability of the BiCMOS designer to avoid the use of MOS transistors is, in most processes, restricted by the lack of a true complementary (vertical) PNP transistor, and the need which then results to perform level-shifting in complex multi-stage circuitry. This will often necessitate the use of a PMOS transistor as a signal-carrying device. If this is the case, wideband configurations such as the common-gate or source-follower configurations should be used to minimize the detrimental effects that the

PMOS transistor will have on the frequency performance of the circuit. The use of minimum gate lengths and large gate-source bias voltages will also help in this regard. However, the need for level-shifting and the detrimental effects that it produces would be greatly reduced if a true complementary PNP transistor were available.

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