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Tunable, High-Q, LC Integrated Filters

by

George Khoury

B. Eng. (Aerospace Engineering)

A thesis submitted to
the Faculty of Graduate Studies and Research
in partial fulfillment of
the requirements for the degree of

Master of Engineering

in

Electrical Engineering

Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada
August, 1995

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Tunable, High-Q, LC Integrated Filters

submitted by

George Khoury, B. Eng.

in partial fulfillment of the requirements for
the degree of Master of Engineering

A handwritten signature in black ink, reading "Calvin Plett", written over a horizontal dashed line.

Thesis Supervisor

A handwritten signature in black ink, reading "B. Singh", written over a horizontal dashed line.

Chairman, Department of Electronics

Carleton University

September, 1995

to my family

Abstract

The design of two monolithic LC frequency tunable filters implemented in a silicon BiC-MOS technology suitable for applications in mobile radio is presented in this thesis. The work is part of a study aimed towards the implementation of a "single-chip" radio. The objective of this work is to design an integrated bandpass filter capable of operating in the 1-2 GHz range with a low noise figure and low power dissipation. The filters are based on positive feedback which is commonly used in negative resistance oscillators. The positive feedback is used to tune the Quality factor Q , of the filter. A portion of this work is directed towards modeling the two architectures, and thus predicting the frequency response of the filter.

The first circuit is based on a variable gain structure which couples the response of two LC tuned circuits, centered at different center frequencies, in varying proportions. This allows the center frequency of the overall circuit to be tuned anywhere between that of the lower frequency LC tank to the higher frequency LC tank.

The second circuit implements an integrated varactor as well as an integrated inductor. Frequency tuning is achieved by varying the capacitance of the varactor. The circuit Q is tuned by means of a positive feedback network.

An experimental monolithic version of the second circuit realizes a tuning range of 200MHz with a center frequency of 1.5 GHz. Experimental measurements are in excellent agreement with simulation results, and illustrate the importance of properly modeling the parasitics around the circuit.

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List of Symbols

Amplifier

Bipolar Junction Transistor (BJT), npn

Capacitor

Current Source

DC Power Terminal

Filter

Ground Terminal

Inductor

Mixer

Operational Amplifier

Resistor

SMA Connector

Varactor

Voltage Source

Abbreviations

ac	alternating current
β	dc current gain
BATMOS	Bipolar Analog Telecom MOS
BiCMOS	Bipolar and CMOS on the same process
BJT	Bipolar Junction Transistor
BPF	Bandpass filter
CAD	Computer Aided Design
CMC	Canadian Microelectronics Corporation
CMOS	Complementary Metal Oxide Semiconductor
dB	decibel
DECT	Digital European Cordless Telecommunications
ESD	Electro-Static Discharge
Δf	Bandwidth (Hz)
FM	Frequency Modulation
GaAs	Gallium Arsenide
GHz	Giga-Hertz
IC	Integrated Circuit
IF	Intermediate Frequency
LNA	Low-Noise Amplifier
LO	Local Oscillator
MHz	Mega-Hertz
NF	Noise Figure
Q	Quality Factor, Ratio of Center Frequency to 3dB Bandwidth
PCS	Personal Communication Systems
PGA	Pin Grid Array
RF	Radio Frequency
SAW	Surface Acoustic Wave
SiO ₂	Silicon dioxide
STF	Stagger-Tuned Filter
VCCS	Voltage-Controlled Current Source
VCO	Voltage-Controlled Oscillator

VLSI
VTF

Very Large Scale Integration
Varactor-Tuned Filter

Chapter 1

Introduction

A portable radio transceiver operating in the GHz range requires the integration of many high level system components. Due to technological limitations many of these components are hard to fabricate in a VLSI environment. Recent introduction of a monolithic inductor [NM90] in a silicon based process has allowed realization of many key elements of the portable radio transceiver. This thesis explores the integration of a high-quality active bandpass filter operating in the GHz range. The band pass filter (BPF) is designed using on-chip inductors and the bipolar transistors of Northern Telecom's BiCMOS process.

Planar on-chip inductors have been used for many years in printed circuit boards and more recently in Gallium Arsenide integrated circuits. In the early development of Silicon integrated circuits, poor processing techniques led to excessive chip area and a low frequency of operation. Recent improvements in processing have led to the realization of metal width and pitch in the low micron range. This allows many more turns per unit area, giving rise to an improved quality factor, Q . The inductors currently used have values ranging from approximately 3 to 8 nanohenries [NM90].

Due to the poor quality of the inductors, positive feedback is used to boost the quality of the overall bandpass filter response. The bandpass filter is based on a modified voltage-controlled oscillator [NM92]. The design is implemented using two technologies. The first version is designed on a printed circuit board working at 100 MHz. This provided quick verification of the design philosophy and architecture. The design is then implemented in a BiCMOS process using npn transistors and integrated inductors.

1.1 Thesis Goals

This research sets out to design an integrated high-Q tunable filter working at 2 GHz. Currently this type of integrated filter does not exist, and filtering at RF is performed by going off-chip into a discrete filter. This presents several problems, since the discrete filter is not tunable, only wideband filtering action is performed and channel selection has to occur at the intermediate frequency IF. Going off-chip also produces the problem of undesirable signal coupling through parasitic elements such as the package leads and bondwires.

With this research, it is hoped that channel selection can occur at RF, which would open up possibilities for new radio architectures.

1.2 Thesis Outline

This thesis is organized over 5 chapters. Chapter 2 presents background knowledge of radio architectures and illustrates possible uses for a highly selective bandpass filter. Electrical noise is discussed, with suggestions on how to improve the noise performance of a circuit which uses Bipolar Transistors (BJT). This chapter also presents the basics for integrated inductors and varactors. Chapter 3 introduces the voltage-controlled oscillator [NM92] and the modifications that are implemented. The theoretical models that describe the operation of the filter are introduced and mathematical models are developed. A varactor-tuned circuit is also developed in Chapter 3 with theoretical modeling and simulation results. Chapter 4 presents the experimental results for the work performed on high-frequency filtering. This included a discrete version which was designed and built to prove the concept, a filter using staggered tank circuits and a varactor-tuned circuit. Conclusions for the work performed, as well as recommendations for further designs using monolithic inductors and positive feedback are provided in Chapter 5.

Chapter 2

Radio Receiver Architectures and Filter

This chapter reviews the general background of a classical FM radio receiver and then presents an alternate topology, which can be used to overcome some of the problems associated with a more highly integrated, low-cost, low-power solution. The development of integrated inductors on a silicon substrate is introduced, and recent papers dealing with monolithic RF components using integrated inductors are reviewed.

Analog RF components have many generic characteristics that affect the behavior of the overall receiver. Three main characteristics, Noise Figure (NF), Gain, and Linearity of a device have a major impact on the quality of the processed analog signal. These characteristics lead to conflicting design requirements and the design of an optimum RF component is usually a compromise between the optimum individual characteristics achievable. In addition, the topology of a radio receiver has a major impact on the design requirements of the RF components. Alterations to the classical topologies can significantly reduce design constraints on individual RF blocks, which in turn can improve the overall performance of the radio.

2.1 An FM Radio Receiver Overview

A generalized block diagram of a single conversion FM receiver is shown in Figure 2.1 [Ke92]. These types of receiver designs are robust, providing good signal to noise ratio and channel isolation for an RF input which varies widely in signal strength, and may contain adjacent channel interference.

Figure 2.1 - Block diagram of a typical FM receiver

The RF signal enters the system at the antenna and is passed to the low noise amplifier, LNA, for processing. The LNA is designed for large gain, large linearity, and low noise. This combination of characteristics allows the LNA to boost the power of the signal, while injecting a minimum amount of noise and producing a minimum amount of distortion. The wideband matching network preceding the LNA is used to match the LNA to the signal source for optimum noise figure performance. Consequently the LNA must have a large enough dynamic range to process the desired signal and any other signals present in the bandwidth of the match. This requirement for large linearity is in contradiction to the requirement of low noise figure, and the final design is a compromise between these specifications. As a result the final design of the LNA is usually one which consumes a lot of power. The output of the LNA is matched to the input of the mixer for optimum power gain. The match can also include an image reject filter to suppress the noise and interfering signals at the image frequency.

The mixer is a frequency translation device which takes the signal power at RF and translates it down to an intermediate frequency (IF). The mixer can be either an active or passive device. The passive device is usually composed of a passive diode mixer. This type of mixer offers a low noise figure and high linearity, but has a few drawbacks. It requires a large amount of LO power, has no conversion gain, and can only be implemented in a discrete form, thus increasing the cost of the receiver. Most silicon implementations of the mixer use a bipolar Gilbert cell. This type of mixer can be integrated, thus reducing the overall cost of the radio and providing the opportunity for conversion gain. An advantage is that an integrated version only requires low power LO drive. The drawbacks with this mixer are higher noise figure and lower linearity than for the passive diode mixer.

The mixer has the same system requirements as the LNA, they both must be able to process the desired RF signal and all other signals within the bandwidth of the radio. This usually results in a mixer design which has high power dissipation and high noise figure.

A high-Q filter is used at IF to suppress out of band interference. Filters of this nature come in a variety of forms, such as Surface Acoustic Wave (SAW), crystal, ceramic, or active tuned filters. The output of the IF filter is further processed by an FM demodulation block where information is extracted from the IF signal.

2.2 An Alternate Receiver Architecture

An alternative FM receiver can be derived from the classical architecture of Figure 2.1. This newer architecture uses a tuned LNA to replace the LNA and image filter of the classical FM receiver. The differences are shown in Figure 2.2.

Figure 2.2 - Block diagram of alternate FM receiver blocks

This architecture is identical to the proceeding one except for the tuned LNA. The tuned LNA is narrow band, and tunable in frequency over a very broad range. This allows the tuned LNA to suppress all out of band interferers and only process the desired channel. This reduces the linearity requirement of the LNA and mixer designs, which results in components that consume less power and conceivably have a lower noise figure.

A discrete LNA would be severely hampered by parasitic elements, therefore this architecture is limited to an integrated implementation. A tunable integrated LNA was previously not possible due to a lack of integrated tuning elements such as inductors. Other techniques of high frequency filtering, for example the use of transconductance filtering, are limited to a few hundred MHz. Recent advances in integrated inductors on silicon substrate [NM90][Lo92] have opened up new possibilities. The integrated inductors have been shown to have values of 3 to 8 nH [NM90], with a Q value of 3 to 8 at a frequency of 1 GHz [Lo93]. The inductors are limited to a frequency range of 1 - 8 GHz [NM90][Lo93]. At frequencies below 1 GHz the resistive losses of the inductor are too great and inductor Q value drops to below 1. At frequencies above 8 GHz the inductor approaches its self resonant frequency.

A couple of approaches have been attempted at increasing the Q of the inductor. One approach is to use special fabrication steps to provide gold metallization over a highly

resistive substrate [AFBM94], but this increases the cost of production and may not be suitable for low-cost, high volume chips. Another approach is to use an active circuit to compensate for inductor resistive losses. Two topologies exist for the active circuit compensation technique. A series-mode topology places an active negative resistor in series with the inductor [DMS93][NM92][Ma94]. The parallel approach has an active negative conductance connected in parallel with the inductor [PT94].

The two topologies for active circuit compensation, as applied to high frequency filtering[DMS93][PT94], have yielded similar results. Along with having an active circuit to perform Q compensation for the integrated inductor, both circuits provide a means to tune the center frequency. This is essential for manufacturing yield because of shifts in center frequency due to process and/or temperature variations. In both design cases, as the circuit Q is tuned, the center frequency has to be retuned. The shift in center frequency is due to changes in parasitics related to changes in the bias condition: These are very small, changing by as little as 2% for a 100% change in circuit Q . Due to the nature of the design, the opposite is not true; as center frequency is tuned, the Q can change over a very wide range of values.

A planar inductor based high-frequency filter is limited to frequencies above 1 GHz. Several emerging standards, DECT and User PCS [MF93] are ideally suited to take advantage of the new silicon based inductors. Digital European Cordless Telecommunications (DECT) has a frequency range between 1.881 and 1.897 GHz with a channel spacing of 1.728 MHz. Personal Communication Systems (User PCS) has a bandwidth of 1.910 to 1.930 GHz with a channel spacing of 1.25 MHz.

The aim of this thesis is to design a frequency tunable high-frequency filter that also performs the function of an LNA. The filter has a frequency tuning range of 1.69 GHz to 2.0 GHz, this allows the filter to operate within the above mentioned standards as well as compensating for process and temperature changes. The filter will be designed for a 3 dB bandwidth narrow enough to select individual channels within the standards. To make the filter usable at the front end of a radio, it must have a low noise figure, large gain and large linearity.

2.3 Electrical Noise

Electrical noise is a fundamental issue in electronics for communications systems. Electrical noise sets the lower limit on the amplitude of the signal that can be processed, and an upper limit on the usable gain of the system [GM92]. Noise is generated from a variety of electrical devices and is generally uncorrelated. This indicates that noise can not be cancelled, but special design techniques can minimize the contribution of an electronic block to the overall noise performance of the system.

2.3.1 Sources of Noise

Thermal noise is accepted to be due to the random motion of electrons in a resistive material. This noise is directly proportional to the resistance and temperature of the material. Thermal noise is modeled either as a voltage source in series with the resistor or to a current source in parallel to the resistor, as illustrated in Figure 2.3

Figure 2.3 - Thermal noise models

The thermal noise generators in Figure 2.3 are given by

$$\overline{v^2} = 4kTR\Delta f \quad (2.1)$$

$$\overline{i^2} = 4kT\frac{1}{R}\Delta f \quad (2.2)$$

where k is Boltzmann's constant and Δf is the bandwidth in hertz.

Current is transferred in discrete amounts equal to the electron charge. Electrical noise that is generated from the non-continuous transfer of electrical charge is called shot noise. If the current has an average value of I_A , then the resulting shot noise current has a mean-square value

$$\overline{i^2} = 2qI_A\Delta f \quad (2.3)$$

where q is the electron charge, and Δf is the bandwidth in hertz.

Both shot and thermal noise are independent of frequency and thus have a uniform power spectral density over the bandwidth of interest. This type of noise is often called Gaussian or White noise [GM92].

Flicker noise is a low-frequency phenomenon, and occurs in all active devices and some passive elements such as carbon resistors. Flicker ($1/f$) noise in a bipolar transistor is caused mainly by traps associated with contamination and crystal defects in the emitter-base depletion layer[GM92]. These traps capture and release carriers in a random fashion and the time constants associated with the process give rise to a noise signal with energy concentrated at low frequencies. Flicker noise is associated with a constant current flow and has a mean-square value of

$$\overline{i^2} = K_1 \frac{I^a}{f^b} \Delta f \quad (2.4)$$

The constant b has a value of about unity, thus the noise spectral density of flicker noise has a $1/f$ frequency dependence.

2.3.2 Equivalent Input Referred Noise of a Bipolar Transistor

The equivalent input-referred noise of a system is a means of expressing the noise at the input to a noiseless system that would produce the same noise at the output as that of a noisy system. The advantages of this figure of merit is that it allows quick comparison of the incoming input signal with the noise of the system and the impact that this noise will have on the signal integrity.

The equivalent input noise is modeled as a voltage source and a current source at the input to the system. The equivalent input noise to a bipolar transistor is illustrated in Figure 2.4.

Figure 2.4 - Equivalent input noise of a bipolar transistor

This configuration accounts for any value of source impedance. Consider the two extreme cases where the input impedance $R_s=0$ and $R_s=\infty$. In the first case, $R_s=0$, the current noise generator is shorted out and the output noise is due to the voltage noise generator. If the input is left open, ie $R_s=\infty$, then the voltage noise generator will not affect the output noise, and any output noise is due to the current noise generator.

It can be shown that the equivalent input voltage noise generator of a bipolar transistor is [GM92]

$$\overline{v_i^2} = 4kTR_{eq}\Delta f \quad (2.5)$$

where

$$R_{eq} = r_b + \frac{1}{2g_m} \quad (2.6)$$

In Equation 2.6, r_b is the base resistance of the bipolar transistor, and g_m is the transconductance. Equation 2.6 indicates that the spectral density of the equivalent input voltage noise generator is independent of frequency, thus it exhibits Gaussian noise. It also shows two means by which the equivalent input referred noise of a BJT can be reduced. The first is by reducing the base contact resistance. In an integrated environment this is equivalent to choosing the larger size devices. Second, by running more current through the device, the transconductance g_m of the device increases, thus reducing the $1/2g_m$ term in Equation 2.6.

The equivalent input current noise generator can be found to be [GM92]

$$\overline{i_i^2} = 2qI_{eq}\Delta f \quad (2.7)$$

where

$$I_{eq} = I_B + K_1 \frac{I_B^a}{f} + \frac{I_C}{\beta(j\omega)^2} \quad (2.8)$$

In Equation 2.8, I_B and I_C represent the base and collector currents respectively, $\beta(j\omega)$ represents the gain through the BJT, and K_1 is the constant from flicker noise.

Equation 2.7 indicates that the equivalent input current noise source comes from a current I_{eq} which shows full shot noise. The current I_{eq} is a fictitious current composed of the base current shot noise, flicker noise and the collector current shot noise referred back to the input. Equation 2.8 indicates that the equivalent input current noise spectral density is not constant with frequency. At low frequencies the flicker term dominates the noise at the input, whereas at higher frequencies the gain of the device decreases and the shot noise due to collector current starts to dominate the input noise of the system.

To optimize the noise performance of a BJT, Equation 2.8 indicates that the device should be run at extremely low currents to reduce contributions from base and collector shot noise. This is in conflict with the findings in Equation 2.6, and the actual optimum noise performance of the BJT is a compromise between the constraints set by Equations 2.6 and 2.8.

The input referred noise of a common emitter amplifier is plotted in Figure 2.5.

Figure 2.5 - Input referred noise of a common emitter amplifier

Figure 2.5 shows the flicker ($1/f$) noise at lower frequencies, and the increase in the input noise as f^2 at higher frequencies. The corner frequency, f_a , is called the flicker noise corner and is a function of the process. For a common emitter amplifier in the BATMOS process, the simulated corner frequency f_a , is approximately 100Hz. Corner frequency f_b can be found using equation 2.9 [GM92]

$$f_b = f_T \sqrt{\frac{I_B}{I_C}} \quad (2.9)$$

Using the data provided from small signal analysis, for the BATMOS 15x transistor, f_b is 1.4 GHz. This value is in close agreement with the simulated value, in Figure 2.5, of 1.9 GHz.

2.4 The Integrated Inductor

Planar inductors are regularly found in a variety of microwave circuits using many different types of substrates (e.g. FR-4, GaAs and ceramic and sapphire hybrids) [NM90][Lo92]. Planar inductors fabricated on silicon substrate were investigated in the early development of silicon integrated circuits. Limitations in processing techniques, a low resistive substrate and a low frequency of operation led to excessive use of chip area and low Q inductors. Advancement in lithographic techniques, high resistive substrates and applications in the microwave frequency range have led to the revival of planar inductors on silicon substrate. In the low Gigahertz frequency range, inductor Q values of 3 - 8 have been reported [NM90][Lo92].

2.4.1 Integrated Inductor Geometry

Figure 2.6 below illustrates the layout geometry of a planar inductor. The planar inductor is a series of microstrip lines.

Figure 2.6 - Geometry of a spiral inductor

When a potential is applied across the inductor, adjacent microstrip lines have current flowing in the same direction. This causes the mutual inductance between adjacent lines to increase resulting in a higher overall inductance. Decreasing the spacing between adjacent

lines, W_s , increases the mutual inductance. The inductor is formed using the top metal layer of the fabrication process [Lo93]. The silicon dioxide SiO_2 , provides isolation of the inductor from the substrate, thus reducing the parasitics to the substrate. Isolation, W_i , of the inductor from adjacent components is provided to prevent coupling. A gap, W_g , of about 5 line widths, W_L , is intentionally left in the center of the inductor. It was found that winding the inductor right to the center reduces the Q [Lo93]. The center winding is contacted with the next lowest metal. This results in larger capacitive parasitics at the port represented by the inner winding; this is taken into account in simulations.

2.4.2 Integrated Inductor Process Parameters

The inductor is fabricated using a planar structure on the active circuit silicon substrate [NM90][Lo93]. A square metal spiral forms the inductor which sits on a thick oxide layer which in turn rests on the silicon substrate. The available inductance ranges from 2 to 8 nH, and are limited to the frequency range 1 to 10 GHz [Lo93]. Below 1 GHz, poor coupling between adjacent windings and high losses through the substrate result in a very low Q value, while self resonance limits their operation above 10 GHz.

Several parameters affect the Q and inductance of the inductor. Figure 2.7, illustrates a cross sectional view through adjacent planar microstrip lines. Increasing the metal width, W_m , and decreasing the spacing, W_s , between adjacent lines results in stronger coupling, which in turn increases the Q of the microstrip lines. Higher inductance is realized by increasing the number of spirals per unit area [Lo93] which is accomplished by decreasing the line width, W_m . A relatively high series resistance results from the thin metal layer, t_m , used to realize the spiral inductor. This degrades the quality of the integrated inductor [LCK94].

Figure 2.7 - Cross-sectional view through a planar inductor

Figure 2.8, is the lumped equivalent model of the inductor. The model is broken up into two sections in order to better approximate the experimental data [Lo93].

Figure 2.8 - Model of the inductor

The self inductance of the planar structure is modeled by L_{1a} and L_{1b} . The sheet resistance of the top metal is modeled by R_{sl1} , and R_{slb} . Capacitors, C_{ox1} , C_{ox2} , and C_{ox3} model the capacitance formed by the oxide layer found between the microstrip lines and the silicon substrate. Losses through the substrate are modeled as capacitors, C_{sb1} , C_{sb2} , and C_{sb3} and resistors R_{sb1} , R_{sb2} and R_{sb3} . The magnitude of the capacitors modeling the oxide and the substrate can be reduced by moving the ground plane further away from the inductor. This

is accomplished by using the top metal layer of the process to form the inductor [Long]. Capacitors, C_{p1} , C_{p2} , and C_{p3} are the coupling capacitance between adjacent line segments of planar structure. These values are on the order of a few 10 fF and have no effect in applications where the frequency of operation is less than 5 GHz.

S-parameters were generated by J. Long [Lo93] based on the dimensions of the metal spirals required to realize the desired inductance. The Eesof linear simulator, Touchstone, was used to optimize the parameters of the distributed model until the S-parameters of the model matched the generated S-parameters. The inductor model is optimized as a one port element to match the layout configuration. Final values for the inductor model are: $L_{1a} = 1.62\text{nH}$; $L_{1b} = 1.62\text{nH}$; $R_{s1a} = 2.63\ \Omega$; $R_{s1b} = 2.63\ \Omega$; $C_{ox1} = 139.8\ \text{fF}$; $C_{ox2} = 2.442\ \text{fF}$; $C_{ox3} = 0$; $R_{sb1} = 357.6\ \Omega$; $R_{sb2} = 2.14\ \Omega$; $R_{sb3} = 0$; $C_{p1} = 7.18\ \text{fF}$; $C_{p2} = 0.05\ \text{fF}$; and $C_{p3} = 0.246\ \text{fF}$. Output from the Touchstone optimizer is shown Figure 2.9. Figure 2.9a shows a plot of the self inductance of the metal spirals as frequency is increased. Figure 2.9b shows a plot of Q vs frequency, and Figure 2.9c shows a plot of the S11 parameter on a Smith Chart. In all three plots the frequency is swept from 0.1 GHz to 10 GHz, and a comparison is made between the data obtained from the generated S-parameters and the data generated using the distributed model.

Figure 2.9a - Inductance vs frequency

In Figure 2.9a, the inductance of the model matches the inductance extracted from the generated S-parameters. In both curves the inductance is relatively constant at low frequencies and starts to increase dramatically at higher frequencies. The increased inductance at higher frequencies indicates that the inductor is approaching self resonance. The inductor has a value of approximately 3.4 nH at the frequency of interest, 1.8 GHz.

The Q data from S-parameters and the distributed model are in agreement in Figure 2.9b. For both curves the Q starts at a low value at lower frequencies, reaches a peak at 2.5 GHz, and then rolls off at higher frequencies. The roll-off at high frequency indicates that the inductor is approaching its self resonant frequency. At the self resonant frequency the reactance of the inductor cancels with the reactance of the parallel capacitance. This results in a low Q which is defined as the ratio of the imaginary to real component of the S-parameter. The plot also shows a poor Q at lower frequencies. This is due to poor coupling and high losses through the square spiral structure. The Q is 5.5 at the frequency

of interest, 1.8 GHz.

Figure 2.9b - Q vs frequency

Figure 2.9c combines the information from Figures 2.9a and 2.9b and plots them on a Smith chart. The plot starts at the left of the Smith chart, at lower frequencies. This point has a low resistive and low reactive value, which indicates an inductor with a low Q. As the frequency is swept from 0.1 GHz to 10 GHz, the S11 parameter traverses a curve towards the region with a higher reactive and higher resistive component. The point of peak Q is found in the middle of the curve. A further sweep of the frequency would result in the inductor reaching its self resonant frequency, at which point it would be capacitive and the curve would end up in the lower half of the Smith chart.

Figure 2.9c - Plot of S11 on a Smith Chart

2.5 Integrated Varactor

The varactor is formed by the base-collector junction capacitance of a BJT. This capacitance is the sum of the base-collector diffusion capacitance (C_{BCdiff}), and the depletion capacitance (C_{BCdep}) [Hs93].

$$C_{BC} \approx K_1 \cdot CJC + K_2 \cdot e^{K_3 V_{BC}} \quad (2.10)$$

Here K_1 , K_2 , and K_3 are constants, V_{BC} is the base collector bias voltage, and CJC is the base-collector zero bias depletion capacitance. The base-collector bias voltage is negative for the intended application. This equation indicates that the base collector capacitance starts out at a value dependant on bias conditions, and decreases exponentially, with base collector bias voltage, to a non-zero value when V_{BC} reaches zero volts.

A series of small signal analysis was performed to extract the shape of the capacitance curve with varying bias voltage. Six 15x devices, and one 5x BJT device are tied in parallel to obtain a large enough variation in capacitance to tune the filter over the desired frequency tuning range. The emitter of each device is tied to the bases to eliminate the need for a dc bias current. Figure 2.10 shows the variation in base collector capacitance

with bias voltage.

Figure 2.10 - Base-collector junction capacitance vs V_{BC} bias voltage

The curve has a maximum capacitance value at zero base-collector bias voltage, and decreases exponentially as predicted by Equation 2.10. The capacitance varies from 1.7 pF to 1.07 pF over the base-collector tuning range. This variation in capacitance provides a frequency tuning range of 200 MHz centered around 1.85 GHz.

In the following chapter, a small signal analysis is performed in order to gain insight into the operation of the filter and to identify the tuning elements so that an accurate center frequency, and Q-tuning function, can be obtained.

Chapter 3

Filter Design

This chapter presents the design for two filters incorporating integrated spiral inductors on silicon substrate. A circuit description, small-signal analysis and root locus plots are given for each circuit. Simulation results excluding board and package parasitics are presented. Package parasitics, however, have a major impact on the frequency response of a circuit and should not to be ignored.

The first filter is derived from the voltage-controlled oscillator (VCO) work of Nguyen & Meyer [NM92]. The VCO design has been modified to facilitate an RF input. This filter features two integrated tank circuits tuned to separate frequencies. The response from each tank is summed using a variable gain amplifier. This enables frequency tuning of the response from the lower frequency tank circuit to the higher frequency tank circuit. The filter has a differential RF input port and single-ended RF output port. The remainder of this thesis will refer to this filter as the Stagger-Tuned Filter (STF).

The second filter is a new and separate design and features an integrated inductor and an integrated varactor. This filter is single ended and is designed for lower power than the STF. This filter is referred to as the Varactor-Tuned Filter (VTF).

Both filters are intended for image reject filter applications at the front end of an RF receiver. They feature a noise figure of 4.5 dB, gain in excess of 50 dB, Q-tuning and a 200 MHz frequency tuning range. The filters are targeted to operate in the 1.7 to 1.94 GHz frequency range. An external current source is used to tune the circuit Q from ten to several hundred, and an external dc voltage is used to tune the center frequency of the bandpass response. Both filters are equipped with an output buffer for driving off chip.

3.1 Stagger-Tuned Filter

A complete schematic of the STF, including the RF input port, is shown in Figure 3.1.

Figure 3.1a - Frequency Control Predistortion Circuit and signal processing core

Figure 3.1b - Switchable capacitor array

Figure 3.1c - Voltage bias circuit and output drive circuit

3.1.1 Circuit Description

The overall schematic of the Q-enhanced, LC, frequency tunable filter, is shown in Figure 3.1. The filter contains two resonant tank circuits formed using LC components. The inductors (L_1 , L_2) are fabricated using planar structures on the active circuit silicon substrate as discussed in chapter 2. The circuit accepts a broadband RF differential input signal (V_{RF}^+ , V_{RF}^-) and converts it to a proportional current through differential pair Q_{14} , Q_{17} . The signal current is fed to a variable attenuator formed by transistors Q_{10} , Q_{11} , Q_{12} and Q_{13} . The single-ended frequency tuning voltage, V_{freq_tuning} , drives the diode connected transistors, Q_1 and Q_2 , to produce a predistorted differential output, V_{fc}^+ - V_{fc}^- . The dc voltage V_{fc}^+ - V_{fc}^- controls the level of attenuation associated with each resonant tank circuit. This provides a means to vary the center frequency of the filter from the left resonant tank, when Q_{10} is on and Q_{13} is off, to the resonant frequency of the right resonant tank when Q_{10} is off and Q_{13} is on. The output from the tuned loads passes through a voltage divider, formed by C_f , C_x , and is fed back to the differential pair Q_{15} , Q_{16} . The bias current, I_{qbias} , determines the gain, g_f , of the differential pair, Q_{15} and Q_{16} , and thus the magnitude of the feedback signal. This allows tuning of the circuit Q by varying I_{qbias} . The voltage divided output is passed to a differential to single-ended converter, Q_{26} and Q_{27} , in Figure 3.1c. The single-ended signal is passed to a darlington pair “emitter-follower output buffer” for driving off-chip.

In the following subsections, the circuit is analysed as smaller functional blocks. The blocks include a predistortion circuit for the frequency tuning voltage, the main signal processing core, a differential to single-ended converter and an output buffer for driving off-chip. Each block is described in detail, as well as its interaction with interconnecting blocks.

3.1.2 Signal Processing Core

The signal processing core is presented in Figure 3.2. This core is composed of an input differential pair, a positive feedback network, a variable attenuator, and two resonant LC filters tuned to different center frequencies.

Figure 3.2 - Signal processing filter core

The RF input voltage is converted to a differential current by differential pair Q_{14} and Q_{17} . The converted input current is delivered to nodes 3 and 4 where they are passed to the variable attenuator formed by transistors Q_{10} , Q_{11} , Q_{12} and Q_{13} . Control voltages V_{fc}^+ and V_{fc}^- , vary the amount of input current delivered to each resonant load. This provides a means to tune the frequency in a range bounded by the center frequencies of each resonant load. The resonant loads convert the current to a differential voltage at nodes 1 and 2, which is then divided down by the capacitive voltage divider formed by C_f and C_x to produce outputs V_A and V_B . These outputs drive the positive feedback differential pair formed by transistors Q_{15} and Q_{16} . The feedback differential pair converts the divided down output voltage to a proportional differential current. The magnitude of the converted current is dependant on the g_m of transistors Q_{15} and Q_{16} , which is controlled by current I_{qbias} . Thus the amount of feedback, and hence circuit Q, is controlled by bias current

of the resistance of the tank circuit, resulting in a higher circuit Q. This is better illustrated by analysis of the transfer function, which is derived from the control diagram of Figure 3.3(b), and is modelled by Equation 3.1. The transfer characteristics of block H_1 in Figure 3.3(b) is the equivalent impedance of L_1 , C_1 , R_1 , C_{f1} and C_{x1} . This impedance, presented in equation 3.1, transforms the input current to a voltage, used to drive the voltage divider.

$$H_1 = \frac{sLR[C_f + C_x]}{s^2LR[C_1(C_f + C_x) + C_fC_x] + sL[C_f + C_x] + R[C_f + C_x]} \quad (3.1)$$

The transfer characteristics of block H_2 is the voltage divider formed by C_f and C_x , and is used to drive the feedback v_{ccs} .

$$H_2 = \frac{C_f}{C_f + C_x} \quad (3.2)$$

Blocks g_m and g_f are the transconductance of the input transistor and feedback v_{ccs} respectively. The voltage at node V_A , can be written in terms of the transfer blocks as:

$$\frac{V_A}{V_i} = -g_m \cdot \frac{aH_1H_2}{1 - ag_fH_1H_2} \quad (3.3)$$

The overall transfer function, Equation 3.4, can be written in terms of component values by substituting Equations 3.1 and 3.2 into 3.3:

$$\frac{V_A}{V_i} = -g_m \frac{sC_f a}{s^2[(C + C_f)(C_f + C_x) - C_f^2] + s[g(C_f + C_x) - ag_fC_f] + \frac{(C_f + C_x)}{L}} \quad (3.4)$$

where g is the conductance of resistor R_1 .

The midband gain G , center frequency ω_o , and Q can be derived by comparing Equation 3.4, with the standard transfer function for a bandpass filter [SS87].

$$\frac{V_o}{V_i} = \frac{As \frac{Q}{\omega_o}}{s^2 + s \frac{Q}{\omega_o} + \omega_o^2} \quad (3.5)$$

The midband gain (G) is given by equation 3.6, equations 3.7 and 3.8 give the center frequency and Q respectively.

$$G = \frac{-g_m C_f a}{g(C_f + C_x) - a g_f C_f} \quad (3.6)$$

$$\omega_o = \sqrt{\frac{(C_f + C_x)}{L[(C + C_f)(C_f + C_x) - C_f^2]}} \quad (3.7)$$

and

$$Q = \omega_o \left[\frac{(C + C_f)(C_f + C_x) - C_f^2}{g(C_f + C_x) - a g_f C_f} \right] \quad (3.8)$$

Equation 3.6 shows that the midband gain is dependant on feedback gain, g_f . Equations 3.7 and 3.8 indicate that the center frequency is independent of variations in Q and feedback gain, but that system Q is dependant on center frequency. This is verified by simulations and measurement results and is shown in chapter 4.

Increasing the feedback gain, g_f , moves the poles closer to the $j\omega$ axis in the complex plane which results in a higher system Q . A root locus plot of Equation 3.4 with varying feedback gain is shown below in Figure 3.4. The typical component values are: $g_m=10e-3$; $C=2.55pF$; $C_f=10pF$; $C_x=5pF$; $L=6.9nH$; $g=1/500$ and $a=1$.

Figure 3.4 - Root locus as a function of increasing feedback gain

Figure 3.4 shows the poles moving closer to the $j\omega$ axis with increasing feedback gain. The center frequency remains constant [FPN86] over the feedback gain range as predicted by Equation 3.6. The Q of the circuit increases with increasing feedback gain.

With an understanding of the operation of the inner loops, the outer loop is presented in Figure 3.5 to illustrate how the two halves of the circuit are combined.

Figure 3.5 - Control diagram of full circuit

The inner loops of the circuit are enclosed within the shaded boxes. The outer loop sums the response from the two inner loops to provide the overall response of the circuit. The input signal is passed through a gain block of $g_m/2$ before being presented to the tuned circuits of the inner loops. Local feedback, $g_{f1}/2$, provides Q-enhancement to each tuned element. The inner loops cross-feed each other through blocks $g_{f2}/2$. The outputs, V_A and V_B , are summed in a differential to single-ended converter (not shown in diagram) and passed to an output buffer for driving into a load. Blocks a and b represent the variable attenuator where:

$$a + b = 1 \quad (3.9)$$

The transfer function of the circuit is derived using Figure 3.5. The transfer function of V_A as a function of V_{in} is given below in Equation 3.10.

$$\frac{V_A}{V_{in}} = -\frac{g_m}{2} \frac{aH_1H_2}{1 - \frac{g_f}{2}bH_3H_4 - \frac{g_f}{2}aH_1H_2} \quad (3.10)$$

where H_1 and H_3 are given by Equation 3.1; H_2 and H_4 are given by Equation 3.2 for each inner loop respectively.

Substituting Equations 3.1 and 3.2 for H_1 , H_2 , H_3 and H_4 and changing component values to G , Q and ω_0 by using Equations 3.6, 3.7 and 3.8, the transfer function for V_A as a function of V_{in} is shown in Equation 3.11.

$$\frac{V_A}{V_{in}} = \frac{-\frac{g_m}{2}sG_1\frac{\omega_{o1}}{Q_1}\left[s^2 + s\frac{\omega_{o2}}{Q_2}\left(1 + \frac{g_f}{2}G_2\right) + \omega_{o2}^2\right]}{s^4 + s^3\left[\frac{\omega_{o1}}{Q_1} + \frac{\omega_{o2}}{Q_2}\right] + s^2\left[\omega_{o1}^2 + \omega_{o2}^2 + \frac{\omega_{o1}\omega_{o2}}{Q_1Q_2}\left(1 - \frac{g_f^2}{4}G_1G_2\right)\right] + s\left[\omega_{o1}^2\frac{\omega_{o2}}{Q_2} + \omega_{o2}^2\frac{\omega_{o1}}{Q_1}\right] + \omega_{o1}^2\omega_{o2}^2} \quad (3.11)$$

Similarly the transfer function for V_B as a function of V_{in} is derived and shown in Equation 3.12.

$$\frac{V_B}{V_{in}} = \frac{\frac{g_m}{2}sG_2\frac{\omega_{o2}}{Q_2}\left[s^2 + s\frac{\omega_{o1}}{Q_1}\left(1 + \frac{g_f}{2}G_1\right) + \omega_{o1}^2\right]}{s^4 + s^3\left[\frac{\omega_{o1}}{Q_1} + \frac{\omega_{o2}}{Q_2}\right] + s^2\left[\omega_{o1}^2 + \omega_{o2}^2 + \frac{\omega_{o1}\omega_{o2}}{Q_1Q_2}\left(1 - \frac{g_f^2}{4}G_1G_2\right)\right] + s\left[\omega_{o1}^2\frac{\omega_{o2}}{Q_2} + \omega_{o2}^2\frac{\omega_{o1}}{Q_1}\right] + \omega_{o1}^2\omega_{o2}^2} \quad (3.12)$$

The root locus of this filter as a function of feedback gain is constructed using the characteristic equation 3.10. Three cases are plotted: 1) $a > b$; 2) $a = b$; and 3) $a < b$. Each case represents one of three conditions in which this circuit operates. The first condition represents the output response when it is dominated by the tuned elements L_1C_1 , the second corresponds to both tank circuits being equally active. The last case defines the output when tuned elements L_2C_2 dominate the output response. Typical component values used are: $g_m=36.7e-3$; $c_{pi}=0.37pF$; $c_{f1}=1.5pF$; $c_{x1}=0.4pF$; $c_{f2}=1.5pF$; $c_{x2}=0.4pF$; $c_1=3.65pF$; $L_1=2.4nH$; $c_2=3.18pF$; and $L_2=2.4nH$. Where c_{pi} is the base-emitter capacitance and g_m is the transconductance of a BJT.

Figure 3.6 - Root locus; $a > b$

Figure 3.7 - Root locus: $a = b$ Figure 3.8 - Root locus: $a < b$

The poles contributed by load L_1C_1 , in Figure 3.6, move towards the $j\omega$ axis with increasing feedback gain and hence dominate the frequency response. Figure 3.8 illustrates the case where the poles contributed by load L_2C_2 dominates the response. In Figure 3.7, both loads are equally active and the poles contributed by each load moves towards the $j\omega$ axis. This gives a composite frequency response of the two individual tuned responses.

In order to have strong coupling between the two tank circuits, which results in a single resonant response, the two tank circuits must be closely spaced in frequency. Additional circuitry is required to extend the frequency tuning range. Switchable capacitors, Figure 3.1b, extend the frequency range of operation from 75 MHz to 200 MHz. When activated, by control signals V_{fc1} , V_{fc2} and V_{fc3} , the capacitors add in parallel to the tank capacitor.

3.1.3 Linear Frequency Response

A standard predistortion circuit [GM93] is used to tune the center frequency using a control voltage. This circuit is shown in Figure 3.1a.

3.1.4 Differential to Single-Ended Converter and Output Buffer

Differential pair Q_{26} , Q_{27} are used to convert the signal from differential to single-ended. The transfer function of V_C as a function of V_A and V_B is given in Equation 3.12.

$$V_C = \frac{g_m R_{18}}{2} [V_A - V_B] \quad (3.13)$$

where g_m is the transconductance of transistors Q_{26} and Q_{27} .

Figure 3.9 - Differential to single-ended converter and Output Buffer

The minimum size output bipolar transistor in BATMOS is a 45x [CMC93]. A Darlington pair, Q_{30} and Q_{31} , is used to boost the input impedance and current gain while providing a low output impedance. Transistor Q_{30} is a 4x device to help reduce the capacitive loading of node V_C . Transistor Q_{31} is a 45x device to conform to the design rules.

3.1.5 Simulation Results

HSPICE [Hs92] is used to perform small-signal simulation to aid in biasing the circuit and to provide an approximation to the frequency response. The response of the circuit is characterized over varying frequency control voltage and varying feedback control current. The noise figure of the circuit is simulated over the entire frequency tuning range.

Initial simulations are performed to verify the circuit operation for selected components, bias currents and bias voltages. The small-signal simulations from HSPICE are compared with the equations for the small-signal model. Adjustments to component values were necessary to compensate for shifts in the desired center frequency due to transistor parasitic capacitances.

Figure 3.10 shows the output for three small-signal analyses. The circuit is first biased to provide a circuit Q of 430 at a frequency control voltage of 2.5 volts. The frequency control voltage is then set to two other values and the output is plotted.

Figure 3.10 - Frequency sweep with fixed feedback current.

The curve with the highest center frequency peaks at 1.892 GHz, with a circuit-Q of 430. This curve is produced with a frequency control voltage, V_{fc} , of 2.5 volts, the middle curve is produced with a V_{fc} of 2.3 volts. This curve has a center frequency of 1.872 GHz and a circuit-Q of 234. The final curve is produced with a V_{fc} of 2.1 volts, and has center frequency of 1.855 GHz with a Q of 95. The feedback current, I_{qbias} , is set to 2.07 mA for all three plots.

Equation 3.8, for circuit-Q, predicts that as the center frequency decreases, if all other parameters remain unchanged, the circuit-Q should also decrease. This is evident from Figure 3.10, where the circuit Q decreases by 335 for a 37 MHz decrease in center frequency.

Figure 3.11 shows the output of three small-signal analyses. The frequency control voltage is set at 2.5 volts and the bias current, I_{qbias} , is swept to produce a wide change in circuit Q.

Figure 3.11 - Sweep of feedback current, with fixed frequency control voltage

From Figure 3.11, the circuit Q changes from 67 to 420 with increasing feedback current. The high Q curve is produced with a feedback current of 2.05 mA, it has a center

frequency of 1.894 GHz and a Q of 420. The middle curve is produced with a feedback current of 1.98 mA, it has a center frequency of 1.897 GHz and a Q of 124. The final curve is produced with a feedback current of 1.90 mA, it has a center frequency of 1.90 GHz and a Q of 67. The frequency control voltage is set to 2.5 volts for all three plots.

In Figure 3.11, there is a slight variation in center frequency as the circuit Q is tuned. Equation 3.7 predicted that the center frequency should be stable over varying feedback current. The observed variation can be attributed to changing bias conditions in the circuit as I_{qbias} is varied. This causes junction capacitance in the active BJT devices to vary slightly which causes slight shifts in the center frequency. The center frequency shifts by 6 MHz for a change in circuit-Q of 353.

The Stagger-Tuned Filter has an overall simulated frequency tuning range between 1.69 GHz and 1.94 GHz. The Q is tunable to several hundred over this entire range.

The HSPICE small-signal analyzer is used to predict the noise figure of the circuit. The circuit has a nominal noise figure of 5 dB, with a slight degradation at the higher frequency end. This degradation is due to a decrease in the BJT current gain, which causes the noise of each BJT device to rise as f^2 [GM93].

3.2 Varactor-Tuned Filter

Recent work in the area of high frequency VCO design [Da93] has investigated the use of base collector capacitance as a tuning element. Discussions with Dauphinee [Da1], and Plett [PI92], coupled with work performed on the stagger-tuned circuit, have resulted in the experimental integrated varactor used in this new iteration of the tuned LC filter.

The following section provides an overview of the circuit operation. Detailed analysis is deferred to subsequent sections of this chapter.

Figure 3.12 - LC Q-enhanced, frequency tunable, RF monolithic filter

3.2.1 Circuit Description

The overall schematic of the varactor-tuned, LC, Q-enhanced filter is shown in Figure 3.12. The circuit accepts a broadband RF input signal at the base of transistor Q_{2a} . Emitter degeneration is used at the emitter of transistor Q_{2a} to extend the linear range of operation [GM93]. The output of Q_{2a} feeds into a cascode transistor, Q_{2b} , to reduce the Miller effect [SS87]. Cascode transistor Q_{2b} feeds the converted input current into the resonant tank, formed by integrated inductor L_1 and integrated varactor D_1 , where it is converted back into a voltage. The tuned voltage is capacitively coupled through C_f to the base of transistor Q_3 . Differential pair Q_4 and Q_3 form the positive feedback network. The effective transconductance of differential pair Q_3 , Q_4 transforms the base feedback voltage to a proportional feedback current. The transconductance of differential pair Q_3 , Q_4 is controlled by the current mirror formed by transistors Q_5 and Q_6 . The feedback current is fed through a cascode, to reduce the Miller effect [GM93], and back into the tuned load where it is summed with the input current and converted back into a voltage. The sense of the feedback current is chosen to provide positive feedback. Transistors Q_{12a} and Q_{12b} form a Darlington pair for driving the off-chip load. The Darlington pair configuration provides a high input impedance and a low output impedance [GM93].

Many considerations were required for the initial selection of component values, transistor sizes, and dc bias conditions. All signal carrying transistors, except Q_{12b} , are chosen as 15x devices. Design guidelines [CMC93] require transistor Q_{12b} to be a 45x device. The 15x device has a reasonably high f_T , a low series base resistance and acceptable junction capacitance. The voltage bias devices, Q_{v1} , Q_{v2} and Q_{v3} , carry a low current and hence do not require a large area. The 4x device was selected for its current-to-area ratio. The current bias devices, Q_5 and Q_6 are selected as 15x devices for their higher current carrying ability.

The major noise contributions by the BJT device is base resistance, base and collector shot noise. As the f_T of the device rolls off at higher frequencies, the collector shot noise becomes dominant [GM93]. HSPICE optimization [Mo95] was extensively used to minimize the noise figure. The optimization goal was set for maximum gain at the

resonant frequency. This goal ensures that the transistors are operating at or near their max f_T point, which reduces the noise of the device.

3.2.2 Small-Signal Analysis

Figure 3.13 shows a simplified circuit which is representative of the varactor-tuned circuit. The distributed inductor model has been simplified to a parallel LR model represented by L_1 and R_1 . The integrated varactor is represented by capacitor C_1 . The voltage controlled current source, v_{ccs} , represents the feedback network formed by transistors Q_3 , Q_4 , Q_7 and Q_8 of Figure 3.12. Many alternatives were explored for the positive feedback path, including feeding back to the emitter or base of the input RF transistor. Ultimately, the best performance was achieved by summing the input signal with the feedback signal at the tuned load. Coupling capacitor C_f is shown as well as capacitance C_x , which represents the base emitter capacitance of Q_3 in parallel with the base emitter capacitance of Q_{12a} .

Figure 3.13 - Simplified circuit illustrating positive feedback

The v_{ccs} is controlled by the voltage potential across its terminals. As this potential increases, the current through the v_{ccs} increases. This behavior is similar to that of a negative resistor. Thus by varying the feedback, g_f , the “negative” resistance cancels part of the resistance of the tank circuit, resulting in a higher circuit Q . This is better illustrated by analysis of the transfer function of Figure 3.13. The techniques used to derive the transfer

function are similar to those used to derive Equation 3.4, so are not repeated.

$$\frac{V_{out}}{V_{in}} = -g_m \frac{sC_f}{s^2 [(C + C_f)(C_f + C_x) - C_f^2] + s[g(C_f + C_x) - g_f C_f] + \frac{(C_f + C_x)}{L}} \quad (3.14)$$

where g is $1/R_1$.

The standard transfer function for a bandpass filter [SS87], Equation 3.5, is used to derive the midband gain G , center frequency ω_o , and Q of the bandpass response in Equation 3.14.

$$G = \frac{-g_m C_f}{g(C_f + C_x) - g_f C_f} \quad (3.15)$$

$$\omega_o = \sqrt{\frac{(C_f + C_x)}{L[(C + C_f)(C_f + C_x) - C_f^2]}} \quad (3.16)$$

and

$$Q = \omega_o \left[\frac{(C + C_f)(C_f + C_x) - C_f^2}{g(C_f + C_x) - g_f C_f} \right] \quad (3.17)$$

Equation 3.15 shows that the midband gain is dependant on feedback gain, g_f . Equation 3.16 indicates that the center frequency is independent of variations in feedback gain. Equation 3.17 represents the system Q , not to be confused with the inductor Q . This equation shows that the system Q can be tuned by varying the feedback gain g_f . It also shows that system Q is dependant on center frequency. This is undesirable and indicates that Q tuning must be performed each time the center frequency is tuned. This is verified by simulations and measurement results and is shown in later chapters.

Increasing the feedback gain g_f , moves the poles closer to the $j\omega$ axis in the complex plane which results in a higher system Q . A root locus plot of Equation 3.14 with varying feedback gain is shown below in Figure 3.14 for typical values of $g_m=10e-3$; $C=2.55pF$; $C_f=10pF$; $C_x=5pF$; $L=6.9nH$; and $g=1/500$.

Figure 3.14 - Root locus as a function of increasing feedback gain

The poles start at the X position with no feedback gain and move towards the $j\omega$ axis as feedback is increased. The circuit Q increases as the poles are moved towards the $j\omega$ axis [GM93], and with enough feedback the poles can be moved into the right half plane resulting in oscillations.

Equation 3.16 is used to select component values for the center frequency. The value of C_1 is selected as the mid point in the C - V_{bc} curve shown in Figure 2.10. The value C_x is obtained by performing an operating point analysis of the circuit and obtaining C_{π} for transistors Q_3 and Q_{12a} of Figure 3.12. The value of C_f is chosen to make the voltage divider formed by C_f , C_x insensitive to process variations. Finally the inductor L_1 is selected from the available values between 2 to 8 nH.

3.2.3 Small-Signal Simulation Results

Initial simulations are performed to verify the circuit operation for selected components, bias currents and bias voltages. The small-signal simulations from HSPICE [Hs92] are compared with the equations for the small-signal model. Adjustments to component values were necessary to compensate for shifts in the desired center frequency due to transistor parasitic capacitances. The response of the circuit is characterized over varying frequency control voltage and varying feedback control current. The noise figure of the circuit is simulated over the entire frequency tuning range.

Figure 3.15 shows the output of three small-signal analyses. The circuit is first biased to provide a circuit Q of 100 at a frequency control voltage of zero volts. The frequency control voltage is then set to two other values and the output is plotted.

Figure 3.15 - Frequency sweep with fixed feedback current.

The curve with the highest center frequency sits at 2.21 GHz, with a circuit-Q of 100. This curve is produced with a frequency control voltage, V_{fc} , of zero volts, the middle curve is

produced with a V_{fc} of 4 volts. This curve has a center frequency of 2.06 GHz and a circuit-Q of 39. The final curve is produced with a V_{fc} of 5 volts, and has center frequency of 1.94 GHz with a Q of 24.

The results are consistent with the small-signal model and the varactor capacitance characteristics developed earlier. As the control voltage, V_{fc} , is swept from zero to five volts, Figure 2.10 indicates the varactor capacitance should go from its lowest value to its highest value. Equation 3.15, for center frequency, indicates that the circuit should have its highest center frequency for the lowest varactor capacitance. At a V_{fc} of 5 volts, the varactor attains the highest capacitance value, and equation 3.15 indicates that the circuit operates at the lowest center frequency. Equation 3.16, for circuit-Q, predicts that as the center frequency decreases and if all other parameters remain unchanged, the circuit-Q should also decrease. This is evident from Figure 3.15, where there is a 75% decrease in circuit Q for a 12% decrease in center frequency.

Figure 3.16 shows the output of three small-signal analyses. The frequency control voltage is set at the mid-point of 2.5 volts and the bias current, I_{qbias} , is swept to produce a 50% change in circuit Q from a value of 30 to a final value of 60.

Figure 3.16 - Sweep of feedback current, with fixed frequency control voltage

In Figure 3.16 variations in center frequency can be attributed to changing bias conditions in the circuit as i_{qbias} is varied. This causes junction capacitance in the active BJT devices to vary slightly which causes slight shifts in the center frequency. The center frequency shifts by 0.6% for a 50% change in circuit-Q. This figure shows that center frequency is relatively insensitive to variations in Q, as predicted by Equation 3.15.

Figure 3.17 steps the frequency control voltage in three jumps, 0 volts, 3.5 volts and 5 volts. The center frequency varies from 1.903 GHz to 2.198 GHz, a change of 295 MHz. The bias current, I_{qbias} , is adjusted at each frequency step to provide the maximum circuit Q. The bias current has a value of 1.085 mA at the higher frequency and 1.36 mA at the lower frequency. All three plots have circuit Q's of several hundred.

Figure 3.17 - Frequency sweep, with Q-adjustments

The HSPICE small-signal analyzer is used to predict the noise figure of the circuit. Figure 3.18 is a plot of noise figure as the frequency control voltage is swept over its operating range. The bias current, i_{qbias} , is adjusted at each frequency step to provide maximum circuit Q.

Figure 3.18 - Noise Figure over the operating range of the filter.

Figure 3.18 shows that the circuit has a nominal noise figure of approximately 6 dB, with a slight degradation at the higher frequency end. This degradation is due to a decrease in the BJT current gain, which causes the noise of each BJT device to rise as f^2 [GM93].

3.2.4 Large-Signal Simulation Results

Large signal simulations are performed on the extracted layout. These simulations exercise the transistor nonlinearities, providing a means of predicting distortion in the circuit. A series of large-signal analyses were performed to determine the 1 dB compression point of the filter. The results of these simulations are plotted in Figure 3.19.

Figure 3.19 - 1dB Compression point of Varactor-Tuned Filter

Figure 3.19 indicates that the input 1 dB compression point is -60 dBm. This value is low, and arises due to the constraint for low power dissipation. The output driver is lightly designed and is not able to handle large amounts of power before being driven into non-linear operation.

Chapter 4

Experimental Results

Experimental results are presented for the discrete and integrated versions of the Stagger-Tuned Filter (STF), as well as the Varactor-Tuned Filter (VTF). The test-setup, measurement procedures, and package modeling techniques are discussed. The performance characteristics of the two integrated filters are compared against each other. Testing was performed to measure the following characteristics: Q-tuning range at selected frequency intervals, the voltage-to-frequency transfer function, power dissipation, noise figure, maximum input power, and dynamic range. The measured results are also compared to the predicted results from simulations and discrepancies are discussed.

4.1 Discrete Version of the Stagger Tuned Filter

In anticipation of the integrated STF, a discrete version is designed to test the theoretical concepts behind the integrated filter. To minimize parasitic effects of board traces and package parasitics, the frequency of operation of the discrete version is designed for operation at 100 MHz.

The circuit is designed on FR-4 board material to obtain a fast, cost effective design. The material is widely used in industry to several GHz, and is therefore able to handle 100 MHz test signals. A transistor array is used to minimize the effects from package parasitics. The array is the "Ultra High Frequency Transistor Array μ PA102 and μ PA103" from NEC corporation. These transistors offer a cut-off frequency f_T of 10 GHz, similar to the cut-off frequency of the transistors used in the fully integrated version.

Discrete inductors are used for tuning the tank circuits. The inductors used have a self resonant frequency ten times higher than the intended frequency of operation. The Q of the inductors are modeled in SPICE simulations as an ideal inductor with a series resistance.

The board was conceptualized with assistance from TRIO [TRIO92], and the actual layout performed by the Electronic Technology Center [ETC92] from Carleton University. Figure 4.1 shows the schematic level diagram for the circuit used.

Figure 4.1 - Schematic of discrete, Stagger-Tuned Filter

In the discrete circuit version of Figure 4.1, resistors $R_{S1,2,3}$ set the maximum current, and potentiometers $R_{pot1,2,3}$ set the tuning range. Inductors $L_{4,5,6}$ act as RF chokes blocking ac signal from getting into the bias circuit. The value of inductors are chosen such that ωL is much greater than the impedance seen by the inductor looking into $R_{S1,2,3}$ (where ω is the frequency of operation). The decoupling capacitors, $C_{15,16,17}$, inductors $L_{4,5,6}$ and series resistors $R_{S1,2,3}$ form a series resonant tank circuit. A rule of thumb is to limit the Q of these tank circuits to less than 1, otherwise oscillations may occur in the biasing circuit.

Decoupling capacitors are chosen based on the impedance of the system. In this system, the impedance of the decoupling capacitors are chosen to be much less than $50\ \Omega$. This helps couple all ac noise and spikes to the ground plane. A tantalum type capacitor is used for decoupling noise from the power supply, as this has a lower series resistance than electrolytic capacitors.

The layout of the discrete filter is shown in Figure 4.2.

Figure 4.2 - Layout of discrete version of the Stagger-Tuned Filter

This circuit is fabricated on FR-4 material, using double-sided copper. In the layout all signal and bias paths are placed on the top layer, reserving the bottom layer for ground plane. DC power lines are routed on the top layer using thick lines to reduce any inductive

effects and series resistance at higher frequencies. Transmission lines, $50\ \Omega$ are used for signals entering or leaving the board. Internal signal lines are routed close to the center of the board to reduce the lengths of the traces. Sharp (90 degree) corners are avoided on signal carrying lines to reduce discontinuity in the signal. Component values for the resonant tank circuits are chosen based on Equations 3.7 and 3.8. The final dimensions of the board are 7.75cm x 8.6cm.

4.1.1 Experimental Set-up

This section describes the test set-up for testing of the discrete version of the stagger tuned filter. SMA type connectors are used to connect the $50\ \Omega$ impedances of the board to the $50\ \Omega$ test equipment. The HP 4195A is configured as a network analyzer and used to determine the frequency response of the board. DC power is supplied to the board by an HP 6215A power supply.

4.1.2 Simulation and Measurement Results

The intended purpose of the discrete version is to verify the concept and theory underlying the integrated stagger tuned filter. As such, only a limited number of simulations and measurements are performed.

The SPICE parameters for the transistors in the transistor array are obtained and HSPICE simulations are performed to model the behavior of the circuit. Bondwire parasitic inductance is included in the simulation model. The SPICE parameters for the transistor array can be found in Appendix A.

Figure 4.3a, shows the simulated frequency response as the Q of the circuit is tuned over three discrete values. Figure 4.3b shows the measured frequency response using the circuit conditions applied to the simulation results. The measured results are in good agreement with the simulated results.

Figure 4.3a - Simulated frequency response of Q-tuning

The center frequency of the simulated and measured circuit is at 100 MHz and 101.15 MHz respectively. This minor variation between simulated and measured results can be accounted for by package inductive and capacitive parasitics that are not included in the simulation results.

Figure 4.3b - Measured frequency response of Q-tuning

In both the simulated and measured results, the center frequency goes through a minor shift, as the circuit Q is varied over a very wide range. The shift in center frequency results from changing collector-base junction capacitance as the bias conditions are changed.

Also found in both figures is the change in the midband gain as the Q is tuned. The gain increases with increased Q , and is predicted in Equation 3.6.

The center frequency of the two tank circuits are separated by only 4 MHz due to the high Q of the tank inductors. High separation results in multiple resonant peaks as is seen in the middle curve of Figure 4.4a. Here the simulated frequency response is shown as the center frequency is tuned over three points of operation. The two extremes of the tunable frequency range as well as a point within the operating frequency are selected for performance verification. At each step, the Q of the filter is retuned to provide a maximum value.

Figure 4.4a - Simulated frequency response as center frequency is tuned

Figure 4.4b shows the measured frequency response as the center frequency is tuned over three values in the range of operation. The bias current is adjusted at each step to provide maximum Q.

Figure 4.4b - Measured frequency response as center frequency is tuned.

The simulated and measured results are in good agreement with one another. The relative error is less than 5 percent for the measured and simulated results for both frequency and magnitude. The experimental frequency range of operation is 1 MHz lower than the simulated frequency range of operation. This can be attributed to package inductive and capacitive parasitics, which were not included in the SPICE simulations.

The center frequency at the extremes of the tuning range coincide with the center frequency of the two tank circuits. These values are in good agreement with the designed values using Equations 3.7 and 3.8.

Verification of the underlying theory governing the operation of the integrated stagger tuned circuit was achieved using the discrete version. Both Q tuning and frequency tuning are possible with the proposed architecture.

4.2 Integrated Filters, Layout Considerations

Layout is an extremely important factor that must be given careful consideration for circuits working at 2 GHz. Parasitic capacitance, inductance and resistance of line and pad circuit elements introduce poles and zeros that play a role in shaping the frequency response of the circuit. To reduce these parasitic elements, power and ground grids are constructed using the maximum allowable line width in the process. Differential traces are placed close together to maintain the same common mode for each signal path of the differential signal.

Coupling between adjacent elements causes unintended interaction between circuit elements. To reduce coupling between adjacent elements they are separated by six times the minimum allowable distance. Several ground and power pads are used to reduce the interaction of elements through power lines.

Care is required to ensure that current density and power dissipation limits are not exceeded for elements and interconnecting lines. All transistors are operated well below their maximum power ratings, multiple vias are used for large current interconnects, and resistor types are selected according to the amount of power that they will dissipate.

The inductor is constructed with top metal layer to reduce the parasitics to the ground plane. The outer winding has a length of 225 μm , line widths are 15 μm , and line spacing is 1.5 μm . These dimensions have been optimized and verified through experimental results by Long [Lo93]. The space in the center of the inductor as well as the separation of the inductor from all other elements is five line widths [Lo93]. The space separation inside the inductor is used to reduce coupling, which results in a decreased inductance between lines on opposite sides of the inductor. The separation between the inductor and other elements is set to reduce coupling between the inductor and other circuit elements.

Pads with no ESD protection are used to minimize losses due to pad parasitics. This leads to the need for extreme caution when handling devices. Future iterations should investigate the addition of ESD protection diodes if the filter is fabricated and packaged as

a stand alone device.

The Stagger-Tuned Filter and Varactor-Tuned Filter were developed using the CADENCE-EDGE environment. The total layout areas for the STF and VTF are $1000\text{ }\mu\text{m} \times 1700\text{ }\mu\text{m}$ and $1000\text{ }\mu\text{m} \times 1200\text{ }\mu\text{m}$ respectively, as shown in Figures 4.5a and 4.5b.

The Technology files from the IC layouts were submitted to the Canadian Microelectronics Corporation (CMC), and fabricated in Northern Telecom's (NT) BATMOS five volt process. The available bipolar devices feature high-speed, low-noise and diffused emitters. The process also uses three layers of metallization, and floating poly-poly capacitors. The process has an f_T of 11 GHz, minimum device sizes (1x) have peak f_T at $I_C = 500\text{ }\mu\text{A}$.

Figure 4.5a - Layout of Stagger-Tuned Filter.

Figure 4.5b - Layout of Varactor-Tuned Filter.

4.3 Integrated Stagger-Tuned Circuit, Board Testing

This section presents the test set-up, measurement procedures, experimental and simulation results for the integrated stagger-tuned filter mounted in a C-Quad package. Ideally, the performance of the circuit is measured in terms of the frequency tuning range, Q-enhancement limits, third order intercept point (IP3in), 1 dB compression point, noise figure and power dissipation. However, large variations between the simulated and actual process parameters has disabled the proper operation of this circuit.

4.3.1 Board Layout

The board layout for the STF, mounted in a C-Quad package, is described in this section. The circuit is fabricated by Northern Telecom and supplied by CMC in the form of loose dice and in a bonded C-Quad package. The C-Quad package is an NTE product with low package parasitics. Typical lead inductance and lead-to-lead capacitance is 6.5 nH and 1.5 pF respectively. The chip cavity and chip size result in a nominal bond wire inductance of 2.4 nH.

The test circuit is constructed on FR-4 substrate. An LM78L05 regulator is used to produce a 5 volt regulated dc supply. Biasing for the chip is produced on the test jig through resistors and potentiometers. An SMA-type connector is used to couple signals to and from the 50 Ω test environment. A schematic diagram of the board is shown in Figure 4.6.

Figure 4.6 - Schematic diagram of test board for the integrated STF

Table 4.1, provides a list of pin numbers, names and description.

Pin #	Pin Name	Description
1	V_{fc1}	Frequency Range Switch #1
4	I_{bias_input}	Current Bias for input Differential Pair
7	V_{bias_input}	Voltage Bias for input Differential Pair
9	GND	Ground
10	V^+_{in}	Positive Differential RF input
12	V^-_{in}	Negative Differential RF input

Table 4.1: Pin Number, Name and Description of STF in the C-Quad Package

Pin #	Pin Name	Description
14	GND	Ground
15	V_{f_tuning}	Frequency Tuning Control
17	GND	Ground
18	V_{CC1}	Power Supply
21	$I_{single-double}$	Current Bias for Frequency Tuning Circuit
23	V_{fc2}	Frequency Range Switch #2
25	I_{q_bias}	Q-tuning Control
29	GND	Ground
31	I_{core}	Current Bias for Voltage Bias Circuit
32	GND	Ground
34	I_{output}	Current Bias for Output Amp.
36	V_{out}	Single-Ended RF output pin
37	GND	Ground
39	V_{CC2}	Power Supply
42	V_{fc3}	Frequency Range Switch #3

Table 4.1: Pin Number, Name and Description of STF in the C-Quad Package

A layout of the board is achieved using techniques from the layout of the discrete version, and with the aid of Lussier [Lu93]. The layout is implemented on a 4 layer board with internal ground planes and DC power lines. Figure 4.7 depicts the top layer of the board layout.

Figure 4.7 - Layout of test jig for the integrated STF

4.3.2 Experimental Set-up and Measurement Procedure

This section describes the test set-up for testing the integrated version of the stagger-tuned filter. The filter is packaged in a C-Quad surface mount package, SMA type connectors are used to connect the $50\ \Omega$ impedances of the board to the $50\ \Omega$ test equipment. Two out of the four test boards had shifted mask layers resulting in all vias being shorted to the ground and power planes.

Initial dc testing was performed to verify basic functionality of the chip. These tests have shown that the current mirrors draw the expected current, but the base currents of accessible BJT devices draw up to 1 mA of current. The high base current was observed on three packaged chips on two test boards. Consultations with Nisbet [Ni95] indicate the

circuit should operate correctly, and the only area of concern is the unconventional configuration of the switchable capacitors. The BJT devices used for switching were not modeled in this configuration. Further probing of the test card shows that these devices are not responsible for the uncharacteristic behavior of the BJT devices.

Due to initial problems with the boards, interconnects were suspected of causing the excessive base currents. A dedicated dc test card is constructed to remove suspicions of faulty test cards. This dc test board yields the same information, correct biasing of current mirrors, and high base currents of accessible BJT devices.

To further remove the possibility of improperly packaged parts or ESD compromised parts, one of the loose dice is mounted on an Al_2O_3 (alumina) microwave substrate. Chip bondable resistors and capacitors are used to bias the circuit. The circuit exhibited the same high base currents as the other two test jigs.

The test insert data for the wafers is obtained to track down a possible cause for the excessive base currents. Test insert data represents measured results from 12 wafers at various sites on the wafers. This data shows that all of the parameters of the batch are close to 100% within specification except for the DC gain and the "Fully Sal. Poly1 RCont". These parameters are less than 50% within specifications. The DC gain, β_{dc} , is very high, resulting in BJT devices with lower than nominal base currents.

This finding explains the abnormally high base currents measured on accessible devices. With the reported values of β_{dc} , the current drawn through resistors R16 and R17, from the schematic in Figure 3.1c, is low. This results in a base voltage which is higher in potential than the collector voltage by as much as 1 volt. The base-collector diode becomes forward biased, causing excessive base currents to be drawn. This behavior can be simulated by altering the nominal β_{dc} in the "typical" BATMOS library. This selective variation however does not consider dependant variations of other process parameters which normally occurs in realistic movements of process controls.

4.4 Varactor-Tuned Circuit, Board Testing in PGA Package

This section presents the test set-up, measurement procedures, experimental and simulation results for the varactor-tuned filter (VTF) mounted in a 68-pin Pin Grid Array (PGA) package. The performance of the circuit is measured in terms of the frequency tuning range, Q-enhancement limits, linearity (dynamic range, 3rd order intercept IP3in, 1 dB compression point), noise figure and power dissipation. The measured parameters are compared with the simulated parameters which include all package parasitics.

4.4.1 Board Layout

The board layout for the VTF is described in this section. The circuit is fabricated by Northern Telecom and supplied by CMC in the form of loose dice and in a bonded 68-pin PGA package. The PGA package has significant parasitics that shape the frequency response of the filter, yet proper modeling of the package parasitics in SPICE still allows for accurate predictions, through simulations, of the frequency behavior. Typical lead inductance and lead-to-lead capacitance is 4.5 nH and 1.4 pF respectively. Due to package geometry and material, there is an additional 0.5 pF capacitor to ground on each pin. The chip cavity is much larger than the chip size resulting in bond wire inductance ranging from a nominal value of 6 nH on one side of the chip to 2 nH on the opposite side of the chip. The RF input and output ports are located on the side of the chip with low bond wire inductance. One of the dc power pads, which directly feeds the integrated inductor, is located on the side with high bond wire inductance. This has the effect of adding a series high Q inductor with the integrated spiral inductor. The impact of the bond wire inductance will be discussed in the following sections.

DC biasing for the chip is produced on the test jig through resistors and potentiometers. An SMA connector is used to couple signals to and from the 50 Ω test environment. A schematic diagram of the board is shown in Figure 4.8.

Figure 4.9 shows the layout for the top and bottom layers of the board.

Figure 4.9 - Layout of Top and Bottom layers of test board for PGA package

4.4.2 Experimental Set-up and Measurement Procedure

This section describes the test set-up used to test the integrated version of the varactor-tuned filter. The filter is packaged in a 68-pin PGA package, SMA type connectors are used to connect the $50\ \Omega$ impedances of the board to the $50\ \Omega$ test equipment. An HP 4396A network analyzer is used to determine the frequency tuning range, Q-enhancement limits and the 1 dB compression point. The network analyzer is calibrated using 3.5 mm calibration standards from Hewlett Packard.

The 3rd order intercept is determined using signal generators and a spectrum analyzer. The output from two signal generators, an HP 8656B and an HP 8642A, are summed using an Omni Spectra signal combiner (PN 2090-4011-00). The output from the combiner feeds the test board containing the test chip. The output from the test board is fed into an HP 8566B spectrum analyzer.

The noise figure is determined using the HP 8970B noise figure meter, and the HP 346B noise source.

4.4.3 Simulation and Measurement Results

Simulations, incorporating the extracted netlist and package parasitics, are performed to provide an approximation of the expected measured results. The manufacturer's electrical model for a CPGA pin is used to model the package parasitics. The model is presented below in Figure 4.10.

Figure 4.10 : C-Quad package parasitic components

Components R_1 and R_2 are the resistance of the package leads, L_1 and L_2 are the self inductance of the leads. Capacitor C_1 is the parasitic capacitance to the ground plane. This capacitance is due to the dielectric material of the package [Bi95]. Capacitors $C_{\text{pp}}/2$ are the lead-to-lead capacitance and are modeled as capacitors to ground to reflect the configuration of the bonded package. Bond wire inductance is modeled by L_{BOND} , using a typical value of 20 nH/inch, and taking an average measurement of the bond wire lengths, a value of 6.0 nH on one side of the chip and 2.0 nH on the opposite side of the chip is used.

Figure 4.11a shows the simulated Q-enhancement limits of the circuit. The frequency control voltage is set to 3.58 volts. The current values through the feedback network are 190 μA , 310 μA , and 375 μA for the low, medium and high Q curves. The low Q curve has a value of 26 and the high Q curve has a value of 436. (medium is $Q=58$)

Figure 4.11b shows the measured Q-enhancement limits of the circuit. The frequency control voltage is set to 3.58 volts. The current values through the feedback network are 491 μA , 575 μA , and 665 μA for the low, medium and high Q curves. The low Q curve has a value of 34 and the high Q curve has a value of 400. (medium is $Q=83$)

Figure 4.11a - Simulated results for Q-enhancement

Figure 4.11b - Measured results for Q-enhancement

The measured results are in good agreement with the simulated results. The center frequency for the simulated results in Figure 4.11a is 784 MHz. The center frequency for the measured results in Figure 4.11b is 750 MHz. This gives a 4.3% relative error between simulated and measured results. This discrepancy can be attributed to unmodeled parasitics on the power pad feeding the integrated inductor.

In both figures, as the circuit Q is increased, the frequency decreases by a small amount. In the simulated results, the center frequency is at 794 MHz for the low Q curve and 784 MHz for the high Q curve. This gives a 1.2% shift in center frequency over the Q-enhancement range. In the measured results, the center frequency is 755 MHz for the low Q curve and 750 MHz for the higher Q curve. This gives a 0.7% shift in center frequency over the Q-enhancement range.

The simulated Q enhancement range is from 26 to 436, this range is achievable by tuning the feedback current from 190 μA for the low Q value to 375 μA for the high-Q value. This represents a 185 μA tuning range. The measured Q enhancement range is from 34 to 400, this range is achievable by tuning the feedback current from 491 μA for the low Q value to 665 μA for the high-Q value. This represents a 174 μA tuning range. This tuning range is in good agreement with the simulated tuning range. The feedback current required for the measured data is approximately 300 μA greater than the simulated data. This indicates that the losses in the actual circuit are greater than those predicated in simulations. This extra loss can come from a variety of sources. Thinner metal on the top layer increases the integrated inductor loss. This can not be accounted for in simulations as worst/best case models are not provided. Losses through the bond wire have not been accounted for in simulations, this loss can contribute to overall losses in the measurement results.

The shape of the measured frequency response is also in good agreement with the simulated response. The simulated and measured circuits have a gain of 2 and 3 dB respectively at 600 MHz. The simulated circuit has a higher gain at 900 MHz than the measured circuit. This is due to the higher center frequency of the simulated circuit.

Figure 4.12a shows the simulated frequency response over three settings of the frequency control voltage. The frequency control voltage is set to 0 V, 3.5 V and 5.0 V for the high, medium and lower frequency response curves. The bias current at each frequency increment is adjusted to provide a gain of 40 dB. The bias current is set to 251 μA , 357 μA and 448 μA for the high, medium and lower frequency response curves.

Figure 4.12b shows the measured frequency response over three settings of the frequency control voltage. The frequency control voltage is set to 0 V, 3.5 V and 5.0 V for the high, medium and lower frequency response curves. The bias current at each frequency increment is adjusted to provide a gain of 40 dB. The bias current is set to 591 μA , 617 μA and 706 μA for the high, medium and lower frequency response curves.

Figure 4.12a - Simulated Frequency Tuning Response

Figure 4.12b - Measured Frequency Tuning Response

The measured results are in good agreement with the simulated results. The tuning range for the simulated results in Figure 4.12a is 152 MHz, from 704 MHz to 856 MHz. The tuning range for the measured results in Figure 4.12b is 120 MHz, from 671 MHz to 791 MHz. This gives a 20.5% relative error between simulated and measured results. The lower frequency limits of operation and lower frequency tuning range of the measured results are due to unmodeled parasitics on the dc power pad feeding the integrated inductor.

In both the simulated and measured circuit, as the center frequency of operation is varied, the feedback current is tuned to maintain the same gain. The simulated feedback current is 250.6 μA , 357.1 μA and 448.3 μA for the high, medium and low center frequency responses. The measured feedback current is 590.7 μA , 617.3 μA and 705.8 μA for the high, medium and low center frequency responses. The feedback current is larger in the measured circuit. This is attributed to higher losses which were not accounted for in simulations.

The power dissipation of the circuit is compared to the simulated power dissipation. Both the simulated and measured circuits are set up for a frequency tuning voltage of 5.0 volts and a gain of 40 dB. The simulated and measured power dissipation are 41 mW and 53.3 mW respectively. The difference in power dissipation arises from several sources. The extra feedback current required to compensate for the extra loss in the measured circuit accounts for 1.3 mW. An additional 5 mW is dissipated from the potentiometer which sets the frequency tuning voltage. The remainder of the power is dissipated in the operational amplifier used to buffer the frequency tuning voltage set by the potentiometer.

A comparison of the simulated and measured noise figures is presented in Table 4.2.

Simulations					Measurements				
V_f	I_Q	F_C	Gain	NF	V_f	I_Q	F_C	Gain	NF
volt	μA	MHz	dB	dB	volt	μA	MHz	dB	dB
0	250	856	40.0	4.35	0	590	791	34.1	5.3
2.5	303	816	35.7	4.35	2.5	593	776	35.7	5.3
5.0	448	704	39.9	4.39	5.0	706	672	40.0	4.5

Table 4.2: Simulated and Measured, Gain and Noise Figure of PGA Packaged Filter Over Frequency Tuning Range

The simulated noise figure is 0.95 dB lower than the measured noise figure. One source for the discrepancy is the higher loss in the fabricated circuit. The higher loss is also supported by the difference in feedback current, for the desired gain, in the simulated and measured results. The measured circuit requires a higher feedback, for the same gain, than the simulated circuit. Poor matching on the input and output port of the filter also accounts for the difference in noise figure.

The linearity of the filter is measured to determine its suitability as an RF front end block. Two measures of linearity are the 1 dB compression point and the third order intercept point. The 1 dB compression point is measured for three settings within the frequency tuning range of the filter. A plot of one of the frequency settings is presented in Figure 4.13.

Figure 4.13 - Plot of 1 dB compression point

The horizontal axis shows the input power and the vertical axis shows the output power. Two curves are presented in this plot, the first is the ideal case where the output power keeps increasing with input power. The second curve is the measured case which shows the output compressing with increased input power. The 1 dB compression point occurs when the measured output deviates from the ideal curve by 1 dB. The output 1 dB compression point, for this plot, occurs at -31.0 dBm, the gain of the filter for this setting is 35.3 dB. The average output 1 dB compression point for this filter over the frequency tuning range is -31.5 dBm. The average simulated output 1dB compression point is -25 dBm. The measured results are in good agreement with the simulated results.

The third order intercept point is the power level where the power in the third order products equals the power in the fundamentals. A two tone test is implemented to test for the third order intercept. The tones are closely spaced, within the 3 dB bandwidth of the filter, with equal power levels. The output consists of the two tones, and the third order products. The average input third order intercept point over the frequency tuning range is -51.45 dBm. The simulated third order intercept point is -52.1 dBm. The measured value

is in close agreement with the simulated value.

Both results, the 1 dB compression point and third order intercept, indicate a low linearity. This is due to a lightly designed output section, the current in the output emitter follower is designed below 1 mA. This design decision results from the constraint for low power dissipation. In the intended application, the filter is part of a multichip environment. Thus the filter would not be driving into a 50 Ω load, but rather into a high input impedance mixer, thus the linearity of the filter would be increased.

4.5 Varactor-Tuned Circuit, Board Testing in MSI250

This section presents the test set-up, measurement procedures, experimental and simulation results for the varactor-tuned filter (VTF) mounted in the MSI250 package. The MSI package is a low parasitic package with typical lead inductance and lead to lead capacitance of 1.0 nH and 100 fF respectively. The performance of the circuit is measured in terms of the frequency tuning range, Q-enhancement limits, third order intercept point (IP3in), 1 dB compression point, noise figure and power dissipation. The measured parameters are compared with the simulated parameters which include all package and board parasitics.

4.5.1 Board Layout

The board layout for the VTF is described in this section. The circuit is fabricated by Northern Telecom and supplied by CMC in the form of loose dice. The loose dice are diced up into 125 mil by 75 mil blocks [Le95]. These dimensions fit into the cavity of the MSI250 package. Enough room remains in the MSI cavity to mount additional microwave chip capacitors. These capacitors have a value of 220 pF, and are used to cancel the package parasitics of RF sensitive ports.

Figure 4.14 - Bonding diagram for the MSI250 package

Figure 4.14. shows the layout for the MSI cavity. one chip capacitor is used to ac short one end of the integrated inductor to ground, another is used to ac ground the frequency tuning port and the third is used to ground the dc power supply pins.

DC biasing for the chip is produced on the test jig through resistors and potentiometers. An SMA connector is used to couple signals to and from the $50\ \Omega$ test environment. A schematic diagram of the test jig is shown in Figure 4.15.

Figure 4.15 - Schematic of test jig for the MSI250 mounted VTF

Layout of the test board is accomplished using techniques from all previous layout experiences. This board also employs a split ground plane to isolate the input and output sections. Layout is accomplished using TANGO [AT93], and milled inhouse using the Quick Circuit 7000 [TT94] milling machine. The test circuit is constructed using FR-4 substrate, with a relative dielectric constant of 4.1 [EI95]. Simulations with package parasitics indicate that the filter operates between 1.4 GHz and 1.6 GHz. Board decoupling capacitors, with a self resonant frequency greater than 2 GHz, are chosen to provide a good ac ground.

Figure 4.16 shows the layout for the top and bottom layers of the board.

Figure 4.16 - Layout of top and bottom layers of test board for MSI package

4.5.2 Experimental Set-up and Measurement Procedure

The equipment and techniques used in section 4.4 are employed to measure the MSI250 packaged filter.

4.5.3 Simulation and Measurement Results

Simulations, incorporating the extracted netlist and package parasitics, are performed to provide an approximation to the expected measured results. An electrical model is developed based on other packages with similar materials and dimensions. This model is presented below in Figure 4.17.

Figure 4.17 : MSI250 package parasitic components

Components L and C_{pp} are the self inductance and the lead-to-lead capacitance of the lead respectively. Bond wires at each port of the circuit have various lengths and are modeled using a typical value of 20 nH/inch. These values range from 0.2 nH to 1.5 nH. The chip capacitors seen in Figure 4.15 are also modelled and have a major impact in package parasitic cancellation.

Figure 4.18a shows the simulated Q-enhancement limits of the circuit. The frequency control voltage is set to 4.12 volts. The current values through the feedback network are 617 μA , 710 μA , and 797 μA for the low, medium and high Q curves. The low Q curve has a value of 29 and the high Q curve has a value of 120.

Figure 4.18b shows the measured Q-enhancement limits of the circuit. The frequency control voltage is set to 4.12 volts. The current values through the feedback network are 2.00 mA, 2.17 mA, and 2.36 mA for the low, medium and high Q curves. The low Q curve has a value of 21 and the high Q curve has a value of 80.

PM-1 3½"x4" PHOTOGRAPHIC MICROCOPY TARGET
NBS 1010a ANSI/ISO #2 EQUIVALENT

PRECISIONSM RESOLUTION TARGETS

Figure 4.18a - Simulated results for Q-enhancement

Figure 4.18b - Measured results for Q-enhancement

The measured results are in good agreement with the simulated results. The center frequency for the simulated results in Figure 4.18a is 1.528 GHz. The center frequency for the measured results in Figure 4.18b is 1.503 GHz. This gives a 1.9% relative error between simulated and measured results. This discrepancy can be attributed to mismatches between modeled and actual parasitics as well as shifts in the process from the simulated nominal conditions.

In both figures, as the circuit Q is increased, the frequency decreases by a small amount. This is consistent with results obtained for the PGA packaged filter. In the simulated results, the center frequency is at 1.542 GHz for the low Q curve and 1.528 GHz for the high Q curve. This gives a 0.9% shift in center frequency over the Q -enhancement range. In the measured results, the center frequency is 1.525 GHz for the low Q curve and 1.503 GHz for the higher Q curve. This gives a 1.5% shift in center frequency over the Q -enhancement range.

The simulated Q enhancement range is from 29 to 120, this range is achievable by tuning the feedback current from 617 μA for the low Q value to 797 μA for the high- Q value. This represents a 180 μA tuning range. The measured Q enhancement range is from 21 to 80, this range is achievable by tuning the feedback current from 2.00 mA for the low Q value to 2.36 mA for the high- Q value. This represents a 360 μA tuning range. This tuning range is in good agreement with the simulated tuning range. The feedback current required for the measured data is approximately 1.6 mA greater than the simulated data. This indicates that the losses in the measured data are greater than those predicted in simulations. This finding is consistent with the data obtained from the PGA packaged filter. This further lends argument to greater losses in the actual system than were simulated. These losses can come from a variety of sources. Thinner metal on the top layer increases the integrated inductor loss. Also a lower current gain in the BJT devices will require a greater amount of feedback to achieve the same Q as in simulations. These losses can not be accounted for in simulations as worst/best case models were not provided.

The shape of the measured frequency response is also in good agreement with the simulated response. Both the simulated and measured results start and finish at a gain of -5.0 dB over the shown frequency span.

Figure 4.19a shows the simulated frequency response over three settings of the frequency control voltage. The frequency control voltage is set to 0 V, 4.12 V and 5.0 V for the high, medium and lower frequency response curves. The bias current at each frequency increment is adjusted to provide a gain of 34 dB. The bias current is set to 710 μA , 906 μA and 812 μA for the high, medium and lower frequency response curves.

Figure 4.19b shows the measured frequency response over three settings of the frequency control voltage. The frequency control voltage is set to 0 V, 4.12 V and 5.0 V for the high, medium and lower frequency response curves. The bias current at each frequency increment is adjusted to provide a gain of 34 dB. The bias current is set to 2.258 mA, 2.394 mA and 2.254 mA for the high, medium and lower frequency response curves.

Figure 4.19a - Simulated frequency tuning response

Figure 4.19b - Measured frequency tuning response

The measured results are in good agreement with the simulated results. The tuning range for the simulated results in Figure 4.19a is 210 MHz, from 1.435 GHz to 1.645 GHz. The tuning range for the measured results in Figure 4.19b is 205 MHz, from 1.399 GHz to 1.604 GHz. This gives a 2.4% relative error between simulated and measured results. This error can be attributed to inaccuracies in the parasitic modeling.

In both the simulated and measured results, as the center frequency of operation is varied, the feedback current is tuned to maintain the desired gain. This feedback current is larger in the measured results. This is due to larger losses than were accounted for in simulation.

A comparison of the simulated and measured noise figures is presented in table 4.3.

Simulations					Measurements				
V_I	I_Q	F_C	Gain	NF	V_I	I_Q	F_C	Gain	NF
volt	μA	GHz	dB	dB	volt	mA	GHz	dB	dB
0	710	1.64	34	5.1	0	2.26	1.60	34	5.7
4.12	812	1.53	34	5.1	4.12	2.41	1.50	34	5.7
5.0	906	1.44	34	5.1	5.0	2.55	1.40	34	5.7

Table 4.3: Simulated and Measured, Gain and Noise Figure, of MSI Packaged Filter Over Frequency Tuning Range

The simulated noise figure is 0.6 dB lower than the measured noise figure. One source for the discrepancy is the higher loss in the fabricated circuit. The higher loss is also supported by the difference in feedback current, for the same gain, the simulated results show a lower feedback current than the measured results. Poor matching on the input and output port of the filter also accounts for the difference in noise figure.

The linearity of the filter is measured to determine its suitability as an RF front-end block. Two measures of linearity are the 1 dB compression point and the third order intercept point. The 1dB compression point is measured for three settings within the frequency tuning range of the filter. The average output 1 dB compression point for this filter over the frequency tuning range is -32 dBm. The average simulated output 1 dB compression point is -25 dBm. The measured results are in good agreement with the simulated results.

The third order intercept point is the power level where the power in the third order products equals the power in the fundamentals. A two tone test is implemented to test for the third order intercept. The tones are closely spaced, within the 3 dB bandwidth of the filter, with equal power levels. The output consists of the two tones, and the third order products. The average output third order intercept point over the frequency tuning range is -17 dBm. This is measured at a gain of 30.5 dB. The simulated output third order intercept point for the same gain setting is -21.6 dBm. The measured value is in close agreement with the simulated value.

Both results, the 1 dB compression point and third order intercept, indicate a low linearity. This is due to a lightly designed output section, the current in the output emitter follower is designed below 1 mA. This design decision results from the constraint for low power dissipation. In the intended application, the filter is part of a multichip environment. Thus the filter would not be driving into a 50 Ω load, but rather into a high input impedance mixer, thus the linearity of the filter would be increased.

5.1 Conclusions

The design of a fully-integrated LC-tuned filter was presented in this thesis. It was successfully implemented in a BiCMOS process and achieved operation in the gigahertz range. Reasonable noise figure and low power dissipation has been demonstrated.

Measurements for four different test jigs were performed. The first test jig was a discrete, frequency scaled, version of the stagger tuned filter. This experiment successfully provided feedback to the designer on the developed models, and verified the architecture of the stagger tuned filter.

The second experiment involved the integrated stagger tuned filter packaged in a C-Quad package. Several attempts were made to achieve proper performance of this filter, but further investigations indicated that a major shift in one of the process parameters significantly altered the dc bias condition of the integrated filter rendering it non-operational. This experiment did, however, demonstrate the importance of a complete process and temperature simulation before sending the circuit out for fabrication.

The third experiment involved the integrated varactor tuned circuit packaged in a 68pin CPGA package. The frequency performance of this filter was dominated by package and bondwire parasitics and operated between 500 MHz and 800 MHz with Q-enhancement to several hundred. The noise figure of the device is 5 dB and the power dissipation is 53 mW. The measured data is in excellent agreement with simulated data which includes all of the parasitic elements. This experiment indicates how important it is to simulate with the proper package parasitics. It also shows that expensive packages are unnecessary as long as the package being used has well-modeled parasitics and that these parasitics are included in the simulation results.

The fourth experiment uses information gleaned from the integrated varactor tuned circuit packaged in the 68pin CPGA package. A low parasitic package is chosen, and elements are added to the package to further reduce the parasitics at selected sensitive ports. This filter operated between 1.4 GHz and 1.6 GHz, with Q-enhancement to several hundred. The noise figure of the device operating at this higher frequency is 5.7 dB. These results are in excellent agreement with simulated results.

An integrated inductor and an integrated varactor have been successfully used to implement a frequency tunable filter operating in the 1 - 2 GHz range. Positive feedback has been successfully used to provide Q-enhancement to the filter. This work shows that simulation with all process models and temperature variations is crucial. Further, to accurately predict the frequency response, all package parasitics should be included in the simulations.

5.2 Recommendations for Further Study

The lack of specifications to work towards complicated the design. Initial research into system requirements and system architecture will help to simplify the design task as well as provide focus for the designer.

The stagger-tuned circuit demonstrated a well behaved frequency response in simulations. A recycle of this circuit, eliminating the process dependant biasing, can provide some further insight into high frequency LC-tunable filters.

The varactor-tuned circuit has demonstrated excellent performance, and further study is highly recommended. This circuit is single-ended; a differential circuit using this design approach can eliminate certain dependencies, such as power supply variations and common-mode parasitic effects.

In the event of a redesign special attention should be paid to increasing the linearity. The increase of linearity can be accomplished by increasing the bias current in the output

driver stage and adding emitter degeneration in the positive feedback network. The increased bias current will increase the power consumption of the filter but will not significantly affect the noise figure. This is due to the large gain preceding the output driver. Assuming the filter will be driving a $50\ \Omega$ load, and the redesign is performed in BATMOS, increasing the bias current in the output driver to 8mA will result in a third order intercept of approximately 0dBm. Using a two stage output driver, and approximately 20mA of current will result in a third order intercept of approximately 12dBm. The addition of degeneration resistance in the positive feedback network will degrade the noise figure slightly, and increase the power consumption. The extra power is required to raise the effective g_m of the feedback transistors to the level of the undegenerated case. By adjusting the value of the capacitive voltage divider, an emitter degeneration resistor of less than $50\ \Omega$ will significantly improve the linearity of the circuit while degrading the noise figure by less than 1 dB.

An application of this filter will require frequency tuning to provide channel selection and to account for process variations. A Q-tuning circuit will also be required to compensate for shifts in the process and the dependance of Q on center frequency. Thus to turn this filter into a usable block in a radio architecture, a tuning circuit is required to properly control the circuit-Q and center frequency.

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Appendices

Appendix A

SPICE Parameters for NEC Transistor Array

Parameter	Default	Value	Units
Af	1		--
BF	100	120	--
BR	1		--
CJE	0	1p	Farad
CJC	0	0.5p	Farad
CJS(CCS)	0		Farad
EG	1.11		eV
FC	0.5		--
KF	0		--
IKF(IK)	∞		Amp
IKR	∞		Amp
ITF	0		Amp
Is	1e-16	7e-16	Amp
ISC	0		--
ISE	0		
IRB	∞		Amp
MJC(MC)	0.33	0.3	--
MJE(ME)	0.33	0.25	--
MJS	0		--
NE	1.5		--
NC	2		--

Table C.1: SPICE BJT Parameters μ PA101G

Parameter	Default	Value	Units
NF	1		--
NR	1		--
PTF	0		Degrees
RB	0		Ohms
RBM	RB		Ohms
RC	0	5	Ohms
RE	0	0.7	Ohms
TF	0	14p	sec
TR	0		sec
VA	∞	25	Volts
VB	∞		Volts
VJE	0.75	0.7	Volts
VJC	0.75	0.7	Volts
VJS	0.75		Volts
VTF	∞		Volts
XQJE	1		--
XTI	3		--
XTF	0		--

Table C.1: SPICE BJT Parameters μ PA101G

END

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FIN