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Overcoming the Limitations of Silicon MMICs

by

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for the Degree of

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Abstract

Microwave circuits in silicon were improved by overcoming the three major limitations present in this technology: low quality passives, low levels of isolation due to the conductive silicon substrates, and the relative low speed of transistors in silicon.

Passives were improved by modifying existing post-process fabrication techniques to achieve higher substrate isolation. Transmission lines were implemented with copper and low-k dielectric with improvements of 30% in their useful operating frequency. Even lower attenuation was achieved using silver in place of copper metalization in coplanar waveguides (CPWs), a result shown to be particularly important for phase noise reduction in VCOs. This thesis also presents an optimized CPW with wavelength reduction aimed at improving passive performance by reducing attenuation, implementing larger phase shifts with shorter lines and by using slotted ground planes for increased cross-talk immunity.

An analysis of coupling or cross-talk effects in inductors, resonators and transmission lines is presented. A commercial EM simulator was used for a near-field full-wave solution of coupling effects in silicon substrates. To verify theory, a novel one-step calibration technique aimed at calculating on-chip coupling is presented here. Measurement results are very accurate and agree with EM simulation within 1 dB.

To offset the relative low speed of silicon devices, distributed circuit techniques to increase the achievable bandwidth of silicon based circuits, a study on the gain-bandwidth limitations of silicon based distributed amplifiers is presented. This analysis was previously only available for GaAs technologies with different process constraints. As a demonstration, a 27 GHz distributed amplifier, fabricated in a standard CMOS technology and capable of 40 Gbit/sec transmission is reported. This amplifier shows the highest bandwidth ever achieved in standard CMOS technologies using cascode gain stages. Finally, this thesis will present a novel distributed amplifier gain cell with gain and bandwidth control. A four stage distributed amplifier with gain-bandwidth control was demonstrated using integrated varactors.

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List of Abbreviations and Symbols

OC-768	Fiber optical standard capable of 40 Gbit/s transmission
MMIC	Microwave and Milimeter Wave Integrated Circuits
SOC	System On Chip
CMOS	Complementary Metal Oxide Semiconductor
TSMC	Taiwan Semiconductor Manufacturing Corporation
GaAs	Gallium Arsenide
RF	Radio Frequency
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SiGe	Silicon Germanium
HBT	Heterojunction Bipolar Transistor
BiCMOS	Bipolar and Complementary Metal Oxide Semiconductor
f_T	Transit Frequency
f_{max}	Maximum stable frequency
CPW	Coplanar Waveguide
DA	Distributed Amplifier
InP	Indium Phosphide
V_{BV}	Transistor's Breakdown Voltage
L_G	Transistor's Gate Length
W_G	Transistor's Gate Width
W_{finger}	Transistor's finger width
V_{supply}	Supply Voltage
WCDMA	Wideband Code Division Multiple Access
EDGE	Enhanced Data Rate for Groupe Special Mobile
Q	Quality Factor
MIM	Metal-Insulator-Metal
AMOS	Accumulation Metal Oxide Semiconductor

HA	Hyper-abrupt varactor
Z_0	Characteristic Impedance
α	attenuation constant
β	Phase Propagation Constant
v_p	Phase Velocity
TEM	Transverse Electromagnetic Mode
ρ	Skin Depth
SiO_2	Silicon Oxide
PA	Power Amplifier
VCO	Voltage Controlled Oscillator
HRS	High Resistivity Substrate
PGS	Patterned Ground Shields
f_{SRF}	Self-resonant Frequency
IC	Integrated Circuit
λ	Wavelength
MESFET	Metal Junction Field Effect Transistor
G_f	Forward Gain
G_r	Reverse Gain
F	Noise Factor
f_c	Cut-off Frequency
CVD	Chemical Vapor Deposition
PVD	Physical Vapor Deposition
VNA	Vector Network Analyzer
SOLT	Short Open Load Thru Calibration
GSG	Ground-Signal-Ground
S_{21}	S-parameter Forward Gain
PN	Phase Noise
FDTD	Finite Difference Time Domain EM analysis
LNA	Low-Noise Amplifier
PCB	Printed Circuit Board
MAG	Maximum Available Gain
GBW	Gain Bandwidth Product

Chapter 1

Introduction

Silicon technologies offer the ability to integrate many electronic functions on a single chip, and to provide very inexpensive components in high-volume production. This has lead to the concept of the silicon “System On a Chip (SOC) [1], in which sensing or control functions are monolithically integrated on a single silicon substrate with DSP, memory, computational units, and complete front and back end wireless communication blocks. For the short-range wireless hand-held market, the silicon SOC concept promises systems solutions which are:

- Smaller: Full integration allows for less circuit area.
- Smarter: Compact integrated logic can be used to create more functional circuits.
- More power efficient: On-chip interconnects between circuits reduces power consumption and this translates into smaller size batteries with longer battery life.
- Less expensive: Increased levels of integration reduce system cost in volume production.

To fully realize the potential of the SOC concept, and particularly the monolithic integration of high bandwidth wireless communication devices with other functions on a silicon platform, it will be necessary to develop monolithic microwave IC (MMIC) technology in silicon. The major obstacles to overcome when designing silicon based microwave circuits are:

- Low quality passive circuit implementation in lossy silicon substrates,

- Strong signal coupling between circuit blocks in conductive silicon substrates at high frequencies,
- Low relative speed (f_T and f_{max}) of silicon devices, compared to devices in the most advanced III-V technologies.

For these reasons, many designers are still using GaAs and other III-V based circuits when high performance is required. The use of these high performance III-V devices does not lend itself to SOC design. Their drawbacks include: high integration is not possible, yield may be low and cost of fabrication is high. As a result, when using III-V devices, board level systems are required with increased area, higher power consumption and higher cost of fabrication.

1.1 Silicon based circuits: a Microwave Option?

Heterojunction bipolar transistors (HBTs) with SiGe alloy bases now have performance approaching that of the expensive and exotic InP, GaAs and other III-V technologies. BiCMOS technologies featuring SiGe HBTs integrated with CMOS are now available from several companies. f_T over 200 GHz has been reported for the most advanced SiGe HBTs [2] while InP devices have shown speeds now close to the 300 GHz mark. Although III-V technologies still have a slight performance advantage over silicon, it is clear that in terms of device performance silicon is becoming a contender for MMIC applications at frequencies as high as 20 GHz or even beyond [3, 4]. In fairness to the III-V technologies, it should be noted that high performance in silicon devices is generally obtained through the use of very small feature sizes, which in turn leads to relatively low breakdown voltages (Table 1.1). Many circuit techniques have been developed in silicon devices to overcome this problem including: cascode gain cell and the use of appropriate current limiting resistors in bias cells. Many silicon foundries also provide transistors which are optimized for high-breakdown voltage rather than speed.

While SiGe HBTs provide the highest performance on any silicon-based devices, there has been much interest in the possibility of using pure CMOS for RF and MMICs. There are two motivations of using pure CMOS for this interest. SiGe HBT technologies are generally very expensive. Also, the minimum feature size in SiGe

technology tends to lag one or two generations behind that of pure CMOS, limiting the digital circuit density which can be placed on a SiGe BiCMOS IC. This is an important issue in view of the rapidly increasing complexity of the digital circuitry in many wireless applications. f_T for RF CMOS has increased from approximately 10 GHz for a 0.5 μm process (e.g. IBM5HP) to about 80 GHz for 0.13 μm processes (e.g. IBM8HP) [5]. Many commercial foundries offer an RF CMOS only option as a subset to their BiCMOS processes. In many instances designs are initiated by using both RF CMOS and bipolar devices in a BiCMOS process, but if transistor performance permits, designers can choose not to use bipolar devices, reducing the number of processing steps and reducing fabrication cost.

Despite the growing interest in pure CMOS MMICs, some have argued that the use of CMOS RF and microwave circuits does not necessarily mean a cheaper solution, as the cost of fabrication for a state of the art CMOS RF process is much higher than a bipolar device with similar performance [6].

In fact Table 1.1 shows that SiGe HBTs can deliver the same RF performance as CMOS devices using two generation older lithography (i.e. 0.25 μm minimum feature size versus 0.12 μm). This corresponds to an important economic advantage, since mask costs are increasing exponentially with successive CMOS generations. It is therefore possible that BiCMOS technologies will continue to dominate the SOC market, with SiGe HBTs supplying the microwave components while CMOS devices fill at the baseband and digital sections of the circuit. Clearly it has not yet been resolved whether SiGe BiCMOS or pure CMOS will be the preferred technology for SOC. Most of the contributions reported here are applicable in either technology.

This thesis shows that silicon technologies can compete in the microwave market provided all three major problems silicon circuits exhibit at high frequencies can be overcome: low quality passives, low levels of isolation due to conductive substrate and relative low speed of transistors in this technology. Better passives which use less resistive metals and achieve better microwave performance will be presented. Also, an understanding of EM coupling effects in silicon based circuits and a one-step calibration technique aimed at calculating on-chip coupling is presented here. Contributions are also made to increasing the useful operating frequency of pure CMOS circuits, with the goal of making pure CMOS technologies competitive for ultra-wideband communications [7]. Specifically a distributed amplifier capable of achieving bandwidths

Table 1.1: A comparison of microwave technologies for comparable performance

Device Parameter	InP DHBT	GaAs HBT	SiGe HBT	n-MOS	p-MOS
size	1 μm	2 μm	0.25 μm	0.12 μm	0.12 μm
f_T	160 GHz	70 GHz	70 GHz	80 GHz	38 GHz
f_{MAX}	200 GHz	70 GHz	90 GHz	80 GHz	40 GHz
J_{cft}	1.2 mA/ μm^2	0.8 mA/ μm^2	2 mA/ μm^2	2.6 mA/ μm^2	1.3 mA/ μm^2
I_{cft}	1 ps/V	0.5 ps/V	0.5 ps/V	1.4 ps/V	0.7 ps/V
BV_{CEO}	6 V	>10 V	2.8 V	>1.2 V	>1.2 V
V_{BE}/V_T	0.8 V	1.4 V	0.9 V	0.35 V	-0.35 V

from a few hundred MHz to 5.5 GHz with good noise performance is demonstrated in 0.35 μm CMOS. Also a 27 GHz distributed amplifier (capable of 40 Gbit/sec transmission in OC-768 optical standards ¹) is fabricated in standard CMOS technologies. This amplifier shows the highest achieved bandwidths in standard CMOS technologies using cascode gain stages [8].

1.2 Thesis Objective

This work is directed at understanding and overcoming the three major limitations present in silicon based microwave circuits: poor quality passives, low device isolation and devices with relatively low speeds in silicon technologies.

The advantages of post-process techniques to reduce substrate losses and the use of better metalization (e.g. copper and silver) will be examined in this thesis. Post-process metalization will be aimed at increasing circuit performance of inexpensive digital CMOS processes not optimized for RF applications.

On-chip coupling mechanisms between circuits ("cross-talk") in silicon processes will be studied in this thesis. The measurement of unwanted cross-talk coupling is facilitated by introducing a novel measurement technique which will allow direct measurement and modeling of this effect and to support circuit design.

¹ Provided group delay is not degraded inside useful bandwidth

Overcoming low device speed is important for silicon devices and this thesis will explore the limitations and use of silicon based distributed circuits as a means of compensating for low f_T .

1.3 Thesis contributions

This thesis makes the following contributions to increasing the competitiveness of silicon technologies for implementing MMICs in the frequency range from 2 to 40 GHz:

1. The first application of post-processing techniques (reported previously for spiral inductors in applications near 2 GHz [9]) to produce copper CPWs over thick low-k polyimide for frequencies up to 40 GHz. Copper CPWs are designed and experimentally characterized [10, 11, 12, 13, 14]. Also, the first experimental demonstration that silver metalization provides reduced loss compared to copper metalization in CPWs at frequencies up to 40 GHz is presented [15, 16, 17, 18].
2. Optimization and refinement (in the context of a typical digital CMOS technology) of a previously reported structure providing wavelength reduction in CPWs by inserting a slotted floating metal shield beneath the line [19]. Demonstration that a slotted ground shield can be placed under the structure to reduce cross-talk without significantly increasing attenuation [20].
3. Introduction of a novel technique for the experimental investigation of coupling between microwave circuits sharing the same silicon substrate. Results obtained from this technique used to develop an accurate equivalent circuit model describing coupling [21, 22, 23, 24].
4. Analytical and experimental definition of the gain bandwidth limit of distributed amplifiers in silicon including the effect of passive quality [25]. Previous work was only available for GaAs circuits with different design constraints.
5. Verification of the theory (of the previous four points), by implementation of two novel distributed amplifiers. One achieved one of the highest small signal

gains in silicon [7, 26] while the other made use of CPWs to achieve the highest frequency at which gain is still available in standard CMOS technologies using cascode gain stages [8].

6. Description of new techniques for gain and bandwidth control in fully-integrated distributed amplifiers, verified by simulation. The use of integrated varactors to vary the properties of artificial transmission lines in distributed amplifiers is discussed.

1.4 Thesis Outline

Available silicon based technologies will be reviewed in Chapter 2, as the basis for MMIC circuit design. In this chapter, we will also emphasize the importance of the use of high quality passives in order to minimize circuit losses. Passive structures available in silicon such as spiral inductors, microstrip, coplanar waveguides (CPW) and coplanar striplines (CPS) will be reviewed. The problem of “cross-talk” in a conductive silicon substrates will also be introduced in this chapter. The distributed amplifier will be introduced in this chapter as an MMIC application. Distributed amplification will play an important role in this work, in placing CMOS as a microwave circuit option by taking maximum circuit advantage of the limited f_T of devices implemented in this technology.

Chapter 3 will explore CPWs as the passive of choice for MMIC design in silicon. The concept of post-processing, in which additional processing steps are carried out to increase the performance or functionality of silicon integrated circuit cores fabricated in commercial technologies will be introduced. Here post-processing techniques will be used to add high conductivity copper and silver passives over thick low-k dielectric. The performance of post-processed CPWs will be compared to native CPWs using the basic aluminum metalization over oxide provided by many older technologies. An optimized topology for a CPW with wavelength reduction techniques and better cross-talk immunity will be studied and optimized in this chapter.

The aim in Chapter 4 will be to provide an understanding of coupling (cross-talk) between circuits sharing the same silicon substrate. This is done initially through full EM simulation of typical coupling problems. A calibration free technique to

accurately measure on-chip coupling will be introduced. Results from this experiment will be incorporated into a circuit model to be used in simulation.

Chapter 5 will deal with the theoretical gain and bandwidth limit for silicon based distributed amplifiers(DA). Comparison to measurements will verify theory.

Chapter 6 will build on the gain-bandwidth theory of distributed amplifiers and explore their design and implementation in silicon. Special emphasis will be given to stability, broadband matching and layout optimization. Two designs will be presented, the first one using spiral inductors with 5.5 GHz bandwidth aimed at high gain. The second design uses CPWs to implement required inductances and pushes the frequency of operation to 27 GHz. Novel tuning techniques for gain/bandwidth control in distributed amplifiers using integrated varactors will also be presented in this chapter.

Finally, Chapter 7 will present the conclusions drawn from this work.

Chapter 2

Silicon Integrated Circuit Technology for MMIC Applications

This background chapter will present an overview of the silicon integrated technology roadmap as it applies to monolithic microwave IC fabrication. Active and passive integrated options for this technology will be discussed in this chapter as the basis for circuit design. The problem of isolating different microwave circuit blocks sharing the same silicon substrate will also be discussed. Finally, distributed amplification is introduced here as a circuit technique capable of enabling high frequency operation for silicon based circuits.

2.1 Integrated Active components

We begin this review by looking at the choice of active devices in current commercial silicon processes. Typical technologies now available are summarized in Figure 2.1 [5]. Today many manufacturers offer BiCMOS technologies as a versatile solution to combine the high performance bipolar SiGe HBTs and high density CMOS transistors, on the same silicon chip.

In Figure 2.1 one can see that there are two major technology trends driving transistor high performance evolution, these are: high speed and high power capabilities.

Bipolar SiGe HBTs have shown very impressive speeds compared to more exotic and expensive III-V competitors (GaAs, InP), placing them in direct competition for the high performance microwave market. Figure 2.1 shows improvements in the

f_T of SiGe HBT devices, from 49 GHz in the 0.5 μm generation to about 210 GHz in the 0.13 μm generation [5].

To quantify high power performance, one figure of merit used is the transistor's breakdown voltage (V_{BV}), which is defined as the maximum input open circuit voltage that the HBT can handle before breakdown occurs. This number can be a misleading parameter used to minimize the attractiveness of silicon based devices for high performance. Although state of the art SiGe HBTs have an open circuit breakdown voltage of only 1.8 Volts, it has been shown that with careful circuit design and the choice of appropriate current-limiting resistors in bias circuits, breakdown voltages are between 3.5 and 6.5 Volts for both 0.5 μm and 0.13 μm generations [27].

Figure 2.1: Silicon integrated technology comparison [5]

Another advantage of BiCMOS processes is that, as the technology evolves, offering faster bipolar devices, MOSFET gate lengths shrink, driving up the speed of digital circuits but more importantly reducing the digital area on-chip. Figure 2.1 shows how the minimum lithographic feature has evolved from 0.5 μm for IBM's BiCMOS 5HP to 0.13 μm for the more exotic BiCMOS 8HP processes. Also, as the gate lengths of CMOS devices gets smaller, their supply voltage needs to be scaled

down. The digital supply voltage has been reduced from 3.3 V for 5HP process to 1.2 V for 8HP processes. This reduction is inevitable as short channel and hot carrier effects need to be minimized in the transistor.

As the supply voltage decreases so does the transistor's ability to deliver power. BiCMOS process have been modified to address this problem by incorporating special high-breakdown devices allowing much higher supply voltages. For example, 5HP process offered two choices of bipolar: a device with $f_T = 50$ GHz / $V_{supply} = 3.3$ Volts intended for high speed and a device with $f_T = 27$ GHz / $V_{supply} = 5.5$ Volts for high power applications.

High power devices are increasing in popularity for wireless products, as the demand for high transmission rate multimedia applications increases. An example of this is WCDMA in North America and EDGE in Europe [28]. The implementation of transistors with high power handling capabilities is still an area of on-going research.

2.2 Integrated passive components

In Section 2.1 it was shown that the high frequency performance (f_T and f_{max}) of the most advanced SiGe HBTs and MOSFETs is now at a level once considered the exclusive domain of III-V materials. It might therefore be argued that the main obstacle to the realization of MMICs in silicon is the integration of high-quality inductors and capacitors. The quality factor Q of these passive components is defined fundamentally as follows:

$$Q = \frac{\text{Energy stored per cycle}}{\text{Energy dissipated per cycle}} \quad (2.1)$$

It should be recalled that at microwave frequencies inductors and capacitors can be synthesized by sections of transmission line with short or open-circuit terminations, provided the wavelength of operation is short compared to chip dimensions. For this reason realization of transmission line structures on silicon ICs with low attenuation and short wavelengths is very important. Transmission line structures compatible with silicon technology are reviewed in this section. It is concluded that coplanar waveguide (CPW) lines offer the most versatile approach to realizing transmission lines for silicon MMICs.

2.2.1 Capacitors

Most of today's integrated technologies offer one or more of the three commonly used types of capacitors:

- MOS(polysilicon gated capacitors on single-crystal silicon)
- PIP (polysilicon-insulator-polysilicon)
- MIM (metal-insulator-metal)

The choice of which capacitor to use depends on the circuit application and which capacitors are available in a given process. For example, if high capacitance per unit area is desired, one may choose a MOS capacitor at the expense of poor linearity and increased parasitics. PIP capacitors suffer from high resistance and parasitic capacitance associated with the use of polysilicon plates close to the silicon substrates, so they are suitable for low frequency applications and they also offer very good capacitance/area ratio. PIP parasitic capacitance can be lessened if designed over deep trench isolation. MIM capacitors have somewhat lower capacitance per area but the reduced metal resistance lowers the losses and makes it the choice for high frequency applications due to having the highest Q of all three capacitors described in this section. For a $20\ \mu\text{m} \times 20\ \mu\text{m}$ device, a MIM capacitor yields a typical Q of 90 @ 2.4 GHz, while MOS and PIP capacitors have typical Q values of 20 and 10 respectively.

Actual parameters extracted from commonly used IBM RF technologies can be seen in Table 2.1 [5]

2.2.2 Varactors

Varactors are important in the implementation of some RF circuits where the ability to tune the device is desired [29, 30]. Tunability is important not only to provide circuit functionality, but also to correct for temperature and processing variations. According to Dunn [5], the key figures of merit for varactors are:

1. Tunability (C_{max}/C_{min})
2. CV linearity for high gain variations

Table 2.1: IBM technology comparison for different integrated capacitor types [5]

Capacitor	Parameter	SiGe 5HP/AM/DM	SiGe 5HPE	BiCMOS 6HP	BiCMOS 7HP
MOS	Capacitance at 0 V (fF/ μm^2)	1.5	1.2	3.1	2.5
	Tolerance (%)	10	15	15	15
	T_{CC} (ppm/ $^{\circ}\text{C}$)	48	21	20	-
	V_{CC} (+5/-5V ppm/V)	1740/1740	-900/-450	-7500/-1500	-5480/-1240
Poly-Poly	Capacitance at 0 V (fF/ μm^2)	-	1.6	-	-
	Tolerance (%)	-	25	-	-
	T_{CC} (ppm/ $^{\circ}\text{C}$)	-	31	-	-
	V_{CC} (+5/-5V ppm/V)	-	-3525/-2475	-	-
MIM	Capacitance at 0 V (fF/ μm^2)	0.7	1.35/2.7	0.7/1.4	1.0
	Stacking	Single	Double	Double	Single
	Tolerance (%)	15	15	15	15
	T_{CC} (ppm/ $^{\circ}\text{C}$)	-57	-44	-44	-15
	V_{CC} (+5/-5V ppm/V)	< 25	< 25	< 25	< 25

3. Quality factor Q

4. Tolerance

5. Capacitance density

There are three types of available varactors in silicon processes: the pn diode, the AMOS accumulation mode capacitor, and the Hyper-abrupt varactor (HA). Their performance versus the five key parameters presented above can be seen in Table 2.2.

Table 2.2: Summarized performance for different types of integrated varactors

Varactor	Tunability	CV Linearity	Q factor	Tolerance	Cap. density	Availability
pn diode	good	good	low	low	low	best
AMOS accumulation	good	poor	good	low	good	good
HA	best	best	best	low	low	poor

Although the Hyper-abrupt varactor (HA) offers the best RF performance (Q in excess of 100 at 2 GHz), it introduces an extra mask due to a retrograde implant required to correct its doping profile and also HA varactors may only be available in some specialized silicon processes [5]. The final decision over which varactor to use,

is a trade-off between electrical performance, their availability in a given process as well as fabrication costs.

2.3 Integrated inductors available in Silicon

Of all the passive devices presented in this section, inductors are truly the bottleneck in limiting the achievable quality of microwave circuits implemented in silicon [31, 32, 33, 34, 35, 36, 37, 38]. To understand the effect the inductors have in the overall quality of a tuned tank formed by a capacitor C and inductor L , consider the equation for the unloaded Q of a circuit:

$$\frac{1}{Q_U} = \frac{1}{Q_L} + \frac{1}{Q_C} \quad (2.2)$$

where Q_U represents the unloaded Q of the resonator tank, Q_L represents the inductor Q and Q_C correspond to the Q of the capacitor in a tuned tank. On chip inductors have been limited to Q factors of around 10 for standard silicon processes while typical Q factor values for MIM capacitors are about 50, so it can be seen from (2.2) that inductor losses will dominate the achievable unloaded Q of the tank circuit.

Inductors can be implemented in silicon using either classical spiral structures or, at higher frequencies, by transmission line sections: microstrips, coplanar waveguides, coplanar striplines, etc.

Inductors are characterized with key design parameters given in Table 2.3.

Table 2.3: Summarized performance for different types of integrated inductors

Inductor	attenuation	f_{self}	Inductance/length	Quality Factor
Spiral	high	low	highest	low
Microstrip	low	high	low	high
Coplanar waveguide	low	high	low	highest

Successful passive circuit design will be based on an optimization and understanding of the device's electrical parameters such as [39, 40, 41]:

- Impedance levels

- Attenuation
- Quality values
- Inductor self-resonant frequencies ¹

Next, we present the most commonly available structures used to implement inductances in integrated silicon processes and how they relate to the design parameters listed above.

2.3.1 Spiral integrated inductors

One disadvantage of microstrips is that their use is limited to circuit applications above about 10 GHz, since high levels of inductance are difficult to achieve without consuming large amounts of chip area. To achieve high levels of inductance, designers have relied on the use of spiral inductors. Typically, these inductors have been implemented using a spiral square configuration, but this square configuration results in an increase in the losses due to sharp bends, which increase reflections [31]. To alleviate this problem, the use of octagonal spiral configurations or even circular configurations are becoming increasingly popular as technologies allow for the use of non-orthogonal geometries in their layout rules. Figure 2.2 show a picture of one such fabricated structure.

Figure 2.2: Layout of a planar octagonal inductor

¹Frequency at which the structure's effective reactance becomes zero

Circuit designers would like to incorporate such inductors into their circuit design, and the use of accurate models becomes crucial. It is also desirable to use a physically based model, in which circuit designers could translate lumped elements to actual structure parameters. One such model is the compact model as shown in Figure B.4. L_{ser} and R_{ser} correspond to the series inductance and series metal resistance respectively. C_{ser} and R correspond to the capacitance and resistance of S_i and S_iO_2 layers, and C_{br} is the capacitance between metal turns.

Figure 2.3: Equivalent circuit for a two port planar inductor

An increase in the surface area of spiral inductors leads to more capacitive injection of signals into the substrate and at high frequencies eddy losses will become important. To counter the effect of eddy current losses, designers have relied on the use of ground planes [32], which will be discussed in a later section of this chapter. Because of extra capacitance added by the ground shields, such structures are known to suffer from a reduction in the self resonance frequency and therefore also a reduction in the useful bandwidth of the inductor.

Some design issues that need to be considered when implementing inductors are:

- The use of multiple metal layer in an inductor can be advantageous if properly designed for. While a reduction in the series resistance can be achieved by using multiple metal layers in parallel, the increase in capacitance will decrease the achievable self-resonant frequency of the inductors.

- Using multiple metal layers in series can be advantageous as it increases inductance levels and quality factor of inductors.
- A good inductor design will have to see a balance between series resistance of the metal used and also a minimization in parasitic capacitance.
- While the use of ground planes can increase the achievable Q factor of the inductors it also increases its substrate capacitance, degrading the performance of the inductor at high frequencies. For high frequency designs, it may not be possible to use ground shielded inductors.

2.3.2 Microstrip

A microstrip transmission line can be implemented in silicon by placing a metal track which is isolated from the ground plane (silicon substrate), by using a dielectric material.

Figure 2.4: Simplified microstrip equivalent model

The equivalent circuit is shown in Figure 2.4. L_{ser} represents the series inductance associated with the metal traces, while R_{ser} represents the series resistance associated with the use of metal conductors with finite resistance. G_{sub} represents the conductance of the silicon substrate and is inversely proportional to the loss tangent

of the material used. Finally, C_{diel} is used to represent the capacitance due to the dielectric which separates the metal traces from the substrate.

Based on this compact model, the quality factor for a microstrip can be described by the ratio of stored energy to dissipated energy as follows:

$$Q = \frac{\omega L}{R_{ser}} \quad (2.3)$$

Figure 2.5 shows a number of transmission line options in silicon. In Figure 2.5(a), metal is shown as the ground plane. Although using silicon as the ground plane results in lower per unit capacitance, and hence the capability to produce lines with higher impedance, silicon is lossy. Hence using silicon as the ground plane will result in a more lossy transmission line. For this reason, metal is often used as the ground plane.

A microstrip line is essentially a parallel plate waveguide which supports a TEM wave (See Figure 2.5a) for cross section) [42]. Some of the highlights of these microstrip lines are:

- simplicity in the layout
- Moderate inductance
- Moderate capacitance
- Low loss
- Reasonable field confinement

2.3.3 Coplanar Waveguides

Although microstrip transmission lines are simple structures, they suffer from high metal resistive losses due to the narrow conductor widths required to achieve useful impedance levels [43]. To alleviate this problem, the ground plane of the transmission line can be moved so that it is in the same plane as the signal line (Figure 2.5b). Such a structure is called a coplanar waveguide or CPW.

The top view of a CPW can be seen in Figure 2.6. The characteristic impedance Z_0 depends on the line width and the gap between the conductor and ground [44, 45,

Figure 2.5: Cross section of four transmission line options in microwave process: a) Microstrip structure, b) CPW structure, c) CPW with ground plane and d) Stripline structure

46]. Since both signal and ground planes are parallel to each other, surface losses are of concern. Elevating CPWs from the substrate is a major key to reducing attenuation due to substrate losses. Another advantage of coplanar waveguides is that the number of design variables controlling line parameters such as line impedance increases. This translates into more design flexibility for engineers.

Figure 2.6: Top view of a Coplanar Waveguide structure

When optimizing the characteristic impedance of a CPW, we are confronted with some design tradeoffs. Figure 2.7a shows a coplanar waveguide with a large gap between the signal and ground ports, which correspond to high values of Z_0 . Larger gaps will imply more coupling to the substrate. Figure 2.7b on the other hand shows the case for low impedance values where the gap between the signal and ground ports have been decreased. As seen in Figure 2.7b, the coupling to the substrate has also been decreased.

2.3.4 Coplanar Waveguides with ground plane

A variation of the CPW includes a ground plane implemented in a lower available metal. Such structure can be seen in Figure 2.5c. The use of the ground plane will prevent the $\vec{H}$ fields from penetrating into the substrate, hence losses will be reduced. However, this is at the expense of an increase in overall capacitance seen by the signal line. To a certain extent the capacitance from the signal line to the bottom metal

Figure 2.7: Choice of Z_0 for a CPW a) High Z_0 b) Low Z_0

plane dominates the overall capacitance and will limit the achievable characteristic impedance of these lines.

2.3.5 Coplanar Stripline

We can further isolate the CPW from radiative loss by sandwiching the CPW with a top and bottom ground planes (Fig. 2.5d). Some of the advantages of Coplanar Striplines are:

- Moderate inductance
- High capacitance
- Low loss
- Good field confinement (e.g. “low cross-talk”).

A disadvantage however is that the achievable impedance levels this line can provide are further reduced. Also, they require a process which has at least three available metal layers with low sheet resistance and the top available metal (usually with the lowest resistivity) would be sacrificed in order to implement the top ground plane.

2.3.6 The lossy transmission line model

When analyzing transmission lines, it is traditional to begin by showing ideal equations which neglect losses. The nature of transmission lines implemented in lossy

silicon substrates, suggest that ideal estimates are of little use and instead the analysis of a lossy transmission line is preferred.

Figure 2.8: Lossy transmission line model

Consider the model show in Figure 2.8. In order to analyze this circuit we begin by using Kirchoffs voltage law

$$v(x, t) - R \cdot \Delta x \cdot i(x, t) - L \cdot \Delta x \frac{\partial i(x, t)}{\partial t} - v(x + \Delta x, t) = 0 \quad (2.4)$$

which can be written as

$$-\frac{v(x + \Delta x, t) - v(x, t)}{\Delta x} = R \cdot i(x, t) + L \frac{\partial i(x, t)}{\partial t} \quad (2.5)$$

and then letting $\Delta x \rightarrow 0$ we get

$$-\frac{\partial v(x, t)}{\partial x} = R \cdot i(x, t) + L \frac{\partial i(x, t)}{\partial t} \quad (2.6)$$

Then we have one equation containing R and L. To get another equation relating G and C we need to apply Kirchoff's current law to the circuit to obtain

$$i(x, t) - G \cdot \Delta x \cdot v(x + \Delta x, t) - C \cdot \Delta x \frac{\partial v(x + \Delta x, t)}{\partial t} - i(x + \Delta x, t) = 0 \quad (2.7)$$

and letting $\Delta x \rightarrow 0$ on this equation we also get

$$-\frac{\partial i(x, t)}{\partial x} = G \cdot v(x, t) + C \frac{\partial v(x, t)}{\partial t} \quad (2.8)$$

Equations (2.6) and (2.8) are called the general transmission line equations. For the case where $v(x, t)$ and $i(x, t)$ are both a time-harmonic cosine function:

$$v(x, t) = \Re(V(x) \exp^{j\omega t}) \quad (2.9)$$

$$i(x, t) = \Re(I(x) \exp^{j\omega t}) \quad (2.10)$$

Using Equations (2.9) and (2.10) and substituting into the general transmission line equations (2.6) and (2.8)

$$-\frac{\partial V(x)}{\partial x} = (R + j\omega L)I(x) \quad (2.11)$$

$$-\frac{\partial I(x)}{\partial x} = (G + j\omega C)V(x) \quad (2.12)$$

These equations are called the time-harmonic transmission line equations. and by combining (2.11) and (2.12) we get

$$\frac{\partial^2 V(x)}{\partial x^2} = \gamma^2 V(x) \quad (2.13)$$

$$\frac{\partial^2 I(x)}{\partial x^2} = \gamma^2 I(x) \quad (2.14)$$

where γ corresponds to the complex propagation constant, as follows:

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \quad (2.15)$$

Similarly, the characteristic impedance can be simplified as follows

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (2.16)$$

This lossy yet simplified model applies to transmission lines in silicon where the wave propagates in a purely TEM mode, but as frequency increases the dielectric and metal losses become significant. A better model to account for the losses just described is the so called Quasi-TEM model.

2.3.7 Quasi TEM model

Losses associated with the transmission lines are taken into account more fully in the Quasi TEM model [47, 48, 46]. The name Quasi TEM is used because most of the energy in the transmission line is still contained within the transverse electric and magnetic fields surrounding the line (Figure 2.9). To understand this physical model we need to consider metal and substrate losses at high frequencies (Figure 2.9).

Figure 2.9: Quasi-TEM model for a silicon based transmission line

Metal Losses The transmission line model shown in the previous section include only losses due to the DC resistance of the metal. To find the DC series resistance of a metal we divide the resistivity of the metal (ρ) by its cross sectional area and multiply by the length L [49],

$$R_{ser} = \frac{\rho L}{Wt} \quad (2.17)$$

It becomes clear that increasing the cross sectional area of the conductor decreases its DC resistance, justifying the use of thick metals. Another reason for wanting thicker metals is that current tends to flow not only along the surface of a conductor but it also penetrates into the metal. At higher frequencies however, EM

waves traveling through the conductor will be limited as to how far they can penetrate. Conductors consequently will see further attenuation of the signals passing through if its thickness is less than the skin depth for that conductor at a particular frequency

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \quad (2.18)$$

where f is the frequency and μ is the permeability of the metal. As shown in [49], (2.17) needs to be modified to now include the useful area rather than the total cross-sectional area

$$R = \frac{\rho L}{Wt - (W - 2\delta)(t - 2\delta)} \quad (2.19)$$

Losses due to metal resistance become considerable at high frequencies. Traditionally, silicon base technologies offer a thick top metal layer for use in the implementation of passives. Series resistance due to metal can be approximated by counting the number of squares and using the corresponding metal sheet resistance value. Spiral inductors with multiple turns will severely suffer from this metal loss effect.

Substrate Losses Silicon is neither a conductor nor an insulator. Process engineers rely on doping silicon to control its conductivity. As a practical substrate used in the implementation of integrated inductors, silicon is a lossy conductor.

Semiconductor materials are typically non-magnetic, so the transmission line will be surrounded uniformly by flux and part of it will penetrate the lossy silicon substrate. This magnetic flux which surrounds the transmission line will induce eddy currents in the substrate which will dissipate power and therefore reduce not only the quality factor for the passives implemented but also their self-resonant frequencies by lowering the self-inductance of the inductor.

In a transmission line, the $\vec{E}$ and $\vec{H}$ fields present in the transmission line can penetrate past the dielectric layer (SiO_2) into the silicon substrate further increasing losses. Magnetic fields which penetrate into the lossy silicon substrate induce currents which further increase substrate losses.

Since the dielectric thicknesses are considerable lower in Si than in GaAs processes ($\approx 2 - 10\mu\text{m}$) the line to ground capacitance is increased. An increase in capacitance to the substrate reduces the self-resonant frequency of the inductors realized in silicon substrates and also cause losses as displacement current spreads through the silicon substrate.

2.3.8 Slow-wave effects in transmission lines

Hasegawa *et. al* [47] studied the properties of Si-SiO₂ transmission lines and suggested that propagation speed of a transmission line can be reduced to about an order of magnitude lower than for a TEM mode.

Slow-wave effects are important in silicon since this technique allows the implementation of large phase shifts with much smaller transmission lines reducing both attenuation and layout area. Applications include: phase shifter, antenna arrays, low-loss inductors, etc.

Figure 2.10: Transmission line in a Si-SiO₂ sandwich dielectric

In a Si-SiO₂ transmission line Hasegawa showed the effective dielectric constant, (between signal and ground), as follows (Refer to 2.10)

$$\epsilon_{r, effective} = \frac{d_{ox} + d_{Si}}{d_{ox}} \epsilon_{r, SiO_2} \quad (2.20)$$

where d_{ox} represents the oxide dielectric thickness, d_{Si} represents the silicon substrate thickness and ϵ_{r,SiO_2} correspond to the dielectric constant of silicon oxide. In an ideal transmission line with distributed inductance L' and C' , these values show similar dependence on the dimensions of the transmission line, that is, both L' and C' will increase or decrease by the same percentage. Since the speed of propagation on the line depends on the product of L' and C' , the speed remains constant. In a Si-SiO₂ system such as the one shown in Figure 2.10, L' and C' are no longer constrained to track each other. The Si acts as a conductor for voltage changes between the metal layers, and voltage changes on the top metal layer are followed by charge at the Si-SiO₂ interface up to frequencies as high as a few GHz (depending on the doping level of the silicon). Hence, the effective C' is equal to the oxide capacitance per meter, and depends only on d_{ox} and NOT on d_{Si} . In contrast, the inductance L depends on the distance between the metal layers, and hence on $d_{ox} + d_{Si}$. Due to these different dependencies, L remains roughly the same as for the TEM mode, but C is much higher, especially if $d_{ox} \ll d_{Si}$. In this way $\epsilon_{r-effective}$ can be much higher than that of Si ($\epsilon = 12$) and SiO₂ ($\epsilon = 4$).

Figure 2.11: Modes of propagation in a transmission line as a function of substrate resistivity

Figure 2.11 gives an overview of the three main wave propagation modes in the Si-SiO₂ system as a function of silicon resistivity. At low frequencies, the slow-wave mode occurs. At high frequencies and high resistivity (i.e. low doping), the silicon approximately acts as an insulator, and TEM mode wave propagation occurs. On the other hand, if the doping is high and the silicon has low resistivity, it acts more or less as a conductor. Hence EM fields don't penetrate deeply in the silicon and only a thin *skin* layer carries the main current (skin effect mode wave propagation). In the region in between, for moderate resistivity, the slow-mode occurs up to its highest frequency. Detailed analysis shows that the maximum frequency (the top of the dashed curve) at which the slow wave occurs is approximately given by [47],

$$f_{slow,max} \approx \frac{1}{2\pi\rho_{Si}\rho_0\rho_{SiO_2}} \frac{d_{ox}}{d_{Si}} \quad (2.21)$$

The peak value is achieved at an effective resistivity

$$\rho_{max} = \sqrt{\frac{\mu_0 d_{ox} d_{Si}}{3\varepsilon_0 \varepsilon_{SiO_2}}} \quad (2.22)$$

For typical CMOS technologies, the highly doped Si substrate effectively acts as a conductor. However, a thin oxide layer in combination with lightly doped epi-layer silicon can show the slow-wave effect up to frequencies well in the GHz region.

Other methods are available for slowing down the velocity of propagation on a transmission line [19]. These methods rely on circuit techniques with standard substrate resistivity used in commercial silicon processes. Some design aspects of slow-wave transmission lines as well as new topologies for better cross-talk immunity will be presented in Chapter 3.

2.4 Signal Coupling in Silicon Technology

Signal coupling through the substrate arises in silicon based circuits as a direct result of the low levels of substrate isolation previously discussed in this thesis. As the capacitance to substrate is increased as a result of the low levels of isolation, large amounts of current are injected into the substrate.

Circuit designers would be interested in knowing without the use of full electromagnetic simulation, how much coupling or cross-talk a particular circuit receives from nearby sources. Does orientation matter? Can such effects be included in simulations? On-chip coupling becomes a nightmare for system engineers when trying to integrate multiple components which are adjacent to each other into a single chip.

Due to the an increase in popularity of direct transmitters, the problem of unwanted signal coupling has become very important as many components all employing large inductors and potentially operating at the same frequency are placed next to each other. This effectively becomes a problem of subsystems talking to each other in a poorly controlled environment. One example of this problem is a power amplifier (PA) placed near to a voltage controlled oscillator, low noise amplifier, mixer, etc. Potentially the PA can inject tones into the VCO and cause frequency pulling. A graphical representation of one such system can be seen in Figure 2.12.

2.4.1 Substrate isolation

The lack of substrate isolation has always been a problem in fully integrated processes, and to date, models still cannot accurately predict the extent of cross-talk between circuit blocks. Substrate isolation becomes critical when fully integrated chips with an RF front end, analog and digital circuitry are implemented. Many of the components used in RF circuitry (e.g inductors) will pick up interference from digital circuitry nearby and radiate it away to other components making it difficult for a system engineer to understand and quantify these effects when assembling the entire chip. Many methods have been proposed to achieve substrate isolation and they will be discussed in the next sections.

High resistivity silicon substrates High resistivity silicon substrates (HRS) have been proposed as a method to increase device isolation. It is possible to increase the resistivity of the silicon substrate from its typical value of $10\ \Omega\text{-cm}$ to values which range up to $1000\ \Omega\text{-cm}$ or more by using float refining techniques. Float refining techniques are only available for smaller size wafers. Reduced wafer size and an increase in the cost of fabrication are drawbacks of HRS.

Effectively the use of HRS reduces currents injected into the substrate, minimizing losses and thereby increasing the quality factor of passives at the expense

Figure 2.12: Coupling difficulties with Direct Transmitters

of an increase in the cost of fabrication and an increase in the potential to latch up [50, 51].

The use of ground planes The use of patterned ground shields (PGS) has been previously discussed in the literature [32, 52, 53, 54, 55, 56]. According to Yue [32] some of the advantages of using PGS are:

- Improved substrate isolation which yields Q improvements of up to 25% compared to structures without PGS.
- Inductor behavior which is independent of variations in substrate resistivity and substrate type(e.g. bulk, epi and SOI).
- Simplification in the inductor model for temperature and process variations, which leads to more accuracy in the simulations.
- The area under the inductor could potentially be re-used as the inductor is isolated by using the PGS.

A graphical view of some of the ground planes available in Silicon processes can be seen in Figure 2.13

Figure 2.13: Types of ground planes used in silicon processes: a)no Substrate Ground (NS) b)Halo Ground contact (HG) c)Cross Bar Pattern (CBP) d) Wide Bar Pattern (WBP) e)Narrow Bar Pattern (NBP) f)Perforated Ground plane (PG) g)Solid Ground plane (SG) [32]

A comparison of the achievable Q and self-resonant frequencies (f_{self}) for all types of ground planes presented can be seen in Figure 2.14 [37]

Figure 2.14: Comparison of the Q and f_{self} for various types of ground planes [32]

There are many instances where the PGS is not appropriate to implementing high performance passives in Silicon. The main drawback to PGS is the reduction in the self-resonant frequency of the inductor due to an increase in the signal to ground capacitance. This limitation can severely affect inductor implementation for frequencies higher than 2 GHz. To minimize parasitic capacitance and to break up eddy currents, ground shields have been perforated. However, the work of Chang [57] also found that higher levels of coupling were observed with lines which had WBP and NBP PGS (Figure 2.14), and he also concluded that enhanced slow mode effects and increase self-inductance are among the benefits for such increase in coupling.

The use of a deep trench Many state-of-the-art process technologies have abandoned the use of thick field oxide isolation between devices and have replaced them with a shallow trench. Both shallow and deep trenches are a logical solution to the current size scaling that CMOS is undergoing and they offer an alternative solution over more bulky field oxide isolation techniques used in the past [58, 59]. Deep trenches are also used under capacitors, inductors and transmission lines to reduce capacitance to substrate.

2.4.2 Sources of coupling in Silicon Substrates

Coupling in silicon substrates can be separated according to their source into two main groups (Figure 2.15):

- Electro-magnetic coupling: due to physical overlap in the magnetic fields of adjacent devices which causes an exchange in energy between them thereby producing coupling as a result.
- Capacitive plus conductive coupling: not to be confused with EM coupling, relates to the electrical currents injected from one device to another in silicon wafers and as a result of the low levels of isolation between devices in these substrates (high substrate doping with increased capacitance).

EM coupling will be dependent on factors such as the size of the devices and the proximity between them. Modelling as a near-field problem using EM simulators might be required. Orientation is also important, as magnetic fields can add constructively or destructively depending on the direction of current flow in inductive circuit elements.

The second type of coupling, capacitive and conductive coupling, depends on the substrate resistivity, any guarding techniques used to short substrate injection of currents to ground and the distance between devices.

2.4.3 EM coupling at microwave frequencies: Near Field vs. Far Field?

Table 2.4 shows the dependence of $\vec{E}$ and $\vec{H}$ fields on distance from a dipole (Refer to Figure 2.16).

The field strength of all three basic terms: Radiation, Induction and Electro-static have been plotted as a function of distance away from the wire in Figure 2.16. At the boundary condition where the distance from the wire is equal to $r = \frac{\lambda}{2\pi}$ the inductive and radiative terms are equal. If the distance from the wire is reduced the field strength is dominated by the inductive term and we are said to be in the *near field* region. For the case where the distance away from the wire is greater than this boundary condition, the radiation term dominates and we are in the *far field* region.

Figure 2.15: Sources of coupling in a silicon IC

Table 2.4: $\vec{E}$ and $\vec{H}$ field equations for a single wire

Term	$\vec{E}$	$\vec{H}$	$Power = \vec{E} \times \vec{H}$
Radiation	$\frac{1}{r^2}$	$\frac{1}{r^2}$	$\frac{1}{r^2}$
Induction	$\frac{1}{r^2}$	$\frac{1}{r^2}$	$\frac{1}{r^4}$
Electrostatic	$\frac{1}{r^3}$	-	$\frac{1}{r^3}$

Traditionally, circuit designers tend to think of coupling as a purely radiative phenomena as long as there is enough separation between the wires (Far field), which for a typical process is anywhere from 50 to 100 microns. In many cases, a *far field* region of operation is assumed purely for simplicity during the analysis of this coupling phenomena.

To investigate this assumption, consider a signal frequency of 5 GHz. The wavelength in air is $\lambda_{air} = 6$ cm or about 3 cm in SiO_2 . Again, the boundary condition occurs at approximately $1/6 \lambda$ which implies that for separations less than 0.5 cm in an SiO_2 , near field conditions apply.

For separations between inductors of approximately $r = 100 \mu m$, this is approximately $1/3000 \lambda$. Clearly this falls in the near field regime in silicon ICs.

Chapter 4 will further discuss EM coupling, its modeling and measurement.

Figure 2.16: Field strength of Radiation and Induction terms as a function of distance away from the wire

2.5 MMIC circuit Applications: Distributed Amplifiers

2.5.1 Introduction

Distributed amplification was first formulated by Percival in 1939 [60]. It is based on the principle of equal line delay and if we can absorb the input and output capacitance of the transistor as part of the lumped elements of an “artificial transmission line”, then the frequency response of the amplifier will no longer be dominated by the f_{max} of the device but rather by the cut-off frequency of this artificial transmission line. This principle, ideally, would see the gain of amplifier cells extend past their corresponding transistor f_T values.

The name artificial transmission line is used because the transmission line under question has been formed by physically placing inductance and capacitance components to form a transmission line section rather than placing a microstrip and calculating its electrical length.

The basic schematic for a distributed amplifier can be seen in Figure 2.17, and an “artificial transmission line” is formed when adjacent transistors are connected by using series inductors L_G and L_D shunted by the input and output capacitances of the transistor. The G and D subscripts are used to denote that there are two artificial lines, one at the gate and one at the drain of the device.

For symmetry, distributed amplifiers can be viewed as a 4 port device, two of these ports are matched to the line impedance (dummy terminations) and the remaining two ports serve as the input and output ports during microwave analysis. A signal is launched via the input port located in the “gate artificial line” or gate line and its output signal collected in the output port located in the “drain artificial line” or drain line.

The signal travels along the gate line, with phase velocity, propagation constant, delay, and attenuation corresponding to the gate line properties which have been tailored by the circuit designer. When the signal arrives at the gate of the first FET, some of it will be collected by the gate of the transistor and the rest will continue travelling along the gate line. The FET will provide some gain and delay to the input signal and deliver the amplifier signal to the output drain line at which point half of the signal will go in the forward direction towards the output port and the other half in the reverse direction towards the dummy termination. The signal at the drain line travelling in the forward direction will continue until it reaches the output port. By properly designing gate and drain lines with the same delay, we can ensure that when the signal arrives at the drain of adjacent devices it will be added constructively, so by the time the signal reaches the output port, it has experienced the amplification provided by the four FETs as seen in Figure 2.17.

2.5.2 Literature Review

Distributed amplification has been around since 1939 [60], but it was not until the early 1980’s that researchers began to implement distributed amplifiers in GaAs. One reason for this was the reduction in the gate resistance of MESFETs which enabled the use of transistors. The use of silica substrates and the relative high speed of GaAs devices enabled distributed amplifiers in the gigahertz range to be implemented in early 1980 [61].

By 1987, the first distributed amplifier was implemented using MOSFETs in silicon technologies.

Since the late 1980's there has been an increased interest in distributed amplification with amplifiers reported in [62], which utilizes bondwire inductances and achieve bandwidths of 3 GHz implemented in a standard $0.8\ \mu\text{m}$ CMOS process. Ballwebber [63] and Ahn [64] reported CMOS distributed amplifiers with 5 dB of gain and bandwidths of 5.5 GHz and 8.5 GHz respectively both using a $0.6\ \mu\text{m}$ standard CMOS process. Recently CMOS distributed amplifiers have been demonstrated with 15 dB of gain while achieving 5 GHz of bandwidth in $0.35\ \mu\text{m}$ CMOS process [7]. Two amplifiers with high bandwidth have been shown recently in $0.18\ \mu\text{m}$ CMOS. The first one uses a Darlington configuration to achieve high gain while achieving a 10 GHz bandwidth [65] and the second one uses a common-collector gain configuration to achieve a bandwidth of 22 GHz using spiral inductors[66]. The design of a 27 GHz fully integrated distributed amplifier will be presented in this thesis outlining the highest frequency of operation for a distributed amplifier using a cascode gain cells and implemented in standard CMOS technologies.

2.5.3 Forward available gain of a distributed amplifier

Consider the current generators $I_1, I_2, \dots, I_n$ shown in Figure 2.17. By using superposition:

Figure 2.17: Distributed Amplifier Schematic

$$I_d = \frac{1}{2} \{ I_1 e^{-jn\beta_d} + I_2 e^{-j(n-1)\beta_d} + \dots + I_n e^{-j\beta_d} \} \quad (2.23)$$

The voltage wave travelling down the gate line due to the input signal (E_s), produces voltages $V_1, V_2, \dots, V_n$ at each gate, where $V_1, V_2, \dots, V_n$ are related to V_{in} , where V_{in} is the voltage across the input terminals of the gate line.

$$V_1 = V_{in} e^{-j\beta_g}, V_2 = V_{in} e^{-j2\beta_g}, \dots, V_n = V_{in} e^{-jn\beta_g} \quad (2.24)$$

We also know that currents and voltages are related by

$$I_1 = g_{m1} V_1, I_2 = g_{m2} V_2, \dots, I_n = g_{mn} V_n \quad (2.25)$$

If it is assumed that the line is lossless, then it can be shown that

$$|V_1| = |V_2| = |V_n| = |V_{in}| \quad (2.26)$$

And also since all transistors are equal

$$|I_1| = |I_2| = |I_n| = |I| \quad (2.27)$$

Substituting (2.25), (2.26) and (2.27) into (2.23) and (2.24)

$$\begin{aligned} I_d &= \frac{1}{2} V_{in} g_m \{ e^{-j(n\beta_d + \beta_g)} + e^{-j((n-1)\beta_d + 2\beta_g)} + \dots + e^{-j(\beta_d + n\beta_g)} \} \\ &= \frac{1}{2} V_{in} g_m e^{-j(n\beta_d + \beta_g)} \{ 1 + e^{-j(\beta_g - \beta_d)} + e^{-2j(\beta_g - \beta_d)} + \dots + e^{-(n-1)j(\beta_g - \beta_d)} \} \\ &= \frac{1}{2} V_{in} g_m e^{-j(n\beta_d + \beta_g)} \left\{ \frac{1 - e^{-jn(\beta_g - \beta_d)}}{1 - e^{-j(\beta_g - \beta_d)}} \right\} \end{aligned} \quad (2.28)$$

From Figure 2.17, $V_{in} = \frac{1}{2} E_s$, therefore

$$|I_d| = \frac{1}{4} E_s g_m \left| \frac{\sin \frac{n}{2}(\beta_d - \beta_g)}{\sin \frac{1}{2}(\beta_d - \beta_g)} \right| \quad (2.29)$$

And also recall that power, $P = I^2 R$, therefore the power dissipated in the load $Z_{\pi d}$ is

$$P_{load} = \frac{E_s^2}{16} g_m^2 \left[\frac{\sin \frac{n}{2}(\beta_d - \beta_g)}{\sin \frac{1}{2}(\beta_d - \beta_g)} \right]^2 Z_{\pi d} \quad (2.30)$$

$Z_{\pi d}$ and $Z_{\pi g}$ correspond to the drain and gate load terminations respectively (Figure 2.17). Also, the power available from the generator is $P_{av} = \frac{E_s^2}{4Z_{\pi g}}$, so that the forward available gain G_f becomes

$$G_f = \frac{gm^2 Z_{\pi d} Z_{\pi g}}{4} \left[\frac{\sin \frac{n}{2}(\beta_d - \beta_g)}{\sin \frac{1}{2}(\beta_d - \beta_g)} \right]^2 \quad (2.31)$$

and this expression becomes independent of frequency if $\beta_d = \beta_g$

$$G_f = \frac{n^2 gm^2 Z_{\pi d} Z_{\pi g}}{4} \quad (2.32)$$

2.5.4 Reverse available gain of a distributed amplifier

The reverse current collected at the dummy termination (see Figure 2.17), can be expressed as follows:

$$I_d = \frac{1}{2} \{ I_1 + I_2 e^{-j\beta_d} + \dots + I_n e^{-(n-1)j\beta_d} \} \quad (2.33)$$

Again using the relationships derived in (2.24), (2.24) (2.26) and (2.27), we can write

$$\begin{aligned} I_d &= \frac{1}{2} V_{in} g_m \{ e^{-j\beta_g} + e^{2\beta_g + \beta_d} + \dots + e^{-j(n\beta_g + (n-1)\beta_d)} \} \\ &= \frac{1}{2} V_{in} g_m e^{-j\beta_g} \left\{ \frac{1 - e^{-jn(\beta_g + \beta_d)}}{1 - e^{-j(\beta_g + \beta_d)}} \right\} \end{aligned} \quad (2.34)$$

And again V_{in} is equal to $\frac{1}{2} E_s$ for a matched line, therefore

$$|I_d| = \frac{1}{4} E_s g_m \left| \frac{\sin \frac{n}{2}(\beta_g + \beta_d)}{\sin \frac{1}{2}(\beta_g + \beta_d)} \right| \quad (2.35)$$

also, the power dissipated in the load $Z_{\pi d}$ is

$$P_{dummy} = \frac{E_s^2 g_m^2}{16} \left[\frac{\sin \frac{n}{2}(\beta_g + \beta_d)}{\sin \frac{1}{2}(\beta_g + \beta_d)} \right]^2 Z_{\pi d} \quad (2.36)$$

and the reverse available gain is given by

$$G_r = \frac{gm^2 Z_{\pi d} Z_{\pi g}}{4} \left[\frac{\sin \frac{n}{2}(\beta_g + \beta_d)}{\sin \frac{1}{2}(\beta_g + \beta_d)} \right]^2 \quad (2.37)$$

But for maximum forward gain, β_d equals β_g (which we write as β), then (2.37) becomes

$$G_r = \frac{n^2 gm^2 Z_{\pi d} Z_{\pi g}}{4} \left(\frac{\sin n\beta}{\sin \beta} \right) \quad (2.38)$$

2.5.5 The Noise Figure of a Distributed Amplifier

The noise figure of a distributed amplifier can be estimated as follows [67]

$$F = 1 + \frac{4\gamma}{Ng_m Z_0} + \frac{Z_0 N \omega^2 C_{gs} \delta}{3g_m} \quad (2.39)$$

where γ and δ correspond to the device dependent drain and gate noise coefficients. The second term of (2.39) describes the drain noise which is dominant at high frequencies. The third term describes the frequency dependent gate noise determining the high frequency performance [68]. Typically, values of $2/3 < \gamma < 1$ and $\delta=4/3$ are reported for long channel devices. [62]. In practice γ and δ can be extracted by fitting simulated or measured noise data from a distributed amplifier into (2.39).

2.5.6 Design Issues

Gain Peaking Equation (2.32) implies that if delay equalization of both the drain and gate artificial transmission line is achieved in the distributed amplifier, its gain response is frequency independent. In a practical implementation of a distributed amplifier and due to the frequency dependence of the artificial transmission lines used, there will be gain peaking near the transmission line's cutoff frequency. Gain peaking is undesired as a flat frequency response would be ideal for this amplifier. One solution to this problem is the use of the staggering technique proposed by Sarma

[69] in which the cutoff frequency of both artificial transmission lines is purposely mismatched by an empirical factor. A commonly used method to achieve this offset is to ratio the total capacitance and inductance of the drain line with respect to the gate line. Figure 2.18 shows the gain response of the amplifier as a function of the offset in the cut-off frequency of the drain and gate lines. The nominal gain is approximately 10 dB but for the case where the cut-off frequency of both lines is the same, variations of gain as much as 100% can be observed.

Figure 2.18: Gain peaking in distributed amplification

A commonly used value for the mismatch used in the staggering technique is 0.7 and Figure 2.18 verifies it.

Stability Due to the additive nature of the gain in distributed amplifiers, it is very difficult to achieve high gain. Stability is a concern in amplifiers with high gain and for this reason stability was ignored for years in distributed amplifier analysis. As shown in literature stability can be an issue [70, 71]. As we move toward designs in which the maximum useful frequency of operation gets close to the f_{max} of the gain stage used, stability is of concern. One of the most common sources of instability in a distributed amplifier is the dependence of the gain cell's gate-to-drain capacitance (C_{gd}) to its

drain to source voltage (V_{DS}). If the distributed amplifier becomes unstable, it will oscillate at the frequency shown below [72]

$$f_{osc} = \frac{\pi W}{\sqrt{L_g C_{gs}}} \frac{1}{\sqrt{2(1 + C_{gd}/C_{gs})}} \quad (2.40)$$

As V_{DS} decreases, the gate-to-drain capacitance increases. This lowers the f_{osc} for the gain cell as shown (2.40) causing the f_{osc} of the gain cell to fall inside the usable bandwidth of the amplifier with instability consequences. Since both C_{gs} and C_{gd} are a function of transistor size a trade-off between gain and stability is expected.

Instability can also occur as a result of feedback in a cascode gain cell. To minimize this effect, damping resistors (for example 10Ω) can be placed at the gate of the cascode transistor of the gain cell [66].

Artificial line terminations Each transmission line need to be terminated by its corresponding load impedance. Line termination can be achieved by using a single capacitor or inductor or by the use of half sections where L and C is halved to double its cut-off frequency improving the frequency response of the line terminations.

Figure 2.19: Transmission Line termination a) k half-section b) m-derived half section

The port impedance of commonly used k-half-sections (see Figure 2.19a), begins to degrade at approximately 40 % of the cut-off frequency of the transmission

line (f_c). To alleviate the poor frequency response problem present in k sections, we replace the capacitance in the k-section by a series LC branch. Such structure is called an m-derived section and can be seen in Figure 2.19b. An m-derived section with an empirically determined factor of $m = 0.6$ will increase the useful bandwidth of the line termination to about 85 % of the f_c of the transmission line. The values for the m-derived section L and C components can be determined as follows (with reference to Figure 2.19b),

$$L_1 = \frac{(1 - m) \cdot L}{2} \quad (2.41)$$

$$L_2 = \frac{(1 - m^2) \cdot L}{2m} \quad (2.42)$$

$$C_1 = \frac{(1 - m) \cdot C}{2} \quad (2.43)$$

where L and C correspond to the distributed inductance and capacitance of the equivalent k-section of the transmission line.

Chapter 5 will present a study on the gain-bandwidth product of silicon based distributed amplifiers. Chapter 6 will present two design examples of distributed amplifiers implemented in silicon, one aimed at high gain and the other to try to push the bandwidth as high as possible.

2.6 Summary

In this Chapter, available silicon based technologies have been reviewed, as the basis for MMIC circuit design. The importance of the use of high quality passives to minimize circuit losses have also been emphasized. Passive structures available in silicon such as spiral inductors, microstrip, coplanar waveguide(CPW) and coplanar striplines(CPS) were presented in this Chapter. The problem of “cross-talk” in a conductive silicon substrate was introduced in this chapter. Finally, the distributed amplifier was introduced in this chapter as a circuit application aimed at pushing the frequency of operation of silicon MMICs.

Chapter 3

CPWs with superior performance implemented in Si

In this chapter we examine methods currently used to implement transmission lines with superior performance for silicon MMIC applications. We then demonstrate improvements to transmission line design by reducing metal and substrate losses.

Also this chapter reports how an existing post-processing technique for forming thick copper interconnect [9] was modified and applied to produce CPWs in Si substrates with reduced metal losses and better substrate isolation.

The first use of silver to reduce metal resistance in transmission lines for silicon MMICs is also discussed in this chapter and RF performance of silver CPWs is compared to copper and conventional aluminum CPWs.

Optimization of the geometry of a “slow-wave” CPW structure described earlier in the literature is also reported [19], and it is shown that the addition of a slotted ground plane to this structure can improve performance while increasing resistance to cross-talk.

3.1 Si based passives with improved performance

In order to produce transmission lines with superior electrical performance at high frequencies in silicon technologies, one must deal with high substrate conductivity and high metal resistance. Ideally it would be desired to elevate transmission lines as far away from the substrate as possible and to use low-k dielectrics, in order to minimize electric field penetration from the transmission into the lossy silicon substrates. Similarly, the search for a low-resistance metal option with high reliability

and compatibility with standard fabrication processes continues. An overview of some current methods used to improved transmission line performance in silicon substrates is presented in this section.

3.1.1 Micromachined passives

Bulk and surface micromachining is now a CMOS compatible process, and researchers have investigated the improvements in passive losses through the use of micromachined techniques. The most common micromachining technique in Si is the creation of cavities beneath transmission lines and inductors. When such cavities are filled with air the dielectric constant is $\epsilon_r = 1$. Inductors with 40% improvement in their cut-off frequency have been reported in the literature whenever air cavities were used due to a reduction in the inductor's parasitic capacitance to the substrate [73].

3.1.2 Passives implemented on high-resistivity Si substrates

Typical microelectronic processes use silicon grown by the Czochralsky technique with resistivity in the range of 10 - 20 $\Omega\cdot\text{cm}$. An alternative technique for silicon crystal growth, float-zone refining, can provide resistivities in excess of 1000 $\Omega\cdot\text{cm}$ [74, 75, 76]. Float-zone substrates are relatively expensive and so far not commercially available in diameters larger than 150 mm. Use of smaller diameter wafers increases per unit area processing costs. Also, the need to preserve high substrate resistivity may restrict process thermal budget.

It has also been shown recently, that surface passivation is very important for high resistivity substrates in order to minimize surface losses. Rong [77] showed that, in the context of CPW attenuation, a non-passivated 3000- $\Omega\cdot\text{cm}$ substrate is equivalent to a 70- $\Omega\cdot\text{cm}$ passivated substrate. He also showed that the Q of a 10 nH inductor was increased by 40% to Q=15 at 2 GHz and a CPW experienced a reduction of 6.5 dB in its attenuation at 17 GHz when using passivated HRS.

3.2 Post-process Copper metalization

In this section a post-processing technique aimed at implementing high-performance passives on circuit cores formed in conventional silicon technologies (particularly those

providing only aluminum metalization) is presented. Although some IBM processes such as the 0.5 micron (IBM5HP), 0.25 micron (IBM6HP) and 0.18 micron (IBM7HP) BiCMOS processes have top thick analog metal layers capable of producing high quality passives [5], the cost of fabrication is very high. Most foundry CMOS technologies provide neither thick top metal nor low-k dielectrics. The use of post-processing will therefore enable a circuit designer to use an inexpensive CMOS or BiCMOS technology while still having access to passives with high substrate isolation (low-k dielectric) and less resistive metals such as copper or silver.

Copper metalization offers strong advantages compared to aluminum for passive applications due to its lower resistivity. This metal is attractive for the implementation of CPWs and design in this section focuses on post-processing fabrication of Cu CPWs. Typical CPW dimensions are sufficiently coarse that simple post-processing techniques using contact lithography and lift-off patterning of metalization can be employed. Use of thick, low-k dielectrics also improves CPW performance by minimizing substrate loss and substrate capacitance.

CPW structures compatible with silicon CMOS technology have been reported previously [31], [32], [44], [45], [78], but have generally made use of aluminum metalization over silicon dioxide dielectric. The resultant substrate losses have made microwave design at frequencies above approximately 10 GHz nearly impossible. One solution to this problem is to use a micromachining technique to suspend the CPW in air, but these structures may be fragile and have low yield [73]. This section presents the fabrication and RF characterization of plated copper CPWs on silicon substrates with resistivities suitable for CMOS IC manufacturing. A thick polyimide layer is used to separate the waveguide from the substrate. Control devices using oxide layers for substrate isolation, and using aluminum metalization, were also fabricated and tested. Circuit application of copper/polyimide CPWs and aluminum/oxide controls in a distributed amplifier were also considered. Very little previous work on this topic is found in the literature. Balaraman has described the use of copper metalization in transmission lines on silicon, but in the context of micromachined switches on high resistivity substrates [79].

The test Cu CPW structures were fabricated on 10 Ω -cm silicon substrates. The fabrication sequence was as follows:

- Spin-on and cure of PI2611 polyimide

- Open vias to underlying metal using oxygen plasma etching
- Deposit Ti/Cu/Al seed layer for plating by e-beam evaporation
- Pattern seed layer by lift-off
- Deposit 2 μm of copper by electroless plating

Plating details are given in Appendix A. An early version of the copper process was developed by Rogers [9], who described the use of this process to produce 2.4 GHz VCO circuits incorporating copper inductors with Q-factors of 16. The resistivity of the plated copper was 1.8 Ωcm , close to that of bulk material. The skin depth in copper at 10 GHz is 0.66 μm , justifying the use of 2 μm thick metalization. All lithography steps were completed using a simple optical mask aligner.

Control CPWs were also fabricated using aluminum metalization and silicon dioxide as an intermediate dielectric. 2 μm thick aluminum lines were deposited by e-beam evaporation and patterned with wet etching, while thick oxides were grown by CVD. Details of these structures are summarized in Figure 3.1.

3.2.1 Copper coplanar waveguides for frequencies up to 14 GHz

The CPWs presented here were modelled using a distributed circuit telegrapher's line approach. The basic circuit element is shown in Fig. 3.2. Series resistance R results mainly from the resistance of the metal interconnect, while conductance G results primarily from losses due to field line penetration into the conductive silicon substrate. CPW center electrode width W and slot spacing S were designed using Agilent's Linecalc and Momentum EM simulators. The target line characteristic impedance Z_0 was 50 Ω . Suitable dimensions to achieve this impedance target are given in Table 3.1.

Completed CPW structures were tested using a Cascade Microtech 9000 probe station with Picoprobe 40A-GSG-150-P probes. S-parameters were measured over the range 0.1-14 GHz using an Agilent 8720ES Vector Network Analyzer (VNA). SOLT calibration was carried out with a standard calibration set (CS-5). The influence of the contact pads was subtracted using Y-parameters [80]. From the measured

Figure 3.1: Cross-section of fabricated CPW a) Aluminum Control Samples b) Copper elevated lines

Figure 3.2: Basic element for distributed circuit model of transmission line

Table 3.1: CPW Geometries to give $Z_0 = 50\Omega$

Metal/Dielectric	W (μm)	S (μm)
Copper/polyimide	10	8.5
Aluminum/oxide	10	6.5

S-parameters, the propagation constant and the characteristic impedance are determined from well-known relationships [81]. Transmission line model parameters L, C, R and G were fit to the data using Agilent ADS software [82].

Figure 3.3 shows line attenuation as a function of frequency. Attenuation increases rapidly with frequency for the aluminum/oxide line, illustrating the importance of substrate losses at high frequencies. The advantages of low-resistance copper metalization and line isolation from the substrate using a thick polyimide dielectric are also evident.

Figure 3.4 shows reasonably good agreement between the measured line characteristic impedance and the design target of 50 Ω . For copper/polyimide lines discrepancies between design and measurement result from inaccuracies in the plating process, which does not use a plating guide. For aluminum/oxide lines width erosion in the wet etching process is responsible for the discrepancies.

Figures 3.6 and 3.5 show the line capacitance and inductance per unit length. Capacitance of Al lines compared to Cu lines can be seen in Figure 3.6. It was noted that the copper CPW is less dependent on frequency compared to the aluminum CPW, but this effect has not been investigated. Figure 3.7 shows the effective permittivity, clearly showing the advantages of low-k dielectrics at high frequencies. Low-k dielectrics account for a reduction in the line capacitance to substrate which minimizes electric field penetration creating better isolation of the conductor line from the lossy and conductive silicon substrate. Finally, Figure 3.8 shows the normalized phase velocity for both Al and Cu lines. The use of low-k dielectrics increase the phase velocity of the line reducing dispersion in the transmission line. Comparison to simulated results for Cu in HP Momentum is also presented.

Some disagreements were found between simulated and measured CPWs and these can be attributed to discrepancies in the fabricated geometries of the CPWs, due to the metal deposition method used here (electroplating).

Figure 3.3: Attenuation Results versus frequency

Figure 3.4: Characteristic Impedance

Figure 3.5: Inductance per unit length

Figure 3.6: Capacitance per unit length

Figure 3.7: Effective permittivity as a function of frequency

Figure 3.8: Normalized phase velocity

3.2.2 Copper coplanar waveguides for frequencies up to 40 GHz

A second version of the copper CPWs was fabricated and characterized for frequencies up to 40 GHz and making use of evaporated copper. S-parameters were measured using an Agilent 8722ES VNA. Completed CPW structures were tested using a Cascade Microtech 9000 probe station with Picoprobe 40A-GSG-150-P probes. SOLT calibration was carried out with a standard calibration set (CS-5). The influence of the contact pads was subtracted using Y-parameters [80].

Fig 3.9 shows line attenuation as a function of frequency. Use of cu/polyimide stack reduces attenuation by 5 dB/mm at 40 GHz.

Figure 3.9: Measured Attenuation versus frequency

Fig 3.10 shows good impedance matching to $50\ \Omega$ for the CPWs for frequencies up to 40 GHz. This was achieved by careful circuit design and the use of commercial tools such as LineCalc (a subset tool of Agilent ADS).

Figure 3.11 shows a comparison of the frequency response of the realizable inductance of CPW lines fabricated using both Cu and Al metalization. Cu lines using

Figure 3.10: Measured port matching as a function of frequency

low-k dielectric show self resonant frequencies of approximately 28 GHz compared with 20 GHz for a Al/SiO₂ control structure.

3.2.3 Post-processed copper on a 0.35 μ m CMOS process

CPW structures were also simulated in Ansoft HFSS [83] for the case where the Cu/Polyimide post-process step was added to a pre-existing CMOS technology (e.g. 0.35 μ m CMOS). Figure 3.12a shows good electric field confinement and isolation from the substrate for the case where Cu/Polyimide CPWs were added by post-processing. Good isolation from the lossy silicon substrate is mainly attributed to the reduction in dielectric capacitance in the use of polyimide and increased elevation from the substrate. Figure 3.12b shows the case for standard CMOS Al/SiO₂ CPWs, clearly showing a higher intensity of electric field reaching the silicon substrate.

Figure 3.11: Extracted inductance as a function of frequency for Cu and Al lines

Figure 3.12: E field confinement in a) Cu/polyimide CPWs b) Al/SiO₂ CPWs using HFSS

3.2.4 A circuit example using Cu lines

Distributed amplification has been proposed as a circuit technique that could extend the useful frequency range of CMOS RF ICs. The basic circuit schematic can be seen in Figure 3.13. As introduced in Chapter 2, this method absorbs the FET's input/output capacitance as part of the lumped elements of an "artificial transmission line", formed with the series inductance that interconnects adjacent drain and gates. The FET's gate to source capacitance (C_{gs}), is about four times larger than the drain to source capacitance (C_{ds}), so extra capacitance (C_{add}) will be required at the FET's drain to equalize the delay through the drain and gate lines and ensure the signal is added constructively at the output.

In practice, at high frequencies the inductance required in Figure 3.13 can be realized by CPW sections. Clearly, success of a distributed amplifier design then depends on the availability of high-quality CPWs with accurately modelled characteristics. This was the main motivation for the study of CMOS-compatible CPWs reported in this thesis.

A comparison of the performance of a distributed amplifier in 0.35 μm CMOS technology using aluminum/oxide CPWs versus copper/polyimide CPWs is presented in this section. Microwave optimization of this circuit was carried out in SPECTRE and using TSMC 0.35 μm CMOS models. Amplifier gain S_{21} is plotted vs. frequency in Figure 3.14. The advantage of using copper coplanar waveguides is the much lower attenuation at higher frequencies(Figure 3.14). The amplifier with copper/polyimide CPWs provides a 3 dB gain at 10 GHz, while the aluminum/oxide CPW control device provides no gain above 5 GHz.

Figure 3.13: Distributed Amplifier schematic

Figure 3.14: Simulated distributed amplifier gain response using Aluminum vs. copper lines

3.3 Passive implementation using silver metalization

High quality passives are important in all RF circuits. For example, Voltage Controlled Oscillator (VCO) noise performance depends closely on the quality of the resonant tank which is mainly dominated by the Quality Factor (Q) of the tank inductor [84]. The Q factor of the passive components is defined by attenuation (α) of EM waves in these components $Q \propto \alpha^{-1}$. Generally three mechanisms contribute to EM attenuation: dielectric loss, conductor loss and radiation loss. The lower the quality of the inductors used the more noise the VCO amplifies around its center frequency due to a broadening of its transfer function.

The implementation of CPWs using Ag metalization has been considered in this section for applications where high performance passives are needed to implement circuits with as low phase noise as possible.

3.3.1 Metal Deposition: Electro-plating vs. PVD sputtering

In contrast to the electroless plating used to implement Cu CPWs, a PVD sputtering and evaporation technique was used to implement Ag CPWs. A brief comparison of these deposition methods is presented below:

Electro and electroless plating Some advantages and disadvantages of this deposition method are (Refer to Figure 3.15):

- Advantages: low temperature of deposition and very good efficiency to fill high aspect ratios
- Disadvantages: relative high resistivity of plated metals (5-10%) and excessive roughness of the plated metal surface.

PVD (Sputtering and Evaporation) Some advantages and disadvantages of using PVD Sputtering/Evaporation are (Refer to Figure 3.16):

- Advantages: relative low temperature of deposition, low resistivity of deposited metals and smooth metal surface after deposition.

Figure 3.15: Electroless plating metal deposition used to implement Cu CPWs

- Disadvantages: poor efficiency to fill up high aspect ratio vias

3.3.2 Fabrication Summary of Ag CPWs

Passives were implemented using Ag metalization as follows:

- Initial substrate: 2 inch Si wafers with $\rho = 7.3 \Omega\text{-cm}$
- Metal deposition using E-beam evaporation (basic pressure of 5×10^{-7} Torr)
- Ti Adhesion layer of approximately 30nm of thickness
- CPW Patterning via lift-off
- Thickness of silver $2 \mu\text{m}$

Additional features of this process are that no backside ground metal or post-anneal are required.

Figure 3.16: PVD evaporation used to implement Ag CPWs

3.3.3 Experimental Setup

CPWs were fabricated on quartz wafers with a nominal thickness $h = 300 \mu\text{m}$. $2 \mu\text{m}$ thick copper and silver films were deposited by e-beam evaporation. The metal patterns were defined through a lift-off process. The dimensions of test devices are: the center conductor width $S = 17 \mu\text{m}$, the slot width $W = 13 \mu\text{m}$, and the ground conductor width $W_g = 170 \mu\text{m}$ ($Z_0 = 85\Omega$).

A quartz substrate has been chosen in this work to eliminate the conductive losses of silicon substrates [77]. CPWs on quartz also have less radiation loss at high frequencies [42]. It is possible then to perform a microwave comparison of results based purely on metal losses between Cu and Ag.

S-parameter measurements were performed in a frequency range up to 20 GHz using a standard AC/S test set and SOLT calibration. From the de-embedded S-parameters, the propagation constant γ and the characteristic impedance Z_c were determined [85].

The lumped-element circuit model of a TEM transmission line was previously shown in Figure 3.2. It can be used to model the dielectric quasi-TEM mode of

propagation when the transverse fields carry the majority of electromagnetic energy. R , L , G , C are per unit length quantities, computed from Equations 3.2 [46].

$$\frac{\gamma}{Z_c} \equiv j\omega C + G \quad (3.1)$$

$$\gamma Z_c \equiv j\omega L + R \quad (3.2)$$

3.3.4 Discussion of Results

Fig. 3.17 shows the real part of the extracted Z_c for Cu and Ag devices as a function of frequency. $\Re\{Z_c\}$ for the silver CPW is less than that of the copper one. At 20 GHz this difference can be estimated as 1 Ohm. The difference in $\Re\{Z_c\}$ for Ag and Cu devices is defined by the different values of R and L at moderate frequencies and, at high frequencies, by the different values of L . A wide range of characteristic impedances ($30\Omega \leq Z_c \leq 300\Omega$) is being used in MMICs. Maximizing characteristic impedance is attractive as less current is needed for the same voltage swing.

High Z_c for CPWs could imply more coupling to substrate as shown in Figure 2.7. Reducing the gap between signal and ground is a simple way to reduce the field penetration into the substrate and CPW odd mode coupling to parasitic microstrip and parallel-plate waveguide modes [86].

R_{DC} and R_s define the losses in the metallization and depend on the metal resistivity. $R_s \propto \sqrt{f}$ is due to the frequency dependent current distribution across the conductor (skin effect and proximity effect). The extracted distributed resistance R for silver and copper devices is shown in Fig. 3.18. It is seen that across the measured frequency spectrum, the Ag CPW has less resistance per unit length than the Cu one. At 20 GHz this difference can be estimated as 2-3 Ω -cm.

Fig. 3.19 shows the extracted distributed inductance L for silver and copper devices. Due to magnetic flux penetration, in addition to the external inductance (L_{ext}), the conductors exhibit an internal inductance (L_{int}) which is frequency dependent.

A closed-form expression for the L is $L(f) = L_{ext} + L_{int}(f) = L_{ext} + L_0/\sqrt{f}$ pf. For low frequencies $L(f) = L_{DC}$ [87]. As can be seen in Figure 3.19 the internal

Figure 3.17: Real part of the characteristic impedance Z_C of silver (thin line) and copper CPWs.

Figure 3.18: Distributed resistance R for silver (thin line) and copper CPWs. It clearly shows the skin effect behavior. For Ag the skin depth is $0.45 \mu\text{m}$ at 20 GHz.

inductance for the Ag CPW is less than for the Cu CPW. At 20 GHz this difference could be estimated as 10^{-10} H/cm.

Fig. 3.20 shows the distributed capacitance C for silver and copper CPWs. Because of their equal dimensions, Ag and Cu devices display the same value of C across the measured frequency spectrum.

3.3.5 Circuit Applications using Ag metalization

One of the critical building blocks of a microwave transceiver is the voltage-controlled oscillator (VCO). Resonant tanks with Q as high as possible are desirable to reduce VCO phase noise. The phase noise PN is proportional to Q^{-2} [84]. Phase noise in a VCO is a design parameter which is particularly likely to benefit from the small improvement in high frequency resistance for silver (as opposed to copper) CPWs. This contention is investigated here using circuit simulation in Agilent ADS by using TSMC 0.18 μm CMOS models and also using co-simulation with Agilent Momentum, [88] for passive EM simulation.

The resistivities for the metal considered in this work can be seen in Table 3.2

Table 3.2: Resistivity for metals considered in this work

	Silver	Copper	Aluminum
Resistivity	$1.59 \mu\Omega\text{-cm}$	$1.68 \mu\Omega\text{-cm}$	$2.65 \mu\Omega\text{-cm}$

The phase noise of the VCO can be approximated using Leeson's empirical formula [84] as follows:

$$PN = \left[\frac{\omega_0}{(2Q\Delta\omega)} \right]^2 \left(\frac{FkT}{2P_S} \right) \quad (3.3)$$

where

- ω_0 corresponds to the center frequency in rads/sec
- Q is the quality of the resonant tank dominated by the inductor Q .
- $\Delta\omega$ correspond to the offset frequency away from the carrier

Figure 3.19: Distributed inductance L for silver (thin line) and copper CPWs

Figure 3.20: Fig. 5. Distributed capacitance C for silver (thin line) and copper CPWs. The variation of C could be explained by the fact that the effective dielectric constant of quartz is a frequency dependent parameter.

- FkT and P_S correspond to the noise density and VCO power respectively

Based on Equation 3.3, it can be seen that $PN \propto Q^{-2}$ and also we know that $Q \propto \alpha^{-1}$. Figure 3.18 shows that at a frequency of 20 GHz there is an improvement in the series resistance of the line of approximately 3 Ω/cm . Recall that the quality factor of an inductor can be estimated as

$$Q = \frac{\omega L}{R_s} \quad (3.4)$$

where L and R_s correspond to the series inductance and resistance respectively. From Figure 3.17 and Figure 3.18, the following data was collected at 20 GHz

Table 3.3: R_s , L and Q extracted from Figures 3.17 and 3.18

Metal	R_s	L	Q
Ag	17 Ω/cm	4 nH/cm	29.56
Cu	20 Ω/cm	4.15 nH/cm	26.07

Based on the previous assumptions

$$\begin{aligned}
 PN_1 &= \frac{k}{Q_1^2} \\
 PN_2 &= \frac{k}{Q_2^2} \\
 \frac{PN_1}{PN_2} &= \left(\frac{Q_1}{Q_2} \right)^2 = \left(\frac{29}{26} \right)^2 \\
 \frac{PN_1}{PN_2} &= 1.2440
 \end{aligned}$$

This translates into a Phase Noise improvement of $10 \cdot \log(1.2440) \approx 1.04$ dBc/Hz.

To verify this simplistic calculations we simulated two inductors with similar dimensions using Cu and Ag metalization in Agilent Momentum [88]. Accurate modeling of these inductors will be discussed in the next chapter of this thesis, but for the purpose of showing the advantages of Ag over Cu metalization a 5 GHz VCO was designed. Phase noise response of this VCO at 5 GHz is shown below in Figure 3.21.

Figure 3.21: Phase noise of a 5 GHz VCO using Cu and Ag inductors

It can be seen that when using Cu metalization the VCOs phase noise is -123 dBc/Hz at 1 Mhz offset. In comparison when using Ag metalization the phase noise drops to -126 dBc/Hz at the same offset, a 3 dB simulated phase noise difference.

In summary, silver CPW offers series resistance advantages of approximately 3 Ω/cm (Figs 3.17 and 3.18) compared to copper and this translates in quality factors with 14% improvement at $f = 20$ GHz. Following Leeson's approximation for the phase noise of a VCO [84], the corresponding improvement in Q of silver CPW over copper controls translates into an expected 1 dBc/Hz improvement in the phase noise for the VCO (simulated improvement was 3 dB at 1 MHz offset).

3.4 CPW Wavelength reduction technique with better cross-talk immunity

At high frequencies the synthesis of inductors and capacitors in silicon ICs using transmission line sections becomes attractive. Implementation of transmission lines in silicon can be done in reference to the basic equations for characteristic impedance Z_0 and phase velocity v_p in a lossless line:

$$Z_0 = \sqrt{\frac{L}{C}} \quad (3.5)$$

$$v_p = \frac{1}{\sqrt{LC}} \quad (3.6)$$

Thin film microstrip lines implemented in silicon tend to have high C and small L , leading to low values of Z_0 unless the strip conductor is made very narrow. However, a narrow strip will give high resistive losses. CPWs allow more flexibility in setting Z_0 , since L increases and C decreases as the gap increases.

To minimize resistive loss in a CPW, it is desirable to make the center conductor wide. This increases parasitic capacitance to the substrate. Current flowing in the substrate as the parasitic capacitance charges and discharges over the RF cycle leads to losses. When inductors and capacitors are synthesized using transmission line sections, it is desirable to keep the sections as short as possible to minimize resistance. This in turn suggests that the wavelength on the line should be as short as possible, which can be achieved by making L and C large to give a small phase velocity (hence the term slow wave CPW).

In a conventional CPW structure, L can be increased by increasing the gap between the conductors to increase the flux linking the circuit, but this will decrease C and raise the line impedance. C could be increased by increasing the metal thickness, but there are severe technological limits to this approach. Long *et al* proposed a modified CPW structure which could realize slow wave behavior without using excessively thick metal. In this new structure an electrically floating metal electrode is placed beneath the conventional CPW. The floating electrode provides increased capacitance through a folded dielectric effect even when the gap between the top

conductors is wide [19]. Losses due to eddy currents in the floating electrode are minimized by slotting the electrode in a pattern resembling railway ties.

Long *et al* [19] demonstrated the advantages of the new CPW structure, but did not investigate optimization of the geometry. Optimization is considered here. The consequences of adding a ground shield beneath the floating electrode in the lowest available metal to minimize field line penetration into the substrate are also considered.

3.4.1 Process of slowing down wave propagation in a CPW

The process of slowing down wave propagation in a CPW is available in the literature [19]. This process can be visualized in Figure 3.22, and can also be summarized as follows:

1. Widening the gap in the CPW: as a result, impedance levels increase due to the reduction in capacitance. The effective inductance increases as the magnetic flux linking the conductor increases, also electric fields are free to penetrate the substrate increasing losses in the CPW.
2. Adding a floating metal shield: a floating metal shield stops electric fields from penetrating the substrate and creates a folded dielectric effect (Refer to Figure 3.22). Impedance levels are still high.
3. Widening signal line: to bring the impedance levels to their original value we widen the conductor line, increasing capacitance and also decreasing line attenuation.

Since both the CPW's effective inductance and capacitance have been increased while still retaining its characteristic impedance, the phase velocity has been decreased as shown in (3.6).

3.4.2 Technology description

Optimization of the slow wave CPW structure in a typical mixed-signal CMOS technology with six layers of copper metalization is considered here. A cross-section through the metal stack is shown in Figure 3.23.

Figure 3.22: Slow Wave process in a CPW [19]

Figure 3.23: CMOS technology with all Cu metal layers

The inadequate thickness of the top analog layers combined with the insufficient levels of dielectric thickness for this process can be expected to give poor quality factors. Slow wave techniques for the implementation of on-chip CPW can be used to advantage here as they can keep attenuation levels low while preserving useful impedance levels (e.g. 50 Ω).

3.4.3 Design and Simulation of proposed Slow Wave CPWs

A cross section of the proposed structure is presented in Figure 3.24, with all corresponding dimensions shown below (Table 3.4):

Figure 3.24: CPW with floating metal and ground plane. Only three metals layers shown: GSG top plane in top metal, floating metal tracks in top metal -1 and ground plane in bottom metal.

Other parameters investigated in this work include the following:

- Overhang Ratio: defined as $\frac{O}{W+2S}$
- Duty Cycle: $\frac{W_T}{W_T+S_T}$

Table 3.4: Slow wave design parameters

Parameter	Description
W	CPW conductor width
S	CPW Ground to conductor Spacing
t_1	CPW metal thickness
t_2	Floating metal track thickness
t_3	Ground plane metal thickness
O	Floating metal track overhang
W_T	Floating metal track width
S_T	Separation of floating metal tracks
H_1	dielectric height 1 (CPW floating track)
H_2	dielectric height 2 (Floating Track gnd)

Figure 3.25: Simulation Setup in Agilent Momentum version 2003A. P_1 and P_2 were defined as internal ports while all other ports were grounds references.

A top view of the simulation setup is shown in Figure 3.25. Electrical Performance parameters for this CPW include: its characteristic impedance Z_0 , attenuation α , effective dielectric ϵ_r , quality factor Q , cut-off frequency f_c . Electrical parameters were investigated versus frequency, floating metal track separation S_T , duty cycle and overhang ratio.

Figure 3.26 shows Z_0 as a function of buried metal track's separation S_T and duty cycle. As expected, decreasing the buried metal track's separation S_T decreases

the capacitance under the conductor line in the CPW increasing its characteristic impedance. Recall from Section 3.4.1 that one of the steps used to slow down the wave in the CPW was to separate ground ports from the center conductor. For buried metal track separations, S_T , larger than $5\mu\text{m}$, these no longer have a dominant effect on the Z_0 of the line. Figure 3.26 also shows that for S_T smaller than $2.5\mu\text{m}$, decreasing the duty cycle reduces the capacitance under the CPW's center conductor, also controlling the Z_0 of the line.

Figure 3.26: Z_0 as a function of slot separation for slow-wave CPW, with duty cycle as a parameter

Figure 3.27 shows Q as a function of slot separation S_T and duty cycle for the slow-wave CPW. Decreasing the buried metal track's separation S_T increases the Q factor of the CPW. This effect is expected for a decrease in S_T , (recall that to maintain the same impedance levels we can make the lines wider or separate the ground plane further away from the center conductor). Decreasing the duty cycle from 0.5 to 0.25 decreases the achievable Q factor of the CPW due to resonant effects and also due to increased eddy currents and losses as the metal track width W_T is increased.

Figure 3.28 shows f_{self} as a function of buried metal track's separation S_T and duty cycle for inductors implemented using these slow-wave CPW. For transmission lines with fixed length used to realize inductances using slow-wave CPWs

they will experience self-resonant frequencies f_{self} or the frequency at which the effective inductance goes to zero. For decreased phase velocity in the CPW, the fixed length inductors implemented using these CPW are expected to see a reduction in the self-resonant frequency f_{self} as seen in Figure 3.28.

Table 3.5: Optimized Slow Wave CPW Parameters (With reference to Figure 3.24)

CPW Parameter	Units	Cheung <i>et. al</i> [19]	This Work
W	μm	16	20
S	μm	20	24
t_1	μm	2.3	2
t_2	μm	1.0	1
W_T	μm	1.6	1
S_T	μm	1.6	1
H_1	μm	4.0	2
H_2	μm	6.0	6
Overhang Ratio	-	8.5	1.5
Duty Cycle	-	0.5	0.5

An optimized version of a CPW with wavelength reduction has been shown in Table 3.5 and final geometries were based on the following design considerations (with reference to Figure 3.24):

- The use of thicker conductive metal lines will allow for CPW geometries to be smaller while still achieving good attenuation levels. Losses will be lower at high frequencies. By the same argument copper metallization is preferred over aluminum due to a 30% reduction in metal resistivity.
- Railroad tie thickness and separation have been optimized. To have noticeable and useful wavelength reduction in the CPW, the parameter S_T must be less than $2.5 \mu\text{m}$.
- The use of larger spacing S_T implies limited wavelength reduction. ϵ_r is reduced as well as the conductor to ground capacitance. If the buried metal width W_T is increased, total capacitance under the CPW signal line increases, also increasing the ϵ_r and leading to a reduction of the line's cut-off frequency (f_c) of the achievable inductances which could be implemented from this CPW.

Figure 3.27: Q as a function of slot separation and duty cycle for slow-wave CPW

Figure 3.28: Inductor self-resonant frequency f_{self} as a function of Slot separation and duty cycle for slow-wave CPW

- Duty Cycle of 0.5 gives more linear response of SRF vs. railroad track separation S_T . As the Duty cycle is decreased to 0.25 resonance effect are noticeable (see Figure 3.28).
- Keeping overhang ratios to values less than 1/5 was needed to achieve the lowest possible attenuation. For the case where larger overhang ratios were used, the total capacitance of the CPW was so large that the folded dielectric effect was no longer dominant and impedance levels dropped. To compensate for the low impedance levels. The CPW signal conductor needed to be made narrower increasing line attenuation.

3.4.4 Folded dielectric effect in CPW

Simulation of CPW performance was carried out using a full three dimensional FEM electromagnetic field simulator (Initial simulation using Agilent's Momentum, further simulations with Ansoft HFSS). Refer to Figure 3.29 a) and b).

Figure 3.29 c) shows the electric field distribution under a simple CPW with no buried metal tracks under its GSG plane. As expected electric field lines from the conductor signal line are terminated at the ground lines located on either side. In contrast, Figure 3.29 d) verifies our previous assumptions in Section 3.4.1 and shows how the electric fields no longer have the same distribution as in a simple CPW. A CPW with floating metal under its GSG plane has a folded dielectric where E-field lines go from the signal line to the floating metal and then from the floating metal back up to the ground plane.

By increasing the electric field under the CPW we have kept the effective inductance constant while increasing the effective capacitance of the CPW, visible by simple inspection of the increase in the effective dielectric under the CPW.

HFSS simulations were carried out for a standard CPW and three variations of a CPW slow wave structure: a) a simple cpw structure b) an optimized version of [19], c) a new slow wave structure with slotted bottom ground plane and better noise immunity and d) the same structure as in c) but with a solid ground plane. Results are shown in Figures 3.30, 3.31, 3.32 and 3.33. Results were extracted from s-parameter data [78]. The physical length of all transmission lines studied was 250 μm . Figure 3.30 shows impedance levels of $Z_0 = 50\Omega$ for all four structures studied.

Figure 3.29: a) Simple CPW structure in HFSS b) Cross section of slow wave CPW structure in Asoft HFSS c) Electric field for a cross section of a simple CPW d) Electric field for a cross section of a Slow Wave CPW showing folded dielectric effect.

Figure 3.31 shows how inductance levels were not altered by the addition of floating metal tracks in structures b) and c), L_{eff} is greatly reduced, however, when a solid ground plane is used d), due to the increase in capacitance. Figure 3.32 shows much better Q factor for CPW slow wave structures b) and c) when compared to a simple CPW structure a). In the same figure for case d) due to the solid ground plane used, substrate current flowing into the bottom plate of the capacitor causes losses at high frequencies and degrading the quality factor of the CPW. Finally in Figure 3.33 attenuation is plotted vs. frequency. For structures b) and c) the attenuation was 0.25 dB for a 250 μm line at 40 GHz, while simple CPW structure a) show about 0.3 dB higher attenuation at 40 GHz while structure d) shows about 1 dB higher attenuation at 40 GHz.

The addition of floating metal tracks to CPW's implemented in silicon for cases b) and c), has been shown to increase the quality factor of these lines when

compared to standard CPW with the same impedance levels. Structures presented in [19] were further optimized in b) and a new structure with slotted metal ground plane presented in c) without degrading electrical performance but with better cross-talk immunity.

Figure 3.30: Z_0 vs. frequency for all structures investigated

Figure 3.31: L_{eff} vs. frequency for all structures investigated

Figure 3.32: Q vs. frequency for all structures investigated

Figure 3.33: Attenuations S_{21} vs. frequency for all structures investigated

3.5 Summary

In this chapter we have presented an alternative method to produce high quality CPWs, which relies on the use of a Cu based post process step utilizing low-k dielectrics. The use of plated copper metalization over thick polyimide dielectric has been found to significantly improve the performance of coplanar waveguide transmission lines fabricated on CMOS-compatible silicon substrates. Compared to control aluminum/oxide CPWs, copper/polyimide devices provide 6 dB less attenuation at 10 GHz. Extraction of the telegraphers line model parameter revealed that this improvement results largely from separation of the line from the lossy silicon substrate by the thick low-k polyimide, with some contribution from the reduced series resistance of the copper. Momentum simulations are in agreement with measurements. The application of copper/polyimide CPWs in a distributed amplifier in $0.35\ \mu\text{m}$ CMOS was presented. These amplifiers were predicted to provide a gain of 3 dB at 10 GHz, while control amplifiers using aluminum/oxide CPWs in the native top metal of the technology could not provide gain at frequencies higher than 5.5 GHz. The copper/polyimide coplanar waveguide appears to have great potential to extend the

application of CMOS ICs to higher microwave frequencies. A second version of this CPWs was fabricated and characterized for frequencies up to 40 GHz. Cu lines using low-k dielectric show an improvement in the cut-off frequency (f_c) of the inductance by about 30%.

The use of silver metalization to fabricate high-quality passives was also considered. Structures were fabricated in-house and electrical performance compared to copper CPWs for frequencies up to 20 GHz. Improvements in the CPW series resistance of up to 3 Ω -cm were observed. VCO inductors implemented using Ag metalization should experience 1 dB improvements in their phase noise when compared to copper (Simulated improvement was 3 dB).

Finally, an investigation of slow wave effects in CPW was presented in this chapter. Although slow-wave CPWs have been reported previously in the literature [19], the optimization for this structures was lacking and also a new structure with increased cross-talk immunity was presented in this work.

Chapter 4

EM Coupling in Si Substrates

4.1 Introduction

In previous chapters, passive components such as transmission line and inductors and distributed amplifiers making use of transmission lines and inductors were studied. However, any time such passive structures are used there is the potential for coupling between such components. Such interactions will be studied in this chapter.

The problem of signal coupling or cross-talk between circuits in silicon is very complex. Although the literature reports attempts to understand this problem, many questions are still unanswered. For example, an IC designer would be interested on how coupling affects other design variables such as impedance levels, quality factors, etc, such that these effects are included into circuit and system simulation.

This chapter will attempt to answer some of these questions by carrying out a study of EM coupling in silicon substrates. Simplistic circuit models for coupling will be replaced by more accurate EM models using Agilent's Momentum [88] and Sonnet simulators [89]. Structures investigated include inductors, resonators and transmission lines (e.g. CPWs).

Finally in this chapter, a new technique for measuring on-chip coupling will be presented. This technique is unique in that no off-chip calibration is required, the experiment is fast, accurate and is able to detect very low levels of coupling with high sensitivity.

4.1.1 Simple coupling model investigation

An ideal semiconductor process used to implement transmission lines should have a thick dielectric layer separating the signal metal layers from the underlying ground plane. An increase in the dielectric thickness will have the effect of reducing the shunt capacitance and therefore providing more isolation from the substrate. A simple coupled inductor model (Figure 4.1a)), is used as a first assessment of coupling between inductors. Frequency is plotted using a logarithmic axis to better observe the linear region of coupling at low frequencies (Figure 4.1).

Coupling is defined as the voltage transfer function between port 1 and port 2 in Figure 4.1(a). Varying inductance levels will affect the amount of coupling between adjacent structures. Figure 4.1(b) shows coupling as a function of the inductance of each adjacent device. Both adjacent inductors were assumed to have the same dimensions.

Mutual inductance ($M = K_m \cdot L$ in Figure 4.1(a)) is a measure of the overlap in the magnetic fields of devices which interact with one another. Mutual inductance is affected by the size of the inductors, the separation between inductors and also their orientation. Figure 4.1(c) shows the relationship between coupling and the mutual inductance of adjacent devices.

The dielectric capacitance (C_p in Figure 4.1(a)) was also investigated for the simple model shown in Figure 4.1a). Results are shown in Figure 4.1d). As frequency increases, the amount of coupling decreases due to the frequency dependence of the dielectric capacitance decreasing coupling as the port is shunted to ground at high frequencies [90].

$$|S_{21}|_{\omega \rightarrow 0} \approx \frac{2M}{Z_0} \cdot \omega \quad (4.1)$$

$$|S_{21}|_{\omega \rightarrow \infty} \approx \frac{2M}{Z_0} \left(\frac{1}{LC_p} \right)^2 \left(\frac{1}{\omega} \right)^3 \quad (4.2)$$

where Z_0 correspond to the characteristic impedance of the inductor. As seen from Equation 4.2, at low frequencies inductor coupling increases linearly as a function of the mutual inductance between structures. As the frequency increases capacitance to the substrate shunts the contribution of coupled magnetic flux.

Figure 4.1: Inductor coupling model investigation as a function of frequency with various circuit components parametrized a) Circuit model, b) parametrized inductance levels L (with $M=40\text{pH}$), c) parametrized Mutual coupling M (with $L=1\text{nH}$), d) parametrized dielectric capacitance C_p (with $M=40\text{pH}$ and $L=1\text{nH}$)

4.1.2 EM Experimental setup

After a preliminary evaluation of the simple model of 4.1(a), inductor structures were defined for EM modeling in Sonnet (Figure 4.2). The geometry of the structures is specified in Table 4.1 and with reference to Figure 4.2. Physical cross-section of the process used during this simulations was shown in Figure 3.23.

Figure 4.2: Inductor Coupling Simulated Structures

Table 4.1: Inductor physical parameters used for EM simulation with Sonnet

Parameter	Unit	Value
Width	μm	200
Length	μm	200
Spacing	μm	5
Turns		2
Separation	μm	25 - 150

The series inductance and Q as a function of frequency for each of the structures investigated are plotted in Figure 4.3. EM investigation for this structure was conducted for frequencies up to 40 GHz. The sizes for this structures were chosen to be appropriate for the frequency ranges investigated.

Figure 4.3: Series inductance and Q as a function of frequency for each structure investigated in Figure 4.2

It is not obvious at first glance how the quality factor of the source and target inductor used for coupling analysis will affect the coupling between them. For the purpose of setting up the structures in this experiment and while there are many ways to modify the quality factor of an inductor (decrease series resistance, increase inductance, etc.), many of these methods rely on changing the physical dimensions of the device, making it difficult to separate losses as a result only of a change in the quality factor of the inductors. Therefore, to understand the effect of the inductor's quality factor Q , an investigation of coupling between inductors using copper and aluminum metalization was carried out (Figure 4.4).

Lower metal resistivity, therefore higher quality factors decrease coupling between inductors by approximately 0.5 dB for frequencies ≥ 5 GHz.

A similar simulation was set up to examine the effect of the thickness of the top conductor on coupling. This thickness was set at $1\mu\text{m}$, $2\mu\text{m}$ and $4\mu\text{m}$. Results are shown in Figure 4.5.

Figure 4.4: Inductor coupling for Al vs. Cu metalization (spacing = 25 μm)

Figure 4.5: Inductor coupling as a function of frequency with metal thickness as a parameter (spacing = 25 μm)

Unlike the case where metal resistivity was varied, modifying the top conductor metal thickness affected coupling levels at low frequencies, as a results of changes in the mutual coupling between structures. For high frequencies, coupling was increased by a factor of 0.3 dB when top thick metal layers were used ($4\text{ }\mu\text{m}$ vs. $1\text{ }\mu\text{m}$)

The effect of substrate resistivity was also investigated. The resistivity of the silicon substrate was varied from a typical $10\Omega\text{-cm}$ to 30, 60 and $90\text{ }\Omega\text{-cm}$. Results can be see in Figure 4.6. State of the art silicon processes have incorporated the option for higher substrate resistivities varying from 10 to $90\Omega\text{-cm}$ for standard commercial processes[5]. As seen from Figure 4.6, at very high frequencies, coupling levels can be increased by as much as 3 dB at 40 GHz when substrate resistivity is increased to $90\Omega\text{-cm}$ from its nominal value of $10\Omega\text{-cm}$. Recall that as substrate resistivity is increased, the substrate will act more as an insulator, with reduced shunt capacitance to ground, and magnetic field coupling will dominate at higher frequencies as shown in Equation (4.2).

Finally, the physical separation between inductors was varied from $25\mu\text{m}$ to $150\mu\text{m}$ in $25\mu\text{m}$ steps and can be seen in Figure 4.7. As expected, increasing the separation between inductors decreases the coupling. Also, as shown in Table 2.4 in page 33, it is expected that power will drop a a rate proportional to r^4 , where r correspond to the separation between the structures in question. EM of coupling as a function of separation between the inductors is shown in Figure 4.7.

For EM simulation results to be of maximum value, they must be reduced to an equivalent circuit model that can be used in circuit simulation. Here the equivalent circuit of Figure 4.8(a) was used.

Figure 4.6: Inductor Coupling as a function of frequency with the resistivity of the Silicon substrate as a parameter (spacing = 25 μm)

Figure 4.7: Inductor coupling as a function of frequency with inductor separation as a parameter

Figure 4.8: Differential Inductor modeling in ADS momentum a) Model fitted from s-parameter data b) Comparison of S_{11} of model vs. EM data, c) Smith chart comparison of S_{11} of model vs. EM data, d) Comparison of S_{21} of model vs. EM data

Alternatively, one can use circuit simulator packages such as HSPICE [91] to fit EM s-parameter data to its equivalent circuit. Details are shown in Appendix B.2.

4.1.3 Coupling between CPW structures

Coupling was also studied for CPW structures. As an example coupling between CPWs is likely to be important in distributed amplifiers. Due to space constraints, both the gate and drain line inductances in a distributed amplifier are normally placed in proximity to each other. The coupling effects between them will not be negligible and must be accounted for during simulation. Consider Figure 4.9 in which two CPWs are placed in proximity to one another. As the physical separation is decreased, coupling is expected to increase as shown in Figure 4.10.

During CPW design and implementation, designers must keep lines as symmetric as possible to reduce slot-line effects. When a CPW is unbalanced due to asymmetric ground planes, it is expected the even modes of coupling are excited increasing coupling between two adjacent lines. This can be seen in Figure 4.11, in which the ground planes of the CPW were made asymmetric (Refer to Figure 4.9b))

Coupling was first modeled as a function of separation, with CPWs separated by $100\mu\text{m}$, $150\mu\text{m}$ and $200\mu\text{m}$. Results can be seen in Figure 4.10. A dip in coupling levels at 5GHz is an artifact of the EM simulator.

Coupling between CPWs was also studied when the ground planes of CPWs were made asymmetric. Results can be seen in Figure 4.11. A dip in coupling levels at 5GHz is an artifact of the EM simulator.

Coupling levels are increased as much as 4 dB when slot-line modes are excited in the CPW. Recall that from basic microwave theory, the coupling coefficient k of a transmission line can be expressed as follows:

$$k = \frac{Z_{0e} - Z_{0o}}{Z_{0e} + Z_{0o}} \quad (4.3)$$

Where Z_{0e} and Z_{0o} represent the even and odd mode impedance of a transmission line [85].

4.2 Coupling in Resonators

In an integrated RF chip, it is expected that most inductors will be implemented in some form of a resonator tank. The basic circuit schematic of two coupled resonator tanks is shown in Figure 4.12.

Figure 4.9: CPW coupling structures using a) symmetric ground planes and b) asymmetric ground planes.

Figure 4.10: CPW coupling S_{14} with separation as a parameter.

Figure 4.11: CPW coupling for separation of 100 μm with and without symmetric ground planes.

Figure 4.12: Coupled resonator equivalent circuit model

The layout for a resonator can be seen in Figure 4.13. Resonators can be designed using multiple capacitors so as not to disturb tank impedance during measurement as shown in Figure 4.13.

Figure 4.13: Equivalent resonator circuit model

Simulations of coupling between resonators centered at the same frequency show interesting results which can be seen in Figure 4.14 and were setup with reference to the equivalent circuit shown in Figure 4.12.

Figure 4.14: Resonator coupling simulations of Figure 4.12 (y axis represent Z_{21} in dB: a) Resonator coupling as a function of the coupling coefficient k for $R1 = R2 = 6 \Omega$, b) Resonator coupling as a function of the coupling coefficient k for $R1 = R2 = 2 \Omega$, c) Resonator coupling as a function of source/load impedance (not shown in Figure 4.12), d) Resonator coupling as a function of resonator Q

In Figure 4.14(a) resonator coupling is shown as a function of the coupling coefficient. As expected, higher levels of coupling coefficient k increase coupling. k can be increased by increasing proximity between resonators or by modifying the orientation of the inductors. Also noticeable is the dependence of the weak mode of coupling in resonators on the resonator's tank quality.

Based on Figure 4.12, resonator coupling can be derived as follows:

$$\begin{aligned}
Z_{21}(s) &= \frac{V_2}{I_1} \\
&= \frac{sM}{(s^2L_1C_1 + sR_1C_1 + 1) \cdot (s^2L_2C_2 + sR_2C_2 + 1) - k^2s^4C_1C_2L_1L_2} \quad (4.4)
\end{aligned}$$

$$\begin{aligned}
Z_{11}(s) &= \frac{V_1}{I_1} \\
&= \frac{(sL_1 + R_1)(1 + sR_2C_2) + sC_2[s^2(L_1L_2 - M^2) + sR_1L_2]}{(s^2L_1C_1 + sR_1C_1 + 1) \cdot (s^2L_2C_2 + sR_2C_2 + 1) - k^2s^4C_1C_2L_1L_2} \quad (4.5)
\end{aligned}$$

where $M = k\sqrt{L_1L_2}$.

Coupling analysis for resonators [90] suggest there are two dominant coupling modes present in resonators. These modes can be found by setting the denominator of Equation 4.4 to zero. The frequencies of oscillation for this modes suggest there is a strong resonator coupling mode at $\omega_o/\sqrt{1+k}$ and a weak resonator coupling mode at $\omega_o/\sqrt{1-k}$.

Figure 4.14(b) also shows circuit simulation results with both strong and weak resonator coupling modes clearly visible. The relative magnitude of the weak mode is dependent on the quality factor of the resonator as well as to the loading to the resonator. If the resonator has low quality factors the weak coupling mode will not be visible as shown in Figure 4.14(d).

Figure 4.15 shows the accuracy of the mathematical equations shown above compared to a circuit simulator(e.g. PSPICE)

Figure 4.15: Resonator coupling modeling comparison of circuit simulator vs. Matlab plot of Equations (4.4)

Based on the analysis presented above, it is possible to estimate coupling levels between on-chip resonators. This theory will be useful as we present next a method of measurement of on-chip coupling and its comparison to uncalibrated resonator measurements.

4.3 A technique aimed at calculating on-chip coupling

A novel experiment for measuring on-chip coupling of integrated inductors using injection locked oscillators is presented in this section [22]. The experiment is unique in that no matching, probe de-embedding or calibration is necessary as the ratio of two signals on the same chip is measured to yield the results. Theoretical and simulated models of injection locked oscillators and inductor coupling are discussed and compared to experimental results measured using a test chip.

The effects of on-chip inductor coupling are directly applicable to many facets of integrated circuit design. A typical 2.5 mm by 2.5 mm RFIC chip could have 15 to

20 inductors with significant coupling between independent functional blocks. Inductor coupling is poorly modelled by most RF design tools making it difficult for both system and circuit designers to incorporate the effects into simulations and the design process. Isolation mechanisms such as guard rings are frequently added to circuit layouts, increasing the manufacturing expense of the chip, and these precautions are often based on little more than empirical assumptions in hopes of minimizing the coupling between blocks. Previous experiments reported in [92], [39] and [40] (to name but a few) have shown that coupling between on-chip inductors can be significant and that the magnitude of the coupling is affected by the spacing and orientation of the inductors. While these experiments have been successful in determining the factors that affect the amount of coupling they require careful matching and de-embedding in order to achieve quantitative results. The experiment presented in this section makes use of oscillators and resonators with on-chip inductors in order to quantitatively analyze the coupling between inductors without the need to match or de-embed any circuits. The absolute ratio between two signals on-chip that experience similar losses is indicative of the coupling magnitude. The experiment requires the injection locking of an on-chip oscillator which were done as separate but collaborative research with Popplewell *et al.* [22] provides more detail. Similarly, a theoretical analysis and simulations of on-chip inductor coupling are presented and the experimental results are compared to the theory.

4.3.1 The RF oscillator as a Sensitive Measurement Device

By using two closely matched oscillators on the same chip the amount of inductor coupling can be measured without matching the input or output of the circuit or making calibration measurements. Figure 4.16 shows the general setup for the experiment.

VCO_1 is injection locked to an external input signal at $f_{LNA} = f_0 - \Delta f$ by way of an LNA with output connected to VCO_1 's tapped resonator. The output of VCO_2 is monitored with a spectrum analyzer and the ratio between the signal strength at f_0 and that at f_{LNA} is indicative of the inductor coupling magnitude. As the total output power of both oscillators is the same and the gain applied by VCO_2 to the coupled tone at f_{LNA} can be determined as discussed in the literature [22], the only

unknown (which can now be determined) is the magnitude of the inductor coupling, as follows:

$$\text{Measurement} = \frac{P_{VCO1} \times \text{Coupling} \times H(s)}{P_{VCO2}} \quad (4.6)$$

$$\text{Inductor Coupling} = \frac{\text{Measurement}}{H(s)} \quad (4.7)$$

where P_{VCO1} and P_{VCO2} correspond to the output power of oscillator 1 and 2 (by design: $P_{VCO1} = P_{VCO2}$). $H(s)$ represent the phase noise of VCO₂. A derivation of the transfer function of the oscillator $H(s)$, e.g. phase noise response, has been provided by Popplewell *et al.*[24].

Figure 4.17 shows a four port inductor coupling structure modelled using Agilent Momentum [88] and a circuit model for the structure. The spacing and orientation of the simulated inductors is the same as those of the inductors in the oscillator pair on the experimental chip.

Simulation results for the structure shown in Figure 4.17 are presented in Figure 4.18. For low frequencies the coupling between both inductors increases linearly as a function of their mutual inductance. At high frequencies however, the inductor ports are shunted to ground by the shunt dielectric capacitance. The predicted coupling between inductors at the frequency of the experiment is approximately -36 dB.

Figure 4.16: Experiment Setup

Figure 4.17: Coupled Inductor Circuit Model and Momentum Structure

Figure 4.18: Inductor Coupling vs. Frequency

Figure 4.19a) shows analysis and measurement results of coupling as a function of the resonator tank Q , for identical resonators placed $175 \mu\text{m}$ apart. Maximum coupling is achieved at the resonant frequency ($f_{res} = 4.5 \text{ GHz}$). From Figure 4.19a) the measured Q is estimated to be 4 at 5 GHz. The coupling coefficient k between the two resonators is a function of the inductor area and the inductor separation. Based on the coupling levels shown in Figure 4.19a), k was estimated to be about 0.025.

Figure 4.19: S_{21} coupling results a) Two identical resonator placed $175 \mu\text{m}$ apart b) Coupling results of using silicon vs. quartz substrates

4.3.2 Radiated versus Conductive Substrate Coupling

An EM simulator was used to separate the substrate conductive coupling from the overall coupling between two inductors by replacing the conductive silicon substrate with quartz, both with dielectric constant ϵ_r of about 4. Figure 4.19(b) shows the result. The conductive contribution is about 3 dB at 4 GHz, but as frequency increases, the substrate resistance R_{sub} decreases due to parasitic capacitance (not shown) across R_{sub} , and hence coupling increases. At 10 GHz, the conductive coupling adds about 5 dB to the coupling between inductors, and hence is the largest contributor.

4.4 Experimental Chip Design

The VCOs implemented are identical and were constructed using a simple cross coupled negative resistance configuration as shown in Figure 4.20. The oscillating frequency can be calculated as

$$f_{osc} = \frac{1}{2\pi\sqrt{L_t C_t}} \quad (4.8)$$

where L_t and C_t correspond to the total inductance and capacitance of the resonant tank. The resistance seen looking into the cross coupled transistor pair is approximately $-\frac{1}{2g_m}$. By properly sizing this negative resistance block any resistive losses present in the tuned tank can be canceled out.

4.5 Experimental Results

The circuits were implemented using the IBM5HP BiCMOS process with three metal layers, including a 2 μm thick analog metal layer approximately 6 μm away from the substrate. Figure 4.21 shows a picture of the experimental chip.

A PCB was designed and the experimental chip was wire bonded to the board for testing. Figure 4.22 shows the PCB complete with the wire bonded test chip.

Prior to conducting the coupling experiment both oscillators were characterized to ensure identical behavior. To measure the coupling between inductors one of the oscillators was injection locked to a signal generator that was used to adjust the frequency of the oscillator and the offset relative to the second oscillator which is free

Figure 4.20: Experiment Schematic

Figure 4.21: On-Chip Coupling Test Chip

Figure 4.22: On-Chip Coupling Test Chip and PCB

running was determined. The output of the second oscillator was monitored and the ratio between the free running tone and the coupled tone from the injection locked oscillator was recorded. As the gain of the second oscillator to the coupled tone can be determined theoretically, the magnitude of the inductor coupling can be extracted. Figure 4.23 shows the spectrum of one such measurement. Note that the alias tone in this figure can be explained by basic sampling theory between the free running frequency of the oscillator and the coupled tone [24].

Figure 4.23: Output Spectrum of Oscillator with Coupled Tone

Also, the simulated single-sided equivalent unloaded bandwidth for the oscillator was 550 MHz. This implies that at an offset of 550 MHz from the carrier frequency of the oscillator, the oscillator gain is zero and inductor to inductor coupling is expected at -36 dB. As the coupled tone moves closer to the carrier frequency the power in the coupled tone will increase at a rate of 20 dB/decade as shown in Figure 4.24.

Figure 4.25 summarizes the measured power ratios between the free running tone and the coupled tone as a function of offset frequency. The coupled power rolls off at approximately 20 dB/decade as suggested by the theoretical oscillator response. The solid line in Figure 4.25 shows the theoretical response predicted by the oscillator theory and the momentum simulations which suggest inductor signal coupling of -36 dB (Also refer to Figure 4.24). The measured results suggest that the inductor coupling is closer to -35 dB, only 1 dB higher than that predicted by the simulations.

Figure 4.24: Description of calibration free measurement

Note that the 1 dB difference between measured and predicted coupling is a very accurate result further showing the high sensitivity of oscillators to coupling.

Figure 4.26 shows the relationship between inductor coupling and inductor separation from center to center at a frequency of 3.5 GHz. The data measured with the injection-locked oscillator coupling into the spectrum of the free-running oscillator is in strong agreement with the simulated coupling for the implemented inductors with 175 μm separation. To consider the coupling at a separation of 305 μm , a tone was injected into one of the on-chip resonators and the coupled tone was measured at the output of the free-running oscillator as before. After accounting for the gain of the oscillator, the measured coupling is -56 dB which is about 6 dB lower than the predicted result. This deviation is understandable as unlike the oscillator to oscillator test, the resonator to oscillator measurement's accuracy is affected by impedance mismatch at the input and further demonstrates the effectiveness of the oscillator to oscillator test. Also important to note that resonator to oscillator coupling might have been affected by metal filling, added in order to satisfy technology requirements during implementation of the IC (See Figure 4.21).

Figure 4.25: Summary of Coupled Power Ratio vs. Offset

Figure 4.26: Inductor Coupling vs. Separation at 3.5 GHz

4.6 Summary

This chapter presented a study of EM coupling in silicon substrates. Structures investigated included inductors, resonators and transmission lines (particularly CPWs). An understanding of how coupling is affected by process parameters such as metal resistance, substrate resistance, separation, etc. has been presented. Coupling was also

found to increase when slot-line effect are allowed to propagate in a CPW and which is a concern in the design of distributed amplifiers. Coupling between resonators was studied in simulation and verified experimentally.

To verify theory, a calibration-free on-chip coupling experiment making use of an injection-locked bipolar oscillator was presented. Two 1.5 nH, three turn inductors spaced 175 μm apart were used. Inductor coupling of -35 dB was measured with ease, while lengthy EM simulations and oscillator theory predict -36 dB of coupling, virtually the same result. Results from this experiment were compared versus EM simulation and incorporated into circuit design. The observed high level of coupling further attests to the importance of considering inductor coupling in RFIC designs.

Chapter 5

Gain, Bandwidth limits for Silicon based distributed circuits

A study of the gain and bandwidth limitations of a distributed amplifier implemented in silicon substrates is presented in this chapter.

5.1 Gain-Bandwidth Limitations

In this chapter, it will be shown that the gain bandwidth product of a fully integrated distributed amplifier in silicon is limited to approximately 55% of the f_{max} of the gain stage used. In this study three commonly used gain stages were considered in a distributed amplifier: single transistor, cascode and Darlington f_T doubler. A limit on the bandwidth for the distributed amplifier is presented as a function of the choice of gain cell, quality of the passives (dependant on the substrate properties), and the number of stages used. Gain and matching considerations are also presented. Measurements of three distributed amplifiers verify the simulation results.

Because the transistor's parasitic capacitances are absorbed in a distributed amplifier, conventional wisdom says the gain bandwidth limitation which limits the frequency behavior of conventional circuits no longer applies for distributed circuits. Most of the analysis found in literature applies to GaAs, InP and other technologies which do not have similar limitations as silicon based devices, making it difficult to extrapolate many of these assumptions [93]. In this chapter, a series of distributed amplifiers in silicon are optimally designed by simulations to explore how the performance depends on the choice of gain cell, the number of stages and the available

inductor or transmission line Q. Performance is measured in terms of the achievable gain and bandwidth.

5.2 Bandwidth of Distributed Amplifiers

Distributed Amplifier theory has already been presented in Chapter 2. To understand the gain bandwidth limitations of a distributed based circuit, consider a single gain stage in a distributed amplifier as seen in Figure 5.1. There are three major sources of frequency limitation as follows:

- The frequency pole formed at the input of the amplifier's gain cell. R_i and C_{gs} correspond to the input series resistance and input capacitance of the transistor. $\omega_g = \frac{1}{R_i C_{gs}}$.
- The frequency pole formed at the output of the amplifier's gain cell. R_{ds} and C_{ds} correspond to the gain stage's output shunt resistance and capacitance respectively. $\omega_d = \frac{1}{R_{ds} C_{ds}}$.
- The cut-off frequency of the artificial transmission line formed by series inductances L_g and L_d and the corresponding input and output capacitance of the gain stage C_{gs} and C_{ds} . $\omega_c = \frac{2}{\sqrt{L_g C_{gs}}} = \frac{2}{\sqrt{L_d C_{ds}}}$

5.2.1 Gate/Drain Artificial line attenuation

The attenuation of the gate and drain artificial line (A_g and A_d respectively) can be seen in ((5.1)) and ((5.2)). Also, A_g and A_d can be plotted as a function of the three limiting parameters described above (ω_g , ω_d and ω_c). The results can be seen in Figures 5.2 and 5.3 [93, 94].

$$A_g = \frac{(\omega_c/\omega_d) X_k^2}{\sqrt{1 - X_k^2 \left[1 - \left(\frac{\omega_c}{\omega_g} \right)^2 \right]}} \quad (5.1)$$

$$A_d = \frac{\omega_d/\omega_c}{\sqrt{1 - X_k^2}} \quad (5.2)$$

Figure 5.1: Gain cell of a distributed amplifier showing frequency limitations

Where X_k corresponds to the frequency normalized to the cut-off frequency of the artificial transmission line ω_c .

$$X_k = \frac{\omega}{\omega_c} = \frac{f}{f_c} \quad (5.3)$$

Reduced attenuation of the gate and drain artificial lines is expected for:

- small ω_c / ω_g factor
- small ω_d / ω_c factor

From a circuit perspective this implies that the gain cell used will have a small series input resistance and large parallel output resistance.

5.2.2 The Bandwidth factor of a Distributed Amplifier

By varying the ω_c / ω_g and ω_d / ω_c factors, it is possible to plot the normalized gain of a distributed amplifier as a function of the normalized frequency X_k (Figure 5.4). The normalized gain of a distributed amplifier corresponds to the frequency dependent gain of the distributed amplifier normalized to its low frequency gain (DC) as follows

$$A_N = \frac{A(f)}{A_0} \quad (5.4)$$

Figure 5.2: Gate line attenuation A_g as a function of ω_g , ω_d and ω_c

The bandwidth factor X can be represented as a measure of how close the 1 dB frequency of the gain response approaches the cut-off frequency of the transmission line. Ideally a flat gain response is desired $X_k = 1$.

$$X = \frac{\omega_{-1dB}}{\omega_c} = \frac{f_{-1dB}}{f_c} \quad (5.5)$$

It can be seen from Figure 5.4 that by reducing the ω_c / ω_g and ω_d / ω_c products increases the bandwidth factor X (Case C). Again this will imply the use of a gain cell with low series input resistance and large parallel output resistance.

5.2.3 The gain factor of a distributed amplifier

For low ω_d/ω_c Beyer *et al.* [93, 94] showed that

$$\frac{A_o f_c}{4 f_{max}} = \sqrt{\frac{n^2 \omega_d}{4 \omega_g}} \cdot e^{-\frac{n}{2} \left(\frac{\omega_d}{\omega_c} \right)} \quad (5.6)$$

where

$$K = \sqrt{\frac{n^2 \omega_d}{4 \omega_g}} \cdot e^{-\frac{n}{2} \left(\frac{\omega_d}{\omega_c} \right)} \quad (5.7)$$

Figure 5.3: Drain line attenuation A_d as a function of ω_g , ω_d and ω_c

and f_{max} defined as the frequency where the maximum available gain becomes unity. K is defined as the gain factor of a distributed amplifier. it can be seen from (5.6) that the gain product K increases by

- Increasing n
- Increasing ω_d/ω_g
- Increasing ω_d/ω_c

The last two conditions will imply a reduction in the bandwidth factor of distributed amplifier which implies that some trade-offs are required.

5.2.4 The gain bandwidth product of a distributed amplifier

By combining the results from the previous two subsections, it is possible to define a Gain-Bandwidth product for a distributed amplifier. This will consist of the product KX , which can be obtained by re-writing (5.6) as follows:

$$A_o f_{-1dB} = 4KX f_{max} \quad (5.8)$$

Figure 5.4: Normalized gain A_N as a function of the normalized frequency X_k

By combining (5.6), (5.7) and (5.8), the gain-bandwidth limit of a distributed circuit can be re-written as follows [93]:

$$\frac{A_0 f_c}{f_{max}} \approx 4 \frac{N}{2} \sqrt{\frac{\omega_d}{\omega_g}} e^{\frac{-N\omega_d}{(2\omega_c)}} \quad (5.9)$$

5.3 CMOS Technology

For the purpose of this experiment, all simulations were carried out in a 0.18 μm CMOS technology with 1 poly layer and 6 Al metal layers(1P6M). To achieve isolation from the lossy substrate, all passives were implemented using the top available metal layer, reducing the series resistance of the line, thereby increase the achievable quality factors of all transmission lines. This gain bandwidth investigation was limited to CMOS devices but some of the conclusions are valid for SiGe as will be shown in the measurement section.

5.4 Lossy transmission lines

The design of the gain cell will not only determine the achievable gain of the distributed amplifier but it will also have have a strong impact on the achievable bandwidth. The input and output capacitance of the gain cell will degrade the performance

of the lossy transmission line increasing the attenuation per stage. In general, we can express the attenuation of a transmission line as follows

$$\alpha = \frac{1}{2} \left(\frac{R_s}{Z_0} + GZ_0 \right) \quad (5.10)$$

attenuation can be decreased at the input gate artificial transmission line by:

- Minimizing series resistance for the transmission line (R_s is decreased) as well as the transistors input series resistance (R_{gate} is decreased)
- Increasing line isolation from the underlying substrate by using top available metal (G is decreased)
- Increasing line impedance which will also increase low frequency gain

Further degradation of the artificial transmission lines is expected when considering the finite output resistance of the transistor. In this case the conductance of the artificial line will be approximately $G = \frac{n}{r_0}$ where n represents the number of gain stages used and r_0 defines the finite output resistance of the amplifier. Similarly attenuation can be decreased by

- Using a cascode gain cell to increase the output resistance of the circuit
- Using the optimum value for the number of stages n (Gain is also dependent on n)

Figure 5.5 shows the gain of the distributed amplifier as a function of the quality factor of the transmission lines used (The bandwidth of the amplifier was kept nearly constant at 20 GHz). Results were plotted for amplifiers employing 3, 4 and 5 single transistor gain stages. As the quality factor of the transmission lines was increased the gain and the optimum number of stages increased. It is clear that the advantage of increasing the number of stages to improve gain is only seen for Q factors greater than 14.

If we replace the single transistor gain stages by cascode gain stages, a similar is presented in Figure 5.6. The advantage of using 5 stages is seen this time for passive devices with quality factors of 8 or greater. Clearly the use of a cascode configuration reduces degradation in the performance of the transmission line.

Figure 5.5: Gain as a function of Q factor for single transistor gain stage in a distributed amplifier

5.5 BW enhancement

Although the distributed circuits do not suffer from the conventional gain-bandwidth limitations seen in conventional amplifiers, it has been shown by Wong that the gain bandwidth product of a distributed amplifier can not exceed the f_{max} of the gain stage used, due to internal dissipation [94]. Therefore the gain stage used in the distributed amplifier must be designed to have the highest possible f_T (a technology dependent parameter) and f_{max} (a layout dependent parameter which also depends on f_T).

The use of f_T doubler will allow for a higher gain bandwidth product for distributed amplifier. Two methods commonly used to double f_T are the use of a differential pair and the Darlington f_T doubler. Differential circuits maintain the input transistor transconductance g_m constant while the input capacitance is halved. The use of a Darlington configuration uses two input devices (double g_m) driven from a single input capacitance value. Due to the increase in layout area needed to implement a differential distributed amplifier, only Darlington f_T doublers will be considered.

An increase in the output resistance is achieved by using a cascode gain cell, minimum gate resistance is achieved by properly sizing the finger width used during

Figure 5.6: Gain as a function of Q factor for cascode gain stage in a distributed amplifier

the layout of the transistors [6]. The use of multiple finger also reduces parasitic capacitance at the drain and source of the device. The use of multiple vias also reduces resistance between multiple metal layers and must be considered. Figure 5.7 shows the Maximum Available Gain MAG for a single gain stage as a function of frequency. Results were plotted for three common gain cell configurations used in distributed amplifiers: single transistor, cascode and Darlington f_T doubler.

Although the Darlington f_T doubler achieves a higher MAG at low frequencies, the use of cascode configuration achieves the highest possible MAG over a larger range of frequencies, justifying the use of this topology over the single and Darlington configurations.

5.6 Gain Considerations

Two other considerations are important when considering the gain of a distributed amplifier:

- It is desirable to have high levels of gain while achieving large bandwidths (large $\frac{A_0 f_c}{f_{max}}$)

Figure 5.7: MAG for various amplifier gain cells investigated

- It is desirable to minimize the gain ripple in the passband (Better unilateral gain cell)

Recall from (5.9), that the gain-bandwidth limit of a distributed circuit can be computed as follows

$$\frac{A_0 f_c}{f_{max}} \approx 4 \frac{N}{2} \sqrt{\frac{\omega_d}{\omega_g}} e^{\frac{-N\omega_d}{(2\omega_c)}} \quad (5.11)$$

and for distributed amplifiers implemented in GaAs, Wong [94] determined that this gain bandwidth limitation is approximately $\frac{A_0 f_c}{f_{max}} \approx 0.8$. This has not been however, verified for distributed amplifier implemented in silicon substrates. A summary of the experimental technique used is presented below:

1. Design a DA using a single, cascode and Darlington gain stage.
2. Assume a constant Q for all passives
3. Optimize the gain bandwidth product (KX)

Optimize ω_c/ω_g and ω_d/ω_c

Calculate optimum number of stages

Reducing R_i and increase R_{ds} by proper transistor sizing

Refinements made by using SPECTRE.

4. Vary the Q of transmission line from 2-20 and repeat steps 1 to 3.
5. Plot GBW of Silicon based DA as a function of the passive Q.

Figure 5.8 shows the simulated ratio of the gain bandwidth limit and the f_{max} for the gain stages examined in this work. An optimum number of stages and an initial value for the Quality factor of 10 was used for all gain configurations and transmission lines respectively. As the bandwidth was increased, the gain was kept nearly constant and the highest possible bandwidth was simulated for each configuration. Results were then normalized to the f_{max} of the gain cell used.

Figure 5.8: Gain bandwidth limit normalized to the gain cell's f_{max}

The cascode gain cell achieved a gain-bandwidth limit of 0.55 normalized to the gain cell's f_{max} . The use of a single transistor gain cell only achieved normalized gain bandwidth products as high as 0.45 and finally the Darlington f_T doubler only achieved gain bandwidth products of 0.37.

5.7 Measurements

Of all the amplifiers simulated, several amplifiers have been fabricated and tested. The first was a cascode design in $0.35\ \mu\text{m}$ CMOS with f_T of 13 GHz and f_{max} of 11 GHz, which achieved gain up to 5.5 GHz with inductor Q of 4 [7]. The second one in a $0.18\ \mu\text{m}$ process with f_T of 62 GHz and f_{max} of 55 GHz and transmission line Q of 12 achieved gain up to 27 GHz [8]. The third amplifier in SiGe [95] with f_T of 120 GHz and f_{max} of 100 GHz had gain up to 50 GHz. Equivalent Q was 14. Table 5.1 shows a comparison of some of these and other published results, all in reasonable agreement with the previous discussion. More details regarding circuit implementation of fully integrated distributed amplifiers in silicon will be presented in the next chapter.

Table 5.1: Comparison of measured and other published results in silicon

Ref	Process	Config.	BW(GHz)	$\frac{A_o BW}{f_{max}}$
[63]	$0.6\ \mu\text{m}$ CMOS	cascade	4	0.44
[7]	$0.35\ \mu\text{m}$ CMOS	cascade	5.5	0.5
[8]	$0.18\ \mu\text{m}$ CMOS	cascade	27	0.49
[95]	IBM7HP SiGe	cascade	50	0.5
[66]	$0.18\ \mu\text{m}$ CMOS	cascade	23	0.4
[65]	$0.18\ \mu\text{m}$ CMOS	darlington/cascade	10	0.18

5.8 Summary

In this chapter, a study of the gain and bandwidth limitations in distributed amplifiers in silicon substrates has been presented. Previously, a comprehensive study was only available for distributed amplifiers implemented in GaAs and other III-V technologies which do not suffer the same limitations as silicon based circuits. The achievable quality factors of passives implemented in silicon were found to be the most dominant factor limiting the gain and bandwidth of silicon based distributed amplifier. The choice of gain topology played an important role in minimizing the transmission line degradation of the attenuation in the transmission line. A cascode transistor configuration achieved the highest gain bandwidth product for all gain stages studied

here. Measurements and literature results agree with the limits presented in this work. Results for distributed amplifiers in CMOS with bandwidths higher than 20 GHz [8, 66] show lower gain-bandwidth products than those shown in Figure 5.8. The lower gain bandwidths achieved by CMOS distributed amplifiers can be attributed to additional high frequency substrate losses in silicon due the choice of passives used (e.g. spiral inductor, microstrip, CPW).

Chapter 6

Distributed Amplifier Design in Silicon

6.1 Introduction

In this chapter, several distributed amplifiers are designed following the design principles in Chapter 3 and verification of the theory and as a demonstration that better theory can lead to being able to take better advantage of the technology in achieving maximum gain and bandwidth as outlined in Chapter 5. The first design is aimed at achieving high gain and uses a $0.35\mu\text{m}$ CMOS technology with spiral inductors to implement artificial transmission lines. The second design uses coplanar waveguides to realized required inductances. Design was implemented in a $0.18\mu\text{m}$ CMOS process and aimed at achieving the largest possible bandwidth.

6.2 Design of High Gain distributed Amplifiers in $0.35\mu\text{m}$ in CMOS

A distributed amplifier was implemented in standard $0.35\mu\text{m}$ CMOS technology with an approximate f_t of 13 GHz. The basic topology can be seen in Figure 3.13. M-derived half sections ($m=0.6$), were used to match the input and output ports to 50 Ohms. The addition of a cascode gain cell allowed for a better unilateral approximation [85], which improves impedance matching and it also reduces the Miller effect in the driver transistor, improving the amplifier's overall frequency response. The gain peaking effect was minimized by purposely mismatching the delay of the

drain and gate lines where $f_{c,drain} = 0.7 \cdot f_{c,gate}$, this can be achieved by modifying the shunt capacitance at the drain of the device C_{add} . Table 6.2 shows the dependence of the gain peaking as a function of this added capacitance C_{add} , where the nominal gain is approximately 16 dB and it drops to 13 dB around 4.5 GHz with a unity gain frequency of the amplifier of approximately 5.5 GHz(refer to Figure 6.1).

Table 6.1: Effect of C_{add} on the gain peaking

C_{add} (fF)	Gain Peak (dB)
450	13.4
480	15.4
520	15.9
560	16.7

Inductors were implemented in top available metal and an octagonal configuration was used to minimize losses due to sharp bends, and to improve the quality factor of these inductors as discussed in Chapter 2. Metal lines used as interconnects were also modelled as transmission lines to account for the phase shift and losses in the signal path. Line termination was provided by the use of m-derived half sections (See Figure 2.19). The circuit used a single 3V supply, which was provided through a drain dummy termination (see Figure 3.13). All s-parameter simulations were carried out in SPECTRE.

Some of the guidelines used for this design and based on the principles discussed in Chapters 2, 3 and 5:

- The number of gain stages used in the distributed amplifier must be optimized for the technology in which it is implemented. While increasing the number of stages N should increase gain as suggested in (2.32), parasitics present in the passives used will limit performance and for Si CMOS based designs should be the limiting factor ($N \leq 5$ as shown in Chapter 5).
- The use of a cascode gain stage improves the unilateral assumption for each gain stage and increases output impedance.
- Increasing the FET transconductance by increasing transistor size increases the input/output capacitance of the device, and for a constant line impedance lowers

the inductance required. Lower inductances allow for higher quality factors and higher self resonant frequencies for these devices and this can be translated into an increase in gain by properly accounting for passive losses.

- Transmission line effects should not be under-estimated and back of the envelope calculations for k and m-section models in general are not enough. Proper transistors models should go hand in hand with the use of EM simulators (e.g. HP Momentum or HFSS) [88].
- CMOS FET transistor layout should be optimized for maximum f_t and for the processes used in this thesis, the length of each finger in this process should be limited to $4\ \mu\text{m}$ [6].
- Layout symmetry is vital to ensure proper phase delay in all artificial transmission lines used, failure to achieve delay equalization will attenuate signal decreasing gain.
- If frequency of operation permits, one should choose coplanar waveguides over microstrip and coil inductors since the coplanar ground plane should reduce losses due to Si substrate and thereby increase gain.
- Avoid the use of coupled differential lines, since it is very difficult to maintain impedance levels due to process variations and other effects [6].

6.2.1 Simulation and Measurement

Figure 6.1 shows a comparison of the simulated S_{21} results versus measured results for this amplifier. There is a difference of approximately 3 dB in the gain response and this can be attributed in part to variations in the simulated and modelled inductors. The mismatch in the model accounts for extra series capacitance C_{ser1} and C_{ser2} (refer to Figure B.4). This capacitance is connected directly in parallel with C_{added} as seen in Figure 6.2, and makes the total capacitance seen at the FET's drain

$$C_{total} = C_{add} + C_{ser1} + C_{ser2} \quad (6.1)$$

where C_{ser1} and C_{ser2} correspond to the series capacitance for the inductor model seen to the left and to right of the FET. An increase in the total capacitance at the

drain will increase the attenuation due to a mismatch in the delay of the gate and the drain artificial transmission lines.

Table 6.2: Measured inductor model parameters

Parameter	Units	Simulated	Measured
L_{ser}	nH	2.11	2.34
R_{ser}	Ω	3.65	4.57
C_{br}	fF	145	130
C_{ser1}	fF	560	745
C_{ser2}	fF	545	690
R_1	Ω	10.3k	15.4k
R_2	Ω	11k	12.1k

Figure 6.1: Simulated and measured S21 response for Amplifier

To further investigate this behavior, break-out circuits were added for stand alone inductors and included in the final layout (Figure 6.4). These measured responses were compared to simulated structures in *HP Momentum* [88] in Table 6.2.1. Similar to the complete DA, all transmission line effects and losses were accounted for modelling metal interconnect lines as transmission lines.

Due to a DC voltage drop in the transmission line, the DC bias on each gain stage will vary and was compensated in our design. The measured input and output matching was also plotted versus simulated results and can be seen in Figure 6.3.

Figure 6.2: Total capacitance seen at the FET's Drain

Figure 6.3: Input matching plot for Distributed Amplifier

S_{11} measurements agree with simulation results over the entire range suggesting good accuracy in both the transistors and transmission line models.

The noise vs. frequency dependence of this circuit also suggest possible use of this amplifier as a broadband LNA in the region of 1 - 3 GHz, where the noise figure drops below 2 dB (Figure 6.5).

Microwave measurements were carried out using the Agilent 8720ES s-parameter network analyzer on a Cascade Microtech 9000 Analytical Probe station.

Figure 6.4: Distributed Amplifier Layout

Figure 6.5: Noise Figure

6.3 A 1-27 GHz Distributed Amplifier in 0.18 μm CMOS

This section will describe the design of a distributed amplifier which operates from 1 - 27 GHz. This amplifier exhibits a measured gain of 6 dB and uses coplanar waveguides to implement required inductances. Power consumption is 68.1 mW while driven from a 3.3V supply but it can operate with supply voltages as low as 1.8V. Chip area is 1.8 x 0.9 mm. Some design challenges present in the design of distributed amplifier have already been discussed in Chapter 2 and in the previous section of this chapter.

6.3.1 CPW modeling

To minimize the losses associated with the underlying silicon substrates, we rely on the use of coplanar waveguides. The ground plane of the transmission line is elevated and placed in the same plane of reference as the signal line. As a result losses due to field penetration into the Si substrate are minimized. A cross section of the fabricated CPWs is shown in Figure 6.6. Design considerations for CPWs were presented in Chapters 2 and 3.

Figure 6.6: Cross section of fabricated CPWs

CPWs were designed by using the conformal mapping technique suggested by Collin (See Appendix C.1.2) [96], but design parameters such as the characteristic impedance and electrical length as shown in Fig 6.7, were refined using packages such as Agilent's Linecalc and Momentum [88].

The line attenuation was also simulated in Agilent Momentum and plotted as a function of line impedance (Fig. 6.8)

Figure 6.7: CPW Z_0 as a function of Width (W) and Spacing (S)

Figure 6.8: S_{21} as a function of line impedance Z_0

Although high levels of impedance are desired for low voltage circuit operation (less current for the same voltage swing) or higher small-signal gain, it can be seen in Figure 6.8 that impedance levels higher than 80Ω are impractical since they will yield large line attenuation values reducing the usable length of the CPW and therefore the achievable inductance at a given frequency.

6.4 Quasi-TEM model

CPWs were modelled using a distributed circuit Quasi-TEM approach. The basic circuit element is shown in Fig. 6.9. Series resistance R_{ser} results mainly from the resistance of the metal interconnect, while conductance G_{sub} results primarily from losses due to field line penetration into the conductive silicon substrate.

Figure 6.9: Quasi-TEM distributed circuit used to model CPWs in silicon

By cascading multiple Quasi-TEM distributed elements more accuracy is achieved. It is desired to have both model accuracy and reduced circuit complexity when modeling CPWs. Figure 6.10 shows the accuracy of modeling an EM structure by using 1 versus 4 distributed elements.

Figure 6.10: S_{11} model fit to EM simulations as a function of the number of Quasi-TEM distributed circuit elements

6.5 CPW Measurement

The CPWs are fabricated through a commercial $0.18\mu\text{m}$ CMOS technology (see Figure 6.12). This process uses a substrate resistivity of approximately $10\ \Omega\text{-cm}$. Top metal is $2\ \mu\text{m}$ thick and placed approximately $6\ \mu\text{m}$ above the substrate. Bottom metal is $0.5\ \mu\text{m}$ thick and placed $0.5\ \mu\text{m}$ above the substrate (Fig. 6.6).

The final fabricated CPW can be seen in Figure 6.12. The effect of the test pad and discontinuities between the lines are removed through de-embedding techniques. This starts with measured s-parameters which are converted to their corresponding ABCD parameters. We can express the ABCD parameters of a transmission line as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma d) & Z_0 \sinh(\gamma d) \\ \frac{\sinh(\gamma d)}{Z_0} & \cosh(\gamma d) \end{bmatrix} \quad (6.2)$$

where the complex propagation constant can be expressed as $\gamma = \alpha + j\beta$. Both the complex propagation constant and the line impedance Z_0 can be expressed in terms of its corresponding ABCD parameters as follows:

$$\gamma = \frac{\text{acsh}(A)}{d} \quad (6.3)$$

$$Z_0 = \sqrt{\frac{B}{C}} \quad (6.4)$$

here d corresponds to the ABCD one step de-embedding length, which can be calculated by using two CPWs as follows:

- Use a long CPW (e.g. $l_1 = 0.7$ mm)
- Use a short CPW (e.g. $l_2 = 0.2$ mm)
- $\text{ABCD}_{\text{final}} = \text{ABCD}_{\text{long}} - \text{ABCD}_{\text{short}}$
- Calculate $d = l_1 - l_2 = 0.5$ mm

Measured results for two CPWs with Z_0 of 50Ω and 80Ω were compared to EM simulations and are in good agreement as shown in Fig. 6.11.

Figure 6.11: Measured Z_0 for CPWs with various impedance levels

To minimize the losses associated with the underlying silicon substrates, we rely on the use of coplanar waveguides. The ground plane of the transmission line is elevated and placed in the same plane of reference as the signal line. As a result losses due to field penetration into the Si substrate are minimized (See Figure 6.12).

Figure 6.12: Coplanar waveguide layout and structure, showing $\vec{E}$ field lines

CPWs were designed by using the conformal mapping technique suggested by Collin [96], but design parameters such as the characteristic impedance and electrical length were refined using packages such as Agilent's Linecalc and Momentum [88]. Although (2.32) suggests that for a distributed amplifier, Z_0 should be as high as possible, this will increase field line penetration into the substrate increasing the losses. The characteristic impedance used for both artificial transmission lines was equal to 80Ω . It is also important to design CPW with high self-resonant frequency f_{self} , such that the useful bandwidth over which the inductance remains constant is at least equal to the bandwidth of the distributed amplifier (The useful bandwidth will be somewhere between $\frac{1}{3}f_{self}$ and $\frac{1}{2}f_{self}$). Fig 6.13 shows the frequency response (Momentum simulation) of a $500\mu\text{m}$ CPW line, which suits the needs of this amplifier.

Figure 6.13: Inductance and Q-factor as a function of frequency for a 500 μm long CPW

6.5.1 Circuit Design and implementation

The following is a list of some of the design difficulties that were addressed during the implementation of this distributed amplifier:

- Gain peaking was controlled by using the staggering technique[69].
- Stability required low gate-to-drain capacitance C_{gd} which is dependant on V_{DS} . This was ensured with sufficiently high V_{ds} [97].
- Line termination was achieved using m-derived half-sections [1].
- EM simulators were used to characterize the coplanar waveguides in order to minimize losses at high frequencies. These results were then incorporated into circuit simulation.
- Transistor sizes vary along the gain stages in this amplifier to compensate for the variation in DC bias for each stage. Affected parameters are g_m , C_{gs} and C_{ds} .

By calculating the optimum number of stages and using the CPW design parameters, the optimum number of stages was calculated to be equal to 4. Then

using (2.32) and the calculated 4 gain stages, the required transistor size and biasing was calculated. Circuit design was implemented using the *Spectre RF* circuit design environment in Cadence and using the models provided by the foundry. Layout implementation for the CPW was imported into Agilent's Momentum using the GDSII format and an EM simulation performed on the final layout views for the CPW, including vias and metal interconnects.

6.5.2 Measurements

S-parameter measurements were carried out using the Agilent 8722ES s-parameter network analyzer on a Cascade Microtech 9000 Analytical Probe station. The complete layout for this circuit can be seen in Figure 6.14.

The S21 response comparison for this amplifier with and without pad parasitic extraction is shown in Fig 6.15 exhibiting passband gain of about 6 dB from 1-27 GHz.

As shown in Figure 6.16, the supply voltage could be lowered to 1.8V and the power dissipation drops to 39.6 mW, while still achieving gain. This would still provide adequate gain for a distributed oscillator [98].

The measured input and output matching was also plotted versus simulated results and can be seen in Figure 6.17 with a return loss better than 10 dB over the entire bandwidth. The group delay for this amplifier is also shown in Figure 6.19.

Large signal IP3 performance was measured using the 8593E Spectrum Analyzer and simulated input referred P_{1dB} compression point was compared with simulated results(Figure 6.18). A summary for the response of this amplifier is presented in Table 6.5.2.

The distributed amplifier results obtained in this work were compared to others available in literature and shown in Figure 6.20. The maximum frequency of operation of the distributed amplifiers was plotted for various state of the art CMOS technologies. Each result correspond to references provided at the end of this thesis work.

Figure 6.14: Distributed Amplifier Layout

Figure 6.15: Simulated and measured S21 response including pad extraction

Figure 6.16: Measured gain as a function of the supply voltage V_{dd}

Figure 6.17: Input and Output matching plot for Distributed Amplifier

Figure 6.18: Measured and Simulated input referred 1 dB compression point

Figure 6.19: Measured distributed amplifier group delay

Table 6.3: Summary of Results

	27GHz CMOS Distributed Amplifier
Technology	CMOS 0.18 μ m
Bandwidth	1 - 27 GHz
Gain	6 $\pm$ 1 dB
Noise Figure	6 dB @ 5 GHz
Input P_{-1dB}	4 $\pm$ 1 dBm
Chip Area	1.8 $\times$ 0.9 mm
Power Consumption	68.1 mW @ $V_{dd} = 3.3V$ 39.6 mW @ $V_{dd} = 1.8V$

Figure 6.20: Comparison of maximum frequency of operation for distributed amplifiers presented in this work vs. results available in literature for various state of the art CMOS technologies

As shown in Figure 6.20, the distributed amplifier presented here and using CPWs shows the highest frequency of operation for an amplifier implemented in standard CMOS technologies using cascode gain stages (0.18 μ m CMOS from TSMC)

6.6 Gain and bandwidth tuning in distributed amplifiers

A new distributed amplifier structure is discussed in this section with tunable gain and bandwidth, as follows:

- **Gain Control:** Achieved by using a cascode gain cell. As the bias of the cascode transistor is changed, the gain can be varied while the bandwidth is not disrupted.
- **Bandwidth Control:** Integrated varactors are added to the output to each one of the gain stages in the distributed amplifier. The delay of the output artificial transmission line is varied, changing its achievable bandwidth, while maintaining a relatively constant gain.

Figure 6.21 shows a circuit schematic of one of the gain cells used to implement the distributed amplifier with variable gain and bandwidth.

Figure 6.21: Gain stage showing gain and bandwidth control input

6.6.1 System setup

To investigate the controllable structure, a test bench was constructed in Agilent ADS using TSMC CMOSp18 RF models as seen in Figure 6.22.

On Gain control mode, the cascode voltage was varied and results can be seen in Figure 6.23. Varying the cascode bias voltage reduces the output resistance of the gain cell reducing its gain.

Alternatively, we can vary the bandwidth control port and adjust the amplifier's frequency response as shown in Figure 6.24.

To aid in the design, it is important to understand the limitations and degradation of the artificial lines when varactors are added for bandwidth control. Next we present the varactor modeling of the structures investigated in this work.

6.6.2 Varactor Modeling

The varactors used in this work were modeled using Agilent ADS and using a $0.18\mu\text{m}$ TSMC CMOS process. Simulation Results are shown in Figure 6.25.

Figure 6.25a) shows the system level test used to study the varactors. Figure 6.25b) shows the varactor's quality factor Q as a function of frequency. As expected the frequency variable impedance of the capacitor reduces the varactor's Q as frequency increases, for frequencies of 20 GHz, the varactor's $Q \approx 104$.

By using the CPW quality factor results of Figure 6.13 and our modeled varactor's Q we can estimate the Q degradation as a result of the use of varactors as follows: since the Q of the transmission line is 25, the combined Q can be calculated to be 20.15.

The degradation in the quality factor of the artificial transmission line is minimized when small varactors with Q larger than 100 are used.

The Varactor's effective capacitance is varied by adjusting the bandwidth control port of Figure 6.21 and results are shown in Figure 6.25c) and 6.25d).

6.7 Summary

In this chapter two fully integrated CMOS distributed amplifiers have been shown. The first one using an old technology $0.35\mu\text{m}$ CMOS, achieved a 5.5 GHz bandwidth.

Figure 6.22: Test bench used to simulate distributed amplifier with gain and bandwidth control

Figure 6.23: Gain and Bandwidth response vs. frequency while varying gain control port

Figure 6.24: Gain and Bandwidth response vs. frequency while varying bandwidth control port

Figure 6.25: Varactor modeling: a) ADS setup, b) Varactor's Q as a function of frequency, c) Varactor's Quality factor as a function of control voltage, d) Varactor Effective Capacitance C_{eff} as a function of control voltage

Results from a commercially available planar EM simulator [88] were in agreement with measured results and offer an accurate method to predict the broadband response of inductors in lossy silicon substrates. M-derived sections were used to accurately match the amplifier over the entire bandwidth and, compared to long k sections, they reduced the circuit complexity and size. Design guidelines were presented to aid a designer in minimizing losses during the design of a fully-integrated distributed amplifier as reinforcement of passive theory and distributed amplifier theory previously introduced in Chapter 2. Where discrepancies were found between measurements and simulations, an attempt was made to explain these.

The second distributed amplifier exhibits a gain of about 6 dB and 27 GHz bandwidth, verifying that bandwidth is about 55% of f_T . Distributed Amplification, which has traditionally been dominated by III-V technologies and more recently by SiGe, is now feasible in CMOS. The use of coplanar waveguides increases the frequency of operation of this amplifier by minimizing losses due to field penetration into the substrate at high frequencies.

This is the highest measured bandwidth ever reported for a distributed amplifier implemented in standard CMOS technologies using cascode gain cells, and results agree with gain-bandwidth of a distributed amplifier fabricated in silicon presented in Chapter 5.

In this chapter a novel gain cell structure to be use in a distributed amplifier and which will enable gain and bandwidth tunability by the use of integrated varactors was discussed. A four stage distributed amplifier with gain-bandwidth control was demonstrated in this chapter using integrated varactors with quality factor of 104. The gain of this amplifier was 10 ± 4 dB while the amplifier's bandwidth was 24 ± 2 GHz.

Chapter 7

Conclusions

7.1 Summary

In this work we have shown that silicon based technologies have the potential to compete with GaAs and other III-V technologies for microwave wireless circuit applications in the 2 GHz to 40 GHz range. In Chapter 2, a silicon technology overview was presented in the context of microwave circuit design. Chapter 2 introduced silicon based passives, their design, limitations, and sources of loss. Also, a comparison of the most commonly used types of transmission lines in silicon was presented here. Due to the lossy nature of silicon substrates, coplanar waveguides (CPW) provide the best choice for broadband circuit design since the ground plane is raised to the level of the conductor plane. The importance of cross-talk isolation in silicon substrates at high frequencies was introduced in this chapter. The distributed amplifier was introduced as a useful circuit technique to maximize the frequency of operations of silicon technology.

Chapter 3 explored CPWs as the passive of choice for MMIC circuit design in silicon. In the processing area, alternative interconnect metals (particularly copper and silver) available in silicon were examined, which combined with the use of low-k dielectrics such as polyimide, have allowed for an improvement in CPWs implemented in silicon substrates. The post-process techniques presented in this chapter will improve the quality of passives in a purely digital silicon process by reducing metal losses and enhancing substrate isolation. In the circuit area, an optimized CPW structure with wavelength reduction and better noise immunity was presented with quality factor improvements of 30% compared to standard CPWs.

Unwanted on-chip signal coupling will affect system-on-chip designs and modeling of this phenomenon is crucial if single chip integration is desired. Techniques to measure coupling effects in the past have included the use of complicated and unreliable off-chip circuit calibration techniques. Chapter 4 presented a study of on-chip coupling between inductors and resonators in silicon substrates. Since it is difficult to suppress on-chip signal coupling completely, new techniques aimed at measuring this effect are presented here and their accuracy compared to numerical EM modeling.

Chapter 5 deals with advanced issues in the design of fully integrated silicon distributed amplifiers. A study of the gain-bandwidth limitations of distributed amplifiers was presented in this chapter. Previous studies to understand the gain-bandwidth limitations of distributed amplifier were only available for GaAs technologies with different processing issues.

Distributed amplification circuit implementation in silicon was presented in Chapter 6. Two examples were presented in this chapter, one aimed at producing high gain and the other aimed at achieving the highest possible bandwidth in this technology. Gain and bandwidth controllability of distributed amplifiers was also studied in this chapter using integrated varactors.

7.2 Thesis Contributions

In summary, this thesis has presented several contributions aimed at furthering the development of silicon MMICs.

1. Implementation of CPW based passive components using a post-process technique with copper and silver metalization [15], and also using low-k dielectrics, has been presented. The post-process technique requires only a simple set of fabrication equipment, of the kind commonly found in university research laboratories. While copper is available in some advanced standard commercial process, silver has not been reported [16, 17, 18]. Post-processing techniques are fully compatible with any pre-existing silicon integrated process and promises to add high performance passives to digital CMOS or bipolar technologies. Full characterization and modeling of Cu CPWs has been provided for frequencies up to 10 GHz [10, 11, 12, 13] and 40 GHz [14]. Previously this was available only up to 2 GHz [9]. Complete fabrication details can be seen in Appendix A.

2. A wavelength reduction technique for on-chip CPWs with better cross-talk immunity and low-loss was optimized [19]. This CPW wavelength reduction technique will provide circuit designers with the ability to implement much wider signal lines with reduced attenuation while still being able to achieve standard on-chip impedance levels (40Ω - 120Ω).
3. A novel calibration-free circuit technique aimed at measuring on-chip coupling in silicon MMICs has been presented here. This technique makes use of the injection locking properties of two identical VCO's placed on the same chip [24]. Measured coupling results agree with theoretical approximations within 1 dB and these results were used to validate circuit based coupling models [21, 22, 23]. The study of on-chip coupling mechanisms was extended also to include Si based CPWs, for frequencies up to 40 GHz.
4. An understanding of the bandwidth limitations of distributed circuits in silicon is presented. Previous analysis has only been available for GaAs devices and is not directly applicable to silicon as the lossy and complex silicon substrates pose additional challenges. The low performance of passives in silicon has been shown to be one of the limitations of distributed based circuits and via simulation work and a comparison to literature results [25], it was determined the ultimate bandwidth of the silicon based distributed amplifier is approximately 55% of the technology's f_{MAX} and not 80% as has been proposed for GaAs based circuits [94].
5. New breakthrough performances for silicon based distributed amplifiers have been reported in this work [8, 7, 26] as a validation of the theory and understanding of the previous four contributions. Distributed amplification has the potential of placing silicon technologies in direct competition with III-V technologies for microwave applications. Design guidelines aimed at minimizing losses in on-chip distributed amplifier have been presented and the use of CPW to implement passives in a silicon technology has pushed the frequency of operation of a CMOS distributed amplifier to 27 GHz, which is the highest frequency of operation for an amplifier implemented in standard CMOS technologies using cascode gain stages (0.18 μm CMOS from TSMC).

6. A new distributed amplifier using integrated varactors to provide gain and bandwidth control is discussed in this thesis. A four stage distributed amplifier with gain-bandwidth control was demonstrated in this thesis through simulation using integrated varactors with quality factor ≈ 100 . The gain of this amplifier was 10 ± 4 dB while the amplifier's bandwidth was 24 ± 2 GHz.

7.3 Future Work

Many areas covered in this thesis could be expanded for future research work:

1. The CPW wavelength reduction technique presented in Chapter 3 showed advantages over standard CPW structures in EM simulation. Another graduate student is incorporating the optimized wavelength reduction techniques presented in this thesis in order to improve the performance of Nonlinear Transmission Lines (NLTL) used for pulse shaping in wireless broadband applications [99]. By slowing down wave propagation, shorter CPWs with reduced attenuation are expected.
2. A calibration free technique for measuring on-chip coupling levels was presented in Chapter 4. During testing of this circuit, on-chip coupling levels were so strong that smaller offsets were difficult to measure, and the receiving oscillator became injection locked. In fact, coupling was so strong that using the high receiver gain of the oscillator, a crude measurement was made between oscillators mounted on two separate PCBs. With roughly 5 cm of separation between the PCBs and a frequency offset of 1 MHz the coupled tone was -40 dBc. This confirms the high sensitivity of oscillators to coupling and suggests that more work should be done to explore the feasibility of communication links between coupled resonators [100]. Other graduate students are currently exploring the use of oscillators such as the ones used in this work in order to implement ultra-low power transceivers in silicon.
3. An understanding of the noise limits of distributed based circuits in silicon is not available in the literature. Such study might increase the feasibility of distributed based circuits in ultra-wideband communications.

4. A new distributed amplifier gain stage with gain and bandwidth control was discussed in Chapter 6. This should be verified experimentally.

7.4 Summary of Publications

The following paper contributions are a direct result of this thesis work:

- [1] R. E. Amaya, N. G. Tarr, and C. Plett, "A 1-27 Fully Integrated CMOS Distributed Amplifier using Coplanar Waveguides," 2004 IEEE RFIC conference, Jun. 2004.
- [6] R.E. Amaya, C. Plett, "The Design of High Gain Fully Integrated Distributed Amplifier in CMOS," 2003 IEEE ESSCIRC conference, Sept. 2003.
- [8] R.E.Amaya and C. Plett and N.G.Tarr, "A 0.5-10.5 GHz CMOS Distributed Amplifier using Copper Inductors," Symposium on Microelectronics Research & Development (MR&DCAN), Sept. 2001.
- [9] R.E.Amaya and V. Levenets and N.G. Tarr and C. Plett, "Copper Coplanar Waveguides in Si Substrates for 10 GHz Applications," 11th Canadian Semiconductor Technology Conference, no. Th1.2, Aug. 2003.
- [10] R.E.Amaya and V. Levenets and N.G. Tarr and C. Plett, "Copper Coplanar Waveguides in Si and suitable for 10 GHz operation," 2003 Advance Metallization Conference (AMC), Oct. 2003.
- [11] R. E. Amaya, V. Levenets, C. Plett, and N. G. Tarr, "Copper Coplanar Waveguides in Si Substrates for 10 GHz Applications," Journal of Vacuum and Science Technology-A, May. 2004.
- [12] R. E. Amaya, V. Levenets, C. Plett, and N. G. Tarr, "Copper Coplanar Waveguides on Si Substrates for Frequencies up to 40 GHz," Symposium on Antenna Technology and Applied Electromagnetics, Jul. 2004.

- [13] V. Levenets and R. E. Amaya and N.G. Tarr and T.J. Smy, "PVD Silver as a Material of Choice for Microwave Passives in Silicon Technology," 205th Meeting of The Electrochemical Society, May. 2004.
- [14] V. Levenets and R.E. Amaya and N.G. Tarr and T.J. Smy and J.W.M. Rogers, "Characterization of silver CPWs for applications in silicon MMICs," IEEE Electron Device Letters, vol. 26, no. 6, pp. 357359, Jun. 2005.
- [15] V. Levenets and R.E. Amaya and N.G. Tarr and T.J. Smy, "Characterization of Silver CPWs for Applications in Silicon MMICs," 2004 Advance Metallization Conference (AMC), Aug. 2004.
- [16] V. Levenets, R. E. Amaya, N.G. Tarr, and T.J. Smy, "Silver coplanar waveguides as the passives of choice for microwave integrated circuits," Accepted for publication at the Journal of Vacuum and Science Technology, Feb. 2005.
- [18] R.E. Amaya and V. Levenets and N.G. Tarr, "Improved Coplanar Waveguides for Silicon RF ICs," Proceedings Micronet Annual Workshop, May. 2005.
- [19] R.E. Amaya, P. Popplewell, C. Plett, "EM and Substrate Coupling in Silicon RFICs," Accepted for publication to IEEE Journal of Solid-State Circuits, Feb. 2005.
- [20] P. Popplewell, R.E. Amaya, M. Cloutier, and C. Plett, "Calibration-Free On-Chip Inductor Coupling Experiment with Injection-Lockable VCOs," in IEEE Bipolar/BiCMOS Technology Meeting Conference, Sep. 2004.
- [21] R.E. Amaya, P. Popplewell, M. Cloutier, and C. Plett, "Analysis and Measurements of EM and Substrate Coupling Effects in Common RF Integrated Circuits," in IEEE Custom Integrated Circuit Conference, Oct. 2004.
- [22] P. Popplewell and R.E. Amaya and C. Plett and M. Cloutier, "Analysis and measurements of injection-lockable oscillators for high-gain, high-Q applications," IEEJ International Analog VLSI Workshop, pp. 35-40, Oct. 2004.

[23] R. E. Amaya, J. Aguirre, and C. Plett, "Gain Bandwidth Considerations in Fully Integrated Distributed Amplifiers implemented in Silicon," 2004 IEEE ISCAS conference, May. 2004.

[24] R.E. Amaya and Jorge Aguirre and C. Plett, "Design of Fully Integrated Distributed Amplifiers in Silicon Substrates," Proceedings Micronet Annual Work-shop (Winner of Best Paper Award), pp. 78, Sept. 2003.

Also, currently accepted for publication:

[TBP] V. Levenets, R. E. Amaya, N.G. Tarr, and T.J. Smy, "Application of PVD Silver for Integrated Microwave Passives in Silicon Technology," Accepted for publication at the IEEE Transactions on Advanced Packaging, Apr. 2005.

Appendix A

Copper fabrication

A.1 Post-process Cu fabrication detailed process flow

1. Metal Deposition

Aluminum evaporation $\approx 2\mu\text{m}$

2. PR processing ("Al shields" mask)

HMDS (1 krpm; 10 sec; 4 krpm; 30 sec)

HPR504 (1 krpm; 10 sec; 4 krpm; 30 sec)

Softbake (105 °C; 1 min)

Mask #1 Expose and Develop (50/50 MIF/DI: 1 min) and rinse (DI: 2 min)

Hardbake (3 min; 135 °C) Descum (1 min; 100 W; 0.3 Torr; oxygen plasma)

Expose time - 3-4 sec for VCO and 8 sec for underpath

3. Al wet etch

Hot phosphoric Acid (H_3PO_4 @ 60 °C) time: 6 - 8 min

DI rinse: 20 min

4. PR strip off

Microstrip 2001@ 90 °C; 10 min + 10 min)

DI rinse 30 min

5. Polyimide applying Adhesion promoter

Apply and wait 20 sec

Spin (3.5 rpm; 30 sec)

Soft bake (105 °C; 1 min) Polyimide (PI2611)

Apply and wait for 20 sec Ramp to 2.5 krpm; 30 sec; 3.0 krpm; sec. (6 mm)

Polyimide softbake 50 °C; 15 min; 100 °C; 30 min; 150 °C; 30 min VM651 should be stored at room temperature. (0.1-0.5 % in DI : 5 ml VM651: 1000 ml DI)

6. PR processing ("Contact windows" mask)

HMDS (1 krpm; 10 sec; 4krpm; 30 sec)

HPR504 (1 krpm; 10 sec; 4krpm; 30 sec)

Softbake (105 °C; 1 min)

Align (mask #2) Expose and Develop (1 min; 50/50 MIF/DI) and rinse (DI; 2 min)

Hardbake (3 min; 135 °C)

7. Polyimide wet etch

Develop (50/50 MIF/DI; 15 min) and rinse (DI; 2 min)

8. PR strip Acetone and rinse in DI

Descum (1 min; 100 W; 0.3 Torr; oxygen plasma)

9. Polyimide curing (NRC)

Ramp to 350 °C at a ramp rate of 4 °C/min

Cure for 30 min at 350 °C Cool down to ambient 9.1 Polyimide curing (CU)

Start (50 °C; 60 min)

Ramp rate 50 °C/hour until 100 °C

Ramp rate 10 °C/hour until 250 °C 2 hours at 250 °C OFF/cool down

10. PR HPR504

(1 krpm; 10 sec; 4 krpm; 30 sec)

Soft bake (1 min @ 105 °C) Hard bake (2 min @ 135 °C)

11. Ti deposition

e-beam, 2000 Å

12. PR processing ("Seed layer" mask)

HMDS (1 krpm; 4 krpm)

HPR504 (1 krpm; 4 krpm)

Softbake (105 °C; 1 min)

Align (mask #3)

Expose (6.5 sec)

Develop (50/50 MIF/DI; 1 min) and rinse (DI; 2 min) No hardbake!

Descum (1 min; 100 W; 0.3 Torr; oxygen plasma)

13. Titanium etch (HF/Nitric)**14. Flood exposure (20 sec)**

Develop (50:50) - 3-4 times

15. Plasma Etch

(0.5 T; 300 W; 4 min; oxygen plasma)

16. Seed layer formation (sputtering)

SputterEtch Ti: 300 Å (adhesion layer) Cu: 1000 Å (seed layer) Al: 300 Å
(protection layer)

17. Lift-off

Cold Acetone in Ultrasonic (10 min; 20 min)

Rinse in alcohol (10 min)

18. Copper plating

Approximate thickness of 2 μm

Appendix B

Microwave Measurements in CMOS substrates

B.1 Measured Parameter extraction

B.1.1 Passive de-embedding

When measuring a passive device pads, feed lines and other components used to facility on-wafer probing of the device are included into these measurements. De-embedding allow us to extract the parasitics for the Device Under Test (DUT) such that only the desired device performance is analyzed. One method used for inductor de-embedding is the one proposed by Cho [101] and originally intended for the de-embedding of transistors. Consider the Figure B.1.

Figure B.1: Passive device equivalent circuit before de-embedding and including pads and feed line parasitics proposed by Cho

where the Passive device correspond to the DUT for this experiment. We require S-parameters for three structures in order to accurately de-embed this structure: device, open and short. The information extracted from the open structure should provide information about the shunt parasitics G1 and G2 if converted to Y-parameters.

$$Y_{11open} = G1 + G3 \quad (B.1)$$

$$Y_{22open} = G2 + G3 \quad (B.2)$$

$$G3 = -(Y_{21open} + Y_{12open})/2 \quad (B.3)$$

G1, G2 and G3 can be easily removed by the use of the the three previous equations. We also assume that the impedance presented by Z1 and Z2 is much smaller that the one presented by G3.

$$Y_{11a} = Y_{11total} - G1 \quad (B.4)$$

$$Y_{22a} = Y_{22total} - G2 \quad (B.5)$$

$$Y_{12a} = Y_{21a} = Y_{21total} \quad (B.6)$$

The subscript “a” denotes that Y parameter do not include G1 and G2. By shorting the signal ports to ground we remove the effect of G3 and we can now look at the input impedance looking into both ports

$$Z1 = (Y_{11short} - G1)^{-1} \quad (B.7)$$

$$Z2 = (Y_{22short} - G2)^{-1} \quad (B.8)$$

the series impedances, Z1 and Z2 are removed by subtraction

$$Z_{11b} = Z_{11a} - Z1 \quad (\text{B.9})$$

$$Z_{12b} = Z_{12a} \quad (\text{B.10})$$

$$Z_{21b} = Z_{21a} \quad (\text{B.11})$$

$$Z_{22b} = Z_{22a} - Z2 \quad (\text{B.12})$$

Again, the subscript “b” refers to the passive device without G1, G2, Z1 and Z2. The Y-parameters for the DUT by itself are found by adding or subtracting G3.

$$Y_{11DUT} = Y_{11b} - G3 \quad (\text{B.13})$$

$$Y_{12DUT} = Y_{12b} + G3 \quad (\text{B.14})$$

$$Y_{21DUT} = Y_{21b} + G3 \quad (\text{B.15})$$

$$Y_{22DUT} = Y_{22b} - G3 \quad (\text{B.16})$$

A second de-embedding method was derived from Koolen [102]. This method uses a two terminal measurements and the equivalent circuit for the DUT including pads and feed lines can be seen in Figure B.2

Figure B.2: Passive device equivalent circuit before de-embedding and including pads and feed line parasitics proposed by Koolen

The Y parameter for the DUT can be extracted directly due to the position of G3 which simplifies analysis

$$Y_{DUT} = [(Y_{total} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1}]^{-1} \quad (\text{B.17})$$

B.1.2 Parameter extraction of Transmission Lines

Having de-embedded the measured s-parameters, we are now in a position to extract some model parameters for inductors. To help our analytical extraction. To ease calculations, we first convert the de-embedded s-parameters into its corresponding ABCD parameters:

$$A = \cosh(l\gamma) = \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} \quad (\text{B.18})$$

$$B = Z_0 \sinh(l\gamma) = \frac{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}{2S_{21}} \quad (\text{B.19})$$

$$C = \frac{1}{Z_0} \sinh(l\gamma) = \frac{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}{2S_{21}} \quad (\text{B.20})$$

$$D = \cosh(l\gamma) = \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{2S_{21}} \quad (\text{B.21})$$

where $l\gamma$ represents the product of the propagation length and complex propagation constant. We only need to know the value of the product of this two quantities as our analysis will assume, which is advantageous since the transmission line actual physical length need not to be known.

$$l\gamma = \cos^{-1} \left[\frac{A + D}{2} \right] \quad (\text{B.22})$$

Similarly, the characteristic impedance Z_0 can be extracted as follows:

$$Z_0 = \frac{B}{\sinh(l\gamma)} \quad (\text{B.23})$$

B.1.3 CPW 1-step de-embedding

If two identical CPW are placed on-chip with different lengths, one could take advantage of the cascade properties of using ABCD parameters and de-embed structure in one step. First we can express the ABCD parameters of a transmission line as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma d) & Z_0 \sinh(\gamma d) \\ \frac{\sinh(\gamma d)}{Z_0} & \cosh(\gamma d) \end{bmatrix} \quad (\text{B.24})$$

where the complex propagation constant can be expressed as $\gamma = \alpha + j\beta$. both the complex propagation constant can be express in terms of its corresponding ABCD paramters as follows:

$$\gamma = \frac{\text{acsh}(A)}{d} \quad (\text{B.25})$$

$$Z_0 = \sqrt{\frac{B}{C}} \quad (\text{B.26})$$

where d correspond to the ABCD one step de-embedding:

- Use long CPW (e.g. $l_1 = 1.25$ mm)
- Use short CPW (e.g. $l_2 = 0.25$ mm)
- $d = l_1 - l_2 = 1.0$ mm

The line attenuation can also be expressed as follows:

$$\alpha(\text{in dB}) = 8.688 \Re(\gamma) \quad (\text{B.27})$$

Finally, other parameters could be extracted as follows:

$$\epsilon_{\text{reff}} = \left(\frac{\tau}{cd} \right)^2 \quad (\text{B.28})$$

$$\tau = \frac{\partial \beta}{\partial \omega} \times d \quad (\text{B.29})$$

where $c = 3 \times 10^8$ m/s

B.1.4 Parameter extraction of microwave MOSFETs

If we consider the circuit shown in Figure , it can be then derived that the Y parameters for this two port network are equivalent to

$$Y_{11} = \frac{I_1}{V_1} = \frac{j\omega(C_{gs} + C_{gd})}{1 + j\omega(C_{gs} + C_{gd})R_g} \quad (B.30)$$

$$Y_{12} = \frac{I_1}{V_2} = \frac{-j\omega C_{gd}}{1 + j\omega(C_{gs} + C_{gd})R_g} \quad (B.31)$$

$$Y_{21} = \frac{I_2}{V_1} = \frac{g_m - j\omega C_{dg}}{1 + j\omega(C_{gs} + C_{gd})R_g} \quad (B.32)$$

$$Y_{22} = \frac{I_2}{V_2} = g_{ds} + \frac{j\omega C_{jd}}{1 + j\omega C_{jd}R_{subd}} + j\omega C_{sd} + j\omega C_{gd} + \quad (B.33)$$

$$\frac{\omega^2 C_{gd}C_{dg}R_g + j\omega g_m C_{dg}R_g}{1 + j\omega(C_{gs} + C_{gd})R_g} \quad (B.34)$$

Figure B.3: MOSFET Equivalent Circuit Model

It can be shown that using Y parameters, the microwave parameters of a MOSFET can be derived as follows:

$$g_t = \Re[Y_{21}]|_{\omega^2=0} \quad (\text{B.35})$$

$$g_{ds} = \Re[Y_{22}]|_{\omega^2=0} \quad (\text{B.36})$$

$$R_g = \Re[Y_{11}]/(\Im[Y_{11}])^2 \quad (\text{B.37})$$

$$C_{gd} = -\Im[Y_{12}]/\omega \quad (\text{B.38})$$

$$C_{gs} = (\Im[Y_{11}] + \Im[Y_{12}])/\omega \quad (\text{B.39})$$

$$C_{dg} = -\Im[Y_{21}]/\omega - g_m R_g (C_{gs} + C_{gd}) \quad (\text{B.40})$$

B.2 Inductor Modelling using HSPICE

Once s-parameter data has been collected from an electromagnetic simulator package such as Momentum, HFSS or Sonnet, it can be imported into HSPICE for parameter fitting. A sample input netlist into HSPICE is shown below (Refer to Figure B.4):

Figure B.4: Inductor Model for HSPICE model fitting (nodes names also shown)

```
.option acct nomod post=2

.net v(p2) vin rout=50 rin=50

vin p1 0 AC 1

L      p1      3      Ls
R      3      p2      Rs
Cs1    p1      1      Cp1
Cs2    p2      2      Cp2
Rs1    1      0      Rp1
Rs2    2      0      Rp2
Cbr     p1     p2     Cbr
```

```

.param
+ Ls = OPT1(3.1n,.1n,100n)
+ Rs = OPT1(20,.1,10k)
+ Rp1 = OPT1(1.8,.1,100k)
+ Rp2 = OPT1(1.8,.1,100k)
+ Cp1 = OPT1(0.327p,.001p,10p)
+ Cp2 = OPT1(0.315p,.001p,10p)
+ Cbr = OPT1(.02p,.0001p,10p)

.AC data=measured optimize=opt1
+ results=comp1,comp2,comp3,comp4,comp5,comp6,comp7,comp8
+ model=converge
.model converge opt relin=1e-4 relout=1e-4 close=10 itropt=30
.measure ac comp1 err1 par(s11m) s11(m)
.measure ac comp2 err1 par(s11p) s11(p)
.measure ac comp3 err1 par(s12m) s12(m)
.measure ac comp4 err1 par(s12p) s12(p)
.measure ac comp5 err1 par(s21m) s21(m)
.measure ac comp6 err1 par(s21p) s21(p)
.measure ac comp7 err1 par(s22m) s22(m)
.measure ac comp8 err1 par(s22p) s22(p)
.ac data=measured
*.print par(s11r) s11(r) par(s11i) s11(i)
*.print par(s12r) s12(r) par(s12i) s12(i)
*.print par(s21r) s21(r) par(s21i) s21(i)
*.print par(s22r) s22(r) par(s22i) s22(i)
*.print z11(r) z11(i) z11(m) z11(p)
*.print z22(r) z22(i) z22(m) z22(p)
*.print z12(r) z12(i) z12(m) z12(p)
*.print z21(r) z21(i) z21(m) z21(p)

.data measured
FREQ      s11m      s11p      s12m      s12p      s21m      s21p      s22m      s22p

1.000e+08  4.708e-02  2.126e+01  9.558e-01  -1.586e+00  9.558e-01  -1.586e+00  4.750e-02  21.59029
1.100e+09  2.093e-01  6.618e+01  9.166e-01  -1.709e+01  9.166e-01  -1.709e+01  2.085e-01  64.92491
2.100e+09  3.884e-01  5.874e+01  8.299e-01  -3.140e+01  8.299e-01  -3.140e+01  3.828e-01  57.20321
3.100e+09  5.369e-01  4.807e+01  7.175e-01  -4.427e+01  7.175e-01  -4.427e+01  5.250e-01  46.39028
4.100e+09  6.483e-01  3.809e+01  5.985e-01  -5.588e+01  5.985e-01  -5.588e+01  6.299e-01  36.3496
5.100e+09  7.243e-01  2.912e+01  4.804e-01  -6.622e+01  4.804e-01  -6.622e+01  7.002e-01  27.37482

.enddata
.param freq=100MEG,s11m = 0 , s11p = 0, s12m = 0, s12p = 0, s21m =0,
+s21p =0, s22m =0 , s22p = 0
.end

```

The output of the HSPICE input netlist will be saved in an output file of extension *.MA0 as follows:

```
$DATA1 SOURCE='HSPICE' VERSION='W-2004.09'
.TITLE '.option acct nomod post=2'
index      ls      rs      rp1
           rp2      cp1      cp2
           cbr      comp1    comp2
           comp3    comp4    comp5
           comp6    comp7    comp8
           temper   alter#
19.0000    3.819e-09  4.5936  462.0355
           366.4058  1.259e-13  1.407e-13
           5.215e-14  1.752e-02  1.565e-02
           1.627e-02  3.032e-02  1.627e-02
           3.032e-02  1.646e-02  1.108e-02
           25.0000   1.0000
```

Appendix C

Supplemental Microwave Theory

C.1 Microwave Network Theory

C.1.1 Image parameter method

The image parameter method may be applied to the distributed amplifier since it consist of a cascade of identical two-port networks forming an artificial transmission line. The image impedance Z_i for a reciprocal symmetric tow-port is defined as the impedance looking into port 1 or 2 of the two-port when the other terminal is also terminated in Z_i . This impedance is given by

$$Z_i = \sqrt{\frac{B}{C}} \quad (\text{C.1})$$

where the ABCD matrix of the two-port is given by

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} \quad (\text{C.2})$$

where $A=D$ by symmetry. The propagation constant for the current and voltage is given by

$$e^{-\gamma} = \sqrt{AD} - \sqrt{BC} \quad (\text{C.3})$$

Thus, wave propagation occurs if γ has an imaginary component. For the T-network shown in Figure C.1, the image impedance and propagation factors are given by

Figure C.1: T-section network

$$Z_i = \sqrt{Z_1 Z_2} \sqrt{1 + \frac{Z_1}{4Z_2}} \quad (\text{C.4})$$

$$e^{-\gamma} = 1 + \frac{Z_1}{2Z_2} + \sqrt{\frac{Z_1}{Z_2} + \frac{Z_1^2}{4Z_2^2}} \quad (\text{C.5})$$

C.1.2 Conformal Mapping Technique

Conformal mapping techniques can be used to determine the electrical parameters of a coplanar waveguide CPW. Details shown below,

Figure C.2: CPW cross section

For the CPW shown in Figure C.2 and implemented on a finite-thickness dielectric substrate. The width of the dielectric substrate is assumed to be infinite. The quasi-static parameters of this transmission line are given by [96]:

$$Z_0 = \frac{30\pi}{\sqrt{\epsilon_{re}}} \frac{K(k')}{K(k)} \quad (\text{C.6})$$

$$\epsilon_{re} = 1 + \frac{\epsilon_r - 1}{2} \frac{K(k')K(k_1)}{K(k)K(k'_1)} \quad (\text{C.7})$$

where

$$k = \frac{a}{b} ; k' = \sqrt{1 - k^2} \quad (\text{C.8})$$

$$k_1 = \sinh(\pi a/2b) / \sinh(\pi b/2b) ; k'_1 = \sqrt{1 - k_1^2} \quad (\text{C.9})$$

K denotes the complete elliptical integral of the first kind. An approximate expression for $K(k)/K(k')$ ($k' = \sqrt{1 - k^2}$) is given by:

$$\frac{K(k)}{K(k')} = \frac{K(k)}{K'(k)} = \frac{1}{\pi} \ln \left(2 \frac{1 + \sqrt{k}}{1 - \sqrt{k}} \right) , 0.5 \leq k^2 \leq 1 \quad (\text{C.10})$$

$$= \frac{\pi}{\ln \left(2 \frac{1 + \sqrt{k'}}{1 - \sqrt{k'}} \right)} , 0 \leq k^2 \leq 0.5 \quad (\text{C.11})$$

C.2 EM simulator theory

C.2.1 Overview of EM solver techniques

There are no analytical solutions or closed form expressions for many microwave applications requiring the need for numerical electromagnetics. In computational electromagnetics, the three major approaches are: the method of moment (MoM), finite element method (FEM) and finite difference time domain (FDTD) method.

- The MoM is based on integral equations and it converts an integral equation into a dense matrix equation. Then it solves the matrix equation through the direct (e.g., Gaussian elimination) method or iteration (e.g., conjugate gradient) method.
- The FEM is based on the Rayleigh-Ritz or Galerkin's procedure that converts Maxwell's equations or the wave equation into a sparse matrix equation. Although the matrix is sparse, its size is much larger than that from the MoM for the same problem.
- The FDTD is based on discretized Maxwell's two curl equations. The FDTD does not resort to matrix equations, but its march-on-time process requires giant computer memory and huge CPU time.

C.2.2 Overview of commercial EM simulators [103]

ADS Momentum

- Momentum (ADS 2002) - Agilent EEsof EDA
- Numerical Method: MoM
- Platforms: Windows and UNIX
- Features: Laterally open formulation.
- Arbitrary number of layers and ports.
- Dual formulation of voltage in a slot.

- Can mix slot and strip formulations in different layers in the same problem.
- Edge element meshing algorithm.
- Box enclosure can be added.
- Optional Empipe optimization module.
- Optional visualization module.
- Momentum RF (added in ADS 1.5):
- Quasi-static solver;
- Star-loop basis functions for low frequency stability;
- Mesh reduction with polygonal cells.
- Comments: Polygons are recombined before meshing; makes it hard to manually control the mesh. Mesher recognizes standard discontinuities, applies predetermined meshing rules.

Sonnet

- em 8.0 - Sonnet Software
- Numerical Method: MoM
- Platforms: Windows and UNIX
- Features: Closed box formulation.
- Number of layers and ports limited only by memory and time.
- Diagonal elements, calibrated internal ports, and dielectric bricks.
- Bulk conductivity for semiconductor substrates.
- Optimization and parametric analysis.
- Optimization of netlist / geometry projects.

- Fast sweep (Adaptive Band Synthesis)
- Support modules for viewing currents and antenna patterns.
- 3rd party module for viewing geometry in 3D.
- Comments: One of the first tools available in this class. Free version with reduced capabilities is available.

HFSS

- Ansoft HFSS 9.0 - Ansoft
- Numerical Method: FEM
- Platforms: Windows and UNIX
- Features: Arbitrary geometry and resolution.
- Tetrahedral edge elements; closed box formulation.
- Second order absorbing boundary conditions (ABCs).
- Perfectly matched layers (PMLs).
- ACIS-based 3D modeler.
- True-surface object modeling is an option.
- Optimization capability added (V8.0).
- Eigenmode-solver added (V8.0).
- Dual processor support (V8.0).
- Macro approach in editor, basic object info is lost.
- Modes-to-nodes feature added (V8.0).
- Comments: Ansoft HFSS 9.0 introduced a completely new interface.

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