A 20kHz Frequency Resolution DCO

By

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Abstract

This thesis presents a Digitally Controlled Oscillator (DCO) design and implementation with its fine tuning band controlled by a Dynamic Element Matching (DEM) technique. All the components of the system are designed in 0.13μm IBM technology. The DCO output frequency ranges from 108MHz to 135MHz. The coarse tuning has 256 tuning levels and the fine tuning has 32 tuning levels resulting in an 8192 level (256 x 32) capacitance selection. The relative process variations that define the capacitors' discrepancies from each other on the same chip are between 0.2% and 0.5% of the absolute capacitor value. These discrepancies have a significant effect on the frequency resolution, especially for small capacitor steps. The proposed DEM technique reduces the process variations and mismatches in the small capacitor deltas used for fine tuning. The measurement results show that a 20kHz frequency resolution can be achieved over process variations. It is proved that the output frequency resolution is improved by dithering among different capacitor groups. The DCO core consumes 1.455mA current from a 1.185V voltage supply. The capacitor dithering introduced extra phase noise to the oscillator. Far out phase noise introduced by dithering cannot be filtered out by a PLL.

Acknowledgements

Firstly, I would like to express my gratitude to my supervisor, Professor Ralph Mason, for his encouragement and support. I appreciate the amount of time Prof. Mason has spent on helping me design and test the chip. The completion of this thesis would not have been possible without his help. Secondly, I would like to thank Prof. Plett and Prof. Rogers who laid a good foundation for me on my fourth year project which preceded my Master's thesis.

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List of Abbreviations

DCO	Digitally Controlled Oscillator
DEM	Dynamic Element Matching
PVT	Process Voltage Temperature
CP	Charge Pump
ADPLL	All Digital Phase Locked Loop
PLL	Phase Locked Loop
VCO	Voltage Controlled Oscillator
PFD	Phase Frequency Detector
LPF	Low Pass Filter
MMD	Multimodulus Divider
CMOS	Complementary- Metal- Oxide- Semiconductor
MIM	Metal-Insulator-Metal
MOM	Metal-Oxide-Metal
PN	Phase Noise
CV	Capacitance versus Voltage
CCCS	Current Controlled Current Source
INL	Integral Non-Linearity
DNL	Differential Non-Linearity

PCB-TF2	Printed Circuit Board Test Fixture 2
PRBS	Pseudo Random Binary Sequence
DRC	Design Rule Check
LVS	Layout Versus Schematic
LSB	Least Significant Bit
MSB	Most Significant Bit
IC	Integrated Circuit
CFP	Ceramic Flat Pack
PFD	Phase Frequency Detector
CP	Charge Pump
LPF	Low Pass Filter
INL	The Integral Nonlinearity

Chapter 1: Introduction

1.1 Chapter Overview

The introduction focuses on the background information, motivation and technical contributions. It also specifies and outlines the thesis organization.

1.2 Motivation

With the rapid development of the integrated circuit industry, analog Phase Locked Loops (PLLs) have been widely used in many frequency synthesizers [10]. However, analog PLLs are difficult to integrate and not easily portable to different process technologies. In addition, as supply voltages continue to decrease with advanced CMOS technologies, it becomes more challenging to design the analog components of the PLL such as the Charge Pump (CP). To overcome these difficulties, the All Digital Phase Locked Loop (ADPLL), - a counterpart of analog PLL, has been developed. In the ADPLL, the Voltage Controlled Oscillator (VCO) is replaced by the DCO (Digitally Controlled Oscillator). The DCO is directly controlled by a digital loop filter, thus the charge pump and loop filter required in the analog PLL can be eliminated [55].

A key component of the ADPLL is the DCO. Some of the DCO main parameters are the center frequency, the frequency tuning range, frequency resolution, power consumptions, phase noise and spurious content. Ideally, a DCO will provide a large

frequency tuning range with high frequency resolution. In many oscillator designs [18, 19, 20, 55, 56], the combination of coarse frequency tuning and fine frequency tuning is employed to increase the frequency tuning range. In integer N ADPLLs, the DCO output frequency can be controlled by capacitor tuning [55]. Therefore, high frequency resolution usually means increasing the number of binary weighted switch capacitor groups in the fine tuning band. However, the fine frequency steps will be strongly affected by capacitor process variations and mismatches, particularly as the capacitor sizes are reduced to increase frequency resolution. One approach that can be used to mitigate this effect is the use of Dynamic Element Matching (DEM) to control the DCO fine tuning band [30]. The use of DEM allows for pseudo random access to different groups of similar capacitors, thereby reducing process variations and mismatches. As a result, small capacitor deltas can be used to achieve a high frequency resolution. In an ADPLL, the dithering will result in a smaller DCO output frequency deviation. Therefore, it is easier for the PLL feedback signal to track the reference signal than without dithering.

1.3 Thesis Focus

This thesis focuses on the use of small deltas between capacitors combined with DEM to reduce process variations and achieve high frequency resolution in a DCO. A tree-structured digital encoder is used as the DEM block. An off-chip inductor is used in this oscillator design to offer high Q and reduce power consumption.

Although this thesis mainly focuses on the fine tuning capacitor bank and DEM implementation of the DCO, Voltage Controlled Oscillators (VCOs) will also be

discussed to compare the advantages and disadvantages of the DCO designed in this thesis.

1.4 Contributions

The major research contribution of this thesis is the implementation of a low power, high frequency resolution DCO. This is the first implementation of DEM applied to capacitor deltas. The capacitor deltas can be averaged out by randomly accessing different unit size capacitors. The equivalent capacitor deltas are reduced to $\frac{1}{\sqrt{n}}$ with n unit capacitors to be used for dithering. With reduced unity capacitor deltas, small step capacitance can be used. Therefore, this thesis presents an architecture suitable for high frequency resolution oscillators by implementing small step capacitance. The oscillator phase noise behaviour is analyzed at different dithering rates, different fine tuning codes and different oscillator output frequencies. The architecture is not limited to the 0.13μm technology or 32-level tree structured decoder. The benefits of the DEM can be enhanced in the implementation of more complicated tree structured decoders and more advanced technologies.

1.5 Thesis Organization

This thesis contains six chapters.

Chapter 1 introduces the concepts of ADPLLs and DCOs.

Chapter 2 provides an overview of PLLs, including analog PLLs and ADPLLs.

Chapter 3 discusses the differences between Voltage Controlled Oscillators and Digitally Controlled Oscillators; Dynamic Element Matching is also discussed.

Chapter 4 details the design and analysis of the Digitally Controlled Oscillator. The tolerance of capacitor process variations is also discussed.

Chapter 5 provides the measurement results. The differences between simulated and measured results are also discussed.

Chapter 6 presents the conclusion drawn from this work. Future research ideas and suggestions to overcome problems encountered in the chip testing are also discussed.

Chapter 2: Analog Phase Locked Loop and All Digital Phase Locked Loop

2.1 Introduction

This chapter aims to give an overview of PLLs. The analog PLL and the ADPLL are introduced to provide background information for the following chapters. Also, a good understanding of the oscillator performance in PLLs is essential to build a functional DCO. Section 2.2 describes common analog PLL components and their transistor level circuits. Section 2.3 describes basic PLL parameter calculations. Section 2.4 describes PLL noise analysis. Section 2.5 describes the All Digital Phase Locked Loop (ADPLL) and its component functionalities.

2.2 Analog Phase Locked Loop and Components Functionality

The PLL is a feedback system that forces the output frequency to follow the reference frequency [5]. The loop normally contains a Phase Frequency Detector (PFD), Charge Pump (CP), Low Pass Filter (LPF), VCO and Divider. The simplified analog PLL block diagram is shown in Figure 2.1 [1]. The PLL output frequency is N times larger than the reference frequency. The N can be either an integer number or a fractional number which depends on the divider's division ratio. The PFD is used to detect output phase/frequency to input phase/frequency difference. A PFD sends up/down signals to the CP to charge or

discharge the CP. Since there is always some difference on the up or down current sources, small current pulses will be injected into the loop filter and these pulses will be integrated by the LPF. The LPF is a linear function that controls the PLL transient response, stability and settling time. The VCO will produce an output frequency proportional to the control voltage passed by the LPF, and this signal will be divided down to the reference frequency. The reference frequency is commonly produced by a crystal oscillator that can supply an extremely accurate frequency to the loop. Generally, this reference frequency is not tunable [2, 3].

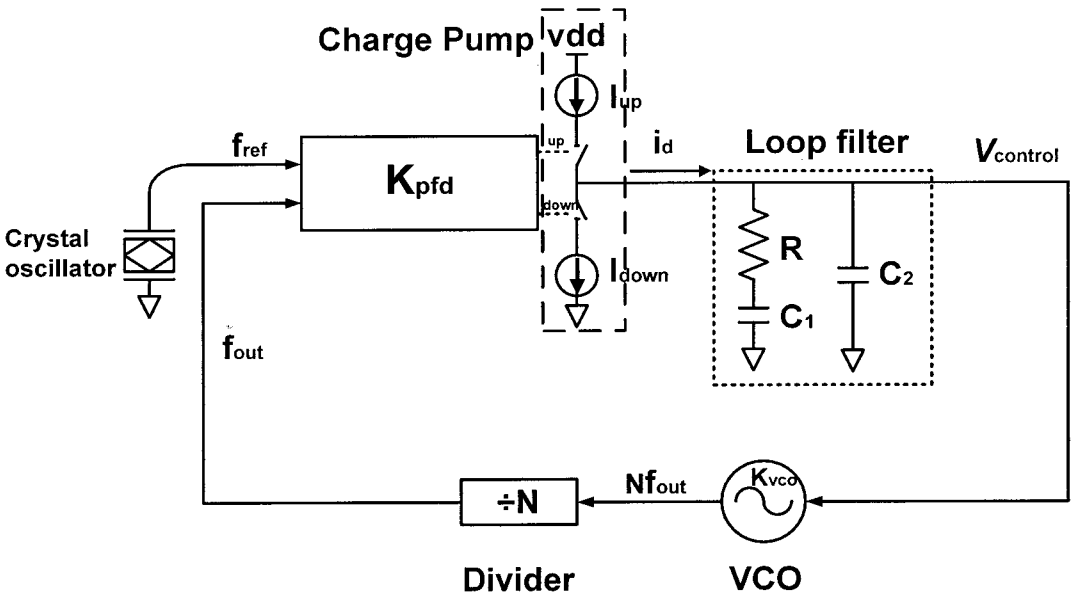


Figure 2.1: The Simplified PLL Block Diagram

2.2.1 VCO

The VCO will ideally have an output frequency proportional to the control voltage as shown in Figure 2.2 [4] where V_c is the control voltage, K_{VCO} is the VCO tuning sensitivity or gain in rad/sec/volt, and ω_{nom} is the oscillator nominal free running

frequency. The control voltage V_{c_nom} is the nominal control voltage corresponding to the VCO nominal frequency. Therefore, the osillator output frequency can be written as:

$$\omega_o = \omega_{nom} + K_{VCO}V_c \tag{2.1}$$

It should be noted that Vc can be a negative voltage so that it can generate frequencies less than ω_{nom}.

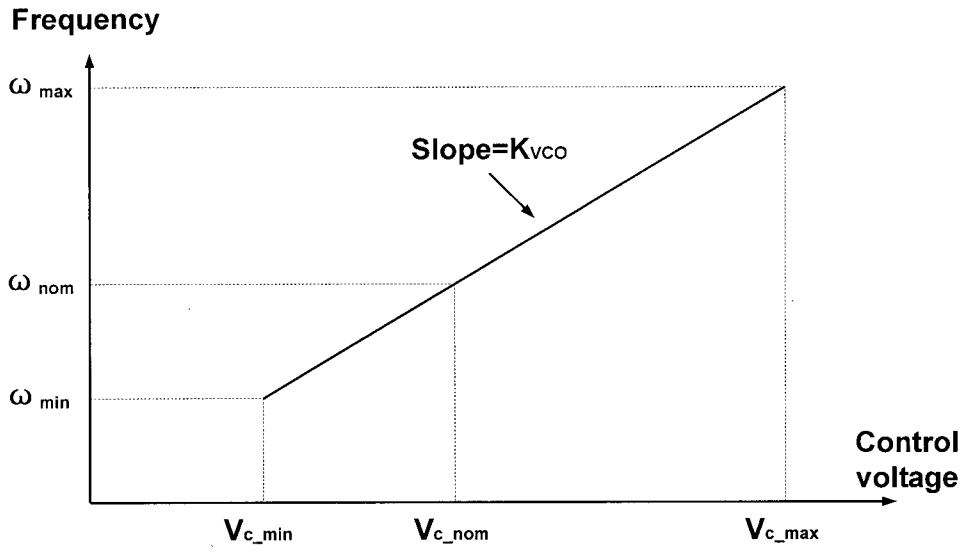


Figure 2.2: VCO Output Frequency vs VCO Input Voltage

2.2.2 Phase Frequency Detector (PFD) and Charge Pump (CP)

The PFD produces up/down signals proportional to the phase/frequency difference between the reference phase/frequency and the feedback phase/frequency. The output voltage is related to the input phase/frequency difference by a constant value K_{phase} where K_{phase} is equal to $\frac{I}{2\pi}$ and I is the current flow through the charge pump [5,6]. The K_{phase} can be a positive or negative number. A basic tristate PFD is shown in Figure 2.3 [5,6]. Either the f_{ref} or f_{out} rising edge causes the corresponding flip-flop's output to go high. The other flip-flop output will be low. The "RST" signal will be high

when both outputs are high which indicates both flip-flop inputs are high and the feedback signal is the same as the input signal. Therefore, both flip-flops will be reset. The charge pump transistor level schematic is shown in Figure 2.4 [5], where M2 and M6 are the current sources, and M3 and M4 are switches that are controlled by the PFD.

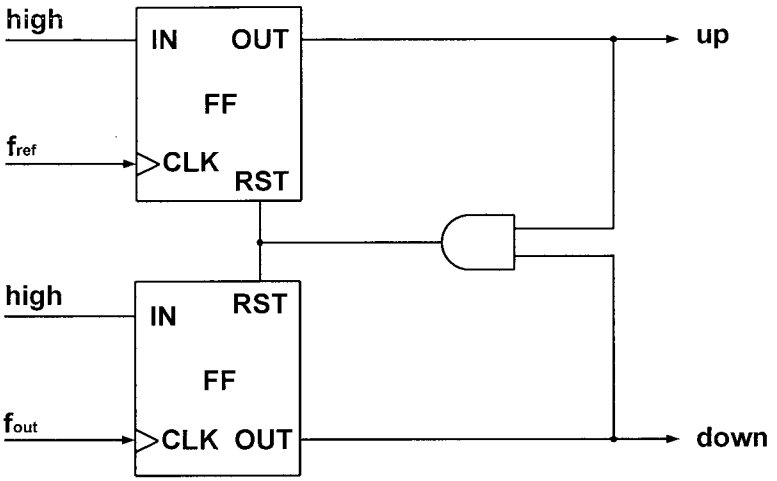


Figure 2.3: A Tristate PFD Circuit

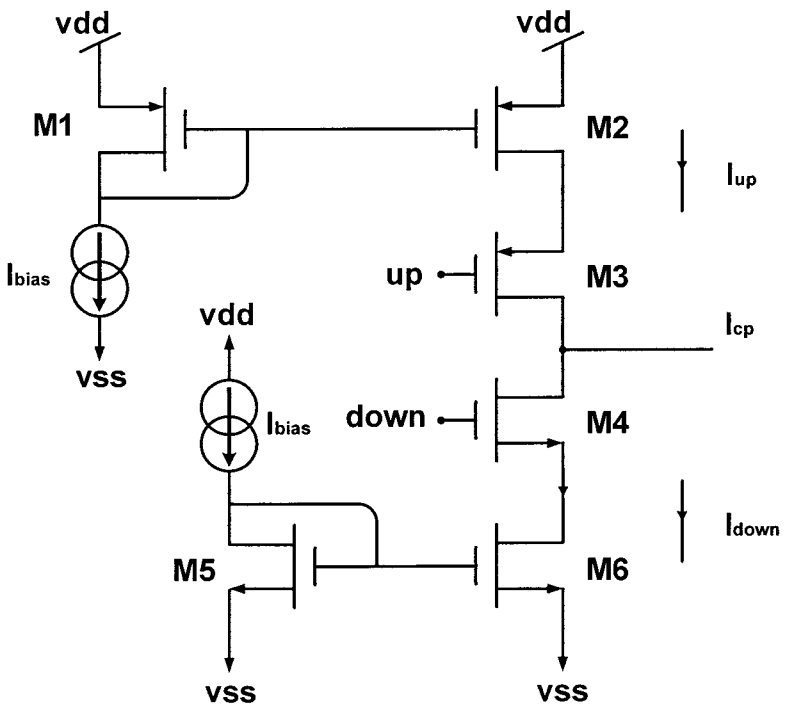


Figure 2.4: A Basic Charge Pump Circuit

The PFD and CP are connected together in Figure 2.5. The signal f_{ref} is the reference signal and f_{out} is the feedback signal. When f_{ref} arrives first, the "up" signal will be sent; and current will flow into the the LPF. As a result, the voltage on the LPF will increase and the VCO frequency will increase. The "up" signal will stay up until the feedback signal arrives. When the "down" signal is sent, a current will be drained out from the LPF [3, 5]. As a result, the voltage on the LPF will decrease and the VCO frequency will decrease. The signal Icp is the output current produced by the CP and can be expressed as:

$$\text{Icp} = \left(\frac{I}{2\pi}\right)(\theta_{ref} - \theta_{out}) \tag{2.2}$$

where θ_{ref} and θ_{out} are the phase of reference signal and the phase of feedback signal and I is the current that flows through the controllable current sources in the charge pump when they are on.

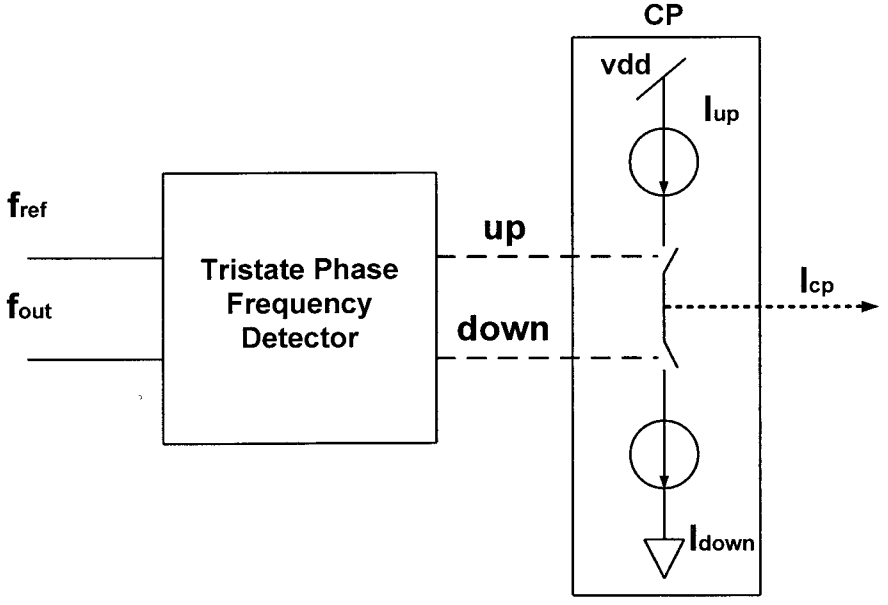


Figure 2.5: Tristate PFD and Charge Pump

2.2.3 The Low Pass Filter (LPF)

A typical loop filter is shown in Figure 2.6 [5] where Icp is the output current from the CP and $V_{control}$ is the VCO control voltage. The LPF converts the output current from the CP into a voltage. A combination of capacitors and resistors are used to stabilize the loop.

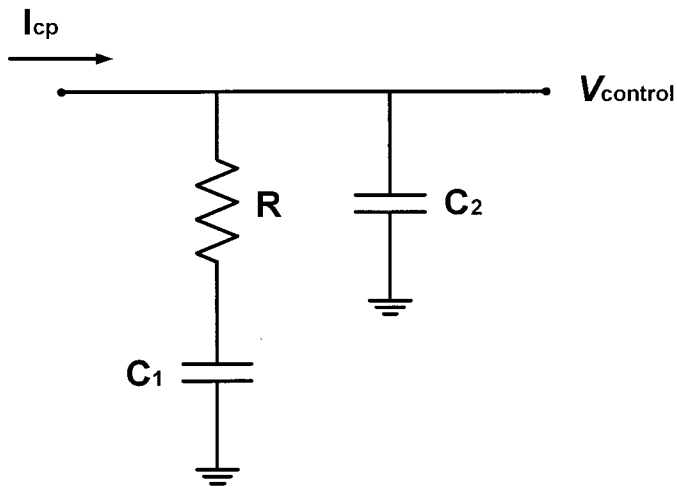


Figure 2.6: Second Order Low Pass Filter

The LPF output voltage can be expressed as the CP output current times the LPF equivalent impedance which is expressed as [5]:

$$V_c = \frac{i_d*(1+SC_1R)}{S(C_1+C_2)(1+SC_sR)} \tag{2.3}$$

where $C_s = C_1 * C_2/(C_1 + C_2)$ and C_2 adds a high-frequency pole to the system. Normally, C_2 is chosen as 1/10 as much as C_1 and helps reduce high-frequency ripples. However, it may not always be appropriate to use a value of one-tenth C_1 for the value of C_2. When R increases at high damping factor ζ, the impedance of series combination

of C_1 and R may become comparable to the impedance of C_2 at the loop natural frequency. In this case, C_2 has to be reduced to be less than 10% of C_1 [5].

2.2.4 The Multimodulus Divider (MMD)

An integer divider called a MultiModulus Divider (MMD) is often used in order to achieve a range of integer division ratio [5]. The MMD is formed by cascading divide by 2/3 modules [5]. An example divide by 2/3 module and MMD are shown in Figure 2.7 and Figure 2.8. In Figure 2.7, the Mod_{in} and R are the control bits used to control the division ration. When R = 0, the circuit will divide the input signal by 2; When Mod_{in}=1 and R = 1, the input signal will be divided by 3. In Figure 2.8, P is the last cell division ratio which is calculated by the procedure in [5]. The division ratio can be expressed as:

$$N = (2^{n-1}P + 2^{n-1}R_{n-1} + 2^{n-2}R_{n-2} + \ldots. + 2R_1 + R_0) \cdot S \qquad (2.4)$$

where R_0, $R_0 \ldots R_{n-2}$, R_{n-1} are the programmable MMD control bits and S is the integer step size. P is the numerator of the last stage division block.

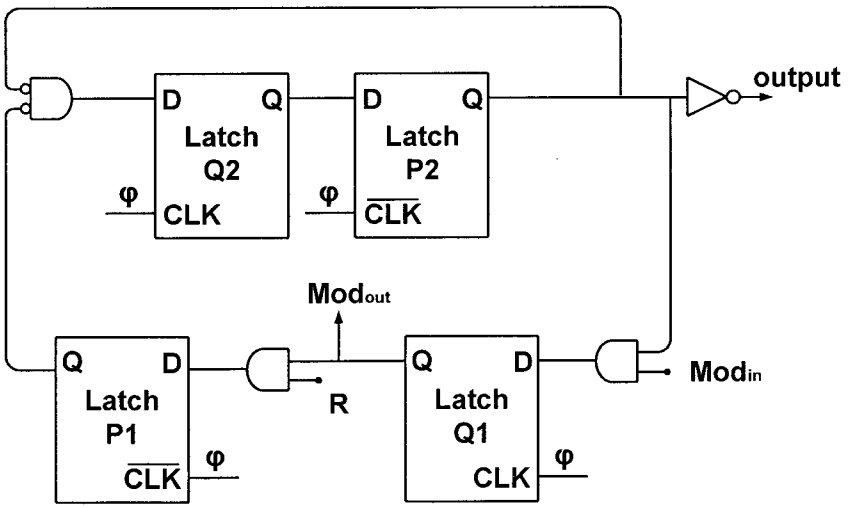


Figure 2.7: A Divided-by-2/3 Circuit

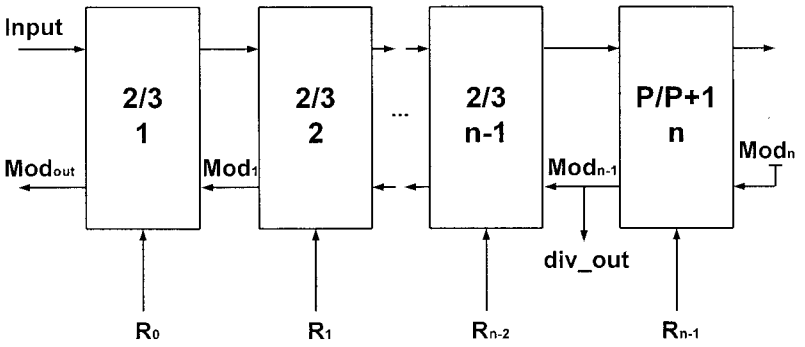


Figure 2.8: An MMD with Step Size 1

2.3 PLL Parameters

Based on the loop components discussed above, the loop transfer function can be expressed as [5]:

$$\frac{\theta_{out}}{\theta_{ref}} = \frac{\omega_n^2(\frac{2\delta}{\omega_n}S+1)}{S^2+2\delta\omega_n S+\omega_n^2} \tag{2.5}$$

where ω_n is the natural frequency and δ is the damping factor. The natural frequency ω_n and damping factor δ can be expressed as [5]:

$$\omega_n = \sqrt{IK_{VCO}/(2*\pi*N*C_1)} \tag{2.6}$$

$$\delta = \frac{R}{2}\sqrt{\frac{IK_{VCO}C_1}{2\pi N}} \tag{2.7}$$

where N is the integer divider ratio. The 3dB loop bandwidth of the system is given by [5]:

$$\omega_{3dB} \approx 2\delta\omega_n, \quad \delta > 1.5 \tag{2.8}$$

$$\omega_{3dB} \approx (1+\delta\sqrt{2})\omega_n, \quad \delta<1.5 \tag{2.9}$$

The reference frequency to maintain stability can be expressed as:

$$\omega_{ref} \geq 2\pi\delta\omega_n \tag{2.10}$$

2.4 PLL Phase Noise

The PLL phase noise mainly refers to noise that causes the fluctuations in the output phase. The PLL output signal can be expressed as [1]:

$$v_0(t) = V_0 cos[\omega_{LO} t + \varphi_n(t)] \tag{2.11}$$

where ω_{LO} is the desired output frequency, $\omega_{LO} t$ is the desired output phase. $\varphi_n(t)$ are the output phase fluctuations which can be expressed as [1]:

$$\varphi_n(t) = \varphi_p sin(\omega_m t) \tag{2.12}$$

where φ_p is the peak phase fluctuation and ω_m is the offset frequency from the carrier. The PLL's rms integrated phase noise is given by [5]:

$$\text{IntPNrms} = \sqrt{\int_{\Delta f_1}^{\Delta f_2} \varphi_{rms}^2 (f)\, df} \tag{2.13}$$

The PLL phase noise is contributed by all the PLL components, including VCO noise, crystal reference noise, frequency-divider noise, phase detector noise, charge pump noise and loop filter noise. The transfer function for the VCO can be expressed as [5]:

$$\frac{\varphi_{noise\ out}(s)}{\varphi_{noise\ VCO}(s)} = \frac{S^2}{S^2 + \frac{IK_{VCO}}{2\pi N} RS + \frac{IK_{VCO}}{2\pi N C_1}} \tag{2.14}$$

Since this is a high pass filter, at low offset frequency the VCO noise inside the loop bandwidth is suppressed. The transfer function for all the other components can be expressed as [5]:

$$\frac{\varphi_{noise\ out}(s)}{\varphi_{noise\ other}(s)} = \frac{\frac{IK_{VCO}}{2\pi N C_1}(1 + RC_1 S)}{S^2 + \frac{IK_{VCO}}{2\pi N} RS + \frac{IK_{VCO}}{2\pi N C_1}} \tag{2.15}$$

This is a low pass transfer function and the noise is surpressed outside the loop bandwidth. As a result, increasing the division ratio N will normally cause the phase noise to increase [5].

2.5 All Digital Phase Locked Loop (ADPLL) and Components Functionality

The ADPLL is almost an entirely digital system which is shown in Figure 2.9 [55, 56]. All function blocks except the xtal oscillator and the oscillator core of the DCO are implemented by purely digital circuits. In Figure 2.9, the phase detector will send a digital signal to the digital Loop Filter (LF). The DCO is controlled by a binary word. The CP and analog LPF of the analog PLL are no longer required. The ADPLL divider can be the same as the divider in an analog PLL[7]-[12].

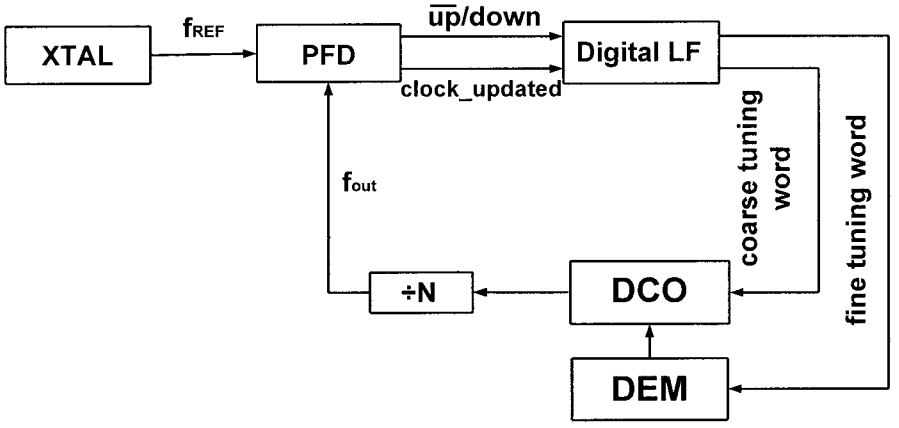


Figure 2.9: All Digital Phase Locked Loop Block Diagram

2.5.1 Digital Phase Detector

A digital phase frequency detector composed of a JK flip-flop and a counter is shown in Figure 2.10 [3]. The reference signal f_{ref} and the feedback signal f_{out} are binary

valued signals to set or reset the JK flip-flop. The output signal $\overline{up}/down$ is proportional to the phase error and it is used to control the counter in the digital loop filter [13]-[15].

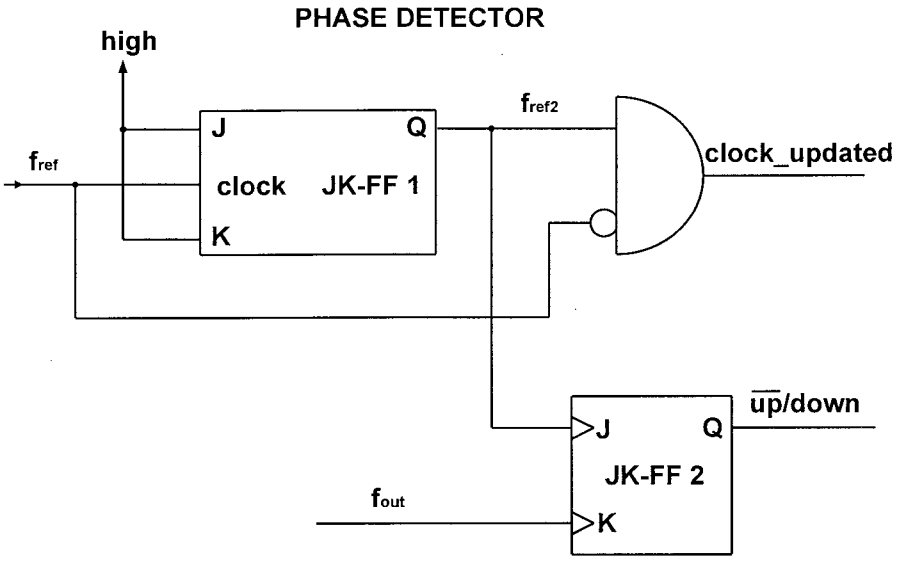


Figure 2.10: Digital Phase Detector

2.5.2 Digital Loop Filter

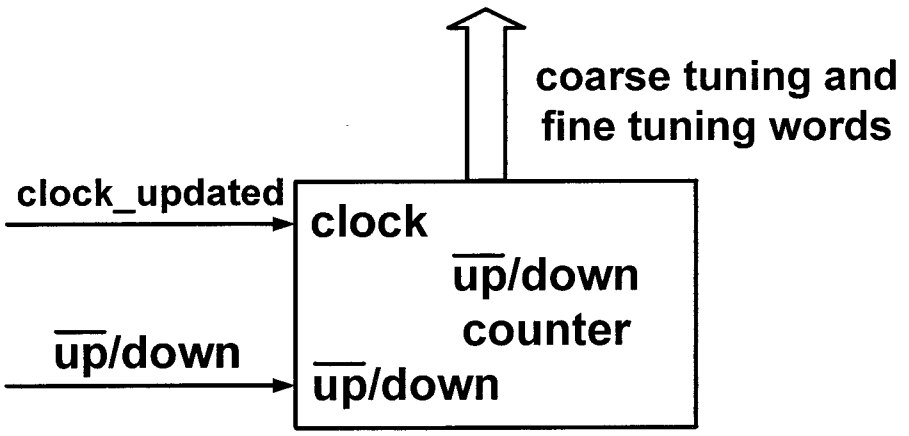


Figure 2.11: Digital Loop Filter

The Digital Loop Filter is shown in Figure 2.11 [3] For each "up" pulse generated by the phase detector, the counter is increased by 1. On the other hand, each "down" pulse will

decrease the counter by 1. Therefore, the result will be an n-bit parallel output signal that will be sent to the DCO [16].

2.5.3 Digital Controlled Oscillator

In an ADPLL, the DCO will be controlled by binary words from the loop filter. The ADPLL loop is shown in Figure 2.12.

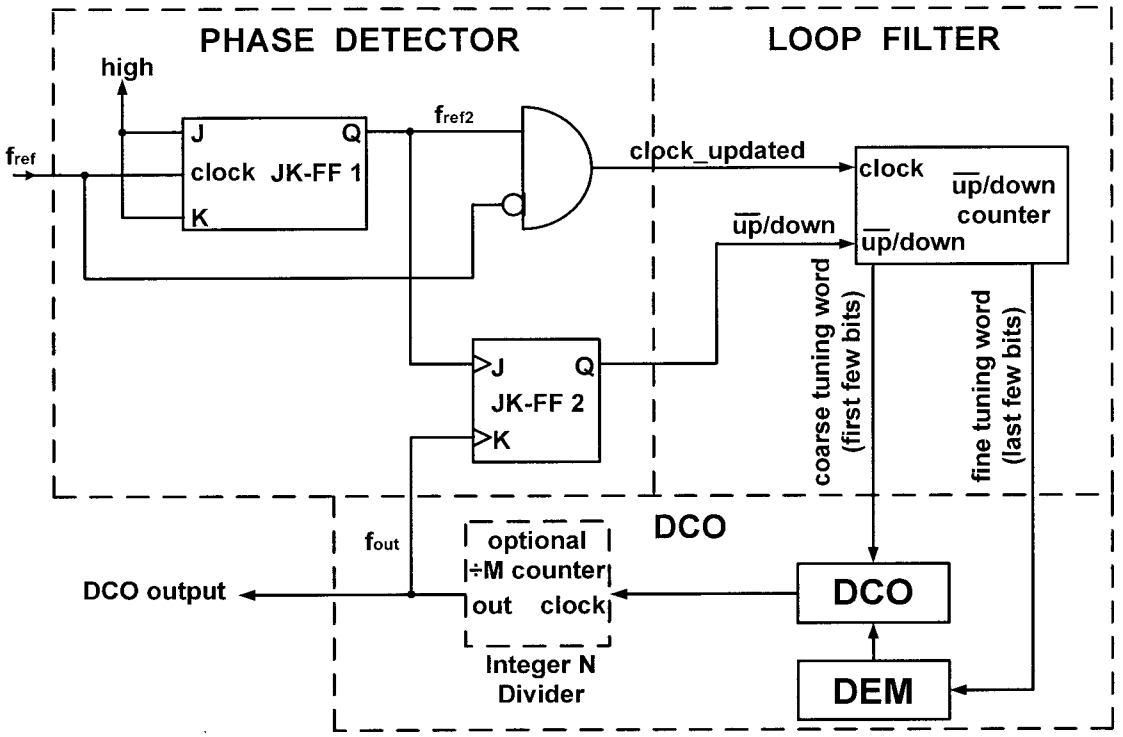


Figure 2.12: A Simplified ADPLL Block Diagram

Figure 2.12 shows that the charge pump used in analog PLLs is eliminated in the ADPLLs. The PLL design portability and testability are also increased. Designs can take advantage of area scaling with nanometer devices. Also large value capacitors for low bandwidth analog PLLs are no longer required. However, the digitally controlled oscillator generally has poorer frequency resolution [64]. Therefore, fine tuning bits are

required to calibrate the limited coarse tuning frequency resolution. Also, although the DCO control logic is more complicated than what is required for a VCO, the ADPLL allows the design to be easily portable to different technologies and avoid the concern of decreasing supply voltage which may force the charge pump transistors out of the saturation region [64].

Chapter 3: Voltage Controlled Oscillator (VCO), Digitally Controlled Oscillator (DCO) and Dynamic Element Matching (DEM)

3.1 Oscillator Fundamentals

A basic oscillator is composed of a resonator and some additional reactive components and resistors that are present for biasing, coupling or decoupling functions. Consider the mathematical expression of the oscillator output frequency as:

$$\omega_0 = 1/\sqrt{LC} \tag{3.1}$$

Ideally, the output frequency depends only on inductors and capacitors in the circuit. However, the parasitic capacitance needs to be considered since the transistor gate capacitance plays an important role in determining the oscillating frequency. Ideally, there should be no phase noise at the output frequency. However, a real oscillator will have phase noise [17]. The components used to characterize the performance of an oscillator are introduced in the following sections.

3.2 Voltage Controlled Oscillator (VCO)

The VCO is an essential block in all analog PLL designs which are used to generate periodic waveforms whether they are sinusoidal, square or triangular. The output frequency is controlled by a loop filter voltage and the output frequency range is defined

by the free running frequency f_c and K_{vco}, where K_{vco} is the sensitivity of the VCO output frequency to the bias voltage or more commonly referred to as VCO gain. Therefore, ideally, the output frequency can be expressed as:

$$f_{osc} = f_{nom} + K_{VCO} * V_{control} \tag{3.2}$$

One of the most popular oscillators is the LC tank oscillator [17]. An LC oscillator must have two fundamental components, one being the resonator and the other a feedback loop. An LC resonator is at the core of many high frequency integrated oscillators and determines the frequency of oscillation. A typical parallel LC resonator is shown in Figure 3.1, where R_p is the equivalent parallel resistance of the LC tank.

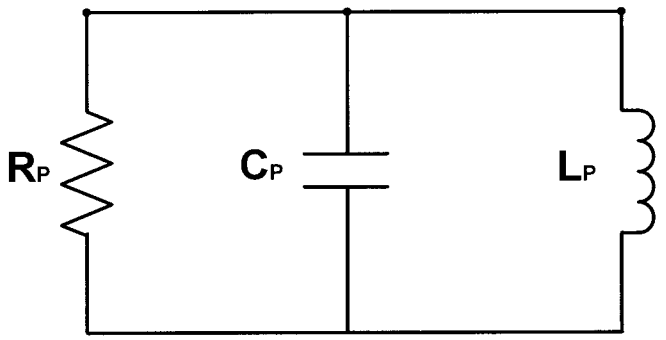


Figure 3.1: A Typical Parallel LC Oscillator Core

Either a noise signal or a small current source provided by the system can cause the resonator to start oscillating. These oscillations will die away unless feedback is added in order to sustain the oscillation [1]. The resulting waveform without feedback is shown in Figure 3.2 [1].

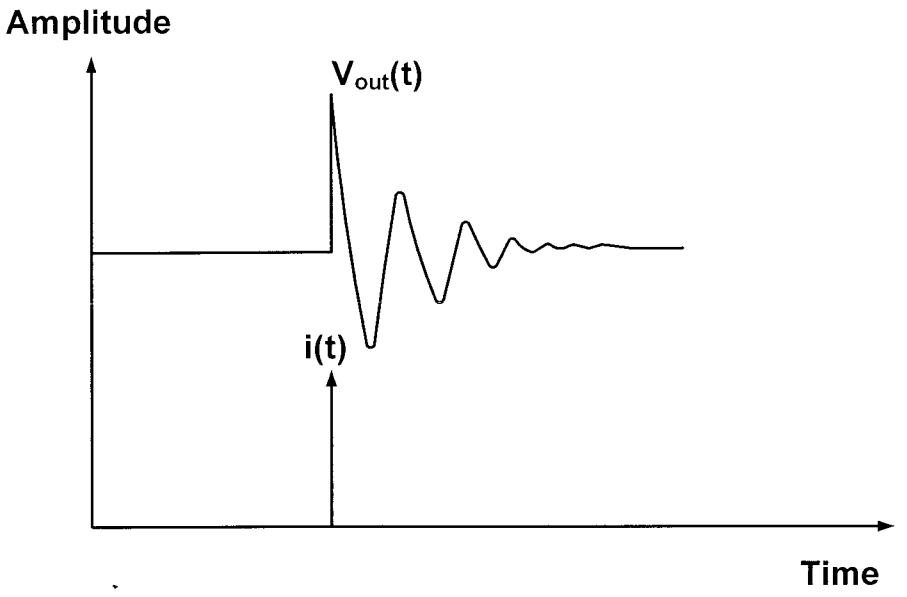


Figure 3.2: LC Resonator without Feedback

As a result, a parallel feedback network must be added to sustain the oscillation and it can be shown that the resulting feedback is equivalent to adding a negative resistance to the circuit [17]. The parallel resonator with equivalent negative resistance $-R_{amp}$ is shown in Figure 3.3. The oscillation amplitude will continue growing with the overall negative resistance. However, power supply rails and nonlinearity in devices will limit the oscillation amplitude of the practical resonator. These will reduce the negative resistance effect to achieve a unity loop gain. In many LC oscillator designs, the inductors are usually of fixed value while the capacitors are tunable to control the output frequency [5]. The output frequency can be calculated using the simplified expression as follows:

$$\omega = \frac{1}{\sqrt{L*(C_{fix}+C_{variance})}} \tag{3.3}$$

where L is the inductor, C_{fix} is the fixed capacitance and $C_{variance}$ is the variable capacitance in the resonator which is typically controlled by a voltage signal, therefore the name Voltage Controlled Oscillator (VCO).

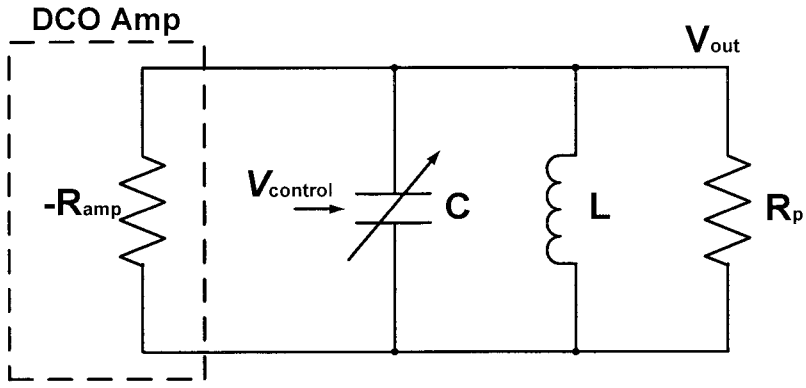


Figure 3.3: A Parallel Resonator with Negative Resistance to the Circuit

There are many oscillator topologies, such as Colpitts oscillator, Hartley oscillator and negative Gm oscillator. The Hartley oscillator and the Colpitts oscillator are shown in Figure 3.4 and Figure 3.5 [17]. Hartley oscillators are inductively coupled, variable frequency oscillators which may be in series or shunt fed. Hartley oscillators have the advantage of one center tapped inductor and one tuning capacitor. This arrangement simplifies the construction of a Hartley oscillator circuit [20]. The Hartley oscillator is not popular for integrated circuit (IC) implementations due to the fact that capacitors are easier to realize than inductors.

Colpitts oscillators are similar to the shunt fed Hartley circuit except in the Colpitts oscillator, instead of having a tapped inductor, it utilizes two series capacitors in its LC circuit [20].

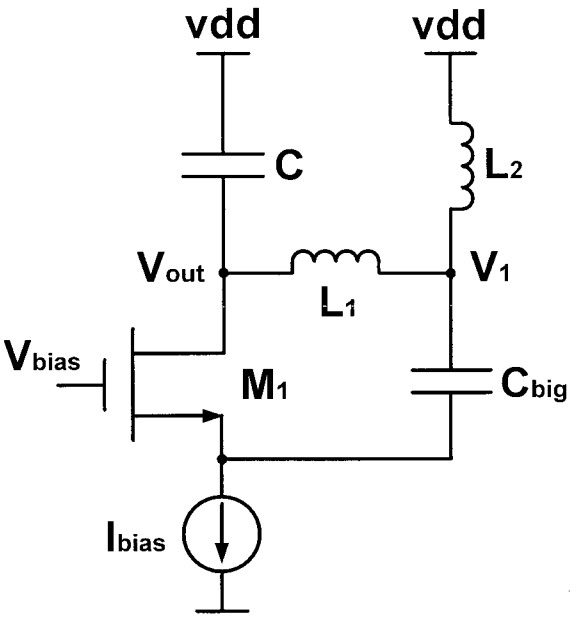


Figure 3.4: Hartley Oscillator Topology

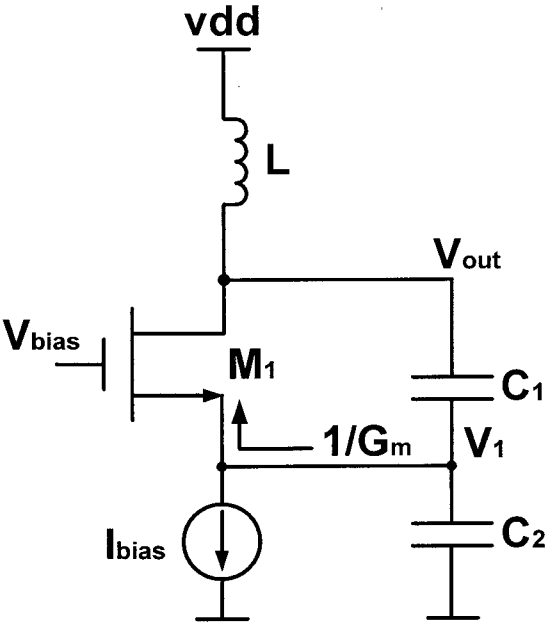


Figure 3.5: Colpitts Oscillator Topology

A common method of creating a voltage controlled oscillator for integrated circuits is to use a negative G_m oscillator because of its high power efficiency and low phase noise

[17]. The negative G_m oscillator topology is shown in Figure 3.6. The cross-connected NMOS transistors generate the negative resistance that starts the oscillation and compensates for the losses of the tank. The tail transistor at the bottom of the circuit is used to control the current flowing in the oscillator. The small signal equivalent model for the negative resistance cell in the oscillator is shown in Figure 3.7. Now assuming that both transistors are biased identically, (i.e. $g_{m1} = g_{m2}$, $r_{gs1} = r_{gs2}$, $v_{gs1} = v_{gs2}$) and the equivalent impedance can be solved as [1]:

$$Z_i = \frac{v_i}{i_i} = \frac{-2}{g_m} \tag{3.4}$$

where Z_i is the equivalent impedance; v_i is the input voltage of the LC tank and i_i is the input current of the LC tank. It can be shown that in the negative G_m oscillator design, the necessary condition for oscillation is that:

$$g_m > \frac{2}{R_{par}} \tag{3.5}$$

where R_{par} is the equivalent parallel resistance of the resonator and g_m is the MOSFET transconductance. The effect of parasitic capacitance on the frequency of oscillations needs to be considered; therefore, the frequency is given by:

$$\omega_{osc} \approx \frac{1}{\sqrt{L(2C_{gs}+\frac{C_{ds}}{2}+C)}} \tag{3.6}$$

where C_{gs} is the parasitic capacitance between the gate and source of MOSFET and C_{ds} is the parasitic capacitance between the drain and source of MOSFET.

The parasitic routing capacitance also needs to be considered; however, its value is unknown. Therefore, measured oscillator output frequency will be lower than the calcultion result from (3.6).

The peak voltage developed across the resonator differentially is given by [1]:

$$V_{tank} = \frac{2}{\pi} I_{tail} * R_{par} \tag{3.7}$$

where I_{tank} is the oscillator tank current.

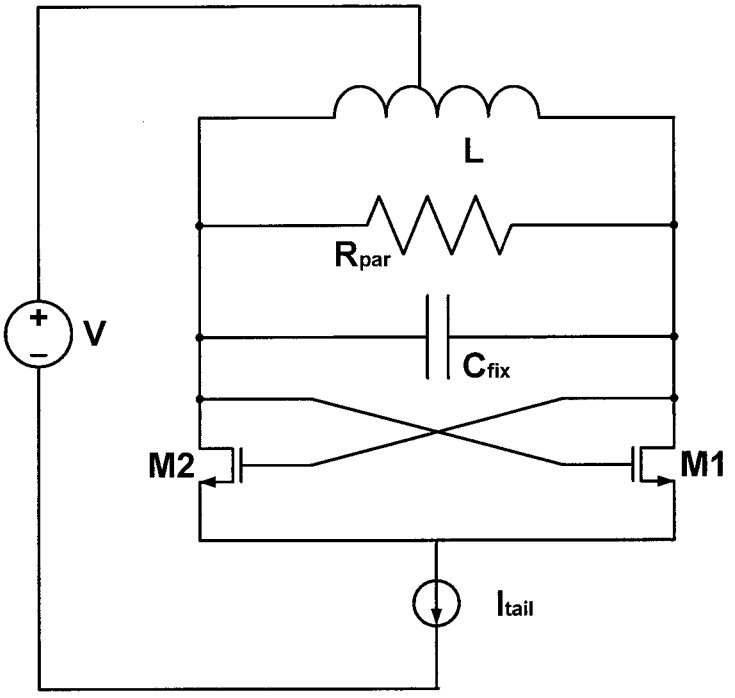


Figure 3.6: Simplified Diagram of a $-G_m$ Oscillator

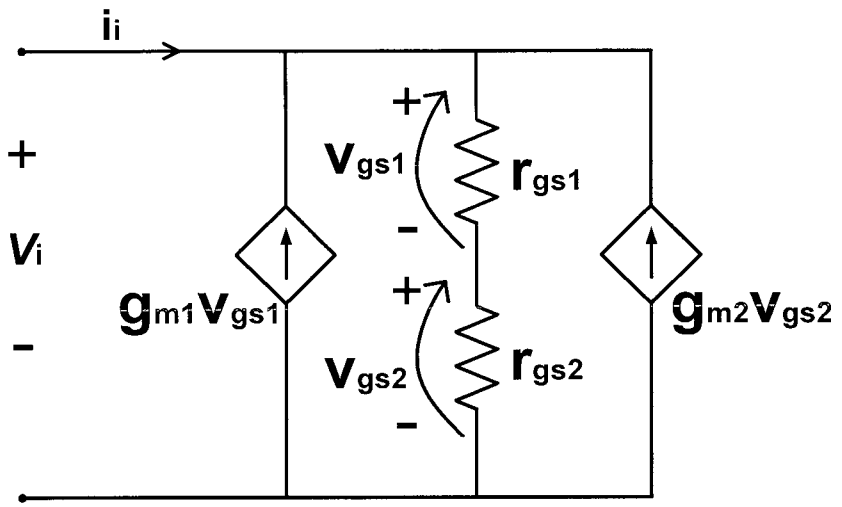


Figure 3.7: Small-signal Equivalent Model for Negative Resistance Cell in the Negative G_m Oscillator

3.3 Digitally Controlled Oscillator (DCO) Fundamentals

A DCO can be considered as an extension of a VCO [7]. Whereas a VCO typically has one input signal controlling the frequency in an analog fashion, a DCO usually has a number of digital inputs controlling the frequency.

Similar to a VCO, an LC resonator based DCO commonly has one or more inductors and capacitors that determine the frequency of oscillation. As well, with a DCO it is much more common to have the capacitors as the variable part of the resonator that can be used to control the frequency [51]. However, now instead of using an analog control signal, the DCO capacitors will be controlled by digital bits (either "high" or "low") as shown in Figure 3.8 [51].

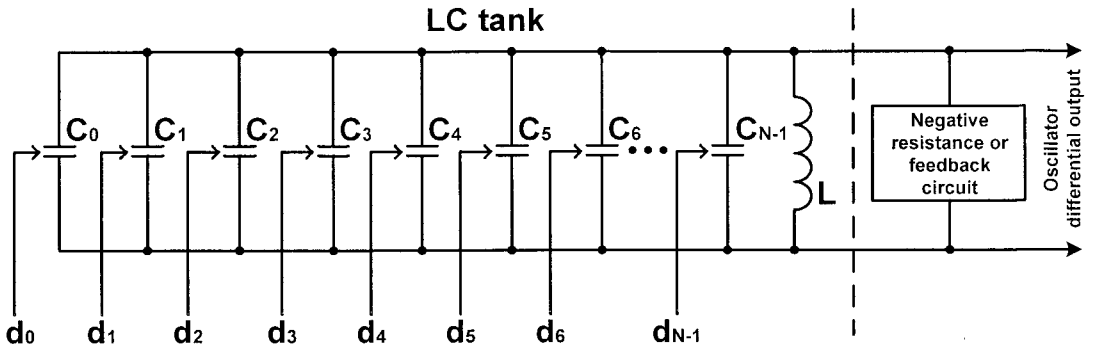


Figure 3.8: DCO Resonator with Digital Control Bits

3.4 Varactors

Varactors are used in many DCO designs as tunable capacitance. Varactors are formed from regular MOS transistors where the gate is one terminal and the source and drain tied together form the other terminal [51]. If a large enough positive voltage is put on the gate of an NMOS transistor (relative to the source/drain connection), an inversion layer of electrons forms along the surface, and the capacitance is at its maximum value. Such a structure, referred to as an inversion mode varactor, is shown in Figure 3.9 [60].

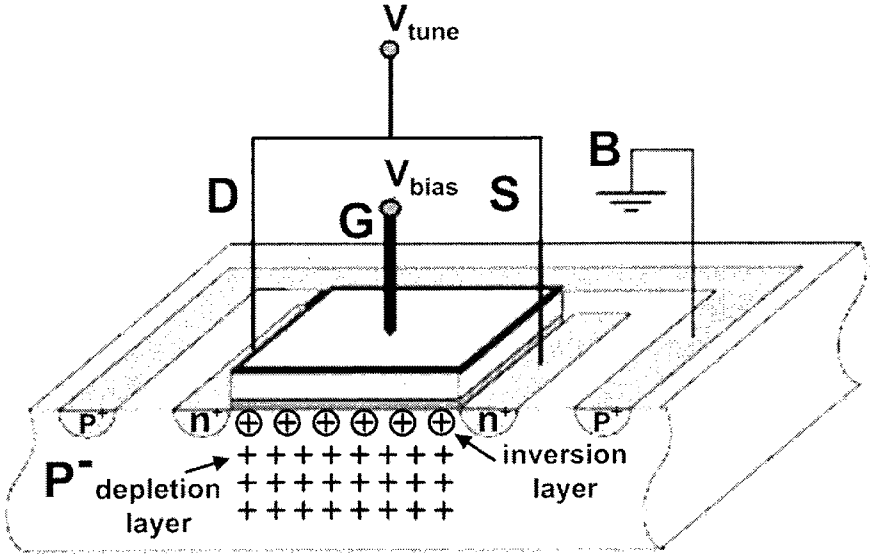


Figure 3.9: Cross Section of Inversion Mode NMOS Varactor [60]

As the gate to source/drain voltage decreases, the depletion layer thickness changes which results in a change in effective capacitance. Therefore, the capacitance is dependent on the gate voltage as shown in Figure 3.11. The NMOS varactor can be modelled by the equivalent circuit shown in Figure 3.10 [60].

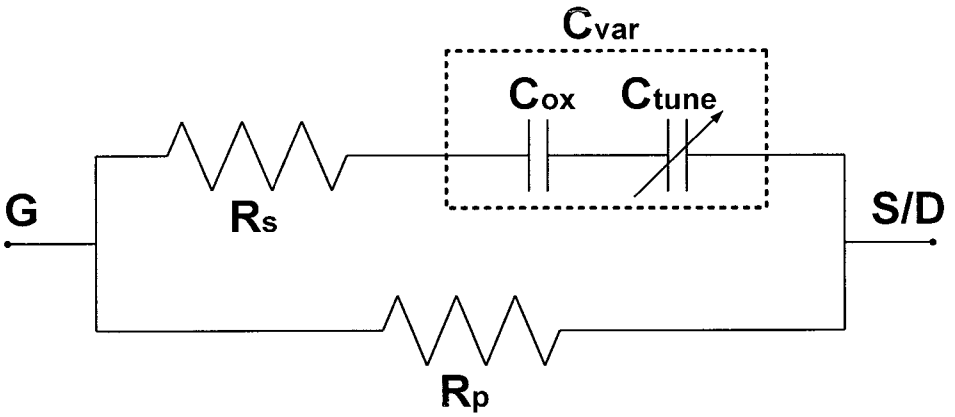


Figure 3.10: Cross Section of Inversion Mode NMOS-Varactor Equivalent Circuit

The capacitance of varactors will vary with the change of bias voltage between the gate (G) and Source/Drain (S/D) connections. Conventional MOS varactors have a wide linear region in the Capacitance versus Voltage (CV) curve which facilitates analog tuning. However, varactors in deep-submicron CMOS processes have a linear region that is greatly compressed as shown in Figure 3.11. Conversely, the flat regions of the CV curve are expanded which is desirable for digital switching [21]. Therefore, the digital signal swing range used to control the varactors can be decreased. It should also be noted that deep-submicron varactors can be made extremely small with a large ratio between their maximum and mimimum capacitance ($\frac{C_{max}}{C_{min}}$) where C_{max} and C_{min} are the maximum and minimum capacitance that can be achieved by the varactors. This large

capacitance ratio increases the output frequency tuning range. Both the traditional CMOS and deep-submicron CMOS CV curves are shown in Figure 3.11 [52].

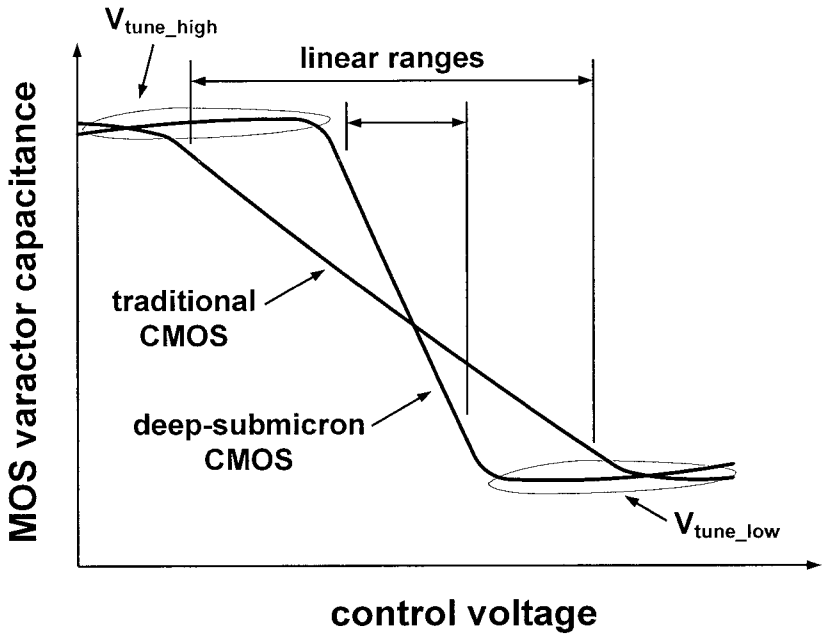


Figure 3.11: Traditional CMOS and Deep-submicron CMOS Capacitance vs Voltage Curve

3.5 Switch Metal-Insulator-Metal Capacitors (MIM-caps)

The single nitride LY to E1 metal-to-metal capacitor (Figure 3.12) is formed by adding a thin layer of metal, LY, between E1 metal and the underlying layer of metal, LY. The top plate of the single capacitor, LY, is connected to E1 with the via level FT.

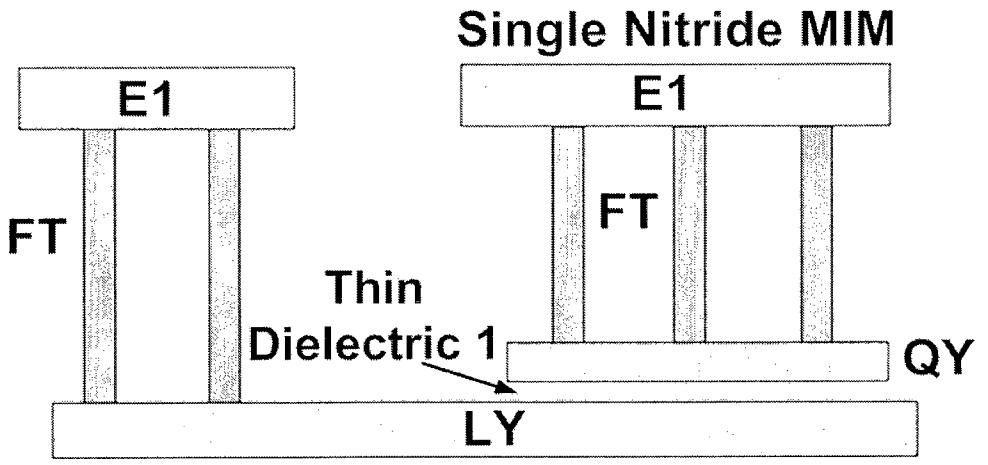


Figure 3.12: Single Nitride MIM-cap Structure

Single Nitride MIM capacitors [61] can be connected into an oscillator by using NMOS transistors as switches. The output frequency is controlled by switching the MIM-caps in and out of the circuit. An example switch circuit [24] is shown in Figure 3.13. The MIM-cap can have a higher Quality factor (Q) than varactors [67]; this can help reduce the power consumption as it reduces the resonator load resistance. The conductivity and quality factor of the switch circuit are affected by the center NMOS transistor (M1). Therefore, it needs to be sized properly to achieve an acceptable conductivity and quality factor. The boundary NMOS transistors (M2 and M3) are used to set the DC bias when the control bit (a) is "high". When the control bit is "low", the boundary transistors are in a disconnected state. They are minimally sized to reduce the parasitic capacitance [22]-[24]. It should be noted that the parasitic capacitance introduced by M1 may also affect the oscillator output frequency.

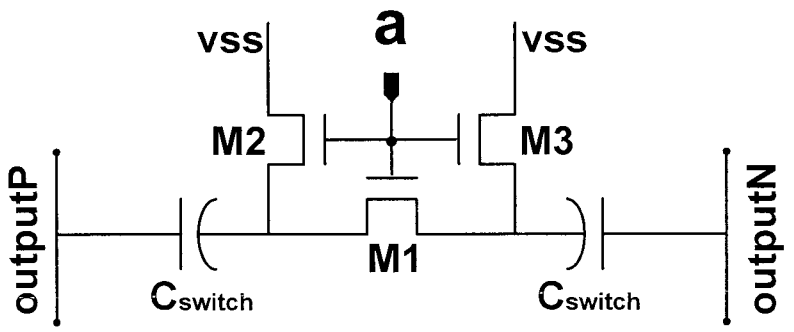


Figure 3.13: MIM-cap Switch Circuit

3.6 Digitally Controlled Oscillator (DCO) Control Bits

In a DCO, there are a number of inputs controlling the frequency; each typically controls it in a binary fashion. That is, bit 1 might change the frequency by 100 kHz, bit 2 by 200 kHz, bit 3 by 400 kHz, bit 4 by 800 kHz, etc. Thus if a design changes the frequency by 1 MHz, bit 4 and bit 2 are set high. The oscillator core is still the same as before with an inductor and capacitor; the control section is what changes – whereas in a VCO, varactors are usually used to change the frequency. With a DCO, digital bits are used to control varactors or switch MIM-caps, thereby affecting the oscillator output frequency differently.

Bits that are used to control these varactors or switch MIM-caps are called tuning bits. In this thesis, switch MIM-caps are used to control the DCO output frequency and its topology is shown in Figure 3.14, where d_k is the k_{th} control bit; C_0 is the unit MIM-cap capacitance.

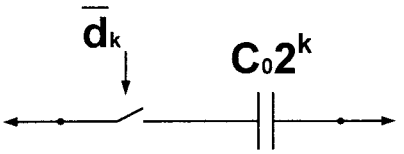


Figure 3.14: Switch MIM-cap Topology

The number of tuning bits depends on the number of tuning steps. If N tuning steps are required, then the number of tuning bits is expressed as below:

$$n = logN/log2 \quad (3.8)$$

where n is the number of tuning bits. The DCO output frequency is given by:

$$f_0 = f_v\left(2^{n-1}\bar{b}_{n-1} + \cdots + 2\bar{b}_1 + \bar{b}_0\right) + f_{min} \quad (3.9)$$

where f_{min} is the minimum oscillator output frequency and f_v is the minimum frequency step size [25]-[27]. The most significant bit (b_n) corresponds to the largest size capacitor in the design and the least significant bit (b_0) corresponds to the smallest size capacitor. During fabrication MIM-caps process variations and mismatches occur and have to be considered if high frequency resolution is desired. One technique to reduce these process variations and mismatches will be discussed in Section 3.9.

3.7 DCO Phase Noise

One of the most important characteristic of an oscillator is its phase noise. An ideal oscillator has all signal power at a single frequency. However, the spectrum of a real oscillator has power at more than one discrete frequency; thus "skirts" are produced as shown in Figure 3.15 [7]. A major challenge in the DCO design is to meet the phase noise requirements. A simplified phase noise formula is given as follow [1]:

$$PN = \left(\frac{|H_1|\omega_0}{(2Q\Delta\omega)}\right)^2 \left(\frac{kT}{2P_s}\right) \quad (3.10)$$

where Q is the loaded quality factor of the tank; $H_1 = 1$; ω_0 is the resonant frequency and $\Delta\omega$ is the offset frequency. The input noise can be expressed as [1]:

$$|N_{in}(s)|^2 = kT \quad (3.11)$$

where k is Boltzmann's constant $1.38 * 10^{-23} J/K$ and T is temperature in Kelvin (298K). Also, the term P_s can be calculated as [1]:

$$P_s = \frac{V_{tank}^2}{2R_p} \tag{3.12}$$

V_{tank} is the peak resonator voltage, and R_p is the equivalent parallel resistance of the oscillator. Equation 3.10 shows that the phase noise will increase at a higher oscillator output frequency ω_0.

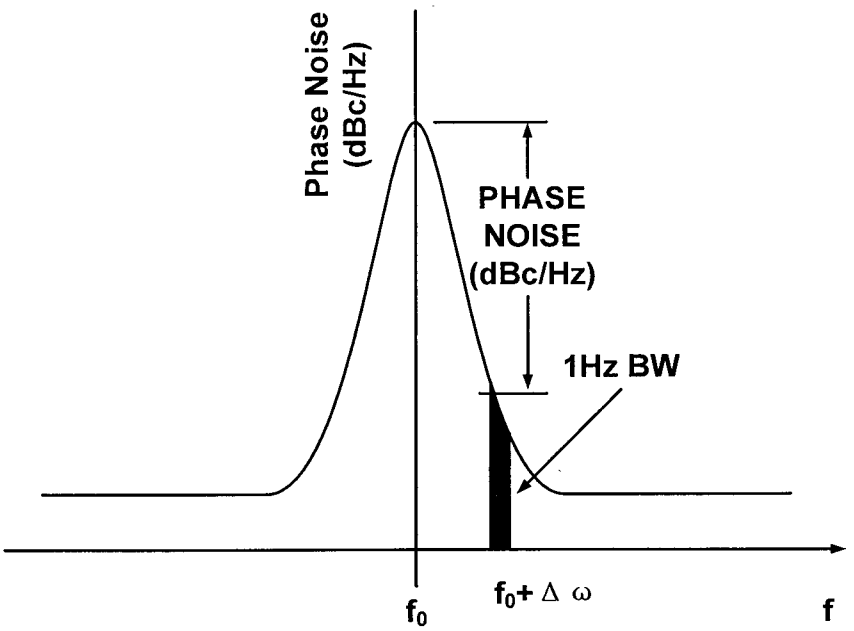


Figure 3.15: The Oscillator Spectrum

3.8 The Tree-Structured Dynamic Element Matching (DEM)

High frequency resolution oscillators usually require precise matching of analog components. One version of Dynamic Element Matching (DEM) can be implemented to randomize the component variations and mismatches [28]. Instead of accessing a single multi-unit component, DEM can randomly access multiple unit components (e.g. small

unit capacitors) at the same time using different unit capacitor combinations in each clock cycle. In DEM, digital logic is used to scramble the unit capacitor in such a fashion that the error introduced by the unit capacitor process variations and mismatches are suppressed within the DEM's signal band. One of the most popular approaches is a tree structured digital encoder [28]. The DEM block and the architecture for a 16-level tree-structured digital encoder is shown in Figure 3.16. Each node represents a switching block labeled as $S_{a,b}$, where "a" represents layer number and "b" represents the position within a layer. The higher level signal processing performed in the switching block is shown in Figure 3.17 and the functional partitioning of the switching block is shown in Figure 3.18.

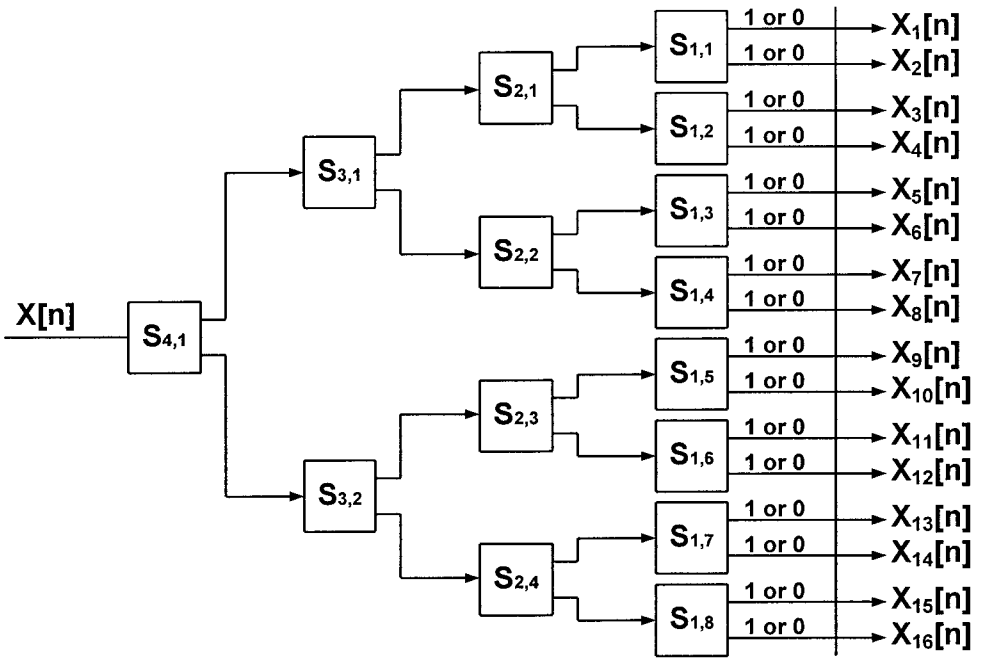


Figure 3.16: The 16-level Tree-structured Digital Encoder

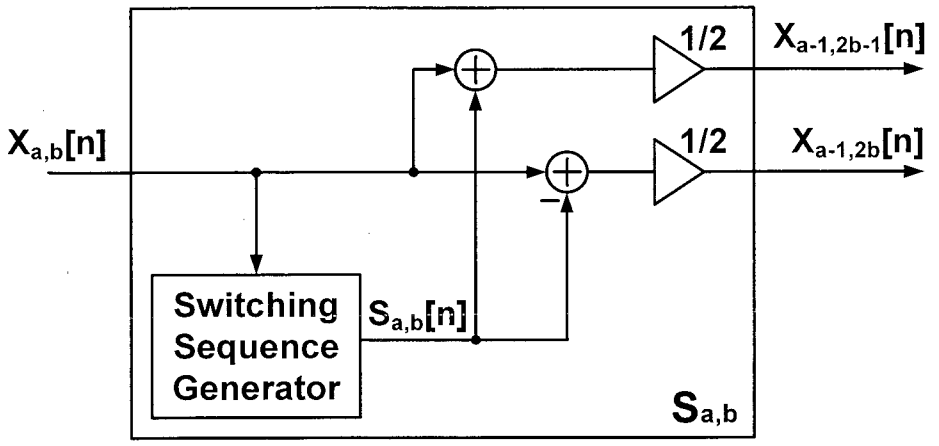


Figure 3.17: The Signal Processing Preformed in the Switching Block

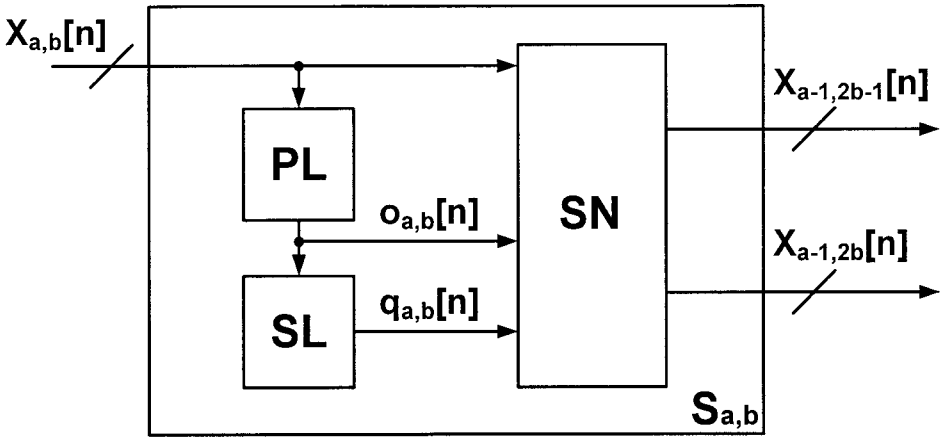


Figure 3.18: A Functional Partitioning of the Switching Block, where SN is the *Splitting Network*, PL is the *Parity Logic*, and SL is the *Sequencing Logic*

In Figure 3.17, the input $x_{a,b}[n]$ represents both the input of $S_{a,b}$ and its numerical value. The switching block input contains two Least Significant Bit (LSB) with both bit 0 and bit 1 being unity weighted. If $x_{a,b}[n]$ is an odd number, one of the LSB will be "1" and the other will be "0" and the parity logic produces a "1". The values of $x_{a-1,2b-1}[n]$, and $x_{a-1,2b}[n]$ will be either $(x_{a,b}[n]+1)/2$ or $(x_{a,b}[n]-1)/2$. Otherwise if $x_{a,b}[n]$ is an even number, the parity bit will produce a "0" . Both $x_{a-1,2b-1}[n]$, and $x_{a-1,2b}[n]$ will be equal to $(x_{a,b}[n])/2$. The divide-by-two operation

is performed by right shifting the a−1 Most Significant Bit (MSB) of $x_{a,b}[n]$ [28]–[36]. In Figure 3.18, the parity logic determines the parity of the switching block input and generates the parity sequence $o_{a,b}[n]$. The sequencing logic produces the sign sequence $q_{a,b}[n]$. Given $x_{a,b}[n]$ and the binary representation of $s_{a,b}[n]$, the role of the splitting network is to perform the arithmetic operations shown in Figure 3.17 that generate the switching block's two output sequences. The switching block and sequencing logic architecture are shown in Figure 3.19 and Figure 3.20.

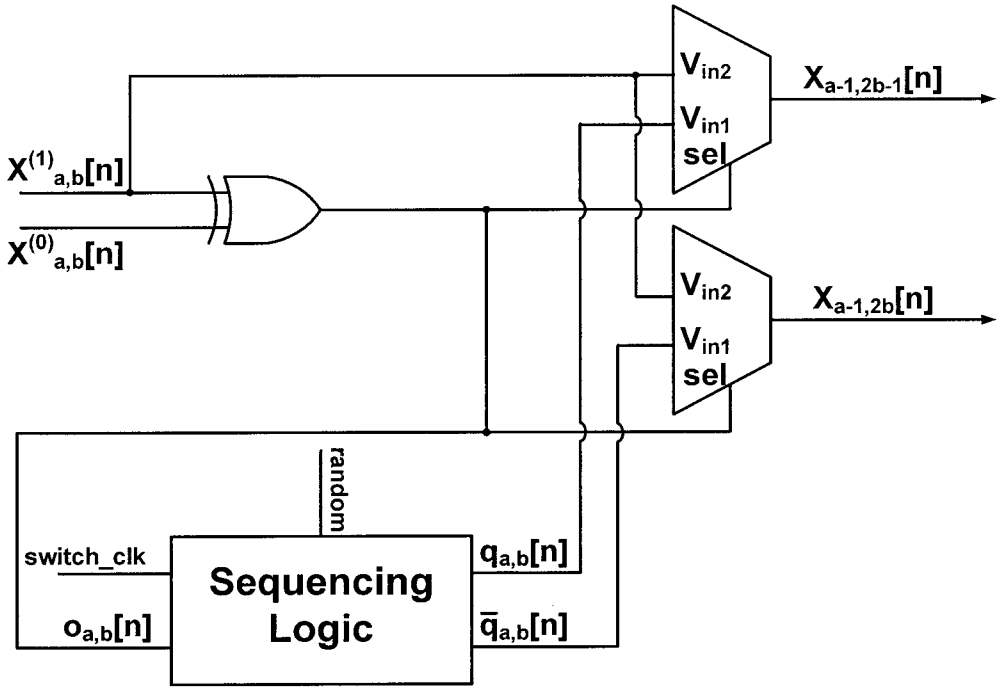


Figure 3.19: Switching Block, SL represents the *Sequencing Logic*

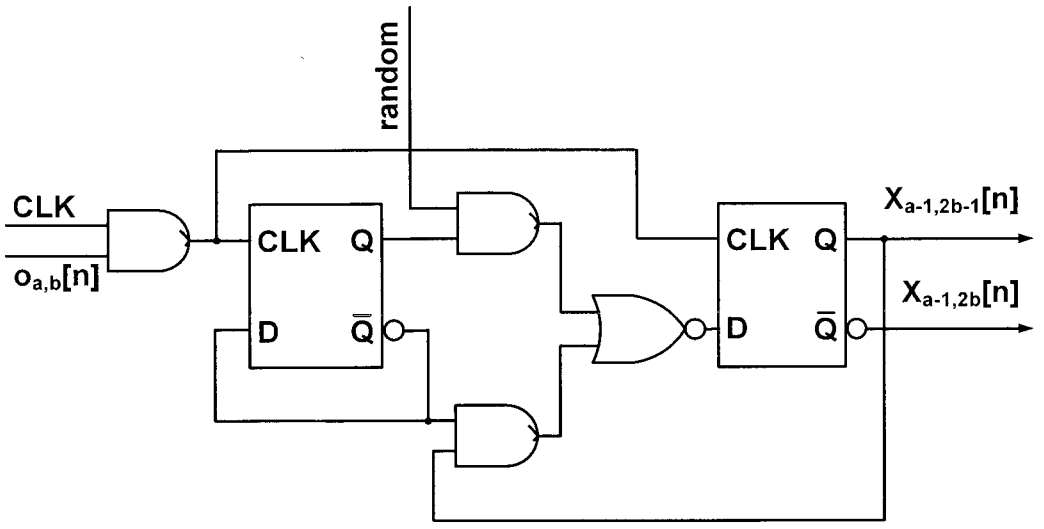


Figure 3.20: Sequencing Logic

As an example, the numerical input number "5" is used to explain the logic of the tree structured switching block. The input "5" is expressed as "4+1" where the "1" is the appended "0th" bit. So the 4-bit binary number can be represented as "1001" where both the last two bits are LSBs. Therefore, three layer tree structured switching blocks are required. Since "5" is an odd number, "101" and "100" are produced after the first layer switching block. At the second layer, the odd number "101" will be split into another two 2-bit binary numbers which are "11" and "10" and the even number "100" is split into two 2-bit binary numbers "10". At the third layer switching block, the "11" will produce two bits of "1", and the "10" will produce a "1" and a "0". As a result, five bits of "1" and three bits of "0" are produced by this three layer tree structured switching block. The "random" is a pseudo random generator; therefore, the sequencing logic $q_{a,b}[n]$ can be either "1" or "0". This results in a random three bits of "0" and a random five bits of "1" to be produced by this three layer tree structured decoder. These random "1" and "0" are

used to dither control bits within the DCO. The phase noise is oversampled by a high dithering frequency; therefore, it is spread over a larger frequency range and the noise floor is decreased.

Chapter 4: DCO Design, Analysis and Process Variation Suppression

4.1 Introduction

This chapter applies the DEM technique to the DCO fine tuning band to suppress process variations and mismatches. The designed DCO frequency resolution is limited by the capacitance tuning steps of the smallest MIM-cap difference for a given technology. However, process variations occur during the capacitor fabrication process, strongly affecting the output frequency step size.

4.2 Proposed DCO Architecture

In the proposed DCO, the NMOS and PMOS oscillator topology is chosen because of its inherent low phase noise and power efficiency [43]-[48]. A simple DEM technique is introduced to time-average the smallest thermal-code capacitors [26], where the thermal-code capacitors refer to the unity weighted capacitors in the fine tuning band. The DCO coarse tuning and fine tuning band combination is designed to achieve a 40kHz frequency resolution with an output frequency range from 170MHz to 220MHz. The DCO specifications are shown in table 4.1 and these are typical specifications that would be required for an ADPLL application [18]. The high level DCO architecture is shown in Figure 4.1. The designed DCO will be used in an ADPLL which will in turn be used to

injection lock the DCO to one of its harmonics. This work provides a number of advantages in the realization of single chip transceivers. First, a separate PLL for the Local Oscillator is no longer required. The low frequency PLL can be the same PLL that is used for transceiver clock generation and therefore does not require any extra power. Second, the low phase noise VCO is eliminated as the phase noise will be determined by the clock PLL, which allows a significant reduction in the VCO power consumption [23].

Table 4.1: The DCO Specifications

Power Consumption	<2.5mW
Coarse Tuning Words	8b
Fine Tuning Words	6b
Frequency Resolution	40kHz
Frequency Tuning Range	25MHz

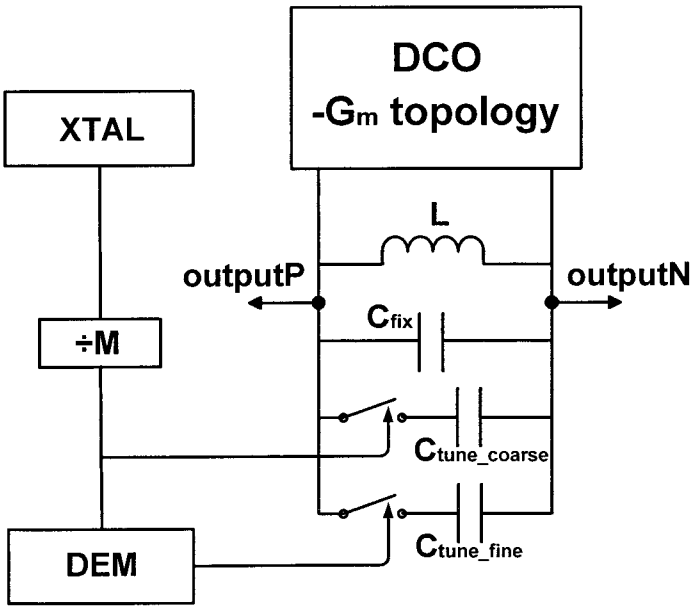


Figure 4.1: Simplified DCO Topology

The LC oscillator resonating frequency is established as:

$$f = \frac{1}{2\pi}\left(\sqrt{L\left(C_{fixed} + C_{coarse} + C_{fine}\right)}\right)^{-1} \tag{4.1}$$

where C_{fixed} is the fixed capacitor. C_{coarse} and C_{fine} are the switch-caps contributed by the coarse tuning and the fine tuning band. The NMOS and PMOS oscillator can start with half as much collector current in each transistor as a Colpitts oscillator under the same loading conditions. As a result, the DCO can sustain smaller parallel resistance for the same bias condition [37]-[39].

4.3 Gm matching

The noise injected into the output nodes of the oscillator can be partially cancelled out if the NMOS gm, the PMOS gm and the capacitance are matched [7]. In order to match the capacitance to a first order, equation 4.2 needs to be satisfied [5]:

$$W_n L_n = W_p L_p \tag{4.2}$$

where W and L are the oscillator core transistor width and length. Equation 4.3 is required to achieve an equal NMOS and PMOS g_m [5]:

$$\sqrt{2\mu_n C_{ox}\frac{W_n}{L_n} I_{DS}} = \sqrt{2\mu_p C_{ox}\frac{W_p}{L_p} I_{DS}} \tag{4.3}$$

where μ_n and μ_p are the NMOS and PMOS transconductivity; C_{ox} is the oxide capacitance and I_{DS} is the transistor bias current. To satisfy both conditions, the NMOS transistor length and width for best phase noise is calculated as [5]:

$$L_n = L_p\sqrt{\frac{\mu_n}{\mu_p}} \tag{4.4}$$

$$\frac{W_p}{W_n} = \sqrt{\frac{\mu_n}{\mu_p}} \tag{4.5}$$

where Lp is the minimum transistor length in a given technology. The basic parameters for 0.13μm technology are shown below:

$$\mu_n C_{ox}=506.449\text{uA}/V^2$$

$$\mu_p C_{ox}=220\text{uA}/V^2$$

The PMOS transistor width was chosen as $L_P = 130nm$ to minimize power consumption. Therefore:

$$L_n = L_P * \sqrt{\frac{u_n}{u_p}} = 1.52L_P = 200nm$$

The bias current I_p of the LC tank is designed to be 300 μA and the PMOS turn on voltage v_{on} is designed to be 300mV. Therefore:

$$W_P/L_P \geq \frac{2I_P}{u_P C_{ox}(v_{on})\text{^}2} = 2 * 300uA/220uA/0.09V^2 = 32$$

$$W_p \geq 9um$$

$$W_n = W_P * \frac{L_P}{L_n} = \frac{W_P}{1.52} = 6\mu m$$

$$g_{mn} = g_{mp} = \mu_n C_{ox} \frac{W_n}{L_n} I_{DS} = \frac{506uA}{V} * \frac{6\mu m}{200nm} * 300\mu A = 4.5mA/V \qquad (4.6)$$

where g_{mn} and g_{mp} are the NMOS and PMOS transconductance. Also, NMOS transistors, PMOS transistors and current mirror transistors are all biased in saturation region. As described in equation 3.5, the MOSFET transconductance needs to be greater than $\frac{2}{R_{par}}$ to sustain the oscillation, where R_{par} is the equivalent parallel resistance of the LC tank. The fixed capacitor is chosen as 17.8pF to balance the on chip space and oscillator sweeping range. Therefore, the equivalent parallel resistance can be calculated as:

$$R_{pL} = \omega * L * Q_L = 2 * \pi * 200MHz * 24nH * 24 = 724\Omega \qquad (4.7)$$

$$R_{pc} = \frac{Q_c}{\omega * C} = \frac{100}{2 * \pi * 200MHz * 17.8pF} = 4471\Omega \quad (4.8)$$

$$R_{par} = \frac{R_{pC} * R_{pL}}{R_{pC} + R_{pL}} = 623\Omega \quad (4.9)$$

where R_{pL} and R_{pc} are the equivalent parallel resistance of the off-chip inductor and fixed capacitor, respectively. Therefore, the total PMOS and NMOS transconductance ($g_{mp} + g_{mn}$) needs to be greater than 3.2mA/V (2/623Ω) and both of them need to be greater than 1.6mA/V. It should be noted that the above calculations did not take the fine tuning load into consideration. Also, the binary weighted capacitance is not loaded into the circuit. When the coarse tuning band and fine tuning band are loaded into the oscillator, the equivalent capacitance is increased and the capacitive quality factor is decreased because the NMOS transistor is connected in series with MIM-caps. Therefore, the R_{pc} is decreased; however, the R_{pL} is the dominant resistance and it does not change. Therefore, the 1.6mA/V transconductance is close to the minimum transconductance requirement. Also, the g_{mn} and g_{mp} are almost three times as large as the 1.6mA/V requirement; therefore, the oscillator should be able to oscillate with the above transistor widths.

4.4 Current Source Design

A typical current source is designed to supply bias current to the oscillator as shown in Figure 4.2. The level of the bias current decides the dc bias level and output amplitude of the oscillator. For testing purposes, M1 was sized to be the same as M2 so that the external bias current is approximately the same as the oscillator bias current (assuming both

devices are in saturation). The bias current is supplied by placing a tunable resistor between the voltage supply and the drain of transistor M2 [40]-[42]. A capacitor may be added between the gate of the NMOS transistor M1 and ground. This provides some noise filtering at the gate of the oscillator current source. Both M1 and M2 are sized to be 50μm to save power and leave a large voltage swing for the LC tank. Transistor M2 is always in the saturation region; transistor M1 is designed to have a 300mV voltage drop and a 100mV turn on voltage.

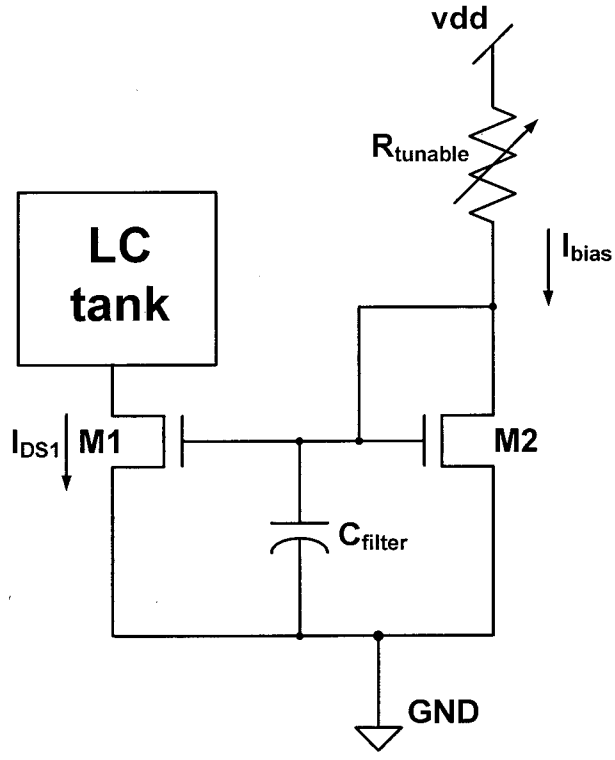


Figure 4.2: DCO Current Source

4.5 DCO Coarse Tuning Band Design

The DCO coarse tuning band contains eight groups of binary weighted switch MIM-caps in parallel with the fixed capacitor. The MIM-caps are switched in and out of the circuit

by changing the digital control bits [43]-[48]. The equivalent capacitance is roughly proportional to the MIM-cap area. Therefore, it is not the W/L ratio, but the W×L product that is important. Both the fine tuning and coarse tuning bands and their control logic are shown in Figure 4.3. The coarse tuning band switches the output frequency range from 170MHz to 220MHz and the unit coarse tuning step is calculated as:

$$\Delta f = \frac{f_{sweep}}{N} = \frac{220MHz - 170MHz}{256} = 200kHz \tag{4.10}$$

The fine tuning relies on the small deltas (5fF) between the differentially connected 200fF and 210fF caps to create small frequency steps. Therefore, if the fine tuning code is tuned from "5" to "6" with the coarse tuning code fixed, the oscillator output frequency is decreased by 20kHz (This will be explained in the following sections). The coarse tuning has 256 tuning levels and the fine tuning has 32 tuning levels resulting in an 8192 level (256 x 32) capacitance selection.

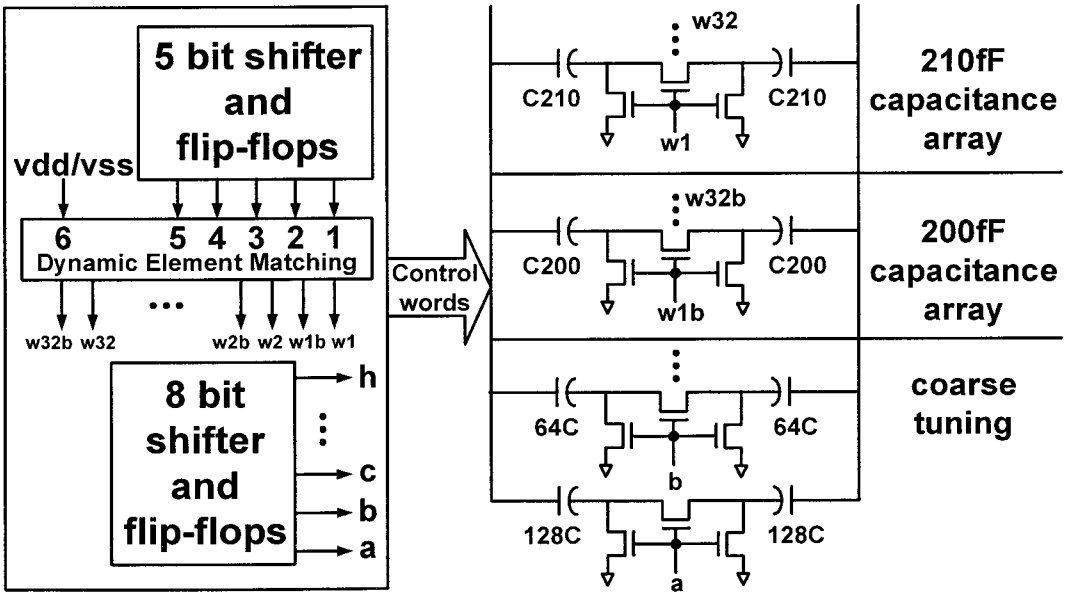


Figure 4.3: Fine Tuning and Coarse Tuning Band Architecture

The coarse tuning band is controlled by an 8-bit binary word which is loaded into the circuit by using an 8-bit shifter and 8 flip-flops [49, 50]. The loading circuit is shown in Figure 4.4. The oscillator output frequency is controlled by changing the control bits. The total capacitance contributed by the coarse tuning band is expressed as:

$$C_{coarse\_tune} = \sum_{0}^{N-1} 2^{k} \Delta C_{coarse} \tag{4.11}$$

where k is the k_{th} control bit and ΔC_{coarse} is the unit binary weighted capacitor which is equal to 138fF [51]-[53].

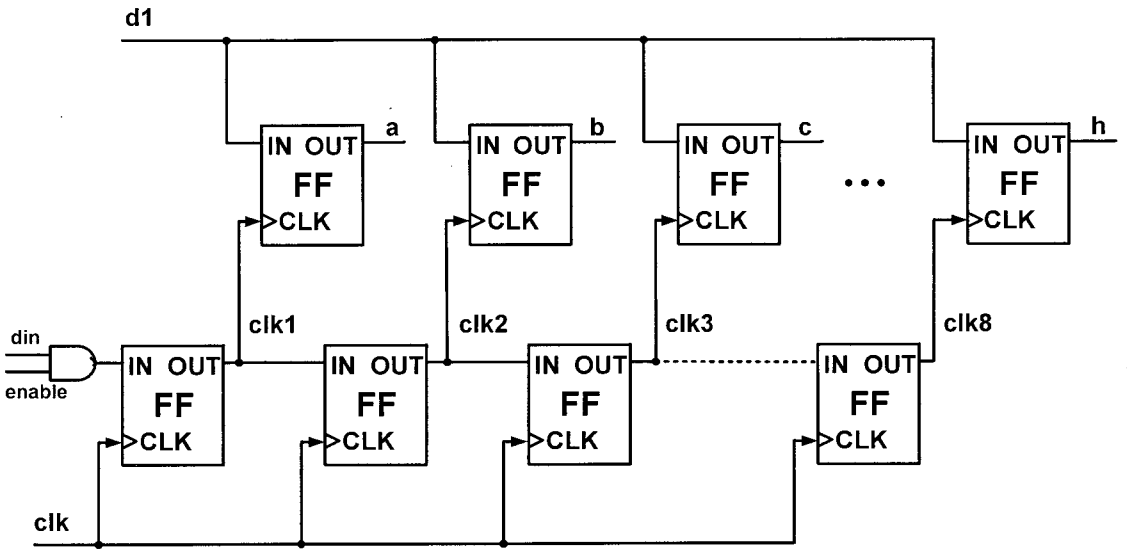


Figure 4.4: Coarse Tuning Band Input Load Circuit

Simulation and iteration are used to modify the binary weighted MIM-cap values to obtain the desired output frequency. Design considerations are summarized as below:

1. The sweeping range of 180MHz to 220MHz needs to be set first.
2. The parasitic capacitance introduced by these center NMOS transistors must be considered.

3. The centre NMOS transistor width can affect the quality factor which may affect the DCO output frequency. Also, the binary MIM-cap is comparable to the fixed MIM-cap; therefore, center NMOS transistor widths need to be large enough so that the LC tank quality factor will not be significantly affected.
4. If both the minimum and maximum oscillator output frequency need to be increased or decreased, then change only the capacitance value and keep the inductor constant.
5. The MIM-caps sizes are set group by group to make them binary weighted. When changing MIM-cap group size, the oscillator output frequency sweeping range needs to be checked again. The most significant bit is set first, and then the second significant bit and so on.
6. The routing capacitance of the off-chip inductor also needs to be considered, however, it is difficult to simulate it. Therefore, the measured output frequencies may have some deviations from the simulated frequencies.

4.6 Inductor Design

In the proposed design, the tank inductor is a high Q off-chip inductor. The inductor has a quality factor of 26 when it is operating at 250MHz [62]. The equivalent quality factor of the LC tank can be calculated by using the formula [17]:

$$Q_{total} = \frac{Q_C * Q_L}{Q_C + Q_L} \tag{4.12}$$

Therefore, the inductor quality factor will significantly affect the quality factor of the LC tank.

As a result, the inductor Q will have a strong effect on the current consumption and noise of the oscillator (a higher Q will result in a lower current consumption and lower phase noise). One way to counteract this effect would be to increase the tank g_m by increasing the NMOS and PMOS transistor size; however, this will introduce more parasitic capacitance which will reduce the tuning range. A large inductor usually has a large Q and a large parallel resistance. The parallel resistance is part of the loop gain and sets the oscillation amplitude [17]. For a given oscillator frequency, the oscillator tuning range controlled by the capacitors shrinks as the inductor value is increased. As a result, a 24nH-0603 HP off chip inductor was chosen to balance loop gain and output frequency sweeping range. This inductor has a quality factor of 26 and a tolerance of 5.2% at the 250MHz oscillator output frequency. The equivalent inductor model is shown in Figure 4.5 [62]. Where R_{var} relates to the skin effect and is calculated as:

$$R_{var} = k \bullet \sqrt{f} \tag{4.13}$$

where k is the Boltzmann constant value which equals $1.3806503 \times 10^{-23}$ m^2 kg s^{-2} K^{-1}; f is the oscillator operating frequency in Hz. At 250MHz, R_{var} is equal to 1.07Ω. $R1$ and $R2$ are the parasitic resistance which are equal to 21Ω and 0.074Ω and C is the lumped capacitance which is 0.039pF.

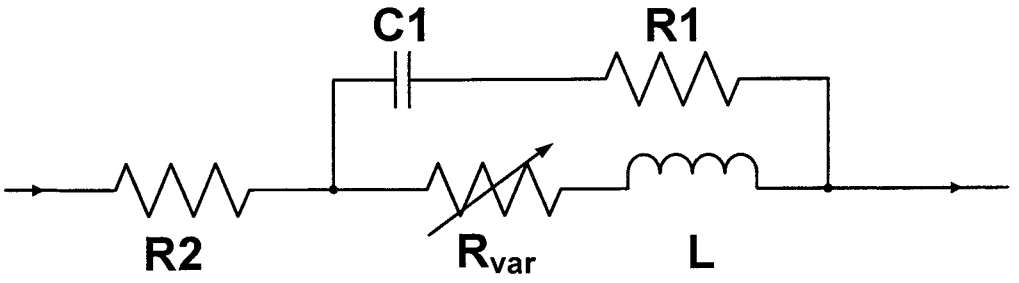


Figure 4.5: The Equivalent Lumped Inductor Element Model

4.7 DCO Fine Tuning Design

The coarse tuning range of the DCO can be achieved by sizing the binary weighted capacitors; however, the fine tuning band is sensitive to the capacitor process variations [54]. Therefore, the DEM technique is implemented to reduce these variations.

4.7.1 Quality Factor Discussion

Since the fine tuning switch MIM-caps are in parallel with the fixed capacitor and coarse tuning switch MIM-caps, the equivalent circuit is shown in Figure 4.6.

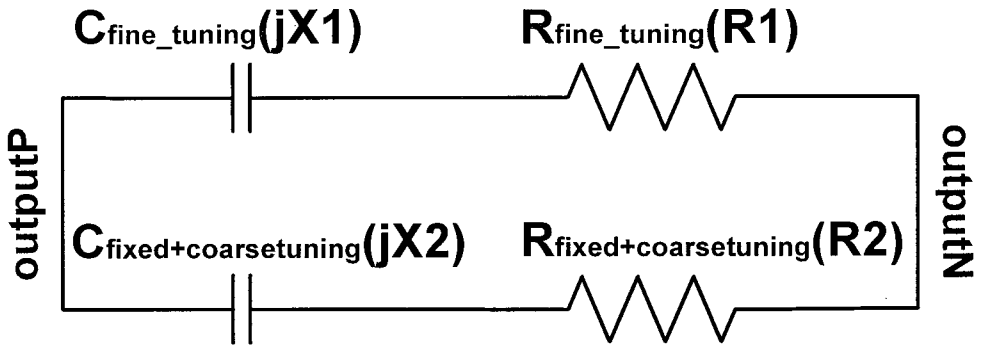


Figure 4.6: The Equivalent Circuit of the fixed MIM-cap and Coarse Tuning Band in parapllel with the Fine Tuning Switch MIM-caps

The equivalent impedance of the top branch and bottom branch are equal to:

$$Z1 = jX1+R1, \tag{4.14}$$

$$Z2 = jX2+R2, \tag{4.15}$$

where $X1 = -\frac{1}{\omega C1}$ and $X2 = -\frac{1}{\omega C2}$.

Therefore, the equivalent impedance of both branches is calculated as:

$$Z_{eq} = \frac{Z1*Z2}{Z1+Z2} = \frac{(jX1+R1)*(jX2+R2)}{(jX1+R1)+(jX2+R2)} \tag{4.16}$$

The switch MIM-cap series resistance is composed of the MIM-cap's equivalent series resistance and the equivalent resistance of the NMOS switch. In Figure 4.6, R1 is the equivalent series resistance of the fine tuning switch MIM-caps whose switches are enabled. R2 is the equivalent series resistance of the coarse tuning switch MIM-caps whose switches are enabled in parallel with the fixed MIM-cap. With the minimum frequency operating at 170MHz (with all the coarse tuning switches enabled which is the worst case scenario) and the inductor value to be 24nH, the total capacitance is calculated as 36.5pF (the off-chip parasitic capacitance is not included). The fine tuning band has a 3.2pF default capacitance which will be discussed in the section 4.7. Therefore, the fixed capacitance in parallel with all the coarse tuning capacitance is calculated as 33.3pF (36.5pF – 3.2pF). Therefore, the sum of the fixed capacitance and coarse tuning capacitance is much greater than the 3.2pF fine tuning capacitance. X2 is much smaller than X1. Because the quality factor of the MIM-cap is close to 100 [65], the fixed MIM-cap resistance is calculated as:

$$r_{serial\_fixed} = \frac{1}{\omega C Q_c} \tag{4.17}$$

There are no switches in series with the fixed MIM-cap, and its quality factor is high. Therefore, the resistance in series with the MIM-cap is low. Also, this fixed MIM-cap series resistance is in parallel with the coarse tuning band serial resistance. As a result, the equivalent resistance of R2 is small. The above equation can be simplified as:

$$Z_{eq} = \frac{j(R1*X2+R2*X1)+ R1*R2-X1*X2}{R1+jX1} \tag{4.18}$$

With both the numerator and denominator multiplied by $1 - jX1$, the following equation can be deduced:

$$Z_{eq} = \frac{j(R1^2 * X2 + X1^2 * X2) + R1^2 * R2 - R2 * X1^2}{R1^2 + X1^2} \tag{4.19}$$

therefore:

$$R_c = \frac{j(R1^2 * X2 + X1^2 * X2)}{R1^2 + X1^2}, \quad r_s = \frac{R1^2 * R2 + R2 * X1^2}{R1^2 + X1^2} \tag{4.20}$$

$$Q_{eq} = \frac{1}{|C_{eq} * \omega| * r_s} = \frac{R_c}{r_s} = \frac{R1^2 * X2 + X1^2 * X2}{R1^2 * R2 - R2 * X1^2} \tag{4.21}$$

With both numerator and denominator divided by $R1^2$, the following equation can be deduced:

$$Q_{eq} = \frac{1}{|C_{eq} * \omega| * r_s} = \frac{R_c}{r_s} = \frac{X2 + X1^2 * X2/R1^2}{R2 - R2 * X1^2/R1^2}$$

Since $X2$ and $R2$ are small, the above equation can be further simplified as:

$$Q_{eq} = \frac{1}{|C_{eq} * \omega| * r_s} = \frac{R_c}{r_s} = \frac{X1^2 * X2/R1^2}{R2 * X1^2/R1^2} = \frac{X2}{R2} = \frac{1}{\omega C2 R2} = Q_2 \tag{4.22}$$

Since the large fixed capacitor and the coarse tuning band capacitors dominate the overall capacitive quality factor, large fine tuning switches are not required. Also, because the fine tuning MIM-caps are small, minimum size NMOS transistors can be used for conduction.

The coarse tuning switches are in series with the MIM-caps, and they can reduce the MIM-cap quality factor significantly if their equivalent resistance is large. Also, large MIM-caps are used in the coarse tuning band and the NMOS transistor width can affect the MIM-cap conductivity. Therefore, the coarse tuning band switches are sized to be

large so that their equivalent resistance is small. The coarse tuning MIM-caps are binary weighted; therefore, the coarse tuning switches are also binary weighted (The largest switch is sized to be 100μm in width, the second largest one is 50μm; etc).

4.7.2 DCO Fine Tuning Switch MIM-cap Branch Design

As shown in Figure 4.3, the fine tuning band includes the DEM control block and two arrays of thermo-weighted switch capacitors. The 200fF capacitors are chosen as the small capacitors which can be achieved in 0.13μm technology. At the default state, all the fine tuning control bits are set low to load all the 200 fF capacitors into the circuit and disconnect all the 210 fF capacitors. A minimum of 3.2 pF of capacitance is loaded into the circuit by the fine tuning band. The fine tuning switch MIM-cap group step size can be calculated to achieve the desired 40kHz frequency resolution. The DCO output frequency is calculated as:

$$f = \frac{1}{2\pi}\left(\sqrt{\mathrm{L}(\mathrm{C_{fixed}} + \mathrm{C_{coarse}} + \mathrm{C_{fine}})}\right)^{-1} \tag{4.23}$$

According to[44, 55, 56], a small frequency step change will result in:

$$\frac{df}{dC} = -\frac{1}{2\pi\sqrt{LC}} * \frac{1}{2C} = \frac{\Delta f}{\Delta C} \tag{4.24}$$

or

$$\Delta f = -\frac{1}{2\pi\sqrt{LC}} * \frac{1}{2C} * \Delta C = -f_0 * \frac{1}{2C} * \Delta C \tag{4.25}$$

where Δf is the fine tuning step size, f_0 is the operating frequency, ΔC is the fine tuning unit step capacitance, and C is the sum of the fixed capacitance, coarse tuning

switch capacitance and the fine tuning default capacitance. Therefore, the following equation is derived:

$$\frac{\Delta f}{f_0} = \frac{-f*\Delta C}{2*C*f} = -\frac{\Delta C}{2C} \tag{4.26}$$

which indicates that the relative frequency resolution is proportional to the change in capacitance [44,55,56]. In addition, the fixed capacitance contributes 17.8pF to the oscillator and there is 3.2pF default capacitance contributed by the fine tuning band. The minimum thermo-weighted MIM-cap step size is calculated as:

$$\Delta C = \frac{\Delta f}{f_0} * 2C = \frac{40kHz}{220MHz} * 2 * (17.8pF + 3.2pF) = 7.64\text{fF} \tag{4.27}$$

The above equation shows the MIM-cap step size must be less than 7.64fF to achieve a 40kHz frequency resolution. As a result, a 5fF capacitor step size is chosen with approximately 52% tolerance. Since all switch capacitors are connected differentially, this corresponds to a 10fF step capacitance between these two thermo-weighted MIM-cap arrays. Therefore, the second thermo-weighted MIM-cap array has values of 210fF.

As discussed in section 4.4, the center connected NMOS transistors are used only for conductivity and these fine tuning capacitors are very small. The minimum transistor width is chosen for all these fine tuning groups.

4.7.3 Absolute and Relative MIM-cap Process Variations and Mismatches

The absolute capacitor process variations are the absolute discrepancies from the desired capacitor value in different chips which can be up to ±20% of the desired capacitor value [67]. The relative process variations define the capacitors' discrepancies from each other on the same chip. These capacitors on a single chip can all be above or below the desired

capacitor value and their relative discrepancies are between 0.2% and 0.5% of the absolute capacitor value if the capacitors are designed using careful layout practices [67]. However, the relative process variations in each chip have a significant effect on the frequency resolution [54].

4.7.4 Dithering Effect on DCO Fine Tuning Band

The 200fF switch capacitor groups are connected to the oscillator when the appropriate control bit is "low" whereas the 210fF switch capacitor groups are connected when the same control bit is "high". As discussed in section 3.8, the DEM block dithers between these 200fF and 210fF capacitor arrays. The process variations for these MIM-caps are assumed to be Gaussian random variables; therefore, the one sigma (σ) standard deviation is calculated to be 1.05fF (210fF * 0.5%). To maintain a high chip yield it would be desirable to have a design which could support a worst case variation of 4 to 5 σ. Using a variation of 4.5σ or (4.725fF) would include approximate 99.9% of all capacitors. Since there are 64 fine tuning capacitors, .999^64 = .938 or 93.8% of the chips will have all the capacitors in this range. Therefore, the discrepancy can be up to 95% (i.e. 4.725pF) as much as the 5fF capacitor step size. With the random dithering between these two capacitor arrays, the resulting standard deviation of the mean is decreased and can be calculated as [63]:

$$SD = \frac{\sigma}{\sqrt{n}} \tag{4.28}$$

where σ is standard deviation, and n is the size of each array which is equal to 8 (The fine tuning code 4 to 28 is used to ensure a minimum of 8 fine tuning capacitors are

dithered at any given time). This results in an equivalent 4.5σ capacitance deviation of 1.67fF and limits the process variations and mismatches to 33.4% of the minimum step size. For an input fine tuning code value "t", the total capacitance contributed by the fine tuning band is equal to:

$$C_{fine} = 200fF * (32 - t) + 210fF * t \pm 1.59fF * (32 - t) \pm 1.67fF * t \quad (4.29)$$

where the 1.59 fF and 1.67 fF are the 4.5σ variations for the 200fF and 210fF capacitance.

4.8 Buffer Stages Design and Simulation

The DCO top level module is shown in Figure 4.7 and the transistor level output buffer is shown in Figure 4.8. Figure 4.8 is composed of a differential to single ended converter, a common source amplifier and an inverter. The differential to single ended converter does not have enough output swing to drive an output load. Therefore, a common source amplifier is used to amplify the signal before it is fed to the inverter to generate a rail to rail square wave.

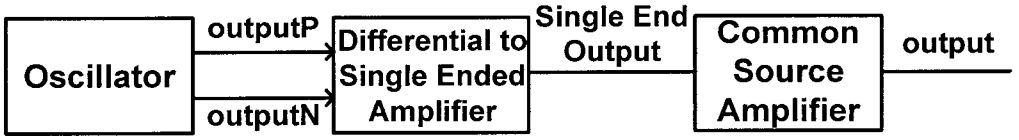


Figure 4.7: Oscillator Core Cascaded with Buffer Stages

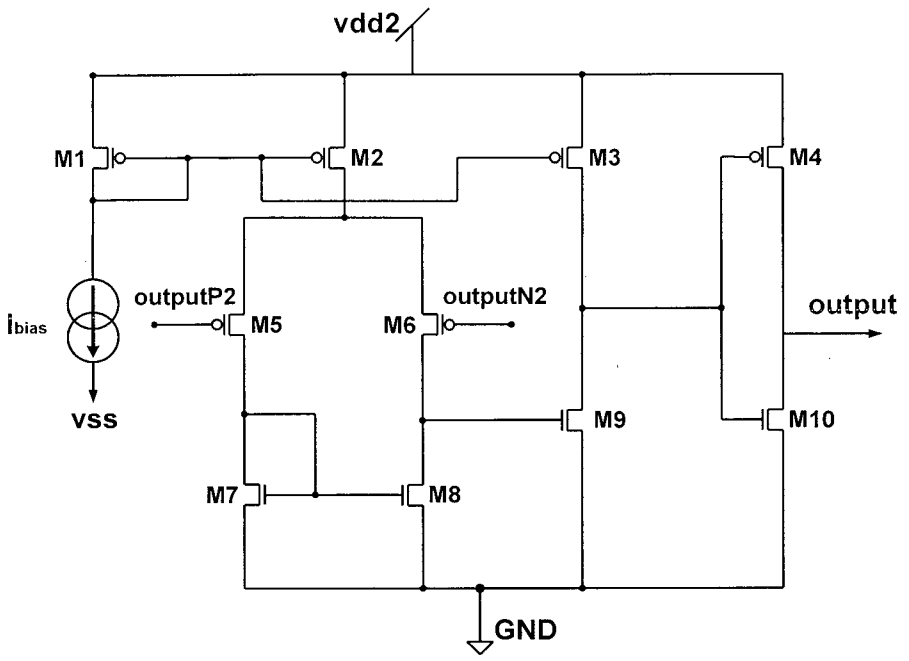


Figure 4.8: Differential to Single-ended Buffer Cascade with a Common Source Amplifier and Digital Inverter

The buffer stage has an independent 1.2V voltage supply. A 50μA bias current is chosen to bias the differential to single ended buffer and the common source amplifier. The PMOS current mirror is used to supply bias current. All these transistors are biased in the saturation region; therefore, the bias current is calculated as:

$$I = \frac{1}{2}\mu C_{ox}\frac{W}{L}(v_{GS} - V_{th})^2 \tag{4.30}$$

The transistor width is calculated as:

$$W = \frac{2*I*L}{\mu C_{ox}(V_{eff})^2} \tag{4.31}$$

where $V_{eff} = v_{GS} - V_{th}$ is the effective voltage.

The voltage drop across these PMOS current mirror transistors are designed to be 450mV and the threshould voltage is estimated as 300mV. The $\mu_p C_{ox}$ is equal to 220.2uA/V^2 in 0.13μm technology. Therefore, PMOS current mirror transistors widths

(M1, M2, M3) are calculated as 6μm. The minimum output frequency amplitude is designed to be 100mV peak to peak. Therefore, the cascaded buffer stages aim to achieve a voltage gain of 15. The differential to single ended buffer stage aims to achieve a gain of 3 and the common source amplifier has a gain of 5. The differential to single ended amplifier gain is given by the formula below:

$$A_v = g_{m5}\left(\frac{r_{ds6} * r_{ds8}}{r_{ds6} + r_{ds8}}\right) \tag{4.32}$$

where g_{m5} is the transconductance of transistor M5; r_{ds6} and r_{ds8} are the output impedance of transistor M6 and M8. The output impedance can be approximated by the formula:

$$r_{ds} = \frac{1}{\lambda I_{ds}} \tag{4.33}$$

Also, the bias current across each transistor M6 and M8 is 25μA. Where λ is the channel length modulation in 0.13μm technology. Therefore, their output impedance is approximately calculated as 80kΩ each. This results in an equivalent 40kΩ output impedance and g_{m5} is calculated to be 7.5μA/V. Different transistor sizes are simulated in Cadence, and transistor widths of M5 and M6 are chosen to be 9μm. The widths of transistor M7 and M8 are sized to be 2μm.

The common source amplifier gain is given by the formula below:

$$A_v = g_{m9}\left(\frac{r_{ds3} * r_{ds9}}{r_{ds3} + r_{ds9}}\right) \tag{4.34}$$

where g_{m9} is the transconductance of transistor M9; r_{ds3} and r_{ds9} are the output impedances of transistors M3 and M9, respectively. The equivalent output impedance of M3 and M9 is calculated to be 200kΩ. Therefore, g_{m9} is calculated to be 25μA/V and transistor M9 is sized to be 4μm.

In order to achieve a high slew rate, the inverter PMOS transistor is sized to be three times as large as the PMOS current mirror transistor and its NMOS transistor is sized to be three times as large as the common source NMOS transistor.

A 50mV peak to peak sin wave was used to test the oscillator buffer stages and the simulation results are shown in Figure 4.9. Figure 4.9 shows the output voltage after the differential to single ended output is 170mV with a voltage gain of 3.4. The output voltage after the common source amplifier is 1.07V with a voltage gain of 6.24.

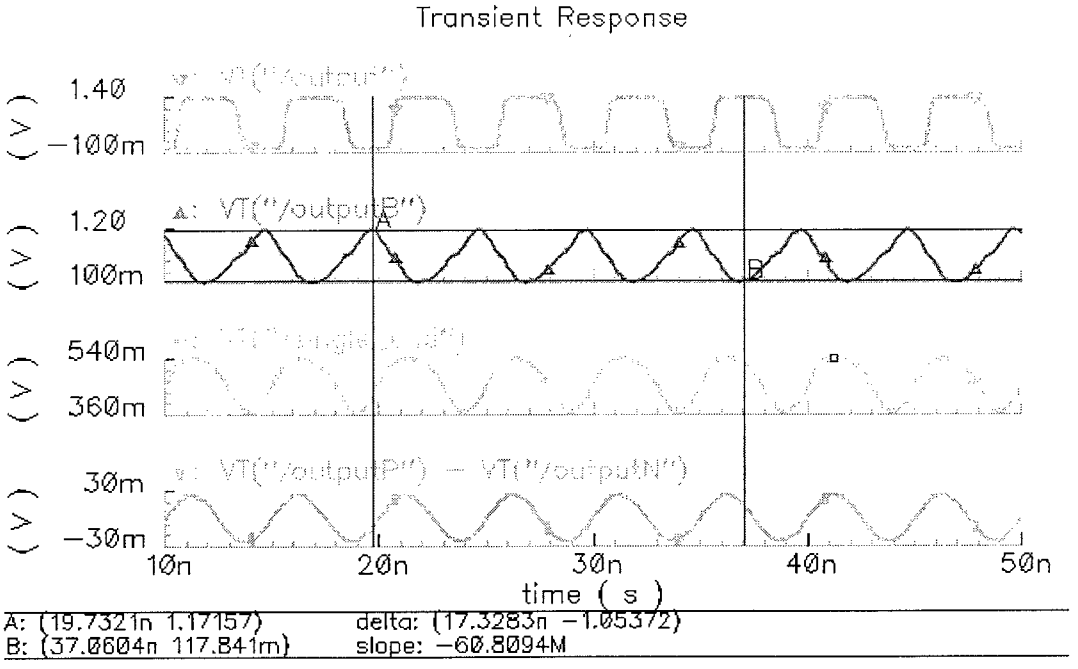


Figure 4.9: Simulated Buffer Stages

4.9 Model of off-chip Parasitics

The off-chip parasitic inductors, capacitors and resistors can affect the oscillator output frequency. They may even affect whether the oscillator is going to oscillate or not. Therefore, these parasitics must be considered in the design stage and they need to be modelled in the simulator. The off-chip parasitics are modelled and shown in Figure 4.10.

The 24 pin Ceramic Flat Pack (CFP) was chosen as the chip package so that the parasitics introduced by bondpads and bondwires are minimized. As shown in Figure 4.5, the off chip inductor also introduces parasitics as discussed in section 4.6. In simulation, the on-chip routing and bondpad parasitic capacitance and routing capacitance between bondpad and oscillator outputs are estimated to be 0.5pF in total. The capacitance between bondwires is estimated to be less than 100fF and the serial parasitic inductance of the bondwires is estimated as 2nH with a Q of 50. Therefore, its parallel parasitic resistance is calaulated to be 68Ω. Each pin package and pcb trace have a parasitic capacitance of 2pF and 3nH series parasitic inductance.

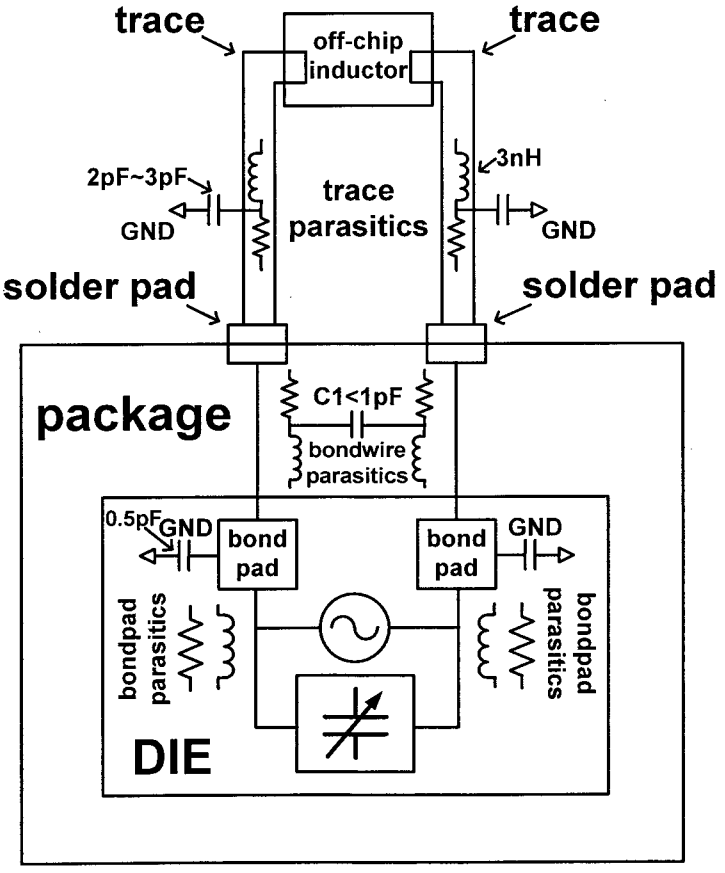


Figure 4.10: Off Chip Parasitics Model

4.10 Design and Simulation of Digital Cells

CMOS topologies are used in all the digital cells. The mobility of the NMOS transistor is more than twice the value of the PMOS transistor in the 0.13μm CMOS technology. Therefore, a 2 to 1 ratio between the PMOS and NMOS transistor widths is used in all these digital cells to achieve an approximately equivalent rising and falling time. A single inverter is built with the PMOS transistor width to be 2μm and NMOS transistor width to be 1μm. The minimum transistor width is not used because it may complicate the routing between digital cells. The MUX gate, which is used to build the switching block, is shown in Figure 4.11. The simulated MUX gate waveform is shown in Figure 4.12. In the MUX gate, M1 to M4 are sized to be twice as large as M9 and M11. Transistors M5 to M8 are sized to be twice as large as M10 and M12. Therefore, these cascaded transistors have approximately the same rising time and falling time as inverters. Figure 4.12 shows the output signal follows the input "b" when the "select" is high; when the "select" is low, the output follows input "a".

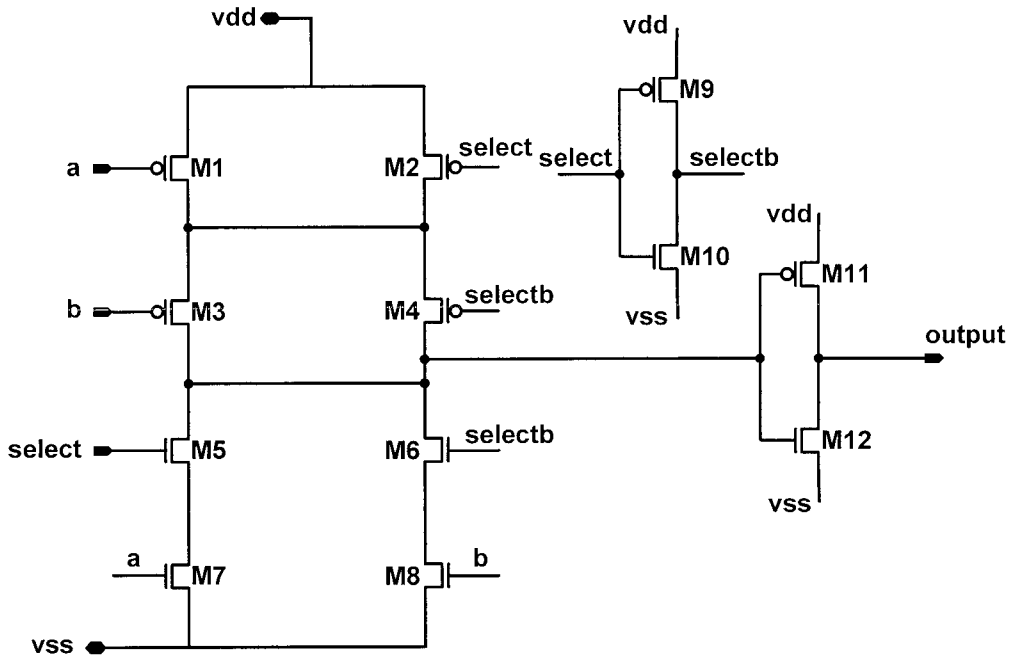


Figure 4.11: MUX Gate

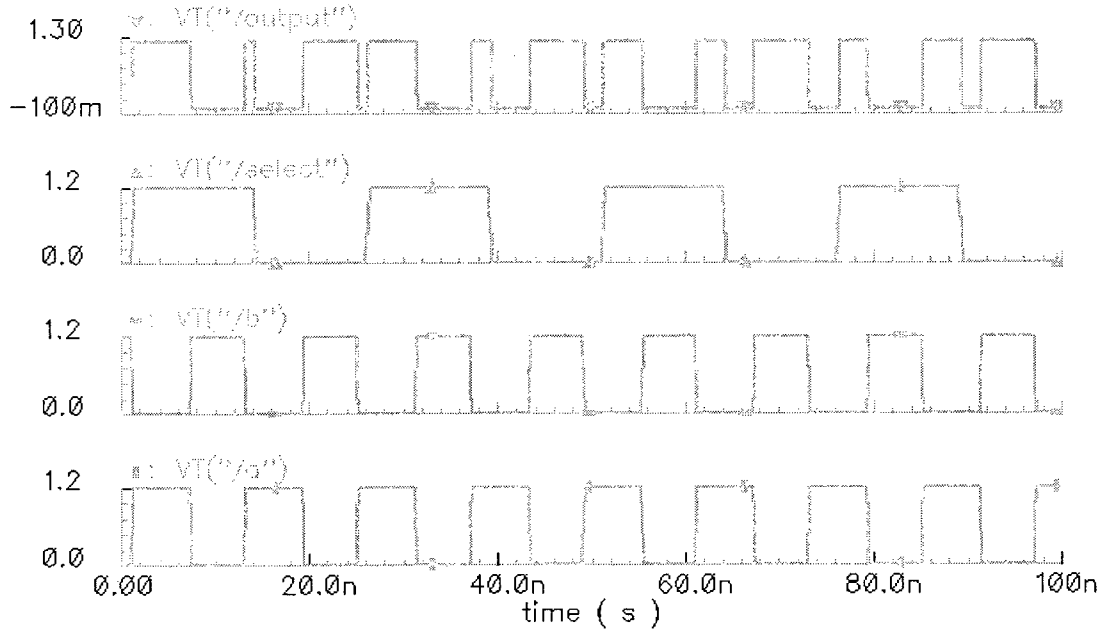


Figure 4.12: Simulated MUX Gate

The XOR gate (used to construct the switching block) is drawn in Figure 4.13 and the simulated waveform is shown in Figure 4.14. The transistors are sized the same as the MUX gate. Figure 4.14 shows the "OUT" is 0 when both input "a" and "b" are high or low; otherwise, the "OUT" is 1.

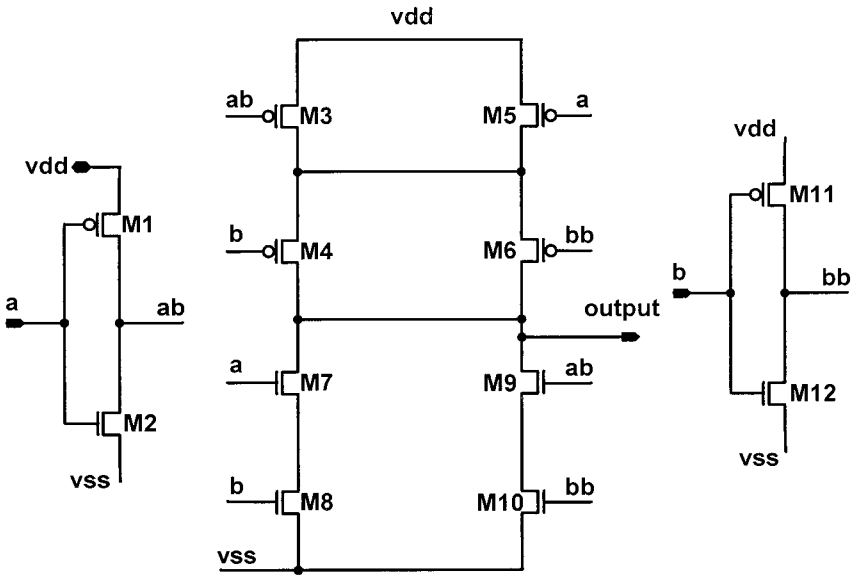


Figure 4.13: XOR Gate

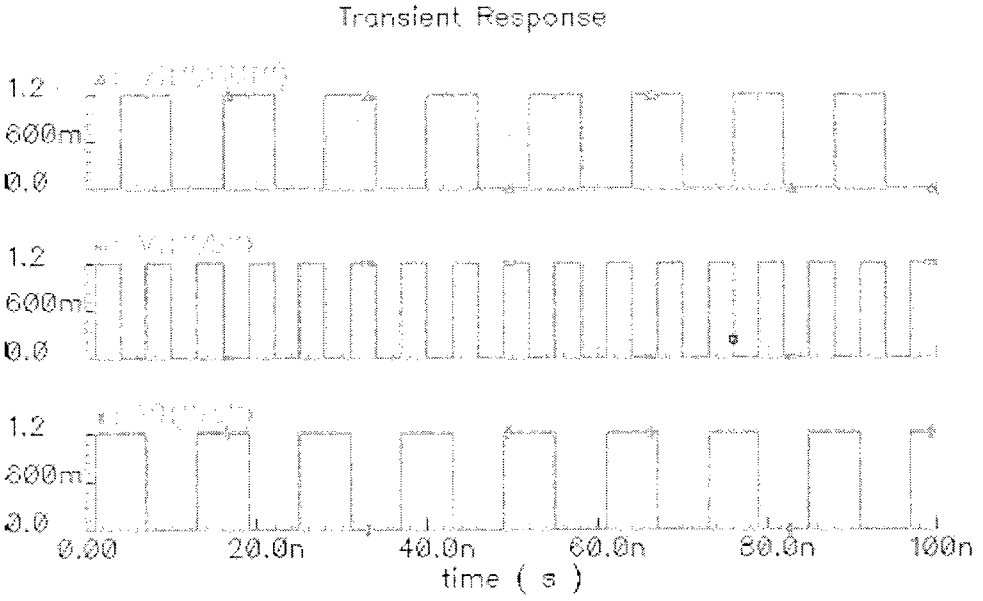


Figure 4.14: Simulated XOR Gate

The CMOS flipflop is used to build the shifters, the input loading circuit and the switching block. The flipflop is drawn in Figure 4.15, and the simulated waveform is shown in Figure 4.16. The transistors are sized the same way as the MUX and XOR gates where "d1" is the input, "clk" is the clock signal and "q" is the flipflop output signal. Figure 4.16 shows that "q" stores the input "d1" at each clock rising edge until the next clock rising edge. Therefore, the flipflop works correctly.

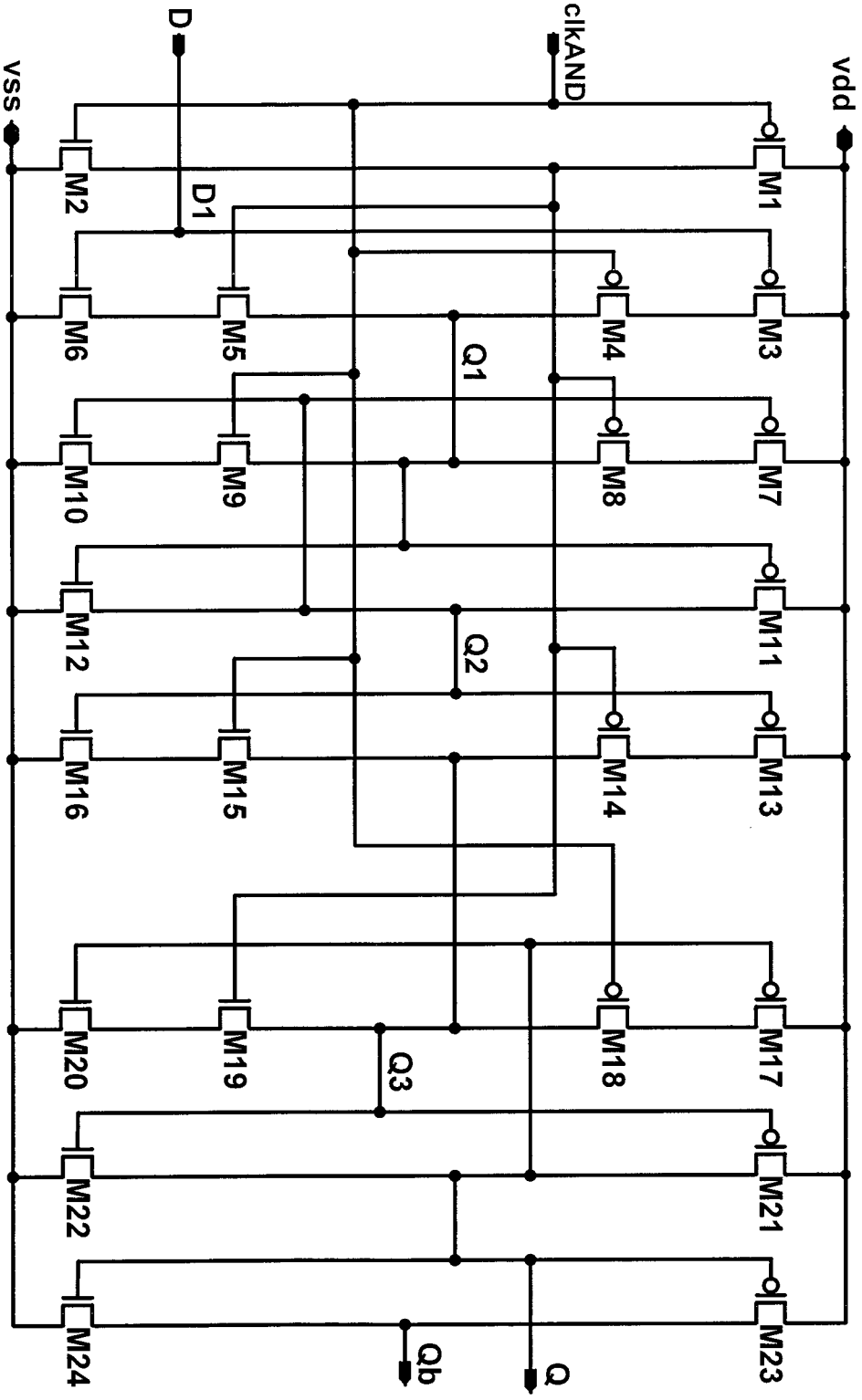


Figure 4.15: CMOS Flipflop

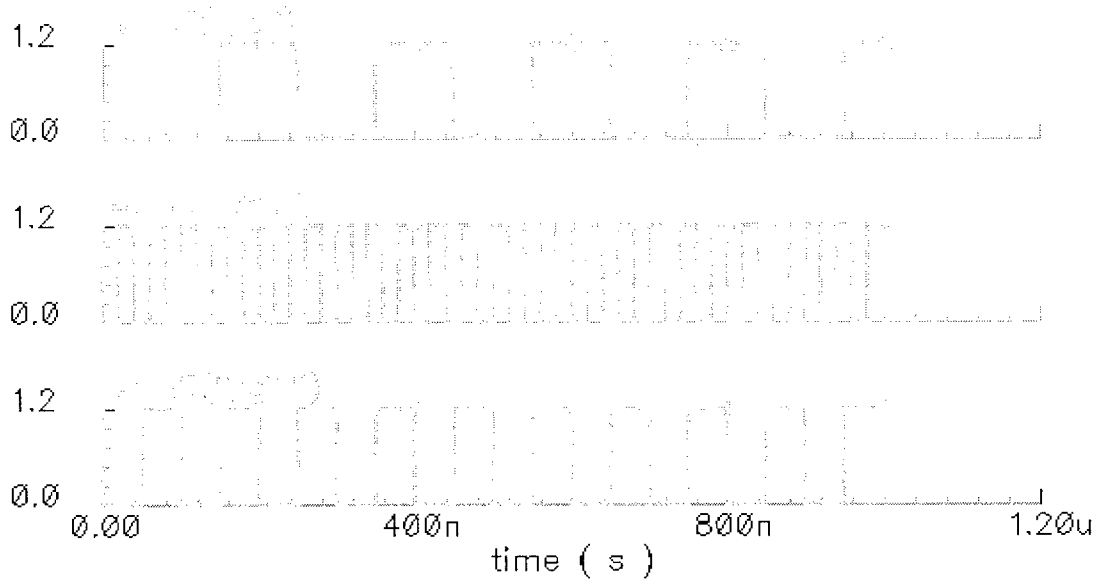


Figure 4.16: Simulated CMOS Flipflop

The designed DEM shifter (used for loading the input bits) is shown in Figure 4.17 and its simulated waveform is shown in Figure 4.18 where "clk_in" is the clock signal; "din_dem" is the input signal of the DEM shifter and "clk1" to "clk6" are the output signals of the DEM shifter. Figure 4.18 shows each output signal has one clock cycle delay which agrees with the design expectation.

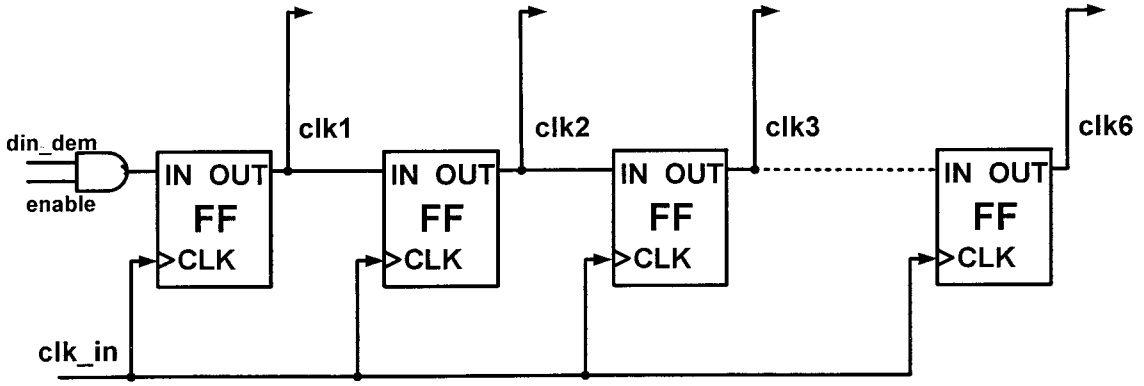


Figure 4.17: Designed Shifter

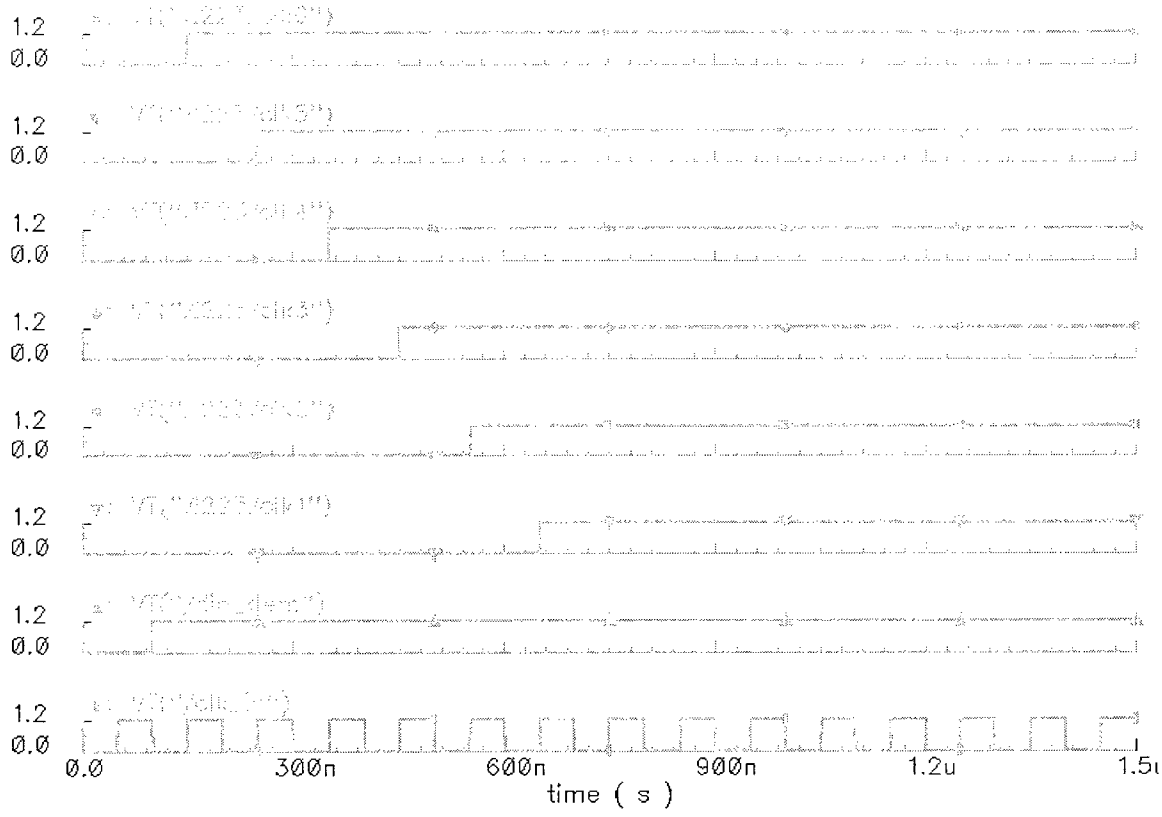


Figure 4.18: Simulated Shifter Waveform

The designed DEM fine tuning band input load circuit (used for loading the input bits into the oscillator) is shown in Figure 4.19, and its simulated waveform is shown in Figure 4.20 where "clk_in" is the clock signal, "din_dem" is the input signal of the DEM shifter and "clk1" to "clk6" are the output signals of the DEM shifter which are used to clock the fine tuning control word. The signal "d1_dem" is the fine tuning control word and signals "d1" to "d6" are the signals loaded into the DEM block to control the fine tuning band. Figure 4.20 shows the control word "dem(111101)" is received by the DEM block after six clock cycles. This can be read by the final output values from "d1" to "d6".

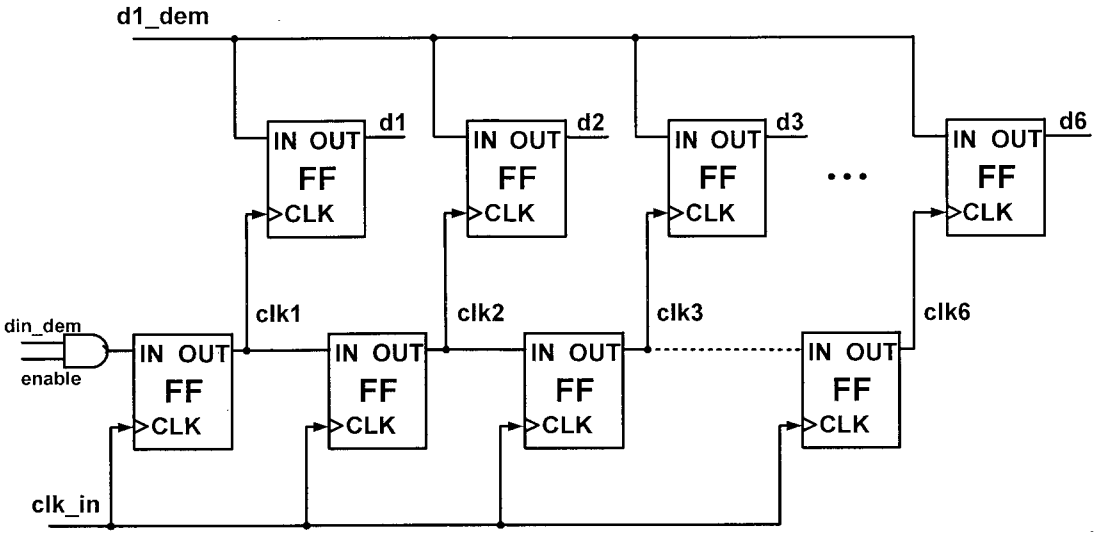


Figure 4.19: Fine Tuning Band Input Load Circuit

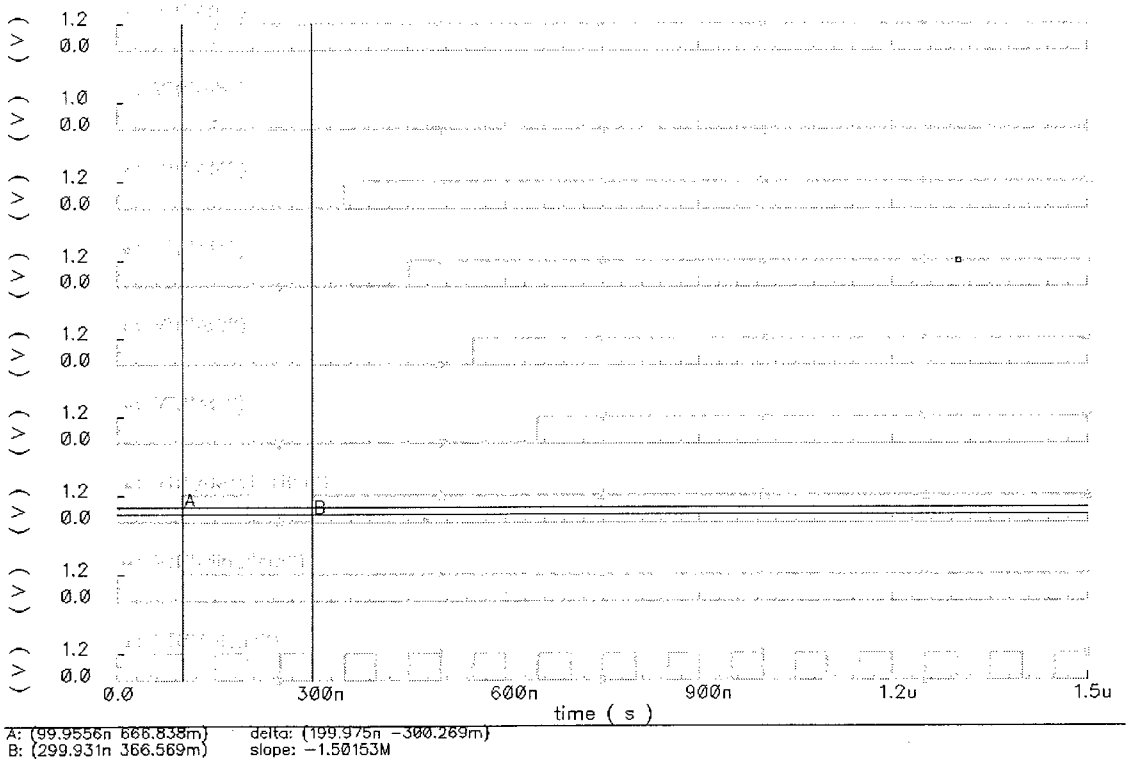


Figure 4.20: Fine Tuning Band Input Load Circuit Waveform

All the basic digital cells used to build the switching block were given and the switching block was drawn in Cadence. The 32-level tree structured digital encoder was designed and simulated. The numerical numbers ranging form 0 to 32 were all simulated and the output waveform conformed to the expected digital logic. A certain number of random "1s" and "0s" were generated by the tree structured decoder at each clock cycle. Therefore, the tree structured digital encoder was found to be working correctly.

4.11 Transient Analysis Simulation Results

The oscillator open loop feedback gain was simulated and the simulated waveform is shown in Figure 4.21. The "input_voltage" is the AC input voltage used to test the gain and "output" is the oscillator output waveform. Figure 4.21 shows that the oscillator output is approximately 3.6 times as much as the input. Therefore, the oscillator should be able to oscillate. The oscillator cascaded with the buffer stages and the parasitics introduced by bondpads, bondwires and off-chip inductor was modelled and simulated. Transient analysis was used to determine the output frequency and the oscillating waveform in the time domain. The oscillator output frequency at 220MHz is shown in Figure 4.22. The oscillator output frequency at 170MHz after the buffer stages is shown in Figure 4.23. The output frequency versus time plot is shown in Figure 4.24 with an 58nH inductor (as discussed in chapter 5) being used. An expanded view of the flat part of the curve is also shown in Figure 4.25 in order to see the variations clearly.

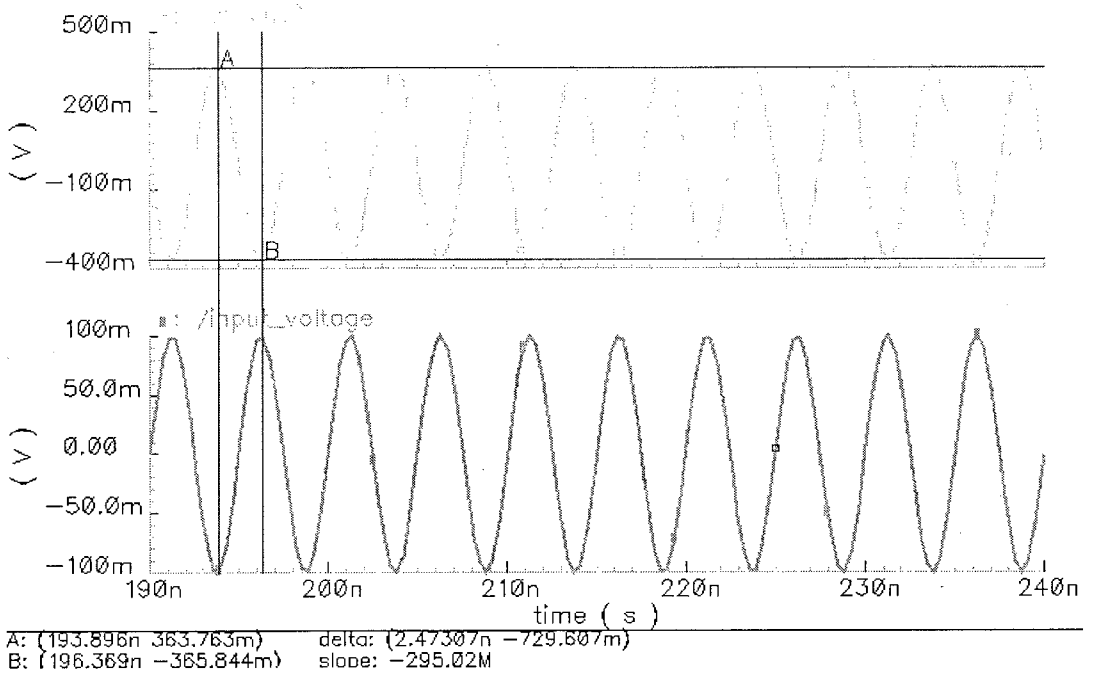


Figure 4.21: Open Loop Feedback Gain

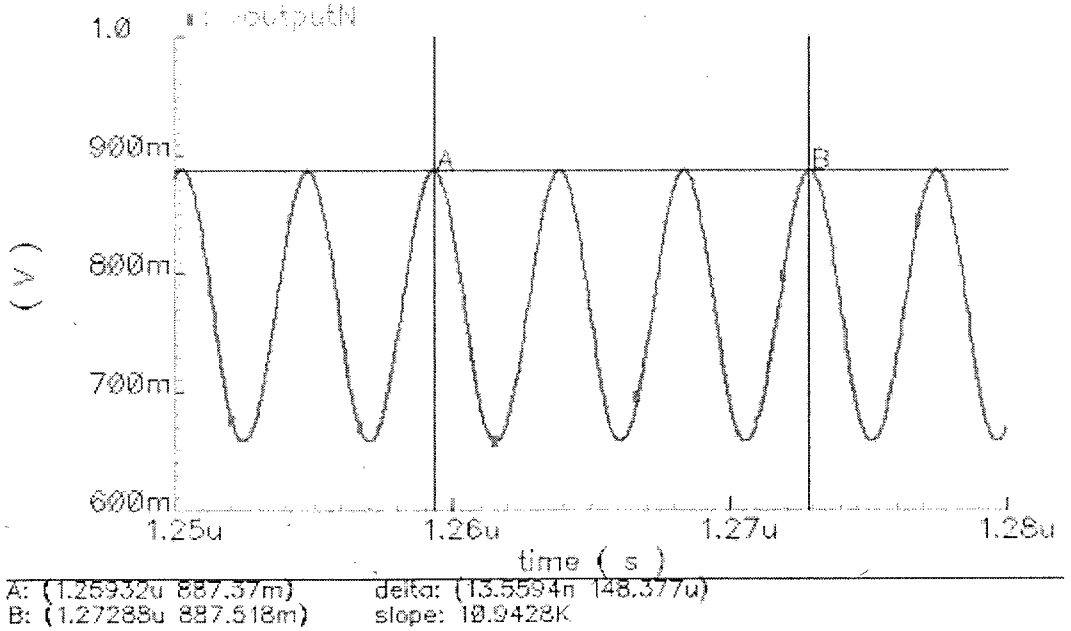


Figure 4.22: Oscillator Output Frequency at 220MHz (minimum tuning codes)

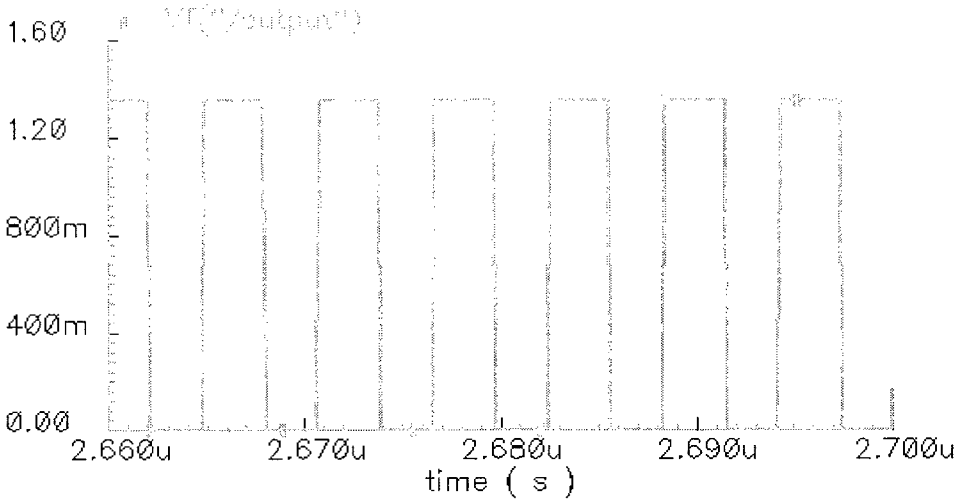


Figure 4.23: Oscillator Output Frequency at 170MHz (maximum tuning codes)

Figure 4.22 and Figure 4.23 show that when the control bits switch from 0000,0000(coarse tuning) + 000,000 (fine tuning) to 1111,1111 (coarse tuning) + 111,111 (fine tuning), the load capacitance increases to its maximum value and the minimum output frequency is obtained.

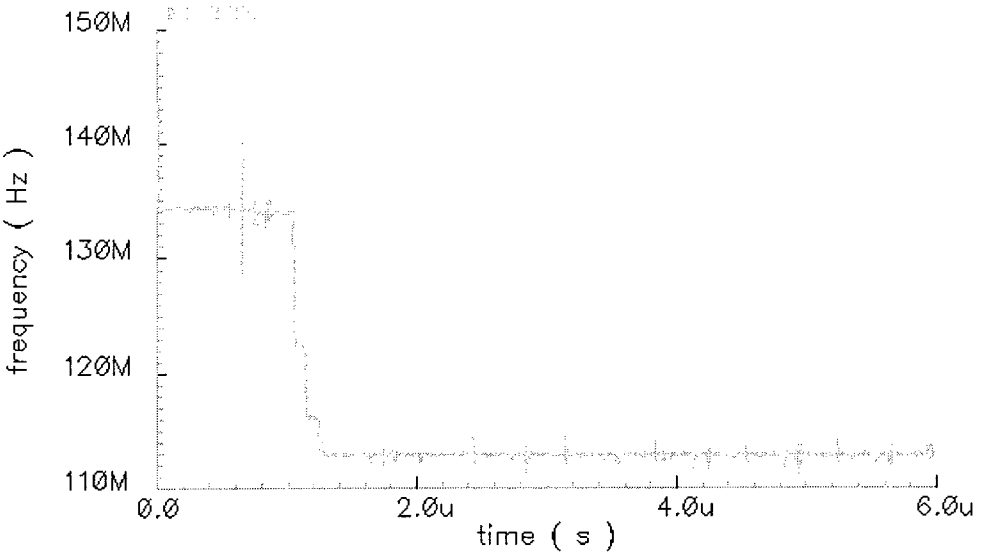


Figure 4.24: Output Frequency vs Time with 50nH Inductor and Fine Tuning Code 3

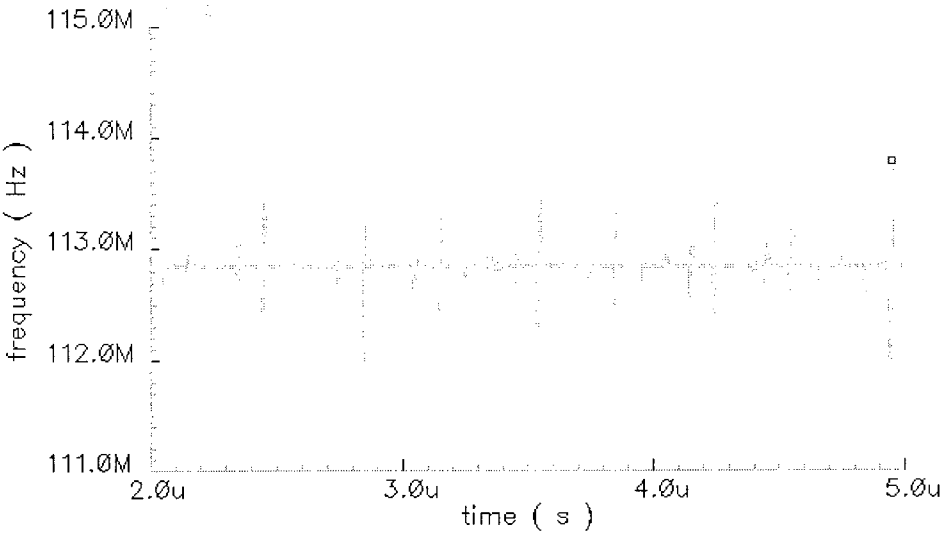


Figure 4.25: Flat Curve of Output Frequency vs Time with 50nH Inductor and Fine Tuning Code 3

Figure 4.24 shows all the control bits are loaded into the oscillator at 1.3μs. Figure 4.25 shows the effects of capacitor process variations (flat part of curve) and mismatches. These variations and mismatches average out over the time domain but at individual time points there are slight variations in frequency. When the 200fF capacitors were switched out there was a certain window of time when the 210fF capacitors had not yet switched into the circuit. This resulted in large frequency deviations. This problem can be fixed by implementing a control block which will do the following in order. The first 210fF cap will be switched into the circuit and a few pico seconds later the first 200fF cap will be switched out. It will then continue on to the second 210fF cap and then the second 200fF cap and so on until all the capacitors have been switched in this way.

4.12 Simulation Results with 58nH Inductor

It should be noted that during testing it was found that a 58nH off-chip inductor was required to provide stable operation over a wide tuning range (this will be discussed in more detail in chapter 5). Therefore, the fine tuning step size is recalculated here using a 58nH off-chip inductor. The coarse tuning band contributes 11.47pF capacitance at 112.811MHz oscillator output frequency. Therefore, the fine tuning step needs to be recalculated as:

$$\Delta f = \frac{\Delta C}{2C} * f_0 = \frac{5fF}{2*(17.8pF+3.2pF+11.47pF)} * 112.811MHz = 8.7\text{kHz} \quad (4.35)$$

The coarse tuning step size needs to be recalculated as:

$$\Delta f = \frac{f_{sweep}}{N} = \frac{136MHz-112.8MHz}{256} = 90kHz \quad (4.36)$$

where f_{sweep} is the oscillator output frequency sweeping range and N is the number of fine tuning steps.

Using a 58nH off-chip inductor, the fine tuning codes ranging from 0 to 32 are simulated and summarized in Figure 4.26 and Figure 4.27. The best-fit curve of the dithered output frequency is plotted in Figure 4.26 and its slope is 0.0079. This indicates the fine tuning band has an average 7.9kHz step size. The Integral Nonlinearity (INL) Error is defined to be the deviation from a straight line. The best-fit curve is used as the straight line such that the maximum difference is minimized. Therefore, those frequency points that are closer to "x = 0" have less deviation from the ideal frequency. Figure 4.27 shows the deviation of the dithered ouput frequencies are much less than the non-dithered output frequencies. In conclusion, the frequency resolution is improved with dithering.

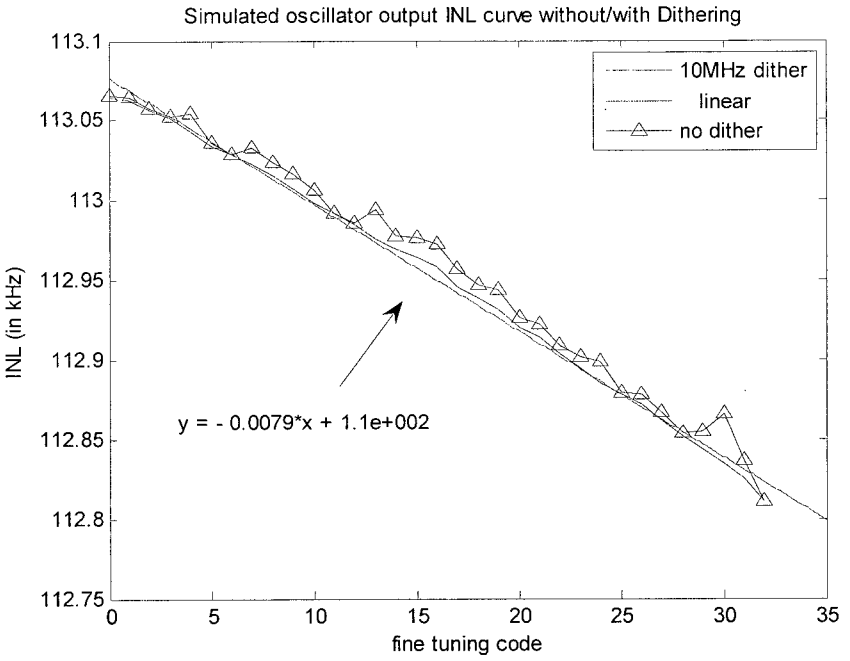


Figure 4.26: Simulated Fine Tuning Steps without/with Dithering

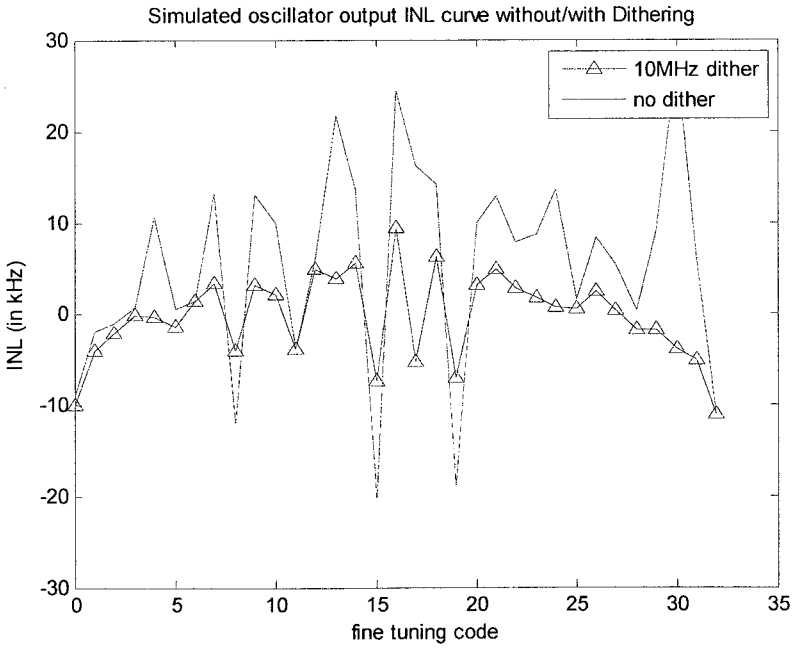


Figure 4.27: The INL of Simulated Fine Tuning Steps without/with Dithering

The minimum output frequency of 112.811MHz and the maxiimum output frequency at 136.231MHz were simulated with 58nH inductor and shown in Figure 4.28 and Figure 4.29.

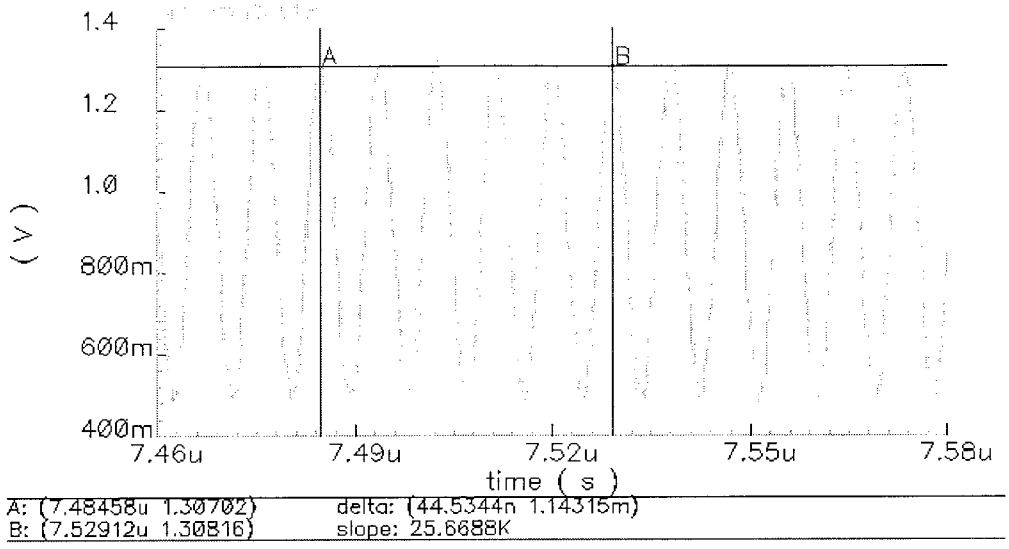


Figure 4.28: Minimum coarse tuning frequency at 112.811MHz

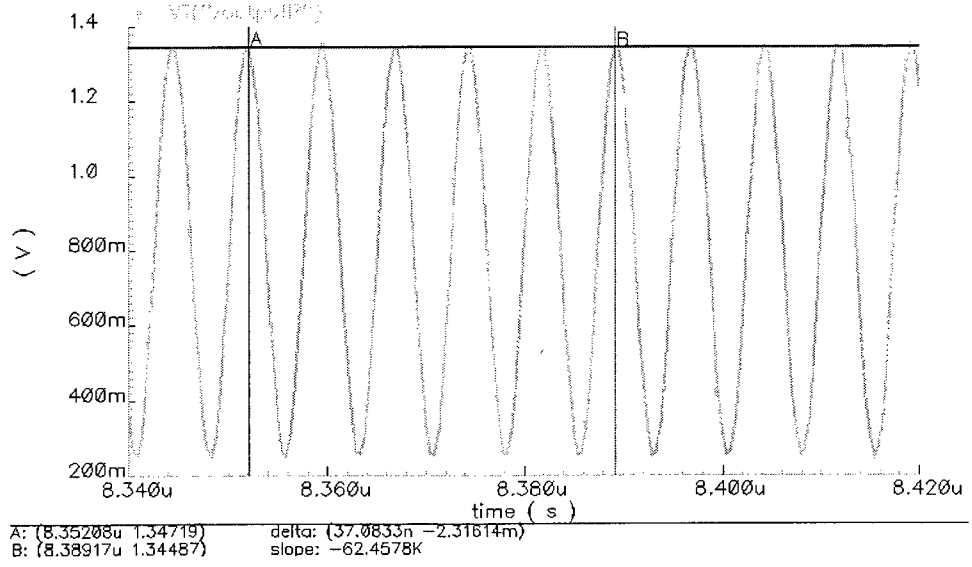


Figure 4.29: Maximum coarse tuning frequency at 136.231MHz

4.13 Far Out Phase Noise in a PLL

A PLL schematic was built in Cadence to test the far out phase noise in the PLL. A 10MHz sine wave with 10mV amplitude is introduced to mimic the far out phase noise produced by dithering. The sum of the sin wave and oscillator feedback signal were fed into the oscillator. This is shown in Figure 4.32. The Discrete Fourier Transform (DFT) of the oscillator output with no dithering and 10MHz dithering frequency are shown in Figure 4.33. Figure 4.33 proves that spurs happened at 10MHz dithering frequency which cannot be filtered out by PLL.

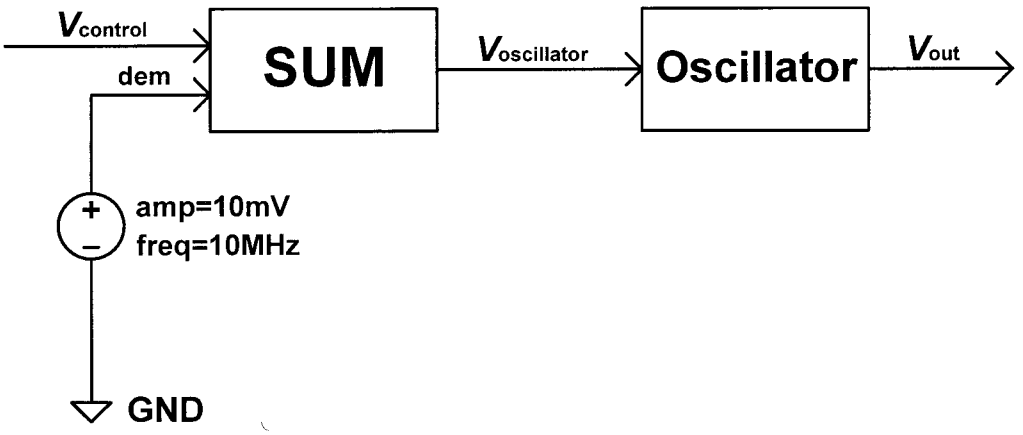


Figure 4.30: Oscillator with Far Out Noise

Figure 4.31: The DFT of the Oscillator Output in a PLL with 10MHz Dithering Frequency (top) and without Dithering (bottom)

4.14 DCO Look Up Table (LUT)

The DCO has a coarse tuning step of 90kHz and a fine tuning step of 8.7kHz. Therefore, 11 fine tuning steps are required to cover one coarse tuning step. The coarse tuning output frequency has deviations from the desired output frequency and the oscillator output frequency is not linearly related to the coarse tuning codes; therefore, a look up table is required for calibration. Both the coarse tuning deviations and the frequency non-linearity can be calibrated by choosing the correct coarse tuning code and fine tuning code combination from the LUT. In Figure 4.34, the first numerical number represents

the coarse tuning code and the second numerical number represents the fine tuning code. The calibration curve is used to linearize the relationship between tuning codes and oscillator output frequency. An example is also given in Figure 4.34; the current point (0, 15) is approximately equivalent to point (1, 4). Their output frequencies should be very close. However, oscillator output frequency at (0, 15) is much smaller than the output frequency at (1, 4). This is caused by the discrepancy when the coarse tuning code flips from 0 to 1. As a result, the point (1,10) is chosen as the next tuning code. Therefore, the coarse tuning code discrepancy is calibrated and the oscillator output frequency is linearly related to the tuning codes.

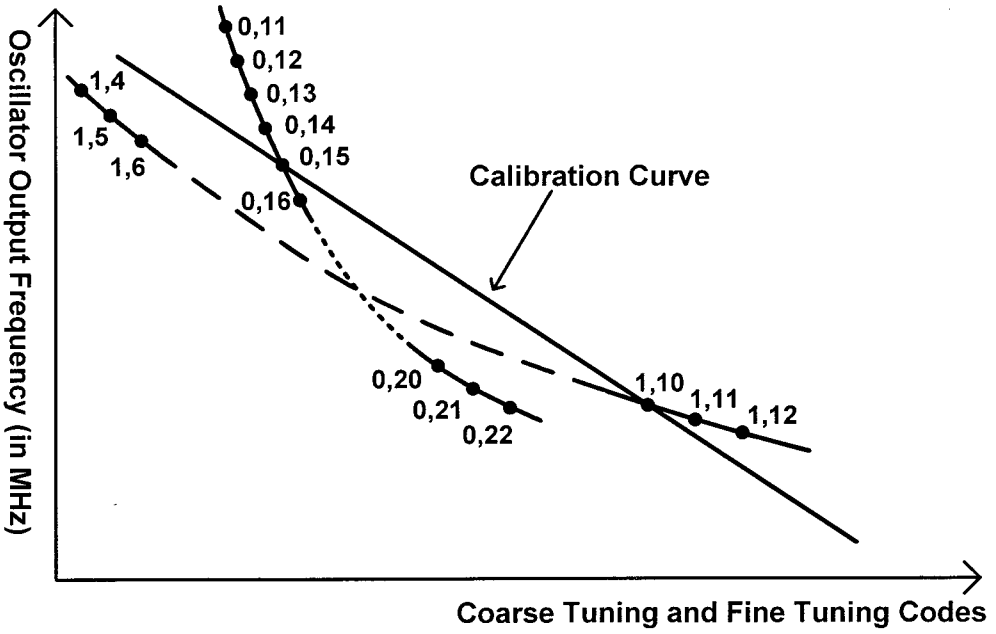


Figure 4.32: DCO Calibration Curve

4.15 DCO Layout Implementation

The implementation of the DCO required 3217 transistors with a total of 2.1mm X 1mm on-chip area in IBM 0.13μm CMOS technology. Layout issues such as: stray resistance, symmetry and wire routing are discussed below.

4.15.1 Stray Resistance

In the layout of analog transistors, it is important to have an accurate aspect ratio. The stray resistance (that is in series with drain and source) needs to be minimized by using multi-gate fingers. Via contacts added along the active regions reduce the series trace resistance. For wide transistors, it is worthwhile to split the layout into parallel connections [57].

4.15.2 Symmetry

Inter-finger connections need to be used in the layout to minimize noise and stray resistance. Therefore, the same number of NMOS or PMOS fingers are used in order to apply inter finger connections in the layout [58, 59].

4.15.3 Rules Implementation on the Designed DCO

The PMOS differential pair, the NMOS differential pair and the NMOS current source are all connected by using multi-gate finger connections. These layout cells are shown in Figure 4.35 and Figure 4.36. The PMOS differential pair and the NMOS current mirror transistors are split into 10 fingers, and the NMOS differential pair is split into 2 fingers. Also, the poly layer gates are connected to the metal layer first by using multiple contacts, and then these gates are connected together by using metal layers. The metal

lines used to connect the gates are designed to be short and thick to reduce stray resistance. Inter-finger connections are used in the layout of the above cells.

In the coarse tuning band, the switch resistance needs to be low. Therefore, the routing resistance must be minimized. The wiring between MIM-caps is made to be short and wide which is shown in Figure 4.37. In the fine tuning band, symmetric layout style is implemented on the 200fF and 210fF thermo-weighted capacitor groups to get matching for fine tuning steps and minimize parasitics caused by wiring. Four groups of thermo-weighted capacitor layouts are shown in Figure 4.38 and the DEM block together with the thermo-weighted capacitors are shown in Figure 4.39. The layout of the digital cells, oscillator core and buffer stages are shown from 4.40 to 4.48. Since the power lines need to supply power for all these on chip transistors, they need to be much wider than the other wires. Also, the buffer stage is powered by a separate power supply. The Electrostatic Discharge (ESD) protection is implemented on transistor input gates to protect transistors from being destroyed by electrostatic discharges. The pads of the differential oscillator outputs ("outputP" and "outputN") are assigned to be very close; therefore, the parasitics introduced by the bonding wire is minimized. The off-chip inductor is put on the Printed Circuit Board and the extra metal traces connected to the inductor pads are cut so that the parasitics introduced by the metal traces are minimized.

The final layout with Design Rule Check (DRC) and Layout Versus Schematic (LVS) clean is shown in Figure 4.49. The fabricated chip picture is shown in Figure 4.50.

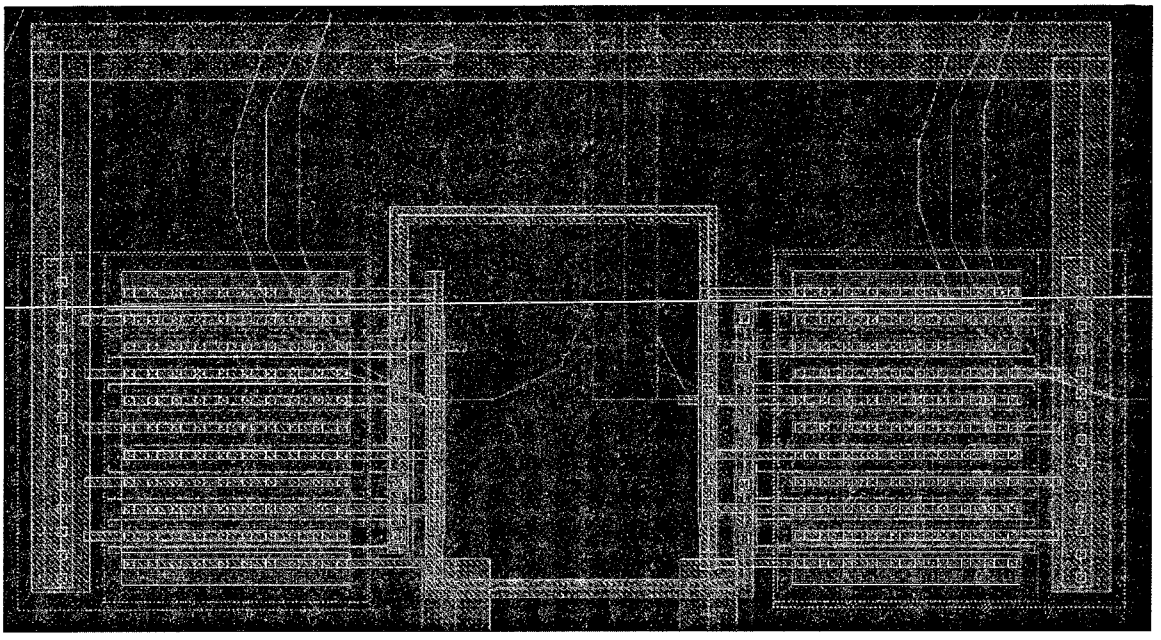


Figure 4.33: Top PMOS Differential Pair Layout

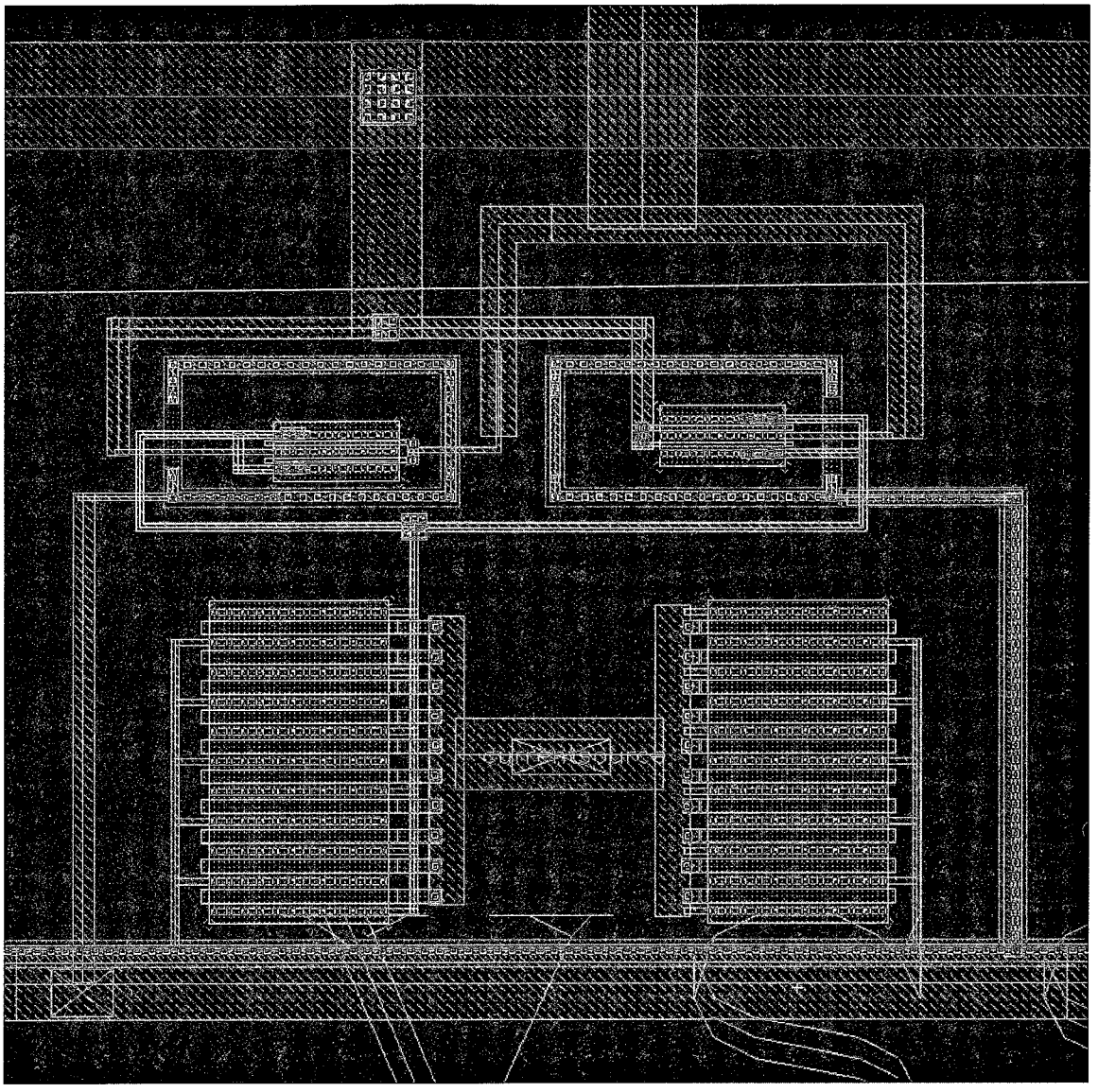


Figure 4.34: Bottom NMOS Differential Pair with NMOS Current Mirror Transistors Layout

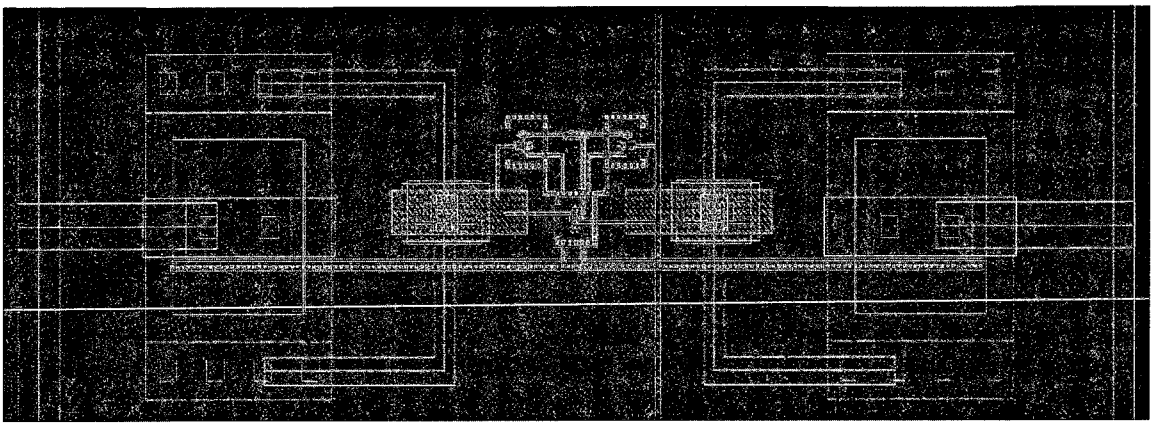


Figure 4.35: Switch MIM-cap Connection

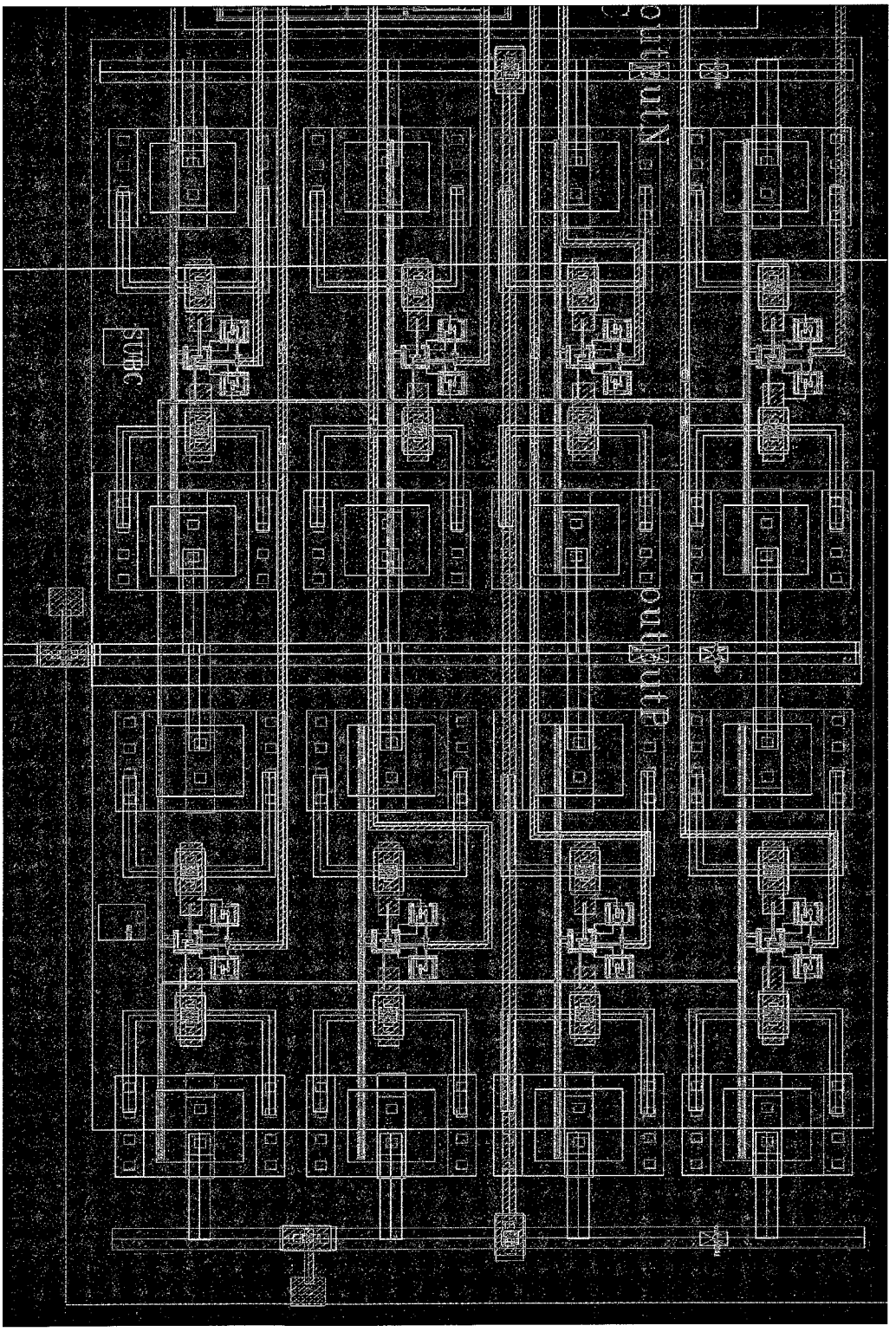


Figure 4.36: Four 200fF and 210fF Switch MIM-Caps

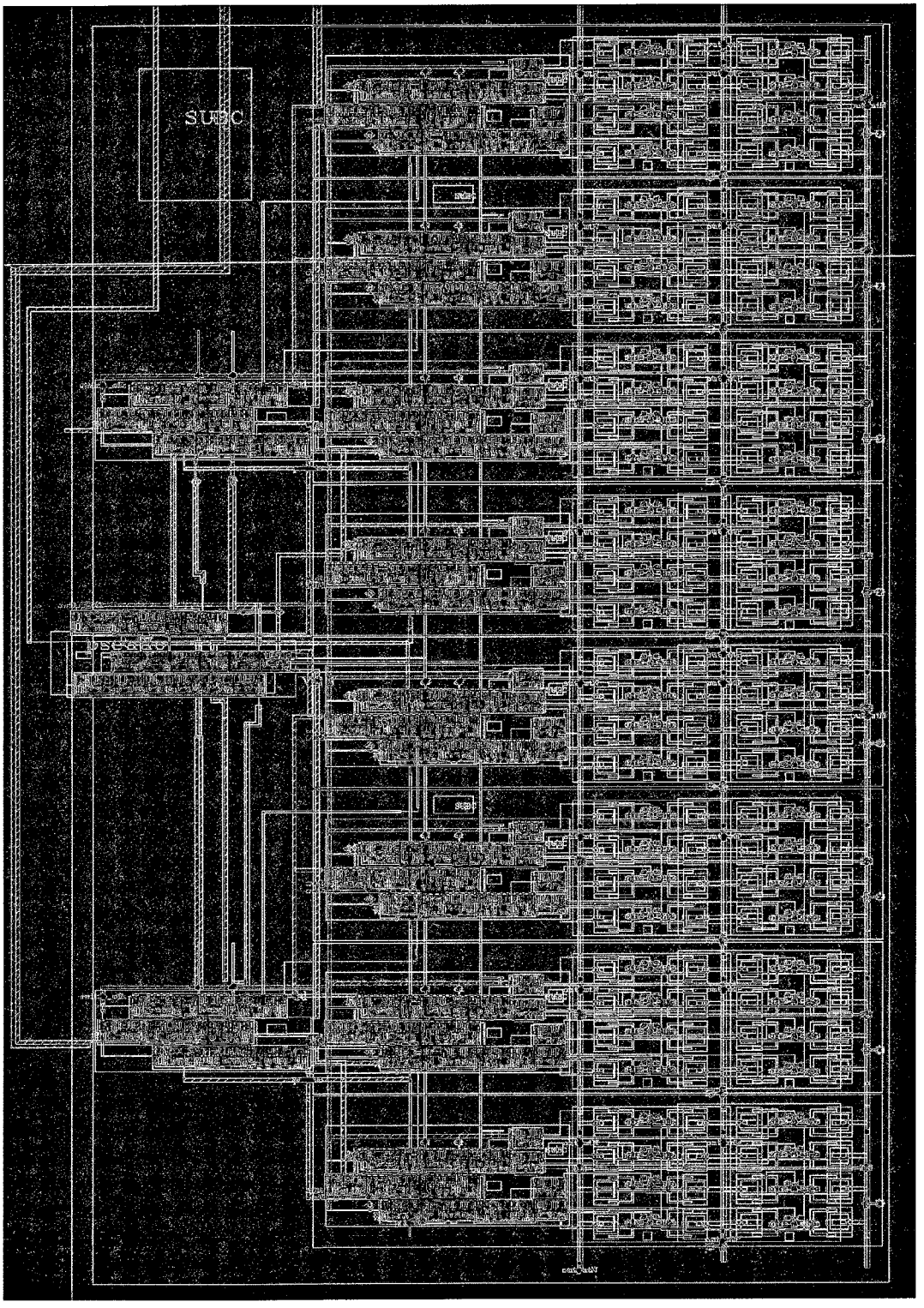


Figure 4.37: The DEM together with The Thermo Weighted Capacitors

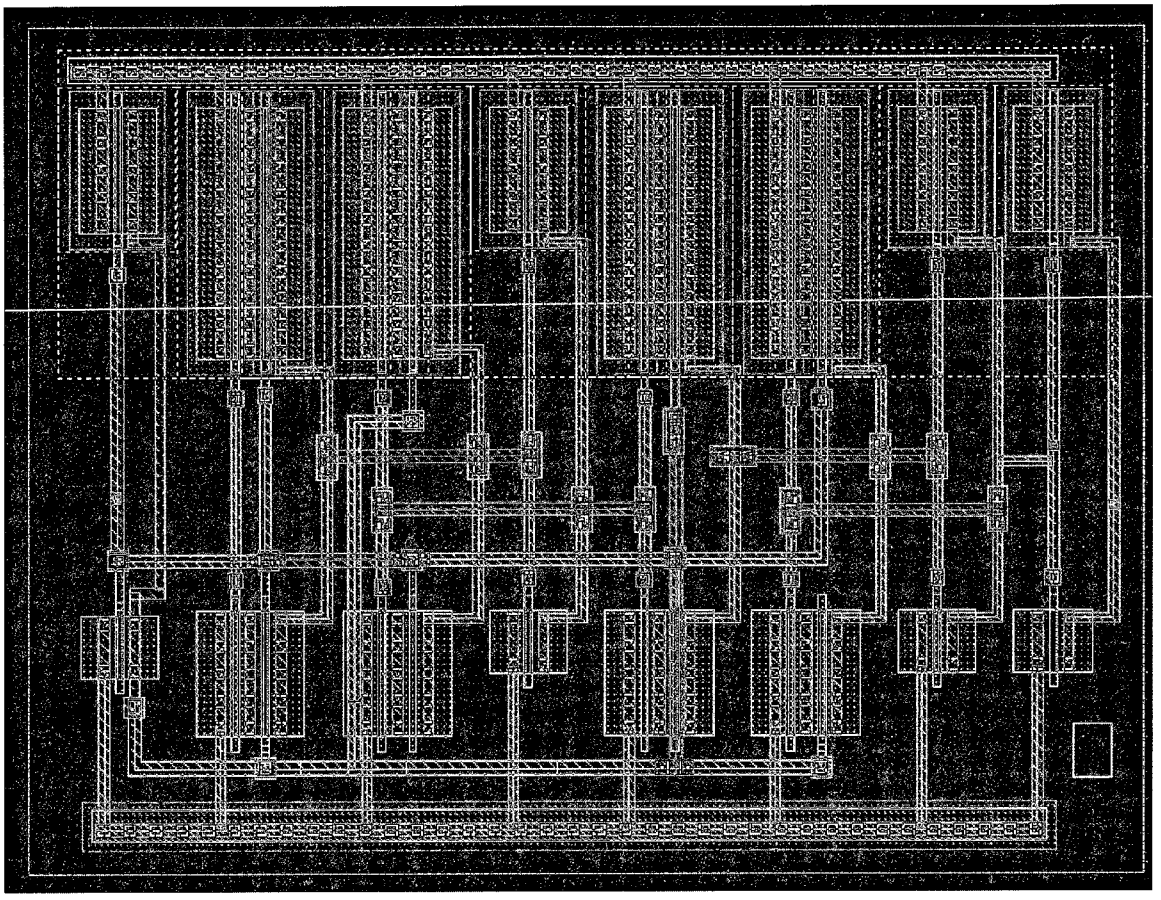


Figure 4.38: D-flipflop Shifter Layout

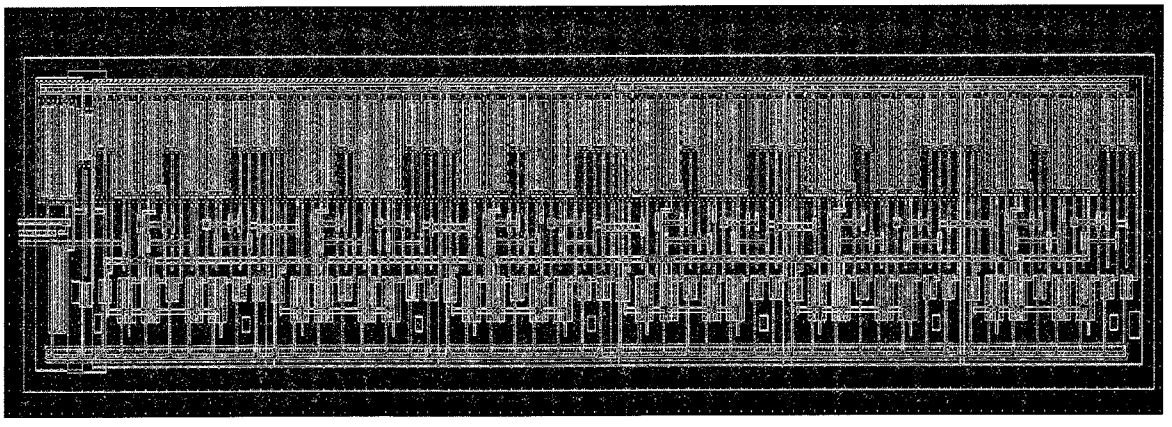


Figure 4.39: DEM Shifter Layout

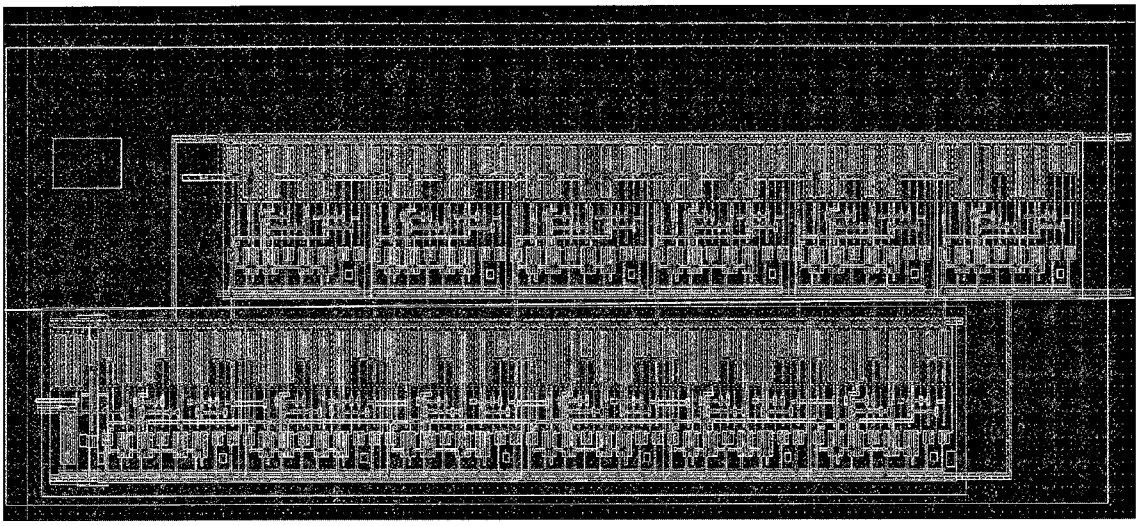


Figure 4.40: Fine Tuning Input Load Layout

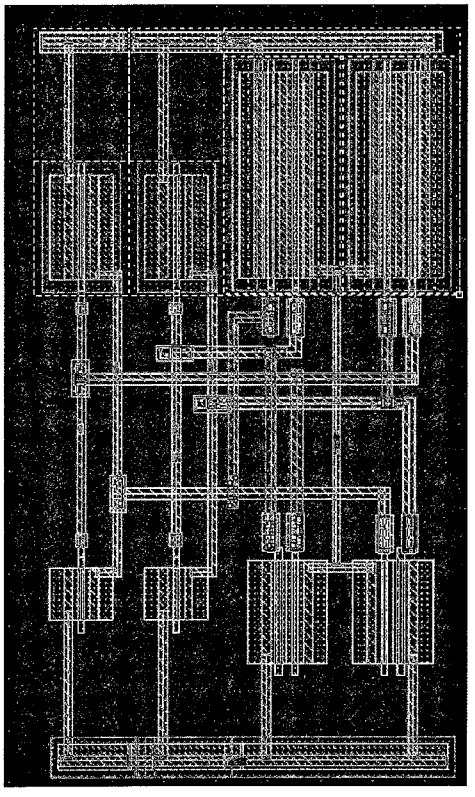


Figure 4.41: MUX Gate Layout

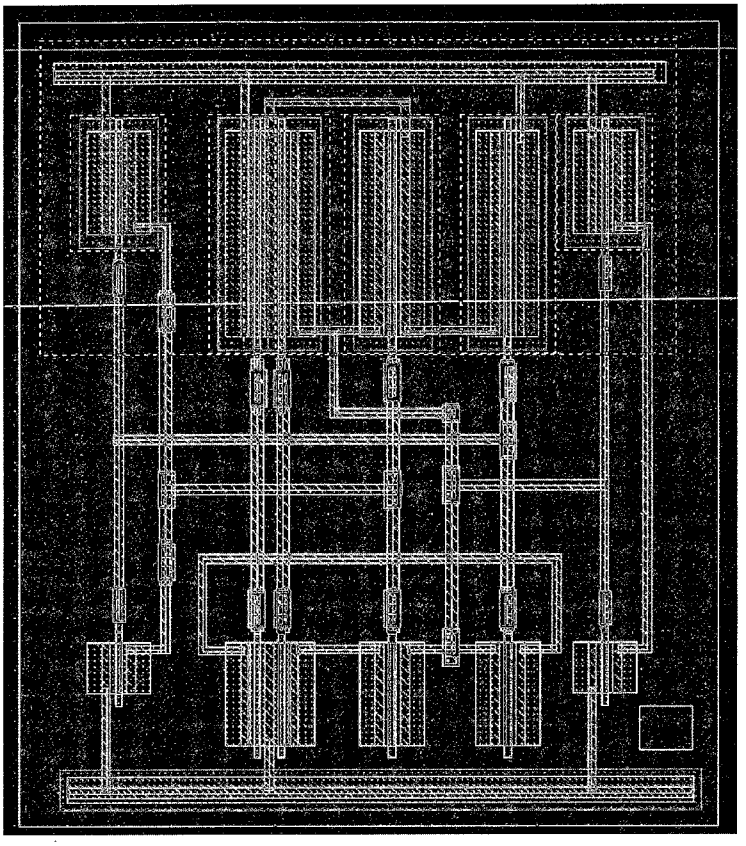


Figure 4.42: XOR Gate Layout

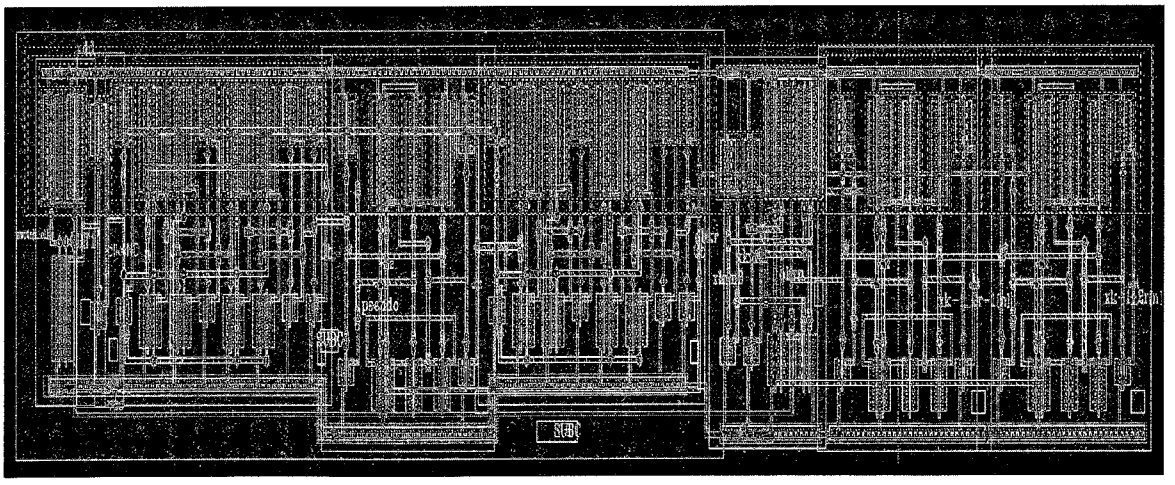


Figure 4.43: Switching Block

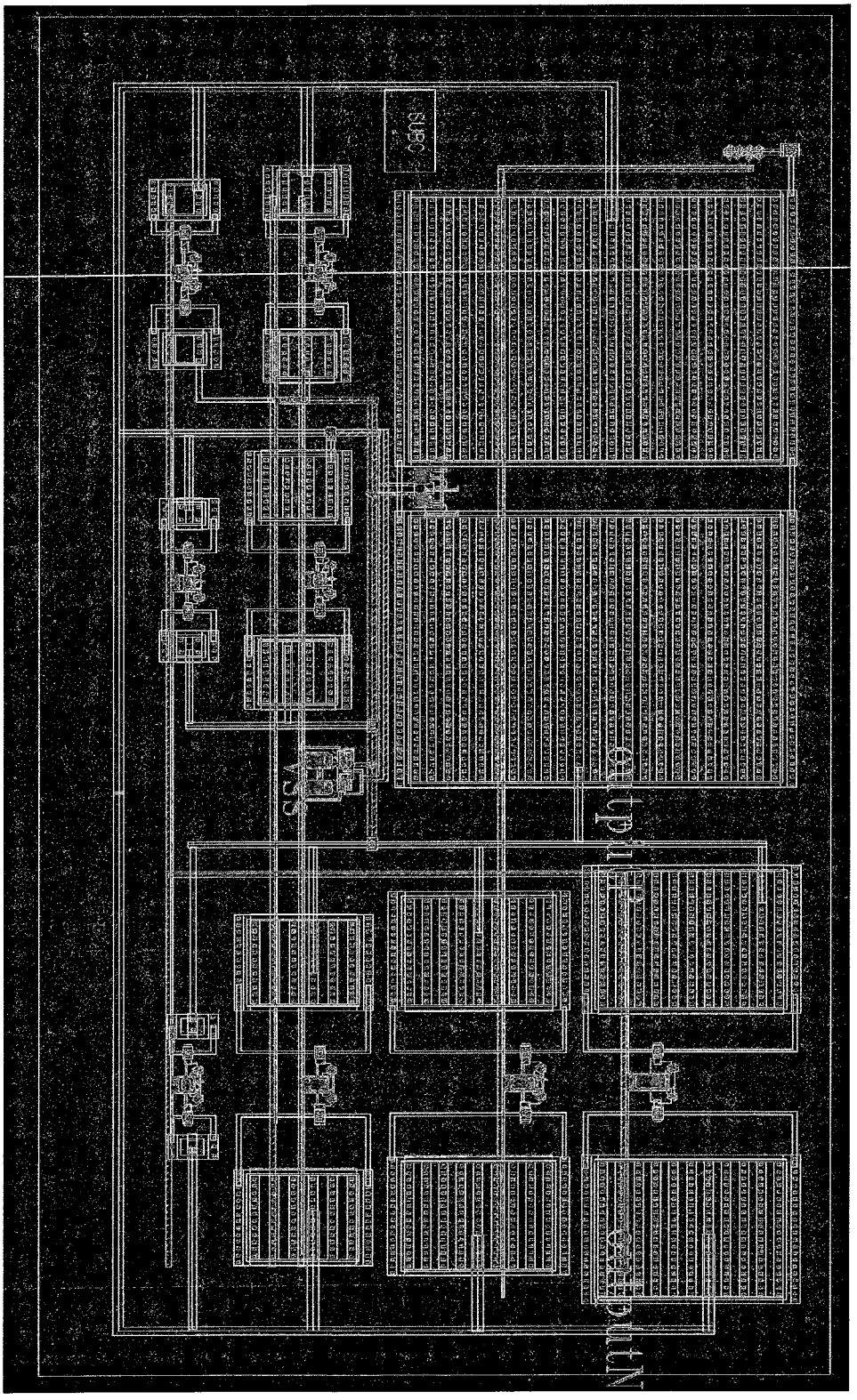


Figure 4.44: Oscillator Core Layout

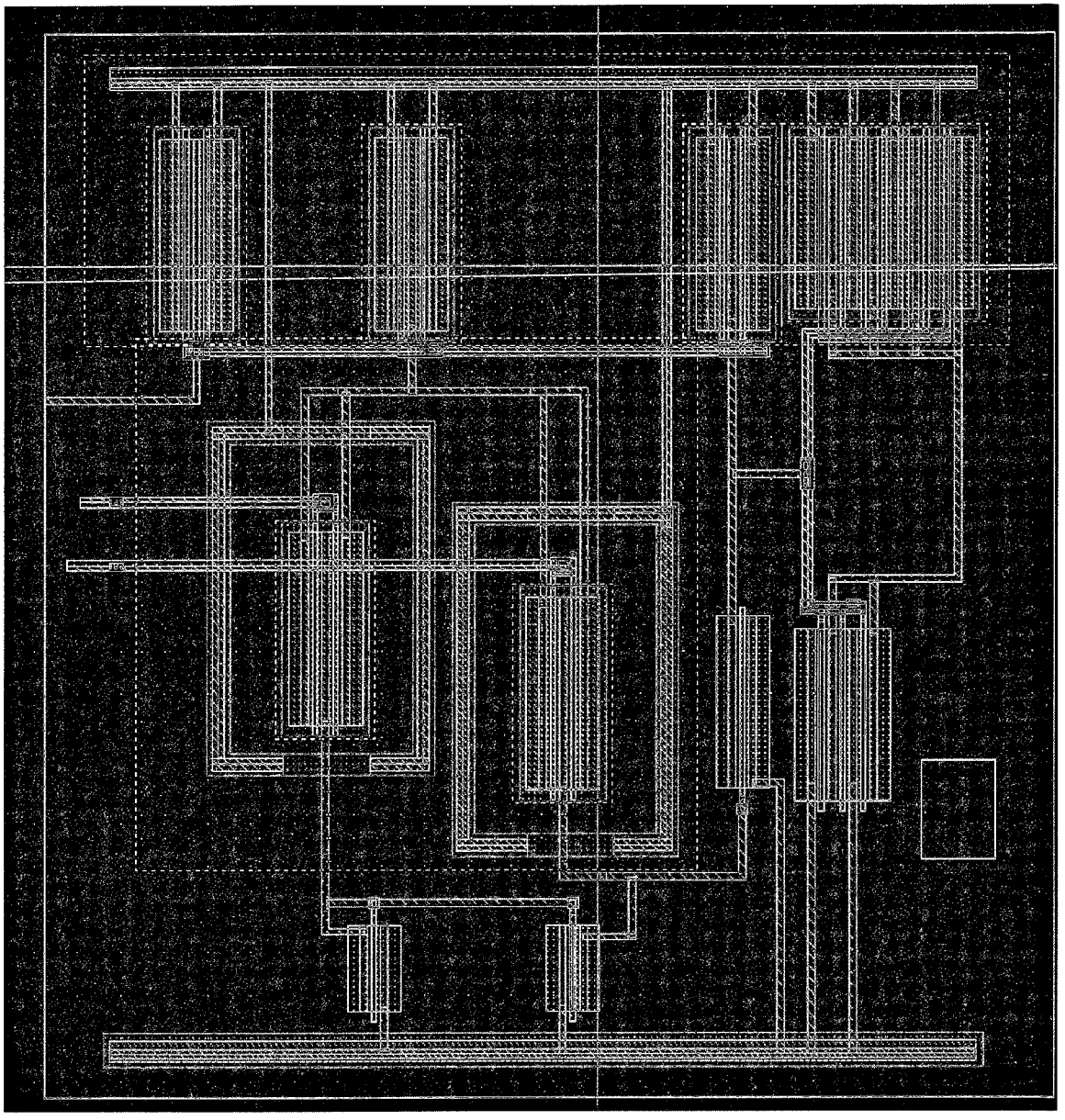


Figure 4.45: Output Buffer Layout

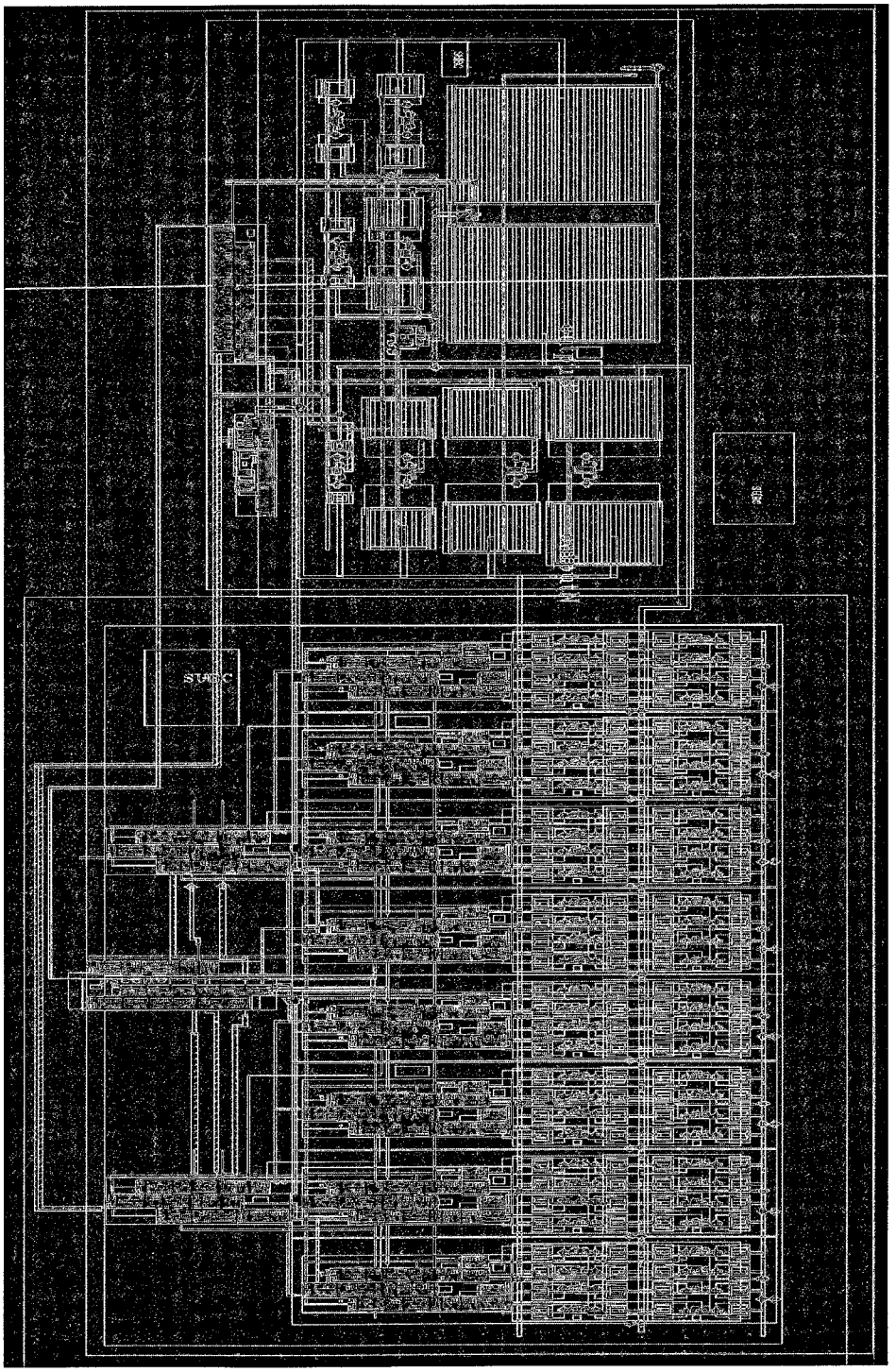


Figure 4.46: Oscillator Fine Tuning and Coarse Tuning Layout

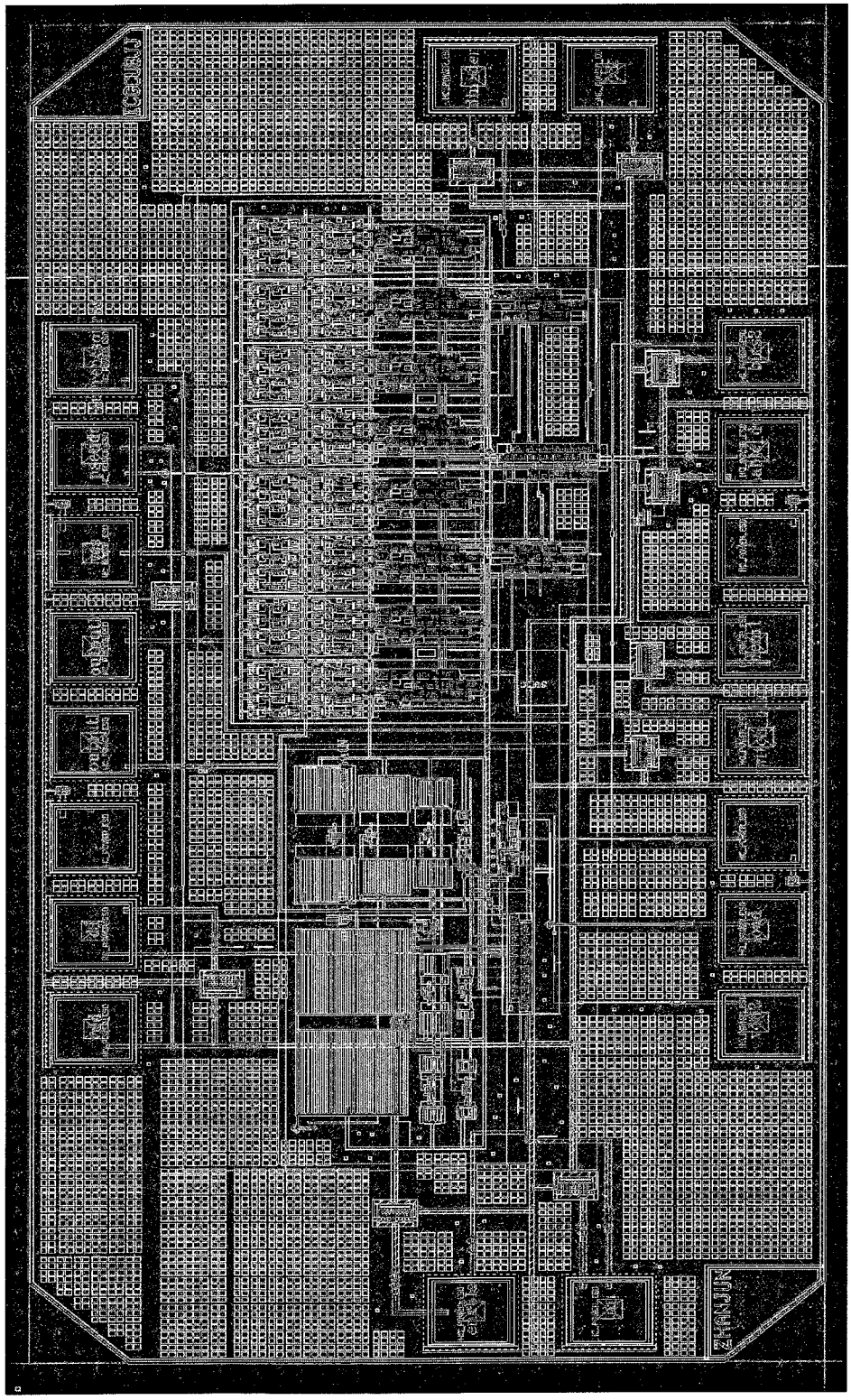


Figure 4.47: The Final Layout with DRC and LVS Clean

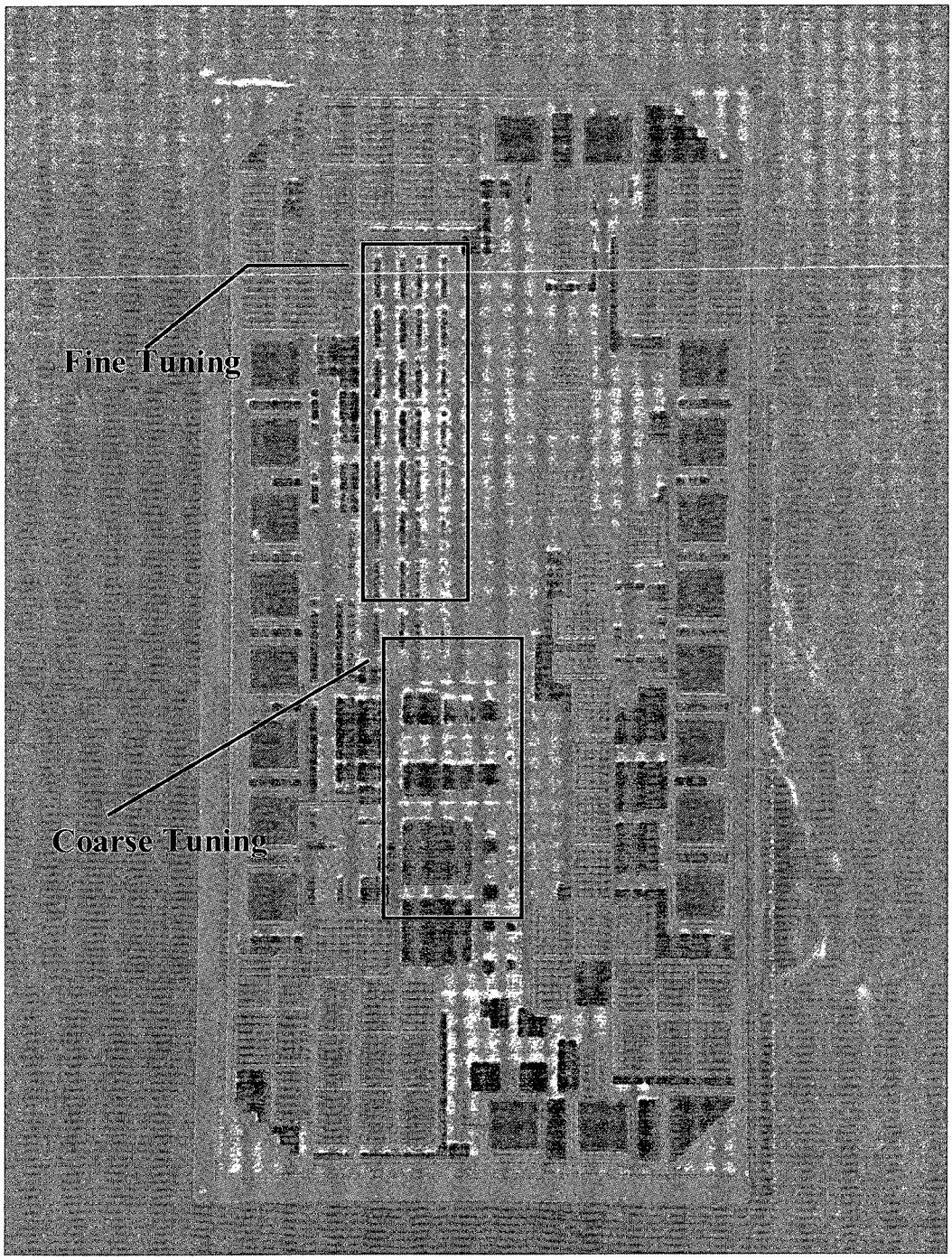


Figure 4.48: Fabricated Chip in 0.13µm Technology

4.16 Post Layout Simulations

The post layout simulations, using a 58nH off-chip inductor, at the minimum and maximum output frequencies are shown in Figure 4.51 and Figure 4.52. The oscillator can start oscillating at 800μA bias current. Both the minimum (112.211MHz) and maximum (135.783MHz) output frequencies are slightly lower than Figure 4.28 and Figure 4.29. This is caused by the wiring parasitics introduced in the testing environment. Also, the routing resistance added in the layout causes the overall Q to be lower than expected. The metal connections also increase the parasitic capacitance and inductance to the oscillator and lower the oscillator output frequency.

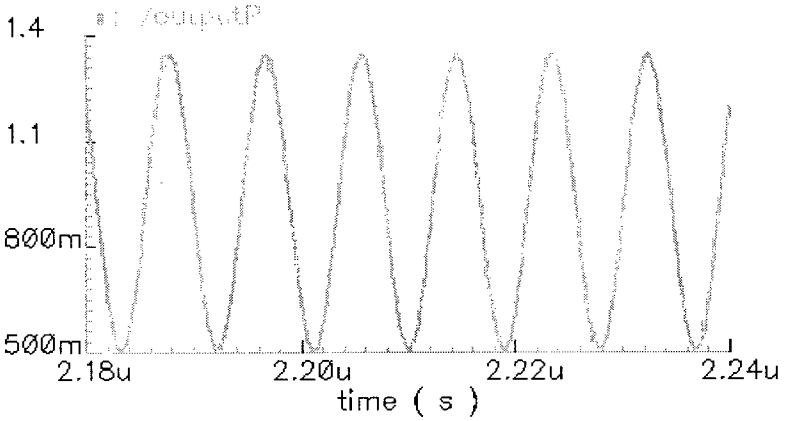


Figure 4.49: Post layout Simulation minimum output frequency at 112.211MHz

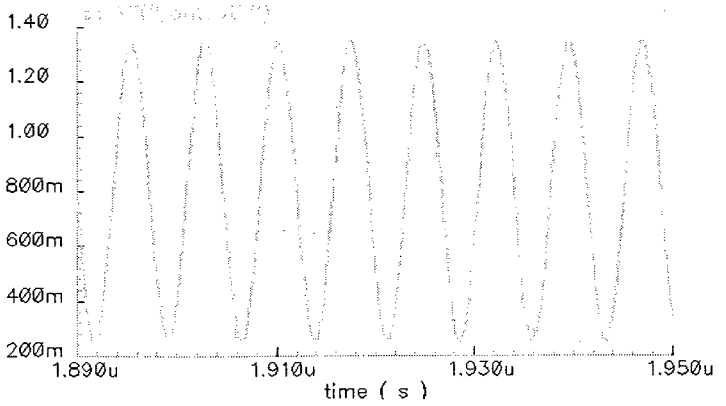


Figure 4.50: Post layout Simulation at the maximum Output Frequency at 135.783MHz

The buffer stages layout is shown in Figure 4.47 and it is simulated with a 400mV peak to peak input voltage (the minimum peak to peak voltage produced by the oscillator core at the minimum output frequency). Figure 4.53 shows that a 1.2V rail to rail voltage is achieved. Therefore, the buffer stages are strong enough to supply a rail to rail voltage to the oscillator output.

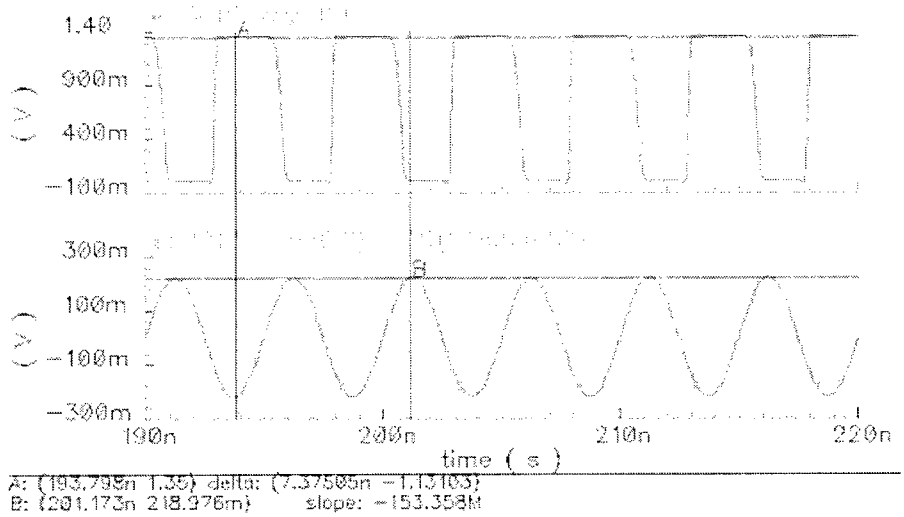


Figure 4.51: Post Layout Buffer

4.17 Power Consumption

On the post layout simulation, the oscillator can oscillate with a 1.2V power supply. The oscillator core consumes 800uA bias current. Therefore, the power consumption is 0.96mW with a 10MHz dithering rate going into the oscillator. The digital block is connected to a separate power supply and the average transient current is measured to be 77μA. Therefore, the digital block consumes 104μW power. The buffer stage takes 2mA current with a 1.2V supply. Therefore, it consumes 2.4mW power.

Chapter 5: Measurement and Discussion

5.1 Testbench Setup

The DCO was fabricated in 0.13μm IBM technology. The power consumption; coarse tuning code output frequency; fine tuning code output frequency; phase noise at different fine tuning codes; different dithering rate, and different oscillator output frequencies were tested. The test bench, shown in Figure 5.1, contains: the Altera DE2 board and a data generator (both for generating test patterns), a breadboard for converting test pattern voltages from 3.3 to 1.5V, the Printed Circuit Board Test Fixture 2 (PCB_TF2) mounted with the packaged test chip and a number of test instruments. The oscilloscope and the spectrum analyzer are used to monitor the output; the source meters are used to measure power consumption and control the supply voltages.

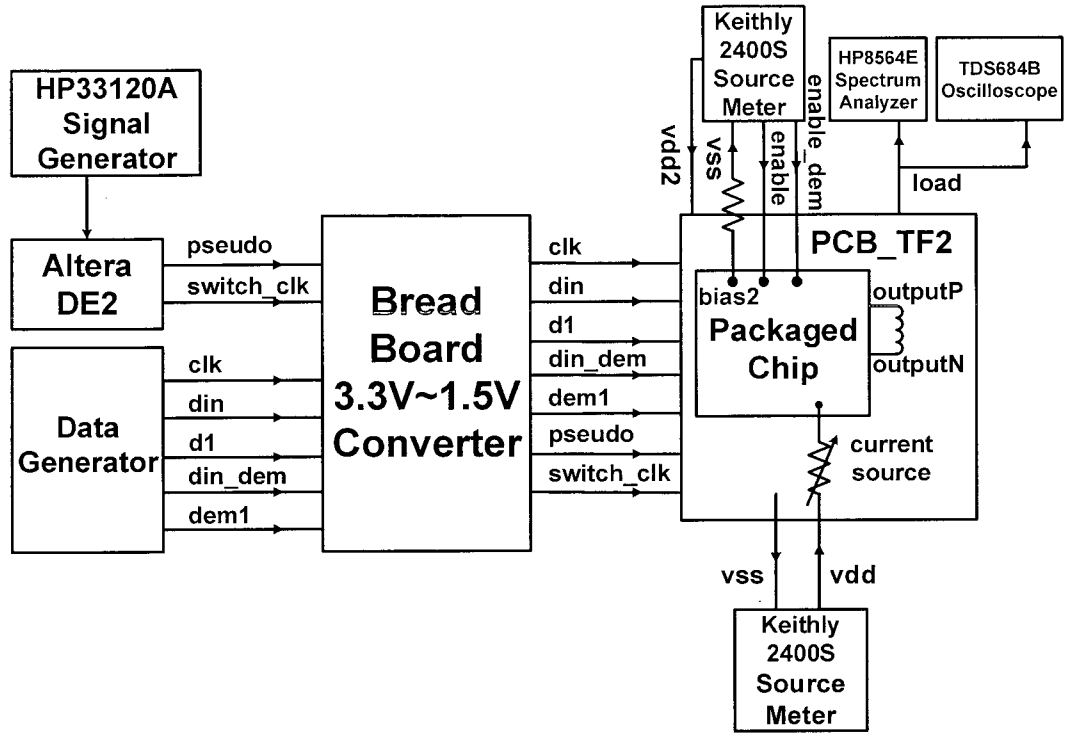


Figure 5.1: Testbench Setup Schematic

5.1.1 Input Signals Supplied by the Altera DE2

The Altera DE2 board is a Field Programmable Gate Array (FPGA) which is programmed to supply testing input signals. The pseudo random bit sequence ("pseudo") and the "switch_clk" are generated by the FPGA board to control the DEM block. The PRBS is generated by a 10-stage pseudo random serial data generator. The verilog code programmed on the FPGA board is shown in appendix A. In addition, a signal generator is externally connected to the Altera DE2 board so that both the switch_clk rate and the dithering rate are programmable.

5.1.2 Data Generator

The coarse tuning and fine tuning control words are programmed using the data generator (HP16500C) and these control words are sent to the chip using a serial shift register. These control words are composed of five input signals – the clock signal (clk), the coarse tuning and fine tuning shifter input signals (din, din_dem), the coarse tuning and fine tuning input signals (d1, d1_dem).

5.1.3 Voltage Converter Design

The output voltage of the Altera DE2 and HP16500C Data generator is 3.3V, whereas the maximum chip input voltage to the test chip is 1.5V. As a result, a voltage divider was used to convert the 3.3V signals to 1.5V. The maximum dither rate desired in this design is less than 10MHz, and therefore, $R * C < \frac{1}{10MHz}$, assuming the load is equal to 10pF; as a result,

$$R * 10^{-11} < 10^{-7} => R < 10^{4}$$

$$I = \frac{V}{R} = \frac{3.3V}{10K} = 0.33mA < 24mA$$

Since the Altera DE2 can drive a maximum 24mA current, a two resistor voltage divider was implemented to convert the output voltage with both resistors less than 5KΩ.

5.1.4 PCB-TF2 Cutting, Soldering and Wiring

PCB-TF2 board discription

The PCB-TF2 test board has two power supplies and two additional bias currents are required. Therefore, the PCB-TF2 was modified and two resistors were added to set bias current. The post layout simulation result shows that the LC oscillator starts oscillating

under 800μA bias current. Parasitic resistance and capacitance may be introduced by the PCB, bondwires and bondpads; therefore, a tunable resistor was added to the PCB to supply a tunable bias current for the LC oscillator. A 1KΩ resistor was soldered between the Vss and bias2 to supply bias current for the buffer stages. In addition, a 24nH off-chip high Q inductor was added between outputP and outputN.

5.2 Bias Voltage

Table 5.1: Simulated Operating Points vs Measured Operating Points

Transistor	Saturation Voltage Vdssat	Operating Point Vds	Post Layout Operating Point	Measured Operating Point
T40 (tank PMOS)	416.5mV	459.3mV	470mV	490mV
T12 (tank NMOS)	492mV	566.3mV	574mV	579mV
T15 (bottom current source NMOS)	233.7mV	324.5mV	306mV	281mV

Table 5.1 shows that the measured DC bias points agree with the simulation and post layout simulation results. As a result, all these transistors are operating in the saturation region and the chip is biased correctly. Note that all these transistors are biased by a 1.35V power supply.

5.3 Oscillating Test and Parasitics Calibration

When connected to the Oscilloscope and Spectrum Analyzer, the oscillator did not oscillate. The bias current was increased, but the oscillator still failed to oscillate. This

may be caused by extra parasitic capacitance and inductance introduced by the PCB-TF2 and the bondpads which were under-estimated at the design stage.

As an experiment, the fixed capacitor was cut out of the circuit using laser trimming and a larger off-chip inductor was implemented, thereby offsetting the unexpected parasitics. It was found that the oscillator functioned correctly; however, a high frequency resolution is desired in this design. Therefore, the off-chip inductor value was increased to 58nH to offer a higher quality factor to the LC tank. This solution reduced the frequency range and shifted the oscillator output frequency downward. On the positive side, the frequency resolution was increased.

5.4 Coarse Tuning Measurement Results

The oscillator was found to operate correctly with a 58nH inductor. The oscillator output frequency ranged from 108MHz to 133.6MHz as plotted in Figure 5.2 and Figure 5.3. The fine tuning frequency step was recalculated as 7kHz (equation 5.8) at 108MHz operating frequency. The binary steps were plotted on a spectrum analyzer, and the summarized results (Figure 5.4) show the coarse tuning output frequencies are not on a straight treadline due to capacitor mismatch as expected. However, this coarse tuning discrepancy can be compensated by using a fine tuning look-up table as described in chapter 4. The average coarse tuning step is approximately equal to 86kHz. The measured minimum and maximum oscillator output frequencies were lower than the post layout simulation. It is believed that this is caused by the under estimation of the parasitic capacitance and inductance introduced by the bondpads, bond wires, PCB traces and the off-chip inductor.

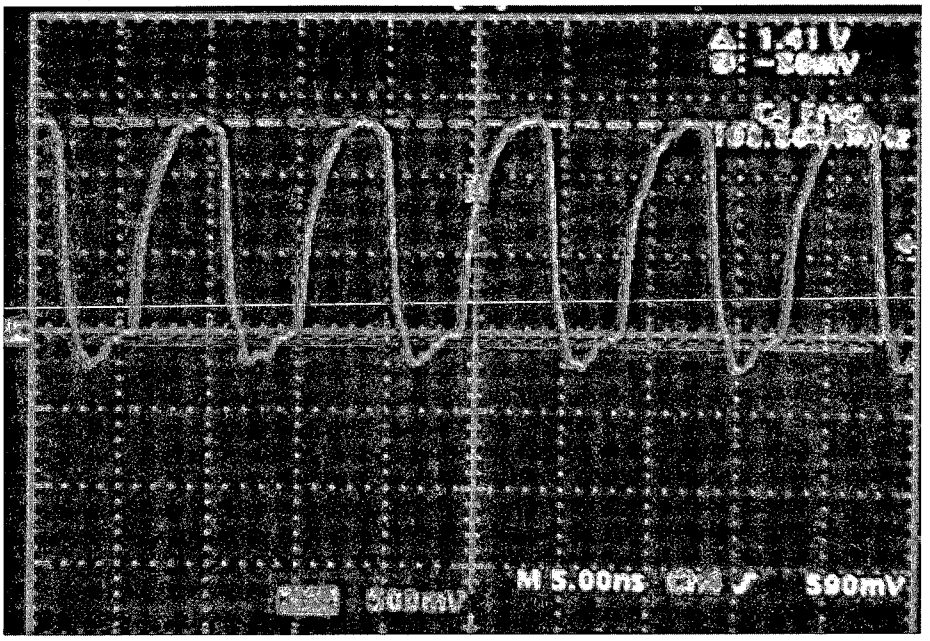


Figure 5.2: 108.8MHz Oscillator Output Frequency Captured on Oscilloscope

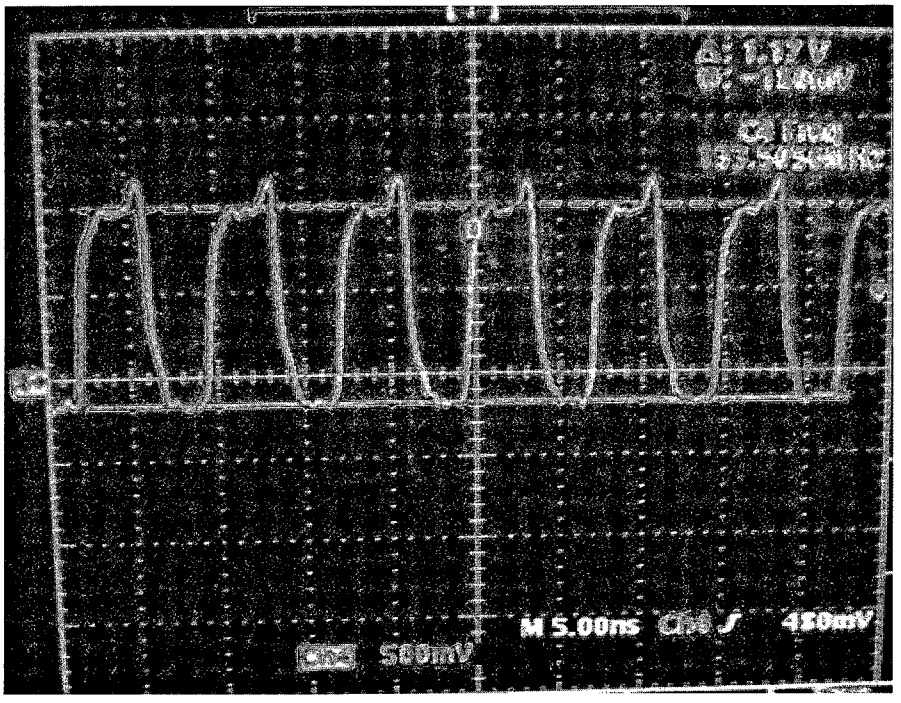


Figure 5.3: 133.5MHz Oscillator Output Frequency Captured on Oscilloscope

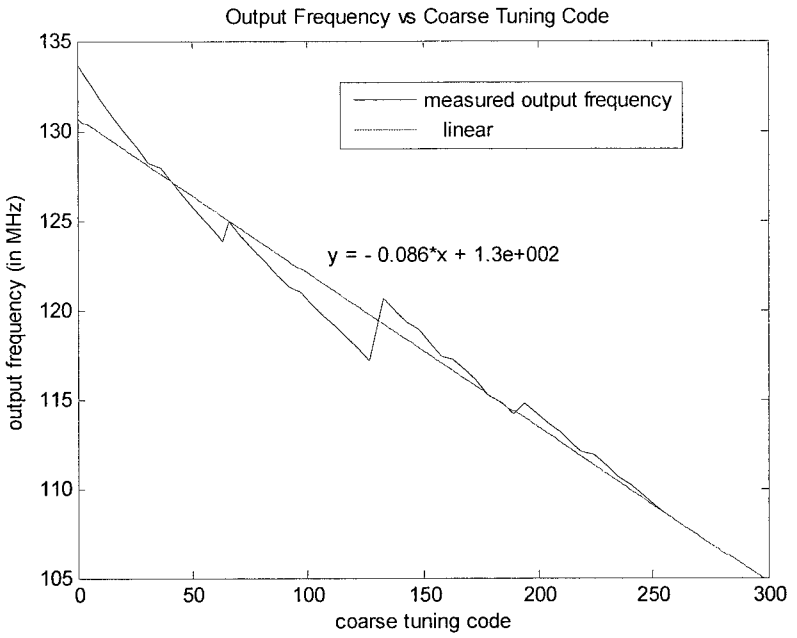


Figure 5.4: Summarized Coarse Tuning Steps

5.5 Measured Fine Tuning Steps

The minimum frequency tuning step was recalculated as 8.7kHz accounting for all the coarse tuning bits loaded into the circuit. The fine tuning steps ranging from 0 to 32 were measured on the spectrum analyzer and the summarized results are shown in Figure 5.5. The best-fit curve is plotted in Figure 5.5. Figure 5.6 shows the deviation of the dithered ouput frequencies are closer to the best-fit curve (the x axis) than the non-dithered output frequencies in most cases. However, from fine tuning code 19 to 24, the non dithered output frequency is closer to the desired output frequency. The non-dithered output frequencies chose a fixed number of capacitors which happened to be close to the desired capacitance. However, the dithered scenario needs to access those capacitors that have relatively large capacitance deviations. Therefore, the non-dithered output frequency turned out to be closer to the desired output frequency than the dithered output frequency

from fine tuning code 19 to 24. In general, the dithered output frequency deviation is still much less than the non-dithered output frequency and the dithered frequency resolution is less than 20kHz. Therefore, the frequency resolution is improved with dithering in most cases. Steps from 4 to 28 are chosen to ensure at least 4 capacitors dithering in each thermo-cap array.

Figure 5.6 shows the frequency deviation of the dithered output frequencies are closer to the best-fit curve (the x axis) than the non-dithered output frequencies in most cases. However, from fine tuning code 19 to 24, the non-dithered output frequency is closer to the desired output frequency. The non-dithered output frequencies chose a fixed number of capacitors which happened to be close to the desired capacitance. However, the dithered scenario needs to access those capacitors that have relatively large capacitance deviations. Therefore, from fine tuning code 19 to 24, the non-dithered output frequency turned out to be closer to the desired output frequency than the dithered output frequency. In general, the dithered output frequency deviation is still much less than the non-dithered output frequency. For this measured chip, the dithered frequency resolution is less than 10kHz with the fine tuning code ranges from 4 to 28. Therefore, the frequency resolution is improved with dithering in most cases. The achieved 10kHz frequency resolution is more than the calculated 8.4kHz frequency resolution. The deviations are contributed by layout defects and parasitics. In layout, there is an uncertainty in matching and routing the unit capacitance. Even though a lot of effort was spent on the thermo-weighted MIM-cap layout, it is very difficult to maintain the 5fF step capacitance. This can affect the oscillator output frequency resolution. This was verified by checking the MIM-cap

routing which is shown in Figure 5.7. Figure 5.7 shows the wires used to control these four 200fF and 210fF capacitors are not symmetric and some MIM-caps have longer routing wires than the others. This results in a larger parasitic resistance in series of the MIM-cap and a larger parasitic capacitance. For the coarse tuning band, although the switch resistance is low enough to give a good Q for the switch MIM-cap branch, the routing resistance added in the layout may cause the overall Q to be lower than expected. The parasitic capacitance, parasitic inductance and parasitic resistance on bondpads, bondwires and off-chip inductor lower the oscillator output frequency and increase the total capacitance. These factors can also affect the output frequency resolution.

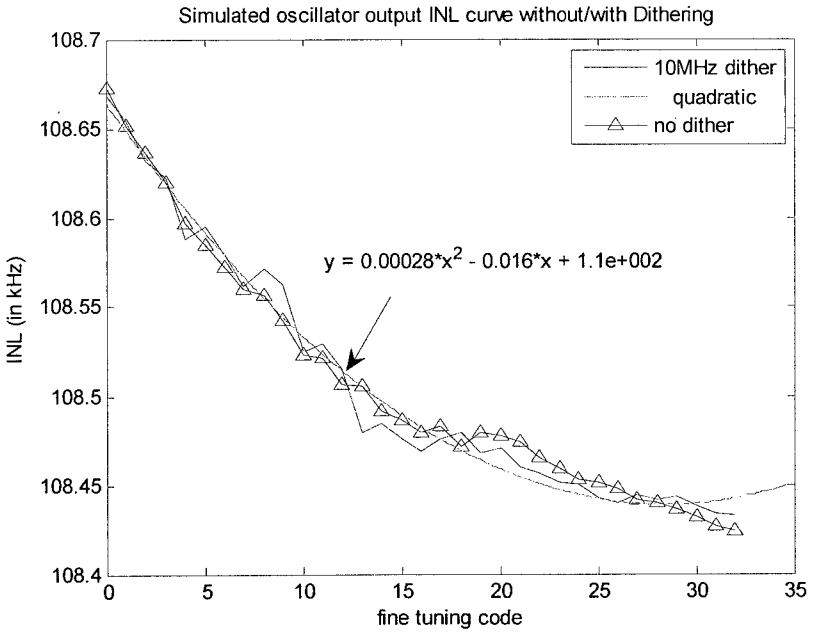


Figure 5.5: Measured Fine Tuning Steps with/without Dithering

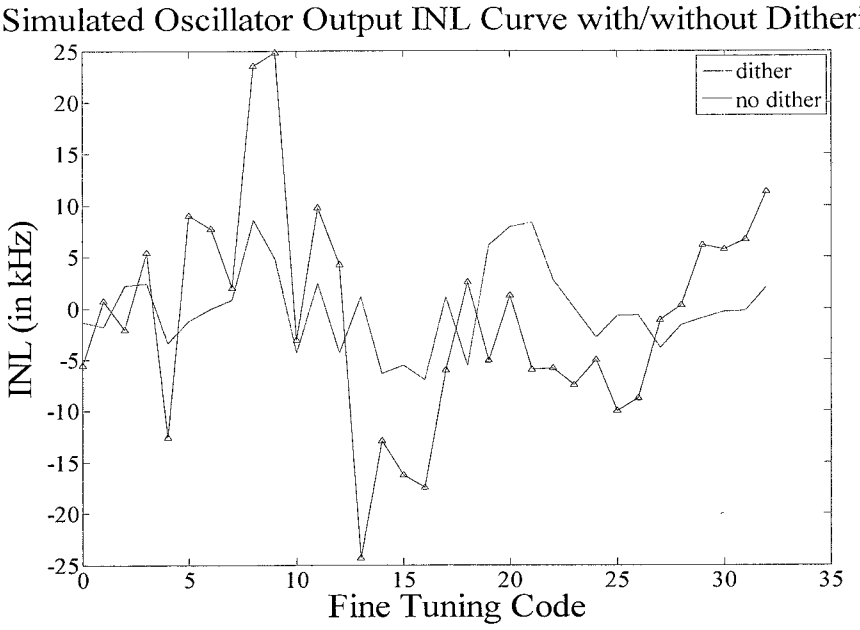


Figure 5.6: Measured INL Fine Tuning Steps without/with Dithering

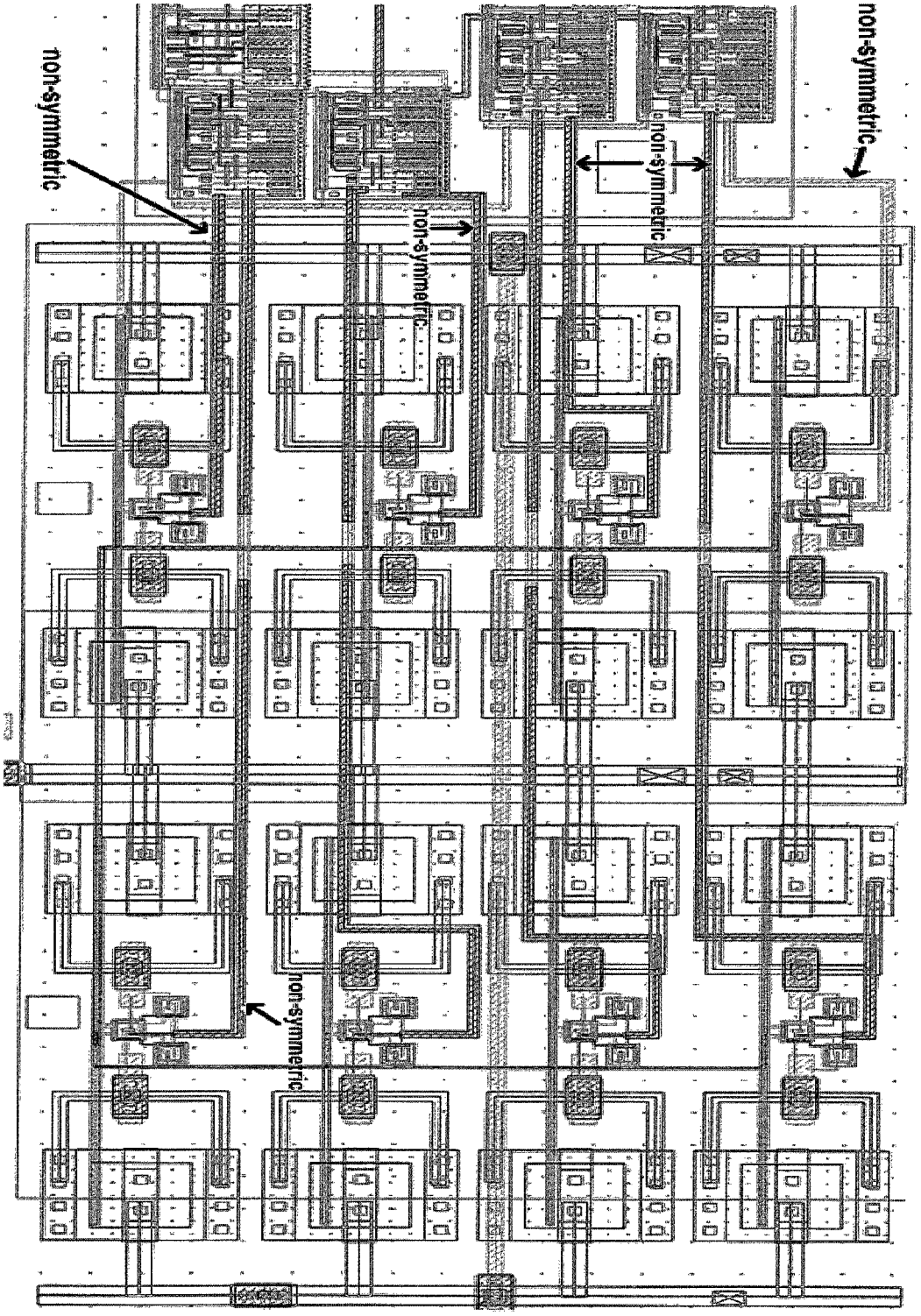


Figure 5.7: MIM-cap Routing

5.6 Comparison of Output Frequency without/with Dithering

The oscillator output frequency is measured without and with dithering. The frequency plot without dithering and with 10kHz dithering frequency is overlapped and shown in figure 5.8. At the 10kHz dithering frequency, different capacitor groups are chosen in each clock cycle and each capacitor group has slightly different total capacitance. This results in a 2.5kHz output frequency span and the capacitor process variations are averaged out. Without dithering, there is only one output frequency which is sitting inside the output frequency span of the dithering scenario, since the same group of capacitors is chosen all of the time. It can also be seen that spurs due to capacitor dithering are below the noise floor which is expected given the small capacitor value changes.

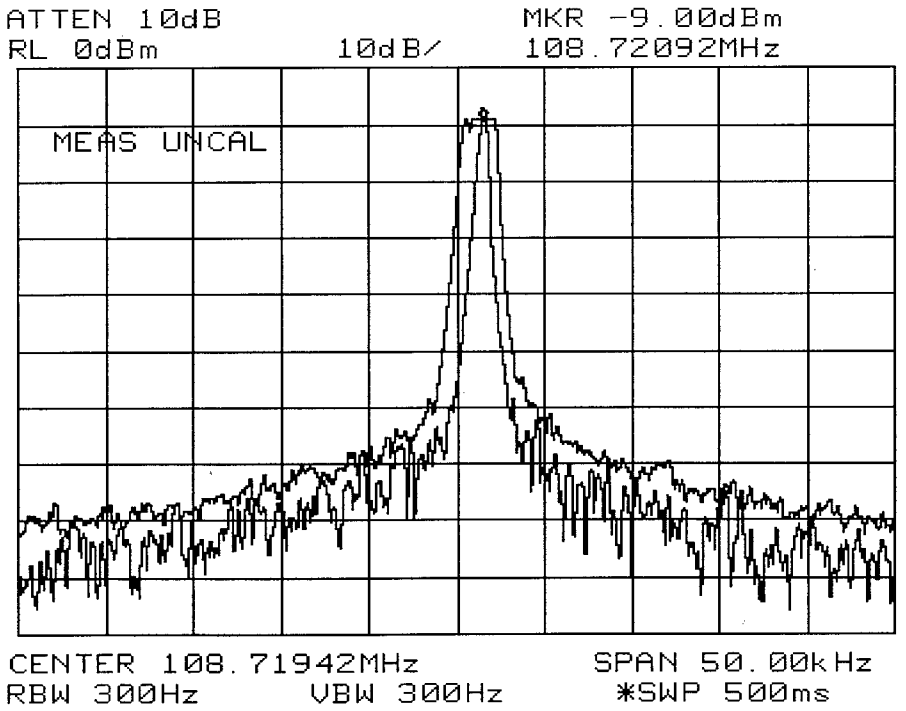


Figure 5.8: 108MHz Oscillator Output Frequency and Fine Tuning Code 16 without Dithering and With 10kHz Dithering

5.7 Phase Noise Plot at Different Oscillator Output Frequencies

The oscillator phase noise at different output frequencies was measured. Therefore, the influence of oscillator output frequency on phase noise can be found. The phase noise at 116.8MHz and 130MHz oscillator output frequencies are plotted in Figure 5.9 and Figure 5.10, respectively.

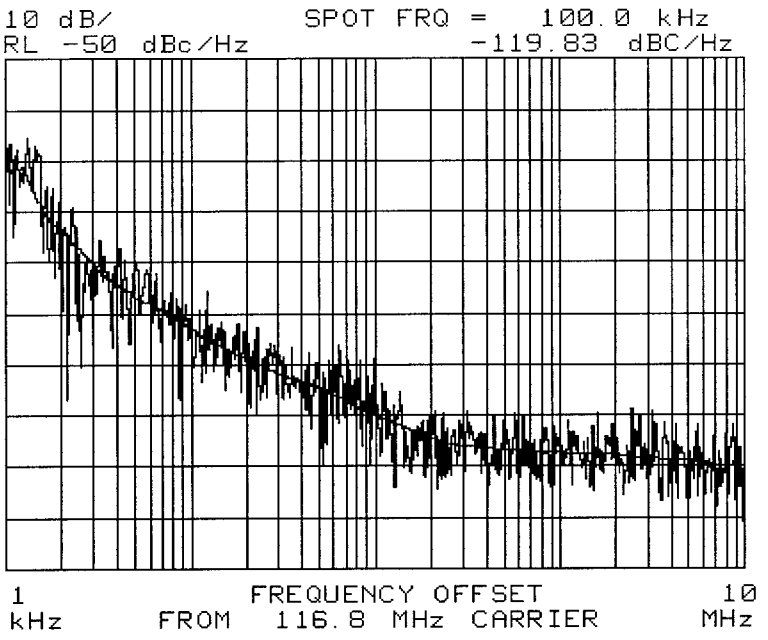


Figure 5.9: Phase Noise Without Dithering at 116.8MHz Output Frequency

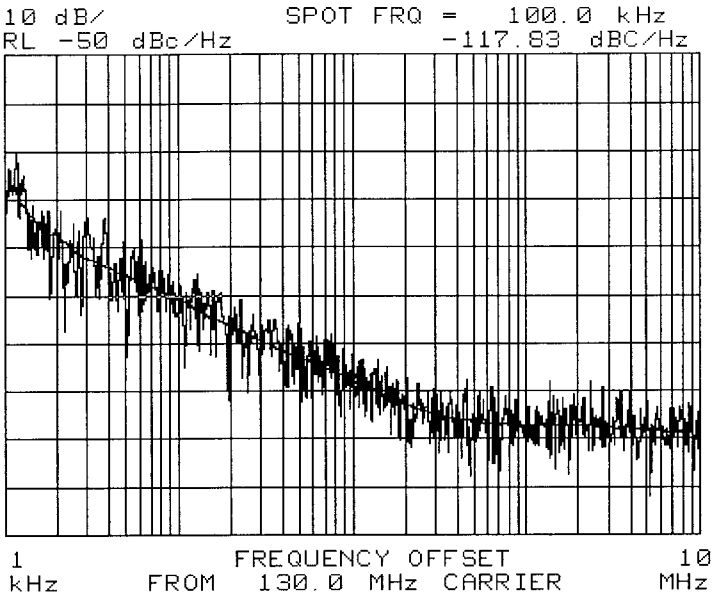


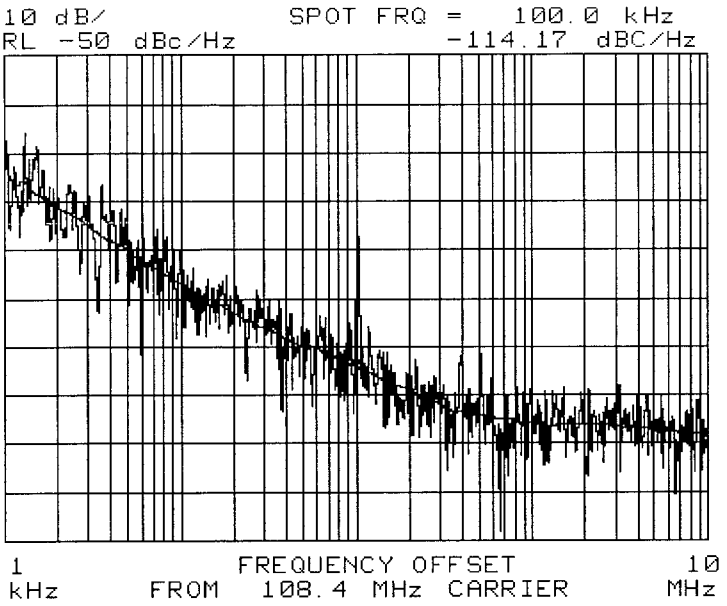
Figure 5.10: Phase Noise Without Dithering at 130MHz Output Frequency

The phase noise at 100kHz offset frequency increases from -119dBc to -117dBc while the oscillator output frequency increases from 116.8MHz to 130MHz. According to equation 3.5, the phase noise will increase at a higher oscillator output frequency. Therefore, the measurement results agree with equation 3.5.

5.8 Phase Noise Measurement at Different Fine Tuning Codes

The oscillator phase noise was measured at different fine tuning codes. Therefore, the influence of fine tuning code on the oscillator phase noise can be found. The design aims to achieve a high frequenecy resolution at different dithering codes. The design expects the phase noise to stay the same at different dithering codes. Figures 5.11 to 5.13 show

the phase noise measurement results by varying the fine tuning code at 1MHz



dithering.

Figure 5.11: Phase Noise at 108MHz and Fine Code 0 with 1MHz Dithering

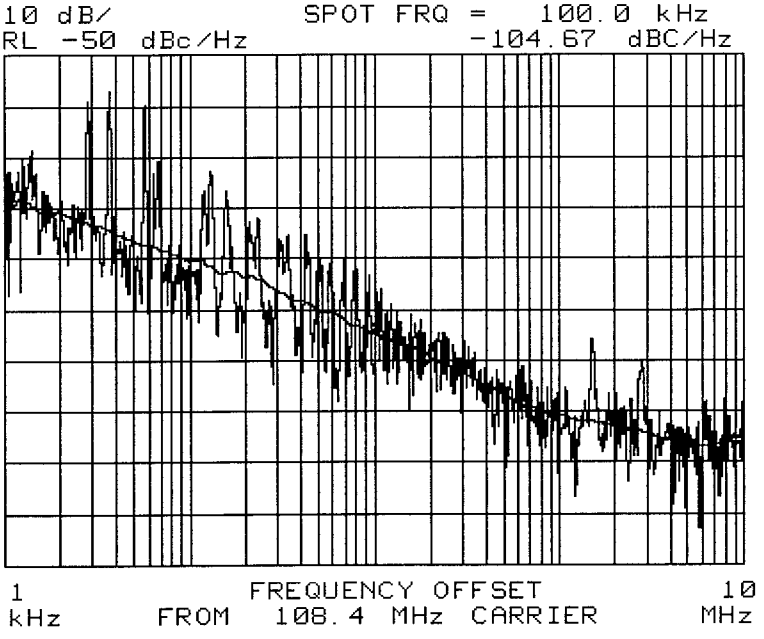


Figure 5.12: Phase Noise at 108MHz and Fine Tuning Code 31 with 1MHz Dithering

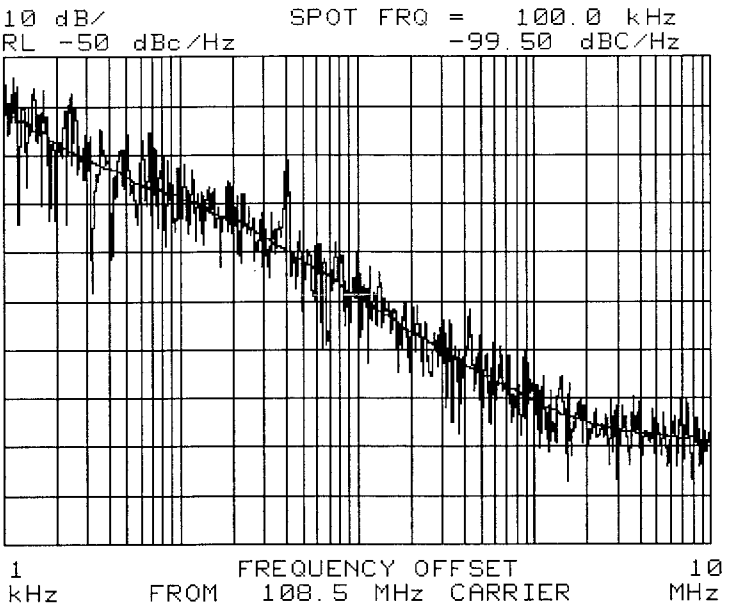


Figure 5.13: Phase Noise at 108MHz and Fine Tuning Code 16 with 1MHz Dithering

Figure 5.11 shows the fine tuning code is "0" and the phase noise is -114.17dBc/Hz. Therefore, all the 200fF capacitors are selected and there is no dithering in both capacitor arrays. In Figure 5.12, the dithering code is "31" and the phase noise is -104.67dB/Hz. Therefore, one 200fF capacitor and thirty one 210fF capacitors are chosen in each clock cycle. In Figure 5.13, the dithering code is "16" and the phase noise is -99.5dBc/Hz, so sixteen capacitors are chosen to dither in both switch MIM-cap arrays. Figure 5.11 to Figure 5.13 show that phase noise increases with the increased number of capacitors dithering in both arrays. These measurement results disagree with the design expectation. This might be caused by the fine tuning switches, which cannot fully charge or discharge the fine tuning MIM-caps. With more MIM-caps dithering in both arrays, more residue charges are left on MIM-caps. This results in residue charges being injected to the oscillator output and increasing the oscillator phase noise.

5.9 Phase Noise Measurement at Different Dithering Frequencies

The oscillator is dithered at different dithering frequencies; the output frequencies and phase noise are measured. Therefore, the influence of dithering frequency on oscillator output frequency and phase noise can be found. Higher dithering frequency can access different capacitor groups more frequently; therefore it can average out process variations further within a certain period time. The spot frequency plots and phase noise plots at different dithering frequencies are shown from Figure 5.14 to 5.17.

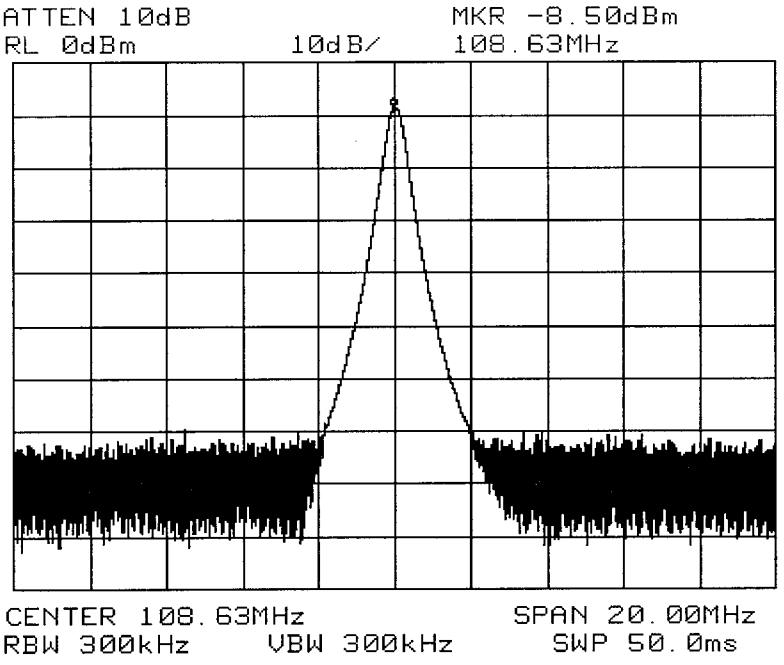


Figure 5.14: 108MHz Oscillator Output Frequency with 10kHz Dithering

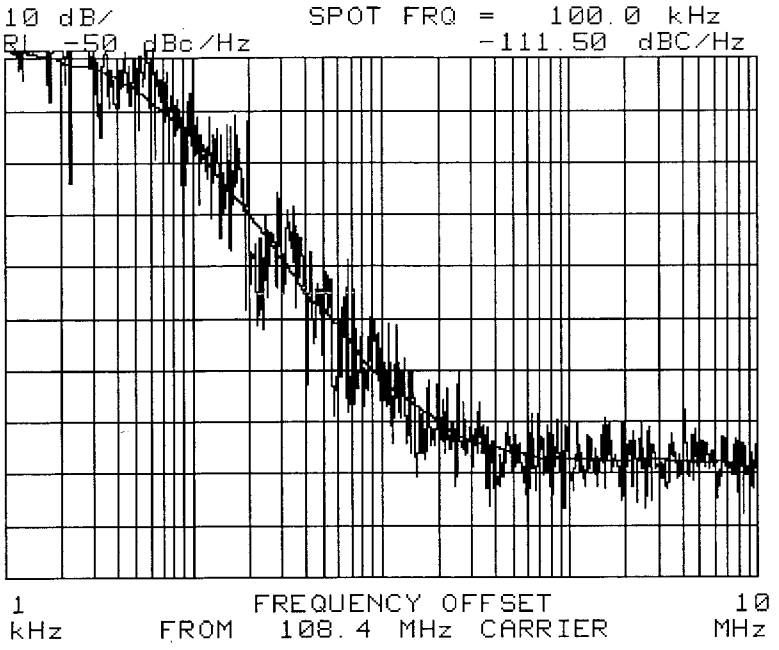


Figure 5.15: Phase Noise at 108.4MHz and Fine Tuning Code 16 with 10kHz Dithering

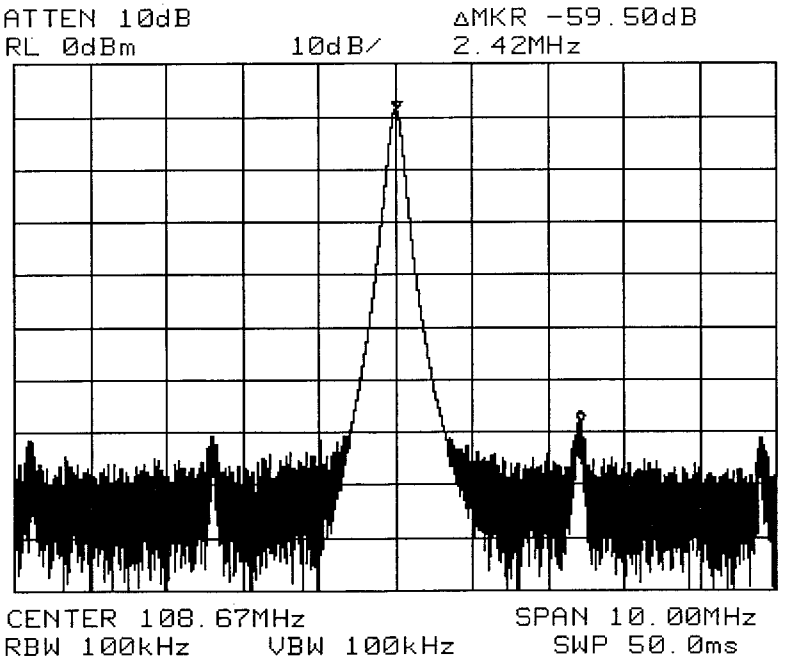


Figure 5.16: 108MHz Oscillator Output Frequency with 10MHz Dithering

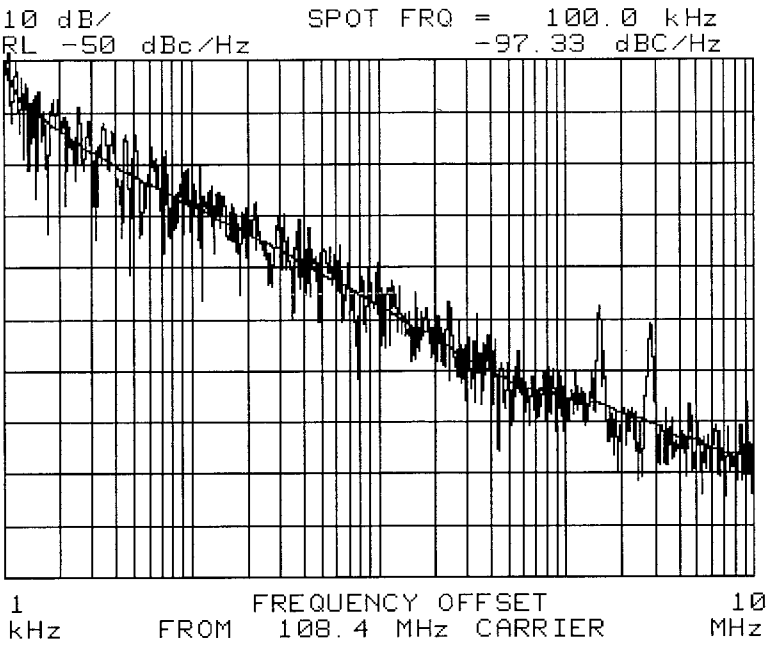


Figure 5.17: Phase Noise at 108.4MHz and Fine Tuning Code 16 with 10MHz Dithering

The measurement results show there are no obvious harmonics when the dithering frequency is low. Harmonics happen at the multiples of 2.4MHz with the dithering frequency at 10MHz. These harmonics are caused by the intermodulations between the output frequency and the dithering signal. However, spurs are also introduced at higher dithering frequencies.

Figure 5.15 and Figure 5.17 show that the phase noise with 10kHz and 10MHz dithering frequencies are -111.5dBc/Hz and -97.33dBc/Hz, respectively. Clearly, the phase noise degrades under a higher dithering frequency. This agrees with the simulation discussed in chapter 4.13, more spurs are introduced at higher dithering frequencies.

5.10 Close in and Far Out Phase Noise in PLL

The oscillator output frequency phase noise without and with dithering are measured to compare the phase noise at different offset frequencies. The output frequency span range also know as the close in phase noise is defined as the deviation of the oscillator output frequency from the center output frequency. The far out phase noise is phase noise that is greater than 50kHz offset frequency. Figure 5.18 shows dithering introduces more close in phase noise at low frequency offset than without dithering. In a PLL, the oscillator phase noise will see a high pass transfer function to the output. However, extra far out phase noise is introduced at a high dithering frequency and the output frequency span range is increased. The close in phase noise can be detected by implementing correct modulation and demodulation method. The far out phase noise cannot be filtered out by an analog PLL as simulated in section 4.13. However, the feedback signal can be used to control the DEM block to suppress the far out phase noise.

This design expects the output frequency span range to be fixed (shown in Figure 5.8) and the phase noise to be close in rather than far out. The far out phase noise and increased frequency span may be caused by noise generated by the digital block. The digital block should be redesigned to have a separate power supply; therefore, the digital block phase noise will not be propagated into the oscillator core causing intermodulation between oscillator output frequency and dithering frequency. This increases the output frequency span range and oscillator phase noise. In conclusion, the high frequency resolution can be achieved by dithering; however, far out phase noise is introduced into the loop and it will not be filtered out.

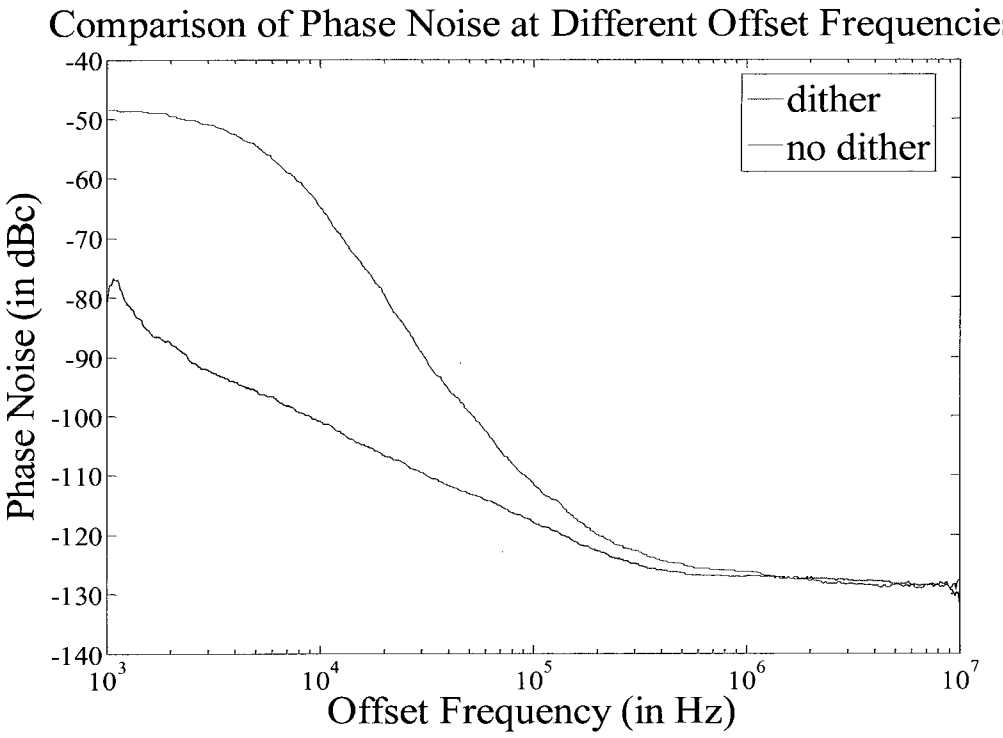


Figure 5.18: Comparison of Phase Noise at Different Offset Frequencies

5.11 Power Consumption

Power consumption is one of the most significant specifications in an oscillator design. In order to measure the power consumption, the testbench shown in Figure 5.19 is used. Two Keithly source meters are used to supply power to the oscillator and the buffer stages separately. The power consumption of the oscillator core is measured at its free running frequency (there is no digital power consumption at the free running frequency).

The spectrum analyzer is used to monitor the oscillator output frequency. The oscillator can start oscillating at 1.185V power supply and 1.455mA bias current. Therefore, the oscillator core consumes 1.724mW power. With a 10MHz dithering rate going into the oscillator, the bias current increases to 1.52mA; therefore, the digital control block consumes 0.077mW power. The source meter2 shows the buffer stage is biased at 12.1mA current with a 1.185V power supply, therefore, it consumes 14.3mW

power. The operating voltage ranges from 1.185V to 1.35V. In the post layout simulation, the oscillator core has a 960mW power consumption. The discrepancy between post layout simulation and measurement results arise from the difference in bias currents. In the measurement, the bias current is increased to be twice as much as the post layout simulation. The parasitic inductors and parasitic capacitors increase the oscillator load; therefore, the bias current has to be increased to sustain the oscillation. The power consumption in post layout simulation and measurements is shown in table 5.2. A tunable resistor is required to bias the buffer stage power. Howver, a fixed resistor was used instead as the PCB board did not have the space for a tunable one. As the buffer stage power consumption was not critical to the oscillator operation, a large bias current was used in testing to guarantee a large output amplitude.

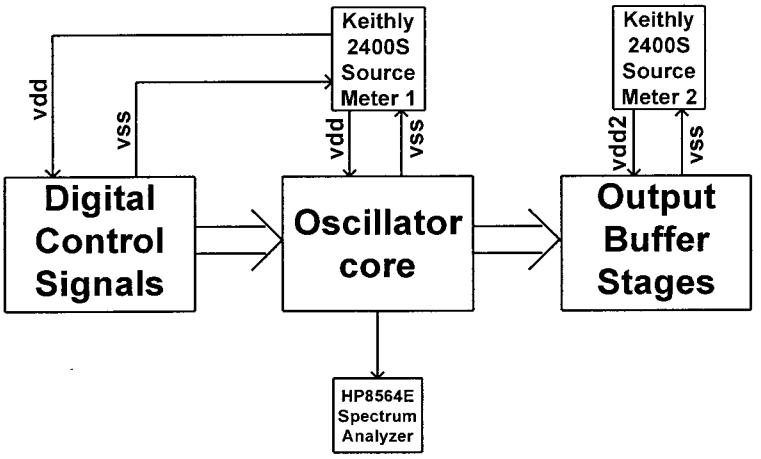


Figure 5.19: Buffer Stage Power Consumption Testbench

Table 5.2: Post Layout Simulation vs Measured Power Consumption

	Ocillator Core	Digital Block	Buffer
Post Layout Simulation	0.96mW	0.104mW	2.4mW
Measurement Results	1.724mW	0.077mW	14.3mW

5.12 Conclusion

The DCO design measured in this section demonstrates the DEM suppresses process variations. The dither in capacitor arrays increases frequency resolution; however, the far out phase noise is also increased. The architecture is not limiting in the 0.13μm technology and 32-level tree structured decoder. The benefits of the DEM can be enhanced in the implementation of a more complicated tree structured decoder and more advanced technologies.

Chapter 6: Conclusion

This chapter will summarize the design issues and discuss improvements for the future.

6.1 Accomplishments

This thesis has explored both the analog portion and the digital portion of an oscillator with a focus on the goal of suppressing capacitor process variations and achieving high frequency resolution. The DEM architecture presented is a sound choice to suppress DCO capacitor process variations when compared to other high frequency resolution oscillators. Chapter 4 presents the design of an oscillator with fine tuning and coarse tuning bands, and the implementation of the DEM architecture on the fine tuning band.

The implementation of a DCO has been presented. Chapter 5 tested the chip and the measurement results show the process variations are suppressed with the dithering on thermo-weighted capacitors. A 20kHz frequency resolution is achieved. The comparisons of the output frequencies between the dithering and non-dithering have been done both in

the simulations and measurements. Both results prove the dithering output frequencies are closer to the desired output frequencies. The measured power consumption is more than the power consumption in the post layout simulation due to the parasitics introduced in the layout process and off-chip components. Far out phase noise is introduced due to the capacitor dithering.

6.2 Issues in the Design

The parasitics in this design were under-estimated. A rough estimation of the parasitic capacitance can be done, thereby reducing fixed capacitance value and saving on-chip space. The parasitic capacitance introduced by the wiring of thermo-weighted capacitors can be reduced with more careful layout. There was a major issue of far out phase noise (i.e. greater than 50KHz offset) that was increased with the increase of dithering frequency. The simulation results verified this shouldn't have happened. The increased far out phase noise in measurement might be introduced by the digital noise. The digital and analog power supplies are using the same voltage source which is a flaw in this design.

6.3 Future work

Higher frequency resolution can be gained by using more advanced technology which shrinks the capacitor difference. Process variations can be further suppressed through adding more capacitor groups and using a more complicated DEM block. A full ADPLL could be programmed on an FPGA board to test the DCO performance in an all digital phase locked loop. The settling time, phase noise and output frequency of the loop could be measured. The whole ADPLL can also be designed, fabricated and tested. The MOS caps or Metal-Oxide-Metal (MOM) capacitors which probably have better matching tolerance could be used to improve frequency resolution.

Verilog Code Programmed on the FPGA Board

Shifter

```
// Zhanjun Bai
//100337107
//9-bit shifter
//Inputs: clk, rst
//Outputs: dout3

module shifter(clk, rst, dout3);
        input clk, rst;   //wire clk, rst;
        output [3:0] dout3;
        assign clk = KEY[0];
        assign rst = KEY[1];
        wire din; // dataout from generator
        reg [3:0] d; // 4-bit din into the shifter
        reg [1:0] counter; // counter to count up to 3 in binary
        reg [3:0] dout2; // 4-bit d into the decoder
generator gen (.clk(clk), .rst(rst), .dataout(din)); // generator to produce random bits
```

```
always @(posedge clk or negedge rst)
begin
        if (rst == 0) // resets the values
        begin
                dout2 <= 4'b0000; d <= 0; counter <= 0;
        end
        else
        begin
                d[3:1] <= d[2:0]; // set the MSB section
                d[0] <= din; // shift in new bit
                counter <= counter + 1;
                if (counter == 3) // output on every fourth cycle
                        counter <= 0;
                begin
                        dout2 <= d; // sends the d value into another output register
                end
        end
end
assign dout3 = dout2;
endmodule
```

Pseudo Random Binary Generator

```
// Zhanjun Bai
```

```
//100337107
//Pseudo Random Binary Generator
//Inputs: clk, rst
//Outputs: dataout

module generator(clk, rst, dataout);
        input clk, rst;
        output dataout; // serial_data_out
        reg [9:0] Q;     // 10 bit Q
        always @(posedge clk or negedge rst)
        begin
                if (rst == 0)
                        Q <= 10'b1010101010; // initial starting value
                else
                begin
                        Q[9:1] <= Q[8:0]; // linear feedback shift register
                        Q[0] <= Q[6]^Q[9];
                end
        end
        assign dataout = Q[9]; // outputs last bit to deserializer
endmodule
```

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