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**A COMPARISON OF PHASE NOISE CONTROL TECHNIQUES
USED IN HIGH RESOLUTION HIGH-SPEED FREQUENCY SYNTHESIZERS
FOR MOBILE RADIO TRANSCEIVERS**

by

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This thesis is submitted to the Faculty of Graduate Studies and
Research in partial fulfilment of the requirements for the
degree of

Master of Engineering

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FOR MOBILE RADIO TRANSCEIVERS**

submitted by Isabelle Jaquet in partial fulfilment of the
requirement for the degree of Master of Engineering.

Prof. T. A. Kwasniewski

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ABSTRACT

This thesis examines the issue of frequency synthesis for application in mobile radio transceivers. In this regard, an overview of the existing high resolution frequency synthesis methods is given. The emphasis is placed on fractional division synthesizers which are shown to be best suited for the selected application area. The results of a comprehensive survey of the phase noise control techniques used in fractional division PLL synthesizers are produced and the techniques with which the control of the phase noise is ensured directly by the noise shaping properties of the bit stream generator are shown to have the greatest potential for digital implementation. A characterization of these techniques through high level simulations are presented and their performance are evaluated and compared. The results of this performance comparison show that $\Sigma\text{-}\Delta$ modulators of order greater than one are the most efficient and reliable methods for phase noise control.

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LIST OF ABBREVIATIONS

DAS	Direct Analog Synthesis
DDS	Direct Digital Synthesis
DPA	Digital Phase Accumulator
DPLL	Digital Phase-Locked Loop
FFT	Fast Fourier Transform
GMSK	Gaussian Minimum Shift Keying
IS	Indirect Synthesis
LS	Level Sampling
MSK	Minimum Shift Keying
OSAD	Oversampled Analog to Digital
PLL	Phase-Locked Loop
S/H	Sample and Hold
UI	Unit Interval
VCO	Voltage Controlled Oscillator

CHAPTER 1

INTRODUCTION

1.1 Thesis Motivation and Objectives

The extensive mobility inherent in almost every aspect of modern life has created a critical need for fast, reliable mobile communications. Over the past decade, the demand for mobile services has expanded rapidly and there are currently over five million mobile communications devices in service worldwide [1]. The use of mobile radio was originally restricted to specialized users such as police departments, taxis and couriers, now it is reaching a far more general public. The expansion to an ever larger user population is imposing new constraints on the design of mobile radio systems.

In particular, to accommodate the thriving demand, better spectrum management is necessary. In this regard, digital modulation techniques, such as *Minimum-Shift Keying* (MSK) or *Gaussian-Minimum-Shift Keying* (GMSK), under which all the information is mapped into a narrow band centred around the carrier frequency [2], are anticipated to become more widely used [3][4]. As a result, the channel spacing could be reduced and more communication channels could be operated simultaneously. Since, in the modulation techniques mentioned above, the implementation of the modulation law that minimized the spectrum width, requires a fine variation of the instantaneous frequency of the carrier [5], the frequency synthesis module has to be able to support high frequency resolution.

Although resorting to closer channel spacing is expected to ease the actual congestion of the spectrum [6], it is most unlikely that this measure will be sufficient to satisfy the

entire frequency allocation demand [7]. A move towards higher operating frequencies is therefore predicted and operating frequencies in the gigahertz range have to be considered as the future requirements for frequency synthesizers in mobile radio applications [8].

Finally, the successful expansion of mobile radio services to a larger user population also depends on the availability of compact, inexpensive, low power consumption, integrated circuit devices. As a consequence, there has been a growing interest in the implementation of mobile radio sub-systems and particularly frequency synthesis modules, as monolithic digital devices.

In consideration of the above factors, the development of high-resolution high-speed digital frequency synthesizers is becoming an increasingly important issue. In the first part of this thesis, the prior art in high resolution frequency synthesis systems will be reviewed with the intention of identifying, based on their potential for silicon integration and high speed operation, those systems that are best suited for mobile radio applications. The objectives of this thesis are to evaluate and compare the phase noise control techniques used in these selected systems.

1.2 Thesis Outline

Chapter 2 begins with a brief introduction of frequency synthesis techniques. The results of an extensive literature review on high resolution frequency synthesizers are then presented. Among the currently available high-resolution techniques, the phase-locked loop system that uses the fractional division technique will be demonstrated to be the most favourable solution. The associated jitter control methods will be reviewed and analyzed in order to select those of most suitability for digital implementation. The performance of the selected techniques will then be evaluated according to the methodology given in chapter 3. The results of this performance evaluation are presented in chapter 4 along with a comparison of the different techniques. Chapter 5 provides a conclusion followed by suggestions for further research.

CHAPTER 2

OVERVIEW OF HIGH RESOLUTION FREQUENCY SYNTHESIZERS

2.1 Introduction

In this chapter, high resolution frequency synthesizers are reviewed. The material presented in this chapter will attempt to fill a gap in the literature through providing a comprehensive survey of the problems posed by the design of high resolution frequency synthesizers and of the currently available solutions to these problems. Frequency synthesizers using fractional division phase-locked loops are discussed in more detail, since they are reported to be particularly suitable for digital frequency modulation applications [5][9]. Within the subject area of fractional division, a special emphasis is placed on jitter control techniques designed to improve spectral purity. This comprehensive survey will provide the necessary background for the investigation of jitter control techniques discussed in chapter 4.

2.2 Frequency Synthesis Techniques

The purpose of a frequency synthesizer is to generate frequencies useful to the user from a small number of stable reference sources, such as crystal oscillators. In the context of multi-channel communication, as discussed in section 1.1, the synthesizer must perform two tasks:

- i) Selection of the desired channel.
- ii) Modulation of the incoming signal onto the selected channel.

Over the past 50 years, a number of frequency synthesis techniques have been developed. These techniques can be broadly divided into three groups: Direct Analog Synthesis (DAS), Direct Digital Synthesis (DDS) and Indirect Synthesis (IS) [10]. A brief discussion of each category follows.

2.2.1 Direct Analog Synthesis

With direct analog synthesis (DAS), the desired frequency is generated directly from the reference frequency using analog techniques, such as, mixing, filtering, division and switching [11][12]. A typical direct analog synthesizer is shown, as an example, in Figure 2.1. High performance, in terms of acquisition time, resolution and operating speed can be achieved with DAS methods. However, this method would result in unreasonably complex circuits if increased performance is required. Another disadvantage of DAS is the possible introduction of spurious sidebands through the use of non-linear elements.

2.2.2 Direct Digital Synthesis

There are several different techniques that are grouped under the DDS category [10]. One feature, that is common to all these techniques, is the requirement for a clock operating at a higher frequency than the synthesized frequency. Because of this feature, DDS is not viewed as a suitable approach for applications, such as mobile radio, where the operating frequency may be required to extend into the gigahertz range.

2.2.3 Indirect Synthesis

With indirect synthesis, the output signal is generated from a secondary oscillator, commonly referred to as a voltage controlled oscillator (VCO). Depending on the DC voltage

Figure 2.1 Direct Analog Synthesizer

supplied to its input, the VCO generates a sinusoidal signal at a desired frequency f_{vco} . Thus, by controlling the input voltage, any frequency within the VCO range can be obtained. However, due to the analog nature of the VCO, there is no certainty that the synthesized frequency will not drift from the required value. To compensate for this potential drift, the VCO is usually included into a phase-locked loop (PLL), device by means of which the VCO is obliged to follow the frequency of the input signal.

2.2.4 Conclusions

When compared to direct analog synthesizers, PLL synthesizers have many advantages. First, they are relatively simple and inexpensive. Second, the non-linear elements used in DAS (mixers) introduce spurious sidebands in the generated signal, whereas, in PLL synthesizers, the spectral performance depends solely on the purity of the control voltage supplied to the VCO. Finally, most of the components included in a PLL are well suited for integrated circuit implementations, the final product being generally cheaper, of a smaller size and lower power consumption than DAS circuitry.

Current integrated circuits (IC) fabrication technologies such as CMOS, Bipolar, BiCMOS and ECL facilitate high-speed circuit design making PLL synthesizers even more popular. Since PLL synthesizers best address the need for speed, compactness and low cost, they are of prime interest for applications, such as mobile radio, aimed at a large market.

2.3 High Frequency Resolution PLL Synthesizers

A brief qualitative explanation of how the different components of the phase-locked loop (PLL) operate together follows. No full mathematical description will be given, since a number of books providing an exhaustive treatment of PLL theory are referenced in the bibliography. The

Figure 2.2 Basic Phase-Locked Loop

Figure 2.3 Digital Phase-Locked Loop

basic PLL of Figure 2.2 is a servo-system including a phase detector which compares its two input signals and produces an error voltage proportional to the phase difference between them. As with any feedback system, the error signal affects the components of the loop (here, the VCO) in such a way as to reduce the error. The output of the phase detector is amplified and low-pass filtered, to eliminate all the unwanted high frequency components, before being applied to the VCO as a control voltage. When the loop reaches equilibrium, the signals of both inputs of the phase detector have the same frequency and a constant phase offset and the loop is said to be "in-lock". For the basic loop of Figure 2.2, equilibrium occurs when f_{vco} and f_{ref} are equal. Since, in this particular case, the only frequency that can be synthesized is equal to f_{ref} , the application of the PLL as a frequency synthesizer is extremely limited. To change the in-lock relation between f_{vco} and f_{ref} , so that a range of useful frequencies can be generated, additional components have to be introduced in the feedback loop. One of the most widely used configuration is shown in Figure 2.3, where the feedback component is a frequency divider and where the synthesized frequency is an exact multiple of the reference frequency.

$$f_{vco} = N \times f_{ref} \quad (2.1)$$

When this is the case, the use of a programmable divider allows a large number of frequencies, all multiples of f_{ref} , to be synthesized by changing the value of N . It can be noted that a PLL structure containing a divider in the feedback loop is often referred to as a "Digital PLL" or DPLL¹ even though most of the blocks of the loop may actually be analog blocks.

Equation (2.1) shows that the smallest achievable frequency step is equal to f_{ref} and is obtained by changing N by 1. When a fine resolution is required, f_{ref} has to be small and N large. However, for several reasons, it is not desirable to decrease f_{ref} beyond a certain limit. First, a low frequency crystal oscillator requires support by complex circuitry for stable operation. Second, fast

¹ Although other definitions of a DPLL are being used, this definition is the one considered throughout this thesis.

PLL settling time and low reference frequency are opposing requirements. In effect, since the main role of the loop filter is to eliminate the harmonics of f_{ref} that could show up at the phase detector's output, its bandwidth (B) has to be substantially lower than f_{ref} [13]. Therefore, the settling time, which is inversely proportional to B [13], increases as f_{ref} decreases, eventually reaching unacceptable high values.

In conclusion, when both a short settling time and a fine resolution are required, significantly more complex circuitry may be needed. To allow for a small frequency increment and for a short settling time, several different techniques have been presented in the literature. Two different approaches will be examined in the following sections. The first uses two or more loops that can be either cascaded [14] or nested [18] while the second retains a single-loop configuration by using the technique known as "fractional division" [15].

2.3.1 Multiloop Systems

Multiloop systems are not a new concept. The first description of a multiloop system implementation can be traced back to 1952 [14]. Indeed, they are still used in some communication equipment, particularly, in the area of microwave synthesizers [16][17].

2.3.1.1 Cascaded Multiloop

A typical cascaded multiloop system is shown in Figure 2.4 [12]. In this example, two loops are used, one which divides the output frequency by N and the other by M. Both VCO frequencies are combined through an analog mixer to produce an output frequency of the following form:

$$f_{out} = N \times f_{ref1} - M \times f_{ref2} + f_{offset} \quad (2.2)$$

Figure 2.4 Cascaded Multiloop Synthesizer

Once the reference frequencies f_{ref1} and f_{ref2} are fixed, the output frequency can be adjusted to the desired value by changing N and/or M . Although f_{ref1} and f_{ref2} have to be kept relatively large to meet the settling time specification, they can be chosen so that the difference between the two is equal to the required increment (Δf). Thus, by simultaneously changing N and M by 1, the output frequency will be changed by

$$\Delta f = |f_{ref1} - f_{ref2}| \quad (2.3)$$

A rough comparison, between the switching time achievable with both the cascaded multiloop and single loop configurations, can be made based upon the example values of Figure 2.4. In this comparison, the settling time value of each loop will be calculated from its reference frequency using the following practical estimations [13].

$$B \text{ (closed loop bandwidth)} = 0.1 \times f_{ref}$$

$$T_{switch} = \frac{3}{B} \quad (2.4)$$

$$\Rightarrow T_{switch} = \frac{30}{f_{ref}}$$

In a multiloop system, a worst case estimate of the total settling time is obtained by taking the sum of the settling time values of each loop. Consequently, if T_1 and T_2 are the switching times achieved by each one of the loops, the corresponding total settling time ($T_{multiloop}$) is given by

$$T_{multiloop} \leq T_1 + T_2 = \frac{30}{f_{ref1}} + \frac{30}{f_{ref2}} = 6.03 \text{ ms} \quad (2.5)$$

This value has now to be compared to the settling time obtained from a single loop system allowing for the same frequency resolution. Since, for a single loop system, the smallest achievable frequency step is equal to the reference frequency, the single loop system achieving a resolution of Δf operates with a reference frequency equal to

$$f_{ref} = \Delta f = |9.9 \text{ kHz} - 10 \text{ kHz}| = 100 \text{ Hz} \quad (2.6)$$

The corresponding settling time is given in equation (2.7). When comparing $T_{\text{multiloop}}$ and $T_{\text{single loop}}$, it becomes apparent that, for the same achieved frequency increment, a multiloop system provides a great improvement of settling time performance.

$$T_{\text{single loop}} = \frac{30}{f_{ref}} = 300 \text{ ms} \quad (2.7)$$

2.3.1.2 Nested Multiloop Operating in Time Domain

The method shown in Figure 2.5 [18] actually postdates fractional division, which will be discussed in section 2.3.2. This method is presented as a time domain alternative to generate a relation similar to a typical fractional division relation (2.8).

$$T_s = (N + \frac{m}{q}) \times T_{ref} \quad (2.8)$$

Consider two signals of periods T_s and T_a related by a vernier relation as in equation (2.9). If a method allows $(N - m)$ periods T_s and m periods T_a to fit within a reference period T_{ref} (equation (2.10)), then the relation between f_{ref} ($1/T_{ref}$) and f_s ($1/T_s$) is defined by equation (2.8).

$$T_a = T_s + \frac{1}{q} \times T_s \quad (2.9)$$

$$(N-m) \times T_s + m \times T_a = T_{ref} \quad (2.10)$$

The nested multiloop system implementing this fractional relationship between T_s and T_{ref} is shown in Figure 2.5. An explanation of how equations (2.9) and (2.10) are actually performed in this system follows.

The main loop which controls the main oscillator (SO) operates with a period T_s while the inner loop, controlling the auxiliary oscillator (AO), operates with a period T_a . Considering first the operation of the inner loop, the divider FD1 divides the output of SO by $q+1$ and, therefore, supplies a signal of period $(q+1)T_s$ to the first input of the phase detector. The feedback divider, present in the inner loop, supplies a signal of period qT_s to the second input of the phase detector. Hence, when the loop locks, T_s and T_a satisfy the relationship defined by equation (2.11). Since equations (2.9) and (2.11) are equivalent, the vernier relation is performed by the inner loop.

$$q \times T_a = (q+1) \times T_s \quad (2.11)$$

The second operation to be executed is defined by equation (2.10). Two dividers, each with a variable division factor (DVDF), are used. At the beginning of the process, the DVDFs are loaded with their respective division factor $(N - m)$ for DVDF1 and m for DVDF2. The system continuously alternates between two different modes: the open-loop mode (*mode1*) and the closed-loop mode (*mode2*). Initially, the switches SW1 and SW2 are open (*mode1*). The divider DVDF1 starts counting the pulses of SO and when it reaches the preset value of $(N - m)$, it issues a pulse that propagates through some control circuitry to close the switches SW1 and SW2. Hence, during the first $(N - m)T_s$ seconds of T_{ref} , the loop is open and no feedback signal is sent to the main phase detector PD1. Once the switches are closed (*mode2*), the inner loop locks itself to the required period T_s and DVDF2 counts m pulses of AO. Then, as another reference period starts, the system returns to *mode1*. The main loop is in lock when $(N - m)$ SO periods and m AO

periods fit exactly into the reference period T_{ref} , thus performing the function described in equation (2.10).

As a result, a fractional relationship is established between T_s and T_{ref} allowing the system of Figure 2.5 to change the output frequency by fractional increment of the reference frequency. This system is therefore capable of achieving any required frequency resolution independently of the reference frequency.

2.3.2 Fractional Division

The fractional division technique was originally introduced as a method to avoid resorting to the complex configuration necessary for multiloop systems. Fractional division is based on the concept that it is possible to achieve small frequency step without decreasing the reference frequency by allowing the divider of the digital PLL to take on fractional values. Although a frequency divider cannot normally divide the incoming frequency by a number other than an integer, the division by a fractional number can be achieved by switching between the two integral division ratios of a dual-modulus divider (Figure 2.6). For example, if the integral division factor is chosen to be equal to N , p times, and to $(N+1)$, q times, once every $(p+q)$ cycles, the VCO output frequency will be divided on average by

$$\frac{p \times N + q \times (N+1)}{p+q} = N + \frac{q}{p+q} \quad (2.12)$$

The notation $N.F$ is often used to represent the fractional division factor, N referring to the integer part of the division factor and F to the fractional part. Here,

$$F = \frac{q}{p+q} \quad (2.13)$$

Figure 2.6 Fractional Division Phase-Locked Loop

The main disadvantages of this otherwise simple technique is that, as it will be further explained in the next paragraph, the pulses at the output of the divider are no longer separated by equal time intervals. This error in the positioning of the edges corresponds to a phase error, commonly referred to as jitter.

First, consider the waveform corresponding to a ideal division of the VCO frequency by a fractional number $N.F$ (Figure 2.7a). Since a division of the frequency corresponds to a multiplication of the period, for every ideal frequency division by $N.F$, the time interval separating two consecutive negative transitions of the waveform, is equal to $(N.F) \times T_{VCO}$ (Figure 2.7a). This ideal waveform can now be compared to the actual waveform obtained through the use of the dual-modulus divider. One common method used to implement a dual-modulus divider is referred to as the "pulse swallowing technique" [19]. The output pulses generated with this technique are shown in Figure 2.7b. It can be seen, that a division by N corresponds to a pulse of period $N \times T_{VCO}$, while a division by $(N+1)$ corresponds to a pulse of period $(N+1) \times T_{VCO}$. As a consequence, each division by N introduces an error in the period and the negative transition occurs earlier than the ideal transition. This time error (Δt_N) between transitions corresponds to a phase error step (equation (2.15)). The result is a voltage jump proportional to this phase error step at the phase detector's output.

$$\Delta t_N = N.F \times T_{VCO} - N \times T_{VCO} = F \times T_{VCO} \quad (2.14)$$

$$\frac{\partial \Delta \phi(n)}{\partial n} = \frac{\Delta t_N}{T_{ref}} = \frac{F}{N.F} \quad (2.15)$$

Likewise, each division by $(N+1)$ introduces a voltage jump proportional to $(F-1)$. An example of the resulting staircase waveform at the phase detector's output is shown in Figure 2.8 ($N.F=6$).

One of the most undesirable features of the signal present at the phase detector's output is its periodicity. In effect, since series of exactly p divisions by N and q divisions by $(N+1)$ are

a)

b)

Figure 2.7 Fractional Division Operation

Figure 2.8 Output of the Sample/Hold Phase Detector

performed every $p+q$ reference periods, the accumulated phase error over $p+q$ reference periods ($\Delta\phi_{n+p+q} - \Delta\phi_n$) is equal to

$$\Delta\phi(n+p+q) - \Delta\phi(n) = p \times \frac{F}{N.F} + q \times \frac{(F-1)}{N.F} \quad (2.16)$$

Substituting the expression of F given by equation (2.13).

$$(N.F) \times (\Delta\phi(n+p+q) - \Delta\phi(n)) = \frac{p \times q}{p+q} + q \times \left(\frac{q}{p+q} - 1 \right) = 0 \quad (2.17)$$

Equation (2.17) shows that the signal at the output of the phase detector is periodic, of periodicity $(p+q)T_{ref}$. This signal is the superimposition of the AC periodic staircase waveform on the steady state DC voltage used to tune the VCO at the required output frequency (Figure 2.8). Of these two components, only the DC part is needed to control the VCO. The AC part, inherent to the fractional division technique, is responsible for an undesired periodic modulation of the VCO frequency, modulation which takes, in the frequency domain, the form of high spurious spectral lines. The presence of these spurious lines in the frequency band of interest cause a severe deterioration of the quality of the synthesized signal.

2.3.4 Conclusions

Although multiloop synthesizers address the need for better resolution while maintaining a decent bandwidth and a reasonably short settling time, they have several disadvantages. The high parts count, due to the use of more than one loop, along with the proper shielding required between loops' analog components, result in a fairly expensive system. A further disadvantage of the cascaded multiloop structure is that the risk of having spurious spectral components is increased by the presence of one or more non-linear elements (mixers). For the nested multiloop structure, the limiting factor is the required time resolution.

In comparison, the fractional division method is simple, inexpensive and therefore appears more desirable. Providing that the aforementioned jitter problem can be controlled, the fractional division technique could result in high resolution, low cost frequency synthesizers for use in consumer products.

2.4 Phase Noise Control Techniques

As explained in section 2.3.2, the implementation of a fractional division into the feedback loop by dynamically changing the division factor introduces periodic jitter that can considerably affect the performance of the system. Since the fractional division method is by far the most promising high resolution frequency synthesis technique, designers have put a considerable design effort to reduce this jitter. The different approaches that have been considered to suppress the high spurious spectral lines can be separated into three categories: analog compensation, randomization or jitter injection technique, and higher order noise shaping methods. None of these techniques, which will be discussed in the following sections, have been, to date, fully analytically described, neither their performance evaluations nor their application constraints have been fully analyzed in literature.

2.4.1 Compensation Techniques

2.4.1.1 Digiphase Principle

Among the analog compensation techniques, probably the most widely used is the digiphase technique. It was first described in a paper by G.C. Gillette published in 1969 [20]. Following this, the digiphase or derivations of it, have been widely reproduced in a large number of textbooks, journal papers and patents [10][13][21][22][23][24][25][26].

Figure 2.9 Simplified Digiphase Synthesizer

Figure 2.10 Digital Phase Accumulator

The digiphase technique was proposed to take advantage of the properties of the module that controls the dual-modulus divider. In effect, as it will be further explained, this module, which consists of an adder and a register (Figure 2.10), always contains a digital representation of the phase error. Because of this important characteristic, it was called digital phase accumulator (DPA). An explanation of the operation of a digiphase synthesizer based upon a simplified block diagram (Figure 2.9) follows.

On each reference period (f_{ref}), the accumulator is incremented by K . When the accumulator content exceeds the capacity ($M=2^L$) of the adder, an overflow occurs and the capacity of the adder is subtracted from the register. Therefore, the register value is increased by $K-M$ on each overflow and by K the rest of the time. The overflow signal is then used to control the divider. Each reference period during which no overflow occurs corresponds to a division by N and the reference periods with overflow correspond to a division by $(N+1)$. Therefore, an increase of the register content by K (no overflow) corresponds to a division by N which, in turn, corresponds to a phase error step proportional to F (see section 2.3.2). Likewise, an increase by $K-M$ (overflow) corresponds to a phase error step proportional to $(1-F)$. For example, Table 2.1 shows the relation between the accumulator content and the phase error for $K=3$ and $M=8$.

Table 2.1 Accumulator Content and Phase Error

$K = 3, M = 8$								
Reference periods	0	1	2	3	4	5	6	7
Accumulator content	0	3	6	1	4	7	2	5
	0	K	$2K$	$3K-M$	$4K-M$	$5K-M$	$6K-2M$	$7K-2M$
$(N.F) * \Delta\phi$	0	F	$2F$	$3F-1$	$4F-1$	$5F-1$	$6F-2$	$7F-2$

a)

b)

c)

Figure 2.11 Cancellation Process in the Digiphase Technique

Since, with the DPA, the average number of reference periods between two overflows is equal to M/K , an average of $(1-K/M)$ division by N and K/M division by $(N+1)$ are performed. As a result, a fractional division by $N.F$, when F is equal to K/M , is achieved (equation (2.18)).

$$N.F = (1 - \frac{K}{M}) \times N + (\frac{K}{M}) \times (N+1) = N + \frac{K}{M} \quad (2.18)$$

From Table 2.1 and equation (2.18), it is shown that the phase error is indeed always proportional to the content of the accumulator.

The cancellation process, devised by Gillette, consists of translating this digital representation of the phase error into an analog voltage by means of a Digital-to-Analog converter (D/A converter). The actual compensation is then achieved by adequately inverting and amplifying the output of the D/A converter in order to produce a waveform that exactly cancels the undesired AC part of the phase detector's output (Figure 2.11a-b). A phase error free voltage can then be supplied to the VCO (Figure 2.11c).

The actual results that can be expected from this method depends substantially upon two factors. First, the cancellation waveform has to be precisely synchronized with the error waveform for the cancellation to proceed (equal delay in the two paths) . Second, the converter and the summer amplifier can introduce their own inaccuracies in the system. Even with high quality devices, the advantage of the cancellation could be partly lost. In conclusion, high spectral purity can only be achieved when the circuit design ensures a perfect matching of the delays and gains in both the error and the signal paths.

2.4.1.2 Level Sampling Technique

The level sampling (LS) system, whose schematic is shown in Figure 2.12 [27], has been proposed to overcome the problems associated with the digiphase technique. In the digiphase

Figure 2.12 Level Sampling Technique

technique, a cancellation waveform had to be created and added to the error waveform to compensate for the phase error. Inaccuracies result from imprecise scaling and synchronization of the cancellation waveform. In contrast, the LS method allows the cancellation of the AC part by directly altering the output of the phase detector. Therefore, this system avoids the use of two different paths, removing the need for fine synchronization.

The operation of this system can be explained with the following example. Consider the error waveform shown in Figure 2.13. Because of its periodicity and its staircase shape, the error voltage takes a different value during each quarter of the total period (T_e). To take advantage of this feature, four sample and hold (S/H) elements are used. They are controlled by a commutator, so that each S/H element always samples the error voltage during the same quarter of T_e . As a result, the output of each S/H unit is constant and equal to the corresponding value of the voltage (Figure 2.14). These four outputs are then fed into a summer which averages them, and a voltage divider then scales the resulting average to generate the desired control voltage for the VCO.

One of the limitations of such a technique lies in the number of S/H units required. Recall that p divisions by $(N+1)$ and q divisions by N every q reference periods are necessary to perform a division by the fractional ratio $(N+p/q)$. As a consequence, the number of reference periods within the repetitive error pattern period is equal to q , thus q S/H units are necessary. Consider, for example, the typical mobile radio specifications used by Molina [5]. A frequency resolution of 781.25 Hz is to be achieved from an operating frequency of 400 kHz. If these specifications have to be met with using the level sampling technique for phase noise compensation, the required number of S/H elements is equal to $400/0.78125$ or 512. It can be concluded that, for a given reference frequency, the overall complexity of the system rapidly increases with the frequency resolution. Furthermore, the average values coming from the summing device are in general different for each division ratio. Since digital modulation techniques requires that the division ratio be continuously changed, a whole set of voltage dividers would have to be used along with the

Figure 2.13 Error Waveform

Figure 2.14 Output of the S/H Units

control circuitry allowing the corresponding continuous adjustment. The level sampling technique is therefore clearly not suitable for the selected application area.

2.4.1.3 Pulse Delay Compensation

Although the pulse delay compensation method [28], shown in Figure 2.15, belongs to the analog compensation techniques, it conceptually differs from the methods presented in the previous sections. In those methods, all the jitter produced by the fractional division propagates through the phase detector and some action is taken *a posteriori* to reduce its unwanted modulation effect. In the pulse delay method, however, the compensation takes place within the feedback loop and directly alters the misplaced pulses.

The system works as follows. As in the digiphase technique, the dual modulus divider is controlled by a phase accumulator (Figure 2.10) whose content is always proportional to the phase error between the actual (f_2) and the ideal (f_{2ideal}) waveform (Figure 2.16b-e). Since the phase shift and the delay between the pulses are two different expressions of the same phenomenon, the content of the accumulator is also proportional to the delay between the two waveforms. The technique then uses an analog representation of this content to drive a variable delay unit. This unit adds an appropriate delay to each pulse of f_2 so that the trailing edges of both waveforms coincide. Thus, by producing a pulse at the end of each delay period, the unit generates a compensated waveform (Figure 2.16f) whose frequency is equal to the ideal frequency. An example of the implementation of the pulse delay unit is shown on Figure 2.17. At each leading edge of f_2 , the ramp generator starts a negative ramp whose slope depends on the D/A's output (Figure 2.17b). When the trailing edge of f_2 is detected, the signal returns to its initial value at a uniform rate until it reaches a reference level and a pulse is issued (Figure 2.17b-c). The reference level can be chosen so that the total delay corresponding to each D/A's output matches the desired value.

Figure 2.15 Pulse Delay Compensation Technique

Figure 2.16 Pulse Delay Compensation Process

Figure 2.17 Pulse Delay Unit

The pulse delay system provides compensation by directly controlling the position of the pulses in time. Satisfactory results can be expected when f_{ref} is low. But, since the delays are fractions of the reference period, it might be difficult to precisely adjust the position of the pulses when f_{ref} is high.

2.4.1.4 Quantized Compensation

The technique described by Ivanov in 1983 [29] is similar to the pulse delay compensation method presented earlier in the sense that it directly performs an adequate positioning of the pulses in time. The values of the required delays are computed, according to a specifically devised algorithm, and then applied to the pulses via a delay generator (Figure 2.18). The originality of this method lies in the assumption that, for a division by a fractional number ($N + \alpha/\beta$), the delay between the actual and ideal pulse is always equal to an integer multiple of a, so called "error quantum". If this assumption is accurate, the need for a high precision variable delay generator is eliminated, instead, any required delay can be produced from a set of discrete delay units, all multiples of this error quantum.

This assumption can be validated using the following reasoning. To achieve the fractional ratio ($N + \alpha/\beta$), a total of α divisions by N and $\beta - \alpha$ divisions by $N+1$ have to be performed. For each division by N a pulse is issued after N VCO periods, likewise, for each division by $N+1$, a pulse is issued after $N+1$ VCO periods. Consider the i^{th} division of the sequence and assume that p divisions by N ($p \leq \alpha$) and q divisions by $N+1$ ($q \leq \beta - \alpha$) have already been performed. The real waveform has gone through K_{actual} VCO periods

$$K_{actual} = p \times N + q \times (N+1) \quad (2.19)$$

Figure 2.18 Quantized Compensation

The position of the last pulse issued in the real waveform becomes

$$t_{actual} = (p \times N + q \times (N+1)) \times T_o \quad (2.20)$$

When considering the ideal waveform at the same i^{th} stage, $(p+q)$ division by $(N+\alpha/\beta)$ have been performed and the position of the last pulse is

$$t_{ideal} = (p+q) \times (N + \frac{\alpha}{\beta}) \times T_o \quad (2.21)$$

The resulting time error (Δt_i) between the two pulses is given by equation (2.22).

$$\Delta t_i = t_{ideal} - t_{actual} = ((p+q) \times \alpha - q \times \beta) \times \frac{T_o}{\beta} \quad (2.22)$$

In summary,

$$\Delta t_i = \omega_i \times \frac{T_o}{\beta} \quad (2.23)$$

and

$$\omega_i = (p+q) \times \alpha - q \times \beta \rightarrow \omega_i \in \mathbb{N} \quad (2.24)$$

whereas ω_i is the integer factor defining the delay to be applied from the error quantum T_o/β .

Equation (2.24) indicates that the assumption made earlier is valid. It also shows that each ω_i value is completely determined by the current division ratio D_{i+1} and the i^{th} previous division ratios. These values can therefore be computed using the following recursive equations.

$$D_{i+1} = N \rightarrow \omega_{i+1} = \omega_i + \alpha \quad (2.25)$$

$$D_{i+1} = (N+1) \rightarrow \omega_{i+1} = \omega_i + \alpha - \beta \quad (2.26)$$

Providing that the total division sequence is known, each delay will be defined. One way to proceed would be to pre-store each division sequence and to use the set of division ratios as an input to the computational unit. Instead, a method was proposed to dynamically generate the division sequence while bounding the jitter. Since divisions by N tend to increase the time error and divisions by $N+1$ tend to decrease it, it is possible to interlace the division by N and $N+1$ to ensure that the absolute value of the time error will never be greater than $2T_0$ ($\omega_i < \beta/2$). The dual modulus divider divides by N and, for each division performed, the time error increases by $\alpha T_0/\beta$. At each stage, a test is performed on ω_i and the divider's modulus is changed to $N+1$ when $(\omega_i + \alpha)$ goes over $\beta/2$. This division by $N+1$ decreases the time error and thus maintains it within the defined limits. The equations describing the complete algorithm are:

$$\omega_{i+1} = \omega_i + \alpha \quad , \text{ if } (\omega_i + \alpha) < \frac{\beta}{2} \quad (2.27)$$

$$\omega_{i+1} = \omega_i + \alpha - \beta \quad , \text{ if } (\omega_i + \alpha) \geq \frac{\beta}{2} \quad (2.28)$$

In conclusion, the system described in Figure 2.18 reduces the jitter in two different ways. First, the jitter is bounded by the use of an specifically devised division sequence. Second, a delay is computed and applied to each pulse exiting the divider to provide an appropriate compensation in the time domain. The use of a computational unit to determine the delays and to control the divider is relatively problem-free. With commonly available computing power, the time needed to compute each new value can easily be made lower than the reference period. However, for high VCO output frequencies (f_{vco} in the gigahertz range) the minimum delay to be applied would be equal to fractions of a nanosecond. It would be unrealistic to implement delay elements and the corresponding control circuitry given such a short time resolution.

2.4.2 Noise Shaping Methods (order > 1)

The notion of noise shaping was first introduced in the context of oversampled sigma-delta (Σ - Δ) modulation. Σ - Δ modulators have been mainly used for implementing high rate Oversampled Analog-to-Digital converters (OSAD) [30]. However, based upon the observed similarities between the digital phase accumulator (DPA) and a typical first order Σ - Δ modulator (Figure 2.19 and Figure 2.20), emerged the idea that the well known noise shaping properties of Σ - Δ modulator could be used advantageously in the context of fractional division PLLs [31]. A brief discussion on these noise shaping properties follows.

One common method to analyze Σ - Δ modulators consists of modelling the quantizer as an additive noise source (Figure 2.21) [32]. This modelling allows the system to be analyzed as a linear system and transfer function, for both the signal and noise, to be derived. In the example of Figure 2.21, these transfer functions can be expressed as

$$H_{\text{signal}}(s) = \frac{1}{s + 1} \quad (2.29)$$

$$H_{\text{noise}}(s) = \frac{s}{s + 1} \quad (2.30)$$

Since the noise transfer function exhibits a high-pass characteristic, the noise is shaped so that very little of its content is in the low frequency range. This feature proves extremely useful in the frequency synthesis context by allowing to attenuate the amount of noise present within the loop filter bandwidth.

The use of higher order Σ - Δ modulators has been proposed to further improve the noise attenuation [31]. The use of these modulators have two main advantages. First, is that each

Figure 2.19 Block Diagram Representation of the Digital Phase Accumulator

Figure 2.20 Model of a First Order Σ - Δ Modulator

Figure 2.21 Linearized Model for a Σ - Δ Modulator

integrator introduces an additional zero in the noise transfer function. This results in a higher order filtering and in an accentuation of the attenuation of the noise near DC. Second, while the quantization noise found in first order Σ - Δ modulators is periodic and results in discrete spectral peaks, higher order modulators are known to decorrelate the noise from the signal and therefore to produce a white or pseudo-white quantization noise [35]. Thus, higher order modulators can provide a greatly improved noise behaviour around DC. The main limitation to the use of higher order loops is the increasing complexity.

2.4.3 Randomization or Jitter Injection

Since the main cause of the presence of undesired spurious spectral lines is the repetition of phase error patterns, the jitter injection method is based on the concept that it is possible to eliminate these lines by randomizing the phase error and therefore destroying the periodicity that originated them. Presented in Figure 2.22 is a technique achieving this randomization which was patented by Wheatley in 1983 for use in a direct digital synthesizer [34].

The system of Figure 2.22, appears to be built around a digital phase accumulator (DPA). The DPA, which was defined in section (2.4.1.1) as a control generator for the dual-modulus divider, is used here as a direct digital synthesizer. The synthesized frequency (f_{out}) is taken to be the overflow signal and is equal to

$$f_{out} = \frac{K}{M} \times f_{ref} \quad (2.31)$$

where K/M denotes the average number of reference periods between overflows. In the case of the DPA, exactly K overflows occur during every sequence of M reference periods. Consequently, considering M successive reference periods, the register content is increased by the input value K on each of the M reference periods and decreased by the capacity M of the accumulator on each of the K overflows. At the end of the sequence, the register content therefore returns to its original

Figure 2.22 Jitter Injection Technique

Figure 2.23 Spectrum Without Jitter Injection

Figure 2.24 Spectrum With Jitter Injection

value, and the operation of the register is periodic of period $M \cdot T_{ref}$.

The periodicity of the register content, in turn corresponds to a periodicity of the overflow signal which is represented, in the output power spectrum as strong spurious peaks (Figure 2.23). To avoid this undesirable effect, the jitter injection element is connected to the synthesizer. Once in every output period, a random number is subtracted from the accumulator (this random number will be added back during the next output period to maintain the required average frequency). Consequently, the occurrences of overflows, which previously were following a strict pattern, have now been randomized and the undesired periodicity has been destroyed. The spurious spectral lines have, therefore, been removed as required. Unfortunately, they have been replaced by white noise representative of the randomization (Figure 2.24). Although the total noise energy has actually been increased, the attenuation of the side-peaks amplitude is considered a performance improvement.

As mentioned earlier, the jitter injection technique was designed for use as a direct digital synthesizer. Its presence in an overview on fractional division phase-locked loop systems is justified since the jitter injection technique is actually a DPA with a randomized input. As such, it has all the functional properties of a DPA and can be used to control a dual-modulus divider. Furthermore, since the DPA can also be identified as a first order Σ - Δ modulator, the jitter injection technique can be considered a first order noise shaping unit.

2.5 Summary

In this chapter, phase-locked loops using fractional division have been demonstrated to be the best potential solution to the problem of high resolution frequency synthesis for mobile radio. The necessity of controlling the phase noise inherent to the fractional division technique has also been established and different methods of achieving this task have been reviewed.

Because compensation methods rely on high precision analog components to perform the compensation (D/A converters or high resolution delay generators), they are not considered a reasonable approach for the selected application area. A new strategy, that has recently emerged concentrates on altering the jitter at the source rather than compensating for it later. In this regard, bit stream generators used to control the dual modulus divider are now in the spotlight and alternatives to the classical digital phase accumulator (DPA) have been developed. The jitter injection technique and the noise shaping methods fall within this new category of phase noise control techniques. Since both these techniques circumvent the use of analog components, they appear to have a great potential for silicon integration and are therefore considered as particularly suitable for mobile radio applications.

Although the jitter injection technique was first introduced in 1981, no analysis of its performance as a bit stream generator has been reported in the literature. As for the noise shaping methods, the emergence of the concept is still recent (November 1989) and no complete characterization is available yet. The lack of documentation has necessitated a detailed performance evaluation of these techniques. The results of this evaluation, which are presented in chapter 4, are meant to provide the necessary background information to the engineer faced with the need to resort to these new methods of jitter control.

CHAPTER 3

PERFORMANCE EVALUATION METHODOLOGY

3.1 Introduction

Analysis of the jitter control techniques conducted in the previous chapter highlights the techniques possessing the highest potential for silicon integration and therefore, most suitable for mobile radio applications. In chapter 4, a comparison of the selected techniques will be made by subjecting them all to the same simulation and performance evaluation environment. In this chapter, the performance evaluation methodology is presented. The proposed methodology consists primarily of two phases. First, a high level simulation of the given structure allows a verification of its functionality. Second, once the proper functional behaviour of the structure has been established, its performance is evaluated by conducting appropriate data processing on the simulation results. Both phases are discussed in detail in the following sections.

3.2 Phase I: High Level Simulation

The high-level simulator used for this study is SPLICE [35] which is an event-driven mixed-mode simulator. In mixed-mode simulation, logical and electrical analysis are performed concurrently, thus allowing the designer to choose the level of analysis best suited to each part of the circuit. The circuit to be simulated is usually described from elementary sub-models which are assembled in a netlist based source deck. Standard models such as NAND, NOR, inverter and buffer are incorporated in the SPLICE program. In addition, an extension of the program has been developed by researchers at Carleton University to allow the user to define fully customized models. These models are described using RATFOR, a FORTRAN preprocessor language.

compiled and linked with the simulator as subroutines, and finally used in the SPLICE source deck as any other SPLICE model. The result is that any complex functional blocks can thus be modelled and incorporated as high level objects into the SPLICE simulator.

Although first-order timing information given by the logical analysis would be sufficient to validate the integrity of the system, electrical analysis mode has been used due to its convenience. Since most of the structures to be examined are required to operate with a fairly large wordlength (>12 bits), the definition of these structures as electrical models allows each bus to be described as one analog voltage, thus significantly simplifying the representation of the complete circuit. This choice also keeps the possibility open to include any of those models as part of a more complex hybrid system without need for further digital-analog interface.

The extraction of the SPLICE model for a simple sub-circuit is given here as an example. The circuit shown in Figure 3.1 is a first order Σ - Δ modulator. It includes a summing node, a non-delaying integrator, a zero comparator and a unit delay. Consider, for instance, the ideal accumulator made from the combination of the summing device and the integrator. If X_n is the n^{th} output of the summing device and Y_n the n^{th} output of the integrator, the difference equation for the non-delaying integrator is

$$Y_n = Y_{n-1} + X_n \quad (3.1)$$

The action of the feedback path is to switch one of the inputs of the accumulator from +M to -M depending on the previous output of the zero comparator (+1 or -1). X_n can therefore be expressed as

$$X_n = K + Z_{n-1} \times M \quad (3.2)$$

Figure 3.1 Schematic of a First Order Σ - Δ Modulator

From equations (3.1) and (3.2), one can now derive the complete difference equation of the system.

$$Y_n = Y_{n-1} + K + Z_{n-1} \times M \quad (3.3)$$

Table 3.1 shows the RATFOR model's description of this accumulator ². It is apparent that the generation of the model file from the difference equation is elementary. Consequently, the description of this structure as a high level digital model is extremely simple and results in better time efficiency than a description involving the standard models incorporated in SPLICE.

3.3 Phase II: Data Processing for Performance Evaluation

In the course of phase I, flat files representing the waveform at each node of interest are created. A set of subroutines have been developed, using C programming language, to process the files and to extract information on the performance of the system under consideration.

As explained in section 2.3.2, the use of the fractional division technique causes the introduction of phase noise. This phase noise (jitter) will flow through the phase detector, corrupt the signal controlling the VCO and alter the quality of the synthesized signal. In the remaining part of this thesis, different bit stream generator structures, used to control the dual-modulus divider will be examined (Figure 3.2). Since the focus is on investigating how these different structures perform at controlling the phase noise performance of the complete synthesizer, the phase noise power spectrum, taken at the output of the phase detector, is considered to contain all the relevant information. It is therefore natural that it has been chosen as the main evaluation basis. Note that the phase detector is followed by a low-pass filter, and that, in fact, only the

² All the RATFOR models developed for the different systems analyzed in this thesis are presented in Appendix A along with the corresponding SPLICE source decks.

```

#elmod1 :accumulator 1
.define elmod1
.numout 1
.numinp 3
.*begin
#-----
#      I. Jaquet
#      June 5,1990
#      ACCUMULATOR 1
#
# Yn   = evop1
# K    = evin1
# M    = evin2
# Zn-1 = evin3
#
#-----

#-----> Variable Declaration

integer outo,out
real    pi,T,nin

#-----> Initializations

genflg = .true.
if(lastim == -1)
{
out = 0
}

#----- > Recalling the Previous Value (Yn-1)

if(lastim != simtim )
{
outo = out
}

#-----> Computing the Difference Equation ( $Y_n = Y_{n-1} + K + M \cdot Z_{n-1}$ )

evop1 = nint(outo + evin1 + evin2*evin3)
out = evop1
.end

```

Table 3.1 RATFOR model description of First Order Σ - Δ Modulator

Figure 3.2 Fractional Division Phase-Locked Loop

amount of phase noise power contained within the bandwidth (f_b) of this filter affects the purity of the VCO output. The bandwidth B is a design parameter of the synthesizer and it will be considered as a variable in this study.

The proposed procedure is as follows (Figure 3.3):

- compute the phase error on the divider's output
- run an FFT to obtain its spectral representation
- consider the integrated power contained within the loop bandwidth ($0 \rightarrow B$).

Ideally, the phase noise power spectrum would have to be normalized with respect to the amplitude of the carrier frequency. However, since the phase error signal does not contain information about the carrier, this standard scaling cannot be used for the phase error spectrum. An alternative scaling of the phase error is suggested.

The phase error or jitter of a squarewave waveform as compared to an ideally periodic waveform is defined in the time domain as an error in the positioning of the edges. Therefore, the first natural unit that one would want to express the jitter in is a absolute time unit (seconds). Although this value is of real importance in some aspect of circuit design ³, it can be demonstrated that expressing the phase error with a relative unit (radians for instance) is preferable for the analysis dealt with in this thesis. Figure 3.4 shows, as an example, the effect of a constant absolute phase error value of 1 μ s on a waveform at 100 kHz (middle plot) being ten times larger than its effect on a waveform at 10 kHz (top plot). In contrast, for a given relative jitter value (0.1 UI or $0.2 \cdot \pi$ rad), the jitter spectral amplitude in dBc remains the same as the average frequency (f_{osc}) changes. This confirms that only a relative unit appropriately characterizes the spectral amplitude of the jitter. From the two most commonly used relative units, radian and "Unit

³ The phase detector has to be designed so that it operates linearly up to the maximum phase error.

Figure 3.3 Performance Evaluation Methodology (1)

Figure 3.4 Example Spectra for Various Absolute and Relative Jitter Values

Interval" (UI), which are strictly equivalent, the "Unit Interval" has been chosen. By definition, a value of one UI corresponds to a phase error of 2π radians. In the remaining part of this report all the time domain jitter values will be expressed in UI. For reasons of consistency, the jitter will also be expressed in UI in the frequency domain and a scaling that leads to a representation of the phase noise power spectrum in UI is therefore proposed. Appendix B documents how this scaling is achieved.

Although the phase noise power spectrum taken at the output of the phase detector is considered as the basis for performance evaluation, it will be shown in section 4.2.2.2 that the power spectrum at the output of the bit stream generator is equivalent to the output of the phase detector and that it can therefore equally well be used as a reference point. In fact, the bit stream power spectra contain all the information relevant to the comparison of the different bit stream generators and in the remainder of this thesis, the attention will be focused on the output of the bit stream generators (Figure 3.5).

3.4 Conclusions

A specific methodology for performance evaluation of digital PLL frequency synthesis systems has been presented. This methodology has been specially devised for analysis and comparison of different bit stream generators when used as jitter control techniques. The performance evaluation of the selected techniques is presented in the next chapter.

Figure 3.5 Performance Evaluation Methodology (2)

CHAPTER 4

JITTER CONTROL BY NOISE SHAPING

4.1 Introduction

In the overview on jitter control techniques of chapter 2, the techniques, for which the jitter is directly controlled by the bit stream generator module, were identified as the most suitable for mobile radio applications. The noise shaping methods, now extended to the digital phase accumulator (DPA) and the jitter injection technique, belong to this category and have therefore been selected for performance evaluation. These techniques were modelled, simulated and their performance was evaluated following the methodology detailed in chapter 3.

In the first section of this chapter, the general principles involved in the control of the phase noise by a noise shaping unit will be detailed. In the second section, the simulation results, obtained for the DPA technique, will be produced with the intention of demonstrating the necessity to resort to more elaborate structures (jitter injection techniques and higher order noise shaping). Finally, the results of the simulation performed on these structures will be presented and their performance will be compared.

4.2 Theory of Jitter Control by Noise Shaping

The main purpose of the use of Σ - Δ modulators in the fractional division PLL context is to take advantage of the noise shaping properties of the bit stream. In a first part, the well known properties of Σ - Δ modulators that are involved in this noise shaping action will be reviewed. Then, the implication of the noise shaped characteristics of the bit stream on the phase noise

performance of the synthesizer will be discussed.

4.2.1 Noise Shaping in Σ - Δ modulation

The view of a Σ - Δ modulator as a noise shaping unit is based on its analysis as a linear system. A representation of a first order Σ - Δ modulator is shown in Figure 4.1 as an example ¹. The two basic elements of this system are an ideal delaying integrator ² and a quantizer which is the non-linearity of the system. One common way to analyze this system is to observe that the main consequence of the quantizer's presence is the introduction of quantization noise. The quantizer is therefore usually modelled as an additive noise source [32]. The substitution of the non-linearity (quantizer) by a linear element (noise source) allows the structure of Figure 4.1 to be seen as a regular linear system. The corresponding discrete time (Z domain) model is shown in Figure 4.2. The transformation of the modulator into a linear system allows typical linear analysis tools to be used. In particular, the transfer functions influencing both the signal and the noise can be derived (Equations (4.1) and (4.2)).

$$\text{Delaying Integrator} = Dint = \frac{z^{-1}}{1 - z^{-1}} \quad (4.1)$$

$$H_{noise}(z^{-1}) = \frac{1}{1 + Dint} = 1 - z^{-1} \quad (4.2)$$

$$H_{signal}(z^{-1}) = Dint \times H_{noise}(z^{-1}) = z^{-1}$$

A similar analysis can be used to determine the signal and noise transfer functions for the general N^{th} order Σ - Δ modulator shown in Figure 4.3.

¹ The term modulator refers to a device that transforms (modulates) the analog input voltage or the multibit input word into single bit representation.

² The term ideal integrator refers to an integrator whose output is not limited.

Figure 4.1 First Order Σ - Δ Modulator Figure 4.2 Z Domain Model for a First Order Σ - Δ Modulator

Figure 4.3 N^{th} Order $\Sigma\text{-}\Delta$ Modulator

$$H_{\text{noise}}(z^{-1}) = \frac{K \times (1 + \sum_{i=1}^{i=N} \alpha_i) \times (1 - z^{-1})^N}{(1 + \alpha_1 \times z^{-1} + \dots + \alpha_N \times z^{-N})} \quad (4.3)$$

$$H_{\text{signal}}(z^{-1}) = \frac{K \times (1 + \sum_{i=1}^{i=N} \alpha_i) \times (z^{-1})^p}{(1 + \alpha_1 \times z^{-1} + \dots + \alpha_N \times z^{-N})}$$

In Equations (4.3), K is the DC gain and p represents the number of delaying integrators used in the system. The actual values of K, p and of the coefficients α_i s depend on the hardware implementation of the modulator. However, since, as it will be further explained, the term $(1 - z^{-1})^N$ present in the noise transfer function is the only term accountable for the noise shaping action, all the coefficients defined above can be considered as of secondary importance for the analysis of noise shaping.

The frequency response corresponding to the general transfer functions given in equations (4.3) can then be computed by letting $z = e^{j\omega T_{\text{clock}}}$. Since a *Bode plot* representation with both the gain and the frequency expressed in logarithmic scales not only allows to display the fine detail of the frequency response near DC but also permits to estimate this frequency response near DC by its straight line asymptote, it is particularly appropriate for the description of noise shaping. Figure 4.4a gives, as an example, the frequency response obtained for the first order system of Figure 4.2 (equations (4.2)). It can be observed from these plots that the noise transfer function shows, at the origin, a slope of 20 dB/decade characteristic of a zero of order 1. Likewise, since the general noise transfer function of a N^{th} order $\Sigma\text{-}\Delta$ modulator shows a zero of order N, the frequency response obtained for such a system is anticipated to display an asymptotic $20 \times N$ dB/decade behaviour near DC. A linear system acts as a filter on the various frequency components applied to its input and the relative changes in the amplitude of the different

Figure 4.4 Theoretical Signal and Noise Transfer Function

frequency components are determined by the transfer function ($H(z)$). If $H(\omega)$ is the frequency response of the system, the relation between the power spectrum at the output ($S_y(\omega)$) and that of the input ($S_x(\omega)$) is given by equation (4.4).

$$S_y(\omega) = |H(\omega)|^2 \times S_x(\omega) \quad (4.4)$$

Consequently, the shape of the frequency response directly defines the attenuations taking place between the input and output power spectra. In particular, the presence of the zero of order N in the noise transfer function of equation (4.3) will cause the quantization noise to be attenuated in the low frequency range. This filtering of the noise around DC and thus around all multiple of the clock frequency is the effect commonly referred to as noise shaping.

It should be noted, however, that there is no account, in the curves of Figure 4.4a, for the sampling effect due to the discrete time operation of the system. Since Σ - Δ modulators operate, as indicated in Figure 4.1 and Figure 4.3, in time with a clock, an intrinsic sampling (sampling frequency = f_{clock}) occurs. This sampling results in a filtering of the bit stream by the function defined in equation (4.5).

$$H(f) = \frac{\sin(\pi \times \frac{f}{f_{\text{ref}}})}{(\pi \times \frac{f}{f_{\text{ref}}})} \quad (4.5)$$

The overall filtering that effects the bit stream spectrum can now be determined as the combination of the filtering due to sampling and of the filtering due to the transfer functions. Figure 4.4b shows a representation of this overall filtering as computed for the first order system of Figure 4.2. Note that the filtering due to sampling mainly modifies the spectrum near the sampling frequency. It has been only mentioned here for the completeness of the description of the bit stream spectrum but it does not have any consequences for the analysis of noise shaping near DC.

Finally, to complete the characterisation of the bit stream power spectrum, the frequency content of the noise has to be determined. In the case of analog Σ - Δ modulators, the quantization noise is almost always assumed to be white and independent from the signal [36]. The presence of analog noise sources makes this assumption valid in most cases. Since the operation of digital Σ - Δ modulators is certainly fully deterministic, the validity of these assumptions for such structures, is very questionable. However, as the order of the modulator increases, its behaviour is expected to become more and more in agreement with these assumptions. In particular, the quantization noise corresponding to modulators of higher order ($N > 1$) has been reported to be white [37]. In the cases where the quantization noise is white, the noise spectral density is constant ($S_x(\omega) = C, \forall \omega$) and the shape of the bit stream noise power spectrum is directly proportional to the frequency response (equation (4.4)). The N^{th} order noise filtering described above has therefore an optimum effect, the noise power spectrum computed at the modulator's output is guaranteed to show a $20 \cdot N$ dB/decade decrease in the low frequency range and the bit stream is successfully noise shaped.

As for the supposition that the noise is uncorrelated with the signal, it is known to be generally faulty. In fact, the incomplete decorrelation of noise and signal may cause the apparition, in the bit stream spectrum, of strong tones located at frequencies equal to

$$f_{\text{tones}} = m \times d \times f_{\text{clock}} \quad (4.6)$$

where m is an integer, d is the density of logical ones in the bit stream or also the DC value of this bit stream. In the context of fractional division PLL, the modulator is clocked with the reference signal f_{ref} ³ and the tones are therefore located at

$$f_{\text{tones}} = m \times d \times f_{\text{ref}} \quad (4.7)$$

³ The justification for this assumption is given in section 4.2.2.1

If in theory, any input value smaller than the feedback value can be used, thus allowing any density between 0 and 1 to be achieved, in practice, extreme values of the input may cause one or more integrator(s) to saturate. A saturation of the bit stream can also, under certain conditions, be observed. Since these saturations introduce non-linearity in the operation, the modulator cannot be operated over the full range of input values. The range of input values that can be used without saturation ($[v_{min}, v_{max}]$) defines the range of density ($[d_{min}, d_{max}]$) that can be achieved in the output bit stream. When operated within these ranges, all the tones are located at frequencies above $d_{min} * f_{ref}$. Consequently, if d_{min} is greater than 0.1, these tones are outside the loop filter bandwidth (recall $B=0.1*f_{ref}$ [13]). Since a d_{min} value of 0.25 has been reported to be typical of second order modulators [31][38] and that the range substantially deteriorates as the order of the system increases, it is reasonable to assume that B and d_{min} will, in most cases, be such that the impact of these tones can be ignored. However, in the few cases where the loop filter bandwidth has to be made larger than d_{min} , the determination of the influence of these peaks will require further study.

4.2.2 Σ - Δ modulation in Fractional Division Frequency Synthesis

In the previous section, the mechanism that allows the binary data stream to be noise shaped near DC has been explained. After a brief discussion on how the bit stream generator should be interfaced with the fractional division PLL, the crucial assumption that the noise shaped characteristic of the bit stream is sufficient to ensure an adequate control on the phase noise spectrum will be justified.

4.2.2.1 *Considerations on the Interfacing*

When incorporating the bit stream generator into the fractional division PLL, the synchronization of the two elements has to be treated with special care. A correct synchronization

Figure 4.5 Synchronisation with a Jittered Signal

Figure 4.6 Proposed Synchronization

is achieved when a new bit of the data stream is read at the beginning of each division (by N or $N+1$). Consequently, the approach that has been considered so far is to clock the modulator with the output signal of the divider (Figure 4.5) [31][23]. With this approach, however, the modulator's input is sampled with a jittered clock (average frequency f_{ref}) and this jittered sampling may affect the operation of the modulator, especially in the case of dynamic inputs. A different approach is therefore proposed here (Figure 4.6). The modulator is clocked with a jitter-free signal (f_{ref}), thus avoiding the deterioration of the modulator's operation that jittered sampling may cause, while the output bits are latched in a buffer and released on the jittered clock to ensure the synchronization with the divider. From this point on, Σ - Δ modulators, for use as bit stream generators for the fractional division PLL, will therefore always be considered to be clocked with the reference signal (f_{ref}).

4.2.2.2 Phase Error Spectrum versus Bit Stream Spectrum

The relation between the bit stream spectrum and the phase error spectrum taken at the output of the phase detector can be determined by observing the waveforms of Figure 4.7. It can be seen from these waveforms that, once a proper synchronization of the complete synthesizer has been achieved, each bit of the bit stream corresponds to a division ratio (N or $N+1$) (Figure 4.7a and b). As explained in the general discussion on fractional division of section 2.3.2, each division by an integral division ratio, in turn, corresponds to the introduction in the jittered waveform of a phase error step (equations (4.8)).

$$\begin{aligned}
 \text{Division by } N &\rightarrow \frac{\partial \Delta \phi(n)}{\partial n} \propto F \\
 \text{Division by } (N+1) &\rightarrow \frac{\partial \Delta \phi(n)}{\partial n} \propto (F-1)
 \end{aligned}
 \tag{4.8}$$

Figure 4.7 Correspondence between Bit Stream and Phase Error Waveforms

A direct correspondence can therefore also be established between the bit values and the instantaneous phase error steps. Although the amplitudes of the two waveforms are different, it is apparent that the transitions of the phase error steps waveform (Figure 4.7c) are strictly identical to these of the bit stream waveform (Figure 4.7a). The frequency contents of the two waveforms are therefore identical. Now considering the phase error waveform present at the output of the phase detector (Figure 4.7d), it represents, by definition, the integrated version of the waveform of Figure 4.7c (equation (4.9)).

$$\Delta\phi(t_n) = \sum_{n=0}^{n=n_{max}} \frac{\partial\Delta\phi(n)}{\partial n} \quad (4.9)$$

Consequently, the bit stream spectrum and the phase noise spectrum, taken at the output of the phase detector, contain the same frequency component and the only difference between the two spectra is caused by the integration that is taking place when computing the accumulated phase error. An ideal integration can be represented, in the Z domain, as a division by $(1-z^{-1})$. The $20*N$ dB/decade attenuation of the noise, present in the bit stream spectrum, therefore becomes an attenuation of $20*(N-1)$ dB/decade in the phase error spectrum. Hence, the use of a noise shaped bit stream in the control of the dual-modulus divider allows the phase noise at the output of the phase detector to be also noise shaped. Consequently, by controlling the rate of noise attenuation in the bit stream, one can also obtain a full control of the phase noise in the low frequency range.

4.2.3 Conclusions

In the above discussion, the phase error spectrum, taken at the output of the phase detector, was demonstrated to be exclusively determined by the bit stream spectral characteristics. Consequently, the amount of phase noise contained in the loop filter bandwidth fully depends on the performance of the Σ - Δ modulator used as bit stream generator. The remaining of this chapter therefore deals with the characterization of selected of bit stream generator structures. The results of a performance evaluation performed on these structures are presented in the following sections.

4.3 Digital Phase Accumulator

The digital Phase Accumulator (DPA) has already been mentioned several times in this thesis. In particular, all the noise shaping methods considered to date (jitter injection technique or Σ - Δ modulators) were reported to be derived from the DPA structure. As a consequence, the performance obtained with the DPA represents a reference in the evaluation of the improvements that can be provided by these noise shaping structures. After a brief discussion on the operation of the DPA as a noise shaping unit, simulation results will be presented.

4.3.1 Operation of the DPA

Figure 4.8 shows a schematic diagram of the digital phase accumulator (DPA). On every reference period, the input value is sampled and added to the previous content of the phase register. When the register content exceeds the capacity (M) of the accumulator, an overflow occurs and M is subtracted from the register. Since the overflow is a non-linear process, the accumulator described in Figure 4.8 is really a non-linear device. However, the linear part and the non-linear part can be separated by representing the accumulator as an ideal integrator followed by a quantizer which symbolizes the non-linear overflow. Furthermore, the subtraction of M from the register content on each overflow can be represented by a negative feedback path (gain M) connecting the output of the quantizer to the input of the integrator. The above considerations allow the DPA to be regarded as a typical first order Σ - Δ modulator (Figure 4.9). As a consequence, an analysis, similar to the one detailed in section 4.2.1, can now be conducted and the transfer functions for both the signal and the noise can be derived from the linear Z-domain model shown in Figure 4.10. These transfer functions are given in equations (4.10). The frequency response of these transfer functions is shown in Figure 4.11, along with the resulting overall filtering combination of the sampling effect and the noise shaping effect (see section 4.2.1). Since curves have been computed from the transfer functions of equation (4.10), they represent the

Figure 4.8 Block Diagram Representation of the DPA

Figure 4.9 The DPA as a First Order Σ - Δ Modulator

Figure 4.10 Linear Z Domain Model for the DPA

Figure 4.11 DPA Transfer Functions

$$\begin{aligned}
 H_{noise}(z^{-1}) &= \frac{(1 - z^{-1})}{1 + (M-1) \times z^{-1}} \\
 H_{signal}(z^{-1}) &= \frac{z^{-1}}{1 + (M-1) \times z^{-1}}
 \end{aligned}
 \tag{4.10}$$

operation of the DPA structure more precisely than the general first order transfer functions. However, the two sets of curves appear to be identical and the interpretation is very similar in both cases. The discussion conducted in section 4.2.1 is therefore not repeated here.

4.3.2 Simulation Results

In this section, the results of the simulation performed on the DPA structure are presented. The top plot of Figure 4.12 shows an example of bit stream power spectrum obtained with a fixed input value ($K = 5233$, $M = 16384$). As predicted from theory, this spectrum displays the 20 dB/decade attenuation characteristic of a first order Σ - Δ modulator. These results therefore confirm the validity of the linear modelling described in section 4.2.1. The content of the spectrum also clearly corroborate the fact that the white noise assumption is not accurate in the case of first order structures. In fact, if M and K do not have any common divisor, the quantization noise is strictly periodic of period $M \cdot T_{ref}$ and this periodicity is represented in the frequency domain by spikes located at frequencies equal to $m \cdot f_{ref}/M$ ($m \in \{1, M\}$). Since, in practice, the capacity of the accumulator is large, the presence of these spikes in the baseband cannot be avoided. As for the amplitude of the spikes, it can be seen, by comparing the bottom plots of Figure 4.12 and Figure 4.13, that it greatly differs from one value of K to the other. For the reasons that will be developed later in this section, the fact that there is little control on the amplitude of the spikes is sufficient to renounce considering the DPA as a satisfactory jitter control technique. Therefore, for the study conducted here, a complete determination of the spectral characteristics of the bit stream noise is not necessary. An exhaustive treatment of this matter can be found in the

Figure 4.12 Bit Stream Power Spectrum for the DPA Structure (1)

Figure 4.13 Bit Stream Power Spectrum for the DPA structure (2)

Figure 4.14 Comparison of Phase Noise Power Spectra

following literature sources [36][39][40].

In the example case shown in Figure 4.13, the amplitude of the peaks increases at a rate of ± 20 dB/decade as the frequency approaches each harmonic of $K/M \cdot f_{ref}$. In such a case, the intrinsic quantization noise also increases at the same rate towards DC and the attenuation of 20 dB/decade imposed on this noise by the noise transfer function only manages to force the peaks to have a constant amplitude. This constant amplitude is clearly visible in the *Bode plot* representation shown in the top plot of Figure 4.13. Although the noise shaping action still takes place as predicted, the noise cannot be guaranteed to decrease towards DC. Because of the direct correspondence that exists between the bit stream and the phase noise, the great variation found in the bit stream spectrum from one input value to the other also reflects on the phase error spectrum (Figure 4.14). Note that the relation between bit stream spectrum and phase error spectrum is as expected from theory (see section 4.2.2.2).

4.3.3 Conclusions

In this section, the results obtained by simulation have been shown to be in agreement with the theory. In particular, the validity of the adopted linear analysis has been established. However, the classical assumption that the noise is white has been confirmed to be incorrect in the case of the DPA. As a result, the DPA structure fails to guarantee an adequate first order noise shaping of the bit stream and it cannot be considered as a satisfactory jitter control technique. Since a completed noise attenuation near DC heavily relies on the assumption that the quantization noise is white, techniques that result in a randomized quantization noise have to be considered. Two of such techniques, the jitter injection technique and a second order $\Sigma\Delta$ modulator will be analyzed in the following sections.

4.4 Jitter Injection Technique

The jitter injection technique was introduced as a technique, for use as a direct digital synthesizer, that uses a randomization process to suppress the periodicity characteristic of a DPA. The claim made by the inventor of this technique is that the spikes present in the DPA's bit stream spectrum are replaced by a noise floor [41]. In this section, the use of the jitter injection technique as a bit stream generator will be examined and a new interpretation will be proposed.

4.4.1 Operation of the Jitter Injection Technique

A block diagram representation of the jitter injection technique is given in Figure 4.15. This system operate as follows. On each overflow, a random number (X_n) is added to the input value K and the resulting sum is fed into the DPA. On the next reference period, X_n will be subtracted to maintain the desired average properties. It should be noted that, in the description of the system made by C.E. Wheatley [41], the random number X_n is required to be taken from a random sequence uniformly distributed between 0 and $K-1$. The detail of the circuitry that generates the random sequence and synchronizes it with the DPA is detailed in the patent that was also granted to Wheatley [34]. The introduction of a random noise at the input of the DPA causes the occurrences of the overflows to be randomized and the quantization noise therefore becomes white. Furthermore, since the jitter injection technique is viewed as a DPA with randomized input, the signal and noise transfer functions are identical in both systems (equations (4.10)). As a consequence, the jitter injection technique operates as a first order noise shaping unit. It is expected to avoid the problems inherent to the DPA through ensuring that the quantization noise in the bit stream spectrum is white and will therefore exhibit a guaranteed 20 dB/decade attenuation of the quantization noise near DC. Note that the assumption made by Wheatley that the output noise takes the form of a noise floor proves inaccurate.

Figure 4.15 Block Diagram Representation of the Jitter Injection Technique

4.4.2 Simulation Results

An example of bit stream and phase error spectra obtained from the simulation of the jitter injection technique is shown in Figure 4.16. This simulation was performed, as suggested in section 4.4.1, with a jitter magnitude equal to the input magnitude ($K = 2501$). The noise spectrum, shown in the top plot, appears to have been successfully randomized by the injection of a white noise at the input of the DPA and the noise level is, as predicted, attenuated at a 20 dB/decade rate towards DC.

However, it can be observed from the results of the simulation performed with a larger input value ($K = 5233$) and thus a larger jitter magnitude (Figure 4.17), that the attenuation may, in some cases, not be as complete as in the example of Figure 4.16. In effect, the process of randomization through the injection of a white noise causes a noise floor to be superimposed on the noise shaped quantization noise. When the jitter injection technique is operated with too large a jitter magnitude the level of this noise floor, which rises as the magnitude of the jitter increases, may become the main contribution to the total bit stream noise in the low frequency range. The consequence, after integration through the phase detector, is an actual increase of the phase noise power near DC which negates the expected improvements (bottom plot of Figure 4.17). In fact, the amount of phase noise power present in the low frequency range even appears to be much higher than with the DPA operated with no random jittering (Figure 4.14 and Figure 4.17).

The top plot of Figure 4.18 shows an example of bit stream spectrum for which the noise floor level has been reduced by lowering the jitter magnitude. An empirical investigation has permitted to determine that the jitter injection technique leads to an acceptable phase noise spectrum when the sum of the input and jitter magnitude is less than half of the capacity (M) of the accumulator. However, as illustrated in the bottom plot of Figure 4.18, such a reduction of the jitter magnitude may, in some cases, result in an incomplete randomization of the quantization

Figure 4.16 Example of Bit Stream and Phase Error Spectra (1)

Figure 4.17 Example of Bit Stream and Phase Error Spectra (2)

Figure 4.18 Example Spectra for Various Jitter Magnitudes

2

of/de

2

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS
STANDARD REFERENCE MATERIAL 1010a
(ANSI and ISO TEST CHART No. 2)

5.2 Suggestions for future research

The material presented in this thesis, in fact, corresponds to the first stage of a much broader project that aims at realizing an integrated circuit implementation of a complete frequency synthesizer for mobile radio. In this regard, now that the most suitable phase noise control technique has been identified, future work could be carried out in optimizing and physically implementing a digital second or third order digital Σ - Δ modulator and in incorporating it into a fractional division frequency synthesizer.

In the course of this thesis, some exploratory work was considered and several new techniques for phase noise control were approached. However, since time did not permit to thoroughly investigate these techniques, another project could be to follow up this study through characterizing alternative methods to those examined here.

Figure 4.19 Z-Domain Model for the Second Order Modulator

Figure 4.20 Transfer Functions for the Second Order Modulator

far (DPA and jitter injection technique), the quantizer was representing an overflow process but, in the cases under consideration in this section, the quantizer is a zero-comparator which issues an output value of +1 when its input is greater than zero and a output value of -1 otherwise. To make the comparison of the bit streams easier, the resulting output waveform was transformed into a logical waveform (0s and 1s) before being applied to the dual-modulus divider. Note that the modulator described in Figure 4.19 also comprises two gain components. The presence of adequately chosen gain components is generally required in all higher order modulators to avoid saturation in the integrators [42]. The choice of these coefficients is therefore of primary importance and should be considered as an integral part of the modulator design. However, the optimization of these coefficients is beyond the scope of this thesis and the simulations were performed with coefficients that were reported to lead to a satisfactory operation [42].

Once the Z domain model is defined, the signal and noise transfer functions representing the modulator can be derived. For the second order modulator of Figure 4.19, these transfer functions can be expressed as

$$H_{noise}(z^{-1}) = \frac{(1 - z^{-1})^2}{1 + (\frac{3M}{2} - 2) \times z^{-1} + (1 - M) \times z^{-2}} \quad (4.11)$$

$$H_{signal}(z^{-1}) = \frac{0.5 \times z^{-1}}{1 + (\frac{3M}{2} - 2) \times z^{-1} + (1 - M) \times z^{-2}} \quad (4.10)$$

The frequency response corresponding to these transfer functions and the overall filtering that results are shown in Figure 4.20.

As for the third order modulator used in this study, its Z domain model is given in Figure 4.21. Like in the case of the second order modulator discussed above, the quantizer is a zero-comparator, all the integrators are non-delaying integrators and optimized feedback

Figure 4.21 Z-Domain Model for the Third Order Modulator

Figure 4.22 Transfer Functions for the Third Order Modulator

coefficients are considered [42]. The transfer functions of this third order modulator are given in equation (4.11) and the corresponding frequency response is shown in Figure 4.22.

$$\begin{aligned}
 H_{noise}(z^{-1}) &= \frac{(1 - z^{-1})^3}{1 + (-3 + 1.02 M) \times z^{-1} + (3 - 1.64 M) \times z^{-2} + (-1 + 0.7 M) \times z^{-3}} \\
 H_{signal}(z^{-1}) &= \frac{0.032 \times z^{-1}}{1 + (-3 + 1.02 M) \times z^{-1} + (3 - 1.64 M) \times z^{-2} + (-1 + 0.7 M) \times z^{-3}}
 \end{aligned} \tag{4.11}$$

4.5.2 Simulation Results

The simulated bit stream and phase error spectra for both the second and the third order modulator are shown respectively in Figure 4.23 and Figure 4.24. In both cases, the assumption that the quantization noise in the bit stream can be considered as random is confirmed. As a consequence, the effect of the transfer function is optimum and the noise is guaranteed to be attenuated at a rate of $20 \times N$ dB/decade in the low frequency range. The anomaly observed at high frequencies in the simulation results is due to the incomplete decorrelation of the noise from the signal. Apart from this detail which was explained to have little consequences on the performance of the system (see section 4.2.1), both the second and the third order modulators are shown to have a nearly ideal behaviour. These structures therefore circumvent all the problems inherent to the other structures examined thus far and allow for an optimal control on the phase noise spectrum.

4.6 Summary

In the previous sections of this chapter, various bit stream generators were characterized and the relative advantages of some of the structures over the others were discussed. In this section, the principal results will be summarized and a classification of the different bit stream

Figure 4.23 Example of Bit Stream and Phase Error Spectra for 2nd Order Modulator

Figure 4.24 Example of Bit Stream and Phase Error Spectra for 3rd Order Modulator

generators will be proposed. This classification will be based on the compared performance obtained with the different structures for a given average output density ($d \approx 0.31$) and a given level of implementation complexity (accumulator's size = 14 bits). The comparison criteria is chosen to be the total amount of phase noise power contained in the loop filter bandwidth (B). However, the bandwidth B is a design parameter of the complete PLL synthesizer and it is considered here as variable (see section 3.3).

The results of this comparison are shown in Figure 4.25. As suggested in section 4.5, the second and third order Σ - Δ modulator, respectively represented with dotted and dashed-dotted lines, provide the best results in terms of attenuation near DC. In addition, the position of the corresponding curves, here computed on a specific example ($d \approx 0.31$), can be predicted and remains unchanged over the operating range and the performance of both Σ - Δ modulators as jitter control techniques is therefore very reliable. In the graph of Figure 4.25, the results for the jitter injection technique are represented with the two dashed lines. The top curve corresponds to the results obtained with a large jitter magnitude and the results are clearly much worse than those obtained with a second or a third order modulator. However, even with small jitter amplitudes, the injection of an external noise causes the total noise power to increase and the performance obtained with the jitter injection technique is rather mediocre. This poor performance, combined with the relatively high implementation complexity due to the use of a random number generator, make the jitter injection technique a less favourable approach than the previously discussed higher order modulators. As for the digital phase accumulator (DPA), its performance is represented with the two solid lines. Both curves show discrete steps coinciding with the spikes present in the phase noise spectrum. The higher of these two solid curves corresponds to the results obtained when the noise shaping fails to guarantee the 20 dB/decade attenuation of the phase noise. In such a case the performance is shown to be substantially degraded. Furthermore, the significant difference in the level of the two curves illustrates the extreme unreliability of the DPA as a phase noise control technique. It should be noted, however, that when the synthesizer is only to synthesize few

- * ——— DPA (top plot = failed noise shaping)
- DPA (bottom plot = with noise shaping)
- * * - - - - Jitter Injection Technique (top plot = large jitter magnitude)
- - - - Jitter Injection Technique (bottom plot = small jitter magnitude)
- 2ND Order modulator
- 3RD Order modulator

Figure 4.25 Comparison between Various Bit Stream Generator Techniques

frequencies (which is certainly not the case in mobile radio applications), and when, at the same time, the capacity of the accumulator is small, all the spikes produced with the DPA may very well lie outside the bandwidth. Under such conditions the DPA would be the simplest and the most preferable technique.

In conclusion, it appears from this study that, for the selected application area, the second or third order $\Sigma\Delta$ modulators are the most promising solutions. Both methods are reliable in ensuring a noise shaping of the bit stream thereby controlling the amount of phase noise influencing the performance of the PLL synthesizer. Because of its higher order, the third order modulator provides a greater attenuation than a second order. However, its implementation requires the use of three integrators and the constraints on the choice of the feedback coefficients is much tighter than for the second order structure. The final decision on which of these structures is to be used must be based upon the application specifications.

CHAPTER 5

CONCLUSIONS

5.1 Summary

The objective of this thesis was to examine the issue of frequency synthesis under the light of the constraints specific to mobile radio applications. Amongst the existing high resolution frequency synthesis techniques, phase-locked loop synthesizers using the fractional division technique were shown to be the best potential solution for the selected application area. However, the necessity of controlling the phase noise inherent to this fractional division technique was established. Since there has been, to date, no literature published on this subject material, a comprehensive survey of the different methods to achieve this task was presented. The analysis of these methods permitted to identify the methods with which the jitter is directly controlled by the bit stream generators as best suited for digital implementation.

Three such techniques were examined in this thesis: digital phase accumulator, jitter injection technique and higher order noise shaping methods. Since very little information, if any, is available on the operation and performance of these techniques as bit stream generators, a characterization of these techniques was conducted. All the selected techniques were classified as digital Σ - Δ modulators and the well known noise shaping properties of these modulators were demonstrated to be the basis of the process of controlling the phase noise. The results of the qualitative performance evaluation of the selected technique has indicated that Σ - Δ modulators of order greater than one were the most efficient and reliable solutions.

5.2 Suggestions for future research

The material presented in this thesis, in fact, corresponds to the first stage of a much broader project that aims at realizing an integrated circuit implementation of a complete frequency synthesizer for mobile radio. In this regard, now that the most suitable phase noise control technique has been identified, future work could be carried out in optimizing and physically implementing a digital second or third order digital Σ - Δ modulator and in incorporating it into a fractional division frequency synthesizer.

In the course of this thesis, some exploratory work was considered and several new techniques for phase noise control were approached. However, since time did not permit to thoroughly investigate these techniques, another project could be to follow up this study through characterizing alternative methods to those examined here.

APPENDIX A

RATFOR MODELS

```

#elmod1 accumulator 1
.define elmod1
.numout 1
.numinp 4
.*begin
#-----
#      I.Jaquet
#      June 5, 1990
#      ACCUMULATOR 1
# count1 = evop1
# K      = evin1
# M      = evin2
# jitter = evin3 (Y/N)
# sinus  = evin4 (Y/N)
#-----
#---->Declaration of variables
integer outo,out_flg
integer i,imax
real   val(100000),nin,jitter,sinus
#---->Initializations
genflg = .true.
if(lastim == -1) {
  open (unit=13,file="..matlab/wave.dat")
  open (unit=14,file="..matlab/ran.dat")
  jitter = evin3
  sinus  = evin4
#---->Jitter injection (read the random values in ran.dat)
  if(jitter == 1.0){
    imax = 16384
    for(i = 0; i < imax; i = i + 1)
      {read(14,*)val(i)}
  }
  else{
    for(i = 0; i < imax; i = i + 1)
      {val(i) = 0}
  }
  out = 0
  flg = 0
  i = 1}
#---->Recalling previous value and write to output file
if(lastim != simtim ){
  pi = 3.1416
  T = 1638.4
  outo = out
  write(13,*) wave}
#---->Computing difference equations
if(sinus == 1.0){
  nin = evin1 + 1000*sin(2*pi*simtim/T)
  evop1 = outo + nin)
}
else{
  evop1 = outo + evin1)
if(evop1 >= evin2){
  out = evop1 - evin2 + val(i) - val(i-1)
  i = i + 1
  wave = 1}
if(evop1 < evin2){
  out = evop1
  wave = 0}
}
.end

```

A.1 RATFOR Model for DPA and Jitter Injection Technique

```

splice
DPA or Jitter Injection Technique
.model accu1 elmod: model=1
.model src1 dc : 5.
.model src2 dc : 16.
.model src3 dc : 0.0
.model src4 dc : 0.0

int1 count1,K M jitter sinus accu1

K K src1
M M src2
J jitter src3
S sinus src4

time 1us 17364us
go
end

```

A.2 SPLICE Source Deck for DPA and Jitter Injection Technique

```

#elmod1 : accumulator 1
.define elmod1
.numout 1
.numinp 3
.*begin
#-----
#   I. Jaquet
#   June 5,1990
#   ACCUMULATOR 1
# count1 = evop1
# K   = evin1
# M   = evin2
# c   = evin3
#-----
#---->Declaration of variables
integer outo,out
real pi,T,run
#---->Initializations
genflg = .true.
if(lasum == -1){ out = 0 }
#---->Recalling previous value
if(lasum != sumum ){ outo = out }
#---->Computing difference equation
evop1 = nint(outo + evin1/2 + evin3*evin2/2)
out = evop1
.end

#elmod2 : accumulator 2
.define elmod2
.numout 1
.numinp 3
.*begin
#-----
#   ACCUMULATOR 2
# count2 = evop1
# count1 = evin1
# str   = evin2
# M     = evin3
#-----
#---->Declaration of variables
integer outo,out;
#---->Initializations
genflg = .true.
if(lasum == -1){ out = 0 }
#---->Recalling previous value
if(lasum != sumum ){ outo = out }
#---->Computing difference equation
evop1 = outo + evin1 + evin3*evin2
out = evop1
.end

```

```

#elmod3 : comparator + delay
.define elmod3
.numout 1
.numinp 1
.*begin
#-----
#   ZERO COMPARTOR
# wave  = output waveform (0.1)
# stream = evop1 (-1,1)
# count2 = evin1
#-----
#---->Declaration of variables
integer in,ino
#---->Initializations
genflg = .true.
if(lasum == -1){ open (unit=16,file="matlab/wave.dat") }
#---->Recalling previous value
if(lasum != sumum ){
  ino = in
  wnte(16,*)wave)
#---->Zero comparator
in = evin1
if (ino >= 0){
  evop1 = -1
  wave = 1 }
else{
  evop1 = 1
  wave = 0 }
.end

```

```

splice
Second order Sigma-Delta Modulator
.model accu1      elmod: model=1
.model accu2      elmod: model=2
.model comp       elmod: model=3
.model src1 dc : - 311
.model src2 dc : 1024

int1      count1, K M str      accu1
int2count2, count1 str M  accu2
comp      str, count2          comp

K  K      src1
M  M      src2

time 1us 17384us
go
end

```

A.4 SPLICE Source Deck for 2nd Order Σ - Δ Modulator

```

#elmod1 . accumulator 1
.define elmod1
.numout 1
.numinp 3
.*begin
#-----
#      I. Jaquet
#      June 5,1990
#      ACCUMULATOR 1
# count1 = evop1
# K      = evin1
# M      = evin2
# c      = evin3
#-----
#---->Declaration of variables
integer outo,out
real  pi,Tnin
#---->Initializations
genflg = .true.
if(lastim == -1) { out = 0 }
#---->Recalling previous value
if(lastim != simtim) { outo = out }
#---->Computing difference equations
evop1 = outo + 0.1*evin1 + nint(0.25*evin3*evin2)
out = evop1
.end

```

```

#elmod2 . accumulator 2
.define elmod2
.numout 1
.numinp 3
.*begin
#-----
#      ACCUMULATOR 2      #
# count2 = evop1           #
# count1 = evin1           #
# str    = evin2           #
# M      = evin3           #
#-----
#---->Declaration of variables
integer outo,out
#---->Initializations
genflg = .true.
if(lastim == -1) { out = 0 }
#---->Recalling previous value
if(lastim != simtim) { outo = out }
#---->Computing difference equations
evop1 = nint(outo + .4*evin1 + .3*evin3*evin2)
out = evop1
.end

```

```

#elmod3 . accumulator 3
.define elmod3
.numout 1
.numinp 3
.*begin
#-----
#      ACCUMULATOR 3      #
# count3 = evop1           #
# count2 = evin1           #
# str    = evin2           #
# M      = evin3           #
#-----
#---->Declaration of variables
integer outo,out
#---->Initializations
genflg = .true.
if(lastim == -1) { out = 0 }
#---->Recalling previous value
if(lastim != simtim) { outo = out }
#---->Computing difference equations
evop1 = nint(outo + 0.8*evin1 + 0.7*evin3*evin2)
out = evop1
.end

```

```

#elmod4 : comparator + delay
.define elmod4
.numout 1
.numinp 1
.*begin
#-----
#      ZERO COMPARATOR
# wave  = output waveform (0,1)
# stream = evop1
# count3 = evin1
#-----
#---->Declaration of variables
integer in,ino
#---->Initializations
genflg = .true.
if(lastim == -1){ open(unit=16,file="..\\matlab\\wave.dat") }
#---->Recalling previous value
if(lastim != simtim){
  ino = in
  write(16,*)wave}
#---->Zero comparator
in = evin1
if (ino >= 0){
  evop1 = -1
  wave = 1 }
else{
  evop1 = 1
  wave = 0 }
.end

```

```

splice
Third order Sigma-Delta Modulator
.model accu1    elmod: model=1
.model accu2    elmod: model=2
.model accu3    elmod: model=3
.model comp     elmod: model=4
.model src1 dc  : -777.0
.model src2 dc  : 2048.0

```

```

int1  count1,K str M    accu1
int2  count2,count1 str M  accu2
int3  count3,count2 str M  accu3
comp  str,count3        comp

```

```

K      K      src1
M      M      src2

```

```

time 1us 17384us
go
end

```

A.6 SPLICE Source Deck for 3rd Order Σ - Δ Modulator

APPENDIX B

SCALING OF THE PHASE ERROR SPECTRUM

The phase error power spectrum is obtained by performing a Discrete Fourier Transform (DFT) on the phase error waveform. The DFT maps the N values of the sampled waveform ($x(k)$) into N complex numbers ($X(n)$). For reasons of computational efficiency, the DFT was performed with a Fast Fourier Transform algorithm (FFT) [43]. If Δt denotes the sampling period of the waveform, $\Delta f = 1/\Delta t$ denotes the frequency resolution of the spectrum. Hence, the term $X(n)$ represents the amount of power present at a frequency $n \cdot \Delta f$. The relation between the time domain values and their frequency domain counterparts can be expressed as

$$X(n) = \sum_{k=0}^{N-1} x(k) \times e^{\frac{2\pi jkn}{N}} \quad (\text{B.1})$$

When temporal weighting, referred to as data windowing, is applied on the data before the actual computation of the FFT the expression of (B.1) becomes

$$X(n) = \sum_{k=0}^{N-1} w(k) \times x(k) \times e^{\frac{2\pi jkn}{N}} \quad (\text{B.2})$$

where the coefficient $w(k)$ are the weighting coefficients specific to the window used. In all the FFT computations performed throughout this thesis the Blackmann-Harris' minimum 4-term weight was used [44].

First consider a phase error waveform corresponding to a constant phase offset of 1 UI. The first term $X_1(0)$ computed with the windowed FFT is equal to

$$X_1(0) = \sum_{k=0}^{N-1} w(k) \quad (\text{B.3})$$

For $N=16384$, the value of $X_1(0)$, sum of all the window's coefficients was calculated and is equal to 5956.93.

Now that a correspondence has been established between value $X_1(0) = 5956.93$ and a phase error of 1 UI, the phase error spectrum can be scaled with respect to unit value of 1 UI = 0 dB by dividing all the terms $X(n)$ by $X_1(0)$. The result is that the whole power spectrum will be expressed in UI dB.

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Figure 4.19 Z-Domain Model for the Second Order Modulator