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“Low Temperature SF₆/O₂ ECR Plasma Etching for Polysilicon Gates”

Submitted by Imad Hasan in partial fulfillment of the requirements for the degree of
Master of Engineering

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September 2001

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Low Temperature SF₆/O₂ ECR Plasma Etching for Polysilicon Gates

By

Imad Hasan

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment
of the requirements for the degree of

Masters of Engineering

Department of Electronics

Carleton University

Ottawa, Ontario, Canada

September 2001

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ABSTRACT

In previous research SF_6 plasma etching at substrate temperatures near -130°C has been shown to provide a promising alternative to conventional chlorine or bromine plasma etching for polysilicon gate formation in deep submicron CMOS. This thesis examines the use of SF_6/O_2 chemistry for polysilicon gate etching at low temperature in an electron-cyclotron resonance (ECR) plasma etcher. The addition of oxygen to the plasma allows anisotropic etching to be obtained at higher temperatures than with pure SF_6 . Sidewall angle, polysilicon etch rate and selectivity to gate oxide and photoresist are reported as a function of temperature in the range -125 to $+25^\circ\text{C}$. Deep submicron gates defined by electron beam direct-write lithography were formed at -100°C with 3:1 selectivity to photoresist and 15:1 selectivity to oxide. Preliminary results on the application of low temperature SF_6/O_2 plasma etching to polycrystalline p+ SiGe alloy gates are also presented.

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List of Abbreviations

ECR.....	Electron Cyclotron resonance
RIE.....	Reactive Ion Etching
ICP.....	Inductively Coupled Plasma
CMOS.....	Complementary metal oxide semiconductor
EBL.....	Electron beam Lithography
VLSI.....	Very large Scale integrated circuit
ULSI.....	Ultra large Scale integrated circuit
ER.....	Etching Rate
SiGe.....	Silicon germanium
PR.....	Photo resist
SEM.....	Scanning Electron Microscope
PMMA.....	Polymethyl methacrylate
CD.....	Critical Dimension
SCE.....	Short channel effect
V_t.....	threshold voltage
eV.....	Electron volt
HDP.....	High Density Plasma

Chapter 1. Introduction

Formation of polysilicon gates for deep submicron CMOS technologies poses severe challenges in plasma etch processing. It is necessary to produce vertical walls in the polysilicon film with very high selectivity to the ultra-thin underlying gate oxide, and to precisely transfer features smaller than 200 nm from photoresist to polysilicon. Modern industry typically uses chlorine or bromine plasma etching at or near room temperature to solve these challenges [1-4]. Both chlorine and bromine can provide highly selective etching of polysilicon over oxide, and give extremely high etch anisotropy in reactive ion etch (RIE) or high density plasma (HDP) systems since the etch rate on sidewalls not exposed to ion bombardment is very low. However, there are problems with these conventional approaches to gate etching. The source gases used (typically Cl_2 or HBr) are highly toxic. Etch rates tend to be low. A breakthrough step may be required to remove native oxide and initiate the etch. Finally, both Cl and Br may form corrosive residues in vacuum systems.

Historically, fluorine plasmas were the first gas plasmas used for dry etching of polysilicon gates. Fluorine plasma gate etching was abandoned by most companies at approximately the 1 μm gate length generation due to the difficulty of obtaining anisotropic etching. Fluorine is so chemically reactive that it strongly attacks silicon even in the absence of ion bombardment, undercutting photomasks. Even an advanced fluorine etch process such as that using SF_6 as a source gas and O_2 as a source of sidewall passivant was unable to produce fully anisotropic gate etching suitable for submicron CMOS [11].

In pioneering studies in the late 1980's and early 1990's S. Tachi and co-workers at Hitachi Corporation showed that SF_6 plasma etching at wafer temperatures near -140°C could produce vertical-wall features in monocrystalline silicon with high selectivity to the photoresist [2-4]. Some preliminary results on the etching of polysilicon gates over oxide were also provided. Several other researchers have since applied cryogenic etching in SF_6 or SF_6/O_2 to the formation of deep trenches in silicon [5-6]. However, since the work of Tachi the technique has not been applied to the problem of polysilicon gate etching.

This thesis examines submicron polysilicon gate formation in SF_6/O_2 mixtures, as opposed to pure SF_6 . It is shown that anisotropic etching of polysilicon with good selectivity to photoresist and oxide can be achieved at -100°C with the addition of O_2 as a sidewall passivant.

Chapter 2 of this thesis expands on the review of previous research on low-temperature SF_6 silicon plasma etching provided above. Following a brief general overview of the subject of plasma etching of silicon, previous work on low-temperature SF_6 etching of deep trenches in silicon and on room-temperature SF_6/O_2 gate etching is reviewed. The advantages of polycrystalline p+ SiGe gates for deep submicron CMOS are also discussed (SF_6/O_2 etching of this material is considered as a secondary objective).

Chapter 3 is the core of the thesis, providing a detailed description of the etching system used, sample preparation, measurement techniques, and the results of experiments on polysilicon gate etching. Data on polysilicon etch rate, on etch selectivity to oxide and photoresist, and on sidewall profile are presented.

At the end of chapter 3 the extension of low-temperature SF_6/O_2 etching to p+ polycrystalline SiGe alloy gates is discussed. This intermediate work function gate material may find important application in deep submicron CMOS, particularly for fully depleted SOI technology. Some preliminary results on etch processes for SiGe alloy are presented here, but the work was hindered by the limitation that only very large grain size in the films could be deposited in the Carleton University microfabrication facility. Chapter 4 presents conclusions and recommendations for future work.

Chapter 2. Background

This chapter reviews current trends in the plasma etching of silicon and polysilicon in Sections 2.1-2.4. The work of S. Tachi *et al* on low-temperature etching is considered in detail in Section 2.5. The “black silicon” method for determining etching conditions is reviewed in Section 2.6. Finally, the motivation for using polycrystalline p+ SiGe alloy gates in deep submicron CMOS is considered in Section 2.7, and the means for forming these gates is reviewed.

2.1 Plasma Etching of Silicon: basic Principles

Polysilicon gate lengths are approaching 0.1 μm in commercial CMOS ULSI technologies, while gate film thickness cannot be reduced much below 0.25 μm . Simultaneously, gate oxide thickness is approaching 3 nm [39]. This places severe constraints on the plasma etch process used to form the gates. Etching must produce high-aspect ratio features with effectively vertical walls, and thus it must be almost completely anisotropic. At the same time the etch must have extremely high selectivity to the underlying ultra-thin gate oxide. High selectivity to photoresist is also required to minimize changes in printed gate dimensions during etching. Etching must be uniform over large areas (up to 200 mm diameter for state-of-the-art facilities), and etch-induced damage and contamination must be minimized. Plasma etch processes have advanced in step with CMOS minimum feature size reduction over the past two decades to meet these challenges.

The basic principles of plasma etching of semiconductors have been reviewed in textbooks by Plummer *et al* [1], van Roosmalen *et al* [2] and others. A typical plasma etch system is shown in Fig. 1. Wafers are placed in a vacuum system between two parallel plate electrodes typically driven by an RF power supply at 13.56 MHz. The chamber pressure is maintained at a level at which a plasma is generated in the region between the plates. Since electrons in the plasma have much higher mobility than the massive, positively charged ions, the electrons are at first preferentially removed from the plasma on each RF cycle. A steady-state condition is rapidly reached in which the plasma acquires a positive potential relative to the electrodes. The potential is typically higher at low system pressure, and is usually on the order of ten to a few hundred volts. A "dark space" or "ion sheath" depleted of electrons forms between the plasma and the electrodes. If the electrodes are asymmetric in size, then the smaller electrode will be at a more negative potential relative to the plasma than the larger electrode. Typically, the wafers are placed on the lower electrode in the system, and the top electrode is electrically connected to the chamber walls, increasing its effective area. In this way, relatively large D.C. potential differences can be established between the wafers and the plasma. Positive ions swept across the dark space will then strike the wafers with significant energy (roughly 10 to 500 eV). Systems, resembling Fig.1, operated at relatively low pressure with large potential differences between the plasma and the wafers have come to be termed "reactive ion etchers" or RIE systems. It will become apparent below that this name is very misleading, but it has become part of the terminology of semiconductor processing.

The source gases used in the etching of silicon and silicon dioxide invariably contain one or more of the halogens fluorine, chlorine and bromine. In the plasma the source gases dissociate to produce highly reactive neutral free radicals, including atomic halogens and in many cases other reactive molecular fragments. Plasma etching of silicon is believed to result almost entirely from chemical reaction with free radicals SiF_2 . The free radicals (S, F, O, SiF_2 , etc) are extremely reactive due to the presence of unpaired electrons (Note that etching is *not* caused by reactive ions such as O^+ , O^{++} , etc).

The central issue in practical dry etching is how to control bottom surface reaction and sidewall reaction independently during etching. The main chemical reactions in plasma etching are spontaneous etching and ion assisted reaction as shown in Fig. 2. The same radicals, e.g. fluorine atoms, are responsible for both reactions. The ion-assisted reaction occurs on the bottom surfaces. Energetic ions which impinge normally on the bottom surfaces enhance the etching reaction between adsorbed radicals and surface atoms [3].

Spontaneous etching takes place between long-lived radicals and sidewall atoms. Because of the random incidence of the fragmented radicals, this reaction occurs isotropically. The flux of the neutrals is dependent on gas pressure, input power density, gas species, discharge frequency, geometry, etc. [4]. The radical flux is at least two/ three orders of magnitudes higher than the ion flux [5]. Hence, highly anisotropic etching requires dramatic suppression of the spontaneous radical etching and sufficient enhancement of ion-assisted reaction. Concerning ion trajectories, oblique incidence is negligible at low gas pressure where the mean free path of ions exceeds the width of the dark space.

Tachi *et al* [6-8] carried out fundamental study of the rates of spontaneous and ion-assisted etching of Si under bombardment with low-energy beams of F, Cl and Br atoms in an ultra high vacuum environment at room temperature [6].

The ion energy dependences of the Si sputtering yields [7] indicate that the chlorine and bromine chemical sputtering yields fall sharply at ion energies below 500 eV. Hence, it is assumed that these species have a low reactivity with Si when the energy is low. Extremely small reaction probabilities are estimated for chlorine and bromine radicals, which have energies of approximately 0.05 eV in dry etching. Thus, sidewall etching is considered small with chlorine and bromine gas plasmas. By ion bombardment the bottom surface reactions with these radicals are enhanced. Tachi classified this variety of plasma etchants as of the “assisting” type [8].

Tachi *et al* [6-8] classified another group of etchants showing weak energy dependence of the sputtering yields as the “unprotecting” type. Atomic fluorine is of this type. Relatively high reaction probabilities are estimated for fluorine atom etching of Si, therefore, unwanted undercutting occurs with fluorine plasmas. To obtain anisotropic etching, an additive gas mixing technique is widely used to provide a sidewall-protecting film (Fig. 3). Often, a carbon-containing compound is added to the plasma to promote sidewall polymer deposition. The polymer protects the sidewall, but is removed from the bottom surface by ion bombardment.

For the assisting type of etch chemistry, anisotropic etching can be obtained without gas mixing. However, the etch rates and selectivities are low for these chemistries. This occurs because the chemical reactivities of these atoms are inherently low, and partly because the dissociation rate in the plasma is also low. On the other hand,

the unprotecting etch chemistries show high etching rates and high selectivities but poor (isotropic) etching profiles [8].

Fig 1. Schematic diagram of an RF-powered plasma etch system

Low temperature gas plasma

Fig.2 Surface reaction and gas phase reaction occurred in plasma-assisted etching

(After Tachi *et al* [23])

Fig 3 Illustration of ion- enhanced etching. In (a) the chemical etch reaction is enhanced by ion bombardment. In (b) an inhibitor is formed which is removed by ion bombardment, allowing chemical etching to proceed. In both cases, anisotropic etching results. (After Plummer *et al* [1])

2.2 Fluorine-Based Silicon Etching

The earliest plasma etch processes for silicon used atomic fluorine as an etchant. Atomic fluorine is extremely reactive, rapidly attacking both silicon and silicon dioxide. In consequence, it has proven very difficult to obtain anisotropic etching and vertical-walled profiles with fluorine chemistry. Early systems typically used CF_4 as a source of fluorine, with oxygen frequently added to react with CF_x radicals and improve selectivity to SiO_2 . Some degree of anisotropic etching could be achieved with this chemistry through the addition of hydrogen (or use of a hydrogen-rich source gas such as CHF_3) to form sidewall polymers. However, introduction of hydrogen removes atomic fluorine from the plasma through the formation of HF molecules, greatly reducing the silicon etch rate. Loss of silicon etch rate in turn reduces selectivity to silicon over silicon dioxide [1].

In the mid-1980's more sophisticated fluorine etch chemistry was introduced based on SF_6 as a source gas [9]. Like CF_4 , SF_6 is a very stable, low-toxicity source. Lacking carbon, SF_6 does not tend to produce polymers. Plasma etching of silicon in pure SF_6 at room temperature therefore tends to be isotropic. To obtain anisotropy with the etching, O_2 is typically added to the source gas stream. It has been shown that the addition of oxygen leads to sidewall passivation with oxyfluorides [10], making etching more anisotropic. However, it is generally agreed that room temperature SF_6/O_2 etching is not sufficiently anisotropic for the formation of deep submicron gates [11]. The best results for SF_6/O_2 gate etching reported to date are those of Zheng *et al* [12].

2.3 Chlorine and Bromine Based Silicon Etching

The difficulty with controlling the inherent isotropy of silicon etching in fluorine plasmas lead industry to consider the use of chlorine and bromine plasma etching. Following the terminology of Section 2.1, atomic chlorine and bromine etch silicon in an assisted type of reaction. Spontaneous etching of sidewalls protected from ion bombardment is therefore very slow. This can lead to highly anisotropic etching provided the mask is not eroded [2]. A small amount of O_2 is often added to chlorine plasmas to provide sidewall passivation and improve anisotropy still further [11]. Reaction of Cl and Br with SiO_2 is also extremely slow, in principle, giving extremely high selectivities to gate oxide. In practice, in the presence of carbon compounds volatilized from photoresist masks Cl etch selectivity to silicon over oxide may drop as low as 10:1.

On the basis of the above considerations, one might conclude that the use of chlorine or bromine chemistries had effectively solved all the problems of polysilicon gate etching for ULSI, and that there is no need to consider alternative approaches. However, the chlorine and bromine etch chemistries are not without drawbacks. The source gases required (typically Cl_2 and Br_2 or HBr) are extremely toxic. These gases are corrosive, and may attack vacuum system components [1]. The high selectivity to oxide usually requires a breakthrough step to remove native oxide and initiate etching. Finally, the use of assisting-type reactions gives a relatively low etch rate, reducing throughput and thereby increasing processing cost.

2.4 High Density Plasma Systems

The inherently low rates of chlorine and bromine plasma etching of polysilicon pose an economic wafer throughput problem for the semiconductor industry. To respond to this problem, techniques were sought to increase the density of reactive species in the plasma. In the basic RIE system of Fig. 1, increasing the input RF voltage and power increases the density of ions and electrons in the plasma, but it also increases the plasma potential relative to the wafers. This raises the average ion bombardment energy, which can cause etch-related damage and generally degrades selectivity. To provide independent control of ion bombardment parameters and plasma density, so-called *high-density plasma* (HDP) etchers have been introduced. Early HDP systems were based on electron cyclotron resonance plasma generation (ECR). A typical ECR system is shown schematically in Fig. 4. Microwave radiation (typically at 2.4 GHz) is used to generate a relatively intense plasma.

In this way, an unprotecting type of etch chemistry at room temperature can be converted to an assisting type of etch at low temperature. The electrons in the plasma are confined by an intense magnetic field, maximizing collisions with neutrals and therefore maximizing ionization. The microwave energy is fed in at the resonant frequency of the electrons orbiting in the magnetic field. Separate DC or 13.5 MHz RF bias is applied to the substrate holder, establishing a potential difference between the wafers and the plasma. The ECR approach is thus able to independently control the plasma density and the ion bombardment energy. The ECR system of Fig. 4 uses a large, cumbersome electromagnet to establish the magnetic field. It is extremely difficult to scale this type of system to large wafer diameters. For this reason second-generation ECR etchers used

distributed pockets of magnetic field created by permanent magnets, as shown schematically in Fig. 5. The etcher used in the experiments reported here is of the distributed ECR type. More recently Inductively Coupled Plasma (ICP) systems of the kind shown in Fig. 6 have become the most popular choice for HDP etchers, due to simpler construction than for ECR systems.

Fig. 4 Divergent beam ECR reactor with optional substrate bias.

(After Van Roosmalen *et al* [2])

Fig. 5 Section of a multiple microwave reactor with internal antennas.

(After Van Roosmalen *et al* [2])

Fig.6 Schematic diagram of Inductively Coupled Plasma (ICP)

2.5 Low Temperature Etching for Silicon Processing

In pioneering work in the late 1980's and early 1990's, S. Tachi *et al* [6-8], [17], and [23-25] explored the cryogenic cooling of substrates as a means of obtaining increased control in plasma etch processes. Tachi's experiments were based on the observation that the spontaneous chemical reaction with the sidewall often has a strong dependence on wafer temperature, and can be suppressed by lowering the temperature. In this way, an unprotecting type of etch chemistry at room temperature can be converted to an assisting type of etcher at low temperature.

The models for ion-assisted reaction are (i) the ion induced damage layer etching model [13], (ii) the ion assisted evaporation model [14], and (iii) the ion assisted reaction excitation model [15]. Among these models, the damage model predicts a spontaneous reaction and therefore is temperature dependent. The same is true for the evaporation model since the reaction of the radicals with the surface atoms takes place before ion bombardment. For the last model, the reaction takes place under an excited condition caused by ion collision. Consequently, the probability does not depend on the wafer temperature. Therefore, with ion bombardment, the etch rate as a function of the wafer temperature should remain constant. This type of ion-assisted reaction is desired for low temperature etching.

Tachi *et al* [6-8] constructed an ECR system in which wafers could be cooled to temperatures as low as -140 °C during etching. Cooling of wafers in a vacuum system presents a difficult technical challenge since wafers are usually slightly bowed and they contact the chuck only at their edges. During etching wafers are heated by ion

bombardment from the plasma and possibly also by heat released in the etching chemical reaction. The wafer temperature will rise far above that of the chuck, even if the chuck is cooled, unless a means to improve heat conduction is provided. In the system of Tachi *et al.* the wafer is clamped to the chuck, and a flow of cooled helium gas is provided across the wafer backside. The temperature of both the wafer and the chuck were monitored with thermocouples. In this way it was shown that the wafer temperature was held within 5 °C of the chuck temperature during etching. Fig. 10.

Tachi *et al* [23] provided data on the temperature dependence of sidewall profile, etch rate and selectivity to photoresist for etching of trenches in monocrystalline silicon using pure SF₆ as a source gas. A narrow range of conditions was found in which anisotropic etching could be obtained in pure SF₆ (Fig. 7). At a pressure of 5 mTorr, anisotropic etching was found at temperatures of approximately -120 °C and below. At 10 mTorr pressure, the maximum temperature for anisotropic etching decreased to approximately -130 °C. These temperatures are very close to the reported temperature for SF₆ condensation in this system, -140 °C, at which etching ceases. Excellent selectivity to photoresist was obtained at these temperatures. Silicon etch rates were as high as 1 µm/min. Although anisotropic etching using fluorine chemistry without a sidewall passivant was demonstrated for the first time, the process window in which this result could be achieved was extremely narrow. Tachi *et al* [25] also, very briefly, considered the application of low-temperature SF₆ etching to polysilicon gate formation. SEM images showing anisotropic gate profiles obtained at -130 °C were presented, but no data on selectivity to oxide was given.

Since the early work of Tachi *et al* [25], low-temperature SF_6 and SF_6/O_2 etching has seen fairly widespread use for the formation of deep trench structures for micromachining and photonics. However, application to gate etching has been ignored.

This thesis extends the work of Tachi *et al* [6.7.8.17.23.25] by investigating low temperature etching of polysilicon gates in SF_6/O_2 mixtures. The additional of O_2 as a sidewall passivant means that anisotropic etching can be carried out at a considerably higher temperature than with pure SF_6 . This widens the window of allowable process parameters, increases throughput, and may reduce system complexity.

Fig.7 Anisotropy ratio for silicon etching in SF₆ as a function of pressure and wafer temperature. (After Tachi *et al* [23])

2.6 The “Black Silicon” Technique

A convenient way to find the processing conditions needed for a vertical wall is the black silicon method [26]. In this method, it is assumed that SF_6 and O_2 are present in the system. There is a constant competition between the fluorine radicals that etch and the oxygen radicals that passivate the silicon. At certain oxygen content there is such a balance between the etching and the passivation that nearly vertical walls result. At the same moment native oxide, dust, etc. will act as micro masks and because of the directional etching, spikes will appear. These spikes consist of a silicon body with a thin passivating siliconoxyfluoride skin. They will become higher in time and, depending on the etch rate, they will exceed the wavelength of incoming light after some time. This light will be trapped in the areas between the spikes, which cause elimination in the reflection. The silicon surface then appears black.

Fig 8. Black silicon formation.

2.7 Polycrystalline SiGe Gates for Submicron CMOS

In recent years, the continuing miniaturization of Si MOS transistors for increased chip-packing density and performance has resulted in significant research efforts in suppression of the so-called “short-channel effects” (SCE’s). The SCE’s are caused by an increased influence of the drain potential on the source depletion region in short devices. These effects are usually tackled by raising the substrate doping level to reduce the lateral extension of the drain depletion region. This, however, can result in significant deterioration of performance of the transistors: the reduced carrier mobility in a heavily doped region results in a decreased current drivability (I_{DS} or I_{on}) of the devices, while the subthreshold voltage swing is increased, resulting in higher levels of off-state leakage currents (I_{off}). A partial solution can be achieved by using vertical doping redistribution to reduce it in the channel region only (“super-steep retrograde” (SSR), or “ground plane” channel designs) [27]. Unfortunately, the removal of the dopants from the interface regions results in unacceptably high off-state leakage, because of the low threshold voltage (V_T) values in this case. King *et al* [27] demonstrates that a complete solution can be achieved by a combination of the channel doping profiling with change in the gate workfunction. The threshold voltage is set by the chosen gate to semiconductor workfunction difference while the channel profile is engineered to control SCE and to obtain desired I_{on} / I_{off} ratio.

Heavily doped n- and p-type polycrystalline Si films (poly-Si), that are conventionally used in modern CMOS technologies as gate materials, have a fixed gate to semiconductor workfunction difference (ϕ_{MS}), determined by the electron affinity and the band gap of the materials. It is well known, however, that the polycrystalline silicon

germanium alloy films (poly-SiGe) have good compatibility with standard CMOS processing. The dopant activation in poly-SiGe is comparable to poly-Si, and is actually better for p-type material. In the p-type SiGe alloy, the workfunction decreases with increasing Ge mole fraction [27-33]. Poly-SiGe is therefore a promising material for p-type gate workfunction engineering. The workfunction change originates in band gap reduction caused mainly by the increase of the effective SiGe lattice constant with an increase in the Ge percentage. For high Ge concentrations it has also been reported [35] that a significant amount of stress in the poly-SiGe grains results in an extra reduction of the poly-SiGe gate workfunction.

A complete compatibility to standard CMOS processing is demonstrated when polycrystalline Si is substituted with SiGe (for Ge fractions below 0.5) to form the gate electrode of the transistors [34]. Performance improvements are achieved for PMOS transistors by careful optimization of transistor channel profile and p-type gate workfunction, the latter by changing Ge mole fraction in the gate. For the 0.18 μm CMOS generation up to 20% increase in the current drive, a 10% increase in the channel transconductance and subthreshold swing improvement from 82 mV/dec to 75 mV/dec resulting in excellent “on”/“off” currents ratio has been recorded in PMOS transistors. At the same time, NMOS transistor performance is not affected by gate material substitution.

In conventional dual gate CMOS technology, boron diffusion through ultra thin gate oxides along with poly-depletion effects are critical issues [35]. In addition, it is difficult to control the threshold voltage (V_t) due to the lateral diffusion of dopants in the connected P⁺/N⁺ silicided gates. Therefore, using a single gate material for both surface p⁺ and n⁺ channel devices is highly desirable. Mid-gap metal gates [36] and adjustable

workfunction poly-Si_{1-x}Ge_x gates [37-38] are two potential solutions. The application of P⁺ poly-Si_{1-x}Ge_x as the gate material eliminates the need for dual doped poly-Si gates and permits adjustment of the V_t through change of the Si/Ge mole fraction. Single gate 0.15 μm CMOS devices have been successfully fabricated using in-situ boron doped polycrystalline Si_{1-x}Ge_x (poly Si_{1-x}Ge_x) as gate material for both surface channel n⁺ and p⁺ MOSFETs.

Introduction of P⁺ SiGe alloy gates in CMOS technology will require the development of appropriate gate plasma etch processes. In this thesis preliminary work on low temperature SF₆/O₂ plasma etching of P⁺ SiGe gates is reported.

Chapter 3. Experimental Procedure

3.1 Equipment

In this chapter we will present the equipment used for etching poly-silicon gates. In addition to the equipment we will cover the wafer preparation technique that has been used to determine the etching rate for the PR, SiO₂, and polysilicon in addition to the wall profile.

The design of our Electron Cyclotron Resonance system (ECR) is much like a down stream reactor with the addition of an applied magnetic field and separate power supply to bias the wafer. This system creates a high-density plasma in which larger percent of gas molecules are ionized than in conventional RIE systems. ECR takes the concept of magnetic field confinement by feeding microwave energy in to the plasma at resonance frequency of electrons in the magnetic field. Usually microwave frequency is 2.45 GHz. This power allows for more efficient transfer of energy to the plasma, and hence a higher ionization frequency. The strength of magnetic field is chosen in order to induce the electrons to move in a spiral or rotating pattern. This enhances the collisional frequency of the electrons in the plasma. The process can then be operated at much lower pressures. A separate RF power supply is used to provide a bias to the wafer in order to attract the ions for ion bombardment.

Low- temperature microwave plasma etching was carried out using a modified Plasma Therm SLR-772 ECR etcher in the temperature range -125 to +25 °C using a custom temperature control system that consists of a Watlow series 945 temperature controller, a Toshiba series EX100 programmable controller, a liquid nitrogen control

and delivery system, an electrode structure with a cooling channel and four electrical heating elements, and a helium gas wafer backside cooling system. The wafer was clamped to an electrode cooled with liquid nitrogen, then the back of the wafer was cooled with He gas. This He gas had been cooled in advance by the liquid nitrogen. The chuck temperature was monitored with a thermocouple. During the etching, it was not possible to monitor the wafer temperature directly because the system does not have a thermocouple attached to the wafer. Other groups who have made measurements with similar systems estimate a 5 °C difference in the temperature between the chuck and the wafer. A similar temperature difference between wafer and chuck is expected here. Mass spectroscopy has been used to determine the end point for etching the polysilicon in the ECR.

Fig.9 A schematic cross-section of a typical ECR etching source. Two electromagnets provide a divergent axial magnetic field 1000gauss near the microwave (2.45 GHz) window. Another magnet arrangement near the substrate permits magnetic field collimation. The substrate is sometimes biased with respect to the plasma using the 13.56 MHz RF generator. (After Oehrlein [40])

Fig .10 A schematic cross-section of the wafer cooling system

3.2 Black Silicon Method

Values of ECR microwave source power, total system pressure, gas flow, and DC bias applied to the wafers common to all experiments described here are listed in Table 1. Microwave power levels below 200 W were found to give unstable plasmas, while at power levels above 300W tuning became extremely difficult. The total pressure was held close to the minimum required to produce a stable plasma, and is similar to that used by Tachi *et al.* The low system pressure maximizes ion free path, which assists anisotropic etching.

The “Black Silicon” discussed in section 2 was used in preliminary experiments to establish approximate processing conditions for anisotropic etching. In general, different materials require slightly different gas mix for anisotropic etching, but for silicon, polysilicon and amorphous silicon, oxygen of around 50% seems to give good results (high selectivity and anisotropic etching).

Blank silicon wafers were etched for 10 minutes at -100°C with various SF_6/O_2 ratios. (Table 2 relates the O_2 percentage to the actual gas flows used). After etching, wafers were examined by eye and in SEM. Results are summarized in Table 3. An SEM image of an example of "black silicon" is shown in Fig.10-1

Fig 10-1 SEM image of an example of "black silicon"

Microwave power	270 W
DC bias	10 V
Total pressure	6 mTorr
Total gas flow	5.5 sccm

Table 1 Basic ECR system Parameters used in all experiments

Total sccm	SF₆ sccm	O₂ sccm	O₂ %
5.56	5.56	0	0
5.56	5.45	0.11	2
5.56	5.34	0.22	4
5.56	5.23	0.33	6
5.56	5.12	0.44	8
5.56	5	0.56	10
5.56	4.89	0.67	12
5.56	4.78	0.78	14
5.56	4.67	0.89	16
5.56	4.56	1	18
5.56	4.45	1.11	20
5.56	4.34	1.22	22
5.56	4.23	1.33	24
5.56	4.11	1.45	26
5.56	4	1.56	28
5.56	3.89	1.67	30
5.56	3.78	1.78	32
5.56	3.67	1.89	34
5.56	3.56	2	36
5.56	3.45	2.11	38
5.56	3.34	2.22	40
5.56	3.22	2.34	42
5.56	3.11	2.45	44
5.56	3	2.56	46
5.56	2.89	2.67	48
5.56	2.78	2.78	50
5.56	2.67	2.89	52
5.56	2.56	3	54
5.56	2.45	3.11	56
5.56	2.34	3.22	58
5.56	2.22	3.34	60

Table 2. SF₆ and O₂ gas flows used to obtain various O₂ concentrations

Parameters were set as follows:

Microwave power Watt	Dc Bias volt	TEMP (°C)	PRESSURE (mT)	O2 Flow %	Comment
270	10	-100	6	10	No change
270	10	-100	6	15	No change
270	10	-100	6	20	No change
270	10	-100	6	25	No change
270	10	-100	6	30	No change
270	10	-100	6	35	No change
270	10	-100	6	40	Slight haze on one side of wafer
270	10	-100	6	44	Haze covers 1/3 of wafer
270	10	-100	6	46	Haze covers most of wafer, one side turning darker (~brown)
270	10	-100	6	48	Entire wafer dark (~Brown)
270	10	-100	6	50	Entire wafer black

Table 3. Results of “black silicon” experiments: wafer appearance as a function of O₂ content in plasma.

On the basis of these experiments, it was concluded that a temperature of -100 °C and O₂ concentration of 46% was a good starting point for experiments on anisotropic etching.

3.3 Substrate preparation

A 100 nm thermal gate oxide was grown on blank lightly-doped silicon wafers at 1100 °C in dry oxygen. A 0.25 µm thick layer of undoped polysilicon was then deposited on the wafers by low-pressure chemical vapour deposition at 627 °C.

The HPR504 photoresist was then applied to the wafers and patterned using a mask, which exposed one quadrant. Polysilicon was etched from this quadrant in hydrofluoric acid/ nitric acid solution to expose the underlying oxide. The photoresist was then stripped, and a new layer of HPR504 re-applied. This second photoresist layer was patterned with a “lines and spaces” mask having a line width of 32 µm and spacing of 44 µm (Fig. 11). The wafers were next subjected to an oxygen plasma “descum” step in a Technics Planar Etch II planar plasma etcher at 0.3 Torr pressure and 100W RF power for 1 minute. The descum step serves to remove any thin residual photoresist film left on the wafer surface after developing which might interfere with initiation of the etch.

The height of the photoresist step on the wafers was measured prior to etching using a DekTak IIA surface profilometer. The evolution of the pattern during etching is illustrated in Fig. 12. After etching the height of the combined photoresist and oxide step in region 2 was measured with the Dektak. The photoresist was then stripped in hot sulfuric acid/hydrogen peroxide solution, and the height of the features etched in the polysilicon and oxide in regions 1 and 2 respectively measured. From the measured polysilicon step height in region 1 and oxide step height in region 2, the polysilicon and oxide etch rates could be determined. By taking the difference in photoresist step height

before and after etching in region 2. and compensating for the relatively small amount of underlying oxide etched. the photoresist erosion rate could be determined.

Polysilicon sidewall angle was measured by cleaving etched samples after stripping photoresist and viewing the samples edge-on in the scanning electron microscope. The relative large length and spacing of the polysilicon lines makes it easy to determine the step.

Fig. 11 Mask used for polysilicon etch experiment

Fig .12 Cross section of test wafers at various stages in the etch process.

3.4 The effect of the temperature on the Etching rate, Selectivity, and wall profile of the poly gate:

Once initial conditions for anisotropic etching had been established using the “black silicon” technique, polysilicon etch rate, anisotropy, and selectivity to oxide and photoresist were studied as a function of wafer temperature in the range of -125 to $+25$ °C. Results are summarized below.

Trial 1: T= 25 °C

The parameters that were used in this trial are specified in table 4 below:

Power W	DC Bias V	Pressure mTorr	O ₂ sccm	SiF ₄ sccm	O ₂ +	Temperature °C
270	10	6	2.56	3.00	46	25

Table 4. Trial 1 system parameters.

End point was reached after etching for 2.0 minutes.

A cross-section SEM of the gate sidewall is shown in Fig.13. The sidewall shows a significant slope, indicating that the etch has a major isotropic component

The etching rate (ER) for Polysilicon, SiO₂, and PR is given in Table 5 below.

Polysilicon ER nm/min	SiO ₂ ER nm/min	PR ER nm/min
113.3	~8.7	46.4

Table 5. Etch rate (ER) for Polysilicon, SiO₂, and PR at 25 °C

The Selectivity for poly and SiO₂ was ~13:1 and for poly and PR ~ 2:1.

The sidewall shows a significant slope, indicating that the etch has a major isotropic component.

Fig .13 Polysilicon etching profile at +25 °C and 46% O₂

Trial 2: -65 °C

The parameters that were used in this trial are given in the table 6 below:

Power W	DC Bias V	Pressure mTorr	O ₂ sccm	SiF ₄ sccm	O ₂ , sccm	Temperature °C
270	10	6	2.56	3.00	46	-65

Table 6. Trial 2 system parameters.

End point was reached after etching for 2.1 minutes. Etch rates are given in Table 7 below.

A cross- section SEM image of the gate sidewall is shown in Fig 14. The sidewall is still strongly sloped, indicating the anisotropic etching has not been achieved.

Polysilicon ER nm/min	SiO ₂ ER nm/min	PR ER nm/min
110	~8.4	36

Table 7. Etch rate (ER) for Polysilicon, SiO₂, and PR at -65 °C

Selectivity improved slightly for lower temperature. For poly:oxide, it was 13 and for poly and PR ~ 3:1.

Fig .14 Polysilicon etching profile at -65 °C and 46% O₂

Trial 3: T= -100°C

The parameters that were used in this trial are specified in table 8:

Power W	DC Bias V	Pressure mTorr	O ₂ sccm	SiF ₄ sccm	O ₂ %	Temperature °C
270	10	6	2.56	3.00	46	-100

Table 8. Trial 3 system parameters.

Endpoint was reached after etching for 2.1 minutes. Fig 15 shows SEM images of the gate sidewall profile. It is apparent that effectively anisotropic etching has been achieved at this lower temperature, giving a vertical sidewall. The Etching rate for the various layers is given in Table 9:

Polysilicon ER nm/min	SiO ₂ ER nm/min	PR ER nm/min
109.5	~7.8	38.0

Table 9. Etch rate for Polysilicon, SiO₂, and PR at -100 °C

The etching time was 2.12 min, which is presented the time to endpoint

The selectivity for poly and SiO₂ was ~14:1, and for poly and PR ~ 3:1

Fig .15 Polysilicon etching profile at -100 °C and 46% O₂

Trial 4: T= -125 °C

The parameters that were used in this trial are specified in table 10:

Power W	DC Bias V	Pressure mTorr	O ₂ sccm	SiF ₄ sccm	O ₂ sccm	Temperature °C
270	10	6	2.56	3.00	46	-125

Table 10. Trial 4 etching parameters

Endpoint was reached after etching for 2.1 minutes.

Fig 16 shows a cross-sectional SEM image of the sidewall profile. The sidewall is once again effectively vertical, indicating that the etching is anisotropic

The Etching Rate (ER) for Polysilicon , Si O₂, and PR is represented in this table :

Polysilicon ER nm/min	SiO ₂ ER nm/min	PR ER nm/min
110.4	~7.3	36

Table 11. Represents the ER for Polysilicon, SiO₂, and PR at -125 °C

The selectivity for poly and SiO₂ was ~15: 1 and for poly and PR ~ 3:1

Fig 16 Polysilicon etching profile at -125°C and 46% O_2

The dependence of the etch rates for polysilicon, oxide and photoresist, the etch selectivity for polysilicon to oxide and photoresist, and gate sidewall angle on temperature are summarized in Figs. 18-22. The steps etched in the gate oxide are at the limit of the measurable range of the DekTak IIA, so the oxide etch rate data has a fairly large uncertainty. Surprisingly, the etch rates for all these materials are relatively insensitive to temperature. The etch rates for polysilicon and photoresist decrease slightly with decreasing temperature. This can be explained by a suppression of spontaneous reaction with free radicals (as opposed to ion-assisted reaction) at low temperatures. Working with SF_6 plasmas under similar conditions, Tachi *et al* [17] also found relatively little dependence of silicon etch rate on temperature. However, the data presented in [17] indicate far lower photoresist erosion rates than found here, with a far stronger dependence on temperature. Presumably the addition of oxygen to the plasma

leads to rapid attack on the organic photoresist. The only parameter which does vary strongly with temperature is the gate sidewall angle. Fig. 22 shows that anisotropic etching (giving vertical sidewalls) is only possible at temperatures near or below -100°C . The addition of oxygen to the plasma allows anisotropic etching to be obtained at considerably higher temperature than is possible with pure SF_6 (-100°C as opposed to -130°C). This is a major advantage for etcher design and operation, since it is much easier to build a system that will cool wafers to -100°C than to -130°C , the time required for cooling is shorter, and liquid nitrogen costs are lower. The price paid for achieving anisotropic etching at higher temperature is increased photoresist erosion rate. It should be noted that although anisotropic etching in SF_6/O_2 was obtained at -125°C with the PlasmaTherm system, there is no advantage in operating at -125°C as opposed to -100°C . Cooling wafers to -125°C requires more time and consumes more liquid nitrogen.

Fig 17 Temperature Vs Selectivity of polysilicon to SiO_2 at 46% O_2

Fig 18 Temperature Vs Selectivity of polysilicon to PR at 46% O₂

Fig 19 Polysilicon ER vs. Temperature at 46% O₂

Photoresist Etch Rate Vs. Temperature

Fig 20 Photoresist etch rate vs. Temperature at 46% O₂

SiO₂ Etch Rate Vs. Temperature

Fig 21 SiO₂ etch vs. Temperature at 46% O₂

Fig 22 Temperature Vs of Side wall angle of the polysilicon etching at 46% O₂

3.5 Electron Beam Lithography

Once an optimum process for forming vertical polysilicon gate sidewalls had been established, the process was applied to produce actual submicron gates. Electron beam direct-write lithography was used for this task. An array of gate lines of 100 nm width and lengths ranging from 0.1 μm to 1 μm was written in Shipley SAL-601, a novolac electron beam resist. The resist was exposed using a JEOL-840 scanning electron microscope with beam control provided by National Pattern Generation System (NPGS) software running on an IBM PC. The electron beam current was 10 pA, and doses ranging from 15 to 25 $\mu\text{C}/\text{cm}^2$ were used. After exposure the patterns were developed in CD-26 developer for 3.3 minutes, and examined in the SEM. The smallest line length after development obtained was 0.6 μm . The polysilicon was then etched to endpoint in the PlasmaTherm etcher at -100 $^{\circ}\text{C}$ with 46% O_2 content. The etch time was ~3.4 minutes. After etching the resist was stripped and the samples again examined in the SEM (Fig. 24). The shortest gate surviving after etch was 0.4 μm long. Shorter gates were not resolved in the etch process. This relatively poor resolution was in part the result of the JEOL-840 SEM being out of calibration at the time of the experiment. The very wavy line pattern apparent in the right hand image in Fig. 24 is a symptom of this poor calibration. The SEM was recalibrated by JEOL shortly after the experiments described here. With the SEM in proper calibration, gate lengths shorter than 0.3 μm were resolved by other researchers using the etch process reported here. An example is shown in Fig 25.

Fig. 23 Shows a block diagram of our electron beam lithography tool.

Fig 24. Submicron gate lines after etching. The dimension mark in the left hand image is 10 μm . in the right 0.1 μm (see Table 12).

The dimension marks can be explained as the following:

Mark	Bar length
One wide	0.1 μm
None	1 μm
One short	10 μm
Two short	100 μm
Three short	1000 μm

Table 12. Represent the dimension marks for the references in the software, which is responsible for capturing the images.

Fig 25 0.3 μm long polysilicon gate defined by SF_6/O_2 etching

3.6.1 Etching SiGe Alloy Gates:

The advantages provided by intermediate work function p+ SiGe alloy gates for deep submicron CMOS were discussed in section 2.7. Once a process for etching submicron polysilicon gates had been developed, an attempt was made to extend this process to polycrystalline p+ SiGe gates. The gate layers for this experiment were formed by rapid thermal chemical vapor deposition (RTCVD) in an AET thermal RTX system shown schematically in Fig 27. This is a single wafer system in which the deposition substrate is heated with a bank of tungsten-halogen lamps. The wafer is enclosed in an evacuated quartz process chamber through which controlled flows of SiH_4 , GeH_4 and B_2H_6 can be maintained. The substrate temperature is measured with a pyrometer which is exposed to the rough back surface of the wafer. A microcomputer controls lamp power to maintain a preset temperature during processing, and also controls the gas flows and system pressure through a throttle valve on the vacuum pump.

For the experiments described here, 100 nm thick thermal oxides were once again grown on 100 mm diameter silicon wafers. On the basis of many earlier experiments conducted in this laboratory to produce device-quality p+ SiGe layers with intermediate work functions [41], the deposition parameters given in Table 13 below were used.

SiH_4 Flow	GeH_4/H_2 Flow scm	$\text{B}_2\text{H}_6/\text{H}_2$ Flow scm	Pressure Torr	Temperature °C
------------------------	---------------------------------------	---	------------------	-------------------

sccm				
4	400 (1.2% GeH ₄ in H ₂)	258(50 ppm B ₂ H ₆ in H ₂)	5	665

Table 13 SiGe Film Deposition Parameters

The deposition time was 500 seconds, giving a film thickness of approximately 250 nm. Following the etch process for polysilicon gates, the oxygen concentration was fixed at 46%, while other parameters were the same as in Table 1. Two trials were carried out at different substrate temperatures. As in the case of etching pure polysilicon gates, endpoint was determined by a rapid drop in the mass spectrometer output at mass 85, corresponding to SiF₃. Results are given below.

Trial 1 : T= -100° C

The parameters that were using in this trial are specified in this table:

Power W	DC Bias V	Pressure mTorr	O ₂ sccm	SiF ₆ sccm	O ₂ %	Temperature °C
270	10	6	2.56	3.00	46	-100

Table 13-1. Etching parameters for SiGe trial 1

Endpoint was reached after etching for 3.34 minutes

The Etching Rate (ER) for SiGe, SiO₂, and PR is given in table 14:

SiGe ER nm/min	SiO ₂ ER nm/min	PR ER nm/min
35.8	~8.4	38

Table 14. Represents the ER for SiGe, SiO₂, and PR at -100 °C

Selectivity for SiGe to oxide was ~4:1 and for SiGe to PR ~ 1:1

Trial 2: T= -125 °C

The parameters that were using in this trial are specified in table 15 below:

Power W	DC Bias V	Pressure mTorr	O ₂ sccm	SiF ₄ sccm	O ₂ %	Temperature °C
270	10	6	2.56	3.00	46	-125

Table 15. Etching parameters for SiGe trial 2

The Etching Rate (ER) for SiGe, SiO₂, and PR at -125 °C is represented in this table:

SiGe ER nm/min	SiO ₂ ER nm/min	PR ER nm/min
35.0	~7.3	38.5

Table 16. Represents the ER for SiGe, SiO₂, and PR at -100 °C
Selectivity for SiGe to oxide was ~4:1 and for SiGe to PR ~ 1:1

Fig. 27 shows SEM images of the gate edge after etching. The very large grain size and "islanding" of the polycrystalline SiGe is apparent in these images. With such a large grain SiGe, it is not possible to obtain accurate information regarding the gate sidewall profile.

Before vertical-walled, submicron SiGe gate can be defined, it will be necessary to produce SiGe films with smaller grain size. This will require the use of a lower deposition temperature. Unfortunately, lower deposition temperatures can not readily be reached with AET thermal system, which uses pyrometry for temperature control. It should be noted that the etch rate of P⁺ SiGe is approximately three times lower than the undoped polysilicon under the same etch conditions. In consequence, the etch selectivity for SiGe over oxide and SiGe over photoresist is relatively poor. The low etch rate of the SiGe films is probably the results of the high boron concentration.

(c)

(d)

(e)

(f)

Fig 27 (a. b. c. d. e. f) represents surface morphology of SiGe for two different etch temperatures and they look grainy.

Fig 27 Schematic of Rapid Thermal Low Pressure

Chapter 4. Conclusion

It has been found that anisotropic polysilicon gate etching with reasonably good selectivity to SiO_2 and photoresist can be obtained using SF_6/O_2 chemistry in an ECR system with cryogenic substrate cooling. In all experiments, microwave power levels were held at 270 W since power levels below 200 W were found to give unstable plasmas, while above 300 W tuning became extremely difficult. The total pressure was held at 6 mTorr, close to the minimum required to produce a stable plasma. The "black silicon" method was found to be very effective in identifying a starting point for anisotropic etch experiments. The method was applied by fixing the substrate temperature and increasing the O_2 content in the chamber atmosphere. Once a suitable initial condition for anisotropic etching had been found, experiments with polysilicon gate etching over oxide were completed. Etching was carried out on samples with 0.25 μm thick polysilicon films using a photoresist mask as described in Chapter 3. Samples were etched until endpoint, determined using a mass spectrometer sampling the reaction chamber gases. The effect of substrate temperature in the range -125 to $+25$ $^\circ\text{C}$ on etch rates and profile was measured. Polysilicon etch rate and etch selectivity for polysilicon relative to oxide and photoresist were determined. Using cross-sectional scanning electron microscopy, the angle of the gate sidewall was measured. Effectively vertical gate sidewalls were obtained at -100 $^\circ\text{C}$, but not at higher temperatures. The polysilicon etch rate at -100 $^\circ\text{C}$ was 110 nm/min, and the selectivity to oxide and photoresist 14:1 and 3:1 respectively. No advantage was found for operation at temperatures below -100 $^\circ\text{C}$. There is no incentive to operate at lower temperatures, since longer cycle times are required to initially cool the wafer and this extra time reduces system throughput, and

consumption of liquid nitrogen required to cool the chuck rises sharply. Rather surprisingly, the polysilicon etch rate was found to increase only slightly with increasing temperature, while selectivity to oxide and photoresist decreased very slightly at higher temperatures.

Once an appropriate etch process had been worked out, the process was applied to produce deep submicron gates. Gates were defined by direct-write electron beam lithography in a SAL601 resist using a modified scanning electron microscope. An array of gates with lengths ranging from 0.1 to 1 μm was written. After etching, the photoresist was stripped and the array examined using the SEM. The shortest gate line resolved in this experiment was 0.4 μm . It is believed that shorter gates could not be resolved in part because of photoresist erosion during etching, and in part because the e-beam lithography system was out of calibration at the time this experiment was carried out. After the work described here was completed, the SEM system was cleaned and recalibrated by the manufacturer. With the system in better calibration, another researcher used the etch procedure reported here to form vertical-walled gates shorter than 0.3 μm .

A preliminary attempt was made to extend the etch process developed for polysilicon gates to P^+ SiGe alloy gates. The motivation for incorporating intermediate work function p^+ SiGe gates in a CMOS technology was explained in Chapter 2. Here p^+ SiGe gate layers were deposited over thermal oxide by rapid thermal chemical vapour deposition and then etched using the procedures developed for polysilicon gates. Etch rates for p^+ SiGe layers were found to be roughly three times slower than for undoped

polysilicon. The reduced etch rates are likely the result of the high boron content. Heavy boron doping is well known to reduce the chemical reactivity of silicon in many situations. The reduced etch rate for the gate translated to proportionately lower selectivities with respect to oxide and photoresist. The extremely large grain size in the RTCVD SiGe films made it impossible to draw any firm conclusions regarding etch anisotropy and gate sidewall angle. By modifying the RTCVD system to allow a lower deposition temperature, it should be possible to produce fine-grain films more suitable for application in MOSFET gates.

4.1 Suggestions for Future Work

Low temperature SF_6/O_2 plasma etching shows considerable promise for deep submicron gate formation, and there are many possibilities for future work. In the experiments described here, bias of 10 V was maintained between the substrate and the plasma. A feedback system adjusts the power level of a 13.56 MHz RF generator applied to the substrate to maintain this bias. It would be of interest to directly vary the RF generator power level and observe the effect on etch rates, selectivity and sidewall profile. The effect of chamber pressure and microwave power level could be investigated, but the range over which these parameters can be varied while still producing a stable plasma is limited. Once the SiGe deposition process has been refined to produce fine-grained material, development of the etch process for submicron SiGe alloy gates should be completed.

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