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**A Switched-Capacitor Circuit Technique
Used to Measure Capacitor Mismatch and
Explore Capacitor and Opamp Nonlinearity**

by

Bill Bereza, B. Eng.

**This thesis is submitted to the
Faculty of Graduate Studies and Research
in partial fulfillment of the requirements
for the degree of**

Master of Engineering

**Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Carleton University
Ottawa, Ontario
Canada
December 1988**

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Explore Capacitor and Opamp Nonlinearity"**

submitted by Bill Bereza in partial fulfillment of the requirements for the degree of Master of Engineering.

Prof. M.A. Copeland
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December 1988

ABSTRACT

In this thesis, a novel switched-capacitor circuit technique is employed to measure mismatch among small capacitors. These smaller capacitors are typical of those used in switched-capacitor filters to allow increases in analog circuit speed in addition to an overall reduction in chip area. However, the accuracy of switched-capacitor filters and the precision of stringent circuit designs is in question due to the inherently poorer matching performance of smaller capacitors.

In addition, this circuit technique is used to explore capacitor and opamp nonlinearity as they are also considered to be a significant source of error.

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LIST OF SYMBOLS

a_i	Coefficients of a Power Series Expansion (Polynomial)
α_i	Voltage Coefficients of Capacitance
A/P	Area-to-Perimeter Ratio
ADC	Analog-to-Digital Converter
C	Capacitor
CMOS	Complementary Metal-Oxide-Semiconductor
CS	Common Source
D(i,j)	Acquired Data Matrix
DAC	Digital-to-Analog Converter
dB	Decibal
dc	Direct Current
ϵ	Mismatch Error of a Capacitor
fF	Femtofarad (10^{-15} F)
G	Gain
γ_i	Linear Voltage Coefficient of Capacitance
HD(2)	Second Harmonic
HD(3)	Third Harmonic
Hz	Hertz
i	Instantaneous Current
K-Pad	Digital Control Pad of Capacitor's Position
KHz	Kilohertz
LHS	Left-Hand-Side
LSB	Least Significant Bit
μ	Micron (10^{-6} m)
mil	.001 of an Inch
MHz	Megahertz
MOS	Metal-Oxide-Semiconductor
MOSFET	MOS Field-Effect Transistor
MSB	Most Significant Bit
N(i,j)	Offset Data Matrix

NP(i,j)	Offset Phase Matrix
OA1	Opamp Used in Resettable Integrator
OA2	Opamp Used in Voltage Follower
Opamp	Operational Amplifier
P(i,j)	Phase of Acquired Data, D(i,j)
PAL	Programmable Array Logic
pf	Picofarad
Poly	Polycrystalline Silicon
ppm	parts per million
ϕ	Clock Phase
q	Instantaneous Charge
R	Resistor
Rd(i,j)	Corrected Data Matrix
Rp(i,j)	Resultant Phase Matrix
RHS	Right-Hand-Side
S	Switch
SC	Switched-Capacitor
SCR	Switched-Capacitor Resistor
SEM	Scanning Electron Microscope
sgn	Sign Function
T	Clock Period
U _s	Dimensionless Surface Potential
v	Instantaneous Voltage
v _d	Difference-Mode Voltage at the Input of an Opamp
v _{oe}	Output of Integrator
v _{of}	Output at Voltage Follower
VLSI	Very Large Scale Integration

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CHAPTER 1 INTRODUCTION

1.1 THESIS MOTIVATION AND OBJECTIVES

A major factor limiting the accuracy of switched-capacitor (SC) filters and the precision of analog-to-digital and digital-to-analog converters is the matching performance of integrated MOS capacitors. In addition, accuracy and precision may be limited by capacitor nonlinearity as well as opamp nonlinearity.

The principal objective of this thesis is to explore the use of a novel SC circuit technique to measure mismatch among capacitors. Furthermore, this circuit will be used to explore capacitor as well as opamp nonlinearity.

1.2 MOTIVATIONAL BACKGROUND

In the past decade, analog MOS technology has entered the VLSI mainstream using switched-capacitor circuit techniques. An important feature of the MOS capacitor, a natural element for precision voltage and charge division, is its ability to store charge for substantial amounts of time. It is possible to sense such a charge nondestructively and continuously since the input impedance of a MOSFET is, for all practical purposes, infinite. Since their conception over a decade ago, many SC circuits and filters have been designed, the precision of which depends upon the implementation of precision passive components. In monolithic form, resistors have poor absolute value as well as inherently poor matching performance. Capacitors, although poor in absolute value, do match well when good process and design techniques are employed [1,2]. In addition, high quality capacitors can demonstrate low voltage dependence, low temperature coefficient, and low silicon area requirements when compared to resistors. A comparison is tabulated in Table 1.1 [2].

Component	Matching	Voltage Coefficient	Temperature Coefficient
R (ion-implant)	.12%	800 ppm/v	400 ppm/C
R (diffusion)	.4%	200 ppm/v	2000 ppm/C
Capacitor (medium) (very large)	.1% .06%	10-100 ppm/v	26 ppm/C

Table 1.1 Characteristics of monolithic passive components.

a) Switched-capacitor

$$i = \frac{C_R(v_a - v_b)}{T}$$

b) Resistor

$$i = \frac{1}{R} (v_a - v_b)$$

Fig 1.1 a) b) By examining the average current flow through both these passive components, the equivalent SCR may be found.

With the ever increasing complexity of circuits, it has been desirable to integrate complete filters and circuits on single chips. A common application of MOS analog integrated filters has been in the voice frequency band (0-4KHz). Such filters require poles to be relatively low in frequency, which often means that large valued passive components must be used [1]. However, by using equivalent switched-capacitor resistors, it is possible to emulate the troublesome and large valued resistor by means of the timed charging of capacitors as follows.

1.2.1 THE SWITCHED-CAPACITOR PRINCIPLE

A synonymous relationship between the current flowing through a branch containing a switched-capacitor and the current flowing through a resistor may be seen with the aid of Fig. 1.1 a) and b). S1 and S2 are two MOS switches that are turned on and off according to two-phase, non-overlapping clock signals, ϕ_1 and ϕ_2 . When ϕ_1 is a logic 1, S1 closes so that C_A is charged to a voltage v_a . When S2 closes during ϕ_2 (logic 1), C_A charges to v_b . The net charge transfer, Δq is

$$\Delta q = C_A(v_a - v_b) \quad (1.1)$$

The amount of current flowing into the equivalent switched-capacitor resistor (SCR), C_A is directly proportional to the amount of charge transferred to and from the capacitor in every clock period T. Then

$$i = \frac{\Delta q}{\Delta t} = \frac{\Delta q}{T} \quad (1.2)$$

Substitution of equation 1.1 into 1.2 yields

$$i = \frac{C_R}{T}(v_a - v_b) \quad (1.3)$$

Referring to Fig. 1.1 b), the current flowing through the resistor is just

$$i = \frac{1}{R}(v_a - v_b) \quad (1.4)$$

By comparison of equations 1.3 and 1.4, the equivalent SCR (switched capacitor resistor) is then

$$R = \frac{T}{C_R} \quad (1.5)$$

This approximation is valid at low frequencies relative to the clock frequency. The smaller the capacitor is, the higher the resistance will be. In addition, it is desirable to reduce the size of capacitors for several other reasons. Opamps may slew faster with less loading. This translates to faster operating speeds. In addition, less silicon will be utilized. However, as the size of capacitors decreases to meet this demand, the matching accuracy between capacitors decreases.

Capacitor mismatch among modest to large sized capacitors has successfully been measured using standard capacitance meters. However, small capacitors as used in SC contexts are inaccurately measured due to the limited resolution of such meters, in addition to the existence of both on-chip and off-chip parasitic capacitance. What is then required is an on-chip, parasitic insensitive measurement technique that is capable of measuring capacitor mismatch of small capacitors with much higher resolution than previously offered.

1.3 THE MISMATCH EXPERIMENT

The approach used here makes use of an opamp in the form of a resettable SC integrator, as seen in Fig. 1.2 in simplified form. Here, the matching between the two capacitors used in the integrator may be determined by manipulating which capacitor is in feedback. A dc input is fed into the input of the circuit, where it is effectively chopped into a square wave at a frequency equal to that of the clock. When the incoming dc voltage is switched to ground (during ϕ_1), the opamp is dc stabilized by the use of a reset switch which shorts the output of the opamp upon itself. As this reset occurs at a relatively high clock frequency, it is expected that there will be no drift or measurement difficulties.

Depending on which of capacitors C_1 or C_2 is in feedback, the output v_o will vary due to the inherent mismatch of capacitors. This difference is sampled and measured by frequency-selective measurement techniques for example using a spectrum analyzer. Frequency-selective measurement techniques have advantages over time domain measurements due to the narrow bandwidth of the measurement filter. This filter excludes much of the noise and allows much more accurate measurement of small-signals.

With this fundamental circuit approach, it is possible to introduce an array of capacitors to be tested for matching. They will be placed strategically across a die to test for systematic variations. The circuit operation is just a logical extension of the two-capacitor case whereby at any given time, one of the capacitors from the array is placed in feedback. The remaining capacitors are then placed together as a parallel combination and act as the feedforward capacitance.

An algorithm is used to mathematically extract the mismatch error. In addition, it provides information about the resolution of this measurement technique.

Fig 1.2 Basic circuit using a resettable integrator.

The complete SC circuit containing an eight-capacitor array was designed, laid out and fabricated in 1.5μ CMOS technology as may be seen in the layout of Fig. 1.3.

1.4 NONLINEARITY EXPERIMENT

Capacitor mismatch is not the only mechanism which gives rise to voltage errors in circuits. Harmonic distortion due to nonlinearity may also manifest itself as a voltage error.

The underlying nature of nonlinearity can be considered in the form of the power series expansion

$$y = a_0 + a_1x + a_2x^2 + a_3x^3 + \dots + a_nx^n \quad (1.6)$$

This expansion may relate to any nonlinear system or element, such as nonlinear charge on a capacitor for example.

The nonlinearity experiment uses a variation of the SC circuit used in the capacitor mismatch experiment. Here, a single capacitor remains in feedback (no swapping action) while the remaining capacitors in the array are combined into the feedforward capacitance like before. Now, a single, low-frequency sine wave is applied to the input of the circuit (instead of dc).

Harmonic distortion of the resulting sine wave at the output may be measured on a spectrum analyzer by measuring the amplitude of the individual harmonics. By a mathematical process, a quantitative link between nonlinearity and harmonic distortion may be made.

Two major sources of nonlinearity are thought to be capacitor nonlinearity and opamp nonlinearity. The measured harmonic distortion will be compared to both theoretical sources of predicted harmonic distortion to see which source dominates.

Fig 1.3 Layout of SC Circuit used in both the Capacitor Mismatch Experiment and the Nonlinearity Experiment.

1.4.1 CAPACITOR NONLINEARITY

Capacitor nonlinearity is often thought about, by circuit designers, in terms of the voltage coefficient of capacitance. The nonlinearity of capacitors stems from the voltage dependent depletion region in the silicon forming the capacitor's plates. Depending on how heavily doped the plates are, this effect may or may not be a dominating factor in the overall linearity of the circuit. In detail, the contribution to harmonic distortion in the circuit from capacitor nonlinearity may be found by solving the charge balance equation for the resettable SC integrator using an expression that represents the nonlinear capacitor. Should the capacitors used be nonlinear enough so that they are the dominant source of harmonic distortion in the circuit, this technique would enable the voltage coefficient of capacitance to be found from the measured harmonics.

1.4.2 OPAMP NONLINEARITY

Opamp nonlinearity comes about primarily from the finite gain of the opamp, which gives rise to a difference-mode voltage at the opamp input. Once again, a charge balance equation may be written for the opamp keeping in mind the nonideal virtual ground. From this, the harmonic distortion arising from the opamp nonlinearity may be understood.

1.5 THESIS ORGANIZATION

This thesis is a study of an exploration into a novel SC circuit technique capable of measuring capacitor mismatch in small capacitors as well as studying both capacitor and opamp nonlinearity.

Chapter 1 gives the motivation for the pursuit of this topic. In addition, the chapter provides an introduction to the topics of the

thesis. In chapter 2, the capacitor mismatch experiment is discussed, including the operating principles of the circuit. Chapter 3 presents the experiment, and the results are disclosed. In chapter 4, the causes of mismatch are briefly revealed.

Nonlinearity is the general topic of chapter 5, providing a necessary preparation for the next two chapters. Chapter 6 discusses capacitor nonlinearity whereas chapter 7 presents opamp nonlinearity, with experimental results. Finally, conclusions and recommendations for future work are presented in chapter 8.

CHAPTER 2 CAPACITOR MISMATCH

2.1 INTRODUCTION

The accuracy and reproducibility of the frequency response in frequency-selective switched capacitor filters as well as the required precision in stringent designs place a tight tolerance on MOS capacitor ratios [3]. Historically, errors due to capacitor mismatch in a well controlled process have been said to be on the order of .1% (i.e. 9 - 10 bit accuracy) relative to one another when constant area-to-perimeter structures were used and common-centroid layout techniques were employed [2,4,5]. However, as the geometric size of capacitors decrease, the matching accuracy may deteriorate.

The objective of this experiment is to measure the mismatch of these smaller capacitors using a novel SC circuit and frequency selective measurement techniques.

2.1.1 CLASSICAL METHODS OF JUDGING MISMATCH

Classically, capacitor mismatch has been measured using capacitor meters or bridges. Unfortunately, the resolution of this type of equipment approaches that of the capacitors used in this experiment. This is compounded by the fact that parasitic interconnect capacitances plague the measurement. Another method to measure the ratio error is to use a binary array of the capacitors in conjunction with a DAC. However, this occupies much chip area.

The SC circuit used here overcomes these problems in that it is much smaller than a DAC and provides for better resolution than previous methods by using measurements in the frequency domain, as will be discussed subsequently. As this is an on-chip measurement technique, the opamp virtual ground allows parasitic interconnect capacitance effects to be considered negligible.

2.1.2 THE TREND TOWARDS SMALLER CAPACITORS

Besides decreasing the geometric size of capacitors in an attempt to reduce overall chip area, circuit operation at higher speeds and larger bandwidths is often accomplished by the reduction of capacitor sizes so that opamp and other gain stages may slew faster.

In ADCs, the speed of the circuit may depend on the overall loading (i.e. the total array capacitance) [4]. As the total array capacitance of an N-bit array is 2^N times larger than the standard capacitor representing the LSB, this capacitor in turn may be designed to be very small, conceivably having poor matching. As the linearity of the ADC is most sensitive to the largest capacitor, each capacitor in the array should be a parallel combination of the smaller unit size capacitors (LSB's) so as to improve matching [5,6]. This improvement in matching is primarily due to the constant area-to-perimeter ratio of the capacitors in the array. This ensures that fringing effects are properly ratioed, and as well guarantees that the mismatch of all capacitors in the array are no worse than that of the unit size capacitor. This also improves capacitor ratio accuracy where large capacitance spreads exist, as seen in high-order SC filters [7].

The physical reasons for capacitor mismatch will be discussed later in chapter 4.

2.2 THE CAPACITOR MISMATCH EXPERIMENT - OVERVIEW OF CIRCUIT OPERATION

An SC circuit used to determine matching performance on an eight capacitor array was designed and implemented on 1.5 micron technology as seen in Fig. 2.1. The circuit consists of a resettable SC integrator (denoted by OA1 in the figure) and a sample-and-hold capacitor followed by a voltage follower (denoted as OA2). Through the use of switches,

any capacitor in the array may be selected to be in feedback while the feedforward capacitance, between the circuit input and opamp virtual ground, is just the parallel combination of the remaining capacitors. The circuit uses two-phase, non-overlapping clock signals, ϕ_1 and ϕ_2 . ϕ_1 resets the integrator to zero every clock cycle, while ϕ_2 delivers an edge to the feedforward capacitance from the dc input and allows amplification to take place with a gain of

$$\frac{V_{op}}{V_i} = \left| \frac{C_x}{C_y} \right| \quad (2.1)$$

where C_x is the effective feedforward capacitance and C_y is the feedback capacitor. The output V_o is sampled and held by ϕ_1 (during the on-time of clock ϕ_1), shortly followed by an integrator reset during ϕ_2 . During the reset phase, the sampled V_o remains held while a new feedback capacitor is selected. Amplification takes place a second time when a new V_o is sampled and held. The entire process of swapping the two capacitors from being part of the feedforward pool, C_x , to feedback, C_y , is repeated several times. The difference between the first V_o and the second V_o shows up as a square wave at V_o at half the clock frequency. This difference is a function of the mismatch between the two swapped capacitors.

2.2.1 THE BASIC TWO CAPACITOR ARRAY CIRCUIT

A simplified version of the switching process may be seen in Fig. 2.2. This depicts the basic two capacitor array along with each capacitor's switching assembly. For the moment, the feedforward pool, C_x , is reduced to one capacitor to simplify the explanation. One of the capacitors is selected to be in feedback by setting its respective capacitor enable pad, K_i , to be a logic 1, making it capacitor C_{i1} .

Fig 2.2 Basic Two Capacitor Array Circuit.

Similarly, the other capacitor is in feedforward, as its enable pad, K_1 , is set to a logic 0 making it C_1 . The virtual ground action of opamp OA1 suppresses parasitic capacitance effects, and hence the input voltage V_i delivers an edge to the virtual ground through C_1 and experiences a gain during ϕ_1 . The output V_{o1} is equal to

$$V_{o1} = -\frac{C_x}{C_y} V_i \quad (2.2)$$

as seen in Fig. 2.3 a), since the input is switched from analog ground to the DC voltage level V_i . When V_{o1} settles, it is sampled and held by ϕ_2 . The integrator resets and the capacitors C_1 and C_2 are swapped by appropriate logic control. During the next ϕ_1 phase, the output V_{o2} is equal to

$$V_{o2} = -\frac{C_y}{C_x} V_i \quad (2.3)$$

as seen in Fig. 2.3 b). Once again, V_{o2} settles and is then sampled. The difference between V_{o2} and V_{o1} is seen as a square wave and is denoted for now by $D(x,y)$ as shown in Fig. 2.3 c), due to any difference in capacitor size.

The eight capacitor circuit is just a logical extension of the fundamental two capacitor case. An analysis follows which derives the relative mismatch between capacitors from the resulting square wave amplitude at V_{o2} . Because this amplitude can be obtained by a single frequency measurement, at half the clock frequency as shown in Fig. 2.3 d), far better resolution can be obtained than has been possible with previous measurement techniques. It is well known that frequency

$$\text{a) } v_{Oy} = -\frac{C_x}{C_y} v_i$$

$$\text{b) } v_{Ox} = -\frac{C_y}{C_x} v_i$$

$$\text{c) } D(x,y) = v_{Ox} - v_{Oy}$$

$$\text{d) Peak at } F_{\text{clock}} / 2.$$

Fig 2.3 Basic circuit operation for the simplified two capacitor case. Swapping of capacitors occurs in a) & b) while the measurement may occur in the c) time or d) frequency domain.

selective measurements have advantages in small-signal measurement because the narrow bandwidth of the measurement filter excludes much of the circuit noise.

2.3 CAPACITOR MATCHING DATA ACQUISITION ALGORITHM AND ANALYSIS

To reiterate, a capacitor is selected to be in feedback by enabling it by its K-pad. All K-pads are set to a logic 0 except the selected one at any given time. A "set" is described as designating two capacitors to be swapped back and forth between the feedback capacitor and the feedforward array. The set K(1,2) for example, would initially entail putting C_1 in feedback so that the output V_{o1} , on the first clock cycle is equal to

$$V_{o1} = \frac{(C_2 + C_3 + \dots + C_8)}{C_1} V_i \quad (2.4)$$

On the second clock cycle, C_2 would be put in feedback and C_1 returned to the feedforward array. During ϕ_2 , V_{o2} becomes

$$V_{o2} = \frac{(C_1 + C_3 + C_4 + \dots + C_8)}{C_2} V_i \quad (2.5)$$

The difference in V_{o1} is $V_{o1} - V_{o2}$ and is designated $D(1,2)$. The fundamental frequency component from the resulting square wave is measured at the output, with a spectrum analyzer.

As will be shown later in the analysis, each die containing eight capacitors may be considered to have an average capacitance C . The mismatch error of each capacitor represents a deviation from this average capacitance. However, spectrum analyzer amplitude measurements

alone yield only the absolute errors of the capacitor deviation. The amplitude measurement does not say whether the capacitor deviation is above or below the average value, C .

Measuring the phase of $D(1,2)$ with respect to a reference signal ($\text{clock}/2$) gives the additional information which will tell whether c_1 is larger or smaller than c_2 . This becomes clear when considering the timing diagram of the example set $D(1,2)$, as seen in Fig. 2.4. Here, the case of c_1 being less than c_2 in absolute value is considered. Here V_{11} is greater than V_{12} and is seen in V_{12} with a negative phase with respect to the reference ($\text{clock}/2$). Had it been that c_2 was greater than c_1 , a positive phase would have been measured.

2.3.1 MISMATCH ERROR OF ALL CAPACITORS

To find the mismatch error of all capacitors on a die, the entire sequence consists of testing all possible combinations, and thereby acquiring amplitudes $D(i,j)$ and phases $P(i,j)$ for each set in the matrix shown below

$$\begin{array}{cccccccc}
 & K(1,2) & K(1,3) & K(1,4) & K(1,5) & K(1,6) & K(1,7) & K(1,8) \\
 K(2,1) & & K(2,3) & K(2,4) & K(2,5) & K(2,6) & K(2,7) & K(2,8) \\
 K(3,1) & K(3,2) & & K(3,4) & K(3,5) & K(3,6) & K(3,7) & K(3,8) \\
 K(4,1) & K(4,2) & K(4,3) & & K(4,5) & K(4,6) & K(4,7) & K(4,8) \\
 K(5,1) & K(5,2) & K(5,3) & K(5,4) & & K(5,6) & K(5,7) & K(5,8) \\
 K(6,1) & K(6,2) & K(6,3) & K(6,4) & K(6,5) & & K(6,7) & K(6,8) \\
 K(7,1) & K(7,2) & K(7,3) & K(7,4) & K(7,5) & K(7,6) & & K(7,8) \\
 K(8,1) & K(8,2) & K(8,3) & K(8,4) & K(8,5) & K(8,6) & K(8,7) &
 \end{array} \quad (2.6)$$

For each set $K(i,j)$, the square wave output and phase $D(i,j)$ and $P(i,j)$ respectively are measured. The sign of the resulting phase is attached to each $D(i,j)$ so

$$D(i,j) = \text{sgn}[P(i,j)] \cdot |D(i,j)| \quad (2.7)$$

An example of this matrix is shown in Appendix A, Fig. A.1. It represents the data acquired from one of several chips. In addition, it is intuitive from the lower left hand side of the matrix that $D(i,j)$ should equal $-D(j,i)$. To clarify, the resulting square wave amplitude $D(1,2)$ for example should equal $-D(2,1)$ as it should make no difference whether C_1 is swapped with C_2 or C_2 is swapped with C_1 . Should the transposition of $D(i,j)$ be unequal or uneven, it would be instinctive that an offset or other cause would be to blame. This redundancy is used in the measurement as a check to eliminate possible error.

2.3.2 ANALYSIS FROM DATA

With all $D(i,j)$ and $P(i,j)$ having been measured, an analysis with regards to an n capacitor array is necessary. Basically, it is necessary to ring the changes on all possible capacitor selections, before enough information is available to find the individual capacitor mismatch. The analysis follows.

Recall that for the SC integrator of interest, the output is

$$V_{oi} = \frac{C_1 + C_2 + \dots + C_n - C_i}{C_i} V_i \quad (2.8)$$

where i denotes which capacitor is in feedback. Now, all capacitors may be written as

$$C_i = (1 + \epsilon_i)C \quad (2.9)$$

where C is the average of the array of n capacitors, and ϵ_i is the error in the i th capacitor. By definition,

$$\sum_{i=1}^n \epsilon_i = 0 \quad (2.10)$$

since the average of all capacitors is C . An equation for the gain of an n capacitor array with $n-1$ capacitors in feedforward is required. Equation 2.8 may be rewritten as

$$\begin{aligned} \frac{V_{o1}}{V_i} &= \frac{(1+\epsilon_1)C + (1+\epsilon_2)C + \dots + (1+\epsilon_n)C - (1+\epsilon_i)C}{(1+\epsilon_i)C} \\ &= \frac{(n-1) + (\epsilon_1 + \dots + \epsilon_n - \epsilon_i)}{1 + \epsilon_i} \end{aligned} \quad (2.11)$$

Equation 2.11 may be reduced by introducing $\epsilon_i = -(\epsilon_1 + \epsilon_2 + \dots + \epsilon_n)$ from equation 2.10, hence

$$\frac{V_{o1}}{V_i} = \frac{(n-1) - \epsilon_i}{1 + \epsilon_i} \quad (2.12)$$

For instance, the set $K(1,2)$ produces the voltage difference $D(1,2)$. This difference may be mathematically found as follows.

$$\frac{V_{o1}}{V_i} = \frac{(n-1) - \epsilon_1}{1 + \epsilon_1}$$

Similarly

$$\frac{V_{o2}}{V_i} = \frac{(n-1) - \epsilon_2}{1 + \epsilon_2}$$

Hence

$$\begin{aligned}\frac{V_{o1} - V_{o2}}{V_i} &= \frac{(n-1) - \epsilon_1}{1 + \epsilon_1} - \frac{(n-1) - \epsilon_2}{1 + \epsilon_2} \\ &= \frac{n(\epsilon_2 - \epsilon_1)}{(1 + \epsilon_1)(1 + \epsilon_2)}\end{aligned}\quad (2.13)$$

To find the individual ϵ_i , consider the addition of all $D(i_{\text{fixed}}, j)$

i.e. Set

$$\begin{aligned}D(1,1) \quad V_{o1} - V_{o1} &= 0 \\ D(1,2) \quad V_{o1} - V_{o2} &= nV_i(\epsilon_2 - \epsilon_1) / [(1 + \epsilon_1)(1 + \epsilon_2)] \\ D(1,3) \quad V_{o1} - V_{o3} &= nV_i(\epsilon_3 - \epsilon_1) / [(1 + \epsilon_1)(1 + \epsilon_3)] \\ D(1,4) \quad V_{o1} - V_{o4} &= nV_i(\epsilon_4 - \epsilon_1) / [(1 + \epsilon_1)(1 + \epsilon_4)] \\ &\vdots \\ &\vdots \\ &\vdots \\ D(1,n) \quad V_{o1} - V_{on} &= nV_i(\epsilon_n - \epsilon_1) / [(1 + \epsilon_1)(1 + \epsilon_n)] \\ \hline \sum_{j=1}^n D(1,j) &= -n^2V_i\epsilon_1 / (1 + \epsilon_1)\end{aligned}$$

$$\sum_{j=1}^n D(1,j) = -n^2V_i\epsilon_1 \quad (2.14)$$

since

$$\frac{\epsilon_1}{1 + \epsilon_1} \approx \epsilon_1$$

solving for ϵ_1 ,

$$\epsilon_1 = \frac{\sum_{j=1}^n D(1,j)}{n^2V_i} \quad (2.15)$$

In general, the error of the i^{th} capacitor in an n capacitor array is

then

$$\epsilon_i = \frac{\sum_{j=1}^n D(i,j)}{n^2 V_i} \quad (2.16)$$

Obtaining the combination of all sets $D(i,j)$ involves a fairly complex control sequence which is best depicted by the K1 and K2 control signals in Fig. 2.4. After deciding which two capacitors are to be swapped into feedback, a PAL chip does the actual switching. After the required amplitude is found, another two capacitors are selected and the process is repeated until the matrix in equation 2.6 is filled.

2.4 THE TEST CAPACITORS

The test capacitors used in this experiment are minimum unit size capacitors designed specifically for SC filtering circuits. The capacitors are nominally .39pf in size. The ability to use the same capacitors as are used in the applications context is one of the advantages of this technique. The capacitors are designed so that their area-to-perimeter ratios remain constant when larger capacitor arrays are built up. The eight capacitors are laid out relative to the rest of the circuit as shown in block form in Fig. 2.5. The significance of the individual capacitors and their positions are listed below.

C_1 - Bottom LHS

C_5 - Bottom RHS

C_2 - Top LHS

C_6 - Top RHS

Fig 2.4 Timing diagram of set K(1,2) with $C1 < C2$.

Fig 2.5 Test capacitor array & general layout.

Fig 2.6 Aliased broadband thermal noise as modeled is the major contributor to the noise floor.

C_3 - Deliberate increase of 1% from unit size

C_4 - Deliberate decrease of 1% from unit size

C_7 - Unit size, inverted

C_8 - Unit size

Capacitors C_1, C_2, C_3 , and C_4 are in a square array to test for effects of local geometric distribution dependence. Capacitor C_5 is placed far away from the square array to test for this effect at a greater distance. Capacitor C_6 is inverted from the normal connection to investigate the effect of stray capacitance. Capacitors C_3 and C_4 have deliberate 1% size deviations for validating the circuit operation and size variation design algorithm.

2.5 RESOLUTION OF THE MEASUREMENT

The resolution of the measurement is ultimately determined by the noise floor of the circuit and the spectrum analyzer. Considering the frequency of operation and the size of the capacitors, the dominant source of noise in this circuit is thermal noise arising from aliasing of the broadband switch noise in the switched capacitors [3,8]. Both the feedforward and feedback capacitor will contribute to the overall thermal noise at the output. This noise may be modeled by inserting ac noise sources in series with the SC resistors as shown in Fig. 2.6. This noise is sampled on the sample-and-hold capacitor.

The switched-capacitor resistor (SCR) equivalents of the feedforward and feedback capacitances R_{ff} and R_{fb} , respectively are calculated approximately by

$$R_c = \frac{T}{C} \quad (2.17)$$

where T is the clock period. As the clock frequency is 200 KHz, $C_{FB} = .39pF$ and $C_{FF} = 2.73pF$, then

$$R_{FB} = 12.8M\Omega$$

$$R_{FF} = 1.83M\Omega$$

The power spectral density (PSD) arising from thermal noise in these two SCR's is $4KTR$ [V^2/Hz] [1]. The voltage spectral density (VSD) for each equivalent resistor is then

$$\begin{aligned}\bar{v}_{FB} &= \sqrt{4KTR_{FB}} \\ &= \sqrt{4 \times .415 \times 10^{-20} \times 12.8 \times 10^6} \\ &= 461nV/\sqrt{Hz}\end{aligned}$$

Similarly,

$$\begin{aligned}\bar{v}_{FF} &= \sqrt{4KTR_{FF}} \\ &= \sqrt{4 \times .415 \times 10^{-20} \times 1.83 \times 10^6} \\ &= 174nV/\sqrt{Hz}\end{aligned}$$

However, v_{FF} experiences a gain equal to the closed-loop gain of the circuit. In addition, these noise sources are uncorrelated. Hence, the total RMS voltage spectral density from thermal noise at the output will be

$$\begin{aligned}\bar{v}_n &= \sqrt{461^2 + (174 \times 7)^2} \\ &= 1306nV/\sqrt{Hz}\end{aligned}$$

This establishes the noise floor of the measurement since the spectrum analyzer noise floor is insignificant, and other thermal noises arising from the circuit are less than this. Also, $1/f$ noise will be insignificant at half the clock frequency. This calculation agreed closely with white noise measured in the experiment. The total RMS output voltage over a frequency range of 3 Hz as dictated by the resolution bandwidth of the spectrum analyzer is

$$\begin{aligned} v_n &= 1306 nV / \sqrt{Hz} \times \sqrt{3} \\ &= 2.26 \mu V \end{aligned}$$

A desired signal comparable to this noise would then be the minimum voltage resolvable. If a spectrum analyzer is used to measure an eight capacitor array, then from equation 2.16,

$$\begin{aligned} \epsilon &= \frac{v_n(n-1)}{n^2 v_i} \\ \epsilon &= \frac{(2.26 \mu V)7}{64 v_i} \end{aligned}$$

If $V_i = .2V$, then the chopped square wave v_i is $.09V_{RMS}$, giving $\epsilon = .00027\%$, equivalent to 18.5 bits of digital accuracy. Any error that is produced which is less than this must be discarded as the signal is comparable to the noise or less and the phase reading could be in error. Note, however that the resolvable error depends on the input voltage. The limit of input voltage is dictated by the breakdown voltage of the capacitors used and the highest voltage placed around them. By increasing the dc voltage at the input, the resolvable error becomes smaller.

Furthermore, by using a lock-in amplifier to measure the data, the

resolution of the measurement increases by orders of magnitude. A lock-in amplifier has the ability to extract correlated signals buried in excess of 60dB of random (i.e. thermal) noise [9]. Depending on the range of the lock-in amplifier available, say in the nanovolt range, it would then be possible to detect a 2.26 nV signal. Hence the potential of the circuit improves to the point where a $2.75 \times 10^{-4}\%$ error could be found. This is equivalent to a resolution of better than 28 bits theoretically.

2.6 SUMMARY AND CONCLUSIONS

A novel SC circuit was presented that provides greatly improved mismatch measurement capabilities over existing techniques. Experiments that verify this will be presented in the next chapter. The circuit, combined with a mathematical algorithm, proved itself to be quite useful in measuring very small differences in small capacitors.

The small test capacitors were strategically placed to test for local distributional effects and variations. As expected, by the nature of the parasitic insensitive configuration used, the effect of the inverted capacitor C_i was inconsequential. The resolution of the measurement, dictated by aliased thermal noise from switched capacitors, has been calculated.

Data acquisition and analysis to establish capacitor mismatch may be carried out swiftly under computer control as will be discussed in the following chapter.

CHAPTER 3 EXPERIMENT AND RESULTS

3.1 INTRODUCTION

The aim of this chapter is to provide a high level overview of the data acquisition and analysis procedure used to measure mismatch in small capacitors. In addition, after discussing the elimination of influences from spurious effects to be discussed shortly, the results will be tabulated and presented.

3.2 AUTOMATED TESTING AND PERIPHERAL HARDWARE

The algorithm for determining the mismatch error of each capacitor, as seen in section 2.3, requires that 49 voltages ($D(i,j)$) with their accompanying phases ($P(i,j)$) be measured for each die. To verify the data, reproducibility is guaranteed by repeating this step to see if there is little or no change in the data as a result. As twenty bonded chips are to be tested, the task of automating the procedure is warranted.

The test set up is shown in block form in Fig. 3.1. A dual phase lock-in amplifier, in addition to other equipment, is connected via HP-IB bus and is controlled by an HP lab computer. The 4-bit latch feeds a decoder which controls the capacitors via eight K-pads as defined in chapter 2. A programmable DAC supplies a precision dc voltage to the input of the circuit and a programmable function generator provides the master clock signal to the test board. Further peripheral hardware resides on the test board.

3.2.1 THE TEST BOARD

The schematic of the hardware, external to the bonded chip, is shown in Fig. 3.2. To reduce the great number of chips on board originally required to satisfy the complex switching requirements, a PAL

Fig 3.1 Computer Controlled Experimental Setup.

chip was programmed to handle the task of enabling the K-pads at the appropriate time.

The bonded chip and test board functions on -2.5V, 0V and +2.5V power rails. However, as the 4-bit latch provides 0 to 5V TTL logic, level translation of the 4 digital bits are accomplished through the use of Schmitt-triggered CMOS inverters (74HC14) as seen in Fig. 3.2. The remainder of the schematic contains straightforward combinational and sequential logic.

3.2.1.1 PRECAUTIONS

The chip was laid out with care so as to avoid capacitive couplings between the analog and digital domains as well as other standard layout precautions.

The test board was carefully designed and built, as analog and digital operations occur simultaneously in close proximity. Several precautions were taken to guard against digital crosstalk into the analog portion of the test board. Both analog and digital sections had separate ground planes to help in isolating power supply noise caused by digital switching. For the same reason, V_{DD} -to-GROUND and V_{SS} -to-GROUND crosslink bars were used topside, opposite the ground plane. Hi-speed CMOS (74HCXX series) ICs were used in place of TTL chips to reduce local glitches in the power rails from current consumption. This in combination with replacing large numbers of logic ICs by a PAL helped to reduce power supply noise.

In addition, critical signal lines were of the shortest possible length with large separations from other signal lines. Ground lines ran alongside strong crosstalkers and finally, analog signals were shielded by coaxial cable.

Upon running the experiment, it was found that these precautions were sufficient in alleviating problems that may have distorted the results due to influences external to the bonded chip.

3.3 INACCURACIES DUE TO SPURIOUS FEEDTHROUGHS CAUSED BY SWITCHES

As stated previously in section 2.3.1, a necessary condition for good data acquisition to have taken place was assumed to be that $D(i,j) = -D(j,i)$. That is, the square wave output should be the same when the definition of the capacitor corresponding to i and that corresponding to j is reversed. In fact, it was observed that a moderate difference existed and as such, the resulting mismatch errors would have been less accurate. This led to the conclusion that a varying displacement (capacitive) feedthrough voltage existed which depended upon which capacitors were selected to be swapped into feedback.

After deliberating the matter, this displacement was regarded as originating from the effects of switch selection-dependent charge dumping into the substrate whose effects are capacitively coupled to the virtual ground of the opamp. Most of this phenomenon is thought to take place when switches are disabled at the end of the reset (ϕ) phase, as shown in Fig. 3.3 a). Furthermore, these spurious digital-substrate feedthroughs, due to digital activity, are dependent upon the polarity of the reference signal with respect to the order of the set. These feedthroughs manifest themselves on the virtual ground node. This changes the balance or symmetry of the acquired data set so that $D(i,j)$ never equals $-D(j,i)$. The magnitude of the spurious displacement effect varies depending on which capacitors are selected. As one switch assembly (containing the ϕ switches) is different from that for any of the other capacitors, matters of self-alignment mismatch in transistors

Fig 3.3 a) Charge dumping occurs during disabling ϕ_1 .
b) Clock Scheme and effects upon V_{op} node.

as well as positional dependence around the circuit could give rise to "set dependent" ($K(1,j)$) feedthrough displacements.

A manner in which these effects cause offsets in the data is now presented. Although all the causes of offset are not fully known, the effects now discussed arise strictly after ϕ_1 opens beyond the switch threshold. The reset switch dumps charge onto the virtual ground where a resulting voltage v_r develops due to the input capacitance of the opamp. The existence of v_r causes amplification to take place during the dead time of the clocks as seen in Fig. 3.3b). When the loop is closed, the magnitude of v_r is determined by the incoming edge from the input as well as the existing dumped charge. This dumped charge causes an effective voltage offset v_{osA} at v_{op} just as ϕ_1 turns on. As the location of the reset switch is permanent, (its location does not change with the sets) the magnitude of the offset v_{osA} , due to charge dumping, will not change. Displacement of the voltage $v_{osA} = v_r(C_{r1}/C_{r2})$ occurs at the output so that $v_{opA} = v_{osA} + v_{oA}$ on the first half cycle of the measurement, when say capacitor A is in feedback. Similarly, when capacitor B is in feedback, $v_{opB} = v_{osA} + v_{oB}$ on the second half cycle of the measurement. Hence, the difference between v_{opA} and v_{opB} which determines the set amplitude $D(A,B)$ is $v_{oA} - v_{oB}$ as expected. This is to say that the effects of charge dumping alone are inconsequential.

However, digital-substrate interactions, whose effects are capacitively coupled, cause set-dependent variations on the virtual ground and the resultant voltage v_r . This set-dependent component of v_r now effects the measurement $D(A,B)$ as the offsets v_{osA} and v_{osB} (denoting which capacitor is in feedback) is no longer equal.

With the above understanding, it was realized that setting the input voltage, V_i to analog ground (0 volts) would allow the various feedthrough displacements to be measured. This is clearly seen as the output v_{op} , during ϕ_1 , will remain at v_{osA} as denoted by the dashed line in

Fig. 3.3 b) for the case of $V_i = 0$. For the first half of the set measurement $D(a,b)$, only V_{os} will be sampled and held on the first clock period. During the next reset phase (ϕ), capacitor B is placed in feedback, as operated by another switch assembly. Now v_{os} is sampled and held. Thus, the output V_o now yields only the difference in feedthrough displacements as denoted by $N(i,j)$ and has characteristic phase $NP(i,j)$, an example of which is given in Appendix A, Fig. A.2.

By subtracting the difference in feedthrough displacements from the data, it is intuitive that the induced error in the results will be cancelled out. Because these displacements are very small, the ability of the lock-in amplifier to pick signals out of noise is very useful.

3.3.1 THE ELIMINATION OF FEEDTHROUGH DISPLACEMENTS FROM DATA

The elimination of the feedthrough as explained above from data requires the use of phase. This may be seen more clearly when considering that the voltage difference, $D(i,j)$, might be conceivably larger or smaller than the feedthrough displacement differences for some particular $D(i,j)$. It is thus possible that the displacement difference could be of opposite phase to the data and hence a knowledge of sign would in fact be required to correct the data. There are eight possible outcomes as graphically described in Fig. 3.4. As depicted, the displacement $N(i,j)$ is subtracted from the data $D(i,j)$ vectorily by assigning signs to the data and displacements according to the signs of their phases $P(i,j)$ and $NP(i,j)$ respectively. Simply by allowing

$$D(i,j) = \text{sgn}[P(i,j)] \cdot |D(i,j)| \quad (3.1)$$

and

$$N(i,j) = \text{sgn}[NP(i,j)] \cdot |N(i,j)| \quad (3.2)$$

the correction is made by the single one-step operation

Fig 3.4 Graphical elimination of all possible cases of feedthrough displacements, $N(i,j)$ from data, $D(i,j)$.

$$Rd(i,j) = D(i,j) - N(i,j) \quad (3.3)$$

where $Rd(i,j)$ is the resultant. If $Rd(i,j)$ is positive, it has positive phase and vice-versa. An example of this operation may be seen in the $Rd(i,j)$ matrix in Appendix A, Fig. A.3.

After the correction is made, the new $Rd(i,j)$ matrix and its transpose was found to be much more acceptable in that $Rd(i,j) = -Rd(j,i)$ and hence the measurement gave self-consistent results.

3.4 EFFECTS OF ADDED CAPACITANCE DUE TO INTERCONNECT METALLIZATION

After a lengthy process of improving the measurement, the capacitor mismatch errors can be scrutinized with considerable depth. As seen from the errors resulting from the $Rd(i,j)$ matrix in Appendix A, Fig. A.3, capacitor C_1 , deliberately placed some distance from the square array C_1, C_2, C_3, C_4 (see Fig. 2.5), was consistently high. In addition, C_4 , the deliberately oversized capacitor was always lower than expected. The rest of the mismatch errors seemed very random, as expected. As data from twenty bonded chips gave the same trend, a closer investigation of the layout was carried out. It was revealed that the measurement for capacitor C_1 was corrupted because two metal lines connecting capacitor C_1 were allowed to run side by side for a short distance. It is a tribute to the precision of this measurement that it is possible to detect and measure the capacitance between short lengths of parallel metal lines, as the following demonstrates.

The top and bottom plates of C_1 have interconnect metallization running from the capacitor to its respective destinations. However, for a length of 120 microns, they run parallel to each other, separated by a distance of 3 microns, as may be seen in Fig. 3.5 a) and b). These offending lines are illustrated in the schematic of Fig. 3.5 c). This

Fig 3.5 a) Photomicrograph of C8 and b) offending metallization

Fig 3.5 c) Schematic of Capacitor Mismatch Circuit denoting offending metallization which adds extra capacitance to capacitor C8.

metallization acts as additional capacitance to C_1 . As small as this additional capacitance is, the sensitivity and resolution of this measurement technique clearly detected it. This additional capacitance was theoretically calculated as follows.

A cross-section of the die was made by cutting through the metallization of interest and SEM photomicrographs were made to verify the dimensions of the adjacent metal lines. Fig. 3.6 depicts the dimensions of the top and bottom plate interconnect metallization. The two lines form a capacitor in their own right, due to the adjacent metallization. In this case, the effects of fringing cannot be neglected. To a good approximation, the capacitance coupled with the fringing effect [10] may be expressed as

$$C \approx \frac{\epsilon_r \epsilon_0}{d} \left(l + \frac{3}{8}d \right) \left(w + \frac{3}{8}d \right) \quad [F] \quad (3.4)$$

Given that $d = 3\mu$, $w = .75\mu$, $l = 120\mu$ and $\epsilon_r = 3.9$, then

$$C = \frac{(3.9)(8.85 \times 10^{-14})}{3 \times 10^{-4}} \left[120 \times 10^{-4} + \frac{3}{8}(3 \times 10^{-4}) \right] \left[.75 \times 10^{-4} + \frac{3}{8}(3 \times 10^{-4}) \right] \\ = 2.61 \text{ fF}$$

It is interesting to note that the effects of fringing account for over 50% of the value of this capacitance.

3.4.1 PROCEDURE FOR SUBTRACTING THE ADDED CAPACITANCE CAUSED BY CAPACITOR INTERCONNECT METALLIZATION

The extra metal interconnect capacitance found in the above section unquestionably affects the outcome of the resulting errors since the

Fig 3.6 Dimensions of the top & bottom plate of interconnect metallization. They run parallel to each other for $120u$, separated by $3u$.

average capacitance is shifted.

From independent tests performed on large capacitors, the unit capacitor used in this experiment is estimated to be

$$C_D = .392656 \quad [pF] \quad \text{nominal}$$

Under normal circumstances, C_D should have been the average capacitance used in this experiment. However, as 2.61 fF of capacitance is inadvertently added to C_D , the average capacitance is elevated by 2.61/8 fF so in reality, the average capacitance is closer to

$$C_{AV} = .392982 \quad [pF]$$

This explains why capacitor C_D is always low as seen in Appendix A, Fig. A3.

A translation is now in order to shift the average capacitance C_{AV} to C_D so as to eliminate the effect of the interconnect capacitance. Let ϵ_x' , as determined from measurements, be represented by

$$C_x' = (1 + \epsilon_x') C_{AV} \quad (3.5)$$

and the real ϵ_x , rendered by

$$C_x = (1 + \epsilon_x) C_D \quad (3.6)$$

Now,

$$C_x = C_x' \quad \text{for } x = 1, 2, 3 \dots 7 \quad (3.7)$$

$$C_8 = C_8' - .00261 \quad [pF] \quad (3.8)$$

Combining equations 3.5 and 3.6, the genuine mismatch error, ϵ_x , is given by

$$\epsilon_x = \left[\frac{(1 + \epsilon_x') C_{AV}}{C_D} - 1 \right] \quad x = 1, 2, 3 \dots 7 \quad (3.9)$$

$$\epsilon_8 = \left[\frac{(1 + \epsilon_8') C_{AV} - .00261}{C_D} - 1 \right] \quad (3.10)$$

Hence, the actual mismatch error, without the intervention of interconnect capacitance is established. An example of this correction is seen in Appendix A, Fig. A4. The results will now be discussed.

3.5 RESULTS

The outcome of this experiment is summarized by presenting the resulting mismatch errors in a form that may be easily understood.

The average error from all capacitors (120 samples in all) is found to be .08%. This would mean that an ADC or DAC design would be limited to 10 bits of precision.

The errors were analyzed for trends in an attempt to link mismatch to systematic errors such as oxide gradients across the die. In addition, local variations with respect to geometric arrangements of the array as well as distant positional dependence were sought. No discernable trends other than random variations were found on any of these counts. To show the mismatch to be totally random in nature, all 120 capacitors were subjected to a Gaussian fit. This proved useful, as seen in Fig. 3.7 a), in that the data has a good correlation factor (.99) as the data fits well to the regressed Gaussian straight line with high confidence (>.95). The mean of all mismatch errors (the distribution is centred about this error i.e. 50% cumulative probability) is very close to zero as expected and as dictated by the

algorithm. From this, the standard deviation is calculated and hence the 3σ point deduced. The standard deviation is found to be .103% and hence 99.7% of all mismatch errors are within .309% (3σ point).

With regards to Fig. 3.7 b) to 3.7 g), each of the individual capacitors C_1, C_2, C_3, C_4, C_5 , and C_6 were checked only for random behaviour. As C_1 and C_6 were used for validation only, they were not used. As there are only twenty bonded chips and hence only twenty samples of each capacitor, the quantity of data is considered to be statistically inconclusive. As such, only insight rather than statistical fact should be extracted from Figs. 3.7 b) through 3.7 g). As seen in these figures, however, all capacitors fit well with a good degree of correlation and the capacitance variations are considered to be random in nature. Nonetheless, their distributions are centred around errors other than zero. This may be simply explained by denouncing the quantity of data as statistically insignificant. Thus more data would have centred the distributions better. Alternatively, as seen by the stray metal to metal capacitance found in conjunction with C_6 , there may be small biases of some sort caused by extra stray capacitance added to some of the other individual capacitors. This would displace the mean away from zero as discussed in the previous section.

3.6 SUMMARY AND CONCLUSIONS

The main concern of this chapter has been to furnish a satisfactory summary of the experimental procedure and precautions used. The problem of added capacitance due to capacitor interconnect metallization was discovered and treated, as well as the effects of spurious feedthroughs. Each of these complications were treated separately and accounting for them produced accurate and valid results.

As no observable trends were seen in terms of local or positional variations, the mismatch errors derived from the data were introduced to

statistical scrutiny in an attempt to validate their random behaviour.

The average mismatch error, .08% is slightly better than what is seen in literature for the size of capacitors used. The 3 σ point spread at .309% covers 99.7% of all samples.

A discussion as to the potential causes of capacitor mismatch and possible improvements follow in the succeeding chapter.

Fig 3.7 a) Gaussian Regression of all samples
(50% cumulative probability denotes mean of distribution)

Fig 3.7 b) Gaussian Regression of All Individual C1 errors.

Fig 3.7 c) Gaussian Regression of All Individual C2 errors.

Fig 3.7 d) Gaussian Regression of All Individual C5 errors.

Fig 3.7 e) Gaussian Regression of All Individual C6 errors.

Fig 3.7 f) Gaussian Regression of All Individual C7 errors.

Fig 3.7 g) Gaussian Regression of All Individual C8 errors.

CHAPTER 4 CAUSES OF MISMATCH

4.1 INTRODUCTION

In order to reduce the physical size of capacitors, the reduction of the oxide thickness between capacitor plates is essential. With advanced MOS structures, the ability to grow uniform, high quality oxide is indispensable. In present technology, thin oxide is grown slowly enough so that uniformity and reproducibility is easily obtained. However, several factors with regards to the oxide and, the deposition of polycrystalline silicon (poly) lead to the mismatch of capacitors.

It is the primary purpose of this chapter to provide insight into the possible causes of mismatch. Although the exact cause is not known, it is believed that a combination of several mechanisms give rise to the overall random mismatch error.

Finally, array design practice must be reviewed so that the mismatch performance offered by individual capacitors does not get undermined by the careless design and placement of capacitors.

4.1.1 HISTORICAL CAUSES OF MISMATCH

Earlier process technology could realize mismatch errors down to .1% using capacitors whose oxides were thick by today's standards. At this point in technology, there were three main mechanisms clearly responsible for mismatch. Fig. 4.1 depicts random edge variations that were caused by the jagged edge nature of the poly (or aluminum) due to rough edges of the developed photoresist and subsequent wet etch of the material [11]. Fig. 4.2 shows the effects of undercutting the mask which defines the top plate of the capacitor. This was due to a poorly controlled lateral etch which occurred during the wet etching phase [5]. In modern processes, plasma etching has taken the place of wet etching, imparting to the capacitor much better edge definition and relatively no

Fig 4.1 Random Edge Variation in a MOS Capacitor

Fig 4.2 Undercut error from poorly controlled lateral etch.

undercut in the conventional sense [2]. SEM photomicrographs of the top and bottom plates of a capacitor are shown in Fig. 4.3 a) and b) so that the edge definition of the plate's periphery may be viewed first hand. As can be seen, grain boundaries make for small notches inwards into the plate. This effect is relatively inconsequential. However, should this effect be severe enough, its consequence can be minimized by designing capacitors to have constant area-to-perimeter (A/P) ratios. This is so that errors in the periphery may be cancelled out when capacitors are ratioed. Such is the structure as seen in Fig. 4.4, a typical capacitor used in this experiment. Constant A/P ratio structures will be discussed shortly.

Finally, long range oxide gradients were thought to have been a major contributor to mismatch. A decade ago, gradients of up to 100 ppm/mil were observed and common-centroid placement of capacitors, as will be discussed later, were required to help minimize this effect [5]. However, improved oxide growth techniques have made oxide gradients much less significant.

Of course, the causes of mismatch depend greatly on the process technology involved in making the capacitors. However, with regard to modern process technology, it may be established that these three generally accepted causes of mismatch are no longer significant. Insight into the advanced causes of mismatch will follow.

4.2 EDGE EFFECTS AS A CAUSE OF MISMATCH

As can be seen in Fig. 4.3 a) and the cross-section of Fig. 4.5 a), the edge definition is quite good. However, upon closer examination of the top plate periphery, the poly at the edge experiences lifting as well as being re-entrant. This is to say that as the reactive ions in the plasma increases in concentration due to less loading, the poly will be etched at a faster rate often at an inwards angle. This angle

a)

b)

Fig 4.3 a) Top plate over bottom plate. b) Bottom plate only.
Effects of edge definition is insignificant.

Fig 4.4 SEM photomicrograph of the poly-poly capacitor used in this experiment.

Fig 4.5 a) SEM photomicrograph of a cross-section of the poly-poly structure. The critical dimensions of the top plate are in question due to the re-entrancy of the top poly plate.

Fig 4.5b) Poly overetching leads to re-entrant poly edges as the plasma increases in concentration.

Fig 4.5c) Compressed oxide grows on newly etched poly surface. This leads to lifting of the perimeter of the Poly2 plate.

depends on how overetched the poly is as seen in Fig. 4.5 b). Upon re-oxidation, the newly bared poly surface oxidizes, thus compressing its newly formed oxide against the old. This effectively lifts the periphery of the top plate as seen in Fig. 4.5 c). This is similar to an effective undercut. The thinner the top plate is, the more vulnerable its periphery will be to lifting. This effective undercut may be minimized as follows.

4.2.1 IMPORTANCE OF CONSTANT AREA-TO-PERIMETER RATIO CAPACITORS

The ratio of the area of the top plate to its perimeter must remain constant for all capacitors in an array. The reasons are two-fold. Firstly, the effective undercut from poly lifting and poly re-entrancy as discussed above is proportional to the perimeter of the top plate. Secondly, the fringing capacitance associated with the periphery (edge component) is, of course, also proportional to the perimeter. It is intuitive that capacitors having constant A/P ratio between them allow these edge effects to be properly ratioed [12]. This allows large arrays to be properly constructed without degrading the potential mismatch performance offered by the individual capacitors. This may be seen more clearly by considering two capacitors C_1 and C_2 as seen in Fig. 4.6. Both these structures are twice the size of the unit capacitor C_1 except that C_2 is a parallel combination of two unit capacitors. For purposes of demonstration, each capacitor is subject to an "effective undercut" Δx around the perimeter of each top plate. Consider the A/P ratio of each structure as follows. Let $L_1 = 2$ units and $L_2 = 2$ units in length.

The unit size capacitor, C_1 has an A/P ratio

Fig 4.6 Two capacitor structures, C_2 & C_1 , are both twice the size of the unit size capacitor, C_1 .

$$A_1 = (L_1 - 2\Delta x)^2 = (\sqrt{2} - 2\Delta x)^2$$

$$P_1 = 4(L_1 - 2\Delta x) = 4(\sqrt{2} - 2\Delta x)$$

$$A_1/P_1 = \frac{1}{4}(\sqrt{2} - 2\Delta x)$$

For the capacitor that is physically twice the size of C_1 , the capacitor C_2 has an A/P ratio

$$A_2 = (L_2 - 2\Delta x)^2 = (2 - 2\Delta x)^2$$

$$P_2 = 4(L_2 - 2\Delta x) = 4(2 - 2\Delta x)$$

$$A_2/P_2 = \frac{1}{2}(1 - \Delta x)$$

For the capacitor that is the parallel combination of two unit capacitors, C_2' has an A/P ratio

$$A_2' = 2(L_1 - 2\Delta x)^2 = 2(\sqrt{2} - 2\Delta x)^2$$

$$P_2' = 2(4)(L_1 - 2\Delta x) = 8(\sqrt{2} - 2\Delta x)$$

$$A_2'/P_2' = \frac{1}{4}(\sqrt{2} - 2\Delta x)$$

As can be seen, the A/P ratio of the unit size capacitor and the parallel combination capacitor are the same. The implications of this are easily demonstrated in ratioed circuits. Consider an opamp to have a closed-loop gain of 2. In the parallel combination case,

$$\frac{C_2}{C_1} = \frac{2(\sqrt{2}-2\Delta x)^2}{(\sqrt{2}-2\Delta x)^2} = 2$$

However, in the physically double sized capacitor,

$$\frac{C_2}{C_1} = \frac{(2-2\Delta x)^2}{(\sqrt{2}-2\Delta x)^2} \neq 2$$

Hence, it is conclusive that perimeter effects are inconsequential if capacitors observing constant area-to-perimeter ratios between them are used in ratioed circuits.

4.3 SURFACE ROUGHNESS OF POLY PLATES AS A CAUSE OF MISMATCH

As stated earlier, the oxide gradient theory of mismatch is really not valid in the sense that the variation of oxide thickness across an entire wafer is less than 10% in modern processes. Should this have been the major mechanism of mismatch, the results would have shown a systematic error on the order of 16 bits accuracy between adjacent capacitors. However, undulation of the oxide does occur and is believed to be a major cause of mismatch. Of course, mismatch is process dependent, although it is believed that this cause is predominant and typical of modern processes and structures.

As seen in Fig. 4.3 a) the surface roughness of the poly plates gives rise to many mechanisms, some of which are not obvious. The actual undulations of the oxide are best seen in the cross-sectional SEM photomicrograph of Fig. 4.7 where the asperities (enlarged or pointy grains) are not as severe as may have been judged by the surface of the plates of Fig. 4.3 a) and b). Nonetheless, a comparison between two capacitors as seen in the SEM photomicrographs of Fig. 4.8 a) and b)

Fig 4.7 SEM photomicrograph of a cross-section of the poly-poly structure. The thinner oxide region may be the consequence of slower growth due to grain orientation {111}. It may also be the consequence of oxide compression at the apex of a grain and the poly floor. Oxide undulations are best seen here.

suggests differences in asperity severity leading to mismatch.

It is intuitive that large capacitors have some average asperity density (total asperity volume/surface area of the plate). Mismatch among large capacitors would be rather small as the asperity density would not change very much from capacitor to capacitor. However, small capacitors will have greater variance of asperity density and thus a greater mismatch, as seen in Fig. 4.8 a) and b).

The asperities or large grains give rise to small local variations in the oxide thickness for the following reasons.

4.3.1 OXIDATION OF POLY AND THE EFFECTS OF GRAINS

The structures and properties of poly depend on several factors. The most important having a bearing on the performance of capacitor mismatch are the temperature of deposition, dopant concentration and subsequent annealing temperature [13]. At temperatures below 580°C, the film is amorphous. Between 580°C and 625°C, the film is poly crystalline with {110} preferred orientation. At 675°C, the {100} orientation dominates. Films that are recrystallized between 900°C to 1000°C tend to have {111} grain orientation.

As the poly grains are of different orientation, the poly will have rough surface features. Annealing serves to smooth out the topography however an enlargement of the grain size may occur.

The oxidation of poly is enhanced not only by high surface concentration of dopants but also by the grain orientation [13]. For instance, {100} poly grows oxide much faster than {111} poly [14]. This is most certainly a cause of mismatch. In addition, high temperature processing is also the cause of enlarged grain boundaries. Not only do these grain boundaries leave ragged edges when etched, but enhanced oxidation has been shown to occur at the grain boundaries. It has been reported that the oxide may grow thicker over the grain boundaries and

#2

#1

Fig 4.8 a) Capacitor #1 has greater asperite density than
b) capacitor #2.

form intergranularity. However, high temperature processing causes oxide undulation to be less severe, as the oxide may reflow so as to smooth out roughness [13].

Furthermore, a grave concern relates not only to how large the asperity is but also how pointy it is. The oxide has a tendency to grow at a slower rate as the oxide becomes compressed at the apex of the asperities and the plate's floor, as seen in Fig. 4.7 and 4.9 a). This effect is thought to be significant and is a culmination of many layers of compressed oxide, whose effect at the end of the thermal oxidation cycle leaves a peripheral dip in the oxide [14].

It has been calculated that in order for a capacitor to have a mismatch of .08%, the oxide thickness would have to change by .2 Angstrom/ μm^2 . As many grains are on the order of $1\mu\text{m}$ in diameter, a small ridge of compressed oxide encircling a grain this size is easily visualized. As seen in Fig. 4.7, a region of oxide may be compressed. A ridge approximately 50nm wide is measured although the oxide thickness deviation cannot be measured. Fig. 4.9 b) depicts such a ridge and how deep the ridge would have to be in order to achieve .08% mismatch. As can be seen, only a $1\frac{1}{3}$ Angstrom deviation in oxide thickness would be required. Depending on the compressivity of oxide and local stresses, this may be optimistic. Certainly though, this is a contributor to mismatch.

Not obvious, as a cause of mismatch, is the excess surface area of the oxide blanket (and the top plate) due to the rough surfaces. As the oxide's (and top plate's) surface area is modulated by excess surface area from the asperities, it is calculated that for an equivalent $16\mu \times 16\mu$ square capacitor, only a $.2\mu^2$ difference in area would yield a .08% mismatch error. This is equivalent to the length and width of the $16\mu \times 16\mu$ capacitor being stretched out an extra .45 μ . As may be seen in Fig. 4.5 a) and 4.7, the grains have valleys or plateaus which require

Fig 4.9 a) Cross-section of the apex of an enlarged grain whose oxide compresses against the floor oxide.

Fig 4.9 b) The effects of depressed oxide around an enlarged grain.

extra area to traverse to the top or bottom of. From these diagrams, it may easily be seen that such effects contribute to mismatch.

Finally, the issue of lithographic accuracy should be addressed. As the plates of capacitors are defined by masks, one must question the accuracy of the pattern generator that makes them. The absolute tolerance is rather high. However, once the pattern is stepped, adjacent capacitors have differences in critical dimensions that is believed to be less than the mismatch of capacitors. That is to say that adjacent capacitor dimensions change by less than .013u, the amount required to give a .08% mismatch [14].

4.3.2 THE PROBLEM OF SURFACE ROUGHNESS ADDRESSED

As already stated, high temperature deposition of polysilicon will lead to rough surface contours due to the random orientation of the grains. Previous research has concluded that for a given capacitor array design, ratio errors are a function of the structure and of course, the process [12]. Up front, good oxide quality is essential. Secondly, flat surface structures such as diffusion (diffused bulk silicon) as seen in Appendix B, Fig. B1, yield the best matching performance. It is not surprising that metal-diffusion structures rated the best, followed by poly-diffusion structures, in terms of matching performance. The worst performance obviously comes from poly-poly structures [12]. Due to the advantages of the poly-poly over poly-diffusion structures, the issue of surface roughness must be addressed if this structure is to be used where good mismatch performance is required.

It has been reported that deposition of amorphous poly, followed by recrystallization (anneal) of the poly, greatly improves the surface quality and smoothness [13,14,15]. However, deposition of amorphous poly must be done at temperatures below 580°C where deposition rates are

slow. Nevertheless, compromises may be made in deposition rates and temperatures so as to optimize surface features and wafer throughput [14].

4.4 MATCHING PROPERTIES OF MOS CAPACITOR ARRAYS

Considerable effort has been put forth in making capacitors that have the best possible matching performance particular to the structure and process at hand. It is imperative though that capacitor arrays be built so as not to degrade the performance offered by the capacitors.

4.4.1 CAPACITOR RATIO ERRORS - DEPENDENCE UPON A/P RATIO

As seen previously in Sec. 4.2.1, edge effects such as effective undercut of the periphery or added capacitance from the edge component due to fringing must be safely ratioed out. The method of cancellation, as seen in the analysis of this former section, validated the logic of designing capacitors to have constant A/P ratios.

However, from a point of view of physical mismatch, there is a greater uncertainty in the performance of smaller capacitors. This is to say that the largest A/P ratio possible for a given capacitor is preferred over other structures [12]. This may be seen when remembering that peripheral effects play a part in contribution to mismatch performance. Minimizing the perimeter should help improve matching performance.

4.4.2 CAPACITOR RATIO ERRORS - DEPENDENCE UPON LAYOUT

Two points of interest pertain to this issue. Firstly, in circumstances where oxide gradients are significant, layout techniques which employ common-centroid placement of capacitors may be required to build arrays [5]. Common-centroid layout makes use of parallel combinations of unit size capacitors which are placed some distance away

from each other. This is done in an attempt to average out the effect of global oxide gradients as seen in Fig. 4.10. On the other hand, if local oxide gradients are present, this technique would not serve to cancel the effect. In addition, the added metallization required to realize this type of array in many instances serves to only complicate the layout.

Secondly, the theme of metallization interconnects is revisited. It has already been seen that parallel runs of metallization of top and bottom plate interconnects add severely to the value of the capacitor under consideration. In addition, arrays and parallel combinations of capacitors must carefully be constructed. The importance of this depends on the structure at hand, of course. Consider the structure in Fig. 4.11 a). The top plate as seen has parasitic metallization having an additional capacitance C' to the bottom plate of the capacitor. However, this does not pose a problem if arrays and combination of capacitors are properly built. Fig. 4.11 b) depicts a voltage divider whose large capacitor is built from ganged unit size capacitors. The voltage divider is designed to have a gain of $1/3$. Here,

$$\frac{V_o}{V_i} = \frac{C+C'}{(C+C')+(2C+3C')} \neq \frac{1}{3}$$

Fig. 4.11 c) depicts the same voltage divider except that the larger capacitor is an unganged combination. Here

$$\frac{V_o}{V_i} = \frac{C+C'}{(C+C')+2(C+C')} = \frac{1}{3}$$

as expected.

Depending on the structure used, proper care should be taken when

Fig 4.10 Common-Centroid Layout of a Voltage Divider.

Fig 4.11 a) Additional parasitic capacitance depends on structure. b) & c) are different array combinations.

designing capacitor arrays, as can be seen from the above. This is done so as not to degrade the potential matching performance offered by the individual capacitors.

4.5 SUMMARY AND CONCLUSIONS

The main concern of this chapter has been to bring the reader to an understanding of the problems faced in realization of capacitors of modern process structures. A new look was taken at the causes of mismatch.

It is assumed that the major cause of mismatch comes about from the surface roughness of the poly plates. Oxide undulation between the poly plates give rise to mismatch due to the following reasons. Firstly, different oxide growth rates occur depending upon which grain orientation exists as the floor. Secondly, compressed oxide at the apex of pointy asperities and the plate's floor give rise to dips in the oxide. Lastly, the additional surface area imparted to the top plate due to oxide undulations is proportional to the asperity density. The issue of surface roughness was addressed and suggested improvements made.

In conclusion, a personal note to designers who lay out arrays with regard to potential parasitics associated with the interconnect metallization of the capacitor structure. Depending on the structure, such parasitics may critically upset the values for the most or least significant bits in ADC's and DAC's depending on the architecture (i.e. integral nonlinearity).

Having concluded the topic of capacitor mismatch, the focal point of attention is now directed towards nonlinear distortion.

CHAPTER 5 NONLINEAR DISTORTION

5.1 INTRODUCTION

Historically, much effort has been put forth into the design of frequency-selective analog filters and other SC circuits [3]. Noise and harmonic distortion in SC filters can often limit high precision performance in stringent designs [16]. The next three chapters concentrate on the measurement and characterization of nonlinear distortion.

The major sources of distortion have been documented qualitatively as capacitor nonlinearity and opamp nonlinearity, including the linearity of the common source (CS) differential input pair [1,12,16,17,18].

Of particular interest in linear and low-distortion applications has been the linearity of capacitors. However, as MOS technology improves with the arrival of superior capacitor structures and improved process control, the effects of capacitor nonlinearity diminish, leaving an uncertainty as to whether it is a significant source of distortion. It is thought that by using a variation of the capacitor mismatch circuit, the nonlinearity and hence voltage dependence of the feedback capacitor of the SC integrator can be measured, should this source of distortion be predominant relative to other sources. On the other hand, should other mechanisms such as opamp nonlinearity be dominant, these are the mechanisms which it will be possible to measure.

The objective of this study is to explore different aspects of filter distortion in an attempt to link fundamental mechanisms to some of the general trends as seen in the nonlinearity experiment. The

implications of these distortion mechanisms ultimately place an upper limit on circuit design capabilities. For instance, in oversampled analog to digital converters, 16 bit accuracy may be required in some applications such as digital audio [19]. This level of accuracy may be limited by distortion mechanisms.

5.2 THE NONLINEARITY EXPERIMENT

A study of nonlinearity may be undertaken by making minor modifications to the capacitor mismatch experiment. Fig. 5.1, showing the circuit used in the nonlinearity experiment, is accompanied by Fig. 5.2 showing the pertinent section of the circuit when it is integrating within the on-time of clock ϕ_1 . Here, the scheme of using a single unit capacitor in feedback with the remaining unused capacitors in feedforward will provide the means to investigate nonlinearity.

The SC circuit contains several basic building blocks typical of those used in most SC filter applications. Perhaps one of the most important components of an SC circuit is the SC integrator whose primary function is carried out in the sampled-data domain. The circuit in our experiment uses a special case of the SC integrator in that it is reset once every clock cycle. To interface the sampled-data domain to the continuous-time world, a voltage follower is often used to terminate the circuit. Finally, switches and capacitors make the list of circuit components complete. Referring to Fig. 5.1, the nonlinearity circuit can be modeled by a block diagram of nonlinear components, Fig. 5.3 [20]. This is to illustrate the obvious factors which could be responsible for nonlinear circuit performance.

The most fundamental building block to be discussed in Fig. 5.3 is the opamp, which is used in both the sampled-data domain and in the transition to the continuous-time domain. If the opamp is nonlinear,

Fig 5.1 Simplified SC circuit used in the nonlinearity experiment.

Fig 5.2 SC integrator as a gain stage.

Fig 5.3 Sources of nonlinear elements as modeled by Fig 5.1. The opamp may be modeled as perfectly linear with nonlinearity $N(a)$.

Fig 5.4 DC transfer curve of opamp.

the resettable SC integrator (a gain stage here) will generate nonlinearity due to the nonideal virtual ground. The voltage follower, not having a virtual ground, will be subject to additional nonlinear distortion due to common-mode signal input to the differential input pair. If transients are incomplete, nonlinear switches in Fig. 5.3 will generate frequency dependent nonlinearities. Finally, the nonlinear capacitors in Fig. 5.3 will generate distortion.

5.3 NONLINEAR DISTORTION

To develop the basic approach used in this thesis, we will concentrate first on the non-time dependent (low frequency) nonlinearity of the opamp. The concept of nonlinear distortion can easily be visualized by considering an overall mid-band transfer characteristic curve as in Fig. 5.4. When the operating range of a circuit, amplifier, or even a single transistor goes beyond the straight line or linear portion about an operating point, distortion occurs. Introducing input frequencies that are less than the open-loop dominant pole of the opamp will allow the consideration of only static or time-independant phenomenon. In the case at hand, it is convenient to represent the overall open-loop amplifier transfer characteristic curve, before high frequency roll-off, by invoking the power series expansion. Assuming that common-mode input distortion effects are negligible, the instantaneous output voltage v_o , as a function of the difference-mode input v_d , is

$$v_o = a_o + a_1 v_d + a_2 v_d^2 + a_3 v_d^3 + \dots + a_n v_d^n \quad (5.1)$$

In concrete terms, a_o here represents the output referred offset (a departure from the bias point of 0 volts) and a is the linear gain

term, namely the slope of the dc transfer curve at the bias point in Fig. 5.4. This coefficient is very large and is essentially the DC gain of the opamp. The distortion components (a_2, a_3 , etc) are very small. If the amplifier transfer characteristic is truly linear, all the a_i coefficients except a_0 and a_1 are zero.

$$v_o = a_0 + a_1 v_d \quad (5.2)$$

Nonlinear distortion measurements, depending on the context of the measurement, usually involve applying as-pure-as-possible sinusoidal test signals to the input of the amplifier. The input voltage, v_i in Fig. 5.2, may be written

$$v_i = V \sin(\omega t) \quad (5.3)$$

Substitution of equation 5.3 into 5.1 when written in terms of v_i yields

$$v_o = a_0 + a_1 V \sin(\omega t) + a_2 [V \sin(\omega t)]^2 + a_3 [V \sin(\omega t)]^3 + \dots + a_n [V \sin(\omega t)]^n \quad (5.4)$$

Assuming the coefficients $a_i = 0$ for $i \geq 4$ and using the trigonometric identities

$$\sin^2(\omega t) = \frac{1}{2} - \frac{1}{2} \cos(2\omega t)$$

$$\sin^3(\omega t) = \frac{3}{4} \sin(\omega t) - \frac{1}{4} \sin(3\omega t)$$

substitution into 5.4 yields

$$v_o = a_o + \frac{1}{2}a_2V^2 + \left(a_1V + \frac{3}{4}a_3V^3\right)\sin(\omega t) - \frac{1}{2}a_2V^2\cos(2\omega t) - \frac{1}{4}a_3V^3\sin(3\omega t) \quad (5.5)$$

Now, using the fact that $a_1 \gg a_2$ and $a_1 \gg a_3$, the byproducts of a_2 and a_3 resulting in a DC and a fundamental term may be neglected. This is the "Almost Linear Approximation" circuit approach used in this thesis. This is to say that in an "almost linear" system whose nonlinearities are very small, having a pure sine wave at the input to the system drives an "almost linear" transfer function whose byproducts may be considered negligible when solving for the fundamental solution. This discussion may be furthered by considering "almost linear" elements such as capacitors and as such, simplify calculations by invoking Volterra theory [21,22,23]. Volterra theory states that a nonlinear relationship may be reduced to a first order or linear equation if it is manipulated with a higher order equation containing the nonlinear terms of the original nonlinear relationship. This will be seen later.

From equation 5.5, it is evident that the output signal includes harmonics of the input signal. It is the existence of these harmonics that is a consequence of nonlinear distortion and is known as harmonic distortion.

5.3.1 RELATIONSHIP TO FREQUENCY DOMAIN MEASUREMENTS

Equation 5.5 may be rewritten into a more practical form

$$v_o = b_o + b_1\sin(\omega t + \phi_1) + b_2\sin(2\omega t + \phi_2) + b_3\sin(3\omega t + \phi_3) \quad (5.6)$$

where the coefficients of the harmonic, b_n , indicate the amount of distortion. A spectrum analyzer may be tuned to the frequency of each harmonic and the magnitude of each harmonic measured giving the value of b_n . Often, the magnitude of the individual harmonic frequency terms are expressed relative to the magnitude of the fundamental frequency and may be expressed in percentage terms.

We now need to relate the measured coefficients b_n to the more meaningful coefficients a_n of equation 5.1. From measurements we find

b_1 - the fundamental amplitude $[v]$
 b_2 - the second harmonic $[v]$
 b_3 - the third harmonic $[v]$

We define

$$\begin{aligned} b_2 &= h(2v)b_1 & [v] \\ b_3 &= h(3v)b_1 & [v] \end{aligned} \quad (5.7)$$

where $h(2v)$ is the harmonic distortion, or relative amplitude of b_2 with respect to b_1 and $h(3v)$ is the harmonic distortion of b_3 in respect to b_1 . This is graphically demonstrated in Fig. 5.5, where the harmonic distortion in dB can be read from the figure. Equating equations 5.5 and 5.6 and separating the variables yields

$$a_1 V + \frac{3}{4} a_3 V^3 = b_1 \quad (5.8)$$

or by the "Almost Linear Approximation",

$$\begin{aligned} a_1 V &= b_1 \\ -\frac{1}{2} a_2 V^2 &= b_2 \end{aligned} \quad (5.9)$$

Fig 5.5 Second and third harmonic distortion in dB as seen on a spectrum analyzer.

Fig 5.6 $q-v$ relationships at various voltage levels

2

OF/DE

2

MICRO

$$-\frac{1}{4}a_3V^3 = b_3 \quad (5.10)$$

There are, of course, higher order harmonic distortions, but we are concentrating on the second and third harmonic here. If the higher order distortions are small enough, they do not impinge significantly on the second and third harmonics.

Often b_i measurements are made with respect to the fundamental, b_1 . This process of normalizing changes a_i in equation 5.1 from a percent to $\%$ /V. In equations 5.8, 5.9 and 5.10 this normalization is easily carried out by dividing through by b_1 . By normalizing, $b_1/b_1 = 1$ (0 dB), $b_2/b_1 = h(2\nu)$ and $b_3/b_1 = h(3\nu)$. Rewriting 5.8, 5.9 and 5.10, we obtain a more practical system of equations relating directly to the harmonics measured.

$$a_1^f V + \frac{3}{4}a_3^f V^3 = 1 \quad (5.11)$$

or, by the "Almost Linear Approximation",

$$\begin{aligned} a_1^f V &= 1 \\ -\frac{1}{2}a_2^f V^2 &= h(2\nu) \end{aligned} \quad (5.12)$$

$$-\frac{1}{4}a_3^f V^3 = h(3\nu) \quad (5.13)$$

where $a_1^f = \frac{a_1}{b_1}$, $a_2^f = \frac{a_2}{b_1}$ and $a_3^f = \frac{a_3}{b_1}$

and where b_1 is just the fundamental output voltage.

Solving for a_1 , a_2 , and a_3 , will yield the coefficients for the nonlinear relationship as given by equation 5.1.

The reader is reminded that we have been dealing here strictly with the opamp, in terms of the difference-mode input v_d . It still remains to relate the distortion to the measurements in the closed-loop circuit of Fig. 5.2, and finally to relate this to the sampled data context of Fig. 5.1.

5.4 CAPACITOR NONLINEARITY COEFFICIENTS

It is now appropriate to formulate an approach for the nonlinearity of the capacitors which are used in the experiment, namely the input and feedback capacitors in Figs. 5.1 or 5.2. Consider the instantaneous charge q stored on a capacitor.

$$q(v) = q_0 + C_{i0}v + C_{i1}v^2 + C_{i2}v^3 + \dots + C_{in-1}v^n \quad (5.14)$$

where v is the small-signal voltage around the capacitor at a bias point.

We consider the capacitor to be an "almost linear" circuit element in the way that was discussed in the previous section. If the capacitor of interest, say C_u , is perfectly linear, the linear charge relation may be written as

$$q(v) = C_{i0}v \quad (5.15)$$

where C_u is the initial small-signal capacitance.

Starting from the fundamental nonlinear charge equation 5.14, the definition of small-signal capacitance is

$$C(v) = \frac{dq(v)}{dv} = C_{i0} + 2C_{i1}v + 3C_{i2}v^2 \quad (5.16)$$

$$= C_{i0} \left(1 + 2\frac{C_{i1}}{C_{i0}}v + 3\frac{C_{i2}}{C_{i0}}v^2 \right) \quad (5.17)$$

$$C(v) = C_{i0}(1 + \alpha_1 v + \alpha_2 v^2) \quad (5.18)$$

Equation 5.15 is the charge-voltage relationship with linear capacitance C_{i0} . Equation 5.18 substituted into 5.15 now gives an expression for nonlinear charges.

$$q(v) = C_{i0}(1 + \alpha_1 v + \alpha_2 v^2)v \quad (5.19)$$

This is yet a further demonstration of Volterra theory. Note that the third order term (C_{i3}) in equation 5.14 has now been dropped. Because of the differentiation of equation 5.14, the terms in α_1 and α_2 of equation 5.18 with respect to equation 5.16 generate the second and third harmonics respectively. From equations 5.17 and 5.18, we identify, for convenience

$$\alpha_1 = 2 \frac{C_{i1}}{C_{i0}} \left[\frac{\text{ppm}}{V} \right]$$

$$\alpha_2 = 3 \frac{C_{i2}}{C_{i0}} \left[\frac{\text{ppm}}{V^2} \right]$$

5.4.1 GRAPHICAL REPRESENTATION OF α_1 and α_2

Equation 5.19 is the nonlinear charge-voltage relationship whose nonlinearities are implied in the nonlinear small-signal capacitance definition of equation 5.18. The charge-voltage relationship when the various nonlinear coefficients are included is seen in Fig. 5.6. This figure depicts the relationship with both coefficients assumed negative and the effect of α_2 less than α_1 .

The capacitance-voltage relationship relates more closely to an understanding of the effect of different orders of voltage coefficients. Expanding the q - v relationship of equation 5.19,

$$q(v) = C_{10}v + C_{10}\alpha_1 v^2 + C_{10}\alpha_2 v^3 \quad (5.20)$$

By inspection, it can be seen that the product $C_{10}v$ is the linear charge, $C_{10}\alpha_1$ is the quadratic coefficient of charge in ppmF/V and $C_{10}\alpha_2$ is the tertiary coefficient of charge in ppmF/V^2 . Referring to Fig. 5.6, region 1 is relatively linear when at low voltages, where the quadratic and tertiary components do not significantly contribute to error. Regions 2 and 3 denote where the higher order terms do contribute significantly to nonlinearity.

Referring to Fig. 5.7, the nonlinear capacitance equation 5.18 is graphically demonstrated. In Fig. 5.7 a), the ideal capacitor, invariant to voltage, is shown with voltage coefficients equal to zero. In Fig. 5.7 b), the linear coefficient α_1 in ppm/V describes the linear fractional change of capacitance with voltage. It is α_1 that is in fact the voltage coefficient of capacitance γ ; as will be discussed later. In Fig. 5.7 c), the effect of the quadratic coefficient α_2 in ppm/V^2 is shown with an apparent parabolic dependence in the capacitance as a function of voltage. Often, this curve is approximated by α_1 as shown in Fig 5.7 c) by the dashed straight line, incorporating both α_1 and the average slope due to α_2 . This straight line approximation and corresponding α_1 is often loosely termed the voltage coefficient γ ; as this specification is sufficient in most circuit contexts. However, stringent precision ratioed circuit designs would suggest that the α_1 specification alone may not suffice as a ratio error would incur due to the α_2 term. That is depending on the voltage amplitude, α_1 can be significantly greater than α_1 .

Fig 5.7 C-v relationships at various voltage levels

Fig 5.8 Simple Voltage Divider.

5.4.2 RATIO ERRORS DUE TO CAPACITOR NONLINEARITY

As already stated, strict designs might not be realizable due to the α approximation. An example of this is easily demonstrated by considering a simple voltage divider shown in Fig. 5.8. Such a voltage divider can be used perhaps as a single component in a much larger array which produces reference voltages to be compared to an input voltage in a successive approximation ADC. For simplicity, consider the case when C_1 is three times the size of C_2 and hence the voltage across C_1 is three times that of C_2 . Now we may consider the effect of α_1 and α_2 on voltage division at different voltages. By substitution into equation 5.18, the attenuation of the voltage divider is

$$\begin{aligned} \frac{v_o}{v_r} &= \frac{C_1}{C_1 + C_2} = \frac{C_1(1 + \alpha_1 v_1 + \alpha_2 v_1^2)}{C_1(1 + \alpha_1 v_1 + \alpha_2 v_1^2) + C_2(1 + \alpha_1 v_2 + \alpha_2 v_2^2)} \\ &= \frac{C_1(1 + \alpha_1 v_1 + \alpha_2 v_1^2)}{C_1(1 + \alpha_1 v_1 + \alpha_2 v_1^2) + 3C_2 \left(1 + \alpha_1 \left(\frac{v_1}{3} \right) + \alpha_2 \left(\frac{v_1}{3} \right)^2 \right)} \end{aligned}$$

where v_1 = voltage across C_1 and v_2 = voltage across C_2 .

If the effect of α_2 is ignored and hence only α_1 is considered, then a linear ratio error is encountered as different voltages are swept through a range.

If α_2 is included in the calculation, then the ratio error is no longer a linear function of voltage. It now has a parabolic dependence. This would normally not be taken into account by circuit designers due to the α approximation.

5.5 EXPRESSING NONLINEARITY

Nonlinearity may be expressed in a variety of ways depending on the context. Classically, when harmonic distortion is of interest, the harmonic content of each multiple of the fundamental frequency is found. When nonlinearity is of interest, the error in a linear relationship is found. Examples of a nonlinear relationship are a transfer function describing the output voltage as a function of its input voltage in an amplifier or charge as a function of voltage in a capacitor. The nonlinear error can be linked to harmonic distortion as shown in Sec. 5.3. This error may then be described in terms of the number of bits accuracy in the same manner as quantization error is converted to digital bit accuracy. If there exists an error in voltage ΔV , then it may be stated, in terms of hypothetical N bit quantization of the voltage, that

$$\frac{\Delta V}{V} = \frac{1}{2^N} \quad (5.21)$$

Solving for N,

$$N = \frac{\log(1/\frac{\Delta V}{V})}{\log 2} \quad (5.22)$$

where N is number of bits and $\Delta V/V$ is the relative error. This will be demonstrated shortly.

5.6 ERROR FROM CAPACITOR NONLINEARITY (Charge-Voltage Error)

As discussed in the previous section, it is often convenient to describe the error in terms of the number of bits resolvable. Where

capacitor nonlinearity is concerned, this is best done through the charge-voltage relationship. Consider a purely linear charge-voltage relationship denoted by a superscript l and a nonlinear charge-voltage relationship, denoted by a superscript n , with only the linear coefficient of capacitance α_1 .

$$q^l(v) = C_{10}v \quad (5.23)$$

$$q^n(v) = C_{10}(1 + \alpha_1 v)v \quad (5.24)$$

Referring to Fig. 5.9, the error Δq is calculated at the voltage of interest, v' .

$$\begin{aligned} |\Delta q(v)| &= |q^l(v) - q^n(v)| \\ &= |C_{10}v - C_{10}(1 + \alpha_1 v)v| \\ |\Delta q(v)| &= C_{10}\alpha_1 v^2 \end{aligned} \quad (5.25)$$

Now, the relative error is

$$\left| \frac{\Delta q(v)}{q^l(v)} \right|_{v'} = \frac{C_{10}\alpha_1 v'^2}{C_{10}v'} = \alpha_1 v' \quad [\%] \quad (5.26)$$

In the case where α_1 and α_2 coefficients are present, then,

$$\begin{aligned} |\Delta q(v)| &= |q^l(v) - q^n(v)| \\ &= |C_{10}v - (C_{10}v + C_{10}\alpha_1 v^2 + C_{10}\alpha_2 v^3)| \\ &= C_{10}(\alpha_1 v^2 + \alpha_2 v^3) \end{aligned} \quad (5.27)$$

Hence the relative error at the voltage of interest, v' , is

Fig 5.9 Nonlinear capacitance error from the contribution of the linear coefficient of capacitance, $\propto 1$.

Fig 5.10 Relationship of v_o vs. v_i of a nonlinear system.

$$\left| \frac{\Delta q(v)}{q'(v)} \right|_{v'} = \frac{C_{10} \alpha_1 v'^2 + C_{11} \alpha_2 v'^3}{C_{10} v'}$$

$$\left| \frac{\Delta q(v)}{q'(v)} \right|_{v'} = \alpha_1 v' + \alpha_2 v'^2 \quad [\%]$$

5.7 ERROR FROM SYSTEMATIC NONLINEAR DISTORTION (AC Transfer Error)

We will now consider a complete circuit, without particular regard to the source of the nonlinearity. It is often desirable to convert the measured harmonic distortion to a quantifying error voltage expressed into the number of bits resolution of the circuit. Consider linear and nonlinear relationships as shown in Fig. 5.10, for example. The error voltage is

$$\begin{aligned} |\Delta v| &= |a_1 v_i - (a_1 v_i + a_2 v_i^2)| \\ &= a_2 v_i^2 \end{aligned} \quad (5.28)$$

The relative error is then

$$\left| \frac{\Delta v}{v} \right| = \frac{a_2 v_i^2}{a_1 v_i} = \frac{a_2}{a_1} v_i \quad [\%] \quad (5.29)$$

Similarly, if there is cubic dependence

$$\left| \frac{\Delta v}{v} \right| = \frac{a_2}{a_1} v_i + \frac{a_3}{a_1} v_i^2 \quad [\%] \quad (5.30)$$

5.8 SUMMARY

A fundamental understanding of systematic nonlinear distortion including opamp and capacitor nonlinearity in both a qualitative and quantitative manner was the main concern of this chapter.

In the next two chapters, an in-depth examination will be carried out of the circuit distortion mechanisms caused by capacitors and opamps respectively, and the results related to the data observed in the nonlinearity experiment.

CHAPTER 6 CAPACITOR NONLINEARITY

6.1 INTRODUCTION

Sampled analog circuit performance is a function of many variables. Linear and low-distortion performance is imperative in stringent designs such as analog-to-digital converters (ADC), digital-to-analog converters (DAC) and switched-capacitor (SC) filters [6].

Capacitor nonlinearity, specifically the voltage dependence of capacitors, has classically always been measured using C-V meters. As MOS technology advances, capacitor voltage dependence decreases and hence larger capacitors are needed to measure any appreciable voltage dependence using C-V meters.

By using a variation of the capacitor mismatch circuit, the nonlinearity and hence voltage dependence of the feedback capacitor of the resettable SC integrator can be measured, should this source of distortion dominate over all others. As the feedback capacitor can be relatively small, this technique has an advantage over the conventional method in saving overall chip area, as well as being useable with capacitor sizes more appropriate to their normal circuit context.

6.2 PRINCIPLE OF OPERATION

As stated earlier, Fig 5.1 shows the circuit used in the nonlinearity experiment and is accompanied by Fig. 5.2 depicting the relevant section of the circuit when it is experiencing gain. The

scheme of using a single unit capacitor in feedback with the other unused capacitors in feedforward will provide the means to measure nonlinearity of capacitors. Assuming the opamp has infinite gain and hence the ability to keep the virtual ground pinned to true ground, the feedback capacitor can be considered to be the primary source of nonlinearity as shown in the following. Consider the circuit with a closed-loop gain of 7 as shown in Fig. 5.2.

$$|gain| = \frac{C_{FF}}{C_{FB}} = 7 \quad (6.1)$$

The current i_1 is flowing from the input v_i to the virtual ground node and i_2 is the current flowing between the virtual ground and the output v_o . By definition, the current flowing through the feedforward and feedback capacitors are

$$i_1 = 7C_{FB} \frac{dv_i}{dt} \quad (6.2)$$

$$i_2 = C_{FB} \frac{dv_o}{dt} \quad (6.3)$$

Assuming that the capacitance C_{FB} is linear and that the input impedance of the opamp is infinite, then $i_1 = i_2$ so that

$$7C_{FB} \frac{dv_i}{dt} = C_{FB} \frac{dv_o}{dt} \quad (6.4)$$

Integrating with respect to dt , the relation between the input and output voltage of the integrator is obtained.

$$v_o = 7v_i \quad (6.5)$$

The subtlety that must be observed is that the voltage across the feedforward capacitor C_{FF} is $1/7$ that of C_{FB} , and thus the contribution of C_{FF} to the total nonlinearity as seen at the output will be relatively small. This may be demonstrated by considering nonlinear current, due to capacitor nonlinearity, flowing through the feedforward and feedback capacitors.

$$i_1 = C_{FF} \frac{d}{dt} (v_i + \alpha_1 v_i^2 + \alpha_2 v_i^3 + \dots + \alpha_n v_i^n) \quad (6.6)$$

$$i_2 = C_{FB} \frac{d}{dt} (v_o + \alpha_1 v_o^2 + \alpha_2 v_o^3 + \dots + \alpha_n v_o^n) \quad (6.7)$$

Note that the coefficients of voltage α_i are the same for both currents i_1 and i_2 . This must be true since the capacitors exhibit the same nonlinearity. Rearranging equations 6.6 and 6.7, we obtain

$$i_1 = 7 C_{FB} \frac{d}{dt} \left[\frac{v_o}{7} + \alpha_1 \left(\frac{v_o}{7} \right)^2 + \alpha_2 \left(\frac{v_o}{7} \right)^3 + \dots + \alpha_n \left(\frac{v_o}{7} \right)^n \right] \quad (6.8)$$

$$i_2 = C_{FB} \frac{d}{dt} [v_o + \alpha_2 v_o^2 + \alpha_3 v_o^3 + \dots + \alpha_n v_o^n] \quad (6.9)$$

A quick check by inspection of the linear terms demonstrates current continuity since $i_1 = i_2$.

$$i_1 = 7 C_{FB} \frac{d}{dt} \left(\frac{v_o}{7} \right) \quad (6.10)$$

$$i_2 = C_{FB} \frac{d}{dt} (v_o) \quad (6.11)$$

It is seen by inspection from 6.8 that

$$v_i^2 = \left(\frac{1}{7}\right)^2 v_o^2$$

$$v_i^3 = \left(\frac{1}{7}\right)^3 v_o^3$$

$$v_i^n = \left(\frac{1}{7}\right)^n v_o^n$$

If $v_i = V_i \sin(\omega t)$ and $v_o = V_o \sin(\omega t)$, we see that the square terms produce second harmonics, the cubic terms produce third harmonics and so on. To first order, it is intuitive that the contribution of nonlinear errors to the total nonlinearity of the feedback capacitor is

$$\left(\frac{1}{7}\right)^2 + \left(\frac{1}{7}\right)^3 + \left(\frac{1}{7}\right)^4 + \dots + \left(\frac{1}{7}\right)^n \approx \frac{1}{50}$$

Hence, the assumption that the feedback capacitor is the primary source of nonlinearity is demonstrated, assuming that capacitors are the only nonlinear elements.

6.3 MOS CAPACITOR STRUCTURES AND CAPACITOR NONLINEARITY

Next to MOSFETS, perhaps the next most important elements of analog MOS circuits are MOS capacitors. Capacitor nonlinearity comes about from the voltage dependence of depletion regions formed within the structure. The two most common MOS structures used in present day technology are the metal- or polysilicon over diffusion structure and the polysilicon-polysilicon structure. Summaries on the fundamental operation of these MOS structures may be found in Appendix B. The next

section is devoted to giving a fundamental understanding of the physical side of voltage dependence with respect to the two structures summarized in Appendix B.

6.3.1 VOLTAGE DEPENDENCE OF CAPACITANCE

As can be seen from semiconductor physics [24], the equations and physical principles which describe C-V behaviour can be very involved. In the context of circuit design, it is convenient to describe the voltage dependence of capacitors in a more simplistic form whereby it is sufficient to specify the nominal capacitance C accompanied by its rate of change of capacitance ΔC over a voltage range ΔV . For this reason the voltage coefficient of capacitance is used and is defined by

$$\gamma_V^C = \frac{1}{C} \frac{dC}{dV} \quad (6.12)$$

Should the doping of the plate or plates be degenerate so they emulate metal as closely as possible, the instantaneous capacitance tends to be a linear function of the instantaneous applied voltage. Considering the Metal-Oxide-Diffusion structure in Appendix A. McCreary [12], using Maxwell-Boltzmann statistics, has expressed γ_V^C for a degenerately doped plate at flatband as follows.

$$C_d = \frac{q}{KT} \frac{dQ_s}{dU_s} \quad (6.13)$$

$$C_d = \text{sgn}[U_s] \left[\frac{\epsilon_s q^2 N_d}{2KT} \right]^{\frac{1}{2}} [e^{U_s} - 1] [e^{U_s} - 1 - U_s]^{-\frac{1}{2}} \quad (6.14)$$

$$\gamma_V^c = \frac{1}{C_d} \frac{dC_d}{dV} = \frac{C_{ox}^2}{\epsilon_{si} q N_D} \frac{e^{2U_s} - 2U_s e^{U_s} - 1}{(e^{U_s} - 1)^3} \quad (6.15)$$

At flatband, $U_s = 0$ or $V = V_{fb}$, and hence

$$\gamma_V^c(V_{fb}) = \frac{C_{ox}^2}{3q\epsilon_{si}N_D} \quad (6.16)$$

For the oxide thickness that exists in the capacitors fabricated, a plot of $\gamma_V^c(V_{fb})$ as a function of doping is shown in Fig. 6.1.

There will be a small error associated with the theoretical γ_V^c as it is based on Maxwell-Boltzmann statistics. As the plates are doped degenerately, an iterative solution using Fermi-Dirac statistics would be complex and would not yield a closed-form solution.

McCreary [12] has shown that heavily doped polysilicon depletes and accumulates in a manner not unlike single crystalline silicon. In the polysilicon-polysilicon or polysilicon-silicon structures, one plate depletes while the other accumulates for an applied voltage and vice-versa when the voltage changes polarity. To clarify and expand upon this point, consider the poly-poly structure as depicted in the Appendix B, Fig. B4. McCreary has modeled this as an oxide capacitance in series with the depletion region capacitance of both poly plates as seen in Fig. 6.2.

$$\frac{1}{C_{total}(V)} = \frac{1}{C_{d1}(V)} + \frac{1}{C_{ox}} + \frac{1}{C_{d2}(V)} \quad (6.17)$$

This follows from the potential diagram shown in Fig. 6.3, as there must exist a finite surface potential ϕ_s and ϕ_s , across the Si/SiO₂ interfaces.

Fig 6.1 Theoretical $\gamma_v^c(\text{fb})$ versus Plate Doping.

Fig 6.2 Poly-Poly structure modelled as a series combination of the oxide (C_{ox}) and two plate depletion capacitances, C_{d1} and C_{d2} .

Fig 6.3 Potential diagram of voltage across poly plates.

Fig 6.4 Symmetrical C-V behaviour when both poly plates are equally doped.

The surface potential ϕ_s would be negligible when computing ϕ_s and vice-versa. This assumption is easily made when at least one plate is degenerately doped. Equation 6.17 is useful when computing C-V curves of, for instance, the polysilicon-polysilicon structure when the plates have different doping. It follows from the symmetry of the C-V curve as shown in equation 6.17, as described by Ellul [25], that the overall voltage coefficient is just

$$\gamma_V^C(\text{total}) = \gamma_V^C(\text{poly 1}) - \gamma_V^C(\text{poly 2}) \quad (6.18)$$

Of course, $\gamma_V^C(\text{poly 1})$ and $\gamma_V^C(\text{poly 2})$, the voltage coefficients with respect to the substrate, are calculated as if they were separate structures using Fig. 6.1. Thus it can be seen by inspection that for equally doped plates the overall voltage coefficient of capacitance for the poly-poly structure will tend to disappear. Also, by the symmetry of the poly-poly structure, the residual voltage dependence of capacitance will have the symmetrical form as shown in Fig. 6.4.

1.3 THEORETICAL DISTORTION CAUSED BY CAPACITOR NONLINEARITY

The single-ended SC integrator is shown in Fig. 6.5. Assuming the opamp is ideal and has infinite gain, the charge balance equations proceed as follows.

When ϕ_2 on :

$$\Delta q_1(2) = \Delta v_1 C_1 \quad \Delta q_2(2) = \Delta v_0 C_2 \quad (6.19)$$

When ϕ_1 on :

Fig 6.5 Single-ended Resettable Integrator.

Fig 6.6 Nonlinear capacitance may be modeled by harmonic generators driving linear capacitance.

V_i	V_o	HD(2)	HD(3)
10mV pk	70mV pk	-134 dB	-182 dB
100	700	-113	-142
142	1 V	-111	-136
286	2 V	-105	-124

Table 6.1 Theoretical harmonic distortion from capacitor nonlinearity.

$$\Delta q_1(1) = 0 \quad \Delta q_2(1) = 0 \quad (6.20)$$

Charge conservation dictates that

$$\Delta q_1(1) + \Delta q_2(1) = \Delta q_1(2) + \Delta q_2(2)$$

$$0 = C_1 \Delta v_i + C_2 \Delta v_o$$

thus

$$\Delta v_o = -\frac{C_1}{C_2} \Delta v_i \quad (6.21)$$

Assuming all components as ideal, the nonlinear capacitor $C_i(v)$ may be expressed as

$$C_i(v) = C_{i0}(1 + \alpha_1 v + \alpha_2 v^2) \quad (6.22)$$

where C_{i0} is the initial small-signal capacitance at a bias point. Substituting equation 6.22 into 6.21 yields

$$\Delta v_o = -\frac{C_{11}(1 + \alpha_1 v_i + \alpha_2 v_i^2)}{C_{12}(1 + \alpha_2 v_o + \alpha_2 v_o^2)} \Delta v_i \quad (6.23)$$

This can be approximated by using the Binomial expansion,

$$\begin{aligned} \Delta v_o &= -\frac{C_{11}}{C_{12}} (1 + \alpha_1 v_i + \alpha_2 v_i^2) (1 - \alpha_2 v_o - \alpha_2 v_o^2) \Delta v_i \\ &\approx -\frac{C_{11}}{C_{12}} (1 - \alpha_2 v_o - \alpha_2 v_o^2 + \alpha_1 v_i + \alpha_2 v_i^2) \Delta v_i \end{aligned} \quad (6.24)$$

as other cross-terms are negligible. Grouping some terms in the previous equation,

$$\Delta v_o = -\frac{C_{i1}}{C_{i2}} \left[1 + \alpha_1 (v_i - v_o) + \alpha_2 (v_i^2 - v_o^2) \right] \Delta v_i \quad (6.25)$$

Recall that

$$v_o = -\frac{C_{i1}}{C_{i2}} v_i \quad (6.26)$$

Substituting 6.26 into 6.25 yields

$$\Delta v_o = -\frac{C_{i1}}{C_{i2}} \left\{ 1 + \alpha_1 \left(v_i + \frac{C_{i1}}{C_{i2}} v_i \right) + \alpha_2 \left[v_i^2 - \left(\frac{C_{i1}}{C_{i2}} \right)^2 v_i^2 \right] \right\} \Delta v_i \quad (6.27)$$

Integrating

$$\int_0^{v_o} dV = -\frac{C_{i1}}{C_{i2}} \int_0^{v_i} \left\{ 1 + \alpha_1 \left(V + \frac{C_{i1}}{C_{i2}} V \right) + \alpha_2 \left[V^2 - \left(\frac{C_{i1}}{C_{i2}} \right)^2 V^2 \right] \right\} dV$$

results in

$$v_o = -\frac{C_{i1}}{C_{i2}} \left\{ v_i + \alpha_1 \left(\frac{v_i^2}{2} + \frac{C_{i1}}{C_{i2}} \frac{v_i^2}{2} \right) + \alpha_2 \left[\frac{v_i^3}{3} - \left(\frac{C_{i1}}{C_{i2}} \right)^2 \frac{v_i^3}{3} \right] \right\} \quad (6.28)$$

The nature of the error terms in equation 6.28 can be seen more clearly when considering a sinusoidal input.

Letting $v_i = V_i \sin(\omega t)$ and substituting trigonometric identities for $\sin^2(\omega t)$ and $\sin^3(\omega t)$ yields

$$v_0 = -\frac{C_{11}}{C_{12}} \left\{ V_i \sin(\omega t) + \frac{a_1}{2} \left[V_i^2 \sin^2(\omega t) + \frac{C_{11}}{C_{12}} V_i^2 \sin^2(\omega t) \right] + \right. \\ \left. \frac{a_2}{3} \left[V_i^3 \sin^3(\omega t) - \left(\frac{C_{11}}{C_{12}} \right)^2 V_i^3 \sin^3(\omega t) \right] \right\} \quad (6.29)$$

$$v_0 = -\frac{C_{11}}{C_{12}} \left\{ V_i \sin(\omega t) + \frac{a_1}{2} \left[\frac{V_i^2}{2} - \frac{V_i^2}{2} \cos(2\omega t) + \frac{C_{11}}{C_{12}} \left(\frac{V_i^2}{2} - \frac{V_i^2}{2} \cos(2\omega t) \right) \right] + \right. \\ \left. \frac{a_2}{3} \left(\frac{3}{4} V_i^3 \sin(\omega t) - \frac{1}{4} V_i^3 \sin(3\omega t) - \left(\frac{C_{11}}{C_{12}} \right)^2 \left[\frac{3}{4} V_i^3 \sin(\omega t) - \frac{1}{4} V_i^3 \sin(3\omega t) \right] \right) \right\} \quad (6.30)$$

v_0 may now be put in the form of

$$v_0 = A_0 + A_1 \sin(\omega t + \phi_1) + A_2 \sin(2\omega t + \phi_2) + A_3 \sin(3\omega t + \phi_3)$$

Expanding out and gathering like terms

$$v_0 = -\frac{C_{11}}{C_{12}} \left\{ \frac{a_1}{4} V_i^2 \left(1 + \frac{C_{11}}{C_{12}} \right) + \left[V_i + \frac{a_2}{4} V_i^3 \left(1 - \left(\frac{C_{11}}{C_{12}} \right)^2 \right) \right] \sin(\omega t + \phi_1) - \right. \\ \left. \left[\frac{a_1}{4} V_i^2 \left(1 + \frac{C_{11}}{C_{12}} \right) \right] \sin(2\omega t + \phi_2) - \left[\frac{a_2}{12} V_i^3 \left(1 - \left(\frac{C_{11}}{C_{12}} \right)^2 \right) \right] \sin(3\omega t + \phi_3) \right\} \quad (6.31)$$

As $\frac{a_2}{4} V_i^3 \left[1 - \left(\frac{C_{11}}{C_{12}} \right)^2 \right] \ll V_i$ in the $\sin(\omega t + \phi_1)$ term (the almost linear approximation)

equation 6.31 may be reduced to

$$v_o = -\frac{C_{11}}{C_{12}} \left\{ \frac{\alpha_1}{4} V_i^2 \left(1 + \frac{C_{11}}{C_{12}} \right) + V_i \sin(\omega t + \phi_1) - \left[\frac{\alpha_1}{4} V_i^2 \left(1 + \frac{C_{11}}{C_{12}} \right) \right] \sin(2\omega t + \phi_2) - \left[\frac{\alpha_2}{12} V_i^3 \left(1 - \left(\frac{C_{11}}{C_{12}} \right)^2 \right) \right] \sin(3\omega t + \phi_3) \right\} \quad (6.32)$$

The input-referred harmonics may now be obtained by looking at the amplitude of the frequency of interest relative to the fundamental frequency. Letting HD(2) be the second harmonic and HD(3) be the third harmonic,

the second harmonic is

$$HD(2) = \frac{\alpha_1}{4} V_i \left(1 + \frac{C_{11}}{C_{12}} \right) \quad (6.33)$$

which agrees with recent literature [12,16].

The third harmonic is

$$HD(3) = \frac{\alpha_2}{12} V_i^2 \left| 1 - \left(\frac{C_{11}}{C_{12}} \right)^2 \right| \quad (6.34)$$

It can be seen that the second harmonic is proportional to the fundamental amplitude and the third harmonic is proportional to the square of the fundamental amplitude as predicted by Lee et. al. [16].

It is interesting to note exactly what these equations dictate. Harmonic distortion emanating from capacitor nonlinearity as found at the output of the opamp may be modeled with the aid of Fig. 6.6. As seen, the nonlinear capacitors may be considered as linear but they are driven by harmonic generators, denoted $HD_{CAP}(2)$ and $HD_{CAP}(3)$. The feedback

capacitor contributes both second and third (even and odd order) harmonic distortion to the output of the opamp magnified by unity. The feedforward capacitor, however, contributes the second harmonic that is multiplied by the closed-loop gain of the opamp. This capacitor also contributes a third harmonic that is magnified by the square of the closed-loop gain. Note that their independent contributions to the total harmonic distortion at the output is superpositional.

From measured results, it should be possible to determine the voltage coefficients α_1 and α_2 , and hence the nonlinear error of capacitors should this be the major source of distortion, through

$$\alpha_1 = \frac{4HD(2)}{(1+G)v_i} \quad (6.35)$$

$$\alpha_2 = \frac{12HD(3)}{(G^2-1)v_i^2} \quad (6.36)$$

where $G = C_{11}/C_{12}$.

6.5 RESULTS AND DISCUSSION

For the capacitors used in the experiment, it would be very lenient to assign $\alpha_1 = 10 \text{ ppm/V}$ and $\alpha_2 = 2 \text{ pfm/V}^2$, from previous literature. This corresponds to approximately 16 bit resolution if a moderate peak voltage is employed. Substitution of these coefficients into equations 6.33 and 6.34 yields Table 6.1 for various input voltages. As can be seen from this table, it would take an extremely linear signal generator or oscillator to have a pure enough sinusoidal test signal with harmonics less than this magnitude. In addition, the dynamic range

required of the overall circuit must be very large. On the latter point, high-Q filter instrumentation such as a lock-in amplifier can measure a correlated signal buried in up to 60 dB of random noise [9]. However the instrument will not read a deep signal such as a -182 dB harmonic. In addition, the analysis proceeds under the assumption that the dominant source of nonlinearity comes from the nonlinear capacitors. In fact, the capacitors were so linear that other sources of nonlinearity, such as the nonideal opamp, dominated the results. This will be shown in the next chapter. Experimental results are superfluous in this chapter for the above reasons.

6.6 SUMMARY AND CONCLUSIONS

Historically, nonlinear capacitance has been important in the circuit design of low-distortion filters [26].

It was thought that nonlinear capacitance could be measured using a novel technique in a circuit context similar to their typical use in SC filters. In addition, this measurement technique would ultimately reduce chip size as compared to conventional C-V techniques, as the capacitor sizes under test can be any size as dictated by the bounds of technology and the needs of the application.

A review of the two most popular capacitor structures along with their theoretical voltage coefficient of capacitance was presented in an attempt to familiarize the reader with up to date technology.

By applying charge balance to the integrator involving an expression for nonlinear capacitance, the theoretical harmonic distortion as seen at the output of the opamp was found. The harmonic distortion from this source may be modeled by harmonic generators driving linear capacitors.

The excellent linearity of the capacitors used in the experiment made the measurement of the voltage coefficients of capacitance unfeasable since in the context used, there were other dominating sources of nonlinearity. These sources of nonlinearity will be the topic of discussion to follow, at which time the general trends of the measured results will be compared to the appropriate theoretical limits.

CHAPTER 7 OPAMP NONLINEARITY

7.1 INTRODUCTION

The objective of this chapter is to explore different aspects of filter distortion in a continuing attempt to link fundamental distortion mechanisms to some of the general trends as seen in the nonlinearity experiment. The implications of these distortion mechanisms ultimately place an upper limit on circuit design capabilities.

Although good design practice and good control of the process technology can eliminate some of the distortion, the nonideal nature of the basic building blocks of SC circuits will unavoidably cause inherent error.

7.1.1 THE BASIC SC FILTER BUILDING BLOCKS

Fundamental distortion mechanisms can only be minimized, never eliminated. Although there are many sources of distortion, two of them are truly fundamental. They are nonlinear distortion due to capacitor nonlinearity (as already discussed) and nonlinear distortion due to opamp nonlinearity. As shown in Fig. 7.1, the opamps used in the experiment are used both in the continuous-time domain (the voltage follower) and the sampled-data domain (the resettable SC integrator).

Capacitors were discussed in the last chapter and in conclusion, it was found that they generated no measureable contribution to overall nonlinearity. This was due to the equally and heavily doped poly-poly plates used and the plate's apparent similarity to metal in allowing the

Fig 7.1 SC Circuit Schematic.

capacitors to exhibit very linear behaviour.

The switches used are minimum size, complementary-pair transmission gates whose contribution to error due to charge dumping and clock feedthrough is minimized and is well understood [1,27]. The SC transients through the switch settle quickly and much before any other operation takes place. Hence, it is concluded that nonlinearity in the switches is relatively inconsequential at the clock rates used here.

Other mechanisms such as slew rate limiting of the opamp and unbalanced output stages may also cause time-dependent distortion [16]. This, however, is only important if the required amount of settling time is not adequate which is not the case in our experiments. It is therefore deemed proper to concentrate on opamp nonlinearity here.

7.2 DISTORTION CAUSED BY OPAMP GAIN NONLINEARITY (FINITE GAIN)

It is now appropriate to relate the open-loop distortion of the opamp, characterized in chapter 5, to the resulting distortion at the output of the closed-loop circuit.

An ideal opamp is considered to have infinite gain and as such would be perfectly linear, leading to no harmonic distortion. Real opamps, on the other hand, have finite gain and hence do not have the ability to keep the virtual ground pinned to analog ground. This gives rise to a difference-mode voltage v_d . This in turn introduces distortion in the circuit.

Consider the resettable integrator in Fig. 7.2 a)

Fig 7.2 a) Resettable SC integrator with nonideal virtual ground giving rise to difference-mode voltage, v_d .

Fig 7.2 b) Opamp nonlinearity is modeled by input-referred harmonic generators HD(2) & HD(3). In closed-loop, harmonic generation of the opamp is amplified by factors relating to the closed-loop gain.

When ϕ_1 on: $\Delta q_1(1) = \Delta q_2(1) = 0$

When ϕ_2 on: $\Delta q_1(2) = (\Delta v_i - \Delta v_d)C_1$ $\Delta q_2(2) = (\Delta v_o - \Delta v_d)C_2$

Note that the capacitances C_1 and C_2 are considered to be linear here.

Charge Balance requires that

$$(\Delta v_i - \Delta v_d)C_1 + (\Delta v_o - \Delta v_d)C_2 = 0$$

Rearranging yields

$$\Delta v_o = \Delta v_d \left(\frac{C_1 + C_2}{C_2} \right) - \Delta v_i \left(\frac{C_1}{C_2} \right) \quad (7.3)$$

It is evident from the $\Delta v_i C_1 / C_2$ term that even with finite gain ($a \neq 0$), the classic opamp gain for inverting (and noninverting) modes still holds.

Based on Section 5.3, we write for the imbedded opamp

$$\Delta v_o = a_1 \Delta v_d + a_2 \Delta v_d^2 + a_3 \Delta v_d^3 + \dots + a_n \Delta v_d^n \quad (7.4)$$

We are now going to bring this opamp into the closed-loop circuit context.

The linear output is just

$$\Delta v_o = a_1 \Delta v_d$$

so by Volterra theory, manipulation of equation 7.3 proceeds as

$$\begin{aligned}
\Delta v_o &= -\left(\frac{C_1}{C_2}\right)\Delta v_i + \left(\frac{C_1 + C_2}{C_2}\right)\frac{\Delta v_o}{a_1} \\
&= -\frac{C_1}{C_2}\Delta v_i + \left(\frac{C_1 + C_2}{C_2}\right)\frac{1}{a_1}[a_1\Delta v_d + a_2\Delta v_d^2 + a_3\Delta v_d^3] \\
&= -\frac{C_1}{C_2}\Delta v_i + \left(\frac{C_1 + C_2}{C_2}\right)\left[\Delta v_d + \frac{a_2}{a_1}\Delta v_d^2 + \frac{a_3}{a_1}\Delta v_d^3\right] \quad (7.5)
\end{aligned}$$

This gives a key insight that the opamp distortion can be considered as input referred to the opamp input, and then multiplied by the closed-loop circuit gain to get the output distortion. From equation 7.5, we would now like to extract equations relating the measured harmonic distortion to the opamp nonlinearity coefficients in equation 7.4. Combining $\Delta v_o = a_1\Delta v_d$ and $\Delta v_o = -C_1/C_2\Delta v_i$, we obtain

$$\Delta v_d = -\frac{1}{a_1}\frac{C_1}{C_2}\Delta v_i \quad (7.6)$$

Substitution of (7.6) into (7.5) yields

$$\Delta v_o = -\frac{C_1}{C_2}\Delta v_i + \left(\frac{C_1 + C_2}{C_2}\right)\left[-\frac{1}{a_1}\frac{C_1}{C_2}\Delta v_i + \frac{a_2}{a_1^3}\left(\frac{C_1}{C_2}\right)^2\Delta v_i^2 - \frac{a_3}{a_1^4}\left(\frac{C_1}{C_2}\right)^3\Delta v_i^3\right]$$

Rewriting and integrating

$$\begin{aligned}
v_o &= \int_0^{v_o} dV = \int_0^{v_i} \left[-\frac{C_1}{C_2} - \left(\frac{C_1 + C_2}{C_2}\right)\frac{1}{a_1}\frac{C_1}{C_2} + \frac{a_2}{a_1^3}\left(\frac{C_1 + C_2}{C_2}\right)\left(\frac{C_1}{C_2}\right)^2 2V - \frac{a_3}{a_1^4}\left(\frac{C_1 + C_2}{C_2}\right)\left(\frac{C_1}{C_2}\right)^3 3V^2 \right] dV \\
v_o &= -\frac{C_1}{C_2}v_i - \frac{1}{a_1}\left(\frac{C_1 + C_2}{C_2}\right)\frac{C_1}{C_2}v_i + \frac{a_2}{a_1^3}\left(\frac{C_1 + C_2}{C_2}\right)\left(\frac{C_1}{C_2}\right)^2 v_i^2 - \frac{a_3}{a_1^4}\left(\frac{C_1 + C_2}{C_2}\right)\left(\frac{C_1}{C_2}\right)^3 v_i^3 \quad (7.7)
\end{aligned}$$

By trigonometric identities in Chapter 5,

$$v_o = \frac{V_i^2 a_2}{2 a_1^3} \left(\frac{C_1 + C_2}{C_2} \right) \left(\frac{C_1}{C_2} \right)^2 - \left[\frac{C_1}{C_2} V_i + \frac{1}{a_1} \left(\frac{C_1 + C_2}{C_2} \right) \left(\frac{C_1}{C_2} \right) V_i + \frac{3 a_3}{4 a_1^4} \left(\frac{C_1}{C_2} \right)^3 \left(\frac{C_1 + C_2}{C_2} \right) V_i^2 \right] \sin(\omega t + \phi_1) \\ - \frac{1}{2} \frac{a_2}{a_1^3} \left(\frac{C_1 + C_2}{C_2} \right) \left(\frac{C_1}{C_2} \right)^2 V_i^2 \sin(2\omega t + \phi_2) - \frac{1}{4} \frac{a_3}{a_1^4} \left(\frac{C_1}{C_2} \right)^3 \left(\frac{C_1 + C_2}{C_2} \right) V_i^3 \sin(3\omega t + \phi_3) \quad (7.8)$$

The second and third harmonics are then easily found as

$$HD(2) \approx \frac{1}{2} \frac{a_2}{a_1^3} \left(\frac{C_1 + C_2}{C_2} \right) \left(\frac{C_1}{C_2} \right)^2 V_i^2 \quad (7.9)$$

$$HD(3) \approx \frac{1}{4} \frac{a_3}{a_1^4} \left(\frac{C_1 + C_2}{C_2} \right) \left(\frac{C_1}{C_2} \right)^3 V_i^3 \quad (7.10)$$

It is interesting to note exactly what equations 7.9 and 7.10 dictate.

From these equations, the opamp may be modeled to have input-referred harmonic generators that operate through to the output in a closed-loop, noninverting mode configuration as seen in Fig 7.2 b).

All external sources acting on the output aside, internal sources of second order harmonics (the a_2 coefficient) would be expected to be less significant when compared to the third order harmonic (the a_3 coefficient). The reason will be discussed in the next section.

A method to characterize opamp nonlinearity and predict harmonic distortion in any closed-loop situation now follows. Equations 7.9 and 7.10 require, by definition, the open-loop characteristic coefficients a_1 , a_2 , and a_3 . They may be acquired from the measured harmonic distortion as produced by the opamp in open-loop. However, it is intuitive from the relative nature of the different species of harmonic distortion in the opamp that there must exist an interrelationship

between their characteristic coefficients. This is to say that there exists a relationship between a_2 and a_1 as well as a_3 and a_1 . Furthermore, these relationships manifest themselves as constants under any loop-gain condition. More on this later.

Now, the open-loop characteristic coefficients, a_i , of the opamp were measured dynamically at low frequency. In Fig. 7.1, all circuit capacitors were placed in the forward loop and a low-frequency sine wave was applied at the output. In principle, the distortion of the opamp directly reflects its nonlinearity coefficients.

In practice, however, there was found to be a very small feedback capacitance even when the opamp was nominally open-loop, due to the parasitic metallization interconnect source-drain capacitance, C_{sd} , of the integrator reset switch. The action of this switch is easily seen in Fig. 7.3 a) and b) whose cause is outlined in the photomicrograph of Fig. 7.3 c). Assuming this capacitance is linear, it simply acts as a source of negative feedback by closing the loop slightly thus reducing the dynamic open-loop gain. The characteristic coefficients measured from this system is termed "pseudo" open-loop coefficients.

As stated earlier, the fact that the absolute values of the open-loop characteristic coefficients are not important but that their relative values are, is now proven. These pseudo open-loop characteristics are found as follows. As the pseudo open-loop gain is 40dB (as reduced by the parasitic feedback capacitance), a 10mV_{RMS} low frequency sinusoid is applied at the input of the integrator. The output is 1V_{RMS} and is equal to the coefficient b_1 from chapter 6. The measured harmonics were $HD(2)=-57\text{dB}$ and $HD(3)=-56\text{dB}$. By using equations 5.8, 5.9 and 5.10, the coefficients

a) Reset integrator

b) Gain of C_{FF}/C_{ds} .

Fig 7.3 a) Action of resettable integrator. All capacitors are put in the feedforward pack. In b), parasitic metallization capacitance C_{ds} interferes with the open-loop gain measurements.

Fig 7.3 c) Photomicrograph denoting how parasitic capacitance arises from line #1 running parallel to line #2 of the pass gate.

$$a_1 = 99.5$$

$$a_2 = 28$$

$$\text{and } a_3 = 6340$$

were found. It is found that a_2 is small compared to a_1 . This will be shown later to occur because the opamp static nonlinearity is dominated by the differential pair which demonstrates polar, odd symmetry.

The parameters a_1 and a_2 were substituted into equations 7.9 and 7.10 to yield the harmonic distortion due to nonlinear gain at different input voltages. The results are compared with the measured values in Fig. 7.4 a) and 7.4 b). As can be seen, there is a good correlation between the measurements and theory. It should be stressed that the ratios a_2/a_1^2 and a_3/a_1^3 , as found from equations 7.9 and 7.10, are constants under any loop-gain condition. This is confirmed by the measured second and third harmonics from the pseudo open-loop case (i.e. gain = $C_1/C_2 = 100$ and feedback factor = $(C_1 + C_2)/C_1 = 101$, etc.) when used with equations 7.9 and 7.10, solving to find the ratios a_2/a_1^2 and a_3/a_1^3 . It was found, as expected, that these constants were identical to the previous case. To further this, any closed-loop case (i.e. gain of 7) would yield the same constants.

In conclusion, by knowing the approximate open-loop gain (a_1), the characteristic coefficients of the opamp (a_2 and a_3) may be found. Then, the harmonic distortion of this opamp, as used in any loop-gain condition, may be theoretically found. This has novel consequences in circuit design in predicting harmonic distortion.

Harmonic Distortion Vs Voltage

Clock Freq. 200KHz Input Signal Freq. 1KHz

Harmonic (dB)

Fig 7.4a) Measured & Theoretical Second Harmonics.

Harmonic Distortion Vs Voltage

Clock Freq. 200KHz Input Signal Freq. 1KHz

Harmonic (dB)

Fig 7.4b) Measured & Theoretical Third Harmonics.

7.2.1 NONLINEARITY FROM THE COMMON SOURCE DIFFERENTIAL PAIR

Up to now, the opamp has been viewed primarily as a "black-box" without discussing the major source of nonlinearity internal to the opamp. Of course, odd and even order harmonic distortion must invariably manifest itself at the output since the input is driven through gain stages and subjected to bias disturbances. However, a major source of distortion to be considered internal to the opamp comes about from the CS differential input pair as shown in Fig. 7.5 a).

It is intuitive from the odd symmetry of the i_d versus v_d curve of Fig. 7.5 b) that only odd order harmonic distortion would be generated from this source. In addition, even order harmonic distortion possesses even order symmetry which stems from even order characteristics as manifested at the output. An example of this is the Class A output stage of the opamp, a well known source of dc offset and even order harmonics which contributes to the existence of the a_0 coefficient.

Although the resettable integrator operates in a different manner than the voltage follower, (Fig. 7.1), it must be acknowledged that the difference-mode voltage v_d operates the same in both and is in fact the same in amplitude for both, for the same output voltage amplitude.

The input referred harmonic distortion is modulated by the closed-loop gain due to the feedback capacitor in the resettable integrator. No such generation occurs in such magnitude in the voltage follower as the gain and feedback factor is unity. Thus, the distortion emanating from the SC integrator is considerably larger than that produced for the same difference-mode voltage v_d in the voltage follower since it has higher closed-loop gain and feedback factor. The effects of the voltage follower are thus considered to be negligible.

Fig 7.5a) Common Source Differential Pair.

Fig 7.5b) Linear region of operation is encompassed on i_D vs v_D curve of CS differential pair.

7.3 INFLUENCE ON HARMONIC DISTORTION DUE TO TIME DEPENDENT EFFECTS

It would be premature to conclude the study of distortion without mentioning time dependent effects. In the previous analysis, we have studied harmonic distortion as a function of voltage at low enough frequencies that time dependent effects were not significant. We have been able to show an adequate link between theory and experiment at such low frequencies. However, there are time dependent effects which come in at high frequency, such as slew rate limiting, charge transfer transients and settling time requirements. It would be possible to generalize the analysis given here to cover such effects, but an attempt to explain these effects quantitatively was not within the scope of this thesis. However, an underlying qualitative understanding is in order. Fig. 7.6 a) and Fig. 7.6 b) depict the measured harmonic distortion as a function of frequency. These graphs depict two cases. The first depicts the results from a lightly loaded integrator and the second case shows the results from a heavily loaded integrator, in an attempt to induce slew rate limiting, as will be discussed.

7.3.1 INFLUENCE ON HARMONIC DISTORTION DUE TO SLEW RATE LIMITING

The ability of a circuit to supply charging current to capacitive loads is governed by slew rate. If the rate of change of voltage at the input is greater than the finite slew rate offered by the circuit, then slew rate limiting occurs, as demonstrated in Fig. 7.7 a) and b).

As can be seen from measurements in Fig. 7.6 a) and b), when slew

Harmonic Distortion Vs Frequency

Clock Freq. 200KHz Input Voltage .05 v [RMS]
Harmonic (dB)

Fig 7.6a) Measured Second Harmonics Vs Frequency.

Harmonic Distortion Vs Frequency

Clock Freq. 200KHz Input Voltage .05 v [RMS]
Harmonic (dB)

Fig 7.6b) Measured Third Harmonics Vs Frequency.

Fig 7.7 The effects of finite slew rate.

Fig 7.8 Linear rise times are the result, as shown, in sampled-data systems when clock frequency is too high.

rate limiting is not evident, harmonic distortion is nearly independent of signal frequency. Nevertheless, whenever the circuit is subject to conditions conducive to slew-induced distortion, a substantial increase in third (and odd) order harmonic distortion is evident. In addition, second (and even) order harmonic distortion does not change comparatively under these circumstances. This agrees with what has been reported in recent literature which states that even order harmonics can be generated if imbalances in the output stage exist. This will only occur under slew rate limited conditions [16,26]. As a class A output stage was used in the opamp of interest, and the current travelling in the branches of the CS differential pair was mirrored, no such imbalance would exist and hence under slew-induced conditions, no difference in 2nd order harmonic distortion would be expected, as seen in Fig. 7.6 a).

7.3.1.1 THE CS DIFFERENTIAL INPUT PAIR - TIME DEPENDENT AND SLEW RATE LIMITING EFFECTS

The CS differential pair was studied extensively as a source of harmonic distortion. The differential pair behaves comparatively linearly at small voltages. In most cases, such as the SC integrator, the large loop gain confines the differential voltage on the input transistors to be small as demonstrated in Fig. 7.5 b).

However, opamps often become initially slew rate limited during a charge transfer due to the nature of sampled data, as capacitors with large voltages across them are often switched across the differential pair. When this input signal is too large, the input is said to be overdriven. When the rise time of an input is faster than the slew rate of the differential pair, slew-induced distortion is the consequence. As a result, nonlinear amplification takes place and the opamp output

swing starts to become slew rate limited as the output can no longer follow the input. This offers a partial explanation to frequency dependent effect [28,29].

Furthermore, if the clock period is too small for the transient to settle, distortion will ensue. This is best explained with the aid of Fig. 7.8 which demonstrates how a resettable SC integrator, affected by slew rate limiting during integration, performs under inadequate settling time. It is evident that a linear voltage rise time, characteristic of slew-induced distortion, occurs as opposed to an exponential voltage waveform indicative of normal operation [16]. It therefore follows that harmonic distortion can be expected to worsen as the sampling frequency increases due to improper settling time, should the slew rate be limited. As long as there is enough time for the transient to settle out, this should not be a problem. Interestingly though, it has been reported that when operating at high speeds with successive approximation ADC architectures, the settling time when switching to the MSB is often insufficient [30]. Furthermore, incomplete charge transfer can be due to nonzero $R_{ON}C$ time constants at the higher circuit speeds [31].

7.3.2 TIME DEPENDENT EFFECTS OF THE VIRTUAL GROUND AND THE EFFECTS OF NEGATIVE FEEDBACK AT HIGHER FREQUENCIES

When operating the opamp at frequencies beyond the open-loop roll-off (dominant pole) frequency, time dependent effects will be present as well as the non-time dependent effects studied previously.

It is well known that the precision provided by opamps is achieved through the use of negative feedback. In fact, it is the phase shift in the loop and the high loop gain that is responsible for reducing distortion. The phase inversion of the negative feedback produces a

stabilizing 180° phase shift; however, an additional 180° can be developed in the various stages of the opamp thus leading to instability and oscillations [29].

It is also intuitive that at higher frequencies, there will be a reduction in phase margin and so the feedback signal does not, in fact retain its perfect inversion with respect to the input phase. As well, there is a reduction in loop gain. This is significant when considering the operation of the virtual ground. When operating at frequencies beyond the open-loop roll-off frequency, larger excursions of the virtual ground are required to keep the output voltage constant with increasing frequency (in a closed-loop constant gain situation). As discussed previously, the harmonic distortion would be expected to rise due to the nonlinearity of the CS differential pair.

As the measurements were confined to relatively low frequencies relative to the closed-loop cut-off frequency ($\sim 2\text{MHz}$), neither feedback or larger virtual ground voltages are expected to contribute significantly to larger distortion. It is believed that the primary source of distortion as seen in the results where capacitive loading was increased come about from the heavy loading of the opamp. This disfigured output, when fed back to the inverting terminal of the opamp, corrupts the virtual ground as there is insufficient charging current. This causes the large increase in harmonic distortion. In conclusion, it can be seen that as the input signal frequency increases and approaches the upper frequency edge as defined by the Full-Power Bandwidth or slew rate limit specification, harmonic distortion increases. The output of the opamp yields more nonlinear gain as witnessed by the corrupted virtual ground through feedback. Longer settling times and the use of a higher slew rated opamps are required to help correct for this.

7.4 SUMMARY AND CONCLUSIONS

An attempt to link fundamental distortion mechanisms with observed data was made. In order to understand the trends offered by the data, the basic building blocks found in most SC circuits were studied. This was done to demonstrate two fundamental sources of distortion, namely capacitor nonlinearity and opamp gain nonlinearity, including the contribution to nonlinearity from the CS differential pair. In addition, the effects of slew rate limiting and secondary sources of distortion were reported.

Capacitor nonlinearity, although not significant in the case at hand, can in fact be a major concern depending on the structure and process used. Opamp gain nonlinearity, being the greatest low-frequency contributor, was studied theoretically and found to correlate well with measurements.

Opamp nonlinearity comes about primarily from the finite gain of the opamp which gives rise to a difference-mode voltage at the input and a gain error at the output. By solving a charge balance equation for the integrator and by allowing the existence of a nonideal virtual ground, the harmonic distortion found at the output of the circuit was theoretically predicted. From these equations, the opamp may be modeled to have input-referred harmonic generators that operate in close-loop in a noninverting mode configuration. The ability to predict harmonic distortion in any closed-loop opamp configuration is feasible once the opamp is characterized. The novel technique of characterizing the opamp in closed-loop form was presented.

As seen in section 5.5, this voltage error is easily converted to the number of bits resolved through the use of equation 5.22. In the case at hand, a moderate voltage swing of $3 V_{pp}$ will degrade the circuit

accuracy to approximately 10 bits. At lower voltages, the accuracy improves considerably due to the more linear region of operation. Slew rate limiting plays an important role at higher frequency if proper design procedures are not followed.

It is the combined effect of all these sources of distortion which would lead to the shape of the trends observed. What has been observed in Fig. 7.4 a) and b) is not straight forward as there are inflection points, peaks and valleys in the data. The effect of phase, superpositional effects and an entire host of other possibilities responsible for these deviations would be a subject for further study.

CHAPTER 8 CONCLUSIONS AND RECOMMENDATIONS

8.1 SUMMARY AND CONCLUSIONS

In chapter 1, a general introduction to the thesis was provided. A major objective of this thesis was to study the implementation of a novel SC circuit technique capable of measuring capacitor mismatch among small capacitors. This could not previously be measured, with any amount of accuracy or precision, due to the limited resolution of existing commercial equipment, as well as problems caused by both on-chip and off-chip parasitic capacitance.

Chapter 2 initially laid the circuit ground work and then provided the reader with an in-depth principle of circuit operation used to determine mismatch. In discussing an n-capacitor array, a mathematical algorithm to extract the mismatch error was derived. From this, the resolution of this measurement technique was found. Aliased broadband thermal noise from switched-capacitors dictated the resolution of the measurement. Eight test capacitors were laid out to test for systematic variations across a die.

In chapter 3, the experiment was discussed in great detail. Upon running the experiment for the first time, spurious digital feedthroughs were postulated to be the cause of inaccurate data acquisition. Upon the elimination of this effect, the resulting mismatch errors beared witness to an unreasonable systematic offset, particularly in capacitor C_1 . Upon re-examination of the layout, this offset was due to the effects of added capacitance due to interconnect metallization. In greater detail, the top and bottom plate of capacitor C_1 had interconnect metallization that ran parallel to each other for a short distance. This effectively added capacitance to C_1 and upset the average array capacitance. The effect of this added capacitance was

formally subtracted and its effect eliminated.

After the above corrections, the results were very random as expected. Furthermore, no systematic variations were found. The average mismatch for these capacitors (1/3pf nominally) was .08% with $\sigma = .103\%$.

In chapter 4, the causes of capacitor mismatch were considered. With the indispensable help of SEM photomicrographs, precious insight was ascertained, dispelling some of the older theories of the significant causes of mismatch. From the SEM photomicrographs, it was seen that the edge definition of the top plate was quite clean. This is due to modern plasma etching and process control. The major cause of mismatch is assumed to come about from the surface roughness of the poly plates. Oxide undulations between the poly plates also give rise to mismatch for several reasons. Firstly, different poly grain types yield different oxide growth rates. In addition, compressed oxide is found at the outer bounds of large asperities where they meet the plate floor. Also, the additional surface area imparted to the top plate due to these undulations effectively increases or decreases the value of capacitance when compared to an average capacitor with an average asperitie density. The issue of surface roughness was addressed and suggested improvements made.

As a second objective of this thesis, the ability to study nonlinearity with this circuit has proven very useful. Two possibly significant sources of harmonic distortion in circuits are known to be capacitor and opamp nonlinearity. The ability to theoretically predict the harmonic distortion due to these sources and relate this to measurements has given considerable insight.

A fundamental understanding of nonlinear distortion in both a qualitative and quantitative manner was the main concern of chapter 5. Both capacitor and opamp nonlinearity were introduced as sources of distortion and the manner in which they give rise to voltage errors in

circuits was covered. By applying a low-frequency sine wave to the input of the SC circuit used in the mismatch circuit, harmonic distortion at the output may be measured and related back to either nonlinear source.

In chapter 6, capacitor nonlinearity is studied in depth. A review of two popular capacitor structures used in industry today was presented. Solving the charge balance equation for the opamp, and using an expression for nonlinear capacitance, would allow the theoretical prediction of harmonic distortion that would be seen at the output of this circuit. This also led to modeling linear capacitors with harmonic generators so as to predict the harmonic distortion at the output of the opamp due to this source of nonlinearity. Should the measured harmonic distortion be predominantly due to capacitor nonlinearity, the technique of finding the voltage coefficient of capacitance from the measured harmonics is deemed feasible. However, as the poly plates of the capacitors under test were so heavily doped, they in fact were found to be extremely linear in nature. As such, they would generate relatively little harmonic distortion.

The dominating source of nonlinearity was found to come about from opamp nonlinearity, as discussed in chapter 7. Opamp nonlinearity has an effect due to the finite gain of the opamp, which gives rise to a difference-mode voltage at the input of the opamp. By solving the charge balance equation for the integrator with finite gain, the ability to predict the harmonic distortion at the output of the circuit is proven by demonstrating a high degree of correlation between theory and measurements. Furthermore, a novel technique to characterize the linearity of the opamp in closed-loop form was presented. In the same manner, a logical extension of this implies that the harmonic distortion in any closed-loop opamp configuration should theoretically be predictable. With the opamp used in this experiment, a moderate voltage

excursion was found to degrade the circuit accuracy to approximately 10 bits for a 3V_{DD} output swing, due to opamp nonlinearity.

Finally, chapter 8 summarizes and concludes the thesis.

8.2 SUGGESTIONS FOR FURTHER WORK

In the discussion of offsets in the acquired data (chapter 3) due to spurious digital feedthroughs, the circuit's sensitivity was obviously enough to be able to detect and register the effects of digital-substrate interactions. Although a nuisance in this case, the ability to study such interactions might prove useful by using the same principles offered by this circuit technique. In the thesis work here, these digital-substrate interactions might, for the most part, have been avoided by shielding the virtual ground from the substrate.

In the same line of thought, the ability to detect the effects of stray added capacitance from interconnect metallization gives rise on thoughts on how to study the placement of interconnect metallization. This also has implications where transmission gate layout, ADC layout, and so on is concerned.

On a different note, to extend the capabilities of this circuit to measure very small capacitances of say intrinsic transistor capacitances is easily done. Such an experiment would allow a study into short- and narrow-channel capacitive effects for use in modeling very small transistor behaviour.

APPENDIX A

Typical data from capacitor mismatch experiment.

Fig A.1 **Data $D(i,j)$ and Phase $P(i,j)$ Matrices.**

Fig A.2 **Offset $N(i,j)$ and Phase $N_p(i,j)$ Matrices.**

Fig A.3 **Resultant $R_d(i,j)$ and Phase $R_p(i,j)$ Matrices.**

Fig A.4 **Final Errors.**

```

##### Disk # 9 DATA FILE 21 NOISE FILE 19 #####
0 .000691 -.00519 .00699 -.000594 .000478 .000451 -.0051
-.000757 0 -.00596 .00618 -.001325 -.000302 -.000293 -.00589
.00508 .00567 0 .01172 .00434 .00539 .00533 3.86E-5
-.0071 -.00611 -.01182 0 -.00749 -.00639 -.00627 -.01176
.000512 .001344 -.00467 .00761 0 .000993 .000999 -.00447
-.000507 .0002096 -.00568 .00651 -.001072 0 -3.54E-5 -.0056
-.000521 .0001896 -.00576 .00649 -.001096 -6.64E-5 0 -.00559
.005 .00556 -.0001237 .01193 .00418 .0053 .00524 0
##### D-v-Phase #####
0 88.3 -90.1 88.7 -86.5 86.9 86.9 -90.6
-87.7 0 -90.6 88.6 -87.4 -85 -85 -90.3
89.1 89.7 0 89.5 89.2 89.5 89.5 71.7
-90.3 -89.6 -90.1 0 -89.9 -89.7 -90 -90
88.6 90.2 -90.7 89 0 90.1 89.9 -90.7
-87.2 83.5 -90.9 88.3 -86.9 0 -52.1 -90.4
-87 82.7 -90.2 89.1 -86.9 -72.9 0 -90.6
88.8 89.1 -74.6 90 89.4 89.4 89.4 0
#####
Analysis in progress
E( 3 )= .00652003484182
E( 8 )= .00643633162146
E( 5 )= .000402289166041
E( 1 )= -.000394652960991
E( 7 )= -.00110270271924
E( 6 )= -.00107163724869
E( 2 )= -.001448622808
E( 4 )= -.00988194353511
Sum of errors = -.000540903642709
Coverage= .00180937275407 (Average capacitive error)

```

Fig A.1 Data D(i,j) and Phase P(i,j) Matrices.

```

#####
Q2 Offset
** *****
0 -9.05E-6 -1.522E-5 -8.63E-5 -.0001583 -.0001483 -.0001576 -4.79E-5
-6.52E-5 0 -6.52E-5 -8.42E-5 -.0001928 -.0001863 -.0001966 -.0001423
-7.35E-5 -5.63E-5 0 -7.8E-5 -.0001912 -.0001832 -.0001913 -.0001473
-1.488E-5 2.081E-5 1.557E-5 0 -.0001373 -.0001269 -.0001291 -2.266E-5
6.06E-5 7.08E-5 7.73E-5 1.541E-5 0 -6.74E-5 -6.9E-5 5.67E-5
4.98E-5 6.42E-5 7.71E-5 1.697E-5 -6.11E-5 0 -6.92E-5 5.8E-5
6.16E-5 8.08E-5 9.42E-5 6.74E-5 -3.493E-5 -3.808E-5 0 7.07E-5
-6.09E-5 -2.073E-5 -2.323E-5 -9.52E-5 -.0001668 -.0001586 -.0001668 0
#####
Offset Phase
*****
0 -76.1 -89.1 -90 -86.8 -87 -87.2 -92.4
-88 0 -86.9 -88.9 -86.9 -87 -87.1 -87.9
-84.7 -84 0 -86.7 -86.4 -86.4 -86.6 -87
-62.1 70.6 72.4 0 -85.1 -85 -85.1 -87.9
87.5 89.2 90.1 95.9 0 -86.4 -86.7 94.9
90.3 89.1 90.3 95.9 -86.3 0 -87.2 95
90.3 89.2 90 91.2 -84.7 -85.2 0 93.7
-79.7 -69.2 -73.7 -86.4 -85.3 -85 -85.2 0
#####

```

Fig A.2 Offset N(i,j) and Phase Np(i,j) Matrices.

Data Disk #9 Data File 21 Noise File 19

```

0      .00070 -.00517 .00708 -.00044 .00063 .00061 -.00505
-.00069 0      -.00589 .00626 -.00113 -.00012 -9.6E-5 -.00574
.00515 .00573 0      .0117 .00453 .00557 .00552 .000186
-.00708 -.00613 -.0118 0      -.00737 -.00626 -.00614 -.0117
.00045 .00127 -.00475 .00759 0      .00106 .00107 -.00453
-.00055 .00015 -.00576 .00649 -.00101 0      3.4E-5 -.00566
-.00058 .00010 -.00585 .00643 -.00106 -2.8E-5 0      -.00566
.00506 .00558 -.00010 .0120 .00435 .00546 .0054 0

#####Rd-^ v~Rp #####
0      88.3      -90.1      88.7      -86.5      86.9      86.9      -90.6
-87.7      0      -90.6      88.6      -87.4      -85      -85      -90.3
89.1      89.7      0      89.5      89.2      89.5      89.5      71.7
-90.3      -89.6      -90.1      0      -89.9      -89.7      -90      -90
88.6      90.2      -90.7      89      0      90.1      89.9      -90.7
-87.2      83.5      -90.9      88.3      -86.9      0      52.1      -90.4
-87      82.7      -90.2      89.1      -86.9      -72.9      0      -90.6
88.8      89.1      -74.6      90      89.4      89.4      89.4      0
#####
Analysis in progress
E( 3 )= .0066798397875
E( 8 )= .00655647342391
E( 5 )= .000377226793967
E( 1 )= -.000286588511026
E( 6 )= -.00109520014778
E( 7 )= -.00115419330279
E( 2 )= -.00128676997096
E( 4 )= -.00981348495683

```

Fig A.3 Resultant Rd(i,j) and Phase Rp(i,j) Matrices.

```

#####
Y42A-E-128 file #A/ 15
#####
E( 3 )= .00759068394818
E( 5 )= .00120317861701
E( 8 )= .000756295995318
E( 1 )= .000536542869056
E( 6 )= -.000278736035968
E( 7 )= -.000307576221531
E( 2 )= -.000446059136166
E( 4 )= -.00905942355287
***** Data (1,1) ->(8,8)SUM=-5.09351697209E-6 Cav= .000588064812507

```

Fig A.4 Final Errors.

APPENDIX B MOS CAPACITOR STRUCTURES

B.1: METAL- OR POLYSILICON-OVER-DIFFUSION STRUCTURE (Poly/Metal - Substrate Structure)

This structure is formed by thermally growing a thin layer of SiO_2 over a heavily doped (say n^+) region as shown in Fig. B.1. This heavily doped region acts as the bottom plate of the capacitor, and the metal or polysilicon deposition serves as the top plate. Ideally, the top and bottom plates would be considered as perfect conductors and the capacitance should be governed by

$$C_o = \frac{\epsilon_{ox} A}{t_{ox}} \quad (B.1)$$

If $V_s > V_A$, this is in fact the case. However, if $V_s < V_A$, the electrons will be repelled (and holes attracted) under the thin oxide in the n^+ region causing a depletion region as seen in Fig. B.2. The capacitance of the structure is now modelled by a series connection of the oxide capacitance C_o and the depletion capacitance C_d . As the width of the depletion layer depends on the applied voltage, it can easily be seen that C_d is a voltage-variable capacitor. The total capacitance is now governed by

$$C = \frac{C_o C_d}{C_o + C_d} = C_o \left[\frac{1 + 2K_{ox}^2 \epsilon_o (V_A - V_s)}{q N_D K_s t_{ox}^2} \right]^{-\frac{1}{2}} \left[\frac{F}{cm^2} \right] \quad (B.2)$$

P- Substrate

Fig B.1 Metal (or Poly) - Diffusion Structure

P- Substrate

Fig B.2 $V_B < V_A$ causing a depletion region.

where N_D is the doping density of the n^+ region, and κ_s and κ_{SiO_2} are the relative permittivity of silicon and SiO_2 respectively. As depicted in Fig. B.3, the total capacitance decreases with increasing $(V_s - V_t)$ when V_s is less than V_t . When $(V_s - V_t)$ reaches the threshold voltage V_T , strong inversion occurs. At low frequency, a further increase in $(V_s - V_t)$ will cause an increase in total capacitance as the p^+ inversion layer builds. At high frequency, a further increase in $(V_s - V_t)$ will continue to degrade the total capacitance as the minority carriers (holes) will not have the time required to build and dissolve the inversion layer. For the high doping density used, V_T will be very large and it is unlikely that $(V_s - V_t)$ will ever reach this point. Also the voltage dependence of the total capacitance can be slight to moderate depending on the n^+ region doping for values of $(V_s - V_t) \ll V_T$.

B.2: POLYSILICON-OXIDE-POLYSILICON STRUCTURE

(Poly-Poly Structure)

This structure is shown in Fig. B.4 and is often offered in "double-poly" processes. Here, two layers of polysilicon are used as the top and bottom plates of the capacitor. The basic advantage of the poly-poly over the poly-substrate structure is the difference in the unavoidable parasitic effects. In the poly-substrate capacitor, where the bottom plate is an implanted layer in the substrate, a stray capacitance from the reverse-biased p-n junction can range from 15% to 30% of the capacitor. For poly-poly structures, the bottom plate parasitic capacitance is typically 5% to 20% of the capacitor, depending on the field oxide thickness under the bottom plate [1].

Fig B.3 Variation of capacitance with applied voltage.

P- Substrate

Fig B.4 An example of a Poly-Poly structure

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