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**DESIGN AND IMPLEMENTATION OF THE ANALOG
SIGNAL PROCESSING CIRCUITS FOR A SINGLE
CHIP MIXED ANALOG/DIGITAL MOBILE RADIO
BASEBAND DATA DEMODULATOR**

by

Angelo Petta

**A thesis submitted to the Faculty of Graduate Studies and
Research in partial fulfillment of the requirements for
the degree of Master of Engineering**

**Departments of Electronics
Faculty of Engineering
Carleton University
Ottawa Ontario
Canada**

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the requirements for the degree of Master of Engineering

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January 1990

Abstract

This thesis reports the results of a design and implementation of a mixed analog/digital baseband data demodulator for narrow-band digital FM radio receiver. It also documents work done on the system level demodulator optimization, a simulation environment created to facilitate such an optimization as well as the design of a library of CMOS standard cells and adopted IC design methodology.

The design has been verified at the system level by means of behavioural modelling with its parameters optimized to achieve satisfactory bit-error-rate (BER).

A set of digital and some analog standard cells (Carleton University standard cell library) was created, verified by simulation, and characterized after fabrication in 3-micron double metal CMOS process (through Canadian Microelectronics Corporation at Northern Telecom).

Originally there were two chips implemented; one containing the analog blocks and the other the digital portions. This would allow functionality of the building blocks to be verified. The fabricated chips were tested to be fully functional and closely agreed with simulated results. Finally the analog/digital baseband data demodulator was implemented onto a single chip. The chip area was approximately 4.0 mm x 1.1 mm.

Due to the complexity of the system and the substantial number of design hours, this project was undertaken by a 2-man team. This thesis concentrates on the design of the analog signal processing elements whereas my fellow colleague [8] was responsible for the design of the digital portion.

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Credit is also due to the entire staff of the Department of Electronics for all their support.

Finally, I would like to dedicate this thesis to my family for if it was not for their love and support this would not have been possible.

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Chapter 1

Introduction

1.1 Motivation

For many years, data has been transmitted over radio. In the last decade or so, data communication has become important in the field of mobile radio. A digital format is used to achieve high speed transmission and the reported modulation technique suitable for mobile radio channels is digital FM [1], [2], [3], [4], [5].

Due to this growing interest in telecommunication, a demand for silicon implementation of these systems has evolved. With the developments in circuit design techniques, it is possible to realize systems which require analog and digital circuitry on the same chip, which is particularly suitable for telecommunication applications. Here in Canada, university research in VLSI circuits for telecommunication is sponsored by ,amongst others, TRIO, CMC , and by NSERC.

One area of ongoing research in telecommunication at Carleton University is in Mobile Communication. It is being headed in a joint effort by the department of Systems and Computer Engineering and the department of Electronics.

1.2 Objective

The primary objective was to design a baseband data demodulator (BDD) integrated circuit used for mobile radio application. To achieve a high first time success rate a hierarchical design methodology was chosen. A semi-custom standard cell library was developed/fabricated/tested to support the IC design methodology.

In order to verify functionality and evaluate system performance to obtain a satisfactory bit-error-rate (BER) a high level simulator was used. This simulator is a modified version of SPLICE (CUSPLICE) [14] which allows additional models to be defined by the user. The models developed for the system simulations, which also included the noisy input signal to the BDD, were based upon the theoretical analysis of the system.

It was decided early in the system design stage that a mixed analog/digital system could best satisfy two of the most important factors that should be considered in IC mobile radio systems. These two factors were power consumption and physical area [6], [7].

The analog circuits were designed using switched-capacitor (SC) techniques and analyzed using the simulator SPICE [33]. Noise models for SPICE were also developed to analyze the noise found in switched-capacitor networks. From the noise analysis, the designer can gain some insight to design better performance circuits.

In laying out SC circuits with previously untested circuitry and/or fabrication process, it is useful practice to include test circuits. Two test chips were designed; one including only the analog portions and the other the digital circuitry. After verifying functionality and performance of the test chips, the BDD system was implemented.

The task of such a project was taken on by a two-man team. I was responsible for the analog designs and my partner/colleague's responsibility was the design of the digital circuits.

1.3 Thesis Format

The actual research covered many topics and in order to ensure coherence of the material presented, several topics are reported in the appendices. Appendix A describes the IC design methodology chosen for implementing the system onto silicon. It also includes the development of the standard cell library which was chosen to support the IC design methodology. Some of the primitive cells developed were integrated and the measured characteristic results of these cells are reported in Appendix B. In Appendix C, some examples of time domain simulation models development for the SPLICE simulator are described. The SPLICE model listing of the baseband data demodulator are also included in this appendix. The synthesis of a SC low-pass filter design is given in Appendix D. Also, results from the SPICE analysis of the filters reported in this thesis is given in Appendix D.

In Chapter 2, the problem specifications are defined and a system design which meets these specifications is described. Various implementation options were considered and a mixed analog/digital design is proposed. High level simulations is the method used to verify the functionality and optimize performance of the design. A comparison between high level system performance results and theoretical results from a literature proved to be

satisfactory.

The next chapter describes the circuit design, implementation of test circuits and the baseband data demodulator. The circuit design section deals with the synthesis of the analog signal processing elements using switched-capacitor techniques to meet the specifications defined by the system performance analysis. The origin of the noise generated in switched-capacitor networks is also considered and noise models suitable for SPICE were developed to determine the dominant noise sources. Practical considerations for MOS implementation is addressed and taken into account in the layout of the test circuits and layouts.

The performance of the fabricated chip which consists of the analog elements is reported in chapter 4. A comparison is also made with the simulated expectations.

Finally, chapter 5 summarizes the achievements of this thesis and includes some discussions on the future research and applications of the baseband system.

Chapter 2

System Design

2.1 Introduction

The problem specification of the overall system (mobile radio) , which is the first phase of the IC design cycle described in full in Appendix A, is outlined at the beginning of this chapter. An analytical description of the overall system is also included. The next phase of the IC design cycle is the design of the system which in this case consists of many subsystems. The focus of this chapter is the design of one of the subsystems, in particular, the baseband data demodulator (BDD) for a mobile radio receiver.

Different implementation options are considered namely completely analog, completely digital or mixed analog/digital circuitry in order to satisfy the requirements. The choice is greatly influenced by the dominant mobile radio system requirements, power consumption and physical area. A mixed analog/digital design is proposed.

Before committing a circuit design to silicon, a designer normally wants some assurance that the design is valid and the circuit functionality verified. One way of checking this is to construct and perform measurements on a laboratory prototype built up of discrete components. There are several limitations with this approach, they are; (i) time consuming and costly to build, debug and test complex circuits in the lab, (ii) frequently impossible to duplicate the characteristics of integrated circuit (IC) devices with discrete transistors. For these reasons, computer simulations have been chosen as the method of verifying the IC designs.

Finally, the performance of the system, based upon simulated results, is compared with theoretical results from literature guaranteeing satisfactory performance.

2.2 Mobile Receiver Description

The transmit and receive channels of the cellular mobile telephone data receivers are in the 900 MHz bands. The binary coded data messages are transmitted at 16kb/s rate

using Manchester coding.

Since the transmission for mobile radio channels is confined to a restricted bandwidth, many methods of spectrum shifting have been reported in literature. An investigation of various modulation techniques, in order to determine the most suitable for digital mobile radio communication, has been on going for many years. Narrow-band digital FM transmission techniques, such as Tamed FM (TFM) [1], [2] and Gaussian baseband filtered minimum shift keying GMSK [3] have been reported to be applicable to mobile radio transmission [4], [5]. This type of digital FM has the following features; (i) constant envelope, (ii) narrow-band spectrum, and (iii) good bit error rate performance. Therefore this type of modulation technique is considered suitable for a mobile radio channel since the transmitted power and the channel bandwidth (which are two primary communication resources) are efficiently utilized.

2.3 Narrow-Band Digital FM System Model

2.3.1 System Model

A block diagram representation of a narrow-band digital FM system is shown in Fig. 2.1.

Figure 2-1: Narrow-Band Digital FM Radio System

The signal $d(t)$ represents NRZ data stream of amplitudes ± 1 corresponding to data "0" and "1", with a bit duration of T . The coded signal $m(t)$ is the Manchester format equivalent of the NRZ.

The signal $s(t)$ at the input of the receiver IF filter can be written as

$$s(t) = \sqrt{2P} \cos(\omega_o t + \theta(t)) + \zeta(t) \quad (2.1)$$

where P is the signal power, $\omega_o = 2\pi f_o$ is the center IF filter radian frequency, $\zeta(t)$ is the white Gaussian noise of one-sided spectral density N_o , and $\theta(t)$ is the data phase after FM modulation given by

$$\theta(t) = 2\pi f_d \int_{-\infty}^t m(t) dt \quad (2.2)$$

where f_d is the frequency deviation. The IF filter is defined by its frequency response $H(f)$ and the corresponding impulse response $h(t)$.

The output $y(t)$ of the bandpass limiter following the IF filter can be expressed as

$$y(t) = \cos[\omega_o + \phi(t) + \eta(t)] \quad (2.3)$$

where $\phi(t)$ is the filtered signal phase which is expressed as

$$\phi(t) = \tan^{-1} \frac{\int_{-\infty}^t h(t-\tau) \sin \theta(\tau) d\tau}{\int_{-\infty}^t h(t-\tau) \cos \theta(\tau) d\tau} \quad (2.4)$$

and $\eta(t)$ is the phase noise

$$\eta(t) = \tan^{-1} \frac{\xi(t)}{\sqrt{2\rho(t)} + \vartheta(t)} \quad (2.5)$$

where $\xi(t)$ and $\vartheta(t)$ are independent Gaussian variables with zero means and unit variance and $\rho(t)$ is the time varying signal-to-noise ratio (SNR) given by

$$\rho(t) = \frac{E_b}{N_o T} \frac{a^2(t)}{\int_{-\infty}^{\infty} |H(f)|^2 df} \quad (2.6)$$

where $E_b = ST$ is the signal bit energy and $a(t)$ is the filtered normalized signal amplitude whose square is expressed as

$$a^2(t) = \left(\int_{-\infty}^t h(t-\tau) \sin \theta(\tau) d\tau \right)^2 + \left(\int_{-\infty}^t h(t-\tau) \cos \theta(\tau) d\tau \right)^2 \quad (2.7)$$

The probability density function of the phase noise is given by [10]

$$p(\eta) = \int_0^{\infty} \frac{x}{\pi} e^{-x^2 - \rho(t) - 2x\sqrt{\rho(t)} \cos \eta} dx ; \quad |\eta| < \pi \quad (2.8)$$

Figure 2-2: Noise Spectrum at FM Discriminator Output

2.3.2 Noise Spectrum

The power spectral density (PSD) of the noise present at the discriminator output can for the case of large SNR, be shown to be

$$S_{nF}(f) \propto f^2 \quad (2.9)$$

for $|f| < \frac{1}{2}B_T$ and zero otherwise [11]. This spectrum is illustrated in Fig. 2.2, where $B_T \approx 2(D + 1)W$ hertz, where W is the bandwidth of the message signal and D is the deviation ratio which is peak frequency deviation divided by W .

The parabolic shape of the noise spectrum results from the differentiating action of the FM discriminator and has a profound effect on the performance of FM systems operating in the presence of noise. The resulting noise spectrum shows that low-frequency message-signal components are subject to lower noise levels than are higher-frequency components.

2.4 Baseband Data Demodulator (BDD)

The design of the baseband data demodulator (BDD) block (thesis topic) of the narrow-band digital FM radio system shown in Fig. 2.1 is described. Some of the basic requirements to be considered are the following :

- 1) The signal spectrum must conform to the available channel bandwidth [i.e. for voice transmission this is the band from 300 to 3000 Hz but in our case we are designing for data

transmission. The data rate is 16 kHz therefore its spectrum will then depend on the type of coding used].

2) The signal should contain timing information that allows efficient clock recovery in the receiver and thus enables bit synchronization.

3) The signal should be immune to noise and interference.

4) To make the system reliable and easy to maintain, its complexity should be minimal.

5) Reasonable cost

6) Special requirements e.g. in a switched network it may be necessary to use a system that is insensitive to the polarity of the received signal.

A given data sequence can be represented by various waveforms shown in Fig. 2.3. In order to decide what waveform is desirable the transmission and detection of these waveforms will be discussed. For illustrative purposes the simplest waveform called non return to zero-level (NRZ-L) is considered.

Figure 2-3: Digital Waveforms

Assume that a 1 is represented by a voltage level $+V$ and that a 0 is represented by a voltage level $-V$. Also assume that this signal is transmitted over a noisy channel of infinite bandwidth. The transmitted and received noisy signals are represented in Fig. 2.4(b) as

waveforms V_T and V_R . If the received pulse sequence is sampled at regular intervals and its polarity checked with a threshold detector, the receiver could then decide whether a 1 or 0 has been transmitted.

Figure 2-4: Integrate-and-dump (a) Diagram (b) Waveforms

From the figure it can be seen that an error will occur if the magnitude of the noise voltage at sampling time is greater than that of the signal. To reduce the likelihood of error (i.e. increase the signal-to-noise ratio at decision time), an integrate-and-dump (I-D) filter (shown in Fig. 2.4(a)) was selected as one of the techniques. For one pulse interval, the signal and noise are integrated by charging a capacitor. A sample is taken at the end of pulse and a polarity decision is made. Immediately afterwards the capacitor charge is "dumped" by closing a switch and the process starts over for the next pulse.

The waveform across the capacitor is shown in Fig. 2.4(b). Integration of the useful

signal, which is constant, results in a ramp voltage that increases linearly with time. Due to the random nature of the noise, the integrated noise voltage does not rise as rapidly and the signal-to-noise ratio at decision time is thus improved by the integration process.

It is of interest to note that if the signal waveform is distorted, it is possible to enhance the SNR and thus decrease the probability of error.

In general, high-fidelity processing of the original waveform does not guarantee optimum error rate. By using filters that produce the highest possible signal-to-noise ratio at decision time, the lowest error rate is obtained.

Let us now consider whether the transmission of NRZ pulses over channels being considered is desirable, or whether other waveforms should be used. A scheme in which a decision on the data symbol is made requires synchronization with the incoming data stream. This fact influences the choice of signaling scheme.

Since the NRZ-L signal has no transitions, it therefore does not provide any timing information for long sequences of 1's or 0's. Synchronization of the receiver clock by the incoming data is thus unreliable, and errors due to shifting sampling pulses can occur even for a high SNR.

In the case of the return-to-zero (RZ) pulse stream, as shown in Fig. 2.3, timing information is provided whenever 1's are transmitted, but it fails for a long 0 sequences since there are no transitions.

A method for overcoming these timing problems would be to insert synchronizing signals having a sufficient number of level transitions into the information pulse stream. This would of course increase the time needed to transmit a message. It appears preferable to find a solution in which a signaling scheme provides better timing information.

One such waveform is the bipolar RZ-L signal, shown in Fig. 2.3. It provides timing information for both 1's and 0's, however since three levels are transmitted, a higher signal-to-noise ratio is required at the receiver than that for binary systems.

One must also pay close attention to those waveforms which have a power spectrum extending down to DC especially if the transmission path blocks the lower frequencies.

A timing scheme which overcomes these problems (timing information and the power spectrum being extended down to dc) is the Bi-Phase-Level waveform [9]. It provides

timing information for both 1's and 0's and it also is a binary system. For these reasons the Bi-Phase-Level also known as Manchester code was chosen as the waveform to be transmitted.

Fig. 2.5 shows a block diagram of a typical baseband data demodulator and the significant waveforms present in the demodulator. The incoming signal is an analog (noisy Manchester coded) signal from the output of the discriminator.

Figure 2-5: Block Diagram and Waveforms of Baseband Demodulator

The output of the BPF is followed by a slicer circuit which converts the filtered analog noisy Manchester coded signal to a digital bit stream. The Manchester bit stream is

then "exclusive-NORed" with the local receiver clock to produce a noisy NRZ bit stream. The receiver clock is generated by the timing-clock recovery circuit which extracts timing information from the received bit stream. The noisy NRZ bit stream enters the integrate-and-dump filter and its output is strobed before each dump by the data strobe.

To improve the bit error rate, the two factors considered in the design of the BPF were the time delay introduced by the BPF and the bandwidth of the BPF.

If the time delay in the bandpass filter is not constant, over the signal spectrum, the demodulated data zero crossing for dotting (101010 data sequence) and all-ones or all-zeros are offset in time relative to the zero crossings of the data clock. This situation is shown in Fig. 2.6 wherein the BPF output zero crossing for dotting occurs early, whereas the BPF output zero crossing for all zeros occurs late. This condition makes it difficult to optimize the data strobe pulse position for both conditions. The use of a Bessel filter which provides nearly constant time delay over the full signal spectrum range may help to alleviate this problem [Pawu81].

The other factor was to determine an optimum bandwidth for the BPF to achieve a high SNR at the output of the BPF. If the noise PSD at the input of the BPF (see Fig. 2.2) was constant over the 3dB bandwidth then a $0.4R$ to $1.2R$ (see Fig. 2.7) bandwidth for the BPF would result in a high SNR at the output of the BPF. However, Fig. 2.2 shows this is not the case and hence some consideration was also given to this parameter (BPF optimum bandwidth).

The error probability is also closely related to the ability of the clock acquisition and bit clock recovery circuits to correctly position the derived clock such that the function of decoding, integration and data strobing may be accomplished even when the incoming data is contaminated by noise. Thus, the demodulator must reconstruct a stable bit clock derived from the noisy incoming data stream. For more details on the timing-clock recovery circuit see [8].

The BDD architecture implementation being completely digital, completely analog or mixed analog/digital will be considered next. As mentioned earlier the basic requirements of the mobile radio system is power consumption and chip area, with the additional requirements mentioned at the start of this section.

A completely digital design will not only require the BDD circuit elements represented

Figure 2-6: Nonuniform IF Time Delay Effect on Zero Crossing

Figure 2-7: Power spectral density for Manchester coded data

by the blocks shown in Fig. 2.5 but also an analog to digital converter (ADC) since the incoming signal is analog. To obtain a high SNR, the ADC should have a high resolution (number of bits) which in turn means more complex ADC hardware and thus, larger silicon area. Hence, a completely digital BDD design though potentially providing high signal processing accuracy becomes a 'last resort' solution. An analog or mixed analog/digital solution promises a substantial saving in silicon cost.

Even though, in general, analog VLSI has the potential to offer lower power, smaller size, and a better performance than digital circuits in many applications, a digital version of the PLL alleviates some of the problems associated with its analog counterpart. For example, sensitivity of d.c. drift and component accuracy, and the need for initial calibration and periodic adjustments etc. More encouragement for the implementation of the PLL in the digital domain has resulted because of today's continued progress in increasing performance, speed, reliability and reduction in size and cost of digital ICs.

Therefore, a mixed analog/digital design was chosen to be implemented. The analog design consisted of the filtering functions and data recovery circuits, and the timing recovery circuit was a digital design.

2.5 Performance Evaluation

The performance of the baseband system was evaluated with the aid of a high-level event driven time domain simulator. The high level simulator used was Carleton University's modified version of SPLICE [13], [14]. SPLICE is an event driven simulator capable of functional and/or electrical simulation of integrated circuits. Modifications made to the simulator allow additional circuit elements to be defined by the user. The non-standard circuit elements (electrical models) are defined in RATFOR, (a language requiring a Fortran preprocessor) compiled and linked into the main simulator code. Once linked with the simulator, the element can be used as part of a circuit netlist.

The approach used for the baseband system simulation was to develop a complete system with a number of SPLICE models. The algorithms used to define the models for SPLICE were fixed and parameters for the more crucial blocks of the baseband system were optimized to obtain a satisfactory BER performance.

2.5.1 Behavioural High Level Models (SPLICE User Defined Models)

The first step in the development of the models was to define the boundary conditions and desired inputs and outputs. The designer may then proceed to a detailed list of functions or operations which must be performed. These functions or operations were defined for the high level simulator SPLICE by means of logical or timing relationships. Each model has been tested to verify its functionality and performance. In addition to the blocks

shown in Fig. 2.4, a model of the incoming signal and noise have been developed based upon the analytical model given in section 2.1. These additional models were necessary for a meaningful system evaluation. A model which detects the bit-error rate has also been developed. (See Appendix C for detailed model definitions).

After verifying each model, the BDD model was developed. The next step was to verify, by simulation, the functionality of the BDD model.

2.5.2 Functional Verification

To verify the functional operation of the BDD model (Fig 2.5), an arbitrary Manchester data stream was fed directly into the input of the BDD model and the output waveforms of each blocks ,which are shown in Fig. 2.8, were analyzed. The data was sent synchronously with the transmitter clock, trace txnrz. Trace rxsig shows the sliced Manchester coded signal which was "exclusive-NORed" with the receiver clock, rxclk. The input to the integrate-and-dump (I-D) was the decoded noisy NRZ data (trace nrz) and the I-D operation is shown in trace D. Comparing the received data (NRZ) with the transmitted data (txnrz trace) verified the system operation.

This simulation run was performed with a Gaussian IF filter, $BT = 2$, $h=1$ and the signal-to-noise ratio, $E_b/N_o = 15$ dB where $h=2\pi f_d T$, B is the bandwidth of the IF filter, T is the bit period, E_b is the signal energy per bit and N_o denotes noise power spectral density.

The next step was to determine what type of test signal format to use to analyze the performance of the system. The test signal formats requirements are;

- i) synchronization of bit and word
- ii) a arbitrary NRZ message signal spectrum (which is translated to Manchester code)

The test signal format used which met the above requirements is shown in Fig. 2.9. [15]. A 10-bit dotting sequence 1010101010 was used for bit synchronization acquisition and the word synchronization acquisition is accomplished with an 11-bit Barker code sequence 11100010010 [15]. Figure 2.10 illustrates the transmitted waveform at the output of the discriminator which in turn is fed to the BDD input (this waveform was generated using the models described in Appendix C).

The system model is now ready for performance optimization. The next issues ad

Figure 2-8: Waveforms of BDD Obtained From Simulations

Bit synchronization 10 bit dotting sequence	11 bit Barker code	Manchester data
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Figure 2-9: Test Signal Format

Figure 2-10: Arbitrary waveform at output of discriminator; (a) without phase noise, (b) with phase noise.

dressed are what design parameters to optimize and the reasons for optimizing these particular parameters.

2.5.3 Optimization Strategy

Our aim was to optimize the parameters for the worst case condition (lowest SNR). The parameters would then remain fixed for other conditions (i.e. SNR values) and the performance evaluated.

As previously mentioned, the BER is dependent on, amongst other factors, the bandwidth of the BPF and the time delay introduced by the bandpass filter, hence a need to optimize these parameters. A study by [12] examines the dependence of BER on the time delay distortion of the bandpass filter. Two different types of BPF filters, the Bessel and Butterworth, were considered. The results obtained in this comparison showed that there was only a slight difference in performance using the different filters and it also demonstrated that a filter with nonlinear phase characteristics (Butterworth) can exhibit performance nearly equal to that of one with linear phase characteristics (Bessel). Based on those considerations a Butterworth type filter was chosen for its ease of implementation. Another parameter considered in the design of the BPF was the order of the filter. To try to fulfill the minimal complexity requirement and a saving in silicon area, a 4th order BPF using cascaded biquads (low-pass and high-pass) was chosen as a starting point. A realistic starting point for the bandwidth parameters would be $0.4R$ (first biquad) and $1.2R$ (second biquad) (R is data rate) which correspond to the 3dB PSD bandwidth points for Manchester data, even though the input to the BDD is not a true Manchester data signal but rather a Manchester data signal that has been distorted by the output of the discriminator.

The comparator used in the slicer block was a cell already existing in Carleton's Standard Cell library and therefore the specifications could not be optimized for our particular application. Instead, the fixed parameters used for the model were the actual measured results obtained from the testing of the comparator. For the integrate-and-dump filter (I-D) there was no need for stringent optimization of parameters. The main concern for the I-D filter was to choose appropriate RC values in order to achieve a high SNR at decision time.

The timing-clock recovery parameters were obtained using theoretical equations based upon system performance requirements (i.e. bandwidth, etc). Hence, the parameters for this block were not optimized via simulations. For more details see [8].

2.5.4 Simulation Results

The simulation results revealed that the optimized bandwidth for BPF was 6.6k - 20k Hz which is a slight difference from the theoretical 3dB PSD bandwidth for Manchester coded data (theoretical - $0.4R$ to $1.2R$ where R was a data rate of 16 kHz). In fact this demonstrated that a Manchester coded data at the input of the BDD rather than the actual signal obtained from the discriminator would have exhibit nearly the same results.

The BER was obtained based on the number of errors present after 100,000 data has been transmitted for different SNR. The simulations were performed with $h=1$ and $BT=2$. The results of BER evaluation using SPLICE and theoretical BER [12] are shown in figure 2.10.

Figure 2-11: Bit-error-rate comparison between simulations and theoretical results

Impairment of the simulated from the theoretical values is as small as 0.5 dB in E_b/N_o at $BER = 10^{-3}$. This can be partly due to the inclusion of the receiver clock jitter and the non-constant time delay of the band-pass filter. Both factors were not considered in the theoretical BER evaluations [12].

2.6 Summary

A system level verified mixed analog/digital baseband data demodulator for a narrow-band digital FM radio system has been designed. The simulator used in evaluating the performance of the baseband system was Carletons' University modified version of SPLICE. Specifications for the building block of the BDD were optimized to obtain a satisfactory BER performance which is comparable with theoretical results from literature.

This completes phase II of the IC design cycle. In the next chapter the circuit design and layout of the analog building blocks will be discussed.

Chapter 3

ANALOG CIRCUIT DESIGN AND INTEGRATION

3.1 Introduction

Having decided on a mixed analog/digital baseband system design, the engineer is faced with a choice of the analog filter design. The design could be passive analog filters, active analog filters or switched-capacitor (SC) filters. The choice will be influenced by consideration of size versus space available, quantity and cost and the degree of precision demanded by the application. Taking these considerations into account SC filters were chosen.

The principle of using periodically-switched capacitors to generate frequency-selective responses has been known since at least the mid 1960s. It wasn't until the late 1970s that integrated circuit switched-capacitor filters became a reality [16], [17]. At present a great number of SC design techniques are well established for practical use [18], [20], [21], [22]. The section on SC filter synthesis presented in this chapter follows an approach based on the work done by A.S. Sedra in [23]

In general, computer simulations would not be very useful if they were used only to analyze the behaviour of ideal circuits. The technique is indispensable, however, in determining the effects of parasitic elements which would make a pencil-and-paper analysis prohibitively complicated. Such is the case with monolithic switched-capacitor filters where stray capacitances, switched resistances, finite op-amp gain, temperature sensitivities and other non-ideal effects including noise generated in switched-capacitor networks can cause actual circuit performance to deviate significantly from that expected. With the capability to simulate by computer, the designer can account for all these effects and adjust component values accordingly, so that the integrated circuit produced is much more likely to be within performance specifications.

As a result of the integrated realization, many non-ideal effects occur in the circuit. The origin of some effects, analysis of its influence on the performance of the circuit and

methods for their eliminations have been considered in the layout.

3.2 SWITCHED-CAPACITOR FILTER SYNTHESIS

There are currently two approaches using MOS technology for the implementation of precision analog filtering functions in monolithic integrated-circuit forms. The first approach is that the analog signal is processed directly in its continuous-time form. The other approach is based on processing samples of the analog signal and thus resulting circuits are discrete-time or sampled-data systems.

Realizing classical RC-active filters completely in monolithic form has proven to be difficult for two reasons: (1) the need for large-valued resistors and capacitors (especially for low-frequency filters), and (2) the need for stable accurate RC time constants. Typically, CMOS technology provides (polysilicon) resistors of $\pm 30\%$ of absolute value accuracy and about 1% best case matching. The SC filter technique overcomes both problems.

The basic principle employed in switched capacitor filter technique is that a capacitor C periodically-switched between two nodes at a sufficiently high rate (f_c). An equivalent resistance between the two nodes can be calculated as $R \simeq 1/Cf_c$. Hence, the realization of filter functions using op-amps, capacitors and periodically-operated switches is possible. MOS technology is particularly suitable for the realization of SC filters because :

- 1) it provides high quality capacitors, offset free switches, and good op-amp performance.
- 2) small-sized capacitors can be used to simulate large resistors which results in less silicon.

The resulting time constant realized using SC techniques is $1/f_c [C_2/C_1]$ which shows the dependence on the clock frequency and the capacitor ratios. Since, in MOS technology, f_c can be accurately controlled using crystal clock oscillators and capacitor ratios can be realized to a high accuracy, SC filters can achieve very precise frequency responses.

Two approaches for obtaining the transfer functions of the SC circuit will be reviewed and their differences will be compared.

3.2.1 1st ORDER BASIC BUILDING BLOCKS

The use of op-amp RC integrators as the basic building block for designing active-RC filters is one of the most popular methods. Second order filter sections known as *biquads* can be realized using a feedback loop containing one inverting and one noninverting

integrator. Cascading the two-integrator-loop biquads will realize higher-order filters or if a low-sensitivity circuit is desired, LC ladder prototype. The L and C elements of the ladder prototype are simulated using op-amp RC integrators.

Integrators are also the basic building blocks of SC filters and Fig. 3.1 shows inverting and noninverting SC integrator circuits [24], [25].

Figure 3-1: Standard stray-insensitive SC filter building blocks: (a) inverting integrator, (b) noninverting integrator .

These circuits have become the standard building blocks of SC networks because of their insensitivity to the stray capacitances present between source and drain diffusions of the MOS transistors and substrates.

It is assumed that the reader has some background in SC analysis and therefore the basic operation for the SC filters of Fig. 3.1 will not be reviewed.

Two approaches for obtaining the transfer functions of SC circuits will be examined. The first approach uses the transfer function of SC circuits obtained by substituting $R = 1/f_c C = T_c/C$ into the continuous-time transfer function. In the other approach, all the resistors in the circuit are replaced with their equivalent switched-capacitors and then the exact transfer function is derived.

3.2.1.1 Resistor Equivalent Transfer Function

The continuous-time equivalent circuit in Fig. 3.2a is that of an inverting (Miller) integrator with a transfer function given by

$$\frac{V_o(w)}{V_i} = -\frac{1}{jwRC} \quad (3.1)$$

Figure 3-2: Continuous-time equivalent circuits: (a) inverting integrator, (b) noninverting integrator .

The transfer function for the SC circuit of Fig. 3.1a is obtained by substituting $R = 1/f_c C = T_c/C$ into (3.1) giving

$$\frac{V_o(w)}{V_i} = - \left(\frac{C_1}{C_2} \right) \frac{1}{jwT_c} \quad (3.2)$$

Thus , the circuit of Fig. 3.1a when clocked at a frequency much higher than the signal frequencies performs the function of an inverting integrator with an integration constant of $T_c(C_2/C_1)$ or equivalently , $(\frac{1}{f_c})(\frac{C_2}{C_1})$.

It can be shown that the circuit of Fig. 3.1b, if clocked at a sufficiently high rate , can be represented by its continuous-time equivalent shown in Fig. 3.2b. The transfer function becomes that in (3.1) except with a positive sign. Therefore the noninverting integrator function has a integration constant of $T_c(C_2/C_1)$ when the SC circuit of Fig. 3.1b is clocked at a high rate. A bonus obtained from the SC circuit of Fig. 1b is that the inversion is obtained by using the correct clocking phase as opposed to an additional op-amp needed in the active-RC case.

3.2.1.2 Exact Transfer Functions

The transfer function above were based on the assumption that the clocking frequency was much higher than the signal frequencies so that the discrete-time operation of the circuits appears almost continuous. Under this approximation, a switched capacitor C is equivalent to a resistance (T_c/C) . In many cases, however, the approximation inherent in this equivalence leads to filter circuits whose responses deviate from the desired one. This can be better understood by deriving the exact transfer function (op-amp gain assumed infinite) of the basic building blocks.

For the inverting integrator of Fig. 3.1a, the output voltage can be written as

$$v_o(n) = v_o(n-1) - \frac{C_1}{C_2} v_{in}(n) \quad (3.3)$$

To obtain the frequency response, the z transform is applied and the rearranged equation yields

$$\frac{V_o}{V_i}(z) = -\left(\frac{C_1}{C_2}\right) \frac{1}{1-z^{-1}} \quad (3.4)$$

This transfer function can be written in an alternate form

$$\frac{V_o}{V_i}(z) = -\left(\frac{C_1}{C_2}\right) \frac{z^{1/2}}{z^{1/2} - z^{-1/2}} \quad (3.5)$$

The response for physical frequencies w can be obtained by substituting $z = e^{jwT_c}$ which results in

$$\frac{V_o}{V_i}(w) = -\left(\frac{C_1}{C_2}\right) \frac{e^{j(wT_c/2)}}{j2\sin(wT_c/2)} \quad (3.6)$$

This transfer function is obviously not that of an ideal integrator. The magnitude is inversely proportional to $\sin(wT_c/2)$ and not to w as is the case for an ideal integrator. There is also an excess phase lead represented by the factor $e^{jwT_c/2}$ which will be shown later not to be important. When designing SC networks, the dependence of $\sin(wT_c/2)$ unless taken into account, causes deviations from the filter response. These deviations can be kept small by clocking the filter at a sufficiently high rate so that $(wT_c/2) \ll 1$ and thus $\sin(wT_c/2) \simeq wT_c/2$ which gives

$$\frac{V_o}{V_i}(w) = -\left(\frac{C_1}{C_2}\right) \frac{e^{j(wT_c/2)}}{jwT_c} \quad (3.7)$$

Note: apart from the excess phase lead this transfer function is identical to that derived above (3.2) using the SC-resistor equivalence. In terms of exact transfer function, ignoring for the time being, the extra delay $e^{jwT_c/2}$, the difference between the ideal (3.2) and (3.6) is

$$\Omega T_c = 2\sin(wT_c/2) \quad (3.8)$$

where Ω is the continuous frequency and w is the sampled-data frequency. This equation shows the frequency warping of the sampled-data domain.

Another point of view can be taken to obtain the same results. The transfer function of (3.6) can be written in an alternate form by multiplying the numerator and denominator by wT_c

$$\frac{V_o}{V_i}(w) = -\left[\frac{C_1}{C_2} \frac{1}{jwT_c}\right] \frac{wT_c/2}{\sin(wT_c/2)} e^{j(wT_c/2)} \quad (3.9)$$

We see now that the first term in brackets is the response of an ideal continuous integrator and the rest of the expression is the deviation from the ideal response caused by the sampling process. The ideal transfer function has been multiplied by a sample-and-hold transfer function which is expected since the output is of a sample-and-hold response.

3.2.2 BIQUADRATIC CIRCUITS

The design of SC biquad circuits uses active-RC integrators as the basic building blocks. The resistors in the active-RC biquads will simply be replaced with the SC equivalent branches. As was the case for the SC integrators, the SC biquads will appear as a continuous active RC biquad if the clocking frequency is much greater than the biquad pole frequency.

3.2.2.1 Resistor Equivalent Transfer Functions

An active-RC biquad based on the two-integrator-loop topology is shown in Fig. 3.3a.

This biquad realizes a bandpass function at the output of OA1 and a low-pass function at the output of OA2. The transfer functions are

$$\frac{V_{o1}}{V_i}(s) = \frac{-s \frac{1}{C_2 R_1}}{s^2 + \frac{1}{C_2 R_6} s + \frac{1}{C_2 C_4 R_3 R_5}} \quad (3.10)$$

$$\frac{V_{o2}}{V_i}(s) = \frac{-\frac{C_2 C_4 R_1 R_3}{C_2 R_6}}{s^2 + \frac{1}{C_2 R_6} s + \frac{1}{C_2 C_4 R_3 R_5}} \quad (3.11)$$

Thus the pole frequency is given by

$$\omega_o = \frac{1}{\sqrt{C_2 C_3 R_3 R_5}} \quad (3.12)$$

the pole Q is given by

$$Q = \sqrt{\frac{C_2}{C_4}} \frac{R_6}{\sqrt{R_3 R_5}} \quad (3.13)$$

and the center-frequency gain of the bandpass function is given by

$$G_o = -\frac{R_6}{R_1} \quad (3.14)$$

Usually the biquads are designed to have equal time constants (maximizing the biquad dynamic range) [23] yielding

$$C_2 = C_4 = C; \quad R_3 = R_5 = R \quad (3.15)$$

Figure 3-3: (a) A two-integrator-loop active-RC biquad, (b) The equivalent SC biquad obtained by replacing each resistor R_i with a capacitor $C_i = T_c/R_i$.

thus

$$\omega_o = \frac{1}{RC} \quad (3.16)$$

For clocking frequencies much greater than the pole frequency, substituting $R = 1/f_c C$ into (3.11) and (3.12) respectively gives the pole frequency as

$$\omega_o = \frac{1}{T_c} \sqrt{\frac{C_5 C_3}{C_2 C_4}} \quad (3.17)$$

and the pole Q is

$$Q = \sqrt{\frac{C_2}{C_4} \frac{\sqrt{C_3 C_5}}{C_6}} \quad (3.18)$$

These SC biquad circuits are also tolerant of the effects of finite settling time of the op-amps [26].

3.2.2.2 Exact Transfer Function

Fig. 3.3b presents an equivalent SC biquad obtained by replacing each resistor with a switched capacitor. Note that positive resistors are replaced with inverting SC branches while the negative resistor is replaced with a noninverting SC branch. The exact transfer function of the SC biquad in Fig. 3.3b for the bandpass function is given by

$$\frac{V_{o1}}{V_i}(z) = \frac{-\frac{C_1}{C_2}z^{1/2}(z^{1/2} - z^{-1/2})}{(z^{1/2} - z^{-1/2})^2 + \frac{C_4}{C_2}z^{1/2}(z^{1/2} - z^{-1/2}) + \frac{C_3C_4}{C_2C_1}} \quad (3.19)$$

for physical frequencies, $z = e^{j\omega T_c}$

$$\frac{V_{o1}}{V_i}(\omega) = \frac{-j\frac{C_1}{C_2}2\sin\left(\frac{\omega T_c}{2}\right)e^{j(\omega T_c/2)}}{\left[\frac{C_3C_4}{C_2C_1} - 4\sin^2\left(\frac{\omega T_c}{2}\right)\left(1 + \frac{C_4}{2C_2}\right)\right] + j(C_4/C_2)\sin(\omega T_c)} \quad (3.20)$$

which, for $\omega T_c \ll 1$, reduces to

$$\frac{V_{o1}}{V_i}(\omega) \approx \frac{-j\omega T_c \frac{C_1}{C_2}e^{j(\omega T_c/2)}}{\left[\frac{C_3C_4}{C_2C_1} - (\omega T_c)^2\left(1 + \frac{C_4}{2C_2}\right)\right] + j(C_4/C_2)(\omega T_c)} \quad (3.21)$$

The fact that the excess phase ($z^{\pm 1/2}$ numerator term) of the two-integrator-loop cancels out confirms the earlier analysis. Note however, that there is a delay of one clock period around the loop.

Apart from the numerator term $e^{j\omega T_c/2}$, this equation is in the form of the second-order bandpass function

$$T(\omega) = \frac{-j\omega k}{(\omega_o^2 - \omega^2) + j(\frac{\omega\omega_o}{Q})} \quad (3.22)$$

where

$$\omega_o = \frac{1}{T_c} \sqrt{\left(\frac{C_3C_4}{C_2C_1}\right) / \left(1 + \frac{C_4}{2C_2}\right)} \quad (3.23)$$

and

$$Q = \sqrt{\frac{C_2}{C_4}} \frac{\sqrt{C_3C_5}}{C_6} \sqrt{1 + \frac{C_6}{2C_2}} \quad (3.24)$$

These equations differ slightly from those given by (3.17) and (3.18). These equations (3.23) and (3.24) are more accurate than (3.17) and (3.18) but the resulting design will still be approximate since it is based on the assumption that $\omega T_c \ll 1$. Better results can be

obtained if design is based on the exact transfer function in (3.19). For example, w_0 can be found from

$$4\sin^2\left(\frac{wT_c}{2}\right) = \left(\frac{C_3C_5}{C_4C_2}\right) / \left(1 + \frac{C_6}{2C_2}\right) \quad (3.25)$$

Designing SC filters using this approach can be found in [24].

The exact transfer function in (3.19) derived from Fig. 3.3b, has one transmission zero at $z = 1$ and another at $z = 0$. While the first zero corresponds to $w = 0$, the second has no corresponding physical frequency.

Therefore, it contributes little to the selectivity of the bandpass filter response. In other words, the original continuous-time active-RC circuit has a zero at $w = 0$ and another at $w = \infty$, both contributing to selectivity, the discrete-time SC filter has only one physical frequency zero (at $w = 0$). If a transmission zero is placed at half the clock frequency ($w = w_c/2 = 2\pi f_c/2 = \pi/T_c$), a more selective bandpass response can be obtained.

The next section will outline the design method used to obtain good transfer-function characteristics of SC networks designed using biquadratic circuits.

3.2.3 Exact Design Method

This section deals with the exact synthesis of biquadratic SC filters whose transfer function will be identical to the desired one. Higher order SC filters can be realized as a cascade of biquads and in the case of odd-order filters, a first-order section. This exact design method, just as others [27], [28], [29], makes use of the bilinear transformation [30], [31].

3.2.3.1 The Bilinear Transformation

In bilinear transformation

$$\lambda = \frac{z - 1}{z + 1} \quad (3.26)$$

maps the unit circle in the z -plane (which is the contour of physical frequency points) onto the entire imaginary axis of the λ plane. The relationship between the frequency w and the corresponding point Ω on the imaginary axis of the Ω plane is given by

$$\Omega = \frac{2}{T_c} \tan(wT_c/2) \quad (3.27)$$

From the equation, we note that $w = 0$ maps to $\Omega = 0$ and $w = \pi/T_c$ (half the clocking frequency) maps to $\Omega = \infty$. This is a one to one mapping with half the unit circle (

$wT_c = 0$ to $wT_c = \pi/T_c$ being mapped onto the positive half of the $j\Omega$ axis ($\Omega = 0$ to $\Omega = \infty$). In the continuous-time analog filter literature there exists a wealth of design data and synthesis methods for filters whose responses are specified along the imaginary axis of a complex plane. These tools can be applied to the design of discrete-time filters (of which SC filters is a special case) via the bilinear transformation.

3.2.3.2 Biquad Design

Since SC filters can be realized as a cascade of biquads, only the synthesis of biquadratic SC filters is considered. For higher order filters, cascade design is performed directly on the transfer function $T(\lambda)$ which can be factored into products of second order (possibly one first order) functions. In designing cascade active-RC filters, the problem of pole-zero pairing, cascading sequence and gain assignments must be considered and such is the case for designing cascade SC filters.

A general biquadratic transfer function is of the form

$$H(s) = \pm \frac{a_2 s^2 + a_1 s + a_0}{s^2 + b_1 s + b_0} \quad (3.28)$$

and the equation derived using the bilinear transformation is

$$H(z) = \pm \frac{m(a'_0 + a'_1 + a'_2)z^2 + m(a'_0 - a'_2)z + m(a'_0 - a'_1 + a'_2)}{z^2 + 2m(b'_0 - 1) + m(1 + b'_0 - b'_1)} \quad (3.29)$$

where

$$m = \frac{1}{1 + b_0 + b_1} \quad (3.30)a$$

$$a'_2 = a_2$$

$$a'_1 = \left(\frac{T_c}{2}\right)a_1 \quad (3.30)b$$

$$a'_0 = \left(\frac{T_c}{2}\right)^2 a_0 \quad (3.30)c$$

$$b'_1 = \left(\frac{T_c}{2}\right)b_1 \quad (3.30)d$$

$$b'_0 = \left(\frac{T_c}{2}\right)^2 b_0 \quad (3.30)e$$

Some of the SC biquads circuits capable of realizing the general transfer function have been given in [32]. One of these circuits is shown in Fig. 3.4 as an example.

Figure 3-4: A SC biquad circuit capable of realizing the general bilinearly transformed function in equation (31).

Analysis of this circuit results in the exact transfer function

$$V_o/V_i(z) = \frac{K_3 z^2 + (-2K_3 + K_1 K_5 + K_2 K_5)z + (K_3 - K_3 K_5)}{z^2 + (-2 + K_4 K_5 + K_5 K_6)z + (1 - K_5 K_6)} \quad (3.31)$$

Design equations for the SC biquad can be obtained by equating the coefficients of like powers of z in eqn (3.29) and (3.31). The pole equations are given by

$$K_4 K_5 = 4mb'_0 \quad (3.32)$$

$$K_5 K_6 = 2mb'_1 \quad (3.33)$$

Since there are 2 equations with 3 unknowns one of the capacitor ratios can be chosen arbitrarily. The one degree of freedom may be used to maximize the dynamic range of the biquad. For high Q biquads, this is approximately obtained when the time constants of the two loops are made equal, that is $K_4 = K_5$.

The transmission zeros are obtained by equating coefficients of corresponding numerator terms. The result for some special cases are:

(a) Low Pass ($a_1 = a_2 = 0$)

$$K_2 = 0, \quad K_1 K_5 = 4ma'_0, \quad K_3 = ma'_0$$

(b) Bandpass ($a_0 = a_2 = 0$)

$$K_1 = 0 \quad K_2 K_3 = 2ma'_1 \quad K_3 = ma'_1$$

(c) High Pass ($a_0 = a_1$)

$$K_1 = K_2 = 0 \quad K_3 = ma'_2$$

(d) Notch ($a_1 = 0$)

$$K_2 = 0 \quad K_1 K_3 = 4ma'_0 \quad K_3 = m(a'_0 + a'_2)$$

The biquad circuits designed using the bilinear transformation (such as the circuit in Fig. 3-4) have frequency responses that are more selective than those studied in section 3.2.2. This result can be observed by considering the low-pass case. The numerator for (3.31) becomes

$$a'_0(z^2 + 2z + 1) = a'_0(z + 1)(z + 1) \quad (3.34)$$

Therefore, the two transmission zeros occur at $z = -1$ and in terms of physical frequencies

$$z = e^{j\omega T_c} = -1 = \cos(\omega T_c) + j\sin(\omega T_c) \quad (3.35)$$

when the sampled-data frequency

$$\omega = \pi/T_c \quad (3.36)$$

which corresponds to a continuous time domain frequency of

$$\Omega = \frac{2}{T_c} \tan\left(\frac{\omega T_c}{2}\right) = \infty \quad (3.37)$$

As an example, a SC low-pass filter (LPF) design using both approaches is given in Appendix D.

From the above analysis the conclusions reached for the synthesis of SC filters are;

- i) the resistor equivalence method should only be used for design with very high relative clock rates and the prewarp equation is $\Omega = \frac{2}{T_c} \sin(\omega T_c/2)$.
- ii) the exact method is recommended for good transfer-function characteristics and the prewarp equation is $\Omega = \frac{2}{T_c} \tan(\omega T_c/2)$.

3.3 Prefiltering Requirements for SCF

A phenomenon inherent in sample-and-hold circuits is called aliasing or folding. The definition for aliasing is the folding of high-frequency signals into the baseband because of sampling a signal at too low a frequency. Thus, high-frequency components become equivalent to low frequencies. Therefore, SC circuits which perform a sample-and-hold function are vulnerable to aliasing. To prevent this, in general, a low-pass continuous-time analog antialiasing filter (AAF) is required before a continuous-time signal can be processed by a SC circuit (see Fig. 3.5).

Figure 3-5: SC circuit with antialiasing prefilter.

A continuous-time low pass AAF with a stopband limit frequency $f_{stop} = f_c/2$ can prevent all aliasing, since only that part of the input spectrum which extends beyond $f_c/2 = 1/2T_c$ is responsible for the aliasing [32].

In most SC system, the antialiasing filter is integrated on a MOS chip which is shared with the rest of the system. The AAF is then typically an active-RC filter, containing thin-oxide capacitors and polysilicon resistors. For details on the design considerations of antialiasing filters integrated on the same chip as the rest of the system see [32].

For our particular application, the antialiasing is performed using an off chip low-pass filter.

3.4 SC Noise Analysis

The noise generated in SCN is attributed to two origins:

- 1) the thermal noise associated with the "on" resistance of the MOS transistors.
- 2) the noise created in the op-amp

In both cases, the bandwidth of the noise signal may exceed the sampling frequency. The periodical transition from the MOS switches from an "on" to an "off" state results in an undersampling (and consequently aliasing) of the different wideband noise associated with the corresponding capacitors and op-amp. Since the different noise sources are uncorrelated, their contributions to the output noise spectrum can be evaluated separately.

A pencil-and-paper analysis of the noise generated in SCN can be complicated and tedious. With the capability to simulate by computer, the designer can then analyze the SCN to determine the dominant noise sources and hence, account for SC noise so that a better performance circuit is designed.

The development of models suitable for SPICE [33] noise simulations of SCN based on [34] work is the focus of this section. The noise analysis reviewed here differs from earlier work [35], [36], [37] by emphasizing approximations that facilitate the use of general-purpose programs, such as SPICE, for accurate SCN noise analysis.

3.4.1 Noise Analysis of SCN

If the input to a sampled data system is white noise of bandwidth BW_n , the output noise spectral density was shown [34] to be

$$\eta_{out}(f) = \eta_n \left[\tau_{SH}^2 \text{sinc}^2 \left[\frac{\tau_{SH} f}{f_s} \right] + (1 - \tau_{SH})^2 \right] \quad BW_n < \frac{1}{2} f_s \quad (3.43)a$$

$$\eta_{out}(f) \leq \eta_n \left[2\tau_{SH}^2 \left(\frac{BW_n}{f_s} \right) \text{sinc}^2 \left[\frac{\tau_{SH} f}{f_s} \right] + (1 - \tau_{SH})^2 \right] \quad BW_n \geq 10 f_s \quad (3.44)b$$

where

the first term represents the tracking term and the second term is due to the sample-and-hold.

τ_{SH} - sample-and-hold duty cycle

BW_n - represents the equivalent noise bandwidth of a noise source, and will be taken to be that bandwidth required to contain the same noise power as the source, but with a uniform spectral density η_n

$\frac{BW_n}{f_s}$ - the number of sidebands folding back in the frequency range $0 < f < f_s$

A better feel for these equations can be gained by looking at a few limiting cases.

Figure 3-6: SCN of a high pass filter

Case 1) $\tau_{SH} = 0$: For this condition the noise is being tracked and not sampled, hence the sampling term drops out and the resulting equation is

$$\eta_{out}(f) = \eta_n \quad (3.45)$$

Case 2) $\tau_{SH} = 1$ and $BW_n > 10f_s$: For this condition , the noise is being sampled-and-held only resulting in no track term.

$$\eta_{out}(f) \leq 2\eta_n \tau_{SH}^2 \left(\frac{BW_n}{f_s} \right) \text{sinc}^2 \left[\frac{\tau_{SH} f}{f_s} \right] \quad (3.46)$$

Case 3) $\tau_{SH} = 1/2$ and $BW_n > 10f_s$:

$$\eta_{out}(f) = \eta_n \left[\frac{1}{2} \left(\frac{BW_n}{f_s} \right) \text{sinc}^2 \left(\frac{f}{2f_s} \right) + \frac{1}{2} \right] \quad (3.47)$$

3.4.2 Noise models for SPICE

The switch capacitors of Fig. 3.6 are replaced with resistors of values

$$R = \frac{1}{Cf_s}$$

to simulate the switching noise kT/C . The op-amp of the SCN (Fig. 3.6) are replaced with blocks shown in Fig. 3.7. The op-amp noise simulation model has a switched output (S_o) which is connected to all the switched capacitors attached to the output of the op-amps. The continuous output (C_o) is connected to the paths that are not switched. Next, the noise simulation models for the filter topology presented above, will be developed.

Figure 3-7: Noise simulation model for high pass filter SCN

Op-Amp Model

The op-amp model, which includes the sampled data effects on the output of the op-amp, is shown in Fig. 3.8.

$$V_{1/f}(t) = \sqrt{A/f}$$

$$V_{n1} = \sqrt{G A}$$

$$\left| V_{n1} \right|_{rms} \quad \left| V_{n1} \right|_{rms} \quad \text{But uncorrelated, used to model foldover noise}$$

C_0 - Output to non sampled paths

S_0 - Output to sampled paths

Figure 3-8: Frequency domain SCN op-amp noise simulation model.

The op-amp noise consists of two parts : wide-band (flat, white noise), and $1/f$ (flicker) noise. The voltage sources $V_{1/f}$ and V_{n1} are used to model the unsampled $1/f$ and flat-band noise respectively. Since the foldover effects are added to the unsampled output noise, the noise sources kV_{n1} and V_{f11} have been placed in series with the continuous output to yield S_0 . The equivalent noise bandwidth (BW_n) of an op-amp will be taken to be that

bandwidth required to contain the same noise power as the op-amp but with a uniform spectral density n_n

Figure 3-9: Voltage-follower output noise spectrum with test configuration.

The foldover factor is derived by simplifying (3.44b) under the constraints that $f \ll f_s$, so the $\sin(x/x)$ term approaches unity. The result is then separated into terms related to the C_o and S_o outputs respectively:

$$\eta_{out}(f) \leq \eta_n + \eta_n \left[2\tau_{SH}^2 \left(\frac{BW_n}{f_s} \right) - \tau_{SH} \right] \quad (3.48a)$$

with the bracketed term representing the foldover effects represented by kV_{n11} . For a τ_{SH} equal to $\frac{1}{2}$, which is the case for our application, equation 3.48a becomes:

$$\eta_{out}(f) \leq \eta_n + \eta_n \left[\frac{1}{2} \left(\frac{BW_n}{f_s} - 1 \right) \right] \quad (3.48b)$$

Since SPICE works with noise voltages rather than powers, the noise voltage gain through sampling is obtained by taking the square root of the bracketed term to yield

$$k = \sqrt{\frac{1}{2} \left(\frac{BW_n}{f_s} - 1 \right)} \quad (3.49)$$

It has been shown [34], for the assumption that the flicker noise spectral density follows an amplitude envelope of the form A/f , that the $1/f$ foldover effects can be closely approximated by adding a constant αA to the presampled $1/f$ spectrum. The contributions of the $1/f$ noise is given as [34]

$$\eta_{out}^{1/f}(f) \leq \frac{A}{f} + (\alpha A) \quad (3.50)$$

The noise voltage gain, due to sampling, for the $1/f$ term is $\sqrt{\alpha A}$.

A detailed outline on how to use SPICE to model the op-amp noise will follow in the next two sections.

Flicker Noise Model

To generate flicker noise, a device model, shown in the boxed circuit, (Fig. 3-10) was used to simulate the unsampled $1/f$ noise component. The noise voltage as seen at the drain is

$$\sqrt{\frac{8kT}{3g_m} + \frac{KF}{fWL_{eff}}} \quad (3.51)$$

where

k - Boltzmann's constant

T - temperature in degrees Kelvin

g_m - transconductance gain of the transistor

W - width of transistor channel

L_{eff} - effective channel length of transistor channel and

KF - flicker noise coefficient

To study the $1/f$ and wide-band noise effects separately, select the bias current and device W/L ratio to assure that the g_m term contributes much less noise than the input-referred op-amp flat-band noise. KF is adjusted to match the measured (or SPICE simulated) op-amp input-referred $1/f$ noise.

Because the flicker noise is to be injected into the noninverting terminal of a high gain op-amp, the dc bias voltage at the drain must be blocked. To avoid loading the drain with the dc blocking circuit (RDC,CBLK), a voltage-controlled voltage source is used as an ideal buffer.

Flat-Band and Foldover Noise Model

The flat-band, folded flat-band, and folded $1/f$ noises can be modelled as white noise sources which are easily simulated by resistors in SPICE. The flat-band noise model uses a resistor value selected to match the measured input referred flat-band noise. The nodal interconnection requirement of SPICE is that all nodes have at least two components connected and a dc path to ground. Therefore, two resistors each twice the value of the

input-referred noise resistance are paralleled to satisfy SPICE nodal requirements.

The V_{n1} source models the unsampled flat-band noise injected into the op-amp, V_{n11} models the wide-band foldover effects and V_{f11} the $1/f$ folded noise. Separate resistors are used to drive V_{n1} , V_{n11} , and V_{f11} so that the sources will be mutually uncorrelated.

The appropriate resistor values corresponding to folded $1/f$ noise are

$$R_{F11A} = R_{F11B} = 2 \frac{\alpha A}{4kT} \quad (3.52)$$

For more details on the development of these models for SPICE see Appendix D.

3.4.3 Model Limitations

In most cases the SCN's are designed with the sample rate much greater than the passband $f \ll f_s$ hence the $\sin x/x$ frequency shaping will not affect the in-band noise significantly.

3.4.4 Simulated Results

Using the models developed for SPICE (see Fig. 3.10), the SC noise found in low-pass (LPF), high-pass (HPF), and band-pass (BPF) filters were analyzed and the simulated results are presented in Appendix D. The shape of the HPF noise response was compared with that found in [34] and the results closely agree therefore verifying the models developed. The analysis revealed that the noise generated by the SC filters is small compared to the noise at the input of the BDD (i.e. $\text{SNR} \geq 10\text{dB}$). Hence, noise due to SC filters will not significantly effect the performance of the overall baseband system.

3.5 Analog Circuit Design

The analog circuits of the baseband system were designed using SC techniques to meet the specifications obtained from the high level simulations. At this stage of the analog design a choice had to be made regarding differential or single-sided techniques for the circuit designs. Using a differential switched-capacitor technique for the design would be effective in reducing the common-mode noise but any (uncorrelated) noise generated in one of the other identical halves of the circuit would not be eliminated in this manner. A disadvantage of differential technique was that it takes up more silicon area. Since common-mode noise was not a major concern for this particular application, a single-ended design was chosen.

Figure 3-10: Complete SPICE op-amp noise model. The boxed circuit is the $1/f$ source, and the resistors are uncorrelated white noise sources.

For the proposed designs, methods are required to analyze the frequency domain and/or time domain performance of the filters. More and more software packages dedicated to the simulation of SC circuits have become available. Some of the packages are DIANA [38], SCOP [39], SWITCAP [40]. An alternate approach is modeling switched-capacitors with frequency dependent resistors for a frequency domain analysis [41] using a continuous time circuit analysis package such as SPICE. Substituting the appropriate SC equivalent circuit, the frequency response of a SC circuit can be analyzed without the aid of a dedicated program. For cases when the sampling frequency is much greater than the bandwidth of filter, the frequency response of the SCN can be analyzed using SPICE by replacing the switched-capacitors with their approximately equivalent resistors $R \approx 1/f_s C$

3.5.1 SC BPF Design

The bandpass filtering function was designed using a cascaded low-pass and high pass biquad filter to achieve adequate sensitivity performance for the application. As previously mentioned, a better performance can be obtained using a Bessel filter instead of Butterworth filter. At this stage of the thesis, I had already designed/tested Butterworth filters and hence decided to use Butterworth filters. This type of filter will not give the best BER performance but it at least ensures a high probability of first time success of the BDD design.

For the Butterworth filters, the following optimized specifications, based upon the simulation results, gave a satisfactory BER performance

- i) 2nd order low/high pass filters
- ii) $Q = \frac{1}{\sqrt{2}}$
- iii) pole frequency of 20.0 kHz for HPF and 6.6 kHz for LPF
- iv) dc gain of unity for LPF and high frequency gain of unity for HPF
- v) sampling frequency of 512 kHz (32 times the data rate).

The resistor equivalent method was used in synthesizing the SC filters. This method was justified by the fact that the sampling frequency was high as compared to the pole frequencies of the filters. The biquad SC low/high pass filter circuit, are shown in Fig. 3.11 a and b respectively. The SCN frequency domain responses, which were analyzed using SPICE by substituting the switched capacitors with their equivalent resistance, shows the

(a)

(b)

Figure 3-11: Switched capacitor filters, (a) low-pass , (b) high-pass .

expected responses (see Appendix D).

3.5.2 Slicer Design

The bit error rate characteristics depends on the offset voltage of the slicer, so a slicer

circuit which cancels offset automatically is used. The circuit used for the slicer is shown in Fig. 3.12. During ϕ_1 , the capacitor C is charged up to the offset voltage V_{off} of the comparator and v_{in} is then sampled on ϕ_2 . Now V_i and V_{off} (stored in C) appear in series at the input of the comparator. The output V_o of the comparator will be high if $V_i < 0$ and low if $V_i > 0$, as in an offset-free comparator. The output V_o is then latched by the data flip-flop circuit. Since this circuit is relatively straight forward, a SPICE simulation to verify its functionality was not performed.

Figure 3-12: Comparator offset cancellation by auto-zeroing

3.5.3 Integrate-and-Dump Filter Design

The integrate-and-dump filter used is shown in Fig. 3.13. During ϕ_1 and ϕ_2 , the circuit operates as a SC integrator. On ϕ_{dump} , C is discharged and now the circuit is ready to start integrating again. ϕ_1 and ϕ_2 operate at the sampling frequency and ϕ_{dump} is obtained from the timing-clock recovery circuit. The functionality of the integrate-and-dump design has been verified using SPICE and the time-domain simulated results are presented in Appendix D.

3.6 Integration of the BDD

A CMOS $3\mu\text{m}$ double metal layer technology has been used to fabricate the analog blocks of the baseband system through the Canadian Microelectronic Corporation (CMC) at Northern Telecom. A semi-custom cell-library technique was adopted for the layout using Carleton's University analog/digital standard cell library.

Figure 3-13: Integrate-and-dump filter .

In laying out SC circuits with previously untested circuitry and/or fabrication process, it is useful practice to include test-circuit versions of the SC circuits on the first chip. The resistor equivalent method was also used to design the test-circuit versions of the SC circuits. After verifying the functionality of the fabricated test-chip, the designer may proceed to the design of the BDD. The implementation of the BDD underwent two design stages. First, the digital timing recovery circuits and analog circuits were implemented on separate chips. After testing the functionality and performance of the separate chips, an integration of the digital and analog circuits onto one chip proceeded. But before discussing the implementation, some layout considerations of SCN are reviewed.

3.6.1 Practical Considerations for MOS SCN Implementation

Integrated circuits to some extent are sensitive to the physical arrangement of its components and their interconnections. Analog ICs are more sensitive than most others. Hence, some basic key points concerning the optimal arrangements (layout) of SC circuits will be the next focus of discussion.

Some of the performance parameters which are often strongly affected by the layout are the following:

1. noise injection from power lines, clock lines, and ground lines
2. noise injection from substrate
3. clock feedthrough noise

4. absolute and matching accuracy of circuit elements used
5. rise time and overshoot, or (equivalently) the high frequency response of the circuit
6. sensitivity to process variations
7. op-amp offset voltages

In preventing noise injection from the power, ground, and clock lines, two precautions of equal importance should be observed. The first is that these lines be kept free from noise and secondly minimize the noise coupling from the lines into the signal path. For chips containing both analog and digital circuitry, which is an increasingly common situation, the first requirement is especially important. Consider the system shown in Fig. 3.14 where both the analog and digital sections are fed by the same positive (V^{dd}) and negative (V^{ss}) bias voltage and both sections also use the same bonding pads and power lines. The positive supplies of both sections share a common resistance R^{w1} , which carries the supply current of the analog section (i_a) as well as that of the digital one (i_d). Due to the switching transients of the digital logic circuits, the digital supply current i_d typically contains some asynchronously recurring large noise spikes. The common resistance R^{w1} consists of the output impedance of the outside power supply providing V^{dd} , the resistance of the bonding wire and bonding contact, as well as the shared portion of the on-chip power line. The line voltage at the analog section will be therefore $v^+ = V^{dd} - (i_a + i_d)R^{w1}$. Hence, the spikes in i_d will appear (multiplied by $-R^{w1}$) in v^+ . The resulting noise is often intolerable for the analog circuit since it has both a large amplitude and a wide bandwidth, leading to noise aliasing effects. The same effects, of course, hold for the negative power supply.

The analog supply noise can be suppressed by considerably reducing the values of the shared resistance R^{w1} and R^{w2} . This can be achieved by using separate (dedicated) power lines for the analog and digital circuitry. Further improvements can be achieved by also using separate bonding pads for these dedicated lines, connected to the same outside pin or in an optimal arrangements, using separate pins as well, which are short-circuited externally. In the latter arrangements, the output impedance of the external supply is the remaining common impedance of the analog and digital lines. This residual impedance can be reduced to a very low value and the spikes noise essentially eliminated by using external decoupling capacitors at the pins. Under these circumstances, the bias voltage lines for the substrate and wells can also be connected to the analog supply pads without introducing

Figure 3-14: Power distribution for I.C. containing both analog and digital circuits.

any digital noise into the substrate or wells. These substrate bias lines must have as many contacts to the substrate (or well) as possible. The purpose of these contacts is to collect the electrons or holes injected into the substrate (or well), keep the substrate (or well) at a fixed potential and thus prevent the occurrence of latch-up, a fatal problem which can

effect CMOS ICs.

To prevent some crucial signal or clock lines either from picking up or injecting noise, they can be shielded from their environment. A possible shielding arrangement for a metal line is shown in Fig. 3.15, where the shield consists of two grounded metal lines and grounded polysilicon layer. Such shielding can also be used to separate the analog and digital circuitries, and to prevent noise from coupling into or out of the substrate.

Figure 3-15: Shielding arrangement for a metal line .

Noise injections from power-supply lines can easily occur in the op-amps and the resulting noise depends on the power-supply rejection ratio PSRR of the op-amp. The low frequency noise usually enters only via the bias circuit and through the asymmetries of the input stage, while the high frequency noise may enter through the stray capacitances and the output stages as well [32]. Some techniques which have been considered in the design of the op-amp in the Carleton University Standard Cell Library [42] for reducing these effects are fully differential circuitry , cascode input stages , supply independent biasing, etc.

Power line or clock line noise can also enter into the signal path through the switches. To illustrate this situation, consider Fig. 3.16, where the switch is assumed to be realized by a CMOS transmission gate. The overlap capacitance of the gate-to-source and gate-to-drain are also shown. Any noise in the four clock signals ϕ_1 , $\overline{\phi_1}$, ϕ_2 , $\overline{\phi_2}$ will be coupled to the output voltage v_{out} of the op-amp with weighting factors C_{ovm}/C_2 or C_{ovp}/C_2 . In designing the clock generator, the reduction of digital noise in the signals ϕ_1 , $\overline{\phi_1}$, ϕ_2 , $\overline{\phi_2}$ should be considered [32], hence a reduction in the coupled output noise.

Another important noise source is due to coupling from the substrate. This effect can

Figure 3-16: Coupling paths from the clock sources to the output .

by reduced by minimizing the noise coupling into the substrate as well as out of it. A number of techniques [32] may be used to reduce this effect.

The inverting input terminals of the op-amp are also susceptible to substrate noise and steps should be taken for protection. The lines connecting the input nodes to any capacitors and switches should be as short as possible. These lines should be either polysilicon or (preferably) metal; the use of diffusion lines must be avoided here because they are too closely coupled capacitively to the substrate. The crossing of input-node lines with any other signal-carrying lines (analog or digital) should be avoided. Whenever possible, the input lines should be shielded (although this may not be necessary for very short lines), and guard rings should be used to shield the input devices of the op-amp.

It is known that considerable capacitance exists between the substrate and the op-amp nodes hence ;

- i) circuitry connected to input node should be minimized
- ii) switch dimensions ideally should have the minimum value allowed by the resolution of the technology
- iii) dedicated low-noise bias voltage supplies for the p-wells and the substrates.

The layout geometry of the op-amp has important effects on its rise time, overshoot, and high frequency response as well as on its sensitivity to process variation and its offset voltage. Some of the considerations to achieve a nominal design of the op-amp can be found in [32].

On a chip containing many op-amps, switches and capacitors, it is usually efficient to

arrange these components in separate areas on the chip. Thus, all op-amps may occupy one row, all capacitors a second one, and all switches a third, with the supply and clock lines running in parallel along the edges. A possible arrangement is shown in Fig. 3.17. All the n-channel switches share a p-well biased by a separate analog negative supply voltage V_- . Separate ground lines are used for the non-inverting op-amp input terminals and the switches. The voltage supply lines (V^+ , V_- , ground) used by the op-amps and switches run along the upper and lower edges of the rows they occupy respectively.

Figure 3-17: A typical layout for a switched-capacitor circuit .

This layout is useful not only for SCF but for any switched-capacitor circuit including

gain stages, rectifiers, oscillators, modulators and so on. There are, however, alternative arrangements described in [32].

3.6.2 Test-Circuit and BDD Integration

The test circuits included on the chip was a biquad SC low/high pass filter and a SC integrate-and-dump filter. The biquad configurations for the low/high pass filter and the integrate-and-dump filter are the same as those shown in Fig. 3.11 (a,b) and Fig. 3.13 respectively. These filters were designed to meet the specifications of the LPF and HPF mentioned in section 3.5.1. See Appendix D for the SPICE analysis of these filters and their deviations from the designed specifications.

The layout of the test-circuit, which was performed manually, is shown in Fig. 3.18. The nonoverlapping clock generator for the switches and the biasing voltages for the op-amps are supplied externally to the chip. These circuits exists as analog standard cells in the library but at the time of submissions, they hadn't been tested. Hence, to ensure a greater chance of functionality, they were not included on chip and this should in no way degrade the performance of the filters.

The layout was carefully designed in order to achieve highly accurate performance and very low noise levels. For example by using the typical layout for SCN shown in Fig. 3.17, the lengths of interconnections are minimized, thus reducing stray capacitance and also a saving in area. Several shielding techniques were also employed in the design to prevent some crucial signal or clock lines from picking up or injecting noise.

The demodulator was manually laid out on a 30-pin pad-frame. The floor plan of the chip is shown in Fig. 3.19 and a plot of the layout is shown in Fig. 3.20. The chip area is 4.5 mm by 2.2 mm.

This layout includes both analog and digital circuitry with the analog section in the lower half and the digital portions in the upper half of the chip. To prevent noise created in digital circuits, which arises during switching transients, from contaminating the analog circuitry a P^+ and N^+ shield surrounds the analog circuitry. The purpose of this shield is to attenuate the digital noise coupled from the substrate. An explanation of this noise source is as follows. The P^+ diffusion nodes of CMOS digital circuit, e.g. drains of pMOS transistors, may rise beyond the potential V_{dd} during switching transients. Since the n-type

Figure 3-18: Test-circuit layout.

substrate is biased at V_{dd} , a $P+$ diffusion at a potential higher than V_{dd} will inject minority carriers (holes) into the substrate. A guard structure which surrounds the analog circuits as shown in Fig. 3-21 helps to attenuate minority carriers from reaching the sensitive analog circuits. A collector guard structure which is based on the design of lateral p-n-p transistor is shown in Fig. 3-22a.

The emitters are the digital $P+$ nodes which are likely to rise beyond V_{dd} . The P -well serves as the p-type collector. The n-substrate is the parasitic base of the lateral p-n-p transistor biased at V_{dd} . It is desirable to have the substrate biasing structure running in parallel with the P -well, as shown in Fig. 3-22a, to keep the substrate biased solidly at V_{dd} potential. Thus minority carriers injected by the $P+$ emitter are intercepted by the P -well collector before they reach the analog circuits. The guard structure should also have as many contacts to the substrate as possible to achieve an equal potential along the

Figure 3-19: Floor plan of the demodulator chip.

Figure 3-20: Layout of the demodulator chip.

structure.

In addition, power supply and analog ground lines are independently wired for both portions and they are also separated by shields. From the layout, one can see that each

Figure 3-21: Analog circuit guard ring structure.

of the blocks constituting the system has its own input/output pads. The reason for this strategy is to make debugging and testing easier and therefore improve the probability of success of the next implementation, an internally connected BIDD layout.

3.7 Summary

This chapter dealt with phase IV and phase V of the IC design cycle described in Appendix A; the circuit design and the layout phases respectively. Since it was decided that the analog circuits would be implemented using switched-capacitor techniques, some approaches for synthesising SC filters were examined. The issue of aliasing and its preventions were also addressed. A study of the noise found in switched-capacitor networks was analyzed with the aid of the simulator SPICE. This noise analysis can help the designer to determine the dominant noise sources and thus design a better performance circuit.

The analog circuits of the baseband system which include a BPF, slicer and an integrate and-dump filter were designed using SC techniques to meet the specifications obtained from

(a) Cross-Sectional View

(b) Top View

Figure 3-22: Guard ring structure.

the high level system simulations. The simulator SPICE was used to analyze the frequency and/or time domain performance of the analog circuits.

Since there had not been any pre-tested switched-capacitor circuitry in the cells available in Carleton's cell library, it was useful practice to include test-circuit versions of the SC circuits on the first chip. This test chip included a Butterworth biquad LPF, HPF and an integrate-and-dump filter. Also a layout of the mixed analog/digital baseband system has been submitted for fabrication. The strategy in this layout was to make debugging and testing easier. All the layouts were carefully designed to achieve highly accurate performance and very low noise levels.

Chapter 4

TEST RESULTS

4.1 Introduction

This chapter discusses the experimental results of the fabricated test-circuit shown in Fig. 3.18. The measurements consisted of time and frequency responses and also a noise power spectral density response (PSD) for the switched-capacitor noise found in the filters. A correlation between expected, based upon simulations, and experimental results can then be made.

4.2 Measurements

The floor plan and test set-up for the test chip of the SC circuits is shown in Fig. 4.1. Power supply voltages of +2.5 and -2.5 volts were used for Vdd and Vss respectively. A series of resistor voltage dividers were used to provide the desired bias voltages for the op-amps. A data generator (HP 8180A) was the equipment used for generating the off chip non-overlapping clocks $\phi_1, \overline{\phi_1}, \phi_2, \overline{\phi_2}$ and $\phi_{dump}, \overline{\phi_{dump}}$ for the switched-capacitor circuits. A spectrum analyzer (HP 3585A) was used to measure the frequency responses and noise power spectral density of the filters.

4.2.1 Time and Frequency Response

The measured frequency response of the filters is shown in Fig. 4.2. Cascading the LPF and HPF externally enabled the measurements of the bandpass filter response. Comparing these responses with the expected results shown in Appendix D, shows almost exact agreement.

Unlike the LFP, HPF, and BPF, time domain measurements was used to verify the operation of the integrate-and-dump (I-D) circuit. Recall, the function of the I-D circuit (see Fig. 3.13) is to integrate the input signal and then reset (i.e. dump the existing charge on the integrating capacitor) the output so that it is ready to start integrating again. Fig. 4.3 shows the clocking scheme to test the operation of the I-D circuit. Prior to the end of

Figure 4-1: Test set-up

a

b

Figure 4-2: Measured magnitude response of filters on test chip; (a) low-pass, (b) high-pass

Figure 4-2 cont d: (c) bandpass

the bit period T , the I-D circuit should reset so that integration for the next bit period can commence. Figure 4.4 shows the input signal being integrated for some time before being reset therefore verifying the operation of the I-D filter.

Figure 4-3: Clocking scheme to test integrate-and-dump circuit.

4.2.2 Noise Measurements

With the switches turning on and off and the input pin connected to analog ground (0 V), one can measure the output noise power spectral density response of a SC network. Fig. 4.5 shows a comparison of the expected and measured PSD of the SC filters. The shapes of the measured PSD response for the filters resemble those obtained from simulations. There is some discrepancy in the magnitudes between measured and simulated filter responses. Further investigation for this discrepancy requires some attention but was beyond the scope of this thesis. The results do however demonstrate the validity of the noise models developed for the simulator SPICE.

4.3 Summary

The measured results presented in this chapter showed that the test-circuit integration was a complete success. The frequency and time responses measured corresponded very

Figure 4-4: Measured results of the integrate-and-dump circuit: (a) positive DC input, (b) negative DC input

closely with the expected results obtained via simulations. Even though the magnitudes of the measured SC noise responses differed slightly with simulated (using SPICE models which I have developed), they can however be used to predict the SC noise found in SCN. The SC noise found in SCN is an area that deserves more attention.

Figure 4-5: Measured noise power spectral density of SC filters; (a) low-pass, (b) high-pass

Figure 4-5 cont'd: (c) bandpass

Chapter 5

SUMMARY

A mixed analog/digital baseband data demodulator chip for a mobile receiver has been implemented using a hierarchical design methodology. A semi-custom standard cell approach was adopted and a mixed analog/digital CMOS 3μ standard cell library was designed/tested to support the IC methodology.

A mixed analog/digital design was selected to satisfy the two basic requirements for a mobile radio system namely minimizing power consumption and physical area. It was decided that the analog section perform the signal processing functions which were designed using switched capacitor techniques and that the timing recovery circuit be a digital design.

In order to evaluate the system more accurately, analytical expressions other than the limited expressions given in literature, were derived. To verify the functionality and evaluate system performance in the early stages of the design, great emphasis was placed on the high level simulations. The high level simulation models were developed based upon theoretical analysis of the system. All the models developed can be used as building blocks to analyze other telecommunication systems. We found the high level simulator, Carleton's University modified version of SPLICE (CUSPLICE), a powerful tool which was a useful aid for the design of mixed analog/digital systems. It gave a good visual indication of what takes place within the receiver and the model developments and verifications is relatively straightforward.

The analog circuits were designed using switched-capacitor techniques and analyzed using the simulator SPICE. Noise models for SPICE were developed to analyze the switched-capacitor noise found in these circuits. These noise models proved to be reasonably accurate in predicting the noise found in switch-capacitor noise.

Two test chips, one containing the analog blocks and the other the digital blocks of the baseband system, have been designed and fabricated using a 3μ double metal layer CMOS technology. Tested results showed full functionality of each block and their performance closely agree with simulated results. The measured noise performance of the analog elements

also showed agreement with simulated results.

The obtained test results has validated the IC design cycle ,described in Appendix A. The test chip circuit was designed and tested in 6 months, a rather quick time considering that the turnaround time for the chip was over 3 months.

A single BDD chip has been submitted but at the time of submitting this document the fabricated chip was not available for testing purposes. The physical size of the single chip is approximately $8mm^2$. It is expected that the BER performance of the single chip will closely agree with simulated system BER performance.

Also from this research a paper titled A CMOS LSI Baseband Demodulator for a Mobile Radio Receiver has been presented at the 1988 CCVLSI conference held in Halifax, Nova Scotia.

5.1 Future Research

A challenging task will be the testing of the single chip BDD. The BDD chip was partitioned into individual blocks with its inputs and outputs accessible externally to the chip. This allows the designer to test each individual blocks for functionality and performance, to observe the interaction of analog/digital circuits on the same chip , and to test and verify the performance of the baseband system by externally connecting each individual block making up the baseband data demodulator.

This task has been undertaken by a summer student and results were not available at the time when this document was submitted. However, functional tests of the individual blocks were performed. An even more challenging task is to compare simulated BER performance with measured BER using those inputs generated for the simulations. The input signal and noise generated for simulation purposes can be converted to a real time analog signal using a digital-to-analog converter. This noisy analog signal would then be the input to the baseband system chip. A better correlation between simulated and measured BER performance can be obtained using this method.

There is an on going effort to develop more analog/digital cells for the CMOS 3μ double metal layer technology standard cell library at Carleton University.

5.2 Application

Since the baseband data demodulator was designed as an application specific integrated circuit (ASIC), its main area of application is for a mobile radio receiver. However, the internal individual blocks of the baseband system, which are now macro cells in the standard cell library, can be used as building blocks for other telecommunication ASICs.

Appendix A

IC Design Methodology

This appendix deals with the design methodology used for implementing the system directly in silicon. It also examines the two design approaches (full custom, semi-custom) and discusses reasons for adopting the standard-cell semi-custom approach. Finally, the development of the standard cell library is described.

IC Design Cycle

The extreme approaches in IC design are fully manual and fully automated design. Computer aids for design have been developed on the basis of these extremes. One approach is to aid the designer in the evaluation of his work and to take over from him the more tedious and routine tasks. This is usually referred to as Computer Aided Design (CAD). A different approach attempts to completely replace human tasks by computerized counterparts. This latter situation is known as design automation.

There is a significant difference between the two approaches. Manual design assisted by CAD can yield highly optimized results at the cost of long design time. Automated design, at present day, leads to much less efficient solutions because of the restrictions imposed by the automatic tools, however the design time is considerably reduced. Taking into account the available resources at Carleton, a manual design assisted by CAD was selected. A design methodology for this approach [43] is shown in Fig. A.1. The creation of a new design specification refers back to a previous one if one does exist, the circuit structure is created with reference to the system definition, and the layout is created with reference to the circuit structure. As shown in Fig. A.1, manual design and CAD tools are used at the different hierarchical levels to obtain the expected performance. It is also worth mentioning that both the system and circuit level structures also exhibit hierarchy.

The problem specification is usually stated by the system engineer. It is important that a complete understanding of design objectives be reached between the VLSI and the system engineers early in the cycle to avoid later implementation failure. The system

Figure A.1. Manual design assisted by computer aids

requirements should spell out the interfacing specifications , functionality needed from the device and speed requirements. In the case of high performance/high speed analog circuitry the technology related limitations have to be considered as well. Therefore it is also important to establish , at the start of the cycle , what VLSI technology (NMOS,CMOS etc) and design technique (gate array, standard cell, full custom etc) will be used.

Device testing consideration should be included early in the design process. Previously the most neglected area, chip testing must begin during the chip-design phase and continue through to fabrication. To design for testability, precautions should be taken against designing circuits that cannot be tested. These include defining test methods and deciding on overall test strategy.

The next phase is the design of the overall system structure which will fulfill the specifications outlined in the previous level. The overall system can be broken down into a number of subsystems each having their own requirements. The subsystems can be further broken down into a number of building blocks which in turn can be broken down further into smaller entities and so on. The smallest entity within a building block is referred to as a cell , an element from a cell collection called a standard cell library. This demonstrates the hierarchy within the system structure level.

A subsystem being the baseband data demodulator was considered first. The simulation

tool used to model the behaviour of this subsystem without decomposing it all the way down to individual transistors was Carleton University's modified version of SPLICE. The simulation and modeling at this level involved the use of delay and timing equations and technology-dependent parameters to enable the designer to evaluate the design at this early stage.

Following the system structure is the the circuit design of the building blocks ,whose specifications were optimized from the high level simulation. Once the circuit is designed, it is analyzed, using simulation tools, to obtain information about the expected performance. Once again, within this hierarchy there exists different levels of hierarchy. For digital circuits, there are three different levels of simulations ;

- i) circuit
- ii) gate/logic
- iii) switch level

Circuit simulation is an electrical simulation of the circuit giving accurate waveform analysis of electrical voltage and current signals. As chip size increases , the time and memory requirements of such simulation become prohibitive. Simplified models can be used to reduce the time and memory requirements.

If the speed of the circuit simulator is insufficient for the analysis of the circuit blocks under consideration, one can use gate/logic level simulators. These types of simulators, deal with logic gates rather the resistors, capacitors, and transistors. The signals are represented as discrete logic states rather than voltages and current waveforms.

A good compromise can be achieved between logic level simulators, where the simulation is fast but modelling and accuracy are a problem, and circuit simulators, where modelling is more precise but the simulation although accurate is time consuming. This is the switch level simulator.

In the case of analog circuits, only a circuit level simulator can provide accurate waveform analysis of voltage and current signals. Typically, it also performs frequency domain and noise analysis.

Once the circuit design of each block has been verified, the designer is ready for the layout design. Knowing the area of the standard cells which includes the input/output pads

and allowing area for routing, the area occupied by the chip may now be estimated. The area to route signals in a standard cell design takes usually 50-80 percent of the total chip area [44]. An approximate size of the chip before layout can therefore be estimated by taking the combined area of the standard cells and multiplying by a factor of 3 to 5. This will determine the size of the standardized pad frame needed and in turn the maximum number of pins which can be used. The overall chip floor plan can now be laid out using the estimated areas of each block. Based on the above considerations the design may be restricted either by area or pin count of a specific pad frame. If it has been determined that the dominant limitation is the area the circuit blocks and/or the system requirements need to be modified. If limited by pin count, then input/output may be multiplexed to overcome this restriction.

The designer is now ready to proceed to the layout phase. The cell layouts in the standard cell library are called into a layout editor and are interconnected according to the function of the block under consideration. The layout can be checked for any design rule violations (minimum dimension, spacings, etc) using the design rule checker (DRC). An extractor is then used to extract from the layout the building block, parameters and their interconnections. This netlist is then compared with circuit netlist obtained in the circuit development phase. A simulation of the extracted layout is then performed and compared with that of circuit simulation. In the case of discrepancy, the designer must correct the circuit.

Once the design of all the building blocks has been completed, the blocks are interconnected to form the entire chip layout. The I/O pads are called into their appropriate locations and the power rails are laid out to supply each block with the required voltage levels. The overall chip layout can now be checked for any design rule violation using the design rule checker.

The Caltech Intermediate Form (CIF) files are sent for masks preparation and silicon fabrication currently through Canadian Microelectronics Corporations (CMC) to Northern Telecom Limited.

Design Approach

In designing integrated circuits there are two design approaches for design

i) full custom

ii) semi-custom

In literature on microelectronic design, the terms custom, full custom, and semicustom may be found with possible varying meaning. Here, the terms are defined as follows

Custom design (or custom specific design, or application specific design) A microdesign to suit the needs of a particular customer's requirement in contrast with off-the-shelf standard items in volume production. Following below are two broad categories that custom design may be divided into.

Full Custom Design The custom design of a particular customer's requirement, using hand crafting or CAD at device level to achieve the smallest silicon area and highest efficiency design possible.

Semi-Custom Design The custom design of a particular customer's requirements, using more expeditious means of design than full custom, namely cell library or gate array.

Full Custom

In a full custom design approach, the objective is to produce the most efficient final design on silicon possible within given time or cost constraints. For full custom design, the circuit and layout design require the expertise in detailed design of gate structure, and interconnect topology at the silicon level. The economics of semicustom is an evolving situation and hence, a full custom design is only justified for very large quantity requirements. Further detailed information is available in literature [45], [46], [47], [48].

Semicustom

The main semicustom design routes are namely (1) the cell-library approach, and (2) the uncommitted masterslice (or masterchip) approach. The distinguishing difference of these two alternatives is that a full mask set has to be generated for the production of cell-library design circuits, but only the final interconnection masks have to be generated for masterslice circuits.

A prerequisite for the cell-library approach is that there should already be available a set of proven standard circuit designs such as gates, latches and other functional entities from which the specific custom requirement may be assembled. A complete monolithic

integrated circuit is assembled by connecting together appropriate cell designs.

The economic advantage in the semicustom cell-library approach compared with full custom design is in the elimination of the costly manpower involvement in the detailed silicon design at the transistor level. A disadvantage is the final silicon area of a cell-library design may be 30-50 percent larger than a corresponding full custom design.

A problem with the cell-library approach is the updating of all the designs in the library which may become desirable or necessary because of changes in fabrication technology. Thus, the extra costs must ultimately be reflected in the final price of the custom design product. Further general details of semicustom design techniques may be found in published literature [46], [47], [48], [49], [50], [51].

The alternative "masterslice" semicustom approach has many possible technical variations. The terminology associated with this area is also somewhat diverse and nonstandardized. The essential feature of all masterslice (or "masterchip") semicustom realizations in the a standard LSI circuit is an uncommitted array of identical cells. They may be fabricated up to but excluding the final metalization interconnect. The custom dedication of such a standard array lies in the design of the final interconnection metalization, which will be unique for every customer's requirement. Hence, the uncommitted masterslice wafers may be fabricated in quantity and held in stock to await final specific dedication.

The diversity of commercial masterslice products and the associated terminology arises from the number of choices of circuit which may be used as the standard cell in masterslice array. Two initial choices are available, (1) whether to provide cells containing uncommitted components such as separate transistors, or (2) to provide cells which are each a fully functional entity such as NAND or NOR gate.

From the preliminary discussions, it may be apparent that the masterslice approach should provide the quickest and most inexpensive route to design and fabrication of a custom LSI circuit, since all the levels of design and fabrication except the final on-chip interconnection are standard. This is generally true, although decreasing CAD costs and commercial interests may change tradeoffs between masterslice and cell-library design costs. However, the masterslice approach cannot provide such efficient circuit as the cell-library approach, when (1) minimization of chip size and (2) optimization of performance are considered. This is because one has to use a particular array size on a masterslice, but

which is likely to contain unused cells in the final design. This in contrast to the cell-library approach, where only the required circuits (macros) are assembled on the chip, and spacing between the circuits is only that required for the specific interconnections rather than predetermined fixed width wiring channels as on uncommitted arrays. Further details of masterslice arrays have been published [46], [47], [48], [49].

Constraints and Limitations

Apart from economic factors, there are other constraints and limitations which dictate whether custom or semicustom circuits shall be adopted for a particular application. The two main factors for VLSI designs at Carleton University are (1) the time factor since designer has a limited time to obtain degree and (2) restrictions imposed by the fabrication facility. Certainly if very quick turn around time is necessary, full custom would be ruled out, and semicustom is the avenue which we considered. Since the masterslice approach is not supported by the foundry, Northern Telecom, this rules out masterslice and hence a cell-library approach was adopted.

Standard Cell Library

A CMOS3 standard cell library has been developed featuring both digital and analog cells which can be used for mixed-mode integration. The library cells were initially designed using Northern Telecom 3-micron CMOS technology. Each cell in the library was characterized using SPICE circuit simulator and the digital cell performances were compared with a commercially available library (Canadian Semiconductor Design Association (CSDA) 3-micron standard cell library). A comparison of cell widths (see Table I) show that the cell widths of Carleton's library are generally smaller than the CSDA cell widths.

The cells were later adopted for the Northern Telecom 3-micron double-metal CMOS technology. Each cell was designed to be compatible with auto-place-and-route (APAR) packages and hand layout techniques. A complete list and description of all the standard cells available in the library is currently being documented.

Design Strategy

Fundamental decisions such as device sizes and beta ratios were made early in the cell development stages. To minimize the propagation delay, the beta ratio (W_p/W_n) was

(in microns)	CMOS3	CSDA
INVERTER	27	27
2-INPUT NAND	36	36
2-INPUT NOR	36	36
2-INPUT XOR	72	81
D-FLIP FLOP	117	135
D-LATCH	63	81

Table A.1. Cell widths comparisons. *Note: the cell height is the same for CMOS3 and CSDA cells.*

determined based on the relative effective mobilities and channel length of the P-channel and N channel transistors. An optimized value for beta in regard to propagation delay time independent of the size of the successive gate is achieved when beta is equal to square root of the ratio of hole mobility to electron mobility [52], [53] The optimum beta ratio for the Northern-Telcom CMOS 3 micron technology is approximately 2:1.

Basic Cell Structure

The basic cell structure of a standard cell is shown in Figure A.2 [52], [54], [55]. There are metal power buses located at the top and bottom of the cell with device areas inbetween. A row of P-channel devices are placed above a row of N-channel devices. Cells are to be placed side by side so that the power buses align. All I/O (polysilicon) terminals are accessible from the top and bottom of each cell. Each cell has its own V_{dd} and V_{ss} substrate/well contact(s) so that a cell can "stand-alone" without requiring adjacent cells to make substrate/well connections.

Figure A.3 shows the constraints on the placement of various layers within a cell. Following these rules when designing the cells allows other cells to be butted together without violating any of the design rules. Note that the dimensions given are 5 micron design scale which are reduced to 3 micron design rules by a 60 percent scaling factor. It also shows no metal 2 within the cell since metal 2 is reserved for routing.

Figure A.2. Digital cell structure.

The cell structures and terminal locations were defined to be compatible with common commercially available automatic placement and routing software. A grid unit of $16\ \mu\text{m}$ was selected to permit unrestricted placement of vias and contacts at every grid point (see Fig. A.4).

Some of the more often used cells were fabricated and tested. The results from the testing can be found in Appendix B.

Figure A.3. Design rule constraints within the cell (5μ design rules)

Fig. A.4. Grid unit definition

Appendix B

Standard-Cell Test Chip Results

The goal of designing this chip is to verify the functionality of some of the primitive combinational gates (minimum size inverter, 2-input NAND, 2-input NOR), D-type flip/flops and input/output pads, and to compare with the simulated propagation delays (obtained using SPICE (level 2)). This appendix includes the methods used for measuring the propagation delays as well as the tested results of the cells implemented on the test-chip. Ten chips in total were fabricated and tested.

Combinational cells

The propagation delays of primitive logic gates (minimum size inverter, 2-input NAND, 2-input NOR) are obtained by connecting the gates in an ring oscillator structure as shown in Fig. B.1. The length of the ring oscillator is 25 inverting gates. Two identical rings of the same gate but with different fanouts are implemented to obtain propagation delays as a function of fanouts. The first ring has a fanout of one; and the second one has a fanout of five. Propagation delay is determined by

$$\tau_{delay} = \frac{1}{f_{osc}} \frac{1}{2} \frac{1}{25} \quad (B.1)$$

where f_{osc} is the oscillation frequency of the ring undertest. Oscilloscope traces of the inverter, 2-input NAND, and 2-input NOR ring oscillator outputs are shown in Fig. B.2a, Fig. B.2b, and Fig. B.2c respectively and the average propagation delays measured are tabulated in Table B.I.

The simulated and measured average propagation delays as a function of fanouts for the primitive gates tested are shown in Fig. B.3. Simulated propagation delay at one fanout has been normalized as one Td unit in the graph. Based on the results obtained, the measured propagation delays are on the average are 20% higher than the simulated results, and the deviation of the measured results among the ten chips tested varies by $\pm 10\%$ of the mean values.

Two identical ring oscillators were designed for each gate type. The first ring does not have the capacitor "C" connected; the other one does. Capacitor "C" is equivalent to four fanout units.

Figure B.1. Ring oscillator structures.

One possibility for the 20% difference between the simulated and measured results could be caused by the fact that the transistor models for simulation contain typical process parameters which are different from the actual process parameters for the fabrication of the test chips. Another source of error is in the estimation of routing capacitance at the output node of each gate used in the simulation (i.e. the edge capacitance of the routing was not included). Also, the capacitance varies depending on the physical layers on which the routing lies above. Whereas for the $\pm 10\%$ deviation among the mean measured value, this could be caused by the variation in processing parameters across the silicon wafer.

Cell	Description	Fanouts	Delay
CINV01	min. inverter	1	1.3 ns
CINV01	min. inverter	5	2.5 ns
CNAN02	2-input nand	1	1.6 ns
CNAN02	2-input nand	5	3.2 ns
CNOR02	2-input nor	1	1.9 ns
CNOR02	2-input nor	5	3.7 ns

1) the measured results are the average of the delays obtained from ten chips

2) $V_{dd} = 5V$

Table B.I. Measured propagation delays of primitive gates.

D-type flip/flop's

A 4-stage ripple counter as shown in Fig. B.4 is used as the test circuit for the flip-flop cells. The counter is made up of master JK-FF with Q and $\overline{Q}$ fed back as inputs. The CLK input is provided by a medium-power inverter cell (CINV03). The propagation delay is obtained by measuring the delay from $A0$ to $A3$. Propagation delay from CLK input to Q is

$$\tau_{delay} = \frac{\text{Delay from } A0 \text{ to } A3}{3} \quad (B.2)$$

The estimated fanout of the Q output is 10. Two ripple counters were designed. First counter was implemented using set/reset JK-FF's (CDFF04); and the second counter used reset JK-FF's (CDFF02). The set and reset inputs of the FF's were tested and found to be functional. The measured and simulated propagation delays are tabulated in Table II. Both counters are operational at an input clock frequency of 25 MHz. Figure B.5 shows the oscilloscope traces of the flip-flop $A0$ output clocked by a 25 MHz input.

Other standard-cells which have been tested to be functional includes exclusive-OR, exclusive-NOR, and passgates. Propagation delay (τ_{delay}) as a function of V_{dd} was also examined; and the results are shown in Table III. The results indicates that τ_{delay} is inversely proportional to V_{dd} ; that is

$$\tau_{delay} \approx K \frac{1}{V_{dd}}. \quad (B.3)$$

This is in agreement with the approximation for propagation delay given by [56] which

Figure B.2. Measured ring oscillator output waveforms.

Figure B.3. Propagation delays versus fanouts .

Figure B.4. Four-stage ripple counter.

Cell	Description	Fanouts	Delays (measured)	Delays (simulated)
CDFF02	D-FF w/ reset	10	7.2 ns	5.6 ns
CDFF04	D-FF w/ reset & set	10	8.1 ns	7.0 ns

- 1) the measured results are the average of the delays obtained from ten chips
 2) $V_{dd} = 5V$

Table B.II. Measured and simulated propagation delays (from CLK to Q) of D-Flip/Flop.

states

$$\tau_{delay} \approx \frac{C_L}{V_{dd}} \left(\frac{1}{\beta_p} + \frac{1}{\beta_n} \right) \quad (B.4)$$

where C_L is the capacitance at the output and β_p and β_n are the transconductance gain of the pMOS and nMOS transistors respectively.

The ten standard-cell test chips were tested to be fully functional. Based on the above observations, the standard-cell designs proved to be successful and the cells displayed good performance. An IC designer can now be confident that his design implemented using the

Vdd	delays	K = delay * Vdd
5.0 V	1.3 ns	6.5 V ns
4.5 V	1.4 ns	6.3 V ns
4.0 V	1.6 ns	6.4 V ns
3.5 V	1.9 ns	6.6 V ns
3.0 V	2.3 ns	6.9 V ns

Table B.III. Propagation delays of CINV01 as a function of Vdd.

Figure B.5. Measured output waveform of divide by 2 counter.

Carleton CMOS3 standard-cells has a high chance of functionality.

Appendix C

SPLICE User Defined Models

The development of the time domain simulation models for the phase signal and phase noise found in Manchester coded narrow-band digital fm with discriminator detection, and a 2nd order low-pass filter is presented in this appendix. Two approaches for generating the phase noise are given. One of the approaches will include the development of a noise generator which will generate noise to fit any distribution provided that the mathematical expressions for either the probability or cumulative density function is given. Equations C.3, C.4 and C.5 are personal contributions from my partner (T. Luk) and the author of this thesis.

Filtered Signal Phase Model Development

Following Cartier [57] , the assumption is made that only the two bits adjacent to the bit under consideration have any effect upon the bit since the transient response due to bits further away would have died out.

Based on the above assumption , given a "0" for the bit under consideration , there are only four combinations which exist ; 000 , 001 , 101 , 100 . These 3-bit patterns are used to derive the Fourier series of $\sin\theta(t)$ and $\cos\theta(t)$.

It has been determined that the optimum performance for Manchester coding is achieved with a time-bandwidth product $BT \approx 2$ and a deviation ratio ≈ 1 [57] and these were the values used for those equations dependent upon them.

Case I : *All zeroes bit pattern " 000 "*

In the case of " all zeroes " bit pattern , the data phase , $\theta(t)$, after FM demodulation is a triangular wave of a period T with zero mean value (see Fig. C.1).

The Fourier Series of $\sin\theta(t)$ and $\cos\theta(t)$ are

$$\sin\theta(t) = \sum_{n=1}^{\infty} a_n \cos(2\pi n f_1 t) \quad (C.1)$$

2

OF/DE

2

METRO

Figure C.1. The data phase signal for the all zeroes bit pattern.

and

$$\cos\theta(t) = A_o + \sum_{q=1}^{\infty} a_q \cos(2\pi q f_1 t) \quad (C.2)$$

where

$$a_n = \frac{4h}{\pi} \cos\left(\frac{\pi h}{2}\right) \frac{|\sin(\frac{n\pi}{2})|}{\pi^2 - h^2}$$

$$a_1 = \frac{4h}{\pi} \sin\left(\frac{\pi h}{2}\right) \frac{|\cos(\frac{\pi}{2})|}{\pi^2 - h^2}$$

$$A_o = \frac{\sin(\frac{\pi h}{2})}{\frac{\pi h}{2}}$$

$$h = 2\pi f_d T \text{ and } f_1 = 1/T$$

Case II . Alternating " one - zero " bit pattern

In this case , the data phase signal , $\theta(t)$, after FM demodulation is a triangular wave of period $2T$ with zero mean value (see Fig. C.2) .

The Fourier series of $\sin\theta(t)$ and $\cos\theta(t)$ is the same as Case I with the exception of $f_1 = \frac{1}{2T}$.

Figure C.2. The data phase signal for the one-zero bit pattern.

Case III. "0011" bit pattern

Both the 001 and 100 bit patterns can be studied using the 0011 bit pattern (see Fig. C.3).

Figure C.3. The data phase signal for the "0011" bit pattern.

The Fourier series of $\sin\theta(t)$ and $\cos\theta(t)$ are:

$$\sin\theta(t) = \sum_{n \text{ odd} > 0}^{\infty} a_n \sin(2\pi n f_1 t) \quad (C.3)a$$

$$\cos\theta(t) = A_o + \sum_{q \text{ even} > 0}^{\infty} a_q \cos(2\pi q f_1 t) \quad (C.3)b$$

where

$$a_n = \frac{4h}{\pi} \frac{4\cos(\frac{h\pi}{T})\sin(\frac{n\pi}{T})\cos(\frac{n\pi}{T}) - 2\sin(\frac{n\pi}{T})}{n^2 - 4h^2}$$

$$a_q = -\frac{4h}{\pi} \frac{\sin(\frac{h\pi}{T})\cos(\frac{q\pi}{T})\cos(\frac{q\pi}{T})}{q^2 - 4h^2}$$

$$A_o = \frac{\sin(\frac{h\pi}{T})}{\frac{h\pi}{T}}$$

$$h = 2\pi f_d T \text{ and } f_1 = \frac{1}{4T}$$

The filtered phase signal may be well approximated by [12]

$$\phi(t) = \tan^{-1} \frac{\sum_{n=1}^{\infty} (|H(nf_1)| |a_n| \cos(2\pi n f_1 t + \angle H(nf_1)))}{\sum_{q=1}^{\infty} (|H(qf_1)| |a_q| \cos(2\pi q f_1 t + \angle H(qf_1))) + A_o |H(0)|} \quad (C.4)$$

for Case I and Case II ; and for Case III

$$\phi(t) = \tan^{-1} \frac{\sum_{n=1}^{\infty} (|H(nf_1)| |a_n| \sin(2\pi n f_1 t + \angle H(nf_1)))}{\sum_{q=1}^{\infty} (|H(qf_1)| |a_q| \cos(2\pi q f_1 t + \angle H(qf_1))) + A_o |H(0)|} \quad (C.5)$$

By choosing an appropriate number of dominating Fourier coefficients , the filtered phase signal $\phi(t)$ may then be calculated in discrete time for each of the four bit patterns (000,001,101,100). The remaining four bit patterns (111,110,010,011) can be treated as (000,001,101,100) case with inverted phase.

Filtered Signal Phase Model Verification Results

Simulation results for the filtered phase signal at the output of the discriminator for cases I,II and III where "0" is the n^{th} bit under consideration is shown in Fig. C.4 (the IF

filter used was a 2nd order Gaussian filter). Figure C.4 also shows the waveform dependence on the number of Fourier coefficients (where n is the number of Fourier coefficients). Figure C.5 shows the filtered phase signal waveform for an arbitrary Manchester coded data stream. It is therefore possible, for the purpose of time-domain simulations, to generate the filtered phase signal for Manchester coded data .

Figure C.5. $\frac{d}{dt}\phi(t)$ waveform for an arbitrary Manchester coded data stream .

Noise Statistics

Before describing the technique used to develop the noise generator simulation model, the background theory pertaining to noise found in narrow-band digital FM systems will be presented.

Theory

The limiter (shown in Fig. 2-1) strips off the envelope and the discriminator recovers the derivative of the output phase. The integrate-and-dump filter following the discriminator

a

b

Figure C.4 $\frac{d\phi(t)}{dt}$ waveform for bit pattern, (a) 000 , (b) 001

Figure C.4 cont'd; (c) 101, (d) 100

reintegrates this derivative producing a "phase difference" $\Delta\Phi(t)$ which can be written as [57], [58], [59]

$$\Delta\Phi(t) = \phi(t) - \phi(t-T) + [\eta(t) - \eta(t-T)] \cdot \text{mod}(2\pi) + 2\pi N(t-T, t) \quad (C.6)a$$

$$= \Delta\phi(t) + \psi(t) + 2\pi N(t-T, t) \quad (C.6)b$$

where

$$\Delta\phi = \phi(t) - \phi(t-T)$$

$$\psi(t) = [\eta(t) - \eta(t-T)] \cdot \text{mod}(2\pi)^1$$

$N(t-T, t)$ denotes the number of "clicks" [60], [61] in the time interval $(t-T, t)$.

A decision, at times which are multiples of bit time T , is made to decide whether a "1" or a "0" was sent (i.e. if $\Delta\Phi > 0$ a "1" was sent and $\Delta\Phi < 0$ a "0" was sent). The ability of the receiver to make correct decisions then depends solely upon the statistics of the noise processes $\psi(t)$ and $N(t-T, t)$ and are assumed to be statistically independent. It is known that

$\eta(t)$ dominates for high SNR and therefore $N(t-T, t)$ will not be considered.

Since $\eta(t)$ and $\eta(t-T)$ are statistically independent random variables the probability density function of $\psi(t)$ is the convolution of two density functions each of the form of (2.8) but with different values of $\rho(t)$. Fleck and Trabka [62] derived the density for $p(\rho)$ for the case when $\rho(t) = \rho(t-T) = U$ and the obtained result is

$$p(\rho) = \frac{e^{-U}}{4\pi} \int_0^\pi \sin(1 + U + U \sin \alpha \cos \psi) e^{U \sin \alpha \cos \psi} d\alpha \quad (C.7)$$

Allowing for different values of $\rho(t)$ and $\rho(t-T)$, the general form of this equation is [12]

$$p(\rho) = \frac{e^{-U}}{4\pi} \int_0^\pi (\sin(1 + U + V \cos \alpha + W \sin \alpha \cos \psi) e^{V \cos \alpha + W \sin \alpha \cos \psi} d\alpha \quad (C.8)$$

$$U = \frac{1}{2}(\rho(t) + \rho(t-T))$$

$$V = \frac{1}{2}(\rho(t) - \rho(t-T))$$

¹ "mod 2π " means that angles are restricted to a 2π interval which is later taken to be $(-\pi, \pi)$. For simplicity of notation the "mod 2π " is omitted.

Figure C.6: Cumulative Distribution Function $P(\psi > \psi_0)$.

$$W^2 = U^2 - V^2$$

and the generalized form for the distribution function $P(\psi > \psi_0)$ is given as

$$P(\psi > \psi_0) = \frac{W \sin \psi_0}{4\pi} \int_0^\pi \frac{e^{-(U-V \cos \alpha - W \cos \psi_0 \sin \alpha)}}{U - V \cos \alpha - W \cos \psi_0 \sin \alpha} d\alpha \quad ; \quad \psi_0 > 0 \quad (C.9)a$$

$$P(\psi > \psi_0) = \frac{1}{2} \quad ; \quad \psi_0 = 0 \quad (C.9)b$$

$$P(\psi > \psi_0) = 1 - \frac{W \sin \psi_0}{4\pi} \int_0^\pi \frac{e^{-(U-V \cos \alpha - W \cos \psi_0 \sin \alpha)}}{U - V \cos \alpha - W \cos \psi_0 \sin \alpha} d\alpha \quad ; \quad \psi_0 < 0 \quad (C.9)c$$

Noise Model Development

To generate variates, in this case the variate is $\psi(t) = \eta(t) - \eta(t - T)$, obeying a given probability density function (pdf), the "inverse transformation method" was used. This method utilizes the fact that the cumulative distribution function (cdf) corresponding to a pdf, can be inverted using random numbers in the range from 0 to 1 which conform with a uniform distribution $U(0,1)$.

Since the exact closed form solution of the inverted cdf is not known, the inverse cdf (for the case $V=0$; $\rho(t) = \rho(t - T)$) was obtained numerically. The method consisted of three steps:

- i) generation of a random number δ_{o1} (see Fig. C.6) in the unit interval (0,1).
- ii) subtraction of δ_{o1} from the original cdf, gives a new equation with a root at ψ_{o1} (see Fig. C.7).
- iii) numerical determination of the root.

Figure C.7: Cumulative Distribution Function $P(\psi > \psi_0) - \delta_{0,1}$

Figure C.8: Distribution function $P(\psi > \psi_0)$ for $\rho(t) = \rho(t - T) = 10dB$.

Noise Model Verification Results

The probability distribution obtained using the numerical inverse transformation method corresponds closely to the theoretical probability distribution obtained using equation (C.9) (see Fig. C.8). The amplitude distribution of noise generated by the presented model converges to the theoretical pdf (obtained using equation C.7) for large samples of noise (see

n-number of points generated by the noise generator

Figure C.9: Probability Density Function of $\psi = \eta(t) - \eta(t - T)$ for $\rho(t) = \rho(t - T) = 10dB$.

Fig. C.9).

Alternate Phase Noise Model Development

The equation used to develop the noise model is given as

$$\eta(t) = \tan^{-1} \frac{\xi(t)}{\sqrt{2SNR} + \vartheta(t)} \quad (C.10)$$

which is similar to equation (2.5) with the exception that the SNR is assumed constant. In equation C.6 $\xi(t)$ and $\vartheta(t)$ are independent Gaussian variables with zero means, unit variance, and bandlimited to the IF bandwidth [1], [2].

A Gaussian zero mean unity variance noise model has been developed and this model was used to generate the phase noise as follows. First of all generating noise at every minimum resolvable time (mrt - a parameter for the high level simulator SPLICE) gives a PSD bandlimited to $1/2\text{mrt}$, shown in Fig. C.10, as opposed to the theoretical bandwidth of infinity. Since we were using a sampling rate of 32 times the data rate, one mrt for our application is equal to $1/32$ of the bit period T . The variance σ^2 is given as

$$\sigma_1^2 = B_{\text{mrt}} N_{o1} \simeq 1.0 \quad (C.11)$$

where

B_{mrt} is the bandwidth of one mrt

B_{IF} is the IF bandwidth and N_{o2}

This noise is then passed through a lpf with a bandwidth equivalent to the IF bandwidth. The resulting PSD is shown in Fig. C.11. The variance in this case is given as

$$\sigma_2^2 = B_{IF} N_{o2} \neq 1.0 \quad (C.12)$$

But what is required is a variance of unity which is not the case for Fig. C.11, so a scaling factor is needed to accomplish this. The scaling factor is determined as follows;

$$B_1 N_{o1} = B_2 N_{o2} = \sigma^2 \simeq 1.0 \quad (C.13)a$$

$$B_1 N_{o1} = B_2 N_{o2} \quad (C.13)b$$

$$\frac{N_{o1}}{N_{o2}} = \frac{B_{IF}}{B_{\text{mrt}}} \quad (C.13)c$$

hence

$$N_{o2} = \frac{T}{2t_s} N_{o1} \quad (C.13)d$$

where $B_{LF} \equiv 1/T$ and $B_{mrt} \equiv 1/(2t_s) \cdot t_s$ is the sampling rate.

Therefore, multiplying the output of the low-pass filter by a constant $T/2t_s$ will then give the required noise characteristics.

Figure C.10. A Gaussian zero mean unity variance power-spectral density distribution.

2nd Order Low-Pass Filter Model Development

A general continuous-time second-order transfer function is

$$H(s) = \frac{k_2 s^2 + k_1 \frac{w_z}{Q_z} s + k_0 w_z^2}{s^2 + \frac{w_p}{Q_p} s + w_p^2} \quad (C.14)$$

where k_2, k_1, k_0 are constants that govern the type of filter required (i.e. low pass, high pass etc) , w_z, w_p are the zero and pole frequencies respectively and Q_z, Q_p are the zero and pole Q's respectively.

To obtain the z domain transfer function the bilinear transformation was used

$$s = \frac{2}{T} \frac{1 - z^{-1}}{1 + z^{-1}} \quad (C.15)$$

Figure C.11. A bandlimited Gaussian zero mean unity variance power-spectral density distribution

where T is the sampling period. This substitution into (3.10) results in

$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{a_2 z^{-2} + a_1 z^{-1} + a_0}{b_2 z^{-2} + b_1 z^{-1} + b_0} \quad (C.16)$$

where

$$a_2 = k_2 \frac{4}{T^2} - 2k_1 \frac{w_s}{Q_s} \frac{2}{T} + k_0 w_s^2$$

$$a_1 = -k_2 \frac{8}{T^2} + 2k_0 w_s^2$$

$$a_0 = k_2 \frac{4}{T^2} + k_1 \frac{2}{T} \frac{w_s}{Q_s} + k_0 w_s^2$$

$$b_2 = \frac{4}{T^2} - \frac{2}{T} \frac{w_p}{Q_p} + w_p^2$$

$$b_1 = -\frac{8}{T^2} + 2w_p^2$$

$$b_0 = \frac{4}{T^2} + \frac{2}{T} \frac{w_p}{Q_p} + w_p^2$$

The difference equation for the filter is

$$V_o = V_i(a_2 z^{-2} + a_1 z^{-1} + a_0) - V_o(b_2 z^{-2} + b_1 z^{-1}) \quad (C.17)$$

This difference equation was used to define the high level filter model for the SPLICE simulator.

To verify the operation of the filter model, the output of the low-pass filter was observed for an input signal containing high frequencies.

Appendix D

SC low-pass filter design and simulation results

The synthesis of a SC low-pass filter design is given in this appendix. These SC low-pass design equations were developed based upon A.S. Sedra [23] research and are authors personal contributions to this area of research. Results from the SPICE analysis of the frequency response and SC noise of the filters can also be found in this Appendix. The SPICE listings for the op-amp model used for the SC noise were included to clearly show the development of the models suitable for SPICE.

The MOS parameters for the SPICE simulator were supplied by Northern Telecom for the $3\mu\text{m}$ double layer metal process.

SC low-pass filter design example

A SC realizations of a low-pass filter using both the resistor equivalent and exact design method starting from a transfer function in the s-domain is illustrated here.

A general biquadratic transfer function of a continuous-time is of the form

$$H(s) = \pm \frac{a_2 s^2 + a_1 s + a_0}{s^2 + b_1 s + b_0}, \quad (D.1)$$

and using the bilinear transformation gives

$$H(z) = \pm \frac{m(a'_0 + a'_1 + a'_2)z^2 + m(a'_0 - a'_2)z + m(a'_0 - a'_1 + a'_2)}{z^2 + 2m(b'_0 - 1) + m(1 + b'_0 - b'_1)} \quad (D.2)$$

where

$$m = \frac{1}{1 + b_0 + b_1}, \quad (D.3)a$$

$$a'_2 = a_2, \quad (D.3)b$$

$$a'_1 = \left(\frac{T_c}{2}\right) a_1, \quad (D.3)c$$

$$a'_0 = \left(\frac{T_c}{2}\right)^2 a_0, \quad (D.3)d$$

$$b'_1 = \left(\frac{T_c}{2}\right) b_1, \quad (D.3)e$$

$$b'_0 = \left(\frac{T_c}{2}\right)^2 b_0, \quad (D.3)f$$

A block diagram which realizes equation (D.1) can be obtained by rewriting it in the form:

$$s^2 V_o(s) = -(a_2 s^2 + a_1 s + a_0) V_i - (b_1 s + b_0) V_i - (b_1 s + b_0) V_o, \quad (D.4)$$

dividing by s^2 and rearranging gives

$$V_o = -\frac{1}{s} \left((a_1 + a_2 s) V_i + b_1 V_o - \sqrt{b_0} V_1 \right), \quad (D.5)$$

where V_1 is defined as follows:

$$V_1 = -\frac{1}{s} \left(\frac{a_0}{\sqrt{b_0}} V_i + \sqrt{b_0} V_o \right). \quad (D.6)$$

Thus, V_1 is obtained by integrating the weighted sum of V_{in} and V_{out} by integrating the weighted sum of V_{in} , V_{out} , and V_1 . A system which can perform these operations and thus produce V_{out} from V_{in} , is shown in Fig. D.1a. Note that a different system would have resulted if equation (D.4) was partitioned differently.

An active-RC realization, for the system in Fig. D.1a, is shown in Fig. D.1b. It should be noted that the resulting circuit is not useful as an active-RC filter, since it contains the negative resistor $-1/\sqrt{b_0}$ which would require additional active elements for its realization. It serves, however as a useful purpose as a model for the final SC circuit. Thus, replace each resistor with capacitors and periodically-operated switches with the correct clock phase. The resulting SC biquad is shown in Fig. D.1c.

The exact sampled-data transfer function $H(z)$ of the SC circuit of Fig. D.b is

$$H(z) = \frac{(\alpha_2 + \alpha_3)z^2 + (\alpha_1\alpha_5 - \alpha_2 - 2\alpha_3)z + \alpha_3}{(1 + \alpha_6)z^2 + (\alpha_4\alpha_5 - \alpha_6 - 2)z + 1} \quad (D.7)$$

Thus the design equation can be obtained by equating the coefficients of the like powers of z in the numerator and denominator of equation (D.2) and (D.7). The results for the pole design equations is;

$$\alpha_6 = \frac{1 - m(a + b'_0 - b'_1)}{m(1 + b'_0 - b'_1)} \quad (D.8)a$$

(a)

(b)

(c)

Figure D.1 Switched-capacitor low-Q biquad: (a) block diagram, (b) active-RC realization, (c) circuit.

$$\alpha_4 \alpha_5 = 2m + (2m(b'_0 - 1) + 1) \frac{1 - m(a + b'_0 - b'_1)}{m(1 + b'_0 - b'_1)} \quad (D.8)b$$

These are two equations with 3 unknowns $\alpha_2, \alpha_3, \alpha_4$. The one degree of freedom may be used to maximize the dynamic range of the biquad. This can be accomplished by choosing equal time constants for the two integrators.

$$\alpha_4 = \alpha_5$$

The zeros design equations for some special cases are:

1) Low Pass ($a_1 = a_2 = 0$)

$$\alpha_2 = 0 \quad \alpha_1 \alpha_5 = \frac{4a'_0}{1+b'_0-b'_1} \quad \alpha_3 = \frac{a'_0}{1+b'_0-b'_1}$$

2) High Pass ($a_0 = a_1 = 0$)

$$\alpha_2 = 0 \quad \alpha_1 = 0 \quad \alpha_3 = \frac{a'_2}{1+b'_0-b'_1}$$

Both the Resistor Equivalent method and the exact transfer function method will be used to design a SC low-pass filter. The performance of the resulting filters which realize the transfer function will also be compared. The specifications are as follows:

i) 2nd order Butterworth

$$\text{ii) } Q = \frac{1}{\sqrt{2}}$$

$$\text{iii) } f_p = 19.2 \text{ kHz}$$

$$\text{iv) } f_c = \frac{1}{T_c} = 512 \text{ kHz}$$

$$\text{v) d.c. gain} = 1.0$$

Resistor Equivalent Method

The active-RC realization for the low-pass case can be obtained by excluding R_2 and C_3 in the general case biquad circuit of Fig. D.1b. and the equivalent SC biquad low-pass circuit is obtained by replacing each resistor with a switched capacitor and setting $\alpha_2 = 0$ and $\alpha_3 = 0$.

The transfer function for the active-RC low-pass circuit defined in terms of R's and C's is given as

$$H(s) = \frac{-\left(\frac{R_1}{R_1}\right)\left(\frac{1}{R_3 R_4 C_A C_B}\right)}{s^2 + \left(\frac{1}{R_3 C_C B}\right)s + \left(\frac{1}{R_3 R_4 C_A C_B}\right)} \quad (D.9)$$

and in terms of the continuous time pole w_{ctp} , the quality factor Q and dc gain G_{dc} is

$$H(s) = \frac{-G_{dc}w_{ctp}^2}{s^2 + \left(\frac{w_{ctp}}{Q}\right)s + w_{ctp}^2}, \quad (D.10)$$

Just as a reminder the pole frequency given in the specifications is that of the sampled-data domain and to get the continuous-time pole which will be used in equation (D.10) the prewarping equation

$$w_{ctp} = \frac{2}{T_c} \sin(w_{sdp}T_c/2), \quad (D.11)$$

where

w_{ctp} - is the continuous-time pole,

w_{sdp} - is the sampled-data domain pole.

The exact transfer function of the SC low-pass biquad in terms of the continuous-time characteristics can be shown to be

$$H(z) = \frac{-G_{dc}\left(\frac{w_{ctp}}{f_s}\right)^2}{z^{-2} + \left(-2 - \frac{1}{Q}\frac{w_{ctp}}{f_s} + \left(\frac{w_{ctp}}{f_s}\right)^2\right)z^{-1} + \left(1 + \frac{1}{Q}\frac{w_{ctp}}{f_s}\right)} \quad (D.12)$$

A comparison of the continuous-time filter and the SC filter performance can now be made. The gain of the continuous-time filter at dc can be calculated by substituting $s=0$ in the transfer function which yields a dc gain of unity. For the SC filter the dc gain can be obtained as follows ;

$$w_{sd} = \frac{2}{T_c} \sin(w_{ct}T_c/2) = 0 \text{ for } w_{ct} = 0 ,$$

therefore $z = e^{jw_{sd}T_c} = e^0 = 1.0$ which is the value substituted into the exact transfer function equation (D.12) to yield a dc gain of unity.

As another check for performance the frequency response of the filters will also be compared at the pole frequency. The frequency response of the continuous time domain at the continuous pole frequency of 19.15 kHz (prewarped value) was calculated to be $0.7071\angle -90^\circ$. This is the expected value.

The frequency response for the SC filter is calculated by substituting $z = 1.0\angle 13.5^\circ$ into the exact transfer function equation (D.12) to yield a gain of $0.7071\angle -96.75^\circ$. As mentioned in chapter 3, the exact transfer function introduces an extra phase delay of $e^{jw_{sd}T_c}$ which for

an $w_{sd} = 2\pi 19.2k$ results in a phase delay of -6.75° . This accounts for the phase difference between the continuous-time and sampled-data filters.

This example showed that the phase response of a SC filtered realized by substituting the resistors of the active-RC filter with the equivalent switched-capacitor filter deviates from that of the active-RC filter. The magnitude responses at the prewarped frequencies of the filters do however agree.

Exact Method Design

The coefficients in equation (D.3) for the low-pass case are ;

$$b'_1 = \left(\frac{T}{2}\right) b_1 = \left(\frac{T}{2}\right) \left(\frac{w_{ctp}}{Q}\right) = \pi \left(\frac{f_{ctp}}{f_s}\right) \left(\frac{1}{Q}\right) = 0.167389085,$$

$$b'_0 = \left(\frac{T}{2} w_{ctp}\right)^2 = \left(\pi \frac{f_p}{f_s}\right)^2 = 0.014009553,$$

$$a'_2 = a'_1 = 0,$$

$$a'_0 = \left(\frac{T}{2}\right)^2 a_0 = \left(\frac{T}{2} w_{ctp}\right)^2 = 0.014009553,$$

$$m = \frac{1}{1 + b'_0 + b'_1} = 0.846454336,$$

$$1 + b'_0 - b'_1 = 0.846620468,$$

The pole design equations become;

$$\alpha_6 = \frac{1 - m(1 + b'_0 - b'_1)}{m(1 + b'_0 - b'_1)} = 0.395428864,$$

$$\alpha_4 \alpha_5 = 2 + 2m(b'_0 - 1) + (2m(b'_0 - 1) + 1)\alpha_6 = 0.066190478,$$

to maximize the dynamic range $\alpha_4 = \alpha_5 = 0.257275101$.

The zero design equations become:

$$\alpha_1 \alpha_3 = \frac{4a'_0}{1 + b'_0 - b'_1},$$

$$\alpha_1 = \frac{4a'_0}{1 + b'_0 - b'_1} \left(\frac{1}{\alpha_3}\right) = 0.257275095,$$

$$\alpha_3 = \frac{a'_0}{1 + b'_0 - b'_1} = 0.016547619,$$

$$\alpha_2 = 0.0$$

and the exact transfer function for low-pass case is;

$$H(z) = \frac{\alpha_3 z^2 + (\alpha_1 \alpha_5 - 2\alpha_3)z + \alpha_3}{(1 + \alpha_6) \left[z^2 + \frac{(\alpha_4 \alpha_5 - \alpha_6 - 2)}{(1 + \alpha_6)} z + \frac{1}{(1 + \alpha_6)} \right]}$$

$$H(z) = \frac{0.011858446[z^2 + 2z + 1]}{z^2 - 1.669191777z + 0.746625566}$$

Checking the gain at dc means substituting $z=1.0$ into the above equation which results in

$$H(1) = 1.0$$

and checking the response at the pole frequency of 19.2 kHz results in substituting $z = 1.0 \angle 13.5^\circ$ into the exact transfer function to yield

$$H(z = 1.0 \angle 13.5^\circ) = \frac{0.046778484}{0.066152442} \angle 90^\circ = 0.7071 \angle 90^\circ$$

which is the expected gain and angle at the pole frequency of the switched-capacitor filter.

This example showed that by using the resistor equivalent method an extra phase delay equal to one period of the sampling time is introduced. The exact transfer function method on the other hand compensates for this extra phase delay by introducing a feedforward capacitor $\alpha_3 C_2$ shown in Fig. D.1c. Comparing the two circuits for the different methods shows that synthesising filters using the exact transfer method, as opposed to the resistor equivalent method, requires an extra component primarily a feedforward capacitor. Hence, as is the case with most things in life, tradeoff between the two methods.

SPICE Analysis of filters

The frequency response deviations from the desired response were considered tolerable. The pole frequency of the LPF, obtained from SPICE analysis, is 20.4 KHz as opposed to the desired value of 19.6 KHz and a Q value of 0.718 as opposed to the desired value of 0.7071. The pole frequency of the HPF, obtained from SPICE analysis, was 8.1 as opposed to the desired value of 6.6 kHz and a Q value of 1.0 as opposed to the desired value of 0.7071. This slight discrepancy is attributed to the fact that the capacitor used in the designs were not the exact calculated values.

a

b

Figure D.2. Frequency response of filters implemented on test-chip, (a) biquad SC low-pass, (b) biquad SC high-pass.

a

b

Figure D.3. Frequency response of filter implemented on test-chip, (a) 4th order SC band-pass, (b) zoom in view of passband .

a

b

Figure D.4. SC noise response of test-chip filters; (a) biquad SC low-pass, (b) biquad SC high-pass

Figure D.4 cont'd: (c) 4th order SC band-pass

Figure D.5. Time-domain response of the Integrate-and-dump filter.

SPICE op-amp noise model

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```

*
*
* The models developed for the SPICE simulator
* for analysing noise found in switched-capacitor
* networks is reported here.
*
*
*
***** subcircuit definitions*****
*****
*
* This model simulates the op-amp as an ideal op-amp
* with one dominate pole which has been measured to be
* approximately 50k Hz for the actual op-amp.

* The values of the capacitor and resistor used in the
* model were chosen as such to give an RC time constant
* equivlent to 50k Hz ( i.e.  $RC = 1/2 \cdot \pi \cdot f$  where  $f=50\text{kHz}$ )
* and also a low output impedance.

.subckt opamp 1 2 3
* node 1 plus terminal
* node 2 neg've terminl
* node 3 output of opamp
*
rout 4 3 50
cl 3 0 91e-09
el 4 0 1 2 708
.ends opamp
*
*
*****
*
* To generate flicker noise (1/f) , a device model
* is used to simulate the unsampled 1/f noise
* component of the op-amp. The KF parameter was adjusted
* to match the measured op-amp input-referred 1/f noise.

.subckt flicker 2 1
* node 2 is the top of the dc blocking capcitor
* node 1 should be at gnd
id 3 0 dc -20e-03
*
mn1 3 3 0 0 ndev l=10e-06 w=200e-06
*
.MODEL PENH PMOS(LEVEL=2 VTO=-0.8 KP=11.46E-6
+ UO=250 GAMMA=0.6 PHI=.6 PB=0.6
+ CGSO=2.5E-10 CGDO=2.5E-10 CGBO=5.0E-10
+ RSH=80 CJ=1.54E-4 MJ=.6 CJSW=4.E-10
+ MJSW=.6 JS=1.0E-5 TOX=5.0E-8 NSUB=5.0E15
+ TPG=1 XJ=5.0E-7 LD=2.5E-7
+ VMAX=7.E4 KF=10E-24)
*+ UEXP=0.139 UCRIT=6.44E4 XQC=.4
.MODEL ndev NMOS(LEVEL=2 VTO=0.7 KP=38.77e-6
+ UO=775 GAMMA=1.1 PHI=.6 PB=0.7 TPG=1.0
+ CGSO=3.E-10 CGDO=3.E-10 CGBO=5.0E-10
+ RSH=25 CJ=4.4E-4 MJ=.5 CJSW=4.0E-10
+ MJSW=.3 JS=1.E-5 TOX=5.0E-8 NSUB=1.7E16
+ XJ=6.0E-7 LD=3.5E-7 VMAX=1.0E5 KF=120E-24)
*+ UCRIT=1.23E5 UEXP=0.022 XQC=.4)
*
el 4 1 3 0 1
cl 2 4 100
.ends flicker
*

```

```

*
*****
*
* The flat-band or thermal noise of the op-amp
* can be modeled as white noise sources which
* are easily simulated by resistors in SPICE.
*
*
.subckt thermal 1 2
il 0 3 dc 1e-06
r1 3 0 12e03
r2 3 0 12e03
el 1 2 3 0 1
.ends thermal
*
*
*****
*
* The folded flat-band noise is also simulated as
* white noise sources using resistors.
*
*
.subckt fldth 1 2
il 0 3 1e-06
r1 3 0 12e03
r2 3 0 12e03
el 1 2 3 0 20
.ends fldth
*
*
*****
*
* Using the models described above the
* complete SPICE op-amp noise model can
* be built (see Fig. 4.10)
*
*
.subckt opnmdl 1 2 3
* node 1 - terminal of opamp
* node 2 continuous output
* node 3 sampled output
x1 5 1 2 opamp
x2 5 4 thermal
x3 4 0 flicker
x4 2 3 fldth
r1 5 0 1e-03
.ends opnmdl
*
.end

```

Appendix E

Bonding Diagram for the Mixed Analog/Digital BDD

CNC MULTIPROJECT BONDING DIAGRAM

RETICLE CODE U292

BRAND ID LABEL IC3

OTHER IDENTIFICATION FEATURES

WAFER NUMBERS

DESIGN FILE REFERENCE

PACKAGE	11K40P1-192G	LID	C-491-175-15M
WIRE ALLOY	99% Al/1% Si	DIA.	.001"
	99% Al/1% Si		.00125"
ELONG.	1.5 - 4%	T.S.	14-16 gms
	1.5 - 4%		10-22 gms
D/A PREFORM	ALLOY 98% Au/2% Si	RECOMMENDED SIZE	W/B METHOD U.S.

BONDING DIAGRAM

NOTES: 1. DIE ATTACH PAD SIZE: .400 X .400
2. ZERO GROUND

PIN	TYPE	IO IN OUTPUT
1	ANALOG	LIMITER IN VDD1
2	ANALOG	LIMITER IN VDD2
3	ANALOG	DIFFERENTIAL
4	CMOS IN	DIFFERENTIAL
5	CMOS IN	DIFFERENTIAL
6	CMOS IN	DIFFERENTIAL
7	CMOS IN	DIFFERENTIAL
8	CMOS IN	DIFFERENTIAL
9	CMOS IN	DIFFERENTIAL
10	CMOS IN	DIFFERENTIAL
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35	CMOS IN	DIFFERENTIAL
36	CMOS IN	DIFFERENTIAL
37	CMOS IN	DIFFERENTIAL
38	CMOS IN	DIFFERENTIAL
39	CMOS IN	DIFFERENTIAL
40	CMOS IN	DIFFERENTIAL

CIFZAP V1.2

'cu040.u292'

Fri Sep 9 18:03:18 1988

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