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**SILICON CARBIDE EMITTER DIODE FORMED
BY LPCVD
FROM DI-TERTIARY-BUTYLSILANE**

by

Susan B. Hewitt

A thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfillment of the
requirements for the degree of

Master of Engineering

**Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Faculty of Engineering
Carleton University**

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ABSTRACT

This thesis reports on the first use of silicon carbide films produced by low pressure chemical vapour deposition (LPCVD) from di-tertiary-butylsilane (DTBS) to form emitters in silicon/silicon carbide heterojunction devices. The thesis covers the development of a process for LPCVD of undoped silicon carbide films, and discusses evaluation of these films using a variety of material characterization techniques. *In-situ* doping of the films with tert-butylphosphine (TBP) is then considered, followed by application of the films in silicon carbide emitter diodes and lateral bipolar transistors.

Stoichiometric silicon carbide films were deposited at a temperature of 750°C, a pressure of 0.50 Torr and a DTBS flow rate of 250 sccm in a conventional hot-wall furnace. The chemical composition was confirmed via Auger electron spectroscopy and Elastic Recoil Detection while Raman spectroscopy and Fourier transform infrared spectroscopy were used to demonstrate the presence of silicon-carbon bonds. Film crystallinity was determined by transmission electron microscopy and electron diffraction. The films were amorphous as deposited, but became microcrystalline following rapid thermal annealing.

In-situ doping was accomplished using TBP at a flow rate of 340 sccm. The dopant was activated by rapid thermal annealing, with best results obtained using a 1100°C, 10 second cycle. The lowest resistivity recorded was 0.02 Ω -cm.

Heterojunction diodes were formed on lightly-doped p-type substrates using the *in-situ* doped silicon carbide films as emitters. The forward characteristics of the diodes were virtually ideal for six decades of current. The diode saturation current agreed well with the value expected for an injection-diffusion current in these lightly doped substrates, suggesting that the forward current was dominated by electron injection into the substrate. This result was confirmed by measurements on lateral transistors, which gave gains comparable to those obtained with high-quality polysilicon emitters. In the reverse

direction, the diodes had a hard breakdown at about 55 V and a leakage current of less than 10 nA/cm^2 at 5 V reverse bias. These results suggest that further investigation of DTBS silicon carbide emitters in a vertical bipolar transistor process is warranted, particularly in view of the low thermal budget associated with the DTBS technique compared to alternative methods of silicon carbide emitter formation.

The undersigned recommend to the Faculty of Graduate Studies and Research the acceptance of the thesis:

"Silicon Carbide Emitter Diodes
formed by LPCVD
from Di-tertiary-butylsilane"

submitted by Susan B. Hewitt in partial fulfillment of the requirements for the degree of
Master of Engineering

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TABLE OF CONTENTS

ABSTRACT	ii
ACKNOWLEDGEMENTS	v
TABLE OF CONTENTS	vi
LIST OF FIGURES	viii
LIST OF TABLES	ix
LIST OF EQUATIONS	x
CHAPTER 1	
INTRODUCTION	1
CHAPTER 2	
BACKGROUND:	
A REVIEW OF PREVIOUS RESEARCH	
ON SILICON CARBIDE EMITTER HBT's	3
2.1 Homojunction Bipolar Transistors	3
2.2 Wide Bandgap Emitter Heterojunction	
Bipolar Transistors	5
2.3 Previous Work	7
CHAPTER 3	
UNDOPED SILICON CARBIDE FILMS:	
DEPOSITION EXPERIMENTS AND MATERIAL	
CHARACTERIZATION	11
3.1 Properties of DTBS	11
3.2 Experiments	12
3.3 Results	15
3.3.1 Elimination of oxygen in the films	15
3.3.2 Stoichiometry of the films	16
3.3.3 Chemical Bonds	17
3.3.4 Crystal Structure	19
3.3.5 Film Uniformity and Thickness	19
3.3.6 Deposition Rate	20
3.3.7 Film Quality and Stress	20
3.4 Summary	21

CHAPTER 4	
DOPED SILICON CARBIDE FILMS:	
EXPERIMENTS AND MATERIAL CHARACTERIZATION	22
4.1 Experiments	22
4.2 Results	24
4.2.1 Material Analysis	24
4.2.2 Bandgap Determination by Optical Absorption	24
4.2.3 Film Crystallinity	25
4.2.4 Resistivity of the Material	28
4.3 Conclusions	31
 CHAPTER 5	
SILICON CARBIDE EMITTER DIODE:	
FABRICATION AND DEVICE	
CHARACTERIZATION	33
5.1 Diode Fabrication	33
5.2 Device Mask Layout	35
5.3 Electrical Characterization	36
5.4 Conclusions	40
 CHAPTER 6	
SUMMARY AND CONCLUSIONS	41
6.1 Summary	41
6.2 Future Work	43
6.3 Conclusions	43
 REFERENCES	44

LIST OF FIGURES

FIGURE NO.		PAGE
2-1	Band Diagram for Wide Bandgap Emitter Heterojunction Transistor	6
3-1	DTBS Structure	11
3-2	Location of Wafers in Furnace Tube	13
3-3	Stoichiometry vs. Temperature	17
3-4	Sample of Typical FTIR Spectrum	18
3-5	Sample of Typical Raman Spectrum	18
3-6	DTBS Flow Rate vs. Deposition Rate	20
4-1	TEM & X-ray Diffraction Patterns for Samples F1100 & F1200	26
4-2	Annealing Experiment on Doped Samples of Run 1-224	30
4-3	Resistance Ratio vs. Temperature	31
5-1	Silicon Carbide Emitter Diode Cross-section	33
5-2	Device Mask Layout	35
5-3	Lateral Bipolar Device	36
5-4	Gummel Plot of Silicon Carbide Emitter Diode	37
5-5	Gummel Plot of Lateral Bipolar Transistor	38
5-6	Reverse Breakdown of Silicon Carbide Emitter Diode	38
5-7	Emitter Resistance of Silicon Carbide Emitter Diode	39

LIST OF TABLES

TABLE NO.		PAGE
3-1	Deposition Conditions of Undoped Runs	14
4-1	Deposition Conditions of Doped Runs	23
4-2	D-spacings for samples F1000	28
4-3	D-spacings for samples F1100	28
4-4	Doped Silicon Carbide Results	29

LIST OF EQUATIONS

EQUATION NO.		PAGE
(1)	Cutoff Frequency, f_T	3
(2)	Emitter-Collector Transit Time, τ_{EC}	3
(3)	Maximum Power Gain, f_{max}	4
(4)	Base Transit Time, τ_B	4
(5)	D-spacing	27
(6)	Ring Radii	27
(7)	Relativistic Momentum	27
(8)	Diode Law	36

CHAPTER 1

INTRODUCTION

Silicon carbide (SiC) has been proposed as an emitter material for silicon-based heterojunction bipolar transistors (HBTs) because its wide bandgap can reduce hole back injection in a npn device. As a result, the base can be doped more heavily than in a homojunction device while maintaining reasonable current gain. This allows the use of a very narrow base without risking punchthrough or incurring an excessively high base sheet resistance, which in turn increases the operating frequency of the device [1].

Previously reported research on SiC emitter HBTs is summarized in Chapter 2 of this thesis. Typically, the SiC film has been formed by chemical vapour deposition from mixtures of silane or disilane and acetylene or propane. Unfortunately, these sources require deposition temperatures greater than 1200°C to form crystalline silicon carbide and greater than 900°C to form polycrystalline silicon carbide. These temperatures are not compatible with the preservation of ultra-shallow base profiles needed in high speed devices. As a result, amorphous silicon carbide films that can be deposited at temperatures of 750°C or less have been examined. Unfortunately, the majority of this work has resulted in devices with unacceptably high emitter resistances.

This thesis examines an alternative method for forming polycrystalline silicon carbide emitters. A single precursor, ditertiarybutylsilane (DTBS), is used as both the silicon and carbon source. Chapter 3 discusses initial experiments aimed at establishing a process for depositing undoped stoichiometric silicon carbide films from DTBS. Extensive material characterization on the films is also presented. Once a procedure for forming stoichiometric SiC films was in place, attention turned to *in-situ* phosphorus doping of the films and to the use of rapid thermal annealing for dopant activation. Results are discussed in Chapter 4. Chapter 5 examines the use of the *in-situ* doped films to form silicon carbide emitter diodes and lateral bipolar transistors, and presents

electrical characterization results for these devices. Conclusions and suggestions for future work follow in Chapter 6.

This work was completed at Northern Telecom Ltd. and Carleton University. Northern Telecom Electronics provided the DTBS deposition and materials analysis. All other processing and electrical characterizations were performed at Carleton University.

CHAPTER 2

BACKGROUND:

A REVIEW OF PREVIOUS RESEARCH ON SILICON CARBIDE

EMITTER HBTs

This chapter begins with a review of device physics and performance considerations for conventional homojunction transistors and heterojunction bipolar transistors with wide bandgap emitters. The advantages of widegap emitters in speed and gain are discussed. Previous attempts to form such devices on silicon substrates using silicon carbide emitters are then examined.

2.1 Homojunction Bipolar Transistors

One of the most important performance aspects of bipolar devices is speed. The most widely used measure of a transistor's speed is its cutoff frequency, f_T . f_T is the frequency at which the common-emitter gain is unity and is given by the following equation

$$\frac{1}{2\pi f_T} = \tau_{EC} = \tau_E + \tau_B + \tau_{CSCL} + \tau_C \quad (1)$$

where τ_{EC} is transit time of the emitter-to-collector and is equal to the following:

$$\tau_{EC} = \frac{dQ_E}{dI_C} \quad (2)$$

where τ_E , τ_B , and τ_C are the transit times for the emitter, base and collector regions, respectively and τ_{CSCL} is the effective electron transit time across the base-collector depletion region [2].

Another and perhaps more useful measure of the speed is $f_{\max}$. $f_{\max}$ is the frequency at which the maximum power gain is unity. It is defined as follows:

$$f_{\max} = \left[\frac{f_T}{8\pi R_B C_{BC}} \right]^{\frac{1}{2}} \quad (3)$$

where R_B is the parasitic base resistance and C_{BC} is the base-collector capacitance [3].

In designing a modern bipolar transistor, it is important to maximize f_T and $f_{\max}$. In a typical modern silicon npn homojunction bipolar transistor, the peak value of f_T is often dominated by the base transit time.

$$\tau_b = \frac{W}{nD_n} \quad (4)$$

where W is the base width, n is a factor dependent on the grading of the base doping profile and D_n is the electron diffusion coefficient [3]. Thus the width of the base is reduced in order to reduce the base transit time and hence increase f_T .

The reduction of the base width is not without cost. First, the narrower base will cause an increase in the base sheet resistance, which in turn causes a decrease in the gain as well as a reduction in the Early voltage [4]. Also when the device is operating at high current density, a high pinched base sheet resistance can result in debiasing of the central region of the emitter [5].

In addition, a narrow base can result in punchthrough occurring between the emitter and the collector regions [6]. The collector-base voltages cause a collector depletion region that may, in narrow base devices, extend completely across the base into the emitter region of the transistor. This depletion region will reduce the energy barrier between the emitter and the base resulting in uncontrollable current injection.

The solution to most of the problems of the narrow base is to increase the doping of the base [6]. Unfortunately, this doping increase can cause difficulties in maintaining a narrow base width -- particularly, if the base is formed by ion implantation. A more pressing problem with the heavy base doping, is that it cannot exceed $5 \times 10^{18} \text{ cm}^{-3}$ at the edge of the base-emitter depletion region [6]. Tunneling across the junction will occur at higher base doping levels. Thus, this limits the base-width to approximately 50 nm for devices that can withstand a 3 V reverse bias voltage on the base-collector junction [6]. This, in turn, limits the f_T to about 50 GHz [6].

To create a base width that is narrower than 50 nm, the emitter doping must be reduced. This will cause an increase in the hole back injection current which will lower the transistor gain [5]. The reduced emitter doping also increases the emitter charge storage time, τ_e , which can reduce f_T since the emitter storage time becomes the dominant term in f_T now that the base transit time has been significantly reduced [5].

2.2 Wide Bandgap Emitter Heterojunction Bipolar Transistors

Heterojunction devices attempt to overcome some of the gain and speed limits imposed on bipolar devices, by performing bandgap engineering on various sections of the transistor. There are generally two methods used -- narrow bandgap bases and wide bandgap emitters. (Wide bandgap collectors may also offer speed advantages for saturating logic.) Since this thesis examines the effect of wide bandgap silicon carbide emitters, the second of these possibilities is discussed further.

Figure 2.1 shows the band diagram of an npn heterojunction transistor with a wide bandgap emitter under normal bias conditions (forward biased emitter, reverse biased collector.) The silicon carbide emitter improves the emitter injection efficiency by increasing the difference between the emitter and base bandgap, $\Delta E_g = E_{g,e} - E_{g,b}$ [7]. The

silicon carbide creates a greater barrier to holes compared to a silicon or polysilicon emitter. As a result, it is possible to produce devices with adequate current gains when they have high base doping and low emitter doping as compared to the homojunction case.

Band Diagram for a Wide Bandgap Emitter Heterojunction Transistor
Figure 2-1

Since there is very little data on the electron affinity of silicon carbide, it is not clear whether or not a "spike" will occur in the conduction band [8]. Internal photo emission data taken by S.G. Meike et al. suggests that there may be a slight offset [8]; however, the current-voltage characteristics recorded by other researches for silicon carbide emitter diodes and transistor indicate that if this spike is present it has little or no effect on the current flow even at relatively high densities [9-16].

The heavier doped ultra-narrow base reduces the base resistance and permits the $f_{\max}$ of the transistor to be greatly increased [4]. The heavy doping also reduces the effect of base punchthrough thus allowing narrow base regions to be produced. The lower

emitter doping allows the emitter-base space-charge region to increase on the emitter side, reducing the emitter junction capacitance, and so increasing $f_{\max}$.

2.3 Previous Work

Early work on silicon carbide emitter HBTs concentrated on the use of crystalline SiC films [13,14]. Unfortunately, these films can not be integrated into a standard micron or sub-micron bipolar process because of the excessive temperature ($>1000^{\circ}\text{C}$) required to deposit crystalline SiC. These temperatures would result in the out-diffusion of the narrow, heavily-doped base and thus would negate any advantage that the wide-bandgap emitter might provide. As a result, more recent work has examined micro-crystalline, poly-crystalline and amorphous silicon carbide emitters [11,12,15,17].

Ruddell *et al.* deposited stoichiometric doped silicon carbide films using a limited reaction processing reactor (LRP) [17]. This group deposited micro-crystalline silicon carbide films at a temperature of 970°C and a pressure of 10 mBar using silane and propane flow rates of 5 sccm and 100 sccm respectively. The crystallite size in their films was 50 nm. These films were *in-situ* doped with 0.1% phosphine gas diluted in nitrogen. The most heavily doped films contained $8 \times 10^{20} \text{ cm}^{-3}$ of phosphorus. The films deposited were used to produce heterojunction bipolar transistors. The LRP reactor performed an *in-situ* plasma pre-clean to remove the native oxides from the wafer surfaces. The wafers then received a 1 minute deposition of silicon carbide to produce a 200 nm film. The film was patterned and etched in CF_4/O_2 plasma and contacted with aluminum. The best HBTs that were produced resulted in an emitter Gummel number that was a factor of two better than the polysilicon reference transistor. These devices had a gain of 14 and a collector current ideality factor of 1.05. The base ideality factor was 1.3. Unfortunately the emitter resistance was relatively high ($0.019 \Omega\text{-cm}$).

Sasaki *et al.* reported a pnp heterojunction transistor formed with a boron doped amorphous silicon carbide (a-SiC) emitter and crystalline (c-Si) silicon base and collector [16]. The emitter film was deposited using plasma-assisted chemical vapour deposition at a temperature of 450°C. At the start of the process, a 0.5 µm layer of field oxide was grown thermally at a temperature of 1000°C for 100 minutes in wet oxygen on a 3-5 Ω-cm (111) p-type pre-cleaned wafer. A window was etched into the silicon dioxide to form the intrinsic base and the wafers were implanted with $^{31}\text{P}^+$ ions at an energy of 160 keV and a dose of $2 \times 10^{12} \text{ cm}^{-2}$. A heavier phosphorus implant was used to form the extrinsic base contact region. Another layer of oxide was grown at 1025°C for 30 minutes in wet oxygen producing a 0.2 µm film. An emitter window was then etched and 60 nm of doped a-SiC was deposited from a mixture of silane, methane and diborane. Aluminum was used as a contact. A CF_4 plasma was used to pattern silicon carbide layers using the aluminum as a mask. The optical bandgap of the films was 1.8 eV. The devices had a current gain of 50 at an emitter current density of 2.4 A/cm^2 . The gain of the devices was less than expected. It was probably limited by recombination at the silicon/silicon carbide interface.

Sugii *et al.* from Fujitsu Laboratories have published extensively on polycrystalline silicon-carbide transistors [10-12,15]. This group grows silicon carbide films in a cold wall reactor. The wafers are placed on an RF induction heated SiC-coated graphite susceptor. The sources for the silicon and carbon are silane and acetylene respectively. Purified hydrogen is used as a carrier gas. The films are *in-situ* doped with phosphine and grown to a thickness of 40 nm. In all cases, the silicon carbide films were grown on (100) oriented silicon wafers that had an epitaxial base of 50 nm grown at 600°C with a carrier concentration of $1 \times 10^{19} \text{ cm}^{-3}$. The wafers were then cleaned and had a hydrofluoric acid dip to remove the native oxide. The silicon carbide films were then deposited. The wafers received another layer of n-type 200 nm doped polysilicon that was used to make contact to the silicon carbide films. In their first paper [10], Sugii *et al.*

reported a heterojunction transistor with a current gain of 15 and an emitter resistivity of 4.3 m Ω -cm. The pinched base sub-emitter sheet resistance was 1 kohm/sq and the junction breakdown voltages were 10 V. According to their research, the bandgap of these films is the same as beta silicon carbide, 2.2 to 2.3 eV. The transistor also avoided base punchthrough since the carrier concentration of the base was high. In addition, the transistor exhibited low forward bias tunneling current.

In later work, di-fluorosilane was incorporated into the silicon carbide deposition step [12]. This enabled fluorine to be used to terminate the dangling bonds at the silicon/silicon carbide interface. The fluorine increased the current gain of the device to 80 and the sheet resistance of the sub-emitter to 1.75 k Ω /sq. The Early voltage of the device was over 100 V while the junction breakdown voltage was 8 V. The collector current density was 6 x 10⁴ A/cm². A reference homojunction transistor with a polysilicon emitter had a current gain of 20.

Their most recent paper examined the operational speed of the fluorine-terminated silicon carbide device [11]. It had a cutoff frequency of 30 GHz when the base concentration was 6 x 10¹⁸ cm⁻³ and its width was 35 nm. At a base concentration of 1 x 10¹⁹ cm⁻³ and a base width of 50 nm, the cutoff frequency was reduced to 25 GHz. The speed of this device was much greater than that of a conventional ion-implanted base, polysilicon emitter transistor fabricated with all other design rules and processes remaining the same. The conventional device could not achieve the same heavily doped, narrow base that the silicon carbide emitter permitted.

The work discussed in the previous chapter is not a complete overview of silicon carbide heterojunction devices. There are hundreds of papers on solar cells and high-power devices that examine crystalline silicon carbide transistor structures. However, since the silicon carbide layers for these type of devices are formed at high temperatures, 1000°C or more, these solutions are not applicable to small geometry, narrow base structures formed in typical bipolar processes. As result, the papers examined in this

chapter, have been the ones that have provided low temperature (800°C or less) depositions that result in non-crystalline silicon carbide layers that are similar to the research discussed in this thesis.

CHAPTER 3.

UNDOPED SILICON CARBIDE FILMS:

DEPOSITION EXPERIMENTS AND MATERIAL CHARACTERIZATION

This chapter reviews the initial experiments performed to determine the optimal conditions for the deposition of undoped stoichiometric silicon carbide using di-tert-butylsilane (DTBS) as a single source. The details of the deposition techniques and the material characterization methods are described in full.

3-1 Properties of DTBS

As earlier stated, DTBS was used as the source of both the silicon and carbon component of the undoped silicon carbide films. DTBS is an alkylsilane with structure shown below in Figure 3-1 [18].

DTBS Structure
Figure 3-1

DTBS is a liquid at room temperature with a high vapour pressure, allowing the vapour to be drawn through a mass flow controller into a standard LPCVD furnace. In the furnace, DTBS adsorbs on the substrate surface and decomposes to form silicon carbide. The details for the reaction mechanism are not yet known.

3.2 Experiments

Silicon carbide films were grown on monitor quality, 150 mm diameter p-type (100) silicon wafers of 8 to 15 Ω -cm resistivity. Identification numbers were laser scribed on the wafers prior to use. Organic and inorganic film contaminants and transition metal deposits were removed from the wafers using the Kern and Puotinen pre-furnace clean (RCA clean) [19]. In addition on some wafers a 300 nm layer of silicon dioxide was thermally grown using wet oxygen prior to the SiC deposition. The silicon dioxide was used to delineate the silicon carbide films from the underlying silicon thus making it possible to determine the thickness of the deposited films by observation of an SEM cross section.

The SiC films were deposited in a modified ASM Plasma 3 low-pressure hot-wall furnace. (Although this furnace had plasma enhanced CVD capability, this was not used in the experiments described here). The temperature of the furnace was determined via thermocouples mounted externally to the quartz tube wall. A temporary internal thermocouple was used approximately once every three months to calibrate the external thermocouples. The operation of the furnace was controlled by computer. The furnace was vented with Nanochem purified argon prior to each deposition step. This procedure helps avoid oxygen and water vapour adsorption on the tube walls which may lead to oxygen contamination in the deposited films. The liquid DTBS source was contained in a stainless steel ampule in an Olin Hunt Model 825 Temperature Controller set at 20°C, giving a vapour pressure of 25 Torr. All gases were injected into the furnace tube through the load end, without the use of a gas distribution manifold.

The wafers were held in an open quartz boat at the locations shown in Figure 3-2. The same locations were used for all the experiments described in this thesis to minimize any changes in the deposited film properties due to local variations in gas flow.

Location of Wafers in Furnace Tube
Figure 3-2

The experiments on the undoped films are summarized in Table 3-2. The objective of these experiments was to determine a baseline process for the deposition of good quality, oxygen free, stoichiometric silicon carbide films. These experiments examined the effects of varying:

- 1) Temperature - 550°C to 800°C.
- 2) Pressure - 250 mTorr to 21 Torr.
- 3) DTBS flow rate - 250 sccm to 350 sccm.
- 4) Argon carrier gas flow rate - no carrier gas or 250 sccm to 1000 sccm.
- 5) Nanochem source gas purification - yes or no.
- 6) Deposition time - 4 mins to 60 mins.

LOT #	DTBS FLOW RATE	TEMP deg C	Argon FLOW RATE	NANO CHEM yes/no	PRESS Torr	DEP TIM E mins	FILM Thick nm	DEP RATE um/min	FTIR Si-O Si-C N/Y	AUGER Si C O % of layer	HRD Si C O H element/Si
1-201	350	600	500	no	0.35	30	328	11	N Y	80 18 2	N/A
1-202	350	600	500	no	0.35	60	328	11	N Y	80 18 2	N/A
1-208	350	600	500	yes	0.35	60	850	14	N Y	72 28 0	N/A
1-209	350	600	1000	yes	0.5	60	930	15	N Y	72 28 0	N/A
1-210	350	600	270	yes	0.35	60	1200	20	N Y	73 27 0	N/A
1-211	350	700	500	yes	0.4	60	>2100 0	>350	N Y	65 35 0	N/A
1-212	350	550	500	yes	0.35	60	90	1.5	N Y	51 30 19	N/A
1-213	350	800	500	yes	0.5	60	>2400 0	>400	N Y	45 55 0	1 0.836 0.061 0.073
1-214	350	700	500	yes	1	60	18500	310	N Y	60 40 0	1 0.707 0.076 0.073
1-215	300	700	500	yes	0.35	3	830	280	N Y	65 35 0	1 0.689 0.089 0.056
1-216	280	700	500	yes	0.4	3	390	130	N Y	61 39 0	1 0.707 0.067 0.034
1-217	250	750	500	yes	0.45	60	28000	470	N Y	56 44 0	1 0.948 0.076 0.053
1-218	250	750	500	yes	0.45	4	1000	250	N Y	58 42 0	N/A
1-219	250	800	500	yes	0.5	4	600	150	N Y	40 56 4	N/A
1-220	250	775	500	yes	0.35	4	730	180	N Y	52 48 0	N/A

Deposition Conditions of Undoped Films
Table 3-1

3.3 Results

The stoichiometry of the films was determined by Auger Electron Spectroscopy (Auger or AES) and elastic recoil detection (ERD). Both techniques are suited to the detection of light elements, which is appropriate for an SiC film. Auger analysis is excellent at determining the percentage of silicon, carbon and oxygen while ERD can determine the elements silicon, carbon, oxygen and hydrogen. The Auger analysis was performed at Charles Evans Associates in California and the ERD was performed by INRS in Montreal.

Fourier transform infrared (FTIR) and Raman spectroscopy were used to examine the chemical bonding in the film. FTIR can be used to infer bond stretch and rotation. Ellipsometry and scanning electron microscopy (SEM) were used to determine the film thicknesses. Since the silicon carbide film looked very similar to the underlying silicon wafer in SEM cross section, a silicon dioxide layer was grown on the silicon wafer to delineate the silicon carbide film from the wafer.

Transmission electron microscopy (TEM) and electron diffraction were used to determine the crystal structure of the films. If crystallites were visible in the TEM image, electron diffraction was performed. The spacing of the concentric rings on the diffraction pattern was used to identify the film crystal structure and to infer the composition.

3.3.1 Elimination of oxygen in the films

AES suggested that the first silicon carbide films deposited using DTBS had a high oxygen content (5 to 10%, depending on the wafer examined). Oxygen is known to form generation-recombination centres that can increase junction leakage. Therefore, even though this percentage of oxygen is at the limit of detectability for Auger analysis, as a precautionary measure steps were taken to reduce oxygen incorporation in the films before pursuing further experiments. The primary source of oxygen was expected to be

outgassing of water vapour from the quartz furnace tube walls. While production furnaces are normally idled at 400°C to 900°C, the research furnace used here was left at a temperature of 50°C when not in use for processing. At this temperature water vapour can easily be adsorbed. Consequently, an argon carrier gas was added during the deposition. The argon gas sweeps the water vapour out of the system. The argon was also purified with a Nanochem filter [20] in order to remove any oxygen or water vapour contamination in the argon source.

Once the Nanochem purified argon carrier gas was introduced, Auger and ERD analysis showed no detectable oxygen in the bulk of most of the films. However, the ERD results did indicate the presence of oxygen at both the surface and at the silicon/silicon carbide interface in all the films. This oxygen is thought to be due to the native oxide layers grown on the surface of the silicon wafer, and on the surface of the silicon carbide. The only silicon carbide film that had a detectable level of oxygen in its bulk region was from run 1-212. But since the thickness of this film is less than 10 nm, this oxygen is also thought to be due to the native oxide layers.

3.3.2 Stoichiometry of the Films

The main factor that controls the stoichiometry of the films is the deposition temperature. Figure 3-3 shows the effect of increasing temperature on the silicon/carbon ratio of the films. A stoichiometric silicon carbide film is formed at a deposition temperature of approximately 775°C. At temperatures above 775°C, the film is carbon-rich and below 775°C, the film is silicon-rich. The stoichiometry was not found to have a significant dependence on pressure or gas flow rate. Similar results have been reported by Levy *et al* using the same DTBS source [21]. As a result all subsequent experiments were performed at temperature of 750 to 775°C, in order to produce stoichiometric or near stoichiometric films.

Stoichiometry vs Temperature
Figure 3-3

3.3.3 Chemical Bonds

FTIR was able to detect the silicon-carbon bond in all of the deposited films. Figure 3-4 shows an example of a typical FTIR spectrum. The large peak at 780 cm^{-1} occurs on all FTIR spectra of the deposited films. This peak corresponds to a silicon - carbon chemical bond [22].

The Raman spectroscopy results indicated that the films deposited at temperature below 750°C were predominately amorphous silicon. Above 750°C , Raman spectroscopy indirectly indicated the presence of silicon-carbon bonds. Figure 3-5 shows a typical Raman spectrum. This graph shows two wide peaks at 1400 and 800 cm^{-1} . Two peaks at these wavelengths have been reported elsewhere for amorphous and micro-crystalline silicon carbide films [23].

Sample of Typical FTIR Spectrum
Figure 3-4

Sample of Typical Raman Spectrum
Figure 3-5

Ellipsometry was also performed on the films at wavelengths of 830.0 and 632.8 nm using a Rudolf ellipsometer. The absorption coefficient for both these wavelengths is effectively zero, since both correspond to photon energies less than the SiC bandgap. The ellipsometer can also be used at a wavelength of 405.0 nm, but this is unsuitable for the present work since silicon carbide is highly absorptive at this wavelength. The refractive index of all the films deposited at 775°C was 2.7 ± 0.2 , which agrees with the known value for bulk silicon carbide [24].

3.3.4 Crystal Structure

The TEM photo shows no resolvable crystal structure, demonstrating that the as-deposited films were amorphous. Changes in crystallinity with annealing are discussed in the next chapter.

3.3.5 Film Uniformity and Thickness

Film thicknesses were determined by a combination of fringe counting and ellipsometry. The first or thinnest fringe is blue followed by a series of pink-green fringes. Each fringe represents a thickness of 90 nm. The fringes are counted to determine an approximate thickness. Ellipsometry was then used to determine the position within the fringe cycle, allowing an unambiguous thickness measurement. In some cases thicknesses were verified by SEM cross-sectional analysis.

The silicon carbide films produced in all of these experiments showed a high degree of cross wafer non-uniformity. The thickness of the deposited films also varies with their location within the quartz boat and with their proximity to the DTBS gas inlet (Figure 3-2). The wafers closest to the tube door where the source inlet is located have up to three times the deposited film thickness of wafers located at the back of the boat. This trend continues across the wafer, with the edge of the wafer closest to the door having the thickest deposit.

3.3.6 Deposition Rate

The experiments covered in this thesis do not contain enough information to determine the effects of each process variable on the deposition rate; however some clear trends do exist. Figure 3-6 shows the effect of DTBS flow on deposition rate at 700°C.

DTBS Flow Rate vs Deposition Rate at 700°C
Figure 3-6

The deposition rate was found to be strongly dependent on temperature. For temperature below 650°C, the deposition rate is below 3 nm/min. The deposition rate for temperatures greater than 700°C is greater than 10 nm/min. Since stoichiometric silicon carbide is formed at 700°C, the deposition rate for all the silicon carbide films is necessarily high.

3.3.7 Film Quality and Stress

The major factor in determining the film specularity was found to be the gas pressure during deposition. The films deposited at low pressures (350 to 500 mTorr) had a specular surface finish. The films deposited at higher pressures (500 to 1000 mTorr) had a very rough finish and tended to flake off the wafer surface. These films had an

appearance similar to badly rusted steel. Consequently, the films produced at high pressures were rejected as being completely unsuitable for further processing.

Films thicker than 1 μm exhibit stress lines parallel and perpendicular to the $\langle 110 \rangle$ direction. These patterns are similar in appearance to a patchwork quilt. Although no quantitative measurements were made, it seems clear that the SiC films were under high tensile stress. At still greater thicknesses the films were found to crack along the stress lines and partially delaminate. Delaminating films were found to tear gouges and holes in the underlying silicon or silicon dioxide layers, presumably due to the mechanical strength of the silicon carbide and its strong adhesion to the substrate. Films thinner than about 200 nm did not exhibit stress lines and did not delaminate.

3.4 Summary

The composition of silicon carbide films deposited by LPCVD from a DTBS source was found to be strongly temperature dependent. A temperature of 775°C was found necessary to produce stoichiometric SiC. At lower temperatures films were silicon-rich, and at higher temperatures carbon-rich. Deposition rates at 775°C are high (approximately 20 nm/min for a DTBS partial pressure of 250 mTorr). For the end-feed reactor used here film thickness was found to vary greatly over the wafer diameter, and along the boat. Films appeared to be under high tensile stress, although this was not measured quantitatively.

CHAPTER 4
DOPED SILICON CARBIDE FILMS:
EXPERIMENTS AND MATERIAL CHARACTERIZATION

This chapter examines the experiments used to determine doping conditions for the silicon carbide films deposited from the DTBS source. The films were doped *in-situ* with phosphorus using another organic source -- tertiarybutylphosphine (TBP). The experiments and the results are discussed in this chapter.

4.1 Experiments

The most commonly used source for *in-situ* doping of polysilicon films is phosphine (PH_3). This might therefore appear to be the most logical source for *in-situ* doping the silicon carbide; however, phosphine is highly toxic, and safety concerns precluded its use here. Thus the alternative source of TBP was used to dope the films.

The TBP is a liquid with a boiling point at atmospheric pressure of 54°C and a vapour pressure at 10°C of 141 Torr [25]. In the present experiments, the TBP source was maintained at a temperature of 20°C and the vapour was injected into the furnace tube through a mass flow controller.

As with the previous set of experiments, the doped films were grown on monitor quality, 150 mm diameter, (100) silicon wafers with a resistivity of 8 to $15\ \Omega\text{-cm}$. All the wafers were scribed for identification and received a pre-furnace RCA clean. In addition, a 300 nm layer of silicon dioxide was thermally grown some of the substrates. The blank wafers were generally used in basic material analysis such as FTIR and AES while the wafers with the silicon dioxide layers were used in resistivity tests and thickness

measurements. These wafers were placed in the quartz boat in the same positions as the wafers in the undoped experiments (see Figure 3-2).

Three experiments or runs were performed using TBP to *in-situ* dope the silicon carbide films. The conditions of deposition are shown below in Table 4-1. Because the doped films needed to be as close to stoichiometric silicon carbide as possible, deposition temperatures of 750, 775 and 800°C were used (Figure 3-3.) In addition, the Nanochem purified argon carrier gas was used during the deposition to minimize the oxygen content of the films. Deposition was carried out at pressures between 350 and 500 mTorr in order to produce specular films. Also the flow rate of the DTBS was maintained at 250 sccm. Since the reaction is mass transport limited, reducing the flow rate reduces the silicon carbide deposition rate.

Run No	DTBS flow rate (sccm)	Deposition Temp. (degrees C)	Argon flow rate (sccm)	Pressure (mTorr)	TBP flow rate (sccm)
1-223	250	750	500	450	130
1-224	250	800	500	500	340
1-225	250	775	500	350	130

Deposition Conditions of Doped Runs

Table 4-1

The flow rate of the TBP varied between 130 and 340 sccm. (The maximum output of the mass flow controller is 340 sccm.) The deposition time for all three experiments was four minutes. These conditions were selected to achieve controlled films thinner than 200 nm. The three films were then subjected to a rapid thermal anneal (RTA)

at 900, 1000 and 1200°C, respectively, for 10 seconds in a nitrogen ambient. The conductivity of the films was determined by a four-point probe resistance measurement.

4.2 Results

4.2.1 Material Analysis

The doped silicon carbide films were tested in various ways in order to determine their chemical composition. Auger results from Charles Evans indicated that the ratio of silicon to carbon in all films was approximately 1 to 1, even for the highest TBP flow rate. Both FTIR and Raman results identified, directly in the case of FTIR and indirectly in the case of Raman (see Section 3.3.3), the presence of silicon-carbon bonds. In addition, ellipsometry performed at both 632.8 nm and 830.0 nm wavelength indicated a refractive index of about 2.7. These conclusions were consistent for samples of doped silicon carbide films measured after rapid thermal annealing. Consequently, it was concluded that the addition of the dopant and the RTAs did not alter the stoichiometry of the silicon carbide films.

4.2.2 Bandgap Determination by Optical Absorption

Optical absorption spectra for doped SiC films deposited at 775°C using the reactor described here have been reported by Tay *et al* [26]. When the absorption coefficient is plotted against the photon energy, the zero absorption bandgap of the material is 2.54 eV. This agrees with the known bandgap of 6H SiC.

4.3.3 Film Crystallinity

The crystallinity of the deposited films changed after rapid thermal annealing. Before the rapid thermal anneal, the films were amorphous just as in the undoped case. A TEM image of the film before the RTA is shown in Figure 4-1. After annealing, the material changed to a microcrystalline phase with a grain size on an order of 20 nm. (See Figure 4-1.) Electron diffraction analysis was used to determine the structure of the crystallites. These films were all grown over the silicon wafers that had a layer of thermally grown oxide.

F1100

F1200

TEM and X-RAY Diffraction Patterns
for Samples F1100 and F1200
Figure 4-1

The radii of the diffraction rings were used to determine the spacing of the lattice planes, d , of the crystallites using the following formula,

$$R = \frac{\lambda L}{d} \quad (5)$$

where the camera constant $L = 100.1$ cm, R is the measured radius of the ring and λ is the electron wavelength given by

$$\lambda = \frac{h}{p} \quad (6)$$

where h is Planck's constant. The 200 keV electrons used in this experiment are relativistic, so the momentum p must be computed using

$$p = \frac{1}{c} \sqrt{(K + m_0 c^2)^2 - (m_0 c^2)^2} \quad (7)$$

where K is the kinetic energy (200 keV) and m_0 the electron mass. Table 4-2 and Table 4-3 show the observed d -spacing for samples F1000 and F1200 respectively [28]. The tables also contain the expected d -spacing values for 5H silicon carbide, beta silicon carbide and silicon. The experimental patterns show no evidence of the ring corresponding to the (111) plane of silicon, which would be expected to be prominent if silicon microcrystallites were present. The best fit appears to be with 5H SiC, although the rings are too broad to discount the possibility that other SiC polytypes might also be present.

Radius (in)	D-spacing of material (Å)	D-spacing of 5H SiC (Å)	D-spacing of 6H SiC (Å)	D-spacing of silicon (Å)
0.55	4.564	4.27	2.621	4.27
0.8	3.138	3.34	2.511	3.34
1.0	2.511	2.52	2.352	2.52
1.2	2.092	2.35	2.174	2.35
1.4	1.793	1.81	1.537	1.81
1.5	1.674	1.68	1.418	1.68
1.7	1.477	1.54	1.311	1.54

D-spacing of Sample F1000
Table 4-2

Radius (in cm)	D-spacing of material (Å)	D-spacing of 5H SiC (Å)	D-spacing of 6H SiC (Å)	D-spacing of Silicon (Å)
.7	3.58	3.34	2.621	3.135
1.05	2.391	2.35	2.511	1.637
1.25	2.008	1.99	2.352	1.358
1.45	1.731	1.68	2.174	1.246
1.6	1.569	1.54	1.537	1.108
1.75	1.434	1.425	1.418	1.045
1.85	1.357	1.376	1.311	

D-spacing of Sample F1200
Table 4-3

4.3.2 Resistivity of the Material

The silicon carbide films that were doped with 130 sccm of TBP did not conduct significantly prior to annealing. These wafers also did not conduct even after successive anneals at 900, 950 and 1000°C. The silicon carbide films doped with 340 sccm of TBP did conduct both prior to and after annealing. Results are given in Table 4-4 for the resistance before and after annealing of various pieces of a single wafer from run 1-224.

Sample	Before RTA		RTA	After RTA		The ratio of the value by before and after RTA
	R_s (kohm/sq)	ρ (ohm-cm)	T_{ann} (degree C)	R_s (kohm/sq)	ρ (ohm-cm)	
F900	33.9	1	900	5.15	0.15	0.15
F1000	49	1.77	1000	5.85	0.21	0.12
F1100	5.75	0.215	1100	0.566	0.02	0.098
F1200	59.8	2.08	1200	9.83	0.34	0.164

Doped Silicon Carbide Results for Run 1-214
(TBP flow rate, 340 sccm)

Table 4-4

The lowest resistance obtained was for the wafer annealed at 1100°C. The sheet resistance of this piece from sample F1100 was 500 Ω /sq, corresponding to a resistivity of 0.02 Ω -cm. The resistance for this piece of the wafer was an order of magnitude lower than for the other pieces of the wafer both before and after the anneal. This piece was located on the edge of the wafer that was the closest to the dopant inlet; consequently, it should contain a higher concentration of dopant and hence have a lower resistance than the other pieces. (See Figure 4-2.)

a) Resistance of Samples Prior to Anneal

b) Resistance of Samples after Anneal
Annealing Experiments on Doped Samples of Run 1-224

Figure 4-2

The resistivity of most of the heavily doped samples were between 0.15 and 0.34 $\Omega\text{-cm}$, after annealing. The exception is sample F1100 which had a resistivity of 0.02 $\Omega\text{-cm}$. These resistances are relatively high compared to phosphorus doped polysilicon layers. However, the ratio of the resistance before and after anneal indicates the effectiveness of the thermal cycle in increasing the conductivity of the films. Figure 4-

3 plots this ratio vs anneal temperature. This plot suggests that the most effective anneal temperature is 1100°C.

The resistance ratio decreases with increasing temperatures for anneal temperatures below 1100°C but increases for temperatures above 1100°C. These results suggest that the dopant could be evaporating from the surface of the silicon carbide film during the higher temperature anneals. Since the phosphorus diffusion coefficient in silicon carbide is very low [27], one might expect that little dopant would reach the film surface and evaporate. However, the fine-grained polycrystalline structure of the annealed films might allow for rapid transport of dopant to the surface via enhanced diffusion along the grain boundaries. This would be a particularly severe effect for the more lightly doped samples, where insufficient dopant might be left to saturate the grains.

Resistance Ratio vs Temperature
Figure 4-3

4.3 Conclusions

It is possible to obtain fairly low resistivities in silicon carbide films deposited from DTBS using TBP as an *in-situ* dopant. However, film resistivities are still very high

compared to heavily doped polysilicon. Resistivity can be reduced by as much as an order of magnitude by rapid thermal annealing at $\sim 1100^{\circ}\text{C}$. Typical resistivities after annealing were 0.15 to 0.35 $\Omega\text{-cm}$. The lowest resistivity obtained was 0.02 $\Omega\text{-cm}$ for a sample located close to the TBP gas inlet. TEM suggests that the film structure changes from amorphous to fine-grained polycrystalline after annealing.

CHAPTER 5

SILICON CARBIDE EMITTER DIODES: **FABRICATION EXPERIMENTS AND DEVICE CHARACTERIZATION**

This chapter discusses the fabrication of diodes and lateral bipolar transistors with silicon carbide emitters deposited using the techniques developed in chapters 3 and 4. The electrical characteristics of these devices are presented and analyzed.

5-1 Diode Fabrication

The cross-sectional structure of the silicon carbide emitter diodes is shown in Figure 5-1. These devices were formed on 50 mm diameter 2 Ω -cm p-type substrates of (100) orientation. The substrate doping was approximately $4 \times 10^{15} \text{ cm}^{-3}$. The wafers received an RCA clean prior to the growth of a 200 nm passivating thermal oxide layer in a dry oxygen ambient.

Figure 5-1

To form diode active areas, windows were etched open in the passivating oxide using buffered hydrofluoric acid with a photoresist mask. Simple hard-contact printing techniques were used for this and all subsequent lithography steps. The photoresist was

stripped in $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$ solution, after which the wafers received another RCA clean. The silicon carbide film for one group of wafers was deposited at 775°C while the film for the second group was deposited at 750°C . The gas flows for DTBS and TBP were 250 and 340 sccm respectively for both groups, while the deposition pressure was 500 mTorr. The deposition time was adjusted to give a film thickness of approximately 100 nm. During the deposition step, the 50 mm diameter diode wafers were attached to 150 mm backing wafers with quartz clips, and positioned at the locations found to give the lowest resistivity in the experiments on *in-situ* doping described in the previous chapter. The 150 mm backing wafers were placed in the quartz boat with dummy wafers in order to maintain the flow patterns of the gases.

After the silicon carbide deposition step, the wafers were overlaid with 60 nm of *in-situ* doped amorphous silicon. This layer was deposited at 560°C and 0.4 Torr pressure from a 150:1 silane/phosphine mixture. After the deposition, the silicon layer was re-crystallized into polysilicon with a 60 min. 650°C anneal step performed in nitrogen. Silicon carbide has been reported as having poor ohmic contact to both metals and silicides; consequently most researchers use a polysilicon layer as an intermediary between the metal layers and the silicon carbide

A positive photoresist mask was next applied to pattern the silicon carbide/polysilicon stack. The stack was then etched in CF_4/O_2 at a pressure of 0.3 Torr and a power of 100 W in a Technics Planar Etch II planar plasma etcher. The underlying oxide layer was used as an etch stop.

Following the etch, the resist was stripped and the wafers received another RCA clean. The devices were then rapid thermal annealed at either 1000 or 1100°C in a Heatpulse 210 system. Both RTAs were performed in a nitrogen ambient for 10 seconds. Ohmic contact to the emitter was made with a 200 nm sputtered TiW barrier layer overlaid with $1\text{ }\mu\text{m}$ of e-beam evaporated aluminum. Aluminum was used as a backside contact. The contacts were sintered at 400°C for 20 minutes in a pure hydrogen ambient.

5-2 Device Mask Layout

Figure 5-2 shows the device mask layout. This mask set contains diodes with active areas ranging from $10\text{ }\mu\text{m} \times 10\text{ }\mu\text{m}$ to $500\text{ }\mu\text{m} \times 1\text{ mm}$. The contact to the p side of the diode is made via the aluminum backside contact while the contact to the n side emitter is made through the contact pads on the front side of the wafer. In some cases the front metal contact overlies the active area, in other cases the contact is made over field oxide adjacent to the active area. Other structures have no metalization at all, so that contact must be made by probing directly into the doped polysilicon.

- 1. Large Area Diode
- 2. Lateral Bipolar Transistor
- 3. Metal Gate Capacitor
- 4. Poly Gate Capacitor
- 5, 6, 7. Diodes - $300\text{ }\mu\text{m}$ square
- 8-17 Small Area Diodes
- 18. Berger Structure.
- 19. Vander Pauw Cross

Device Mask Layout
Figure 5-2

There is also a lateral bipolar junction transistor. These devices consist of a 10 μm wide, 200 μm long emitter stripe separated from a u-shaped collector stripe by a 30 μm region of p-type substrate, as shown in Figure 5-3. In the case of this BJT, both the emitter and the collector are formed from the silicon carbide/polysilicon stack. In addition to the diodes and transistors, the mask also contains a van der Pauw cross for measuring the sheet resistance, a coarse Berger structure for measuring contact resistivity, and capacitors.

Lateral Bipolar Device
Figure 5-3

5-3 Electrical Characterization

The slight difference in the deposition conditions and the annealing temperature between group 1 and group 2 did not appreciably change the device electrical characteristics. Consequently, the following discussion is of typical device characteristics found on both wafers.

The current-voltage characteristics for a typical SiC emitter diode are shown in Figure 5-4. The forward characteristics are ideal over nearly six decades of current. If the diode law is written in the form

$$J = J_0 e^{qV/nKT} \quad (7)$$

the ideality factor, n , is approximately 1.01. Assuming an electron lifetime of 10 μsec in the bulk substrate and a temperature of 25°C, an injection-diffusion saturation current J_0 of $2 \times 10^{-11} \text{ A-cm}^{-2}$ would be expected at this substrate doping. This is close to the measured J_0 value of $6 \times 10^{-12} \text{ A-cm}^{-2}$, implying that the diode current is dominated by the injection into the bulk.

Gummel Plot of Silicon Carbide Diode
Figure 5-4

The high injection efficiency of the SiC emitter was confirmed by measurements on lateral bipolar transistors. A typical Gummel plot for one of these devices is shown in Figure 5-5. The peak current gain β is approximately unity. Although the gain is low, it is comparable to that seen on identical devices with good quality polysilicon emitters. The

gain is almost certainly limited by recombination along the silicon surface, especially since the device has a large emitter-collector separation.

Gummel Plot of Lateral Bipolar Transistor
Figure 5-5

The reverse breakdown characteristics are shown in Figure 5-6. The figure shows a typical reverse characteristic for a large-area diode. The hard breakdown occurs at ≈ 60 V reverse bias. At 5 V, reverse bias, the leakage current is less than 10 nA-cm^{-2} .

Reverse Breakdown of Silicon Carbide Diode
Figure 5-6

One of the main problems encountered in the use of SiC emitters for high-speed HBT's has been the inability to reduce the resistivity of the SiC layer below $10 \text{ m}\Omega\text{-cm}$. Assuming a uniform resistivity of $10 \text{ m}\Omega\text{-cm}$ throughout the 100 nm thick emitter film, one would expect the emitter resistance to be approximately $10 \Omega\text{-}\mu\text{m}^2$. (Any obstacle to electron transport across the SiC/substrate interface would only add to this figure.) This lies somewhat below the upper bound of $100 \Omega\text{-}\mu\text{m}^2$ generally considered acceptable for emitter resistance in high-speed ECL circuits. Unfortunately, relatively little information regarding emitter resistance can be obtained from the diodes, since the resistance of these devices is dominated by the thick lightly-doped substrate. Figure 5-7 shows that the smallest device's (emitter window of $20 \mu\text{m}$ square) J-V characteristics deviate from the extrapolated ideal J-V curve by 270 mV at a current density of $100 \text{ A}\text{-cm}^{-2}$, indicating that the SiC emitter resistance is less than $7 \times 10^6 \Omega\text{-}\mu\text{m}^2$. Fabrication of vertical bipolar transistors would allow more accurate measurement of the emitter resistance and injection efficiency.

Emitter Resistance of Silicon Carbide Diode
Figure 5-7

As expected, the use of a heavily doped polysilicon overlay allowed low resistance contacts to be made to the SiC emitter. Reasonably good ohmic contacts were also formed when the TiW contact layer was deposited directly over SiC without an intermediate polysilicon buffer.

Diffusion of common dopants in SiC is relatively slow, so it would be expected that phosphorus diffusion from the silicon carbide into the underlying substrate would be negligible, particularly given the short anneal cycle used here. However, the sheet resistance of the annealed SiC overlying the silicon substrate is only half that of material over oxide, suggesting that some diffusion into the underlying silicon has occurred. This is also consistent with the relatively high reverse breakdown voltage noted above, which suggests that some rounding of the junction edges has occurred.

5-4 Conclusion

SiC films formed by LPCVD from a di-tertiary-butylsilane source doped *in-situ* with tri-butyl-phosphine can serve as a good-quality emitters. The forward characteristics of such devices formed on lightly doped silicon substrates are ideal for over six decades of current. These devices were formed using much lower thermal budget than in previously reported SiC emitters. The maximum thermal budget of a 10 second 1000°C RTA cycle would enable the preservation of shallow implanted bases and thus permit high performance transistors to be formed. It remains to be seen whether or not the *in-situ* doping technique can be used to provide low enough emitter resistance to allow the passage of the high current densities ($\sim 10^5$ A-cm⁻²) required in high-speed bipolar devices without introducing unacceptably large voltage drops.

CHAPTER 6

SUMMARY AND CONCLUSIONS

This chapter summarizes the experimental results reported in the previous chapters, and examines the prospects for future work on silicon carbide emitter films deposited from DTBS.

6-1 Summary

In the initial experiments, a process for the LPCVD of undoped SiC films from a DTBS source in a conventional hot-wall furnace was developed. The films were characterized using Auger electron spectroscopy (AES), ellipsometry, Fourier transform infrared spectroscopy (FTIR), transmission electron microscopy and electron diffraction, and Raman spectroscopy. AES showed that stoichiometric films were obtained at a temperature of approximately 750°C, pressure of 0.45 Torr and DTBS flow rate of 350 sccm. Under these conditions the deposition rate was ~ 25 nm/min. Deposition at lower temperatures gave silicon rich films, while at higher temperature the films became carbon-rich. A peak at 800 cm⁻¹ in the FTIR spectrum revealed the existence of silicon-carbon bonds. Ellipsometry confirmed that the films had the refractive index of 2.7 expected for bulk silicon carbide. Both transmission electron microscopy (TEM) and Raman spectroscopy showed that the as-deposited films were amorphous. However, TEM showed the presence of micro crystallites after rapid thermal annealing at 1100°C. Although no quantitative measurements of film stress were made, tensile stress was high enough to cause film cracking for layers thicker than approximately 1 µm. Levy *et al* reported similar results for undoped SiC films deposited from DTBS [26].

Once the conditions required to form stoichiometric undoped SiC from DTBS were established, *in-situ* doping using tri-butylphosphine (TBP) as a phosphorus source was examined. High flow rates of TBP (>340 sccm) were needed to obtain films with

measurable conductivity at a deposition temperature of 775°C. Auger electron spectroscopy showed that doping did not affect film stoichiometry. Rapid thermal annealing at 1000 to 1200°C was used to activate the dopant. Compared to as-deposited films, the resistivity dropped by approximately an order of magnitude after annealing at 1100°C, but rose slightly at higher temperatures. Annealing had far less effect than for *in-situ* phosphorus-doped amorphous silicon, where the resistivity can be lowered by over three orders of magnitude. The most conductive film had a resistivity of 0.02 Ω-cm, comparable to the lowest values reported by other groups for thin SiC films [53-55].

In-situ doped SiC films were used to form the emitters for diodes on 2 Ω-cm (100) p-type substrates. Lateral BJTs with 10 μm by collector stripes were also fabricated. Figure 5-4 shows the forward characteristics of a typical diode. The ideal diode law $J = J_0 e^{\frac{qV}{kT}}$ is obeyed for over six decades of current. The saturation current J_0 was extrapolated from the characteristic and compared with the theoretical injection-diffusion saturation current, J_{00} , calculated from the known substrate doping and an assumed electron lifetime of 10 μsec. The actual and theoretical saturation currents agreed closely, suggesting that the diode current is dominated by electron injection into the substrate. This conclusion is supported by the lateral bipolar transistor, which typically gave a common emitter current gain slightly greater than unity. Comparable current gains are routinely obtained for lateral BJTs with polysilicon emitters on these substrates.

Typical diode reverse characteristics are shown in Figure 5-6. Forward breakdown occurs at about 60 V reverse bias, and the leakage current at 5 V reverse bias is less than 10 nA/cm². The low reverse leakage current and high breakdown voltage are very desirable for circuit applications, but suggest that some diffusion of dopant from the SiC into the substrate has occurred, giving rounded edge to the junction depletion region.

6-2 Future Work

The generally promising results obtained with SiC emitter diodes suggest that an attempt be made to fabricate high performance vertical HBTs with silicon carbide emitters. Some work should also be done on alternative doping sources for the DTBS films. The resistivity of the SiC films might be lowered if they were doped by phosphine instead of TBP.

6-3 Conclusions

Silicon carbide emitters formed by LPCVD from di-tertiary-butylsilane show promise for the use in HBTs. Stoichiometric SiC films can be produced at temperatures below 800°C, which is compatible with the preservation of shallow implanted base profiles. With *in-situ* phosphorus doping using tri-butylphosphine, film sheet resistance after rapid thermal annealing at 1100°C is comparable to the lowest values reported by other groups. Diodes with good reverse leakage and breakdown characteristics in which the forward current is dominated by electron injection into the substrate have been formed on lightly-doped p-type substrates. Whether or not such devices may be suitable for use as emitters for high-speed ECL will depend on the achievement of sufficiently low series resistance values.

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