Low Power Gamma-Ray FG-MOSFET Dosimeter in 0.13 μm CMOS Technology

by

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Abstract

A new MOSFET dosimeter consisting of a floating-gate sensor and a reference gate-connected transistor of identical geometry fabricated in close proximity on the same silicon chip is described. In this research, 0.13 μm IBM RF-CMOS technology is used as opposed to previous work done in an older 0.8 μm DALSA CMOS technology. A set of three single floating-gate MOSFETs and their reference pairs are fabricated to realize the physical characteristics of the dosimeters prior to and after irradiation. Each of these has a gate-extension with a different size. Then these dosimeters are integrated into low-power readout circuitry. The readout circuitry is a unity-gain buffer that reflects the floating-gate voltage on the sensor and it consumes 376.8 μW of power. The integrated sensor reaches a sensitivity of 0.4 mV/Gy and is targeted for low sensitivity/ high radiation exposure applications such as blood sterilization.

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I would also like to thank my best friend and older brother, Mr. Farhad Ramezankhani and his wife for their support throughout this period of time.

On a personal note, I wish to thank my parents for their love and support throughout my studies.

Dedication

This dissertation is dedicated to...

my parents,

for their unconditional love and support,

my grandmother,

for believing in me and for her support and encouragement. Her absence is deeply felt.

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List of Symbols

A	area
C	columb or capacitance
C_{FB}	capacitances from the floating-gate to the bulk (F)
C_{FS}	capacitances from the floating-gate to the source (F)
C_{FD}	capacitances from the floating-gate to the drain (F)
C_{ox}	capacitance of oxide (F cm^{-2})
Csum	sum of capacitances (F)
D	radiation dose (J kg^{-1})
E	electric field (Vcm^{-1})
E_{dep}	energy deposited during irradiation (J)
E_{ox}	electric field across gate oxide (Vcm^{-1})
f	frequency (Hz) or fading
f	fraction of radiation generated charge trapped at interface
gm_{FG}	trans-conductance of the transistor from the floating-gate (A/V)
I_D	drain–source current (A)
I_{inj}	injector current (A)
I_{tun0}	pre-exponential current (A)
J	joule
k	Boltzman constant (1.38 × 10-23 eV/K)
L	gate length of a transistor
m	mass of matter (Si or SiO_2)
N_{it}	absolute interface trap density (cm^{-2})
N_{ot}	absolute bulk oxide trap density (cm^{-2})
O	Oxygen
q	electron charge (1.6×10^{-19} C)
Q_{col}	total charge collected (C)
Q_{fg}	charge trapped on the floating gate (C)
Q_{it}	interface trapped charge (C)
Q_{ot}	oxide trapped charge (C)
R(E)	recombination rate of the e-h pairs
T	absolute temperature (K)
t_{ox} or d_{ox}	thickness of (gate) oxide
U_T	thermal voltage (V)
V_D	voltages at the drain (V)
V_{DD}	Positive supply voltage (V)
V_{DS}	drain to source voltage (V)
V_f	constant that varies with oxide thickness (V)
V_{FGo}	initial floating gate potential (V)
V_G	gate voltage (V)
V_{inj}	tunnelling injector voltage (V)
V_{out} or V_o	output voltage (V)
V_{ox}	voltage across the oxide (V)

V_S	source voltage (V)
V_{ss}	negative supply voltage (V)
V_{th}	threshold voltage (of transistor) (V)
$V_{th}(0)$	threshold voltage (of transistor) immediately after irradiation(V)
$V_{th}(t)$	threshold voltage (of transistor) some time after irradiation (V)
V_{th0}	threshold voltage (of transistor) before irradiation (V)
W	channel width
W/L	width/length (of the gate of a transistor)
$W_{e\text{-}h}$	electron-hole pair creation energy (eV)
α	technology constant (cm^2)
δN_{it}	interface trap density (cm^{-2})
δN_{ot}	net oxide trapped charge density (cm^{-2})
ΔV_{ot}	change in oxide voltage due to irradiation (V)
ΔV_{th}	change in threshold voltage (V)
ε_{ox}	permittivity of oxide (F cm^{-1})
ε_s	permittivity of silicon (F cm^{-1})
κ	Sub-threshold slope
μ	transistor charge mobility ($cm^2\ V^{-1}\ s^{-1}$) or micro ($1x10^{-6}$)
μ_o	charge mobility before irradiation ($cm^2\ V^{-1}\ s^{-1}$)
μ_p	hole mobility before irradiation ($cm^2\ V^{-1}\ s^{-1}$)
Ψ_s	surface potential (V)
Ω	Ohm
ρ_{sio2}	SiO_2 material density

List of Abbreviations

1/f	flicker noise
^{137}Cs	Caesium-137
^{60}Co	Cobalt-60
Al	aluminum
BMC	Best Medical Canada
BPSG or bpsg	Boro-Phospho-Silicates-Glass
CMOS	Complementary Metal–Oxide–Semiconductor
dB	Decibel
dBm	measured power referenced to one milliwatt
DIS	Direct Ion Storage Dosimeter
E-beam	Electron beam
EEPROM	Electronically Erasable Programmable Read-only Memory
e-h	electron-hole pair
ESD	electro-static discharge
FG	Floating-Gate
FG-sensor	Floating-Gate Sensor
FGMOS	Floating-Gate Metal-Oxide-Semiconductor
FG-MOSFET	Floating-Gate Metal–Oxide–Semiconductor Field Effect Transistor
FGRADFET	Floating-Gate Radiation-sensitive Field Effect Transistor
FOX or fox	Field Oxide
FST	Fast Switching Traps
G	gain
γ-ray	radiation produced by gamma radiation rays
Gy	SI unit of radiation [gray]
h	holes
HCI	Hot Carrier Injection
IBM	A Commercial Foundry
IC	Integrated Circuit
I-V	current voltage
krad	kilo rad (radiation unit)
M2	metal 2 in fabrication process
M3	metal 3 in fabrication process
M8	metal 8 in fabrication process
MOSFET	Metal–Oxide–Semiconductor Field Effect Transistor
NRC	National Research Council of Canada
n-well	n-type well
Op-amp	operational amplifier
ox	gate oxide or oxide
PMOS	p-type Metal Oxide Semiconductor
p-sub	p-type silicon substrate
RADFET	Radiation-Sensitive Field Effect Transistor
RF	Radio Frequency

R_f	feedback resistance
SI	System International (of units)
Si	Silicon
SiO_2	Silicon di-oxide
SoC	System-on-Chip
SPE	Signal Processing Electronics
SST	Slow Switching Traps
ST	Switching Traps
STI	Shallow Trench Isolation
X-ray	High energy ionizing radiation

Chapter 1 Introduction

This chapter provides a brief background and motivation for this work. The thesis objectives and thesis organization are also presented.

1.1 Thesis Background and Motivation

Gamma-ray dosimetry is important to a wide range of applications such as space exploration, packaged food sterilization, nuclear facility monitoring, radiation therapy and many other usages in the biomedical field.

In the case of medical procedures involving blood transfusion, X-ray and Gamma-ray sterilization of the blood is required to avoid patient infection. Present day blood sterilization systems rely on a human operator's assessment of the color change of "rad tags" placed on each blood bag. Such crude reading mechanisms and human error cause uncertainties in the operation of the blood irradiator machine, which consequently means blood bags can be under- or over-irradiated, hence, wasting the blood. It would be a desirable upgrade if the tags could be read and interpreted automatically without being subjected to human intervention. Currently available dosimeters cannot be integrated onto ICs for automatic readout; therefore, where many blood bags are being irradiated, it takes time to process all the bags and precision is lost as the operator gets tired. Moreover, rad tags are not reusable, hence increasing the cost of blood sterilization when large quantities are involved.

Common silicon-based MOSFETs could be used as dosimeters to address both of these issues (cost and automatic readout). Floating-gate MOSFET dosimeters are based on the measurement of the threshold voltage, which ideally changes as a linear function

of absorbed dose. In addition, current MOSFET CMOS technology can be used for the associated digital, analog and radio frequency functions of automatic dosimetry readout.

A sensor device in a CMOS system would typically consist of the components shown in Figure 1. This system can get very complex with the addition of extra circuitry around the sensor, including:

1. The sensing component (which may include signal processing electronics to interface with the other components).
2. The readout component (which may consist of a wireless RF transmitter).
3. The powering component (which may be augmented by calibration and control functions).

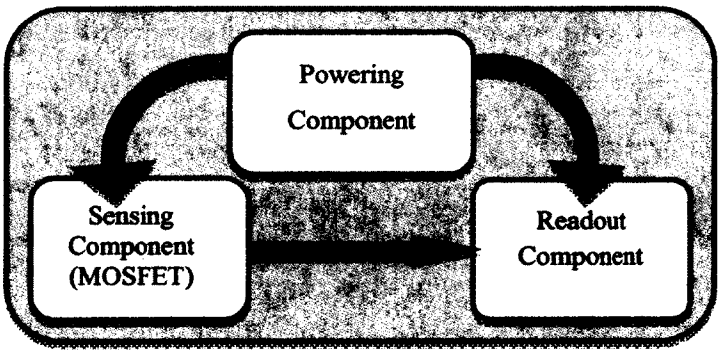

Figure 1- System level structure of a sensor device

Over the past few years, researchers in Carleton's Department of Electronics have been pursuing elements of the system concept shown in Figure 1. Focusing on the sensing component, Dr. G. Tarr developed a two-chip dosimeter (Figure 2(a)) consisting of a floating-gate (FG) MOSFET radiation sensor with a non-FG reference (Chip #1) and a high-precision op-amp with precision-matched resistors (Chip #2) [**1**]. Improvements to the FG sensor design and monolithic integration with the op-amp (signal processing

electronics) were recently implemented in Dr. M. Arsalan's dosimeter chip as depicted in Figure 2(b) [2]. The previous dosimeter designs have been implemented in an older (thick oxide) CMOS process which is ideal for dosimeter sensitivity, but ill-suited to any form of RF wireless readout.

This work attempts to take the floating-gate MOSFET dosimeter concept a step further in making it a monolithic solution in a 0.13 μm RF-CMOS process, meaning that both the FG sensor, its reference pair and the signal processing electronics i.e. the interface circuitry, be implemented on a single chip that could eventually contain RF wireless circuitry.

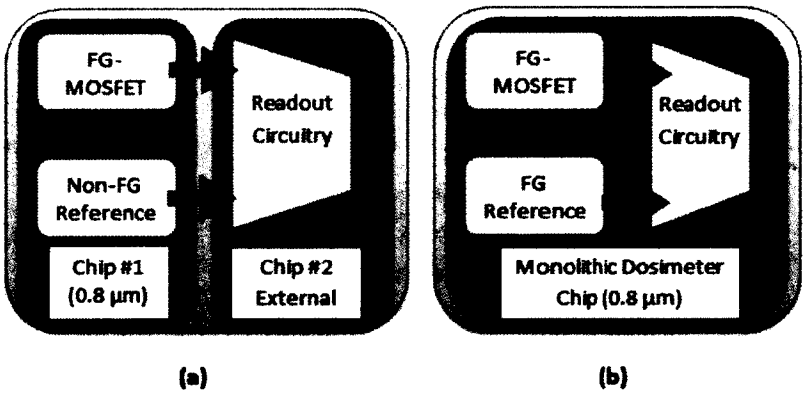

Figure 2- Dosimeter architectures: (a) Previous implementation by Dr. G. Tarr; (b) Recent implementation by Dr. Arsalan [2]

1.2 Thesis Objectives

The overall objective of this thesis work is to demonstrate the feasibility of using a modern RF-CMOS process for the realization of a □-ray dosimeter. The specific objectives pursued in this research are as follows:

1. Conduct a comprehensive review of the current state of the art of radiation dosimeters to situate FG-MOSFET sensor devices in a broader context.

2. Perform an experimental analysis of the sensitivity of floating-gate dosimeters to understand key design trade-offs.
3. Design and lay out various IC configurations of floating-gate dosimeters in 0.13 μm RF-CMOS technology with the aim of investigating device parametric and geometric effects.
4. Design appropriate readout interface by embedding the dosimeter within operational-amplifier circuitry on the same IC chip.
5. Following fabrication in a commercial foundry (IBM), carry out full characterization of the performance of the dosimeters before irradiation to verify baseline operation.
6. Perform irradiation of the dosimeters; analyze the devices' performance and sensitivity in order to assess the validity of the various dosimeter designs.

1.3 Thesis Organization

The remainder of this thesis is organized as follows. Chapter 2 presents the theory of the operation of MOSFET dosimeters. Chapter 3 presents different approaches to the design of dosimeters, their applications, and the benefits of continuing research work on modern on-chip integrated dosimeters. Chapter 4 introduces the design of the new modern CMOS dosimeter along with layout considerations and initial testing. Chapter 5 contains testing procedures, test results and discussion. Chapter 6 provides conclusions and discusses future work on possible improvements on sensitivity of dosimeters, tackling issues found during the design and testing, better designs for the readout circuitry, and other sensor configurations.

Chapter 2 Theoretical Concepts of MOSFET Dosimetry

In the first part of this chapter, an introduction to the applications, the sources, the nature, and the units of radiation are presented to familiarize the reader with necessary background information. Then an introduction to MOSFET operation as well as the impact of radiation on MOSFET operation is presented.

2.1 Radiation

Ionizing radiation is thoroughly discussed in the following sub-sections.

2.1.1 Radiation Applications

Sterilization using gamma radiation has been used in commercial and medical fields since the early 1960's [3], [4]. Irradiation of food packaging [4] is an example of commercial application of gamma radiation. Irradiation of surgical gloves, gowns, masks, dressings, raw materials for pharmaceuticals and cosmetics, and blood [3] are examples of medical sterilization applications. It is clear that dosimetry plays a crucial role at various stages of the process, namely, dose setting, process validation and process control. Therefore, every radiation sterilization facility must have a well-equipped dosimetry system. The gamma irradiation source has an advantage over other radiation sources such as X-ray and e-beam in processing non-uniform and high density products. In general, the above-mentioned products and substances are considered thermo-sensitive which means that the sterilization process of these devices needs to be done without changes in their temperature, hence the usefulness of gamma irradiation source.

2.1.2 Gamma Radiation Sources

The most suitable gamma radiation sources for radiation processing are ^{60}Co and ^{137}Cs because of the relatively high energy of their gamma rays and fairly long half-life (30.1 years for ^{137}Cs and 5.27 years for ^{60}Co). However, the use of ^{137}Cs has been limited to small, self-contained dry storage irradiators, used primarily for the irradiation of blood. Currently, all industrial and commercial radiation processing facilities employ ^{60}Co as the gamma radiation source. Because of its short half-life, ^{60}Co is not naturally found and has to be produced for irradiation purposes. ^{60}Co decays into a stable non-radioactive nickel isotope ($^{60}_{28}Ni$) while emitting one negative beta particle of maximum energy 0.313 MeV with a half-life of 5.27 years. The Nickel-60 produced is in an excited state and immediately emits two photons of energy 1.17 MeV and 1.33 MeV in succession and then it reaches a stable state. It is these two gamma ray photons which are used in ionizing radiation processes in the ^{60}Co irradiators [**3**].

The strength and the activity of the cobalt source decreases with the decay of every ^{60}Co atom such that it drops by half in 5.27 years or 12% every year [**3**].

Radiation absorbed dose (rad) is the unit of absorbed dose by a material under radiation. 1 rad = 0.01 J/kg of radiation energy. "Gray" (Gy) is the SI unit of absorbed dose and it is equivalent to 100 rad [**5**]. This is the unit which is of interest in this thesis.

2.2 Phenomenological Description of Ionizing Radiation Effects on MOS Devices

Ionizing radiation possesses enough energy to create electron-hole pairs in MOSFET oxide regions, noting that creation of an electron-hole pair in thermally grown oxide requires 17 eV of energy [**1**], [**6**].

The radiation damage in the SiO_2 layer consists of three components:

- The buildup of trapped charge in the oxide;
- An increase in the number of interface traps;
- An increase in the number of bulk oxide traps.

Electron-hole pairs are created within the SiO_2 layer by ionizing radiation or may be injected into the SiO_2 by internal photoemission from the contacts. These carriers can recombine within the oxide typically in picoseconds or transport through the oxide. Electrons are highly mobile in SiO_2 and are mostly swept out of the oxide without being trapped and collected by the positive electrode also in times on the order of picoseconds at room temperature for typical oxide thicknesses of ($t_{ox} < 100$ nm) and $E_{ox} > 10^5$ Vcm^{-1}. Holes on the other hand, have a very low effective mobility and transport through the oxide in a complex trap-hopping process. Some of the holes may be trapped within the oxide leading to a net positive charge. Other holes may move to the Silicon-SiO_2 interface where they capture carriers and create interface traps [7].

Other researchers such as [8] have explained the mechanism in terms of chemical bonding radiation-induced charge generation in SiO_2. The gamma photons interact with the electrons in SiO_2 molecules, releasing secondary electron-hole pairs i.e. photons break $Si - O$ and $Si - Si$ (oxygen vacancy) covalent bonds, which in turn create secondary electrons that are highly energetic and may recombine with the holes right on the spot or may escape the recombination. The maximum energy of a secondary electron is 1.33 MeV in the case of a ^{60}Co irradiation source. Electrons which escaped will leave the oxide, losing their energy through collisions with other secondary electrons or with

the bonded electrons in $Si-O$ and $Si-Si$ bonds releasing more secondary electrons. The following chemical bond equation illustrates this point [**8**]:

$$\equiv Si - Si \equiv \xrightarrow{e^-} \equiv Si^+ + Si^\circ \equiv +2e^- \qquad 2\text{-}1$$

where $\equiv Si$ indicates a silicon atom bonded to three "bridging" oxygen atoms, $Si^\circ \equiv$ is a silicon atom with three oxygen bonds and an extra electron i.e. a hole trap at an oxygen vacancy and the trivalent silicon, $\equiv Si^+$, means a positively charged silicon atom with three bonds with oxygen atoms.

Holes which are left behind as a result of the electron-hole pair generation do not stay in their place permanently but rather slowly travel in the direction of the applied electric field within the oxide toward one of the interfaces. Moreover, even in the case of zero gate voltage bias, the potential due to the work function difference between gate and the substrate is large enough to move the holes toward one of the interfaces (Gate-SiO_2 or Si-SiO_2 interfaces).

When holes reach the Si-SiO_2 interface, they can also break the strained oxygen vacancy bonds $\equiv Si - Si \equiv$ as below [**8**], [**9**],

$$\equiv Si - Si \equiv + h^+ \rightarrow \equiv Si^\circ + \equiv Si^+ \qquad 2\text{-}2$$

and also break the strained $\equiv Si - O - Si \equiv$, resulting in the creation of amphoteric nonbridging oxygen centers:

$$\equiv Si - O - Si \equiv + h^+ \rightarrow \equiv Si - \dot{O} + \equiv Si^+ \qquad 2\text{-}3$$

Figure 3 shows a brief summary of different processes affecting MOS devices under radiation [**7**].

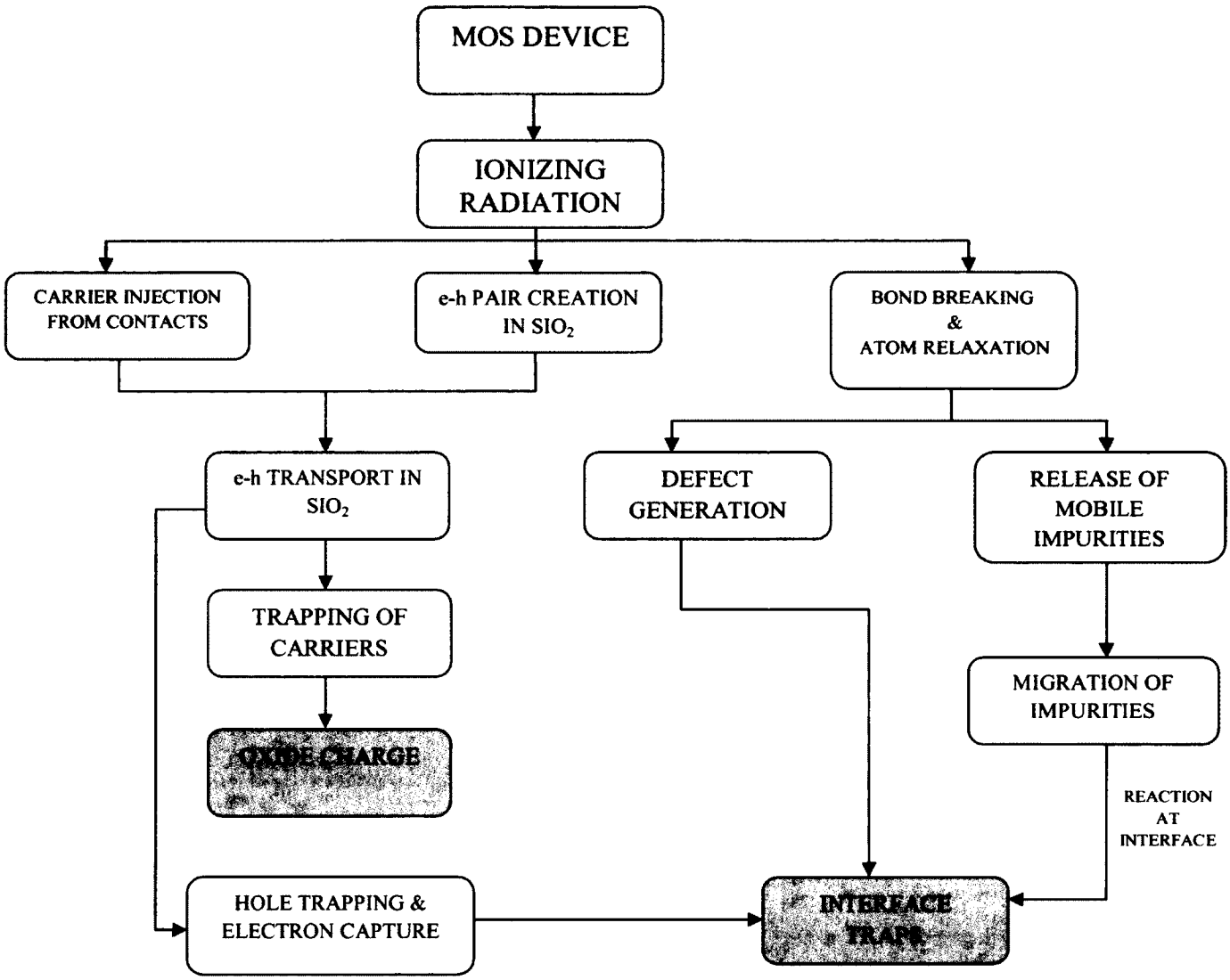

Figure 3- Schematic diagram illustrating the possible processes by which ionizing radiation can create changes within an MOS device [7]

The number of oxide and interface traps is also proportional to the total dose absorbed. Therefore, the effects of the creation of interface and oxide traps can be a means by which radiation can be measured in MOS devices.

The brief introduction of radiation effects on MOS devices which is presented above is explained more in depth in the next section.

2.3 SiO_2 Charge Characteristics

In this section, non-idealities of oxide are presented and the ones which are responsible for changing MOS characteristics under irradiation are named. This is important to understanding the change in threshold voltage that relates to dosimeter sensitivity. Then each subsection will describe the creation and effect of these non-idealities in detail.

Figure 4 illustrates the basic radiation induced effects in MOS structures in the case of positive gate bias. These steps have to do with generation, transport, and trapping of holes in the oxide. The fourth process indicated in the figure is that of the radiation induced buildup of interface traps which, depending on the silicon surface potential, can shift the threshold voltage either positive or negative.

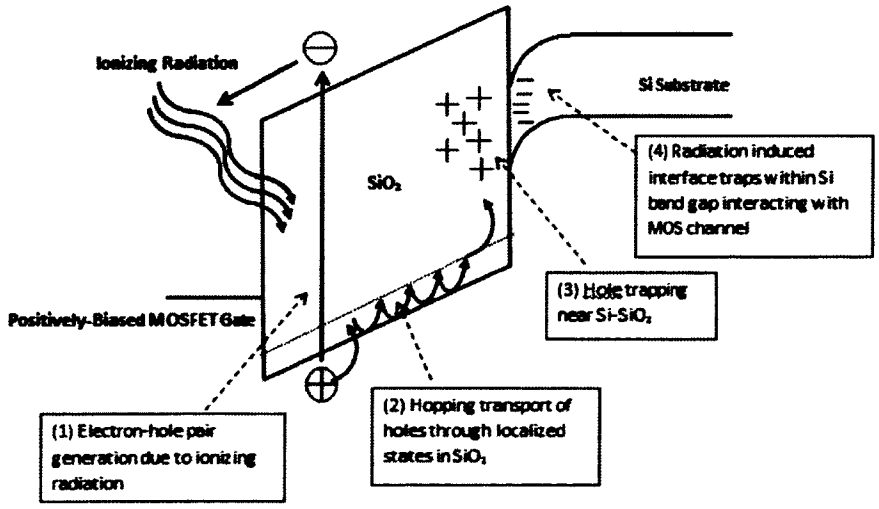

Figure 4- Representation of basic ionizing radiation effects in SiO2 under positive gate bias [10]

Figure 5 shows the approximate placement of the non-idealities of SiO_2. The four major categories of charges are mobile ionic charge, oxide-trapped charge, fixed oxide charge, and interface trapped charge. The mobile ionic charges are less important than other non-

idealities since commercial processes are done in a clean environment which stops most of this contamination from affecting the silicon oxide regions. There have been many debates and discussions [**8**] regarding further breakdown of these categories into more specific charge types which will be briefly discussed in the later sections.

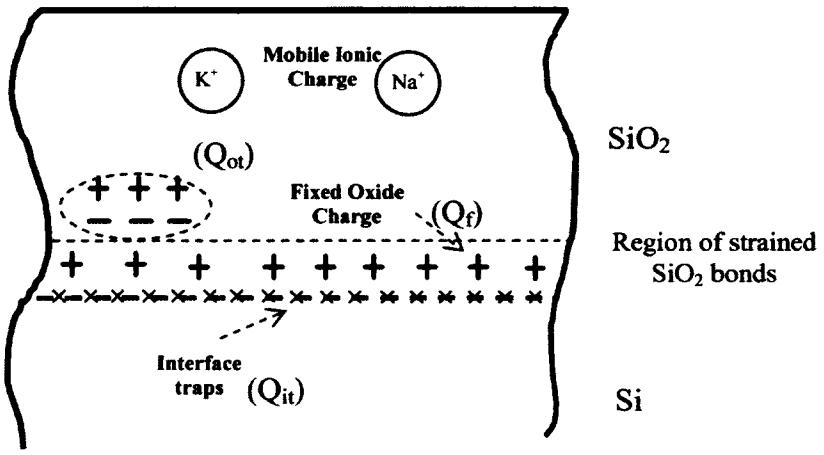

Figure 5- Terminology and physical placement of charges associated with thermally oxidized silicon [11]

2.3.1 Interface Oxide Traps Q_{it}

Ristic [**8**], Fleetwood [**12**], and others have studied the interface-trapped charge Q_{it} (shown in Figure 5), historically called the interface state, fast state, or surface state, and have shown that Q_{it} exists within the forbidden gap due to the interruption of the periodic lattice structure, such as in radiation exposure, at the surface of a crystal.

2.3.1.1 Interface Trap Creation

As it is suggested by [**7**], hole trapping in SiO_2 is an "intrinsic" property of Si-O bond. Also, straining of the Si-O bonds in the SiO_2 structure would easily break these bonds by ionizing radiation which creates the following chemical reaction:

$$\equiv Si - O - Si \equiv \xrightarrow{Irradiation} \equiv Si - \dot{O} + Si^{+} \equiv \qquad 2\text{-}4$$

where $\equiv Si - \dot{O}$ indicated a non-bridging oxygen defect. It was found that the transition from Si to essentially stoichiometric SiO_2 happens in only one atomic layer, hence a sharp transition. However, the first $1 - 4$ nm of oxide thickness is a region of strained SiO_2 bonds where the density of $Si - O - Si$ bonds is larger with a bonding angle of 120^o as opposed to the bulk oxide normal angle of 144^o [**13**]. In general, ionizing radiation such as □-ray causes the generation of fixed trivalent silicon – otherwise called E' center – and a mobile non-bridging oxygen defect that migrates to the Si-SiO_2 interface [**13**]. It is determined that the Si-SiO_2 interface is structurally prone to radiation damage specially the creation of trivalent silicon defects. The said researchers have shown that the only radiation-generated defects in silicon oxide are E' centers. The following points gathered by [**13**], [**7**] and [**8**] indicate that E' centers are indeed holes created by ionizing radiation:

- A strained defect-containing or defect-prone region exists in SiO_2 near the silicon interface;
- E' centers are created in SiO_2 under irradiation;
- The centers are more concentrated near the Si-SiO_2 interface;
- The centers are annealable by an electron flux or at elevated temperature.

2.3.1.2 Interface Trap Types

As is explained in [**8**], the defects at the Si-SiO_2 interface, which are also known as fast switching traps (FST), are classified as part of a more general category, the switching traps (ST) or the interface states. A defect or trap that captures a carrier from the MOS device channel or in other words, exchanges charge with channel, represents the ST [**8**]. ST could be in the oxide, close to the oxide/substrate interface, known as slow switching traps (SST), or exactly at the interface between oxide and substrate (FST).

How quickly or how often the switching trap captures a carrier or releases it depends on the distance to the interface [**12**]. This carrier capturing phenomenon decreases the carrier mobility in the channel, which decreases the current which in turn decreases the slope of the subthreshold characteristics. The change in effective mobility due to a radiation-induced increase in interface traps, δN_{it}, is parameterized as follows [**14**]:

$$\mu = \frac{\mu_o}{1 + \alpha \delta N_{it}} \qquad 2\text{-}5$$

where μ_o is the mobility before irradiation, α, $(8 \pm 2) \times 10^{-13}$ cm^2, is the adjustment factor which varies from technology to technology. It is observed that the mobility decreases with increasing the interface trap.

2.3.2 Oxide Bulk Traps Q_{ot} (Fixed Traps)

As has been explained in the past sub-sections, traps created within the oxide can be categorized into interface traps or bulk traps (Figure 5). The bulk traps however, are considered an important factor only in thick gate oxide MOS devices, such as >20 nm oxides as reported in [7]. Therefore, their effect in ultrathin gate oxides (3.15 nm) which this thesis work deals with, is negligible comparing to the effect of interface traps.

In general, the oxide traps (positive traps due to ionizing radiation) cause a parallel shift in the V_G vs. I_D curve in MOS devices since the positive traps create an electric field in the MOS channel which depending on the type of carriers in the MOS device (holes in pMOS and electrons in nMOS) causes the carriers to be repelled from or get attracted to the channel which in turn makes the pMOS harder to turn on, or nMOS easier to turn on respectively. Figure 6 illustrates the effect of radiation-induced interface and bulk oxide traps on V_G vs. I_D curves of an nMOS. For the pMOS case, both the interface and bulk

oxide traps cause the threshold voltage to change in the same direction (pMOS harder to turn on), hence creating a more significant response to radiation.

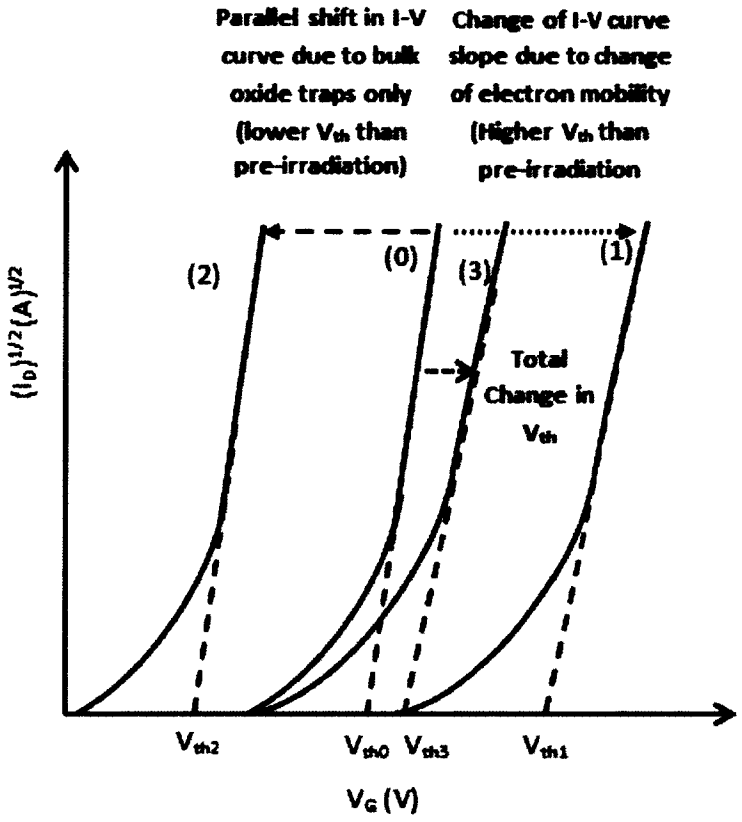

Figure 6- Transfer characteristics of nMOS transistor [8]:
Curve (0): the device before irradiation;
Curve (1): the nMOS with only the interface trap generation after irradiation;
Curve (2): the device characteristics only affected by bulk oxide traps;
Curve (3): the two effects combined

2.3.3 Shallow Trench Isolation Traps

Radiation-induced electron-hole pairs and creation of traps not only take place in the gate oxide but also in the shallow trench isolation (STI) separating 2 or more transistors in the substrate [15], [16]. It needs to be explained that shallow trench isolation in modern CMOS processes such as 0.13 μm IBM process is equivalent to the

field oxide in older CMOS processes. They differ mainly in thickness (the STI is thinner than the field oxide) and in the elimination of unwanted field oxide current leakage due to its shape. STI will be used instead of the field oxide where 0.13 μm technology is being discussed.

In general, the basic processes which contribute to the irradiation effects in gate oxides also apply to STI. However, there are factors which may cause major differences in the response of the gate oxide and STI to irradiation. Some are listed below:

- thickness difference with respect to gate oxide (STI thickness in 0.13 μm technology is 350 nm);
- employing different processes in making the STI than that used in gate oxide, such as CVD (chemical vapor deposition), inclusion of chemicals in the STI, dry or wet oxidation, as-grown or etch-back;
- structure difference, such as using multilayer oxides in gate oxide process as opposed to the STI.

The major effect of the STI on radiation sensitivity of a MOS device is the "square dependency" of ΔVot (voltage change in oxide) to oxide thickness under irradiation. On the other hand, there are offsetting factors which minimize the increase in charge generation and trap creation in STI; mainly, the decrease in the electric field present in STI. This factor causes a larger recombination process (lower charge yield) and longer charge travel to either of the interfaces, resulting in lower sensitivity. However, if a positive bias is applied to the RADFET gate, in the case of non-floating-gate MOSFET

dosimeters, the sensitivity increases significantly as opposed to no-bias scenario [17], [18].

2.4 High-Dose Effect

It is ideal to expect a MOSFET dosimeter to act linearly with dose absorbed, but at high dosages which is a relative measure and is determined by the fabrication process, silicon orientation, and radiation environment, the response of the MOSFET is "sub-linear" [7]. This saturation of ΔV_{th} with dose is a general feature in MOS dosimeters. It is believed that two processes cause this saturation, mainly the buildup of radiation-generated interface traps and more importantly a reduced rate of buildup of oxide-trapped charge with radiation.

As holes pile up in oxide traps during irradiation, the space charge alters the oxide electric field. If a positive bias is applied to the gate during irradiation, the accumulation of positive charge in the oxide results in an increase in the electric field between the positive charge and silicon substrate, but also reduces the electric field between the charge generated and the gate. This in turn decreases the yield (increasing the recombination of generated charge), leading to a sub-linear (less sensitive) response. Figure 7 illustrates the physical phenomena happening during irradiation in different dose ranges.

In Figure 7(a) of the illustration which corresponds to lower dose exposure which in turn corresponds to low space charge density, the electric field in the oxide is only slightly influenced by the trapped-hole buildup, and the holes are uniformly distributed throughout the oxide, and ΔV_{ot} (change in oxide potential) varies linearly with dose.

Once a critical point is reached where the density of space charge is given by the formula in Figure 7(b), and that $\Delta V_{ot} = -V_g$ (for positive gate bias), the generated charge (traps) causes the electric field at the gate to approach zero. In this point, the generated electron-hole pairs start to recombine more in the lower field region in oxide because there is no electric field to separate the generated charges. In this case the sensitivity starts to go down, hence a sub-linear change in ΔV_{ot} with irradiation. As more space charge accumulates in the oxide with increased dosage – such as in Figure 7(c) – the low-field area in oxide starts to expand towards the silicon and the trapped-hole distribution becomes more restricted to the area near the Si/SiO_2 interface. In this case, the response saturates and sensitivity is lost beyond this point.

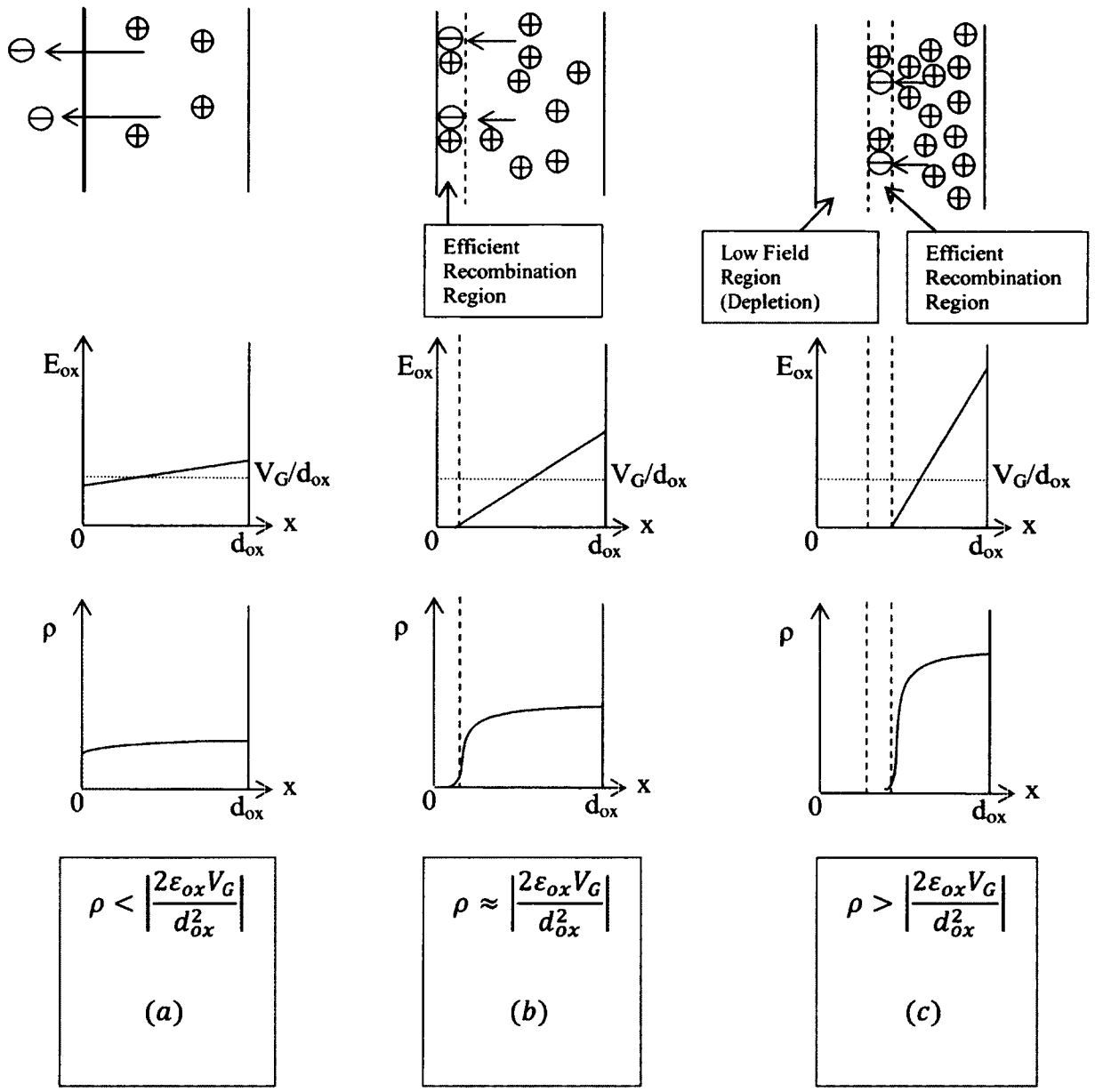

Figure 7- Illustration of charge buildup in a MOS device in a) low dose exposure, b) critical dose: zero-field at the left electrode with onset of efficient electron/trapped-hole recombination, c) high dose: expanded zero-field region with larger recombination region within oxide bulk [7]

ρ [q/cm^3] is oxide charge volume density, ε_{ox} is the SiO_2 permittivity [F/cm], V_G [V] is the MOSFET gate voltage, E_{ox} [V/cm] is the electric field within the oxide region, and d_{ox} [cm^2] is the oxide thickness. The high dose effect accounts for the major limitation of MOS radiation sensors and it is also evident that gate bias under irradiation

plays an important role in sensor's response to irradiation. The higher the gate bias, the wider the range of the MOS sensor's response before it gets saturated.

2.5 Fading: a Post-Irradiation Effect on MOS Dosimeters

After an irradiation, the MOS characteristics will not be stable with time. This effect is undesirable since ideally one would like to be able to access the irradiation result in the form of threshold voltage shift over a long period of time. The changes in threshold voltage after irradiation have been shown to be the result of the effects of changes in the radiation-induced interface traps and trapped oxide charge [**19**], [**20**]. In thin oxides such as that focused on in this research, the bulk oxide traps – though few in quantity in comparison to other effects – are annealed out over time at room temperature by tunneling electrons from the channel. The duration of this annealing effect depends on temperature and on the bias applied during irradiation. The lower the temperature, the lower the rate of post-irradiation threshold voltage changes; and also the lower the applied bias to the gate during irradiation, the slower the changes to the threshold voltage changes after irradiation [**21**], [**22**].

From the above explanations, fading can be formulated as below [**8**]:

$$f = \frac{V_{th}(0) - V_{th}(t)}{V_{th}(0) - V_{th0}} \qquad 2\text{-}6$$

Where V_{th0} is the pre-irradiation threshold voltage, $V_{Th}(0)$ is the threshold voltage immediately after radiation, $V_{th}(t)$ is the threshold voltage after irradiation. $(V_{th}(0) - V_{th0})$ can be rewritten as $\Delta V_{th}(0)$ which means the threshold shift immediately after irradiation.

2.6 MOSFET Dosimeter

As has been discussed, MOSFETs offer a promising future in integrated circuit dosimetry. Before we can discuss MOSFETs as dosimeters, it is important to realize the characteristic which make the MOS devices suitable for dosimetry.

An MOSFET device has four terminals: the Drain, the Source, the Gate, and the Body (Substrate). There are two types of MOS devices, n-type and p-type, where in the n-type MOSFET the dominant carriers are electrons, and in the p-type the holes are dominant. This thesis does not intend to explain every detail regarding the structure of an MOSFET device but rather focuses on the specifications that are directly or indirectly related to dosimetry application.

2.6.1 MOSFET Threshold Voltage

As has been explained briefly in the last section, the ionizing radiation causes a shift in the threshold voltage of the MOS devices. Before getting into details of the effects of radiation exposure on the threshold voltage, the threshold voltage of an MOS device is formulated.

In an MOS device, the long channel saturation and linear region current (I_{DS}) approximations are given as below:

(In saturation region) $$I_{DS} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{GS} - |V_{thp}|)^2 \qquad 2\text{-}7$$

(In linear region) $$I_{DS} = \mu_p C_{ox}\frac{W}{L}\left((V_{GS} - |V_{thp}|)\,V_{DS} - \frac{V_{DS}^2}{2}\right) \qquad 2\text{-}8$$

where C_{ox} is the gate-oxide capacitance per unit area, μ_p is the hole mobility, V_{DS} is the drain-to-source voltage, V_{GS} is the gate-to-source voltage, V_{thp} is the pMOS threshold voltage, and W and L are the width and length of the transistor respectively.

Of all the parameters in the above formulae, the threshold voltage V_{thp} and carrier mobility change with ionizing radiation exposure, hence a change in the channel current I_{DS}. Hence, the following formulae can be written which show the changes in the MOS characteristics with respect to irradiation [8].

$$\Delta V_{th} = A \cdot D^n \qquad 2\text{-}9$$

where ΔV_{th} is the shift in threshold voltage caused by radiation, A is a constant; D is the absorbed dose which represents the average energy absorbed per unit mass of irradiated substance at a point when the photon flux is constant.

$$D = \frac{E_{ab}}{m} \left[\frac{J}{Kg}\right] \qquad 2\text{-}10$$

where E_{ab} is the average absorbed energy in the matter and m is the mass of the matter and n is the degree of linearity of the MOS sensor response with radiation, which is desirable to be 1. For n=1, A represents the sensitivity, S, of the pMOS dosimeter,

$$S = \frac{\Delta V_{th}}{D} \left[\frac{V}{Gy}\right] \qquad 2\text{-}11$$

The two types of MOSFETs (n-channel and p-channel) can be considered for dosimetry but usually the p-channel device is favorable because of advantages it has over the n-channel devices.

In n-channel devices, after an ionizing radiation exposure, the interface-trap density N_{it} may increase by a factor of 100 times over the pre-irradiation values to levels in the low 10^{12} cm^{-2} range [7]. For dose rates of 1-10 Gy/s, N_{it} may be compensated by the positive oxide-trapped holes N_{ot} in the gate and field oxide regions of n-channel transistors, causing the device to appear to be radiation-hardened meaning the n-channel devices are less sensitive to ionizing irradiation [8]. The following formulae illustrate the effects of N_{it} and N_{ot} on threshold voltage and channel current [14]:

$$I_D = \pm \frac{1}{1 + \alpha \delta N_{it}} \left[\frac{\mu_o W C_{ox}}{L} \left(V_G - V_{tho} - \frac{V_D}{2} \right) V_D + \frac{\mu_o W}{L} V_D q(\delta N_{ot} \mp \delta N_{it}) \right] \quad 2\text{-}12$$

Equation 2-12 shows the current in small drain bias approximation. V_{tho} is the threshold voltage before irradiation, δN_{it} (cm^{-2}) is the change in the number of interface states per area of oxide, and δN_{ot} (cm^{-2}) is the change in the number of bulk oxide traps per area of oxide due to irradiation. It is important to notice that the upper ± sign is used for nMOS transistors, and the lower ones for pMOS transistors. For nMOS devices, the term (δN_{ot} – δN_{it}) minimizes the effect of irradiation to a point where if both the components were almost equal, it would be neglected, but in pMOS dosimeters, this term increases, hence an increase in sensitivity. This is one of the reasons why pMOS dosimeters are preferred over the nMOS ones (illustrated in Equation 2-12).

The other reason is the fact that pMOS transistors have a lower 1/f noise factor than nMOS transistors. However, lower 1/f noise is more important in dosimetry applications where higher sensitivity in measurement is required. In higher radiation

dosage applications, such as in this research, where there is a larger noise tolerance, 1/f noise consideration is a secondary factor.

The threshold voltage shift can be written as follows [**14**]:

$$\Delta V_{th} = -\frac{q\delta N_{ot}}{C_{ox}} \pm \left(\frac{\alpha I_D L}{\mu_o W C_{ox} V_D} + \frac{q}{C_{ox}}\right)\delta N_{it} \qquad 2\text{-}13$$

where the first term multiplied by δN_{it} takes mobility degradation into account, and the second term takes into account the reduction in mobile carriers in the channel. The first term of the equation accounts for the effect of oxide traps in threshold shift. The importance of using pMOS over nMOS is once again emphasized in this equation since the '+' sign reduces the effect of radiation on threshold shift in nMOS, but the '-' sign of the second term adds to the effect.

As the gate-oxide thickness reduces, the MOSFET becomes less sensitive to radiation [**23**] because of the reduction in N_{ot}, but N_{it} does not reduce as much compared to N_{ot} with gate thickness which means that buildup of radiation induced N_{it} is a major source of shift in threshold voltage [**24**]. In general, N_{ot} anneals out with time, but N_{it} is retained and becomes the dominant cause for sensitivity [**24**].

Chapter 3 Dosimeter Background, Previous Work and Proposed System Concept

This chapter reviews previously developed dosimeter devices, focusing first on non-MOSFET technologies and then on the floating-gate MOSFETS pioneered at Carleton University. Finally, it describes the proposed wireless dosimeter system concept, setting the stage for the design approaches adopted in this thesis.

3.1 Dosimetry Approaches

Each of the dosimeters mentioned in this section is utilized in a different field of science and because of their characteristics and properties, they adequately fit a specific application. Almost all the focus of researchers on dosimeters have been dedicated to making devices that are more and more sensitive to radiation with a broader range of sensitivity in different environments.

There are two dosimetric measurement techniques:

1. Total dose measurement, as in thermo-luminescent dosimeter (TLD) [**25**], film badges [**26**], and rad tags [**27**] which will be explained in more detail later.
2. Dose rate measurement, as in silicon diode detectors.

The measurement of both of the above-mentioned quantities is desired in radiation environments.

In the total dose measurement technique, the complete dosage can be read after exposure, such as in the case where the dosimeter is worn by a technician who is exposed

to radiation, or where materials are subjected to radiation such as in the blood irradiation application or in surgical device sterilization.

In dose rate measurements, the radiation dose as a function of time is measured, and if it is higher than the safe rating, then an indication will alarm the user such as in the case of survey meters, pocket dosimeters, and audible alarm rate meters [**28**]. Diode dosimeters measure dose rates and through circuit design, the dose rate can be integrated to give the total dosage but it does not retain this information after the irradiation.

Each of the mentioned dosimeters is introduced briefly in the following sub-sections.

3.1.1 Thermo-Luminescent Dosimeters (TLD)

A TLD is a phosphor such as lithium fluoride in a crystal structure. When it is exposed to ionizing radiation, the radiation deposits all or part of the incident energy in that material. Some of the atoms in the material that absorb the energy become ionized, creating free electrons and holes. Imperfections in the lattice structure act as trap sites for free electrons. Heating the crystal causes the crystal lattice structure to vibrate, releasing the trapped electrons. The released electrons return to their lowest energy level, releasing the captured energy as light. The number of photons counted is proportional to the quantity of incident radiation [**25**]. TLD is used in almost all radiation working environments and is made in a variety of sizes and shapes. For example, a TLD ring can be worn by a person, and after the irradiation period, it is sent back to the supporting company for readout of the amount of radiation exposure. Another variation of the TLD can be worn on the wrist, but the principle of operation and readout is the same [**29**].

TLD users include: first responders to disasters, dental and veterinary clinics, National Defense, research, industry.

Some of the advantages of using TLD's are: small size which makes point dose measurements possible, applicable to X- , gamma- and beta-ray radiation, and in some models, neutron radiation sensitive; reasonably priced compared to other dosimeter options; durable against different environmental factors [**30**].

Some of the disadvantages are: signal erasure during readout, no instant readout, time consuming readout and calibration [**30**].

3.1.2 Film Dosimeters

The film dosimeter is a piece of radiation sensitive material. The film changes color under different amounts of radiation. Also a set of filters are incorporated with the film which helps in the process of calculating the absorbed dosage [**26**].

Some of the advantages are: 2-D spatial resolution, very thin, which does not perturb the beam; measures exposure to gamma, X-ray and beta radiation; certain models can also be used for neutron radiation; provides a permanent record - the film itself - of radiation exposure; reasonably priced, and long-term proven technology.

Some of the disadvantages are: a need for darkroom and processing facilities, difficulty to control variation between films and batches in process, one-time use, human error involved in the reading procedure [**30**].

3.1.3 RAD TAG Dosimeters

The reading procedure in rad tag involves color change on the exposed film, whereas that of film dosimeters involves film development much like the old camera films made by Kodak [31]. Figure 8 shows a rad tag indicator with color coding scale.

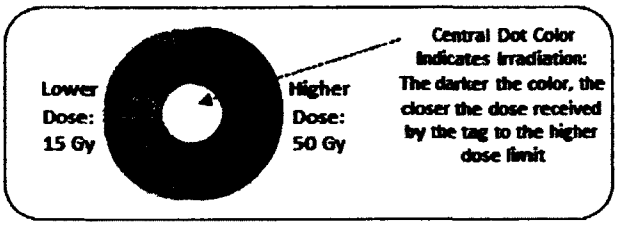

Figure 8- A rad tag radiation indicator unit designed for low dosage applications [32]

Rad tag dosimeters are very limited in their operation. They are made to sense a limited range of radiation and via color change; the operator can empirically interpret the dosage. This type of dosimeter indicates a lower and upper limit on the tag and the white dot in the middle indicated a color close to either of the boundaries indicating whether you are close to the lower limit or to the upper limit. Therefore, any dosage information between the two limits is subject to human judgement which introduces errors in interpretation. Also this type of dosimeter does not indicate the time rate of radiation but just the total dose information. Hence any undesirable change in the source of irradiation which affects the time rate of radiation will not be monitored [32].

3.1.4 Diode Dosimeters

The incident ionizing radiation generates electron-hole pairs throughout the diode. The minority carriers (electrons on the p side and holes on the n side) diffuse toward the pn junction. Those carriers within approximately one diffusion length from the junction edge are able to reach it before recombination. They are then swept across the junction by

the built-in potential and measured by an electrometer. The current observed is the radiation-induced photocurrent [33].

Diode dosimeters are used in applications that require real-time personnel and area monitoring, military and medical applications.

Some of the advantages are: small size, high sensitivity, instant readout, no external bias voltage, simple instrumentation.

Some of the disadvantages are: requirement of power connection cables, variability of calibration with temperature, need for special care to ensure constancy of response [30].

3.1.5 Direct Ion Storage Dosimeter

A dosimeter device which is closely related to MOSFET dosimeters is called DIS (Direct Ion Storage) dosimeter. Its operation can be understood by considering a MOS memory cell.

In a non-volatile memory cell, information is stored as an electronic charge on the floating gate of a MOSFET transistor. The early memory designs only stored digital information, meaning either high or low amount of charge on the floating gate to represent binary bits 0 and 1. In 1991, a new type of memory cell was designed which could store analog information, meaning any value of charge could be transferred onto the gate, introducing analog Electronically Erasable Programmable Read-Only Memory (EEPROMs). The radiation sensitivity of a normal solid-state memory cell is inherently too low for use as detectors for ionizing radiation in radiation protection applications. The main reason for this is that the memories are deliberately designed to be insensitive to

ionizing radiation so that they can retain charge on the floating gate and be used in space and military environments without causing single event upsets [34], [35]. However, in the design of the DIS, an opening is created in the oxide layer surrounding the floating gate so that it is exposed to the air around it. Then, via charge tunneling, the floating gate is charged. A metallic enclosure is used to create the ionization chamber. The metal casing can be coated with different materials to detect different particles. Once a radiation incident occurs, the high-energy particles would ionize the air in the system, which consequently changes the amount of charge on the floating gate, hence, changing the channel current in the MOSFET [36].

An EEPROM memory cell is shown in Figure 9, which could also be utilized as a DIS. Figure 10 , and Figure 11 show the changes made to the EEPROM in order to make it suitable for ion chamber dosimetry and the concept of operation of the device as a dosimeter, respectively.

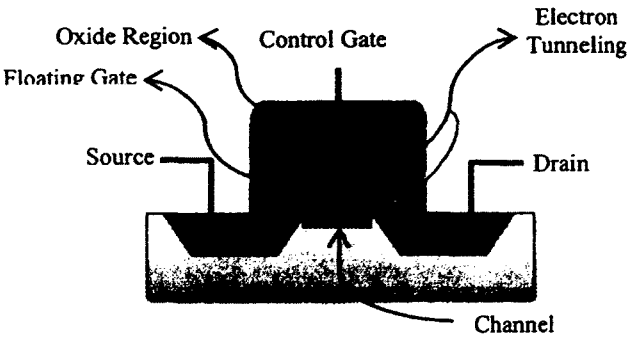

Figure 9- An EEPROM memory cell before being modified for use as a DIS [36]

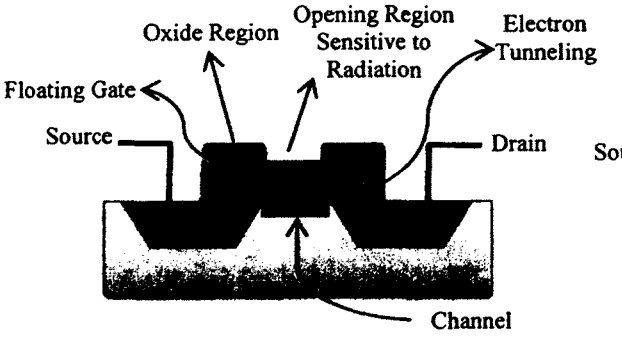

Figure 10- A DIS memory cell with an opening in the oxide to expose the floating gate [36]

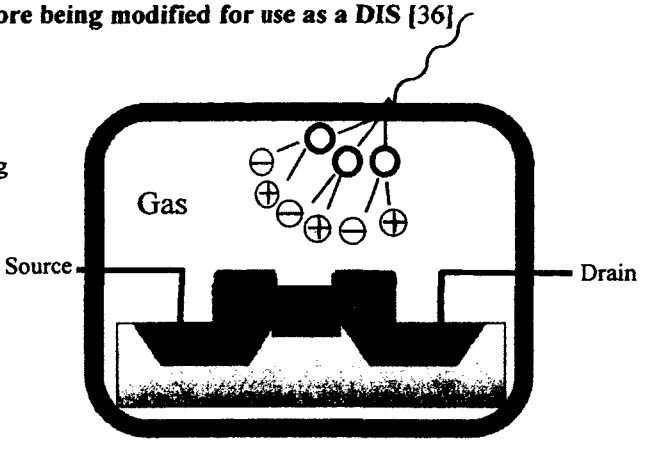

Figure 11- The operation concept for DIS memory cell [36]

MIRION Technology™ [37] is a company that commercializes the DIS dosimeters (memory cells) and also offers the DIS Reader, which is necessary to read the dosimeter. Hence a real-time readout is not made possible in this technology which renders this product unsuitable in environments where the readout in real-time is a necessity. Moreover, the DIS dosimeter measures 41 x 44 x 12 mm in size (aimed at lower dosage and higher sensitivity applications), which is considered large for many medical applications. An image of the DIS product and the reader device is provided in [38].

The DIS dosimeter is used in personnel and area monitoring applications. Some of the advantages are: accurate and precise reading, recommended for beam calibration, instant readout. DIS is highly sensitive to radiation. Some of the disadvantages are: requirement for high voltage supply and an on-site reader, and a large size, which makes it unsuitable for this research [30].

To summarize, neither the diode nor the DIS dosimeter devices report dose rate and store the accumulated dose as a function of time simultaneously. As for the film badges and rad tags, the human error involved in the reading procedure becomes an important factor when measuring radiation dose because of crude measurement scales and a large tolerance range.

3.2 Different MOSFET Dosimeter Approaches

With the advancement of IC technology and the expansion of its use on different scientific fronts such as space applications, satellite communication, interplanetary exploration, and military applications, issues began to arise from the resulting radiation environments. The IC capabilities fell short of expectations because of degradations in performance due to latch-up (triggering of parasitic semiconductor-controlled rectifier present in Si CMOS circuits) and gate leakage initiated by radiation. For decades, scientists have been exploring different solutions to overcome such problems in ICs. As a result, radiation hardening techniques in IC technology have been introduced and also dosimetry has been developed as a means of measuring the amount of radiation the ICs have been exposed to. Hence, IC dosimetry in its infancy was realized as a side effect of the radiation on ICs.

In this section, different Si MOSFET IC dosimeters are introduced. They are categorized into:

1. Thick oxide, and thin oxide devices;
2. Double-poly gate devices;
3. Single-poly gate devices:
    a. Floating-gate devices
    b. Non-floating-gate devices

Generally, the older IC technologies inherently have thicker gate oxides and with the advancement of fabrication techniques, the gate oxide thickness has been significantly reduced. Hence, the devices studied can also be categorized into older and recent devices. The double polysilicon gate devices are usually the ones fabricated for memory cell design purposes.

The use of FETs as dosimeters was pioneered by Holmes-Siedle [**39**]. For the first time in the field of electronics, a dosimeter device was created in 1970 utilising threshold voltage shift as a result of radiation exposure in MOSFETs. Also, the name "Space Charge Dosimetry" was coined for this principle. The MOS transistor used in [**39**] is a pMOS with the sensitivity of 1 mV/Rad and a 100-ft cable was used to route the dosimeter to an amplifier as a readout device.

The main advantages of the method with respect to other relative methods of measuring integrated dose such as TLDs, are:

1. The great compactness (the sensor element can be as small as 10^{-4} cm^{-3});

2. The possibility of remote, continuous and non-destructive electrical readout and the wide range of materials in which the charge build-up may be produced and possibly enhanced by doping or defect introduction;
3. The enhancement of linearity and dynamic range compared to other dosimetry techniques;
4. The increase of precision, i.e. only 1 or 2% variation in measurements whereas for the TLDs there is at least 10% variation in reading.

The limitations of MOSFET dosimetry are:

1. The basic stability of the MOS transistor and the stability of the other circuit components under radiation exposure;
2. The sensitivity of the transistor to temperature changes, which is possible to compensate;
3. Sensitivity to the voltage supply;

The paper also predicts that with the increase in the complexity of MOSFETs, the sensitivity to radiation also increases and the dosimeters can be used as personnel radiation monitoring which requires mRad resolution.

The first attempt to fabricate floating-gate MOSFETs in a standard CMOS technology, where charging and discharging of the floating gate is done by means of tunneling, is presented in [**40**]. The device is fabricated in a standard 2 μm p-well, double-polysilicon technology from ORBIT-Semiconductor. The MOSFETs are programmable (charging and discharging) by Fowler-Nordheim tunneling at about 12 V, which is delivered to the device in pulses of different durations, where it is

experimentally found that the threshold voltage could be shifted from -4 V to +4 V. The design consists of W/L = 3 μm / 2 μm, a gate oxide thickness of 75 nm and a control gate created in the second layer of poly-silicon. The layout is shown in Figure 12. The paper successfully illustrates the possibility of changing the threshold voltage by applied voltage to the control gate which is designed using the second poly layer.

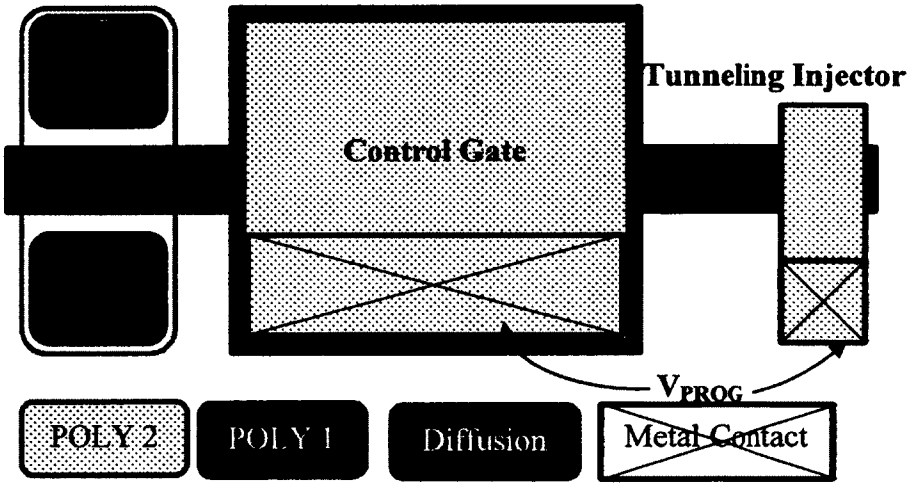

Figure 12- Schematic drawing of the device with the connections for programming voltage V_{prog} and operating voltage V_{gs} [40]

The design introduced in **[41]** is a custom-fabricated wireless dosimeter which includes a gate-connected MOSFET sensor with the active region of 0.3 μm x 50 μm enclosed in a 20 mm x 2.1 mm glass tube for in vivo measurements, meaning it is implanted in the patient's body. It has a range of up to 80 Gy above which its response saturates. The device has a sensitivity of 0.45 mV/cGy, which is very low and it is not capable of real-time radiation monitoring. The wireless transmission range is very limited (12 cm) and has a fading time of 20 minutes, meaning it starts introducing measurement error of about 2% in its dosage information. The MOSFET sensor is sitting separate from the signal processing circuitry, hence it is not a "System on Chip" solution, and besides

the cost of the tube, the cost of the packaging needs to be also included which makes it an expensive device. An important characteristic of this device is remote RF (Radio Frequency) powering of the entire system which makes reading the dose possible without the use of a battery. However, this requires a large external powering apparatus. It also includes a temperature sensor which can also be wirelessly read.

In [**42**] gate-connected stacked up p-MOSFETs with 1.6-μm thick gate oxide are employed as dosimeters and tested under Co^{60} source. The paper reports that the sensitivity of the device consisting of two identical MOSFETs was not improved enough compared to that of one MOSFET. On the other hand, the system shows better linearity, than that with one MOSFET. The MOSFETs are fabricated in a custom process at LAAS-CNRS Laboratory in Toulouse, France.

A miniature MOSFET probe is presented in [**43**] which reports on the design of a wired gate-connected dosimeter. The MOSFET is obtained from Dr.A.Holmes-Siedle, REM Oxford, England. The wafer is cut in 0.55 mm x 1.10 mm dimensions each including a single MOSFET. The MOSFET is wired for readout. A 5V bias is applied to the gate, which under gamma radiation is capable of sensing 4 mV/cGy. This MOSFET probe has a limited application of only 10 Gy and the wiring used for readout makes it unsuitable for most medical applications where wires can disrupt the radiation pattern for example in cancer radiotherapy.

Some papers such as [**44**] reported using discrete component MOSFETs in their experiments. These devices usually do not contain information with regards to the gate oxide thickness, but by their high sensitivity to radiation, it can be concluded that they

have thick oxides. However, the purpose of this research is to utilise integrated MOSFETs so that monolithic dosimeters would be realizable.

pMOS dosimeters have extensively been studied in [8], [45], [46], [47], [48], [49] and [50], mainly published by the Applied Physics Laboratory (APL) which is part of the Electronics Engineering Faculty in University of Nis in Serbia. These publications range from the study of the dependence of the MOSFET dosimeter sensitivity to the physical parameters of MOSFETs such as gate oxide thickness, to biasing conditions on the terminals during irradiation, to post-irradiation testing procedure, to annealed or non-annealed test samples, to radiation dosage. However in none of these publications has a discussion with regards to the integrated very thin oxide floating-gate MOSFETs been presented.

3.3 Recent Works on Floating-gate Dosimeters at Carleton University

There are a few very important publications related to this research within the literature available on this topic. The cornerstone of this novel design has been laid at the Department of Electronics at Carleton University by Dr. Garry Tarr and his research team. In the first of many publications on the subject [51], a novel MOSFET-based dosimeter that uses a floating polysilicon gate was reported. As in previous MOSFET dosimeters, absorbed dose is inferred from changes in threshold voltage. The prototypes have been fabricated in 5 μm nMOS integrated-circuit technology, and can achieve sensitivities up to 280 mV Gy^{-1} for a ^{60}Co gamma source. This design uses 2 polysilicon layers of which the closest one to the body is floating and the one on top of it is a control gate which is biased positively during the irradiation. The gate oxide is 50 nm thick and the inter-polysilicon oxide is 140 nm thick. The electrons generated within the field oxide

during irradiation would get attracted to and trapped in the floating gate; hence, threshold voltage change. The significance of this MOSFET design in comparison to the earlier versions presented by other researchers is the use of a "gate extension" which is a stretch of polysilicon gate on top of field oxide which increases the sensitivity of the MOSFET to radiation significantly. Figure 13 illustrates this design.

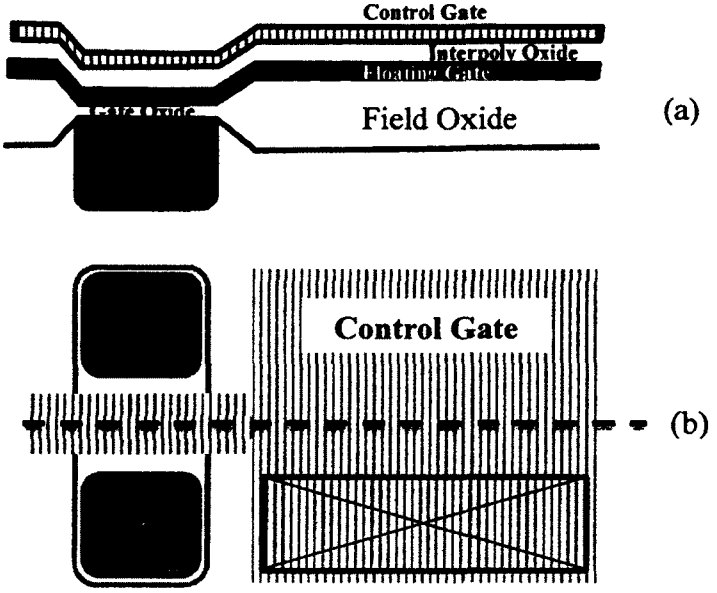

Figure 13- Cross section (a) and plan view (b) of floating-gate dosimeter with gate extension over field oxide [51]

In the next revision of the design, [52] presents new enhancements to the design mentioned above. The revised design is presented in Figure 14.

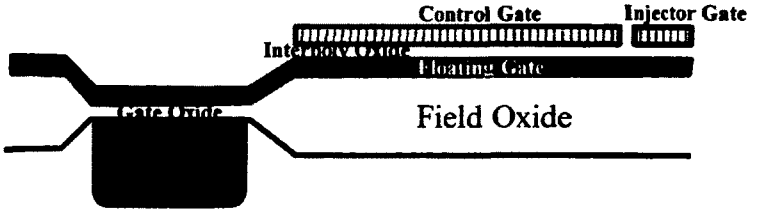

Figure 14- Cross-section of floating-gate MOSFET dosimeter along device width. [52]

The first improvement is that the design is implemented in the 1.5-μm commercial CMOS technology by Mitel Semiconductor which is an available, less expensive technology than the custom 5-μm process previously used.

The second improvement is the use of an injector gate in the second polysilicon layer which makes this device a zero-bias sensor which means that it does not require external biasing during irradiation. The control gate bias is used to set the desirable threshold voltage while maintaining a set value of current I_D at a drain-source voltage V_{DS} while the injector gate is used to inject charge on the floating gate to reach that set I_D current before irradiation. This would create an electric field between the charged floating-gate and the bulk of the MOSFET which during irradiation separates the generated electron-hole pair and discharges the floating-gate charge; hence a change in threshold voltage and current in the channel.

The third change in the design is the use of device pairs (shown in Figure 15) as opposed to using a single device under irradiation which improves the sensitivity of the response by eliminating temperature dependent threshold drift which could mistakenly be interpreted as an indication of radiation-caused discharge of the device **[53]**. In this method, one of the floating-gate MOSFETs is not charged and the other is charged to a desired negative or positive threshold voltage and the output is read as the difference in the threshold voltage change in the two. The sensitivity of this device pair is reported to be 70 $mVGy^{-1}$ up to a total dose of 200 Gy.

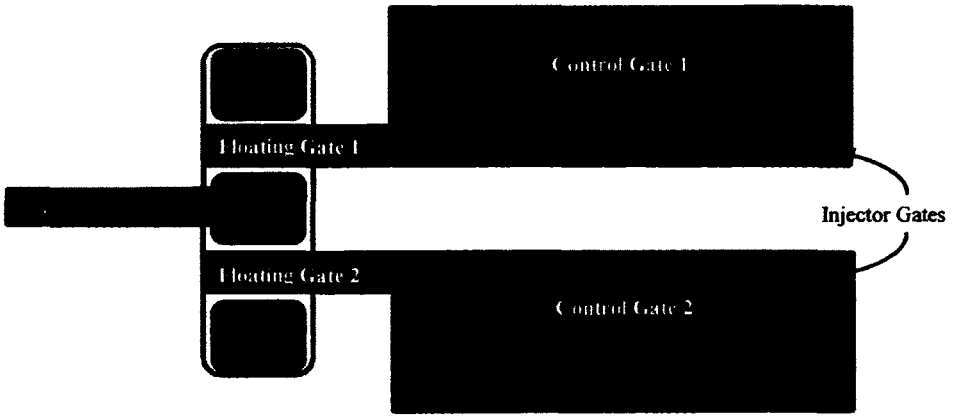

Figure 15- Plan view of matched pair of floating gate MOSFET sensors used to construct dosimeter. (Gate extensions over field oxide not to scale) [53]

On further refining the previous work, [1] presents the following new techniques to improve the response of the dosimeters:

1. The removal of the control gate, which increases the sensitivity of the dosimeters by an order of magnitude. This way, the only means to pre-charge the floating-gates is to use the small injector gate to charge the floating-gate through application of ~ -20 V such as before, but the difference is that without the control-gate, the only means to realize whether the floating-gate has been charged or not is through monitoring I_{DS} while the other terminals are grounded except the drain which is biased at V_{DS} = -0.1 V.
2. The use of a second shield ring consisting of the first polysilicon layer and the first metal layer to suppress noise on the substrate which had previously caused erratic changes on the floating-gate potential.
3. The use of the second metal layer shield grounded to the substrate potential covering the entire active region of the MOSFET and the gate extension as shown in Figure 16 to protect them from electrostatic fields.

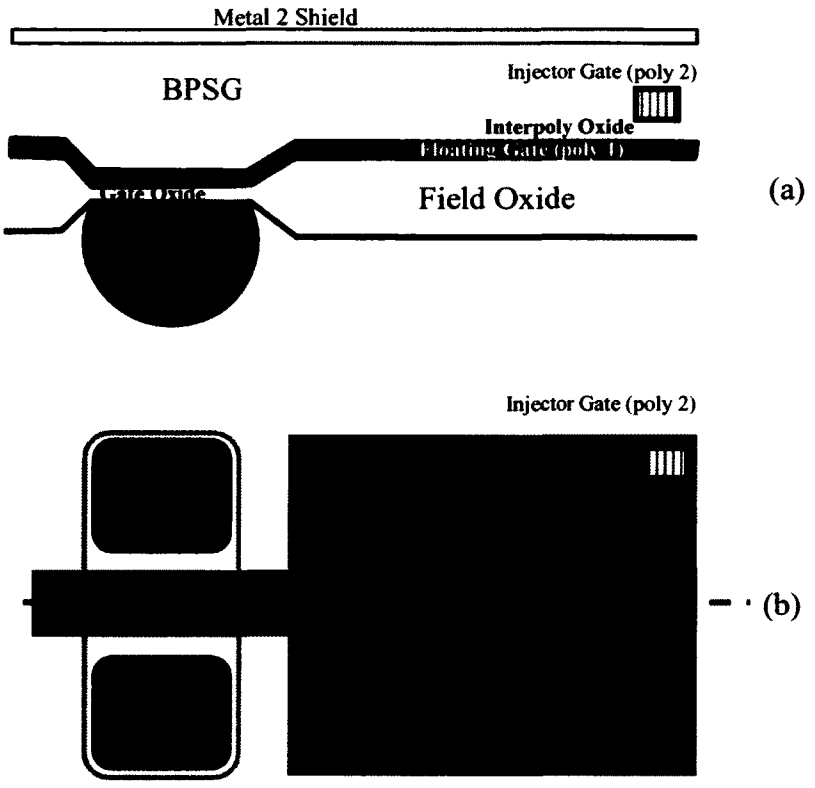

Figure 16- Structure of floating gate sensor transistor. Metal2 layer is used as a shield for better noise and electro-static field immunity. (a) Cross-section (b) Plan view [1]

4. Dosimeter readout circuitry shown in Figure 17 minimizes temperature effects on I_{DS}. In this technique, V_{OUT} is equal to V_{GS} of the floating-gate MOSFET.

This is the first step towards integrating the dosimeter MOSFET with the readout even though in this paper the readout circuit is an off-the-shelf component as opposed to being implemented on the same chip.

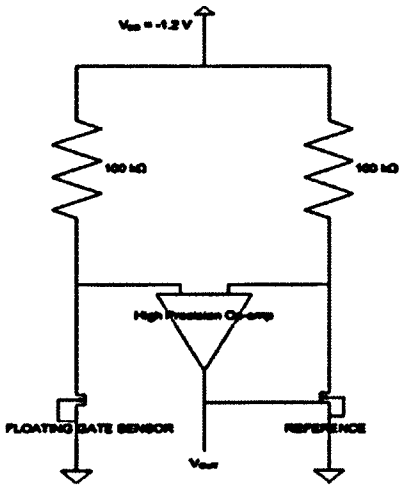

Figure 17- Dosimeter readout circuitry [1].

In this paper, the sensitivity of the MOSFET pair is 3 mV/cGy at a pre-charge floating-gate potential of -7 V up to a total ionizing dose of 10 Gy.

3.4 Most Recent Related Work

The most recent work done on the floating-gate MOSFET dosimeters (FGMOSFETs) has been presented in [**54**], [**2**], and [**55**]. This work is the continuation of the research conducted at Carleton University [**56**], [**52**], [**1**], [**53**] and [**51**].

3.4.1 Design Specifications

In [**2**], the commercially available double-polysilicon 0.8 μm DALSA technology has been used to implement the FGMOSFETs and the readout circuitry. The gate oxide thickness is 17 nm with 450 nm thick field oxide. The dosimeters built in this work are W/L = 20 μm / 4 μm with the gate extension of 100 μm x 80 μm. The reported sensitivity is 1.46 mV/cGy to □-ray radiation for a total ionizing dose of 10.37 Gy.

The floating-gate MOSFETs have been built in pairs where one has a gate extension and the other one serves as a reference device with the same dimensions except

for the absence of the gate extension. Both the MOSFETs are equipped with charging devices which are used to pre-program the floating-gates. It is mentioned that radiation discharges the one with extension because of a large charge-collection body of field oxide underneath the gate extension but leaves the reference MOSFET charge unchanged since it is insensitive to radiation.

3.4.2 Readout Circuitry

The channel current of the irradiated pair is changed due to change in threshold voltage caused by the discharge of the floating-gate and I_D is converted to a voltage by using op-amp (operational amplifier) blocks and then the voltages are differentially read by an adder/subtractor block. This method is specifically of interest because any temperature or gradient process variation in fabrication is eliminated at least to the first order. This point was also previously discussed in [**57**] and is also a common approach to sensor design when any unwanted effect is to be eliminated.

3.4.3 Significance of the Previous Design

In [**2**], the significant changes compared to [**1**] are as follows:

1. The removal of the second polysilicon layer which was used as the injector gate, as shown in Figure 18; this reduces the overall capacitance on the floating gate, therefore, an increase in sensitivity. The floating-gate is pre-charged through drain tunneling by a charging structure placed on the side. This structure is shown in Figure 19. The use of a single polysilicon instead of two layers in the design is also consistent with modern CMOS processes which do not contain the second polysilicon layer. It is also noted in [**2**] that the use of drain tunneling mechanism

does not totally take care of the unwanted capacitance created by the side-injector, but definitely decreases it compared to the previous second polysilicon layer method.

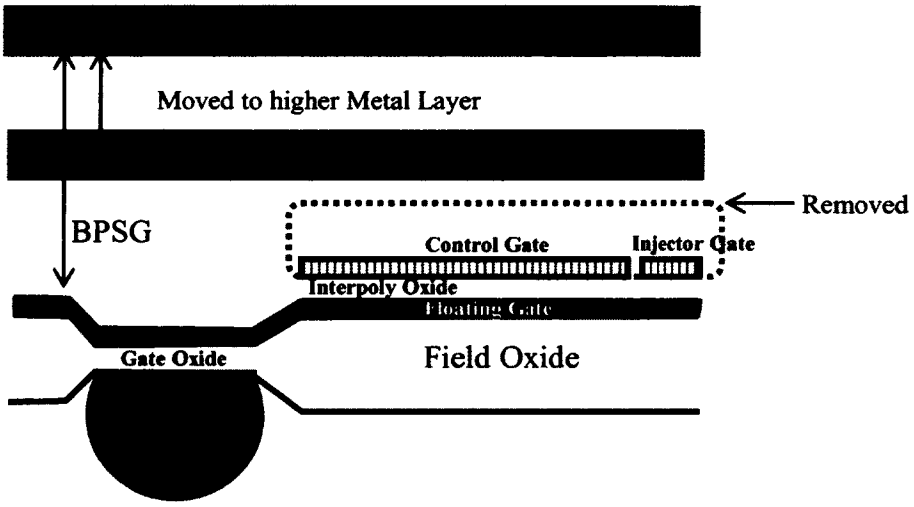

Figure 18- Cross section of the modified FGRADFET structure [2]

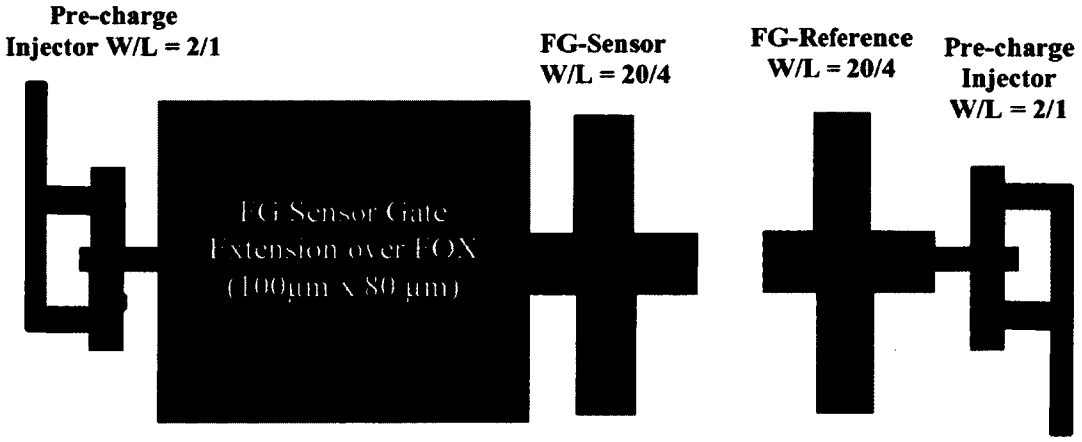

Figure 19- Top view of the pre-charge injectors, the FG-Sensor and the FG-reference [2]

2. The use of metal 3 shielding instead of Metal 2 which increases the effective BPSG volume for the radiation to produce electron-hole pairs. This layer also works as a shield for protecting the sensitive floating-gate from electrostatic fields generated by other components of the chip or by outside sources.

3. The work in [2] was extended in [55] to improve the usability of the dosimeters by adding a separate chip containing the wireless transmission circuitry (with on-chip antenna) which transmits the voltage change value as a result of received dose to a receiver circuit. The transmission circuitry has been implemented in 0.13 μm RFCMOS technology for high frequency application.

3.5 System Concept

In this thesis, I have researched the feasibility of using the modern 0.13 μm CMOS (Complementary Metal-Oxide-Semiconductor) technology in high-radiation dose measurement dosimetry applications such as in biomedical applications including surgical tool and blood sterilization, and to design, characterise and test the MOSFET dosimeters implemented in this technology.

Effective sterilization of blood and medical equipment requires radiation dosimeters to measure the dosage received to ensure that any unwanted substances have been destroyed. These devices currently suffer from several operational and practical limitations (high operating voltages, need for wired connection to interfacing equipment) which make them bulky and expensive. The key to achieving numerous dosimeter enhancements (such as immediate, non-destructive, wireless read-out; extremely small size and power consumption; permanent storage of dose and wide dose range; compatibility with microprocessors; very low cost) is to employ modern commercial CMOS technology in their fabrication. This would constitute an extension beyond the well-established metal-oxide-semiconductor field-effect transistor (MOSFET) used as a dosimeter for ionizing radiation [58].

3.6 Benefits of Proposed Approach and Design

Many of the research works presented in the last section have introduced techniques to tackle radiation dosimetry problem using MOSFETs, but each of them had some limitations. The most recent work done by Dr. Tarr, Dr. Arsalan et al. and presented in the last section, creates the drive for further research on wireless low-power floating-gate CMOS dosimeters.

3.6.1 System-on-chip Solution to the Dosimeter Problem

As it stands now, the FGMOSFETs (floating-gate MOSFETs) and the readout circuitry presented in [2] are implemented in 0.8 μm DALSA process, but the RF transmitter is designed and implemented in 0.13 μm IBM RF-CMOS technology (Figure 20(a)). It is the aim of this research to design the CMOS dosimeters and the readout circuitry in 0.13 μm IBM RF-CMOS technology which will get us one step closer to a monolithic solution where the RF transmission circuit is integrated on the same chip. This is depicted in Figure 20(b).

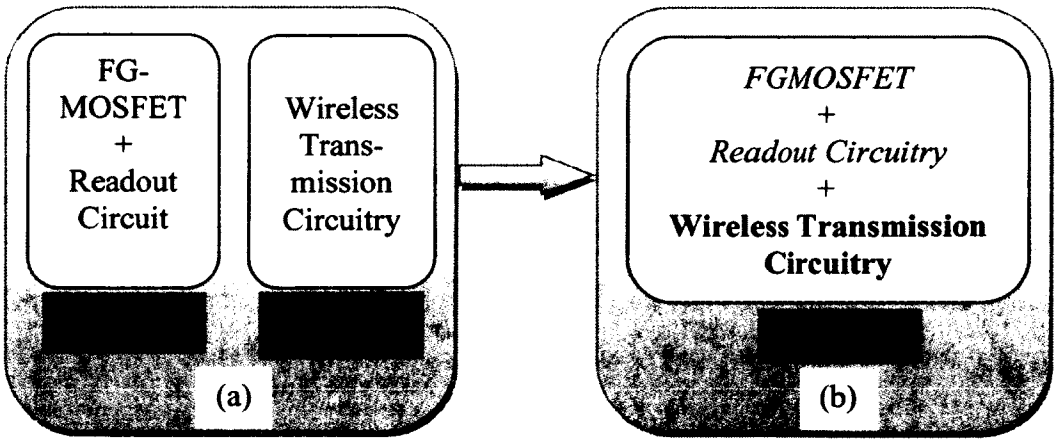

Figure 20- (a) previous research done, (b) research work done in this thesis (italic) and the future work (bold)

To have the entire dosimeter system built on the same chip will be beneficial due to the following reasons:

1. It makes the end product cheaper to manufacture since the manufacturer uses only one technology process for fabrication and also the cost of packaging the chip decreases because the cost of bonding two chips together and gluing them on a single substrate has been removed.
2. Design uncertainties related to the use of two different technologies are eliminated.
3. 0.13 μm technology is more widely used in IC design industry making it a better choice in design than 0.8 μm technology in terms of long-term availability for potential industry users.
4. As IC technology gets more and more advanced, the power consumption of the circuits shrinks in doing the same job as older technologies since the voltage supplies are minimized. This can be seen in the recommended biasing voltages for optimum operation of the transistors in 0.13 μm IBM RF-CMOS technology package. The low-power operation of bio-sensors such as dosimeters is desirable since it allows for power scavenging techniques such as RF powering for wireless operation of the sensor and the readout circuit.

Chapter 4 Floating-Gate Radiation Field Effect Transistor (FGRADFET) Design

The previous chapters extensively discussed the physical effects of ionizing radiation on MOS transistors with a conclusion that pMOS dosimeters are preferred over the nMOS dosimeters, and that the generation of interface and bulk oxide traps are the major factors in shifting the threshold voltage and mobility in channel carriers. It was also mentioned that gate oxide thickness reduction in recent MOS technologies has had an adverse effect on radiation sensitivity; therefore, it was concluded that to increase the sensitivity in ultrathin gate oxide dosimeters, floating-gate MOS dosimeters must be used. To reiterate the focus of this research, the previously developed FGRADFET utilizing a 0.8 μm DALSA process could not integrate circuitry on the same chip and the work at hand tries to verify the feasibility of realizing FGRADFETs in a 0.13 μm MOS technology suitable for RF. Moreover, it will explore an original approach to read out the measured dose.

From this point onwards, floating-gate MOS dosimeter is only used to describe the pMOS dosimeter. The names "FGRADFET" or just "RADFET" also refer to the same device which may be used interchangeably throughout the thesis.

The following sub-sections discuss the design of a new ultrathin gate-oxide dosimeter in IBM's 0.13 μm CMOS technology.

4.1 Floating-Gate MOSFET Theory

In this section, FG-MOS transistors are briefly explored and the purpose of using these devices in the ionizing radiation application of this research is explained. Finally, formulae related to radiation sensitivity of these devices are introduced.

4.1.1 Single-Polysilicon FGRADFET Structure and Principle of Operation

As explained previously, modern CMOS dosimeters suffer from low sensitivity because of decreased gate-oxide thickness, which decreases the effect of N_{it} and N_{ot} on channel current and mobility. An approach to increasing the sensitivity of these dosimeters is to electrically float the gate of the MOSFET such that the gate is surrounded by dielectric materials. The gate is isolated from the bulk by SiO_2, and by boro-phosphoro-silicate glass (BPSG) from the top metal layers. The floating-gate by itself does not increase the sensitivity, but rather an extension to the floating-gate is needed. The floating-gate extension is a much larger area of polysilicon laid over the STI. The STI region is as large as the floating-gate extension above it and its depth is 0.35 μm. This extended layer increases the gate's radiation exposure. The STI region works as a large source of generated electron-hole pairs during irradiation which helps increase the sensitivity by the following phenomena.

As explained in [55], [2], [59] and [1], the floating-gate needs to be charged with electrons before the irradiation by some mechanism to be explained later. Once the floating-gate is "charged", an electric field is created within the STI and gate oxide regions between the gate and the substrate – in the case of a double-polysilicon structure, the electric field is created between the floating-gate and the substrate and the control gate. In pMOS dosimeters, an accumulation (injection) of negative charge on the

floating-gate induces positive mobile charge in the channel which lowers the magnitude of the threshold voltage since a channel inversion is induced. During irradiation, the holes which are generated move under the influence of this electric field towards the floating-gate and neutralize the mobile charge placed on it. This in turn will increase the threshold voltage which will cause a change (decrease) in I_{DS} under a constant V_{DS}. This change, along with the change in mobility and the creation of N_{it} and N_{ot} centers, contributes to the overall sensitivity of the RADFET.

4.1.2 FGRADFET Circuit Model

The best way to represent a floating-gate RADFET is to use capacitive modeling as shown in Figure 21. Here, C_{STI}, C_{OX}, and C_{BPSG} are respectively the capacitances associated with the trench isolation, gate-oxide, and BPSG material on top of the floating-gate; while C_{DEP}, C_{FB}, C_{FS}, and C_{FD} are the depletion region, body, source and drain coupling capacitances, respectively [**59**]. The capacitances associated with the pre-charging MOS device are not considered here because they are electrically open-circuited while the dosimeter is in operation.

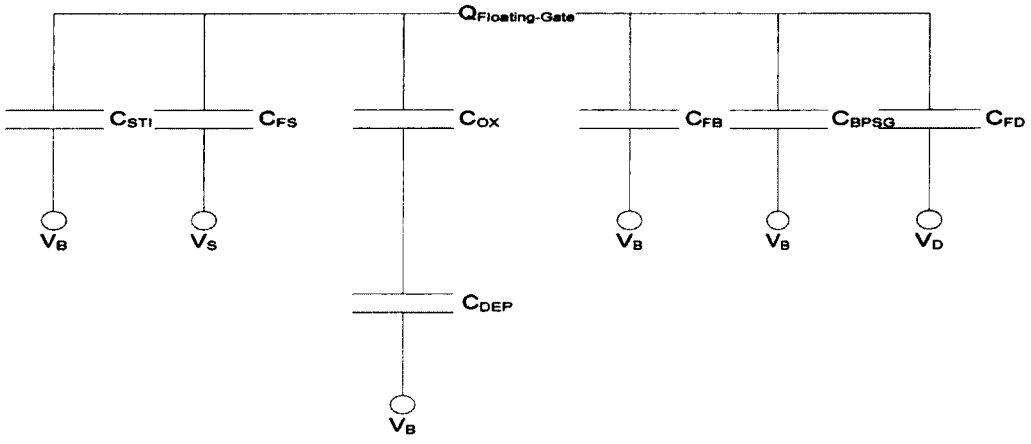

Figure 21- Capacitive model of the FGRADFET excluding the pre-charger MOS device

The following equations describe the radiation effect on the floating-gate MOSFET. The floating-gate voltage can be expressed as:

$$V_{FG} = \frac{C_{FS}V_S + C_{FD}V_D + C'_{ox}\psi_s + Q_{FG}}{C_{sum}} \quad 4\text{-}1$$

where V_S and V_D are the source and drain voltages, ψ_s is the surface potential, Q_{fg} is the charge on the floating-gate, and C'_{ox} is the total oxide capacitances in the BPSG, gate, and STI regions as defined by:

$$C'_{ox} = C_{ox} + C_{BPSG} + C_{STI} \quad 4\text{-}2$$

and finally:

$$C_{sum} = C_{FS} + C_{FD} + C_{FB} + C'_{ox} \quad 4\text{-}3$$

The change in V_{FG} with respect to the change in Q_{fg} is

$$\frac{\partial V_{FG}}{\partial Q_{fg}} = \frac{1}{C_{sum}} + \frac{C_{ox}}{C_{sum}}\frac{\partial \psi_s}{\partial Q_{fg}} \quad 4\text{-}4$$

which simplifies to the following for negligible changes in surface potential with floating-gate charge.

$$\frac{\partial V_{FG}}{\partial Q_{fg}} = \frac{1}{C_{sum}} \quad 4\text{-}5$$

Also, for the MOS dosimeter operated in the above-threshold region where the surface potential is nearly constant, the change in current with respect to radiation is as follows:

$$\frac{\partial I_D}{\partial Q_{fg}} = \left(\frac{\partial I_D}{\partial V_{FG}}\right)\left(\frac{\partial V_{FG}}{\partial Q_{fg}}\right) = \left(\frac{\partial I_D}{\partial V_{FG}}\right)\frac{1}{C_{sum}} \quad 4\text{-}6$$

Knowing that $\partial I_D/\partial V_{FG}$ is the transconductance of the transistor g_{mFG}, and

$$g_{mFG} = 2\sqrt{KI_D} \tag{4-7}$$

where K is the proportionality constant, then

$$\frac{\partial I_D}{\partial Q_{fg}} = \frac{2\sqrt{KI_D}}{C_{sum}} \tag{4-8}$$

In the sub-threshold operation region of the dosimeter, the current varies exponentially with the floating-gate voltage and the change in current with respect to Q_{FG} is as follows:

$$\frac{\partial I_D}{\partial Q_{fg}} = \frac{\kappa I_D}{U_T C_{sum}} \tag{4-9}$$

where κ is the subthreshold slope and U_T is the thermal voltage.

The ionizing radiation generates electron-hole pairs by depositing energy E_{dep} in the material it hits, and the charge created is

$$Q_{gen} = \frac{qE_{dep}}{W_{e-h}} \tag{4-10}$$

where Q_{gen} is the amount of charge created, and W_{e-h} is the electron-hole pair generation energy which is 17 eV for SiO_2 [**1**], [**6**]. Of the generated electron-hole pairs, some recombine at a fraction R(E) and some get separated by the electric field E in the oxide and are collected. The collected charge Q_{col} can be expressed as follows:

$$Q_{col} = (1 - R(E))Q_{gen} = (1 - R(E))\frac{qE_{dep}}{W_{e-h}} \tag{4-11}$$

Equation 4-11 can be further broken down if E_{dep} is expressed as follows:

$$E_{dep} = D \cdot m \tag{4-12}$$

where D is the total absorbed dose, and m is the mass of the oxide. The mass m can be expressed as

$$m = \rho_{SiO2} \cdot A \cdot t \tag{4-13}$$

where ρ_{SiO2} is the oxide density, A is the area of the capacitor between the floating-gate and the bulk, and t is the oxide thickness. Hence the total collected charge can be expressed as below:

$$Q_{col} = (1 - R(E)) \frac{q \cdot D \cdot A \cdot t \cdot \rho_{SiO2}}{W_{e-h}} \tag{4-14}$$

It is important to notice that the RADFET consists of different oxide regions which contribute to charge generation such as the gate oxide, BPSG, and the STI; therefore, the above equation needs to be generalized as follows:

$$Q_{col} = \frac{qD}{W_{e-h}} \sum_i (1 - R_i(E_i)) A_i t_i \rho_i \tag{4-15}$$

Equation 4-15 accounts for the electric fields across the gate oxide, STI, and the BPSG within the dosimeter. It also accounts for the areas, thicknesses, and different dielectric densities in the above-mentioned regions.

Having derived the above equation for the collected charge, the change in current can be expressed as below:

$$\Delta I_D = \frac{g_{mFG}}{C_{sum}} \Delta Q_{fg} \tag{4-16}$$

where ΔQ_{fg} is the change in charge, which is equivalent to Q_{col}. Therefore,

$$\Delta I_D = \frac{g_{mFG}}{C_{sum}} \frac{qD}{W_{e-h}} \sum_i (1 - R_i(E_i)) A_i t_i \rho_i \qquad 4\text{-}17$$

To further expand the equation, C_{sum} is included in Equation 4-17.

$$\Delta I_D = \frac{g_{mFG}}{C_{FS} + C_{FD} + C_{FB} + C_{ox} + C_{BPSG} + C_{STI}} \frac{qD}{W_{e-h}} \sum_i (1 - R_i(E_i)) A_i t_i \rho_i \qquad 4\text{-}18$$

Of the capacitances in Equation 4-18, the drain, source and body capacitances can be neglected because of their small size compared to the other capacitances.

$$\Delta I_D = \frac{g_{mFG}}{C_{ox} + C_{BPSG} + C_{STI}} \frac{qD}{W_{e-h}} \sum_i (1 - R_i(E_i)) A_i t_i \rho_i \qquad 4\text{-}19$$

From Equation 4-19, it is concluded that increasing ΔI_D with respect to absorbed dose necessitates a decrease in C_{sum} and an increase in E (the electric field in oxide regions). An increase in E causes more generated electron-hole pairs to be separated, and less to be recombined, hence a decrease in R(E). The other parameters such as oxide thicknesses and densities are not under the control of designers and are set by the CMOS foundry [**59**].

4.2 Pre-charging Mechanism

Earlier, it was mentioned that the floating-gate dosimeter requires mobile charge to be injected on it prior to irradiation. Since there is no electrical connection to the gate to put charge on it, other physical methods need to be explored. The most relevant device to FGRADFETs is the EEPROM, which was discussed in the second chapter. The EEPROM consists of an upper control gate which is electrically connected and a lower polysilicon gate which is electrically floating. The EEPROMs utilise avalanche injection or tunneling as two methods for adding on or taking away charge from the floating-gate

[60]. The same methods can be used for injecting charge onto the floating-gate dosimeter with the exception that in modern IC technologies such as 0.13 μm IBM RF-CMOS, there is no second polysilicon available to be used as a control gate. However, this limitation does not impede the pre-charging process in the case of single-poly dosimeters. For the purpose of pre-charging, a shorted pMOS (drain and source connected together) is used as can be seen in Figure 22-(a). In this process, electrons tunnel through the oxide barrier in the presence of a high electric field to increase charge on the floating-gate. This quantum mechanical tunneling process is an important mechanism for thin oxide barriers such as those found in metal-semiconductor junctions or highly-doped semiconductors. In this case, a voltage difference between the tunneling junction (the shorted pMOS) and the floating-gate causes the electrons to tunnel through the pMOS gate oxide to the floating-gate [61]. The magnitude of this tunneling current depends on the oxide voltage, V_{OX}. The following equation approximates the tunneling current [62].

$$I_{tun} = -I_{tun0}\, WL\, e^{\left(-\frac{V_f}{V_{ox}}\right)} \qquad 4\text{-}20$$

where I_{tun0} is a pre-exponential current, V_f is a constant that varies with oxide thickness, and W and L are the width and length of the tunneling pMOS respectively. In Equation 4-20, increasing the area of the shorted pMOS and increasing the voltage across the oxide increase the tunneling current, hence producing a more rapid pre-charging process. Figure 22-(b) shows the cross section of the FGRADFET containing parametric information and different regions corresponding to the schematic.

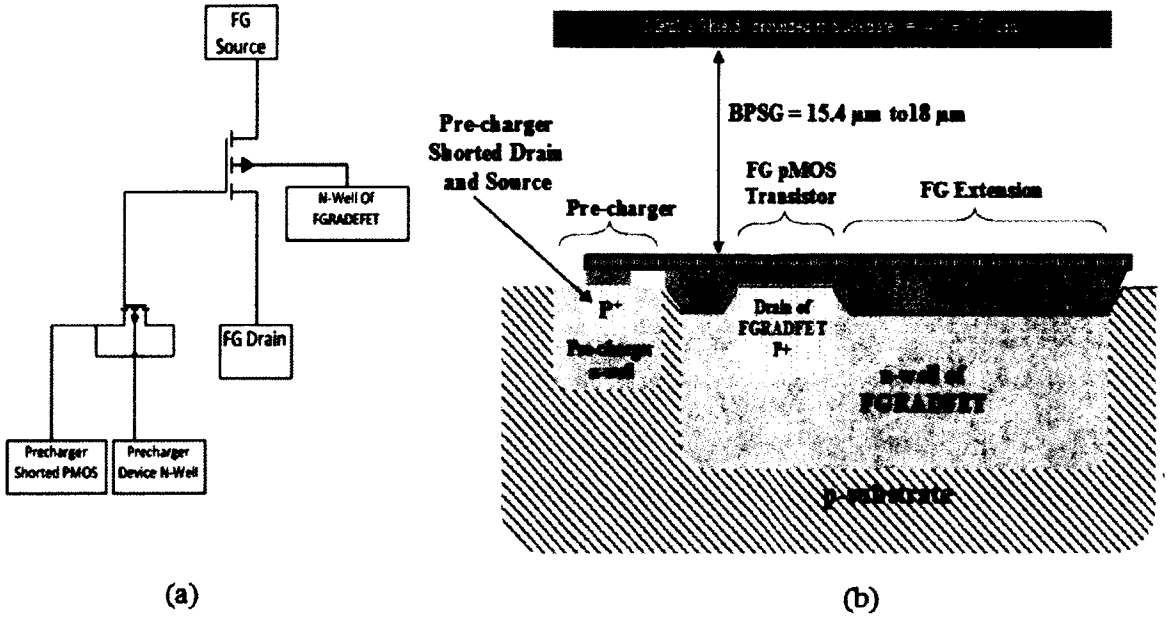

Figure 22- FGRADEFT and the pre-charging shorted pMOS in 0.13 μm CMOS technology (a) schematic, (b) cross section of FGRADFET

4.3 Proposed Dosimeter IC

Sections 4.1 and 4.2 explored some aspects of the design of FGRADFETs. The important parameters are sensitivity of the RADFET, the pre-charging mechanism, and the readout circuitry. In this section, the main dosimeter IC design is introduced and layout considerations are explained. In later sections, experimental verification of the dosimeter design is considered before irradiation testing which is done in Chapter 5.

The dosimeter prototypes are laid out on a 2 mm × 1 mm area of the p-substrate 0.13-μm IBM RF-CMOS IC. The chip area is divided into three sections consisting of the following designs:

1 Three single FGRADFETs with different gate extension sizes that are paired up with their identical reference MOSFETs;

2 Three integrated dosimeters, including the readout buffer;

3 One readout circuitry without any dosimeter attached for operation verification, design validation, and offset measurement purposes.

The three gate extension sizes will allow the full range of possible FGRADFET sensitivities to be explored. Figure 23 shows a conceptual floor plan.

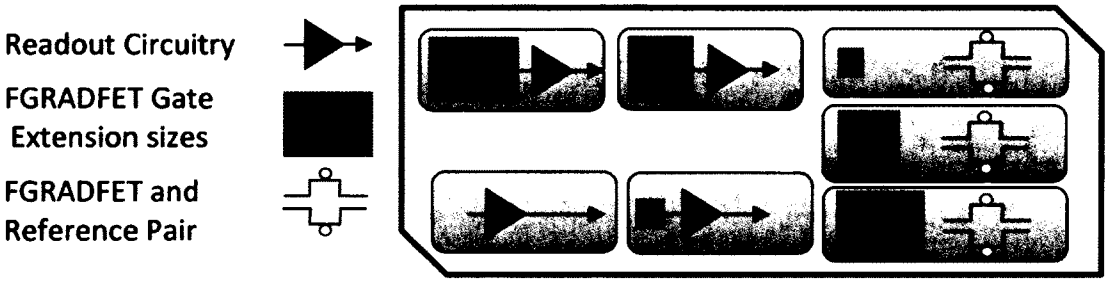

Figure 23- Conceptual floor plan of the chip

The next sub-sections introduce these different devices in detail.

4.3.1 Single FGRADFETs Design

Three different variations of the FGRADFET design are proposed. Figure 24 is a simplified schematic of the FGRADFET along with the reference pMOS device and the pre-charger device. Each of these devices is paired with an identical replica of itself except for the gate connection of the reference pMOS. The pMOS is a reference device to determine the amount of charge present on the floating gate. It serves two purposes:

1. To determine the amount of charge on the floating-gate by measuring the I_{DS} current in the channel of the FGRADFET at a set V_{DS}, then trying to achieve the same current at the same V_{DS} by setting the gate voltage to different values on the reference MOSFET. This method is useful in pre-charging stage to indirectly determine how much charge has tunnelled to the floating-gate.

2. To be able to use an external high precision amplifier to differentially read the output of the pair.

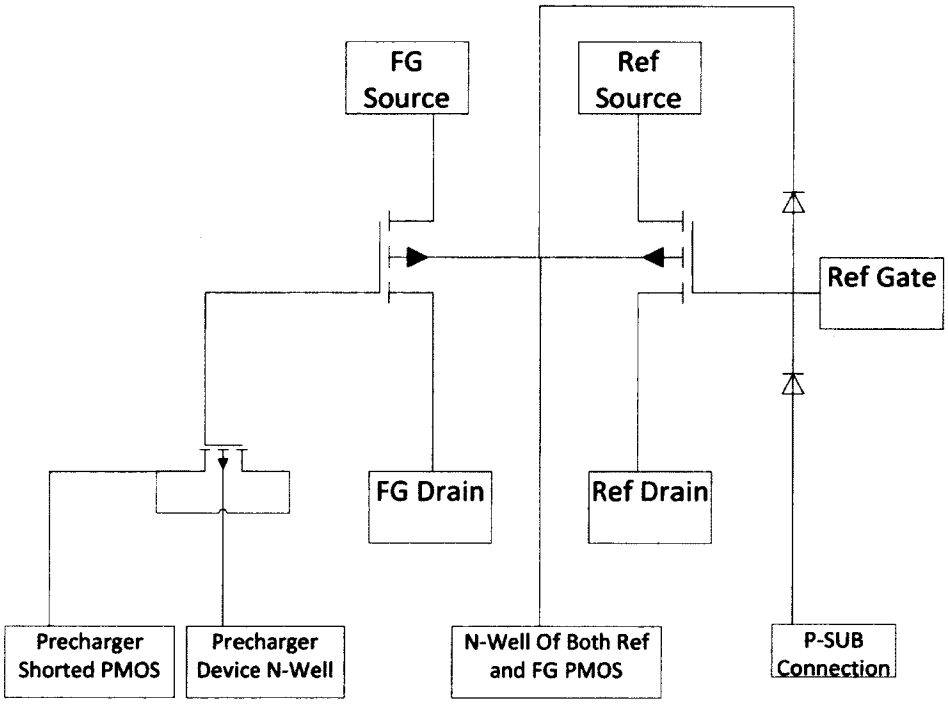

Figure 24- FGRADFET and reference MOS devices

4.3.1.1 Design concept

The 130-nm technology is a typical p-substrate technology which means that the pMOS's have to be laid out in an n-well. In Figure 24 the n-well contact for the reference and the RADFET are the same to save pad area even though the two have separate n-wells. Furthermore, there is a double diode electrostatic discharge protection (ESD) placed at the gate of the reference device to prevent any damage to it. The gate of the pMOS is only capable of handling voltages of up to ~ 2 V; hence, it can be easily damaged by ESD. To save pad area, the double diode is placed between the p-sub pad, which is connected in a network throughout the entire chip with multiple pads and the n-well connection. It is a safe and effective way to save pad area because the p-sub

connection can always be put at ~ -1 V (allowed voltage range for this technology is between -1.2 V to 1.2 V) while the n-well of the devices is at 0V which keeps the double diode reverse biased at all times.

Figure 25 shows the FGRADFET as captured in the Cadence CAD tool. Not counting the p-sub contact, there are 8 pads for each pair of devices; two of which are used by the pre-charging shorted pMOS and the n-well associated with it. The pre-charging device has its own separate n-well connection. This will allow the voltages of the shorted source/drain and the n-well to be freely changed with respect to the FGRADFET. Hence the pre-charging device can be negatively or positively biased with respect to the FGRADFET and the effects of this bias can be studied. The FGRADFET and the reference pMOS are situated in separate n-wells but they are connected to each other by a metal layer to a common bonding pad that allows for saving bonding pad area on the chip (see Figure 24).

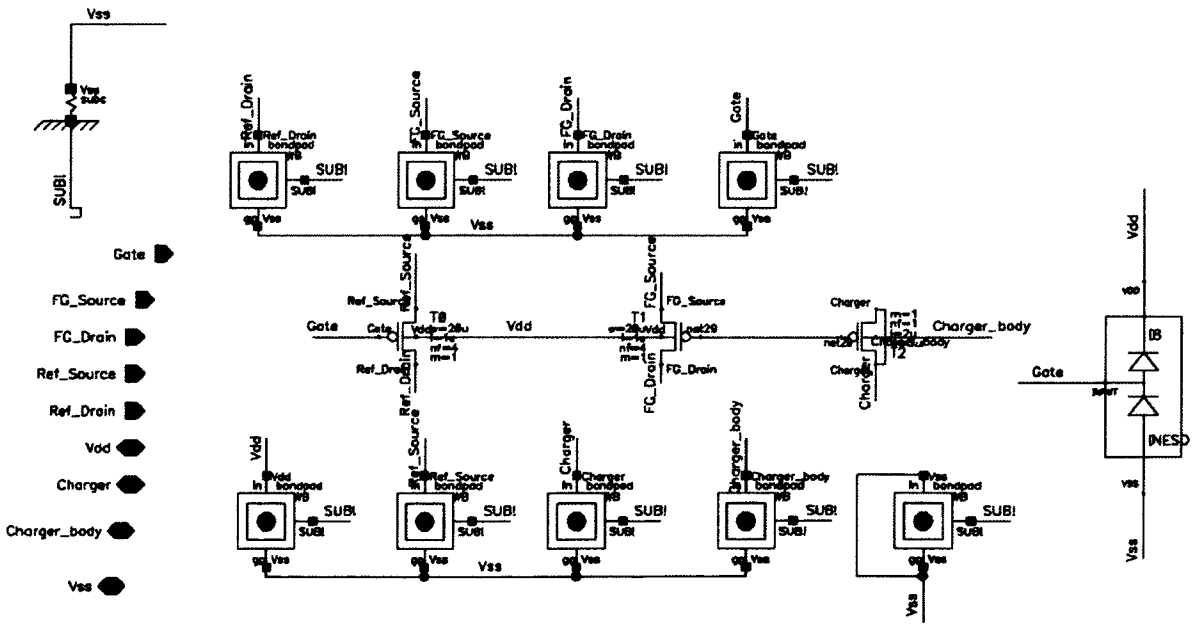

Figure 25- FGRADFET and reference pair schematic

For all of the design variations, the active region of the FG device is sized at W/L = 20 μm / 1 μm in 4 × 5 μm fingers. This sizing is chosen to enable comparison with the results in [**55**].

For the sensitivity analysis of the FG devices, three different floating-gate extensions were laid out. Considering the antenna rule limitation for this technology, the largest gate extension area achievable is 100 times the active region area. It should be noted that the antenna rule sets a limitation on how large in area a conductive layer such as polysilicon or metal routing can be before it can destroy the dielectric layer which separates it from other conductive layers in fabrication process. In the case of the polysilicon gate, the area of polysilicon outside the active region which is defined by W × L of the MOSFET cannot be larger than 100 × W × L for IBM's RF-CMOS process.

To remain safely within limits of the antenna rule, the largest extension ratio used is 90:1. The other gate extension sizes are: small - no gate extension, which means the pre-charging device gate was connected to the floating gate using a short path of polysilicon preventing large extension creation; and medium - 45:1 ratio of gate extension which is mid-way between the largest gate extension and no gate extension. The three gate extensions cover the entire allowed range of floating gate extension to study the sensitivity of the FG sensors. Figure 26 shows an expanded view of the small FGRADFET device while Figure 27 illustrates the complete layout of the same device with all components (vias, ESD protection, contact pads, routing, and metal fill) included. As can be seen in Figure 26, the upper device is the floating-gate dosimeter and the pre-charging device to its right, and the lower device is the gate-connected identical reference pMOS transistor.

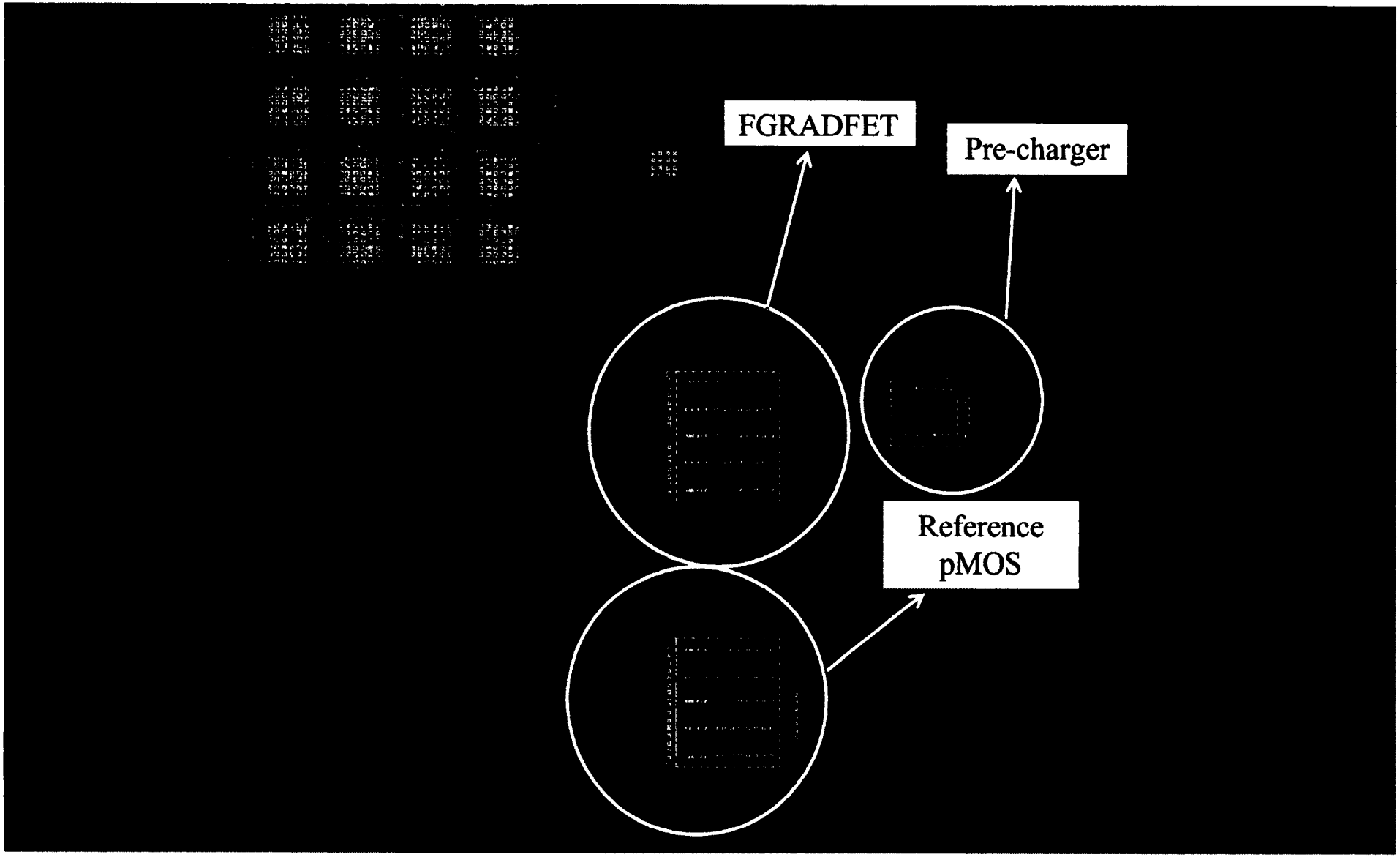

Figure 26- Expanded layout of small FGRADFET

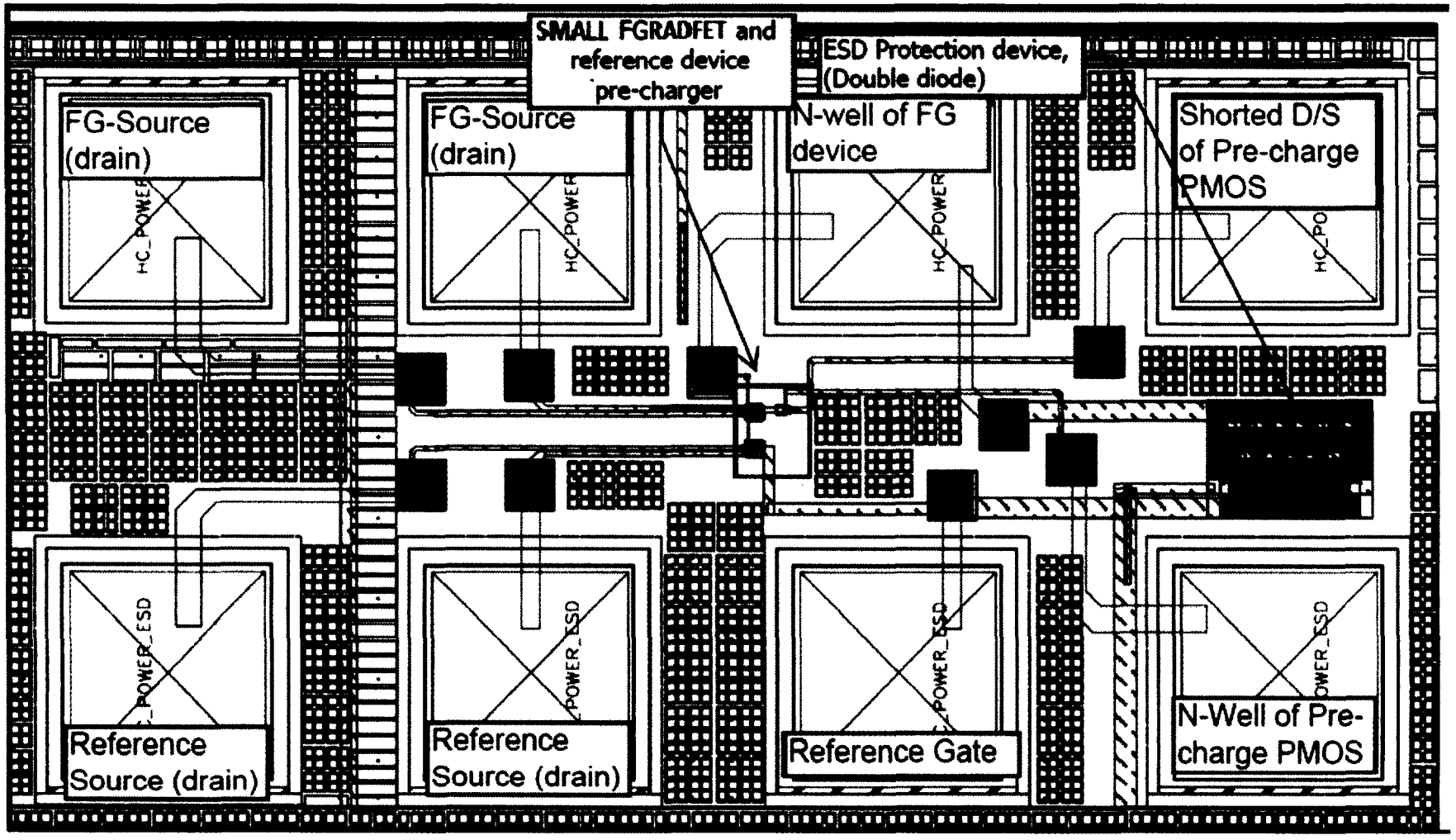

Figure 27-Small FGRADFET and the reference pMOS with no gate extension

Further details on the testing method are given in the testing strategy section (sec. 4.3.2).

Except for the small FGRADFET, the devices are covered by a metal-8 sheet (highest and thickest metal layer available in this technology) to shield its very sensitive floating-gate (see Figure 22-(b)). This shield is connected to the p-sub using metal contacts and vias. The metal shield is necessary because the floating-gate is fairly sensitive to ambient light and electromagnetic fields around it from external sources. Also, it serves the purpose of increasing the volume of BPSG for generation of electron-hole pairs during irradiation. As given in the manufacturer's specifications, the polysilicon layer is between 13 μm and 18 μm (taking into account process variations noted in the design specifications) below the metal-8 shield. The metal-8 shield is (4.0 ± 0.5) μm thick and is made of aluminum.

In Figure 27, the top three metal layers (metal 6, 7, and 8) are shown as small square boxes. The total surface area covered by these metal layers need to fulfill a certain percentage of the total area of the chip; that is the reason for the small square blocks present on the surface. The metal fill is there to even out the surface of the chip and has no other purpose.

4.3.1.2 Medium and Large Extension FG-Sensor and Reference Pair

The layout of the medium and large gate extension FGRADFETs are presented in Figure 28 and Figure 29, respectively. They differ from the small gate extension case only by the increasing size of polysilicon areas circled in the figures.

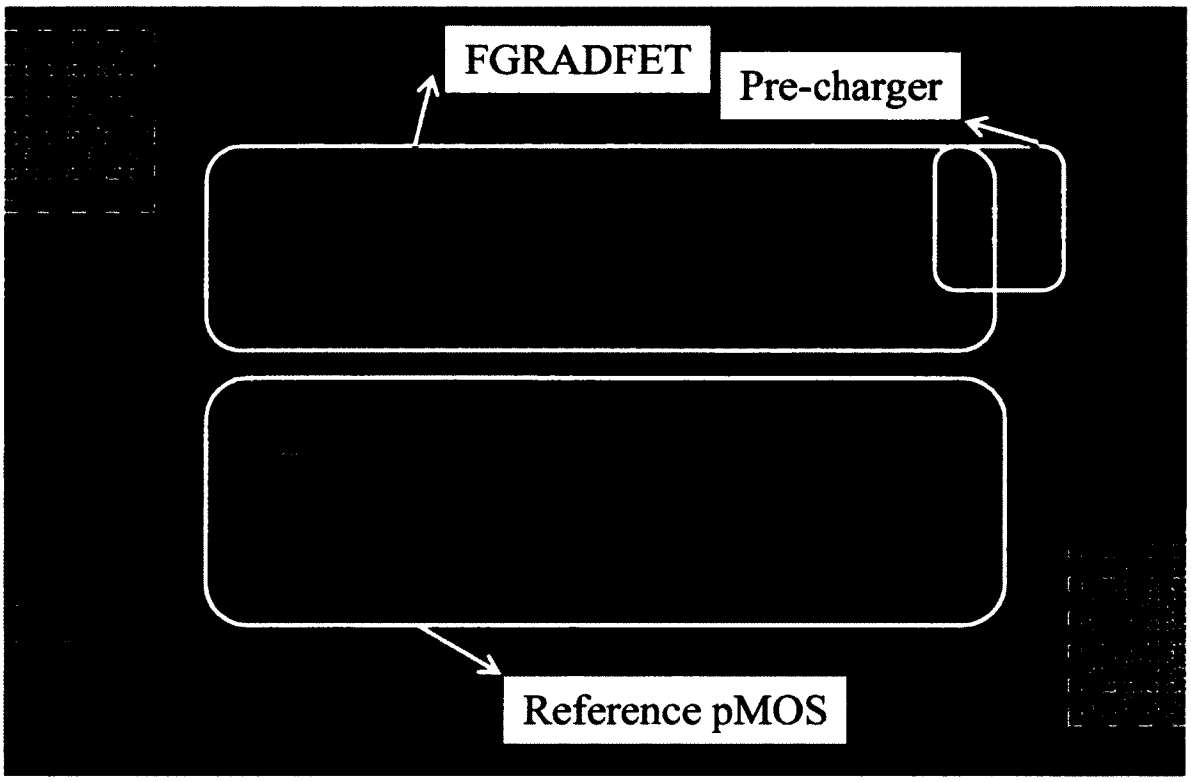

Figure 28- Expanded layout of medium FGRADFET

The medium gate extension is 60 μm x 15 μm = 900 μm^2. This is 45 times the active region area of 20 μm^2.

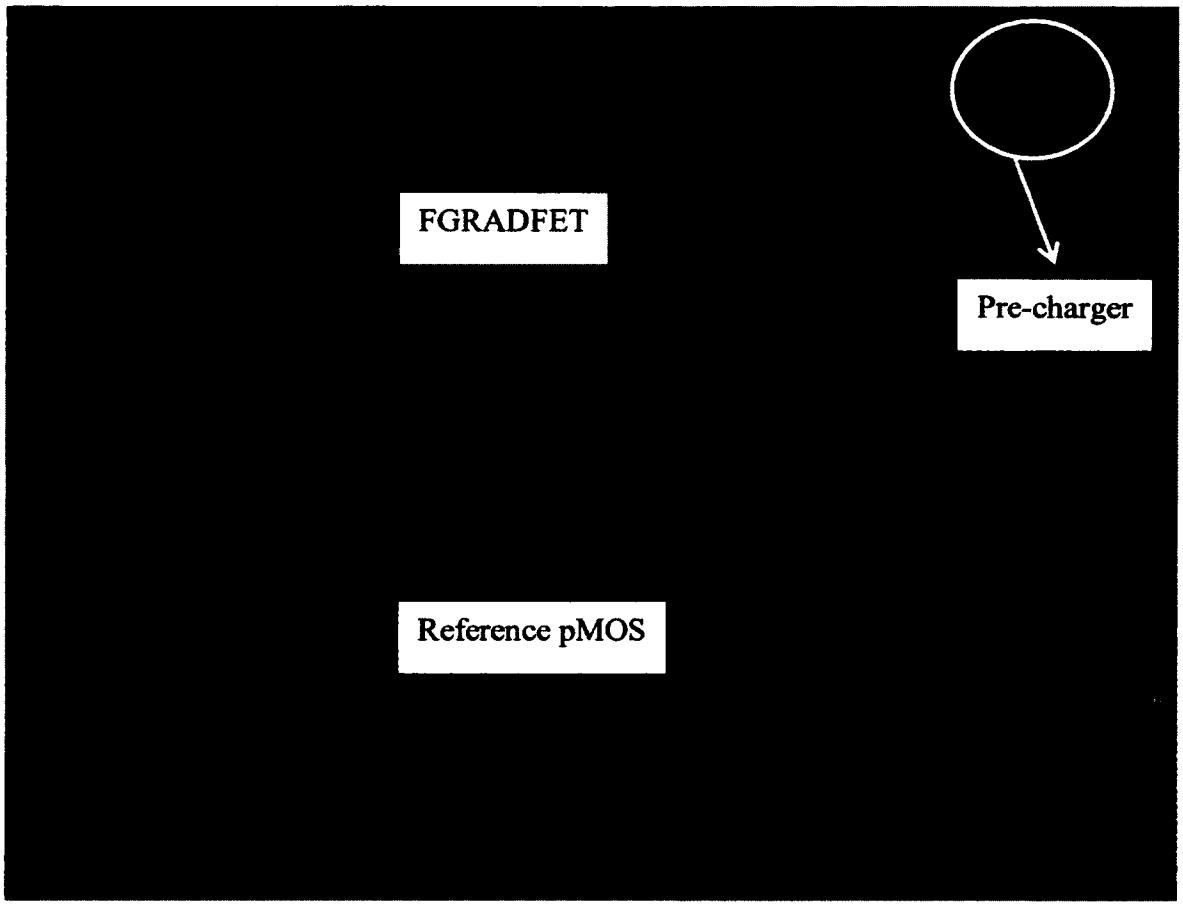

Figure 29- Expanded layout of large FGRADFET

The large gate extension is 60 μm x 30 μm = 1800 μm^2. This is 90 times the active region area of 20 μm^2.

As the three versions of the FGRADFET and reference pairs are identical except for the gate extensions, it is reasonable to only present one set of test procedure and results for the three cases.

4.3.2 Single FGRADFET Initial Testing

The design layouts presented in the previous sub-section were sent out for fabrication and 40 individual chips were received for testing.

This section presents the verification testing strategy and functionality test results of the FG device and the reference. Figure 30, Figure 31, and Figure 32 show a microscopic photograph of the IC, the test setup with various power supplies and meters, the semiconductor parameter analyzer (SPA), and the probing station, and a sample IC under the microscope, respectively.

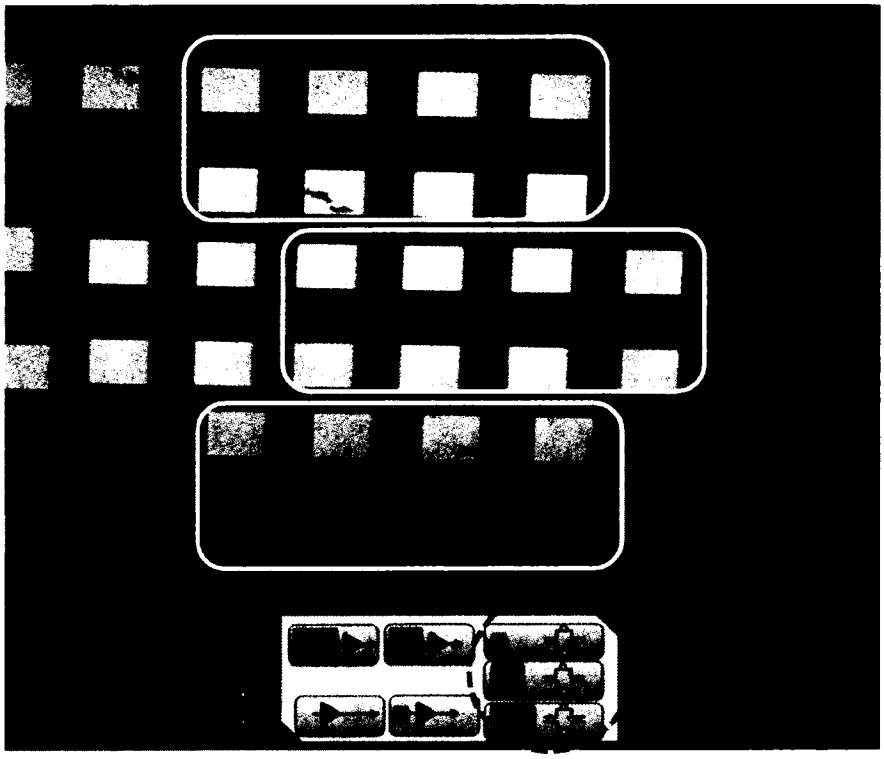

Figure 30- A microphotograph of the FGRADFET pairs. The encircled area of the "floor plan" corresponds to the microphotographed chip.

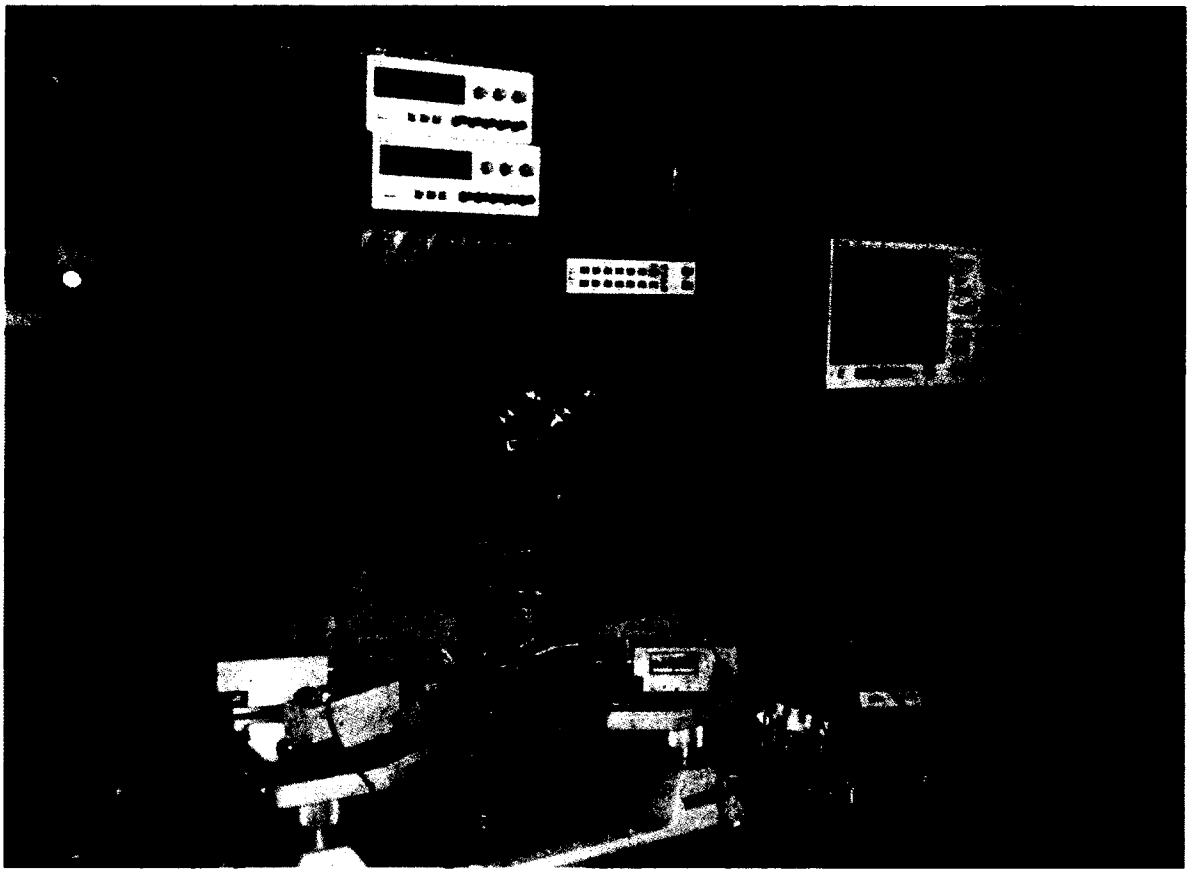

Figure 31- Test setup and various measurement and supply tools

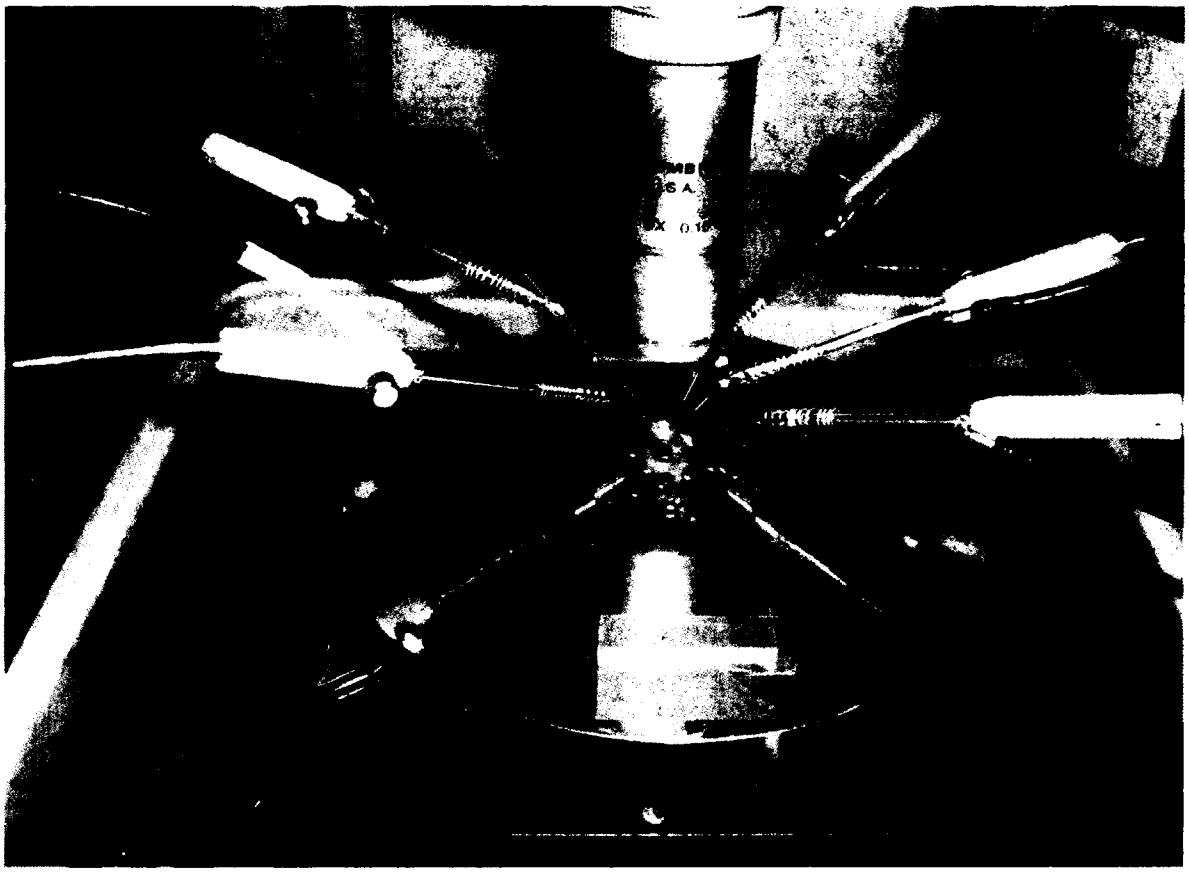

Figure 32- A sample IC under the microscope

At first, the junction diodes of the FGRADFET will be tested, then the FGRADFET itself is tested, and at last the reference MOSFET is tested. The reason for testing the FGMOS before the reference MOSFET is to prevent any charge transfer from the reference MOSFET's gate (while testing the reference MOSFET) into the neighboring floating gate of the sensor.

The testing is done using the probing station in the RF cage and the Agilent semiconductor parameter analyzer (SPA-4155) is used to collect current and voltage data. To minimize any accidental charging the tester is grounded and also before touching

down the probes, they are touched by a piece of grounded wire to ensure the probes do not transfer charge into the floating-gate. The testing is done with the microscope light OFF, and the RF cage light OFF also.

4.3.2.1 Junction Diode Testing

Before testing the FGRADFET, each of the p-n junctions in the device is tested to verify if there are any flaws in the design. The various p-n junction diode I-V curves are presented in Figure 33 (showing drain to n-well, source to n-well, and n-well to p-sub junction diode characteristics.

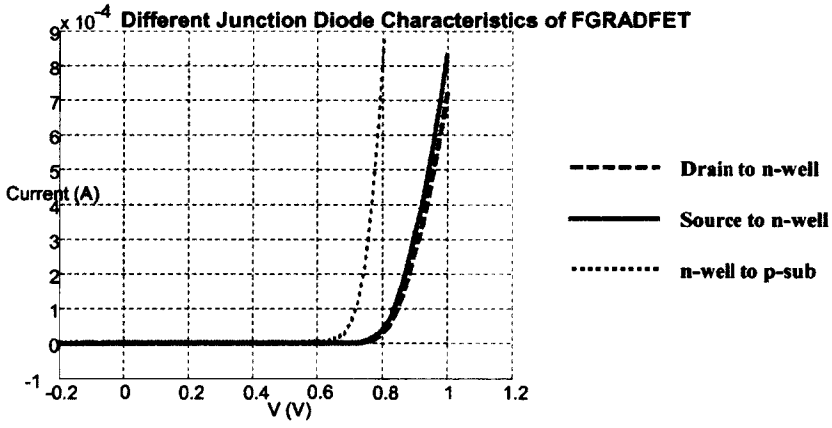

Figure 33- FGRADFET junction diode verification testing

The n-well to p-sub junction diode is forward-biased at a lower voltage; hence it rises faster, which is due to the light substrate doping. To prevent damage to the junctions, the current compliance on the SPA4155 was set to 1 mA after which the test halts.

It is apparent that the junctions of the FGRADFET are all laid out correctly and the junction diodes are properly working.

4.3.2.2 Small FGRADFET Testing

The floating-gate device has three contact pads: the drain, the source, and the n-well. The p-sub connection is a general terminal for the entire chip, which can be left out since the active area of the device is sitting in the n-well which is isolating the source and drain diffusion regions from the p-sub. Therefore, it should not matter whether the p-sub connection is connected or left floating.

Note: The FGMOS device with no gate extension does not have the metal-8 shield on it because of its small size.

Figure 34 illustrates the schematic with the circuit biasing. The pMOS is biased in a common source configuration with the n-well and the source tied together and to the ground of the SPA4155 while the drain is connected to the other in/out terminal of the SPA4155.

The schematic also includes the double diode connection with the gate and substrate pad to examine the effects of having them connected or floating even though they are not part of the FGRADFET.

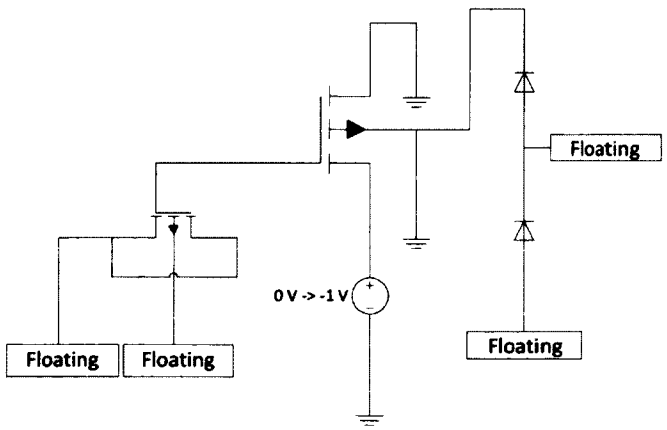

Figure 34- FGRADFET device biasing for testing the charge presence before the pre-charge stage

Figure 35 shows the I-V curve of the FGRADFET considering the biasing condition in Figure 34 and the microscope light being OFF.

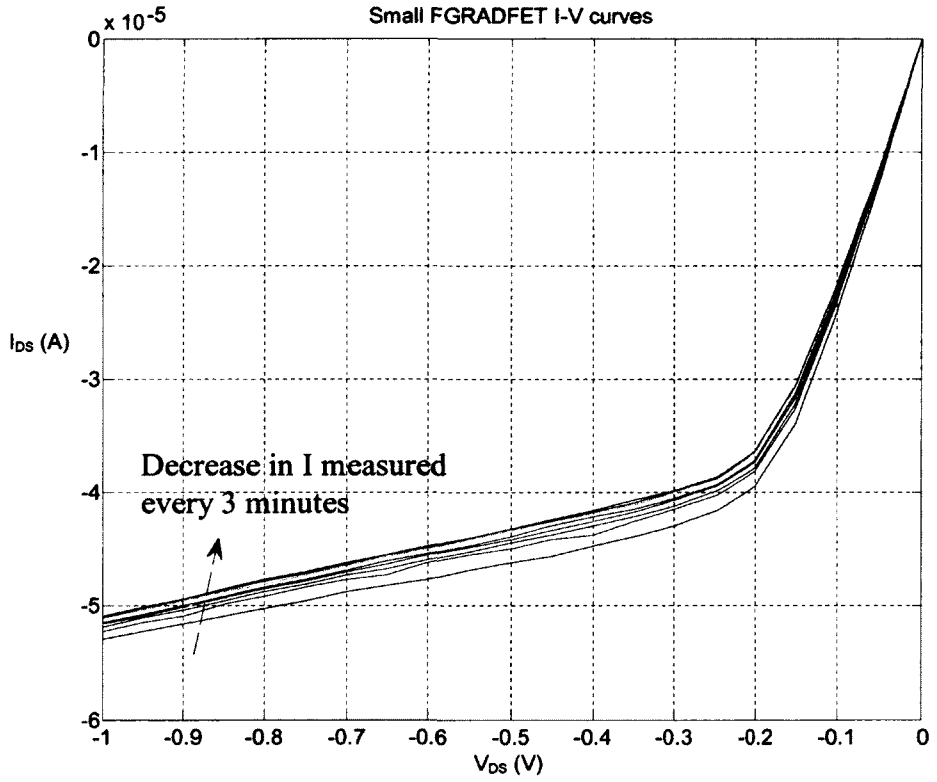

Figure 35- Pre-irradiation FGRADFET I-V Curves measured every 3 minutes

It is shown that there is current flowing in the channel of the FGMOS before any pre-charging attempt. The I-V curve looks somewhat the same as that of a regular (gate-connected) MOSFET. There is a decrease in current over time. The current was read every 3 minutes until it stabilized. It is surprising to have a large amount of current flowing through the channel at different values of V_{DS}. One reason could be the effect of the drain and source voltages on the floating-gate which are capacitively coupled to the floating-gate, inducing a voltage on the gate which in turn creates a channel at larger V_{DS}. Different connection variations were investigated on this sample with the light ON or

OFF. Given the highly sensitive nature of the floating-gate to light, it would be necessary to cover the devices to obtain reliable results.

Next, the effect of the gate voltage of the reference MOSFET on the current through the FGRADFET is studied as shown in Figure 36 . This test is done to illustrate the effect of different voltage biases applied to circuitry close to the FGRADFET and the sensitivity of the FGRADFET to such bias voltages.

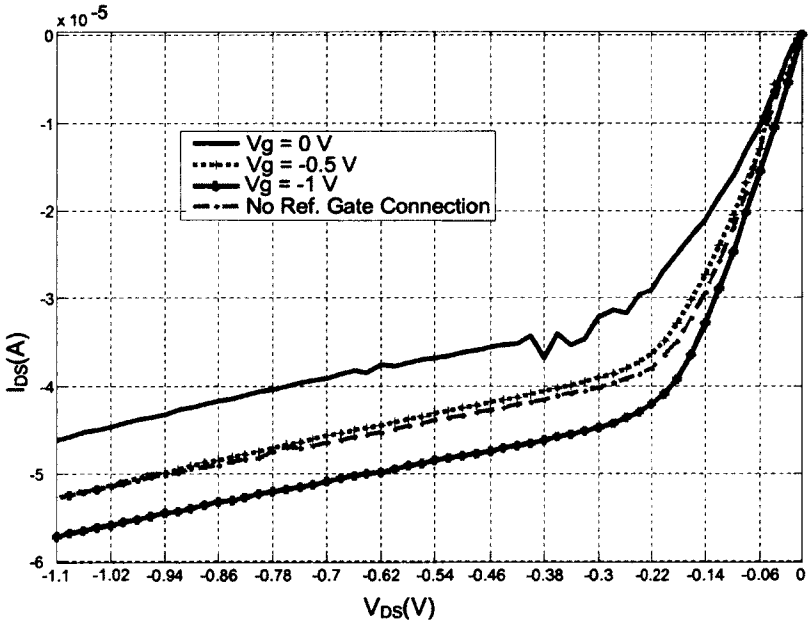

Figure 36- The effect of different reference MOSFET gate biasing on FGRADFET channel current

As it can be seen in Figure 36, the more negative the gate voltage of the reference MOSFET, the larger the current in the channel of the FGRADFET. This is due to the induced voltage on the neighboring FGRADFET gate due to close proximity to the gate of the reference MOSFET (note the layout in Figure 26), which may be due to polarization of the BPSG around the floating-gate.

4.3.2.3 Small Reference MOSFET Functionality Testing

In this section the reference MOSFET laid out in Figure 26 is tested for performance and functionality. Figure 37 shows the biasing of the reference MOSFET.

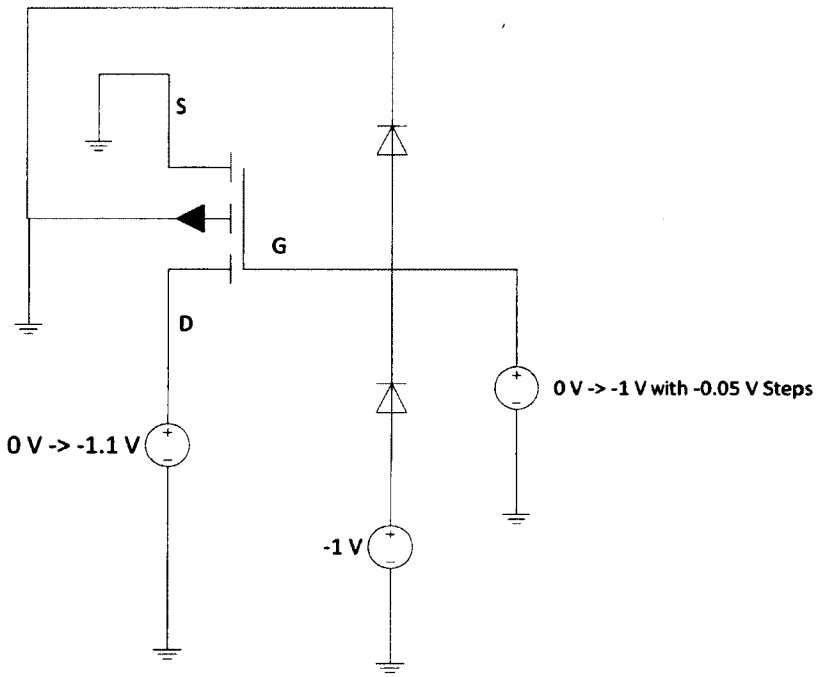

Figure 37- Biasing of the reference pMOS

This is the MOSFET with no gate extension. (It was previously noted that the gate-connected dual of the FGRADFET also has the same gate extension as the FGRADFET). Figure 38 shows the I-V curve with biasing conditions mentioned in Figure 37. The family of curves follows the expected behaviour of typical pMOS device in the 0.13 μm IBM process.

It should be noted that as illustrated in Figure 37, the double-diode protection is not forward-biased under any biasing condition within the range mentioned above; therefore, its connection to the n-well does not pose any problem to the proper operation of the circuit.

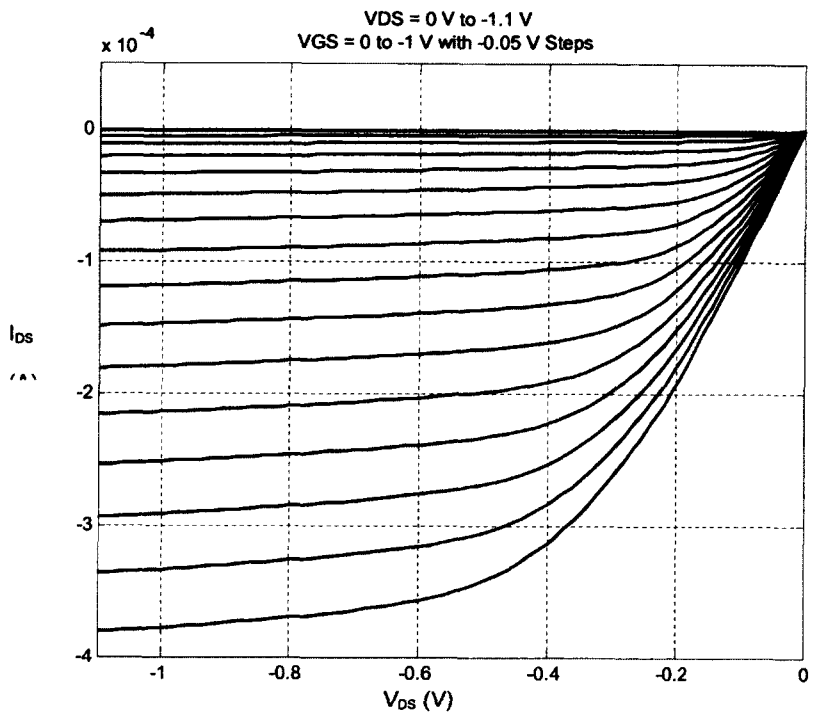

Figure 38- I-V characteristics of small reference MOSFET with p-sub connected

To further test the reference pMOS, the p-sub connection is disconnected; hence, the lower part of the double diode protection is left floating. Figure 39 shows the I-V curve results. Again, the expected behaviour is observed.

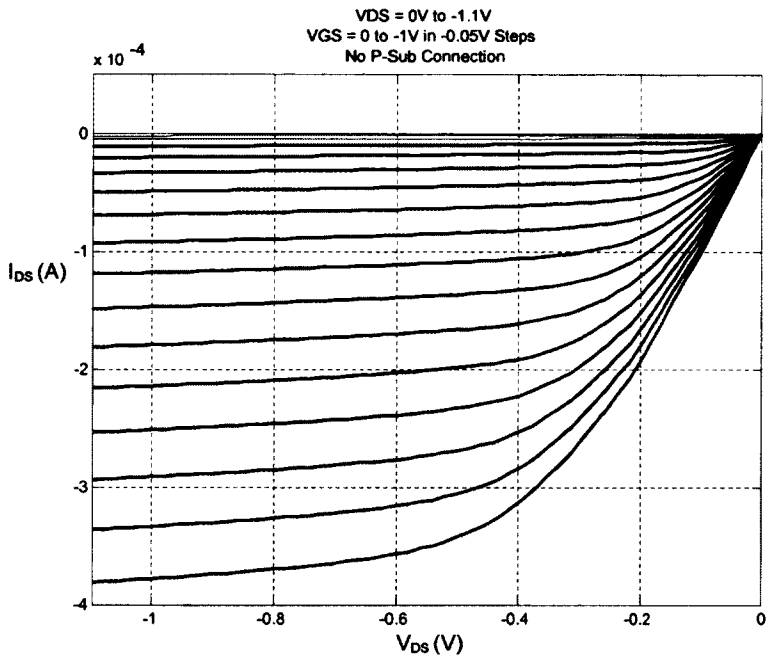

Figure 39- I-V characteristics of the reference MOSFET with no p-sub connection

It is seen that the double diode protection's presence does not change the I-V curve of the reference MOS when comparing Figure 38 and Figure 39.

4.3.2.4 Medium and Large Gate Extension FGRADFETs

As was mentioned in the earlier parts of section 4.3, there are three variations of gate extension laid out for the FGRADFET pairs. This section presents the medium (45 times the active region area) and large (90 times the active region area) extension designs. The testing procedure is the same for all the sample variations, and results are presented in Figure 40 and Figure 41 for the medium and large FGRADFETs, respectively. These plots show the same general I-V characteristics as seen for the small gate extension device, except for the scale of current and the presence of more noise. The plots contain results of four different chips to illustrate the chip-to-chip variation. This was a great challenge in the measurement process which is why some of the

measurements were repeated over and over and superposed to create an approximate (average) trend in curves (bold lines). It can also be observed that one of the four chips has FGRADFET devices that produce a much larger current than the other chips. This phenomenon can have no other explanation than it has more interface traps (or charge trapped near the interface of Si-SiO_2) compared to the other chips. Nonetheless, it is observed that current increases from the no-gate extension version to the largest of the extensions indicating that the larger the area, the greater the interface traps; and hence the stronger the channel created in the FGRADFET.

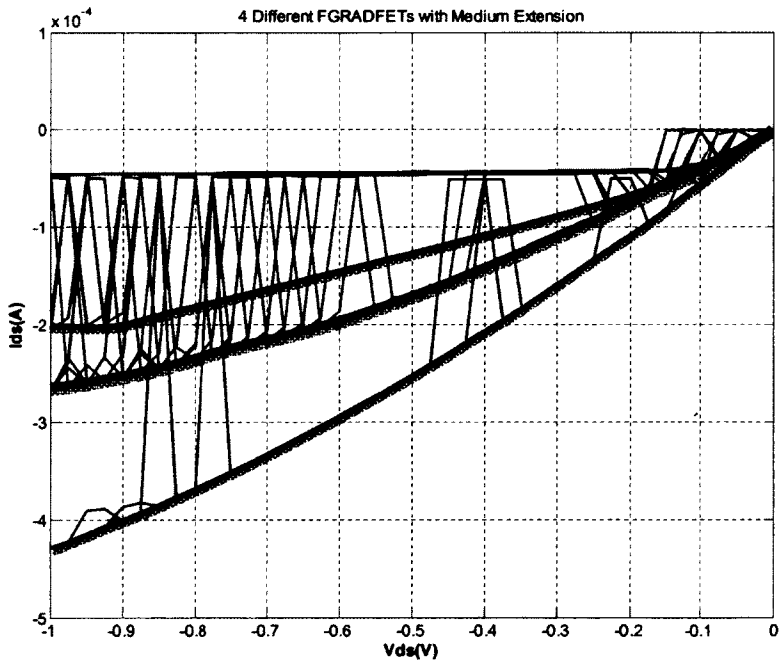

Figure 40- Medium FGRADFET with 45:1 ratio of gate extension area

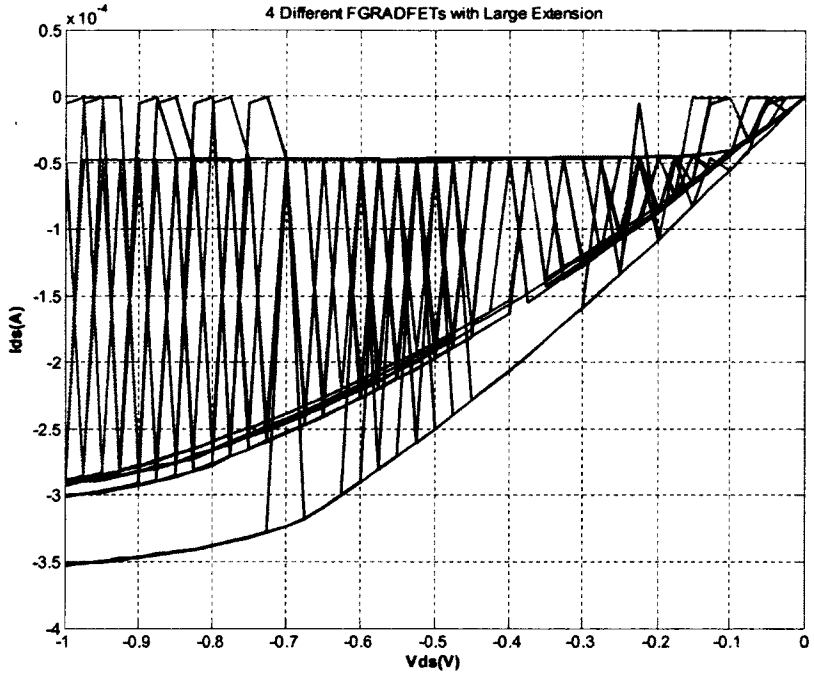

Figure 41- Large FGRADFET with 90:1 ratio of gate extension area

Overall, it seems like the spikes in the above figures are caused by environmental factors such as probe vibration around the test area caused by the probe chuck vacuum pump.

4.3.2.5 Medium and Large Gate Extension Reference MOSFETs

Figure 42 and Figure 43 illustrate the I-V curves of the medium and large reference MOSFETs, respectively. These plots are nearly identical to Figure 39 (the small reference MOSFET) indicating that there is no effect on the channel current caused by the gate extensions in reference MOSFETs.

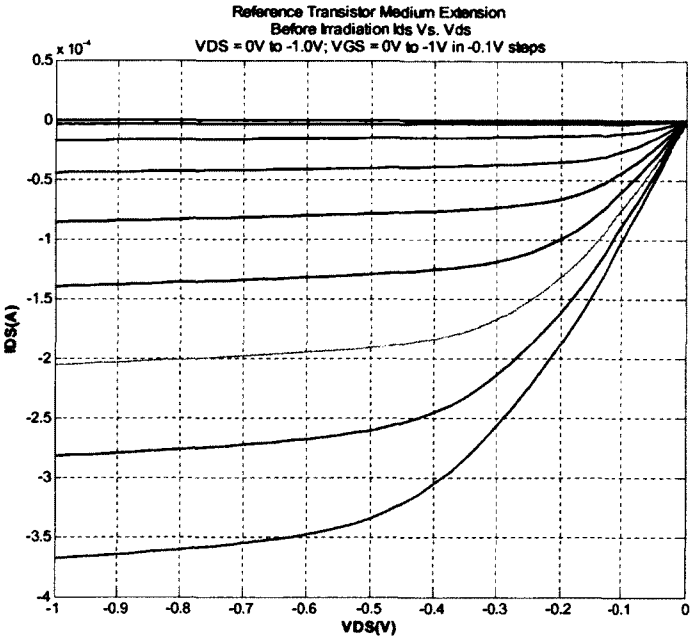

Figure 42- I-V characteristics of the medium gate extension reference MOSFET

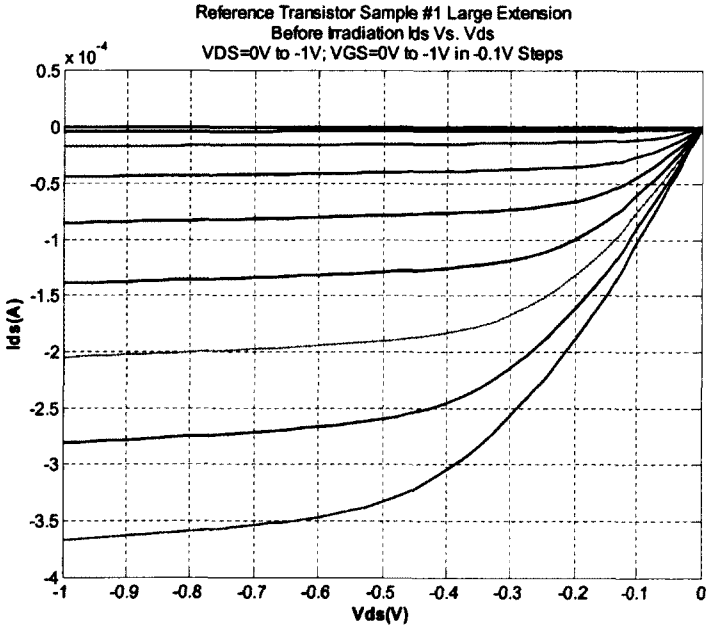

Figure 43- I-V characteristics of the large gate extension reference MOSFET

4.3.2.6 The Pre-charging Mechanism

As mentioned in the earlier sections, due to the absence of the second polysilicon layer to use as a pre-charger/control gate, another mechanism is to be used for putting charge on the floating-gate. What has been proposed by [**55**] is to use a pMOS which has its drain and source contacts shorted to each other and its gate connected to the floating-gate of the RADFET. This is depicted in Figure 34. Then a large gradual negative voltage starting at 0 V and increasing to ~ -15 V is applied to the drain/source contact where current starts flowing from the contact through the pre-charger's gate oxide to the floating-gate. At all times during the pre-charge process (shown in Figure 45-a), the FGRADFET is biased in a common-source configuration where the source and body contacts are grounded, and the drain is set to -0.1 V hence a small amount of current flows through the channel to allow monitoring of the charge level on the floating-gate. Once enough charge has tunneled through the floating-gate, a strong electric field induced by the mobile charge on the floating-gate causes an increase in I_{DS}. This process is continued until a desired amount of charge is placed on the gate prior to irradiation. Figure 44 illustrates the FGRADFET and pre-charging devices.

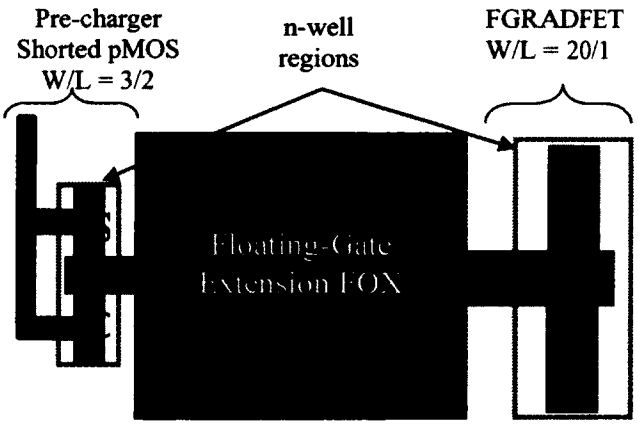

Figure 44- Simplified FGRADFET and pre-charging device

Several other methods were also employed in order to charge the FGRADFET as listed below:

1. Grounding all the FGRADFET and the pre-charger n-well terminals but the pre-charger terminal. Then increased the voltage on that terminal by ramping up the voltage in small (~ -20 mV) steps. The voltage was increased in the negative direction up to -9 V. -9 V is the maximum voltage that can be applied to the shorted pMOS drain/source before the gate oxide gets permanently damaged; hence, a short-circuit current flowing through the shorted pMOS and the drain (or source) of the RADFET (Figure 45-b)
2. Pulsing to the pre-charger device while other terminals are grounded. It is believed that pulsing high voltages up to -9 V is a better method of charging the floating-gate, since pulses would stress the oxide only for a short period of time as opposed to the ramp-up which constantly stresses the oxide. This method also provides a quantized method to pre-charge the gate to a certain voltage. This means that if one desires to set the floating-gate charge such that a certain voltage is achieved on the gate, it could be automated easily by knowing how many pulses of what pulse amplitude and duration needs to be applied to always achieve that voltage. But in the ramp-up voltage, there needs to be a constant – 0.1 V applied to the drain of the FGRADFET and it has to be constantly monitored (Figure 45-c).
3. The last method tried is the HCI (hot carrier injection). In this case, the RADFET is used to inject hot electrons onto the gate. The lateral electric field in the channel is increased well above normal operational limits while the gate potential is also kept high to induce a channel. Pinch-off is used to accelerate holes in the channel which

collide with the lattice and emit electrons which acquire enough energy to overcome the conduction band energy of the oxide and cross to the floating-gate. This method however causes degradation in RADFET operation by creating interface traps near the Si/SiO_2 interface at the drain side (Figure 45-d).

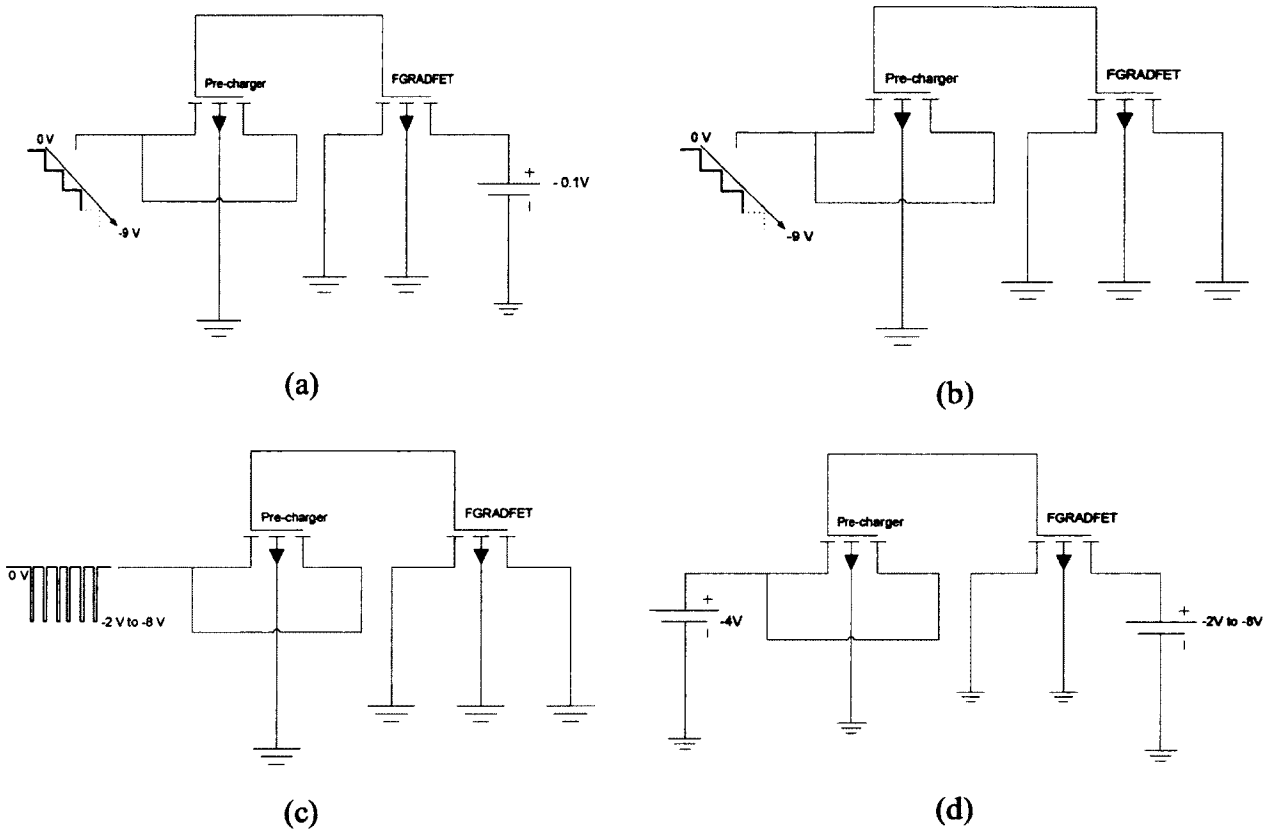

Figure 45- Different pre-charging methods
(a) Small negative steps applied to the pre-charger terminal while -0.1 V is applied to the FGRADFET drain
(b) Small negative steps applied to the pre-charger terminal while all other terminals are grounded
(c) Negative pulses applied to the pre-charger terminal while all other terminals are grounded
(d) Hot carrier injection method

What was not taken into account (since it was found out later on during the testing phase of the research) was the fact that the gate oxide of MOSFETs in 0.13 μm technology is far thinner (~3.15 nm) than that in the DALSA 0.8 μm process (~ 17 nm). This allows for significant direct tunneling currents through the oxide even at relatively

low electric fields [63]. For this reason the floating gate cannot hold charge for more than a second. However, this does not mean that the FGRADFET in this research is not capable of sensing the radiation. As will be seen in Chapter 5, sensitivity has been obtained even without the floating-gate being charged. There is a thick gate oxide variation of transistors available in the 0.13 μm IBM technology (which was discovered after the design submission for chip fabrication) which could be used to eliminate this direct tunneling issue in the future work.

4.3.3 Integrated FGRADFET (Dosimeter) Design

4.3.3.1 Overview

In this section, the complete FGRADFET dosimeter is introduced. The integrated FGRADFET is the same FGRADFET devices with the same pre-charging mechanism but they are embedded in a readout circuitry. This means that there is no need to directly read the channel current and compare it with the pre-irradiation one to determine how much it has changed with radiation exposure. Many different readout mechanisms have been introduced including the most significant designs by Dr. G. Tarr [1], [56]. The aim of this research has been to take a step further in the direction of making the FGRADFET's - introduced and explored in the last section- a system on a chip solution.

In integrated designs introduced by authors in the literature review, the sensitivity was defined by changes in the channel current under a certain bias with respect to the amount of radiation received. Hence, there was always a need for an extra step in changing this current into voltage. The extra step would cause an increase in area, measurement errors, and inaccuracy because of the offset thereby introduced, whereas the

design proposed in this research eliminates the need for an extra I-V conversion step; hence, not only does it address the above issues, but also lowers the power consumption of the readout circuit which is extremely important in bio-sensor applications.

4.3.3.2 Unity-Gain Amplifier and Dosimeter Design

The most significant characteristic of the integrated dosimeter in this design is that the sensing component is part of the readout. The readout circuit is a simple unity-gain 2-stage differential amplifier with pMOS input stage (shown in Figure 46), one input of which is the FGRADFET and the other being just a pMOS of the same W × L size but no floating-gate extension. The gate of the non-sensing pMOS (inverting input) is tied to the last stage's output, making it a unity-gain amplifier.

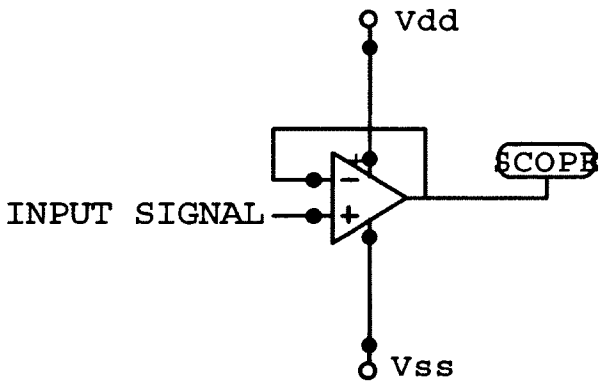

Figure 46- Standard unity-gain amplifier

A unity-gain amplifier – as the name suggests – has a gain of one, which means that its output voltage has a one-to-one ratio to its input voltage (± an offset voltage) that is applied to the gate of the non-inverting input of the op-amp.

In the case of the dosimeter, the induced voltage on the FGMOSFET as a result of mobile charge creates an output voltage. By the unity-gain op-amp's one-to-one ratio of input to output voltage, it can be deduced that the floating-gate voltage, which is created by the electrons placed on the gate by the pre-charging device, appears as the op-amp's output voltage.

Once irradiated, the injected electrons (placed on the floating-gate by the pre-charging process) recombine with holes created in the process of electron-hole pair generation due to irradiation in the gate oxide and the STI regions. This lowers the amount of charge on the floating-gate hence the current in the channel decreases, so this is reflected in the output of the op-amp as a change in the voltage. Most of the electrons generated as a result of the electron-hole pair generation process escape the oxide regions and recombine in the positive terminal of the MOSFET device. Some of them recombine with holes within the oxide regions.

Moreover, as explained in the theory, positive interface traps are also generated as a result of irradiation at the Si-SiO_2 interface. Positive interface traps interact with the channel, trapping holes, which decreases the mobility of the holes in the channel.

This also lowers the amount of current in the channel, which in turn changes the output voltage of the readout op-amp. The integrated FGRADFET and the simplified physical phenomena are illustrated in Figure 47.

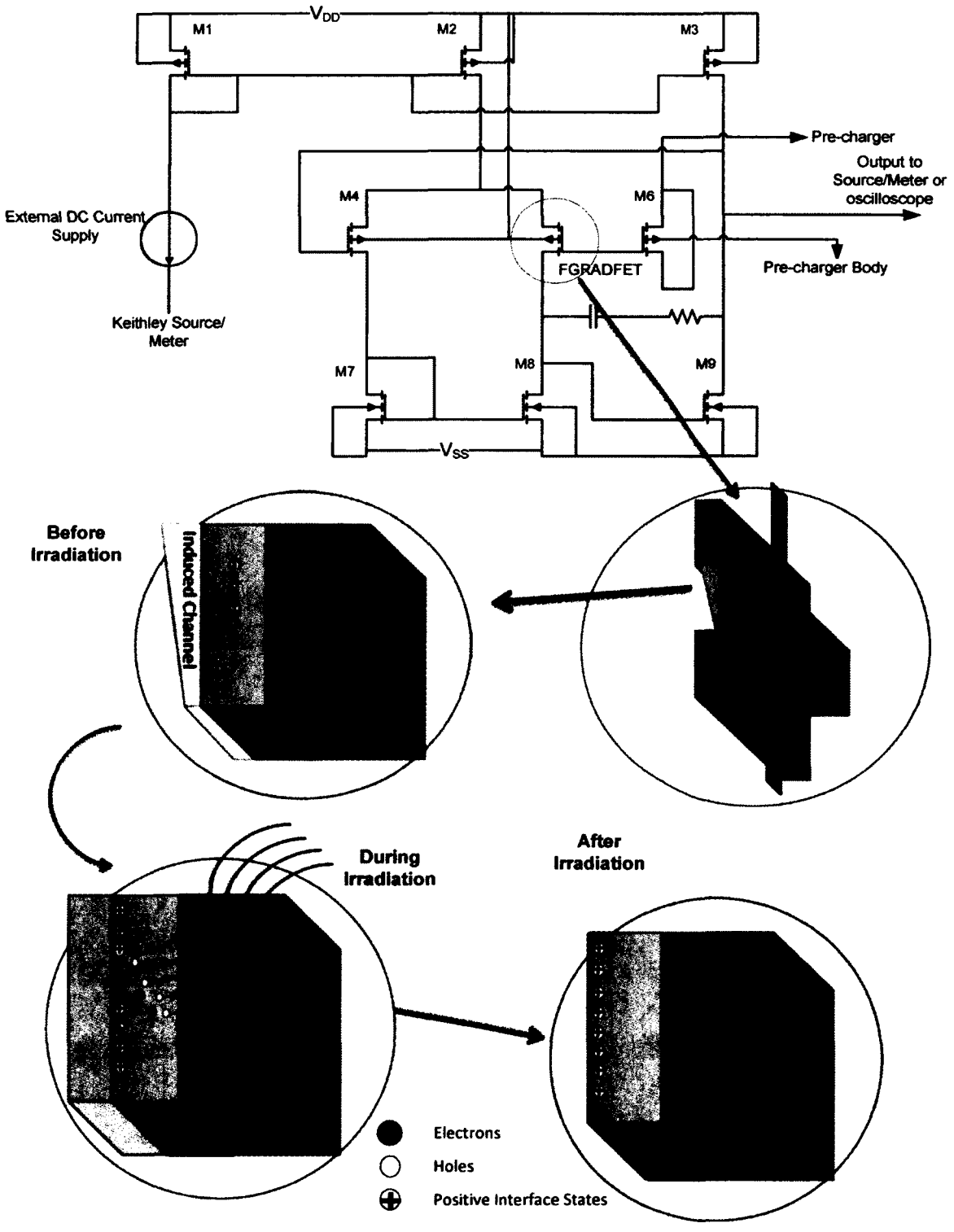

Figure 47- Integrated FGRADFET irradiation and the physical phenomena depicted

This design addresses the issue of noise and also temperature variations. Since the readout is a differential amplifier, the input stage of the op-amp differentially cancels out any common variations which affect both sides of the input. Having one side of the differential input as the sensor would mean that any temperature variation and common mode noise are minimized in the response of the sensor and the only effect it encounters is the effect of radiation on the floating-gate.

In previous research work done by Dr. M. Arsalan, to create a differential pair, the reference device is also floating-gate MOSFET which is also pre-charged to the same level as the floating-gate sensor. The only difference between the two is the use of gate extension for the sensor and eliminating the extension for the reference MOSFET to de-sensitize it. Nonetheless, this approach causes a small amount of radiation sensitivity happening in the reference device too which gets cancelled out by the action of the differential pair; hence losing some sensitivity. But in this proposed research the reference MOSFET is gate-connected; therefore, there is no need for pre-charging and there is no loss of sensitivity through common changes of threshold due to irradiation.

Also, in general, it is beneficial in terms of lower 1/f noise considerations to have the input stage of the diff-amp (differential amplifier) be pMOS transistors. This further emphasizes the benefits of using pMOS RADFET over nMOS ones, meaning not only do pMOS RADFETs have higher sensitivity, but also in terms of readout circuit design, they create less noise in the circuit output.

To add to the benefits of this design, process variations which cause issues such as offsets and performance changes are minimized via using fingered MOSFETs rather

than single large MOS devices for the input stage as well as other transistors in the circuit. This approach creates experimental test results which match simulations more closely. This approach has been proven to not adversely affect the sensitivity. Another consideration in the design is the use of an external current source for biasing the readout circuitry. There are three very important reasons why this was done:

1 This research aims to prove the feasibility of using 0.13 μm technology for radiation sensitivity; hence a bulk of the work which would be dedicated to designing the current mirror was instead directed to more detail analysis of the sensor itself. Hence time constraints in terms of fabrication deadline were satisfied.

2 Considering the level of expertise required to design a perfect current mirror, it would not make sense to include a current mirror in the integrated design just to later find out that the current mirror does not set the bias current correctly, and because of that the readout circuitry and as a consequence the entire sensing system does not function properly. This would have rendered the results of irradiation useless. Therefore, cautious decision was made to use an external current source.

3 The other very important conclusion which this research aims to draw is to study the effects of supply voltage changes on the sensitivity of the readout circuitry. Had a current mirror circuit been included in the design, the correct operation of the readout circuitry would only be possible only in the case of using 1.2 V (-1.2 V) supplies, and further study of "shrinking" the power supply would not be possible. Power supply reduction in readout circuitry is an important factor in trying to make wireless sensors with minimal power consumption for battery-operated and battery-less readout circuitry.

4.3.3.3 Dosimeter Layout

The sizes of the resistor and capacitors and transistors used in this design including the FGRADEFT and the pre-charger device are given in Table 1. The sizes below were calculated and simulated through general 2-stage differential operational amplifier design that can be found in most electronic design books such as Smith and Sedra [**64**] .

A point to consider regarding the size of the FGRADFET is that since the single FGRADFET and reference pairs were designed and laid out in the first stage of the design, keeping the size of the FGRADFET in the integrated design the same as that of the single device is crucial in that performance comparisons can be drawn from the two. Therefore, the readout circuitry's MOSFET sizes are calculated based on having an input differential stage with W/L = 20 μm / 1 μm.

Table 1- Integrated dosimeter component sizes

Component	M1	M2	M3	M4	FGRADFET	M7	M8	M9	M6	R	C	Gate Extension Area

Figure 48 shows the layout of the integrated dosimeter. The top section of Figure 47 and Figure 49 also provide the schematic and the fabricated chip, respectively. The blocks of the dosimeter variants and the readout circuit are marked for clarity.

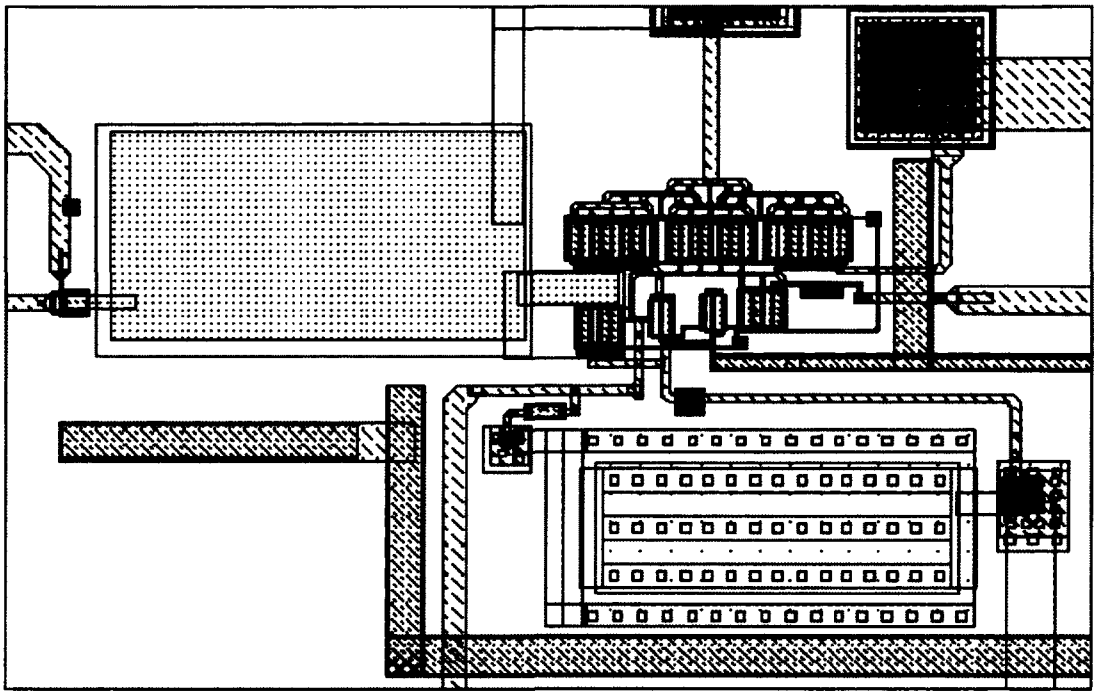

Figure 48- A sample layout of the integrated FGRADFET with 90:1 ratio of FG extension

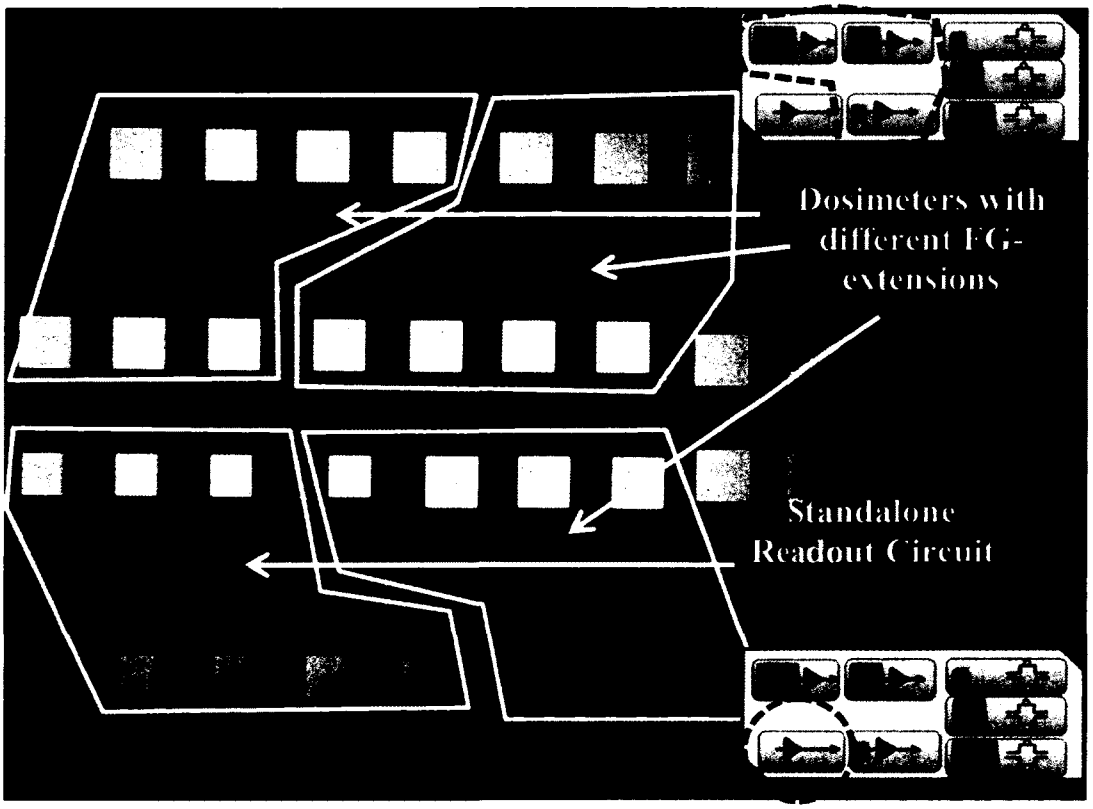

Figure 49- Photomicrograph of the dosimeters and the readout block. The encircled area of the "floor plan" corresponds to the microphotographed chip

It should be noted that the design and sizes of the integrated dosimeter are the same for all 3 variations, but the only parameter that changes is the area of the gate extension connected to the floating-gate.

4.3.3.4 Simulated Performance of Readout Circuit

The two stage amplifier has the design specifications shown in Table 2. These were chosen to provide stability (phase margin) of 65° and the required gain (55 dB) for adequate unity gain amplifier performance [**64**]. Also, Figure 50 illustrates the simulated gain and phase margin of the 2-stage operational amplifier. The 3-dB bandwidth is 52 kHz, which is well beyond the frequency needed for this application.

Table 2- Important design specifications of the 2-stage readout circuitry

Design Spec.	Gain	Phase Margin	V_{dd} (V_{ss})	Power Consumption	Unity-gain DC offset	-3dB Bandwidth	Current Source

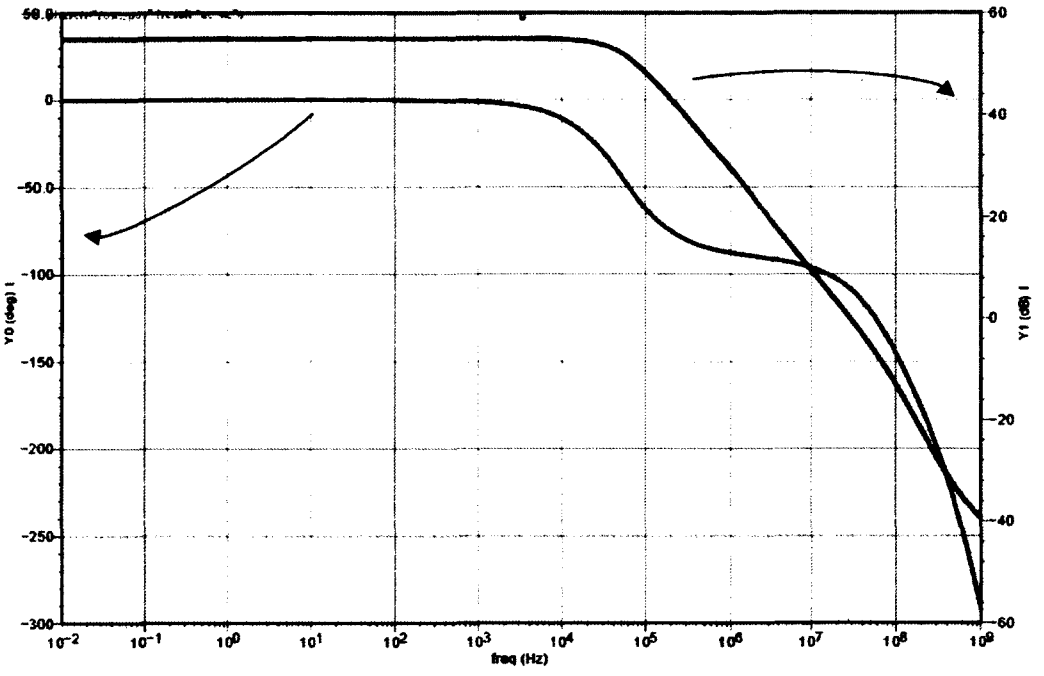

Figure 50- Gain and phase simulation of the readout circuitry

Table 2 and Figure 50 describe the 2-stage operational amplifier (the readout circuitry) where both sides of the differential input are regular gate-connected pMOS's with identical sizes.

4.3.4 Unity-Gain Readout Circuit Initial Testing

This section presents initial test results for the unity-gain readout circuit of the dosimeter, whereas the full dosimeter initial testing is presented in Chapter 5.

After the initial simulated performance validation of the op-amp, it is tied in a unity-gain configuration to verify that the output voltage indeed follows the non-inverting input voltage. The simulated and measured chip test results are shown in Figure 51 and Figure 52, respectively. Both figures match nearly perfectly, as is expected for such a

basic circuit. It should be noted that all 9 samples measured yield identical characteristics.

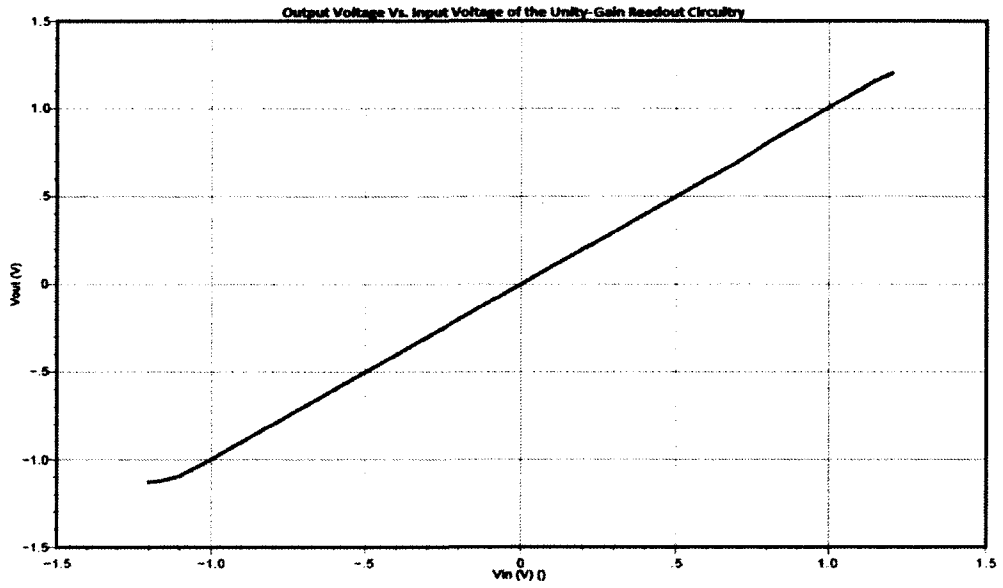

Figure 51- Simulated V_{out} vs. V_{in} plot of the unity-gain readout circuitry

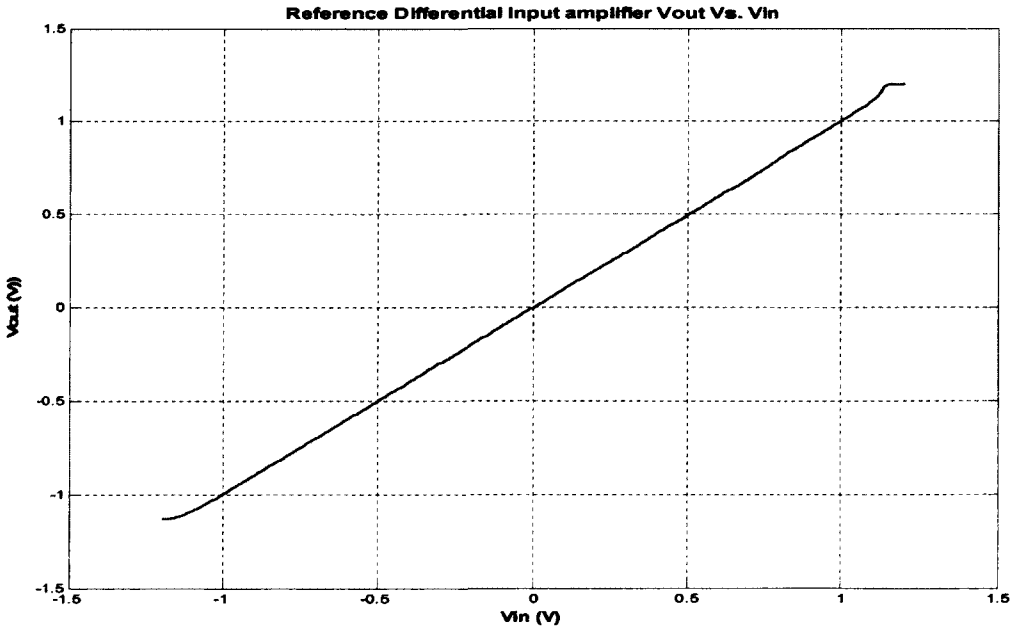

Figure 52- Measured V_{out} vs. V_{in} plot of the unity-gain readout circuitry from a sample readout circuitry (Not a FGRADFET sensor)

The measured data of the readout circuitry show an output voltage offset of +4 mV to +6 mV over the entire range of output voltage, with an offset of <1 mV near V_{in} = 0 V.

Figure 53 shows the plot of the ratio of measured output voltage points to the simulated ones to demonstrate more detailed information not seen in Figure 51and Figure 52. The spikes near the centre of Figure 53 are a result of dividing very small numerical values and are not indicative of any performance degradation around V_{in} = 0 V.

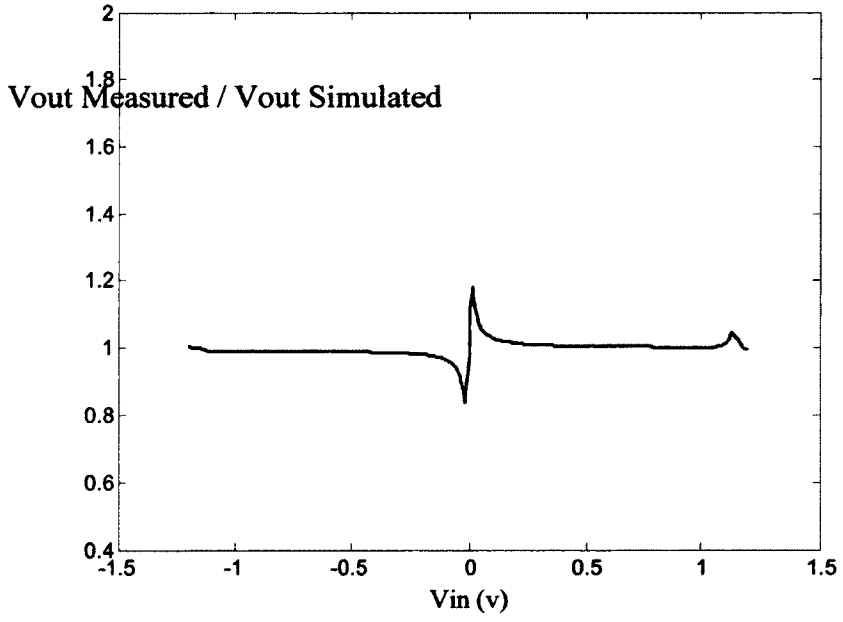

Figure 53- Ratio of measured readout circuit output voltage to simulated readout circuit output voltage

With the constant voltage offset measured in 9 samples of the chips, all integrated FGRADFET output voltages measured need to be subtracted from this offset to ensure that its effect has been eliminated before irradiation.

For the post irradiation measurements, the output value of the reference readout circuitry can be measured on a chip-by-chip case and then subtracted from the output of the integrated FGRADFETs.

4.4 ESD Protection Strategy

ESD protection is an important topic in chip design since their testing and handling may cause a flow of sudden and high current or voltage into one of the input or output terminals. ESD can also damage the chips while being handled in fabrication; therefore, many or all of the chips may be received already damaged and inoperable. To prevent such inevitable issues with fabrication, handling, and testing, it is necessary to design and place ESD protection components on chip. The two places on a chip that usually require ESD protection devices are the input gates – or generally any in/out terminals that share a connection to a gate – and power supply lines. The double-diode protection and the power clamp are the two ESD protection devices which are used throughout this design to serve this purpose, respectively. These devices were placed on the chip as per IBM's design kit recommendations.

Chapter 5 Irradiation Test Procedure and Results

5.1 Overview

Irradiation has been done twice at the National Research Council of Canada (NRC). A photo of the ^{60}Co irradiator machine is shown in Figure 54. The machine has a cylindrical chamber which has a 5.5 inches diameter and 7.5 inches of height.

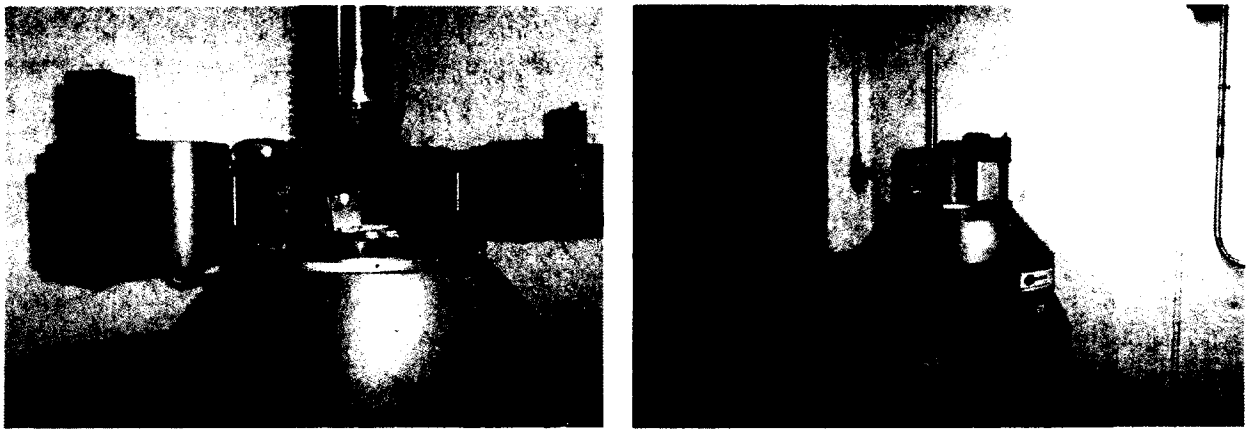

Figure 54- Irradiation machine at NRC

According to the laboratory instructor – Leslie Brown at the Institute for Biological Sciences at NRC – who is in charge of the irradiator, the calibration done in March 23rd 2007 indicated a dose rate of 64.9 Gy/hr. ^{60}Co has a half-life of 5.27 years which means that the dose rate has been decreased to 35.6 Gy/hr in the time range starting from the calibration date up to the irradiation date of October 14th 2011 [**65**]. Knowing the less sensitive nature of the samples in comparison to the previous research work, and the higher dose range applications of blood and surgical tools sterilization, and also knowing that the floating-gate RADFETs cannot be pre-charged, it was decided to irradiate the samples at a higher total dose to be able to observe a noticeable change in circuit

responses. At both irradiation occasions, the samples were left in the irradiator for 24 hours for a total dosage of 24 × 35.6= 854.4 Gy at room temperature.

There were some difficulties experienced during testing phase, as listed below:

- Long travel time to drop off the samples and bringing them back for testing: The concern is that transient post-irradiation effects, if any, are missed because of a ~2 hour time lapse before testing the samples.
- Long duration of the irradiation: since the irradiator has a low dose rate, the time to irradiate samples are long, making it difficult to test numerous samples and in shorter periods of time.
- Radiation pattern: the radiation exposure pattern within the chamber in which the samples are placed is not uniform. This may cause non-uniform radiation results in different chips depending on their physical position and orientation.

5.2 Irradiation Test Results

In this section, the irradiation test results are presented and discussed. This section is divided into three sub-sections:

1. Single FGRADFET and reference radiation test results;
2. Integrated FGRADFET radiation results;
3. Changes in sensitivity with respect to V_{DD}.

5.2.1 Single FGRADFET Radiation Test Results

In the first set of test samples taken for irradiation, there were 4 chips, numbered 1 to 4. Here, the results of irradiation for the FGRADFETs are presented. The results are illustrated in Figure 55, Figure 56, and Figure 57 for small, medium, and large gate extensions, respectively. In these figures, the "pre-irradiation" curves are those shown previously in the single FGRADFET initial testing section. Where there are a lot of spikes present due to probes' vibration caused by the vacuum pump, a solid line has been drawn to show the representative curve.

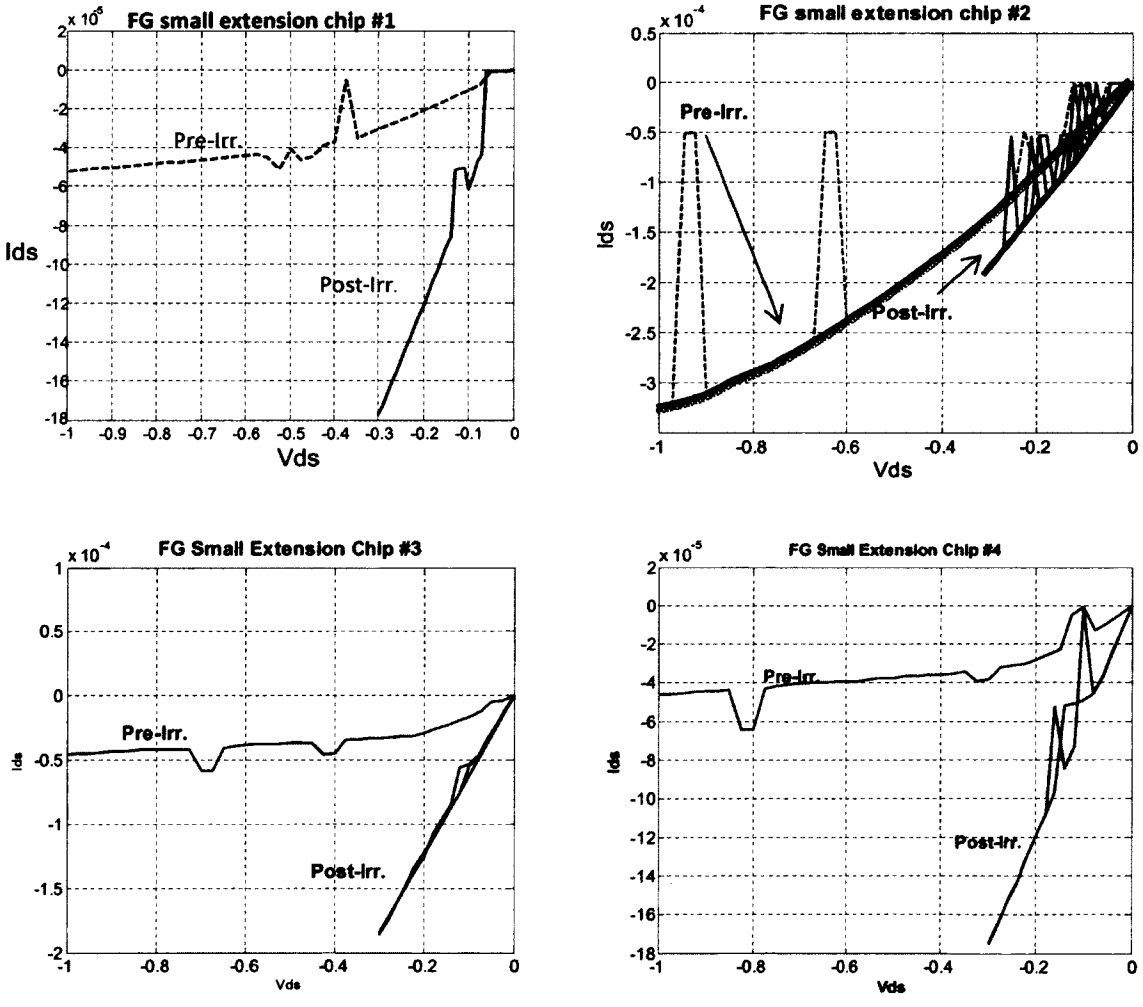

Figure 55- Small extension pre- and post-irradiation results of 4 samples

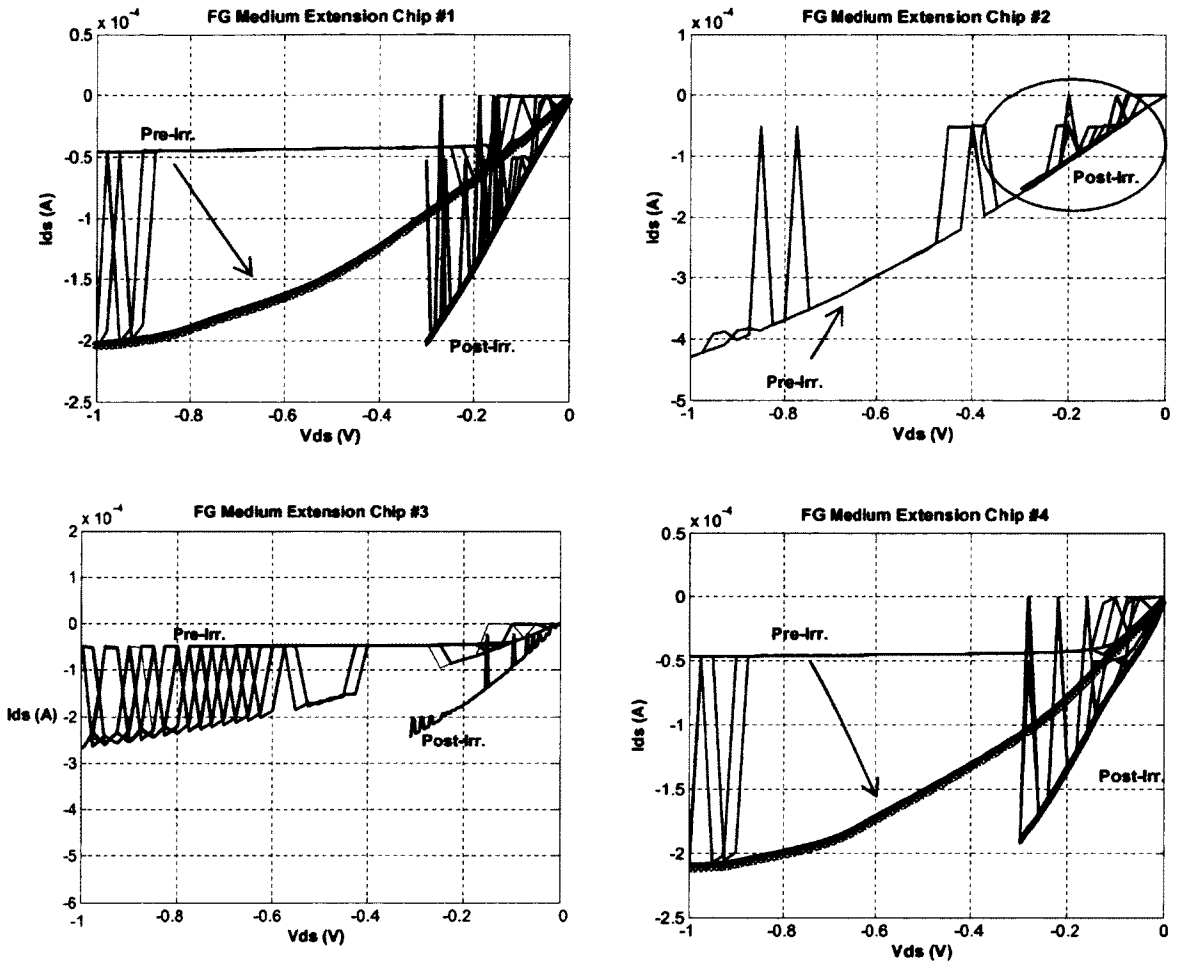

Figure 56- Medium extension pre- and post-irradiation results of 4 samples

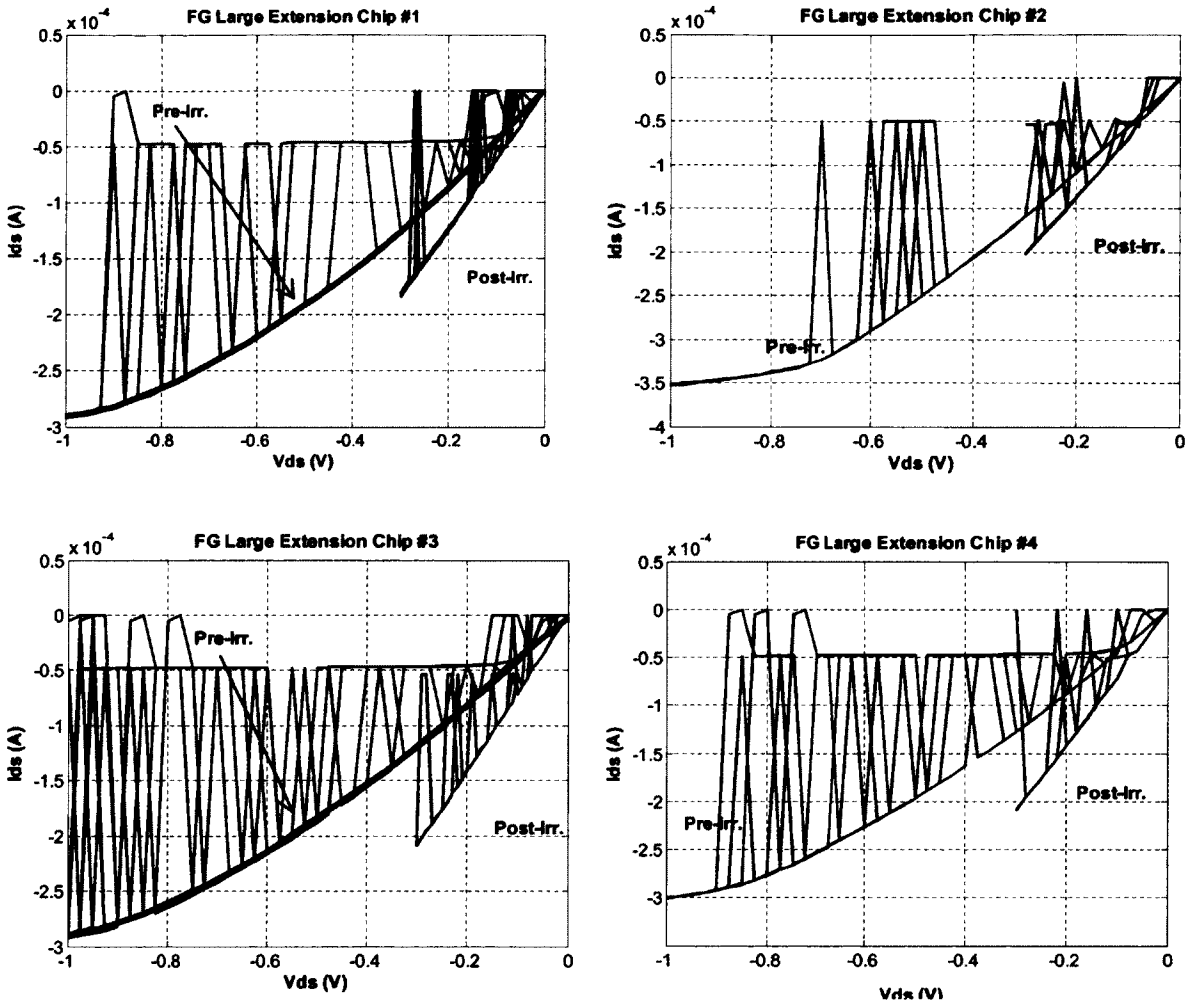

Figure 57- Large extension pre- and post-irradiation results of 4 samples

In the pre-irradiation V_{DS} vs. I_{DS} plots shown in the figures, the increase in current with respect to gate extension is observed which was also previously noted as well. This is due to the presence of interface states. Since the irradiated FGRADFETs show an increase in channel current, it is determined that the threshold voltage has decreased due to the creation of negatively charged interface states as opposed to previously believed positive interface states.

After the irradiation, almost all of the I_{DS} values reach ~ 2×10^{-4} A from their previous much lower current values at V_{DS} = - 0.3 V. This could be explained by the saturation in sensitivity in all devices after irradiation. The V_{DS} for post-irradiation testing was not swept to V_{DS} = -1 V because of possible strong electric field effects on interface states and bulk traps recombination.

There are a lot of spikes present on the curves for both pre- and post-irradiation plots; hence, it was decided to re-sweep each curve many times and overlap them to be able to create a trend. Manually taking an average of the many sweeps would create the same curves, but it would have taken away the spikes. The spikes could be induced by the function in the SPA tool which steps up the drain-source voltage, but it is not a consistent issue and is present sometime and not present at some other times. Another reason is the vibration of the probes on the contact pads (due to the probe chuck's vacuum pump) which creates these random spikes. This is a more realistic reason. Also, ambient interference could be a reason which induces spikes in the highly sensitive floating-gate.

5.2.2 Reference MOSFET Radiation Test Results

In this section, the reference MOSFETs are irradiated and the pre- and post-irradiation results are presented. In each pair of swept I_{DS} vs. V_{DS} curves, the upper curve is the pre-irradiation curve, and the lower curve is the one for post-irradiation. In this case, the channel current shows an increase. The plots for one chip sample in all three gate extension variations are shown in Figure 58. The changes in the channel current in the medium and large extension reference MOSFETs are almost the same, but that of the small extension shows less change implying a less sensitive device. The gate extension in the small extension device is almost non-existent; hence, there are fewer number of traps

created. Also the fact that the gate is connected to a potential makes the effect of the traps less pronounced compared to the changes in current in the floating-gate devices shown in Figure 55, Figure 56, and Figure 57.

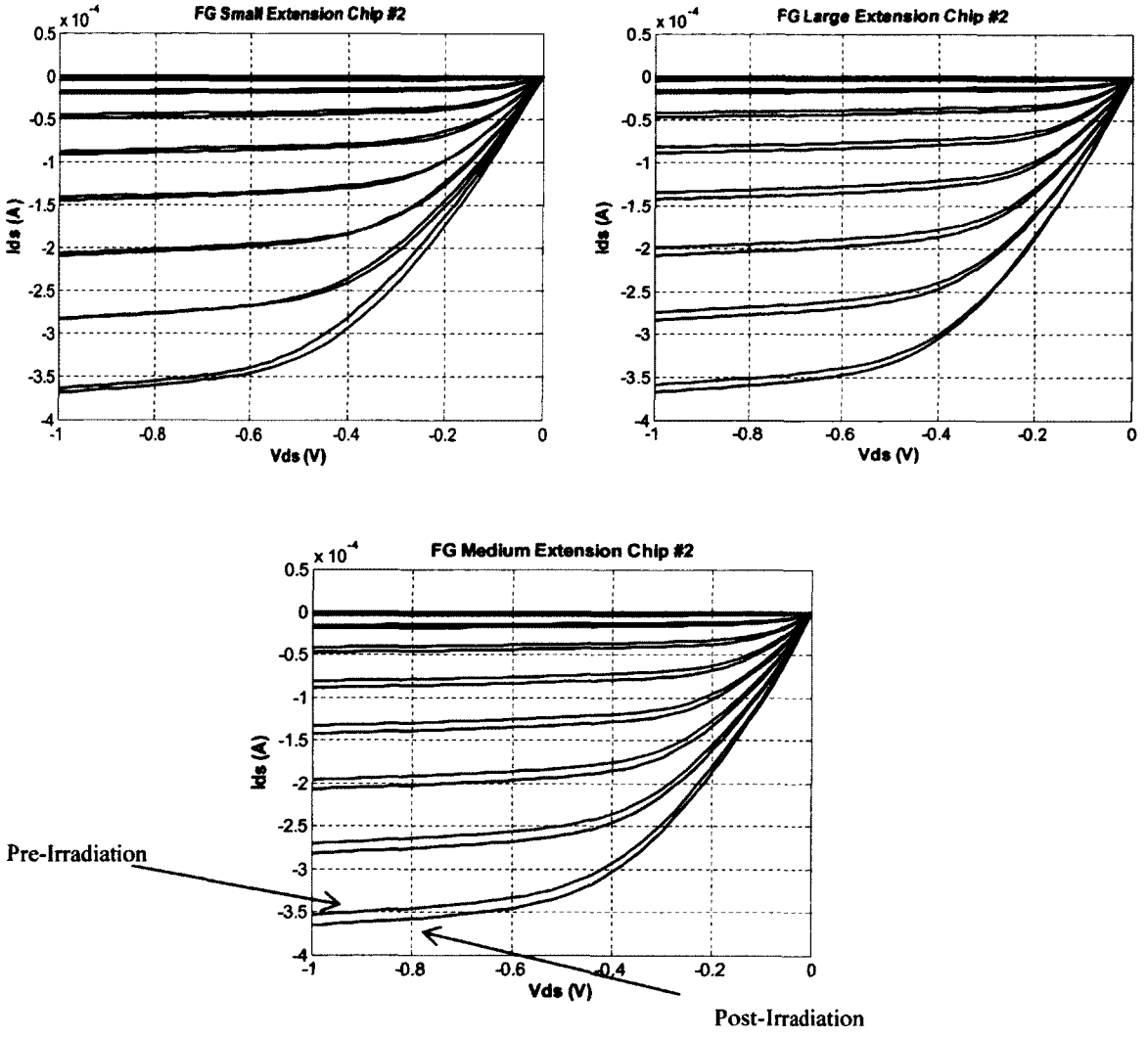

Figure 58- Reference MOSFET I_{DS} vs. V_{DS}

5.2.3 Integrated FGRADFET Irradiation

As was mentioned before, there are two sets of IC that were irradiated. The first irradiated set contained 4 chips on a test glass which was irradiated on October 14th 2011. The measured V_{out} values are presented in Table 3. The pre-irradiation values are taken on October 12th 2011. The integrated dosimeter is powered by $V_{DD} = -V_{SS} = 1.2$ V and the external current source supplies -100 μA.

Table 3- Pre- and post-irradiation output voltages of the first set of samples

		Sample #1 V_{Out} (V)		Sample #2 V_{Out} (V)		Sample #3 V_{Out} (V)		Sample #4 V_{Out} (V)	
Gate Extension Size	Small	0.272	0.019	0.172	0.127	0.261	0.133	0.295	0.055
	Large	0.335	-0.0005	0.245	0.181	0.189	0.0295	0.289	0.007

To observe the output voltage behaviour over time, the output voltage of the above 4 samples were taken during a period of time. Figure 59 shows the trend of this behaviour. In most cases, rebound of output voltage is observed which can be attributed to interface and bulk traps being recombined and the BPSG relaxation as Dr. G. Tarr explains in [1].

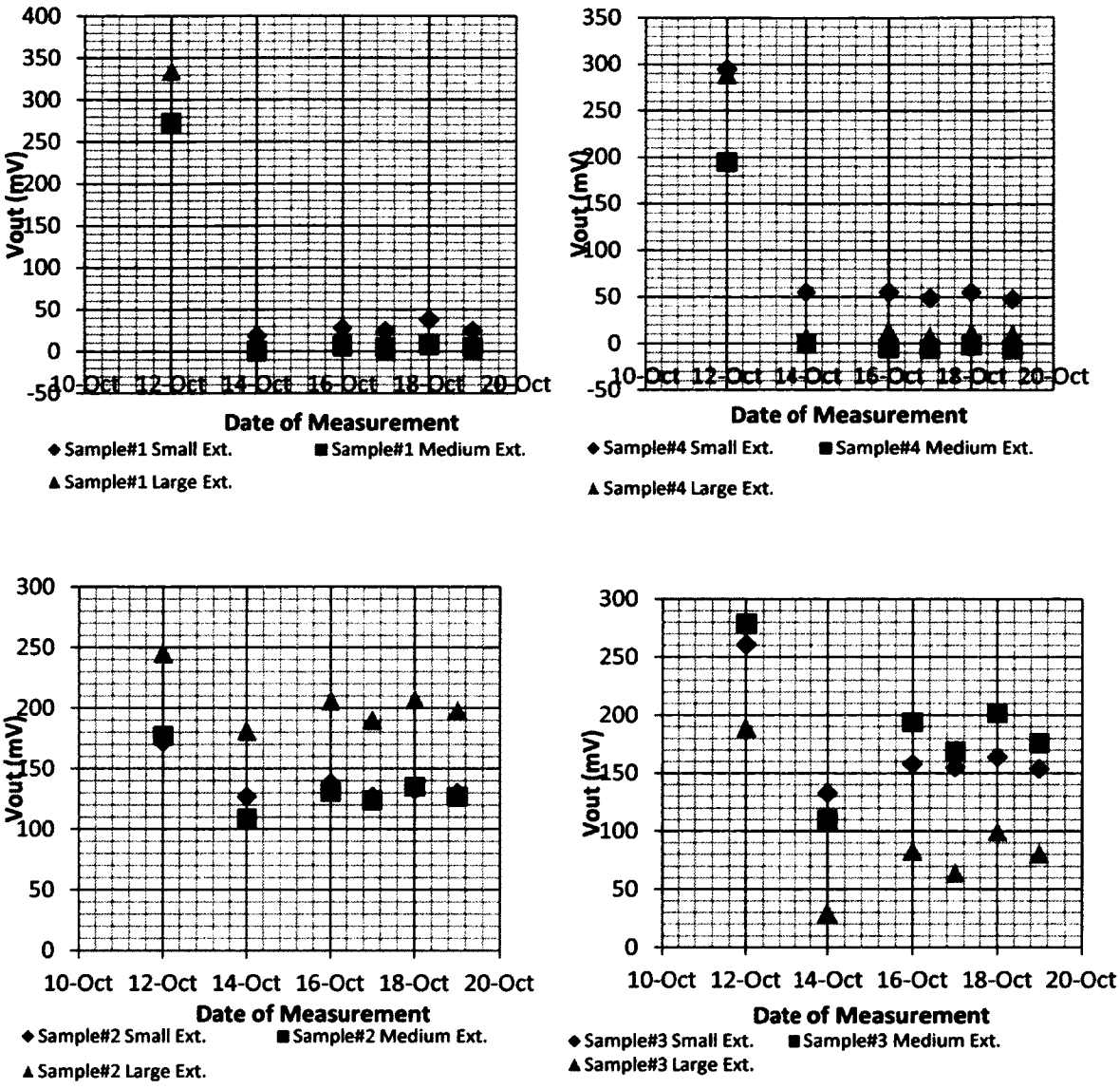

Figure 59- Plots of pre- vs. post-irradiation output voltage measurements of the 4 dosimeter samples

An important fact to note is that in most cases measured, including three of the four plots above, the integrated FGRADFETs with small and medium gate extensions follow closely and generally have a lower sensitivity to irradiation, whereas in the lower left plot, the integrated dosimeter with the large gate extension shows less sensitivity than the ones with the small and medium extensions. That plot particularly shows a lower sensitivity to irradiation overall, which leads us to believe that unless the floating-gates

can be pre-charged, the sensitivity of the dosimeters would vary. This is also observed in results of the second round of irradiation done on a new set of chips shown in Figure 60.

The second set included the already irradiated first set plus another test glass containing 5 chips which were not irradiated previously. The second irradiation testing was done on November 14th 2011 with the same amount of dosage. The reason for re-irradiating the first set was to understand whether the integrated circuits fabricated can withstand a total ionizing dose of ~1710 Gy or the circuit would be damaged. The results of the second round of irradiation are presented in Table 4.

Table 4- Output voltage changes of dosimeters for second round of irradiation performed on November 14th 2011

	27-Oct			03-Nov			15-Nov			16-Nov			22-Nov			02-Dec		
	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L
2	134	131	200	---	---	---	---	---	---	---	-12	44	77	30	100	80	53	123
4	50	-6	7.7	---	---	---	---	---	---	---	-10	6	37	-9	18	41	4	9
10	163	234	254	166	233	251	101	130	138	120	136	154	124	174	184	135	184	202
12	200	261	258	212	260	254	119	92	60	124	140	94	150	169	150	153	186	168

Due to probe issues which were not noticed while performing measurements, the data gathered for the first 4 chips in some pre- and post-irradiation stages were not valid, hence the results were not complete. But the valid data recorded by later measurements (as shown in 16-Nov, 22-Nov, and 02-Dec in Table 4) show that the chips already irradiated once, have a much lower sensitivity to irradiation. In other words, they are

saturated, and interface traps have built up so much that the dosimeters have lost their linearity. Another point is that no matter how much dosage the irradiated chips have been exposed to, the output voltage does not go lower than 0 V. This fact means that the range of operation of the integrated dosimeter is positive unless the floating-gate can be pre-charged to a specific negative voltage. It could be explained by the positive bias applied to the drain and source of the FGRADFET in the readout circuit. A fraction of this positive voltage appears on the FG as a result of capacitive coupling and capacitive voltage division. Figure 60 depicts the radiation results presented in Table 4 for better clarity.

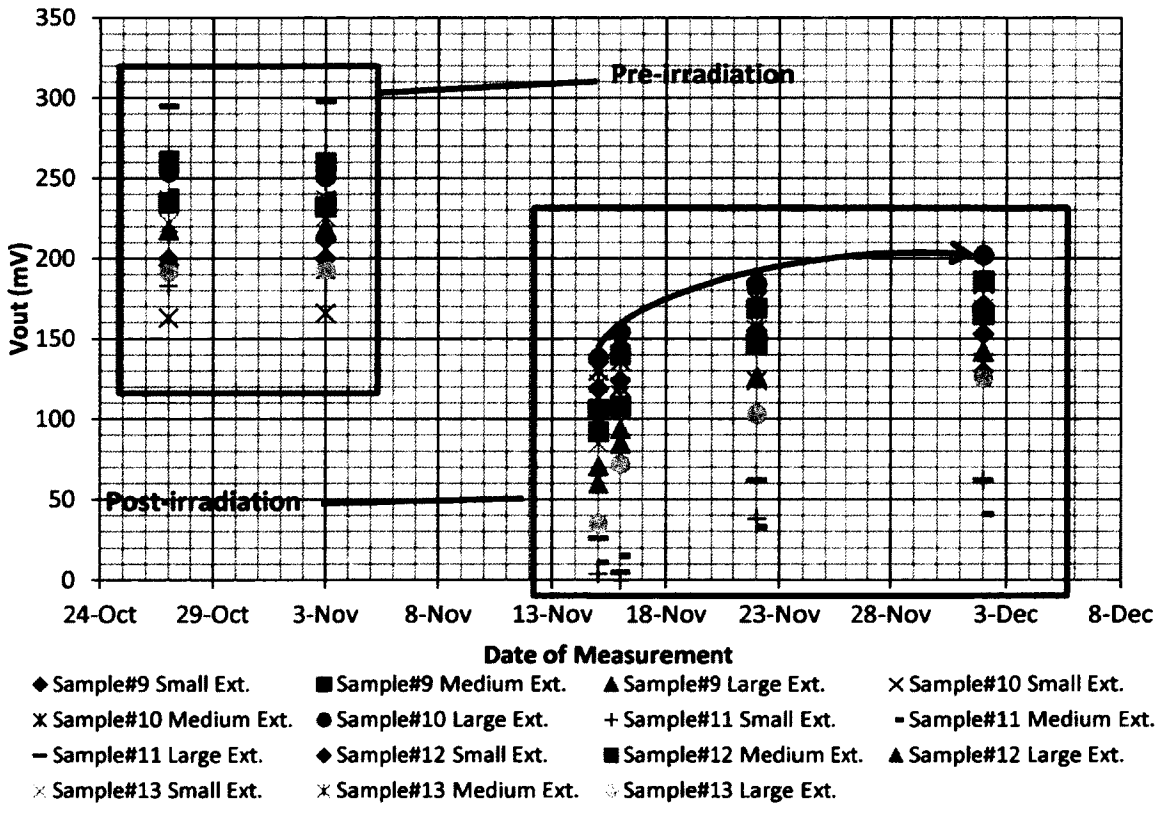

Figure 60- Pre- and post-irradiation output voltage results of 5 samples not previously irradiated

An important point to consider in Figure 60 is the rebound (bounce back) of the output voltage within days after irradiation. This is most likely a result of the interface states and bulk traps being recombined at room temperature (annealed).

In this figure, the output voltages of different samples vary a lot for both before and after irradiation. The wide variation is most likely a result of not being able to pre-charge the floating-gates. If they could have been pre-charged, then all of them would have at least the same output voltage before irradiation. Then their variations in response to irradiation, if any, would be a result of fabrication process variations, and radiation exposure inconsistency in exposure environment.

Figure 61 shows the simulation plot of the output vs. input voltage of the unity-gain readout circuitry (which does not contain any sensing part) along with the current changes in the non-inverting differential input branch. This plot creates a link between the radiation results presented in Figure 55, Figure 56, and Figure 57 and the post-irradiation test result illustrated in Figure 60. The branch current could not be measured since there is no means to separate it from the total current flowing through the entire integrated circuit. As is illustrated in the measurement plots of single FGRADFETs, the channel current increases after irradiation. In the dosimeters, the output voltage decreases after irradiation. If one of the output voltages is taken as an example, a 5 μA increase in current interprets to an output voltage decrease of 250 mV, due to irradiation.

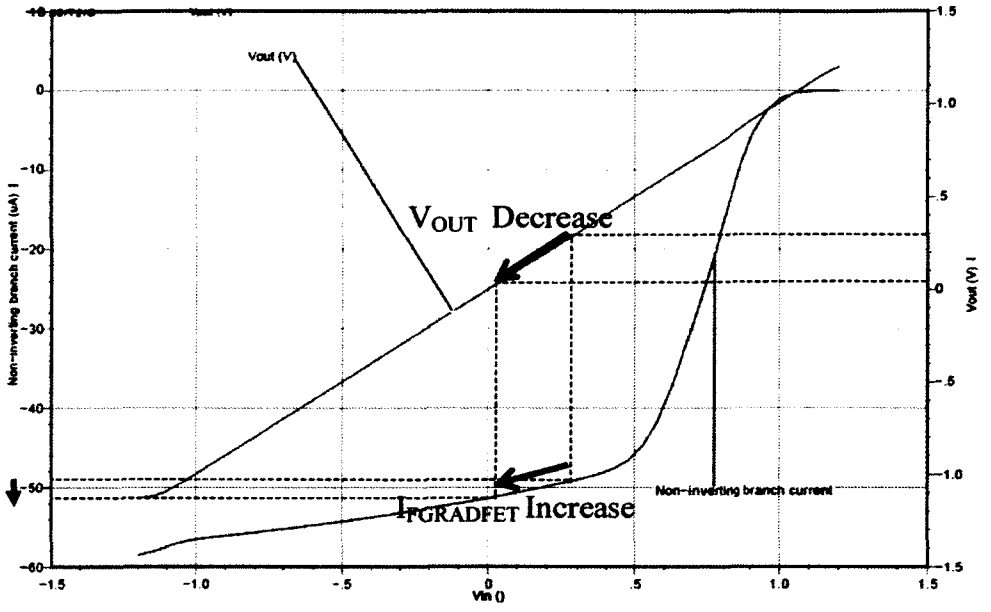

Figure 61- Changes in V_{out} as a result of changes in non-inverting branch current of readout circuit (simulated)

Figure 62 shows the measured V_{out} vs. V_{in} of the readout circuitry after irradiation. Here, the operation of the readout circuitry is examined under irradiation. As per the plot of 4 different samples below, the operation characteristics of the unity-gain readout circuitry such as linearity or gain do not change under irradiation. The only minimal change is the output offset of 8 mV across the tested samples. The maximum negative shift observed is -6 mV, and the maximum positive shift observed is +2 mV. Hence, output voltage shifts recorded after irradiation in Figure 60 are not due to the influence of radiation on readout circuitry, but are due solely to the FGRADFET embedded into the readout circuitry.

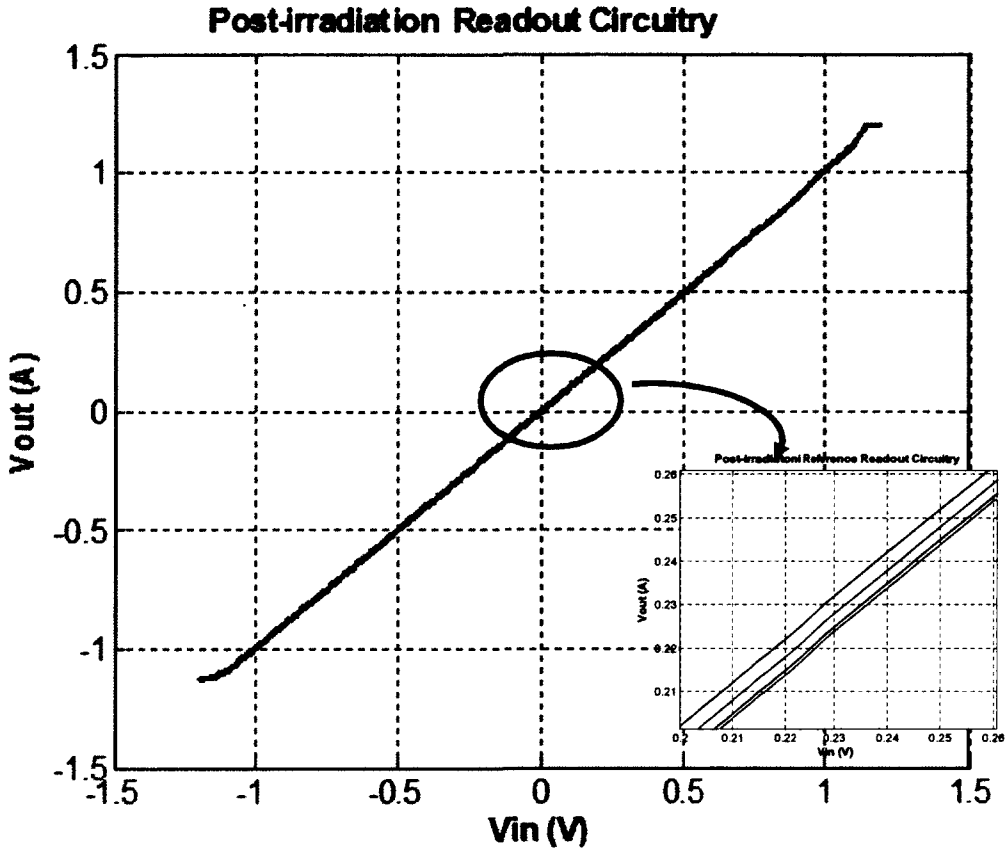

Figure 62- There is a maximum of 8 mV offset voltage observed between post-irradiated readout circuits' output voltages

5.2.4 Changes of V_{out} with Power Supplies V_{DD} (V_{SS})

One of the aspects of designing the integrated dosimeter is to investigate the feasibility of operating the sensor (readout + FGRADFET) under lower than nominal 1.2 V and still maintain the sensitivity. To fulfill this need, the integrated dosimeter's output is measured against changes in the supply voltages. Aside from this point, the floating-gate is capacitively coupled to the drain and source diffusions and its voltage takes effect from the voltages applied to these two areas. Figure 63 illustrates this point. This fact can only be simulated since in practice, there is no means of touching the floating-gate by a probe.

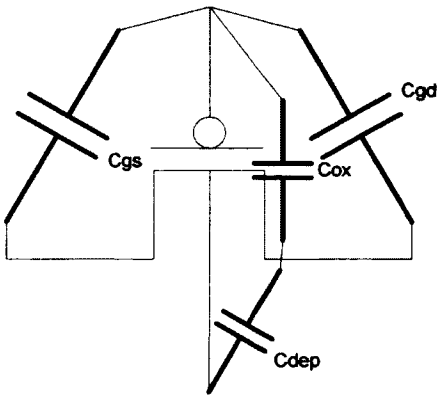

Figure 63- Capacitive coupling of the floating-gate to the body and source and drain diffusions

In the simulation environment, there is no need to place parasitic or coupling capacitors which are shown in Figure 63, since they are already taken into account automatically. The simulation result of an FGRADFET is presented in Figure 64. The gate voltage changes with the change in V_{DS} even though there is no electrical connection between the two. The larger the drain-source voltage, the larger the voltage is going to be on the floating-gate. This change in the floating-gate voltage causes a change in the depletion capacitor "C_{dep}" which causes a change in channel current. This chain effect is difficult to calculate but can be simulated. Therefore, it is desirable to keep V_{DS} as low as possible to eliminate this adverse effect. However, this effect does not seem to interfere with radiation sensitivity of the FGRADFET since changes in V_{out} as a result of irradiation is a relative measure.

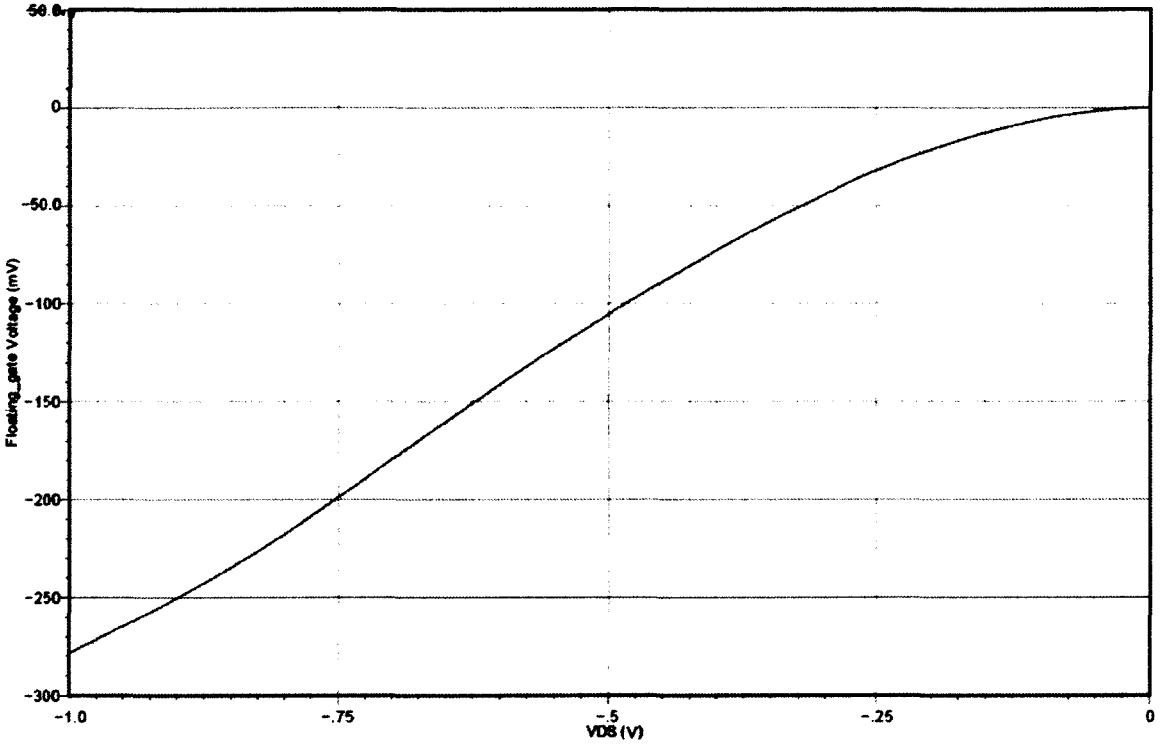

Figure 64- Simulated plot of V_{FG} vs. V_{DS}

As is shown in Figure 65, change in supply voltages causes change in V_{out} of the dosimeter. As V_{DD} ($-V_{SS}$) is scaled from 0.6 V to 1.2 V, V_{out} changes as well. The change is not linear since as explained in the last paragraph, the effect of changing V_{DS} causes non-linear capacitance and current changes in the FGRADFET. Figure 65 shows two samples of pre- and post-irradiated integrated dosimeters. In general, it can be concluded that operating the readout circuitry at biases lower than 1.2 V but higher than ~ 0.7 V does not jeopardize sensitivity.

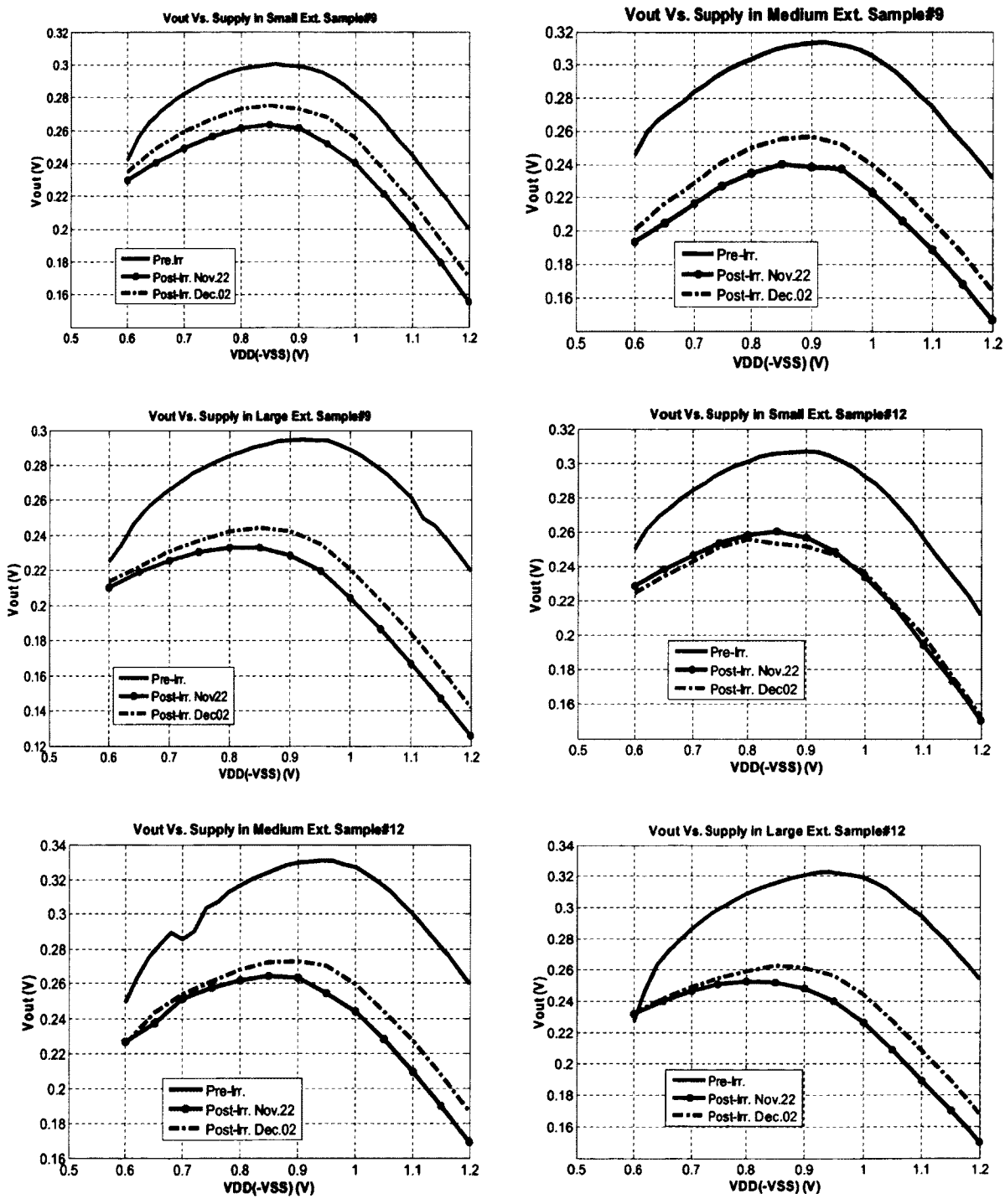

Figure 65- Changes of the output voltage of the integrated dosimeter chips with changing the power supply voltages which causes a change in drain-source voltage of the FGRADFET

It should be noted that lowering voltage supplies to 0.6 V keeps all the transistors in the readout circuitry in saturation. Decreasing it below 0.6 V causes the readout circuitry to fail since some of the transistors leave saturation.

5.2.5 Chapter Summary

This chapter introduced the testing environment (NRC irradiator machine). It also dealt with the irradiation of all variations of the FGRADFETs and their corresponding reference MOSFETs. Then, the pre- and post-irradiation results of the readout circuitry and the dosimeters were presented. Also, the sensitivity with respect to power supply range was discussed.

A maximum sensitivity of 0.4 mV/Gy was recorded for the dosimeters which was expected of such thin oxide devices. A power consumption of 753 μW at V_{DD} (V_{SS}) of 1.2 V (-1.2 V) was observed. At lower V_{DD} (V_{SS}) of 0.6 V (-0.6 V) a power consumption of 376.8 μW was recorded.

It is believed that if the dosimeters were irradiated with ionizing radiation in shorter than 24-hour intervals of time, sensitivities much higher than this would be reached since transistors could have been irradiated past their saturation point where they do not detect radiation.

Chapter 6 Conclusions and Future Work

This chapter summarizes the research work and the contributions of this thesis and proposes future work which will help researchers to advance the art of FG dosimeters and will also pave the way for future System-on-Chip wireless dosimeters.

6.1 Conclusions

Following a comprehensive review of radiation dosimeters, a novel floating-gate dosimeter architecture was proposed in chapters 2 and 4, and an extensive amount of theoretical background and analysis were presented. Floating gate MOSFET dosimeters had not been previously reported in advanced, thin gate oxide commercial CMOS technologies such as the 0.13 μm IBM technology used here. The new design developed in Chapter 4 and validated in Chapter 5, is the first of its kind that proves the feasibility of such technology for ionizing radiation applications.

Specifically, a chip with dimensions of 2 mm × 1 mm was designed and fabricated which contains three different parts:

1. Three pairs of FGRADFETs and reference transistors of identical active regions and gate extensions. These devices allowed measurement of the FGRADFETs' physical and electrical characteristics. The pair helped eliminate common variables such as temperature, light sensitivity, and environment noise. These variables adversely affect the performance of the FGRADFETs.
2. A fully differential readout circuitry which is a unity-gain amplifier. This block did not have any dosimeter attached to it. The purpose of the stand-alone readout circuitry was to confirm the correct operation of the circuit, measurement of

power consumption, and output voltage offset. The output voltage offset was measured to be 4 mV in unity-gain configuration.

3. A novel integrated FG dosimeter. This block integrated (embedded) the FGRADFET into the readout circuitry instead of connecting it to the readout circuitry via an intermediate circuit block. In this work, the output voltage of the readout circuitry was the FG radiation sensor's gate voltage. This method eliminated the need for converting the current in the channel of the device into voltage before it was readout and compared with its pre-irradiation value. The fully differential readout circuitry also minimized temperature and process variations, as well as induced noise on the device by surrounding electronic components.

A grounded metal-8 shielding component was placed on the floating-gate and gate extension provided extra protection against ambient light and electro-magnetic noise.

A comprehensive testing procedure which covered the operation of the single and integrated RADFETs was presented in Chapter 4 and 5. Many different test cases were introduced and implemented to fulfill the objectives of this thesis.

A maximum sensitivity of 0.4 mV/Gy was recorded in the integrated dosimeters which is expected of such thin oxide devices. A minimum power consumption of 376.8-μW was observed for the dosimeters as compared to the design in [2] with 2 mW of power consumption. It is believed that if the dosimeters were irradiated with ionizing radiation in shorter than 24-hour intervals of time, sensitivities much higher than this

would be reached since transistors could have been irradiated past their saturation point where they do not detect radiation.

6.2 Proposed Future Work

To continue the work presented in this thesis, the following research directions are proposed:

1. Investigating the reasons for the generation of negative interface states observed in the post-irradiation testing as opposed to previously believed positive interface traps.
2. Performing more refined testing of the existing chips, such as:
   2.1. Testing the dosimeter for the pre- and post-irradiation performance variations as a result of temperature change;
   2.2. Irradiating the chips using smaller dosages and shorter time durations;
   2.3. Irradiating the chips using different sources such as X-ray or ^{137}Cs.
3. The use of thicker gate oxide transistors available in 0.13 μm technology package is recommended to eliminate the issue of charge leakage from the pre-charged floating-gate. The gate oxide of such transistors has 6.15 nm of thickness.
4. For better understanding of the physical behavior of the floating-gate devices, more expertise with using available simulation tools such as Sentaurus is needed. It is also necessary to introduce and explore different methods to model the environmental effects such as optical and thermal sensitivity, as well as noise vulnerability.
5. At the current stage of research on the modern ultra-thin gate oxide processes such as 0.13 μm, only medium to high ranges of ionizing radiation dosage can be detected, but it is desirable to expand their application into different ranges of radiation sensitivity. For example, on the lower end of the spectrum, such as in the blood

irradiation process, radiation dosage of up to 55 Gy is used; and on the higher end, such as in sterilization of packaged food and surgical tools, kGy range of radiation is used. A future potential research ground is to use photodiodes to create a bias on the floating-gate during irradiation to further increase sensitivity. The photodiodes create a bias across them once illuminated; hence this property can be used to apply a positive or negative bias on the FGRADFET gate during irradiation. This configuration would be useful for both a floating-gate and a non-floating-gate variant of the integrated dosimeter.

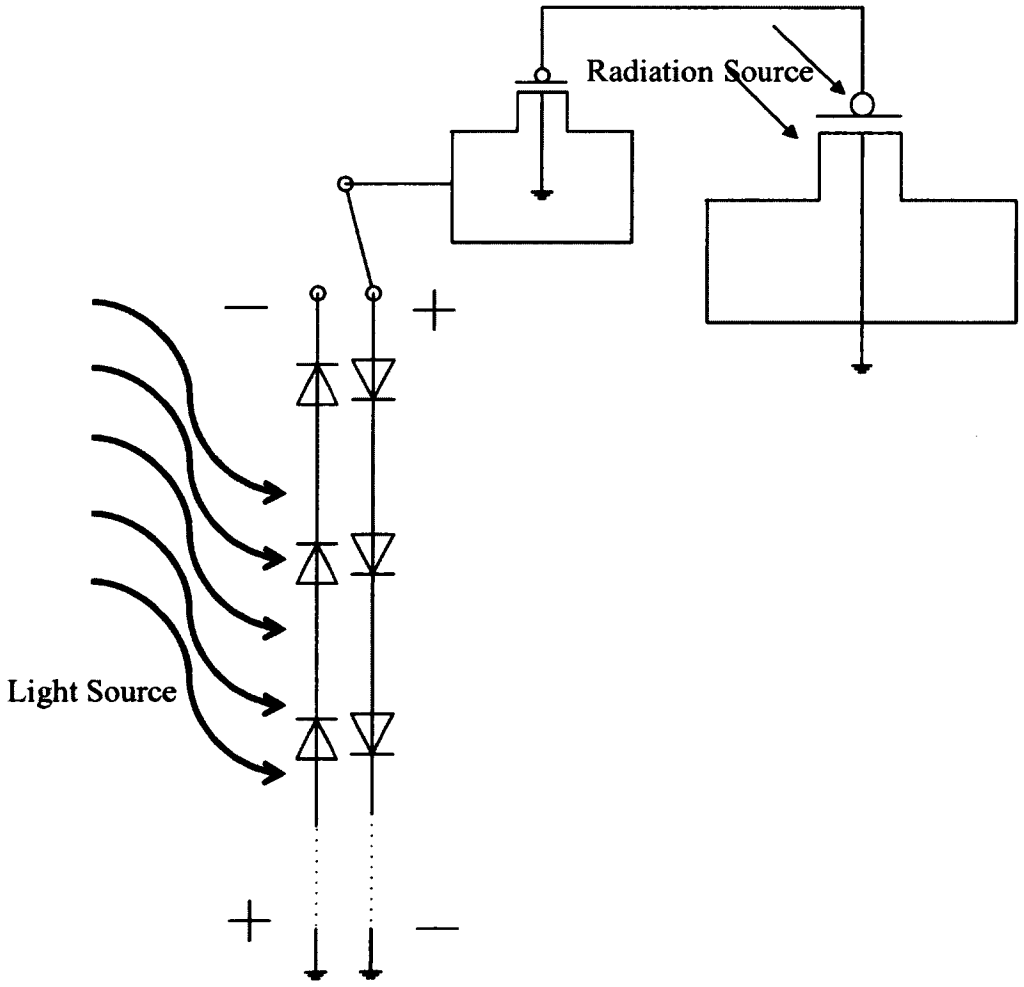

Figure 66- Proposed use of photodiodes in creating a positive or negative bias during irradiation

6. Research and development of power harnessing methods such as RF powering to run the readout or any other component on the dosimeter chips without using any battery or storage devices. This is a very promising area.

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