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A 64k Dynamic Random Access Memory Feasibility Study

University — Université

Carleton University

Degree for which thesis was presented — Grade pour lequel cette thèse fut présentée

Master of Engineering

Year this degree conferred — Année d'obtention de ce grade

1984

Name of Supervisor — Nom du directeur de thèse

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**A 64K DYNAMIC RANDOM ACCESS MEMORY
FEASIBILITY STUDY**

by

© Robert A. PENCHUK, B. Eng.

A thesis submitted to the Faculty of Graduate
Studies and Research in partial fulfillment
of the requirements for the degree of

Master of Engineering

Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada
May 1984

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submitted by Robert A. Penchuk in partial fulfillment
of the requirements for the degree of Master of
Engineering.

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May, 1984

ABSTRACT

Most dynamic random access memory (DRAM) designs utilize a fabrication process developed to most effectively realize an electrical design. When research for this thesis began virtually all DRAMs were made with an NMOS process.

This thesis examines the feasibility of making a dense DRAM, which is inherently analog intensive, using an existing CMOS process optimized for digital circuitry. Various DRAM design approaches based on one transistor per memory cell are examined. The design of a test chip and the correlation of the experimental results of electrical performance from this chip with simulations are then given. The research shows that a 64K DRAM with reasonable performance is feasible with this process.

ACKNOWLEDGEMENT

I would like to thank Dr. A. R. Boothroyd and Dr. J. P. Knight for supervising the thesis. I would also like to thank Mr. L. E. Trunley for making it possible for me to use Northern Telecoms facilities, Dave Smith and Robert Hadaway for advice and for co-ordinating and assembling the test chip cells, and Albert Loro for his microsurgery work on the fabricated devices. Finally, I would like to acknowledge the help of Northern Telecom Electronics for the use of their design and test facilities and for the fabrication of the test devices.

TABLE OF CONTENTS

ABSTRACT	i
ACKNOWLEDGEMENTS	ii
TABLE OF CONTENTS	iii
LIST OF FIGURES	v
LIST OF TABLES	ix
LIST OF SYMBOLS AND ABBREVIATIONS	x
CHAPTER 1 INTRODUCTION	1
1.1 Thesis Objective	1
1.2 Dynamic RAM Operation	2
1.3 Dynamic RAM Issues	6
1.4 Thesis Organization	10
CHAPTER 2 PRELIMINARY TEST CHIP DESIGN CONSIDERATIONS	14
2.1 Introduction	14
2.2 Fabrication Process Description	15
2.3 Solutions to Design Constraints	18
2.3.1 Word Line And Bit Line Pitch Constraints	18
2.3.2 Maximum Tolerable Soft Error Rate	28
2.3.3 Signal Margin Limitations	29
2.4 Design Approach	31
2.5 64K DRAM System Architecture	35
CHAPTER 3 SIGNAL MARGIN ANALYSIS/	38
3.1 Introduction	38
3.2 Threshold Voltage Mismatch	38
3.3 Sensitivity To Process Tolerances	39
3.3.1 Sense Amplifier Sensitivity	39
3.3.2 Bit Line Capacitance	55
3.3.3 Memory Cell Storage Capacitance	56
3.4 Reference Cell Schemes	58
3.4.1 Introduction	58
3.4.2 C/2 Reference Scheme	59
3.4.3 V/2 Reference Scheme	62
3.5 Thermal Generation	64
3.5.1 Introduction	64
3.5.2 Leakage Calculations	69
3.6 Capacitive Coupling And Charge Sharing Effects	75
3.6.1 Introduction	75
3.6.2 Coupling Effects For The Test Chip	78
3.6.3 Coupling Effects For A 64K DRAM	98
3.7 Resulting Worst Case Signal Margin	104

CHAPTER 4	LATCHING SCHEMES	107
4.1	Introduction	107
4.2	With P-Channel Isolating Transistors	111
4.3	With N-Channel Isolating Transistors	115
4.4	Without Bit Line Isolating Transistors	116
CHAPTER 5	SOFT ERROR RATE ANALYSIS	121
CHAPTER 6	WORD LINE CONSIDERATIONS	136
6.1	Calculation Of Word Line Loading	136
6.2	Rov Decoder Performance	139
CHAPTER 7	CONCLUSIONS.	141
7.1	Estimated Worst Case 64K DRAM Performance	141
7.2	Summary	146
7.3	Recommendations For Future Work	149
REFERENCES		151
APPENDIX A	TEST CHIP CELLS	154
APPENDIX B	SIMULATION OF SUCCESSFUL LATCH	182
APPENDIX C	SIMULATION OF UNSUCCESSFUL LATCH	186
APPENDIX D	SIMULATION OF WRITE OPERATION	190
APPENDIX E	SIMULATION OF READ OPERATION	196
APPENDIX F	SIMULATION OF 64K DRAM ACCESS TIME	200
APPENDIX G	SIMULATION OF DECODER OPERATION	205

LIST OF FIGURES

FIGURE NO.		PAGE
1.2.1	Conventional Open Bit Line NMOS Structure	3
1.2.2	Charge Sharing During Read Operation	4
2.2.1	Cross Section Of CMOS Structure	15
2.2.2	Memory Cell Utilizing Inversion Layer For Storage .	17
2.3.1	First Solution To Word Line Pitch Constraint . . .	19
2.3.2	Second Solution To Word Line Pitch Constraint . . .	19
2.3.3	Reducing Bit Line Pitch Constraint	21
2.3.4	Comparison Of Conventional And Zig-Zag Layout . . .	23
2.3.5	Folded Bit Line Structure	25
2.3.6	Bit Line Access	26
2.4.1a	Dynamic NOR Decoder	33
2.4.1b	Dynamic NAND Decoder	33
2.5.1	64K DRAM System Architecture	37
3.3.1.1	Regenerative Sense Amplifier	40
3.3.1.2	Model Used For Latching Operation Simulation . . .	44
3.3.1.3	Latching Waveform Used For Experimental Tests . . .	46
3.3.1.4	Schematic Of Setup Used To Test Sense Amplifier Sensitivity	51
3.3.1.5	Test Setup	52
3.3.1.6	Sense Amplifier Response With Initial Offset Voltage Less Than 8mV	53
3.3.1.7	Sense Amplifier Response With Initial Offset Voltage Equal To 8mV	53
3.3.1.8	Sense Amplifier Response With Initial Offset Voltage Greater Than 8mV	54
3.4.2a	Mask Level Sketch Of C/2 Reference Cell	60

3.4.2b	Schematic Of C/2 Reference Cell	60
3.5.1.1	Gated Diode Electrometer Schematic	66
3.5.1.2	Cross-Section Of Gated Diode Structure	67
3.5.1.3	Orthogonal View Of Gated Diode Structure	67
3.6.1.1	Capacitive Coupling During Write Operation	77
3.6.1.2	Capacitive Coupling During Read Operation	77
3.6.2.1	Model Used To Simulate Capacitive Coupling During A Write Operation	79
3.6.2.2	Word Line Waveform Used For Simulation Of Write Operation	80
3.6.2.3	Model Used To Simulate Capacitive Coupling And Charge Sharing During A Read Operation	81
3.6.2.4	Word Line Waveform Used For Simulation Of Read Operation	82
3.6.2.5	Circuit Used To Test Functionality Of Memory Cells	
3.6.2.6	Setup Used To Test Memory Cell Performance	89
3.6.2.7	Reading Logical 0 With 8 Small Memory Cells Per Bit line	90
3.6.2.8	Reading Logical 1 With 8 Small Memory Cells Per Bit Line	90
3.6.2.9	Reading Logical 0 With 16 Small Memory Cells Per Bit Line	91
3.6.2.10	Reading Logical 1 With 16 Small Memory Cells Per Bit Line	91
3.6.2.11	Reading Logical 0 With 32 Small Memory Cells Per Bit Line	92
3.6.2.12	Reading Logical 1 With 32 Small Memory Cells Per Bit Line	92
3.6.2.13	Reading Logical 0 With 8 Large Memory Cells Per Bit Line	93
3.6.2.14	Reading Logical 1 With 8 Large Memory Cells Per Bit Line	93
3.6.2.15	Reading Logical 0 With 16 Large Memory Cells Per Bit Line	94

3.6.2.16	Reading Logical 1 With 16 Large Memory Cells Per Bit Line	94
3.6.2.17	Reading Logical 0 With 32 Large Memory Cells Per Bit Line	95
3.6.2.18	Reading Logical 1 With 32 Large Memory Cells Per Bit Line	95
3.6.3.1	Gate To Storage Node Coupling During Write Operation For A 64K DRAM	100
3.6.3.2	Capacitive Coupling And Charge Sharing During Read Operation For A 64K DRAM	102
4.1.1	Regenerative Sense Amplifier	108
4.1.2a	Optimum Latch Waveform	111
4.1.2b	Commonly Used Latch Waveform	111
4.2.1	P-Channel Isolating Transistor Scheme	112
4.4.1	Complementary Sense Amplifier	117
4.4.2	Worst Case SCAMPER Simulation Of Latching Operation	120
5.1	Funneling Phenomenon	123
5.2	Circuit Timing For Soft Error Test	133
5.3	Circuit Schematic For Soft Error Test	134
5.4	Complete Cycle Test	134
5.5	Soft Error Detector	135
6.1.1	Word Line Capacitive Loading For Two Memory Cells .	136
6.2.1	Row Decoder Performance	140

A.1	Quadrant 1 Metallization Pattern	155
A.2	Structure With Small Memory Cells	157
A.3	Structure With Large Memory Cells	158
A.4	Cell Placement	160
A.5	Sense Amplifier Schematic	163
A.6	Sense Amplifier Layout	164
A.7	Sense Amplifier End Cap Layout	165
A.8	Sense Amplifier End Cap Layout	166
A.9	Memory Cell Schematic	168
A.10	Small Memory Cell Layout	169
A.11	Large Memory Cell Layout	170
A.12	Decoder Schematic	172
A.13	Decoder Layout	173
A.14	Word Line Driver Schematic	174
A.15	Word Line Driver Layout	175
A.16	Column Access I/O Schematic	176
A.17	Column Access I/O Layout	177
A.18	Interconnect Between Memory Cell Groups	179
A.19	Interconnect Between Column Decoders	180
A.20	Row Decoder To Small Memory Cell Interface	181

LIST OF TABLES

TABLE NO.	PAGE
3.3.1.1 Nominal Sensing Node Capacitance	42
3.3.2.1 Bit Line Capacitance	56
3.3.3.1 Memory Cell Storage Capacitance	57
3.5.2.1 Leakage Data For Gate Bounded Junction	70
3.5.2.2 Leakage Data For Field Oxide Bounded Junction	72
3.5.2.3 Thermal Generation Losses	74
3.6.2.1 Simulated Coupling Effects During Write Operation For Test Chip	80
3.6.2.2 Simulated Coupling And Charge Sharing Effects For Read Operation With Test Structure Using Small Cells	83
3.6.2.3 Simulated Coupling And Charge Sharing Effects For Read Operation With Test Structure Using Large Cells	84
3.6.2.4 Simulated Voltage Imbalance At Sense Amplifier	96
3.6.2.5 Measured Voltage Imbalance At Sense Amplifier	96
3.7.1 Results Of Worst Case Read Operation Simulation For 64K DRAM	105
7.1.1 Access Time Estimate For A 64K DRAM	143
7.1.2 Area Estimate For A 64K DRAM	144
7.1.3 Estimated Worst Case 64K DRAM Performance Figures	145

LIST OF SYMBOLS AND ABBREVIATIONS

A	junction area
A_{FIJ}	field induced junction area
A_{MJ}	metallurgical junction area
C_{bl}	bit line capacitance
C_{bts}	bit line to storage node overlap capacitance
C_{btw}	bit line to word line overlap capacitance
C_{gd}	gate to drain overlap capacitance
C_{gs}	gate to source overlap capacitance
C_{jn1}	junction component of memory cell storage capacitance
C_{jn2}	junction component of bit line capacitance
C_{sn}	sense amplifier sensing node capacitance
C_s	memory cell storage capacitance
CMOS	complementary metal oxide semiconductor
DRAM	dynamic random access memory
I	leakage current
$I_{gen,FIJ}$	field induced junction leakage current
$I_{gen,MJ}$	metallurgical junction leakage current
LSI	large scale integration
MC	master clock used for test chip
n_i	intrinsic carrier density
NMOS	n-channel metal oxide semiconductor
q	electron charge
TR	signal for the gate of the bit line isolating transistor
V_{bl}	bit line voltage
V_r	reverse bias junction voltage
V_{stor}	memory cell storage node voltage

VDD	drain supply voltage
VIN	input signal and bit line precharge level for the test chip
VLSI	very large scale integration
VSS	source supply voltage
VT	threshold voltage
W	depletion layer width
WD	word line signal used with the test chip
W_{FIJ}	field induced junction depletion layer width
W_{MJ}	metallurgical junction depletion layer width
τ_g	thermal generation lifetime

CHAPTER 1

INTRODUCTION

1.1 Thesis Objective

This thesis is concerned with determining the feasibility of making a 64K DRAM with a process not designed for making memory. The process was designed to support custom CMOS LSI; thus the usual and optimum approach of developing a process specifically for the realization of a DRAM design can not be taken.

Although the thesis research is essentially a feasibility study for a 64K DRAM the results of the work are equally applicable to memories with smaller capacities, such as a 4K DRAM, which would support other circuits on the same die in custom LSI applications. An example is the use of DRAM to support a single chip microprocessor design.

To determine the feasibility of a 64K DRAM with the existing process the critical components, namely sense amplifiers and memory cells, must be developed and tested in isolation so that their performance may be evaluated without interactions between them giving misleading results. For this reason a test chip was deemed necessary. This thesis examines the critical components of a DRAM both theoretically and experimentally with correlation of the results where possible.

1.2 Dynamic RAM Operation

Figure 1.2.1 below shows one column of a typical DRAM structure using n-channel transistors. A 5V supply will be assumed throughout this section.

With reference to Figure 1.2.1 the read operation may be described as follows. The conventional DRAM structure is symmetric with n rows of memory cells on either side of a sense amplifier. Two additional rows are used for reference cells, one used in conjunction with memory cells attached to bit line A and the other used with memory cells attached to bit line B. The memory cell may be in one of two states. For n-type memory cells, (as shown in Figure 1.2.1), a logical 0 state is represented by a discharged capacitor and a logical 1 state is represented by a charged capacitor. The reference cell is in a state which may be referred to as a logical 1/2. The reference cell has an amount of charge stored on its capacitor approximately equal to half of the charge stored on a memory cell storage capacitor in the charged state. Further detail on reference voltage generation may be found in Section 3.4.

Assume the case where a memory cell in the logical 0 state which is attached to bit line A is being read. Both bit line A and bit line B are precharged high by circuitry which is not shown and the latch node is held high, thus preventing the cross-coupled pair of transistors which form the sense amplifier from conducting. The memory cell stor-

Figure 1.2.1

Conventional Open Bit Line NMOS Structure

age capacitor is connected to bit line A by raising the potential of its word line. Simultaneously the reference cell storage capacitor is connected to bit line B by raising its word line potential. Charge sharing then occurs between the two storage capacitors and bit lines. This is illustrated in Figure 1.2.2 assuming typical values for storage and bit line capacitance.

Figure 1.2.2

Charge Sharing During Read Operation

Charge sharing with the reference cell causes bit line B to drop slightly below 5V. Charge sharing with the memory cell causes bit line A to drop even further below 5V. Thus a small voltage imbalance will form across the sense amplifier. The latch node is then lowered from 5V to 0V in such

a manner that only one of the transistors forming the sense amplifier will turn on. For more detail on sense amplifier latching the reader is referred to Chapter 4. This action causes bit line A to discharge through the sense amplifier while bit line B remains very close to 5V, (recall that a slight drop in bit line voltage occurs when the reference cell is charge shared with the bit line). The voltage imbalance across the sense amplifier is now comparable with the power supply voltage. As the memory cell access transistor remains on throughout this latching process the initial voltage level in the memory cell is reinstated.

At this point, data for an entire row of memory cells, all of which share a common word line, are represented as complementary signals with each column using one pair of bit lines. The column decoder then selects one pair of bit lines to be connected to the I/O lines thus completing the read operation. The memory cell access transistor is then shut off thereby storing the regenerated data.

Leakage due to thermal generation will eventually discharge the memory cell storage capacitor to a level where the sense amplifier can no longer reliably detect the voltage imbalance produced during a read cycle. Therefore each memory cell must be read on a continual basis to prevent loss of data. The act of reading for the sole purpose of regenerating data which were degraded by leakage is called refreshing. Since the contents of the memory cells are not

used externally during refresh the column decoders are not activated.

Before a subsequent read or refresh may occur the reference level must be regenerated, (refer to Section 3.4 for details of this operation), and the bit lines must be precharged up to 5V again.

The write operation is virtually identical to the read operation with one exception. When the column decoders select one pair of bit lines for connection to the I/O lines the bit line pair and associated sense amplifier are driven to a new state by the I/O lines instead of the bit lines driving the I/O lines, as would occur for a read operation.

1.3 Dynamic RAM Issues

The major issues regarding DRAM design constraints, as well as general issues to be considered during design, are as follows:

- i) Word line and bit line pitch constraints.
- ii) Maximum tolerable soft error rate.
- iii) Signal margin limitations.
- iv) Speed.
- v) Market competition.
- vi) Use as a process test vehicle.

One limitation on the size of the memory cell, (thus the density of the overall design), is that it should be compatible with the minimum bit line pitch and word line pitch of peripheral circuitry, (such as the decoders and sense amplifiers). The bit line pitch is the spacing between two adjacent bit lines. Similarly the word line pitch is the spacing between two adjacent word lines. If the pitch requirements are not met the DRAM structure becomes very area intensive.

Another limitation on the size of the memory cell is the requirement for a sufficient difference in charge on the storage capacitor, representing the difference between a logical 0 and a logical 1. Insufficient charge difference results in a large number of soft errors. Soft errors are random errors which occur when floating nodes, such as the storage capacitor, are excessively discharged due to charge collection. The amount of charge stored in a memory cell is typically equivalent to 100,000 to 1,000,000 electrons. This amount of charge is small enough that ionizing radiation in the form of alpha particles, emitted by the package, can destroy the integrity of the data by discharging a memory cell while data are stored, or by discharging a bit line or sense amplifier while data are transferred to and sensed by the sense amplifier during a read operation. A detailed discussion of soft errors is given in Chapter 5.

The next design constraint is that of sufficient signal margin. Signal margin is defined as the worst case voltage

difference distinguishing a logical level, (either a logical 0 or a logical 1), from a reference level. Signal margin is limited by the charge stored in the memory cell and by the loss in signal due to charge sharing when data are transferred from the memory cell storage capacitor to the larger capacitance of the bit line and the input to the sense amplifier, (as previously illustrated in Figure 1.2.2). Typical signal margins are on the order of 100mV to 300mV. This signal margin is low enough that capacitive coupling between word lines and bit lines must be considered. The sensitivity of the sense amplifier, which is the minimum signal that it can reliably detect, also reduces the signal margin.

The final design constraint is that of operating speed. Operating speed is limited by the time constant of interconnect, by the latching speed and by the time required to pass data from the bit lines to the I/O lines. Decoding time is mostly limited by the time constant of interconnect. Using metal rather than polysilicon wherever possible will reduce the speed limitation due to interconnect. Latching speed is inversely proportional to the signal margin, thus an increase in signal margin not only reduces the noise susceptibility of the DRAM but also increases its speed. The time required to pass data from the bit lines to the I/O lines may be reduced by increasing the gain of the transistors which separate the bit lines from the I/O lines. The size

of these transistors are often constrained by the bit line pitch.

A general issue to be considered when designing a DRAM is that the DRAM market is very competitive with low profit margins. To make a competitive DRAM and to overcome the above mentioned design constraints, process and circuit designers must work closely together. Circuit designers should be able to explain the DRAM design problems to a process designer and suggest solutions through various process modifications or alternatives. The process designer should be able to advise the circuit designer of the feasibility of such process changes and explain the tradeoffs of the changes from an economic and reliability point of view. Such interaction is essential when taking the usual approach of developing a fabrication process specifically for an electrical design.

Until very recently all DRAMs were made with an NMOS technology. However CMOS technology offers the advantages of reduced peripheral circuit complexity and improved noise immunity. It has recently become evident that CMOS can be competitive despite increased cost and decreased density associated with the process [1,2].

As a DRAM typically contains thousands of identical cells each taxing the design rules to their limit it makes rigorous demands on the integrity of the process technology used to fabricate it. It is, in fact, often used as a test vehicle for monitoring the yield of a process. The small

signal margins used are also useful in predicting the impact of soft errors on other VLSI designs. When VLSI designs other than DRAM are implemented junction capacitance will be reduced, due to geometry scaling, to such a level that alpha particles may discharge floating nodes. Thus simple dynamic circuitry may not operate reliably. .

1.4 Thesis Organization

The feasibility study begins at Chapter 2 with a description of the available process. Conventional solutions to the DRAM issues which were discussed in Section 1.3 are then presented. The appropriate choice of solution for each issue, for the fabrication process available, is then given. As previously discussed in Section 1.1 a test chip is deemed necessary to justify the chosen solutions. The approach used to design and lay out the test chip as well as a description of it is given in Chapter 2. By laying out the test chip the minimum pitch dimensions are found. If it is found that the size of the memory is limited much more by the pitch requirements than by the minimum stored charge, variations in system architecture may be used to alleviate the problem. Chapter 2 continues with choice of the optimum system architecture for the DRAM, based upon the established values of minimum pitch dimensions. At this point the bit line loading, (number of memory cells/bit

line), is determined, an essential requirement before circuit simulation of the DRAM can be undertaken.

Further research and theoretical predictions for a 64K DRAM are then undertaken and are treated in Chapters 3 to 6. The test chip is then analysed and experimental performance data is presented to verify the theoretical predictions. To facilitate comparison of theoretical and experimental results the data gathered from the test chip are given in the section where the corresponding theory is presented.

Knowing the bit line loading, the worst case signal margin may be investigated. Signal margin analysis is the subject of Chapter 3, which constitutes a major contribution of the thesis. Signal margin is determined by summing up several components which fall into several categories, the most important of which are the worst case threshold imbalance, and sensitivity to process tolerances. To make the treatment manageable, the memory cell, bit line and sense amplifier are treated in isolation. Although the same process variations will occur in all memory cells, bit lines and sense amplifiers at the same time, the number of combinations of process changes is difficult to analyse. By computing the resulting worst case signal margin after all process tolerances are taken into account one can then determine whether the interactions between the tolerances of each component should be included. This approach simplifies computation, allows comparison of individual components and builds an added safety margin into the design. Worst case

supply voltage is used in determining the worst case signal margin in the memory cell.

An accurate reference signal is required to allow the sense amplifier to detect the difference between a logical 0 and logical 1 level after the memory cell has transferred the data signal to the bit lines, (refer to Section 1.2 for an explanation of the read cycle). This consideration is next addressed in Chapter 3 which continues with a comparison of two possible reference schemes. Upon transferring the data signal, which is represented by a charged or discharged capacitor state, to the higher capacitance bit line, signal degradation due to charge sharing occurs. The nominal signal margin of the data after charge sharing with the bit lines is necessary at this point, so that the reference level may be determined. These reference schemes solve the problem introduced by capacitive coupling between the gate of the access transistor, (which separates the memory cells storage capacitor from the bit line), and the bit line, as well as variations of the charge stored in the memory cell due to changes in operating temperature and/or power supply voltage. Worst case reference cell variation due to process tolerances is then added. The best reference scheme is chosen and used throughout the remaining analysis.

Also treated in Chapter 3 is the loss of charge in the memory cell due to thermal generation, the influence of capacitive coupling effects and charge sharing effects between the memory cell storage capacitor and the bit line.

The chapter concludes with estimates of the worst case signal margin at the sense amplifier sensing nodes, taking into account all the factors analysed.

Chapter 4 investigates various latching schemes. The latching process is taken to include all steps following the introduction of a voltage imbalance on the bit lines up to the point where the imbalance is regenerated into an imbalance comparable with the power supply voltage.

Chapter 5 is concerned with analysing the soft error susceptibility of DRAM in general. Accurately predicting the soft error rate of a structure through mathematical means is very difficult. The chapter illustrates the degree of difficulty by describing the various parameters which would have to be taken into account. This treatment of soft error rate analysis is then used to reinforce the choice of an empirical approach for predicting the soft error rate. An estimate of the soft error rate is then given.

Chapter 6 deals with word line considerations. This includes the row decoder performance in conjunction with the distributed time constant of the polysilicon word line.

The thesis concludes with an estimate of the performance of a 64K DRAM using the existing CMOS process. A summary of the main points brought forth in the thesis is made followed by a recommendation for future work required to develop a 64K DRAM.

CHAPTER 2

PRELIMINARY TEST CHIP DESIGN CONSIDERATIONS

2.1 Introduction

As was discussed in Section 1.1 a test chip is necessary to establish the feasibility of a 64K DRAM with the available process. The test chip is intended to provide data on the functionality and performance of critical components, namely the sense amplifier and the memory cell. This data can then be correlated with results from simulations to substantiate the validity of the models that are used. Simulations based on the same models may then be performed for a 64K DRAM.

Before the test chip can be designed solutions, which are compatible with the available process, must be found for the design constraints outlined in Section 1.3.

The issues to be resolved are:

- i) Word line and bit line pitch constraints.
- ii) Maximum tolerable soft error rate.
- iii) Signal margin limitations.

The available process will now be described followed by solutions for the above design constraints problems.

2.2 Fabrication Process Description

The fabrication process is a 3 micron p-well CMOS process, (refer to Figure 2.2.1). An n-type substrate adjustment implant is used to increase the threshold voltage of parasitic transistors. This implant also increases the substrate doping near the surface for p-channel devices. A Boron implant is also used to adjust the threshold of p-channel devices to match that of the n-channel devices.

There are two interconnect layers, one metal and the other polysilicon. The same polysilicon layer is also used to form self aligned transistor gates.

Figure 2.2.1

Cross - Section Of CMOS Structure

The process is primarily a digital process with little facility for highly linear capacitors for analog applications. To increase the versatility of the process a p+ capacitor implant was added to make polysilicon to substrate capacitors without the requirement of biasing the silicon surface into inversion with the top polysilicon capacitor plate. This capacitor structure was only intended for limited use within a digital design. In contrast, however, DRAM design is very analog intensive with the capacitor used in the memory cell being of key importance.

Two candidates for the memory cell storage capacitor are now described. The first candidate requires the top polysilicon plate to bias the silicon surface into inversion thus forming the bottom capacitor plate. This is illustrated in Figure 2.2.2. The storage capacitance for this memory cell is the polysilicon capacitor plate to inversion layer capacitance, (referred to as oxide capacitance), in parallel with the inversion layer to substrate capacitance, (referred to as depletion or junction capacitance). The advantage of this structure is that either p-type or n-type memory cells may be made. The disadvantage is that the polysilicon capacitor plate must always be biased to invert the silicon surface. This prevents a single polysilicon line from being shared as a gate for one memory cell and a capacitor plate for an adjacent memory cell.

The second candidate uses the p+ capacitor implant to form the bottom capacitor plate. The structure is identical

Figure 2.2.2

Memory Cell Utilizing Inversion Layer For Storage

to Figure 2.2.2 with the exception that the inversion layer is replaced with an implanted layer. Since a similar n+ capacitor implant does not exist in this process only p-type memory cells can be used with this approach. The advantage is that the polysilicon capacitor plate may be used as the access gate for adjacent cells. As will be shown in the following section, this is a requirement to implement a structure which reduces the constraint imposed by bit line and word line pitch, described in Section 1.3. The disadvantages are that p+ junction capacitance per unit area is lower than n+ junction capacitance, (with this process), and that the p-well can not be used to isolate the memory cells

from substrate current thereby making the memory cells more sensitive to noise.

2.3 Solutions To Design Constraints

2.3.1 Word Line And Bit Line Pitch Constraints

The minimum size of the memory cell is determined by one of two criteria. The first criterion is that the memory cell meet the bit line and word line pitch. The second criterion is the minimum required stored charge. The second criterion is primarily limited by the process whereas the first criterion may be controlled to some degree through use of various design structures. It is desirable to have the memory cell size constrained by the process rather than by design since the purpose of this thesis is to determine if a 64K DRAM can be made without process changes.

Several structures will be described later which increase the bit line pitch at the expense of reducing the word line pitch. It is easier to design peripheral circuitry around a memory array which has a narrow word line pitch than one with a narrow bit line pitch, as will now be shown.

The row decoder and word line driver are the cells that are constrained by the word line pitch. Narrow word line pitch may be accommodated in one of two ways. The first is to place the row decoders and drivers on either side of the memory array with one side used for even rows and the other

Figure 2.3.1

First Solution To Word Line Pitch Constraint

Figure 2.3.2

Second Solution To Word Line Pitch Constraint

for odd rows. This is illustrated in Figure 2.3.1. A second more area intensive way of accomodating narrow word line pitch is shown in Figure 2.3.2. This solution is more area intensive since it requires that not only the row decoder and driver fit in between two adjacent word lines but the feed through interconnect for adjacent row decoders as well. These two solutions may be used either together or separately to accomodate narrow word line pitches. However for very narrow word line pitches the second solution becomes area intensive thus negating its purpose.

There is not as much flexibility in placing cells to meet the bit line pitch. With reference to Figure 1.2.1 illustrating the conventional open bit line structure one can see that the first solution used to alleviate the word line pitch constraint can not be applied to the sense amplifiers. However the second solution used to alleviate the word line pitch may be used. The application of this solution to the bit line pitch constraint is illustrated in Figure 2.3.3. A similar staggering of the column decoders would also be required.

There are two drawbacks to this solution. One drawback is that any pair of bit lines associated with one column are different lengths, thus they will not be capacitively balanced. Capacitive balance of the bit lines would have to be maintained by extending one bit line length until the two are equal. This results in wasted space. Another drawback

Figure 2.3.3
Reducing Bit Line Pitch Constraint

is that the noise sensitive bit lines must be routed through adjacent sense amplifiers.

It has been shown that while reducing the word line pitch constraint is possible, no easy solution exists for reducing the bit line pitch constraint. However several approaches exist which increase the bit line pitch while decreasing the word line pitch.

One could design the memory cell to have a large bit line pitch and a narrow word line pitch. Unfortunately this increases the size of the memory cells access transistor thus reducing the ratio of storage capacitor area to memory cell area.

A better solution is to use an arrangement called the zig-zag structure [3], shown in Figure 2.3.4. This structure is similar to the conventional open bit line structure shown in Figure 1.2.1 except that the bit line zig-zags between two adjacent collinear strips of memory cells, previously defined as columns. For the zig-zag structure a column will be taken to include all memory cells attached to a single bit line. This approach still uses the same number of bit lines and sense amplifiers, and has the same number of memory cells per bit line as the conventional open bit line structure. Every second memory cell on each bit line has been staggered. This solution requires the use of the p+ capacitor implant as described in Section 2.2 since the polysilicon word line will have to be shared as a gate and a capacitor plate between memory cells.

(a) Conventional Layout

(b) Zig-Zag Layout

Figure 2.3.4

Comparison Of Conventional And Zig-Zag Layout

Another approach, which alleviates the bit line pitch constraint is to use a folded bit line structure [4]. In the folded bit line structure the memory cell signal and the reference cell signal used during the read operation are on physically adjacent bit lines, (as opposed to being on physically opposite sides of the sense amplifier cell). Refer to Figure 2.3.5 for a schematic of the folded bit line structure.

The reader may find it useful to compare Figure 2.3.5 with the open bit line structure shown in Figure 1.2.1. The actual memory cell layout for the folded bit line structure is similar to the zig-zag layout except the bit line does not zig-zag between collinear strips of memory cells.

The folded bit line structure has two main advantages over the open bit line structure regardless of whether the conventional or zig-zag layout is used. The first concerns noise immunity. Since the pair of bit lines from the differential inputs of the sense amplifier run adjacent to each other, common mode noise cancels in the amplifier.

The second advantage is that the folded bit line structure easily permits balanced access to bit line pairs, (see Figure 2.3.6a below). Contrast this to bit line access using the open bit line structure which may be arranged in one of two ways as shown in Figures 2.3.6b and 2.3.6c. The arrangement shown in Figure 2.3.6b has a single ended I/O. This increases the time required to write or read a memory

Figure 2.3.5
Folded Bit Line Structure

Figure 2.3.6
Bit Line Access

cell. The arrangement shown in Figure 2.3.6c has a fully differential I/O but has several disadvantages:

- i) The column decoder must be duplicated resulting in an area penalty.
- ii) Coupling between column decoders and sense amplifiers is increased.
- iii) Column decoder design complexity increases since the bit lines must be routed through them while still maintaining the same bit line pitch.
- iv) Bit line noise is increased since the bit lines are run close to the column decoders.

The disadvantage of using the folded bit line scheme, which applies only to the available process, is that p-type memory cells must be used. As described in Section 2.2 the use of p-type memory cells increases the noise sensitivity of the memory cells as well as decreases the junction component of storage capacitance. However, further research showed that the reduction in the junction part of storage capacitance is not as significant as the reduction in the junction part of bit line capacitance. Thus while the stored charge in the memory cell is reduced slightly the voltage imbalance on the bit lines during a read operation is increased through the use of p-type memory cells. The reader is referred to Section 3.3 where a breakdown of the memory cell and bit line capacitance calculations are given.

By using p-type memory cells with a folded bit line architecture the size of the memory cell is constrained by the requirement for a minimum level of stored charge which is primarily a process constraint rather than by pitch requirements which is primarily a design constraint. Although the process is fixed for the purpose of this thesis, common approaches used to alleviate the process constraint will be given.

2.3.2 Maximum Tolerable Soft Error Rate

As described in Section 1.3 there is a minimum requirement of stored charge in the memory cell to prevent an excessive soft error rate. The level of stored charge in the memory cell also affects signal margin but in practice the maximum tolerable soft error rate dictates the required amount of stored charge. To increase the stored charge in the memory cell one can increase the storage capacitance and/or increase the stored potential.

Storage capacitance may be increased by:

- i) Decreasing the dielectric thickness.
- ii) Increasing the dielectric constant by resorting to special dielectrics (i.e. $\text{SiO}_2/\text{Si}_3\text{N}_4$ sandwich).
- iii) Increasing capacitor area by etching moats into the silicon [5].
- iv) Decreasing depletion layer widths by special implants.

Increasing the stored potential is obtained by bootstrapping the word line to prevent loss of stored potential due to the threshold voltage of the memory cell access transistor. For various practical reasons, (one of which is the possibility of forward biasing a junction), bootstrapping is more suitable to an NMOS technology rather than CMOS. For this reason bootstrapping will not be used in the DRAM design.

2.3.3 Signal Margin Limitations

The final design constraint is the requirement for a sufficient signal margin, where the signal margin is defined to include the sense amplifier sensitivity and variations in the reference level. When a memory cell is read, signal degradation occurs due to charge sharing between the storage

capacitor and the bit line. The bit line capacitance may be reduced by using a metal rather than diffused bit line. Avoiding diffused bit lines also significantly reduces soft errors by minimizing the junction area which could collect charge from the substrate.

An accurate reference level is required which will compensate for:

- i) Changes in power supply voltage.
- ii) Leakage due to thermal generation.
- iii) Memory cell access gate to bit line capacitive coupling.
- iv) Process variations.
- v) Bit line noise.

For simplicity a reference cell is not used with the test chip but two memory cells are used in complement to store one bit pair. Reference level generation will be dealt with in Section 3.4.

The final issue to be dealt with to maximize signal margin is that the sense amplifier sensing nodes and Bit line must be capacitively balanced over all process variations, (i.e. mask misalignment). The best way to achieve this is to capacitively balance each mask level in the fabrication process. This ensures that the sense amplifier sensitivity, (ability to reliably latch small voltage imbalances), will be optimized. The cross-coupled transistor

pair forming the sense amplifier should have the same gain and should be placed close to each other to reduce threshold differences between the two due to process variations. This will be dealt with in more detail in Section 3.2.

2.4 Design Approach

Schematics and plots of the mask level design for the test chip cells are given in Appendix A. For reasons stated in Section 2.3 a folded metal bit line approach using p-type memory cells is used.

The column decoder and sense amplifier cell design were carried out to the density limit set by the layout rules. The wider of these two cells set the bit line pitch. The narrower cell was then readjusted to the established bit line pitch. The column decoder was designed as a basic decoder plus an additional cell to interface it to a pair of bit lines. The schematic and layout of this interface cell is shown in Figures A.16 and A.17 respectively. The interface cell connects a selected bit line pair to a pair of I/O lines. It also contains a transistor to connect the bit line pair together for implementing the $V/2$ reference scheme which is described in Section 3.4.3. The reference scheme was not tested as it turned out that sufficient data were obtainable by storing a bit as a complementary pair using two memory cells. The design of the column decoder as a basic decoder plus an add-on cell was chosen so that the

basic decoder design could also be used as the row decoder with another add-on cell. This simplifies design and testing. The decoder was chosen to be an n-channel dynamic NOR type. An n-type was chosen over a p-type for its speed advantage while a dynamic decoder was chosen over a static one for its area advantage. A NOR decoder as shown in Figure 2.4.1a has several advantages over the NAND decoder shown in Figure 2.4.1b.

The NOR decoder has a symmetrical output thus it may be shared between two blocks of memory cells. Also NOR decoders are faster than NAND decoders. The disadvantage of the NOR decoder is that it consumes more power than the NAND decoder. Assuming that we have n decoders, during a decode operation $n-1$ decoders are deselected by discharging their output nodes through one or more transistors. The output node of the selected decoder will remain high. In contrast, with n NAND decoders only one is selected with its output node going low. The NOR decoder not only consumes more power but also creates a large substrate charging current during a decode operation thus increasing the noise floor. However, by using n-type decoders with p-type memory cells the memory cells are shielded from the injected carriers by a reverse biased p-well.

After the bit line pitch was established from the column decoder and sense amplifier design a small and a large memory cell were designed each with the same bit line pitch. By performing a survey of other DRAM designs, the

Figure 2.4.1a

Dynamic NOR Decoder

Figure 2.4.1b

Dynamic NAND Decoder

minimum stored charge required to reduce the soft error rate to an acceptable level was determined. The details of this analysis are covered in Chapter 5. The required minimum stored charge was used to determine the size of the large memory cell. The resulting word line pitch as determined from the large memory cell was very close to the word line

pitch as determined from the decoder design and the decoder to word line interface cell design, (basically a word line driver as shown in Figures A.14 and A.15), thus the large memory cell was increased to meet this pitch. The small memory cell was designed to the density limit set by the layout rules. The small memory cell was intended to have a significant soft error rate which could be easily measured, for use in Chapter 5.

Two DRAM structures were designed. One uses the small memory cell with an area of 184 square microns and a storage capacitance of approximately 15fF. The other uses the large memory cell with an area of 416 square microns and a storage capacitance of approximately 60fF. Each structure contains three groups of memory cells. Each group has 3 pairs of bit lines attached to 3 sense amplifiers so that disturbance effects between sense amplifiers as well as between memory cells can be observed. The three groups have different bit line loadings. The first one has 32 cells per bit line, the second has 16 cells per bit line and the third has 8 cells per bit line. Capacitive coupling and charge sharing effects may then be observed for different bit line loadings. All three groups share the same row decoder thus reducing the number of bonding pads required. For simplicity all timing is required to be generated off chip.

2.5 64K DRAM System Architecture

It has now been determined that a metal folded bit line structure using the large p-type memory cells should be used. The actual system architecture must now be defined. To define the system architecture one must determine the number of blocks that the memory cell array should be divided into. This in turn gives the bit line loading which will be used during analysis in the following chapters.

The bit line loading may be halved by sharing the column decoder between two arrays. Reducing the bit line loading reduces the bit line capacitance and thus increases the signal margin. This is possible with a symmetric decoder such as the NOR decoder, (refer to Figure 2.4.1a). Word line delay is reduced by sharing the row decoder between two arrays. This results in four blocks of memory cells as shown in Figure 2.5.1. An additional advantage to this scheme is that only one block needs to be activated at one time thus reducing power consumption. Alternatively a design is possible which makes the architecture 64K by 1 bit or 16K by 4 bits by removing the 4:1 bidirectional multiplexor/demultiplexor.

Some designs exist with more than four blocks [6]. Increasing the number of blocks beyond four reduces bit line loading and/or word line delay at the expense of circuit complexity and increased area, (since the decoders must be duplicated).

Word line delay may be further reduced by using word line repeaters [1]. As word line length increases the delay increases approximately in proportion to the square of the length since both resistance and capacitance increase. By using a repeater the total delay is the sum of two smaller delays. The same inverter used as the word line driver, (Figures A.14 and A.15), is used twice to form the word line repeater.

The architecture to be used for the 64K feasibility study will consist of an array of p-type memory cells using the folded metal bit line arrangement being divided into four blocks by symmetric n-type NOR decoders. Each of the four blocks will be further subdivided by word line repeaters.

Figure 2.5.1

64K DRAM System Architecture

CHAPTER 3

SIGNAL MARGIN ANALYSIS

3.1 Introduction

This chapter is concerned with determining the worst case signal margin for both the structure using small memory cells and the structure using large memory cells which were discussed in Chapter 2.

The effects of process variations, such as threshold voltage variation, polysilicon and metal over/under etching and polysilicon to device well misalignment, on the memory cells, reference cells, bit lines and sense amplifiers are analysed. Signal loss due to thermal generation at 75 degrees Celsius as well as at room temperature, (23 degrees Celsius), is calculated along with capacitive coupling and charge sharing effects. In conclusion an estimate is made of the signal margin resulting from the combination of all these effects. A worst case supply voltage of 4.5V will be assumed for this chapter.

3.2 Threshold Voltage Mismatch

Mismatch of threshold voltage between the cross-coupled transistors of the sense amplifier reduces the sense amplifier sensitivity, (i.e. it increases the minimum voltage

imbalance required for a successful latching operation). This, in turn, reduces the signal margin.

It has been reported in literature [6] that for a modern MOS process, such as the one in concern, closely spaced large geometry transistors will have a threshold voltage variation of approximately 2mV . Large geometry means that no short or narrow channel effects will be present in the transistor.

Threshold voltage mismatch alone does not determine sense amplifier sensitivity. Capacitive imbalances between the sensing nodes must also be considered. Capacitive imbalance is considered in Section 3.3.1 where the resulting sense amplifier sensitivity is calculated.

3.3 Sensitivity To Process Tolerances

3.3.1 Sense Amplifier Sensitivity

The sensitivity of a sense amplifier determines the minimum voltage imbalance that it can reliably detect and latch. With the aid of Figure 3.3.1.1 the latching operation will be briefly described.

A voltage imbalance of dV volts is developed across the sensing nodes, (drains of transistors 1 and 2), as a result of charge sharing between the bit lines and the reference and memory cells. The latch node is then ramped slowly from V_{DD} to V_{SS} . When the latching node reaches one threshold

Figure 3.3.1.1

Regenerative Sense Amplifier

below the gate of transistor 2 then transistor 2 will turn on thereby discharging the bit line attached to its drain. As long as the latch node is ramped to VSS slowly enough so that the drain of transistor 2 can follow its source within one threshold then transistor 1 will not turn on.

Although having no off-side conduction is desirable, a successful latching operation does not imply that no off-side conduction will occur. A successful latch is one where the polarity of the initial voltage imbalance is preserved following the latching operation and where the voltage imbalance is increased to a level where less sensitive circuits such as pull up transistors can fully regenerate the voltage imbalance to a level comparable with the supply voltage. No off-side conduction is desirable but is hard to obtain in practice as will be shown in Chapter 4.

For a successful latch two conditions must be met. The latch waveform must not go to VSS too fast or excessive off-side conduction will occur. This lower limit is on the order of a few tens of nanoseconds. The second condition is that the latching operation must be fast enough so that the voltage imbalance is not lost by capacitive discharge. This upper limit is on the order of milliseconds. The latching waveform used for experimental verification of sense amplifier sensitivity as shown in Figure 3.3.1.3 is well within these limits.

Sense amplifier sensitivity is limited by the threshold imbalance between the cross-coupled transistor pair of the sense amplifier and by capacitive imbalance between the sensing nodes. Threshold imbalance was determined to be approximately 2mV, (refer to Section 3.2). The effect of capacitive imbalance was simulated using SCAMPER. Then the threshold voltage imbalance was added to the simulated minimum resolvable initial voltage imbalance across the sensing nodes. A more accurate representation would have included the threshold voltage imbalance in the model used during simulations, however the method used will give a conservative design. In fact, if no off-side conduction occurs and the threshold voltage imbalance is less than the initial voltage imbalance across the sensing nodes then the threshold voltage imbalance does not affect sense amplifier sensitivity at all. Instead it will only change the time at which the on-side transistor starts to conduct.

Worst case capacitive imbalance will now be calculated for use in succeeding simulations. The layout used for capacitive calculations is shown in Figure A.6. To minimize capacitive imbalance under a worst case process each component contributing to the capacitance of the sensing nodes was individually matched to its symmetrical counterpart as closely as possible. The various capacitance components, evaluated from the mask layout, are listed in Table 3.3.1.1 for nominal process conditions.

	Left Sensing Node	Right Sensing Node
	(fF)	(fF)
N+ Junction	27.4	27.4
Metal to Substrate	7.9	6.8
Metal to Polysilicon	1.4	0.9
Polysilicon to Substrate	4.9	4.9
Gate Capacitance	12.4	12.4
Total	54.0	52.4

Table 3.3.1.1
Nominal Sensing Node Capacitance

When calculating the junction capacitance both planar and peripheral components are taken into account. A reverse bias junction voltage of 5V is assumed. Although at the beginning of the latching operation one sensing node is reverse biased by slightly less than 5V the difference in junction capacitance is insignificant. A reduction in capa-

capacitance imbalance is still possible by readjusting the metal mask dimensions.

Both sensing nodes track each other with respect to over or under etching of the polysilicon or metal masks and metal mask misalignment. Polysilicon to device well misalignment adds an additional 0.8fF capacitive imbalance, (0.4fF per sensing node), assuming worst case junction capacitance. Thus the capacitance at the left sensing node is 54.4fF and at the right sensing node is 52.0fF giving an imbalance of 2.4fF.

The latching operation was simulated with SCAMPER using the model shown in Figure 3.3.1.2. Node numbers and transistor names correspond to those used in the simulations. Source files and simulation results for a successful and an unsuccessful latching operation are shown in Appendix B and C respectively. Simulations were performed assuming a nominal process, a 5V supply voltage and operation at room temperature. Junction capacitance is automatically included in the definition of the transistor models however the other parasitic capacitances listed in Table 3.3.1.1 have to be explicitly added to the circuit description. Worst case parasitic capacitances are used. The latch waveform used for the simulation is a 1350 nanosecond ramp with a slope equal to the slope at the beginning of the exponential latch waveform, (see Figure 3.3.1.3) used during experimental tests. With reference to Figure 3.3.1.2 the sequence used

to simulate the latching operation may be explained as follows.

Figure 3.3.1.2

Model Used For Latching Operation Simulation

Transistors MISN1 and MISN2 are always held off. They are included in the circuit description to include their contribution to junction capacitance, (included in Table 3.3.1.1). Normally transistors MISP3 and MISP4 are used to precharge the bit lines to the same potential preceeding a read operation, however they may also be used to set up a voltage imbalance across the sense amplifier to test its sensitivity. Transistors MISP3 and MISP4 are turned on thus transferring a voltage imbalance between nodes 5 and 6 to nodes 3 and 4. These transistors are then shut off leaving

the sensing nodes floating. Node 9 is then ramped to VSS thus completing the latching operation. Simulations show the sensitivity of the sense amplifier to be between 0.5mV and 1mV. By adding the threshold imbalance of 2mV the worst case sensitivity becomes 3mV. This figure does not include the effect of noise. This sensitivity compares favourably with the 15mV sense amplifier sensitivity of a recent 256K DRAM design by Fujitsu [7].

By avoiding the use of isolating transistors between sense amplifiers and bit lines, (refer to Section 4.4), the sensitivity may be improved further. As will be shown in Section 3.3.2, the bit line capacitance is identical for both sides of the sense amplifier. Without the isolating transistors the sensing node capacitance would include bit line capacitance and thus the capacitive imbalance of the sense amplifier would be less significant.

A schematic of the circuit used to obtain experimental results for sense amplifier sensitivity using packaged devices is shown in Figure 3.3.1.4. A small voltage imbalance is set up across the sensing nodes by gating the precharge transistors. The precharge transistors are then shut off leaving the sense nodes floating. The latch node is then brought to VSS using the exponential waveform shown in Figure 3.3.1.3. One bit line should then be pulled to VSS and the resulting potential difference between the two bit lines be observed at the output of a comparator connected to the bit lines with the column decoder. As

stated earlier the latching waveform shown in Figure 3.3.1.3 is slow enough to prevent excessive off-side conduction yet fast enough to prevent loss of voltage imbalance due to capacitive discharge. The range of latching times which satisfy these two constraints is quite large thus the waveform does not have to be accurately controlled.

Figure 3.3.1.3

Latching Waveform Used For Experimental Tests

Table 3.3.1.1 shows that the left sensing node has a higher capacitance than the right sensing node. To achieve charge balance between the two nodes the right node is

charged to 5V and the left node is charged to 5V minus a small offset, dV , determined by a precision voltage source, (illustrated in Figure 3.3.1.4). To compensate for threshold imbalances in the cross-coupled transistor pair forming the sense amplifier the offset must be increased or decreased slightly depending upon which transistor has the higher threshold voltage. At this point the offset determined by the precision voltage source represents the sense amplifier sensitivity. The latch node is then lowered to VSS resulting in an equal probability of the sense amplifier toggling either way. The isolating transistors are then turned on and the output observed. The offset voltage was adjusted until the output randomly toggled between two states as shown in Figure 3.3.1.7. This offset voltage represents the sense amplifier sensitivity which was observed to be approximately 8mV. Actually Figures 3.3.1.6 to 3.3.1.8 represent the next case to be considered where the isolating transistors are always biased on, however the same sensitivity and a similar toggling effect were observed for both cases.

A test was then performed with the isolating transistors left on through out the test cycle. As shown in Figure 3.3.1.4 the gates of the isolating transistors are held at 7V to prevent any threshold voltage loss between the sensing nodes and bit lines. If the gates of the isolating transistors are held at 5V it takes too long to precharge both bit lines to the same level following a latching operation.

This long precharge time results from the isolating transistors going into cut-off as soon as the bit lines are charged to one threshold below the gate voltage of these transistors. The total sense amplifier capacitive imbalance with these transistors always on now includes the capacitive imbalance of the column access I/O cell, (refer to Figure A.16 for a mask level plot of this cell). This cell contributes 4fF more capacitance on the right bit line than on the left bit line. Thus the polarity of the sense amplifier capacitive imbalance is now reversed. The right node, which previously had a capacitance 2fF lower than the left node, now has a capacitance 2fF higher than the left node. Note that although the capacitive imbalance is now reversed, the threshold voltage mismatch between the cross-coupled transistor pair forming the sense amplifier will remain the same assuming the same sense amplifier is tested. Therefore the net sense amplifier sensitivity should be lesser or greater than the sensitivity with the isolating transistors gated by an amount approximately equal to the threshold voltage mismatch. By following the same steps as taken in the previous case, apart from gating the bit line isolating transistors, the sense amplifier sensitivity was once again found to be 8mV however the polarity of the required initial voltage offset was reversed. The test setup is shown in Figure 3.3.1.5. Results from sensitivity tests with the bit line isolating transistor always biased on are shown in Figures 3.3.1.6 to 3.3.1.8. Figure 3.3.1.7 illustrates the

case where the offset voltage equals the sense amplifier sensitivity with the output randomly toggling between states. Figures 3.3.1.6 and 3.3.1.8 illustrate a stable output with the offset voltage lesser than and greater than the sense amplifier sensitivity respectively. The four traces shown in each of these figures correspond to the nodes labelled on the schematic of the test setup shown in Figure 3.3.1.4.

The polarity of the sense amplifier sensitivity reversed as expected when the effective capacitance imbalance was reversed. However, it was expected that the sensitivity would change by an amount equal to the threshold voltage imbalance of the cross coupled transistor pair. The fact that it did not change suggests that the sense amplifier sensitivity obtained in both cases was a result of capacitance imbalance only. As previously discussed threshold voltage variations will affect the sense amplifier sensitivity only if the initial voltage imbalance across the sense amplifier is less than the threshold voltage imbalance or if off-side conduction occurs. The discrepancy between the theoretical and measured sensitivities is most likely due to noise. Noise will discharge the sensing nodes to some degree thus reducing the actual voltage imbalance at the sense amplifier from the imbalance determined by the precision voltage source. Since all timing was generated off chip there was a problem with noise while performing the test. Ringing was observed on all of the timing signals due

to impedance mismatches between the timing signal generator, (Tektronix 9100 digital analysis system), and the test jig. This problem was reduced by increasing the capacitance that the timing signal generator had to drive thereby slowing down the signal transition time. Other noise sources may be from power supply fluctuations, pick up from surrounding test equipment or any ringing still remaining on the timing signals. The experimental results show that the sense amplifier sensitivity is less than or equal to 8mV including test jig noise. Since the noise associated with this test is considered to be greater than that of an actual 64K DRAM design the feasibility study will proceed assuming the theoretical sense amplifier sensitivity of 3mV.

Figure 3.3.1.4

Schematic Of Setup Used To Test Sense Amplifier Sensitivity

Figure 3.3.1.5

Test Setup

Column Enable
Bit Line Precharge
Latch Node

Output

Figure 3.3.1.6

Sense Amplifier Response With Initial Offset
Voltage Less Than 8mV

Column Enable
Bit Line Precharge
Latch Node

Output

Figure 3.3.1.7

Sense Amplifier Response With Initial Offset
Voltage Equal To 8mV

Figure 3.3.1.8

Sense Amplifier Response With Initial Offset
Voltage Greater Than 8mV

3.3.2 Bit Line Capacitance

Since the bit lines are populated with memory cells alternately oriented 180 degrees from each other, there should be no difference in capacitance between any two bit lines, (refer to Figure A.10 and A.11 for a mask level plot of the small and large memory cells respectively). This holds true for either the open or folded bit line approach. Any mask misalignment or over/under etching of layers produce equal effects on any bit line. Local variations in oxide thickness are also insignificant as the bit line will be approximately 5000 microns long assuming a 64K DRAM design using the large memory cells.

The nominal and worst case bit line capacitances for both the structure using small memory cells and the structure using large memory cells appears in Table 3.3.2.1. The total capacitance is broken down into a fixed and a voltage bias dependent junction capacitance since this information is required for simulating charge sharing effects in Section 3.6.

In Table 3.3.2.1 the following relationship holds:

$$\text{Total} = \text{Fixed} + \text{Junction}(0.6/(\text{Vr}+0.6))^{**1/2}$$

Where Vr is defined as the reverse bias junction voltage.

For the 64K DRAM feasibility study the large memory cells will be used with a bit line loading of 128 memory

		Structure With Small Cells		Structure With Large Cells	
		nominal	worst case	nominal	worst case
Capacitance		(fF/bit)	(fF/bit)	(fF/bit)	(fF/bit)
Fixed		1.98	2.22	4.76	5.33
Junction (zero bias)		4.73	5.50	7.71	8.91
Total	Vr=0V	6.71	7.72	12.47	14.24
	Vr=5V	3.53	4.02	7.28	8.25

Table 3.3.2.1
Bit Line Capacitance

cells per bit line. Therefore the bit line capacitance will be:

$$\text{Nominal: } C_{bl} = 609 + 987(0.6/(V_r + 0.6))^{1/2} \text{ fF}$$

$$\text{Worst case: } C_{bl} = 682 + 1140(0.6/(V_r + 0.6))^{1/2} \text{ fF}$$

3.3.3 Memory Cell Storage Capacitance

The nominal and worst case memory cell storage capacitance for both the small and large memory cells appears in Table 3.3.3.1. The total capacitance is again broken down into a fixed and a voltage bias junction capacitance since this information is required for simulating charge sharing effects in Section 3:6.

		Small Memory Cell		Large Memory Cell	
		nominal	worst case	nominal	worst case
Capacitance		(fF)	(fF)	(fF)	(fF)
Fixed		14.9	11.9	58.4	51.4
Junction (zero bias)		7.1	5.9	19.0	16.1
Total	Vr=0V	22.0	17.8	77.4	67.5
	Vr=5V	17.2	13.8	64.6	56.7

Table 3.3.3.1
Memory Cell Storage Capacitance

In Table 3.3.3.1 the following relationship holds:

$$\text{Total} = \text{Fixed} + \text{Junction}(0.6/(\text{Vr}+0.6))^{**1/2}$$

Where Vr is defined as the reverse bias junction voltage.

For the 64K DRAM feasibility study the large memory cells storage capacitance will be:

$$\text{Nominal: } C_s = 58.4 + 19.0(0.6/(\text{Vr}+0.6))^{**1/2} \text{ fF}$$

$$\text{Worst case: } C_s = 51.4 + 16.1(0.6/(\text{Vr}+0.6))^{**1/2} \text{ fF}$$

The worst case difference in storage capacitance between two memory cells due to process variations will be 4.1fF for either the small or large memory cells. This difference results from polysilicon to device well misalignment only since the storage capacitance of all memory cells

track each other with respect to polysilicon, and metal mask over/under etching and gate oxide thickness variations.

3.4 Reference Cell Schemes

3.4.1 Introduction

As stated in Section 2.3, an accurate reference level is required which will compensate for the following:

- i) Changes in power supply voltage.
- ii) Leakage due to thermal generation.
- iii) Memory cell access gate to bit line capacitive coupling.
- iv) Process variations.
- v) Bit line noise.

To achieve this a reference cell, similar to the memory cell is used. One row of reference cells is used for each array of memory cells.

With a p-type memory cell a logical 1 is represented by a discharged capacitor. During a read operation, assuming a precharged high bit line the memory cell will transfer zero charge to the bit line for a logical 1 and a small amount of charge for a logical 0. The reference cell must transfer an amount of charge to an adjacent bit line, (both of these bit lines are input to one sense amplifier), equal to half of

the charge produced by reading out a logical 0. The reference cell may be thought of as storing a logical 1/2. Two common approaches to designing such a reference cell will now be described.

3.4.2 C/2 Reference Scheme

With this scheme the reference cell is comprised of an access transistor similar to the one used in the memory cells, a storage capacitor whose capacitance is half the storage capacitance used in the memory cell and a reset transistor. Refer to Figure 3.4.2a for a mask level sketch of this reference cell and Figure 3.4.2b for the corresponding schematic.

From the relationship, $Q=CV$, it is apparent that it takes half as much charge from a precharged bit line to charge a discharged reference cell of capacitance $C/2$ than it does to charge a discharged memory cell of capacitance C .

The advantage of this scheme is that the reference voltage can be generated very quickly by simply discharging the storage capacitor of the reference cell. Another advantage is that since the reference cells storage capacitor is discharged when reset one need not worry about losing the reference charge by thermal generation, or other leakage sources or ionizing alpha particle radiation, (alpha particle radiation is treated in Chapter 5).

Figure 3.4.2a

Mask Level Sketch Of C/2 Reference Cell

Figure 3.4.2b

Schematic Of C/2 Reference Cell

The disadvantage of this scheme is that it is very hard to make an accurate reference cell whose storage capacitance is half that of the memory cell. Since the memory cell is usually designed with the design rules taxed to their limit the reference cell can not be a scaled down version of the memory cell. The storage capacitance of the memory cell is the sum of an oxide capacitance, a planar junction capacitance and a side wall junction capacitance. The storage capacitance of the reference cell may still be the sum of the above mentioned capacitance components but the percentage of the total capacitance contributed by each component will be different. This makes this cell very process sensitive as changes in oxide thickness, mask alignment, over/under etching of masks and variations in diffusion concentrations and depths all will influence the storage capacitance of the reference cell differently than the storage capacitance of the memory cell.

3.4.3 V/2 Reference Scheme

With this scheme the reference cell is electrically and physically identical to the memory cell with which it is used. Refer to Figure A.9 for a schematic of the memory cell and Figures A.10 and A.11 for mask level plots of the small and large memory cells respectively.

If we neglect for the moment that the storage capacitance has a voltage dependent junction component then from the relationship, $Q=CV$, one can see that the same amount of charge is required from the bit line to discharge a capacitor of capacitance C , initially charged to $V/2$ volts, as is required to charge a capacitor of capacitance $C/2$, initially charged to 0 volts. Actually the storage capacitance of the memory cell and reference cell using the $V/2$ scheme will be slightly different due to the voltage dependent junction capacitance component. This will be accounted for in the simulations of capacitive coupling and charge sharing in Section 3.6.

To generate an accurate $V/2$ level to store in the reference cell the usual approach is to charge one bit line, discharge an adjacent bit line and then connect the two bit lines together. This $V/2$ value is then written into the reference cells on both bit lines. Since the capacitance of any two bit lines is the same, (as previously discussed in Section 3.3.2), charge sharing between the two bit lines

will indeed produce an accurate $V/2$ level independent of any process variations.

One advantage of this scheme is that the memory cells and reference cells track each other with respect to process variations. Another advantage is that if thinner or different dielectrics become available the devices could be manufactured with the same photomask set since the reference cell would not have to be redesigned. This is advantageous when developing the DRAM since making new masks is expensive and increases the time required to develop the DRAM.

There are two disadvantages to this scheme. The first is that the time required to generate the reference voltage is greater with this scheme than with the $C/2$ reference scheme. The second disadvantage is that the $V/2$ reference scheme is not soft error immune. The resulting increase in soft error rate is very small since the small area of the reference cell within which an alpha particle must strike and the short time span that the reference voltage is held, make the probability of a successful strike very low. Further discussion of alpha particle induced soft errors may be found in Chapter 5.

Based on the ability for the $V/2$ reference scheme to track process changes and allow for process modifications this reference scheme is considered to be the best choice.

3.5 Thermal Generation

3.5.1 Introduction

Since there is no feedback in a DRAM memory cell one stored logic state will eventually decay into the other state. Since p-type memory cells are being used, the logical 0 state, (storage capacitor depleted), is unstable. One mechanism for the decay of the unstable state is by collection of thermally generated carriers. The other mechanism is by collection of carriers generated by ionizing radiation, (refer to Chapter 5 for details).

To get an estimate of the signal margin loss due to thermal generation, data from an experiment [8] with a gated diode electrometer is used. A gated diode electrometer is a structure used to measure low leakage currents, (shown in Figure 3.5.1.1). Its operation will now be described. A p+n diode is formed by a p+ junction in an n-type substrate. The cathode, (substrate), is always at VDD. The anode, (p+ diffusion), is charged to VSS by turning on the access transistor with a precharge line. This reverse biases the diode, thus setting up an unstable state which will decay by leakage due to thermal generation. By using the equation, $I = C(V)(dV/dt)$, the leakage current can be derived by measuring the rate of voltage decay across the reverse biased diode and by calculating the capacitance of the diode. The anode voltage shown as V_r in Figure 3.5.1.1 is measured by a

source follower. To cancel out the characteristics of this source follower a second source follower is used. The source voltage of the source follower shown on the left side of Figure 3.5.1.1 is tracked by the source follower on the right side due to the negative feedback applied to the operational amplifier. The output of the operational amplifier is then monitored giving the anode voltage of the diode. It should be noted that the diode capacitance changes as the reverse bias voltage decays. By calculating the voltage drop over a very short time period the change in capacitance may be neglected. Also the leakage decreases as the reverse bias voltage decays thus a worst case situation is assumed by calculating leakage when the junction has a maximum reverse bias voltage.

Leakage current data were available for a p+n gated diode isolated from the field oxide periphery by a surrounding gate ring biased into accumulation for 23 degrees Celsius and 75 degrees Celsius, (see Figures 3.5.1.2 and 3.5.1.3).

To include leakage from the field oxide edge the gate ring was inverted and a new junction area calculated. The field induced junction leakage under the gate is included as metallurgical junction leakage but scaled appropriately to account for the different depletion layer width. Surface generation leakage under the gate is not significant in strong inversion thus it does not have to be included. Leakage at a field oxide edge should be higher than at a

Figure 3.5.1.1

Gated Diode Electrometer Schematic

Figure 3.5.1.2
Cross-Section Of Gated Diode Structure

Figure 3.5.1.3
Orthogonal View Of Gated Diode Structure

gate edge due to an increase in stacking faults introduced by the nitride mask used to define the device well.

Leakage data with the field oxide edge effects included were available for 23 degrees Celsius but not for 75 degrees Celsius. To estimate a leakage rate for 75 degrees Celsius a scaling factor is applied to the data for 23 degrees Celsius. The scaling factor is calculated from the increase in leakage current versus temperature using the experimental data obtained with the gate ring biased into accumulation. This assumes that the junction leakage and peripheral leakage have similar characteristics with respect to temperature.

The following assumptions are made to estimate signal loss due to thermal generation.

- i) A refresh cycle occurs every four milliseconds. This refresh period is chosen to conform with conventional standards.
- ii) The storage node junction is reverse biased by 5V. This represents a worst case situation and will only occur if the word line is bootstrapped to avoid threshold losses when writing data into the cell. Another consideration is that data were not available for a reverse bias of one threshold below VDD.
- iii) Nominal junction capacitance is assumed since this is used when interpreting the gated diode

results. A change in junction area due to process variations will not significantly change the rate of voltage decay in the memory cell since voltage decay rate is equal to the leakage current divided by the capacitance, both of which are directly proportional to the junction area.

$$dV/dt = (I/A)/(C/A)$$

- iv) The storage capacitance after four milliseconds is approximately equal to the initial storage capacitance. This will be verified in Section 3.5.2 after the leakage calculations.
- v) The leakage rate is assumed to be constant even as the reverse bias on the junction decreases. Actually the leakage will decrease as the reverse bias decreases so this assumption adds a margin of safety. Also the reverse bias voltage does not change appreciably over the time period in concern as will also be verified after the leakage calculations.

3.5.2 Leakage Calculations

Leakage rates determined from the gated diode electrometer measurements [8] are first summarized. The leakage

rates for the small memory cell, large memory cell and the reference cell are then inferred.

The leakage rate of a junction at a tapered field oxide edge is affected by nitride defects. The nitride defects come from the nitride mask used to define the device well. These defects act as generation/recombination sites thus increasing the leakage. For this reason it was considered necessary to consider the leakage rate of a junction bounded by field oxide separately from a junction bounded by a gate. Subsequently this will permit the separation of leakage associated with the junction from leakage associated with nitride defects along the field oxide periphery. Table 3.5.2.1 presents leakage current data for a junction not bounded by field oxide. To obtain these results the gate ring, (refer to Figures 3.5.1.2 and 3.5.1.3), was biased into accumulation to separate diode A, (inner junction), from diode B, (outer field oxide bounded junction).

Temp.	Leakage Current (I)	Junction Area (A)	Leakage per Area (I/A)
(°C)	(pA)	(μm^2)	(pA/ μm^2)
23	1.2	205,426	5.842E-6
75	213.0	205,426	1.037E-3

Table 3.5.2.1

Leakage Data For Gate Bounded Junction

To get data for a junction bounded by field oxide the gate ring was biased into strong inversion. The leakage under the gate is then included as metallurgical junction leakage but scaled to account for the different depletion layer width. The following equations show the dependence of metallurgical junction leakage, ($I_{gen,MJ}$), and field induced junction leakage under the gate, ($I_{gen,FIJ}$), on depletion layer width, (W), and junction area, (A).

$$I_{gen,MJ} = (qXn_iXW_{MJ}A_{MJ})/\tau_g$$

$$I_{gen,FIJ} = (qXn_iXW_{FIJ}A_{FIJ})/\tau_g$$

$$\begin{aligned} \text{Channel area} &= \text{polysilicon gate area} \\ &\quad - \text{p+ side diffusion area under the gate} \\ &= 49,710 \mu\text{m}^2 \\ &\quad - 1,342 \mu\text{m}^2 \\ &= 48,368 \mu\text{m}^2 \end{aligned}$$

$$\begin{aligned} \text{Effective junction area} &= \text{area inside gate (diode A)} \\ &\quad + \text{area outside gate (diode B)} \\ &\quad + \text{channel area X } (W_{FIJ}/W_{MJ}) \\ &= 205,426 \mu\text{m}^2 \\ &\quad + 77,915 \mu\text{m}^2 \\ &\quad + 48,368 \times (1.89/0.75) \mu\text{m}^2 \\ &= 405,066 \mu\text{m}^2 \end{aligned}$$

$$\text{Field oxide periphery} = 2,300 \mu\text{m}^2$$

Diodes A and B are shown in Figures 3.5.1.2 and 3.5.1.3. By using the data from Table 3.5.2.1 leakage data for a junction bounded by field oxide may be separated into leakage dependent on the junction area and leakage dependent on the length of the junction periphery where nitride defects are prominent. These results are presented in Table 3.5.2.2.

Temp.	Total Leakage Current	Estimated Junction Leakage Current	Net Peripheral Leakage Current	Net Peripheral Leakage per Length
(°C)	(pA)	(pA)	(pA)	(pA/μm)
23	3.0	2.366	0.634	2.757E-4
75	533.0	420.0	113.0	4.910E-2

Table 3.5.2.2

Leakage Data for Field Oxide Bounded Junction

Leakage calculations are now performed for the memory and reference cells. The total junction area will include the area under the capacitor plate which is implanted separately from the source/drain junctions. The leakage rate of the junction under the capacitor plate and the source and drain junctions are assumed to be the same. SUPREMEII simulations show that the junction depth is within 5% of the junction depth of the source and drains. Peripheral leakage will be calculated separately from junction leakage. The total leakage current will then be calculated and the voltage drop of the logical 0 state in the memory cell will be derived assuming a four millisecond refresh cycle.

For the small memory cell:

Junction area = $51.2 \mu\text{m}^2$
 Field oxide bounded junction length = $19.2 \mu\text{m}$
 Storage capacitance, (Cs) = 17.2 fF

At 23 degrees Celsius:

Junction leakage = $5.842\text{E-}6 \text{ pA}/\mu\text{m}^2 \times 51.2 \mu\text{m}^2$
 = $3.0\text{E-}4 \text{ pA}$
 Peripheral leakage = $2.757\text{E-}4 \text{ pA}/\mu\text{m} \times 19.2 \mu\text{m}$
 = $5.3\text{E-}3 \text{ pA}$
 Total leakage = $3.0\text{E-}4 \text{ pA} + 5.3\text{E-}3 \text{ pA}$
 = $5.6\text{E-}3 \text{ pA}$

Voltage drop = $(I/\text{Cs})(dt)$
 = $(5.6\text{E-}15 \text{ A}/17.2\text{E-}15 \text{ F})(4\text{E-}3 \text{ sec.})$
 = $1.3\text{E-}3 \text{ V}$

At 75 degrees Celsius:

Junction leakage = $5.3\text{E-}2 \text{ pA}$
 Peripheral leakage = $9.4\text{E-}1 \text{ pA}$
 Total leakage = $9.9\text{E-}1 \text{ pA}$

Voltage drop = $2.3\text{E-}1 \text{ V}$

For the large memory cell:

Junction area = $136.3 \mu\text{m}^2$
 Field oxide bounded junction length = $43.8 \mu\text{m}$
 Storage capacitance = 64.6 fF

At 23 degrees Celsius:

Junction leakage = $7.8\text{E-}4 \text{ pA}$
 Peripheral leakage = $1.2\text{E-}2 \text{ pA}$
 Total leakage = $1.3\text{E-}2 \text{ pA}$

Voltage drop = $8.0\text{E-}4 \text{ V}$

At 75 degrees Celsius:

Junction leakage = $1.4\text{E-}1 \text{ pA}$
 Peripheral leakage = 2.2 pA
 Total leakage = 2.3 pA

Voltage drop = $1.4\text{E-}1 \text{ V}$

There is no leakage due to thermal generation in the C/2 reference scheme. With the V/2 reference scheme the leakage should be approximately the same as the leakage in a memory cell since the junction areas are the same and the capacitances are within 5%, (this difference is due to the different reverse bias junction voltage for the reference cell compared to the memory cell).

A summary of voltage loss due to thermally generated leakage currents is shown in Table 3.5.2.3.

Temp.	Small Memory Cell	Large Memory Cell
(°C)	(V)	(V)
23	1.3E-3	0.8E-3
75	0.23	0.14

Table 3.5.2.3
Thermal Generation Losses

The following will verify the assumption that the reverse bias voltage will not change appreciably and that junction capacitance will remain approximately constant after four milliseconds.

Initially:

$$C_s = (0.6/(5.00+0.6))^{**1/2}$$

$$= 0.3273$$

After four milliseconds:

$$C_s = (0.6/(4.86+0.6))^{**1/2}$$

$$= 0.3315$$

Therefore the change in junction capacitance will be:

$$1 - (0.3273/0.3315) = 1 - 0.987 = .013 = 1.3\%$$

Other leakage sources are also present. There will be a small amount of subthreshold leakage through the memory cell access transistor. Subthreshold leakage between memory cells is also possible due to parasitic transistors formed with the capacitor plate acting as the gate.

3.6 Capacitive Coupling And Charge Sharing Effects

3.6.1 Introduction

Capacitive coupling from the gate of a memory cell access transistor to its storage capacitor occurs when data are written into and read from the cell. The coupling effects during a write and read operation do not always cancel each other out. The net difference between coupling effects may be comparable to the signal loss in the memory cell due to thermal generation. As an example consider the case illustrated in Figures 3.6.1.1 and 3.6.1.2 where a logical 0 value is written into a p-type memory cell. Gate to source coupling is only important when the transistor is off, otherwise the source will be clamped to the bit line through the access transistors channel. When a logical 0 is written into a p-type memory cell, the transistor cuts off. The source, (storage node), will thus be affected by coupling for 100% of the gate transition from 0V to 5V. If the

bit line is subsequently charged to 5V and then the memory cell connected to the bit line, (during a read cycle), the bit line will become the transistors source and the transistor will turn on when the gate is lowered to one threshold below 5V. In this case coupling will affect the stored signal in the memory cell for only a fraction of the gate transition from 5V to 0V.

The net coupling effects may be eliminated by ensuring that the source of the memory cell access transistor does not switch from the storage capacitor to the bit line. With p-type memory cells this may be accomplished by precharging the bit line to 0V before a read operation. As will be shown later precharging the bit line to 0V will also give the largest signal margin.

The model used for simulating coupling includes all parasitic capacitances between the gate, storage node and bit line as well as coupling due to gate to source and gate to drain fringing fields. These are added to an existing model used with SCAMPER which already includes gate to source and gate to drain coupling due to source and drain side diffusion under the gate.

The results of simulation studies of coupling effects for the test chip are given in the following section. These are compared with measured results. For simplicity and ease of interpretation, coupling and charge sharing effects are included together when simulating a read operation.

Figure 3.6.1.1
Capacitive Coupling During Write Operation

Figure 3.6.1.2
Capacitive Coupling During Read Operation

Simulation investigations of coupling effects for a 64K DRAM are also presented.

3.6.2 Coupling Effects For The Test Chip

The reader is reminded that the test chip consists of two structures, one using small memory cells and the other using large memory cells. Each structure contains three groups of memory cells each with a different bit line loading, (number of memory cells per bit line).

A write operation will first be simulated. This gives the resulting stored voltage in the memory cell after including the gate to storage capacitor coupling. Since the test chip experiments were performed at room temperature with a cycle time much less than the standard four millisecond refresh cycle, no significant memory cell voltage loss will occur, (refer to Section 3.5 for an estimate of memory cell voltage loss over a four millisecond refresh cycle). The resulting stored voltage is then used as an initial condition to simulate capacitive coupling and charge sharing effects during a read operation.

The model used to simulate capacitive coupling during a write operation is shown in Figure 3.6.2.1. The source file and output for SCAMPER simulations of the structure using large memory cells are given in Appendix D. The model shown in Figure 3.6.2.1 includes capacitors to represent fringing fields, (C_{gd} and C_{gs}), as well as layout dependent parasitic

capacitances, (C_{btw} and C_{bts}). The storage capacitance is broken into two components, one fixed and the other voltage dependent. The voltage dependent capacitance is modelled with a FORTRAN subroutine for use with SCAMPER. This routine is also included in Appendix D.

Figure 3.6.2.1

Model Used To Simulate Capacitive
Coupling During A Write Operation

During a write operation the coupling from the gate of a memory cell to its storage capacitor is not a function of bit line capacitance. Therefore simulated results shown in Table 3.6.2.1 apply to all of the three memory cell groups

which have different bit line loadings. The word line waveform used to obtain the data in Table 3.6.2.1 is shown in Figure 3.6.2.2.

	Structure with Small Memory Cells		Structure with Large Memory Cells	
	(Volts)		(Volts)	
Vbl	0.000	5.000	0.000	5.000
Vstor(t1)	1.531	5.000	1.623	5.000
Vstor(t2)	1.976	5.160	1.772	5.087

Table 3.6.2.1
Simulated Coupling Effects During
Write Operation For Test Chip

Figure 3.6.2.2
Word Line Waveform Used For
Simulation Of Write Operation

The model used to simulate capacitive coupling and charge sharing effects during a read operation is shown in Figure 3.6.2.3. It is similar to the model shown in Figure 3.6.2.1 except a fixed, (C_{bl}), and a voltage dependent, (C_{jn2}), bit line capacitance are included and the bit line is floating.

Figure 3.6.2.3

Model Used To Simulate Capacitive
Coupling And Charge Sharing During A Read Operation

2

The value of $V_{stor}(t_2)$ from Table 3.6.2.1 is used as an initial condition to simulate a read operation. The source file and output for one of the SCAMPER simulations of a read operation are given in Appendix E. Simulated results are shown in Tables 3.6.2.2 and 3.6.2.3 with the word line waveform shown in Figure 3.6.2.4.

Figure 3.6.2.4

Word Line Waveform Used For
Simulation Of Read Operation

	8 Small Cells Per Bit Line		16 Small Cells Per Bit Line		32 Small Cells Per Bit line	
	Logical 0	Logical 1	Logical 0	Logical 1	Logical 0	Logical 1
	(Volts)	(Volts)	(Volts)	(Volts)	(Volts)	(Volts)
Vstor(t2)	1.976	5.160	1.976	5.160	1.976	5.160
Vbl(t2)	5.000	5.000	5.000	5.000	5.000	5.000
Vbl(t3)	3.443	4.427	3.986	4.625	4.415	4.780
Vbl(t3) -Vbl(t2)	-1.557	-0.573	-1.014	-0.375	-0.586	-0.220
Voltage Imbalance	0.984		0.639		0.366	

Where: Voltage Imbalance = (Vbl(t3)-Vbl(t2) for logical 1)
 -(Vbl(t3)-Vbl(t2) for logical 0)

Table 3.6.2.2
 Simulated Coupling And Charge Sharing Effects
 For Read Operation With Test Structure Using Small Cells

	8 Large Cells Per Bit Line		16 Large Cells Per Bit Line		32 Large Cells Per Bit Line	
	Logical 0	Logical 1	Logical 0	Logical 1	Logical 0	Logical 1
	(Volts)	(Volts)	(Volts)	(Volts)	(Volts)	(Volts)
Vstor(t2)	1.772	5.087	1.772	5.087	1.772	5.087
Vbl(t2)	5.000	5.000	5.000	5.000	5.000	5.000
Vbl(t3)	3.282	4.732	3.856	4.820	4.327	4.892
Vbl(t3) -Vbl(t2)	-1.718	-0.268	-1.144	-0.180	-0.673	-0.108
Voltage Imbalance	1.450		0.964		0.565	

Where: Voltage Imbalance = (Vbl(t3)-Vbl(t2) for logical 1)
-(Vbl(t3)-Vbl(t2) for logical 0)

Table 3.6.2.3
Simulated Coupling And Charge Sharing Effects
For Read Operation With Test Structure Using Large Cells

By using a Model 18 Picoprobe, (20fF tip), to probe the metal bit line, the functionality of the memory cell was confirmed. The bit line voltage change as a result of a read operation was also measured. By calculating the difference in the measured bit line voltage change for a logical 1 against a logical 0 the voltage imbalance can be determined. The observed voltage imbalance for the various bit line loadings may then be compared to the theoretical values given in Tables 3.6.2.2 and 3.6.2.3.

The timing signals used to obtain the experimental data were generated with the circuit shown in Figure 3.6.2.5a. The timing signals, namely VIN, TR and WD along with the clocks used to generate these signals are shown in Figure

3.6.2.5b. The signals VIN, TR and WD correspond to the signals shown on the schematic of the setup used to test the memory cell performance illustrated in Figure 3.6.2.6.

The operation of the circuit used to generate the timing signals may be explained as follows. A binary ripple counter, (4020), is used to produce a master clock, (MC), plus two clocks whose frequencies are half, (MC/2), and a quarter, (MC/4), of the master clock. The MC clock and the inverted MC/2 clock are used as inputs to a NAND gate to produce the word line signal, (WD). The MC/2 inversion also adds a delay to prevent glitches from being generated on the WD signal. The MC and MC/4 clocks are used to produce the signal, (TR), for the gate of the bit line isolating transistor. A level translator increases the swing of the TR signal from 5V to 7V so that a full 5V may be passed through the bit line isolating transistor. Finally the MC clock is fed into a divide by 10 counter, (4017), to produce the signal, (VIN), which provides the input data as well as the bit line precharge level used prior to a read operation. The divide by 10 counter is arranged to reset on the fourth count giving the VIN signal a duty cycle one fourth that of the master clock. To obtain the proper phase relationship between VIN and MC the output from the 4017 counter is chosen after the circuit is powered up. The VIN signal is delayed from the master clock and thus from the TR signal to ensure that the VIN signal does not change before the bit line isolating transistor, controlled by TR, shuts off.

The experiment used to test the functionality of the memory cells and to determine the resulting voltage change on the bit line during a read operation will now be described. A logical 0 is written into the memory cell; the bit line is charged up to 5V; then the memory cells access transistor is turned on resulting in charge sharing between the memory cells storage capacitor and the capacitance associated with the bit line. The test is then repeated with a logical 1 written into the memory cell. The difference between the bit line voltage change when reading a logical 1 compared to reading a logical 0 gives the voltage imbalance across the sense amplifier which would result if a pair of bit lines were simultaneously used by one sense amplifier, (as is normally done), to compare the state of a memory cell against a reference level, (in this case another memory cell). The resulting voltage imbalance for the three different memory cell sizes may then be compared against the values obtained from simulations given in Tables 3.6.2.2 and 3.6.2.3.

The experimental results are shown in Figures 3.6.2.7 to 3.6.2.18. These photographs show the bit line voltage change resulting from reading out a logical 0 and a logical 1 for each of the different bit line loadings used for the small and the large memory cells. The photographs also show the relationship between the bit line voltage and the signals VIN, TR and WD which are also shown on the schematic given in Figure 3.6.2.6. The probe used to measure the bit

line response was later confirmed to be leaking excessively thus the uniform decay of the bit line voltage towards 0V shown in the photopgraphs should be ignored. Since the probe used to obtain the bit line response had a gain of 10, the vertical scale shown in the photographs as 100mV/division is actually 1V/division. These photographs show the bit line voltage to drop more for a read out of a logical 0 than for a logical 1 as expected. They also show the increase in bit line voltage due to capacitive coupling between the memory cell access gate and the bit line when the memory cell is shut off.

(b)
Figure 3.6.2.5

Circuit Used To Test Functionality Of Memory Cells

Figure 3.6.2.6

Setup Used To Test Memory Cell Performance

Figure 3.6.2.7

Reading Logical 0 With 8 Small Memory Cells Per Bit Line

Figure 3.6.2.8

Reading Logical 1 With 8 Small Memory Cells Per Bit Line

VIN
TR
WD
Bit Line
Response

Figure 3.6.2.9

Reading Logical 0 With 16 Small Memory Cells Per Bit Line

VIN
TR
WD
Bit Line
Response

Figure 3.6.2.10

Reading Logical 1 With 16 Small Memory Cells Per Bit Line

VIN
TR
WD
Bit Line
Response

Figure 3.6.2.11

Reading Logical 0 With 32 Small Memory Cells Per Bit Line

VIN
TR
WD
Bit Line
Response

Figure 3.6.2.12

Reading Logical 1 With 32 Small Memory Cells Per Bit Line

Figure 3.6.2.13

Reading Logical 0 With 9 Large Memory Cells Per Bit Line

Figure 3.6.2.14

Reading Logical 1 With 8 Large Memory Cells Per Bit Line

Figure 3.6.2.15

Reading Logical 0 With 16 Large Memory Cells Per Bit Line

Figure 3.6.2.16

Reading Logical 1 With 16 Large Memory Cells Per Bit Line

Figure 3.6.2.17

Reading Logical 0 With 32 Large Memory Cells Per Bit Line

Figure 3.6.2.18

Reading Logical 1 With 32 Large Memory Cells Per Bit Line

A summary of the simulated voltage imbalance at the sense amplifier from Tables 3.6.2.2 and 3.6.2.3 is given in Table 3.6.2.4. The resulting voltage imbalance determined by inspection of Figures 3.6.2.7 to 3.6.2.18 rounded to the nearest 100mV is given in Table 3.6.2.5.

	Small Cell	Large Cell
	(mV)	(mV)
8 Cells/Bit Line	984	1450
16 Cells/Bit Line	639	964
32 Cells/Bit Line	366	565

Table 3.6.2.4
Simulated Voltage Imbalance At Sense Amplifier

	Small Cell	Large Cell
	(mV)	(mV)
8 Cells/Bit Line	400	600
16 Cells/Bit Line	300	400
32 Cells/Bit Line	200	300

Table 3.6.2.5
Measured Voltage Imbalance At Sense Amplifier

The discrepancy between the measured and simulated results for voltage imbalance at the sense amplifier is due to the defective probe loading down the bit line. It is also quite probable that the fabrication process conditions were not nominal thus further contributing to the discrepancy. Due to the limited availability of the Model 18 Pico-probe at the time this experiment was performed the test could not be repeated. The measurements prove that the memory cell is functional since it is able to remain in an unstable state for a finite period of time. By inspecting the photographs in Figures 3.6.2.7. to 3.6.2.18 one can see that the memory cell can retain a reasonable amount of charge for 1.5 microseconds. The photographs also show that the bit line voltage started to drop as soon as the bit line isolating transistor, controlled by TR, was shut off even though VIN was still high. This proves that the apparent bit line leakage was not through the bit line isolating transistor. The bit line voltage decay could not be from an excessively leaky bit line since the bit line was already discharged when at 5V, (upper supply rail). By performing measurements with the Picoprobe on test inserts the probe was proven to be leaking excessively.

In light of the fact that the measured results were affected by the leaky probe the simulated results are believed to be more realistic. Thus the same model of the memory cell will be used to simulate the voltage imbalance for a 64K DRAM in the following section.

3.6.3 Coupling Effects For A 64K DRAM

By using the same parasitic and overlap capacitances used to simulate the test chip, but assuming worst case memory cell and bit line capacitance and 128 memory cells per bit line, simulations for a 64K DRAM were performed. The model and the word line waveform used to simulate a write operation are shown in the previous section in Figures 3.6.2.1 and 3.6.2.2 respectively. A source file and output for SCAMPER write operation simulations similar to the ones used for the 64K DRAM simulations are given in Appendix D. Simulation of a write operation was performed to determine the change in storage node voltage, with respect to its initial value, at the end of the gate ramp. The storage node voltage change was determined as a function of bit line voltage and is shown in Figure 3.6.3.1. This figure shows the magnitude of the gate to storage node capacitive coupling and illustrates its dependence on bit line voltage.

With reference to Figure 3.6.3.1, the storage node voltage change is shown to be smallest when writing in 5V. As the bit line is lowered the storage node voltage change increases linearly. This is a result of the memory cell access transistor shutting off sooner thus reducing the time that the storage node is clamped to the bit line. This point was previously illustrated in Figures 3.6.1.1 and 3.6.1.2. The storage node voltage change remains the same for bit line voltages from 0V to 1.5V, (slightly lower than

the threshold voltage of the memory cell access transistor). For this range of bit line voltage the access transistor cuts off when writing data into the memory cell therefore gate to storage node capacitive coupling will change the storage voltage for the entire gate transition from 0V to 5V.

Channel charge also affects the storage node voltage change. For bit line voltages greater than the access transistors threshold voltage channel current continues to flow even after the gate potential is raised to a level that would turn the transistor off. The channel current will continue to flow until the channel charge is used up. This will not occur for bit line voltages less than the access transistors threshold voltage as the access transistor will cut off preventing the flow of channel current.

The model and the word line waveform used to simulate a read operation are shown in Figures 3.6.2.3 and 3.6.2.4 respectfully. A source file and output for SCAMPER read operation simulations similar to the ones used for the 64K DRAM simulations are given in Appendix E. The read operation simulations give the resulting bit line voltage change as a result of gate to bit line and gate to storage node capacitive coupling as well as charge sharing between the storage capacitor and the bit line. The resulting bit line voltage change was determined as a function of initial bitline precharge voltage before the memory cell was accessed. Bit line voltage change is shown in Figure

Figure 3.6.3.1
Gate To Storage Node Coupling During Write Operation
For A 64K DRAM

3.6.3.2 for a logical 0 and a logical 1 stored in a memory cell. Also shown is the bit line voltage change when accessing a reference cell using the $V/2$ reference scheme with 2.5V stored in the cell as well as for a modification to the reference scheme using 3.3V, (half-way between 5V and the threshold voltage of the access transistor). The bit line voltage change at the end of the gate transition from 5V to 0V is shown with a solid line and 20 nanoseconds after the transition with a dashed line. Depending on the initial bit line voltage complete charge transfer between the storage capacitor and the bit line might not occur as the access transistor could eventually cut off. Also charge transfer slows down as the access transistor approaches cut-off. An increase in bit line voltage change thus signal margin is obtainable by waiting for this slow charge transfer process to complete. Figure 3.6.3.2 shows that an increase in signal margin of approximately 30mV is possible by waiting 20 nanoseconds for the charge transfer to occur.

Despite the fact that incomplete charge transfer occurs for an initial bit line voltage of 0V the difference in bit line voltage change between reading a logical 1 and a logical 0 is greater than for an initial bit line voltage of 5V. In fact, this difference is greater even immediately after the gate transition. This increase is a result of the reduction of the voltage dependent junction capacitance associated with the bit line. The optimum initial bit line voltage of 0V also eliminates any difference in gate to

Figure 3.6.3.2

Coupling And Charge Sharing During Read Operation
For A 64K DRAM

storage node coupling for a write operation compared to a read operation, (this was discussed in Section 3.6.1).

Figure 3.6.3.2 also shows that the use of a 2.5V reference level is not desirable unless the word line is bootstrapped to allow 0V to be stored in the memory cell. The optimum reference level is 3.3V, (half-way between 5V and the threshold voltage of the access transistor). This ensures a good balance between the signal margin for a one and the signal margin for a zero. From Figure 3.6.3.2 one can see that 20 nanoseconds after the access transistor is fully on the signal margin for a zero, (difference between the 3.3V reference level and a logical 0), is 98mV and the signal margin for a one, (difference between the 3.3V reference level and a logical 1), is 102mV. These values are reasonable since published data [9] show a typical nominal signal margin, (also referred to as useable signal), to be on the order of 100mV to 300mV.

The peculiar behavior of the resulting bit line voltage change for a stored low may be explained as follows. For initial bit line voltages from 0V to approximately 1.7V the memory cell access transistor is cut off. The bit line initially drops due to gate to bit line coupling, not due to charge sharing between the storage capacitor and bit line. Eventually charge sharing raises the bit line voltage. For initial bit line voltages from approximately 1.7V to approximately 3V charge sharing between the storage capacitor and

bit line lowers the bit line voltage with gate to bit line coupling contributing very little.

We have now established that the optimum 64K DRAM approach should use an initial bit line precharge level of 0V and a reference level of 3.3V. The 3.3V reference level was optimized for nominal process and operating conditions apart from including worst case memory cell and bit line capacitance which affects the signal margin for a one and a zero equally. Under worst case conditions the threshold voltage will increase and the 3.3V reference level will no longer be optimum. Although a reference voltage generator which compensates for threshold voltage changes could be designed the analysis will proceed assuming a fixed reference level of 3.3V.

3.7 Resulting Worst Case Signal Margin

Assuming a worst case process, an operating temperature of 75 degrees Celsius and a supply voltage of 4.5V the worst case signal margin will now be calculated. Following the same procedure used in Section 3.6 to simulate a write operation, using the same model and word line waveform that were given in Figures 3.6.2.1 and 3.6.2.2 respectively, the resulting voltage stored in the memory cell after the gate transition may be determined. The resulting voltages stored in the memory cell for a logical 0 and a logical 1 were found to be 1.987V and 4.598V respectively. The resulting

voltage stored in the reference cell using a 3.3V reference level was found to be 3.442V. These levels will decay towards 4.5V due to thermal generation. From Section 3.5 it was determined that the voltage loss for a large memory cell or reference cell at 75 degrees Celsius would be approximately 0.14V over a standard four millisecond refresh period. The net stored voltage levels after including losses due to thermal generation are used as initial conditions to simulate a read operation. Following the same procedure used in Section 3.6 to simulate a read operation, using the same model and word line waveform that were given in Figures 3.6.2.3 and 3.6.2.4 respectively, the bit line voltage change following the gate transition is determined. Results from this simulation are given in Table 3.7.1.

	Logical 0	Reference Level	Logical 1
	(Volts)	(Volts)	(Volts)
Vstor(t2)	2.127	3.592	4.500
Vbl(t2)	0.000	0.000	0.000
Vbl(t3)	-0.004	0.055	0.109

Table 3.7.1
Results Of Worst Case Read Operation
Simulations For A 64K DRAM

It was previously determined in Section 3.3.1 that the worst case sense amplifier sensitivity is 3mV. By deducting this value from the voltage imbalance determined from Table 3.7.1 the worst case signal margin for a zero and a one are

thus 54mV and 51mV respectively. The signal margin for a one which is the smaller of the two will be used to estimate the worst case maximum latching speed in the following chapter.

CHAPTER 4

LATCHING SCHEMES

4.1 Introduction

Latching speed is inversely, (but not directly), proportional to the initial voltage imbalance across the sense amplifier caused by charge sharing between the memory cells storage capacitor and the bit line. The worst case voltage imbalance determined in Chapter 3 will be used to determine the minimum required latching time after determining the optimum latching scheme to use. The minimum latching time will then be used to estimate the worst case access time for a 64K DRAM.

Due to bit line pitch constraints sense amplifiers usually consist of a simple cross-coupled pair of transistors with a common source which will be referred to as the latch node. The sense amplifiers are regenerative in that an initial small voltage imbalance across the sense amplifier is developed into a large imbalance comparable with the power supply voltage following the latching sequence thereby automatically writing a fully restored signal back into the memory cell. With reference to Figure 4.1.1 the latching sequence will be explained.

A voltage imbalance of dV volts is developed across the sensing nodes, (drains of transistors 1 and 2), as a result

Figure 4.1.1

Regenerative Sense Amplifier

of charge sharing between the bit lines and the reference and memory cells. The latch node is then ramped slowly from VDD to VSS. When the latch node approaches one threshold below the gate of transistor 2 then transistor 2 will turn on thereby discharging bit line 2. As long as the latch node is ramped to VSS slowly enough so that the drain of transistor 2 can follow its source within one threshold then transistor 1 will not turn on. To achieve this without ramping the latch node to VSS unnecessarily slow a complex latch voltage waveform is required which is composed of two logarithmic functions, one for when the sense amplifier is operating in the triode region and one for when the sense

amplifier is in the saturation region, [10]. When the sense amplifier first turns on transistor 2 will be operating in saturation, if the imbalance is less than one threshold voltage. As the latch node continues towards VSS transistor 2 will eventually go into the triode region.

In practice it is impossible to bring the latch node to VSS without having some off-side conduction, (in this case through transistor 1), thus reducing the potential of bit line 1.

There are several factors which will cause the potential of bit line 1 to drop. One factor is that parasitic capacitance between the two sensing nodes as well as between the sensing nodes and the latch node always exists. Thus bit line 1 will follow bit line 2 and the latch node to a small degree.

Another factor is that when sensing the unstable state of the memory cell, (logical 0 for p-type memory cells), both the bit line with the memory cell attached and the bit line with the reference cell attached have previously undergone charge sharing with the memory cell and reference cell respectively. Therefore the off-side does not start off at a full high value to begin with.

To achieve the best signal margin the signal after or during sensing must be restored by pull-up or pull-down devices, depending on whether an n-channel or p-channel sense amplifier is used. Some off-side conduction is tolerable if both the memory cells and sense amplifiers are

designed with the same type of transistor, (i.e. either n-channel or p-channel). As long as the off-side conduction is less than the threshold of the memory cell then no degradation in stored charge will occur. If n-channel sense amplifiers and memory cells are used the bit line is precharged high before a read operation. As the highest value that can be written back into the memory cell is only one threshold below the upper supply rail, some off-side conduction is tolerable.

Although an optimum latching pulse has been described in literature [10], it is not used in practice because of its complexity and due to the fact that the advantage of using this scheme, which is to have no off-side conduction is hard to obtain due to the reasons previously stated in this section. After accounting for process tolerances it is doubtful whether there would be any significant increase in latching speed if such a waveform were used for the latch node. A common approach is to use either one or two ramps at the latch node to approximate the two logarithmic functions. Refer to Figure 4.1.2 for an illustration of the optimum and the commonly used approximation to the latching waveform.

Although an n-channel sense amplifier, as treated in Chapter 3, will have a higher gain than a similar sized p-channel sense amplifier, thus increasing latching speed, the optimum bit line precharge level of $0V$, as determined in the previous chapter, can not be used. A trade off of speed

Figure 4.1.2a
Optimum Latch Waveform

Figure 4.1.2b
Commonly Used Latch Waveform

for noise immunity can be made by using p-channel sense amplifiers and precharging the bit lines to 0V before a read operation.

Several schemes involving isolating transistors between the bit lines and sense amplifiers will now be discussed.

4.2 With P-Channel Isolating Transistors

By using a p-channel equivalent of an n-channel scheme [11], which uses bit line isolating transistors as preamplification stages, a high sensitivity can be achieved. With

reference to Figure 4.2.1 the scheme may be described as follows.

Figure 4.2.1

P-Channel Isolating Transistor Scheme

The only substrate connections which are relevant to this discussion are those of the isolating transistors. Initially the latch node is held low so that the sense amplifier is off. The n-channel precharge transistors are then turned on charging the internal sensing nodes to 0V and the bit lines to the threshold of the p-channel isolating transistors. The isolating transistors are now cut off. The precharge transistors are then shut off, then the memory cells and reference cells are connected to the bit lines. Since a similar charge transfer mechanism occurs for both

the memory cell and reference cell, for simplicity, only the case where the memory cell transfers charge from the storage capacitor to the sense amplifiers sensing nodes is analysed. Assuming a logical 1, (stable state with 5V on the memory cell storage node), charge sharing occurs between the small storage capacitance of the memory cell and the large capacitance of the bit line until the memory cell access transistor cuts off. This in turn increases the bit line voltage thereby turning the isolating transistor on. Charge transfer then occurs between the large bit line capacitance and the small sensing node capacitance until the isolating transistor cuts off again.

This two stage charge transfer mechanism passes the charge from the small storage capacitance of the memory cell to the sensing nodes small capacitance resulting in a signal at the sensing nodes independent of bit line capacitance. The back-gate bias effect aids charge transfer from the bit line to the sensing nodes by lowering the bulk to source voltage of the isolating transistors when charge is dumped on the bit line thus lowering the threshold of these charge transfer devices. Also the sensitivity of this preamplifying circuit is independent of the bit line isolating transistors threshold.

There are several disadvantages to this scheme. Capacitive imbalance between the sensing nodes is more significant when the sensing nodes are isolated from the typically well balanced bit line capacitance.

Another disadvantage is that by operating the bit line isolating transistor near cut off the gate drive is low and thus charge transfer is very slow. It also takes a long time to charge the bit lines to the point where the isolating transistors are cut off so that a negligible amount of current will flow through the channel. If incomplete precharge is used charge transfer between the bit lines large capacitance and the sensing nodes small capacitance will continue after the precharge transistors are shut off. Thus the memory cell and reference cell must be quickly read out, a voltage imbalance developed across the sensing nodes and the bit lines lowered to 0V by additional transistors before the sensing nodes rise to a level where the sense amplifier will no longer operate.

With a metal bit line scheme, precharging the bit line through two transistors in series rather than just one significantly increases the bit line precharge time making it a poor candidate for the 64K DRAM design. Also by including an isolating transistor one bit line will be discharged through two transistors in series rather than one thus increasing the time to fully restore the bit lines. This scheme is more suitable for use with a diffused bit line where bit line resistance is already high.

4.3 With N-Channel Isolating Transistors

By using n-channel isolating transistors with p-type memory cells and sense amplifiers gate drive may be increased and the problem of incomplete precharge and long bit line precharge times due to operating the isolating transistors near cut-off may be avoided.

With this scheme the memory cell is first charge shared with the bit line and the sensing node capacitance. The isolating transistors are then shut off and sensing from the smaller sensing node capacitance would be possible. After the latching operation the isolating transistors are then turned on again and one bit line would discharge through the sense amplifier.

The problem with this scheme is that, like the previous scheme using preamplifying p-channel isolating transistors, a bit line must discharge through two transistors in series thus increasing the time to fully restore the signal on the bit lines. Gating the isolating transistor off and on also increases the access time. It should be noted that with large DRAM designs interconnect capacitance and resistance plays a large role in determining access time since delays in gating devices may be quite substantial.

4.4 Without Bit Line Isolating Transistors

Connecting the bit line directly to the sense amplifier is the best approach for a metal bit line DRAM. Although the sensing nodes will have a higher capacitance causing a small increase in latching time this is far out-weighed by the reduction in time required to precharge the bit lines and the time to discharge one bit line through the sense amplifier.

Although bit line isolating transistors are still being used as noted in a recent metal bit line design [12], several recent metal bit line designs have been investigated which do not use bit line isolating transistors [1,7,13].

All of the latching schemes investigated so far employ some form of bit line restoration to compensate for off-side conduction. In a CMOS design this is easily achieved by using an n-channel amplifier to restore the bit line signal developed by the p-channel sense amplifier. The latching node for the n-channel restore amplifier may be the complement of the latching signal for the p-channel sense amplifier or it may be held at VSS during the latching operation since it will not sink current until the p-channel sense amplifier has raised one bit line above the threshold of the transistors used in the n-channel restore amplifier. A schematic of this scheme is shown in Figure 4.4.1.

This scheme is similar to a recent CMOS DRAM design by Intel [1] with a few exceptions. The first is that the $V/2$

Figure 4.4.1
Complementary Sense Amplifier

reference scheme is used instead of the C/2 reference scheme to improve process variation tracking ability. The second is that the p-channel sense amplifier has been separated from the column decoder. The p-channel sense amplifier is responsible for resolving the minimum voltage imbalance on the bit lines. The sensitivity of the n-channel restore amplifier is not as critical. Since a fair amount of substrate current may be generated from a dynamic NOR column decoder, the p-channel sense amplifier should be separated from the column decoder. If an n-channel decoder is used the substrate current generated by the decoder will be shielded from the p-type memory cells by a reverse biased p-well however isolating the column decoder from the sense amplifier is still recommended as this will allow future conversion to n-type memory cells, (if deemed necessary), with minimal change to the sense amplifier design.

A SCAMPER simulation assuming the scheme shown in Figure 4.4.1 was performed using the worst case signal margin of 51mV derived from the previous chapter. The results of this simulation appear in Figure 4.4.2. The results are also shown along with the source file in Appendix F. The simulation assumes a worst case process including worst case mask misalignment, an operating temperature of 75 degrees Celsius, a supply voltage of 4.5V and 20 nano-second rise and fall times on all lines. A 2pF I/O line loading was assumed which is larger than the true I/O capacitance since reduction in capacitance due to reverse bias-

ing the associated junction capacitance was not included. A width to length ratio of 2 was assumed for the column access I/O transistors, although this ratio could be increased by redesigning the column access I/O cell. The assumed rise and fall times of 20 nanoseconds is a very conservative estimate. This figure could possibly be reduced to 5 nanoseconds by redesigning the decoders, sense amplifiers and other associated circuitry so that all lines are run in metal rather than polysilicon. Considering the above approximations and the fact that the simulation is for worst case conditions the access time estimated from Figure 4.4.2 may be substantially improved.

From Chapter 3 the worst case voltage imbalance available to the sense amplifier for the latching operation was determined. The optimum latching scheme to use with the given process was then found. By using the established voltage imbalance and latching scheme along with a model of the memory cell, determined from the test chip design, a simulation of a read operation was performed. An existing operational amplifier design was used to simulate the output driver which is attached to the I/O lines. Figure 4.4.2 indicates that the output will be valid 60 nanoseconds after the latch nodes have completed their transition to turn the sense amplifiers on. The access time will be estimated in Chapter 7 after the required time to drive the word line is estimated in Chapter 6.

Figure 4.4.2 Worst Case SCAMPER Simulation Of Latching Operation

CHAPTER 5

SOFT ERROR RATE ANALYSIS

Errors in data read out from a DRAM may be hard errors or soft errors. Hard errors are a result of process and/or design related physical flaws in the DRAM such as open circuits. Such errors affect yield and may be minimized by good process control and redundant circuit implementation. Soft errors are random errors which are a result of charge collection by the memory cells, reference cells, bit lines or sense amplifiers due to either system noise or ionizing radiation.

Reduction of soft errors due to system noise may be achieved by separating the most sensitive circuits, such as the sense amplifiers, from noisy circuits, such as the decoders and the timing sequence generator. A guard ring placed around the memory array will also reduce system noise effects.

The soft error rate is dependent on both the process used and the physical layout and timing of the DRAM. This chapter will mostly be concerned with soft errors due to ionizing radiation.

Ionizing radiation in the form of alpha particles are emitted by Thorium and Uranium traces in the package. These alpha particles, which are doubly charged helium nuclei, (2 protons; 2 neutrons), have an average energy of 5MeV. As

they pass through the die they lose energy by ionization at a rate of 3.6eV per generated electron/hole pair. Thus for an average alpha particle strike $1.4E+6$ electron/hole pairs may be generated. Since the charge stored in a memory cell is typically on the order of a few hundred thousand to a few million electrons the level of carrier generation due to alpha particles can not be neglected. In fact, cosmic radiation itself can generate 100,000 electron/hole pairs per strike [14].

To reduce the number of carriers that are collected one can reduce the collection area and/or reduce the collection time. Collection area refers to the area of junctions which are part of the memory cells, reference cells, bit lines or sense amplifiers. The best way to reduce the junction area is to avoid diffused bit lines. Collection time refers to the time that a junction is floating and is susceptible to a change in potential due to capture of generated carriers. This may be minimized by reducing the time that the bit line and sense amplifier are left floating before a memory cell is read.

In general, use of p-type rather than n-type memory cells reduces the soft error rate. If p-type memory cells are used the memory cell will be discharged by collection of holes rather than electrons. Since hole mobility is lower than electron mobility the rate of collection of carriers by diffusion will be reduced and more of the generated carriers will recombine before they reach the junction in concern.

A significant proportion of carriers collected by a junction may be collected by drift. In fact, charge collected by drift may account for as much as half of the total charge collected by a junction from an alpha particle strike [15]. Carrier collection by drift occurs due to a phenomenon called funneling [16,17]. With reference to Figure 5.1 below the funneling phenomenon may be briefly described as follows.

Figure 5.1
Funneling Phenomenon

When an alpha particle strikes the die an electron-hole plasma forms along the alpha particle track with a typical plasma density of $1E+18$ to $1E+19$ cubic centimeters [17], which is several orders of magnitude greater than typical substrate doping densities. If the alpha particle strikes a junction the resultant electron-hole plasma quickly neutralizes the junction depletion layer in the vicinity of the plasma. Rapid collection of holes from the track then occurs. The resulting high current density along the track causes the electric field which was initially defined to the junction region to be displaced down into the substrate along the alpha particle track so causing the flow of holes into the junction from an extensive volume of plasma. When the plasma density eventually approaches the substrate doping density the junction depletion region starts to reform. The entire funneling process occurs in approximately 0.1 nanoseconds for silicon with a doping density of $1E+15$ cubic centimeters [17]. Further charge collection then occurs by the slower diffusion process.

For n+p junctions the length of collection by drift is $(1+(u_n/u_p))W$ [16] not including any angle dependency, (where W is defined as the junction depletion layer width following charge collection). For p+n junctions the length of collection is $(1+(u_p/u_n))W$ [16]. Since the length of carrier collection is shorter for p+n junctions compared to n+p junctions then fewer carriers will be collected thus making p-type memory cells more soft error immune than n-type memo-

ry cells. This conclusion also applies to the bit lines since they are composed of the same type of junction as the memory cells.

Other techniques used to reduce alpha particle induced soft errors involve using reverse biased wells, increasing the substrate doping and using buried epitaxial layers.

By placing the memory cells in a reverse biased well the memory cells are effectively isolated from any carriers generated after the alpha particle approaches or passes through the well.

Use of buried epitaxial layers or an increased substrate doping will cause carriers generated by alpha particles to be initially captured then redispersed more evenly over the memory array so that the level of carrier collection by any one memory cell is reduced.

Therefore the optimum solution is to use p-type memory cells placed in an n-well. Since the available process is a p-well process and only p-type memory cells can be used with the folded bit line architecture, (refer to Chapter 2), the soft error rate reduction by using the well is not obtainable. It should be noted that the reduction in soft error rate by using a well will be greater than the reduction in soft error rate by switching from n-type to p-type memory cells. However p-type memory cells were chosen so that the folded bit line approach could be used, (refer to Chapter 2 for justification for using the folded bit line approach).

Another common technique used to reduce the soft error rate is to prevent alpha particles from striking the die by coating the die with an alpha barrier such as Polyimide [18] or Room Temperature Vulcanizing, (RTV), rubber [19]. Such barriers block nearly all alpha particles leaving just small traces of alpha particles generated by metal interconnect and by the bulk.

Estimating a soft error rate requires consideration of several factors. If an alpha particle strikes a memory cell the cell will discharge into the stable state. With p-type memory cells the stable state is a logical 1. However, strikes on the bit line can cause a logical 0 to change into a logical 1 or vice versa depending on whether the bit line which is struck is servicing the memory cell or the reference cell. The same argument used for a bit line strike also applies for a sense amplifier strike. Therefore it is possible that an alpha particle striking the memory cell could change the stored state from a logical 0 to a logical 1 and a subsequent strike on the bit line servicing the reference cell could change it back into a logical 0 again.

Although the junction area in the large memory cell is 43 times smaller than the total junction area of the bit line populated with 128 memory cells the collection time of the memory cell is four milliseconds, (standard refresh cycle), as opposed to a few tens of nanoseconds for the bit line, (refer to Figure 4.4.2). Thus the product of collection area multiplied by collection time is a few thou-

sand times higher for the memory cell than the bit line for the proposed 64K DRAM design. Therefore we should expect to get more soft errors due to memory cell strikes rather than bit line or sense amplifier strikes..

Alpha particle strikes which just miss a junction can still result in a sufficient change in junction potential due to collected carriers to cause a soft error.

The number of carriers which are generated also depends on the incident angle of the alpha particle [20,21].

To determine analytically the soft error rate of a specific structure with a specific process all of the factors mentioned above would have to be considered in conjunction with the use of a three dimensional model capable of analysing carrier flow from the point of generation to the point of collection at a junction. This is clearly not an easy task. Therefore an empirical approach to determine the soft error rate is justifiable.

The approach taken to determine the minimum acceptable memory cell storage capacitance was to perform a survey of other DRAM designs with acceptable soft error rates and to choose a similar sized storage capacitance. A survey of 10 NMOS DRAMs using a 5 volt supply voltage revealed storage capacitances between 30fF to 60fF. Some designs used bootstrapped word lines to maximize the stored charge while others did not. A recent report [2] states that most DRAM designers feel that 35fF is the minimum allowable storage capacitance before an unacceptable amount of alpha particle

induced soft errors occur. This assumes a full 5V difference between a stored logical 0 and a stored logical 1 or a stored charge of 175fC. If bootstrapping was not employed only a 3V difference would exist assuming the same threshold voltage used with the available process. This translates into a minimum acceptable memory cell storage capacitance of 60fF.

The above conclusions are based upon reported experience with NMOS designs. In general, CMOS designs are less prone to soft errors than are NMOS designs. By placing the memory cells in a reverse biased well a reduction in the soft error rate by two orders of magnitude has been reported [1,22]. Although a reverse biased well is not used for this 64K DRAM feasibility study specific features of the CMOS process used in the present work, which give it an advantage over NMOS designs, are the use of p-type memory cells and a higher substrate doping near the surface, (compared with conventional NMOS DRAMs). The later results in the dispersal of generated carriers more evenly over the memory array. Thus the figure quoted above for minimum memory cell storage capacitance has a built-in safety margin.

An acceptable number of soft errors is considered to be less than 1000fits, (where a fit is defined as one failure in $1E+9$ device-hours). This roughly translates to one error in 114 years of operation.

To further substantiate the choice of a 60fF memory cell storage capacitance an accelerated soft error exper-

iment was performed with the DRAM test chip. A 118nCi Americium 241, (Am241), alpha particle source was used. Am241 is a commonly used source owing to its availability and long half life, (roughly 240 years) [23]. The intensity of the source, (expressed in Curies), was chosen to be the same as that used to obtain existing data [23] with which the results of this test are compared.

With reference to the circuit timing diagram shown in Figure 5.2 and the circuit schematic shown in Figure 5.3 the cycle used may be described as follows.

The column is decoded to connect the bit lines to the I/O lines and output driver. Then 5V is written into the memory cell connected to the left bit line and 0V is written into the memory cell connected to the right bit line. As this makes the output driver go high it will be referred to as writing in a high state although two cells are actually being written into with complementary data. Data must be written in through the sense amplifier due to a design error. The bit lines are then discharged to 5V and left floating. The pair of memory cells are then charge shared with the bit lines and the latch lowered from 5V to 0V thus discharging one bit line. This same sequence is then repeated with the exception of writing a low level into the memory cell connected to the left bit line and a high level into the memory cell connected to the right bit line.

To further accelerate the soft error rate all tests were performed with the structure utilizing small memory

cells, (storage capacitance of 15fF). A typical cycle is shown in Figure 5.4.

To prove the feasibility of using the DRAM for special applications which do not require refreshing, the DRAM was slowed down to a cycle time of 840 milliseconds so that 680 milliseconds elapsed between writing data in and reading it back. This is not the upper limit on storage time. For soft error testing the cycle time was reduced to 1.5 milliseconds. Further cycle time reduction was not possible due to ringing problems from the instrument used to generate the timing signals, (Tektronix DAS model 9100).

A soft error detector was designed and built to log soft errors, (refer to Figure 5.5 for a schematic). Its operation is described as follows. During a write operation a strobe is initiated which latches the data output, (refer to Figure 5.3), into a D-type flip flop. This selects either the shift register for lows or for highs. As previously defined a low refers to the resulting state of the data output driver thus a low occurs from a high level on the left bit line and a low level on the right bit line. During a subsequent read the output is checked against this latched value. If they differ, the shift register is incremented by one. As testing was expected to run for many hours unattended an overflow detector was designed which could only be reset manually.

A control test was run without the alpha particle source in place for 12 hours resulting in zero soft errors.

A test was then performed with the alpha particle source placed directly over the die with the alpha particle source holder touching the ceramic package. Over a 20 hour test zero soft errors were recorded. The alpha particle source was then removed and the die was exposed to various levels of room light. Increasing the level of light increased the number of soft errors. Roughly an equal number of low and high errors resulted. The decoders were designed to remain off in the presence of light. The fact that both low and high errors occurred in equal numbers implies that the decoders and the output driver were functioning properly. Earlier probing tests showed that the decoders and the output driver could tolerate a limited level of light exposure and still function acceptably. By increasing the intensity of the light further the decoders eventually shut off and only one type of error occurred from then on as the output driver remained in the same state since it was effectively separated from the bit lines. The decoders are more light sensitive than the output driver. If one assumes the quantum theory of light then the light exposure test is similar to an accelerated test except photons of light take the place of the alpha particles. These photons will still generate electron/hole pairs which will be collected by the memory cells, bit lines and sense amplifiers. The light exposure test verifies the functionality of the soft error detector and the operation of the DRAM.

In a typical test with a 64K DRAM using a 118nCi Am241 alpha particle source a few hundred to a few thousand errors occur per hour of testing [23]. The test with the DRAM test chip lasted 20 times longer, (increasing collection time), but exercised an area 32,000 times smaller, (collection area), assuming a similar sized memory cell. A rough estimate reveals that 1,600 times, (i.e. $32,000/20$), fewer soft errors should occur. This translates to an expected soft error accumulation of zero to a few errors. Note that although the bit line loading on a 64K DRAM would be much greater than that of the test chip the same amount of charge is still required to upset the bit line as is required to upset a memory cell.

Although the experimental results obtained are not statistically significant they do confirm that the predicted soft error rate is consistent with error rates observed in tests on large memories.

Figure 5.2

Circuit Timing For Soft Error Test

Figure 5.3

Circuit Schematic For Soft Error Test

Row $\overline{en}$
PC
Latch
Data Output

Figure 5.4

Complete Cycle Test

Figure 5.5
Soft Error Detector

Figure 5.5
Soft Error Detector

CHAPTER 6

WORD LINE CONSIDERATIONS

6.1 Calculation Of Word Line Loading

By referring to the large memory cell schematic and layout shown in Figures A.9 and A.11 respectively one can verify that the capacitive loading on the word line is as shown in Figure 6.1.1 below.

Figure 6.1.1

Word Line Capacitive Loading For Two Memory Cells

Recall that the word line forms the gate for half of the memory cells and the top storage capacitor plate for the

remaining memory cells. When the storage capacitance was calculated the oxide and junction components were added in parallel but when calculating the capacitive loading on the word line the oxide and junction components are added in series. The word line resistance has to be averaged over two cells since the width of the polysilicon used to form a gate is much smaller than the width of the capacitor plate. When calculating the capacitive and resistive loading of the word line for the test chip the effect of the polysilicon interconnect between the three groups of memory cells per structure was included. The interconnect used for the test structure using large memory cells along with the metal probe pads used for testing the row decoder is shown in Figure A.18. Since the same decoder is used for both the structure using small memory cells and the structure using large memory cells then the row decoder performance for only the structure using large memory cells was tested.

By considering the row with the highest loading, (18 memory cells and two interconnect lines); a load capacitance of 316.8fF and a load resistance of 2,291 ohms is obtained. These figures are used below, (Section 6.2), in the simulation of row decoder performance.

To simulate the word line loading for a 64K DRAM using the large memory cells the effect of the interconnect is removed. Thus the resulting load capacitance per memory cell pair is 32.0fF and the load resistance per memory cell pair is 128.4 ohms. For a 64K DRAM using the previously

described four block architecture the word line is populated with 128 memory cells, (64 memory cell pairs); the load capacitance then becomes 2.0pF and the load resistance 8,200 ohms giving a time constant of 16 nanoseconds. As previously described, (in Chapter 2), the use of word line repeaters or buffers may be used to reduce the time required to drive the word line. Without word line repeaters a time period equal to approximately three time constants is required to drive the word line to 95% of its full voltage transition giving a required time of 48 nanoseconds. By using four word line repeaters the required time will be roughly 12 nanoseconds. This assumes that one repeater will not switch states until its input has reached 4.75V. The actual required time will depend on the switching point of the repeaters. This analysis assumes that the channel resistance of the word line driver and repeaters is negligible compared to the resistance of the word line. The word line driver designed for the test chip has a significant channel resistance when turned on however it was felt that the word line driver could be redesigned with a significantly lower channel resistance. This analysis also neglects the distributed nature of the lines and the fact that the capacitive loading due to every second memory cell access gate, (refer to Figure 6.1.1), will reduce as the transistor turns on.

6.2 Row Decoder Performance

To simplify the test chip design the same cells are used to form the row decoder and the column decoder. Special cells are used to interface the decoders to the bit lines for a column decoder, (column access I/O cell), and to the word line for a row decoder. The decoders were designed to facilitate testing of the DRAM test chip. Therefore no attempt was made to optimize the decoder.

By using the word line loading calculated in the previous section the row decoder performance was simulated using SCAMPER. The word line was modelled as a distributed one step pi network including the effect of the 100fF Picoprobe, (Model 12), used to observe the word line during an experimental test. Based on a report [24] which gives the appropriate model to use for particular line loadings the model chosen will give no more than 3 percent error. From simulation the time required for the word line to rise from 0V to 5V was found to be 26 nanoseconds. The reader is referred to Appendix G for a source file and output for the SCAMPER simulation of row decoder performance. By using the test setup shown in Figure 3.3.1.5 the time required for the word line to rise from 0V to 5V was estimated to be between 25 and 40 nanoseconds, (refer to Figure 6.2.1 for the word line response). This agreement between the simulated and measured word line rise time reinforces the previous calculation of word line loading.

Figure 6.2.1
Row Decoder Performance

Note: Noise superimposed on the above waveforms was due to the picoprobe; not row decoder noise.

CHAPTER 7

CONCLUSIONS

7.1 Estimated Worst Case 64K DRAM Performance

The purpose of the research was to determine the feasibility of realizing a 64K DRAM with an existing CMOS process technology. With this end in mind, it is appropriate to base performance estimates upon worst case conditions, as was done in the work presented in the foregoing chapters. This basis of performance estimation should be taken into account when comparing the DRAM performance figures arrived at here with published data on commercial DRAMs. Only by carrying out a complete 64K DRAM design, and testing units fabricated with the available processing technology would realistic comparison with other DRAMs become possible. It is to be expected that such performance would be better than the estimates given in this thesis, perhaps significantly so.

In Table 7.1.1 below an estimate of 112 nanoseconds for access time is given, based on the assumption of the following worst case conditions.

- i) All rise and fall transition times are taken to be 20 nanoseconds. In practice this may be

substantially reduced through use of metal interconnect.

- ii) An operating junction temperature of 75 degrees Celsius is assumed. The actual environmental operating temperature represented will be greater than 75 degrees Celsius by an amount which depends on the thermal resistance between the die and the package exterior.
- iii) Worst case process conditions, including mask misalignment and over/under etching of layers, is made with no correlation between memory cells, bit lines and sense amplifiers.
- iv) A worst case supply voltage of 4.5V is assumed.
- v) No load is attached to the output driver. Thus the access time calculations do not include the time required to drive external pins. The output driver used is not meant for driving such a large load. For custom applications, however, the output driver will only be required to drive other cells on-chip and will not be burdened by bonding pad and package pin capacitance.

Results of simulated access time are shown in Figure 4.4.2 with the source file and output for the SCAMPER simulation given in Appendix F.

Row decode and enable time:	20 ns.
Time to drive word line to within 95% of supply rail using 4 repeaters:	12 ns.
Latch transition time:	20 ns.
Time required to drive output to supply rail following latch transition:	60 ns.
<hr/> Total:	<hr/> 112 ns.

Table 7.1.1
Access Time Estimate For A 64K DRAM

The worst case estimated access time is reasonable compared to nominal access times for commercial DRAMs of 70 to 250 nanoseconds if one considers the approximations made.

By increasing the gain of the transistors in the column access I/O cells and by increasing the gain of the sense amplifiers the access time may be substantially reduced. Increasing the gain of the memory cell access transistor does not affect the access time significantly. Another major contributor to operating speed limitation is that of interconnect resistance and capacitance, however this is mostly a process, not a design limitation.

To calculate the overall die size required for a 64K DRAM the four block architecture discussed in Chapter 2 is used. To calculate row and column decoder area a slight modification was made to make the decoders symmetrical. The resulting new decoder area was then used. To obtain sufficient gain for the p-channel sense amplifier with the constraint of the existing bit line pitch two sense amplifi-

ers were linked in parallel with each other. The assumption of 4 repeaters per row was used with repeaters for memory cells, reference cells and sense amplifiers. An area estimate of the basic memory structure is given in Table 7.1.2, to which must be added an allowance for remaining peripheral devices and circuits as discussed below. Since all of the cells forming the basic memory structure have common word line and/or bit line pitches no interconnect is required for the basic structure.

65,536 Large Memory Cells:	27,300,000 μm^2
512 Reference Cells:	200,000 μm^2
128 Symmetrical 7 Bit Column Decoders: . .	1,400,000 μm^2
512 Symmetrical 9 Bit Row Decoders: . . .	6,460,000 μm^2
2128 Repeater:	7,600,000 μm^2
512 P-Channel Sense Amplifiers:	880,000 μm^2
256 N-Channel Restore Amplifiers:	540,000 μm^2
<hr/>	
Subtotal:	44,380,000 μm^2

Table 7.1.2
Area Estimate For A 64K DRAM

To compensate for the area required for bonding pads, protection devices, address latches, buffers, column/row address multiplexors, timing circuitry, a bidirectional 4:1 multiplexor/demultiplexor and driver and associated interconnect an additional 20% should be added to the above subtotal to arrive at an estimate of die size. The basis for using 20% for area compensation comes from observing the proportion of die size required for such circuits in photographs of commercial 64K DRAMs. Thus the resulting die size

is 53,256,000 square microns or 82,550 square mils. This figure is 40% smaller than the largest chip made with this CMOS process. With reference to Table 7.1.2 the memory cells are shown to use only half of the die area. The area covered by memory cells will be the most susceptible to silicon defects as a higher proportion of this area is active area, (junctions and channel area). Considering the fact that the estimated die size for the 64K DRAM is 40% smaller than the largest chip successfully made with this CMOS process and the fact that only half of the die area for the 64K DRAM will have a higher susceptibility to silicon defects it is concluded that a 64K DRAM is feasible. However the die size is still too large to fit in a standard 16 pin DRAM package. Commercial 64K DRAMs use column and row address multiplexing so that a 16 pin package may be used. The maximum allowable die size for a 16 pin DRAM package is roughly 300 mils by 160 mils, (roughly 48,000 square mils).

Estimated worst case performance figures are summarized in Table 7.1.3 below.

Access Time, (on-chip):	112 ns.
Die Size:	82,550 mil ²
Memory Cell Size:	416 μ m ²
Storage Area/Memory Cell Area:	20 %
Storage Capacitance:	60 fF
Stored Charge:	180 fC
Bit Line /Memory Cell Capacitance:	18:1
Sense Amplifier Sensitivity:	3 mV
Useable Signal At Sense Amplifier:	51 mV
Signal Margin, (expressed in electrons):	330,000 electrons
Soft Error Rate:	<1000 fits

Table 7.1.3
Estimated Worst Case 64K DRAM Performance Figures

7.2 Summary

Although 64K designs were in existence at the outset of this thesis the design was complicated by several factors. One factor was that the design was constrained to an existing CMOS fabrication process. This process was intended for digital circuits whereas the design of a DRAM is very analog intensive. Another factor was that virtually all DRAMs reported were made with an NMOS technology thus information obtained from preliminary research was not always applicable to a CMOS design.

At many stages of the design value judgements were required. Trade offs between area, speed and soft error immunity were frequent. For example choosing an architecture with more than four blocks or increasing the number of word line repeaters would trade off area for speed.

The design started by considering the many design options available to overcome the inherent difficulties in designing a DRAM. The options best suited to the available process were then chosen. Analysis of architectures revealed that dividing the memory cells into four blocks and sharing the column and row decoders between blocks would be the best approach. Consideration of the sensitivity of the design to process variations as well as thermal generation losses established the chosen DRAM design to be well balanced and able to track process variations easily. This is an important consideration since it will improve parame-

tric yield, (yield based on parameter variations; not faults such as open circuits). It was also desirable to make the design as independent of the process as possible since this process was not yet fully defined. A novel approach to generating a reference level was taken. It combines the advantages of being able to track process variations as with the $V/2$ reference scheme yet is much faster. Since the word lines were not bootstrapped, a stored logical 0 value depended on the memory cell access transistor threshold voltage. Thus the optimum choice of reference level was no longer half-way between the power supply rails. The novel reference scheme used compensates for this by having the ability to track threshold voltage variations.

It was then determined that the optimum bit line precharge level before a read operation should be 0V. This yields the largest signal margin in spite of the fact that incomplete charge transfer between the memory cells storage capacitance and the bit line occurs. Also gate to source coupling effects, which may amount to several hundred millivolts, can only be eliminated through use of this precharge level. The optimum latching scheme for use with a metal bit line populated with p-type memory cells was found to consist of a p-channel sense amplifier with an n-channel bit line restoring amplifier both without any isolation from the bit lines.

Soft error rate analysis was undertaken and led to the conclusion that the optimum CMOS DRAM design should use

p-type memory cells placed in an n-well. P-type memory cells were shown to collect less charge from alpha particle strikes than n-type cells, by both the slow collection process due to diffusion currents, and rapid collection due to drift currents resulting from the funneling phenomenon. The available process did not accommodate the use of p-type memory cells in an n-well since it was a p-well CMOS process. The next best solution to soft errors which is to use n-type memory cells in a p-well was not used as it would not permit the use of a folded bit line architecture. A folded bit line architecture was considered better than an open bit line architecture since it is quieter, gives balanced access to the bit lines and is easier to lay out, (thereby permitting a better design).

The final conclusion is that a 64K DRAM realized in the available CMOS process, is certainly feasible though not competitive. The DRAM is too large to fit in a standard 16 pin DRAM package. However it is well suited for use as memory support for custom chip designs supporting many functions on the same die. The design shows that large DRAM memory structures may be successfully incorporated onto custom chip designs thus greatly expanding the range of applications for custom integrated circuits that can be undertaken in the future.

7.3 Recommendations For Future Work

Now that the best approach to making DRAM with this process has been defined the next step should be to design a large array to get more accurate data on the soft error rate, the effect of disturbance between memory cells and yield statistics.

Design of the necessary timing logic will be required. Since the latching pulse is independent of the bit line loading it might be possible to design one timing generation module for any size of memory required. Such a design would be of tremendous benefit in making the memory structure compatible for an automated layout scheme.

Read/refresh contention and refresh timing should also be designed so that, external to the structure, the DRAM will appear as a static RAM, thus facilitating its use.

Depending on the outcome of future soft error rate analysis and yield statistics work on error checking and correcting circuitry and redundancy implementation may be required.

Predecoding schemes should also be investigated to replace the dynamic NOR decoders with lower power and quieter NAND decoders.

In conclusion work on improving the performance of the DRAM through use of process modifications which are compatible with other custom designs already in use could be undertaken. The most obvious modifications would be the use

of thinner dielectrics to improve storage capacitance, and the use of double level metal and polycides or silicides to reduce interconnect delay. Polycides or silicides would be most effective in reducing the word line delay. Reducing interconnect delay sufficiently would also permit the repeaters to be removed thus decreasing the required die size by over 10%, (refer to Table 7.1.2 for the area required for the repeaters and Table 7.1.3 for a die size estimate).

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APPENDIX A

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TEST CHIP CELLS

Figure A.1

Quadrant 1 Metallization Pattern

BONDING PADS FOR DRAM STRUCTURES

<u>PAD #</u>	<u>SIGNAL</u>
1	Data output
2	Bias current for output driver,BI
3	Bias voltage for output driver,BV
4	Row decoder precharge transistor,PC4
5	40K resistor,R40K
6	40K resistor,R40K
7	VDD
8	VSS
9	Row address,R0
10	Row address,R1
11	Row address,R2
12	Row address,R3
13	Row address,R4
14	Row address,R5
15	Row address,R6
16	Row address,R7
17	Row enable
18	Row enable (complement)
19	Voltage supply for bit line precharge transistor,VH2
20	Voltage supply for bit line precharge transistor,VH1
21	Bit line precharge transistor,PC2
22	Bit line precharge transistor,PC1
23	Latch node
24	Isolating transistor 2
25	Isolating transistor 1
26	Bit line charge share transistor
27	Data input 2
28	Data input 1
29	Column enable (complement)
30	Column enable
31	Column address,C4
32	Column address,C3
33	Column address,C2
34	Column address,C1
35	Column address,C0
36	Column decoder precharge transistor,PC3

Pad numbers refer to the numbering system shown in the Figures A-2 and A-3

30 K

X22 CELLS

CELL	DESCRIPTION
X22RP2A	Sense amplifier
X22RP2B	Small memory cell (4 bits)
X22RP2E	Decoder end cap with precharge transistor
X22RP2F	One bit of decoder
X22RP2G	Decoder end cap with access transistor
X22RP2H	Bit line to I/O connection; bit line charge sharing
X22RP2I	Inverting buffer for row decoder
X22RP2J	P-well cap for X22RP2G (right side)
X22RP2K	Cap for X22RP2A (right and left side)
X22RP2L	Top and bottom cap for X22RP2B
X22RP2M	Right and left side cap for X22RP2B
X22RP2P	Big memory cell with matching bit line and row pitch
X22RP2Q	Right and left side cap for X22RP2P
X22RP2R	Column decoder to column decoder interconnect
X22RP2S	Left side cap used for connecting X22RP2A cells
X22RP2T	Right side cap used for connecting X22RP2A cells
X22RP2V	WORD/CAPACITOR PLATE line jumpers for big memory cells
X22RPC	Metal to poly contact for decoders
X22RPR1	Complete structure with small memory cells
X22RP1	X22RPR1 without pads and pad connections
X22RPR2	Complete structure with large memory cells
X22RP2	X22RPR2 without pads and pad connections
X22RP4	Row Decoder To Small Memory Cell Interface

LIBRARY CELLS USED

CELL	DESCRIPTION
FFY0A6	High speed op-amp
FFYR40K	40K P-well resistor
INVB	Minimum sized inverting buffer

Structure: X22RPR2

Figure A.4
Cell Placement

The following are schematics and plots of the cells which were designed and used for the X22 DRAM test structures.

LEGEND

Device Well
Metal
P-well;P-guard;N-guard(exclusion mask)
Polysilicon
P+ Doping;N+ Doping(exclusion mask)
Capacitor Implant
Contact

Sense Amplifier And End Caps .

Cells: RP2A;RP2K:RP2S:RP2T

notes:

- i) RP2S and RP2T are used to connect the sense amplifier cells between groups, (3 groups of 3 sense amplifiers exist on each structure).
- ii) When RP2S or RP2T are not used RP2K must be used to ensure sufficient N+,P+ and P-well overlap of device wells.
- iii) RP2K must be flipped about the y-axis to be used on the left side of RP2A

Cell: RP2A

Figure A.5
Sense Amplifier Schematic

Cell: RP2A

Cell: RP2K

Figure A.6
Sense Amplifier Layout

Cell: RP2S

Figure A.7

Sense Amplifier End Cap Layout

Cell: RP2T

Figure A.8

Sense Amplifier End Cap Layout

Memory Cells And End Caps

Cells: RP2B;RP2M;RP2L;RP2P;RP2Q

notes:

- i) RP2L is wider than RP2B so that a special cell would not be required for the left most bit in the array to ensure N+,P+ overlap of the device well.

Cell: RP2B or RP2P

Figure A.9

Memory Cell Schematic

Figure A.10
Small Memory Cell Layout

Figure A.11
Large Memory Cell Layout

Decoders

Cells: RP2E;RP2F;RP2G;RP2J;RPC;RP2I;RP2H

notes:

- i) RP2E,RP2F and RP2G cells form a NOR decoder.
- ii) The number of RP2F cells required is equal to the decoder bit width minus two.
- iii) RP2J ensures sufficient N+,P+ and P-well overlap of device wells on the right side of RP2G.
- iv) RPC is used to 'program' the decoder by either connecting the true or complement of each address bit.
- v) RP2I is an interface cell used to convert the decoder into a row decoder. RP2I may also be used as a word line repeater,(ref. Chapter 3).
- vi) RP2H is an interface cell used to convert the decoder into a column decoder.

Figure A.12
Decoder Schematic

Figure A.13

Decoder Layout

Cell: RP21

Figure A.14
Word Line Driver Schematic

Cell: RP21

Figure A.15

Word Line Driver Layout

Figure A.16
Column Access I/O Schematic

Cell: RP2H.

Figure A,17

Column Access I/O Layout

Interconnect Cells

Cells: RP2V;RP2R;RP4

Notes:

- i) RP2V is used between the 3 groups of large memory cells.
- ii) RP2R is used between the 3 groups of column decoders. Both RP2V and RP2R incorporate probing pads to facilitate debugging.
- iii) RP4 is only required with the structure using small memory cells since the word line pitch is greater on the row decoder than on the memory cells.

CMOS3 PROCESS (FIRST UPDATE) 830606
VALUES OF PLOTTED VARIABLES

TIME(SEC)	*BL1	*BL2	*IO	*NIO
.0	.0	.0	.0	.0
4.000E-09	-1.5328E-03	-1.5371E-03	-5.3897E-11	1.0449E-09
8.000E-09	2.3558E-03	-3.0522E-03	-1.0722E-10	2.0716E-09
1.200E-08	2.4279E-02	-2.6865E-03	-4.9102E-11	3.0884E-09
1.600E-08	5.6760E-02	1.2255E-02	1.3576E-10	4.1780E-09
2.000E-08	9.2042E-02	4.1211E-02	3.6429E-10	5.4095E-09
2.400E-08	.11435	6.2341E-02	5.9686E-10	6.7282E-09
2.800E-08	.12372	7.1600E-02	8.2959E-10	8.0586E-09
3.200E-08	.16222	.10671	1.0625E-09	9.3897E-09
3.600E-08	.32428	.25918	1.2965E-09	1.0722E-08
4.000E-08	.66934	.58918	1.5331E-09	1.2056E-08
4.400E-08	1.0557	.95602	1.7732E-09	1.3395E-08
4.800E-08	1.3559	1.2297	2.0161E-09	1.4735E-08
5.200E-08	1.5888	1.4262	2.2611E-09	1.6078E-08
5.600E-08	1.7715	1.5598	1.0086E-04	1.0089E-04
6.000E-08	1.9171	1.6407	3.0689E-03	3.0444E-03
6.400E-08	2.0042	1.6435	3.2666E-02	3.2249E-02
6.800E-08	1.9940	1.5236	.13297	.13021
7.200E-08	1.8992	1.3045	.31731	.30054
7.600E-08	1.7638	1.1007	.56374	.48402
8.000E-08	1.7214	1.0139	.77136	.61165
8.400E-08	1.7619	.99356	.93232	.69856
8.800E-08	1.8449	.99154	1.0664	.76474
9.200E-08	1.9521	.98791	1.1849	.82047
9.600E-08	2.0756	.97372	1.2916	.86578
1.000E-07	2.2130	.94419	1.3879	.89426
1.040E-07	2.3656	.89393	1.4741	.90033
1.080E-07	2.5350	.82347	1.5512	.89140
1.120E-07	2.7193	.73941	1.6199	.86671
1.160E-07	2.9130	.65071	1.6812	.82704
1.200E-07	3.1072	.56506	1.7360	.77497
1.240E-07	3.2929	.48783	1.7853	.71428

Cell: RP2V

Figure A.18

Interconnect Between Memory Cell Groups

Cell: RP2R

Figure A.19

Interconnect Between Column Decoders

Cell: RP4

Figure A.20

Row Decoder To Small Memory Cell Interface

APPENDIX B

SIMULATION OF SUCCESSFUL LATCH

S C A M P E R - 2.03.0 FILE-SENSETST TIME-14:39 1984-MAY-14 MON S C A M P

```

.....
TESTS SENSITIVITY OF SENSE AMPLIFIER
(X22RP2A)
.....

```

```

E00 VDD GND 5
E01 VSS GND 0
E1 1 GND INIT(5)
E2 2 GND INIT(5)
E3 3 GND INIT(0)
E4 4 GND INIT(0)

```

```

..... INITIAL VOLTAGE IMBALANCE EQUALS 1.0 mV .....

```

```

E5 5 GND 4.9990
E6 6 GND 5.0000
E7 7 GND TABLE(5E-9,5) (15E-9,0) (25E-9,0) (35E-9,5)
E8 8 GND TABLE(5E-9,5) (15E-9,0) (25E-9,0) (35E-9,5)
E9 9 GND TABLE(40E-9,5) (1490E-9,0)
E10 10 GND 0
E11 11 GND 0
MISN1 VSS 3 10 1 3 5 43.2 49.7 1 26.4 30.2
MISN2 VSS 4 11 2 3 5 54 49.8 1 30 30.0
MISP3 VDD 3 7 5 3 5 54 49.7 1 30 30.2
MISP4 VDD 4 8 6 3 5 46.8 49.8 1 27.6 30.0
MISN5 VSS 3 4 9 3 5 46.8 49.7 1 27.6 30.2
MISN6 VSS 4 3 9 3 5 46.8 49.8 1 27.6 30.0

```

```

..... SENSE AMPLIFIER OFFSET CAPACITANCES .....

```

```

CL 3 VSS 26.6E-15
CR 4 VSS 25.0E-15
$PROCESS
FILE CM3
$S
$TIME(2E-9,40E-9) (20E-9,1000E-9)
$PLOT *BL1 -NV(1) NOPR
$PLOT *BL2 -NV(2) NOPR
$PLOT *LEFT -NV(3) NOPR
$PLOT *RIGHT -NV(4) NOPR
$PLOT *CHARGE -NV(7) NOPR
$PLOT *LATCH -NV(9) NOPR
$PLOT *TSFR -NV(10) NOPR
$GRAPH,*CHARGE,*TSFR,*LEFT,*RIGHT,*LATCH,*BL1,*BL2
$ANAL TIME

```

CHOS3 PROCESS (FIRST UPDATE) 830606

A : CHRG B : TSFR C : LEFT D : RIGH
 E : LATC F : BL1 G : BL2

APPENDIX C

SIMULATION OF UNSUCCESSFUL LATCH

S C A M P E R - 2.03.0 FILE-SENSETST TIME-14:21 1984-MAY-14 MON S C A M P

```

.....
TESTS SENSITIVITY OF SENSE AMPLIFIER
(X220P2A)
.....

```

```

E00 VDD GND 5
E01 VSS GND 0
E1 1 GND INIT(5)
E2 2 GND INIT(5)
E3 3 GND INIT(0)
E4 4 GND INIT(0)

```

```

***** INITIAL VOLTAGE IMBALANCE EQUALS 0.5 mV *****

```

```

E5 5 GND 4.9995
E6 6 GND 5.0000
E7 7 GND TABLE(5E-9,5) (15E-9,0) (25E-9,0) (35E-9,5)
E8 8 GND TABLE(5E-9,5) (15E-9,0) (25E-9,0) (35E-9,5)
E9 9 GND TABLE(40E-9,5) (1490E-9,0)
E10 10 GND 0
E11 11 GND 0
MISN1 VSS 3 10 1 3 5 43.2 49.7 1 26.4 30.2
MISN2 VSS 4 11 2 3 5 54 49.8 1 30 30.0
MISP3 VDD 3 7 5 3 5 54 49.7 1 30 30.2
MISP4 VDD 4 8 6 3 5 46.8 49.8 1 27.6 30.0
MISN5 VSS 3 4 9 3 5 46.8 49.7 1 27.6 30.2
MISN6 VSS 4 3 9 3 5 46.8 49.8 1 27.6 30.0

```

```

***** SENSE AMPLIFIER OFFSET CAPACITANCES *****

```

```

CL 3 VSS 26.6E-15
CR 4 VSS 25.0E-15

```

```

$PROCESS

```

```

FILE CM3

```

```

$$

```

```

$TIME(2E-9,40E-9) (20E-9,1000E-9)

```

```

$PLOT *BL1 -MV(1) NOPR

```

```

$PLOT *BL2 -MV(2) NOPR

```

```

$PLOT *LEFT -MV(3) NOPR

```

```

$PLOT *RIGHT -MV(4) NOPR

```

```

$PLOT *CHARGE -MV(7) NOPR

```

```

$PLOT *LATCH -MV(9) NOPR

```

```

$PLOT *TSFR -MV(10) NOPR

```

```

$GRAPH,*CHARGE,*TSFR,*LEFT,*RIGHT,*LATCH,*BL1,*BL2

```

```

$ANAL TIME

```

CHOS3 PROCESS (FIRST UPDATE) 830606

A : CHRG B : TSFR C : LEFT D : RIGH
 E : LATC F : BL1 G : BL2

APPENDIX D

SIMULATION OF WRITE OPERATION

S C A M P E R - 2.03.0 FILE=COUPLIN1 TIME=15:12 1984-MAY-14 MON S C A M P

.....
 * CAPACITIVE COUPLING BETWEEN BIT LINE AND
 * LARGE MEMORY CELL DURING A WRITE OPERATION
 * ASSUMING A NOMINAL PROCESS

KDD VDD GND 4.5
 ESS VSS GND 0
 EBL BL GND 0
 ESTOR STOR GND INIT(5.000)
 EWD WD GND TABLE(0E-9,4.5) (20E-9,0) (40E-9,0) (60E-9,4.5)

MISP1 VDD BL1 WD STOR 3 6 18 27 3 18 21

.....
 * "FBCS" AND "FBBL" ARE SUBROUTINES TO INCLUDE VOLTAGE
 * DEPENDENT JUNCTION CAPACITANCE.

.....
 * PARASITIC CAPACITANCES

CGS WD STOR 0.69E-15
 CGD WD BL 0.69E-15
 CBTW BL WD 0.45E-15
 CBTS BL STOR 0.45E-15

.....
 * BIT LINE AND MEMORY CELL STORAGE CAPACITANCES

CS STOR VDD 51.4E-15
 CJN1 STOR VDD FBCS
 CBL BL VDD 42.6E-15
 CJN2 BL VDD FBBL
 OSTOR STOR GND

SBL BL1 BL

\$PROCESS

FILE CM3

\$\$

**TEMP=348

\$TIME (2E-9,64E-9)

\$PLOT *WD =NV(WD)

\$PLOT *BL =NV(BL)

\$PLOT *OSTOR =V(OSTOR)

\$PLOT *IBL =I(SBL)

\$GRAPH *WD,*BL,*OSTOR

\$ANAL TIME

CMOS3 PROCESS (FIRST UPDATE) 830606

A : WD B : BL C : OSTO

CMOS3 PROCESS (FIRST UPDATE) 830606
VALUES OF PLOTTED VARIABLES

TIME(SEC)	*WD	*BL	*OSTO	*IBL
.0	4.5000	.0	5.0000	1.7457E-09
2.000E-09	4.0500	.0	4.9744	5.8323E-07
4.000E-09	3.6000	.0	4.8906	3.4734E-06
6.000E-09	3.1500	.0	4.7323	6.4223E-06
8.000E-09	2.7000	.0	4.5130	8.6879E-06
1.000E-08	2.2500	.0	4.2432	1.0107E-05
1.200E-08	1.8000	.0	3.9365	1.0855E-05
1.400E-08	1.3500	.0	3.6055	1.1194E-05
1.600E-08	.90001	.0	3.2595	1.1318E-05
1.800E-08	.45001	.0	2.9041	1.1342E-05
2.000E-08	6.8397E-06	.0	2.5429	1.1320E-05
2.200E-08	.0	.0	2.3063	6.0307E-06
2.400E-08	.0	.0	2.1703	3.6404E-06
2.600E-08	.0	.0	2.0842	2.4340E-06
2.800E-08	.0	.0	2.0238	1.7346E-06
3.000E-08	.0	.0	1.9792	1.2964E-06
3.200E-08	.0	.0	1.9452	1.0080E-06
3.400E-08	.0	.0	1.9185	8.0907E-07
3.600E-08	.0	.0	1.8969	6.6598E-07
3.800E-08	.0	.0	1.8790	5.5942E-07
4.000E-08	8.9997E-10	.0	1.8639	4.7778E-07
4.200E-08	.44998	.0	1.8831	2.1166E-07
4.400E-08	.89998	.0	1.8950	2.1162E-07
4.600E-08	1.3500	.0	1.9063	2.1162E-07
4.800E-08	1.8000	.0	1.9176	2.1162E-07
5.000E-08	2.2500	.0	1.9288	2.1162E-07
5.200E-08	2.7000	.0	1.9400	2.1162E-07
5.400E-08	3.1500	.0	1.9512	2.1162E-07
5.600E-08	3.6000	.0	1.9624	2.1162E-07
5.800E-08	4.0500	.0	1.9736	2.1162E-07
6.000E-08	4.5000	.0	1.9848	2.1162E-07
6.200E-08	4.5000	.0	1.9848	5.6369E-12
6.400E-08	4.5000	.0	1.9848	5.6369E-12

[illegible]

APPENDIX E

SIMULATION OF READ OPERATION

S C A M P E R - 2,03.0 FILE-COUPLIN1 TIME-15:10 1984-MAY-14 MON S C A M P

```

.....
CAPACITIVE COUPLING BETWEEN BIT LINE AND
LARGE MEMORY CELL DURING A READ OPERATION
ASSUMING A NOMINAL PROCESS
AND A BIT LINE LOADING OF 8
MEMORY CELLS
.....

```

```

EDD    VDD    GND    4.5
ESS    VSS    GND    0
EBL    BL     GND    INIT(0)
ESTOR  STOR   GND    INIT(5.000)
EWD    WD     GND    TABLE(0E-9,4.5) (20E-9,0) (40E-9,0) (60E-9,4.5)

```

```

MISPI VDD BL1 WD STOR 3 6 18 27 3 18 21

```

```

.....
"FBCL" AND "FBBL" ARE SUBROUTINES TO INCLUDE VOLTAGE
DEPENDENT JUNCTION CAPACITANCE.
.....

```

PARASITIC CAPACITANCES

```

CGS    WD     STOR  0.69E-15
CGD    WD     BL   0.69E-15
CBTW   BL     WD   0.45E-15
CBTS   BL     STOR 0.45E-15

```

BIT LINE AND MEMORY CELL STORAGE CAPACITANCES

```

CS      STOR  VDD    51.4E-15
CJW1    STOR  VDD    FBCL
CBL     BL    VDD    42.6E-15
CJW2    BL    VDD    FBBL
OSTOR   STOR  GND
SBL BL1 BL

```

\$PROCESS

FILE CM3

\$\$

**TEMP=348

\$TIME (2E-9,64E-9)

\$PLOT *WD =MV(WD)

\$PLOT *BL =MV(BL)

\$PLOT *OSTOR =V(OSTOR)

\$PLOT *IBL =I(SBL)

\$GRAPH *WD,*BL,*OSTOR

\$ANAL TIME

CMOS3 PROCESS (FIRST UPDATE) 830606

A : WD B : BL C : OSTO

CHOS3 PROCESS (FIRST UPDATE) 830606
VALUES OF PLOTTED VARIABLES

TIME(SEC)	*WD	*BL	*OSTO	*IBL
.0	4.5000	.0	5.0800	1.7457E-09
2.000E-09	4.0500	-5.1404E-03	4.9743	5.5727E-07
4.000E-09	3.6000	4.2779E-02	4.8908	3.2137E-06
6.000E-09	3.1500	.16791	4.7332	5.9168E-06
8.000E-09	2.7000	.35769	4.5152	7.9747E-06
1.000E-08	2.2500	.59040	4.2479	9.2424E-06
1.200E-08	1.8000	.84745	3.9448	9.8811E-06
1.400E-08	1.3500	1.1149	3.6192	1.0129E-05
1.600E-08	.90001	1.3837	3.2809	1.0145E-05
1.800E-08	.45001	1.6475	2.9374	9.9932E-06
2.000E-08	6.8397E-06	1.8939	2.5990	9.2474E-06
2.200E-08	.0	2.0728	2.3895	4.3722E-06
2.400E-08	.0	2.1550	2.2898	1.8810E-06
2.600E-08	.0	2.1904	2.2461	7.8091E-07
2.800E-08	.0	2.2051	2.2277	3.1841E-07
3.000E-08	.0	2.2114	2.2197	1.1614E-07
3.200E-08	.0	2.2141	2.2163	3.1417E-08
3.400E-08	.0	2.2150	2.2152	2.0433E-09
3.600E-08	.0	2.2153	2.2149	-5.0013E-09
3.800E-08	.0	2.2153	2.2149	-4.7438E-09
4.000E-08	8.9997E-10	2.2152	2.2150	-3.0060E-09
4.200E-08	.44998	2.2463	2.2506	8.4045E-07
4.400E-08	.89998	2.2651	2.2711	1.7097E-07
4.600E-08	1.3500	2.2788	2.2854	1.6988E-07
4.800E-08	1.8000	2.2908	2.2976	1.6985E-07
5.000E-08	2.2500	2.3022	2.3092	1.6983E-07
5.200E-08	2.7000	2.3134	2.3204	1.6981E-07
5.400E-08	3.1500	2.3245	2.3316	1.6979E-07
5.600E-08	3.6000	2.3356	2.3428	1.6977E-07
5.800E-08	4.0500	2.3467	2.3540	1.6975E-07
6.000E-08	4.5000	2.3577	2.3651	1.6973E-07
6.200E-08	4.5000	2.3577	2.3651	5.1110E-12
6.400E-08	4.5000	2.3577	2.3651	5.1110E-12

APPENDIX F

SIMULATION OF 64K DRAM ACCESS TIME

S C A M P E R - 2.03.0 FILE-SENSE TIME-15:07 1984-MAY-14 MON S C A M P

```

.....
* 64K DRAM ACCESS TIME SIMULATION USING THE
* MODEL 3.3V REFERENCE SCHEME AND
* AND AN N-CHANNEL BIT LINE RESTORE AMPLIFIER
.....

```

```

..... OUTPUT DRIVER .....

```

```

$SUBCCT OA6 1 2 3 4 5 6 7 8
$
MOA6 OA6 VDD VSS OUT IO NIO 40K6 40K7 SUB
SSUB SUB VDD
SBIAS 40K6 40K7
R40 40K6 VDD 40000
.....
EDD VDD GND 4.5
ESS VSS GND 0
E1 1 GND INIT(0)
E2 2 GND INIT(0)
EIO IO GND INIT(0.0)
ENIO NIO GND INIT(0.0)
ESTOR STOR GND INIT(4.500)
ESTOR STOR GND INIT(2.127)
EREF REFSTOR GND INIT(3.592)
EWD1 WD1 GND TABLE(0E-9,4.5) (20E-9,0)
EREFWD REFWD GND TABLE(0E-9,4.5) (20E-9,0)
ELATCHN 3 GND TABLE(20E-9,4.5) (40E-9,0)
ELATCHP 4 GND TABLE(20E-9,0) (40E-9,4.5)
ECOL COL GND TABLE(55E-9,0) (75E-9,4.5)

```

```

..... MEMORY CELL .....

```

```

MISP5 VDD 1 WD1 STOR 3 6 18 27 3 18 21

```

```

..... REFERENCE CELL .....

```

```

MISP6 VDD 2 REFWD REFSTOR 3 6 18 27 3 18 21

```

```

..... SENSE AND RESTORE AMPLIFIERS .....

```

```

MISM1 VSS 1 2 3 3 5 46.8 49.7 3 27.6 30.2
MISM2 VSS 2 1 3 3 5 46.8 49.8 3 27.6 30.0
MISP3 VDD 1 2 4 3 10 46.8 49.7 3 27.6 30.2
MISP4 VDD 2 1 4 3 10 46.8 49.8 3 27.6 30.0

```

```

..... COLUMN ACCESS I/O TRANSISTORS .....

```

```

MISM7 VSS 1 COL IO 3 5 40 40 3 30 30
MISM8 VSS 2 COL NIO 3 5 40 40 3 30 30

```

SENSE AMPLIFIER OFFSET CAPACITANCES

CLN 1 VSS 25.0E-15
 CRN 2 VSS 26.6E-15
 CLP 1 VDD 25.0E-15
 CRP 2 VDD 26.6E-15

I/O CAPACITANCE

CIO IO GND 2E-12
 CNIO NIO GND 2E-12

PARASITIC CAPACITANCES

CGS1 WD1 STOR 0.69E-15
 CGD1 WD1 1 0.69E-15
 CBTW1 1 WD1 0.45E-15
 CBTS1 1 STOR 0.45E-15

CGS2 REFW REFW REFSTOR 0.69E-15
 CGD2 REFW 2 0.69E-15
 CBTW2 2 REFW 0.45E-15
 CBTS2 2 REFSTOR 0.45E-15

MEMORY CELL, REFERENCE CELL AND BIT LINE CAPACITANCES

C1 STOR VDD 51.4E-15
 CJN1 STOR VDD FBBS
 CBL1 1 VDD 682E-15
 CJNBL1 1 VDD FBBL
 CREP REFSTOR VDD 51.4E-15
 CJNR REFSTOR VDD FBBS
 CBL2 2 VDD 682E-15
 CJNBL2 2 VDD FBBL

\$PROCESS

FILE CM3

\$\$

**TEMP=348

\$TIME(4E-9,124E-9)

\$PLOT *BL1 -NV(1)

\$PLOT *BL2 -NV(2)

\$PLOT *MEMWD-NV(WD1) NOPR

\$PLOT *REFWD-NV(REFWD) NOPR

\$PLOT *NLATCH-NV(3) NOPR

\$PLOT *PLATCH-NV(4) NOPR

\$PLOT *IO -NV(IO)

\$PLOT *NIO -NV(NIO)

\$PLOT *COL -NV(COL) NOPR

\$PLOT *OUT -NV(OUT) NOPR

\$GRAPH,*BL1,*BL2,*MEMWD,*REFWD,*NLATCH,*PLATCH,*IO,*NIO,*COL,*OUT

\$ANAL TIME

CMOS3 PROCESS (FIRST UPDATE) 830606

A : BL1 B : BL2 C : MEMW D : REFW
 E : NLAT F : PLAT G : IO H : NIO
 I : COL J : OUT

CMOS3 PROCESS (FIRST UPDATE) 830606
VALUES OF PLOTTED VARIABLES

TIME(SEC)	*BL1	*BL2	*IO	*NIO
.0	.0	.0	.0	.0
4.000E-09	-1.5328E-03	-1.5371E-03	-5.3897E-11	1.0449E-09
8.000E-09	2.3558E-03	-3.0522E-03	-1.0722E-10	2.0716E-09
1.200E-08	2.4279E-02	-2.6865E-03	-4.9102E-11	3.0884E-09
1.600E-08	5.6760E-02	1.2255E-02	1.3576E-10	4.1780E-09
2.000E-08	9.2042E-02	4.1211E-02	3.6429E-10	5.4095E-09
2.400E-08	.11435	6.2341E-02	5.9686E-10	6.7282E-09
2.800E-08	.12372	7.1600E-02	8.2959E-10	8.0586E-09
3.200E-08	.16222	.10671	1.0625E-09	9.3897E-09
3.600E-08	.32428	.25918	1.2965E-09	1.0722E-08
4.000E-08	.66934	.58918	1.5331E-09	1.2056E-08
4.400E-08	1.0557	.95602	1.7732E-09	1.3395E-08
4.800E-08	1.3559	1.2297	2.0161E-09	1.4735E-08
5.200E-08	1.5888	1.4262	2.2611E-09	1.6078E-08
5.600E-08	1.7715	1.5598	1.0086E-04	1.0089E-04
6.000E-08	1.9171	1.6407	3.0689E-03	3.0444E-03
6.400E-08	2.0042	1.6435	3.2666E-02	3.2249E-02
6.800E-08	1.9940	1.5236	.13297	.13021
7.200E-08	1.8992	1.3045	.31731	.30054
7.600E-08	1.7638	1.1007	.56374	.48402
8.000E-08	1.7214	1.0139	.77136	.61165
8.400E-08	1.7619	.99356	.93232	.69856
8.800E-08	1.8449	.99154	1.0664	.76474
9.200E-08	1.9521	.98791	1.1849	.82047
9.600E-08	2.0756	.97372	1.2916	.86578
1.000E-07	2.2130	.94419	1.3879	.89426
1.040E-07	2.3656	.89393	1.4741	.90033
1.080E-07	2.5350	.82347	1.5512	.89140
1.120E-07	2.7193	.73941	1.6199	.86671
1.160E-07	2.9130	.65071	1.6812	.82704
1.200E-07	3.1072	.56506	1.7360	.77497
1.240E-07	3.2929	.48783	1.7853	.71428

APPENDIX G

SIMULATION OF DECODER OPERATION

S C A M P E R - 2.03.0 FILE=DECODER TIME=00:25 1984-MAY-13 SUN S C A M P

.....
 ' 8 BIT N-CHANNEL DYNAMIC NOR DECODER
 ' USED WITH X22 TEST STRUCTURES

\$SUBCCT RP2E 1 2 3 4 5 6 7
 \$SUBCCT RP2F 1 2 3 4 5 6 7
 \$SUBCCT RP2G 1 2 3 4 5 6 7 8 9 10
 \$SUBCCT RP2I 1 2 3 4
 \$SUBCCT INVB 1 2 3 4

\$
 MBT7 RP2E VDD VSS PC4 G7 NOR B7 NB7
 MBT6 RP2F VDD VSS G6 B6 NB6 VSN NOR
 MBT5 RP2F VDD VSS G5 B5 NB5 VSN NOR
 MBT4 RP2F VDD VSS G4 B4 NB4 VSN NOR
 MBT3 RP2F VDD VSS G3 B3 NB3 VSN NOR
 MBT2 RP2F VDD VSS G2 B2 NB2 VSN NOR
 MBT1 RP2F VDD VSS G1 B1 NB1 VSN NOR
 MBT0 RP2G VDD VSS NPASS PASS G0 NOR INP B0 NB0 VSN
 MIV1 RP2I VDD VSS ROW INP

SVSS VSS VSN

S7 G7 B7
 S6 G6 B6
 S5 G5 B5
 S4 G4 B4
 S3 G3 B3
 S2 G2 B2
 S1 G1 B1
 S0 G0 B0

..... LOAD OF PROBE ON WORD LINE

CROW ROW1 VDD 100E-15

..... DISTRIBUTED LOAD OF WORD LINE

CL1 ROW1 VDD 158E-15
 RROW ROW1 ROW 2291
 CL2 ROW VDD 158E-15

ENOR NOR GND INIT(0)
 EINP INP GND INIT(5)
 EROW ROW GND INIT(0)
 EDD VDD GND 5
 ESS VSS GND 0

```

E7 B7 GND 5
E6 B6 GND 0
E5 B5 GND 0
E4 B4 GND 0
E3 B3 GND 0
E2 B2 GND 0
E1 B1 GND 0
E0 B0 GND 0

```

```

ENB7 NB7 GND 0
ENB6 NB6 GND 5
ENB5 NB5 GND 5
ENB4 NB4 GND 5
ENB3 NB3 GND 5
ENB2 NB2 GND 5
ENB1 NB1 GND 5
ENB0 NB0 GND 5
EPC4 PC4 GND TABLE(0,5) (10E-9,0) (30E-9,0) (40E-9,5)
EPASS PASS GND TABLE(30E-9,0) (40E-9,5)
ENPASS NPASS GND TABLE(30E-9,5) (40E-9,0)

```

```

$PROCESS

```

```

FILE CM3

```

```

$$

```

```

$TIME(2E-9,70E-9)

```

```

$PLOT *PC4 = NV(PC4) NOPR

```

```

$PLOT *PASS = NV(PASS) NOPR

```

```

$PLOT *NOR = NV(NOR) NOPR

```

```

$PLOT *INP = NV(INP) NOPR

```

```

$PLOT *ROW = NV(ROW) NOPR

```

```

$GRAPH *PC4,*PASS,*NOR,*INP,*ROW

```

```

$ANAL TIME

```

CHOS3 PROCESS (FIRST UPDATE) 830606

A : PC4 B : PASS C : NOR D : INP
E : ROW

END

11-06-86

FIN