ANALYSIS AND DESIGN OF A SCALABLE DIGITAL INPUT
CLASS D AUDIO AMPLIFIER TOPOLOGY

By
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Abstract

A digital input Class D audio amplifier is investigated in this thesis. The intended application is headphone enabled portable audio players such as smart phones and tablets. The topology is intended to be predominately digital and thereby allow for rapid scaling in deep submicron CMOS processes. Class D was chosen for its natural compatibility with pulse modulation schemes and theoretical 100% efficiency. Current Class AB amplifiers offer very good audio quality but generally poor efficiency.

The Class D amplifier with global feedback was prototyped with a Field Programmable Gate Array (FPGA) and commercial 16b Analog to Digital converter (ADC). Measurement and simulation results indicate stable operation with greater than 30 dB of noise rejection at 1 kHz. A revised design operating at a lower frequency with improved noise rejection was simulated.

An integral component of the topology is the 2.82 Msps 16b ADC. To meet the power specification of <5 mW a unique variant of the successive approximation algorithm termed the Configurable Offset with Preamplifier (COP) ADC was developed. The core of the ADC consists of a preamplifier array and latched comparator. Intentional mismatches are introduced to produce voltage references for the conversion process and thereby eliminating the need for a Digital to Analog Converter (DAC). The core circuits of the COP ADC were implemented in 0.13 μ m CMOS. The COP ADC required external digital control and clocks via a FPGA. A passive charge sharing sample and hold circuit and calibration algorithm are also required for a complete solution.

Both AC and DC automated measurements yield 13.8b resolution over a 293 mV_{pp} operating range and 6.25 MHz comparator clock. The maximum INL=0.5 LSB, DNL=1 LSB and core power consumption of 1.5 mW. In addition, gain and rejection ratio formulas for a asymmetric differential pair amplifier were derived and correlated well with simulation results.

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List of Abbreviations and Symbols

A_{cm}	common mode voltage gain
A_{cm-dm}	common to differential mode voltage gain
A_{dm}	differential mode voltage gain
A_{dm-cm}	differential to common mode voltage gain
ADC	analog to digital converter
CDRR	common mode to differential mode rejection ratio
CMRR	common mode rejection ratio
CMOS	complimentary metal oxide semiconductor
COP	configurable offset with preamplifier
C_{gb}	gate-bulk capacitance of a MOSFET
C_{gd}	gate-drain capacitance of a MOSFET
C_{gs}	gate-source capacitance of a MOSFET
C_{ox}	total gate capacitance
dB	decibels
dBfs	decibels relative full scale
dBm	$10 \log_{10}(\text{Power in Watts}/1 \text{ mW})$
dBV	$20 \log_{10}(\text{Voltage in } V_p)$
dB μ V	$20 \log_{10}(\text{Voltage in } \mu V_p)$
dBV $_{rms}$	$20 \log_{10}(\text{Voltage in } V_{rms})$
dB μ V $_{rms}$	$20 \log_{10}(\text{Voltage in } \mu V_{rms})$
DCRR	differential to common mode rejection ratio
DAC	digital to analog converter

DEM	dynamic element matching
DNL	differential nonlinearity
DPWM	digital pulse width modulator
DSP	digital signal processing
η_c	collector efficiency
ϵ_{ox}	dielectric permittivity of SiO ₂
FIR	finite impulse response filter
FPGA	field programmable gate array
GM	gain margin
g_m	transconductance
g_{mb}	bulk conductance
INL	integral nonlinearity
k	Boltzmann constant ($1.3809 \times 10^{-8} \text{ fC} \cdot \text{V/K}$)
LPF	least significant bit
LSB	low pass filter
MASH	multi-stage noise shaping
MOSFET	metal oxide semiconductor field effect transistor
MP3	MPEG-1 audio layer 3
NFET, NMOS	N-channel field effect transistor
NPWM	natural sampling pulse width modulation
OSR	oversampling ratio
PA	power amplifier
PCB	printed circuit board
PFET, PMOS	P-channel field effect transistor
PI	proportional-integral
PID	proportional-integral-derivative
PM	phase margin
PWM	pulse width modulator
r_o	transistor output resistance
R_{ds}	drain to source resistance
RF	radio frequency
RMS	root mean square
SAR	successive approximation register
SDM, $\Sigma\Delta$	sigma-delta modulator

SMPA	switching mode power amplifier
SNR	signal to noise ratio
THD	total harmonic distortion
THD+N	total harmonic distortion plus noise
T	temperature in Kelvin
t_{ox}	gate oxide thickness
UPWM	uniform sampling pulse width modulation
V_{DS}, v_{ds}, V_{ds}	drain-source voltage
$V_{DS(sat)}$	drain-source saturation voltage
V_{GS}, v_{gs}, V_{gs}	gate-source voltage
V_{OD}, v_{od}, V_{od}	overdrive voltage ($V_{od} = V_{gs} - V_{th}$)
V_{th}	threshold voltage
ω	2π frequency (rad/sec)

Chapter 1

Introduction

There are a multitude of electronic devices with audio recording and playback capability. Be it smart-phones, tablets, laptops, or wireless headsets, these ubiquitous devices are a mainstay of modern society. In particular, portable, battery operated devices require reliable and energy efficient solutions. For such applications quality audio performance and extended battery life are critical factors.

The level of integration in various portable electronic devices continues to expand while also being shrunk to more compact form factors. This trend is, in part, facilitated by the continued scaling of transistors. According to Moore's law [3], the number of transistors on an integrated circuit will double every 18 months. While porting digital designs to new processes is relatively straightforward, analog designs can require significant redesign effort. Moreover, power efficiency is critical in alleviating thermal stress and extending battery life. New power efficient architectures that are readily ported to new processes are highly desirable. This essentially entails an alternate design methodology in which the analog functionality is shifted as much as possible into the digital domain.

In a digital audio system the Power Amplifier (PA) has historically been the most inefficient and biggest energy consuming component. To derive a highly efficient audio amplifier without compromising audio performance is a significant challenge. Amplifiers can be divided into either linear or switching mode type with the majority of audio systems being linear amplifiers. While linear amplifiers offer good audio quality the efficiency can be very poor. Switching mode amplifiers are potentially much more efficient and are amenable to digital pulse modulation techniques. Given these two advantages the industry is trending towards adopting switching mode amplifier technology.

High efficiency audio amplifier requirements are motivated by different factors according to a given application. For example, thermal issues are critical for home audio amplifiers with high output power multi-channel loads, while for portable audio devices, battery life is of utmost importance. Of course, systems with high efficiency will deliver both extended battery life and reduced thermal stress in a more compact form factor.

One of the challenges in designing switching mode PA's is to produce high quality audio with low distortion. Switching mode PA's are coupled to digital pulse modulators. Any perturbation in the modulated waveform amplitude or timing leads to distortion. The PA needs to be linearized to correct such errors. This can be accomplished with a variety of techniques such as negative feedback, feed forward or pre-distortion for example.

The research in this thesis is in the domain of low power and high efficiency digital audio circuitry for portable battery operated devices. In particular, an architecture is proposed which features: a switching mode amplifier, direct digital input, a merger of the Digital to Analog Converter (DAC) and Power Amplifier (PA) circuits, and global feedback with a digital loop filter. Traditional solutions consider the main blocks in an audio system such as the DAC, modulator and PA as separate entities and are designed individually whereas here, a more fully integrated approach is taken. Another feature of the proposed architecture is that it is highly digital and designed to scale with minimum redesign effort. The challenges, advantages and disadvantages of this approach will be discussed.

1.1 Motivation

Transistors continue to scale unabated according to Moores law. According to the semiconductor roadmap [4] the current 22nm devices in 2012 are forecasted to scale to 5.9nm by 2026. Smaller devices provide greater economies of scale, higher levels of integration and higher operating frequencies. While digital circuits immediately benefit from scaling, analog, mixed-signal and RF circuit designers are faced with significant challenges [5]. Lower supply voltages and short channel effects such as reduced channel impedance (r_{ds}), hot-carrier effects and velocity saturation complicate the design of scaled analog circuits. Thus, it is apparent that any mixed signal circuit which maximizes the digital circuitry and minimizes the analog circuitry will more readily and expeditiously benefit from CMOS scaling. Such circuits will benefit from lower cost due to reduced die size, lower power as a result of lower parasitic capacitances, and higher yield due to

the level of digital integration.

The application of interest here is portable digital audio players. In particular, headphone enabled devices such as tablets, smart phones and MP3 players where power efficiency is crucial. That is, the circuit efficiency must be maximized to extend battery life. Furthermore, if the system architecture is such that it is predominately digital then device scaling benefits are more readily achieved. Thus the focus of this report will be in developing a robust system architecture with a high level of digital integration and efficient power amplifier that lends itself to the benefits of scaling. Audio signals are analog by nature, therefore there is no such thing as a purely digital audio amplifier and some degree of analog signal processing is inevitable.

1.2 Objectives

The thesis objectives are as follows:

- To investigate fully CMOS integrated, digital input, switching mode audio amplifiers for low voltage, low power applications.
- To linearize the PA with global feedback and a digital loop filter.
- To incorporate a design that is highly digital and readily scalable to new processes. The power consumption should be comparable to current linear analog amplifiers.

To achieve these goals requires a novel approach to the system architecture and circuit design. This inherently involves a certain degree of risk associated with the new methodology. The risk is somewhat mitigated by simulations and prototyping as much as possible prior to integrated circuit fabrication.

1.3 Contributions

This research makes contributions in the field of digital audio amplifiers for headphone enabled devices. Such devices require a maximum of 10mW of power for sufficient volume. In particular, the contributions can be classified as either related to system analysis or ADC design. The contributions are as follows.

Analysis and design of a scalable low power digital input, switching mode Class-D amplifier system that is linearized by means of digital feedback. The operating frequency is $1/8$ that of a high power system with digital feedback [6]. The system analysis and prototype measurements

are published in the following article [7].

T. Forzley and R. Mason, "A low power Class D audio amplifier with discrete time loop filter compensation," in *Circuits and Systems and TAISA Conference, 2009. NEWCAS-TAISA '09. Joint IEEE North-East Workshop on*, pp. 1-4, June, 2009.

Contributions were also made in the area of low power ADC design. The COP ADC is an alternate approach to the conventional SAR ADC that eliminates the need for a Digital to Analog Converter (DAC). Instead, the DAC reference voltages are replaced with offset voltages induced by intentional circuit asymmetry. High resolution offset control is achieved using a unique combination of mismatch techniques.

The core components of a low power Configurable Offset with Preamplifier (COP) ADC were fabricated in the IBM 0.13 μm CMOS process. The circuitry includes a preamplifier array, comparator, biasing and digital interface circuitry. Testing yielded a 14b resolution, significantly higher than current state of the art 6b implementation [8]. Though further development is required for a fully functional solution, the configurable offset approach is a unique alternative. The COP ADC architecture and simulation results were published in the following article [9].

T. Forzley and R. Mason, "A scalable Class D audio amplifier for low power applications," in *Audio Engineering Society Conference: 37th International Conference: Class D Audio Amplification*, pp. 11-20, Aug. 2009.

Formulas for differential and cross coupled gains of an asymmetric differential amplifier were derived based on an equivalent half circuit analysis [10]. The formulas were verified in simulations of mismatched differential amplifiers. To the best of the authors knowledge these formulas have not been published elsewhere.

The contribution towards a low power scalable Class D power amplifiers has been acknowledged by the Audio Engineering Society (AES). In a review of Class D power amplifiers the AES journal included system block diagrams and measurement results from the authors aforementioned publications. The article citation is [11].

F. Rumsey, "Class D power amplification," *J. Audio Eng. Society*, vol. 57, no. 12, pp. 1087-1093, Dec. 2009.

1.4 Organization

The report begins with a background introduction to classical and modern audio systems followed by the simulation, prototype and analysis of the proposed system. The background and literature review serve to highlight the motivating factors in deriving the proposed architecture. Test and measurement results for both a FPGA system prototype and application specific integrated circuit are included. Finally, the conclusions section summarizes the key accomplishments and future work that remains. Each chapter includes a summary of key points.

Chapter 2 provides an introduction to the key elements of a digital audio system. Fundamental background information regarding pulse modulators and power amplifier design is included. Pulse width and sigma delta modulator concepts are explained and compared. In the power amplifier section, classes of linear and switching mode amplifiers are discussed. This chapter highlights the potential large gains in efficiency as the motivation in migrating to switching mode amplifiers.

Chapter 3 presents the portable audio system target specifications followed by an introduction to amplifier linearization techniques. A literature review of switching mode audio systems is presented. The publications are sorted and categorized according to the input signal type (analog or digital) and feedback (open loop, local or global feedback). Emphasis is placed on digital input designs. The trade-offs among the various architectures is discussed.

Chapter 4 details the system architecture investigated. The overall system operation is explained followed by a description and analysis of each block. Closed loop operation is analyzed in the frequency domain based on Bode plots and phase margin analysis to design an analog loop filter that is transposed into the digital domain. The simulation, design, construction and testing of a prototype is presented. An alternate, lower power variation of the system is presented with simulation results. The final section analyzes switching and conduction losses in Class D PAs.

Chapter 5 begins with a discussion on the general SAR ADC algorithm followed by an introduction to the COP ADC architecture. The circuit design and CMOS implementation are presented followed by analysis and simulation results.

Chapter 6 includes a description of the hardware and software for both DC and AC testing of the integrated circuit. Measurement results are compared to simulation results. A table to compare the work to current publications is included.

Chapter 7 includes conclusions and recommendations for future work.

Chapter 2

Background

Predominately, all audio is now distributed in digital format with analog systems virtually non-existent. Consumer audio playback, distribution and duplication is solely a digital process performed on a personal computer, tablet or smartphone. Fig. 2.1 is a typical digital audio player consisting of five main components:

- A digital audio source which streams the bits at a specific frequency, i.e. 16 bits at 44.1 kHz
- A modulator to modulate the data into a high frequency pulse stream.
- A Digital to Analog Converter (DAC) to convert the modulator data to an analog waveform.
- A Power Amplifier (PA) to drive the load with sufficient power for the desired audible level. The PA can also include filtering.
- Speakers that convert electrical energy into audible sound waves.

Each of these components will now be discussed in more detail.

Figure 2.1: Digital audio system block diagram.

2.1 Digital Audio Source

Historically, digital audio has been based on the “redbook” standard otherwise known as CD-DA (Compact Disc-Digital Audio). Developed in 1980 by Philips and Sony it was intended to be a universal medium for distributing digital audio. The audio data is Pulse Code Modulated (PCM) with 16b per channel resolution at a rate of 44.1kHz which corresponds to 1.4112 Mb/s for stereo.

To reduce storage requirements for portable devices, CD's are often converted to various lossy compressed audio formats. MP3 is a lossy compressed audio format designed to compress the file while still remaining faithful to the original. MP3 reduces the data rate ranging from 96 to 320 kb/s with the higher rate delivering better audio quality. Thus, at 128 kb/s the storage requirements are reduced by 11:1 compared to PCM. The compression method is referred to as perceptual coding [12]. Psychoacoustic models are used to discard or reduce precision of components deemed less audible to human hearing.

Lossless compression formats enable the original uncompressed data to be recreated exactly. That is, no information is removed from the source and the compressed file is completely faithful to the original. Examples of lossless audio formats are Free Lossless Audio Codec (FLAC), WavPack, and Apple Lossless Audio Codec (ALAC). Typically, a compression ratio of about 2:1 relative to PCM is achieved. Lossless compression formats are evaluated based on processing requirements and compression ratio.

2.2 Modulator

Pulse modulators which are common in audio applications, encode data into a stream of binary pulses with variable widths or density. These pulses are compatible with switching mode amplifiers that operate as switches in either a “high” state with the load connected to the DC supply or in “low” state with the load connected to ground. The two predominant modulators are Pulse Width Modulation (PWM) and Sigma-Delta Modulation (SDM or $\Sigma\Delta$). Although the output of the modulators are binary, they are distinctly analog and susceptible to timing and amplitude errors. This is an important fact to keep in mind during the course of the audio system design.

Figure 2.2: Natural sampling PWM (NPWM) circuit.

2.2.1 Pulse Width Modulation

A Pulse Width Modulation (PWM) scheme is shown in Fig. 2.2. The circuit compares the input waveform $v_i(t)$ to a carrier waveform $v_c(t)$ resulting in a pulse output with variable duty cycle $d(t)$. The sawtooth carrier frequency is on the order of 400-600 kHz for 20 kHz audio bandwidth. This method of generating PWM is referred to as Natural sampling PWM (NPWM). The carrier waveform can be trailing edge, leading edge or triangular which is preferred due to its lower harmonic content [13]. Sources of error include jitter in the carrier waveform, non-linear rise and fall times of the sawtooth waveform, power supply noise, and slew rate limiting of the comparator.

In the case of a digital input $v_i(t)$, a method to mimic the analog NPWM process is required. Therein lies the problem, to translate PWM from an inherent analog process to a digital one without introducing distortion. To emulate NPWM in a digital process would require $v_i(t)$ to be sampled at an infinite rate and is therefore not possible. The simplest sampling process to approximate NPWM is the Uniform PWM (UPWM) process which samples the waveform at regular intervals however, UPWM introduces significant distortion and is therefore undesirable. Fig. 2.3 highlights the difference between NPWM and UPWM. While the natural sampling correctly determines the intersection points, the uniform sample introduces distortion indicated by Δ in Fig. 2.3. Various algorithms try to predict the intersection point [14] with the goal being to optimize accuracy while minimizing computation complexity.

The linearity of the different sampling processes can be determined analytically from a double

Figure 2.3: PWM waveforms for the natural sampling (NPWM) and uniform sampling (UPWM) processes.

fourier series expansion [14]. The final results of which are given in equations (2.2.1) and (2.2.2) for NPWM and UPWM respectively. These equations are useful in calculating the distortion arising from a particular sampling process.

$$F_{NPWM}(t) = K + \frac{M}{2} \cos(\omega_i t) + \sum_{m=1}^{\infty} \left[\frac{\sin(m\omega_c t)}{m\pi} - \frac{J_0(m\pi M)}{m\pi} \sin(m\omega_c t - 2m\pi k) \right] - \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm \infty} \frac{J_n(m\pi M)}{m\pi} \sin \left(m\omega_c t + n\omega_i t - 2m\pi k - \frac{n\pi}{2} \right) \quad (2.2.1)$$

$$F_{UPWM}(t) = K - \sum_{n=1}^{\infty} \frac{J_n \left(\frac{n\pi\omega_i}{\omega_c} \right)}{\frac{n\pi\omega_i}{\omega_c}} \sin \left(n\omega_i t - \frac{2n\pi k\omega_i}{\omega_c} - \frac{n\pi}{2} \right) + \sum_{m=1}^{\infty} \frac{\sin(m\omega_c t) - J_0(m\pi M) \sin(m\omega_c t - 2m\pi k)}{m\pi} - \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm \infty} \frac{J_n((m\omega_c + n\omega_i) \frac{\pi M}{\omega_c})}{(m\omega_c + n\omega_i)} \sin \left[(m\omega_c + n\omega_i) \left(t - \frac{2\pi k}{\omega_c} \right) - \frac{n\pi}{2} \right] \quad (2.2.2)$$

For the NPWM process the four components of (2.2.1) are explained as follows,

- The first term K is simply the DC component.
- The second term represents the input signal from which we note there are no harmonics, only the fundamental
- The third term represents the high frequency carrier and its harmonics. Since the carrier frequency is much higher than the input signal it is outside the audio band. These tones are usually low pass filtered.
- The fourth term is the intermodulation products of the carrier and input signal. It is noted that for n=-1 to -∞ foldback distortion occurs. The degree of distortion is a function of the modulation index M, the ratio of ω_c/ω_i and the bandwidth of interest.

For UPWM the first, third and fourth terms in (2.2.2) are similar to (2.2.1). The second term corresponds to the input signal and its harmonics which are distortion terms absent in NPWM. Fig. 2.4 is a plot of the UPWM second and third order harmonics normalized to the fundamental for a modulation index M=1. For the UPWM process it is evident that a large oversampling ratio is required for low harmonic distortion. For example, a 20 kHz bandwidth signal with a sampling ratio on the order of 5,000 (100MHz) would generate -70dBc second order distortion.

A PWM waveform could be directly derived from the digital data using the circuit shown in

Figure 2.4: Second and third order harmonic distortion relative to fundamental with $M=1$.

Fig. 2.5. This circuit converts a b -bit input at sample rate f_s to a PWM waveform with the same frequency as f_s . Note that the counter requires a high speed $2^b f_s$ clock to define the timing edges for the digital modulator and is therefore critical in maintaining system performance and limits the practical application of this architecture. For PCM audio system with 16-bit resolution and a samples rate of 44.1 kHz the minimum pulse width that must be precisely controlled is,

$$\delta t = \frac{1}{2^b f_s} = \frac{1}{2^{16} \cdot 44.1 \times 10^3} = 346 \text{ ps} \quad (2.2.3)$$

which is on the order of 2.9 GHz. While this is possible with modern CMOS processes several complications arise. Three predominant limitations towards a practical implementation are,

- The high speed bit clock must be stable so as not introduce jitter. Any jitter in the clock signal creates distortion which degrades audio quality. The jitter must be limited to a small fraction of the minimum pulse width.
- The digital circuit must eventually drive the switching amplifier. A Class D switching amplifier is a large inverter (with large parasitics) capable of driving low impedance loads. To drive the switching amplifier with fast slew rates will require a large tapering ratio. This would increase current consumption and reduce overall efficiency.
- The direct implementation of PCM to PWM in this manner is a uniform sampling process

Figure 2.5: Direct digital conversion PCM to PWM

(UPWM) and is inherently non-linear. To improve linearity the data must be oversampled which in turn further compounds the jitter and power issues.

In conclusion, the direct PCM to PWM digital conversion is not practical. As such there are a variety of methods to reduce harmonic distortion in the PCM to PWM process [14], [15], [16].

2.2.2 Sigma-Delta Modulation

Sigma-Delta ($\Sigma\Delta$ or SDM) modulators are used extensively in data converter applications. Traditional Nyquist rate converters operate moderately above the Nyquist rate (twice the signal bandwidth) and their linearity and accuracy are inherently limited by component matching accuracy. On the other hand SDM converters operate on the principle of oversampling and noise shaping which requires considerable digital circuitry and some analog stages. While such converters tend to operate at significantly higher sampling rates compared to Nyquist converters, the stringent component matching accuracy requirements are relaxed. Thus, SDM data converters obtain higher resolution at the expense of increased digital circuitry and higher frequencies. As CMOS devices continue to scale smaller the trade-off becomes more economical and oversampling converters will continue to infringe on applications once dominated by Nyquist converters. Audio applications with bandwidths of 20kHz and high resolution requirements on the order of 16-24

Figure 2.6: First order Sigma-Delta modulator: a) System block diagram, b) Input and output time domain waveforms, c) Noise shaped spectral output.

bits are ideally suited to SDM implementation.

The operation of a first order modulator is illustrated in Fig. 2.6 with input $U(z)$, output $V(z)$ and quantization error $E(z)$. In the case of an ADC the quantization error $E(z)$ models the difference between the discrete ADC levels and the analog input signal. Detailed and comprehensive analysis can be found in [17]. Linear analysis of Fig. 2.6a yields,

$$V(z) = z^{-1}U(z) + (1 - z^{-1})E(z) \quad (2.2.4)$$

which indicates that the output is the sum of the delayed input $U(z)$ plus $E(z)$ multiplied by $(1 - z^{-1})$ which has a high pass transfer function as shown in Fig. 2.6c. This characteristic of suppressing baseband noise and shifting it to higher frequencies is referred to as *noise shaping*. Higher L^{th} order loop filters yield more aggressive noise shaping $(1 - z^{-1})^L$ which in turn, increases the resolution by $L+1/2$ bits. Fig. 2.6b is a time domain plot of the modulated output for a sinusoidal input.

2.3 Digital to Analog Converter

An ideal Digital to Analog Converter (DAC) converts the digital input into an analog signal without distortion and a high Signal to Noise Ratio (SNR). The DAC can be either of Nyquist or over sampled architecture. In the Nyquist case the modulator block in Fig. 2.1 is not necessary. The Nyquist DAC directly converts the 16b output from the digital audio source to an equivalent analog signal.

With an oversampling DAC a modulator is used to reduce the number of bits. For example, a SDM can effectively reduced the 16b to a single bit with high fidelity. In this case the binary output is is directly compatible with switching mode amplifiers.

2.4 Power Amplifier

The Power Amplifier (PA) must reliably and efficiently deliver sufficient power to the load. In this application the load is a headphone typically with an impedance of 16Ω or 32Ω . PA designs with low efficiency will generate heat, dissipate significant power and increase battery drain.

Power amplifiers are generally classified into two categories either linear or switching. The term “linear” does not imply that such amplifiers do not exhibit any non-linear behavior but rather act as a current source with the output voltage proportional to the input. That is, the transistor is in the saturation region for some period of time. Examples of linear PA’s are Class A, AB, B and C.

In switching mode PA’s such as Class D, E and S, the transistor operates as a switch in either an open or short state. These PA’s are directly compatible with pulse modulation schemes such as PWM or SDM being the most common.

2.4.1 Linear Amplifiers

A schematic for the linear amplifiers Class A, AB, B and C is shown in Fig. 2.7 where M1 is nMOS transistor, RFC is a choke, C_b is DC blocking capacitor, LC is a parallel tank circuit and R is the load resistor. The tank circuit is resonant at the operating frequency at which point it is ideally infinite impedance and a short circuit for all other frequencies. This ensures that the output voltage across the load resistor is sinusoidal. Depending on the bias conditions imposed at v_g the current conduction i_d in the driver transistor will vary. The fraction of a full cycle for

Figure 2.7: Basic circuit configuration of a single ended Class A, AB, B or C amplifier.

Table 2.1: Conduction angles and efficiency ratings for linear mode amplifiers.

Class	Conduction Angle	Maximum Theoretical Efficiency
A	360°	50%
AB	180° - 360°	50% - 78.5%
B	180°	78.5%
C	0° - 180°	78.5% - 100%

which i_d flows is referred to as the conduction angle where a full cycle is 360°.

Table 2.1 lists the different classes of linear amplifiers according to the conduction angles from 360° for full conduction to 0° for no conduction. In addition, the maximum theoretical efficiency corresponding to each class is specified.

The efficiency values in Table 2.1 are the theoretical limit under maximum output power conditions. When the output voltage is less than full scale the efficiency is significantly reduced. In this case, the difference between the output and the supply voltage is dropped across the output transistor resulting in wasted energy. There are many variations of the linear amplifier design which attempt to alleviate this affect.

As an example, one architecture to minimize this affect is the Class G amplifier in which multiple supply voltages are used [18], [1]. G2 refers to two voltage supplies, G3 to three supplies and so on. By lowering the supply voltage for low level signals the energy wasted in the output transistor is reduced. While improving the overall efficiency the requirement for multiple supply

Figure 2.8: Current-Voltage plane operating locus of different power amplifier classes.

voltages, drive control circuitry and crossover distortion detract from the efficiency improvements.

2.4.2 Switching Mode Power Amplifiers

Switching Mode Power Amplifiers (SMPA) operate fundamentally differently than linear amplifiers. Fig. 2.8 illustrates the typical load lines in the current-voltage plane for different classes of amplifiers and illustrates the difference between linear and switching amplifiers. For SMPAs in which the devices are either switched off (no current flow) or on (current flow with ideally zero on resistance) the amplifier dissipates no power. Conventional Class A, AB and C designs have load lines that swing through a locus with a high current-voltage (power) product while the switching amplifier essentially hugs the axis with small current-voltage product, ideally zero. Furthermore, it will be shown that Class A through C amplifiers theoretical efficiency is reduced as the drive level is reduced relative to full scale while SMPAs are essentially constant. This is important in audio systems as the volume is often backed off from full scale in typical background music listening.

An inherent disadvantage of SMPAs is Electromagnetic Interference (EMI) arising from the transient rail-to-rail switching action. EMI can result in failure to meet regulated FCC (North America) or CE (European) standards. The EMI frequency spectrum is modulation dependant

and as such is different for PWM and SDM implementations. EMI can cause conductive or radiated interference.

SMPAs are identified using an alphabetic nomenclature in continuation from the linear amplifiers. The most common switching amplifiers are Class D and E. The difference being related to the application requirements on bandwidth and switching frequency. Class D is applicable at lower frequencies (up to MHz range) and Class E is adopted at higher frequencies (up to GHz range). For applications with switching frequencies on the order of kHz to the MHz range the switching time (rise and fall times) are not a significant fraction of the switching period. In these cases Class D is suitable. Such applications include DC-DC converters and audio amplifiers for example. For audio applications with PWM or SDM signals the switching rate may be a few hundred kHz to a few MHz depending on the modulator architecture.

Audio applications of Class D have been commercially adopted by many semiconductor companies. The designs vary in output power capability depending on intended use, i.e. low power portable designs (mW output) or high power home or automotive (several watts) audio systems. Some example manufacturer part numbers and output power capabilities are Texas Instruments (TPA2010D1 / 2.5W), Maxim (MAX9700 / 1.2W, MAX9709 / 50W) and Wolfson (WM88956 / 40mW).

Applications at high frequency can be limited by the ability of the transistor to behave as a near ideal switch. At Radio Frequencies (RF) the switching time can become a significant fraction of the switching period thereby reducing efficiency while increasing noise and distortion. In an attempt to overcome finite switching times the Class E amplifier was developed [19]. Class E is a switching mode amplifier which has a load network synthesized to eliminate simultaneous voltage and current during switching and is tolerant to finite switching times.

The standard binary SMPA switching scheme can be extended to multi-levels. This reduces the peak voltage across each device and minimizes switching losses by lowering the switching frequency [20].

2.5 Speakers

Speakers are transducers which convert electrical signals into audible sound waves. They are specified by bandwidth, impedance, sensitivity and maximum power capability. For example, a low cost pair of ear bud type headphone speakers (Sony MDR-E8181) have a $16\ \Omega$ impedance, 12

Figure 2.9: Headphone impedance measurement of Sony MDR-E8181.

Hz to 22 kHz bandwidth and a 108 dB/mW sensitivity. The impedance measurement is shown in Fig. 2.9. The impedance is $16\ \Omega$ over the audio bandwidth and exhibits a resonance at 2.25 MHz.

A Class D switching mode amplifier with single and differential load configurations is shown in Fig. 2.10. Headphones are typically connected in the single ended configuration while earpiece or hands free speakers are connected in a differential or Bridge Tied Load (BTL) configuration. BTL offers the advantage of suppressing common mode noise and providing twice the voltage swing across the load for a given supply voltage. This provides a quadrature increase in available power. The disadvantage of BTL is the need for extra components.

Figure 2.10: Speaker connection configurations, a) single ended, b) differential or BTL.

2.6 Power Amplifier Efficiency

In this section PA efficiency is analyzed for both linear and switching mode amplifiers. Efficiency formulas are defined followed by theoretical calculations for both linear and switching mode amplifiers.

2.6.1 Definitions

Efficiency is broadly defined as the ratio of the output power to the input power. In specifying the efficiency one must specify whether or not the input power includes both the DC supply and the RF drive power or only the DC supply power. The most common definitions are as follows [21].

The collector efficiency is defined as,

$$\eta_c = \frac{P_o}{P_{dc}} \quad (2.6.1)$$

Where P_o is the output power dissipated in the load and $P_{dc} = V_{dc}I_{dc}$ is the power extracted from the DC supply to the collector or drain of the power amplifier. The P_o term includes the fundamental and harmonic components but the harmonics tend to be negligible relative to the fundamental.

The overall efficiency takes into account the input drive level which can be significant and is defined as,

$$\eta_o = \frac{P_o}{P_{dc} + P_{in}} = \frac{P_o}{P_{dc} + P_o/G_p} \quad (2.6.2)$$

where the power gain is given as,

$$G_p = \frac{P_o}{P_{in}} \quad (2.6.3)$$

Finally, the power added efficiency which takes into account the input power is defined as,

$$\eta_{pa} = \frac{P_o - P_{in}}{P_{dc}} = \frac{P_o - P_o/G_p}{P_{dc}} \quad (2.6.4)$$

From the various definitions it is apparent that one must use caution to compare different

Figure 2.11: Maximum theoretical collector efficiency η_c versus conduction angle.

designs using the same criteria and efficiency formulas. The standard within this report will be to use the collector efficiency definition.

2.6.2 Linear Power Amplifier Efficiency

Fig. 2.11 is an extension of Table 2.1 in which the efficiency is plotted for all conduction angles. We observe that theoretically 100% efficiency can be achieved, however as indicated in Fig. 2.12, the output power decreases to zero. This implies that as we decrease the conduction angle to increase efficiency we must increase the peak collector current to satisfy the drive requirements. Ultimately, the selection of the conduction angle is a trade-off among collector efficiency, peak collector current and power gain. Detailed derivations of the equations to create these plots can be found in [21] and [22].

It should be emphasized that the efficiencies of Fig. 2.11 are for an ideal circuit with full scale output. Should the output power be reduced so will the efficiency. To examine the impact on efficiency due to output swing we define,

Figure 2.12: Normalized maximum power output capability versus conduction angle.

$$\beta = \frac{V_{op}}{V_{cc}} \quad (2.6.5)$$

where V_{op} is the peak amplitude of the sinusoidal output as measured at the load resistor ($0 \leq \beta \leq 1$). The collector efficiency equations which take into account drive levels for Class-A, B and G (two levels) amplifiers are,

$$\eta_A = \frac{\beta^2}{2} \quad (2.6.6)$$

$$\eta_B = \beta \frac{\pi}{4} \quad (2.6.7)$$

$$\eta_G = \frac{\beta \frac{\pi}{4}}{(\alpha + (1 - \alpha) \cos \theta_t)} \quad (2.6.8)$$

where

$$\theta_t = \begin{cases} \pi/2 & : \beta \leq \alpha \\ \arcsin(\alpha/\beta) & : \beta \geq \alpha \end{cases}$$

and α is the fraction of V_{cc} for the two level Class G amplifier.

Figure 2.13: Collector efficiency η_c of ideal Class-A, B, G2 ($\alpha=0.5$) amplifiers.

The collector efficiency for Class A, B and G are plotted in Fig. 2.13 with β expressed in dB full scale ($\beta=1$ is 0 dBfs). Significant efficiency reduction is encountered as β decreases. Furthermore, real world signals with amplitude variation will effectively reduce the efficiency. The peak to average or crest factor for a waveform γ can be calculated by,

$$CF = \frac{|\gamma|_{peak}}{\gamma_{rms}} \quad (2.6.9)$$

which for a sinusoid is $\sqrt{2}$ or 3dB. The net impact of the crest factor is to reduce the average efficiency of the amplifier. Music and audio typically are modeled with Gaussian probability distribution functions from which the average efficiency is calculated. The average efficiency for various crest factors with optimized α parameter at each crest factor is plotted in Fig. 2.14.

Given the efficiency dependance on output power (volume), it would be useful to know preferred listener volume settings. An empirical study [23] indicates that for 99% of time the listener will set the music volume at or below -24 dBfs. While this is a generalization, it serves to highlight that many listeners tend to set the volume well below full scale. For the linear amplifier designs this is detrimental to efficiency however, Class D amplifiers maintain a theoretical 100% efficiency.

By way of example consider what a Class B amplifier might realistically achieve in terms of

Figure 2.14: Average efficiency for Class B, G2 (two level) and G3 (three level) for audio signals with Gaussian probability distribution function [1].

efficiency. The efficiency will be very low considering a typical audio signal has a crest factor on the order of 12-20 dB and the listener will generally back off the volume anywhere from -10 to -40 dBfs. Assuming a modest crest factor of 10dB from Fig. 2.14 we obtain $\eta_{avg} \approx 39\%$. Furthermore, the efficiency must be derated according to the volume setting. Assuming the volume is set at -20 dBfs from (2.6.7) $\eta_{avg} \approx 3.9\%$. The efficiency is significantly lower than the theoretical limit of 78.5%.

To estimate the efficiency the following factors need to be considered,

- Consider which Class of PA is to be used. e.g. A, B, AB, G2, G3, etc.
- Estimate the crest factor and extrapolate η_{avg} from Fig. 2.14.
- Estimate the nominal volume setting (dBFS).
- Derate the efficiency according to the corresponding formula for the class of PA being used.
- Factor in any non-idealities of the circuit such as component losses and nominal bias.

2.6.3 Class-D Efficiency

As previously stated, classical amplifier designs such as Class A and AB suffer from poor efficiency at low drive levels. For signals with high crest factors the overall efficiency can be very poor.

Figure 2.15: Class D circuit: (a) MOS circuit schematic, (b) equivalent ideal circuit.

These amplifiers provide the best efficiency results with constant envelope modulation schemes and high drive levels. Alternatively, the theoretical efficiency of Class D amplifiers is 100% independent of output level.

Class D is a switching mode amplifier using two active devices driven in a two-pole switch configuration. The output of which defines a rectangular voltage waveform at the input to a tuned load circuit. The load circuit uses either a band-pass or low-pass filter to remove harmonics and extract the fundamental. For audio systems a low pass filter is required. A Class D amplifier with a series tuned LC filter and its switching equivalent is shown in Fig. 2.15a. The equivalent ideal switching model in Fig. 2.15b. In analyzing the circuit the following assumptions are made:

- The series resonant LC circuit is tuned to the switching frequency at which point it exhibits zero impedance. At all other frequencies the impedance is infinite. This ensures a sinusoidal output at the switching frequency and eliminates the inherent harmonics from the square wave voltage waveform imposed by the switching action at the input to the load network.
- The MOS switches have zero ON resistance and infinite OFF resistance and can switch instantaneously without crossover distortion.
- Device parasitics are ignored and the load network components are ideal.

Assuming a 50% duty cycle square wave input, the voltage waveform of Fig. 2-16a can be expressed mathematically as,

$$v_2(\theta) = \begin{cases} V_{cc} & : 0 \leq \theta \leq \pi \\ 0 & : \pi \leq \theta \leq 2\pi \end{cases} \quad (2.6.10)$$

where $\theta = \omega t$. Using Fourier analysis $v_2(\theta)$ can be expressed as a summation of sinusoids [24],

$$v_2(\theta) = V_{cc} \left(\frac{1}{2} + \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{\sin(2n-1)\theta}{2n-1} \right) \quad (2.6.11)$$

Since the series LC resonator passes only the fundamental switching frequency (n=1) the output current is sinusoidal,

$$i_o(\theta) = I \sin \theta = \frac{2V_{cc}}{\pi R} \sin \theta \quad (2.6.12)$$

and the output voltage is,

$$v_o(\theta) = R i_o(\theta) = \frac{2V_{cc}}{\pi} \sin \theta \quad (2.6.13)$$

From Fig. 2.16c,d The currents in Q1 and Q2 are half sinusoids corresponding to when each device is conducting. The peak current amplitude I is given by,

$$I = \frac{2V_{cc}}{\pi R} \quad (2.6.14)$$

The output power dissipated in the load resistor R is given by,

$$P_o = \frac{I^2 R}{2} = \frac{2V_{cc}^2}{\pi^2 R} \quad (2.6.15)$$

The DC input current can be calculated from the average current drawn from the supply,

$$I_{dc} = \overline{i_1(\theta)} = \frac{1}{2\pi} \int_0^{2\pi} i_1(\theta) d\theta = \frac{I}{\pi} = \frac{2V_{cc}}{\pi^2 R} \quad (2.6.16)$$

The DC input power is calculated from,

$$P_{dc} = V_{dc} I_{dc} = \frac{2V_{cc}^2}{\pi^2 R} = P_o \quad (2.6.17)$$

Figure 2.16: Voltage and current waveforms in an ideal Class D switching mode amplifier a) voltage v_2 at the input to the load network, b) resistor voltage v_o , c) Q_1 drain current i_1 , d) Q_2 drain current i_2 , e) resistor current i_o .

Figure 2.17: Switching amplifier with various load networks.

and the collector efficiency is a 100% since,

$$\eta_c = \frac{P_o}{P_{dc}} = 1 \quad (2.6.18)$$

In the efficiency derivation a 50% duty cycle was assumed but with PWM or SDM the duty cycle will naturally vary. In this case it is of interest to extend the efficiency analysis for variable duty cycles and load networks. The voltage waveform and load networks are shown in Fig. 2.17 in which the same ideal assumptions as those made in analyzing Fig. 2.15 apply here as well.

The fourier series for the periodic pulse waveform is given by,

$$V_n(\theta) = \frac{\phi}{\pi} + \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{(-1)^n}{n} \sin n\theta \cos n\theta \quad (2.6.19)$$

where $\theta = \omega t$. To calculate the load voltage the transfer functions are required. The transfer functions for the zero order (all pass), second order bandpass and second order low pass networks are,

$$H_0(\omega) = 1 \quad (2.6.20)$$

$$H_{bp}(\omega) = \frac{R}{R + j(\omega L - 1/\omega C)} \quad (2.6.21)$$

$$H_{lp}(\omega) = \frac{1}{1 - \omega^2 LC + j\omega L/R} \quad (2.6.22)$$

The load networks are passive and linear therefore superposition can be used to calculate the output voltage. For the fundamental ($n=1$) and harmonic components ($n>1$) output voltage across the load resistor R is given by,

$$V_R(n) = HV_n \quad (2.6.23)$$

from which the output power can be calculated

$$P_R(n) = \frac{|V_R(n)|^2}{2R}. \quad (2.6.24)$$

The input power can be calculated from the voltage and current waveforms,

$$P_{in} = \sum_{n=1}^{\infty} \frac{V_n I_n}{2} \cos \varphi = \sum_{n=1}^{\infty} \frac{V_n^2}{2Z_{in}} \cos \varphi \quad (2.6.25)$$

where φ is the input voltage and current phase difference and Z_{in} is the network input impedance. The efficiency can then be calculated by taking the ratio of the fundamental output power to the total input power,

$$\eta = \frac{P_R(1)}{P_{in}}. \quad (2.6.26)$$

As an quantitative example assume a switching frequency of 1 MHz, $R=16 \Omega$, $L=1 \text{ mH}$, and $C=25.3 \text{ nF}$ for the circuit in Fig. 2.17. Using these component values the efficiency is calculated according to (2.6.26) and plotted in Fig. 2.18. Based on the results the following observations are made:

- Even with ideal switching the zero order network does not result in 100% efficiency. This is due to energy wasted in the form of harmonics. The peak efficiency for the zero order model of 81% occurs at $\phi = 90^\circ$.

Figure 2.18: Switching mode amplifier efficiency calculation for various load networks. Resonant frequency 1 MHz, $R=16\ \Omega$, $L=1\ \text{mH}$ and $C=25.3\ \text{nF}$.

- For the bandpass network the efficiency is improved relative to the zero order but has not reached 100%. The bandpass 20 dB/dec roll off reduces the harmonic content but does not entirely eliminate it. For a series RLC circuit $Q = 1/R\sqrt{LC} = 0.39$ and is limited by the minimum headphone impedance of $16\ \Omega$. Since this is a bandpass resonant circuit 1 MHz it does provide a baseband output for the headphone.
- The second order low pass network attains virtually 100% efficiency across the full range of ϕ since harmonics are significantly filtered. The second order low pass filter has a 40 dB/dec roll off above the cutoff frequency. This configuration is applicable to audio applications.

In conclusion, assuming ideal switching devices and load network components is insufficient to yield 100% efficiency. Due consideration must be given to select the appropriate load network towards eliminating harmonics.

2.7 Key Points

- A digital audio system consists of digital audio source, modulator, DAC PA and speakers.
- Common modulation schemes are PWM and Sigma-Delta.
- Sigma-Delta modulators operate on the basis of oversampling and noise shaping.

- The analog version of PWM is referred to as natural sampling or NWPM. It does not distort the input signal.
- A discrete time PWM process with uniform sampling UPWM distorts the input signal.
- The two classes of PA's are linear and switching mode.
- Linear amplifiers achieve maximum efficiency at full scale output. The efficiency is reduced below full scale.
- Ideal switching mode amplifiers can achieve 100% efficiency at or below full scale output. This assume that the devices behave as ideal switches and an appropriate low pass filter network is present to remove harmonics.
- The collector efficiency is defined as $\eta_c = P_o/P_{dc}$ where P_o is the output power delivered to the load and $P_{dc} = V_{dc}I_{dc}$ is the power from the supply.

Chapter 3

Audio Amplifier Technology Review

This chapter begins by providing a table of system specifications for low power stereo headphone applications. This is followed by a discussion on typical sources of amplifier distortion and various correction techniques. A literature review of switching mode amplifier designs with various modulation and linearization techniques are briefly explained.

The majority of the papers are targeted towards full 20kHz bandwidth stereo applications and a few towards hearing aids with reduced bandwidth requirements. Many switching mode PA designs assume analog inputs and therefore require a DAC to interface with the digital audio source. For battery operated devices the goal is to merge the DAC and PA in a single chip scalable solution for rapid deployment in new fabrication processes.

3.1 System Specifications

The target specifications for a low power portable digital audio system are summarized in Table 3.1. The nominal supply voltage is based on a 130 nm CMOS process and will change depending on the chosen CMOS technology. At the nominal audio output power of 0.1 mW the system power consumption should be 10 mW or less for two channel operation. The total power consumption was selected to be competitive with commercial parts (low-voltage and low-power stereo audio digital-to-analog converter with headphone amplifier TI PCM1770).

The headphone sensitivity and output power are chosen to produce an output level of 100 dB. For a 5 mW output and a 95 dB/mW sensitive headphone the audio output will be 102 and 105 dB for a 32 Ω and 16 Ω headphones respectively. The output power should vary less than 1 dB over the audio band.

Table 3.1: Low power digital audio system specifications.

Parameter	Conditions	Values
Supply Voltage	Max	1.2 V
Nominal output power	16 or 32 Ω	0.1 mW
Power consumption	Nominal output power, stereo	10 mW
Max output power	16 Ω	10 mW
Headphone sensitivity	min	95 dB/mW
Load Impedance	min / max	16 / 32 Ω
Frequency response	20 Hz to 20 kHz	$< \pm 0.5$ dB
Total Harmonic Distortion	1 kHz	-70 dBc
SNR	A-weighted @ 0 dBm	≥ 90 dB
Power supply rejection	≤ 20 kHz	≥ 40 dB

The Total Harmonic Distortion (THD) is a figure of merit calculated by taking the ratio of the harmonic distortion relative to the fundamental. This can be expressed as a percentage,

$$\text{THD} = \frac{1}{V_1} \sqrt{\sum_{i=2}^{\infty} V_i^2} \times 100\%. \quad (3.1.1)$$

For good quality audio performance a THD on the order of 0.01 to 0.1% (-80 to -20dB) is required. For this application the target is 0.03% or -70dB. To account for noise and distortion the THD+N is often specified and can be calculated as follows

$$\text{THD+N} = 10 \log \left(\frac{\sum_{i=2}^{\infty} V_i^2 + N_o}{V_1^2} \right) \quad (3.1.2)$$

where N_o is the noise power integrated over the bandwidth of interest.

The frequency response of human hearing is inherently non-linear across the audio band. Various weighting filters, using the nomenclature A, B, C and D, have been developed to model this phenomena. Fig. 3.1 is a plot of the A-weighting filter model of human hearing sensitivity. This filter is the most common model applied in stereo applications. Tones in the 1 - 6 kHz range are accentuated and rapidly desensitized outside of this bandwidth. Signal to Noise Ratio (SNR) measurements are often specified with the amplifier output filtered using A-weighting.

The Power Supply Rejection Ratio (PSRR) is an important parameter in order to maintain quality audio performance. The systems ability to reject noise superimposed on the DC supply

Figure 3.1: A-Weighted filter response commonly used in audio measurements.

is determined by external power supply filtering, closed loop system response and deployment of differential circuits on-chip. The supply noise is usually a small percentage of the DC value so a 40dB target is a conservative specification to not not degrade the SNR. If good on-chip PSRR is obtained this can reduce the complexity and cost of the external power supply filter. In certain instances, such as in GSM handsets, a PSRR on the order of 65-80dB is required for a direct battery connection. Otherwise, a linear regulator would be required to isolate the audio system from the battery noise. This is obviously undesirable as the regulator will increase design complexity and increase power consumption.

3.2 Sources of Distortion

Distortion arises from amplitude and/or timing errors in the modulated pulse density waveform. Such errors can occur in the switching stage of Class D amplifiers resulting in harmonic distortion. Many designs incorporate feedback which serves to lower the output impedance, enhance noise immunity and most importantly, to linearize the PA. While feedback has many benefits, the tradeoff is increased system complexity and potential instability.

Audio systems can have either analog or digital input. With analog input, the feedback can be a passive or active network to realize the required frequency domain transfer function. If the

system is of the digital input type then the feedback signal must be digitized with an ADC. The resolution, speed and power consumption of the ADC are challenging and limiting factors.

There are several sources of distortion arising from the switching action of the PA. The sources can be broadly categorized into pulse timing and amplitude errors [25]. The timing errors arise from:

- Finite switch-on and switch-off delays.
- Blanking or deadtime delay's to ensure that simultaneous conduction of the nfet and pfet devices does not occur and thereby momentarily short the supply to ground [26], [27].
- Finite rise and fall times of the output when changing states.
- Reference clock jitter.

Sources of amplitude errors:

- Finite and nonlinear R_{ds} which can cause amplitude modulation.
- Substrate coupled noise.
- Power supply noise.
- Power supply droop.

3.3 Linearization Techniques

While efficiency concerns have been discussed in detail we now turn our attention to compensation or linearization techniques. A high degree of linearity is essential for high quality audio where harmonic distortion will degrade the THD performance. In wireless applications linearity requirements are stringent to avoid intermodulation products can interfere with adjacent channels. Thus, in applications like these, distortion will degrade system performance and must be mitigated.

Linearization techniques can either be applied in an open or closed loop manner. The feasibility of the selected approach will depend on the system bandwidth requirements and frequency of operation. Common techniques include negative feedback, indirect feedback, pre-distortion, and feed forward.

Figure 3.2: Closed loop control system.

3.3.1 Negative Feedback

Negative feedback is a classic technique which has been in use for decades. The concept is to feedback a sample of the output and subtract it from the input to generate an error signal. The closed loop response is to minimize this error, ideally setting it to zero. A closed loop control system with feedback is shown in Fig. 3.2. This could represent an op-amp with open loop gain $G(s)$ and negative feedback $H(s)$ for example.

In the open loop case $H(s)=0$ and output of the open loop system is

$$Y(s) = G(s)X(s) \quad (3.3.1)$$

In the closed loop $H(s) \neq 0$ resulting in an error signal $E(s)$. The closed transfer functions are,

$$Y(s) = \frac{1}{1 + GH(s)} X(s) \quad (3.3.2)$$

and for the error function,

$$E(s) = \frac{G(s)}{1 + GH(s)} X(s). \quad (3.3.3)$$

Therefore, if $|1 + GH(s)| > 1$ over the bandwidth of interest the error will be reduced accordingly.

The process represented by the transfer function $G(s)$ is subject to disturbances from the external environment, process mismatches, temperature, etc. In an amplifier it could be subject to external power supply noise, substrate noise or have a non-linear transfer function that results in distortion. From (3.3.1) it is clear in an open loop system that all disturbances or noise sources

directly affect the output, however a closed loop senses the changes and reduces the error by a factor determined by (3.3.3).

The system sensitivity is defined as the percentage change in system transfer function to the percentage change of the process transfer function [28]. The system transfer function is defined as,

$$T(s) = \frac{Y(s)}{X(s)} \quad (3.3.4)$$

where the sensitivity is defined as,

$$S = \frac{\Delta T(s)/T(s)}{\Delta G(s)/G(s)} \quad (3.3.5)$$

which in the limiting case can be expressed as a derivative,

$$S = \frac{\partial T(s)/T(s)}{\partial G(s)/G(s)} \quad (3.3.6)$$

Applying (3.3.6) to the open loop transfer function gives,

$$S_G^T = \frac{\partial T}{\partial G} \frac{G}{T} = 1 \frac{G}{G} = 1 \quad (3.3.7)$$

and any error introduced in $G(s)$ will appear at the output. For the closed loop sensitivity,

$$S_G^T = \frac{\partial T}{\partial G} \frac{G}{T} = \frac{1}{(1 + GH)^2} \frac{G}{G/(1 + GH)} = \frac{1}{1 + GH} \quad (3.3.8)$$

and assuming $|1 + GH| > 1$ the system error sensitivity is therefore reduced. Likewise, consider the system feedback sensitivity,

$$S_H^T = \frac{\partial T}{\partial H} \frac{H}{T} = \frac{-GH}{1 + GH} \quad (3.3.9)$$

and assuming $|GH| \gg 1$, then $S_H^T \rightarrow 1$. Any error in $H(s)$ will directly impact the output response. Thus, care must be taken in designing the feedback network so as not to degrade system performance.

While closed loop PA systems enhance linearity and reject noise there is also the possibility of instability. Closed loop operation usually requires the addition of a compensation or loop filter. From (3.3.2) the loop will be unstable when

$$|GH| = 1 \text{ and } \angle GH = -180^\circ. \quad (3.3.10)$$

As a result the condition for stability becomes

$$|GH| < 1 \text{ at } \angle GH = -180^\circ. \quad (3.3.11)$$

Two common stability parameters are Gain Margin (GM) and Phase Margin (PM). The phase margin (PM) is the amount by which the phase of $GH(s)$ is greater than -180° at unity gain $|GH| = 1$. The gain margin (GM) is the factor by which the gain is less than unity when $\angle GH = -180^\circ$.

In the analysis thus far, the feedback has been assumed to occur instantaneously without delay. In reality, loop delay is inevitable and, in some cases, significantly degrade the PM. The phase shift (rads) caused by a loop delay τ seconds is,

$$\delta\theta = -\omega\tau \quad (3.3.12)$$

where ω is the frequency of interest. At this point it is worth highlighting the significance of (3.3.12) pertaining to analog and mixed signal control systems.

In purely analog control circuits, transistors typically have delays on the order of picoseconds. Such delays are not significant even at RF frequencies and it is assumed that $\tau \rightarrow 0$.

In mixed signal systems there is invariably a conversion process from the analog to digital domain. This is accomplished by an ADC which can be modelled as a sample and hold circuit. Consider the continuous time waveform $u_i(t)$ sampled every T seconds as shown in Fig. 3.3. The result is, that the average $\overline{u_o(t)}$, lags $u_i(t)$ by $T/2$, or in other words $\tau = T/2$. While this can be alleviated by reducing T , an increase in power consumption, particularly in the ADC will arise. The delay associated with the sample and hold process is one of the most important factors in digital control systems [29].

In summary, feedback is an effective and widely used method to linearize audio amplifiers. The feedback desensitizes the amplifier to external noise sources and environmental conditions. The cost to achieve such benefits are,

- Increased complexity and extra circuitry associated with the feedback network.

Figure 3.3: Sample and hold delay.

- Loss of gain relative to open loop.
- With feedback there are stability concerns while open loop systems are typically stable.

3.3.2 Alternative Linearization Techniques

Alternatives to direct feedback include indirect feedback, pre-distortion and feed-forward techniques. These methods are often chosen in applications where the stability and bandwidth limitations of direct feedback are problematic, typically at RF and microwave frequencies. These are often sophisticated high power applications such as cellular base station transmitters as opposed to the low power IC applications considered here.

Two indirect feedback methods are polar and Cartesian correction where the RF output is down converted and compared with the baseband input. In polar correction both amplitude and phase are detected and corrected. Cartesian correction is an extension of polar correction applied to quadrature I and Q systems common in many communication systems.

Pre-distortion is an open loop compensation technique. While compensation is not as precise as closed loop systems it does have advantages in that stability and bandwidth limitations are eliminated. In pre-distortion, the known amplitude and phase non-linearities are applied to the input signal to offset the PA non-linear characteristics. While this technique can be effective it is difficult to compensate for a wide variety of parameters such as temperature and process variations.

The final technique is feed-forward compensation which has the accuracy of a feedback system

without the associated bandwidth and stability concerns, however such high performance comes at a cost. The feed-forward loop requires complex gain and phase tracking circuitry as well as an additional power amplifier which reduces the overall efficiency [30].

3.4 Switching Mode Audio Amplifiers

A typical pulse modulation system for audio applications is shown in Fig. 3.4. The audio source is a standard 16 bits/ch PCM at 44.1 kHz. The pulse modulator converts the bitstream into a series of binary pulses. The two predominate modulation schemes are PWM and $\Sigma\Delta$. These pulse modulators enable implementation of a Switching Mode Power Amplifier (SMPA) with theoretical 100% efficiency. The output signal is demodulated by way of a low pass filter preceding the speaker. The feedback control provides error correction to reduce distortion and noise. In some instances suitable performance is obtained without feedback, such open loop designs are susceptible to significant performance degradation. The trade-off with closed loop systems is better performance at the expense of extra circuitry and potential instability, however if properly designed significant performance enhancement can be obtained.

Figure 3.4: Pulse modulation system with feedback.

Class-D amplifiers with a theoretical 100% efficiency have received much attention in the literature. These amplifiers in combination with a $\Sigma\Delta$ or PWM modulator provide a direct digital to analog audio system. Though conceptually simple to design many challenges arise. Ideally, one would like to achieve low distortion, high dynamic range, high SNR, high efficiency and stability while driving low impedance loads. This often requires feedback to linearize the PA. A literature review of various Class D designs is presented in the following sections.

3.4.1 Switching Mode Power Amplifier Categories

Table 3.2 groups published SMPA architectures into five categories depending on the input signal (analog or digital) and feedback (analog, digital or open loop). These designs range from mono to multi-channel with power ratings from mW to over 100 W. For closed loop systems, the feedback can either be analog or digital. Block diagrams of the five categories are provided in Fig. 3.5. Though overly simplified they serve to highlight the different approaches of each category. The modulators are PWM, $\Sigma\Delta$ or a hybrid combination of both. In addition, there are often DSP blocks for volume control, rate conversion, filtering and other functionality. For complete design details, the papers listed in Table 3.2 and references therein should be consulted. Furthermore, a technical summary of many common Class D topologies can be found in [31], [32]. Of most interested are digital input categories III-V for fully integrated single chip solutions.

Table 3.2: Overview of current switching mode audio power amplifier techniques.

Category	Input	Feedback	References
I	Analog	-	[33, 34]
II	Analog	Analog	[35–45]
III	Digital	-	[46–52]
IV	Digital	Analog	[53–57], [31]
V	Digital	Digital	[6], This work ([7, 9])

Category I

The category I amplifiers have analog input and no feedback. An off chip DSP and DAC are required for a complete digital audio system. With an open loop systems there is no correction for non-linearities, power supply noise, temperature variation nor process variation. A degree of common mode noise rejection can be obtained with differential structures and a Bridge Tied Load (BTL) [31,51]. The environment in which these designs are used must therefore be carefully considered.

In the Phase Shifted Carrier PWM (PSCPWM) [33] technique a multi-level PWM signal is synthesized from a single supply voltage by controlled phase shifting of the carrier to N paralleled switching legs. The advantages of this scheme are an effective sampling frequency increase by a factor of N and reduced voltage and current stress on the transistors. The design complexity and

Figure 3.5: Block diagrams of different Class D categories.

cost will increase due to more switching legs, increased filtering components and phase shifting circuitry sensitivity.

An fully integrated $0.25\ \mu\text{m}$ CMOS design [34] implements a 3rd order single bit Sigma-Delta modulator. To reduce conduction losses and achieve high efficiency, the switching stage must have a much lower R_{ds} than the load impedance. To accomplish this the switching transistors are very large, $W_p = 34,000\ \mu\text{m}$. The switching stage is driven by a series of six tapered inverters. An efficiency of 91% at 1 W power into a $4\ \Omega$ load is achieved. While the efficiency is very high at full output power the efficiency below full scale is not specified. Its possible the efficiency below full scale is degraded due to the switching losses associated with the large inverter parasitics. The THD+N ranges from 0.03 to 1.5% depending on the output power.

Category II

A number of SMPAs in the literature are category II analog PWM [36–38,40,58] designs. Each of these designs implements the feedback quite differently. For example, in [36] there are dual current and voltage sensing feedback loops while another approach [37] has three nested voltage feedback loops designed using classical gain and phase margin compensation techniques. Theoretically, the linearity measured in terms of the THD response should be reduced by a factor equal to the loop gain, however in [37] the improvement from two loops 0.045% to three loops 0.040% is marginal. In addition, the THD results expected from nesting the loops are significantly worse than theoretically calculated. Thus the improvements from nested loops are of limited value considering the extra design effort, stability, increased component count and reliability issues encountered.

A low-power hearing aid design [38] has poor THD performance due to a low power exponentially rising and falling PWM carrier. Compared to an ideal triangular waveform the exponential waveform introduces significant distortion in the PWM process. Another issue arises from carrier feed-through in the forward path coupling into the feedback path. To reduce this effect, attenuation is added in the feedback path but this is counterproductive since the loop gain is reduced. With a difference amplifier and summer integrator in the feedback, the THD is on average improved by a factor of 2.5 or 8 dB.

A variant of analog feedback systems discussed thus far is shown in Fig. 3.6. This system is referred to as Pulse Edge Detection and Correction (PEDEC) [41]. The error processing unit directly compares the input PWM waveform v_r (ignore the delay block for now) to the output

Figure 3.6: Pulse edge detection and correction system.

PWM waveform following the power stage v_f . These two PWM waveforms will be different due to the non-idealities and external noise sources. Based on the difference of the two waveforms a correction signal v_e is generated. It is used to re-time the incoming PWM waveform. For example, a droop in the power supply would be compensated by increasing the incoming pulse width such that the average voltage is correct.

With proper loop filter design the frequency response and linearity can be improved. However, one must consider the effect of the propagation delay from the input v_r to the output v_o which will cause an offset between v_r and v_f thereby introducing errors at v_e . To compensate for this offset a delay block is added to the v_r . The accuracy of this delay block then becomes a critical parameter in obtaining optimal performance. Without proper delay offset the output noise floor increases significantly. How well this delay can be predicted and controlled is a limiting design factor.

A similar technique [59] which precedes [41] uses a tapered delay line with 30 taps and 2.5ns resolution to re-time the edges. Simulations show significant reduction in distortion but as in [41], an increase in the noise floor degrades SNR performance.

Sigma-Delta SMPA's such as [34, 42, 43] are alternatives to PWM. Sigma-Delta has the benefit of high linearity however, the switching frequency is higher than PWM. A $2 \times 40\text{W}$ Class D chip fabricated in $0.6\ \mu\text{m}$ BCDMOS with analog feedback provides 67 dB power supply noise rejection, 0.001% THD, 104 dB dynamic range and 88% power efficiency [43]. The design includes a 7th order single bit Sigma-Delta architecture with dynamic hysteresis and $128\times$ oversampling ($\sim 6\text{MHz}$). The purpose of the hysteresis in the feedback is to reduce the average switching frequency and thereby reduce switching losses. This requires extra circuitry and poses stability

issues but it effectively reduces the switching frequency by roughly one third. Another feature of the design is to use less aggressive noise shaping to allow for a broader range of stable inputs. In a sense, trading off audio band SNR for an increase in modulation index from 50% to 90%.

Another 7th order $128\times$ oversampling single bit Sigma-Delta design in a $0.35\ \mu\text{m}$ CMOS process requires an off-chip inverter to act as the power stage [42]. Similar to [43] the loop filter poles and zeros are modified to provide for a higher modulation index of 89%. This design achieves 111 dB SNR, 0.0015% THD+N and consumes 60 mA from a 5V supply. The load impedance is not specified so efficiency cannot be calculated.

Integrating high fidelity audio in mobile handsets presents unique challenges. For example, when a Global System for Mobile communications (GSM) handset transmits signals, the RF PA can sink significant current from the battery. This action is repeated every 4.6 ms (217 Hz) during transmission and causes supply fluctuations. Low Dropout (LDO) regulators are generally used to isolate the audio amplifier from this power supply noise but this will reduce the overall efficiency. A direct battery hookup Class-D amplifier bypasses the LDO and is directly connected to the battery. In this case, the Power Supply Rejection Ratio (PSRR) is an important Class D specification.

A low-distortion third-order Class-D amplifier that is fully integrated into a $0.18\ \mu\text{m}$ CMOS process was designed for direct battery hookup in a mobile application [44]. The amplifier with third-order loop filter has a 217 Hz PSRR of 88 dB. A power efficiency of 85.5% when delivering an output power of 750 mW to a $8\ \Omega$ load from a 3.7 V supply THD+N of 0.018% is achieved. The THD+N is 0.018%

In [39] the architecture, design, and implementation of two analog class D audio power amplifiers using $0.5\ \mu\text{m}$ CMOS standard technology are introduced. The amplifiers are designed to consume significantly less power than former implementations. Both designs operate with a 2.7 V single voltage supply and deliver a maximum output power of 250 mW into an $8\ \Omega$ load. The two Class-D amplifiers are based on a hysteretic sliding mode controller, which avoids the task of generating the highly linear triangle carrier signal used in conventional architectures. Experimental results of the yield an efficiencies on the order of 90% and THD+N of 0.03%. Both class D amplifiers achieve a PSRR of 75 dB at 217 Hz and 90 dB SNR. A similar approach is taken in [45].

Category III

Since virtually all audio is encoded and distributed digitally it is therefore desirable to have a digital input PA. This approach is attractive since the DAC, modulator and amplifier can be optimized towards a fully integrated low power solution. As in the analog domain the modulation scheme can be PWM, Sigma-Delta or a combination of both. Category III are open loop digital input amplifiers. Without feedback, the system performance is susceptible to power supply noise and switching distortion. There are several category III Class D PA designs in the literature. A few examples will be presented in this section.

In [50] an architecture based on a 4th-order digital PWM modulator with feedback is presented. The feedback is local to the modulator and does not encompass the PA, hence it is category III. In this manner, distortion arising from the uniform sampling of the baseband signal is reduced by the modulator loop gain. The loop processes the PWM signals at a clock frequency of 24 MHz and provides pulse edge timing resolution of 42ns. The achieves 120 dB dynamic range over a 20 kHz bandwidth, provides 88% power efficiency at 400 mW while driving an 8 Ω load. Since the PA is open loop the PSRR is very poor. At 125 mW output power the PSRR is ~ 6 dB and would therefore require a regulator to operate in a GSM handset. A recent open loop design for low power applications < 1 W includes efficiency results with and without a regulator to isolate the Class D PA from battery noise [51]. The efficiency is reduced from 81% to 72% which includes the digital power consumption. This design is an open loop filterless Class D PA with BTL configuration.

Multi channel integrated designs for 5.1-channel applications have been developed. In [52], a single-chip, digital-input class-D audio amplifier with a low-voltage digital circuit and high-voltage switching power stage for moderate-performance speaker systems is presented. To avoid supply bounce, a multi-phase PWM switching technique prevents the multi-channel output stages from simultaneously switching. Fabricated with 0.35/ $3\mu\text{m}$ 3.3/18 V 1P3M CMOS technology, the 5.1-channel amplifier achieves 13 W RMS power per channel and 35 W RMS for the subwoofer channel. The distortion is less than 0.7% and power efficiency of 88%.

A low power stereo headphone design with 12.5 mW max output power in 65 nm CMOS is of particular interest [49]. This design has a 103 dB SNR (A-weighted, zero-input) and 80% efficiency at 12.5 mW. The nominal power draw from the 1.2 and 2.5 V supplies is only 1.3 mW per channel. Since the PA is open loop it is susceptible to power supply noise and does not

correct for errors in the switching stage. Furthermore, since the load is single ended rather than differential (bridge tied load) there is virtually no power supply noise rejection.

A 350 mW output power PA yields an efficiency in the 66-79% range depending on the load impedance [46]. The THD is on the order of 0.07% and maximum SNR is 74dB. The modulator is a single bit 3rd order $\Sigma\Delta$ with $128\times$ oversampling. Another $\Sigma\Delta$ open loop Class D amplifier with a multi-level MASH 2-2 modulator has been simulated in [47]. The multi-level serves to reduce the switching frequency but requires multiple power supplies and switches. For IC applications the multiple power supplies are generally not available and multiple switches leads to increased losses.

An open loop PWM based Class D amplifier has a power output 100 W [48]. Sophisticated DSP algorithms are required to correct for the UPWM distortion and the digital PWM operates at a clock frequency of 196.6 MHz. To ensure the dynamic range is greater than 100dB a timing precision of better than 13ps is required.

Category IV

Category IV amplifiers have digital input and local analog feedback for the switching stage. These topologies require an analog loop filter which consumes extra power and increases the overall noise level. With a properly designed loop filter the need for a regulated power supply can be eliminated and the switching stage can be directly connected to the battery terminals.

Category IV amplifiers usually use a second order analog loop filter consisting of two first order integrators. Scaling to a new process requires redesign and verification.

A PWM Class D audio amplifier accommodates digital input with an integrated DAC configured to realize a direct connection between the DAC and the analog feedback loop [54]. Targeted towards higher power applications in the 10-100 W range the power switching stage is located off-chip. The published performance is; 0.0018% THD+N at 10 W output power, 0.004% THD+N with 100 W output power and 113 dB dynamic range. The paper does not indicate which fabrication process was used nor any efficiency data. The unique feature here is the dual role of the DAC reconstruction filter. The third order reconstruction filter converts the segmented current DAC output to voltage and also acts as a loop filter for the feedback from the power stage to improve linearity. While this reduces circuitry, it also adds complications in that the optimum DAC reconstruction filter may not provide the optimum stability and loop bandwidth solution

for the amplifier. That is, it must improve linearity and provide good phase margin.

A fully integrated low-power $0.5\ \mu\text{m}$ CMOS DAC and Class D PA with 70% efficiency is presented in [53]. Here a single bit 5th order modulator is the PA driver. The PA has local feedback for improved linearity. Since the modulator has single bit output it is amenable to directly drive the PA, in this sense the output is treated as an analog signal. The PA analog loop filter is second order integrator.

In [56] a digital input PWM amplifier with analog feedback implements a 7b flash converter and third order integrating loop filter to digitally linearize the PA. This architecture is interesting in that it has a low switching frequency of 375kHz and a fairly low 7b resolution ADC which runs at twice the switching frequency. A discrete circuit implementation achieved a dynamic range of 100 dB and THD of 85 dB. Issues to be resolved towards an IC implementation of this architectures are the RC time constant $\pm 5\%$ tolerances for the third order error integrator, power requirements for the flash ADC converter, pulse width jitter sensitivity and loop stability due to correction delays. There is also an unexplained increase in second order harmonic distortion that needs to be addressed.

In [55] a class-D audio amplifier for mobile applications is fabricated in a $0.14\mu\text{m}$ CMOS. The amplifier has a simple PDM based digital interface for audio and control. The audio system consists of a Parser, Digital PWM controller, 1-bit DAC, analog feedback loop and the Class-D power stage. With a $4\ \Omega$ load and output power of 3.4 W the PA efficiency is 90%. Two other notable category III designs are [31] and [57].

Category V

Category V topologies deploy global feedback which encompasses the modulator, loop filter and Class D PA. It corrects for power stage errors due to power supply noise, clock jitter and switching artifacts. In addition, modulator errors such as UPWM distortion will be corrected. This allows the designer the ability to design a simple, low power modulator without sophisticated DSP correction algorithms. The degree of error correction is determined by the loop filter design and stability requirements.

A highly digital based architecture has two main advantages. First, the quiescent bias current associated with analog circuits is eliminated. Secondly, the design is readily scaled to new fabrication processes. There are also other advantages such as yield. The performance of analog

circuits is susceptible to process variation which can lower overall yield.

Category V is highly scalable as both the modulator and loop filter are digital. The ADC design in category V would be more complex than the analog loop filter in category IV, however ADCs are commonly one of the first building blocks developed in new processes. This allows for the opportunity to purchase the design from a third party and maintain a time to market advantage relative to category IV.

While global feedback offers several desirable features and advantages, it receives modest attention in the literature. The main disadvantage of global feedback is the requirement of a high resolution ADC which impacts overall system efficiency. Furthermore, the ADC architecture has significant impact on system performance, loop filter design and stability. Therefore, selecting either an oversampling or Nyquist ADC must be considered in the initial design phase. To the best of the authors knowledge the only global feedback related publications are [6] and this work [7,9].

Home stereo or multichannel audio applications typically specify a maximum of 200 W per channel. Typical listening volumes be much lower than the maximum. A Class-D amplifier with global feedback for home audio is presented in [6].

In this design the loop filter becomes a complex task to achieve acceptable performance. The filter factors which have to be traded off include maximizing gain, $\Sigma\Delta$ ADC quantization noise suppression and phase margin. The phase margin was 32° with a master clock operating at 19.66 MHz. The ADC was a high performance 24b $\Sigma\Delta$ which consuming a maximum power of 1 W [60]. The prototype achieved a THD+N of 0.001% with 15 W output to a $8\ \Omega$ load. No efficiency values are provided.

For headphone applications the target specifications are given in Table 3.1. For a global feedback system with power output in the mW range, the ADC must be low power. The ADC used in [6] is not feasible due to power consumption, frequency of operation and quantization noise associated with the $\Sigma\Delta$ process [7,9]. The approach taken here is to slow the master clock frequency to 2.822 MHz and use a low power SAR ADC.

3.4.2 Commercial Class-D Amplifiers

There are quite a few commercially available Class D amplifiers for low power applications. Wolfson, Texas Instruments and Analog Devices all manufacture a variety Class D amplifiers for low power applications. Output power specifications range from 25 mW for headphones and 1-2

W for speakers. These designs are predominately analog input. Of interest here are the DAC and PA integrated solutions with digital input.

Wolfson Microelectronics for example has two stereo DACs integrated with a headphone and speaker amplifier. The headphone amplifier is a Class AB while the speaker driver is Class D. The WM8986 is targeted to portable audio devices and is a fully integrated stereo DAC with microphone preamps, headphone and speaker amplifier. The headphone driver provides. The headphone driver provides 20 mW of power 20 mW with a THD+N of -70 dB. The Class D speaker driver delivers 1 W with 87% efficiency. Analog Devices SSM2517 is a mono digital input Class D amplifier. Output power is 1.38 W into 8 Ω with 92% efficiency and 1% THD+N. Quiescent power consumption is 10.4 mW.

The Texas Instruments PCM1770 device is a CMOS, monolithic, integrated circuit which includes DAC stereo converters, headphone circuitry, and support circuitry. The data sheet does not specify the type of headphone amplifier but it appears to be Class AB. Maximum output power with a 16 Ω load is 13 mW per channel. There is no efficiency data provided however the quiescent power consumption is 6.5 mW.

3.5 Key Points

- The research is focused on low power headphone applications according to the specifications of Table 3.1.
- Distortion in pulse density modulation techniques is any perturbation in the waveform amplitude or timing.
- Open loop systems are susceptible to distortion. Closed loop systems are desensitized according to the loop gain.
- Techniques to linearize the PA include: negative feedback, indirect feedback, pre-distortion and feed forward.
- Switchmode power amplifiers require either $\Sigma\Delta$, PWM or a hybrid combination of these modulation techniques.
- The literature summary has been subdivided into five categories. They are sorted according to input type (analog or digital) and feedback (open loop, local feedback or global feedback).

Chapter 4

System Design

In this chapter a Class D amplifier topology with direct digital input for low power applications is presented. Global feedback and a digital loop filter serve to correct errors and linearize the PA. The main advantage being an inherent ability to scale the design to deep submicron processes with minimal redesign effort in the analog domain. The digital core of the system is a high resolution hybrid multi-bit $\Sigma\Delta$ -Pulse Width Modulation (PWM) modulator without the need for Dynamic Element Matching (DEM). Furthermore, DSP algorithms to correct for UPWM distortion are not required due to the global feedback.

A prototype based on a FPGA and commercial 16b analog to digital converter (ADC) validates the design principles. Prototype measurement results indicate greater than 30 dB of noise rejection at 1 kHz with a discrete time Proportional plus Integral (PI) digital loop filter.

Portable audio devices such as MP3 players, tablets, smart-phones, laptops and wireless headsets require good quality audio performance and optimum energy efficiency. A set of typical specifications were given previously in in Table 3.1.

First, the system architecture under investigation is explained followed by a discussion on each of main components. Simulation and measurement results based on a FPGA and commercial ADC are presented.

4.1 System Architecture

The proposed topology shown in Fig. 4.1 consists of interpolation filters, digital loop filter, $\Sigma\Delta$ modulator, PWM, Class D amplifier, low pass second order output filter, first order low pass

Figure 4.1: Block diagram of the Class D amplifier with digital compensation.

filter in the feedback and an ADC. The combined $\Sigma\Delta$ and PWM blocks are referred to as digital PWM (DPWM). A brief explanation of operation is now provided before more detailed analysis of each of the blocks.

The input to the loop $V_i[i]$ is the i^{th} sample of the interpolated and filtered digital audio source. The interpolation filter is required to oversample the digital audio source (16 bits at 44.1 kHz) while removing aliasing components. The input $V_i[i]$ is compared to $V_o[i]$ which is the digital output of the feedback ADC. The difference between $V_i[i]$ and $V_o[i]$ results in the error signal $e[i]$ which is processed by the loop filter. The discrete time loop filter $C(z)$, defines performance parameters such as noise immunity, load sensitivity and stability. Proper loop filter design is required to obtain the full benefits of feedback while maintaining stable operation.

The DPWM input $d[i]$ undergoes two processing stages. First, the signal is $\Sigma\Delta$ noise shaped and multi-bit modulated. For a 16b input corresponding to 2^{16} levels the resulting $\Sigma\Delta$ output is 9 discrete levels (3.2 bits). Secondly, the PWM converts the 9 levels into the corresponding duty cycles $d(t)$. The duty cycles range from 0, 12.5, 25, ...100%. The net result is a two stage DPWM that quantizes and noise shapes a 16bit input to an intermediate 3.2 bits then single bit output with high linearity and $> 100\text{dB}$ SNR. This two stage approach is taken for the following reasons:

- Directly converting the 16b audio to PWM is not practical due high clock frequency and jitter sensitivity. The 9 level PWM is used to convert the multi-bit output to a single bit for the Class D amplifier.
- Using multi-bit $\Sigma\Delta$ with $64\times$ oversampling provides an SNR $>100\text{dB}$ and high linearity. Multi-bit allows for a higher SNR at lower OSRs which in turn reduces PA switching losses.
- The number of PWM bits is a trade-off between modulation index and minimum duty cycle. More PWM bits increases the modulation index and linearly reduces the duty cycle thereby increasing jitter sensitivity. As the modulation index increases to 100% the output power

approaches full scale.

The DPWM single bit output is directly compatible with the Class D switching amplifier. Other DPWM examples include DC-DC converters [61] and an audio DAC [62] (uncompensated open loop and no PA). The PWM output drives the Class D amplifier followed by a low pass filter.

Since the discrete PWM process is not a true “natural” sampling process, harmonic distortion will arise. However, since the modulator lies within a closed loop system the distortion will be reduced according to the loop gain. This is advantageous in eliminating the need for DSP interpolation algorithms as required as in [56], [15].

The most challenging aspect of this architecture is the ADC. It requires 16b precision at a conversion rate of 2.822 MHz (64× oversampling) corresponding to the DPWM operating frequency. In addition, low power operation is critical in maintaining the overall system efficiency gained from the Class D amplifier.

An ADC can be either a Nyquist or $\Sigma\Delta$ type converter. Nyquist rate converters operate slightly above the Nyquist rate and typically rely on precision matched components. On the other hand, $\Sigma\Delta$ converters operate at much higher sample rates and in turn the matching precision is relaxed [63]. The quantization and noise shaping associated with the $\Sigma\Delta$ process leads to significant out of band noise peaking at $f_s/2$. This noise can saturate the DPWM modulator and cause loop instability. While this noise can be digitally filtered the filtering process introduces loop delay. which in turn leads to reduced phase margin. Hence, though $\Sigma\Delta$ converters have some advantages, they are not practical for this architecture.

In [6] a Class D amplifier with digital compensation incorporates a $\Sigma\Delta$ feedback ADC (Analog Devices AD7760 20Msps 24b ADC which dissipates 1W). In this case the ADC output is not decimated and filtered, the filtering is incorporated in the loop filter. Since the loop is operating at a sample rate of 19.66 MHz some loop delay associated with filtering can be tolerated. In addition, since ADC is operating at a very high OSR, the noise is shifted higher in frequency and is easier to filter. Even so, the author acknowledges that a commercial version of the prototype would require additional analog circuitry to contend with excessive quantization noise. While this approach is acceptable for high output power applications on the order of several watts and up its not a viable solution for low power applications.

Figure 4.2: Input and output spectrum of an ideal interpolation filter..

4.1.1 Interpolation Filters

The function of the Interpolation Filter (IF) shown is twofold. Firstly, to increase the sampling rate from f_N (44.1 kHz) to $OSR \cdot f_N$. This allows for noise shaping in the DPWM module. Secondly, to suppress the spectral replicas and minimize the out of band power. This improves the dynamic range of the control loop and relaxes the linearity requirements placed on the Class D amplifier and analog low pass filter. This is due to reduced intermodulation distortion products folding in band. The input and output spectrum of an ideal interpolation filter is shown in Fig. 4.2

Efficient Interpolation Filters (IF) are multi-stage structures. The IF upconverts the input sample rate from f_N to f_s in multiple stages. In theory, it is possible to construct a single stage filter that oversamples directly from f_N to f_s however this would lead to a large complex digital filter operating at f_s . This would be inefficient and could generate significant digital noise.

To obtain high efficiency the most complex filter with the highest tap count is implemented at the lowest operating frequency. As an example consider a three stage IF. The first stage must remove the first adjacent (between f_B to $3f_B$) and subsequent odd order aliases. Therefore, the first stage has the most stringent specifications and will be the most complex filter. With odd order aliases removed the requirements and complexity of the second stage is reduced since the remaining aliases are further apart and steep rolloff rejection is not required. The third and final stage operates at the highest frequency $f_s = OSR \times f_N$ and is usually a sample or zero order hold. This results in a sinc function response that adds further filtering. A three stage IF [64] provides $64\times$ oversampling, a passband ripple of $\pm 0.06\text{dB}$ and out of band attenuation of 43dB.

In the FPGA prototype to be presented no IF filters are used. The baseband audio signal is

directly oversampled at f_s . A complete three stage IF filter design will be presented in a following section.

4.1.2 DPWM

DPWM is the cascaded combination of the multi-bit $\Sigma\Delta$ and PWM highlighted in Fig. 4.1. The DPWM converts a 16b input to a single bit output, in essence an ideal 16b PWM which is not practical to implement directly. This two stage approach offers the following advantages,

- Multi-bit facilitates higher SNR and lower out of band noise at reduced clock frequencies.
- $\Sigma\Delta$ provides high linearity
- PWM acts as a parallel to serial converter compatible with Class D switching amplifier.

Sigma Delta Modulation

A brief introduction to the operation of a first order single bit $\Sigma\Delta$ modulator was given in Sec. 2.2.2. There are extensive variations $\Sigma\Delta$ modulators of different orders and either multi or single bit. The tradeoffs between single and multi-bit $\Sigma\Delta$ modulators are as follows:

- Multi-bit quantization error is reduced by 6dB per bit added to the quantizer resolution. Therefore, an equal improvement in SNR and reduced out of band noise is achieved. The reduced out of band noise relaxes the requirements on the demodulating low pass filter.
- Since there is no filtering prior to the Class D amplifier a single bit modulator with high out of band noise is more likely to cause folding of the noise spectrum in the region around $f_s/2$ into the signal band (DC to 20 kHz).
- Since multi-bit modulators generate less quantization noise they can achieve a given SNR specification at a lower OSR compared to single-bit modulators. As a result lower power operation may be achieved.
- Single bit is directly compatible with a Class D amplifier while multi-bit's require additional circuitry. For example, a PWM which performs the parallel to serial conversion.
- Multi-bit modulators tend to be more stable over a larger range of input values. This allows for a higher modulation index.
- Multi-bit is less sensitive to clock jitter due to lower clock frequency.
- Multi-bit element mismatches introduce an output error which will generate harmonic distortion as well as increased noise. One way to overcome this affect is to by spreading the energy of the harmonic spurs into pseudo-random noise using a technique called dynamic element matching [65]. Single-bit inherently does not have this problem.

Figure 4.3: $\Sigma\Delta$ SNR calculations for $L=1$ to 4 with $M=2$.

The $\Sigma\Delta$ theoretical performance is determined by the oversampling ratio (OSR), noise shaping loop filter order and number of output bits. The SNR can be calculated from [62],

$$\text{SNR} = (6L + 3) \log_2 \text{OSR} - (8L - 4) + 20 \log_{10}(M - 1) \quad (4.1.1)$$

where L is the loop order, OSR is the oversampling ratio and M output levels. Fig. 4.3 is a plot of (4.1.1) for $L=1$ to 4 and $M=2$ (single bit). For multilevel $M > 2$ and the SNR is increased according.

A popular topology which relaxes the stability requirements of higher order modulators is a cascaded structure in which each subsequent stage processes the quantization error from the preceding stage. This is commonly referred to as a MASH (**M**ulti-st**A**ge noise-**S**Haping) modulator.

Fig. 4.4 is the block diagram of a modified version of the standard MASH 1-2 modulator [62]. The 1-2 nomenclature implies a first order loop filter followed by a second order, hence an overall third order response. There are many other third order $\Sigma\Delta$ configurations however, the MASH 1-2 was selected to address challenges specifically related to this application. In particular,

- The signal transfer function can be made delay free so as not to degrade loop stability.
- All coefficients are unity or $1/2$ which simplifies hardware implementation.

Figure 4.4: Sigma-Delta MASH 1-2 block diagram.

- The multi-bit output yields a high modulation index.

The transfer function is derived from algebraic analysis of Fig. 4.4 as follows,

$$P_1 = (U - z^{-1}C_1) + z^{-1}P_1 \quad (4.1.2)$$

$$P_2 = P_1 + kFz^{-1} \quad (4.1.3)$$

$$C_1 = P_2 + E_1 \quad (4.1.4)$$

$$= P_1 + kFz^{-1} + E_1$$

$$= U + (1 - z^{-1})(E_1 + kFz^{-1})$$

$$I = P_1 - C_1 \quad (4.1.5)$$

$$= -E_1 - kFz^{-1}$$

Since the second stage of the MASH 1-2 has delay free integrators C_2 is given by,

$$C_2 = I + (1 - z^{-1})^2 \quad (4.1.6)$$

and the overall output $V(z)$ is,

$$\begin{aligned}
 V &= C_1 + (1 - z^{-1})C_2 \\
 &= U + (1 - z^{-1})(E_1 + kFz^{-1}) + (1 - z^{-1})[I + (1 - z^{-1})^2 E_2] \\
 &= U + (1 - z^{-1})^3 E_2
 \end{aligned} \tag{4.1.7}$$

from which we note the signal transfer function is unity and third order noise shaping has been achieved.

The feedback path with scaling factor $0 < k < 1$ is set so that the first integrator output of the second stage isn't overloaded [62]. A value of $k=1/2$ was selected to optimize the modulation index and efficient hardware implementation.

Modulation Index

Since the output power is limited by $P_o = V^2/R$ any reduction in output swing will reduce the available power and SNR accordingly. This is especially important in low voltage applications where voltage headroom is at a premium and the modulation index must be optimized.

In Fig. 4.4, $Q_1 = 1/3$ which results in seven possible quantization values of $C_1=(-1, -2/3, -1/3, 0, 1/3, 2/3, 1)$ likewise for $Q_2 = 1/6$, $C_2=(-1/6, 1/6)$. Overall the output will have a total of 9 possible levels from $-4/3$ to $+4/3$ in $1/3$ increments. Assuming an input range for U of ± 1 the effect modulation index is the ratio of first quantizer C_1 to the total quantizer summation $C_t = C_1 + C_2$ which in this case is $C_1/C_t = 1/(4/3)$ or 75%. This results in 2.5dB SNR degradation. Third order noise shaping can be achieved with three first order loop filters in a MASH 1-1-1 configuration however this significantly degrades the modulation index and in turn the SNR as $C_t = C_1 + C_2 + C_3$ will increase and thereby decrease C_1/C_t .

MASH 1-2 Simulations

The MASH 1-2 SNR and modulation index performance was verified in Matlab simulations. A time domain plot is provided in Fig. 4.5 of a 10 kHz tone. Note that the quantization fractions have been scaled to integer values. The top plot is output of first order modulator, C_1 . The middle plot is the differentiated values of C_2 . The bottom plot is the final output $V(z)$ with 9 integer values ranging from -4 to +4.

Figure 4.5: MASH 1-2 time domain plots for a 10 kHz input with a sample rate of 400ns (OSR=62.5): a) Output of the first order sigma-delta, b) Output of the second order sigma-delta, c) Overall third order noise shaped output obtained from the sum of plots a and b.

Figure 4.6: Nine level MASH 1-2 SNR plot. Matlab simulation with 1 kHz tone and $k=1/2$.

The theoretical SNR calculation is as follows:

$$\begin{aligned}
 \text{SNR} &= (6L + 3) \log_2 \text{OSR} - (8L - 4) + 20 \log_{10}(M - 1) \\
 &= (6 \cdot 3 + 3) \log_2 62.5 - (8 \cdot 3 - 4) + 20 \log_{10}(9 - 1) \\
 &= 123.3
 \end{aligned} \tag{4.1.8}$$

where $L=3$ is the loop order, $M=9$ the number of output levels and $\text{OSR}=62.5$ assuming a 20 kHz audio bandwidth. The OSR is 62.5 rather than 64 simply for simulation and FPGA implementation convenience ($62.5 \times 40k=2.5$ MHz).

The Matlab simulated and theoretical calculated SNR values are plotted in Fig. 4.6. The maximum input amplitude is 71.25% or -2.94dB full scale (dBfs). Larger amplitudes result in rapid SNR degradation. There is approximately 2dB offset between the two curves which is attributed to noise leakage in the windowing process. This phenomena is related to the windowing process resulting in folding of high frequency noise to baseband. This is mitigated by applying a Hanning window instead of a rectangular window [63].

Figure 4.7: PWM parallel to serial conversion process.

PWM

The PWM following the MASH 1-2 in Fig. 4.7 converts the multi-bit output to a single bit. The conversion is accomplished by incrementally varying the duty cycle from 0 to 100% in 12.5% increments according to the MASH 1-2 output. For example, with a clock frequency of 2.5 MHz the clock period is 400 ns. For a MASH 1-2 output of $V(z) = -1/3$ the PWM duty cycle would be 37.5% (high for 150 ns and low for 250 ns).

There are various implementations of digital PWM [66] each with various trade-offs in terms of complexity, power consumption, linearity and sensitivity to process and environmental conditions. A digital implementation of a PWM circuit was discussed in Chapter 2 Fig. 2.5. With low OSR's this circuit is not feasible due to high counter clock frequency and harmonic distortion, however due to the high OSR and reduced number of bits from the MASH 1-2 modulator the circuit is feasible in this application.

Multi-bit Selection Criteria

The MASH is inherently multi-bit due to the summation of the cascaded modulators. The number of bits at the MASH output is determined by the quantizer which determines the number of PWM duty cycles. The trade-offs related to selecting the number of MASH quantizer bits are as follows,

- **PWM Frequency:** The MASH multi-bit output is transformed into a binary signal via the PWM module. More bits infers smaller pulse widths. This translates into increased clock jitter sensitivity and higher PWM operating frequency.
- **Modulation index:** Modulation indices approaching 100% are ideal as both full scale SNR and maximum output power are achieved. The modulation index increases with the number of bits.
- **SNR_i:** The in-band SNR_i is the SNR within the audio band and for 16 bit audio is on the order of 96dB. SNR_i increases with the number of bits according to (4.1.1).

- SNR_o : The out of band SNR_o is the ratio of the in-band signal (± 20 kHz) to the integrated out of band noise (20 kHz to $f_s/2$). The out of band energy can give rise to intermodulation distortion within the audio band due to the switching stage non-linearity. Larger SNR_o reduces the impact of this affect.

4.2 Control Loop Analysis

A closed loop control system with continuous and discrete time models is presented in this section. The control loop is a classical negative feedback design. Negative feedback has several desirable features such as,

- Improved linearity since any distortion introduced by the switching stage is reduced by the loop gain.
- Improved noise rejection. For example, supply or substrate or coupled noise be reduced by the loop gain.
- Reduced second order distortion due to mismatches in the pfet and nfet of the Class D switching stage.
- Reduced distortion inherent in the UPWM process.
- Reduced sensitivity to environmental conditions.

A closed loop system requires a loop filter (compensator) to ensure system stability with sufficient phase margin. Further complicating the design is the mixed signal nature of the architecture that requires mapping between the continuous 's' and discrete 'z' domains. To design the digital compensator a s-domain model of Fig. 4.1 is formulated and then transformed into the z-domain. Fig. 4.8 is a linear model of the amplifier with feedback. The objective is to design a compensation network $C(s)$ to track the input and make the loop insensitive to external noise sources and improve linearity. The remaining transfer functions are defined as follows: $P(s)$ for the pulse modulator DPWM, $G(s)$ for the power stage and low pass filter transfer function, and $H(s)$ for the ADC.

Ultimately $C(s)$ will be converted to an equivalent discrete model $C(z)$ shown in Fig. 4.8b. The approach taken here is to model the system using conventional control system theory in continuous time and then convert $C(s)$ into an equivalent discrete model $C(z)$. This approach is known as digital redesign [67]. The closed loop transfer function of the continuous time model is:

$$\frac{V_o(s)}{V_i(s)} = \frac{CPG(s)}{1 + CPGH(s)} \quad (4.2.1)$$

Figure 4.8: Feedback compensation model a) Continuous time model, b) Mixed signal model digital redesign

and the loop gain $T(s)$ is the cascaded gain of all stages in the loop,

$$T(s) = C(s)P(s)G(s)H(s). \quad (4.2.2)$$

The loop response to additive noise is determined by solving for the transfer function at injection node. The noise could be distortion caused by a non-linearity in the switching stage, variation in the PWM duty cycle or power supply ripple for example. Noise injected in the forward $n_f(s)$ and reverse $n_r(s)$ paths are analyzed in Fig. 4.9. Setting $n_r(s)=0$ and $V_i=0$ the transfer function for noise injected in the forward path is,

Figure 4.9: Forward and reverse noise injection loop analysis

$$\frac{V_o(s)}{n_f(s)} = \frac{G(s)}{1 + T(s)}. \quad (4.2.3)$$

Thus for large loop gain $|T(s)| \gg 1$ the noise appearing at the output is attenuated. Setting $n_f(s)=0$ and $V_i=0$ the transfer function for noise injected in the feedback (reverse) path is,

$$\frac{V_o(s)}{n_r(s)} = \frac{-1}{H(s)} \frac{T(s)}{1 + T(s)}. \quad (4.2.4)$$

Assuming $|T(s)| \gg 1$ the noise transfer function will be proportional to $1/H(s)$ which is a constant. As a result (4.2.4) offers little or no noise reduction.

4.2.1 Continuous to Discrete Time

Initially, the loop analysis is based on continuous s-domain models for all transfer functions. Subsequently, once the loop has been compensated and stabilized, the loop filter $C(s)$ is converted to a z-domain model $C(z)$. The pole-zero matching method is accurate and is relatively insensitive to coefficient variations [68].

The rules governing the pole-zero transformation method of an arbitrary transfer function $C(s)$ are [67]:

1. If $C(s)$ has a pole at $s = -\alpha_p + j\omega_p$, then the discrete equivalent $C(z)$ has a pole at

Figure 4.10: Prototype hardware and measurement implementation.

$z = e^{(-\alpha_p + j\omega_p)T_s}$, where T_s is the period of the sampling frequency.

2. If $C(s)$ has a zero at $s = -\alpha_z + j\omega_z$, then the discrete equivalent $C(z)$ has a zero at $z = e^{(-\alpha_z + j\omega_z)T_s}$.
3. All zero's at $s = \infty$ are mapped to the point $z = -1$.
4. A unit delay is represented by z^{-1} .
5. The gains are matched at band center or similar critical point such as DC and is selected such that $C(s)|_{s=0} = C(z)|_{z=1}$.

4.3 System Prototype

The prototype shown in Fig. 4.10 consists of a FPGA, ADC, signal generator to model a noise source and a differential amplifier to buffer the output for spectrum analyzer measurements. The compensator and modulator functionality are implemented in the Altera Stratix FPGA. A commercial 16b ADC from Analog Devices is used in the feedback path. The power stage and filtering are implemented with dual low pass filtered opamps.

A Class D amplifier usually has a second order low pass LC filter connected to the load. In the FPGA prototype it was convenient to use opamps as buffers and filters but they are not capable of driving low impedance loads. In this case, the distortion from the Class D switching stage is omitted in the model. Therefore, to measure the loop response a calibrated tone is injected into

the loop in both the open and close loop cases. The loop response can then be determined by comparing the output of the open and closed loop measurements.

The DPWM and ADC transfer functions are unity and delay free $P(s)=1$ and $H(s)=1$, respectively. The opamp first order LPF corners at 25 kHz and scales the FPGA PWM output to levels compatible with the ADC. The transfer function is given by:

$$F(s) = \frac{\alpha}{\beta s + 1} \quad (4.3.1)$$

where $\alpha = 0.64$ is an amplitude scaling factor for the ADC and $\beta = 5.67 \times 10^{-6}$ sets the corner frequency.

The compensator $C(s)$ characteristics are specified from Bode plot analysis of the control loop transfer functions. The FPGA DPWM $P(s)$ output is low pass filtered adding 90° phase shift to the loop. A lag compensator [69] of the form,

$$C(s) = C_o(1 + \frac{\omega_L}{s}) \quad (4.3.2)$$

is sufficient to verify system performance. This type of compensator increases the loop gain such that the output is better regulated at frequencies below f_L and is also referred to as a proportional-plus-integral, or PI controller. Increased loop gain is beneficial towards improved noise immunity however, the tradeoff is increased loop bandwidth.

Based on Bode plot analysis $C_o = 8$ and $f_L = 10$ kHz increased the loop gain and conservatively limited the closed loop bandwidth to $1/20$ of the switching frequency to avoid feedback of the switching ripple [70]. Pole-zero matching [67] transforms $C(s) \rightarrow C(z)$ which can then be implemented as a digital filter. Applying pole-zero matching to (4.3.2) with $f_s = 2.5$ MHz the z-domain transfer function becomes,

$$C(z) = \frac{8.125 - 7.875z^{-1}}{1 - z^{-1}} \quad (4.3.3)$$

where the the coefficients have been rounded to the nearest binary fraction to simplify hardware implementation.

Figure 4.11: FPGA prototype open loop frequency response assuming $H(s)=1$ and $P(s)=1$

4.3.1 Bode Plot Analysis

A Bode plot of the open loop network is given in Fig. 4.11. The transfer function of the DPWM modulator $P(s)$ and ADC $H(s)$ are assumed to be unity. The transfer functions for the LPF $F(s)$ and compensator $C(s)$ responses are added to get the overall loop gain $T(s)$. The unity gain frequency for $T(s)$ occurs at 141.5 kHz. The phase margin at unity gain is 97° however, this does not take into account the ADC sampling delay. The ADC sampling (zero order hold) in effect adds $1/2$ clock cycle [29] loop delay and therefore reduces the phase margin. At 2.5 MHz the net phase margin is 87° as indicated by the delayed $T(s)$ phase plot.

The closed loop transfer function is plotted in Fig. 4.12. The magnitude variation over the audio band is less than 1 dB. The 3 dB corner frequency occurs at 122 kHz.

Figure 4.12: FPGA prototype closed loop frequency response assuming $H(s)=1$ and $P(s)=1$

4.3.2 ADC

The ADC requires 16b resolution and a conversion rate of 2.82 MHz. For the prototype, an Analog Devices AD7621 16b Successive Approximation Register (SAR) ADC met the requirements. In addition, it does not add shaped quantization noise like a $\Sigma\Delta$ converter would. While suitable for FPGA system verification, the AD7621 consumes 70 mW which is excessive for low power applications.

In order to address this limitation, a low power ADC architecture will be introduced in following chapters. For the time being the objective is to perform system level verification with the AD7621.

4.3.3 Simulations

The mixed signal system was modelled in Simulink. For simulation purposes the interpolation filters were bypassed by directly oversampling the input tone. The LPF was modelled as a linear transfer function given by (4.3.1) and an ideal ADC modelled by a 16b quantizer and zero order hold. The clock frequency for the simulations was 2.5 MHz.

Simulation FFT results at the output of the MASH 1-2 and LPF in closed loop operation are plotted in Fig. 4.13. For a -6dBfs input the SNR at the LPF output is 109 dB (full scale input SNR=115dB). Though the Simulink model is linear, harmonic distortion arises due to the discrete PWM sampling process. While the even order harmonics are suppressed differentially, the odd order harmonics are reduced by the loop gain. Hence, while distortion is observed at the output of the MASH 1-2 within the loop it is subsequently suppressed at the output due to feedback.

4.3.4 Measurements

The hardware for mono operation is given in Fig. 4.10. The prototype uses an Altera Stratix FPGA and external test boards for the opamps and ADC. Though no power stage is implemented, the hardware is sufficient to test the system architecture and loop dynamics.

The ability of the loop to reject noise, such as that from the power supply or compensate for distortion in the switching stage is set by the loop gain. Since the DPWM $P(s)$ and ADC $H(s)$ are ideally unity gain the loop gain is set by the compensator $C(s)$ and LPF $F(s)$ as:

Figure 4.13: FFT plot at the output of the MASH 1-2 and differential LPF. Plot obtained with $f_s=2.5$ MHz and applying a hanning window.

$$\frac{V_o(s)}{V_f(s)} = \frac{1}{1 + C(s)F(s)} \quad (4.3.4)$$

where $V_f(s)$ is a noise source in the forward path of the loop. Fig. 4.14 is a plot of the theoretical, simulated and measured loop response. The measurement was performed by injecting a tone into one of the opamps and comparing the open and closed loop responses on a spectrum analyzer. The results are in generally good agreement with some discrepancy due to the pole-zero mapping process and coefficient quantization.

The results of Fig. 4.14 indicate the control loops ability to reduce power supply noise and non-linear switching effects. Furthermore, the non-linear effects associated with UPWM sampling [14] are also reduced. This avoids the need for complex high speed DSP algorithms to synthesize low distortion PWM when generated outside the loop as in [56]. The final plot of Fig. 4.15 is the measured differential PWM output with a 1 kHz input tone. Both the differential output and feedback help to suppress harmonics.

Figure 4.14: Frequency response of the control loop compensation.

Figure 4.15: FPGA PWM output as measured on a HP3585A spectrum analyzer (-6dBfs, 20 Hz-22 kHz, 10dB/div).

Figure 4.16: Block diagram for revised system with reduced operating frequency.

4.4 Revised System Design

A revised design with a lower operating frequency $OSR=32\times$ is given in Fig. 4.16. The motivation being to reduce the ADC power consumption and Class D switching losses. Analysis of switching losses is provided in Sec. 4.5 and ADC power consumption in Chapter 5. Lowering the operating frequency exasperates the loop delay and complicates the compensator design.

In the revised design the feedback is tapped at the load resistor following the Class D amplifier LC network. In this case the LPF in the feedback path (used in the FPGA prototype) can be eliminated. The second order low pass LC filter introduces a 180° phase shift above the corner frequency. This will require a redesigned compensator $C(s)$ to ensure stability. Recall, in the case of the FPGA prototype there is only a 90° phase shift associated with the opamp first order LPF.

Reducing the operating frequency from 64×44.1 kHz to 32×44.1 kHz would be beneficial from two perspectives. First, reduced amplifier switching losses and lower digital circuitry power consumption. Secondly, the ADC input referred noise bandwidth would be reduced by one half. The disadvantage is that the phase margin degradation associated with the ADC sampling delay will be doubled. Furthermore, the high frequency noise from the DPWM will be more difficult to filter while maintaining loop stability. The modulator SNR will be reduced by 21 dB according to (4.1.9) as well.

As in the FPGA prototype case the DPWM transfer function $P(s)$ and the ADC transfer function $H(s)$ are unity. The ADC conversion delay will be accounted for in the phase margin analysis and a second order low pass filter and switching stage will be modelled.

The Class D amplifier with second order LC filter is analogous to a continuous conduction

DC-DC buck converter for which the transfer function $G(s)$ is of the general form [69]:

$$G(s) = \frac{V_{cc}}{1 + \frac{s}{Q_o\omega_o} + (\frac{s}{\omega_o})^2} \quad (4.4.1)$$

where V_{cc} is the supply voltage. With the Class D amplifier and LCR second order low pass filter the transfer function can be expressed as,

$$G(s) = \frac{V_{cc}}{1 + R_i/R + s(R_iC + L/R) + s^2LC} \quad (4.4.2)$$

where R_i is a series resistor to account for the inductor Q . By equating the coefficients of (4.4.1) and (4.4.2), formulas for ω_o and Q_o are,

$$Q_o = \frac{1}{R_i\sqrt{C/L} + \sqrt{L/C}/R} \quad (4.4.3)$$

$$\omega_o = \frac{1}{\sqrt{LC}} \quad (4.4.4)$$

4.4.1 Interpolation Filters

The general concepts of IF design were discussed in Sec. 4.1.1. For the revised system an IF with OSR=32 will be implemented in the mixed signal model. The block diagram of the IF filter is illustrated in Fig. 4.17. The IF consists of two FIR filter stages followed by a digital sample and hold register. The IF suppresses aliases between baseband and f_s by first removing the odd order aliases and then the even order aliases.

Fig. 4.18 is a plot of input spectrum and frequency response of each filter. The first stage of the IF operates at $2f_N$ and suppresses the odd-order images. The operation is illustrated in Fig. 4.18a and b where the first plot shows the Nyquist sampled input signal followed by the spectrum of the first stage. This filter has stringent passband and rejection characteristics. This filter is efficiently realized with a 51-tap Halfband FIR filter. Halfband filters are very economical since every second tap weight is zero except for the center tap. The 51-tap Halfband provides an 0.003 dB passband ripple response with a minimum stopband attenuation of 75dB.

The second stage of the IF has a clock frequency of $8f_N$ and removes the even-order images. As shown in Fig. 4.18c this rolloff is much less abrupt than the first stage. For this stage a

Figure 4.17: Block diagram of OSR=32 interpolation filter a) Baseband input spectrum, b) Halfband FIR 2x, c) LPF FIR 4x, d) S/H 4x, e) cascaded output.

25-tap LPF FIR filter provided a minimum of 70dB stopband attenuation and 0.36dB passband ripple.

Finally, a digital sample and hold register operating at $32f_N$ provides some extra sinc function filtering as shown in Fig. 4.18d. The cascaded IF response is illustrated in Fig. 4.18e.

4.4.2 PID Compensator

A PID compensator is comprised of a PD and PI transfer function. Each serves a specific purpose in shaping the open loop magnitude and phase response. The role of each is as follows,

- PD is a proportional-plus-derivative or lead transfer function that is used to increase phase margin. A zero is added to the loop gain far below the crossover (unity gain) frequency such that the phase margin is increased. A pole above the crossover frequency is added to limit the gain of the zero.
- PI is a proportional-plus-integral or lag transfer function that increases low frequency loop gain such that the output is better regulated from DC to frequencies well below the crossover frequency. An inverted zero is added well below the crossover frequency.

PID (proportional, integral, derivative) controllers are common in compensating second order systems. The PID controller incorporates aspects of both PI and PD controllers to improve phase margin and low frequency regulation.

The first step is to calculate the parameters which define the transfer functions with component values $L=10\text{ }\mu\text{H}$, $C=5.23\text{ }\mu\text{F}$, $R=32\text{ }\Omega$, and $R_i = 0.2\text{ }\Omega$ (derived from inductor Q). These standard components values that can be obtained in a 0805 package. From (4.4.3), (4.4.4) $Q_o=5.3$ and $f_o=22\text{ kHz}$ respectively.

Figure 4.18: Interpolation Filter frequency response, a) Baseband input spectrum, b) Halfband FIR 2x, c) LPF FIR 4x, d) S/H 4x, e) cascaded output.

The PID was designed in an iterative process to optimize the phase margin and while increasing the loop gain. For the PD controller

$$PD(s) = k_o \frac{1 + s/\omega_z}{1 + s/\omega_p} \quad (4.4.5)$$

where $k_o=10.72$, $f_z=37.7$ kHz and $f_p=525.6$ kHz. The PI controller transfer function is

$$PI(s) = 1 + \frac{\omega_{iz}}{s} \quad (4.4.6)$$

where the inverted zero $f_{iz}=10$ kHz. Substituting k_o , f_z , f_p , f_{iz} and multiply PD and PI to get PID,

$$C(s) = PID(s) = PD(s)PI(s) = \frac{4.52 \times 10^{-5}s^2 + 13.56s + 6.734 \times 10^5}{s(3.028 \times 10^{-7}s + 1)} \quad (4.4.7)$$

The PID transfer function is then converted to a discrete model using the pole-zero matching technique resulting in,

$$C(z) = \frac{61.08 - 108.9z^{-1} + 48.32z^{-2}}{1 - 1.076z^{-1} + 0.07576z^{-2}} \quad (4.4.8)$$

4.4.3 Simulations

The system will be simulation in two steps. The first step will be fundamental Bode plot analysis based on the s-domain transfer functions. This will be followed by Simulink simulations to verify the mixed signal model operation.

The Bode plot of the open loop gain $T(s)$ is given in Fig. 4.19. Note that the continuous model exhibits a phase margin of 58° at the crossover frequency of 141 kHz however, the actual mixed signal phase margin is 38° due to the ADC sampling delay. The closed loop frequency response is given in Fig. 4.20 where the corner frequency occurs at 225 kHz.

The mixed signal model was then simulated in Simulink. In this manner system functionality such as SNR and noise immunity is verified. The baseband input to the IF filters is a 20 kHz bandwidth sampled at 40 kHz. With an OSR=32 the loop operating frequency is 1.28 MHz. Using the DPWM as in the FPGA prototype the maximum SNR calculated from (4.1.1) is SNR=102.3 dB.

Figure 4.19: Revised design open loop frequency response, $H(s)=1$ and $P(s)=1$

Figure 4.20: Revised design closed loop frequency response, $H(s)=1$ and $P(s)=1$

Figure 4.21: Revised design closed loop mixed signal Simulink model SNR.

The theoretical SNR can be benchmarked relative to the closed loop mixed signal model. In Fig. 4.21 the input amplitude is swept and SNR calculated at each point. In this simulation the input is 1 kHz tone with calibrated noise floor set with a random noise generator. As explained in the Sec. 4.1.2 the modulator will be unstable at full scale and is therefore scaled back -6dBfs yielding a 95.5 dB (~ 16 b) SNR. The spectral output is shown in Fig. 4.22. Note that the aliasing components at 39, 41, 79, 81, 319 and 321 kHz result from the interpolation filtering process.

The ability of the loop to reduce noise introduced in the forward path is plotted in Fig. 4.23. The noise rejection is simulated with a 1kHz tone input and a calibrated interference tone injected at the switching stage. Good agreement between the theoretical and Simulink model is achieved.

Figure 4.22: Revised design closed loop spectral output.

Figure 4.23: Revised design forward path noise suppression.

Figure 4.24: Class D amplifier consisting of a driver and power stage.

4.5 CMOS Class D

An unloaded Class D amplifier is shown in Fig. 4.24. It consists of a driver stage and power stage. The power stage is a large inverter capable of driving the $16\ \Omega$ or $32\ \Omega$ headphone impedance with minimal losses. Since the power stage is a large device, a series of tapered inverters is required to switch it efficiently. The series of tapered inverters is referred to as the driver stage.

The amplifier losses can be divided into switching P_s and conduction P_c losses. The total power loss is defined as,

$$P_t = P_c + P_s. \quad (4.5.1)$$

The switching losses are related to the charging and discharging of the MOSFET gate capacitance during each switching cycle. When analyzing the switching losses there is no load on the power stage. Conduction losses are related to $I^2 R_{on}$ of a loaded power stage. These two losses will be examined independently and then summed to determine total loss.

4.5.1 Switching losses

Tapered buffers have traditionally been analyzed from a digital perspective in terms of minimizing propagation delays. A summary of the publications related to propagation modelling can be found in [71]. Since current CMOS technology operates in the GHz range, significantly higher than the application here, the propagation delay is of less interest than the switching losses.

The most common taper ratio [72] is,

$$\kappa = \sqrt[n]{\frac{C_{out}}{C_{in}}} \quad (4.5.2)$$

which can be associated to the gate capacitance by the MOSFET dimensions,

$$\kappa = \sqrt[n]{\frac{C_{ox}L(W_n^p + W_p^p)}{C_{ox}L(W_n^d + W_p^d)}} = \sqrt[n]{\frac{W_n^p + W_p^p}{W_n^d + W_p^d}} \quad (4.5.3)$$

where W_x^y represents the gate width of a particular transistor. The subscript $x = n$ or p refers to either a nfet or pfet device respectively. The superscript $y = p$ or d refers to the power stage or first stage of the tapered buffer driver respectively.

The power stage dimensions are $W_p^p=4\text{mm}$ and $W_n^p=1.76\text{mm}$ with minimum length $L=0.13\text{ }\mu\text{m}$. The sizing matches the g_m of the devices and provides low channel resistance $R_{ds} \approx 0.8\text{ }\Omega$ to minimize conduction losses. The objective is to design the driver with optimum taper ratio κ in order to minimize switching losses. The switching energy (Joules) per cycle can be calculated from,

$$E(J) = V_{cc} \int_T i(t) dt \quad (4.5.4)$$

where T is one period of the switching cycle. Note that $i(t)$ is significant only during the rising and falling transition edges and virtually zero at other times.

To find the optimum tapering ratio the switching losses for various tapering ratios have been simulated with $W_n^p=1.76\text{m}$, $W_p^p=4\text{mm}$, $W_n^d=160\text{nm}$, $W_p^d=400\text{nm}$. The rise/fall time and energy are plotted in Fig. 4.25. The rise/fall time decreases with the taper ratio as the size mismatch between adjacent inverters is reduced. At the same time the energy per cycle of the power stage is reduced however, the driver energy is increasing. These two opposing trends suggest an optimum taper ratio is attainable.

The faster rise/fall time lowers the energy in the power stage since there is less time for simultaneous nfet and pfet conduction. The driver energy steadily increases due to increased capacitive loading. The net result is an optimum tapering ratio of $n=6$ beyond which the power stage energy reduction experiences diminishing returns and is offset by increased energy consumption of the driver.

Figure 4.25: Simulation of Class D amplifier. a) Average 10% to 90% rise/fall time, b) Energy per switching cycle.

With the optimum taper ratio determined the power dissipation as a function of frequency can be calculated from,

$$P_s(W) = \frac{E(J)}{T} \quad (4.5.5)$$

where T is the period of one switching cycle and is plotted in Fig. 4.26.

4.5.2 Conduction losses

Unlike switching losses, conduction losses are not a function of frequency. If the rise/fall time is a negligible fraction of the switching cycle then the R_{ds} impedance transition is assumed to be instantaneous. The conduction losses take into account the resistive losses associated with the channel resistance R_{ds} and interconnect wiring losses R_w such that the total resistance is,

$$R_{on} = R_{ds} + R_w. \quad (4.5.6)$$

The conduction losses for a differential bridge tied load is calculated from,

Figure 4.26: Total switching losses of the driver and power stage as a function of frequency.

$$P_c = P_{to} \left(1 - \frac{R_l}{R_l + 2R_{on}} \right) \quad (4.5.7)$$

where R_l is the load impedance (16 Ω or 32 Ω) and P_{to} is the total power dissipated in the resistors.

4.5.3 Total losses

The total losses include both the switching and conduction losses. Depending on the frequency of operation and power output either the switching or conduction losses can dominate. As an example calculate the losses for a Class D amplifier with the following specifications,

- Differential bridge tied load
- ($W_n^p=1.76\text{mm}$, $W_p^p=4\text{mm}$)
- Driver taper ratio $n=6$
- $R_{ds}=0.8 \Omega$
- $R_w=0.4 \Omega$
- $R_l=32 \Omega$
- $f=2.82 \text{ MHz}$
- $P_{to}=100\text{uW}$

From Fig. 4.26 with an operating frequency of 2.82 MHz the switching losses are 77 uW per amplifier or 154 uW for a bridge tied load. The conduction losses are then calculated from (4.5.7) to be $P_c=7$ uW. In this case the switching losses are predominate and the total losses according to (4.5.1),

$$P_t = P_c + P_s = 154 + 7 = 161\text{uW} \quad (4.5.8)$$

4.6 Key Points

The design, simulation and construction of a digital input closed loop Class D amplifier has been presented. Some key points of the design are as follows:

- A prototype operating at 2.5 MHz was constructed with an Altera FPGA, Analog Devices 16b SAR ADC and dual low pass filtered opamps.
- Noise injection measurements were performed and were in good agreement with theoretical predictions. At 1 kHz the noise rejection is 34dB
- The DPWM consists of multi-bit $\Sigma\Delta$ and PWM hybrid configuration. Any distortion arising from the modulator is compensated by the loop gain.
- the closed loop was analyzed in the frequency domain using phase margin analysis. The continuous time transfer functions were then converted to the discrete time domain using the pole zero matching technique.
- A revised system design was proposed operating at half the frequency of the prototype. The goal being to reduce overall power consumption. This design was simulated in Simulink but not prototyped.
- The Class D amplifier losses consist of switching and conduction losses. Switching losses are frequency dependant and conduction losses are frequency independent.

Chapter 5

Low Power ADC Design

As highlighted in Chapter 4 the quantization noise arising from the $\Sigma\Delta$ process complicates the process of feedback design. The approach taken here is to use a Nyquist type data converter which avoids the noise shaping process. Of particular interest is a specific Successive Approximation Register (SAR) ADC with programmable thresholds. While this architecture alleviates the quantization noise restriction, other significant challenges arise.

This chapter begins with an explanation of the generic SAR algorithm followed by a new implementation approach. Simulation and analytical calculations for key design parameters such as gain, common mode noise rejection, RMS input referred noise, resolution and tuning range are presented. In addition, design challenges are discussed.

5.1 SAR Algorithm

ADCs are categorized as either Nyquist or $\Sigma\Delta$ type. A Nyquist rate converter operates slightly above the Nyquist rate and typically relies on precision matched components. On the other hand, $\Sigma\Delta$ converters operate at much higher sample rates and in turn the matching precision is relaxed [63]. $\Sigma\Delta$ converters fundamentally involve quantization and noise shaping. This leads to significant out of band noise peaking at $f_s/2$. Though the noise can be digitally filtered, the filtering introduces delay. In a closed loop application such as this, the delay leads to reduced phase margin and potential instability. Hence, though $\Sigma\Delta$ converters are preferred, they are problematic for closed loop Class D systems. In light of this, a Nyquist type ADC is proposed for this application. In particular, a Successive Approximation Register (SAR) ADC is investigated.

SAR ADCs are frequently selected for medium to high resolution applications (8 to 16b) with

moderate conversion rates (up to 5 Msps) requiring low power consumption. As a result SAR ADCs are ideal for a wide variety of portable battery operated applications.

The SAR ADC utilizes a binary search algorithm. Therefore, while the internal circuitry may be running at several Megahertz (MHz), the actual ADC sample rate is $1/N$ of that number where N is the resolution or number of converter bits.

The SAR algorithm flowchart is given in Fig. 5.1 where the input is assumed to be within $\pm V_{ref}/2$. Upon assertion of the start signal the input V_{in} is sampled and the DAC output is set to 0V. The comparator then determines the signal polarity with the resulting $b_i=0$ or 1 sign bit stored. Consequently, the next bit is determined by setting $V_{DAC} = V_{ref}/4$ or $-V_{ref}/4$ for $b_1=1$ or 0, respectively. Likewise, the process repeats in total N times while adjusting the DAC at each iteration by a factor of $\pm V_{ref}/2^{i+1}$ accordingly. At the end of the conversion cycle the N -bits stored in the SAR are a valid digital representation of the analog input.

Two SAR circuit block diagrams are shown in Fig. 5.2. The conventional approach is shown in Fig. 5.2a which is a direct implementation of the flowchart. For this architecture the resolution is typically limited by the DAC linearity. Process and mismatch errors generally dictate that converters with a resolution of 12 bits or higher will require laser trimming and/or a calibration procedure.

An alternative approach is proposed in Fig. 5.2b where the DAC has been replaced by a comparator with programmable offsets. The offset or threshold voltage, represents the tipping point of the comparator. Shifting the offset voltage V_{off} is analogous to the functionality of setting V_{DAC} . In essence, V_{off} replaces V_{DAC} in accordance with Fig. 5.1.

One way to create offsets is by introducing intentional mismatch or asymmetry in a differential circuit. In conventional circuit design asymmetry is highly undesirable due to degradation of the Common Mode Rejection Ratio (CMRR). Thus, while introducing intentional offsets a degraded CMRR is one penalty of this approach.

Multiple forms of mismatch techniques are combined to allow both coarse and fine offset tuning to within a fraction of a LSB. The manner in which these offsets are generated and selected is explained in the following sections.

Figure 5.1: SAR ADC algorithm flowchart

a) Conventional SAR ADC functional block diagram.

b) Offset configurable SAR ADC functional block diagram.

Figure 5.2: Conventional and alternative SAR ADC block diagrams.

5.2 COP ADC Architecture

The concept and design specifics of a Configurable Offset with Preamplifier (COP) SAR ADC or simply COP ADC are now introduced. The COP ADC shown in Fig. 5.3 is a more detailed circuit diagram of the system shown in Fig. 5.2b. It is meant to operate in accordance to the process flow of Fig. 5.1 where V_{DAC} has been replaced by V_{off} which is variable. In this section the progression to circuit level implementation is made.

The COP ADC consists of input track and hold capacitors, an array of preamplifiers with fixed offsets, a high resolution low power comparator and digital circuitry for calibration and successive approximation. In addition to the preamplifier array, the comparator has a series of offset mechanisms that can be digitally controlled, hence the COP acronym.

Figure 5.3: COP SAR ADC block diagram

An important aspect of the design is the method in which the offsets are generated. The preamplifier offsets are configurable in ± 30 mV steps while the comparator has three offset controls. The comparator steps are ± 8 mV, ± 316 μ V and ± 16 μ V. Overall, the four offset settings are independently controlled and can be superimposed to generate any desired offset limited by the smallest step size (16 μ V).

The target specifications for the COP ADC are listed in Table 5.1. The conversion rate is

set according to the DPWM frequency of 64×44.1 kHz or 2.82 Msps. Likewise, the comparator frequency is 16×2.82 Msps or 45.16 MHz. The input voltage swing is $2.4 V_{pp}$ which is the maximum swing across the load assuming a 1.2 V supply. The maximum swing will never be achieved due to saturation limit of the DPWM. A more practical swing of $1.6 V_{pp}$ would provide 10mW of power to a 32Ω load without saturating the DPWM. The ADC power dissipation will dominate the overall system budget. To the best of the authors knowledge the commercial ADC with comparable specifications and lowest power consumption is the Analog Devices AD7985 16b SAR. The AD7985 datasheet specifies a power consumption of 28mW at a sample rate of 2.5 Msps.

The input referred noise is a critical spec. It is calculated from simulations by integrating the input referred noise from DC to one half the sample frequency (in this case 22.58 MHz). The noise consists of both thermal and flicker noise contributions. The end result is that excessive noise will result in comparator errors. Since noise reduction entails increased power requirements it is important to specify the noise correctly.

The probability of errors is determined from the ratio of the integrated noise to the lsb. Assuming a Gaussian noise distribution the lsb voltage step size should be 6 to 7 time the rms noise voltage [73]. In this case the probability of comparator error is less then 10^{-9} when $lsb = 6e_{noise}$, ie. the probability the noise exceeds 6 standard deviations. Here, e_{noise} is the integrated input referred noise of the cascaded preamplifier and comparator. This is a stringent requirement of which the impact on SNR is not clearly defined.

It has been demonstrated for SAR ADCs the noise specification can be relaxed to $1/2lsb$ with the addition of an extra comparator iteration [74]. In this approach for the first N iterations the SAR operates in a high noise state wherein $e_{noise} = 1/2lsb$ and then for an extra error correction iteration N+1 it operates in the low noise state where $e_{noise} = 1/4lsb$. This only slightly increases the overall power consumption. Based on measurement results SNR, INL and DNL specifications are published rather than noise specifications.

The following sections explain in each circuit in more detail. Note that the fabricated integrated circuit consists of the preamplifiers and comparator which form the core of the COP ADC. The track and hold has been omitted and the ADC control logic can be implemented in a FPGA for maximum flexibility.

Table 5.1: Initial COP ADC target specifications.

Parameter	Specification
Process	0.13um IBM CMOS
Supply	1.2 V
Power consumption	<5 mW
Conversion rate	2.82 Msps
Sample frequency	45.16 MHz
Input voltage	2.4 V _{pp} differential
Resolution	16b or 36.6uV
Input referred noise	<1/2 lsb
Calibration	Digital

5.2.1 Track-and-Hold

Since the COP ADC must perform N comparisons, the input voltage is sampled and held constant during the conversion cycle. An effective and low power solution is to use passive charge sharing. It begins with tracking the input voltage by closing SW_t and opening SW_h . The tracked voltage is then sampled and held by opening SW_t and closing SW_h . The track and hold settling times are determined by the $R_{SW}C$ time constant. Once sampled, the input voltage is held until the conversion cycle is complete (16 clock cycles). Upon completion the track and hold process is repeated for the next conversion.

Passive charge sharing approaches which use N binary weighted capacitors [75] suffer from the fact that the differential comparator input voltage is coupled to the capacitance array which changes after each iteration [76]. Since this COP ADC requires only two fixed capacitors for track C_t and hold C_h it is not hindered by this affect. Only a constant fixed offset need be calibrated out. Track and hold capacitors should be sized according to limiting the noise according to kT/C .

5.2.2 Preamplifier

A preamplifier provides several essential functions such as signal gain, isolating the source from comparator kickback, reducing the comparator input referred noise and increasing the tuning range. Since the preamplifier is the first stage of the ADC its noise specification is important in determining the ADC resolution. The penalty paid for the aforementioned benefits is increased power consumption.

Figure 5.4: Differential amplifier.

The COP ADC has an array of preamplifiers, all connected to a common resistive load. The array consists of a balanced differential pair and several intentionally mismatched differential pairs. The mismatches are intentional so as to produce an array of linear offset voltages. The drawback of this approach is compromised common mode noise rejection.

In the following section analytical expressions are derived for gain, common mode noise rejection and offset voltage. The formulas are then shown to provide very good agreement with simulation results. In addition, flicker and thermal noise contributions are discussed and simulated.

Gain and Rejection Ratios

We begin with defining the gain parameters for a generic amplifier in terms of common and differential mode voltages. Subsequently, a differential pair CMOS amplifiers is analyzed to derive gain and noise rejection parameters. Equivalent half circuit models for the common and differential modes take into account mismatches and simplify the analysis. Using this approach gain and rejection ratio formulas are derived.

Based on small signal analysis, several performance parameters of the differential pair amplifier can be derived. Small signal analysis is valid for signal levels in which the resulting nonlinearity is insignificant. The differential amplifier of Fig. 5.4 can be characterized in terms of its common and differential mode input and output. The differential mode input and output are defined as,

$$v_{id} = v_{i1} - v_{i2} \quad (5.2.1)$$

$$v_{od} = v_{o1} - v_{o2}. \quad (5.2.2)$$

The input and output common mode are defined as,

$$v_{ic} = \frac{v_{i1} + v_{i2}}{2} \quad (5.2.3)$$

$$v_{oc} = \frac{v_{o1} + v_{o2}}{2} \quad (5.2.4)$$

The general equations defining the gain parameters for a differential amplifier [10] are,

$$v_{od} = A_{dm}v_{id} + A_{cm-dm}v_{ic} \quad (5.2.5)$$

$$v_{oc} = A_{dm-cm}v_{id} + A_{cm}v_{ic} \quad (5.2.6)$$

from which four gain parameters can be extracted. The differential mode voltage gain A_{dm} relates the change in the differential output to differential input. This is the desired voltage gain:

$$A_{dm} = \left. \frac{v_{od}}{v_{id}} \right|_{v_{ic}=0} \quad (5.2.7)$$

The common mode voltage gain A_{cm} relates the voltage change in the common mode output to common mode input:

$$A_{cm} = \left. \frac{v_{oc}}{v_{ic}} \right|_{v_{id}=0} \quad (5.2.8)$$

The differential mode to common mode voltage gain A_{dm-cm} relates the change in the common mode output to differential mode input:

$$A_{dm-cm} = \left. \frac{v_{oc}}{v_{id}} \right|_{v_{ic}=0} \quad (5.2.9)$$

The common mode to differential mode voltage gain A_{cm-dm} relates the change in the differential mode output to common mode input:

$$A_{cm-dm} = \left. \frac{v_{od}}{v_{ic}} \right|_{v_{id}=0} \quad (5.2.10)$$

A differential amplifier amplifies differential input signals while rejecting any changes in its common mode input. Common mode noise needs to be sufficiently suppressed otherwise it can propagate and degrade the performance of subsequent stages. Common mode noise may originate from a variety of sources such as the power supply or substrate coupling. The differential voltage gain A_{dm} should therefore be much larger than the gain parameters of (5.2.8)-(5.2.10).

For a perfectly symmetric amplifier with pure differential input ($v_{ic} = 0$) the output is purely differential ($v_{oc} = 0$), therefore $A_{dm-cm} = 0$. Likewise, in a perfectly symmetric amplifier $A_{cm-dm} = 0$, however symmetry alone does not guaranty $A_{cm} = 0$. Rejection ratios can be defined to quantify susceptibility to undesirable noise. The most prevalent of which is the Common-Mode-Rejection-Ratio (CMRR) defined as:

$$CMRR = \left| \frac{A_{dm}}{A_{cm}} \right|. \quad (5.2.11)$$

Similarly, the Differential to Common mode Rejection Ratio (DCRR) and Common mode to Differential mode Rejection Ratio (CDRR) are defined as:

$$DCRR = \left| \frac{A_{dm}}{A_{dm-cm}} \right| \quad (5.2.12)$$

$$CDRR = \left| \frac{A_{dm}}{A_{cm-dm}} \right| \quad (5.2.13)$$

An unbalanced amplifier with a non-zero A_{dm-cm} will generate some common mode output for a pure differential input. While not desirable this will have minimal impact on latter circuits which can reject the common mode component according to the CMRR. Of more concern is a non-zero A_{cm-dm} in which a common mode input is converted to a differential output. The resulting differential output will be indistinguishable from the desired signal and therefore cannot be rejected by subsequent stages.

Due to process and mismatch variation practical amplifiers will exhibit some degree of asymmetry which results in non-zero A_{dm-cm} , A_{cm-dm} and A_{cm} . In this particular application, mismatch is deliberately introduced thereby further exasperating the problem. As a result, the rejection ratio performance will be degraded. Thus the gain parameters must be calculated or simulated to determine their impact on overall system performance.

Figure 5.5: Source coupled differential pair amplifier.

The direct approach to calculate the gain terms is to analyze the complete small signal equivalent circuit of Fig. 5.5. Alternatively, exact half circuit analysis is possible if the cross coupled gain terms A_{dm-cm} and A_{cm-dm} are taken into account [10]. Using this approach the mismatch in g_m , g_{mb} and r_o have been taken in account while assuming a matched load resistance R . Based on the analysis in Appendix A the derived gain equations are:

$$A_{cm-dm} = R \frac{\alpha_1}{\alpha_2} \quad (5.2.14)$$

$$A_{dm-cm} = \frac{R(-4r_o(R+r_o)\Delta g_m - 4g_m R \Delta r_o + \Delta g_m \Delta r_o^2)}{4\alpha_2} \quad (5.2.15)$$

$$A_{cm} = \frac{-R(4g_m r_o(R+r_o) + R\Delta g_m \Delta r_o - g_m \Delta r_o^2)}{\alpha_2} \quad (5.2.16)$$

$$A_{dm} = R \frac{\alpha_3}{2\alpha_2} \quad (5.2.17)$$

where,

$$\alpha_1 = -4r_o\Delta g_m(R + r_o + 2R_{tail}(1 + g_{mb}r_o)) + 8g_m\Delta g_mr_o^2R_{tail} - 4\Delta r_og_m(R + 2R_{tail}) + (\Delta g_m + 2g_{mb}R_{tail}\Delta g_{mb})\Delta r_o^2 \quad (5.2.18)$$

$$\alpha_2 = 4(R + r_o)(R + r_o + 2R_{tail}(1 + (g_m + g_{mb})r_o)) + 2RR_{tail}(\Delta g_m + \Delta g_{mb})\Delta r_o - (1 + 2(g_m + g_{mb})R_{tail})\Delta r_o^2 \quad (5.2.19)$$

$$\alpha_3 = -4r_o(4g_m^2r_oR_{tail} + 2g_m(R + r_o + 2R_{tail} + 2g_{mb}r_oR_{tail}) - r_oR_{tail}\Delta g_m(\Delta g_m + \Delta g_{mb})) - 2(R + 2R_{tail})\Delta g_m\Delta r_o + (4g_m^2R_{tail} + 2g_m(1 + 2g_{mb}R_{tail}) - R_{tail}\Delta g_m(\Delta g_m + \Delta g_{mb}))\Delta r_o^2 \quad (5.2.20)$$

The difference and average parameter values are defined as,

$$\Delta g_m = g_{mM1} - g_{mM2} \quad (5.2.21)$$

$$\Delta r_o = r_{oM1} - r_{oM2}$$

$$\Delta g_{mb} = g_{mbM1} - g_{mbM2}$$

$$g_m = (g_{mM1} + g_{mM2})/2 \quad (5.2.22)$$

$$r_o = (r_{oM1} + r_{oM2})/2$$

$$g_{mb} = (g_{mbM1} + g_{mbM2})/2$$

Offset Voltage

The COP ADC uses an array of preamps like that of Fig. 5.5 with intentional differential pair mismatch to generate offsets. The amplifiers are connected in parallel though only one is active at any instance in time. Assuming a matched load R, the differential input referred offset voltage V_{io} , can be derived from DC analysis to equalize the diff pair drain currents [10] given as,

$$V_{io} = \Delta V_t + \frac{V_{gs} - V_t}{2} \left(\sqrt{\frac{1}{1 + \frac{\Delta(W/L)}{2(W/L)}}} - \sqrt{\frac{1}{1 - \frac{\Delta(W/L)}{2(W/L)}}} \right) \quad (5.2.23)$$

where the average and difference quantities are defined as,

$$\Delta(W/L) = (W/L)_1 - (W/L)_2 \quad (5.2.24)$$

$$(W/L) = \frac{(W/L)_1 + (W/L)_2}{2} \quad (5.2.25)$$

$$\Delta V_t = V_{t1} - V_{t2} \quad (5.2.26)$$

$$V_t = \frac{V_{t1} + V_{t2}}{2} \quad (5.2.27)$$

For small mismatches (5.2.23) can be approximated by the simplified equation,

$$V_{io} = \Delta V_t - \frac{V_{gs} - V_t}{2} \cdot \frac{\Delta(W/L)}{(W/L)} \quad (5.2.28)$$

Noise

The preamplifier is the first stage in the COP ADC, hence its noise contribution is significant in the overall system performance. Though the comparator stage can contribute significant noise as well, its contribution is reduced by the preamplifier gain.

The dominant noise sources in active fets are thermal and flicker noise. The input referred thermal and flicker noise spectral densities (V^2/Hz) are given by [77],

$$V_{ni}^2(f) = \frac{8kT}{3g_m} + \frac{\kappa}{WLC_{ox}f} \quad (5.2.29)$$

where

- κ is dependant on device characteristics and can vary significantly for devices within the same process,
- k is Boltzmann's constant 1.38×10^{-23} J/K,
- T is the temperature in Kelvin,
- W is the device width,
- L is the device length,
- C_{ox} is the gate capacitance per unit area.
- g_m is the transconductance

Figure 5.6: Simplified model for low and moderate frequencies with zero gate current.

The MOSFET can be modelled as a noiseless device with an equivalent noise source determined by (5.2.29) applied to the gate as shown in Fig. 5.6

The RMS noise is calculated by integrating the noise spectral density over the Nyquist bandwidth,

$$V_{ni(rms)} = \sqrt{\int_0^{f_s/2} V_{ni}^2(f) df} \quad (5.2.30)$$

and $f_s/2$ is calculated from,

$$f_s/2 = N \times OSR = 16 \times 64 \times 44.1 \times 10^3/2 = 22,579.2 \text{ kHz} \quad (5.2.31)$$

where N is the number of bits and OSR is the oversampling ratio of the DAC SDM.

Equation (5.2.29) offers insight into how to approach noise reduction. For the flicker noise contribution it is apparent that larger devices are better since the $1/f$ noise is inversely proportional to device size WL . In addition, p-channel devices have less $1/f$ noise than n-channel devices. The thermal noise is due to the resistive channel R_{ds} of the transistor operating in saturation. Thermal noise can be reduced by increasing g_m . Since g_m is proportional to the $\sqrt{I_d}$, a quadrature increase in current is required to reduce the thermal noise spectral density by $1/2$. According to 5.2.30 the RMS voltage will in turn be reduced by a factor of $1/\sqrt{2}$.

Preamplifier Array Analysis and Simulations

The fabricated preamp schematic is shown in Fig. 5.7. It consists of multiple differential pairs connected in parallel. The drains of the differential pairs are all tied to the matched resistive load. The common load eliminates the need for switches and associated charge injection errors.

Figure 5.7: Preamplifier schematic.

The array consists of a matched differential pair and several intentionally mismatched pairs. These mismatched pairs introduce both positive and negative offsets to extend the COP ADC tuning range. During the conversion cycle the COP ADC algorithm dictates which one of the preamplifiers is enabled at any given time.

Table 5.2 lists the preamp array design parameters valid for a bias current of $I_{bias}=1.25\text{mA}$ and load resistance $R=750\Omega$. In total there are 9 preamps in the array, the 5 listed plus another 4 which swap W_1 and W_2 of preamps 1-4. This provides both positive and negative offset tuning.

The small signal differential voltage gain A_{dm} calculated using (5.2.17) is plotted Fig. 5.8a. In addition, the unbalanced and balanced conditions have been simulated. These two conditions

Table 5.2: Preamplifier array device parameters($V_{cc}=1.2\text{V}$, $R=750\Omega$ and $I_{bias}=1.25\text{mA}$).

Preamp	W_1 (μm)	W_2 (μm)	g_{m1} (mS)	g_{m2} (mS)	g_{mb1} (mS)	g_{mb2} (mS)	r_{o1} (Ω)	r_{o2} (Ω)	R_{tail} (Ω)
0	152	152	11.29	11.29	1.75	1.75	3103	3103	1565
1	192	112	13.89	8.67	2.17	1.34	2373	4266	1565
2	224	80	16.02	6.47	2.53	0.99	1931	5970	1550
3	248	56	17.69	4.70	2.81	0.72	1627	8489	1531
4	264	40	18.84	3.45	3.01	0.53	1408	11850	1531

exist due to the introduction of intentional device mismatch. Unbalanced refers to the case where the common mode voltage results in unequal bias current distribution ($I_{d(M1)} \neq I_{d(M2)}$). In the balanced case the gate voltages have been adjusted to counter the offset voltage and divide the bias current equally ($I_{d(M1)} = I_{d(M2)}$). Depending on the input voltage and SAR algorithm, the preamp may be in either the balanced or unbalanced state. The balanced/unbalanced terminology is not to be confused with device mismatch.

The remaining gain parameters are plotted in Fig. 5.8b. This plot contains both simulated and calculated values using (5.2.14)-(5.2.16). While A_{cm} is insensitive to mismatch both A_{dm-cm} and A_{cm-dm} increase in a somewhat linear fashion. Thus, designs with intentional device mismatch pose additional challenges compared to the matched case where these terms tend to zero. Fig. 5.9 is a plot of the rejection ratios according to formulas (5.2.11)-(5.2.13) and expressed in dB.

Recall that the gain parameters were derived assuming a small signal model. Simulations indicate that the rejection ratios are fairly constant up to the 3 db compression point, that is the input amplitude where the small signal gain A_{dm} is 3 dB lower. For input amplitudes up to the 3 dB compression point the CMRR, DCR and CDRR degrade on the order of 1 to 3 dB. Beyond the compression point the further degradation is observed.

The simulated and calculated (5.2.23) input referred offsets are plotted in Fig. 5.10. The formula derived from the DC analysis using the square law formula tends to underestimate the simulation results based on the more accurate BSIM model. The preamp array is designed to provide 30mV steps over a range of ± 120 mV. This represents the largest offset adjustment in the COP ADC.

The simulated balanced and unbalanced input referred noise results are plotted in Fig. 5.11 for both the 50 MHz and 25 MHz comparator clock frequency. The frequency will depend on the control system selection and DPWM oversampling ratio which will either be $16 \cdot 64 \cdot 44.1$ kHz = 45.16 MHz or $16 \cdot 32 \cdot 44.1$ kHz = 22.58 MHz respectively. The chosen 50 MHz and 25 MHz frequencies are rounded values convenient for subsequent simulations which include the clocked comparator. The continuous time preamplifier does not require a clock, the clock frequency simply sets the noise bandwidth of interest. Therefore, the noise is either integrated from DC to 25 or 12.5 MHz accordingly.

Assuming a white spectral noise density, the integrated RMS noise would be reduced by a factor of $\sqrt{2}$ or approximately 30% for a bandwidth reduction of 50%. In Fig. 5.11 for the matched

Figure 5.8: Preamplifier simulated and calculated a) differential gain A_{dm} , b) rejection ratios for the preamplifier array.

Figure 5.9: Preamplifier simulated and calculated normalized rejection ratios.

diff pair (preamp setting=0), the noise reduction is 17.5%. The limited noise reduction is due to low frequency flicker noise. Flicker noise accounts for 50% and 60% of the total noise in the 50 MHz and 25 MHz simulations respectively. To reduce the flicker noise a pfet preamp should be used. For high resolution low sampling rate applications, pfet preamplifiers are preferred. For high sample rate low resolution applications in which the thermal noise dominates nfets are preferred.

5.2.3 Comparator

The comparator of Fig. 5.12, compares the input voltage v_{in} to a reference v_{ref} and generates an output v_{out} . If $v_{in} > v_{ref}$ then $v_{out} = 1$ otherwise $v_{out} = 0$. The reference voltage can be fixed or variable depending on the application. A fixed reference voltage can be generated from a simple resistive divider while a DAC can be used as a variable reference.

The SAR algorithm requires a variable reference. Rather than using a DAC to generate reference voltages, deliberate mismatches can be introduced to create high resolution programmable offsets while lowering power consumption.

Figure 5.10: Preamplifier simulated and calculated input referred offsets.

Figure 5.11: Preamplifier simulated input referred noise.

Figure 5.12: Comparator with variable and fixed reference voltages.

Latched Comparator

One particular comparator architecture or latch type voltage sense amplifier as it is also referred to [2], is shown in Fig. 5.13 along with corresponding device sizes in Table 5.3. It features a differential input pair (M1,2) feeding a current into a pair of inverters (M3,4 and M5,6) in a positive feedback configuration. In this manner a large gain is created and any small difference at the input of M1,2 is rapidly amplified to full logic levels at the output. The sense amplifier is used in several digital applications which are summarized in [78]. Often it is used in input/output circuits as a low power alternative to rail-to-rail logic.

The transient response of the comparator output nodes are sketched in Fig. 5.14. The clk signal controls the operating modes. When clk is low the comparator is in reset mode and when its high the comparator is in the comparison or evaluation mode. When clk is low transistors M7-M10 are switched on and nodes X_1 , X_2 , V_{o1} and V_{o2} are pulled high. Nodes X_1 and X_2 are charged according to the time constant $R_{on}C_{X_{1,2}}$ where R_{on} is the on resistance of M7 or M10 and C_{X_1} , C_{X_2} represent the total parasitic capacitive loading at X_1 , X_2 respectively. During reset, the comparator core is inactive, its memory is cleared and it draws virtually no current from the

Table 5.3: Latched comparator device sizes.

Parameter	M1 (μm)	M2 (μm)	M3,5 (μm)	M4,6 (μm)	M7-10 (μm)	M11 (μm)
W	51	51	10	22.5	10	5
L	0.14	0.14	0.14	0.14	0.12	0.14

Figure 5.13: Latch type voltage sense amplifier [2].

supply. When clk goes high the comparator senses the differential input $V_{i1} - V_{i2}$ and the output is set accordingly to full logic levels by the positive feedback configured pair of inverters (M3,4 and M5,6).

The non-linear behavior of the latch comparator results in the transistors operating in different regions. During the comparison mode, its possible for the transistors to operate in, or transition from, the subthreshold, triode or saturation regions. As a result, the small signal parameters are continuously varying. Therefore, it is convenient to linearize the circuit during different phases of operation where the small signal parameters are assumed to be constant. The phase transition is considered to be instantaneous, however precise definitions of the edges is unknown and must therefore be approximated [79].

The comparison mode can be divided into three phases. Phase 1 commences upon the rising edge of clk , M1 and M2 are in saturation and the cross coupled inverters are inactive. Nodes X_1 , X_2 and output nodes V_{o1} and V_{o2} are pulled high from the reset mode. Any voltage difference between V_{i1} and V_{i2} causes an imbalance in the drain currents of M1 and M2. As a result, nodes X_1 and X_2 discharge at different rates.

Figure 5.14: Transient response of the output nodes during reset and compare clock phases.

Phase 2 occurs when either X_1 or X_2 discharges to $V_{cc} - V_{Tn3,5}$, where $V_{Tn3,5}$ is the threshold voltage of M3 or M5 which, as an approximation, are considered equal. Now M1, M2, M3 and M5 are in saturation. At this point M3,5 start to conduct and generate a voltage difference at the output V_{o1} and V_{o2} . Nodes $X_{1,2}$ continue to discharge towards zero volts and nodes V_{o1} , V_{o2} discharge towards $V_{cc} - |V_{Tp4,6}|$.

In phase 3 only the cross coupled inverters are active as the positive feedback rapidly amplifies the initial differential input voltage to full logic levels. Here M1,2 are no longer in saturation as the node voltages X_1 and X_2 tend to zero. As a result M1 and M2 exert no further influence on the decision process. Subsequently, the output reaches a steady state condition with complimentary output logic levels and no further current is drawn from the supply.

Offset Configuration

One of the design challenges of the sense amplifier or comparator as it shall be referred to, is contending with the inevitable device mismatches which shift the comparator tripping point. This

shift is known as an offset voltage. Given a mismatch between M1 and M2, the drain voltages will exhibit different slew rates due to current imbalance, hence an offset is created. One method to null the offset is to capacitively load the drains of M1,2 to counter the current imbalance. This technique was first used in [80] where up to $\pm 120\text{mV}$ of offset in 8mV steps was achieved. Moreover, the trimming capacitors were uniquely implemented using 4-bit binary weighted PMOS devices as parasitic capacitors on the drains of M1,2.

Rather than trying to null the offset, subsequent research exploited the mismatch effect in ADC designs. A n -bit flash ADC consists of 2^n comparators each of which requires a unique reference voltage. The core of a 4b 1.25GS/s flash ADC [81] consists of 15 comparators each with intentionally mismatched input pairs. These mismatches eliminate the need for a resistor ladder network. Furthermore, each comparator is calibrated to within $1/4$ LSB using the binary weighted PMOS trimming capacitor technique adapted from [80]. With a $200\text{mV}_{\text{pp-diff}}$ input range each offset is 12.5mV and can be calibrated to within 3mV with the 16 binary weighted PMOS trimming capacitors.

The SAR algorithm compares the input to a DAC generated reference voltage multiple times. Each time the DAC voltage is adjusted up or down in a binary weighted fashion depending on the comparator output. Here, the DAC has been replaced by reference “voltages” that are programmable precision offsets. These offsets are created by two methods. The first method is to intentionally mismatch the input pair M1,2 by a factor ΔW [81], [82]. This will create an imbalance in drain currents of M1 and M2 at the onset of the comparison cycle. From (5.2.28), assuming that both devices have the same gate length and threshold voltage, the input referred offset with mismatch $\Delta W = W_1 - W_2$ is approximately,

$$\Delta V_{\text{off}} = \frac{\Delta W}{W} \frac{V_{gs} - V_t}{2}. \quad (5.2.32)$$

Furthermore, multiple mismatched differential pairs can be connected in parallel and individually enabled. In this manner, a sequence of linearly spaced offsets can be obtained. The array consists of a matched differential pair, two pairs for positive offsets and two pairs for negative offsets. The device dimensions are specified in Table 5.4.

The second method is to vary the capacitive load C_{var} tied to the drains M1,2 [80]. The difference $\Delta C = (C_{\text{var},M1} - C_{\text{var},M2})$ must be compensated $\Delta I = (I_{M1} - I_{M2})$ during the initial slewing of the comparison phase. This is a useful technique for fine tuning the offset according

Table 5.4: Comparator mismatched device sizes.

Setting	M1 (μm)	M2 (μm)
-2	21	81
-1	33	69
0	51	51
1	69	33
2	81	21

to:

$$\Delta V_{off} = \frac{\Delta C}{C_{tot}} \frac{V_{gs} - V_t}{2} \quad (5.2.33)$$

where $C_{tot} = (C_{var,M1} + C_{var,M2})/2$. Fig. 5.15a is a diagram of the comparator complete with tuning capacitors and reset transistors M7-M10.

To summarize, the use of the dynamic latched comparator has evolved and been adapted over time to various applications. The initial application was as a low power sense amplifier to eliminate the transmission and reception of rail to rail logic [2], [78], [80]. Adoption into various ADC architectures with 4-9b resolution soon follow such as flash ADCs [81], [82] and charge sharing SARs [75], [74]. None of these techniques dynamically adjusts the offset during the ADC operation. Rather the comparator offset is calibrated and fixed during ADC operation. In the COP ADC [9] approach, the offset is dynamically adjusted during each conversion cycle (16 times for 16 bits). The only other known SAR ADC with a similar approach is the Threshold Configurable TC-ADC [8] with a resolution of 6b. Threshold or offset configuration are conceptually the same, the difference being only in terminology. What distinguishes the approach taken here is the threshold/offset implementation technique for 16b precision. A unique approach is required to achieve 16b versus 6b resolution.

While previous literature has focused on binary weighted arrays of PMOS capacitor banks for moderate resolutions on the order of 4-9b, the current application requires higher 16b precision. As a result a new approach is required to generate finer offsets. In Fig. 5.15 there are 3 offset methods: mismatches in the diff pair ΔW , mismatches in C_{var} binary weighted array by factor w and C_{var} delta array by factor dw . The dual array of binary weighted and delta tuning devices in Fig. 5.15b is the key to precision offset control. While the binary weighted device widths are scaled by a $2 \times w$ ratio (course tuning), the delta array adjusts the width incrementally by

dw (fine tuning). The capacitance loading is set as follows. When zero volts is applied to the gate the device is active and the intrinsic gate capacitance is added to the node. When V_{cc} is applied, the device is off and only the extrinsic parasitic capacitance exists [83]. In this manner, the capacitive loading and in turn the offsets can be precisely controlled.

For $V_{cc}=1.2V$ and the load driven differentially by two switching stages the maximum output swing is $2.4V_{pp}$ differential. Therefore, for 16b resolution the lsb value is $2.4/2^{16} = 36.6\mu V$ differential. Calibration requires tuning of less than 1/2 LSB. To achieve this resolution requires both course and fine tuning PMOS arrays of PMOS devices. Five binary weighted PMOS devices yield a course tuning resolution of $\pm 316\mu V$. Fine tuning to $16\mu V$ resolution is obtained by switching in one of the fine tuning caps with $w=5\mu m$, $L=0.5\mu m$ and $dw=100nm$. Fig. 5.16 is a plot of the input referred offset for four course (binary weighted) and fine adjustments ($dw=100nm$). This data was generated based on a schematic simulation which does not take into account parasitics associated with layout extraction. The digital circuitry setting the gate voltages on PMOS devices was modelled in verilogA code rather than actual gates.

The comparator power consumption was simulated while being clocked at 50 MHz. The transient current was integrated and averaged over time to determine the average power. The peak current is approximately 5.2mA but only for a very short time as the regenerative time constant is $<1ns$. As a result the average current turns out to be $100\mu A$ or $120\mu W$. The comparator power is an order of magnitude less than the preamplifier.

Comparator Noise

The comparator noise performance is a limiting factor in the ADC design. For high resolution applications a preamplifier is required to reduce the input referred noise at the expense of increased power consumption. An analytical model of the thermal noise [79] provides insight to the design process. While the analysis provides guidance to the designer, ultimately the final design remains largely an iterative procedure since factors such as device mismatch and flicker noise are unaccounted for. Hence, optimization of noise performance remains largely an iterative and tedious design procedure.

The comparator was simulated with Cadence PSS/Pnoise with a 1 MHz input tone and 25 or 50 MHz clock with 300 harmonics of the 1 MHz beat frequency. The total noise was calculated by numerical integration of the input referred noise from 1k to 12.5 or 25 MHz. The simulation results are plotted in Fig. 5.17 where the noise is reduced from 72 to $57\mu V_{rms}$ when the sampling

Figure 5.16: Example of combined course and fine PMOS comparator offset tuning simulation (Course is swept from 0 to 4w, fine is -15dw to + 15dw).

is reduced from 50 to 25 MHz. When preceded by a preamplifier the cascaded input referred noise is reduced by the amplifier voltage gain.

5.3 Cascaded Performance

The ADC design goal of 16b resolution at a sample rate of 2.82 MHz with approximately 5mW power constraint is very aggressive. The proposed preamp and latched comparator architecture held promise of possible solution however, significant limiting factors were encountered during the design process. Factors such as limited tuning range, degraded noise rejection due to mismatches and the need for increased power to reduce noise.

5.3.1 Tuning Range

The functional input voltage range is the tuning range. The tuning range V_{tune} and number of bits n set the lsb according to $V_{\text{tune}}/2^n$. For a specified resolution of n bits, V_{tune} and the lsb are linearly related. Increasing V_{tune} relaxes the noise specification which is a fraction of a lsb. Therefore, it is desirable to maximize V_{tune} to the fullest extent possible.

Figure 5.17: Integrated input referred comparator noise.

V_{tune} is determined by superposition of offsets using the methods explained perviously. The maximum V_{tune} is limited by two practical design constraints. Firstly, increased mismatches leads to degraded CMRR, CDRR and DCRR parameters. This implies an inherent increase in susceptibility to external noise sources. Secondly, very large mismatches can lead to device sizes which are not feasible nor practical.

The input referred offset can be tuned to $16 \mu V$ resolution for an input of 280mV peak to peak differential. This is accomplished by superposition of the preamp, comparator differential input pair, binary weighted and delta tuning cap offsets. This yields 14.5b of resolution.

5.3.2 Cascaded Noise

The noise performance of the preamp and comparator have been characterized individually, therefore the next step is to determine the cascaded performance. The cascaded input referred noise can be calculated from the individual noise contributors. Consider Fig. 5.18 where G is the differential mode voltage gain of the preamplifier, $v_{in_p}^2$ and $v_{in_c}^2$ are the integrated input referred noise of the preamplifier and comparator respectively. The total input referred noise can be calculated from each contributor [84] as,

$$v_{in_{tot}} = \sqrt{v_{in_p}^2 + \frac{v_{in_c}^2}{G^2}} \quad (5.3.1)$$

where $v_{in_{tot}}$ is the RMS input referred noise voltage. The simulated cascaded noise plots for both sample rates are shown in Fig. 5.19. The noise was numerically integrated up to half the sample rate with no comparator mismatch.

At the onset, the design goal was to achieve an input referred noise which is a fraction of a lsb. The noise should be on the order of 1/2 to 1/6lsb. The former tending to be error prone and the latter requiring significant power increase. Assuming a full swing of $2.4V_{pp}$ the lsb is $36.6 \mu V$ so the input referred noise should be in the range of 6.1 to $18.3 \mu V$. The initial design did not anticipate the increased noise due to mismatch nor limited tuning range, thus in Fig. 5.19 for 50 MHz and preamp=0 the noise $14.5 \mu V$ result was deemed acceptable. Subsequently, increased noise due to mismatch and limited tuning range effectively required re-design to reduce the system noise further. Due to time constraints in the fabrication schedule, the decision was made to proceed with the current design.

A potentially significant noise reduction is possible with a comparator modification. The thermal noise contribution of some of the devices, including M1 and M2 in Fig. 5.15 are proportional to kT/C_x [79]. C_x is the total capacitance on the drain nodes of M1 or M2 determined from $C_x = C_{var} + C_p$ where C_p includes the layout and device parasitic capacitances. Thus, adding extra capacitance C_{extra} to C_x will reduce the noise. The tradeoff in doing so is to slow down the discharge or slewing rate during the comparison mode and also an increase in power. In Fig. 5.20 the cascaded noise reduction for $C_{extra}=2pF$ yields a relative noise reduction of $5.5 \mu V$ and current increase of $240\mu A$. Even with the extra 2pF loading the comparator decision is made well within the 10 ns window. Increasing C_{extra} above 2 pF yields diminishing returns. Note that changing the loading on C_x requires redesign of PMOS arrays comprising C_{var} . In addition, the time the RC time constant during reset will increase. As with the preamplifier the comparator could also be implemented in PMOS to reduce 1/f noise.

Figure 5.18: Cascaded noise block diagram.

Figure 5.19: Integrated input referred cascaded preamp and comparator noise.

Figure 5.20: Cascaded noise reduction for 50 MHz sample rate and corresponding comparator current increase.

5.4 Key Points

This chapter began with an introduction to the general SAR algorithm which require a n-bit DAC. To eliminate the DAC, the COP ADC topology was introduced, analyzed and partially implemented in the IBM 0.13 μm process. The only other comparable design is the 6b TC-ADC [8] developed in parallel to this work.

The core of the COP ADC is the preamp array and latched comparator. Each of which was analyzed and simulated individually and then cascaded. The key points of this chapter are:

- The COP ADC uses four offset tuning techniques. These are preamp mismatch, comparator mismatch, binary weighted capacitor bank and delta capacitor banks.
- The tuning range using superposition of the four offset methods is 280 mV with a resolution of 16 μV peak to peak differential.
- The preamp array provides signal gain and offset adjustment while reducing the input referred noise of the comparator.
- Mismatched preamplifiers suffer from reduced noise rejection CMRR, DCRR and DCRR. Analytical expressions have been derived for all gain parameters and rejection ratios. These expressions were verified with simulations.
- The dynamically latched comparator uses a unique combination of PMOS devices to precisely control the offset. In one of the arrays the width w is binary weighted while the other

array introduces a delta change $w+dw$.

- For lower $1/f$ noise the preamp and comparator should be designed with PMOS transistors.
- for low frequency operation the resolution is $280\text{mV}/16\mu\text{V}=17,500$ or 14.1b. The worst case noise performance is $21\mu\text{V}$ from Fig. 5.19. Assuming a noise allowance of $1/2\text{lsb}$ the resolution at 50MHz would be $280\text{mV}/42\mu\text{V}=19,048$ or 12.7b.
- At the expense of a slight increase in power, an extra fixed capacitive load $C_{extra}=2\text{pF}$ will reduce the cascaded noise by $5\mu\text{V}$. The binary and delta weighted capacitive arrays would have to be redesigned in this case.

Chapter 6

ADC Test and Measurements

Custom hardware and software for an automated measurement platform was developed for testing the COP ADC. Two platforms were developed for both DC and AC characterization. Offset measurements are presented and compared to simulation results. Due to hysteresis and noise limitations a fully functional ADC could not be tested.

The chapter concludes with a comparison table of recently published digital input Class D amplifiers and a list of key points.

6.1 Integrated Circuit Overview

The Integrated Circuit (IC) block diagram with pinout is shown in Fig. 6.1. The IC was fabricated in the IBM CMRF8SF 0.13 μm CMOS process and wire bonded in a CFP-24 surface mount package. The analog and digital sections have separate supplies and corresponding ground pins. Test points provide both input and output access to the internal nodes between the preamplifiers and comparator. These pins are controlled by active high logic applied to the control pins 14 and 15. The TPOUT pins are buffered internally with a pair of source followers capable of driving 50 Ω loads with minimal attenuation. The TPIN pins are connected to the internal nodes via transmission gates. Table 6.1 includes a list of the pins with brief descriptions.

6.2 Digital Interface

The PC digital interface consists of six data pins D(5:0), three clock pins (CLK_COMP, CLK_REG and CLK_DATA) and two active high enable pins (ENTP_OUT and ENTP_OUT) for the test

Figure 6.1: Integrated circuit block diagram and pinout.

Table 6.1: Pinout with description.

Pin	Reference	Type	Description
1	OUTP	Digital	Comparator output (P)
2	OUTN	Digital	Comparator output (N)
3	CLK_COMP	Digital	Comparator clock
4	CLK_REG	Digital	Clock to load 24b config register
5	CLK_DATA	Digital	Clock to load DIN(5:0) data
6	DGND	Power	Digital supply ground
7	D(5)	Digital	Config register CR(23:20)
8	D(4)	Digital	Config register CR(19:16)
9	D(3)	Digital	Config register CR(15:12)
10	D(2)	Digital	Config register CR(11:8)
11	D(1)	Digital	Config register CR(7:4)
12	D(0)	Digital	Config register CR(3:0)
13	VCCD	Power	Digital Supply
14	ENTP_OUT	Digital	Enable buffered output test points
15	ENTP_IN	Digital	Enable input test points
16	TPIN_P	Analog	Test point input (P)
17	TPIN_N	Analog	Test point input (N)
18	TPOUT_P	Analog	Test point output (P)
19	TPOUT_N	Analog	Test point output (N)
20	VIN_P	Analog	Preamplifier input (P)
21	VIN_N	Analog	Preamplifier input (N)
22	VCC	Power	Analog Supply
23	BIAS	Analog	Bias reference voltage
24	VSS	Power	Analog ground

Table 6.2: Config register settings for programmable offsets.

Parameter	Register	No. of settings	Decimal Settings
Preamplifier select	CR(23:20)	9	1 to 9
Comparator Diff Pair select	CR(19:15)	5	1,2,4,8,16
Comparator binary weighted PFETs (neg)	CR(14:10)	32	0 to 31
Comparator binary weighted PFETs (pos)	CR(9:5)	32	0 to 31
Comparator Delta PFETs	CR(4:0)	32	0 to 31

Figure 6.2: Digital interface timing diagram.

points. All digital circuitry operates on an independent 1.2V DC supply.

The four different offset options are configured with a 24b register CR(23:0). Table 6.2 lists the parameters and associated control bits. The data must be parsed into into 6 nibbles for loading on the data pins D(5:0). This reduces the clock frequency by a factor of six compared to loading the data in a serial manner.

The data is loaded according to the timing diagram of Fig. 6.2. All clock signals are derived from the master clock, CLK_REF. With 6 data lines D(5:0), 24 bits are clocked in after the fourth falling edges of CLK_DATA. Subsequently, the config register is loaded on the falling edge of CLK_REG. At this point the IC is ready for comparator operation, upon assertion of the following CLK_COMP pulse.

6.3 Measurement System

There are two fully automated DC and AC measurement systems. Each system is explained in this section along with measurement results. In addition, the custom designed two layer FR4 test PCB with 2oz copper and thickness of 0.062 inches is described.

6.3.1 Printed Circuit Board

Testing was facilitated by way of a custom designed two layer Printed Circuit Board (PCB) shown in Fig. 6.3. The PCB schematic and layout are included in Appendix B. The PCB has the following features.

- Separate analog and digital power supplies and ground planes
- Buffered 1.2V to 3.3V level shifters for comparator OUTP,N (pins 1,2)
- Differential to single ended low noise opamp circuit for TPOUT_P,N (pins 18,19)
- Single ended balun or differential input to TPIN_P,N (pins 16,17)
- Header jumpers for ENTP_OUT and ENTP_IN enable (pins 14,15).
- Multiple VIN_P,N (pins 20,21) connection options including, differential, single ended with balun and single ended with balun and sample and hold.

Figure 6.3: Populated PCB for DC and AC measurements.

6.3.2 Automated Testing

The testing was completed in two phases. In the first phase, DC measurements were obtained from an automated General Purpose Interface Bus (GPIB) based system. Subsequently, AC measurements were completed using an Altera DE2 FPGA as the controller.

DC Measurements

The DC measurement system of Fig. 6.4 consists of a computer, logic analyzer and source meter. The computer requires MATLAB with GPIB toolbox to control the Keithley 2600 source meter and HP16500C logic analyzer. In this arrangement the digital interface is handled by the logic analyzer. This includes generating all required clock and data signals to configure the DUT CR(23:0) register. In addition, the logic analyzer captures the DUT (comparator) output bits.

Figure 6.4: DC Automated measurement system.

The logic analyzer to DUT interface consists of six bits for data and three for clocks with timing as per Fig. 6.2. The dual channel Keithley source meter generates the DUT DC input with a programmable resolution of $2\mu V_{pp}$ differential.

The DC measurement procedure is as follows. Program the CR(23:0) config register for the desired offset and then step the source meter voltage repeatedly until the comparator changes state. Each time the voltage is changed a delay is added to ensure the source meter has settled to the new voltage. The source meter voltage at which point the comparator changes state is the input referred voltage offset. The DUT is characterized by repeating this process for other settings.

AC Measurements

Unlike the DC measurement system, the AC measurement system sweeps the DUT input voltage at a specified frequency. This is a more realistic model of performance where transient affects are taking into account. This is best implemented with a FPGA such as the Altera DE2. Fig. 6.5 is a block diagram of the AC test system in which the FPGA controls all aspects of testing and data acquisition. The reference clock frequency (CLK_REF) is obtained from the FPGA 50 MHz reference oscillator. The DUT differential input voltage is derived from an Analog Devices AD768 16b 30Msps DAC. A low noise differential opamp (OP8139) is required to scale the DAC voltage and set the common mode voltage to $V_{cc}/2$. Scaling the DAC output is required to ensure 1/2 LSB DNL and 1 LSB INL. This occurs when the OP8139 maximum output is $340mV_{pp}$ differential with 14b resolution ($20\mu V$ LSB).

Figure 6.5: AC Automated measurement system.

6.4 Measurement Results

The measurement results for both the DC and AC test setups will be presented. In the DC measurements each family of offsets is measured independently. The data is then numerically superimposed to determine the overall tuning range and resolution. The superposition principle is verified in the AC measurements where all offset combinations can be measured directly. The AC measurements also account for transient effects.

6.4.1 DC Measurements

With the measurement system of Fig. 6.4 the offsets were measured for each of the four offset configurations. With GPIB controlled instruments delays are introduced to allow for instrument settling time. The logic analyzer is configured with a CLK_REF of 50 MHz from which all clock and data waveforms are synchronized. The measured and simulated (layout extracted) offsets are presented in Figs. 6.6a-d. The non-linearity in Figs. 6.6a,b is due to the on-chip interconnect and R_{on} impedance of the digital control devices. This problem can be corrected by inserting an appropriately sized pair of inverter buffers (one in the digital section and one in the analog section) to provide a low impedance ground at the gates of the PMOS devices.

The binary weighted data of Fig. 6.6b can be shifted up or down to create a family of traces. This is possible since there is independent control of the PMOS positive and negative arrays as per registers CR(14:10) and CR(9:5) in Table 6.2. This is not possible for the delta case since the arrays share common control lines.

Table 6.3 was calculated by curve fitting the measurements to a linear first order polynomial.

Table 6.3: DC Measured input referred offset resolution and tuning range.

Offset Parameter	Resolution pk-pk diff (V)	RMS _e	No. Steps	Range
Delta caps	15.5uV	4.96μV	±15	±232.5uV
Binary weighted caps	316uV	131.5μV	±15	±4.74mV
Comparator diff pair	7.9mV	2.14mV	±2	±15.8mV
Preamp diff pair	29.85mV	3.07mV	±4	±119.4mV

The RMS error between the measured and simulated data is calculated from,

$$RMS_e = \sqrt{\frac{1}{n} \sum_{i=1}^n (V_{om,i} - V_{os,i})^2} \quad (6.4.1)$$

where V_{om} and V_{os} are the measured and simulated offsets, respectively.

The overall tuning range is obtained by superposition of the offset families. Sufficient overlap of the various tuning ranges is required to avoid missing codes. Strictly speaking, linear superposition of the offsets is an approximation due to slight gain variation across the preamplifier array. Complete characterization of the offsets is best suited to AC measurements. Simulations confirm that the offset variation is directly proportional to the gain variation in the preamp array. For mismatched preamps the gain is reduced according to Fig. 5.8a and as a result, the comparator input referred offset will increase proportionally.

The calculated tuning range based on the DC measurements is 282.6 mV. The resolution with no missing codes is 17.1uV which equates to 14b. The INL and DNL plots are given in Fig. 6.7.

To achieve the required 16b operation two improvements in the design are required. First, the tuning range needs to be increased and secondly, the cascaded noise needs to be reduced. These two changes pose significant risk and challenge. Increasing the tuning range requires extending the mismatch in the preamp and comparator. This will inevitably lead to an undesirable increase in A_{dm-cm} and A_{cm-dm} . Noise reduction comes at the expense of increased power consumption.

Hysteresis

While doing manual characterization and DC measurements hysteresis was observed. That is, the comparator exhibits a tendency to remain in its past state. Hysteresis is a memory effect that is usually associated with capacitor charge retention and/or feedback. This affect was not

Figure 6.6: Measured and extracted layout offset simulations. Voltages are input referred peak to peak differential.

Figure 6.7: INL and DNL plots normalized to LSB (LSB= $17.1\mu\text{V}$) based on superposition of DC measurements.

foreseen during the design phase since the comparator has a reset phase in which all relevant internal capacitances (offset capacitor arrays and positive feedback inverters) are pre-charged. Schematic simulations indicate no discernable hysteresis however, extracted layout simulations show approximately $50\text{-}75\mu\text{V}$. This amount is significantly less than measurements.

One possible cause of hysteresis in latched type comparators is due to the data dependent loading of the flip flop connected to the output of the comparator [80]. It is proposed that buffering the output of the comparator would result in virtually no hysteresis effect though this was not experimentally proven.

The hysteresis in [80] was in the range of $3\text{-}7\text{mV}$ while measurements for this design are on the order of $1\text{-}2\text{mV}$. To date, hysteresis has not been an issue for latched comparators since it is less than the resolution of interest. For example, for a 6b ADC with programmable latched comparator the LSB is 5mV [8], therefore hysteresis is of little consequence. For 14-16b resolution and LSBs on the order of microvolts it becomes a fundamental limitation.

Its possible that some feedback associated with the PCB is contributing to the hysteresis though this remains to be verified. One way to mitigate the hysteresis is to double the number of comparator operations. For a n -bit SAR there is usually n samples. If instead, there are $2n$ samples and every 2nd sample is used to clear the hysteresis. This can be accomplished by enabling the appropriate preamp to produce a DC offset that will clear the comparator hysteresis. Though technically feasible, it is a undesirable approach due to increased power consumption.

6.4.2 AC Measurements

The DAC AD768 and opamp OP8139 are configured for 14b operation over a range of 340mV_{pp} differential equating to a resolution of $20.75\mu\text{V}_{\text{pp}}$. The FPGA generates all timing waveforms and steps the DAC register in a linear fashion, generating a triangular waveform. For each period of the triangular waveform the DUT configuration register is fixed. Thus, the DUT offset is obtained directly from the DAC register at the comparator tripping point. The DAC register is stored in the FPGA SRAM for post processing. Measured waveforms for the DAC (triangular) and DUT (square wave) differential outputs are given in Fig. 6.8. Considering all register settings there are 1,474,560 possible combinations.

The FPGA timing is based on CLK_REF derived from the onboard 50 MHz oscillator. It is divided by eight to produce a CLK_REG frequency of 6.25 MHz which is the sample rate. Note

Figure 6.8: AC test waveforms including differential DAC and comparator output.

that CLK_REG and CLK_DAC are essentially the same where CLK_DAC is the clock for loading the DAC register.

After measuring the offsets the FPGA SRAM data is post processed in Matlab to determine the tuning range and resolution. The INL and DNL plots calculated from the measured data are plotted in Fig. 6.9. The maximum INL is 0.5 LSB and DNL 1 LSB. The tuning range was 293.33mV_{pp} differential with 14b resolution (LSB=20.75μV).

Table 6.4 summarizes the results for cycling the DUT through all offset combinations. The overall tuning range of 293.33 mV_{pp} differential is 3.8% greater than the DC tuning range of 282.6mV_{pp} with assumed superposition. This difference can partially be attributed to calibration and measurement error in the opamp gain. The AC results are important for two reasons. First, the superposition assumption of DC measurements is verified. Secondly, dynamic measurements at a sample rate of 6.25 MHz take into account transient effects though only at 1/8 the intended rate. For these test results we can calculate the ADC figure of merit as,

$$FOM = \frac{V_{cc}I}{f_s \cdot 2^{ENOB}} = \frac{1.2 \times 10^{-3} \cdot 1.25}{((6.25 \times 10^6)/14) \cdot 2^{13.8}} = 0.24 \text{ pJ/conversion.} \quad (6.4.2)$$

Offset superposition is critical with respect to automated testing in a commercial production environment. In this case, the goal would be to characterize the device using only a subset of

Figure 6.9: AC measured INL and DNL plots with $\text{LSB}=20.75\mu\text{V}$ at a sample rate of 6.25 MHz

Table 6.4: Measured input referred offset resolution and tuning range.

State	Range (mVpp)	LSB (uV)	No. of bits	Missing Codes	Max INL (LSBs)	Max DNL (LSBs)
DC	282.60	17.09	14.0	0	0.38	0.41
AC	293.33	20.75	13.8	0	0.50	1.00

measurements to reduce verification time. Whether or not this is practically feasible requires further analysis to determine total process and corner variation. Its possible further circuitry dedicated to calibration is necessary.

Using the AC measurement data an inferred SNR can be calculated for a sine input of 222.5 Hz, calculated from the 6.25 MHz frequency, resolution and maximum input amplitude. The calculated SNR was 84dB (14b) where the noise was integrated from DC to $f_s/2 = 3.125$ MHz.

Noise

The comparator input RMS noise determines the confidence level for reliable offset measurement. A noisy differential comparator is shown in Fig. 6.10. The digital output for a given input can be modelled as,

$$v_o = \text{sign}(V_{o2} - V_{o1}) = \frac{1 + \text{sign}(v_{din} - v_n)}{2} \quad (6.4.3)$$

where $v_{din} = V_{i1} - V_{i2}$ and v_n is the input noise voltage [79]. If the argument of the sign function is positive the output is 1 (V_{cc}) whereas it is 0 ($-V_{cc}$) for a negative argument. This model neglects any memory or hysteresis effects due to parasitic feedback in the IC or PCB. Assuming v_n is modelled as zero mean white Gaussian noise, then the probability of a high output as a function of v_{din} corresponds to the comparator output mean (expected value) and can be calculated as,

$$p(v_{din}) = \frac{1}{\sqrt{2\pi}\sigma_n} \int_{-\infty}^{+\infty} v_o \exp\left(-\frac{v_n^2}{2\sigma_n^2}\right) dv_n = \frac{1 + \text{erf}\left(\frac{v_{din}}{\sqrt{2}\sigma_n}\right)}{2} \quad (6.4.4)$$

where

Figure 6.10: Noisy differential comparator model.

$$\text{erf}(\alpha) = \frac{2}{\sqrt{\pi}} \int_0^{\alpha} e^{-x^2} dx \quad (6.4.5)$$

and σ_n is the standard deviation of the input noise v_n . Experimentally, the noise σ_n can be obtained from probability plots of the comparator output as a function of input voltage [79], [85].

Fig. 6.11 is a simplified single ended block diagram of the noise measurement setup. The source v_s , as in previous tests, is the DAC AD768 and opamp OP8139 combination. The input noise contribution of the source is σ_{ns} . The second noise source σ_{ni} , is the input referred noise of the “comparator”, the components within the dashed rectangle. Assuming the noise sources are uncorrelated, the total noise is calculated from,

$$\sigma_{ntot} = \sqrt{\sigma_{ns}^2 + \sigma_{ni}^2}. \quad (6.4.6)$$

The technique used is to apply a v_s ramp voltage and observe the output, v_{out} . Due to the presence of noise, the comparator threshold will vary. By repeating the measurement several times the probability of getting a high output can be plotted. Using this approach two sets of probability curves are plotted in Figs. 6.12, 6.13. Each curve was generated based on 512 measurements with comparator sampling at 1.25 MHz. The ramp voltage was a 38 Hz triangular waveform with 20.75 μV resolution.

The input noise can be extracted by curve fitting with equations (6.4.4), (6.4.5) or more simply by extracting the standard deviation using the 50% to 90% span of the input voltage [86]. Intuitively, the steeper the transition zone from low to high state, the lower the noise. Note that in these plots the offsets have been removed. In addition, we are effectively measuring σ_{ntot} rather than the desired σ_{ni} . To obtain σ_{ni} it must be de-embedded from (6.4.6) by either quantifying σ_{ns} . Alternative methods include both open [87] and closed [85] loop methods. These approaches can provide more accurate results but do not eliminate the source noise contribution.

Table 6.5 lists the noise values extracted from the measurement results. The noise increases

Table 6.5: Noise measurements.

State	Input Noise σ_{ntot} (μV_{rms})
Preamp0	89.9
Preamp1	79.8
Preamp2	84.8
Preamp3	92.4
Preamp4	107.7
CDP0	88.2
CDP1	100.9
CDP2	119.9

Figure 6.11: Input noise associated with the source and cascaded preamp and comparator.

with increasing device mismatch. This is to be expected given the simulation results presented in Chapter 5. In addition, when mismatch is introduced to generate an offset the CMRR, DCRR and CDRR parameters are degraded. Therefore, source noise is more likely to affect performance. There is an anomaly in that Preamp0 noise values are higher than that of Preamp1,2. This could be due to measurement error and would require re-testing to confirm.

Some test system modifications to reduce the source noise include,

- Repeating the measurement using the Keithley source meter and GPIB control.
- Replacing the DAC AD768 with a lower noise, higher resolution DAC.
- Reconfiguring the measurement system for closed loop operation [85].

Figure 6.12: Measured probability of a high output as a function of input voltage for different preamp settings.

Figure 6.13: Measured probability of a high output as a function of input voltage for different comparator diff pair settings.

6.5 Comparison Table

Table 6.6 is a summary of recent publications related to digital input Category III-V Class D amplifiers. Analog input Category I-II Class D amplifiers are not included as they require an external DAC for a complete solution. The reader is referred to [39, 55] for analog input comparison tables. All power consumption values are for single channel operation. The performance values for the parameters are explained in the following sections.

Most of the listed publications are for higher power applications (>400 mW) such as hands free speakers in handsets or tablet/laptop speakers. In these cases the overall efficiency is better than lower output applications. This can partly be attributed to the overhead associated with the quiescent power.

6.5.1 Quiescent Power Estimate

The total power consumption of the system will include switching losses of the power stage, COP ADC and digital circuitry. The digital circuitry power consumption can be estimated from,

$$P_d = \frac{1}{2} f C_t V_{cc}^2 \quad (6.5.1)$$

where f is the clock frequency, C_t is the total capacitance and it is assumed that on average 50% of the gates are active. C_t can be estimated by first obtaining the equivalent number two input nand gates for each digital circuit and multiplying by the input capacitance. For the interpolation filters, loop filter, DPWM and clock divider circuits $P_d = 52\mu\text{W}$.

During normal operation the Class D PA will incur both switching and conduction losses. In the quiescent case it is assumed that there is no load or zero output power. In this case there are switching but no conduction losses.

For a differential bridge tied load configuration as given in Sec. 4.5.3 the switching losses are $2 \times 77 = 154\mu\text{W}$. The core of the COP ADC consisting of the preamp and comparator dissipates 1.5 mW of power. The estimated quiescent power per channel is 1.706 mW.

Table 6.6: Published specifications for digital input Class D audio amplifiers. All power specifications are for single channel mono operation.

Parameter		[49]	[50]	[51]	[53]	[57]	[31]	[55]	[88]	Linear [89]	[6]	This work
Category	I-V	III	III	III	IV	IV	IV	IV	IV	IV	V	V
Analog	(V)	2.5	3.0	5.0	5.0	4.8	5.0	5.0	5.0	1.8	25	1.2
Digital	(V)	1.2	1.2	1.2	5.0	1.2	1.8	1.8	1.8	1.8	FPGA	1.2
Max POUT	(mW)	12.5	400	1000	1000	330	1000	3400	2400	15	15000	10
Max efficiency	(%)	80	88	81	70	84	92	90	86	36.5	-	80.3
THD+N	(%)	0.1	1	0.2	0.1	-	1	10	1	0.03	0.001	-
PSRR @217 Hz	(dB)	-	-	64	90	90	80	85	85	105	-	78
SNR A-weighted	(dB)	103	92	104	-	93	92	-	96	91	-	84
Dynamic Range	(dB)	96	120	104	83	-	92	103	-	-	-	-
Quiescent Power	(mW)	1.3	6.48	8.3	-	-	-	7.6	10.4	6.8	-	1.71
Process		65nm	65nm	0.13 μ m	0.5 μ m	90nm	0.14 μ m	0.14 μ m	-	BiCMOS	PCB	0.13 μ m

6.5.2 Maximum System Efficiency

The maximum collector efficiency can be determined by extension of the quiescent power to account for additional conduction losses incurred at maximum output power. Note that the efficiency to be calculated includes all system components, not just the PA efficiency as is sometimes reported.

Applying equation (4.5.7) and assuming a bridge tied load with $R_l = 32\Omega$ and $R_{on} = 1.2\Omega$, the conduction loss $P_c = 0.75$ mW for an output power 10 mW. The switching losses have been accounted for in the quiescent power calculations, therefore only the conduction losses need to be added. The peak efficiency which occurs at maximum output power is $\eta_c = 10/(1.706 + 10.75) = 80.3\%$.

6.5.3 Other Parameters

The noise rejection at 217 Hz is based on the sum of two values. A common mode rejection of 30 dB is assumed for the differential bridge tied load and another 48 dB from feedback (Fig. 4.14). This is sufficient for direct battery connection in GSM handsets.

The listed SNR of 84dB is the theoretical limit for a 14b ADC and has been verified in simulink. The dynamic range and THD+N values are not specified since a fully functional mixed signal simulation of the entire system was not completed.

6.6 Key Points

In this chapter the AC and DC automated test setup was presented including details of the custom designed verification PCB. The details of the digital and analog IC interface were provided along with a pinout table and timing diagrams.

AC measurements were completed after DC measurements with the results being well correlated. The AC measurements could be significantly improved with a higher resolution 18b DAC and ideally eliminating the opamp buffer to keep noise to a minimum. Ideally the measurements should be limited by the noise of the DUT and not the source.

Measurement results indicated hysteresis which is not accounted for in simulations. This imposes a limitation on the COP ADC resolution in which full 14b resolution can not be obtained

directly. Hysteresis and source noise are two limiting factors in completely characterizing the COP ADC.

Other key points from this chapter are:

- The DC measurement system was based on GPIB instrument control. Automated testing software was written in Matlab.
- The AC measurement system was based on an FPGA controller. Automated testing software was written in Verilog.
- The 1x2mm die was bonded to a 24 pin surface mount package and soldered to the test PCB.
- The input voltage operating range and resolution for the AC and DC measurements were similar. Approximately 280 mV with 14b resolution and no missing codes. The AC sample rate was 6.25 MHz which is 1/8 the required frequency.
- The DC measurements measured each set of offsets and then applied superposition to predict the tuning range. The AC measurements verified this assumption by measuring all offset combinations.
- Noise measurements are higher than simulated but include noise from the source. An alternate measurement approach is required to measure the preamp and comparator noise. This can include using a lower noise/higher resolution DAC, switching to a GPIB measurement system or using a closed loop measurement system [85]. Worst case $\sigma_{ntot}=120 \mu\text{Vrms}$.
- Noise σ_{ntot} increases as the degree of device mismatch increases. This is due to increased thermal noise and degraded noise rejection ratio performance.
- There was significantly more hysteresis in the measurements than simulations. Schematic simulations do not reveal hysteresis but extracted simulations show a small amount on the order of 50-75 μV .
- One way to mitigate the hysteresis is to double the number of samples in the SAR algorithm to clear the memory effect. The tradeoff being either reduced conversion speed or increased power if the clock frequency is doubled.
- Since the COP ADC was not fully functional it could not replace the commercial ADC (AD7621) in the FPGA system verification test platform.

Chapter 7

Conclusions

At the onset of this research the goal was to design a low power switching mode Class D amplifier that is scalable. The system specifications were chosen to be comparable with current commercial products. While no immediate benefits would be obtained, the architecture would have the advantage rapid porting to new processes with minimal redesign and faster time to market.

Significant progress towards achieving the initial goals has been made though considerable challenges remain. While a predominately digital system with global feedback was demonstrated the ADC power consumption remains a significant obstacle. Furthermore, system analysis indicates that the shaped quantization noise associated with $\Sigma\Delta$ ADCs is problematic in closed loop operation. This limits the designers options in selecting an ADC architecture.

To meet the system requirements the design of a low power ADC was undertaken which led to the so called COP ADC. The ADC required 16b resolution at 2.82MSPs and maximum power of 5mW. The COP ADC was designed in a 0.13 μ m IBM process and tested on custom designed automated platform. While the concept of the COP ADC architecture was validated, full functionality according to specifications was not met. Limited tuning range, noise and hysteresis are issues that require further research and development. Despite these limitations significant advancement in the design and analysis of an alternate low power ADC architecture was made. Measurement results from both the AC and DC tests were well correlated. An operating range of 293mV with 13.8b resolution with 6.25MHz clock was achieved. The maximum INL=0.5 LSB, DNL=1 LSB and a figure of merit of 0.24pJ/conversion.

The COP ADC design implemented various unique design concepts. In particular, the precision DAC required in conventional SAR algorithm was eliminated by a series of digitally controlled

offsets. These offsets were implemented by direct device mismatch and capacitive loading techniques. The capacitive loads are parasitic PFETs which exploit sub-micron transistor mismatches to achieve precision femto-Farad capacitive tuning. This technique is used to generate offset in the microvolt range. For larger offsets in the millivolt range differential pairs in the comparator and preamplifiers are grossly mismatched.

Formulas for differential mode gain and rejection ratios were derived using equivalent half mode circuit analysis to account for the effects of device mismatch. This analysis is normally inconsequential as differential circuit design and layout are carefully optimized. The COP ADC uses several intentional mismatch techniques to create voltage offsets. As a result, CMRR, DCRR, and CDRR are finite and cannot be neglected. In particular, CMRR and DCRR render the preamplifier and comparator susceptible to external noise. The formulas for a differential pair amplifier were verified in simulations.

7.1 Future Work

The following issues that arose in this thesis should be studied in greater detail in future work.

1. The system prototype presented in Chapter 4 included a first order low pass filter and simple PI loop filter operating at $64\times$ oversampling. To reduce power consumption a revised design was proposed operating at $32\times$ oversampling. The revised design included the interpolation filter, a PID loop filter and second order low pass output filter. Prototype verification and experimentation of this system to confirm simulation results is necessary. The lower frequency operation is critical in determining the required ADC specifications. It is also recommended that alternate loop filter designs be considered and the effect of open loop bandwidth be further evaluated.
2. The COP ADC is based on a NMOS preamplifier array and latched comparator. A significant portion of the total noise contribution is from flicker or $1/f$ noise. It is therefore recommended that these circuits be implemented with PMOS devices to assess the reduction in flicker noise versus increased thermal noise tradeoff.
3. The presence of hysteresis in the current design requires further investigation. The hysteresis effect does not appear in schematic simulations and only very minimally in extracted simulations. It could be related to the test PCB but that is unconfirmed.

4. In Chapter 6 noise measurements were undertaken, however these measurements include both the source and DUT noise. The DUT noise must be de-embedded from the total noise measurement. This requires equipment to measure and quantify the source noise such as a low noise differential probe and low frequency spectrum analyzer. Alternatively, a closed loop measurement system as in [85] would be another option.
5. Upon resolving the hysteresis issue it would be beneficial to implement the full SAR algorithm. This would require verilog coding and timing analysis in a FPGA controller configuration.
6. The prototype COP ADC did not include a track and hold circuit. The track and hold circuit is an integral part of the ADC design. A passive track and hold based on capacitive charge sharing is required for low power operation. It consists of capacitors and FET switches. Capacitor sizing is determined by the oversampling ratio and theoretical kT/C noise limit. The FET switches are then sized according to required sampling time constant.
7. Calibration procedures for the COP ADC require investigation. Due to process and mismatch variations the offsets can shift which can result in increased INL and possibly missing codes. Extra calibration circuitry may be required to fine tune the offsets. This requires comprehensive simulations and measurements to determine the statistical variation to be compensated.
8. The gain formulas derived for mismatched differential amplifiers are quite lengthy and not very intuitive. These formulas should be carefully examined and simplified if possible.

Appendix A

Mismatch in differential amplifiers

The amplifier of Fig. A.1 with intentional mismatches in M1 and M2 will have non-zero A_{dm-cm} and A_{cm-cm} . Analytical expressions for all differential gain parameters will be derived which take into account mismatches in g_m , g_{mb} and r_o . This is accomplished by analyzing cross coupled single ended circuits which account for the mismatched parameters [10]. Applying this procedure, the equivalent common and differential mode cross coupled single ended circuits are given in Fig. A.2 and Fig. A.3 respectively. In these figures the following definitions apply,

$$\Delta g_m = g_{mM1} - g_{mM2} \quad (\text{A.0.1})$$

$$\Delta r_o = r_{oM1} - r_{oM2}$$

$$\Delta g_{mb} = g_{mbM1} - g_{mbM2}$$

$$g_m = (g_{mM1} + g_{mM2})/2 \quad (\text{A.0.2})$$

$$r_o = (r_{oM1} + r_{oM2})/2$$

$$g_{mb} = (g_{mbM1} + g_{mbM2})/2$$

By deriving equations for v_{od} and v_{oc} all relevant gain parameters can be derived. This is accomplished by appropriately applying KVL and KCL to the single ended equivalent circuits. First, Apply KCL to the differential mode circuit of Fig. A.3,

$$\frac{i_{Rd}}{2} = g_m \frac{v_{id}}{2} + v \frac{\Delta g_m}{2} + \frac{i_{r_{od}}}{2} - v_{tail} \frac{\Delta g_{mb}}{2} \quad (\text{A.0.3})$$

Applying KCL to the common mode circuit of Fig. A.2 yields,

Figure A.1: Differential amplifier for mismatch analysis.

Figure A.2: Single ended common mode cross coupled half circuit of the differential amplifier with mismatch.

Figure A.3: Single ended differential mode cross coupled half circuit of the differential amplifier with mismatch.

$$i_{Rc} = g_m v + \frac{\Delta g_m}{2} \frac{v_{id}}{2} + i_{r_{oc}} - v_{tail} \Delta g_{mb} \quad (\text{A.0.4})$$

Next apply KVL to the common mode circuit,

$$\begin{aligned} v &= v_{ic} - v_{tail} \\ &= v_{ic} - 2i_{Rc} R_{tail} \end{aligned} \quad (\text{A.0.5})$$

$$\begin{aligned} v_{oc} &= -i_{Rc} R \\ &= 2i_{Rc} R_{tail} + \frac{\Delta r_o}{2} \frac{i_{r_{od}}}{2} + i_{r_{oc}} r_o. \end{aligned} \quad (\text{A.0.6})$$

Finally, apply KVL to the differential mode circuit to get,

$$\begin{aligned} \frac{v_{od}}{2} &= \frac{\Delta r_o}{2} i_{r_{oc}} + \frac{i_{r_{od}}}{2} r_o \\ &= -\frac{i_{Rd}}{2} R. \end{aligned} \quad (\text{A.0.7})$$

The end result is five equations (A.0.3) to (A.0.7) and five unknowns ($i_{Rc}, i_{Rd}, i_{r_{oc}}, i_{r_{od}}$ and v). These equations can be manipulated into the standard form,

$$v_{od} = A_{dm}v_{id} + A_{cm-dm}v_{ic} \quad (\text{A.0.8})$$

$$v_{oc} = A_{dm-cm}v_{id} + A_{cm}v_{ic} \quad (\text{A.0.9})$$

from which the expressions for the gain parameters are,

$$A_{cm-dm} = R \frac{\alpha_1}{\alpha_2} \quad (\text{A.0.10})$$

$$A_{dm-cm} = \frac{R(-4r_o(R+r_o)\Delta g_m - 4g_m R \Delta r_o + \Delta g_m \Delta r_o^2)}{4\alpha_2} \quad (\text{A.0.11})$$

$$A_{cm} = \frac{-R(4g_m r_o(R+r_o) + R\Delta g_m \Delta r_o - g_m \Delta r_o^2)}{\alpha_2} \quad (\text{A.0.12})$$

$$A_{dm} = R \frac{\alpha_3}{2\alpha_2} \quad (\text{A.0.13})$$

where,

$$\alpha_1 = -4r_o\Delta g_m(R+r_o+2R_{tail}(1+g_{mb}r_o)) + 8g_m\Delta g_m r_o^2 R_{tail} \quad (\text{A.0.14})$$

$$-4\Delta r_o g_m(R+2R_{tail}) + (\Delta g_m + 2g_{mb}R_{tail}\Delta g_{mb})\Delta r_o^2$$

$$\alpha_2 = 4(R+r_o)(R+r_o+2R_{tail}(1+(g_m+g_{mb})r_o)) \quad (\text{A.0.15})$$

$$+2RR_{tail}(\Delta g_m + \Delta g_{mb})\Delta r_o - (1+2(g_m+g_{mb})R_{tail})\Delta r_o^2$$

$$\alpha_3 = -4r_o(4g_m^2 r_o R_{tail} + 2g_m(R+r_o+2R_{tail}+2g_{mb}r_o R_{tail})) \quad (\text{A.0.16})$$

$$-r_o R_{tail} \Delta g_m (\Delta g_m + \Delta g_{mb}) - 2(R+2R_{tail})\Delta g_m \Delta r_o$$

$$+(4g_m^2 R_{tail} + 2g_m(1+2g_{mb}R_{tail}) - R_{tail}\Delta g_m(\Delta g_m + \Delta g_{mb}))\Delta r_o^2$$

Calculating the gain parameters (A.0.10) to (A.0.13) for a balanced differential pair ($\Delta g_m \rightarrow 0$, $\Delta g_{mb} \rightarrow 0$ and $\Delta r_o \rightarrow 0$)

$$A_{dm} = -g_m \frac{Rr_o}{R+r_o} \quad (\text{A.0.17})$$

$$A_{dm-cm} = 0 \quad (\text{A.0.18})$$

$$A_{cm-dm} = 0 \quad (\text{A.0.19})$$

$$A_{cm} = -g_m \frac{Rr_o}{R+r_o+2R_{tail}+2(g_m+g_{mb})r_o R_{tail}} \quad (\text{A.0.20})$$

Furthermore, assuming $r_o \rightarrow \infty$ the CMRR by definition is,

$$\begin{aligned} CMRR &= \left. \frac{A_{dm}}{A_{cm}} \right|_{r_o \rightarrow \infty} \\ &= 1 + 2(g_m + g_{mb})R_{tail} \end{aligned} \tag{A.0.21}$$

which is a well known formula for matched differential pairs [10].

Appendix B

PCB CAD

Figure B.1: Verification PCB schematic

Figure B.2: Verification PCB layout, top later.

Figure B.3: Verification PCB layout, bottom later.

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