Wideband tunable transmission-line N-path filter on CMOS 130 nm

by

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A thesis submitted to the Faculty of Graduate and Postdoctoral Affairs in partial fulfillment of the requirements for the degree of

Master of Applied science

in

Department of Electronics

Carleton University
Ottawa, Ontario

Abstract

This research aims to increase the bandwidth of a transmission-line N-path filter around the clock frequency. The proposed filter consists of two four-path parallel stages with series inductors. The filter solves the trade-off between in-band insertion loss and out-of-band rejection of the original N-path filter. The proposed filter is tunable between 0.1 and 1 GHz. Post layout simulation results show that bandwidths of 80 MHz can be achieved when the filter is tuned to 1 GHz. A high-frequency 4-phase non-overlapping clock generator with a 25% duty cycle is designed to drive the proposed filter; an off-chip clock is applied at 4 times the switching frequency. The proposed filter has a die area of 1.5 mm^2 and was fabricated with CMOS 130-nm technology. The post-layout simulation results show that the filter is tunable from 0.1 to 1GHz, bandwidth of 80 MHz can be achieved at 1 GHz and the noise figure of the filter is less than 3.2 dB over the frequency range. Unfortunately, the clock generator is not working properly, which is why measurement results show discrepancies from the simulated results. Several hypotheses are explored to explain the cause of these differences.

Acknowledgements

First, I would like to acknowledge my supervisor Prof. Calvin Plett, who supported me throughout this research and provided insightful comments on this thesis.

Thank you to all the staff in the department office who helped me with everything administrative, and for being so kind and patient.

Thanks to the following people who helped me with the software and other parts of my design: William Che Knisely, Thomas Michael Pepler and Ahmad Eldahshan.

I would like to acknowledge CMC Microsystems for the provision of products and services that facilitated this research, including the CAD tools, fabrication services using the 130-nanometre CMOS technology from IBM.

Finally, a huge thank you to my dearest Mom, Lili, for her love and encouragement and she supported in my life throughout the years; and to my father, Khalil, who always encouraged me to continue my education and then my lovely husband Nasser for believing in me and supporting me.

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Chapter 1. Introduction

This chapter explains the fundamentals of wireless receivers and their enormous important in modern life. In section 1.1 different architectures of the receiver with the introduction of direct conversion receiver are explained. Afterward, performance metrics characterizing receivers will be reviewed.

1.1 Motivation

Wireless communication is an essential part in our modern lifestyle. The recent demand for new multi-band, multi-standard receivers, such as GSM, LTE, WCDMA, and GPS, has attracted the attention of a lot of researchers. Higher data rates and increasing bandwidth of standards require to add more bands. Growing commercial demands for high linearity, high Q, and tunable on-chip filters make this research necessary and relevant.

Rapid growth of communication wireless and limitation of radio spectrum call for highly flexible wireless transceivers which have result in the Cognitive radio concept. Cognitive radio is programmed and configured dynamically and can automatically detect available channels in the wireless spectrum to avoid user interference and congestion by choosing the best wireless channel in its proximity. The main advantage of CR-based networks is providing higher spectral efficiency, supporting a higher number of users, and achieving higher coverage. Cognitive radio requires a system that can handle any type of modulation for a received signal and can adjust to the required frequency band and bandwidth. This system is called a Software-Defined Radio (SDR). One of the main challenges of designing SDR is finding an RF band-pass filter with tunable center frequency

RF filtering plays a significant role in zero-If transmitters and receivers. Zero-If transmitters and receivers' architecture are presented below. The architecture of integrated RF transceivers is mostly determined by system requirements and RF bandpass filter performance. This thesis discusses programmable on-chip filtering in wireless applications.

1.2 Wireless Transceivers

In this section receiver and transmitter architecture which is suitable for CMOS integration is illustrated to understand the role of RF filtering. Wireless receivers have been used to pick up the desired signal and transform it from the electromagnetic domain to the electrical domain, then to shift the frequency of the signal, amplify it, and process the signal such that analog to digital converters (ADC) may convert the analog signal to the digital domain. Different receiver architectures exist; heterodyne and direct conversion receivers are the most used.

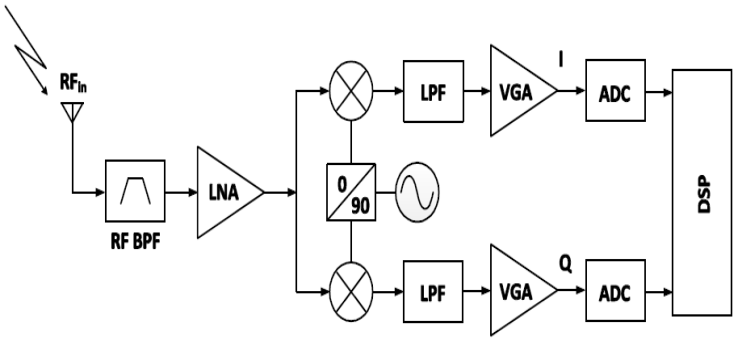
In heterodyne receivers, the received signal first enters a pre-select filter which rejects out-of-band signals. Then, a low-noise amplifier boosts the signal amplitude. Another bandpass filter follows the LNA to reject the unwanted image frequency band. Then the RF signal is down converted to an intermediate frequency (IF) using a mixer. Next, the signal is converted to a baseband signal for further processing after passing through a narrow band IF filter.

On the other hand, the direct conversion receiver, which is known as a zero-IF receiver or a homodyne serves to demodulate incoming radio signals by using a local oscillator when the LO is phase-locked with the received signal's carrier. The local oscillator frequency is set to the desired carrier frequency or very close to it.

In Zero-If architecture, the RF signal directly down converts to a BB signal without any intermediate frequency stages, thus eliminating the need for an IF stage. The Zero -IF architecture has an advantage over the super-heterodyne architectures because it requires fewer bandpass filters. Zero-If transmitter and receiver are shown in Figure 1-1.

Figure 1-1 [1] shows that at the receiver side, the signal is received by the antenna, is then filtered by a bandpass filter, which aims to remove all large out-of-band blockers and is amplified by an LNA. This amplified signal is converted down to baseband frequency by using a mixer that is fed by a local oscillator signal. The signal is finally low pass filtered. Then, the variable gain amplifier (VGA) amplifies the signal to create an optimum match with the analog to digital converter's dynamic range. In other words, the VGA ensures that the appropriate input signal amplitude obtains for the converter's specific dynamic range. Demodulation and data coding will be performed afterward by digital signal processing. Modulation, frequency conversion, and power amplification are three functions of the transmitter.

At the transmitter side, digital signals will be converted to analog by passing through a digital to analog converter (DAC). The baseband signal is upconverted to RF after filtering. Before the signal is emitted by the antenna, a power amplifier amplifies the signal, so proper filtering should be completed prior to up conversion so that the device satisfies the transmission mask requirement. Implementing the analog RF filter to have both high Q-factor and high dynamic range is, however, a difficult task.



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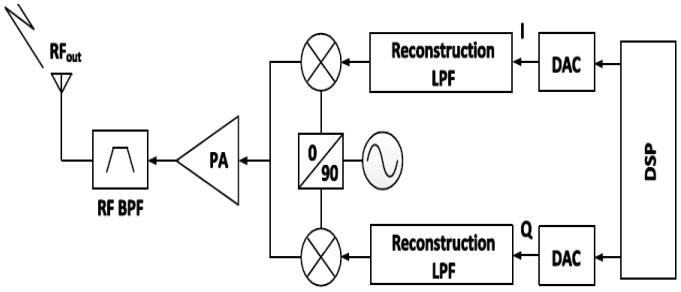


b)

Figure 1-1 Zero-IF architecture a) Receiver b) Transmitter [2]

In zero-IF transceivers, there are some problems such as 1/f noise and LO self-mixing [3]. These issues have been solved through extensive digital calibration. The dynamic range limitations of the zero-If transceiver, however, remain problematic for the technology. For example, on the receiver side, the input signal at the antenna contains the desired channel and interferers. The strength of in-band interference is limited due to the radio standard, but out-of-band blockers might be much stronger because they originate from other wireless networks. Therefore, before the LNA, some RF pre-filtering is needed to properly reject out-of-band blockers without affecting the receiver's noise figure and in-band distortion level. Typically, pre-filtering is done using an off-chip BPF, for example, a surface acoustic wave (SAW) filter or a bulk acoustic wave (BAW) filter.

These filters have high Q, small size, and good power handling. The drawback to these filters is that their off-chip status adds size and cost to any device in which they are installed. External SAW/BAW filters are applied to remove out-of-band blockers in single standard traditional receivers. However, in dynamic spectrum access applications, SAW filters are no longer suitable because the desired received frequency changes based on time and location. We, therefore, need programmable RF filtering.

In the following section, the necessity of the reconfigurability of the RF pre-filtering in the next generation of the wireless transceivers is discussed.

1.3 Tunable Filter Application

In recent years, the growth of wireless communication systems results in many wireless standards. A smartphone, for instance, typically supports Wi-Fi connectivity, GPS, and Bluetooth. The phone works over different frequency bands and communication standards, and portable phones must have long battery life and be sold for low cost and small size. By taking size, cost, and battery life into account, the idea of sharing the transceiver's hardware is motivated which leads to Multi-band multi-standard concept. Multi-band multi-standard transceivers share the transceivers hardware as much as possible in a single chip which can help to save battery charge while reducing cost and size.

In single RF front end transceivers, a tunable filter or bank of switched filters are used to receive multi-band frequencies. For a limited frequency band, using a bank of switched filters make sense. With growing numbers of frequency bands as wireless communications become increasingly popular, a tunable filter becomes a good option.

Such a filter, possessing low in-band insertion loss and high out-of-band rejection that has a wide bandwidth at the frequency of interest, increases our telecommunications capacity while maintaining affordability and the device's size. This thesis focuses on creating tunable, fully integrated filters for the application of cognitive radio and signal classification receivers.

1.4 Performance Metrics Characterizing Receivers

To evaluate wireless transceivers, performance metrics should be specified. The fundamental parameters of any receiver, as might be clear from the above review, relate to human perception of the signal's strength and efficacy: noise is the primary concern, and all means of measuring a signal are tied to this range of phenomena.

Noise

The weakest signal a receiver can discriminate depends on the input noise and how much thermal noise the receiver adds to the signal. The most appropriate way of quantifying this effect is the signal-to-noise ratio. Ascertaining this ratio requires an understanding of noise in a CMOS receiver, which derives from three sources: thermal noise, shot noise, and flicker noise.

Thermal Noise

Thermal movement of charge carriers can cause thermal noise, existing resistor elements in any circuit modeling cause thermal noise. Thermal noise can be model by white noise. Its spectral density is constant.

Shot Noise

Shot noise is caused by the discrete nature of electric charge where charge carriers are passing a potential barrier such as P-N junctions or gate barriers. Again, shot noise can be modeled by white noise. Its power spectral density is constant.

Flicker Noise

Carriers released at the silicon channel and the oxide can cause flicker noise. Flicker noise is also known as 1/f noise because it has a 1/f power spectral density due to the time constant of this phenomenon. The noise of a system can be specified in three ways, namely: the noise factor (Fn), noise figure (NF), and noise temperature (Te). Input noise originates in the black body radiation phenomenon. Similarly, the noise of a system can also be specified in the same three ways, to wit: noise factor (Fn), noise figure (NF), and equivalent noise temperature (Te).

The input noise and the desired signal will see the same gain in a signal chain. Noise added by the system will degrade the signal-to-noise ratio. A system's noise factor is related to the output noise power and input noise power as shown in (1-1).

The following equation defines a receiver's overall noise performance:

$$\text{Noise factor} = \frac{\text{SNRin}}{\text{SNRout}} \tag{1-1}$$

The output noise power is a function of the noise factor, receiver gain, and bandwidth. It can be calculated by using the function (1-2).

$$\mathrm{N_{out}(dBm)} = -174\mathrm{dBm} + 10\mathrm{logBW} + \mathrm{NF[dB]} + \mathrm{G[dB]} \quad (1\text{-}2)$$

The minimum signal that the system can detect is calculated by dividing the output noise (N_{out}) by the receiver gain, which appears in equation (1-3).

$$\mathrm{MDS[dBm]} = -174\mathrm{dBm} + 10\mathrm{logBW} + \mathrm{NF[dB]} \quad (1\text{-}3)$$

Since a higher data rate system requires more bandwidths for a specific modulation scheme, the minimum detectable signal (MDS) is increased.

1.4.1 **Phase Noise**

Waveform's jitter—phases of a waveform randomly fluctuate—when they encounter noise or poor conditions. The ideal signal is indicated by a single spectral line in the frequency domain. However, unwanted amplitude and phase fluctuation exit in presence of the signal in the real world. The signal is presented by the spread of spectral lines due to random amplitude and phase fluctuations. So, phase noise is the representation of random fluctuation in the frequency domain. The received RF signal changes frequency using a local oscillator. In the local oscillator, we expect to have a tone in the frequency spectrum to shift the frequency content, but since we have non-idealities, the jitter component appears in the frequency spectrum.

$$\mathrm{LO(t)} = \mathrm{A}\cos(\omega_{\mathrm{LO}}(\mathrm{t}) + \varphi_{\mathrm{n}}(\mathrm{t})) \quad (1\text{-}4)$$

$\varphi_n(t)$ in equation (1-4) indicates phase noise. A receiver's RF signal passes through the mixer and is multiplied by the local oscillator (LO). Multiplying the RF signal with LO in the time domain translates to convolution in the frequency domain, blockers near the RF signal can consequently be downconverted on top of the desired signal, so reciprocal mixing can cause noise, which is shown as ((1-5). Based on the below formula, phase noise is constant across the bandwidth.

$$\mathrm{P(phase\ noise)} = \mathrm{Pblocker[dBm]} + \mathrm{L(\Delta f)} + 10\mathrm{logBW} \tag{1-5}$$

1.4.2 **Nonlinearity**

In a nonlinear system, the output spectrum consists of new frequencies different from the input frequency. For example, in a nonlinear system, if the input signal is a sinusoid, the output spectrum has components at integer multiples of the input frequency. In a non-linear system, by increasing the input power, the output power is also increased to a certain point. After the output power reaches its maximum, the system's gain starts to reduce. p_{1dB} or 1dB compression point is the output power level where the gain of the system is reduced by 1 dB from its constant value.

1.4.3 **Desensitization**

Imagine a scenario in which a low-power signal arrives with a high-power unwanted signal. In such a case, receiver desensitization is caused by an odd order intermodulation product. This effect reduces the wanted signal strength. Assume, there is a strong interfering signal in the presence of a received signal, the non-linearity within the receiver mixer and amplifier chain caused intermodulation products. Intermodulation products reduce effective gain in wireless devices. If the interference signal is strong enough, the resulting product subtracts from the desired signal product, thus reducing the device's effective gain.

Intermodulation distortion on radio receivers should be minimized to ensure that only signals received at the radio antenna pass through the radio and appear at the output. Intermodulation distortion (IMD) is a common measure of the linearity of amplifiers, mixers, and other RF components. To understand these effects, we assume that the input signal is as shown in (1-6):

$$x(t) = A_1 \cos \omega_1 (t) + A_2 \cos \omega_2 (t) \tag{1-6}$$

Therefore, the output up to the third order would be reflected in the solution to (1-7):

$$y(t) = a_0 + a_1 \left(x(t)\right) + a_2(x(t))^2 + a_3(x(t))^3 \tag{1-7}$$

By expanding this equation, components at the fundamental frequency and at, $\omega_1 \pm \omega_2$, $2\omega_1 \pm \omega_2$, $2\omega_2 + \omega_1$ appear at the output. Second-order nonlinearity refers to second-order intermodulation distortion (IMD2) can cause $\omega_1 \pm \omega_2$ products. $2\omega_2 \pm \omega_1$ and $2\omega_1 \pm \omega_2$ component is referred to third-order intermodulation distortion (IMD3). Second-order distortion can be problematic in homodyne receivers. Third-order distortion is problematic in all receivers regardless of their architecture. Second and third-order intercept points indicate two most important linearity specification of a system. Radio's susceptibility to interference for the nearby users is determined by the receiver's intermodulation performance. Second and third-order intercept points predict the receiver's intermodulation performance.

1.4.4 **Cross-modulation Distortion**

Odd-order nonlinearities can cause cross-modulation such that amplitude modulation of one signal transfers to another signal. An example would be if a broadcast receiver were placed near to a broadcast transmitter, there would likely be cross modulation which would be heard as an annoying combination of the two signals. A strong continuous wave (CW) blocker near the receive band as well as an out-of-band modulated jammer near the receiver band causes the modulated jammer and the CW signal to cross-modulate.

This phenomenon creates in-band distortion. The IIP3 performance of the LNA determines the receiver's cross–modulation performance. By using the active post distortion (APD) method or linearity enhancement techniques IIP3 performance of the CMOS LNA may be improved. However, off-chip filtering may be required due to limitations in the down converter.

1.4.5 **Dynamic Range**

"Dynamic range" refers to the receiver's ability to process a range of input powers from the antenna. By applying a single test frequency, we can test a receiver for its upper dynamic range limit, which is defined by the 1 dB compression point (P1dB). The 1 dB compression point is the point where the output is 1 dB down from the ideal linear response. The upper power limit determination of dynamic range is specified by the input power at that point. The difference between the 1dB compression point and the system noise floor power level is the dynamic range.

1.4.6 **Possibilities for RF Tunable Filtering**

In this thesis, we are looking for tunable on-chip filtering. A range of possible RF tunable filtering exists but each filter topology has its own positive and negative aspect. Filters can be sorted into one of two categories: passive or active. The active filter uses active components, like op-amp, and passive components like resistors and capacitors. They typically do not use inductors because inductors are lossy, heavy, bulky and expensive at lower frequencies. RF active filters can have a high-quality factor. Their application is limited because they provide more noise and nonlinearity, which results in their having a limited dynamic range. These filters also require more power to reduce noise contribution.

In contrast, a passive filter consists of the passive components such as: resistors, capacitors, and inductors. SAW or BAW filters are passive filters, the resonance frequency for which is determined by the piezoelectric material dimension and its properties. These filters are not, however, appropriate to serve as a band-pass filter with tunable center frequency.

Integrated LC filters with variable capacitors are also passive filter which provides tunability, but they perform poorly by suffering from the loss of on-chip inductors that have low-quality factors. Limited Q-factor of on-chip inductors increases the insertion loss of the filter and shape-factor of the filter. The Q-enhancing technique in combination with negative impedance can compensate for the resistive loss of inductor, which is good, but the filter has a limited dynamic range [10].

An FBAR resonator is a radio frequency filter designed to remove frequencies that are not supposed to be transmitted. The FBAR resonator filter can have a Q factor in the range of 1K and it requires very little power. The FBAR resonator suffers, however, from poor center frequency accuracy, which is caused by a fabrication defect resulting in thick material layers. This type of resonator further lacks tunability. It is not suitable for different frequency bands; an array must be used to operate across frequency bands, which increases the installation area and costs [4][5].

References [6] and [7] discuss tunable off-chip and cavity bandpass filters. These filters can provide low insertion loss and significant out of band rejection, but they are not a suitable size for use in a mobile handheld device.

The electrostatically actuated MEMS resonator is a tunable bandpass filter, but it is not practical in a 50-ohm system environment at GHz frequency: its impedance level might be at least several kilo-ohms [8]&[9].

Researchers have grown very interested in frequency translate filtering as a way to implement on-chip RF pre-filtering. Figure 1-2 shows that this technique, down converts the first input signal at RF frequency, then low pass filters and upconverts again at RF frequency. The low pass filter can be implemented by using an RC network. Upconverting and down converting a signal can be accomplished with switches. One of the advantages of this approach is the filter's high-quality factor (Q).

The low-pass filter's bandwidths can consequently be lower than the RF center frequency (switching frequency). In short, the filter's quality factor is very high. This technique's advantage is that its center frequency is tunable with clock frequency. In the other words, we can change the center frequency of the filter with changing the clock frequency. The architecture shown in Figure 1-2 shows the concept of frequency translated filtering, although it is usually a multiple path, driven by multiple phase clocks. Therefore, this type of filter is labeled as an N-path filter in literature. N-path technique is based on frequency translated filtering. The N-path filter architecture is consisting of multiple paths that are driven with multiple phase clock. N-path filter concept is discussed in the next chapters.

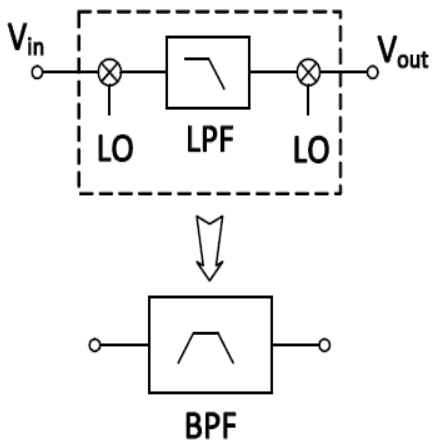


Figure 1-2 Frequency translated filtering [2]

1.5 Research Objectives

This thesis concentrates on N-path filters for RF frequencies. Lower supply voltage headroom and a short-channel effect were two obstacles in CMOS technology, however rapid development of CMOS technology provides MOS switches with low on-resistance and with less parasitic capacitances. Also, high-quality factor capacitance can be realized with new CMOS technologies. In this work, our goal was to find a tunable wideband bandpass filter with sharp rejection around our frequency of interest which was 1GHz.

A simple effective way to attain this purpose (a tunable filter) is to use the N -path filter. The N-path filter is a high Q tunable filter with just switches and capacitors. The traditional N-path filter topology suffers from some issues, namely: a tradeoff between the in-band insertion loss and out-of-band rejection and second-order filtering which is not good enough for an application that requires sharp filtering. To overcome this drawback, a high order N-path filter is desired. The traditional N-path filter also provides constant bandwidth over frequency.

In this thesis, we are aiming to give a brief overview of the N-path filter and next present a passive transmission line N-path filter which improves the tradeoff between out-of-rejection and in-band insertion loss of the traditional N -path filter. The wideband transmission line N-path filter is introduced afterward.

1.6 Contribution

This research aimed to realize a tunable filter that has wide bandwidth around our frequency of interest. The original N-path filter can offer high Q filtering at the flexibly programmable RF center frequency. However, the original N-path filter high-frequency performance is limited by the switch resistance and parasitic capacitance of the switches.

To improve the high-frequency performance of the filter, a transmission line N-path filter is presented which reduced the in-band insertion loss and increasing out-of-band rejection. The transmission line four path filter is designed and simulated in CMOS 130nm. In this work, we aimed to achieve wider bandwidth than what is reported by others. There was a lot of optimization done to increase the bandwidth of transmission line four path filter around our frequency of interest. A wideband transmission-line four-path filter is designed and fabricated based on low-cost CMOS 130 nm technology. The post-layout simulation shows that the bandwidth of the filter has been improved to over 80 MHz, at 1 GHz central frequency, while the operating frequency is between 0.1 GHz and 1 GHz. A high-frequency four-phase non-overlapping clock generator with a 25% duty cycle is design and fabricated on CMOS 130 nm technology to drive the switches of the transmission-line four-path filter. The previous implementations of N-path filters and clock generators as referenced in this thesis were done in 65 nm CMOS. In this thesis, successfully implementing the filter and clock generator with four non-overlapping phases in an older and slower process (CMOS 130 nm) was more challenging and hence an accomplishment.

1.7 Organization of Thesis

This thesis is organized into five chapters:

Chapter1 describes the type of wireless transceiver and performance metrics that characterize receivers and RF tunable filter possibility.

Chapter 2 discusses the N-path filter and presents the transmission-line N-path filter as a solution that resolves the tradeoff between in-band insertion loss and out-of-band rejection in traditional N-path filters. The design technique that increases the in-band bandwidth of the transmission-line N path filter will be compared with the traditional N-path filter.

Chapter 3 discusses clock generation architecture that generates four non-overlapping clocks around the desired frequency. The transmission-line N-path filter needs the non-overlapping clock to drive the gates of the switching transistors.

Chapter4 discusses the implementation and measurement results of the wideband transmission-line N-path filter. The chapter demonstrates the layout of the transmisson line N-path filter and clock generator.

Chapter 5 summarizes the work and presents possible future lines of inquiry.

Chapter 2. Integrated Analog Bandpass Filters

2.1 N-path Filtering Concept

This chapter discusses the history and the current state of the art of N-path filtering. The preceding chapter presented an overview of the art; this chapter delves more deeply into the concept of an N-path filter, its transfer function, harmonic selectivity, harmonic folding, and limitations presented by the filter's original topology. This chapter presents the transmission-line N-path filter approach afterward. Chapter 3 presents a Clock generator that provides N-phase non-overlapping clocks to drive switches in the filter. Chapter 4 presents the simulation and measurement results of the transmission-line N-path filter.

The N-path filter is a relatively new technique for on-chip RF pre-filtering at RF frequencies, but it derives from a technique used in the kHz frequency range. The oldest N-path filter was introduced in 1953 [11]. In [11], the tunable switched-RC BPF filter was mentioned, but transistors were not available at that time, so mechanical switches were used. Mechanical switching complicated the N-path filter's implementation during the 1950s because it required matching different paths. A mechanical switch increased the complexity of switching frequencies such that the filter's potential was never fully realized. Its maximum switching frequency for integrated signals was too low [12].

New CMOS technology resurrects the N-path filter because it can provide switches with low on-resistance and low parasitic capacitance. High-quality capacitance is another factor that has become available.

The rapid development of CMOS technology has attracted researchers' interest for RF applications. CMOS technology is, however, a good candidate for implementing an on-chip N-path filter because N-path filters consist of switches and capacitors without any inductor. N-path filtering down-converts the signal to the baseband by using a set of switches that operate as a mixer. The down-converted signal passed through a low-pass filter, and the signal is up-converted back to the RF frequency. In fact, the N-path filter characteristically converts low pass to bandpass filtering around the mixing frequency, which is defined by the clock frequency. We can design an on-chip bandpass filter with the N-path technique by sending the signal through the low pass filter. This process is technically easier than designing a bandpass filter.[2]

Figure 2-1 shows a block diagram of an N-path filter. The filter consists of N time-invariant networks and 2N frequency mixers, which should be driven by the multiphase clock. The center frequency of the filter is defined by the mixing frequency, and each path has a T/N time shift where T is the period of the mixer clock. If the LTI network consist of a low pass filter around DC, the input signal is down-converted first, then filtered through the low-pass filter, and is up-converted again, thus resulting in a bandpass filter around the mixing frequency. The mixers are realizing with switches driven by a multiphase clock. The charge does not exchange between capacitors p and q in Figure 2-1, which are performing the mixing function. Implementing the low pass filter can be done through a simple RC network. Resistors can be shared between all paths because resistors are memory-less elements. The first and second sets of switches are identical, so each switch can replicate the other's task. N-path filter architecture can therefore be converted in a single-ended N-path filter, which is shown in Figure 2-1(b) [2].

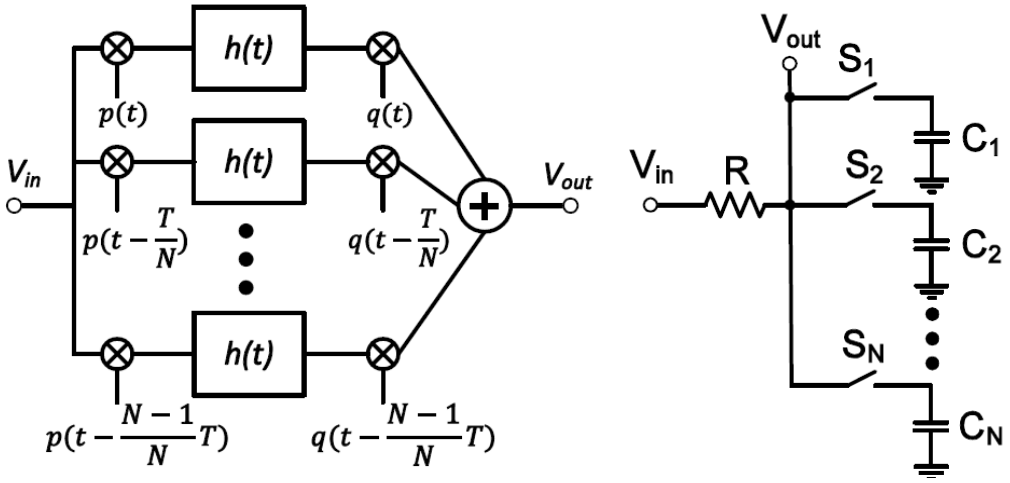


Figure 2-1 (a) N-path filter architecture. (b) single port, single ended N-path filter [2]

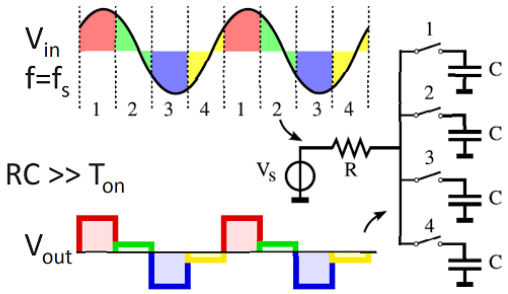
Although the N-path filter is a high Q tunable bandpass filter, a number of phenomena degrade the performance of the N-path filter and must be resolved. These include the on-resistance of the switches, R_{sw}, the translations of the source impedance, harmonic folding, poor filter shape, and the finite rise and fall times of the LO, some of which will be discussed later.

2.2 Single-Ended Switched RC N-Path Filter

The single-ended switched RC N-path Filter with a non-overlapping clock is shown in Figure 2-2. Figure 2-2 a) shows the time domain waveform for a 4-path switched-RC filter. At any moment in single-ended N-path filters, the output voltage is the voltage of the only capacitor that is connected to the output, if the time constant (RC) is much bigger than $T_{on} = \frac{T_S}{N}$ (that is, RC is larger than the ON time of the switch).The output voltage is calculated as the average of the input voltage over the time that the capacitor looks at the input voltage.

If the switching frequency is equal to the input frequency, every period a specific capacitor will observe the same part of the input waveform. Since each capacitor looks at the other part of the waveform, the output voltage is akin to a staircase approximation of the input voltage. Capacitors conduct no current because they experience a steady DC voltage[33].

However, if the input frequency is different from the switching frequency, the capacitor conducts current when the switch is ON. This occurrence ensures that the average voltage on a capacitor is zero. In summary, when the input voltage frequency and the switching frequency are different, the output voltage will be suppressed depending on the RC time and on time of the switch and the offset of input voltage frequency with switching frequency.



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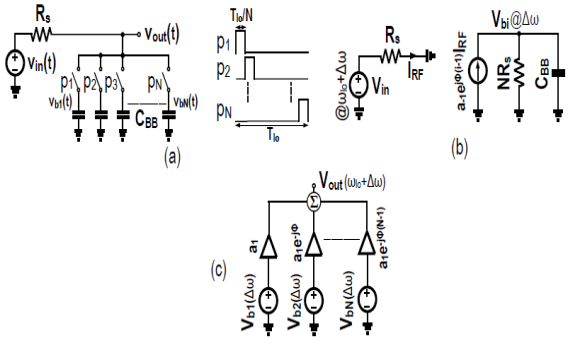


b)

Figure 2-2 4-path switch-RC filter: a)Time domain waveform b) single ended N-path filter with multiphase clocking

Time domain analysis is used to understand the behavior of a single-ended N-path filter. Time domain input current is first down-converted by N-phase non-overlapping time domain clocks ($P_i(t)-\ P_N(t)$), which results in a baseband current $I_{BB}(t_i)$. The baseband current then experiences low pass filtering that creates baseband voltage $V_{BB}(t_i)$. Complex baseband impedance filters the baseband current out by convolving $Z_{BB}(t)$ with $I_{BB}(t_i)$. The baseband voltage is then upconverted by the time domain clock again and creates the input voltage, which is shown in (2-1)[13].

$$\mathbf{V_{RF}(t)} = \sum_{\mathbf{i=1}}^{\mathbf{N}} \mathbf{LO_i}\,(\mathbf{t}).\{|\mathbf{LO_i(t).\,I_{RF}(t)}| \ * \ \mathbf{Z_{BB}(t)}\} \tag{2-1}$$

Frequency domain of input voltage is shown in (2-2)[13].

$$\mathrm{V_{RF}(t)} = \mathrm{N} \sum_{\mathrm{m=-\infty}}^{\infty} \sum_{\mathrm{m=-\infty}}^{\infty} \mathrm{a_n\ a_m\ I_{RF}}(\omega - (\mathrm{n+m})\omega_{\mathrm{LO}}).\ \mathrm{Z_{BB}}(\omega\ - \mathrm{n}\omega_{\mathrm{lo}}) \tag{2-2}$$

where, ω_{lo} is the clock frequency and $(n+m) = kN$ where k is an integer. The magnitude of the Fourier coefficient for a non-overlapping clock is shown by a_n and a_m, which is defined by $|a_n| = \left|\sin(n\,\frac{\pi}{N}\,/(n\pi)\right|$. The input impedance of a single-ended N-path filter with the N phase non-overlapping clock with R_S and R_L as port impedance is shown in (2-3)[13].

$$\mathrm{Z_{in}}(\omega) = \ \mathrm{R_{on}} + \mathrm{N} \sum_{\mathrm{n=-\infty}}^{\mathrm{n=+\infty}} |\mathrm{a_n}|^2\ \mathrm{Z_{bb}}\,(\omega - \mathrm{n}\omega_{\mathrm{lo}}) \tag{2-3}$$

where R_{on} is switch resistance, N is the number of the path, Z_{bb} is baseband impedance ($Z_{bb} = \frac{1}{j\omega C_{bb}}$). ω_{lo} is clock frequency, and $|a_n| = \left|\sin\left(n\frac{\pi}{N}\right)/(n\pi)\right|$ is the Fourier coefficient for a multiphase clock.

2.3 Analysis of N-path Filters

State Space Analysis of LPTV Circuits allows us to model the behavior of N-path filters. To be able to calculate the transfer function of the N-path filter, we assume that: 1) Switches are ideal, therefore, when the switch is ON, the switch impedance is zero and when the switch is OFF, the switch impedance is infinite, and switching instantaneously occurs. In [1], exhaustive analysis has been used to calculate N-path filters' transfer function. The transfer function can, however, be more simply calculated in the following paragraph.

Figure 2-1(b) shows the single-ended N-path filter with a non-overlapping clock with a duty cycle of $\frac{1}{N}$. If the time constant (RC) is much greater than $\frac{T_S}{N}$ (T_S is period of the clock), the baseband voltage is the baseband signal. When the clock is high, the current can be defined by $\frac{(v_{in}(t)- v_{bi}(t))}{R_s}$, which represents the superposition of the RF current and the baseband current. The RF current is caused by $v_{in}(t)$ and the baseband current is caused by $v_{bi}(t)$.

To be able to find baseband voltage, an equivalent circuit is shown in Figure 2-3 for the RF and baseband parts. Assume the input signal is located at $\omega_{lo} + \Delta\omega$, $v_{in}(t) = V_{in}\, e^{j(\omega_{lo}+\Delta\omega)t}$, $\frac{v_{in}(t)}{R_s}$ is converted to the baseband current by using a mixer. The baseband current created by input voltage passes through the baseband capacitor and is calculated by convolving $\frac{v_{in}(t)}{R_s}$ and $P_i\,(t)$ with the magnitude of, $a_{-1}\, e^{j\emptyset(i-1)}\, \frac{v_{in}(t)}{R_s}$, which is the Fourier coefficient of $P_i\,(t)$, where $\emptyset$ is the difference between $P_1\,(t)$ and $P_2\,(t)$. The baseband voltage can be calculated by multiplying the baseband current with the impedance seen from it as shown in (2-4) [14].

$$\mathbf{V_{bi}}(\mathbf{j}\omega\Delta) = \mathbf{a_{-1}}\, \mathbf{e}^{\mathbf{j}\emptyset(\mathbf{i-1})}\, \mathbf{I_{RF}} * \frac{\mathbf{NR_s}}{\mathbf{jNR_sC_{BB}}\Delta\omega + \mathbf{1}} \tag{2-4}$$

The baseband current is just present for $\frac{1}{N}th$ of the time so, NR_s is presented as the effect of baseband current on baseband voltage [14].So, $\mathrm{V_{bi}}(\mathrm{j}\Delta\omega)$ as a function of input voltage $\mathrm{V_{in}}(\omega_{\mathrm{lo}} + \Delta\omega)$ is shown in (2-5) [14].

$$\mathbf{V_{bi}}(\mathbf{j}\Delta\boldsymbol{\omega}) = \mathbf{Na_{-1}}\ \mathbf{e^{j\emptyset(i-1)}}\mathbf{G}(\Delta\boldsymbol{\omega})\ \mathbf{V_{in}}(\boldsymbol{\omega_{lo}} + \Delta\boldsymbol{\omega}) \tag{2-5}$$

where $\mathrm{G}(\Delta\omega)$ is

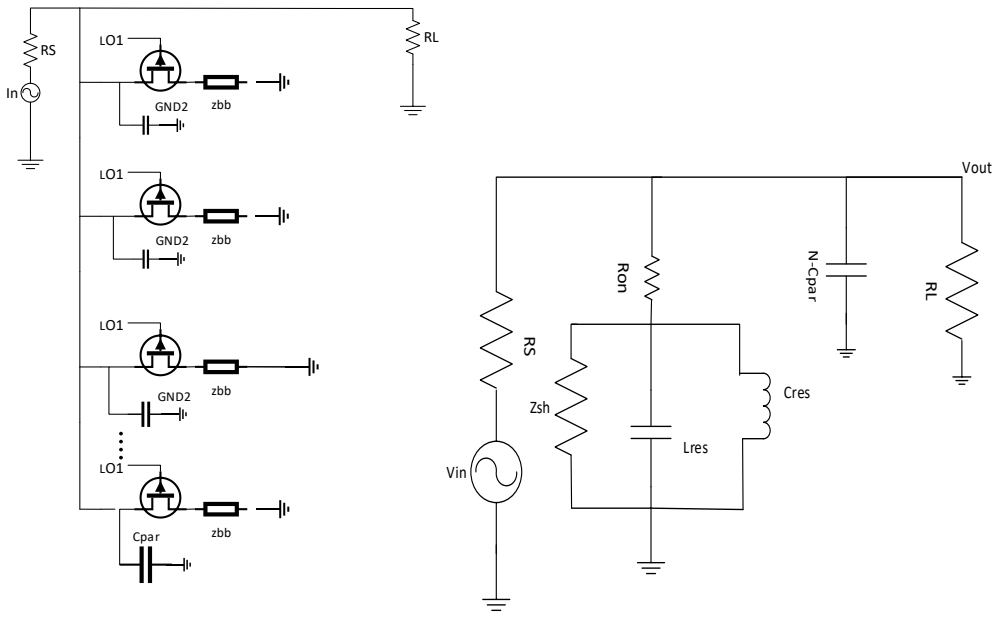
$$\mathrm{G}(\Delta\omega) = 1/(\mathrm{jNR\_s\ C\_BB}\ \Delta\omega + 1) \tag{2-6}$$

Basband voltage of all nodes V_{bi} , are then upconverted from $\Delta\omega$ to $\omega_{lo} + \Delta\omega$ at node V_{out}. The output voltage (V_{out}) is composed of N path output voltages; each path contribution is equal to: $V_{bi}a_1\ e^{-j\emptyset(i-1)}$. Since all paths are identical, the contribution of all paths will be N times the contribution of one path, which allows each path's output voltage to be calculated with (2-7) [14]:

$$\frac{\mathrm{V_{out}}\big(\mathrm{j}(\omega_{\mathrm{lo}} + \Delta\omega)\big)}{\mathrm{V_{in}}\big(\mathrm{j}(\omega_{\mathrm{lo}} + \Delta\omega)\big)} = \mathrm{N^2}|\mathrm{a_1}|^{\,2}\ \mathrm{G}(\mathrm{j}\Delta\omega) = \mathrm{sinc^2}\ (\frac{\pi}{\mathrm{N}})\ \mathrm{G}(\mathrm{j}\Delta\omega) \tag{2-7}$$

2.4 RLC Model, Bandwidths and Quality factor

The transfer function of the N-path filter around the frequency f_s, is like a high-Q tank circuit. A single-ended N-path filter driven by N-phase non-overlapping clocks with port impedance R_s and R_L, baseband impedance ($Z_{bb}(w) = \frac{1}{(jwc_{bb})}$), parasitic capacitance C_{par}, is shown in (2-3) (a).



(a) **(b)**

Figure 2-3 (a) shunt N-path filter architecture(b) RLC model for N-path filter

The behavior of the N-path filter around the switching frequency can be model by the RLC circuit. An approximate linear time variant lumped elements model of the N-path filter at frequency near $w_{LO}$is indicated in Figure 2-3 (b). The value of L(L_{res}) and C (C_{res}) is shown in (2-8) and (2-9)[13]. Note that the value of L (L_{res}) depends on the clock frequency, unlike the value of C (C_{res}) and R (Z_{sh}).

$$L_{res} \approx N\,|a_1|^2\,(C_{bb}\ {w_{lo}}^2) \tag{2-8}$$

$$C_{res} = C_{bb}\,/(N\,|a_1|^2) \tag{2-9}$$

To be able to include the loss of the input signal, which is upconverted to the harmonic of clock frequency, $\boldsymbol{Z_{sh}}$ is defined. $\boldsymbol{Z_{sh}}$ is calculated based on (2-10)[13] where $\boldsymbol{R_a}$ is equal to:

$\boldsymbol{R_a = R_s \parallel R_L}$.

$$Z_{sh} = R_{sh} = (R_a + R_{on})\left\{\frac{\operatorname{sinc}\left(\frac{\pi}{N}\right)^2}{1 - \operatorname{sinc}\left(\frac{\pi}{N}\right)^2}\right\} \quad (2\text{-}10)$$

At high frequency for frequency f=fc (clock frequency), the $Z_{sh}L_{res}C_{res}$ circuit resonates at fc and becomes open; therefore $\frac{vout}{vin}$ ~1. For frequency $f \neq f_c$ $C_p$is open circuit, L_p is a short circuit parallel to R_P. Under these circumstances, $\frac{Vout}{Vin} = \frac{R_{on}}{R_{on}+R_s}$. With these definitions in hand, we can calculate an N-path filter's bandwidth and quality factor. To calculate the bandwidth of N-path filter, the N-path filtering concept is explained again to find the bandwidth easily.

Based on Figure 2-4, the operation of the N-path filter in the frequency domain is discussed. The desired signal is the signal shown with a dashed line. The original spectrum in Figure 2-4 (a) is shifted to baseband in Figure 2-4 (b) and then it is filtered in Figure 2-4 (c). After the signal is shifted back to RF and only desired signal remains in Figure 2-4 (d), therefore the N-path filter has twice the bandwidth of the low pass filter [15].

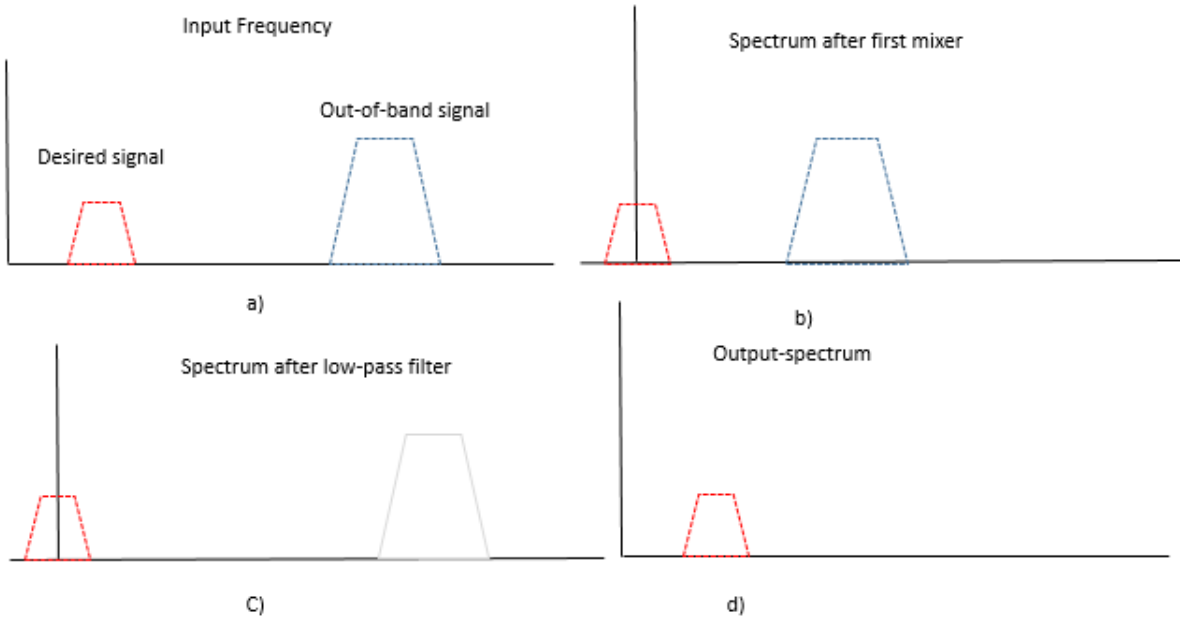


Figure 2-4 Operation of N-path filter

The bandwidth of the low pass filter must first be calculated. The low pass filter is the first-order RC network, so its bandwidth is depended on the value of R and C and the clock's duty cycle. R is equal to the total resistance, which includes any resistance like source resistance and switch resistance. The bandwidth of the low pass filter is shown (2-11).

$$\mathbf{BW_{low-pass}} = \frac{\boldsymbol{D}}{\boldsymbol{2\pi RC}} \tag{2-11}$$

The bandwidth of the baseband filter can be calculated with function (2-12)[15].

$$\mathbf{BW_{band-pass}} = \frac{\boldsymbol{D}}{\boldsymbol{\pi RC}} \tag{2-12}$$

By decreasing the number of phases, the duty cycle increases, and the bandwidth consequently increases, on the other hand, decreasing the number of paths can increase the effect of harmonic folding. The quality factor of the filter is calculated by $Q = \frac{BW}{f_s}$. Because the bandwidth is dependent on the RC time constant and the number of paths, it can be as low as a few MHz. Clock frequencies on the order of GHz can, therefore, have a very high-quality factor. The filter's quality factor can be calculated by (2-13).

$$\mathrm{Q} = \frac{\mathrm{f_{lo}}}{\mathrm{BW}} = \mathrm{f_{lo}} \mathrm{N} \pi \mathrm{R_S} \mathrm{C_{BB}} \tag{2-13}$$

Although the N-path filter is a high-Q tunable bandpass filter, it suffers from some issues like harmonic folding, on resistance of the switch, and poor filter shape which will be explained in the next sections [6]-[7].

2.5 Harmonic Folding

Although the N-path filter can provide good tunability, however, it suffers from two drawbacks: Harmonic Selectivity (HS) and Harmonic Fold Back (HFB). Harmonic Selectivity means that the filter has an extra passband around frequencies kf_s (K= 2, 3, 4...). Using the differential N-path filter topology can cancel the even part of HS [1]&[30]. The N-path topology also helps to reduce harmonic folding to a large extent. Mixing with the square waves clock can cause the folding of higher harmonics into the fundamental frequency. In fact, the terms of "harmonic folding" mean folding of the spectrum located near the harmonic of the clock into the desired band. Based on [18], the magnitude of the baseband impedance, scaled by a sinc function and is up- converted to the clock's harmonics. This phenomenon is called "harmonic replicas". Signals located at $|kN-1|f_{lo}$ fold back into the signal at f_{lo}, where N is the number of phases and K ∈Z. Harmonic folding can be reduced by increasing the number of paths (N). The maximum number of phases in a multiphase clock generator is limited by the process technology, which is not able to operate at high frequency. The $(N-1)\ f_{lo}$ is the strongest harmonic that can be folded to the filter passband. Increasing the number of the paths requires more clock phases, as discussed above. Multiple clock phases are difficult to create at high frequency because the increasing number of phases requires digital logic. Digital logic operates at a high frequency, which is not practical because of the limitation on the process technology. Harmonic aliasing can be suppressed up to (N-1) times the harmonics of the LO frequency. For example, a four-path filter, with an LO frequency of 500 MHz will fold a blocker located at 1.5 GHz back to 500 MHz. By increasing the number of the paths and clock phases, the folded harmonics can be pushed further away. For an 8-path filter, the first folding back will occur from $7f_{lo}$. So, to be able to increase between f_{lo} and the first folded component around $(N-1)\ f_{lo}$, the number of the paths should be increased [2].

To suppress the negative effects of folding back, a pre-filter may be placed in front of the N-path filter. Increasing the number of paths can also relax the pre-filter transition band requirement. Notice that in the N-path filter, we assume all paths are identical and the clocking signal is ideal; in reality, however, they are not ideal. If there is a mismatch in clocking signal, or between paths, as previously explained, harmonics of k· (N-1) and k· (N+1) fold into the desired signal and even order components are no longer canceled. When even order exists, we can observe extra frequency components in the output. Using large capacitance values can help to remove the mismatch between the paths, but the clock's signal mismatch may remain [2].

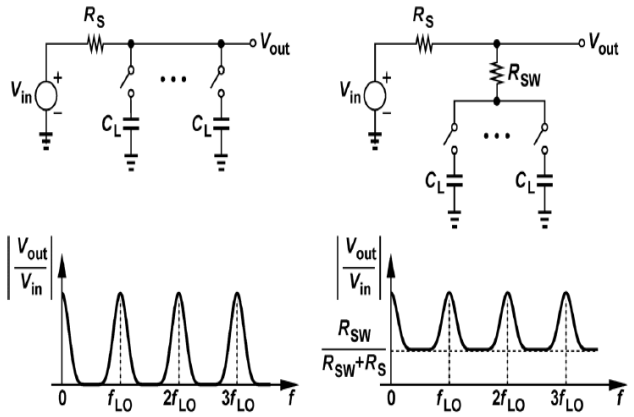
2.6 The Effect of Switch Resistance and The Clock's Duty Cycle On N-path Filters

Switches have non-zero resistance, which can influence a filter's transfer function. In fact, switch resistance can change the transfer function of the N-path filter by adding poles and zeros into the filter's transfer function. These unwanted zeros are far from the passband of the filter and they can limit the filter's stop-band rejection. For the frequency far from the switching frequency, on resistance of the switch limits the maximum filter rejection. Frequencies close to the switching frequency do not significantly suffer from switch resistance[31].

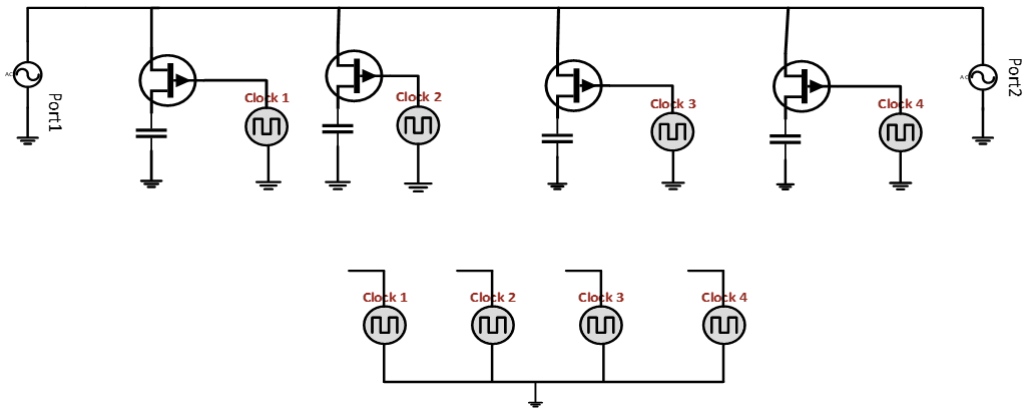
Switch resistance can further reduce the filter's quality factor by reducing the baseband signal's bandwidth. The switch resistance R_{sw} can limit the ultimate rejection by an amount calculated by: $\frac{R_{sw}}{R_{sw}+R_s}$ [19] & [20].

Some simulation is done to show the effect of switch resistance and duty cycle on transfer function of N-path filter. The input impedance of the N-path filter around the switching frequency is resistive and has a high impedance, which is like an equivalent tank circuit at the resonance frequency.

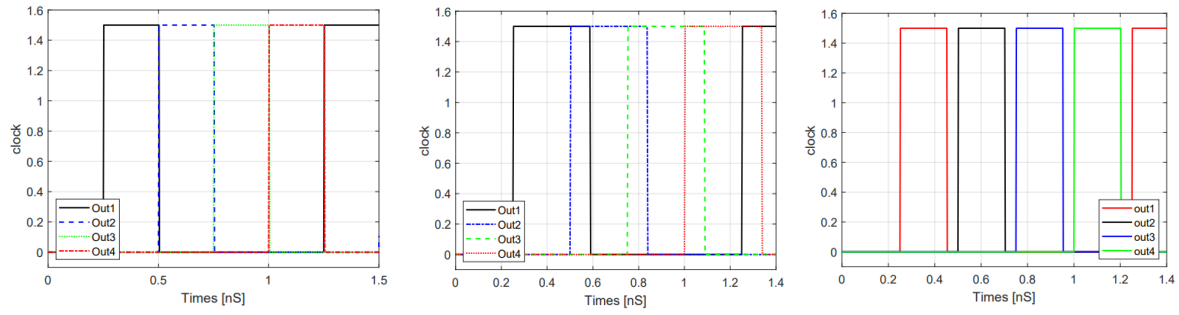
For frequencies far from the switching frequency, however, the N-path filter has a small impedance. If the duty cycle of the multiphase clock “D” is less than 1/N, all switches are off for periodic time intervals. Therefore, the output signal of the N-path filter tracks the input signal. For the frequencies far away from the switching frequency, reducing the duty-cycle from 1/N results in a higher input impedance that translates to less rejection. Reducing the duty-cycle decreases pass-band insertion loss as well, however maximum rejection degradation is much more than pass-band insertion loss. If D is larger than (1/N), two switches can be “on” at the same time, which results in charge sharing between capacitors. Charge sharing between capacitors destroys the filter shape completely.



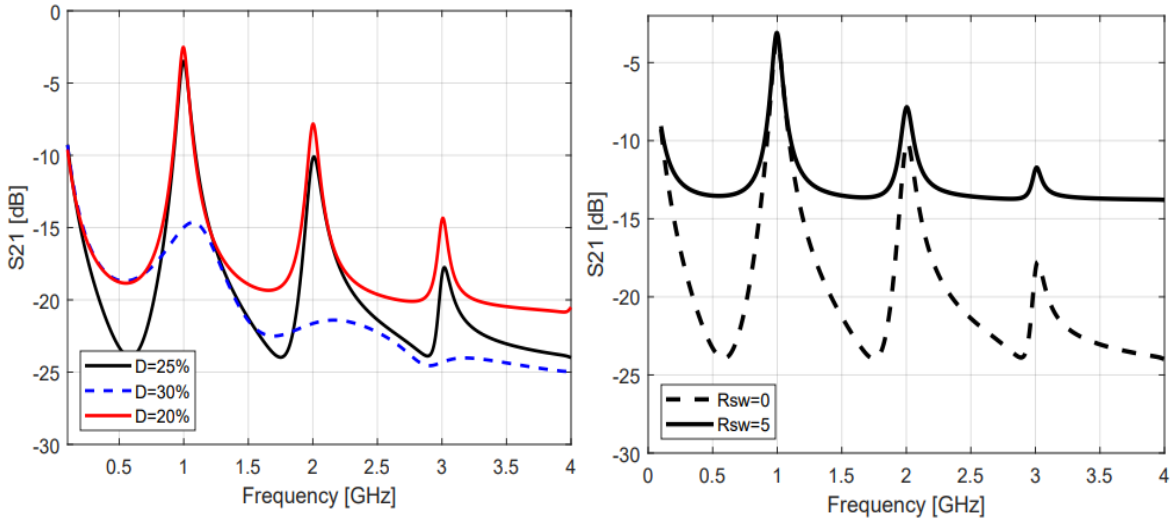
(a) (b)



c)



(d) (e) (f)



(g) (h)

Figure 2-5 N-path filter a) ideal b) with on resistance of the switch [28]

c) Schematic for the 4-path filter (switch size (w=1.2µm, L=120nm), C=40pF),d, e, f) clock generator with different duty cycle D=25%, D=30% and D=20%, respectively, g) effect of increasing the clock duty cycle in 4-path filter (C=40p, fs=1GHz, N=4) h) Switch resistance effect in 4-pathfilter for $R_{sw} = 0$ and $R_{sw} = 5$

Figure 2-5 a, b) show the effect of the switch on resistance on the N-path filter's transfer function. Figure 2-5 c) shows the schematic of the 4-path filter, with switches driven with ideal 4-non overlapping clocks with zero rise time and fall time. Figure 2-5 d, e, f) show the clock generator representation for different duty cycles (D=25% (ideal case), D=30%, D=20%). Figure 2-5 g) shows the comparison of 4-path filter transfer function simulation result for different duty cycles including D=25%, D=30%, and D=20%. Simulation is done by using PSS+PSP analysis with using external ideal clock generator as shown in Figure 2-5 d, e, f). Figure 2-5 h) shows the simulation result for 4-path filter for different switch resistance using ideal 4-non overlapping clocks. As has been seen, the on resistance of the switch limits the stop-band rejection of the filter. To minimize $\boldsymbol{R_{sw}}$, the width of the switches should be increased, which results in higher power consumption in the LO path.

2.6.1 **The Effect of Parasitic Capacitance On N-path Filters**

The switch parasitic capacitance of the N-path filter can also change the transfer function of the N-path filter. The parasitic capacitance of the switch can change the center frequency of the filter by shifting the passband's center to a lower frequency. Peak frequency is determined by (2-14) [13].

$$w_0 = \frac{1}{\sqrt{L_{res}\,(C_{res} + NC_{par})}} = \frac{1}{\sqrt{\frac{C_{par}\,N^2\,|a_1|^2 + C_{bb}}{C_{bb}\,\omega_{Lo}{}^2}}} \tag{2-14}$$

Based on (2-14), peak frequency is shifted to a lower frequency by increasing parasitic capacitance. This increase can cause unwanted peaking in the filter's passband. By increasing C_{bb}, the effect of parasitic capacitance will be reduced, but this reduction negatively affects the filter's bandwidth. Increasing parasitic capacitance can also cause loss in the filter, which results in reducing the filter's voltage gain. When the switch is ON, charge between the baseband capacitor and parasitic capacitor will be shared, therefore the gain of the filter is reduced.

2.6.2 **Filter shape**

The original N-path filter results in a second-order N-path filter, which is not good enough for many applications. A better filter shape may be obtained by increasing the N–path filter's order to have a better shape around the switching frequency. It has been known that any filter type and order (Butterworth, Chebyshev etc.) can be obtained by cascading shunt and series LC sections. This design methodology cannot, however, be applied to N-path filters: the linear periodic time variant (LPTV) nature of the N-path filter will not allow a cascading N-path filter. A four-order N-path filter is achieved by subtracting two second-order bandpass filters, which is presented in [14]. Two second order four-path filters with slightly different center frequencies are subtracted by using a Gm-C technique to do frequency shifting. This approach weakens the effect of switch resistance on stop-band rejection. In [14], the result of measurement shows that stopband rejection can be more than 55dB while having a better pass-band shape compared to the original N-path filter. This filter is implemented in CMOS 65nm and the center frequency of the filter is tunable from 400MHz to 1.2 GHz [14].

In [16], to implement higher-order filtering, the LC resonator in a coupled resonator LC bandpass filter is replaced by an N-path switched- RC network. In [17], the high order N-path filter was presented with a gyrator. The capacitor in the LC low pass filter in this source can be replaced by a N-path switches-RC networks and the inductor can be replaced by a gyrator. In this way, low-pass filter characteristics can be transformed into bandpass filter characteristics. A tunable 6^{th} order eight-path bandpass filter in CMOS 65 nm is presented in [14]. The 6^{th} order LC bandpass filter is shown in Figure 2-6 (a).

A series LC can be replaced with a shunt LC by using two gyrators, and a shunt LC resonator can be replaced with the switched capacitor counterpart. The 6^{th} order bandpass filter achieves 59 dB out-of-band rejection. The filter is also tunable in the range of 0.1 to 1.2 GHz. As explained above, there are a lot of ways to increase the order of filters. This thesis uses a design methodology that only uses passive elements to increase the order of the N-path filter. We talk about this methodology in Chapter 3.

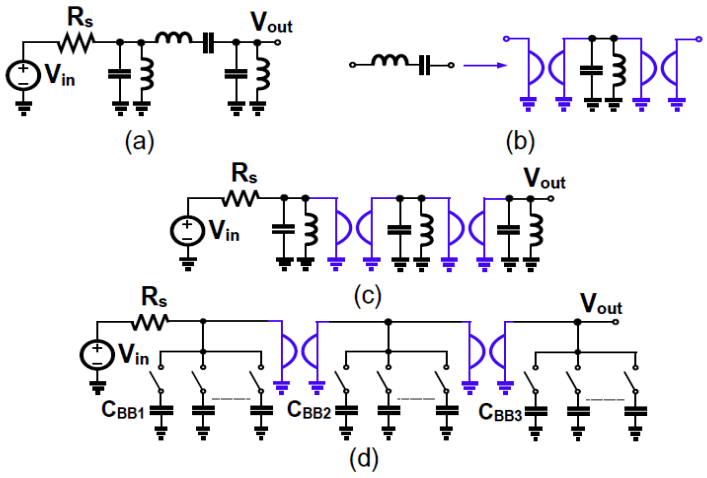


Figure 2-6 **a) 6^{th} order LC bandpass filter, b) series LC convert to parallel LC using two gyrators, c) parallel LC tank can be substituted by switched capacitor counterpart**

2.7 The relationship between insertion loss and out-of-band rejection

We may use two different architectures to implement an N-path filter: shunt and series architectures. Figure 2-7 and Figure 2-8 respectively show shunt switch N-path architecture and the series switch N-path architecture [34].

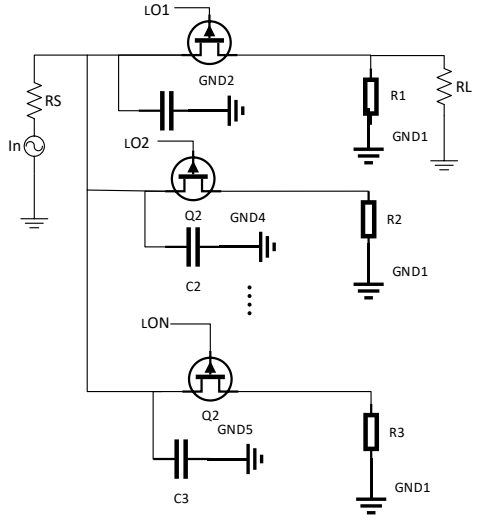


Figure 2-7 Shunt switched N-path architecture

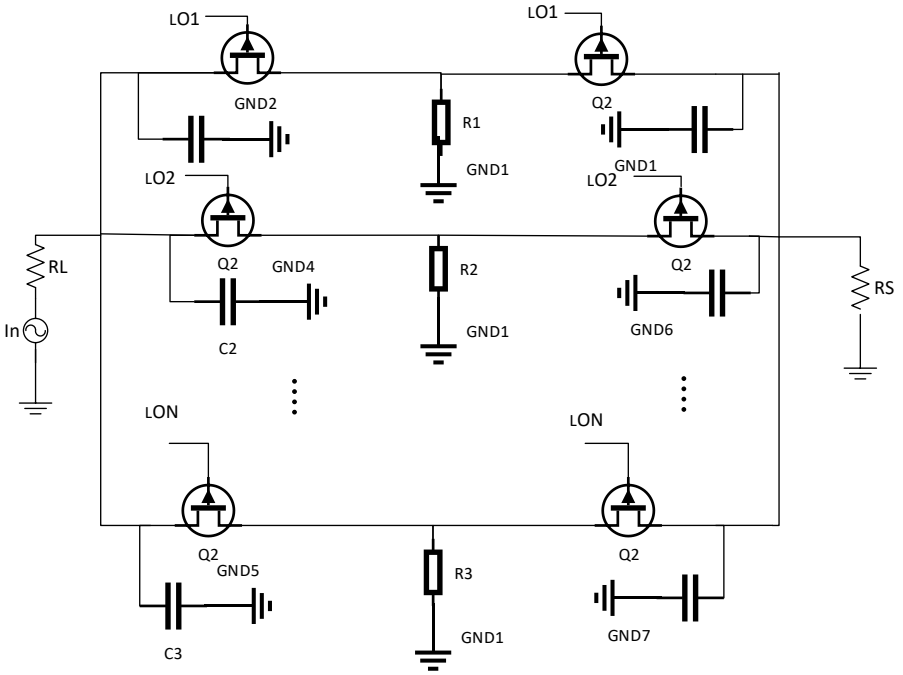


Figure 2-8 Series switched N-path architecture

In a shunt architecture, the peak in band gain near $\boldsymbol{\omega_{lo}}$ is based on (2-15) [13],

$$S_{21\,\mathrm{peak}}(s) \approx \frac{G_o}{1+\frac{s}{\omega_{p1}}} \tag{2-15}$$

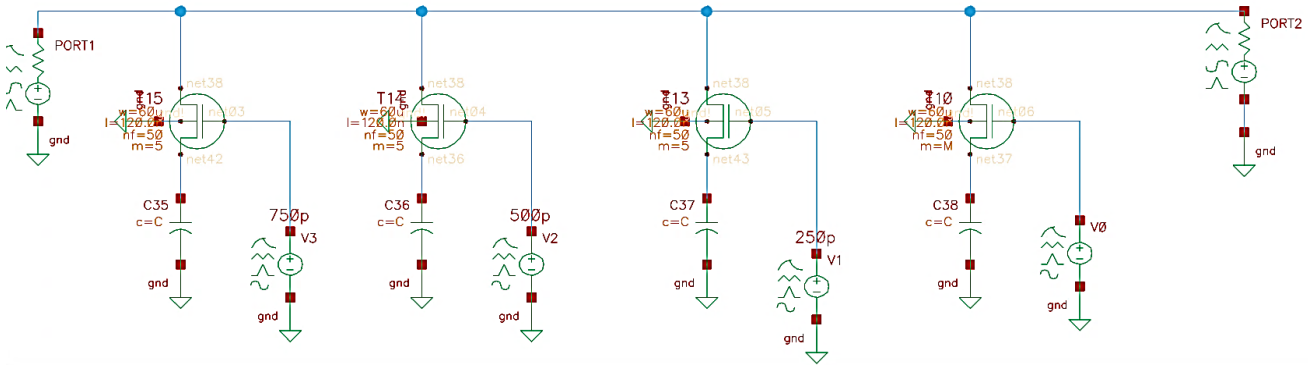
where G_o and ω_{p1}can be calculated by (2-16)[13].

$$G_o = \frac{2}{\frac{R_s}{(R_{on}+Z_{sh})+2}} \qquad \omega_{p1} = \frac{(R_{on}+Z_{sh})+2}{NC_{par}R_s} \tag{2-16}$$

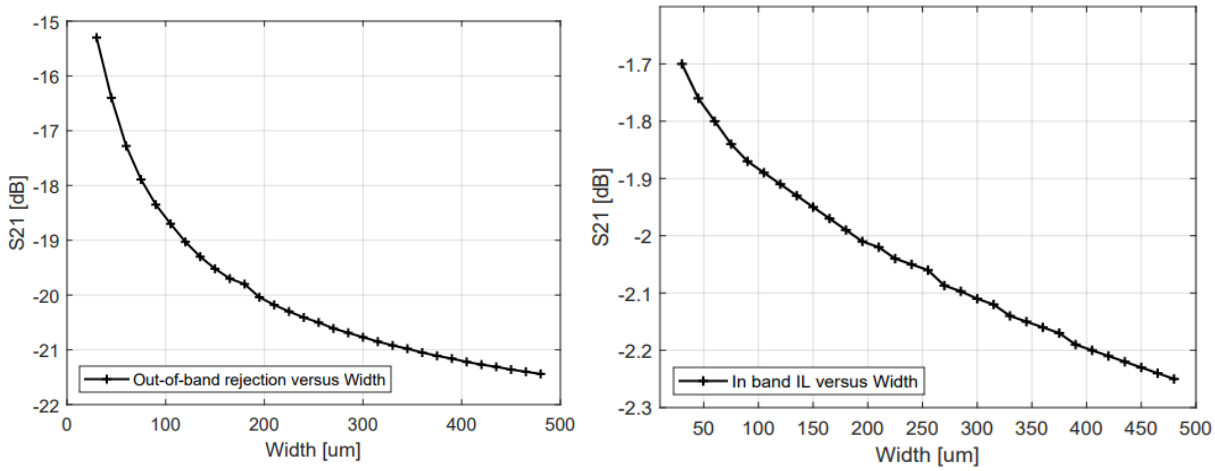
Out of band gain of this architecture is approximately based on (2-17) [13]:

$$S_{21\,\mathrm{out-of-band}}(s) \approx 2\,\frac{R_{on}}{R_S} \tag{2-17}$$

Increasing the switch size (keeping transistor gate length constant) reduces the on resistance of the switch (R_{on}) but increases parasitic capacitance (C_{par}). Based on (2-15) and(2-16), increasing the widths of the transistor causes w_{p1} and G_o to decrease. In-band gain will consequently be reduced, but out-of-band rejection will be improved. Figure 2-9 a) shows schematic of 4-path filter, ideal 4-non overlapping clocks drive the switches. Figure 2-9 b) shows the simulation result of the filter transfer function by using PSS+PSP analysis for different transistor size at 1GHz clock frequency with finite rise time and fall time (rise time and fall time=20pS, pulse width=200pS, $f_s = 1GHz$). The simulation result shows that by increasing the widths of the transistors, in-band insertion loss will be reduced, and out-of-band rejection will be improved.



(a)



(b) (c)

Figure 2-9 a) schematic for 4-path filter(L=120nm,C=50pF,W=Variable,) b) Out-Of-band rejection versus width of transistor and (c) In band insertion loss versus width

Increasing transistor size implies a tradeoff between in-band insertion loss and out-of-band rejection. In addition, the frequency of passband peak is predicted as (2-18) [13] &[32].

$$\omega_0 = \frac{1}{\sqrt{L_{res}(C_{res} + N\,C_{par})}} = \frac{1}{\sqrt{\frac{C_{par}N^2\,|a_1|^2 + C_{bb}}{C_{bb}\,\omega_{lo}{}^2}}} \tag{2-18}$$

Again, by increasing the transistor width, the parasitic capacitor phenomenon will increase, and the peak frequency drops, as shown in Figure 2-10.

Figure 2-10 shows the simulation result for 4-path filter as shown in Figure 2-9 a) by using PSS+PSP analysis at 1GHz clock frequency. Ideal 4-non overlapping clocks drive the switches with zero rise time and fall time. The parasitic capacitance effect can be reduced by increasing the value of C_{bb}, but increasing C_{bb} results in decreasing bandwidth and increasing chip area. Solving this tradeoff requires the introduction of a transmission-line N-path filter.

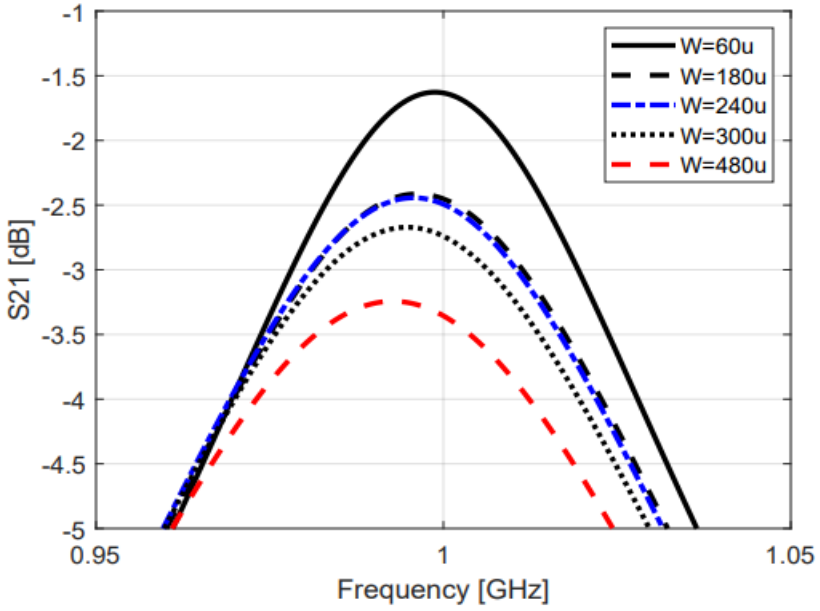


Figure 2-10 Peak frequency shifted by increasing width of transistor

2.8 Summary

The following briefly explains the typical problems presented by N-path filters. The filters characteristically suffer from switch on resistance, which limits the out-of-band rejection, as previously discussed. Increasing the size of the switches reduces it's on resistance, and therefore improves out-of-band rejection; however, by increasing switch sizes, the parasitic capacitance also increases.

This unwanted increase results in decreasing in-band insertion loss. So, there is a tradeoff between insertion loss and out-of-band rejection. Moreover, the parasitic capacitance of switches shifts the center frequency ω_0 of the passband to a lower frequency. Reducing the switch's parasitic capacitance and on resistance can be accomplished with device scaling. A further drawback is seen with this method: aggressively scaled device limits the switch gate clock voltage swing.

The N-path filter suffers from harmonic folding, too: signals which are located at $|kN-1|f_{lo}$ fold back into the signal at f_{lo}, where N is the number of phases and K is an integer. A four-path filter, for example, the most dominant harmonic folding components fold from 3fs and 5fs back into the passband around fs. Harmonic folding of N-path filters can be reduced by increasing the number of the paths, however higher number of the paths requires a higher number of clock phases, and this is typically limited by process technology.

Overall, the N-path filter provides high Q tunable filtering however it suffers from some limitations such as switch resistance and the parasitic capacitance of switches which limits the in-band insertion loss and out-of-band rejection of the filter. Switch resistance limits the filter's out-of-band rejection; parasitic capacitance increases the filter's in-band insertion loss. Transmission line N-path filter solves the tradeoff between the in-band insertion loss and out-of-band rejection.

The original N-path filter topology results in second-order filtering, which is not good enough for some applications that require sharp filtering around the center frequency. A higher-order N-path filter is required to overcome this drawback. Transmission-line N-path filters also provide sharp filtering around the center frequency. The transmission-line N-path filter has been proposed to improve high-frequency performance of the original N –path filter.

Chapter 3. The Transmission Line N-path Filters

The original N-path filter performance in high frequency is limited by the switch resistance which increases in-band insertion loss and the switch parasitic capacitance which limits the out-of-band rejection of the filter. The switch parasitic capacitance also shifts the peak band-pass response to a lower frequency. Moreover, the original N –path filter provides a poor filtering shape due to second-order configuration of the filter.

This chapter presents the analysis and design of the wideband transmission line N-path filter approach which solves the tradeoff between the in-band insertion loss and out-of-band rejection of the original N-path filter. The transmission line should more accurately be called an artificial transmission line. The in-band bandwidth around the desired frequency is also improved compared to the original N–path filter. First, the transmission line N-path filter configuration is introduced, then the wideband transmission line N path filter is presented.

The in-band insertion loss of the transmission- line N- path filter is reduced by absorbing shunt switch parasitic capacitance into the transmission-line. The out-of-band rejection of transmission-line N-path filter improves due to low pass filtering caused by on-resistance of the switch and transmission-line, which ends up solving the tradeoff between in-band insertion loss and out-of-band rejection.

The in-band insertion loss of the T-line N-path filter is consequently less sensitive to parasitic capacitance due to the parasitic capacitance being absorbed into the transmission-line. The transmission-line N-path filter provides sharp filtering because it uses a higher-order filter technique. It can provide better in-band P1dB compression, in-band IIP3, and filtering of out-of-band jamming signals.

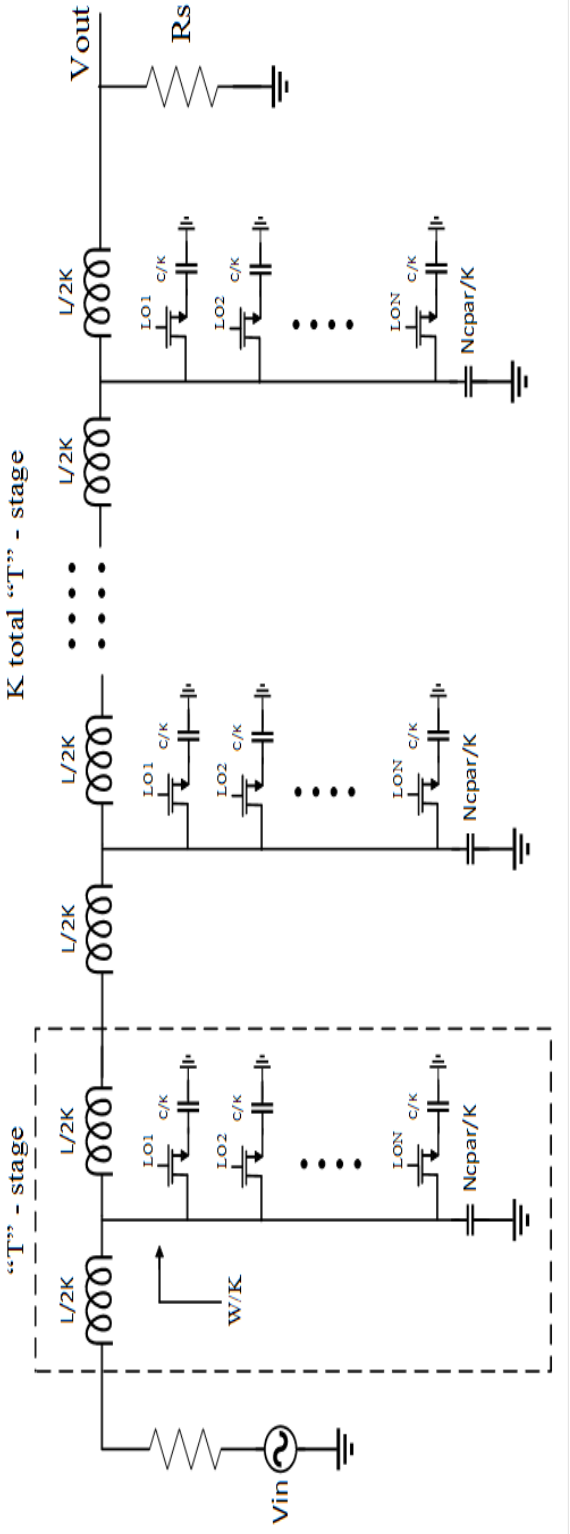


Figure 3-1 Transmission-line N-path filter [13]

The transmission line N-path filter structure is shown in Figure 3-1, where K is the total number of stages and N is the number of the path. Basically, if we have a traditional transmission-line, it has a characteristic impedance defined by (3-1).

$$\mathbf{Z_0} = \sqrt{\frac{\mathbf{L}}{\mathbf{C}}} \tag{3-1}$$

If we consider $Z_0 = R_s$ (port impedance) according to (3-1) to minimize reflection insertion loss, inductance values (L) can be determined by capacitance value, which in the present case is the parasitic capacitance of the switches. Since inductors are not ideal, the finite Q of the inductor limits the in-band insertion loss.

A lumped equivalent-circuit model of transmission-line N-path filter is used, which we may use to better understand the behavior of transmission-line N-path filters.

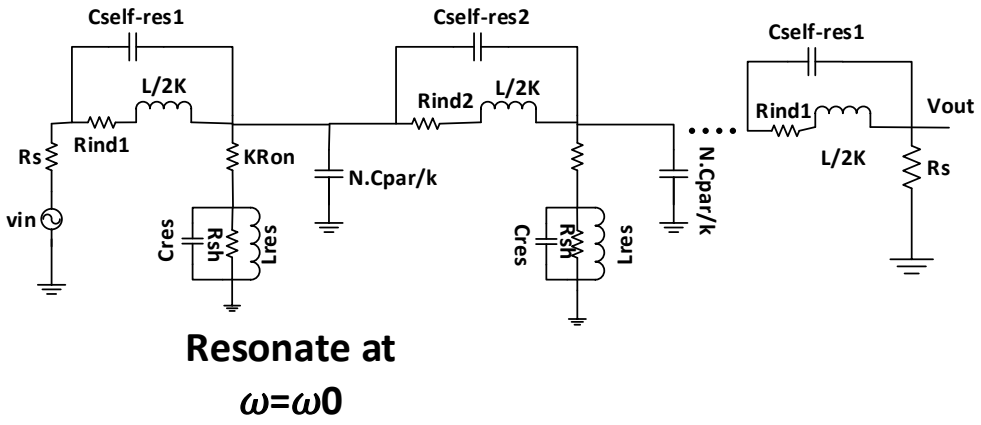


Figure 3-2 Equivalent circuit for TL N-path filter [13]

Figure 3-2 represents the equivalent circuit for transmission-line N-path filters. As has been seen, the transmission-line N-path filter is composed of the original N-path filter with the inductors, which are used to absorb switch parasite capacitances. The N –path filter's traditional behavior around the center frequency is approximated by an equivalent RLC tank circuit (C_{res},

L_{res}, and R_{sh}). The self-resonance of the inductor is caused by the parasitic capacitance $C_{self-res}$. R_{ind} denotes the inductor's resistive loss due to its finite Q.

In the transmission-line N-path filter, in-band insertion loss is limited by the finite Q of the inductor and harmonic loss R_{sh}. The transfer function of the transmission-line N-path filter is obtained with (3-2) [13].

$$\mathbf{A_v(s)} = \frac{\mathbf{4\,N^K\,|a_1|^{2k}\,K^{(2K+1)}\,R_s\,s}}{\mathbf{C_{bb}}^{\mathbf{k}}\,\mathbf{L^{(K+1)}\,s^{(2K+2)} + 4C_{bb}}^{\mathbf{k}}\,\mathbf{K\,L^K R_s\,s^{(2k+1)}} + \cdots} \tag{3-2}$$

Note that the transfer function does not include the inductor's effect of finite Q, such as inductor loss and parasitic capacitance. The transmission-line N-path filter introduces additional poles that result in a new frequency(ω_n) based on (3-3) and (3-4) [13].

$$\omega_{L0} = 1/\sqrt{C_{res}\,L_{res}} \tag{3-3}$$

$$\omega_n = \omega_{L0}\,.\sqrt{1+\frac{2}{L}\left(\frac{N\,|a_1|^2}{C_{bb}\,{\omega_{L0}}^2}\right)} \tag{3-4}$$

The structure's transfer function illustrates an interesting higher pole ω_n, which is dependent on ω_{L0} value, ω_{L0} is a resonant frequency discussed before. Increasing ω_n causes ω_n to approach ω_{L0}. ω_{L0} and ω_n are two of the filter's frequencies that depend on each other where C_{res} and L_{res} represent RLC-equivalent circuit of the N-path filter, and C_{bb} is the baseband capacitance of the filter (C/K). A transmission-line N-path filter will permit bandwidth changes versus LO frequency, which does not occur in traditional single-stage shunt N-path filters (the BW is traditionally constant despite LO changing). In the transmission Line N path filter, ω_n moves toward ω_{L0} with increasing frequency. This movement explains why passband bandwidth changes with LO frequency in the transmission line N-path filter.

Figure 3-3 shows the schematic of the 4-path transmission line filter with using ideal clocks. Figure 3-4 shows simulation result of the 4-path TL filter using PSS+PSP analysis, LO frequency is swept from 0.3GHz to 1GHz. Four non-overlapping ideal clocks with 25% duty cycle are used to drive the transistors with zero rise time and fall time. Figure 3-4 shows that in transmission line N-path filter with increasing LO frequency, ω_n becomes closer to ω_{L0}. For instance, when LO=1.5 GHz, you can see that $\omega_n$is closer to ω_{L0} compare to LO=1GHz; when LO=2GHz, $\omega_n$and ω_{L0} are matched.

Figure 3-5 shows schematic of 4-path transmission line with different stages. Figure 3-6 shows simulation result of the filter using PSS+PSP analysis, four non-overlapping ideal clocks with zero rise time and fall times are used to drive the transistors. Figure 3-6 shows that with increasing the number of stages(K), in-band insertion loss has been improved. The figure shows that increasing K results in better in-band insertion loss compared to the original N-path filter.

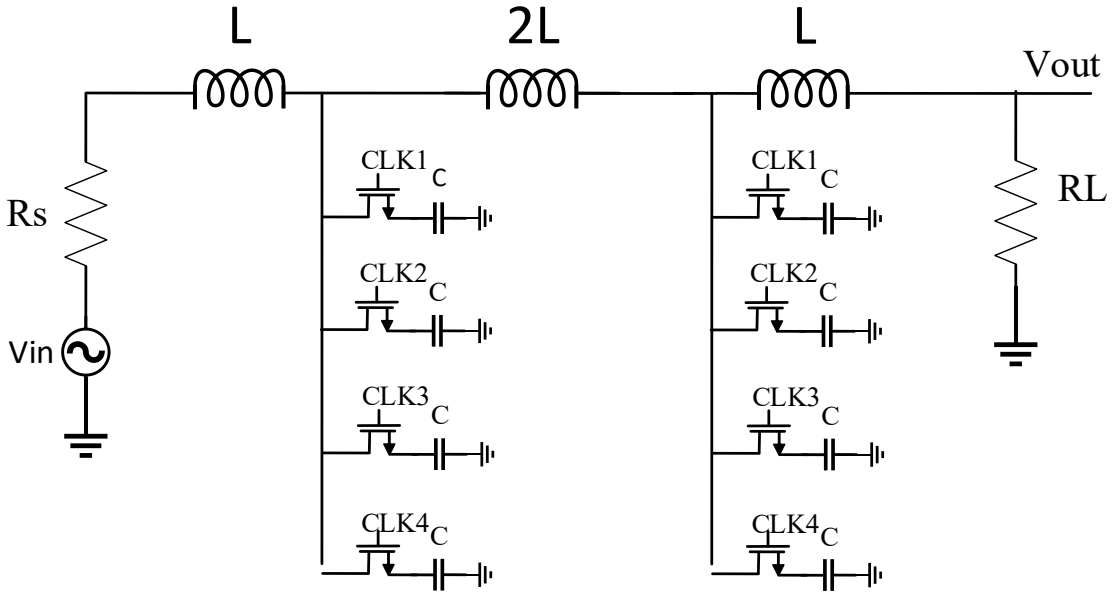


Figure 3-3 Schematic of two-stage4-path transmission line filter

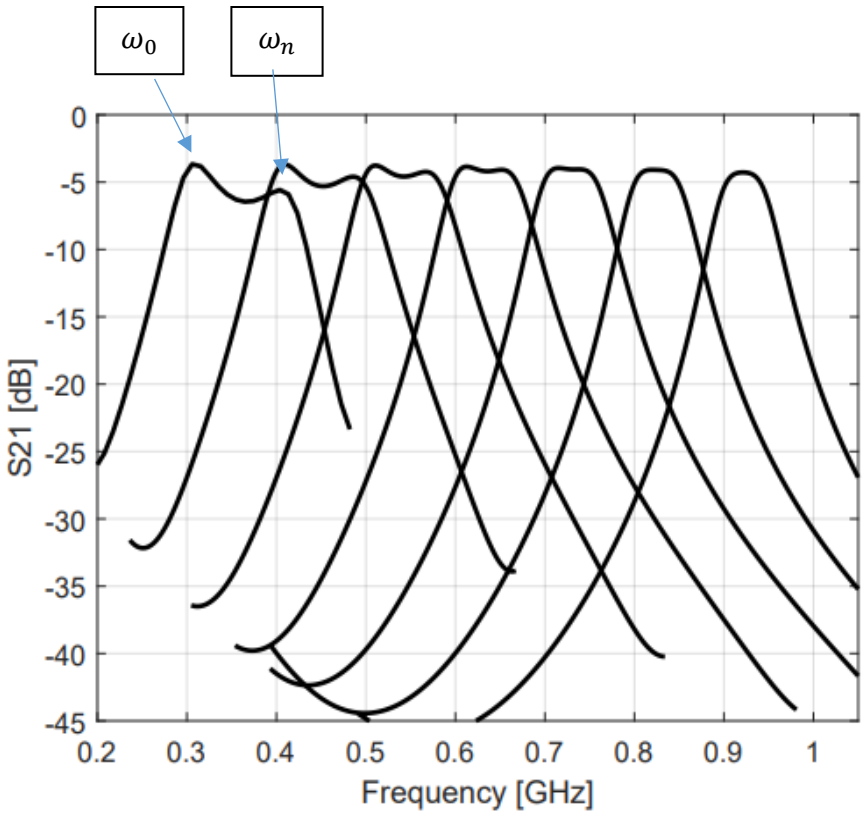


Figure 3-4 In band insertion loss of transmission-line 4path filter for different LO frequencies (W=300μm, C=40pF, L=3n)

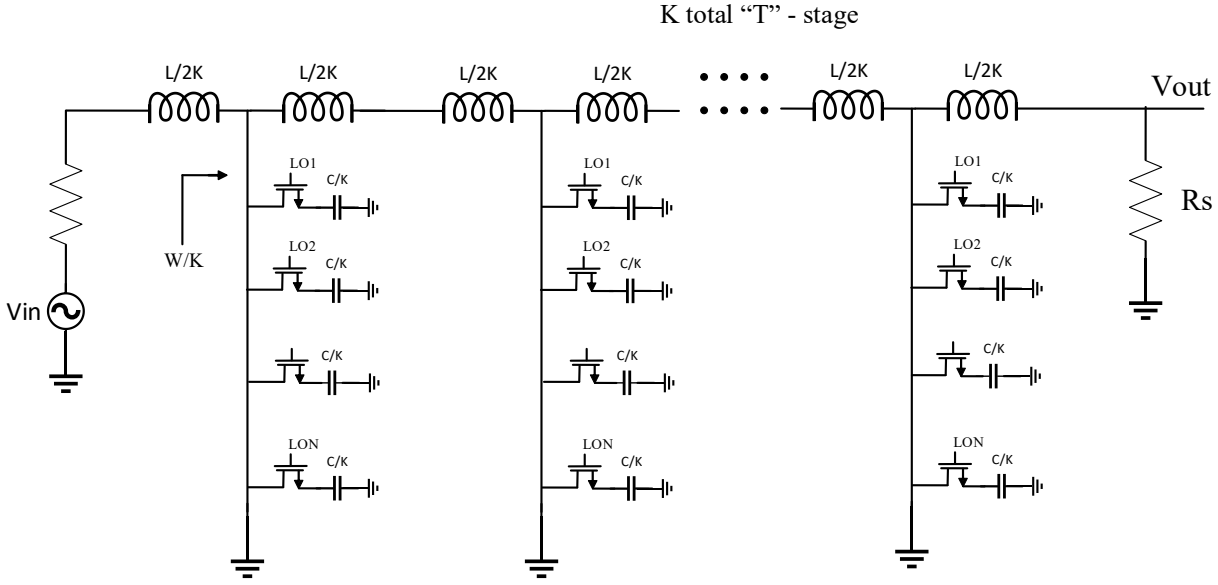


Figure 3-5 Schematic of 4-path transmission line filter with with K stages

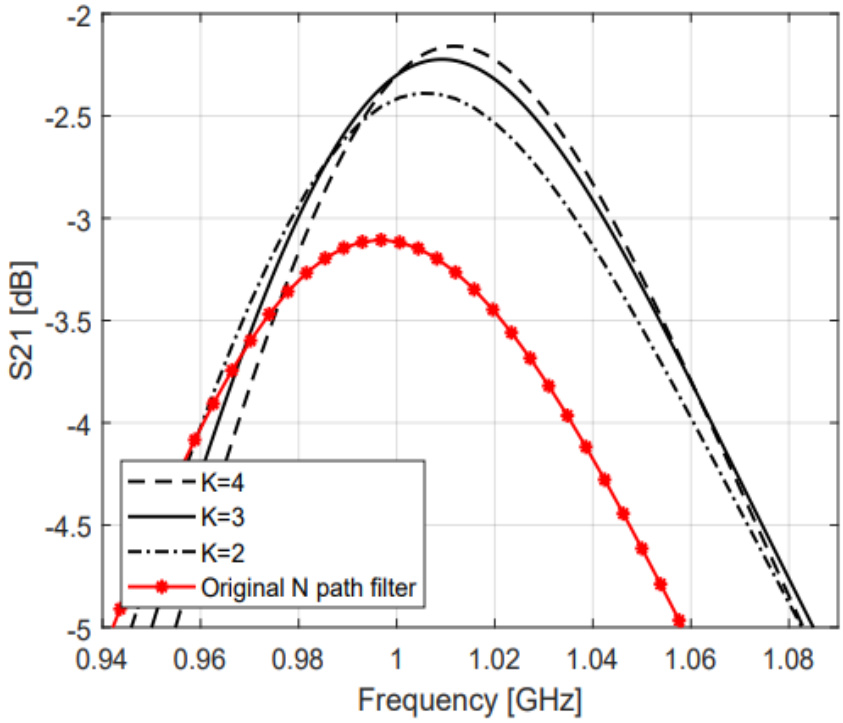


Figure 3-6 Effect of K (number of stages) on in-band insertion loss of transmission-line four-path filters (width of transistor=600u, C=20p, L=1.5n)

Transmission Line N-path filter out-of-band rejection is improved by low-pass filtering created by transmission-line inductance and switch ON resistance. In the original N-path filter, the out-of-band rejection is limited by $\frac{R_{sw}}{R_{sw}+R_s}$.

Figure 3-7 is the out-of-band rejection model for transmission-line N path filter. Frequencies far away from the clock frequency $(f \neq f_c)$ approximate the transfer function by calculating (3-5) [13], which is superior to a traditional N-path filter.

$$\mathbf{S_{21}} = \frac{\mathbf{8\,R_s K^{(2K+1)} R_{on}{}^{K}}}{\mathbf{S^{K+1} L^{K+1}}} \tag{3-5}$$

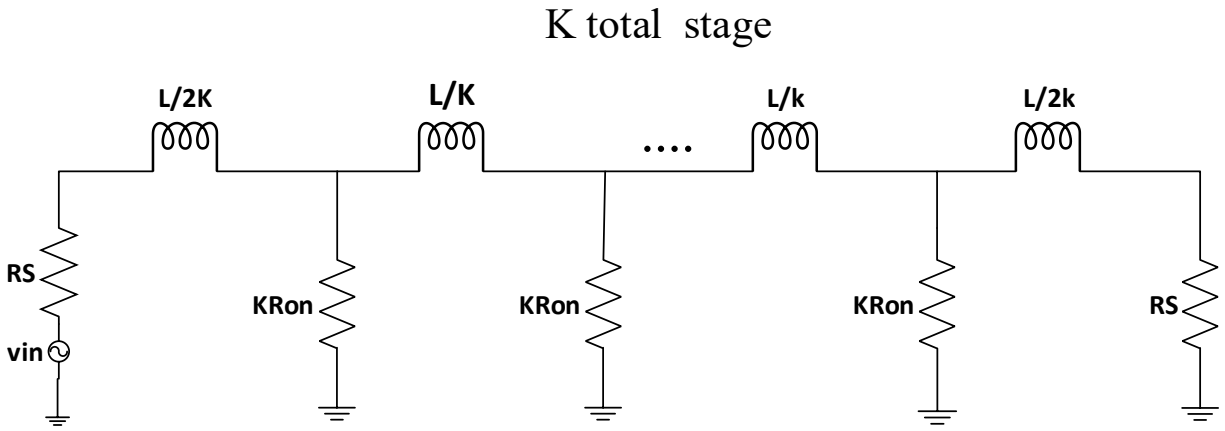


Figure 3-7 The out-of-band rejection model for T-line N-path filter [13]

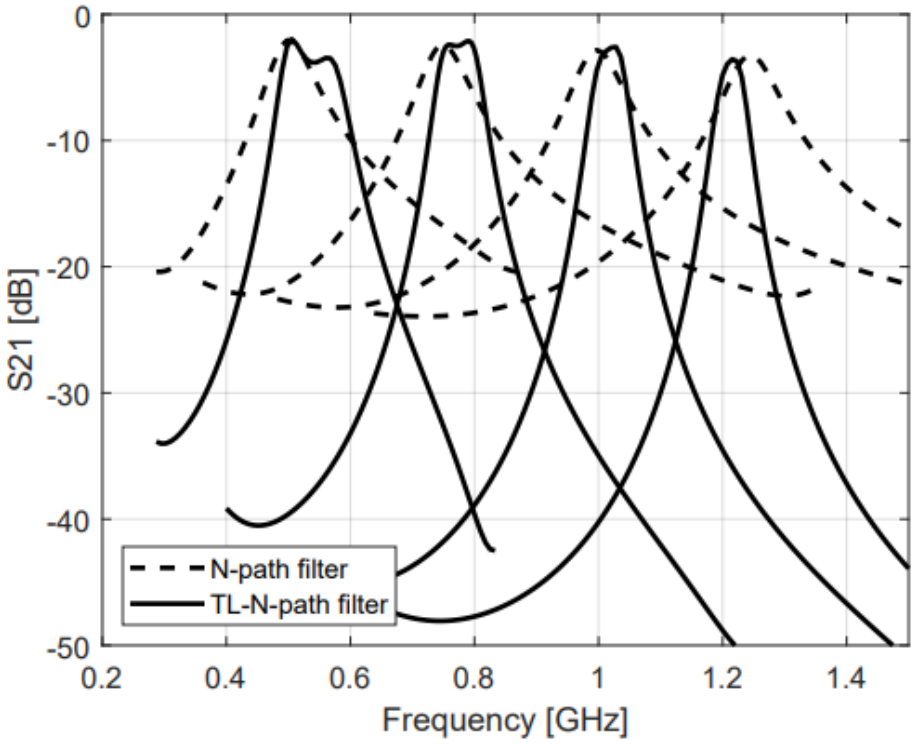


Figure 3-8 Simulated Transfer function as a function of LO frequency of four-stage (K = 3); transmission-line N-path filter in Figure 3-3 and single-stage traditional N-path filter in Figure 2-9(N = 4, W/L = 300u/120nm C=40p, L=3n)

Figure 3-8 shows the comparison between simulation result of the original 4-path filter and transmission Line 4-path filter transfer function by using PSS+PSP analysis. The transfer function of original 4-path filter shown in Figure 2-7 is simulated for different LO frequency. The transfer function of transmission line 4-path filter shown in Figure 3-5 is plotted for different LO frequency too, four ideal non-overlapping clocks drives the transistors for both original 4-path filter and transmission line 4-path filter. Figure 3-8 presents the out-of-band rejection improvement for transmission-line four-path filters over frequencies compared to the original N-path filter with the same component values.

3.1 Wideband Transmission Line N-path Filter

The four-path transmission-line filter is composed of ideal inductors and capacitors that must be replaced with real inductors and capacitors. CMOS8RF technology provides scalable, high-Q inductors with low parasitic capacitance. The inductor pcell offers substantial flexibility by changing its parameters. These parameters relate to the outer diameter, inductor coil width, configuration (single, parallel, or series), and the number of turns to achieve the desired inductance and performance. CMOS8RF technology offers five models of inductors which are: ind, inds, indp, symind and symindp. After comparing all types of the inductor, one notes that symind inductors are symmetrical with center taps, which have lower parasitic capacitance-to-substrate and higher Q compared to others.

The transmission-line N-path filters, in which the ideal inductors are replaced with the symind inductor, can provide less resistive loss. Less resistive loss results in better in-band insertion loss in the frequency response.

Due to the finite Q of the inductors, in-band insertion loss has some dependence on parasitic capacitance, so the inductor parameter should be chosen to minimize the parasitic capacitance of the inductors to reduce the effects of additional poles due to series transmission lines and parasitic capacitance. The inductor value is chosen so that it can absorb the switch's parasitic capacitance and improve in-band insertion loss.

IBM CMOS 8RF process features a variety of device including high quality metal-insulator-metal (MIM) capacitors and thick oxide nFETs with high breakdown voltages too. Capacitors are also replaced with MIM capacitors in TL N-path filter topology.

We use a transistor as a switch, thus allowing the switch's parasitic capacitance to be calculated or simulated based on the transistor width. We then chose the inductor's value so that it can absorb the switch's parasitic capacitance. The transmission line inductance and ON resistance of the switch causes a low-pass filtering effect that can improve the TL N-path filter's out-of-band rejection. The inductor's value should be chosen to also provide reasonable out-of-band rejection too.

Figure 3-9 shows Architecture of proposed transmission line N-path filter with using real inductor and capacitors. Input and output GSG are placed along midline at the right and left side of the chip and it is included in schematic to be more realistic.

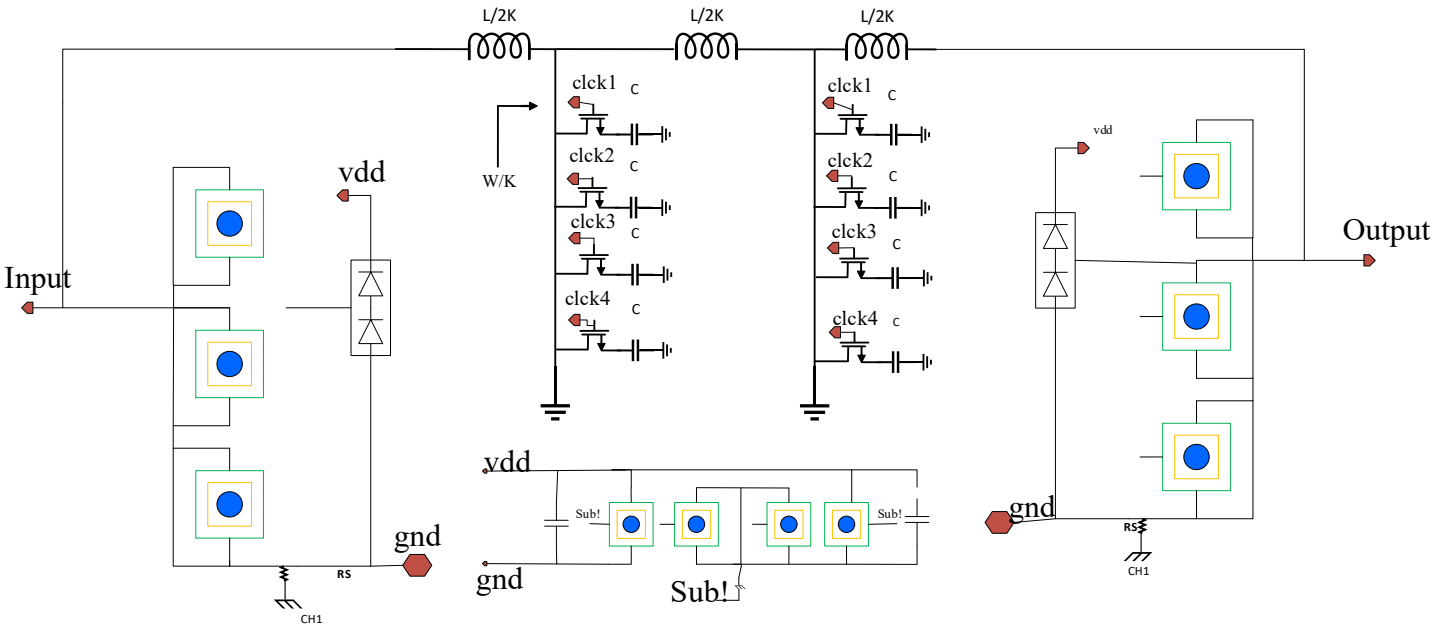


Figure 3-9 Architecture of the proposed transmission Line 4-path filter

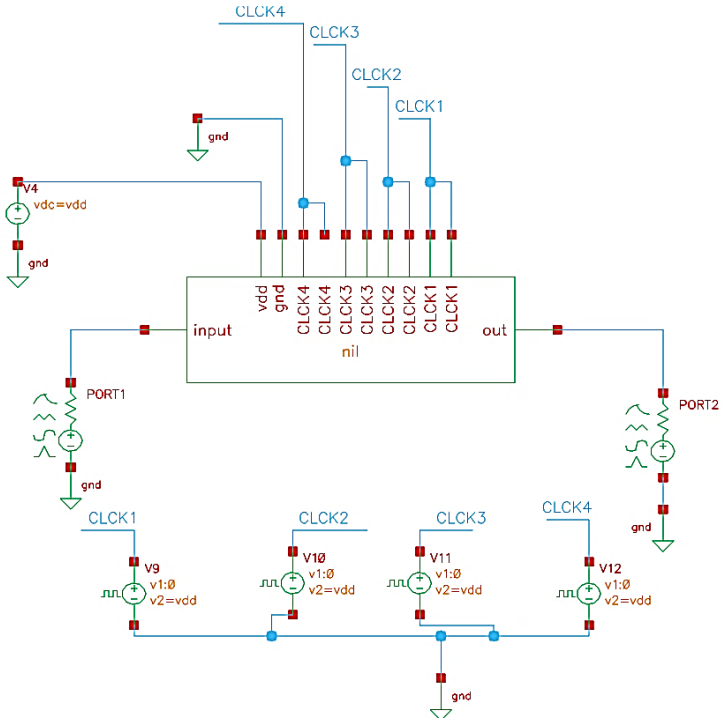


Figure 3-10 Test bench configuration for the proposed filter transfer function evaluation

Figure 3-10 shows the test bench configuration which is used to plot the transfer function of propose filter using PSS+PSP analysis. As you can see four non-overlapping clocks drive the transistors with finite rise time and fall time. Figure 3-11 shows the simulation result of the transmission-line four-path filter shown in Figure 3-9, which is tunable between 0.2 GHz and 1.1 GHz. In this thesis, our purpose is to increase passband bandwidth as far as we can, and to achieve a good in-band insertion loss and out-of-band rejection. Transmission-line N-path filter's bandwidths can change in comparison to LO frequency; it is no longer constant in the transmission-line N-path filter, unlike in traditional single-stage shunt N-path filters for which bandwidth is constant. In the proposed wideband TL N-path filters, for instance, the bandwidth differs between LO=500MHz and LO=1GHz. The reason for this difference is because a transmission-line N-path filter, has two poles ω_{lo} and ω_n . ω_n moves toward ω_{lo} as LO frequency increases. This movement explains why bandwidth changes across different frequencies.

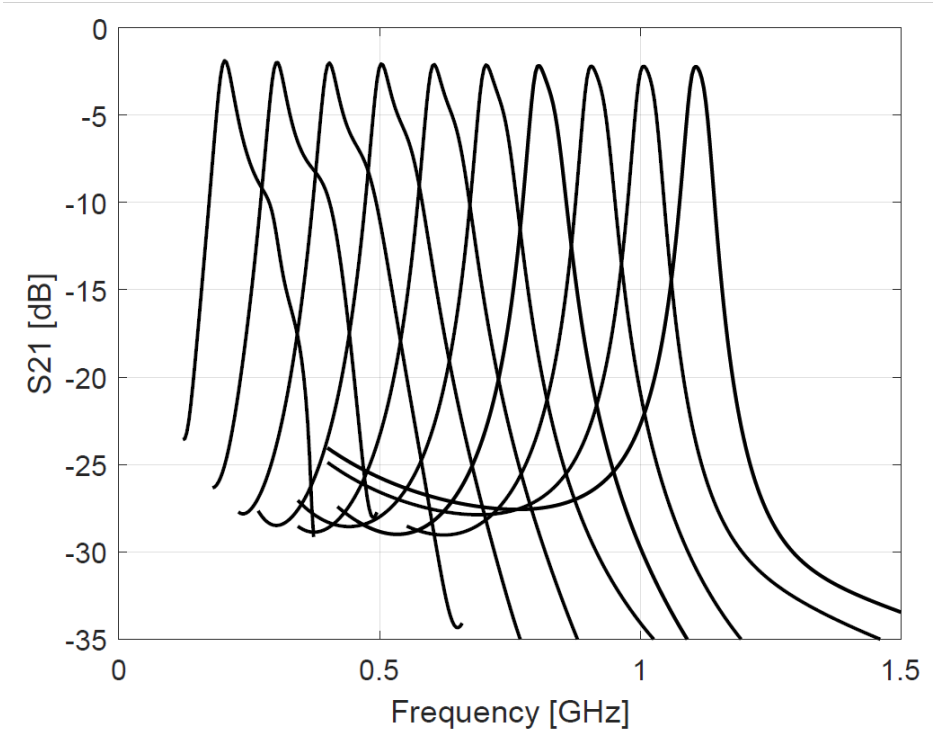


Figure 3-11 Simulation results of the proposed filter (width of transistor =300μm K=2, C=40p, L=3n)

We obtain different bandwidths for different LO frequencies. Overall, for a traditional N-path filter, bandwidth is constant over the frequency range, but transmission-line N-path filter bandwidth changes over frequency change.

Figure 3-12 describes the effect of L and C on the bandwidth of the transmission-line N-path filter at 1 GHz. The inductor value is kept constant (L=3n) to permit investigation into the capacitor's impact on the transmission-line N-path filter's bandwidth. The capacitor's value is kept constant (C=20pF) to permit observation of the inductor's performance. These observations show that the value of L and C are inversely proportional to the bandwidth of the transmission-line N-path filter. Increasing inductor and capacitance value reduces the filter's bandwidth. The value of the inductor and capacitor should be small to increase the filter's bandwidth. However, reducing the inductor and capacitor results in increased in-band insertion loss and reduced out-of-band rejection. C = 20 pF, and L = 3nH are then chosen for final design.

The proposed wideband two-stage four-path transmission-line filter and the test bench configuration shown in Figure 3-9 and Figure 3-10, is used to simulate the transfer function of the filter by using PSS+PSP analysis. Again, ideal four non-overlapping clocks drive the transistors with finite rise time and fall time. Figure 3-11 shows the simulation results of from a 0.1 to 1.2 frequency range

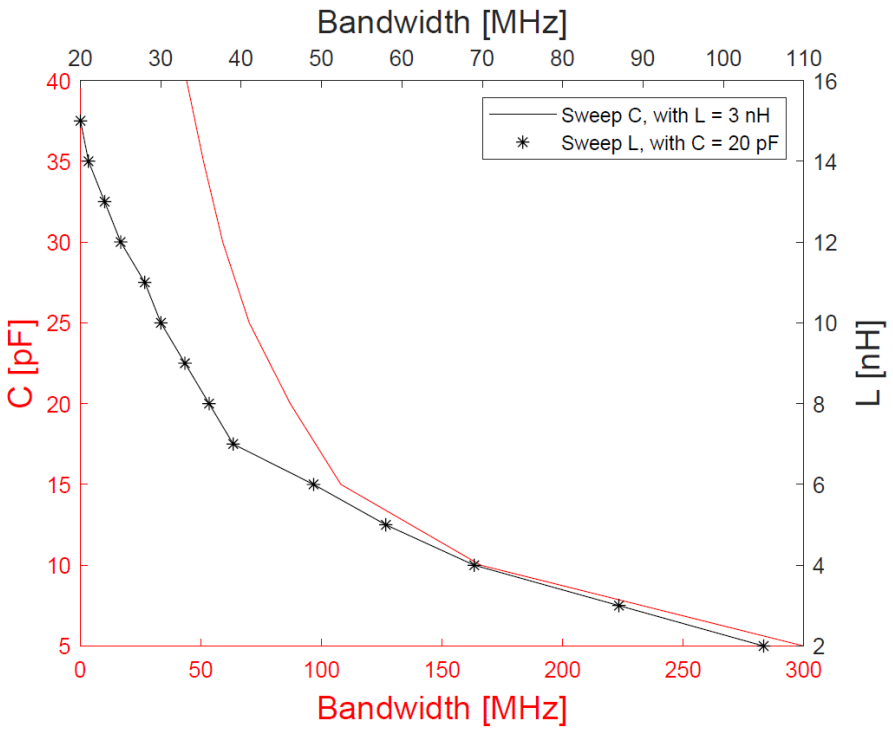


Figure 3-12 Impact of L, and C on bandwidth of transmissions line four-path filter at 1 GHz

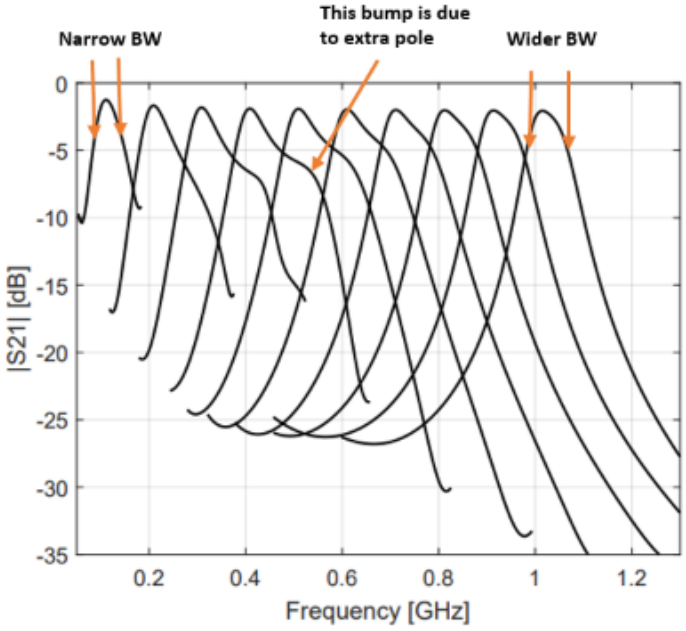


Figure 3-13 Final simulation results of the proposed wideband tunable four-path filter from 0.1GHz to 1GHz. (K=2 N=4 L=3nH, C=20pF, Width of switch =300μm R_S=50ohm)

3.2 Noise Analysis

The output noise power of the N-path filter is mainly caused by the source and switch resistance. In transmission line N-path filter, the main contribution to the noise figure is due to the loss of input signal that is up-converted to harmonics of the clock and dissipated at the port impedance and limited Q of inductors.

The inductor's losses may be modeled as an ideal inductor with series resistance contributing to the noise figure. So, to reduce the noise contribution from the inductors, its series unwanted resistance should be minimized. The design's inductor parameter is chosen so that it increases its quality factor, thus reducing series resistance to reduce the noise. Figure 3-14 shows the noise figure of the proposed filter over frequency. The proposed filter and its test bench configuration shown in Figure 3-9 and Figure 3-10 is used to simulate the noise figure of the filter by using PSS+PNOISE analysis. Ideal four non-overlapping clocks drive the transistors with finite rise time and fall time.

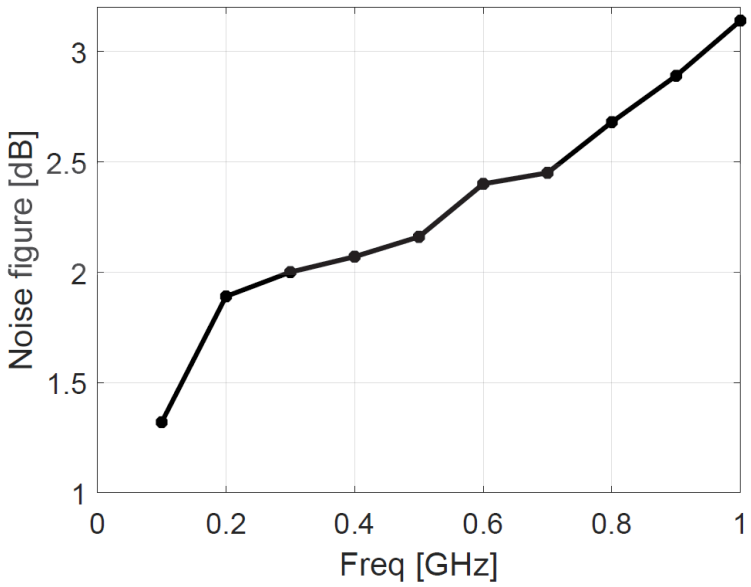


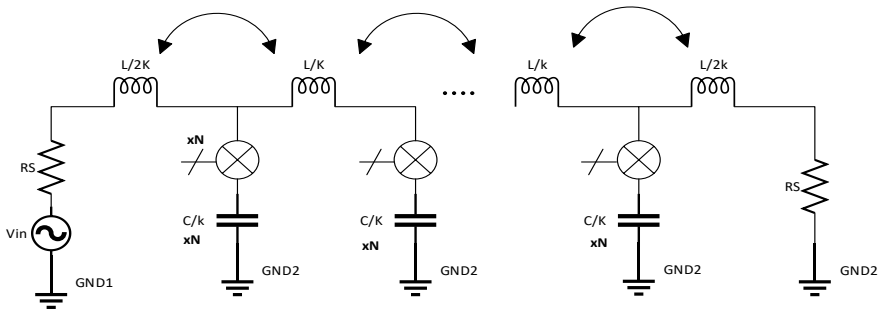
Figure 3-14 Noise figure of the proposed filter using an ideal clock

(N = 4, W/L = 300u/120nm C=20p, L=3n)

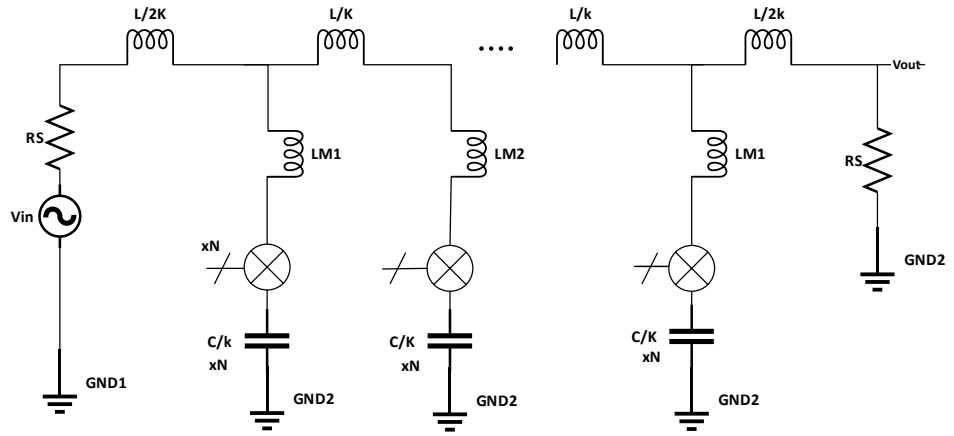
3.3 Inductor Coupling

The changing magnetic field that surrounds the inductor results in an induced electro-magnetic field (EMF) within itself that is generated by the inductor. The fact that this EMF is induced in the same circuit where the current is changing is called self-induction, (L). If the EMF is induced into an adjacent coil situated within the same magnetic field, the EMF is said to be induced by mutual induction. Mutual induction is the operating principle of any electrical component that interacts with another magnetic field. Inductors close to each other therefore create mutual coupling, which can be modeled by an induced inductance. In the case of transmission-line N-path filters, the filter's input capacitive response resonates with induced inductance to create a transmission zero. To shows the effect of the inductor coupling ,the proposed filter and its test bench configuration shown in Figure 3-9 and Figure 3-10 is used to simulated the transfer function of the filter with and without induced inductance by using PSS+PSP analysis. Ideal four non-overlapping clocks drive the transistors with finite rise time and fall time.

Figure 3-15 shows the effect of inductor coupling in a transmission-line N-path filter, which is represented by LM_N in Figure 3-15 b).Figure 3-16 shows the effect of inductor coupling in the filter's transfer function. The in-band insertion loss is degraded by adding induced inductance. The induced inductance also resonates with input capacitance and creates transmission zero in the frequency response.



a)



b)

Figure 3-15 a) Coupling between inductors in transmission-line N-path filter. b) T-line N-path filter by considering coupling inductance

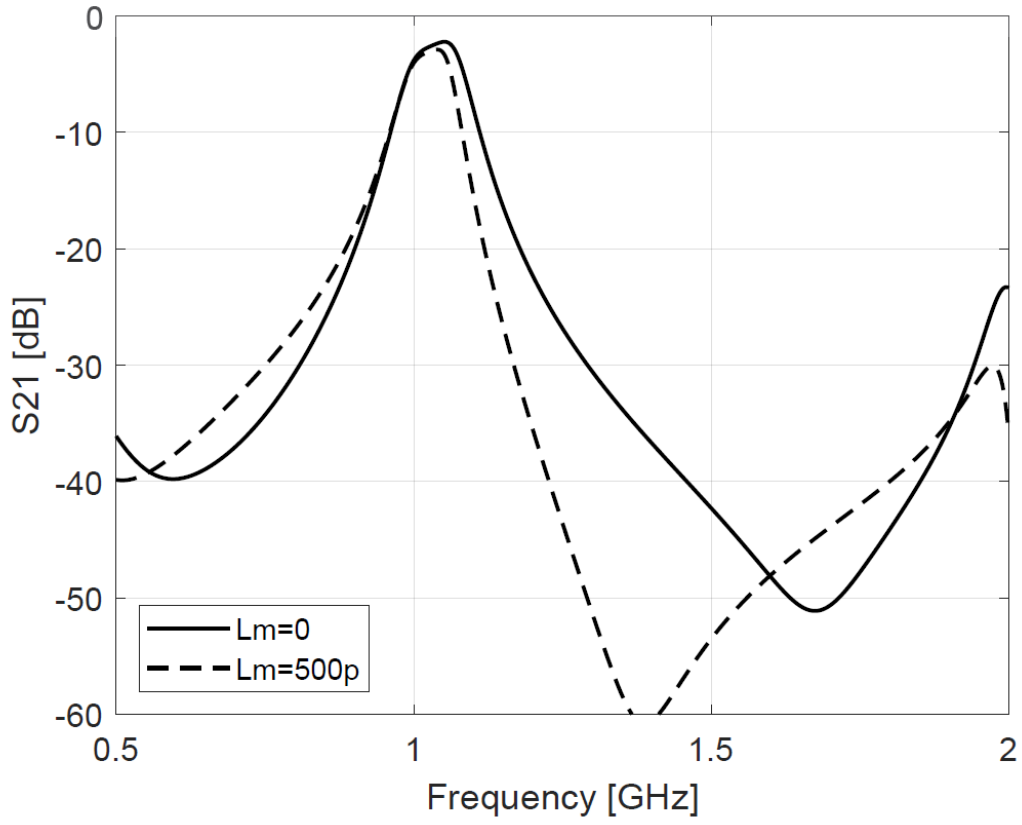


Figure 3-16 Simulated N-path filter with and without series induced inductance (fLO = 1G, K = 2, N = 4, LM1 = 500 pH, Cbb=20 pF, W = 300 µm)

3.4 Summary

In this chapter, an integrated tunable bandpass filter based on an N-path network is analyzed. Although an N-path filter provides a high Q tunable bandpass filter, it suffers from some limitations such as parasitic capacitance of the switch, switch resistance, harmonic folding, and poor filter shape, etc. Switch parasitic capacitance and switch resistance limits in-band insertion loss and out-of-band rejection of the filter respectively.

The transmission line N-path filter removes the tradeoff between out-of-band rejection and in-band insertion loss of the original N-path filter by absorbing parasitic capacitance of the switch into a transmission line that improves in-band insertion loss. Also, low-pass filtering created by the switch on-resistance and transmission line inductance improved the out-of-band rejection.

In Transmission Line N-path filter, the inductance values should be determined so that it can absorb the parasitic capacitance of the device(switch) which result in improving in-band insertion loss, and also improve the out-of-band rejection of the filter simultaneously.

The transmission line N-path filter also provides high-order filtering that causes sharp filtering around our required frequency. In a transmission line N-path filter bandwidth can change versus LO which doesn't happen in traditional single stage shunt N-path filters (the BW is traditionally constant with LO). The effect of L and C on transmission line N-path filter bandwidth is investigated. The inductor and capacitor values are inversely proportional to the bandwidth of the transmission line N-path filter and decreasing L, and C results in higher bandwidth. The value of L and C should be optimized so that we can achieve the maximum in-band bandwidth around our desire frequency with reasonable in-band insertion loss and out-of-band rejection.

Chapter 4. Implementing Wideband Transmission-Line N-path filters

The wideband transmission line N-path filter was presented in Chapter 3. The transmission Line N-path filter improves the tradeoff between in-band insertion loss and out-of-band rejection of the filter. The inductance value is designed so that it absorbs the parasitic capacitance of the switch that can improve in-band insertion loss, also low pass filtering created by on-resistance of the switch and inductance can improve out-of-band rejection. Therefore, the inductance value should be chosen to improve the in-band insertion loss and out-of-band rejection simultaneously. The effect of the L and C were investigated on the bandwidth of the filter. So, the L and C value is chosen to achieve maximum bandwidth at our desired frequency(1GHz) and improve in-band insertion loss and out-of-band rejection.

The four-stage (K = 2) transmission-line four-path filter was implemented in a 130 nm bulk CMOS process with a schematic diagram shown in Figure ***3-9***. A single-ended design was chosen to facilitate broadband tuning without requiring a balun. A single-ended design was also chosen because it exhibits an even and odd harmonic passband [4].

The process technology used in this work is the IBM CMOS8RF process, a high-performance 130 nm CMOS-based technology with substrate conductivity of 1-2 Ω cm and based on a no epitaxial p-doped substrate. The process stack contains one poly layer and eight metal layers. Those eight metal layers consist of three thin copper layers, two thick copper layers, and three RF metal layers, which are composed of low-resistive thick copper, and low-resistive thick aluminum. The M1 ground plane is chosen to isolate the inductor from substrate noise and prevent induced currents in the substrate

4.1 Clock Generation

A high-frequency clock generator with four non-overlapping clock phases will drive the proposed wideband four-path transmission-line filter. This section explains the design for a high-frequency four-phase non-overlapping clock generator with a 25% duty cycle. The clock generator configuration is realized in a CMOS130 nm process and is shown in Figure 4-1.

An external off-chip clock is applied at four times the switching frequency. The external clock is divided by four by using a divider. The divider is realized with a D flip-flop based on transmission gates. The D flip-flop divides the external clock by four and then the AND gate between node A and B generates the clock's 25% duty cycle. In other words, to generate a 25% duty cycle clock, the output and a delayed version of the output is sent to an AND gate to reduce the clock's propensity for overlapping. D flip-flop based on transmission gates has been used due to their lower power consumption and higher speed. The four-phase divider output is then buffered before capacitively driving the gates of the switching transistors.

Out1, Out2, Out3, and Out 4, which are represented at the bottom of Figure 4-1, are the four non-overlapping clock signals with a 25% duty cycle that drive the four-path filter. The external off-chip clock, applied at four-times the switching frequency, is depicted at the top of Figure 4-2. If the adjacent clock signals overlap, the result would be a reduction of voltage gain, quality factor, and linearity of the filter.

φ_0 , φ_{90} , φ_{180}, and φ_{270} are the four clock phases that still have some overlap. Since the N-path filter requires non-overlapping clocks, series inverters are used right after φ_0 , φ_{90} , φ_{180}, and φ_{270},which causes the output of the clock generator, to be non-overlapping.

In symmetric inverter, rise time and fall time should be the same, which requires that PMOS and NMOS have same transconductance. The size of the PMOS transistors of inverters should be three times bigger than the NMOS transistors because PMOS has lower mobility. In first inverter (inverter 1), the PMOS is 3 times larger than NMOS for making equal resistance of both transistor, which result in the same rise time and fall time. However, in second inverter (inverter 2), PMOS is the same size as NMOS, in this case rise time and fall time are not the same anymore, by this way we can delay the edge of the pulses, so that they can provide four non overlapping clocks.

A tapered buffer is used to drive the transistor gate, which carries a large capacitive load due to the transistor's parasitic capacitance. The output buffer design was based on using a string of inverters where each has an increasing width compare to the last. By sizing up an inverter, its delay will be reduced, and input capacitance may be increased. The number of stages in the buffer depends on the load capacitance. In this design, since load capacitance is very large (load capacitance is the parasitic capacitance in the gate of the transistor which is large due to size of the transistor), size ratio between inverters in the chain is five. In terms of achievable speed, we can derive the optimum number of inverters. Each inverter drives five times the capacitance above its own input node. The output buffer in our design methodology consists of buffer 1Y, 5Y, and 25Y, where Y is the size of the original inverter.

A careful wiring layout is required to ensure that the external clock drives the gates of all D flip-flops. All D flip-flops should be at the equidistant from the master clock, so that all see the clock at the same time. The multiphase clock generator's maximum frequency is limited by the process technology, which must use higher-frequency digital logic to process a higher number of phases.

Figure 4-2 shows the final layout of the high frequency multiphase clock generator with D flip flop architecture at the top.

The duty cycle defines the ratio of the active(up) time to the entire cycle time. At high speed with finite rise time and fall time, the following stage does not turn on or turn off instantly at some exact voltage, so the effective duty cycle is difficult to determine. The apparent duty cycle would change depending on the voltage and what frequency is used. The zero-volt voltage is considering defining the duty cycle. The effective duty cycle is reduced by increasing the switching frequency. The reason is the rise time and fall time of the multiphase clock consist a significant portion of the pulse with increasing switch frequency which result in the increased insertion loss.

Although the clock generator is supposed to generate a 4-non overlapping clock with a 25% duty cycle, however, the produced clocks have non-zero rise time and fall times. So, the generated clocks duty cycle might be a little bit different than 25%. Figure 4-3 shows the post-layout simulation result of the clock generator. This layout shows four non-overlapping clocks for different external clocks where $F_{externalclock} 1, 2, 3, 4$ GHZ, respectively. For instance, the duty cycle of the generated clocks for $F_{externalclock} = 2\text{GHz}$ is about 26%. Post-layout simulation, after RLC extraction, and EM simulation, further reveals that the proposed high-frequency configuration generates four non-overlapping signals for an input frequency of up to 4 GHz.

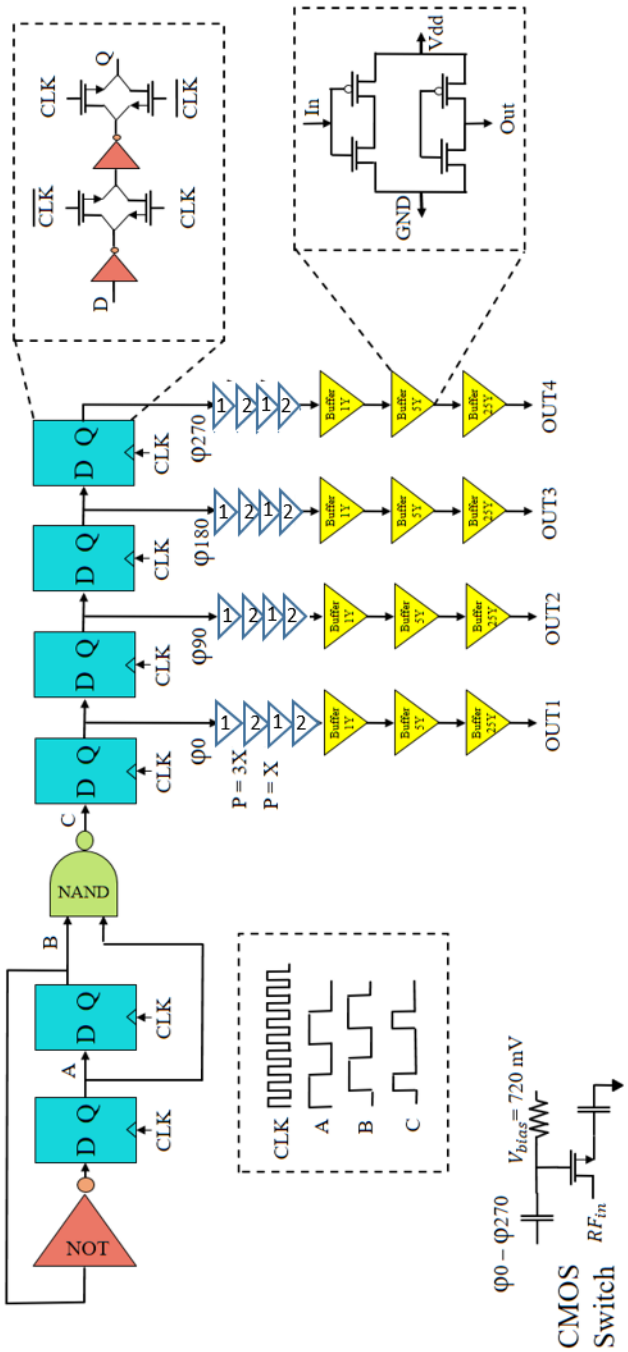


Figure 4-1 Configuration of high-frequency multiphase clock generator

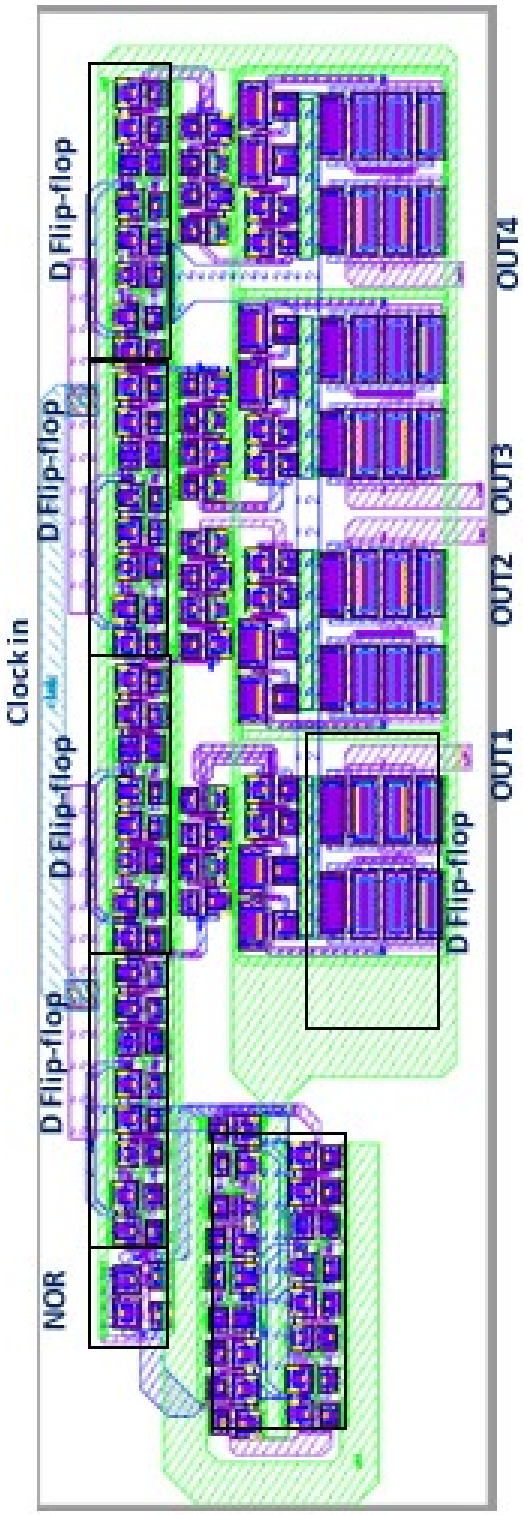


Figure 4-2 Final Layout of high frequency multiphase clock generator

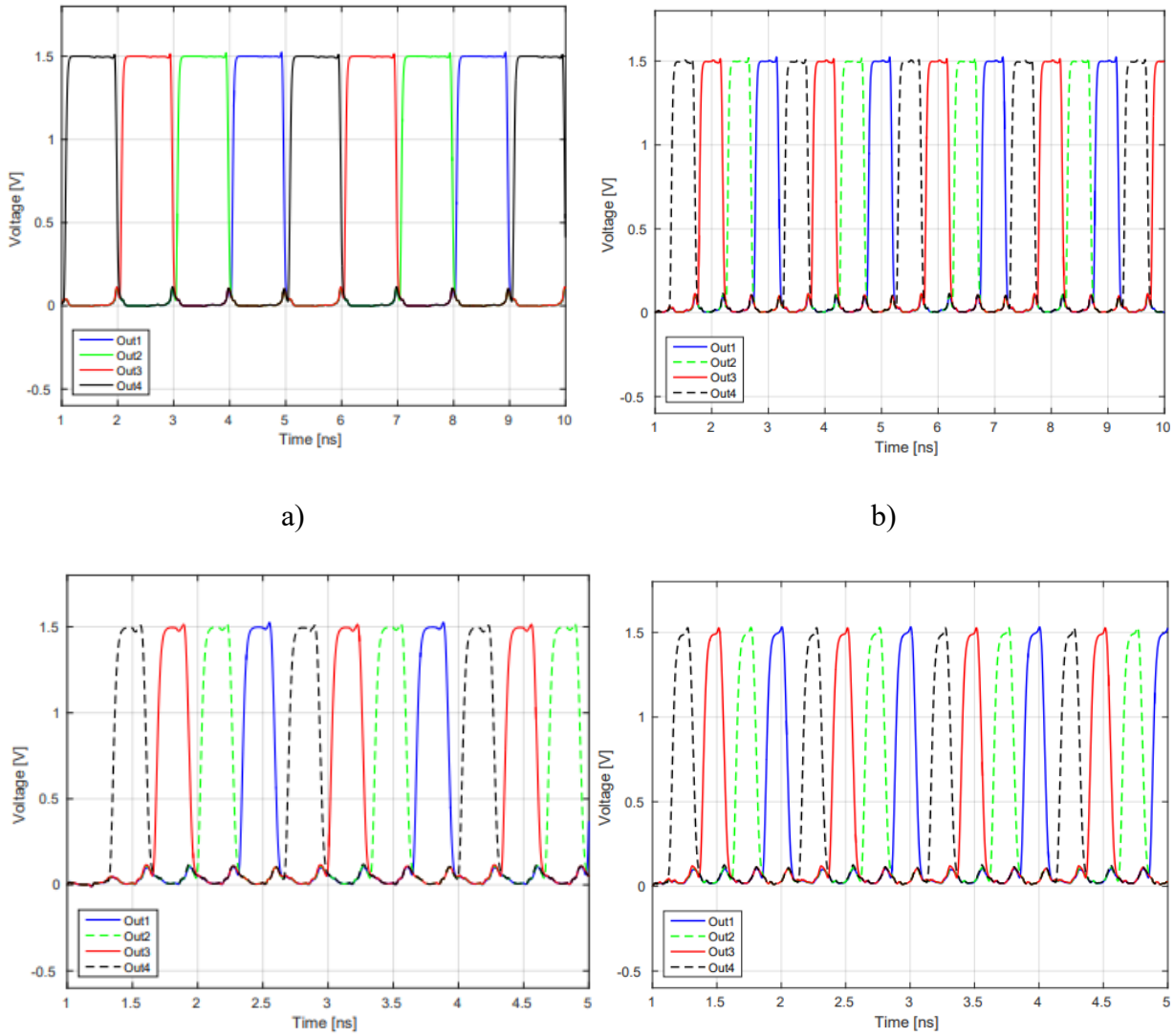


Figure 4-3 Post simulation (RLC extraction) results of clock generator a) 1 GHz, and b) 2 GHz. c) 3GHz, d) 4GHz

4.2 Implementing the Transmission-Line N-path Filter

In this section, the transmission-line N-path filter architecture's final layout is presented, and it is divided into two parts: an analog part and a digital part. The analog part is based on the transmission-line N-path filter layout; the digital part is the clock generator layout, which should drive the transistors' gates in the filter. The inductor's ring protects the inductor from the rest of the circuit, so there is no further need to protect the digital from its analog counterpart. As discussed above, our proposed filter consists of three inductors, eight switches (transistors), and eight capacitors.

4.3 Floor Planning

The proposed chip's floor plan was laid out in the graphic form. The chip's two parts were separated by function. The analog part, which consumes more area than the digital part due to the presence of inductors, was situated at the chip's center. The analog part contains inductors, transistors, and capacitors. An initial floor plan is shown in Figure 4-4.

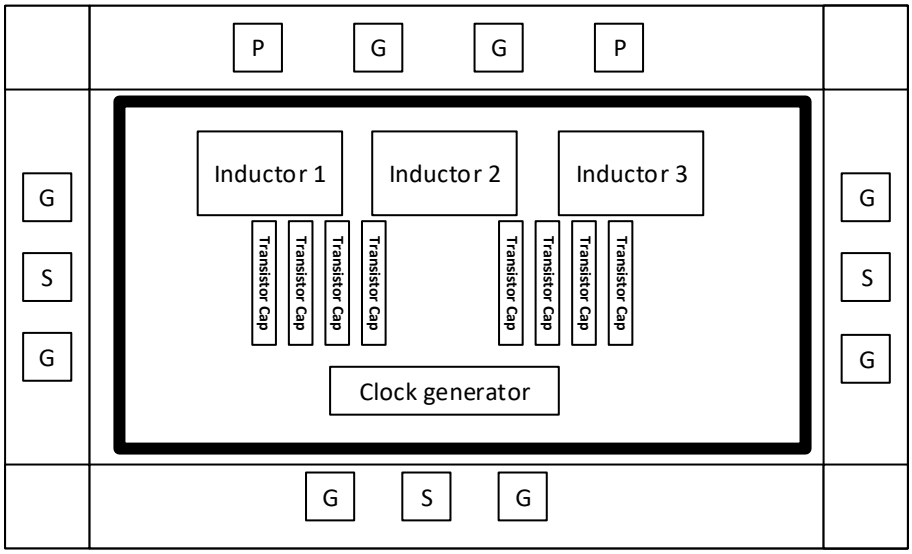


Figure 4-4 Initial floor plane with pad allocation

A two-stage transmission-line four-path filter consists of eight transistors and capacitors, three inductors, and a clock generator, which generates four non-overlapping clocks for each stage. The clock generator's output (out1, out2, out3, and out4) are connected to the transistor's gates. The respective node connections were established so that the same phase shift occurs between the output of the clock generator to the gate of the transistors.

The design is completed with the component module and its reference layout is generated. The module layouts are first arranged based on the floor plan; the respective connections are created using the top three metals to reduce losses.

CMOS 130nm technology is used to implement the proposed wideband four-path filter. The technology provides a variety of devices, such as: thick oxide NFETs with high breakdown voltages; a high Q inductor with low parasitic capacitance; and high-quality metal-insulator-metal (MIM) capacitors. MIM capacitors are used in the layout. The MIM aspect ratio is 3:1 to create accurate models. To achieve the best Q in a MIM cap, the L dimension should be kept short so that (minimum L = W/3). Symmetrical inductors are used in the layout because they have the highest Q and the lowest parasitic capacitance to the substrate of all the inductors in this technology.

Components are placed close to each other to reduced die area and parasitic capacitance and resistance. First, all the transistors and caps should be as close as possible to each other to be able to make connections between the transistor's gates and the clock generator output (out1, out2, out3, and out4) with the same phase delay. It should be mentioned that if transistors are very close together, they might cause coupling. EMX simulation is used to determine optimal transistor placement without causing coupling. All connections between the transistor's gates and clock generator output are designed so that each provides the same phase delay.

Inductor parameters should be chosen so that it provides the highest quality factor and less parasitic for specific inductor value. EMX simulation is conducted to extract the expected inductance and quality factor at the desired frequency of 1 GHz for various symmetrical inductor dimensions.

In this thesis, our purpose is to design a tunable filter that can provide wide bandwidths around the frequency of 1 GHz with reasonable in-band insertion loss and out-of-band rejection. The size of the transistor, capacitors, and inductors is chosen so that it passes our requirement.

Figure 4-5 shows the final layout of the proposed wideband four-path filter, in a 1×1.5 mm die with CMOS 130-nm technology. The three bottom pads are reserved for GSG probe for signal input. The three top pads are reserved for the GSG probes for the filter's output. The four leftmost pads are reserved for the power supply (VDD-, and VDD+). The three rightmost pads are reserved for GSG probing of the clock signal. GSG probe pads are allocated a 150-µm-wide perimeter from the process chip ring.

The separation between the inductors is increased to reduce mutual coupling between the inductors. EMX simulation shows that increasing the separation to 80 µm results in mutual coupling of less than -100 dB in the desired frequency range, which is good enough for this application. Figure 4-6 a) shows the EMX simulation configuration and simulated mutual coupling between the two adjacent inductors. In the EMX simulation, each inductor has two ports. Mutual coupling (|S31|) is shown in Figure 4-6 b). Several iterations were done during the design before converging to the final fabrication version.

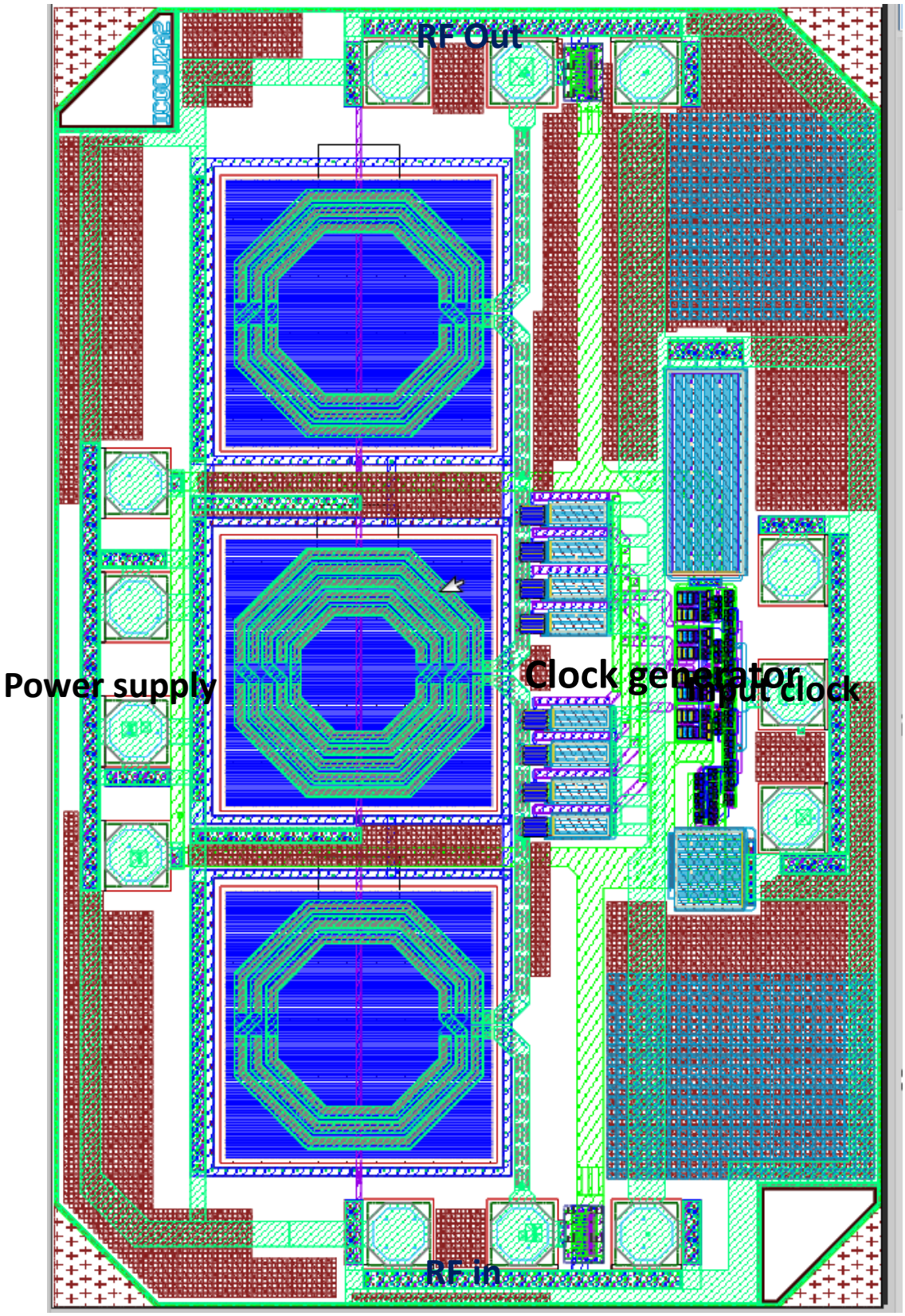
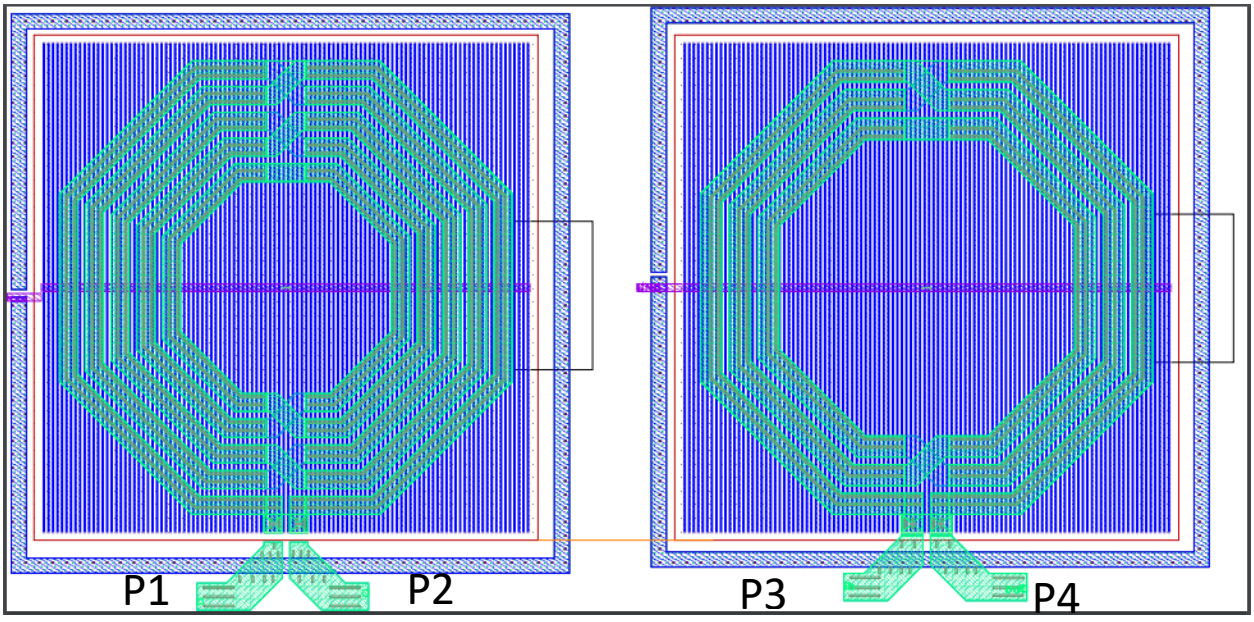


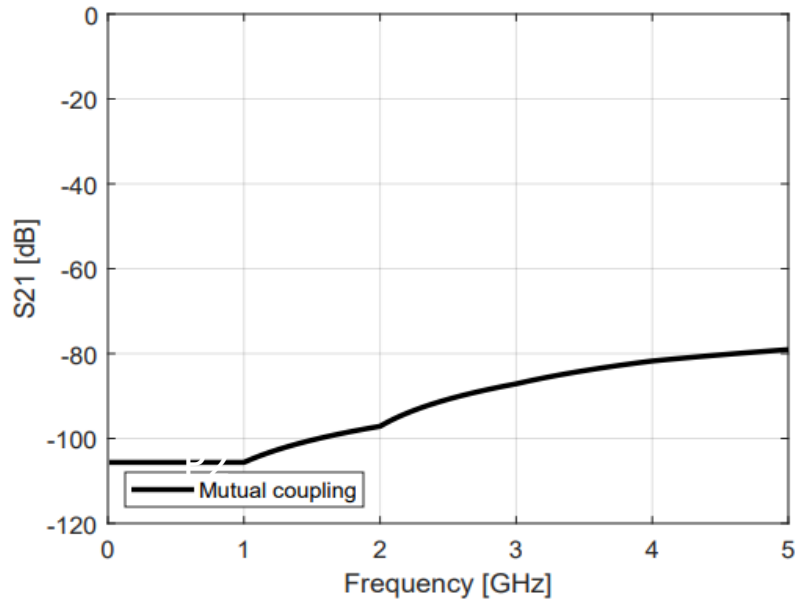
Figure 4-5 Final layout of the proposed wideband 4-path filter (1mm× 1.5 mm)

The final implementation was connected to a virtual test bench and large signal analysis was done by using PSS+PSP simulation to evaluate the design's performance.

Figure 4-7 shows the simulation results for the parasitic RLC extracted version of the proposed filter shown in Figure 3-9 from 0.1G to 1G frequency range in Cadence software by using PSS+PSP analysis. The simulation is done for whole circuit including the filter and on-chip clock generator. The on-chip clock generator is fed with an ideal square wave clock with zero rise times and fall times. The on-chip clock generator generates four non-overlapping clocks as shown in Figure 4-3. The duty cycle of generated clocks is depending of the switching frequency we use and it is different for different switching frequency. The bandwidth varies from 70 Mhz to 110 MHz over the frequency range. There is a slight difference between schematic simulation and RLC extraction simulation due to additional parasitic found in post layout. Figure 4-8 shows that the bandwidth of the filter is around 80MHz at 1GHz.



a)



b)

Figure 4-6 a) EMX simulation setup for mutual coupling between the 2 adjacent inductances, b) Simulated mutual coupling result (|S31|)

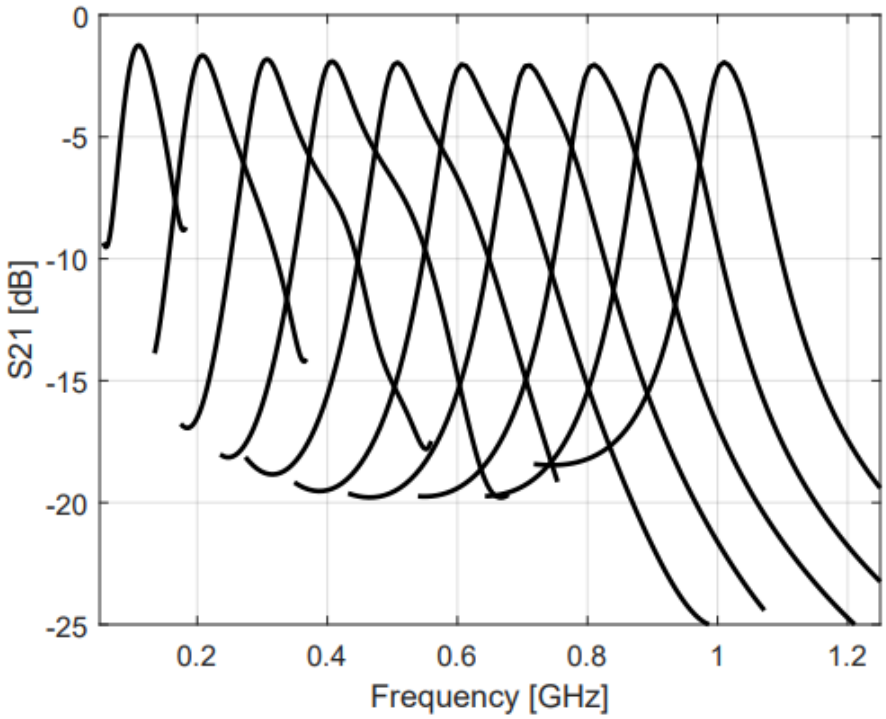


Figure 4-7 Final post layout simulation results of the proposed wideband tunable four-path filter from 0.1GHz to 1GHz. (K=2, N=4, L=3nH, C=20pF, Width of switch =300µm R_s=50ohm).The on-chip clock generator in circuit is fed with square wave signal with zero rise time and fall time

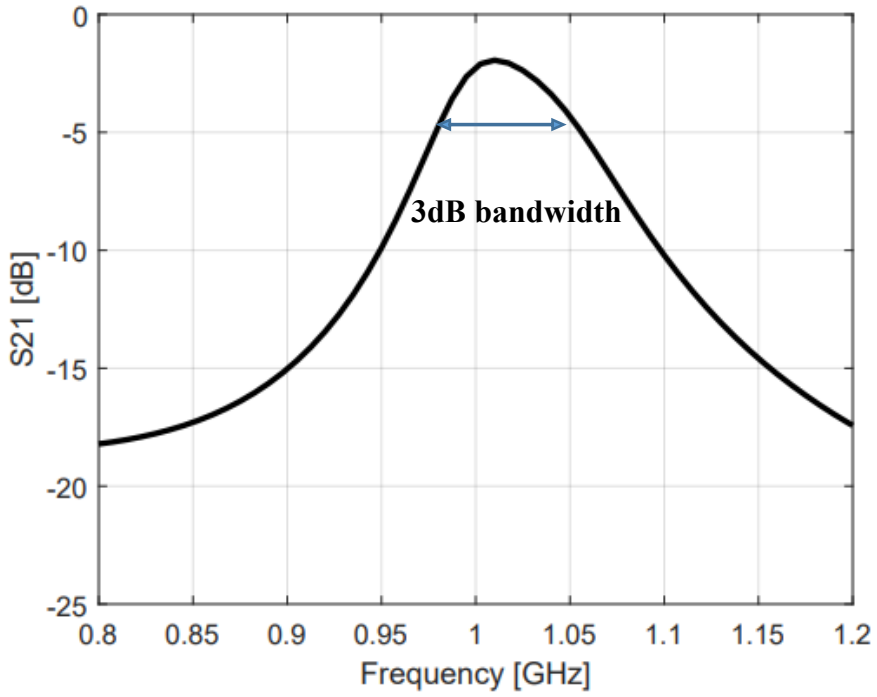


Figure 4-8 Final post layout simulation results of the proposed wideband tunable four-path filter at 1 GHz

A final parameter values table and their reference design kit models are provided in Table 1 and Table 2. Tables are sorted by active and passive components.

Table 1 Active Component Summary –Final Design

Parameter	M1/M2	M3/M4	M5/M6	M7/M8	Units
Component Name	nfet_rf	nfet_rf	nfet_rf	nfet_rf	-
Multiplicity	3	3	3	3	-
L_{gate}	120	120	120	120	nm
N	50	50	50	50	fingers
W_{finger}	2	2	2	2	µm
Total width	300	300	300	300	µm

Table 2 Passive Component Summary Final Design

Parameter	C1/C2/C3/C4	C5/C6/C7/C8	Units
component Name	mimcap	mimcap	-
Capacitance value	20	20	pF
Length	57	57	µm
Width	171	171	µm
	L1/L3	L2	
Component name	symindp	symindp	
Outer dimension	300	300	µm
Coil width	14	12	µm
N turn	3	5	µm
Space	5	5	µm

Table 3 Performance summary and comparison

	This work	[1]	[27]	[28]	[29]
CMOS Tech	130nm	65nm	65nm	65nm	65nm
Frequency range	0.1-1	0.1-1	0.1-1.2	0.05-2.5	2
NF (dB)	3.2	3-5	2.8	2.9	5.8
BW(MHz)	100	35	8	0.35-20	4
Filter order	7	2	6	-	6
V_{DD}(Volts)	1.2	1.2	1.2	1.2	1.2/2.5

Table 3 summarizes the performance and compares it to other designs from the literature. As you can see, in this work bandwidth is significantly higher than what has been observed in other designs. It should be noted that the bandwidths reported in this work are based on simulation results but the number for the others are based on measurements. As a result, the comparison may not be completely fair, but is shows the potential of this method.

4.4 Summary

This chapter presents a high-frequency 4-phase non-overlapping clock generator with a 25% duty cycle to drive the 4-path filter. An external off-chip clock is applied at 4-times the switching frequency. Post layout simulation of the proposed clock generator, after RLC extraction, and EM simulation shows that the proposed high-frequency configuration generates 4 non-overlapping signals with 23% duty cycle for an input frequency up to 4 GHz. The wideband transmission line N-path filter is analyzed and implemented in a 1×1.5 mm die with CMOS 130nm technology. The proposed filter design is done by using a component module. The module layout is created based on the floor plan. The layout inductors and capacitors are replaced with symindp inductors and MIM caps respectively. The separation between inductors is 80 μm result in mutual coupling less than -100 dB around the desired frequency.

To simulate the frequency response of the proposed filter, a large-signal analysis is done by using PSS+PSP simulation. The post-layout simulation shows the filter is tunable from 0.1G to 1G frequency range and the bandwidth varies from 70MHz to 110Mhz over the frequency.

Chapter 5. Measurement Result and Analysis

This chapter presents measurement results and analysis. Test apparatus is also reviewed.

5.1 Test Apparatus

The test was completed at Carleton University's Department of Electronics.

The test Apparatus consisted of:

- a probe station equipped with a 3p sets of GSG and one set of GSSG probes and coaxial cable to provide RF stimuli.
- an Agilent network analyzer (HP 8720ES); and
- a Rhode and Schwarz signal generator (SME06).
- Power supply (E3630A)

5.2 Measurement Test Bench

The measurement was performed for a small signal analysis setup by using the vector analyzer. Figure 5-1 shows the block diagram for a small signal analysis setup. A calibration substrate was used to de-embed the effect of the probe and cable, thus bringing the calibration plane to the probe tips. Figure 5-2 shows the measurement setup, which is a cascade probing station with four probe holders from north, south, east, and west used to measure the performance of the proposed wideband transmission-line N-path filter.

An Agilent network analyzer is used to measure the filter's S-parameters. SOLT calibration is performed to de-embed the impact of the cables and probes. The Rohde & Schwarz signal generator is used to generate a clock generator input signal up to 6 GHz.

Figure 5-3 is a micro-photograph of the fabricated wideband transmission-line N-path filter with CMOS 130 nm technology. Figure 5-4 is a closer look at the fabricated central inductor, which was designed to be 6nH. Final parameter values of passive and active components and reference design kit models are provided below. The first phase of measurements was the verification of DC points to determine if the active device (switches) is functional. The supply voltage was set to 1.5V and DC current was observed which means switches are working. The frequency of the VNA was swept from 0 to 4GHz.

A bias tee is used at the input port of the DUT to block DC from getting through to the circuit and only allow the AC/RF signal to pass through. A Bias tee can be used like a diplexer, which has an ideal capacitor that allows AC through, but that blocks the DC current. A diplexer also has an ideal inductor that blocks AC but allows DC.

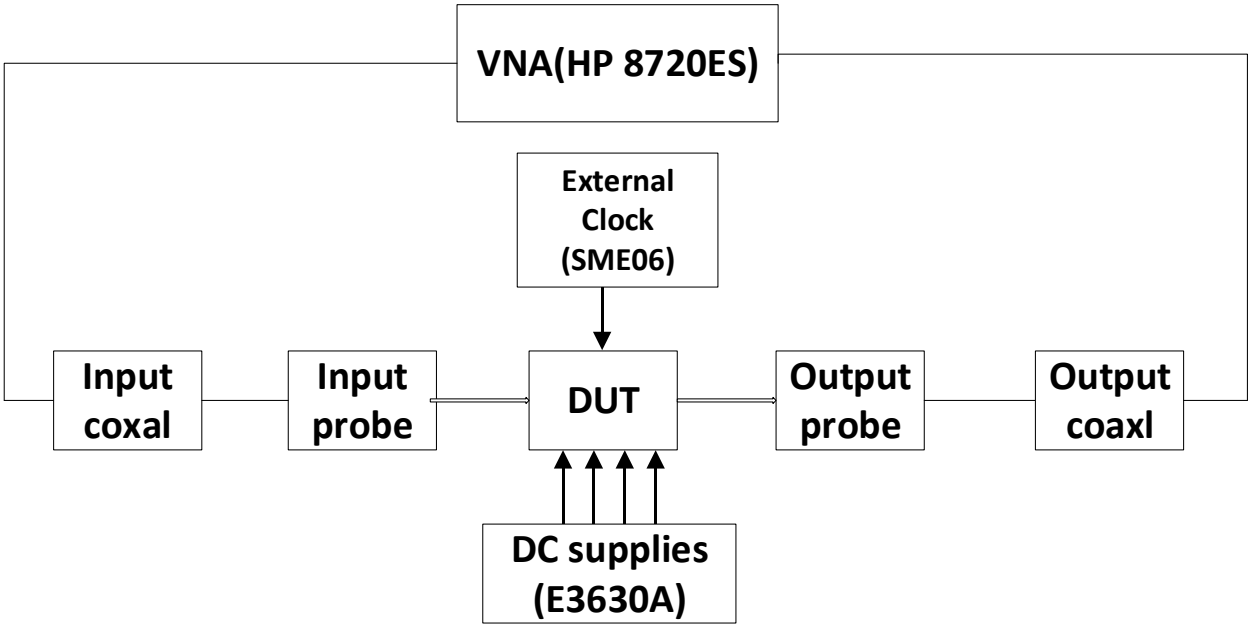
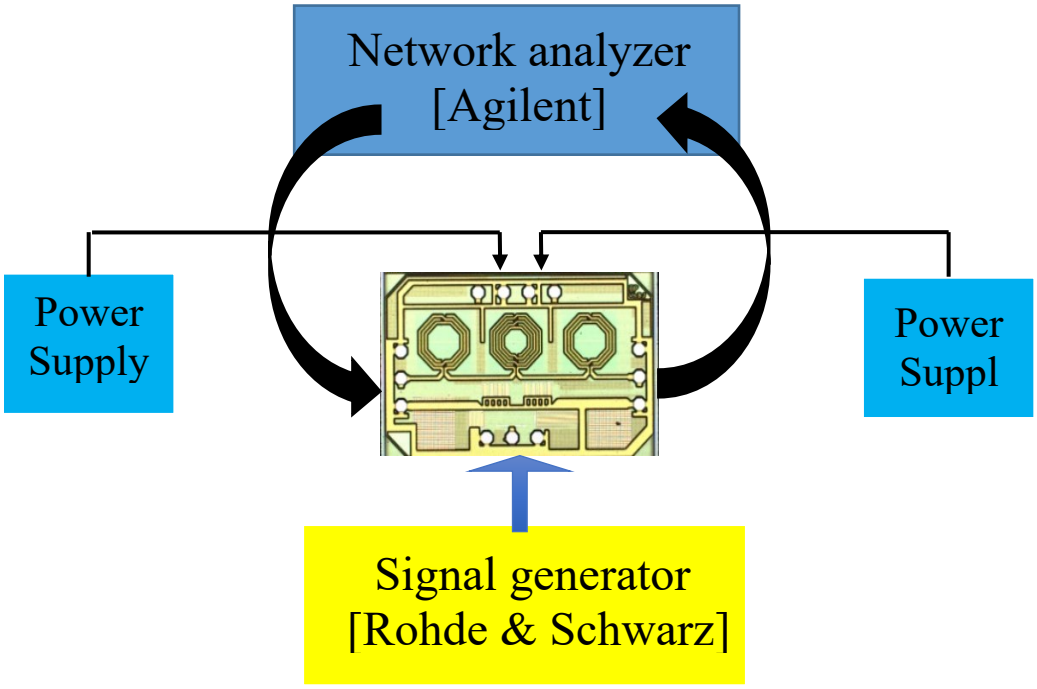


Figure 5-1 block diagram for small signal test bench



a)

b)

Figure 5-2 (a) Experimental setup diagram of the transmission-line N-path filter (b) photograph of the measurement setup

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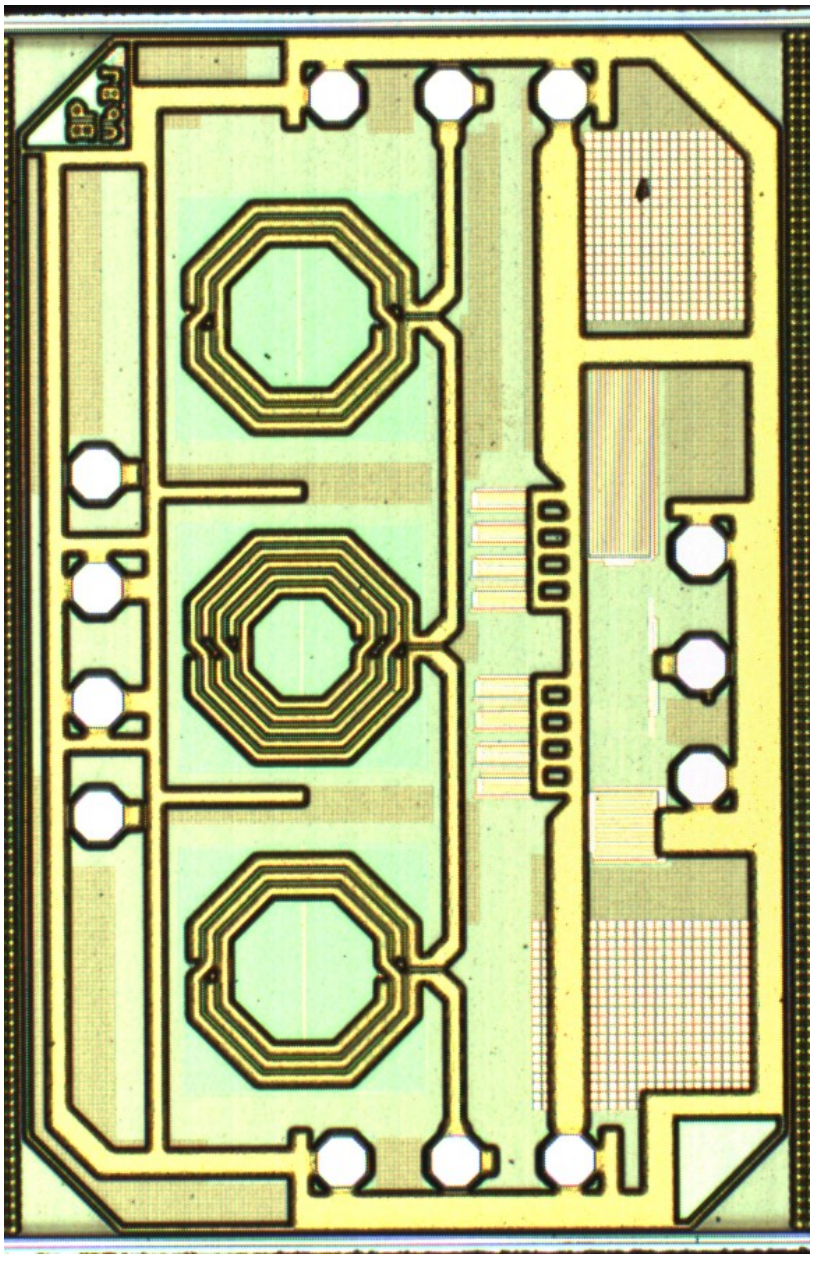


Figure 5-3 Micro-photograph of the fabricated transmission-line N-path filter with CMOS 130 nm technology (1mm× 1.5 mm)

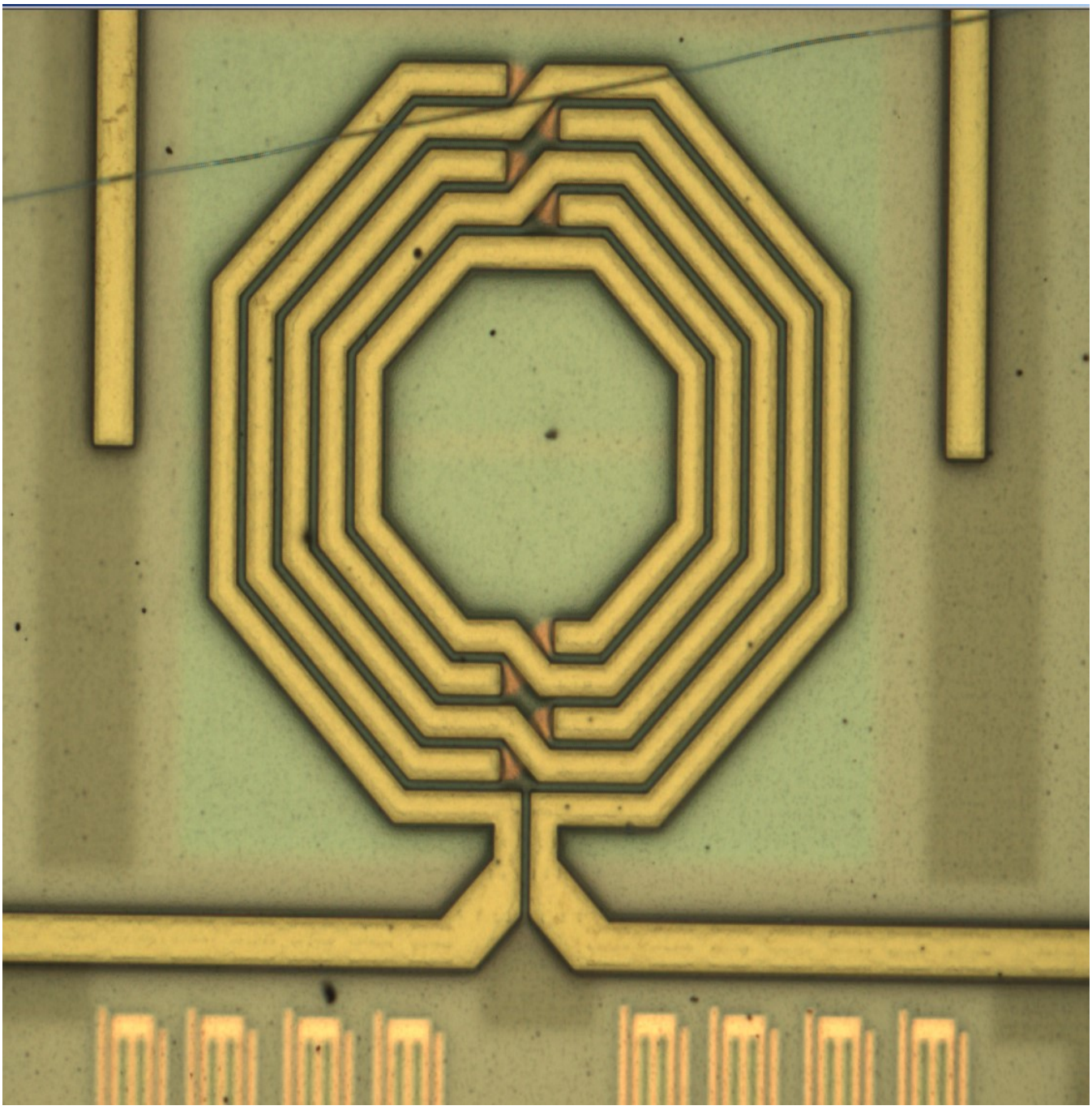


Figure 5-4 Micro-photograph of the fabricated inductor, with CMOS 130 nm technology

5.3 S-parameter Measurement Result

The test plan for the filter was conducted in three stages for different chips. First, the dc voltages were set to 1.5 volts and the dc current draw was measured. Second, the signal generator was set to generate sin wave signal as the input for the circuit for different frequency. Third, the vector network analyzer was used to extract small signal S-parameter of the filter. There is significant performance discrepancy between measurement and simulation result. The potential root causes of the degradation as opposed to the fully characterized filter performance is discussed in the following.

5.3.1 Operating point verification

The first phase of measurement is the verification of the DC voltage to determine if the active device were functional. The supply voltage was set to 1.5 V. The circuit draws current when the external clock was applied in the circuit

5.3.2 Signal generator

The Rhode and Schwarz signal generator were used to produce the input signal for the filter and it offers a frequency range up to 4GHz. The signal generator power level was set to 0dBm and generating sin wave signals. Since the signal generator produced a sine wave signal up to 4GHz, the on-chip clock generator can generate 4 –non-overlap clocks up to 1Ghz (4GHz divided by 4).

The post-layout simulation in Figure 4-7 is done where a voltage pulse generator is used as the input (external clock). To be able to have a consistent comparison between measurement and simulation, we require to have the equipment to generate pulse signal, since we do not have such equipment, we use a signal generator that generates sin wave signal.

To see the effect of injecting sin wave signal instead of pulse signal as an input signal of the clock generator, some simulation is done. Figure 5-5 shows two different input signals at 500MHz that are used to feed the circuit as the clock generator input signal. Although, different input signal is injected as clock generator input, the generated clocks (out1, out2,out3,out4) which drive the gate of the transistors are pretty much the same at the both cases as shown in Figure 5-6.

Figure 5-7 shows the post-layout simulation result for the transfer function of the proposed filter where the clock generator input is sinewave or pulse signal at switching frequency of 500MHz. This comparison shows using the sinewave waveform instead of the pulse signal as the input signal does not make any significant change in the transfer function of the filter. So, there should not be any problem using sinewave waveform as the input signal.

5.3.3 **Small-signal measurement**

Small signal measurements were conducted using a vector network analyzer. The measurement is done for different external clocks frequency. The resulting return loss (S_{11}) and forward gain (S_{21}) are provided in Figure 5-8 below. Figure 5-8 shows measurement result where the on-chip clock generator of the filter is fed by the signal generator at 2GHz that produce 4-non overlap clocks at 500MHz.The result shows that the filter is not working properly.

The best way to find the reason why the filter does not work is to measure the filter and clock generator separately, however since the clock generator is on-chip, we are not able to measure it by itself. The return loss achieves a minimum of -12 dB at 500MHz and forward gain is -3 dB at 500MHz. Figure 5-9 compares measurement results in Figure 5-8 with post-layout simulation result. The sine wave signal is used as an external clock for the circuit (sine wave signal with 500MHz injected to on-chip clock generator in the circuit to produce 4-nonoverlapping clock) for post-layout simulation.

The comparison in Figure 5-9 shows the discrepancy between measurement and simulation results. The following section will discuss various hypotheses for performance discrepancy and what testing was completed to evaluate them.

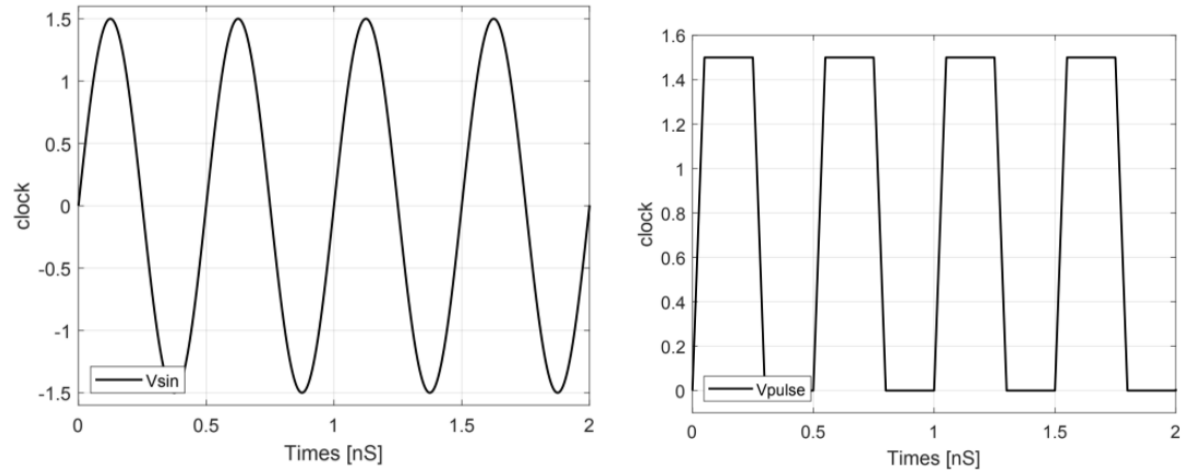


Figure 5-5 different input signal at frequency of 500MHz a) sinewave waveform b) pulse signal with $t_n/10$ rise time and fall time (50ps)

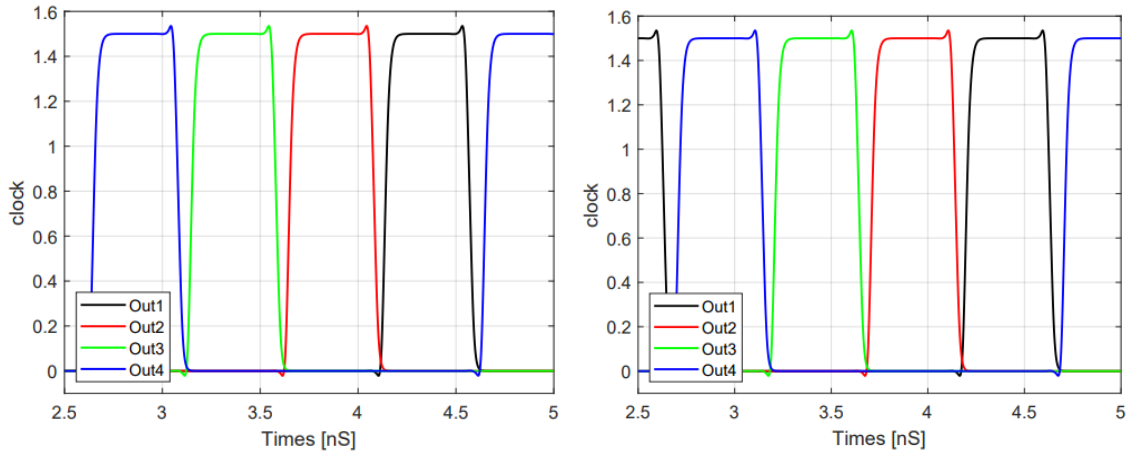


Figure 5-6 Clock generator output (ou1, ou2,out3,out4) for different input signal 500MHz a) sinewave waveform b)pulse signal with $t_n/10$ rise time and fall time (50ps)

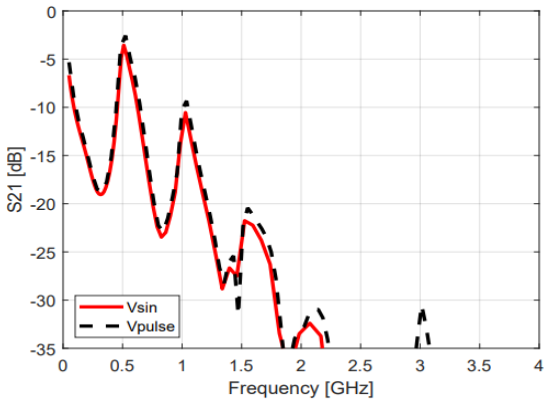
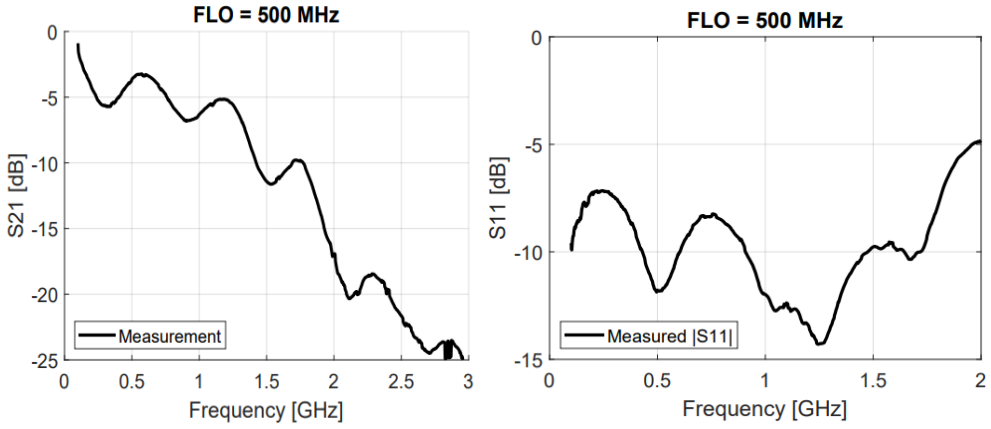


Figure 5-7 RLC extraction simulation for transfer function of the proposed filter with two different input signals (sinewave waveform and pulse signal) at switch frequency of 500MHz



(a) (b)

Figure 5-8 Measurement result of fabricated circuit at 500MHZ switching frequency

a) S_{21} b) S_{11}

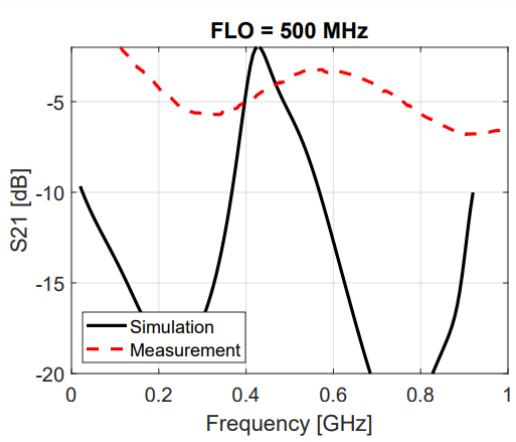


Figure 5-9 Comparison of Measurement result of the circuit with post-layout simulation of the circuit using sine wave clock as external clock frequency at 500MHZ

5.4 Analysis

There are two hypotheses for the performance discrepancy compared to more ideal clocks. Both are evaluated here. As mentioned above, the circuit draws current whenever the external clock is applied in the circuit. It was assumed that active devices were functional. Switches under this assumption seem to be working, which means that the filter should function if the switches properly work. Since the filter measurement result is quite different from the simulated result, something might be wrong with the clock generator. The expected behavior of an ideal TL N-path filter is that it provides an open circuit for the input voltage, at f_s, so that the desire RF signal passes through and short circuit for frequency other than f_s, however, non-idealities such as finite rise time and fall time, reducing in an effective duty-cycle of the clock below 25%. Reducing the duty cycle to less than 25% means for some time all switches are off periodically that result in higher impedance for frequency far away from the switching frequency which translates to less rejection and a lower impedance for the desired frequency which translate to a lower gain. The degradation of the maximum rejection is much more than the insertion loss reduction in passband. Reducing duty cycle by a large amount, can result in significant reduction in out-of-band rejection of the filter transfer function.

The first hypothesis was that the clock generator is not working properly. The clock generator is supposed to generate 4-non overlapping clocks. In the N-path filter only one of the switches should be on, and only one path should be conducting. This switch and path is then turned off, and then another switch and path should be turned on, and this sequence should continue. However, if there is a problem with the clock generator, it could be that more than one switch is on at the same time (D$>$ 25%), or that there is a significant delay between switches turning on (D$\ll$ 25%).

If the duty cycle of the generated clocks is bigger than 25% (D> 25%), then generated clock phases might be overlapping for which two switches can be ON at the same time, result in charge sharing between capacitors that would cause the destruction of the filter shape.

If the duty cycle of the generated clock is less than 25%, all switches are off periodically for some time result in less rejection and lower insertion loss in the passband.

The other assumption is that the clock generator is not working at all. Each of these assumptions was further evaluated with simulations described below.

One of the problems with this circuit is that the clock generator is part of the circuit and it cannot be measured separately to see if it is working. One option was to design the filter without the clock generator and feed the circuit with an off-chip clock generator. Such an off-chip clock generator was not available. The research was conceived of according to the availability of resources. Some simulation was conducted for each case. The simulations were first conducted in a case of generating clocks that are not non-overlapping clocks, and then in a case where that clock generator does not work at all. The measured transfer function (S21) and return loss (S11) are provided in Figure 5-11 (b) and Figure 5-12 respectively. Figure 5-11 (b) compares the simulated versus measured |S21| of the filter when the FLO is 500 MHz.

The simulated analysis is done using an ideal clock with 15% duty cycle with finite rise time and fall time. This comparison shows there is a correlation between the measured and simulated |S21| of the filter at FLO = 500 MHz. There remain, however, discrepancies between the measurement results and simulation results when using a more ideal clock.

5.4.1 **Hypothesis 1**

The first assumption is if clocks have overlap and switches are on at the same time, overlapping clocks result in charge sharing in the capacitor. Overlapping clocks result in the destruction of the filter shape somehow. If D was a little bit less, but still bigger than 25%, it might be agreeing somehow since the ripple is still there although maybe less than the measured result. Figure 5-10 shows simulated transfer function of the filter if clocks have overlap. The switches are fed by clocks that have 30% duty cycle (the overlapping clocks are ideal clocks).As can be seen in Figure 5-10, although clock overlap destroys the pass-band transfer to below -5db, due to charge sharing between the signal path, there are still somewhat ripple which shows some similarity with TL N-path filter shape.

The second assumption as mentioned above is, the clock generator has a non-zero rise time and fall time that results in the duty cycle falling below 25%, which causes lower maximum rejection of the filter and higher in-band insertion loss. In a case, that duty-cycle of the 4-phase non-overlapping clock is 15% with finite rise time and falls time, the transfer function of the proposed filter is plotted. Figure 5-11 (a) shows the ideal clock with D=15% with fall time and rise time of 50pS. Figure 5-11 (b) compares the transfer function of the proposed filter when using an ideal clock in Figure 5-11 (a) with measurement results at a frequency of 500MHz.This comparison shows a correlation between measurement and simulation results. The input impedance should be well matched across the desired frequency. Figure 5-12 shows the measurement of S_{11} around 500MHz is about -12 dB, which is better than -10 db.

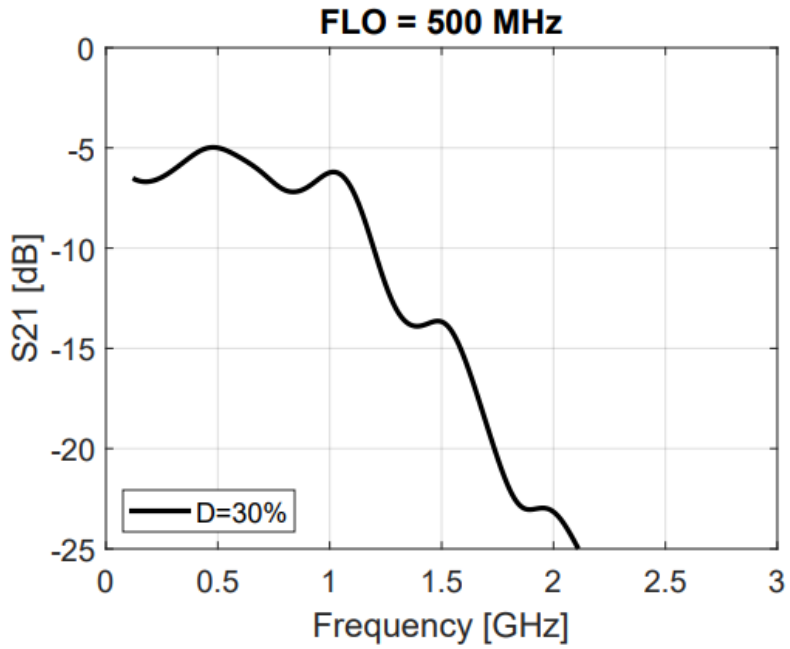
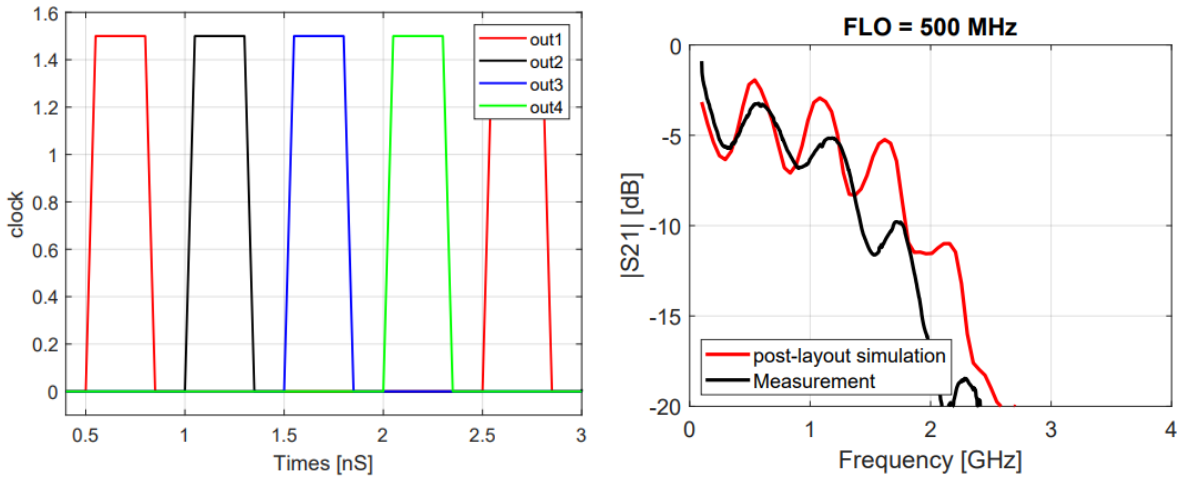


Figure 5-10 Simulated |S21| of the transmission-line N-path filter with using ideal clock as input of the circuit with 30% duty cycle at FLO = 500 MHz



(a) (b)

Figure 5-11 (a) ideal clock with D=15% which is injected into the circuit (b) Comparison between measured |S21| of the transmission-line N-path filter and Simulation result (RLC extraction) with ideal clock shown in (a) at FLO = 500 MHz

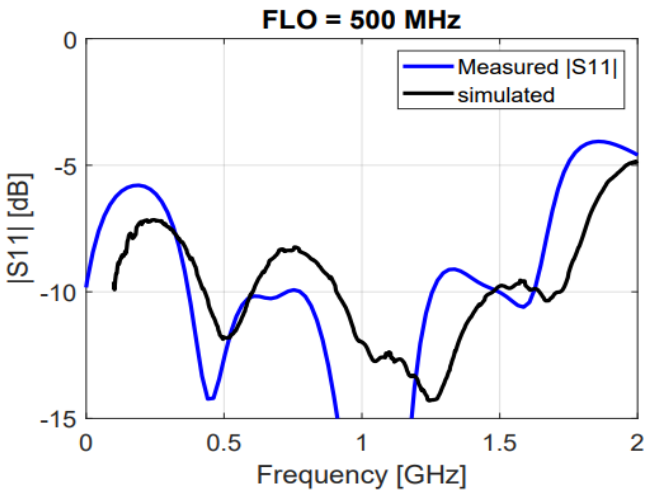


Figure 5-12 Measured |S11| of the transmission-line N-path filter at FLO = 500 MHz with injecting input signal into the switches as shown in Figure 5-11 (a)

5.4.2 Hypothesis 2

If the clock generator is not working at all, all switches are off. The simulated result is shown in case the clock generator is not functional at all and it compares with the measurement result when the clock is not applied.

Figure 5-13 compares measurement results and simulation results in a case where no clock drives the gate of the transistor and shows a correlation between them.

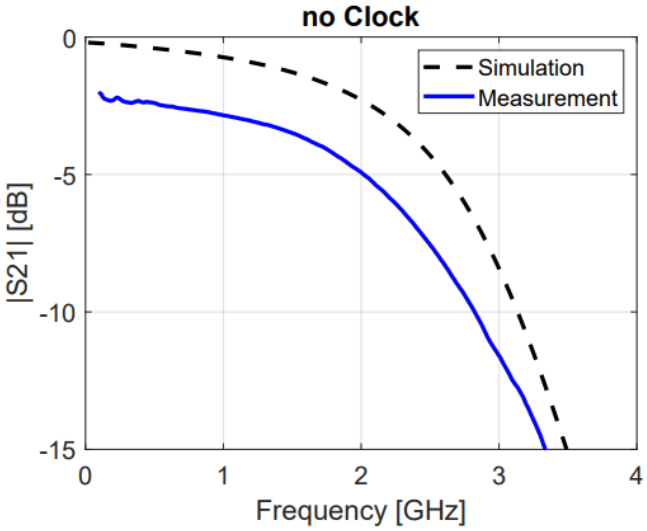


Figure 5-13 Comparison between Measured |S21| of the transmission-line N-path filter and Simulation result when clock is not applied

5.5 Summary of the chapter

In this chapter, measurement have been shown in Figure 5-8 for switching frequency of 500MHz. The measurement result of single–ended two stages transmission line N-path filter fabricated in a 130-nm CMOS technology shows that the return loss achieves a minimum of -12 dB at 500MHz and forward gain is -3 dB at 500MHz, with low out-of-band rejection which is about 5-7db around the switching frequency.

There is discrepancy between measurement results and post-layout simulation results of the proposed filter. From above, it seems plausible that the clock generator was not working exactly as predicted by the extracted simulation. The plot shows that if the duty cycle was somehow less, the resulting figure for S21 and S11 are in fairly good agreement with the measurement results. Although with a duty cycle of 30% the filter function was changed significantly, the shape of the filter still shows some resemblance. So, it seems possible that a duty cycle slightly more than 25% that resulted in a little bit of charge sharing could also result in the shape shown by measurements. This demonstrates that the design of the clock generator is quite critical to the overall filter performance.

Chapter 6. Conclusion and Future Work

This research aimed to increase the bandwidth of transmission-line N-path bandpass filters with center frequency at the clock frequency. A wideband transmission-line four-path filter is designed and presented based on low-cost CMOS 130 nm technology. The bandwidth of the filter has been improved to over 80 MHz, at 1 GHz central frequency, while the operating frequency is between 0.1 GHz and 1 GHz. A high frequency four-phase non-overlapping clock generator with a 25% duty cycle is based on CMOS 130 nm technology to drive the switches of the transmission-line four-path filter. The post-layout simulation of the two-stage transmission line 4-path filter achieves less than 5-db insertion loss across the tuning range from 0.1 GHz to 1 GHz, and 20-30-dB out-of-band rejection. The bandwidth is varying from 59 to 107 MHz over the tuning range, and it is about 80 MHz in 1 GHz. The post-layout simulation result in Figure 4-7 shows that the on-chip clock generator produces 4-non overlapping clocks. Because the generated clocks have non-zero rise and fall times, the duty cycle changes depending on which voltage it is measured at. At 0 V, it is measured to be about 26% at 500 MHz, but for somewhat higher voltages where switching occurs it will be less than the ideal case of 25%, so safely non-overlapping.

The measured results are presented for the proposed wideband transmission-line N-path filter. Initially, there were some discrepancies between the measurement results and the simulation results. Measurement results did not match the simulation results discussed in the previous paragraph in that there was minimal difference between the passband and stopband gain. These discrepancies were attributed to clock phases.

Based on the first hypothesis, if the duty cycle of the generated clocks is much less than the ideal 25%, for example 15% which is 10% less than the ideal case, then there is considerable time for which all switches are off which results in less rejection and higher insertion loss for in-band frequency. This was verified through simulation with D=15% resulting in correlations between measurement results and simulation results at a frequency of 500 MHz. If the clock generator is not functional at all, the filter shape completely destructs, and it is not like the TL N-path filter shape anymore.

Because the simulation result with duty cycle of 15% matched the measured result, this was deemed to be a likely cause of the discrepancy. It was also shown with a duty cycle of 30%, there was hardly any difference between the filter passband and stopband. It seems possible that with less clock phase overlap, the simulation results might match the measurements results more closely, but this was not explored further. In conclusion duty cycle is very important. Although duty cycle can be reduced by quite a bit before significant damage is done to the filter, a small amount of clock overlap will do much more damage to the filter shape.

6.1 Future work

The rapid improvement in process scaling of CMOS technology, attract the researcher's interest in N-path filtering. This thesis presents the high-frequency transmission line N-path filter to improve the tradeoff between in-band insertion loss and out-of-band rejection in a traditional N-path filter. The following are some areas for possible future work.

1 First, one of the biggest challenges in this work is that the clock generator and the filter cannot be tested separately. For the next step, the filter and clock generator should also be implemented as breakout circuit so they can be measured separately. For instance, in our case, the measurement result shows that the filter does not work properly, but we are not sure if this issue is related to the clock generator or the filter. In our case since the circuit draws the current, we guess the switch is working, then the filter should be functional, and we guess that there is a problem with the clock, but direct clock measurements are needed to verify this.

2 The harmonic mixing of the passive switching mixer causes harmonic folding in the N-path filter. The folded harmonic can be pushed away by increasing the number of the paths, however increasing the number of the path required higher-frequency digital logic which is limited by the process technology. Therefore, an RF pre-filtering is needed to remove the folded harmonic. So, designing the RF-pre-filtering can be considered as future work. It would also be suggested to explore the possibility of alternative clock generators that do not require an input clock frequency at N times the filter frequency as a way to reduce the limitation on process technologies.

3 In addition to harmonic folding of TL N –path filter, there is harmonic selectivity in the transfer function of the filter as well, which means that there is frequency selectivity around higher harmonics of the switching frequency. Even harmonics can be removed using differential structures, however selectivity around odd harmonics still remain. A trade-off would be that a differential TLNF would require twice as many inductors, and since inductors are very large, differential TLNF requires more area.

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