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Oversampled Analog-to-Digital Converter and Subscriber Line Channel Modelling for Digital Subscriber Loop Transmission

by

Thean S. Chee, B.C.S.

A thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfilment of the requirements
for the degree of

Master of Engineering

Ottawa-Carleton Institute for Electrical Engineering
Faculty of Engineering
Department of Systems and Computer Engineering
Carleton University

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submitted by Thean S. Chee, B.C.S.
in partial fulfilment of the requirements
for the degree of
Master of Engineering

Thesis Supervisor

Thesis Supervisor

Chairman, Department of Systems and Computer Engineering

Carleton University
October 18, 1990

Abstract

This thesis reports on the work performed in modelling the channel and the line interface of a *digital subscriber loop* (DSL) transceiver, and its analog-to-digital (A/D) interface composing of an oversampling analog-to-digital converter. The digital subscriber line channel and the quantization noise of the oversampling A/D converter were analyzed and modelled. A simulation environment for a transceiver operating on the DSL is created from the derived models.

To Mom and Dad.

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Chapter 1

Introduction

The *Integrated Services Digital Network* (ISDN) concept was proposed to provide switched and non-switched digital circuits which will support a wide range of telecommunications services. It is envisioned to be an enduring solution for “universal connectivity” evolving from existing voice and data networks. Initially, access to ISDNs will be by the use of full duplex transmission systems operating over twisted metallic pair cables (loop plant) of existing local telephone networks. It will provide virtually all voice, data, and video telecommunications services to telephone subscribers using the existing loop plant which is originally installed for voice frequency analog transmission. As a result, the loop plant¹ is conditioned and installed to facilitate voice grade communication. However, the conditioning of these subscriber lines for voice band transmission poses as structural impediments to reliable transmission of very high rate digital signals.

¹Subscriber lines with digital transmission capability are called *digital subscriber lines* (DSL).

1.1 Thesis Motivation and Objective

The realization and implementation of DSLs in the existing loop plant requires sophisticated signal processing, transmission, and detection techniques. The design of a transceiver operating in such a medium is considered to be a challenging task which requires both system and hardware considerations. To aid in the design of the transceiver, a fast, robust, and flexible tool is required. The objective of this thesis is to develop a simulation environment which provides a simulation model for the digital subscriber loop line interface for the use of transceiver architecture optimization and performance analysis during the design process. Specifically, two topics of high interest have been identified. They are the modelling of an arbitrary constitution of the twisted-pair copper loop plant and the quantization effects of the oversampling A/D converter.

1.2 Thesis Organization

This thesis is organized in six chapters. The thesis attempts to address the issues of modelling and providing a simulation environment for the twisted pair digital subscriber loop. The environment of the digital subscriber loop is presented in Chapter 2. An overview of commonly encountered impairments of the digital subscriber loop channel and the different possible transmission schemes in this media are discussed. The modelling issues are presented Chapters 3 and 4. In Chapter 3, the topic of modelling the digital subscriber loop channel is described. And, in Chapter 4 the study and attempt to model the quantization noise of the oversampling A/D is reported. Chapter 5 deals with the issues of simulating a transceiver operating in the digital subscriber loop media using the reported work from the modelling chapters. Finally, in Chapter 6 a summary of the thesis is presented and conclusions will be drawn.

Chapter 2

Digital Subscriber Line Technology

The connection between the ISDN switch (or remote digital terminal) and the ISDN user is a critical component in the end-to-end digital path that forms the basis of the network. Since a majority of the users are presently served by a single twisted pair of telephone wires, full-duplex (i.e., simultaneous two-way) service at rates sufficient to accommodate ISDN must be provided over this link. Due to the copious use of the present loop plant, the most common access to ISDNs by the individual subscriber is through a repeaterless DSL system connection between the serving center and the customer premises over the existing plant. Thus, as ISDN draws closer to a widespread reality, DSL transmission technology is of key importance.

2.1 Digital Subscriber Lines

Digital Subscriber Lines describe a technology that provides full-duplex communication link on a single twisted metallic pair wire which allow the transmission of

digital data signals at a rate sufficient to support the ISDN *Basic Access*¹ [Ame88]. As a means to economically accommodate access to ISDNs, the DSLs must be realized through the use of the existing wire loop plant. Unfortunately, the existing wire loop plant has been designed and installed for the economic provision of voice frequency transmission in mind. As a result, bridged taps² and mixed wire gauges, which are used to provide an economically flexible plant, and loading³ coils which are installed to facilitate voice band communications, are prevalent. The existence of these elements, although aid in providing better quality voice grade service, constitute a serious impediment to reliable data transmission at high rates.

In order that the realization of DSLs be economical, it is important that its installation should not require any special engineering, operations or administrative procedures [Lec86, Lec89]. Therefore, it is desirable that no plant conditioning be necessary beyond the removal of loading coils⁴. It is required that the DSL environment perform with a *Bit Error Rate* (BER) of less than 10^{-7} over essentially all of the nonloaded loops in the North American wire pair plant.

2.2 Impairments in the Digital Subscriber Line system

The transmission capability of the DSL system is governed by the line characteristics of the loop plant. The DSL transceiver must contend with the nonidealities of the existing plant which may have detrimental effects on the quality of the transmitted signals.

¹An integral part of ISDN is the provision of full-duplex digital transmission capability at the Basic Access information rate of 160 kb/s.

²Bridged taps are open-circuited cable pairs bridged onto the main cable pair.

³“Loading” refers to the equalization of lossy subscriber lines, using inductors.

⁴The ANSI standard is based on the use of cables without loading coils.

The principal impediments to the reliable transmission of high rate digital signals and its performance on the subscriber loops are:

- cable attenuation,
- echo,
- intersymbol interference,
- crosstalk noise,
- impulse noise.

In addition to introducing distortion on the transmitted signal, the above mentioned impairments limit the rate and range at which we can communicate over the twisted pair.

2.2.1 Cable Attenuation

The attenuation characteristic of the loop plant is dependent on the configuration and composition of the plant. The wire gauge, line lengths of the twisted pair, the presence of bridged taps, the length of these bridged taps, wire gauge changes, and inductive loading on the lines, are some of the important parameters of the loop plant which govern its attenuation characteristic. The transmission loss exhibited by a typical cable is an increasing function of frequency, line length, and signaling rate.

The amplitude-versus-frequency characteristic of a typical cable pair is shown in Figure 2.1. The attenuation characteristic exhibited by a typical cable pair is proportional to the square root of the frequency within the voice band. As depicted in Figure 2.1, the attenuation introduced by the cable is very small at low frequencies, and consequently overloading can occur if a significant energy level is permitted within this range of low frequencies. This is particularly true for voice frequency communication, where the energy of the signal is predominantly located between 0-4 kHz.

Figure 2.1: Attenuation of typical subscriber line cable at 55°F [Lab82].

It is common practice in voice grade transmission to circumvent the above mentioned problem by adding series lumped inductances at uniform intervals on the line, to provide a low-pass network to deliberately decrease the low-frequency attenuation. This results in both a lower and more uniform loss in the voice band frequencies. However, this makes the line act as a low-pass filter with abrupt cutoff as shown in Figure 2.2. The transfer function of the cable significantly attenuates the line response outside the 0–4 kHz voice band bandwidth. Due to this detrimental effect of the loading coils, which impedes the transmission of the much higher data rates required by ISDN, the standard for the implementation of the ISDN for the North American continent is based on the use of cables without loading coils [Ame88].

For baseband transmission, pulse attenuation has been shown to obey a power law relation to cable length and baud rate over a useful range of rates [CT85]. The loss due to cable length is related to the increase in loop impedance as line length increases, and hence greater attenuation. One effect of bridged taps is to further load the cable, providing an overall additional attenuation. The severity of the attenuation

Figure 2.2: Amplitude-versus-frequency characteristic for a typical loaded and unloaded cable pairs [Lab82].

characteristic caused by bridged taps does not lie as much as in the position of the bridged tap with respect to main line but in the length of the bridged tap itself.

The loss due to the signaling rate can be attributed to the amplitude-versus-frequency characteristic of the cable. The faster the signaling rate the greater the high frequency content of the transmitted signal, and consequently the greater the attenuation in this band of frequencies as predicted by the amplitude-versus-frequency characteristic of the channel.

It is common on duplex links of the two-wire voice frequency line to use *hybrid* transformer circuits to provide isolation between the transmitting and receiving paths on the two-wire line. The hybrid circuits are typically realized by a set of coupled coils consisting of two transformer-coupled balanced circuits. With the presence of these transformers, the amplitude-versus-frequency response of the cables will be altered, introducing greater attenuation to the transmitted signal at DC and low frequencies. The typical frequency characteristic of the subscriber line cable with the hybrid circuit

Figure 2.3: Attenuation of typical subscriber cables with hybrid circuits.

is illustrated in Figure 2.3. With the DC and low frequency components of the signal being removed by the transmission channel, the transmitted baseband pulse will be dispersed over a longer period of time, resulting in long slowly decaying pulse tail, contributing to *intersymbol interference* (ISI). The effects of the DC cutoff is better exemplified in Figure 2.4. The presence of the transformer results in the long negative tail of the response. Effectively, the cable and hybrid transformer acts as a low-pass filter with passband attenuation, attenuating and dispersing the pulse as the cable length increases.

2.2.2 Echo

Echos are portions of the transmitted signal power received at the receiver due to reflections caused by the electrical imperfections of the transmission medium. The major causes of echos are wire gauge changes, bridged taps, frequency variability of the line characteristic impedances, and leakage through the line coupling transformer

Figure 2.4: Effect of removing low-frequency components [Ben65].

(hybrid transformer circuits).

The echo signals caused by wire gauge changes can be explained by the nonuniformity and mismatches of the line impedance as a result of the gauge changes. Ideally, the line impedance value is closely matched by the input and output impedances of the line driver circuits of the transmitter. This ensures that the transmitted signal is launched efficiently into the cable, and no reflection from the cable occurs at the receiving end of the cable. However, the presence of gauge changes on the cable will disturb the cable's line impedance characteristic. This interferes with the efficient power transfer of the transmitted signal from one end of the cable to the other causing part of the transmitted signal energy to be propagated back throughout the cable.

A similar but more severe effect of impedance discontinuities on the subscriber line is the existence of bridged taps. Bridged taps cause part of the transmitted signal travelling down the main cable to be diverted into the tap. This can be viewed as a discontinuity in the line impedance at the tapping junction resulting in a reflection

of the transmitted signal comparable to the effects of wire gauge changes except it is much more pronounced. The energy of the reflected signal travels back on the main cable with an attenuation and delay which depends on the length of the tap.

Another source of echo can be attributed to the mismatching of the balancing impedance of the line coupling transformer circuit to the impedance seen on the transmission line. A balanced line coupling transformer is typically used to isolate the transmit and receive paths on the twisted pair channel of the near-end transceiver. This circuit is designed to provide infinite attenuation to the signal between the transmitting and receiving paths of near-end transceiver when both the impedances of the line and the balancing network of line transformer are matched as explained in Figure 2.6. Due to the mismatch in the impedances, a leakage of the transmitted signal is present at the near-end receiver. This leakage signal can be viewed as the near-end trans-hybrid echo of the transmitted signal.

2.2.3 Intersymbol Interference

Intersymbol interference (ISI) is a consequence of the dispersion of the transmitted pulse due to the band limited nature and nonlinear phase characteristic of the channel. ISI usually constitutes most of the energy in the samples of the received pulse. Generally, it is not realistic or possible to restore a transmitted pulse to its original shape due to effects of the transmission medium, or even to provide equalization to the extent that it is confined to a single time slot. The signal of the transmitted pulse will spill over into the adjacent signaling time slots. This dispersion of the transmitted pulse yields a *precursor* and *postcursor* of the transmitted pulse. The former refers to the samples of the pulse response prior to the ideal sampling instant of the received pulse, while the latter refers to the samples of the pulse response following the ideal sampling instant of the received pulse respectively. The precursor and post-cursor from adjacent transmitted pulses sum together in a given time slot to form the intersymbol interference. Neighbouring symbols interfere with one another

during the sampling instants causing erroneous data symbols to be interpreted by the receiver if nothing is done to curb the dispersed transmitted pulse.

The loop plant constitution also plays a role in the generation of ISI. For example, the existence of bridged taps result in "*ghost pulses*" that are delayed relative to the main received pulse and result in post-cursor ISI. This can also be considered as echos caused by the presence of bridged taps.

ISI can theoretically be cancelled by *adaptive equalization* techniques. Typically, a *linear feed-forward equalizer* can be used to remove precursor ISI, while the post-cursor ISI is dealt with effectively by using a *decision feedback equalizer* (DFE) [Pro83]. Precursor ISI can be tolerated without the use of the feed-forward equalizer by means of selecting an appropriate timing algorithm as long as the transmission requirements are not compromised [ACCC87, CGH⁺89].

2.2.4 Crosstalk Noise

Crosstalk can be viewed as the interference caused between neighbouring cable pairs due to electromagnetic coupling of one line to the other. It typically arises from the capacitive and inductive coupling among different pairs of transmission lines within the same cable bundle. Signals transmitted on a pair of wires create electromagnetic fields that surround the wires. These fields will induce interfering voltages and currents on nearby wire pairs. To minimize such coupling between wire pairs, multipair cables like those used for the DSLs application call for the twisting of each wire pair within the cable. This reduces the amount of coupling between pairs to a tolerable level but is not totally removed due to the imperfections in the geometry (unbalances) of the wires. The residual coupling results in random variation from cable to cable and pair to pair as a result of manufacturing variations. The coupling effects depend on the cable's terminating impedance and the frequency content of the signals in the cable. The coupling is more evident as the frequency of the signals increases and the total coupling depends on the exposure of the length of

the cables. The coupling is strongest between immediate-neighbour pairs, of which there are only a few, even in a large cable. The crosstalk mechanism not only couple unwanted signals from other communication channels but also can couple in noise or interference from power lines, radio stations, switching offices, and many other sources of electromagnetic radiation.

The crosstalk between the pairs within a cable can be separated in two categories, *near-end crosstalk* (NEXT) and *far-end crosstalk* (FEXT). NEXT represents a crosstalk from a local transmitter into a local receiver, while FEXT represents a crosstalk from a local transmitter into a remote receiver, as illustrated in Figure 2.5. Where present, NEXT will be the dominant impairment when compared to FEXT because FEXT will typically experience the usually large crosstalk coupling loss in addition to the line attenuation [Mes86, CA85]. The NEXT is not attenuated as much as the FEXT by the line and could thus pose a problem if the *disturbed* line is long and hence very lossy. Both forms of crosstalk have a power spectral density which is increasing with frequency, and therefore, it is beneficial to minimize the bandwidth required for transmission in a crosstalk-limited environment.

NEXT is generally considered as one of the primary performance limiting factor for most digital transmission systems. It is also the impairment which dictates the rate and range limitation of a subscriber loop transmission system [Jos88]. Typically, the crosstalk interference is treated as a stationary random additive noise of unknown details except for its spectrum [Ame88]. By considering only the magnitude characteristic and disregarding the phase characteristic, we effectively randomize the noise phase to make it stationary. However, more recently a more realistic treatment of NEXT has been proposed by taking into account the phase characteristic of the NEXT interference [CGS83a, CGS83b, FLF89, PF89]. It is found that the NEXT interference is cyclostationary in characteristic due to the periodic nature of the digital waveforms in the interfering systems.

Figure 2.5: Illustration of near-end crosstalk (NEXT) and far-end crosstalk (FEXT).

2.2.5 Impulse Noise

Of all the impairments discussed thus far, least is known about impulse noise. It appears as sudden, random, large spiked pulses of short duration, and having an approximately flat frequency spectrum over the frequencies of interests [Lab82]. Impulse noise generally results from electromechanical switching transient^c in the subscriber line network, such as telephone switching relays and dial-pulse signaling telephones. Several characterization of this impairment have been attempted [Cor, McD87, Kap89] and data collected have shown that it varies substantially in frequency of occurrence, intensity, and characteristics from location to location, and from time to time even at the same location. It is difficult to make general discussions on impulse noise since its properties are greatly influenced by the loop constitution.

2.3 Transmission Methods

Simultaneous two-way data transmission in the same bandwidth normally requires separate channels, and in the telephone network it is generally realized by using a four-wire circuit. Duplex transmission on a two-wire circuit is desirable whenever it is impractical to provide four-wire service. Furthermore, due to cost reasons a two-wire system is expedient. Since the existing loop plant was originally designed to cater for predominantly voiceband transmission, the loop plant is virtually always two-wire. In consequence, simultaneous full bandwidth duplex transmission on a two wire system is desired for transmitting data signals over the DSLs.

The design of a system to derive a full-duplex data stream from a single wire pair is a significantly challenging task. Extensive field trials, simulations and research has been carried out by various operating telephone companies and organizations to evaluate several transmission schemes, for which there has been three prevalent proposed technologies: *frequency division multiplexing*(FDM), *time compression multiplexing*(TCM), and *echo cancellation*(EC) using hybrid transformer couplers⁵.

Of the three schemes mentioned, composite schemes have been proposed to exploit the advantages from each of the above mentioned methods with a goal of achieving a compromise between circuit complexity and transmission performance. These combined approaches like, for example, a method which includes both TCM and EC, called the *echo cancellation burst mode* (ECBM) [MRV86, BMT85, FTM85], and also a combination of EC and FDM [Mes86] have been proposed. These approaches generally increase the transmitted signal bandwidth and, therefore, reduce the ultimate range as dictated by cable attenuation, but exchange this compromise for a simplification in some portion of the design of the overall system. Since these hybrid methods are not conforming to any standards, only the FDM, TCM and EC will be discussed in further detail in the following sections.

⁵ Hereafter this transmission scheme will be subsequently referred to as the *hybrid* scheme.

2.3.1 Time Compression Multiplexing Scheme

Time compression multiplexing (TCM) refers to the method of establishing a two-way communication link on the same physical channel by separating the transmit and receive channels by ensuring that the transmitter on both ends of the communication link transmit at different allocated time slots. In this scheme, the bit-stream in one direction is divided into traffic *bursts* with each transmitting end alternating their utilization of the channel at regular intervals. Since the intervals for the transmit and receive times are isolated, the separation of the two opposite directions of transmission is thus simplified. However, this type of isolation would necessitate a line rate in the loop plant in excess of twice the average data rate.

Due to the higher transmission rate, one would imagine the TCM system to be quite sensitive to crosstalk. Nevertheless, crosstalk noise can be easily controlled by enforcing all transmission bursts in the same cables to be synchronized [Mes84, Lec86, LL88]. Furthermore, because of the increased signaling rate TCM systems generally have a larger bandwidth requirement. This translates into a system which experiences a higher loss and limited range capability due to cable attenuation. In addition to cable attenuation, loss due to bridged taps is more pronounced as a result of its spectral distorting effects [Lec86]. This suggests more complex signal processing elements which have bandwidth capacity of at least twice as large are required.

A major advantage of the TCM scheme is that reflections in the line during the transmission burst is not a severe problem since during this time window the near-end receiver will be inactive. However, when the receiver is activated, it becomes necessary to ascertain that the residual reflections and pulse dispersion from the burst transmission will not be detrimental to the reception of the far end data. These reflections die down quite rapidly but lingering effects prevail due to line termination impedance mismatch and bridged taps effects. Therefore, a guard time is required so that the transmitter and receiver remain idle between bursts while the line transients subside. As a result, the instantaneous line rate in the TCM system is governed by

the length of a transmission burst, the time for a pulse to travel down a line, and the guard time between bursts. A more subtle advantage of the TCM system is that the signal processing requirement and circuit complexity of the transceiver is greatly simplified when compared to the FDM or EC methods. Studies have shown that the TCM system under certain condition and considerations prove to be a favourable method of transmission [KYT86].

2.3.2 Frequency Division Multiplexing Scheme

The frequency division multiplexing (FDM) scheme is used most commonly when data streams are transmitted over existing analog carrier systems and voice band data transmission. The two-way data transmission on a common wire pair is achieved by separating the transmit and receive data streams on nonoverlapping frequency bands of the channel.

FDM transmission scheme has the major advantage of being less susceptible to crosstalk noise. The system could be designed to heavily attenuate the crosstalk path through the design of the bandpass filters used in the system. Another advantage of FDM is that it is not prone to propagation delay unlike the TCM scheme.

However, the FDM scheme is not used due to its shortcomings when applied to the DSL environment. The implementation of the FDM scheme on the loop plant would imply a passband system operating in a very restrictive band limited medium. Such a system would require relatively expensive, complicated and stringent bandpass filtering. Due to high transmission rate required by ISDN which demands large bandwidths, this scheme proves to be impractical due to the attenuation characteristic and inadequate total bandwidth of the subscriber line channel which limits the transmission rate and range capability of the system. Another disadvantage of FDM is the rather strict linearity requirement of the transmission medium.

2.3.3 Echo Cancellation Scheme

The echo cancellation (EC) method for duplex transmission on DSLs is based on a similar two-wire to four-wire conversion technique used in voiced telephony. As with the voice telephone system, this scheme uses a hybrid transformer circuit to provide coupling for the transmission and reception paths, as well as the directional isolation between the two opposing transmission paths on the common wire pair. Thus, a virtual four-wire connection is established on the two-wire twisted pair.

The hybrid circuit is typically realized by transformer coils or by an equivalent electronic circuit. Transformers provide efficient coupling between circuits having different impedances or between balanced and unbalanced circuits. This is particularly true in the application of DSLs, where one must contend with loop plants of various configurations and different line lengths. As a result, hybrid circuits with transformer coils are most commonly used for the echo canceller scheme for duplex transmission in the DSL application. A typical example of a hybrid circuit using transformer coils is illustrated in Figure 2.6. Ideally, the balancing impedance on the hybrid transformer circuit should match the impedance of the transmission line so that there would not be any leakage of the transmitted signal from the local transmitter to the local receiver. However, in practice this is hardly ever possible due to the numerous line configurations of the loop plant which results in the different line impedances. Since it is impractical to tailor the balancing impedance of each hybrid transformer installed on the subscriber line to a specific loop configuration, a compromise balancing impedance is chosen, to give the best overall performance for a majority of the loop compositions in the plant. Due to the mismatch between the compromise hybrid termination and the line impedance, some feed-through of the transmitted signal may leak from the local transmitter to the local receiver, resulting in a familiar problem called *echos*. Typically, the amount of attenuation of the echo signal that can be achieved by the hybrid circuit using the compromise balancing impedance is approximately at most 10 dB [Mes84, AHM82a].

The above shown is a simple electronic version of the transformer hybrid circuit. The transformer is used to serve as an balanced to unbalanced converter and to couple the transmit and receive signals on the same two-wire facility. The transmit signal, $y(t)$, and receive signal, $r(t)$, are both superimposed on the transformer windings with $r(t)$ from far end transmitter passing through a voltage divider with impedance R in series with the line impedance, Z_L . The voltage at the center of this voltage divider consists of the received signal, $r(t)$, plus the feedthrough transmitted signal, $y(t)$. To cancel the undesired feedthrough transmitted signal at the center of this node, a second voltage divider consisting of impedances R in series with a fixed balancing impedance Z_B generates a replica of the transmitted signal, $y(t)'$, and a differential amplifier is used to subtract the replica from the signal across the transformer. When $Z_B = Z_L$, the replica, $y(t)'$ will be identical to the actual near end transmitted signal, $y(t)$, making the loss from transmit to receive port will be infinite.

Figure 2.6: Example transformer hybrid network [LM88].

As a consequence of cable attenuation, the transmitted far end signal may experience attenuation of greater than 40 dB on the lossiest loops⁶. Typical specifications of a 10 dB trans-hybrid loss of the feed-through echo signal will imply that the received signal may be 30–40 dB below this interference which suggests further attenuation of the echo signal is required. The further eradication of the interference is achieved by means of adaptive cancellation techniques to achieve greater isolation between the transmitted and received signal. An adaptive *echo canceller* is used to learn the impulse response of the echo channel creating an accurate replica of the echo signal and subtracts the replica signal from the received signal to cancel the interference. Since a *signal-to-noise ratio* (SNR) of at least 20 dB is required for reliable data transmission [Mes86], the echo canceller is required to achieve a degree of cancellation of the order of 50–60 dB of the echo signal.

A major factor which makes the echo cancellation scheme attractive is its ability to provide better range (longer loop length) with only half the bandwidth requirement commanded by the other schemes mentioned previously. As a result of its lower bandwidth requirement, it is more tolerant to cable attenuation and near end crosstalk coupling. Furthermore, full duplex simultaneous transmission and a line transmission rate equal to that of the data rate makes this scheme very appealing.

The main difficulty in the echo cancellation scheme lies not in the algorithm but in its complex realization, arising from the tremendous degree of cancellation and signal processing task that is required. Nevertheless, the advancements in *very large scale integrated* (VLSI) circuit techniques will likely reduce the cost of the complexity involved in realization of the echo canceller, making the hybrid system very competitive to the other transmission methods. This method of duplex transmission has been gaining acceptance, and in most parts the method of choice for simultaneous duplex transmission on the digital subscriber lines. And, most recently standard development within ANSI indicates the adoption of this scheme for the implementation of

⁶A line attenuation of 40–50 dB is measured on a 5 km subscriber line at 80 kHz [AHM82a].

the North American Basic Access to ISDN [Ame88].

2.4 The U-Interface Reference Point

The location of the interface to the ISDN access line is defined in the North American standards as the *U-interface* reference point [Ame88]. It describes the full duplex digital data signal connection on the two-wire subscriber line between the serving center (or central office) *line termination* (LT) and the customer premise *network termination* (NT) [Mes86]. The *U*-reference point is the interface where the duplex four-wire transmission system at the subscriber network end is converted to the duplex two-wire transmission system which accesses the basic ISDN network.

The ISDN *U*-interface transceiver is required to furnish a full duplex *Basic Access* transmission rate of 160 kbits/s⁷ using the 2B1Q (two binary, one quaternary) line code based on the echo cancellation transmission scheme [Ame88]. The 2B1Q line code is a ± 3 and ± 1 four level code, (where two bits of user data is encoded into one of the four-level symbols) which allows information to be transmitted at half the data rate of 80 kbauds/s. This line code was chosen due to its narrow bandwidth characteristic. This makes the system less susceptible to line attenuation effects and more tolerant to crosstalk noise due to its lower signaling rate. However, the 2B1Q line code has a large content of low frequency components which results in a much longer tail in the received baseband pulse over the subscriber lines due the DC and low frequency cutoff of the DSL channel. This demands greater complexity and higher precision signal processing to be implemented on the 2B1Q transceiver.

⁷The Basic Access rate consists of two B-channels of 64 kbits/s, one D-channel of 16 kbits/s, and a maintenance and supervisory channel of 16 kbits/s

Chapter 3

Digital Subscriber Loop Channel Modeling

In anticipation of the growing demand for the ISDN digital transmission services over the existing telephone network, it is important to assess the digital transmission capability of the 2-wire twisted-pair subscriber loop plant and to design appropriate transceiver elements. The design of any digital transmission system requires accurate and efficient verification environment. The methods of assessing such a system can be performed by either: simulation, emulation, or prototyping (bread-boarding).

During the last decade, tremendous advances has been achieved in computer hardware technology making the computer an increasingly capacious and faster computing “*work horse*”. Consequently, it makes computational methods for the analysis and design of complex systems, which previously was very time consuming and impractical, more and more appealing today. This leads to the prevalent use of computers as a tool to execute initial study for the analysis, performance, and feasibility of complex systems even before their actual construction. A simulation-based approach appears to be the most cost effective and efficient method for initiating such investigations. The ideal simulation evaluation environment would include exact functional models of the system components.

In this chapter, the characterization of the DSL system components for the modelling and simulation of the DSL channels will be presented. The discussion is restricted to the DSL system employing the hybrid echo cancellation transmission scheme.

3.1 Modelling and Simulating the Digital Subscriber Loop Components

The constitution of the front-end of a digital communication system in a DSL using the hybrid echo cancellation transmission scheme is typified by the block diagram shown in Figure 3.1. The system consists of a transmit and receive path. The transmit path of the transceiver consists of a *digital-to-analog* (D/A) converter, a pulse shaper, a band-limiting low-pass filter, a line driver, and a hybrid coupler which acts as the line interface. The hybrid coupler which is used to isolate the transmit and receive channels on the same cable pair at the line interface is also common to the receive path of the system. The receive path of the transceiver after the hybrid coupler consists of a line receiver, an anti-aliasing low-pass filter, and an *analog-to-digital* (A/D) converter.

For the modeling and simulation purposes of the DSL channel, each functional element of the system is treated as a modular component (*“black-box”*), so that any change to the individual elements of the DSL system has no effect on the remaining elements of the system. This will provide the foundation of a modelling and simulation environment which could be easily programmable and reconfigurable. Structured software organization and a robust programming environment is a must for the provision of the evolution of the overall system as well as for the maintainability and usefulness of the simulation environment.

The DSL channel (for the purposes of the succeeding reported work) is defined as the components of the transceiver’s front-end after the D/A converter in the transmit

Figure 3.1: Block diagram of line-interface system of a digital subscriber loop transceiver.

path and before the A/D converter in the receive path. It should be pointed out that in the discussion that follows in this chapter pertaining to the modeling of the DSL channel, only ideal line interface circuit components are assumed. Any nonidealities of the components in the system (for example, nonlinearities of the line drivers, pulse shaper or A/D and D/A converters which may introduce harmonic distortion into the signals) or impairments of the DSL channel (for example, impulsive and crosstalk noise) are not taken into account. To include such non-idealities and impairments of the channel to make the DSL channel model more realistic, models for such noise sources will have to be derived and incorporated into the overall system as functional blocks that produce these impairments.

The approach presented here for obtaining the overall response of the DSL channel uses the well-known technique of multiplying the Fourier coefficients of a time-domain signal by the appropriate transfer functions corresponding to the respective components of the system, then resuming to get the resultant time-domain behavior of the system. This approach has the advantage of being easily implementable on a digital computer. The method used for obtaining a model of the DSL channel is to first establish the frequency characteristic of each of the functional block that make up the DSL channel. The frequency characteristic for each functional block can be obtained

through various means using linear systems and electric circuit theory. The analysis is performed in the frequency domain using Laplace, Fourier or z-domain methods to derive the transfer functions of the functional blocks. From the derived transfer functions, the frequency characteristic of each functional block is computed at a set of discrete frequencies to approximate its continuous spectral characteristic. The overall system's spectral characteristic is obtained by performing a multiplication of the frequency characteristic of each respective functional block. This operation is equivalent to performing a time convolution of all the impulse responses of the respective functional blocks if a time-domain analysis were performed instead (this of course being a less efficient approach in the computational sense). Finally, the *Inverse Discrete Fourier Transform*¹ (IDFT) is used to obtain the time-domain impulse responses of the DSL channel for the end-to-end transmitted signal, as well as the near-end trans-hybrid echo signal. The accuracy attainable by the described methodology is acceptable for engineering assessments. The main disadvantages are that the method is limited to linear systems and requires the assumption of periodic waveforms (because of the Fourier analysis used). The latter, however, is not a severe restriction for the analysis of most digital transmission system like that of the DSL system.

The overall digital subscriber loop channel can essentially be simulated as two systems working in tandem—an end-to-end signal channel and a trans-hybrid echo channel. These channels are represented in terms of their respective impulse responses or, equivalently their corresponding system transfer functions. A simulation model for the DSL system is shown in Figure 3.2.

¹Due to computational efficiency the *Inverse Fast Fourier Transform* (IFFT), it is used to compute the IDFT. Justifications of using the DFT to approximate the continuous *Fourier Transform* or similarly the IDFT to approximate the continuous *Inverse Fourier Transform* and their relationship are presented in [CLW67].

Figure 3.2: Simulation model for the DSL system.

3.2 Two-Port Network Parameters

Techniques are available, based upon linear *two-port* network characterization, for analyzing and characterizing the various components on the DSL system (for example, the evaluation of the loop physical characteristics, that is, segment lengths and corresponding gauge types, locations and properties of bridged taps, etc.) [Lab82]. The two-port network approach may also be used to characterize complex circuit elements if the transfer characteristic of the element is not easily and directly obtainable. A physical transmission system like that of the DSL system shown in Figure 3.1, often can be represented as a tandem connection of linear two-port networks, each of which is described by an input-output relation of a *transfer function*.

3.2.1 ABCD-matrix Description of a Two-Port Network

There are several approaches for the characterization of the two-port network² but the one that suits our intentions best for obtaining the transfer characteristic is

²A discussion on the other approaches namely, the *z*-parameters, *y*-parameters, *g*-parameters, and *h*-parameters characterization method of the two-port network can be found in [Hue72]. For a more general purpose characterization where an arbitrary network is to be considered, a more general formulation method (for example, the *modified nodal analysis* (MNA) [VS83]) will have to be adopted.

Figure 3.3: Two-port network with definition of voltages and currents for the $ABCD$ -matrix.

the $ABCD$ -parameter description of the two-port network.

Let us consider a general two-port network that is characterized by its $ABCD$ -parameters, as given in Figure 3.3. It has four individual terminals, which has an input port and an output port for which we assume the reference directions for the input and output currents and voltages are as shown. The $ABCD$ -parameters are the quantities $A(s)$, $B(s)$, $C(s)$, and $D(s)$ which specify the relationship between the input voltage and current as functions of the output voltage and current. The exact relations are

$$\begin{bmatrix} V_i(s) \\ I_i(s) \end{bmatrix} = \begin{bmatrix} A(s) & B(s) \\ C(s) & D(s) \end{bmatrix} \begin{bmatrix} V_o(s) \\ I_o(s) \end{bmatrix} \quad (3.1)$$

where all quantities are functions of the Laplacian complex variable s which is a complex function of frequency, $s = j\omega$. The $ABCD$ -parameter relation in Equation 3.1 written in matrix form is commonly known as the *chain matrix*. Notice that the parameters are concerned with the transmission of a signal from the input port to the output port. As a result, the transfer function of the two-port network is easily obtainable by solving the set of linear equations described by Equation 3.1.

The device is characterized if we can determine the functional relationship between the input and output voltages v and currents i of the device. If we obtain an expression relating the voltages v to the currents i , we have effectively determined a mathematical *model*, or equation to represent the terminal characteristics of the element. Indeed,

Figure 3.4: Test conditions used to define the $ABCD$ -parameters of a two-port network [Hue72].

this functional relationship is used to *define* the element. The characterization of the $ABCD$ -parameters can be summarized in Figure 3.4.

One of the important properties of the $ABCD$ -matrix is the ease by which tandem connections of the two-port networks are handled. Consider a cascaded combination of two-port networks shown in Figure 3.5. The input-output relationships are given by

$$\begin{bmatrix} V_1(s) \\ I_1(s) \end{bmatrix} = \underbrace{\begin{bmatrix} A'(s) & B'(s) \\ C'(s) & D'(s) \end{bmatrix} \begin{bmatrix} A''(s) & B''(s) \\ C''(s) & D''(s) \end{bmatrix}}_{\text{tandem connection}} \begin{bmatrix} V_3(s) \\ I_3(s) \end{bmatrix} \quad (3.2)$$

$$\begin{bmatrix} V_1(s) \\ I_1(s) \end{bmatrix} = \begin{bmatrix} A_{eq}(s) & B_{eq}(s) \\ C_{eq}(s) & D_{eq}(s) \end{bmatrix} \begin{bmatrix} V_3(s) \\ I_3(s) \end{bmatrix} \quad (3.3)$$

The tandem chain matrices of the various elements in cascade may be represented by an equivalent single chain matrix through matrix multiplication. The matrix multiplication principle above extends to as many tandem elements as necessary and is often termed the *chain rule*. The overall transfer characteristic of the system is then equal to the product of all the individual characteristics. Once the $ABCD$ -matrix of

Figure 3.5: Tandem connection of two two-port networks.

an end-to-end circuit is obtained, it completely defines the desired electrical properties of the entire system.

The chain matrix gives us a ready technique for systematically analyzing a transmission system which consist of a combination of different circuit elements and components.

3.2.2 Computation of the the System Transfer Function from the $ABCD$ -parameters

Once the $ABCD$ -matrix of a system has been qualified, the overall transfer function of the system can be obtain by solving the system of linear equations obtained from the chain matrix relation shown in Equation 3.1 for a the system which has its output port terminated by an load impedance $Z_l(s)$, as that shown in Figure 3.6. The chain matrix equation is given by

$$V_i(s) = A(s)V_o(s) + B(s)I_o(s) \quad (3.4)$$

$$I_i(s) = C(s)V_o(s) + D(s)I_o(s) \quad (3.5)$$

But, at the output port we find that,

$$V_o(s) = I_o(s)Z_l(s) \quad (3.6)$$

Figure 3.6: Two-port network with load impedance Z_l .

Therefore,

$$I_o(s) = \frac{V_o(s)}{Z_l(s)} \quad (3.7)$$

Substituting Equation 3.7 into Equation 3.4 and solving for $\frac{V_o(s)}{V_i(s)}$, we obtain the transfer function of the system with load impedance $Z_l(s)$ express as

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{1}{A(s) + \frac{B(s)}{Z_l(s)}} \quad (3.8)$$

If no load impedance is actually present the system, the resulting transfer function may be obtained by setting $Z_l(s) = \infty$ in Equation 3.8, reducing the transfer function expression obtained from the $ABCD$ -parameters to simply

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{1}{A(s)} \quad (3.9)$$

3.3 Subscriber Loop Model

In this section, we are going to briefly summarize the main equations which are necessary to analyze the subscriber loop channel, starting from the line circuit-theory parameters.

The twisted copper pair cable used in the subscriber loop plant is a two-conductor cable with a uniform cross-section and hence can be viewed as a *uniform transmission line*. A uniform transmission line can be represented by a pair of conductors as shown in Figure 3.7. The physical properties of the cable (such as the conductivity,

Figure 3.7: A uniform transmission line, where x is the distance along the line.

diameter, and spacing of the conductors, and the dielectric constant of the insulation) determine the electrical *primary constants*, R , L , G , and C . These constants represent the uniformly distributed *series resistance* in ohms per unit length, *series inductance* in henries per unit length, *shunt conductance* in mhos per unit length, and *shunt capacitance* in farads per unit length, respectively, of the cable. All of these parameters of the transmission line are in general functions of frequency, and they differ for different cross-sections (for example, different gauge cables). Commonly, these parameters are determined experimentally for a given cable and operating temperature. The primary constants of cables used in the DSL application for the different wire gauges and operating temperatures have been tabulated [Ame88]³. A simple lumped-parameter model for a short section of a transmission line is shown in Figure 3.8.

While the details of the the cable characteristics depend on the cross-section geometry, operating temperature, and cable type, the basic theory of transmission line does not. The voltage and current as a function of distance along the line consists of two propagating waves, one from source to termination and the other from termination to source [LM88]. The former is termed the *source wave* and the latter is called the *reflected wave*. The transmission characteristic of the transmission line are described by two complex quantities, termed the *secondary constants*. The secondary constants comprise of two measures expressed as the *characteristic impedance* Z_0 and

³The methodology employed is exact if the cable data used are exact [Lab82].

Figure 3.8: Lumped-parameter model for a short section of transmission line [LM88].

the *propagation constant* γ . Both of these constants are calculated from the primary constants directly by the following relationships. The characteristic impedance, Z_0 is given by

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (3.10)$$

while the propagation constant, γ is expressed as

$$\gamma = \alpha + j\beta \quad (3.11)$$

or may be equivalently expressed in terms of the primary constants as

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \quad (3.12)$$

The characteristic impedance Z_0 gives the ratio of the voltage to the current at any point of the line (independent of its length, x) for either the source or reflected wave. The propagation constant can be described as a function of the line's *attenuation constant* α and the *phase constant* β which are respectively the real and imaginary parts of Equation 3.11. The attenuation constant has the units of *nepers per unit length* and the phase constant has the units *radians per unit length*. The derivation of the above equations can be found, for example in [Joh50].

Figure 3.9: Illustration of an open-ended bridged tap tapped into a uniform transmission line.

3.3.1 Uniform Transmission Line Model

Usually, the transmission properties of the loop are obtained, particularly where computer programs are written, using the concept of its $ABCD$ -matrix representation. The elements of the $ABCD$ -matrix for a uniform transmission line of length l given in terms of the secondary constants can be written as

$$\begin{bmatrix} A = \cosh \gamma l & B = Z_0 \sinh \gamma l \\ C = \frac{1}{Z_0} \sinh \gamma l & D = \cosh \gamma l \end{bmatrix} \quad (3.13)$$

where Z_0 and γ are defined in Equation 3.10 and 3.12. The derivation of the elements for the $ABCD$ -matrix for the uniform transmission line above can be found in [Bro73, Gri70].

3.3.2 Model for Open-Terminated Bridged Taps

As suggested earlier in Chapter 2, bridged taps are a common occurrence on telephone cables, especially in subscriber loops. Figure 3.9 shows a bridged-tap cable configuration of length l tapped into a uniform transmission line. It may be seen as a shunt impedance across the line. Assuming that the bridged tap is of an open

termination variety, the impedance looking into the bridged tap Z_{BT} may be derived from the $ABCD$ -parameters of the bridged tap as a uniform transmission line of length l which is given by

$$Z_{BT} = Z_0 \frac{\cosh \gamma l}{\sinh \gamma l} = \frac{Z_0}{\tanh \gamma l} \quad (3.14)$$

Furthermore, the $ABCD$ -matrix for the bridged tap as a shunt impedance is given by

$$\begin{bmatrix} A_{BT} & B_{BT} \\ C_{BT} & D_{BT} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_{BT}} & 1 \end{bmatrix} \quad (3.15)$$

resulting in

$$\begin{bmatrix} A_{BT} & B_{BT} \\ C_{BT} & D_{BT} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_0} \tanh \gamma l & 1 \end{bmatrix} \quad (3.16)$$

as the $ABCD$ -matrix for an open-terminated bridged tap.

3.4 Modeling of the DSL Line Interface Circuit

Using the concept of the $ABCD$ -matrix we can proceed to model the rest of the components in the DSL channel which compose the *line interface* circuit. The task is to derive the $ABCD$ -matrix expressions for the for the following line interface shown in Figure 3.10.

3.4.1 Hybrid Transformer Model

The schematic of the hybrid transformer which converts a four-wire transmission path to a two-wire transmission path adopted for the modeling exercise is depicted in Figure 3.11. The schematic shows a fully differential circuit for the suppression of a portion of the echo signal using *common-mode* rejection provided by the differential topology of the circuit. The differential circuit is a way of achieving accurate performance and allows for simplification of the analog circuit. In addition, it results in an improved power supply rejection and higher noise rejection as compared to the single ended circuit approaches.

Figure 3.10: DSL line interface circuit [Lab].

Figure 3.11: Hybrid transformer of the line interface circuit [Lab].

Figure 3.12: Transformer model.

Transformer Model

A realistic model for the transformer⁴ in the hybrid transformer circuit will have to be adopted for the analysis of the line interface circuit. A transformer is a device consisting of two mutually coupled inductor coils. A transformer that has a high degree of coupling between the two coils is seen as a tightly coupled transformer with a *coupling coefficient* $k \cong 1$ [Bud87]. A tightly coupled transformer with an open *primary shunt inductance* of L_p , an open *secondary shunt inductance* of L_s , a *turn ratio* of $1:N$, and a *coupling coefficient* k can simply be modeled as a circuit shown in Figure 3.12. In the model adopted, the mutual interaction between the primary and secondary sections of the transformer is accounted for by the *current-dependent* current source $[kNI_s(t)]$ on the primary side and by the *voltage-dependent* voltage source $[kNV_p(t)]$.

A physical transformer that is fully characterized may be represented with the above mentioned transformer model as the circuit shown in Figure 3.13, whereby R_p

⁴The discussion and derivation of the model of a transformer can be found extensively in basic electric circuits text books, such as [Bud87, BV87, Mat64]. What is presented here is the discussion of the lumped parameter model of the transformer that was adopted for modeling of the hybrid transformer circuit.

and R_s are the *winding resistance* for the primary and secondary coils respectively, L_{lp} and L_{ls} are the *leakage inductance* for the primary and secondary coils respectively, and C_{sp} and C_{ss} are the *self capacitance* or *stray capacitance* for the primary and secondary coils respectively.

Figure 3.13: Physical transformer model.

Incorporating the ideal transformer model into the physical model and “lumping” the secondary winding resistance R_s , stray capacitance C_{ss} , and leakage inductance L_{ls} over to the primary side of the circuit by their equivalent elements by $R_{eq} = R_p + \frac{1}{N^2}R_s$, $L_{eq} = L_p + \frac{1}{N^2}L_{ls}$, and $C_{seq} = \frac{1}{N^2}C_{ss}$ we obtain the a simplified model of the physical transformer as shown in Figure 3.14.

Figure 3.14: Equivalent model for physical transformer.

3.4.2 Trans-Hybrid Channels of the Hybrid Transformer Circuit

It can be seen that there are principally three channels through the hybrid transformer circuit that needs to be characterized, namely the *trans-hybrid transmit path*,

Figure 3.15: Illustration of the transmit, receive and echo channels on the hybrid transformer.

receive path, and *echo path* as displayed in Figure 3.15. Including the physical transformer model of Figure 3.14 into the hybrid transformer circuit of Figure 3.11, the characterization of the $ABCD$ -matrix for the transmit and receive paths, as well as the echo path through the hybrid transformer were obtained. The characterization was performed by ignoring the primary stray capacitance C_{sp} and the assumption of a transformer coupling coefficient of $k = 1$ was adopted to allow for a more manageable analysis of the line interface circuit.

Loop equations for the various loops in the line interface circuit were derived from the schematic of the circuit. The node voltages and loop currents were solved from the loop equations using the *Mathematica* [Wol88] symbolic manipulation program. Following, the $ABCD$ -parameter characterization of the trans-hybrid transmit, receive and echo paths of the hybrid transformer as summarized previously in Figure 3.4 were obtained using the appropriate node voltages and loop currents. Verification of the $ABCD$ -matrices of the various trans-hybrid channels was performed by comparing the time and frequency responses obtained from the transfer functions derived using the $ABCD$ -parameters to that obtained from a circuit simulation of the equivalent circuits representing the various trans-hybrid channels using a commercially available electrical circuit simulator *HSPICE*⁵ [Met88].

⁵The current version of *HSPICE* only provides a model for the *lossless* transmission line, however,

Figure 3.16: Echo path model.

Trans-Hybrid Echo Path Model

The constitution of the subscriber loop plant influences the overall echo path of the hybrid transformer. Realizing this, the $ABCD$ -matrix and transfer function of the echo path in the hybrid transformer was derived as a function of the loop impedance.

The loop impedance of the subscriber loop, $Z_L(s)$ can be easily obtained once the overall equivalent $ABCD$ -matrix of the subscriber loop is derived. With reference to Figure 3.17, the total impedance looking into the input port of the subscriber loop plant as two-port network that is terminated by an impedance $Z_t(s)$ can be obtained as follows. From the chain matrix equation of the two-port network in Figure 3.17, we get

$$V_i(s) = A_i(s)V_t(s) + B_i(s)I_t(s) \quad (3.17)$$

$$I_i(s) = C_i(s)V_t(s) + D_i(s)I_t(s) \quad (3.18)$$

But at the output port we observe that

$$V_t(s) = I_t(s)Z_t(s) \quad (3.19)$$

a subscriber line used for the DSL is *lossy*. The transmission line element defined in *HSPICE*, models only one propagation mode which is generally adequate for modelling a single wire and ground plane, but, the subscriber line is a twin-lead transmission line that has two propagating modes.

Figure 3.17: Input impedance of a two-port network.

Substituting Equation 3.19 into Equation 3.17 and 3.18 and taking the quotient. The input impedance of the equivalent subscriber loop as a two-port network that has a termination impedance of $Z_t(s)$ can be expressed as

$$Z_L(s) = \frac{V_i(s)}{I_i(s)} = \frac{A_i(s)Z_t(s) + B_i(s)}{C_i(s)Z_t(s) + D_i(s)} \quad (3.20)$$

Using Equation 3.20 in the $ABCD$ -matrix of the trans-hybrid echo path, the resulting transfer function for the trans-hybrid echo channel which has termination impedance, $Z_r(s)$ at the receive port can be expressed in the form similar to that of Equation 3.8 as

$$H_{echo}(s) = \frac{1}{A_E(s, Z_L(s)) + \frac{B_E(s, Z_L(s))}{Z_r(s)}} \quad (3.21)$$

Transmission Path Model for the Subscriber Loop Channel

Once the trans-hybrid transmit and receive path $ABCD$ -matrices of the hybrid transformer, and the equivalent subscriber loop plant's $ABCD$ -matrix are derived, the transmission channel of the subscriber loop plant can be obtained by viewing the transmission channel of the subscriber loop as a two-port network as displayed in Figure 3.18.

Figure 3.18: Transmission channel of the subscriber loop.

Figure 3.19: Transmission channel model.

3.5 Transmission and Echo Channel for the Digital Subscriber Loop

The transmission channel and echo channel models of the subscriber loop are acquired in accordance to the system representation as depicted in Figure 3.19 and 3.20. They form the basis for the computation of the overall transfer function of the transmission channel and echo channels. The frequency characteristic of each element in the system is computed from their respective transfer function at a set of discrete frequencies. The overall transfer characteristic of the transmission and echo channels are obtained through the multiplication of the set of computed discrete spectral coefficients of the respective components of the subscriber loop system. Finally, the time-domain characteristic of the channels are obtained by computing the *Inverse Fast Fourier Transform* on the set of discrete spectral coefficients representing the overall transmission and echo channels, yielding the line channel impulse response and the echo channel impulse response respectively.

Figure 3.20: Echo channel model.

3.6 Simulated and Measured Line and Echo Responses

The final verification of the developed models for the various components of the line interface circuit, the hybrid transformer, and the transmission line and bridged tap equations was performed by comparing the simulated line and echo responses with that of the pulse responses obtained from measurements of the actual channels. The overall line interface circuit simulation of Figure 3.10 for the transmitted pulse shown in Figure 3.21 over a homogeneous 26 AWG PIC transmission line of varying line lengths between 0.4 km to 5 km for the line and echo responses is compared to its measured counterparts⁶. For the ISDN Basic Access Rate of 80 *kilo-bauds-per-second*, the frequency responses of simulated line and echo channels were calculated from DC up to 5.12 MHz (corresponding to half the sampling rate of 10.24 MHz) in equally spaced frequency samples. This translates into a 128-sample per baud impulse response in the time domain. Beyond half the sampling rate, the magnitude of the frequency responses are assumed negligible—an assumption equivalent to that having a *brickwall* low-pass filter with a cutoff at half the sampling rate as would be used if the actual measured responses were performed instead. The simulated⁷ line and echo pulse responses and the responses obtained through measurements are illustrated in

⁶The measured responses of the physical line and echo channels were provided courtesy of Mitel Semiconductor, Kanata, Ontario, Canada.

⁷The program segment of the definition for an example DSL loop constitution can be found in Appendix A.

Figure 3.21: Transmitted pulse produced by pulse shaper [Lab].

the following.

Figure 3.22: Measured and simulated line pulse response for a 0.4 km 26 AWG PIC cable.

Figure 3.23: Measured and simulated line pulse response for a 1 km 26 AWG PIC cable.

Figure 3.24: Measured and simulated line pulse response for a 2 km 26 AWG PIC cable.

Figure 3.25: Measured and simulated line pulse response for a 3 km 26 AWG PIC cable.

Figure 3.26: Measured and simulated line pulse response for a 4 km 26 AWG PIC cable.

Figure 3.27: Measured and simulated line pulse response for a 5 km 26 AWG PIC cable.

Figure 3.28: Measured and simulated trans-hybrid echo pulse response for a 0.4 km 26 AWG PIC cable.

Figure 3.29: Measured and simulated trans-hybrid echo pulse response for a 1 km. 26 AWG PIC cable.

Figure 3.30: Measured and simulated trans-hybrid echo pulse response for a 2 km 26 AWG PIC cable.

Figure 3.31: Measured and simulated trans-hybrid echo pulse response for a 3 km 26 AWG PIC cable.

Figure 3.32: Measured and simulated trans-hybrid echo pulse response for a 4 km 26 AWG PIC cable.

Figure 3.33: Measured and simulated trans-hybrid echo pulse response for a 5 km 26 AWG PIC cable.

Figure 3.34: A closer comparison between measured and simulated line pulse response for a 4 km 26 AWG PIC cable.

The simulated pulse responses obtained for the line and trans-hybrid echo channels show close correspondence with that obtained from measurements. There is however a slight discrepancy at the start of the trans-hybrid echo pulse response that is visible. The discrepancy could be attributed to capacitive and inductive effects that was present during actual measurements which was not considered for the simulation models.

Chapter 4

Quantization Noise in Oversampling Analog to Digital Converters based on Σ - Δ Modulation

The proliferation of digital techniques in most implementations of many *integrated circuits* (IC) involving signal processing is currently becoming more and more widespread, particularly so in the areas of digital data transmission. The implementation of digital systems versus a conventional analog technology has many advantages. In particular, the digital method is:

- Inherently free of component drift and circuit noise.
- Capable of more powerful and flexible algorithms due mainly to higher achievable accuracy.
- Easier to simulate and test.
- Easier to layout and adapt to future smaller feature size technology.

- More reliable and repeatable.

However, in many real time applications, virtually every *digital signal processing* (DSP) system requires an interface to the outside analog world. In cost-competitive IC applications, the problem then becomes one of designing the analog interfaces and integrating them with the DSP circuits.

Currently, the technology of choice for implementing digital ICs is the CMOS process, especially in light of the high packing densities and low power consumption achievable by the CMOS devices. However, with CMOS devices the design problem is made particularly acute for the analog interface designer because the CMOS fabrication process is generally optimized for the implementation of digital circuitry. In addition, the performance of the overall system is usually limited by the performance of the analog interface, so a high performance system requires a high performance converter. As a result, the emergence of powerful DSP implemented in CMOS VLSI technology creates the need for high resolution A/D and D/A conversion. Unfortunately, the same linear dimensional scaling in VLSI technology that makes possible the continuing dramatic improvements of available DSP complexity also severely constrains the dynamic range available for implementing interfaces between the digital and analog representation of signals.

In the realization of the ISDN *U*-interface transceiver, stringent linearity requirement of more than 70 dB¹ is commanded from the analog to digital blocks. Providing reliable circuits having these orders of absolute precision is difficult and expensive. This demand, together with the large baseband bandwidth, makes the development of the analog parts of the converter a very challenging task. The high demands on linearity of the A/D converter, and the requirement to avoid trimming, or self calibration cannot be fulfilled using standard approaches such as a simple capacitor or resistor networks.

¹Peak signal power versus total harmonic distortion power within signal bandwidth.

An increasingly popular architecture for A/D converters in such applications uses oversampled² techniques based on *sigma-delta* ($\Sigma\text{-}\Delta$) modulation, hence the name *oversampled* A/D³ converter. The advantages of the oversampling A/D converters over conventional ones are:

- No post-fabrication trimming or external components are required.
- Low quantization noise and distortion are obtainable.
- High degree of linearity is achievable without very complex and precise circuitry.
- Anti-aliasing filtering requirements are relaxed⁴.
- The architecture requires a minimal number of analog components and the analog circuitry in most parts is insensitive to component mismatch, gain, and settling time.
- It is very amenable for LSI and VLSI implementations due to its robustness against circuit imperfections.

²Oversampling implies that the signal be sampled at a rate much higher than the Nyquist rate. The Nyquist rate is the minimum sampling rate required to accurately reproduce the original signal from its samples.

³Oversampling A/D converters have been successfully used for the U-interface of an ISDN where monolithic high-resolution A/D conversion is required for echo cancellation [CGH⁺89, KHE⁺86, ACCC87, SRD⁺87].

⁴The sampling theorem states that a sampled signal can be perfectly reconstructed provided that the sampling frequency is at least twice the signal bandwidth (generally referred to as the Nyquist frequency/rate) and that the sampling occurs at uniformly distributed time instants. An anti-aliasing filter preceding the sampler ensures that the first of these requirements is fulfilled. Oversampled A/D converters put considerable less stringent requirements on this filter than Nyquist rate converters since the signal is sampled at a frequency which far exceeds its bandwidth.

4.1 Operation Principle of Oversampling Analog-to-Digital Converters

Oversampling A/D converters are encoders whose architecture is based on Σ - Δ modulator which combine sampling at rates well above the Nyquist⁵ rate with nonlinear feedback and digital filtering. The architecture of the converter is composed of two separate sections. The first consists of a Σ - Δ modulator that modulates the analog input into a *simple* digital form (by means of course quantization, typically one bit⁶ per sample) at a high sampling rate. It is followed by a digital low-pass filter which decimates the modulated digital code words at the Nyquist rate to produce the increased word length *pulse code modulation* (PCM) output, equivalent to that of a conventional A/D converter. Oversampling and decimation of the Σ - Δ modulator output⁷ is claimed to provide an overall result which is a good approximation to the action of the uniform scalar quantizer of the conventional A/D converters [Gra87]. In short, it is a class of system which employs oversampling and course quantization to achieve high resolution A/D conversion at a lower rate, whereby speed of operation and timing accuracy (easier to achieve in VLSI) replaces the associated precision in circuit elements and stringent tolerances (a difficult task in VLSI) required in the

⁵The Nyquist rate is the minimum sampling rate required to accurately reproduce the original signal from its sample as defined by the Sampling Theorem.

⁶Multilevel quantization is possible [Can74], it is commonly used to reduce the modulation or sampling rate. However, this option requires multiple threshold spacing in the modulator to be established which requires precision circuitry. This of course, defeats the purpose of resorting to the oversampling A/D converter architecture which promises an implementation which eliminates the need for precise and complex circuitry. With a single threshold, the inconvenience of establishing threshold spacing is alleviated.

⁷Information theory [Sha48] predicts that when a band-limited signal is oversampled, the output data can tolerate the reduction in amplitude resolution, and yet maintain a similar in-band signal-to-noise ratio. The band-limited signal is oversampled and quantized, with the result that only a fraction of the total quantization noise power corrupts the signal [Haw89].

implementation of high resolution conventional A/D converters. This tradeoff is of importance for integrated circuit design.

4.1.1 Noise Shaping Section of the Oversampling Converter

To utilize the full advantage of oversampling, the analog-to-digital conversion process must be combined with that of *noise shaping* through which a high level of activity or *chaotic*⁸ behavior is induced within the modulator such that large-scale errors introduced through coarse quantization in the modulator is transformed and spectrally shaped by the modulator in such a manner that the noise contribution in the signal band is minimized and taking on a more benign form. The oversampling process evenly distributes the overall quantization noise over a greater bandwidth ranging from DC to half the sampling rate while the noise shaping mechanism of the modulator shifts the noise from the signal band to frequencies well outside the band of interest. The quantization noise can be viewed as a wide-band noise source which is spectrally weighted by the modulator.

The quantization noise energy is then removed without affecting the signal band by a decimating digital low-pass filter operating at the output of the modulator. Typically, a digital *finite-impulse response* (FIR) low-pass filter is used to perform the decimation and anti-aliasing task. It has the advantage of being relatively insensitive to coefficient roundoff error.

The modulating encoders usually used for noise shaping belong to a family of digital pulse modulation system in which the discrete amplitude output pulses and its density are made to vary in accordance with the input signal at the sampling instants. Such systems are related to a class of non-linear sampled-data feedback control system. Familiar examples of such techniques used in oversampled data conversion

⁸The behavior of nonlinear systems that operate within a recursive environment which exhibit nondeterministic behavior, where the slightest change in initial conditions or system parameter can have dramatic effects on future system states.

Figure 4.1: Block diagram of a basic Δ modulator

circuitry include delta (Δ) modulation and Σ - Δ modulator.

4.1.2 Delta Modulation

Initial work on oversampled encoders was mostly theoretical and based on Δ modulation [Goo69, Ste75]. Δ modulation can be classified under the order of differential pulse code modulation which assumes a high degree of correlation between successive samples of a band limited signal. This assumption is correct when the signal in question is sampled at or faster than the Nyquist rate, particularly when oversampling is performed.

The principle of Δ modulation is to encode the *sign* of the difference between the present value of the input signal and its previous sample into binary pulses or *bit streams*. The block diagram of the basic Δ modulator is depicted in Figure 4.1. The general system consists of the following components. A band-limited analog signal $x(t)$ forms the input to the modulator. The bit stream output of the modulator $q(t)$ consists of a pulse train having amplitudes of either $\pm\Delta$ spaced uniformly in time during the sampling instants. The binary quantizer output is described by

$$q(t_n) = \begin{cases} +\Delta & \text{if } e(t_n) \geq 0 \\ -\Delta & \text{if } e(t_n) < 0 \end{cases} \text{ where } t_n \text{ is the } n\text{-th. sampling instant} \quad (4.1)$$

Figure 4.2 illustrates an example of how the signals $\hat{x}(t)$ and $q(t)$ within the Δ modulator vary with time to track the input analog waveform $x(t)$. At the n -th. sampling instant, the output pulse from the previous sampling instant, $q(t_{n-1})$ is locally decoded back into an analog waveform by the integrator in the feedback loop of the modulator producing the reconstructed analog input signal $\hat{x}(t_n)$. $\hat{x}(t_n)$ is then subtracted from the $x(t_n)$ to form the error signal $e(t_n)$ which is quantized to one of two possible levels $\pm\Delta$ depending on its polarity to produce $q(t_n)$. It should be noted that it is the *sign* of the error that is quantized and not its magnitude. The integrator in the feedback path will produce an increase of a positive step⁹ at its output if $q(t_{n-1})$ is a positive pulse while the reverse occurs if $q(t_{n-1})$ has the opposite polarity. As a result, the reconstructed analog signal $\hat{x}(t)$ is a stair case shaped waveform which oscillates about and tracks the input $x(t)$ as shown in the example. $\hat{x}(t)$ represents the quantized form of the analog input signal and it differs from the original analog input $x(t)$ by the quantization error $e(t)$ induced from the previous sampling instant. The close-loop arrangement of the Δ modulator ensures that the error signal $e(t)$ is minimized through the switching of the output pulses allowing the feedback signal to follow the input signal. The modulator attempts to generate a bit stream pattern $q(t)$ whose average value approximates the mean of the slope of the input signal over a brief time window. In other words, the bit stream output of the modulator is representative of the instantaneous slope of the input signal $x(t)$. From the example, it can be seen that if the slope of the input signal $x(t)$ is positive and while this condition still exists the output pulse stream $q(t)$ has more positive pulses than negative ones. The reverse occurs when $x(t)$ has a negative slope. Furthermore, at the maxima of the input waveform where the slope is close to zero, there are approximately equal number of positive and negative polarity $q(t)$ pulses. The same can be said for the minima of the input waveform.

⁹The integration of a ideal impulse function having a positive weight is an step function having a step size of the impulse weight.

Figure 4.2: Δ modulator waveforms within the structure.

Figure 4.3: Δ modulation demodulator.

The modulation process executed by the Δ modulator can be seen as a form of differentiating the input signal $x(t)$. The modulated signal $q(t)$ comprises of a quantization noise component and a signal component where the rate of occurrence of each binary pulse is directly proportional to the rate of change of the input amplitude. In order to recover the input signal component from the bit stream $q(t)$, the demodulation process would consist of first integrating the bit stream sequence as in the feedback loop of the modulator. This reverses the differentiation operation performed by the modulator and produces a reconstructed signal which is identical to $\hat{x}(t)$ in the feedback path modulator. Following the integration process, the reconstructed signal is low-pass filtered to remove the high frequency quantization noise component, thus, recovering a replica of the original analog waveform $x(t)$. The demodulation scheme of the Δ modulation output bit stream is shown in Figure 4.3.

A common deficiency in the Δ modulation scheme, other than the quantization error, arises when the feedback waveform $\hat{x}(t)$ is unable to track the input signal $x(t)$ closely, that is, $\hat{x}(t)$ does not always vary about $x(t)$ as depicted in Figure 4.2. This problem is referred to as *slope overload* and is exemplified in Figure 4.4. The situation emanates when the slope of the input signal $x(t)$ is greater than the maximum slope associated with the feedback signal $\hat{x}(t)$. However, this is not generally the case as during the condition of slope overload the slope of the input may even be zero, as is apparent near the maxima and minima of the input waveform from Figure 4.4. It is noted in [Ste75] that the overload characteristics in the Δ modulator is a function

Figure 4.4: Slope overload in the Δ modulator.

of the input signal frequency. As a result, Δ modulation is suitable for input signals whose spectral densities fall with increasing frequency and whose sample values are highly correlated. This shortcoming limits the use of Δ modulation in A/D converter circuits for a broader range of input signals and applications. Especially, in the ISDN setting where the analog interfaces of the transceivers must accept a wide range of signals, and their design may not rely on properties of restricted classes of signals nor properties of special receivers. Furthermore, the architecture of the Δ modulator is very sensitive to the imperfections and mismatch of the components of the D/A in the feedback path because the D/A imperfections are multiplied by the large baseband gain of the integrating filter in the demodulator [Can85].

From the description above, we see that the Δ modulator can be viewed as an A/D converter structure having an analog input signal $x(t)$ and a digital binary output bit stream signal $q(t)$. Nonetheless, in order to use it to produce a multibit representation of a sampled waveform as in a conventional PCM A/D converter, further processing

of the bit stream output has to be executed. Since a differentiation process was involved in producing the bit stream output of the Δ modulator, the signal content embedded in the bit stream will acquire a power spectral density that is high-pass in nature. Unfavourably, the power spectral density of the quantization noise is also of a high-pass variety, thus making the post processing (employed to discriminate the signal component from the quantization noise) of the bit stream directly difficult. To overcome this difficulty, an extra integrator is included preceding the Δ modulator to produce an input to the Δ modulator which is an integrated version of the original input signal. This forces the signal component in the output bit stream of the Δ modulator to procure a power spectral density which has baseband characteristics. Thus, making the separation of the input signal content and the quantization noise of the bit stream output directly an easier task. This modified arrangement of the Δ modulator yields an architecture called the Σ - Δ modulator.

4.1.3 Sigma-Delta Modulation

Sigma-delta (Σ - Δ) modulation, as is Δ modulation belongs to the family of differential pulse code modulation system. However, the distinction between the two modulation schemes is that the output bit stream of the Σ - Δ modulator is driven to match the input signal in an integrated error sense, unlike Δ modulation, where the output bit stream encodes the difference between the successive samples of the input signal.

A construction of a simple first order Σ - Δ modulator is given in Figure 4.5. The Σ - Δ modulator in principle resembles a Δ modulator which is preceded by an integrator. The input signal to the modulator is first integrated before it is encoded into a bit stream by the Δ modulator. The waveform at the output of the integrator in the feedback path of the Δ modulator, $\int \hat{x}(t)$ now tracks the integral of the input signal $x(t)$ with some error $e(t)$, instead, producing an output bit stream which oscillates between the binary levels that bracket the input amplitude in a way that keeps the

Figure 4.5: Block diagram of a first order Σ - Δ modulator.

average pulse density proportional to the applied input signal level.

Since the modification to the architecture involves only the forward path of the structure, it is evident that only the signal characteristic will be altered. The noise content generated through the quantization process in the feedback loop remains unchanged as the integrator at the input to the Δ modulator is not in the noise path of the modified structure. The integration process at the input of the Δ modulator causes the signal information embedded in the output bit stream of the Δ modulator to be located at baseband frequencies. Consequently, low-frequency components of the modulated pulse stream represents the input signal directly. At the same time, the noise shaping process is preserved, retaining the high-pass nature of the quantization noise process. The noise shaping process in the Σ - Δ modulator can be viewed as making a prediction of the quantization noise situated at low-frequencies and subtracting it from the signal [Can74, TC90]. While the Δ modulation scheme tries to make predictions of the signal values, Σ - Δ modulation on the other hand makes predictions of the quantization noise.

A rearrangement of the integrator positions in the feedback loop can further reduce the number of integrator blocks required for the construction of the first order Σ - Δ

Figure 4.6: Alternate arrangement of the first order Σ - Δ modulator.

code. The two integrator blocks in the architecture shown in Figure 4.5 can be replaced by a single integrator after the summing node in the forward path of the feedback loop as illustrated in Figure 4.6. The Σ - Δ modulation system shown here is exactly equivalent in operation to the architecture shown in Figure 4.5. The error signal produced in this arrangement before the quantizer is given by

$$e(t) = \underbrace{\int x(t)dt}_{\substack{\text{integrator} \\ \text{output at } \Delta \\ \text{modulator} \\ \text{input}}} - \underbrace{\int \hat{x}(t)dt}_{\substack{\text{integrator} \\ \text{output in} \\ \text{feedback path} \\ \text{of } \Delta \text{ modulator}}} \quad (4.2)$$

where the signals $x(t)$ and $\hat{x}(t)$ in the structure is integrated before the error signal $e(t)$ is formed. By reordering the position of the integrators, we find that in the modified arrangement, a difference signal is formed before the integration is performed to produce the error signal $e(t)$, which can be written as

$$e(t) = \int \{x(t) - \hat{x}(t)\}dt \quad (4.3)$$

Equation 4.2 and 4.3 show that the signal present at the input of the quantizer are

Figure 4.7: Demodulation scheme of Δ - Σ modulation

essentially identical, and therefore suggests that both the Σ - Δ modulation system shown in Figure 4.5 and Figure 4.6 are indeed equivalent.

Since the Σ - Δ modulator is in essence a Δ modulator which integrates its input prior to modulation, the recovery process of the input signal $x(t)$ from the bit stream produced by the Σ - Δ modulator involves the addition of a differentiator to the demodulator of the Δ modulator (shown in Figure 4.3). This is to compensate for the extra integrator placed before the input to the Δ modulator. The demodulation scheme is depicted in Figure 4.7. The structure of the demodulator can be further simplified by removing the integrator and differentiator blocks as they are complementary operations and can therefore be eliminated to produce a demodulator which simply consist of a sharp cut off low-pass filter to remove the effects of quantization.

The operation of the Σ - Δ modulator is such that the transfer function of the modulator seen by the signal and noise are distinct. Where the signal content is concerned, the modulator should ideally possess a transfer function which has a low-pass filter type characteristic with minimal distortion in the signal band. On the contrary, for the quantization noise, the feedback structure should maintain a transfer function which is of a high-pass variety. The signal transfer function should be ideally flat in the signal band whereas the noise transfer function pushes the in-band noise out and reduces the proportion of the noise within the signal band; albeit the expense of amplifying the total noise power at higher frequencies. In other words, the bit stream output of the modulator consists of two components: first, a signal component which is modified by the signal transfer function, and second, a noise component (introduced

through quantization) which is modified by the noise transfer function.

Due to the deficiencies inherent in the Δ modulation scheme, the Σ - Δ modulator is a more favourable architecture for the implementation of oversampled A/D converters. The main advantage of Σ - Δ modulation over Δ modulation is that it is more robust to circuit imperfections and component mismatches. This is because in Σ - Δ modulation the input signal content in the structure is located at baseband frequencies and the effective gain of the integrators is large in this region. As a result, the distortion and inaccuracies in the forward path of the feedback loop have only a second order effect on the overall properties of the modulator [Can74]. This reasoning could be attributed to the *demodulation* process of the Σ - Δ modulator's output bit stream. Since the low-frequency components of the modulated signal represents the input signal directly, no further post processing of the bit stream is necessary other than low-pass filtering the bit stream to remove the high frequency quantization effects. Whereas, Δ modulation requires the integration of the output bit stream in its demodulation process. The integrators intrinsically have large baseband gains that will amplify any nonlinear distortion which may have been embedded in the output bit stream of the Δ modulator (caused by circuit imperfections and component mismatches in the forward path of the modulator). This makes the Δ modulation scheme more susceptible to circuit flaws. Additionally, the Σ - Δ could be more suitable for a much wider range of input signals and applications as it is observed in [Ste75] the the overload characteristics of the Σ - Δ structure is independent of the frequency of the input signal. However, as will be discussed in the following sections, the overload and quantization noise characteristics of the Σ - Δ modulator is in fact a *function of the input signal amplitude*.

So far, the discussion on the topic of noise shaping has been limited to that of the first order structures, this was done so as to familiarize the reader with the mechanics and workings of the noise shaping modulator. It should be pointed out that there exists other variations of the Σ - Δ modulator architecture used for the implementation of

oversampling A/D converters. Such architectures include higher order serial [Can85, MUI+87, KGWK86] and cascaded structures [RvBR+89, LC88, CWG89, UHKI86] which uses multiple modulators to achieve higher order noise shaping functions. The higher order noise shaping functions shapes the quantization noise spectra in such a manner that results in a lower quantization noise power which spans over a much wider baseband bandwidth. Although, the higher order noise shaping is able to suppress the quantization noise at frequencies of interests more effectively, it is generally known that the quantization noise power in such structures tend to increase more rapidly the higher the order of noise shaping employed. Typical noise spectra of the

Figure 4.8: Typical noise spectra example of a first-order, second-order and third-order Σ - Δ modulator.

higher order Σ - Δ modulator is given in Figure 4.8. Note that noise shaping moves the noise away from baseband, at the expense of increasing the total noise power at higher frequencies. Consequently, the conversion of the bit stream output of such modulator to its equivalent PCM digital representation requires a decimation filter which is of a higher order that has a sharper cut-off characteristic to suppress the higher order quantization effects. These architectures promise better resolution and

bandwidth performance figures through their more complex noise shaping capabilities at the expense of requiring more precise¹⁰ analog circuit components, and inherent instability problems.

4.1.4 Performance Characteristics of the Σ - Δ Modulator

Although there are many other parameters of the architecture of the Σ - Δ modulator that influences the performance of the structure, for example, the integrator gains, these parameters are intrinsic to a particular structure, the overall behavior of the Σ - Δ modulator depends markedly on the amplitude of the input signal. There are principally three distinct regions of input signal range: high input which drives the structure into saturation, normal region where the structure typically operates and acts as a high resolution A/D converter, and idle channel which the input signal amplitude is very small. The graph in Figure 4.9 shows an example *signal-to-noise ratio* (SNR) versus input signal power which delineates these three regions of operation of the Σ - Δ modulator structure. The abscissa of the graph shows the input signal power computed with respect to the quantizing level Δ in decibels (dB). The shape of the SNR curve of the Σ - Δ modulator appears to be a constant for very low input levels, and gradually takes on a linear function of the input signal when there is enough signal content within the structure, and finally as the input signal level approaches the quantizing levels there appears to be a drastic degradation in the SNR characteristic of the structure.

In the idle channel region of operation, the SNR curve tends to flattened out, indicating that the distortion is proportional to the input signal level. A heuristic explanation is as follows: in the idle channel condition the bit stream output of the Σ - Δ modulator primarily consist of a very *stable-pattern* where the quantization noise is highly correlated, the effect of the input signal is to disrupt the idle-pattern's spectrum in a manner akin to frequency modulation [AS83]. At baseband frequencies

¹⁰The higher noise shaping coders is more sensitive to component accuracy.

Figure 4.9: Typical Σ - Δ modulator signal-to-noise ratio characteristics.

lies the component of the input signal and its harmonics whose amplitude are directly related to the input signal level. Since the harmonics are the primary components of the distortion and they are a function of the input signal, the SNR remains relatively constant.

The normal region is characterized by the linear relation between SNR and input signal power. The curve in this region is substantially linear, indicating that the noise power is relatively constant. In this region, the quantizing error can be seen as being uncorrelated with the input signal amplitude. It is in this region of operation which the Σ - Δ modulator acts as a high resolution A/D converter.

In the overload region, we observe a decline of the SNR characteristics as the input amplitude is increased prior to the saturation levels. Here, the instantaneous quantization noise frequently exceeds the quantizing levels for large input amplitudes

due to the very high signal variance encountered by the integrators of the modulator as reported by Candy [Can85]. Since the output bit stream of the modulator is always oscillating between two quantizing levels, the output power is fixed, independent of input power. The output power must be shared between *signal* and *noise*. And when the high amplitude input signal drives the structure into saturation, the noise due to quantization forms a major component of the modulator pulse stream. The total distortion components may include harmonics of the input signal, indicating that the quantization error signal is highly correlated with the input signal. One of the practical implications when the structure is operating in the overload region as described above is when the integrators are driven into saturation. The stability of the Σ - Δ modulator depends on the manner in which the integrators come out of saturation and is dependent on the actual circuit involved.

4.2 Motivation and Scope of Modelling the Σ - Δ Modulator

The primary motivation for the undertaking of the succeeding reported work on the Σ - Δ modulator was for the development of an efficient *systems-level* model for simulating the oversampling A/D converter architecture which is typically employed for the ISDN *U*-interface transceiver. The developed simulation model could to be incorporated into the systems-level simulation environment of a transceiver to provide worthwhile insight into the important system-level design issues, such as stability and convergence behavior of the various adaptive digital signal processing blocks of the transceiver.

The theoretical analysis of Σ - Δ modulators is considered an extremely difficult problem [HKB90, BBS⁺90] even if ideal components are assumed. This is due to the active feedback arrangement and grossly nonlinear characteristics of the modulator [GV68, Ath75, Ath81]. Usually, functional simulation techniques have been employed

to examine the design trade-offs and performance measure of the modulator because the use of conventional circuit and system analysis to the study the higher order Σ - Δ modulators has, to date, proven to be intractable [BW88]. By contrast, the cycle-by-cycle functional simulation of modulator's operation in the time domain is a relatively simple task. Unfortunately, to obtain an understanding and accurate performance estimates of such converters, notably time-consuming and computationally intensive numerical difference equation simulations of long data traces are required. This is due to the oversampling process and the long term memory of the modulator's structure. The speed of simulation is of overwhelming importance as the modulator must be simulated for a large number of clock cycles, often tens of thousands, to obtain any useful understanding of the operation of the modulator. To make matters worse, to include such simulations in the transceiver system-level simulation setting is just unrealistic and impractical, especially when the simulation of a transceiver may span a very large number of symbol periods together with the converter's oversampling rate that is typically several tenfolds the baud rate of the transceiver. In spite of the overhead, it is only the numerical simulation that can provide the required confidence in the design and optimization of system performance, and the verification of new algorithms adopted for the transceiver architecture. As a result, a computationally efficient model which could capture the effects of quantization in the Σ - Δ modulator could prove to be a useful endeavour.

The treatment of the investigation and modeling the impairments of the Σ - Δ modulator used for the implementation of oversampling A/D converters is restricted to a noise analysis that is concerned with the quantization effects introduced when all the components and parameters of the modulator are ideal. The study of the effects of circuit imperfection and other sources of noise in the Σ - Δ modulator has been attempted [Dav87, Ril89] and is beyond the scope of the thesis. The main emphasis of the work here is to study the mechanics and operation of the Σ - Δ modulator for the development of its simulation model. The model should capture the effects of algo-

rithmic nonlinearities indigenous to the system due to the hard-limiting of the signals by the quantizer as well as amplifier saturation of the integrators in the modulator. Furthermore, we shall assume ideal characteristics for the interpolation/decimation¹¹ low-pass filter function and concentrate more on the performance of the noise shaper.

For the purposes of this thesis, the analysis will be restricted to the second-order serial coder structures. Even though, higher order coders are sometimes preferred because of their superior noise performance, increased resolution and relative freedom from harmonic quantization effects. However, these higher-order systems suffer from potential instability due to the accumulation of large internal signal variances in the integrators occurring from high input signals and their sensitivity to certain values of the loop parameters. As a result, the available dynamic range of the converter employing the higher order structures is reduced unless painstaking design steps are undertaken. It is documented that when more than two integrators are used, the structure has the tendency to lock into undesired modes of operation where by its performance is ruined for high input levels [Can85, AP87]. In addition, the higher the order, the more complicated the analysis and less tractable the problem becomes. Due to the above and its very common usage, the second order serial structure seems like the ideal candidate for analysis purposes.

The scope of the analysis defined may initially seem restrictive, however, the method employed which will be presented in the following sections can be extended to higher order modulators or modulators with different architectures other than the one discussed here. This is possible because regardless of the configuration, it is theoretically conceivable to derive a set of difference equation and the corresponding transfer function of the discrete time system model that approximates the continuous time system which provides a full description the modulator. Obtaining the transfer functions to describe the modulator is quite straight forward. Thus, the analysis is

¹¹The performance of the converter depends heavily on the filter used. Typically, the order of the filter used should be at least higher by one than the order of the noise shaping function implemented [KHE⁺86].

generally performed based on the transfer function and its associated discrete-time difference equation representation of the modulator.

Although $\Sigma\text{-}\Delta$ modulation is conceptually simple, the system is difficult to analyze. An examination the literature at hand on the subject reveals a lack of comprehensive theoretical analyses of the modulator which fully accounts for the nonlinearity of the system. The nature of the modulator's structure prohibits simple analysis — the feedback loop introduces stability problems, and it contains a mix of analog and sampled digital signals that include non-linearities. Due to the complex dependencies of the feedback and nonlinearity inherent in the system, this makes the analysis of the modulator using regular linear systems theory methods directly not possible. Direct mathematical formulation has been developed to try to predict the complex behavior of the highly nonlinear system and to provide some worthwhile insights into important issues such as the *signal-to-noise ratio* (SNR) characteristics of the modulator and its stability. Regrettably, such treatments has been limited to first order coders with extremely confining assumptions¹² with a very restricted class¹³ of input signals [Gra87, Gra89, GCW89, CB81]. More recently the quantization noise issues for the second-order structure and more generic type of architectures have been addressed [LKB90, HZ90, AP87, Sti88]. These approaches entail complicated analysis which may or may not be solvable for each different architecture.

4.3 Models for the $\Sigma\text{-}\Delta$ Modulator

The discussion that pertains to the $\Sigma\text{-}\Delta$ modulator thus far treats it as an analog device. Though, for the analysis and understanding of the dynamics and operations

¹²Such assumptions were made so as to reduce the analysis of the highly nonlinear system down to a simple linear model. The drawbacks of these simplifying assumptions will be further discussed in the sections to follow.

¹³The types of input signal used for the analysis of the $\Sigma\text{-}\Delta$ modulator has been limited primarily to well defined input signals, for example, sinusoidal or constant (DC) signals.

of the structure, a *discrete time* representation of the modulator better serves the purpose. The modulator can be treated as a discrete time system by inserting fictitious sample-and-hold circuit¹⁴ into the structure. This will allow us to approximate the actual behavior of the continuous time system using z -domain analysis. For an accurate system level analysis, the continuous-time information of the waveforms within the structure and the state of the subcircuits between sampling epochs is not necessary. Hence, the treatment of the modulator as a sampled-data system is useful because it allows for the analysis of the structure only at the sampling intervals.

An analog signal $x(t)$ is sampled to form a discrete time signal $x_n = x(nT_s)$ where $T_s = \frac{1}{f_s}$ is the sampling period. It is usually assumed that if $2W$ is the Nyquist rate of the original signal, then the oversampling ratio $R = \frac{f_s}{2W}$ where f_s refers to the sampling frequency is large. Most of all analytical developments found in the literature adopt such an assumption and as a result the input analog waveform can be seen to change very little over R samples sampled at the rate $2RW$. Such an assumption above makes the behavior of such systems for quiet or DC inputs of significant importance since it can be interpreted as an approximation to the performance for arbitrary inputs of bandwidth W . Such analyses for quiet inputs to the Σ - Δ would not be directly applicable for our purposes as we require a simulation model of the Σ - Δ modulator which operates in a much wider range of input signals.

The problem of studying nonlinear systems can be avoided altogether by simply reducing each nonlinear operation in the structure by an approximating linear operation and studying the resulting linear system [GV68]. This is commonly done when the analysis or modeling of the Σ - Δ modulator is required. The relation of this approximation to the performance of the actual system depends on the validity of the linearizing approximation. Basically there are several different paradigms for acquiring the quantization noise model for the Σ - Δ modulation system: *full measurement*

¹⁴The discrete time model of the Σ - Δ modulator would be a natural description for the switched capacitor implementation of the modulator.

based characterization of the quantization noise power of the structure, *exact analysis* technique, *simple additive white noise source approximation*, and the *quasi-linear* approximation for the nonlinearity element.

4.3.1 Full Measurement Based Characterization Approach

The easiest way of deriving a simulation model for the Σ - Δ modulator would be to obtain the *worst-case* noise figure of the device. The noise model is one which consists of an additive node which injects the worst case random distortion into the system independent of the input signal. This independent worst case noise source model although is representative of the worst case conditions of the A/D converter, it is not useful for a simulation in which design optimization of the various transceiver blocks (for example, the optimization of the nonlinear echo canceller section of the transceiver) is needed. Such a model can only provide an indication of the performance of the device during worst case conditions. Designing a system for the worst-case conditions will ensure reliable operation of the system but may sometime be an overkill of the design when the worst-case conditions do not frequently occur.

Another possible approach in the measurement based method is a model obtained through standard practice of quantifying the quality of an A/D converter by means of its response to sinusoidal inputs. The behavior of the quantization noise as a function of input signal amplitude is fully characterized through measurements of the actual device for each input signal range. The measurements obtained are used to derive a simple model for simulating the quantization effects of the device as a node that introduces additive noise which is input signal dependent (as defined from the measured characteristics of the quantization noise of the device). Although this approach reflects a much closer and more realistic behavior of the quantization noise of the device, an accurate and complete characterization is extremely difficult, especially when the converter is operating at a very high clock rate as in the oversampling A/D converter. Any modifications to the structure of the device will require a repeat of

the cumbersome measurement process. In addition, this method may require a very complex model.

4.3.2 Exact Analysis Approach

The basis of the *exact analysis* technique applied to the analysis of first Σ - Δ modulators for DC and sinusoidal inputs is contained in the papers by Gray [Gra89, GCW89]. And more recently, an analysis for the second order structure with DC input using a similar approach is presented by He, et al. [HKB90]. Instead of assuming the memoryless and uniformity characteristics, this approach tries to derive the true quantizer noise behavior by solving a system of nonlinear difference equations, and then actually determine the long-term noise spectrum and distribution. The analysis presented in these papers are generally limited to only the normal region of operation of the Σ - Δ modulator. The idle channel and overload regions of the modulator are overlooked. The direct employment of this approach in obtaining an computationally efficient simulation model with transient behavior of the modulator for all input regions are not easily obtainable and directly applicable. In addition, the mathematics required for such analyses are extremely complex and may at times not be solvable.

4.3.3 Simple Additive White Noise Approximation for the Σ - Δ Modulator's Nonlinearity

The simplest analytical model for the Σ - Δ modulator quantization noise is the additive white noise approximation for the modulator's quantizer. In this approach, one tries to model the quantization noise by choosing an input-independent additive noise source having a similar long-term average qualification as the actual quantizer noise. The quantization noise of the Σ - Δ modulator is commonly defined [Gra87, Gra89, GCW89] as the difference between the quantizer output and input. In the majority of the previous work on modeling and analyzing the Σ - Δ modulator's

quantization noise behavior [Can85, CB81, AS83], the system has been modeled by replacing the nonlinear element with a unity gain linear element followed by an *white* additive noise process. In other words, it is assumed that the binary quantization noise can be replaced by a white noise source, which is, signal independent, memoryless, and is a uniformly distributed sequence of random variables [Can85, Can74]. Such an assumption, thereby allows for the linearization of the nonlinear element within the structure and reduces the noise analysis to a simple matter of linear difference equations and linear systems spectral analysis. It is further assumed that the input to the modulator is sufficiently active to make the quantization noise random to allow the white noise assumption to be valid [CB81]. For the preceding assumptions to be valid, the simple model for the quantizer cannot account for the behavior of the system when it has large input signals that forces the modulator operate in its overload region¹⁵.

This simple model has proven to be inadequate for the accurate analysis of higher order modulator stability since it does not reflect the dependence of the nonlinear system on the input signal. Besides the stability issue, the simple model also fails to fully describe the dramatic degradation of the baseband SNR as the system is driven into saturation for increasing input levels as the simple model stipulates a constant noise power spectral density for all input signal amplitudes. This, however, is inaccurate, as the input signal amplitude increases towards the overload region as indicated in Figure 4.9, it is observed that the noise power actually increases while the signal component diminishes even for increasing input level and causing instability to the system resulting in the degradation of the SNR characteristic. This simple model

¹⁵The analysis of the sigma-delta modulator when driven into saturation maybe of importance in the application of digital subscriber loops due to the unpredictability of the types of signals and impairments encountered in the environment of DSLs, namely, impulsive noise, transformer overloading, etc. The occurrence of such events will cause transient overloading of the delta-sigma based A/D converter which may effect the convergence characteristic and performance of the adaptive signal processing blocks of the transceiver

cannot explain the increase in quantization noise power and the diminishing signal content in the output bit stream of the modulator for increasing input signal levels. Moreover, since the system involves a feedback structure it is unrealistic to assume that the additive noise process is independent and memoryless hence successive input cannot be assumed to be independent. In order to model the noise in the output of the one bit coder, it is more appropriate to include the global gain that is attributed the quantizer.

Regardless, the simple white noise model is used for most treatments of the Σ - Δ modulator for convenience and because some results based on the assumption do agree well with simulation and experimental results (overall SNR characteristics when the modulator is operating in its normal region, for example) [Gra89]. Clearly, such assumption can only give partial insight into the modulator's behavior, where a more detailed study requires the inclusion of a more accurate model for the nonlinear element that reflects the dependence of the nonlinear behavior of the system on its input signal levels.

4.3.4 Quasi-linear Approximation Model for the Σ - Δ Modulator's Nonlinearity

The quasi-linear approximation method described here is a derivative from nonlinear control systems theory. The underlying principle for the quasi-linear approximation approach is to determine the operation performed by the nonlinearity on an input of finite size and approximate this in some way by a linear operation [Ath75, Ath81, GV68, BF71, Vid78]. Its basis is to replace each nonlinear element in the system by a linear gain which is chosen to reflect the operation of the actual nonlinearity that is dependent on a given input to the nonlinearity. This however results in different linear approximation for the same nonlinearity when driven by inputs of different forms, or even when driven by inputs of the same form but of different amplitudes. Quasi-linearization results in a linear description of the system,

of/de

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but it is not true linearization since the characteristic of the linear approximation change with certain properties of the signals circulating through the system. A linearized model depends only on the system and the choice of nominal operating point while a quasi-linear model depends on the system and certain properties of the signals within the system. A completely linear model can exhibit only linear behavior, whereas a quasi-linearized model exhibit the basic characteristic of the nonlinear behavior: *dependence of performance on signal amplitude*.

The quasi-linear approximating functions, which describe approximately the transfer characteristics of the nonlinear system, are termed *describing functions*. The quasi-linear gains are dependent on the form and amplitude of the input signal to the system. These gains which are a function of the input signal will influence the overall transfer function of the model for the signal and noise. The solution procedure of the describing function method doesn't break down, in the sense of becoming more complicated. In the case for sinusoidal and constant signal, the order of the linear part is of very little consequence. In the case of random signals, the analytical expression for mean-squared signal levels becomes more complicated with increasing order of the system. Systems of arbitrary order can be handled with nearly equal facility.

The criterion used for the development of describing function is the minimum mean squared error. The quasi-linear systems used to approximate the nonlinearity are designed to minimize the mean squared difference between the output of that approximator and the output of the nonlinearity. As is always true in optimum linear theory — the quadratic error criterion, of all reasonable criteria, leads to the most tractable formulation of the optimum design problem. Not only is this approach tractable, but also because the development based on this criterion runs a very close parallel to other optimum linear theory based on the same criterion.

A major limitation on the use of these describing functions to describe system behavior is the requirement that the actual signal at the nonlinearity input is of a similar form as the signal used to derive the describing function. In other words, the

fundamental limitation of the describing function technique is that the form of signal at the input to the nonlinearity must be guessed in advance. This approach still is based on an assumed approximation and does not address the issue of deriving the behavior of the quantization noise (rather assuming it to have a specific form). A less obvious limitation is the fact that the analysis answers only the specific questions asked of it. Another difficulty which the user of describing function theory must be alert to is the possibility of multiple solutions. More than one solution may exist where the solutions represent different possible modes of operation of the system. A final limitation of the use of describing function theory is the fact that there is no satisfactory evaluation of the accuracy of the method. Since the describing function analysis technique must be based on the use of approximate analytic techniques, and these techniques will be inadequate to answer all questions regarding system behavior, the study must be verified — preferably by computer simulation — before accepting the analysis.

In the following, the characterization and analysis of the quantization noise behavior of the Σ - Δ modulator will be conducted using the describing function method. Such a method of characterization of the quantization noise for the Σ - Δ modulator was initiated by Ardalan and Paulos [AP87] of North Carolina State University and a similar type of analysis was being pursued at the same time by Stikvoort [Sti88] of Philips Research Laboratory. In [AP87], only DC and sinusoidal excitations are discussed. The analysis found in these publications account for the influence of the input signal level on the noise shaping function of the Σ - Δ modulator.

z -Domain Analysis of Σ - Δ Modulator Structure

A second-order double-loop Σ - Δ modulator used for discussion to be presented in the following is shown in Figure 4.10. The system is basically representative of two first order Σ - Δ modulators cascaded in a serial fashion. The structure is implemented with two integrators, a comparator or quantizer, a delay element, and gain stages (α_1 ,

Figure 4.10: Second-order Σ - Δ modulator used for analysis and characterization.

Figure 4.11: Discrete time representation of second-order Σ - Δ modulator.

α_2 , β_1 , and β_2) in the feedforward and feedback paths. The gain stages in the loop determines the overall transfer function of the structure and consequently the noise shaping characteristics to the modulator.

In order to analyze the structure, the continuous time system is converted to its discrete time representation to allow for a discrete time analysis using z -domain analysis, as shown in Figure 4.11. In the diagram, *integrator 1* is the discrete time representation of a simple integrator while *integrator 2* is a discrete time delaying integrator representing the continuous time integrator and delay element before the quantizer in Figure 4.10.

A z -domain block diagram representation of the discrete time system the modulator in Figure 4.11 is shown in Figure 4.12 where the integrators are represented

Figure 4.12: z -domain block diagram of the Σ - Δ modulator.

Figure 4.13: Block diagram of z -domain Σ - Δ modulator.

by transfer functions $H_1(z)$ and $H_2(z)$ respectively. The simple integrator's transfer function is given by

$$H_1(z) = \frac{1}{1 - z^{-1}} \quad (4.4)$$

and the delaying integrator's transfer function is given by

$$H_2(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (4.5)$$

It can be shown that any multi-loop system similar to that in Figure 4.12 can be represented by an equivalent single loop system shown in Figure 4.13 with the appropriate choice of loop filters $H_i(z)$ and $H_f(z)$. For the second-order structure analyzed, we have

$$H_i(z) = \frac{\alpha_1 \beta_1 H_1(z)}{\beta_2 + \alpha_2 \beta_1 H_1(z)} \quad (4.6)$$

and

$$H_f(z) = H_2(z)[\beta_2 + \alpha_2 \beta_1 H_1(z)] \quad (4.7)$$

Figure 4.14: Minimum mean squared error linearized gain modeling of nonlinearity.

Modelling of the Nonlinear Quantizer

The quasi-linear gain representing the nonlinearity can be obtained as prescribed by the describing function technique. The technique is summarized in the following and it is a generalization of the analysis presented in [AP87]. In order to model the nonlinearity, we associate a quasi-linear gain K_x with the signal component of the input to the nonlinearity, and similarly, a quasi-linear gain K_n is associated with the quantization noise component present at the input of the nonlinearity (due to the feedback loop of the Σ - Δ modulator).

The quasi-linear gains are obtained by solving a system identification problem of the system shown in Figure 4.14. Let us assume for the moment that the statistical properties of the signals present in the model of the quantizer are stationary. Then the identification problem is to determine the linear approximators K_x and K_n such that the mean-squared approximation error in modeling the nonlinear element using the quasi-linear gains is minimized. The error in the identification problem can be expressed as

$$e(t) = q(t) - K_x x(t) - K_n n(t) \quad (4.8)$$

We must therefore minimize

$$E\{e^2(t)\} = E\{[q(t) - K_x x(t) - K_n n(t)]^2\} \quad (4.9)$$

where $E\{\cdot\}$ denotes the time average or expectation operator. Expanding Equation 4.9 above results in

$$\begin{aligned} E\{e^2(t)\} = & E\{q^2(t)\} + K_x^2 E\{x^2(t)\} + K_n^2 E\{n^2(t)\} - 2K_x E\{q(t)x(t)\} \\ & - 2K_n E\{q(t)n(t)\} + 2K_x K_n E\{x(t)n(t)\} \end{aligned} \quad (4.10)$$

We obtain the minimum mean squared error criterion by taking the partial derivatives of $E\{e^2(t)\}$ and setting them to zero, we get

$$\begin{aligned} \frac{\partial}{\partial K_x} E\{e^2(t)\} = \\ 2K_x E\{x^2(t)\} - 2E\{u(t)x(t)\} + 2K_n E\{x(t)n(t)\} = 0 \end{aligned} \quad (4.11)$$

and

$$\begin{aligned} \frac{\partial}{\partial K_n} E\{e^2(t)\} = \\ 2K_n E\{n^2(t)\} - 2E\{u(t)n(t)\} + 2K_x E\{x(t)n(t)\} = 0 \end{aligned} \quad (4.12)$$

Solving the system of linear equations for K_x and K_n yields

$$K_x = \frac{E\{q(t)n(t)\}E\{x(t)n(t)\} - E\{n^2(t)\}E\{q(t)n(t)\}}{E^2\{x(t)n(t)\} - E\{n^2(t)\}E\{x^2(t)\}} \quad (4.13)$$

and

$$K_n = \frac{E\{q(t)x(t)\}E\{x(t)n(t)\} - E\{x^2(t)\}E\{q(t)n(t)\}}{E^2\{x(t)n(t)\} - E\{n^2(t)\}E\{x^2(t)\}} \quad (4.14)$$

If one assumes that the signal and the noise components at the input to the quantizer are independent and uncorrelated as was done in [AP87], implying that the term $E\{x(t)n(t)\} = 0$, then the complexity of the Equations 4.13 and 4.14 diminishes to

$$K_x = \frac{E\{q(t)x(t)\}}{E\{x^2(t)\}} \quad (4.15)$$

and

$$K_n = \frac{E\{q(t)n(t)\}}{E\{n^2(t)\}} \quad (4.16)$$

The assumption made simplifies the problem significantly, however, the justification of such assumptions in the application of the Σ - Δ modulation system is questionable. The assumption that the signal component and the noise component are uncorrelated at the input to the quantizer of the Σ - Δ modulator may not be correct. Especially, when the modulator is operating at the extreme ends of the input level scale of the modulator in the idle channel and overload regions. Furthermore, it is a known fact that the signal and noise component present at the input of the quantizer are indeed correlated to the input signal amplitude [Gra89, GCW89, HKB90].

Since the output of the single bit quantizer depends on the sign of its input, the approach to determine the quasi-linear gains representing the quantizer in Equations 4.13 and 4.14 requires an estimate of the probability density function of the signals present at the input and output of the quantizer. A closed form solution for the minimum mean squared quasi-linear gains for the quantizer shown above is difficult to obtain. Even if solutions were obtainable it would be only for special classes of input signal. The analytical solutions presented in [AP87] do not provide a ready to use solution as they only pertain to DC and sinusoidal inputs. It is clearly not applicable for our attempts to model the Σ - Δ modulator for a wide range of input signals. Such direct mathematical modeling presented above may sometimes be non-solvable or tractable. Furthermore, the efficiency of deriving a model by such means are questionable. Also, in most available treatments of the quantization noise model for the Σ - Δ modulator, the analysis presented is based on producing a similar long-term average behavior as the actual quantizer noise, for example, the same long-term sample distribution and power spectrum. This approach is not useful in trying to derive a simulation model where the actual short term nonlinear behavior of the system is to be represented accurately and efficiently. Such short term effects of the quantization noise could prove useful, especially during the simulation of transmission transients

and external noise injection into the received signal like impulse noise and crosstalk noise while simulating the DSL transceiver.

Based on the quasi-linear model for the quantizer element in the Σ - Δ modulator, the quantizer can be modeled as a linear structure shown in Figure 4.15. The Σ - Δ

Figure 4.15: Representation of the quantizer as a quasi-linear gain.

modulator can be viewed as two separate linear structures working in tandem, one corresponding to the input signal component in the signal path and the other relating to the quantization noise component in the noise path. In each path of the system, the quantizer stage replaced by a quasi-linear gain stage as illustrated in Figure 4.16. Separate transfer functions can be derived for these two paths with the quasi-linear gains playing an important role in the frequency responses in each of the respective systems. Now, the nonlinear system can be studied as two interlocking linear systems that is a function of its input signal. The system in Figure 4.16 can be represented as the simplified system in Figure 4.17 where the transfer functions $H_s(z)$ and $H_n(z)$ account for the transfer function for the signal and noise paths respectively. The equivalent transfer function for the signal is given by

$$H_s(z) = \frac{K_x H_i(z) H_f(z)}{1 + H_f(z)} \quad (4.17)$$

Figure 4.16: Quasi-linear model for the Σ - Δ modulation system.

Figure 4.17: Linearized model of the Σ - Δ modulator.

and for the noise is expressed as

$$H_n(z) = \frac{1}{1 + K_n H_f(z)} \quad (4.18)$$

The transfer function for the signal when expanded appears to be low-pass in nature while the transfer function for the noise is high-pass in characteristic. This high-pass nature of the noise transfer function is responsible for the noise shaping behavior of the structure at high frequencies.

4.4 Computer Simulation of the Σ - Δ modulator

Although the describing function technique may not seem plausible to be adopted directly for our intentions due to its complex mathematical and long term averaging type solutions, it nevertheless provides some valuable insights for a deeper understanding of the mechanics of the Σ - Δ modulation system, especially in explaining and verifying the nature of the Σ - Δ modulator and its different operating regions. In the following discussion, we shall try to ratify the feasibility of using the quasi-linear description for the Σ - Δ modulator. This is done by comparing the spectral properties of the quasi-linear representation of the modulator to the power spectrum of the modulator's output bit stream obtained from simulations of the modulator operating at the oversampled rate for different quasi-linear gains and different input signal amplitudes respectively.

An intuitive appreciation for the quasi-linear model for the quantizer element can be obtained by the following argument. The increasing input signal amplitude will produce a higher internal signal variance in the integrators. At some point the increasing input signal amplitude will cause the output of the integrators to exceed the threshold of $\pm\Delta$. When this happens, the Σ - Δ modulator can be said to be operating in the *overload* region. The signal amplitude at the input of the quantizer will be in excess of the quantizing levels, and when the input of the quantizer is quantized to the quantizing levels of either $\pm\Delta$, the quantizer can be seen as a gain stage having a value of less than unity. Conversely, when the input signal to the quantizer is less than the quantizing levels (in the case of the *idle* channel and *normal* region of operation), the quantization of quantizer's input signal to the quantizing levels of $\pm\Delta$ the quantizer can be seen as a gain of greater than unity. The values of these gains representing the quantizer as a gain stage will govern the pole and zero locations of the transfer function of the respective signal and noise paths and hence their frequency characteristics. The role of the quantizer as a gain stage is evident by comparing the spectrum of the input signal to the quantizer and that of

Figure 4.18: Power spectrum of simulated quantizer input signal and output bit stream (a sine wave input to the modulator with -6 dB input level).

the quantizer's output bit stream for a sinusoidal input signal to the Σ - Δ modulator, as shown in Figure 4.18. Furthermore, the quantizer seems to work as an element that modulates the in-band noise components to higher frequencies, aiding in the separation of the signal component and the quantization noise component.

We shall now analyze the effects of the input signal amplitude on the shaping of the signal and noise path spectra using the above arguments and looking at the quantizer as a gain element. The Σ - Δ modulation system to be investigated is the modulator shown in Figure 4.11. The structure can be decomposed into its respective signal and noise path models. Decomposing the original structure into its equivalent representations as depicted in Figure 4.12 and 4.13 and using z -domain methods, the signal path transfer function as a function of its quasi-linear gain K_x can be expressed as

$$H_s(z) = \frac{K_x \alpha_1 \beta_1 z^{-1}}{1 + (\alpha_2 \beta_1 - \beta_2 - 2)z^{-1} + (1 + \beta_2)z^{-2}} \quad (4.19)$$

and similarly, the noise path transfer function as a function of its quasi-linear gain

K_n can be expressed as

$$H_n(z) = \frac{1 - 2z^{-1} - z^{-2}}{1 + \{K_n\alpha_2\beta_1 - K_n\beta_2 - 2\} + (1 + K_n\beta_2)z^{-2}} \quad (4.20)$$

The parameters¹⁶ of the Σ - Δ modulation system (as shown in Figure 4.12) used for our analysis are $\alpha_1 = 0.42$, $\alpha_2 = 0.333$, $\beta_1 = -0.5$, and $\beta_2 = 0.333$ together with a quantizer step size of $\Delta = 1.8$. It is further assumed that the operating clock rate of the Σ - Δ modulator is $f_s = 10.24$ MHz with the baseband bandwidth of the converter limited to 40 kHz.

The signal and noise spectra for the modulator can be computed using Equation 4.19 and 4.20 by substituting $z = e^{j\omega T_s}$. We find that the quasi-linear gains in the transfer function do indeed influence the spectral characteristic of the signal and noise path transfer functions. As the input signal amplitude increases, one can conjecture that the gains K_x and K_n would decrease. As postulated, the signal path transfer function possesses a spectrum which is low-pass in characteristic, while the noise transfer path function exhibits the noise shaping process with a spectrum which is high-pass in nature. It is interesting to note from the transfer function of the signal path that for K_x gains larger than unity, the bandwidth of the signal path transfer function is extremely wide. However, for K_x gains less than unity, meaning that the structure is operating in its overload region (for large input signal amplitudes) the bandwidth of the signal path gets progressively narrower. The above observation is displayed in Figure 4.19. The noise path transfer function predicts that for K_n gains greater than unity high frequency noise shaping occurs providing very low-distortion to the baseband frequencies. But, as the input amplitude increases, the gain K_n would decrease, causing the noise spectra to be pushed further in-band as shown in Figure 4.20.

Following the preceding analysis, an examination of the behavior of the Σ - Δ oper-

¹⁶The chosen values of the Σ - Δ modulator's parameters correspond to that of an actual implementation of the oversampling A/D converter used for the U -interface transceiver provided by Mitel Semiconductor, Kanata, Ontario, Canada [Lab].

Figure 4.19: Calculated signal path power spectrum, $|H_s(e^{j\omega T_s})|^2$ for varying quasi-linear gain K_x .

Figure 4.20: Calculated noise path power spectrum, $|H_n(e^{j\omega T_s})|^2$ for varying quasi-linear gain K_n .

Figure 4.21: The signal-to-noise ratio plotted against the amplitude of a sinusoidal input for the structure shown in Figure 4.11.

ating in the three regions of operation was performed. This was executed by performing systems simulations of the $\Sigma\Delta$ modulator structure in the time domain which operate at the oversampled rate. The systems simulation performed is proceeded by the calculation of the power spectrum of the output bit stream of the $\Sigma\Delta$ modulator as a function of sinusoidal inputs of varying amplitude. The aim here is to try to relate the operation of the $\Sigma\Delta$ modulator (by looking at the spectral characteristic of the output bit stream of the modulator) to the behavior that can be predicted by the quasi-linear model of the modulator's signal path and noise path transfer characteristic.

The overall system signal-to-noise characteristic was first obtained to identify the three regions of operation of the device discussed earlier. The signal-to-noise ratio¹⁷ versus input level of the structure under study is shown in Figure 4.21.

The time domain simulation of the structure depicted in Figure 4.11 was executed driven by a 10 kHz input sinusoid of varying amplitude. The observations of the

¹⁷The signal-to-noise ratio characteristic is obtained by simulation of the system in Figure 4.11.

signals at various critical nodes of the modulator were analyzed. The spectral characteristic of the output bit stream of the modulator were computed using the *Discrete Fourier Transform* (DFT). Rationalization for the observations from simulation was attempted using the quasi-linear model for the quantizer. This was done to show that the quasi-linear method does in fact explain some aspects of the nonlinear behavior of the Σ - Δ modulation system. The emphasis of the simulations was to try to capture the behavior of the modulator in the three regions of operation of the Σ - Δ modulator. The simulations performed consisted of the Σ - Δ modulator with ideal¹⁸ and non-ideal¹⁹ integrator elements.

The simulation observations of the Σ - Δ modulator that uses ideal integrators are summarized in the following. In the idle channel operating region (for input signal levels below -100 dB), we observed a very strong *tone* component at frequencies in close proximity of half the sampling frequency. This tone component in the spectra represents the average output frequency peak occurring when there is insufficient randomization in the signals present within the modulator. This is indicative of a constant oscillatory behavior of the output bit stream or limit cycle²⁰. At the baseband frequencies, the spectrum of the output bit stream consists of small levels of random²¹ spectral components. The 10 kHz component of the input signal appears at the same level as the noise components within the baseband frequencies. The spectral characteristic of the output bit stream predominantly consisted of random noise components distributed throughout the entire band of frequencies. Note that the baseband noise levels appear to be increasing proportionally with the increasing the input signal level. This observation seem to confirm the heuristic argument of the

¹⁸Ideal integrators refer to integrators which output is unlimited.

¹⁹Non-ideal integrators refer to integrator whose output is limited to a specified level to try to simulate the saturations of the operational amplifiers used to built the physical integrators.

²⁰This observation may not be present in the physical (analog) implementation due to noise sources present that will disrupt the limit cycle.

²¹The random spectral components could be computational anomalies of the DFT due to the finite precision digital word length constraint.

Figure 4.22: Power spectrum of simulated output bit stream, input level -200 dB, for the modulator with ideal integrators.

constant nature of the signal-to-noise ratio characteristic in the idle channel region. Some examples of the spectrum of the output bit stream of the modulator operating in the idle channel region is presented in the following in Figure 4.22 through 4.24.

As the amplitude of the input signal increases towards the boundary between the idle channel and normal regions the output of the modulator starts to progressively exhibit the high frequency noise shaping characteristic typical of the $\Sigma\Delta$ modulator structure operating in its linear operating region. Once the input level crosses over into the normal mode of operation the 10 kHz component of the input sinusoid starts to appear in the spectrum of the modulator's bit stream. The component of the input sinusoid progressively becomes the dominant component at baseband frequencies as the input signal level increases from -80 dB. At the same time the noise shaping at higher frequencies becomes more and more evident.

When the modulator is operating as a high resolution A/D converter in its normal operating region, we find that as the input signal level increases the signal component in the output bit stream increases proportionally. The noise floor in the baseband

Figure 4.23: Power spectrum of simulated output bit stream, input level -150 dB, for the modulator with ideal integrators.

Figure 4.24: Power spectrum of simulated output bit stream, input level -100 dB, for the modulator with ideal integrators.

Figure 4.25: Power spectrum of simulated output bit stream, input level -80 dB, for the modulator with ideal integrators.

frequencies on the other hand, remains *unchanged* for the range of input signal in the normal region of operation until the modulator starts to saturate and enter its overload region. Examples of the spectrum of the output bit stream of the modulator operating in the normal region can be found in Figure 4.25 through 4.27

From the signal-to-noise ratio versus input amplitude function of the modulator, maximum signal-to-noise ratio was achieved when the input signal amplitude is in the vicinity of -6 dB, just before saturation of the $\Sigma\text{-}\Delta$ modulator structure sets in. Beyond this point, the structure begins losing its noise shaping ability at the higher frequencies and starts migrating the quantization noise from higher frequencies down to the the lower frequencies, moving the noise components in-band. An example of the preceding observation is shown in Figure 4.28. For input levels beyond 6 dB as shown in Figure 4.29, the component of the input sinusoid can no longer be distinguished from the random noise components at baseband frequencies. The signal component appears to have been filtered out by the structure. Noise seems to be the dominant component in the output bit stream of the $\Sigma\text{-}\Delta$ modulator. The above

Figure 4.26: Power spectrum of simulated output bit stream, input level -30 dB, for the modulator with ideal integrators.

Figure 4.27: Power spectrum of simulated output bit stream, input level -6 dB, for the modulator with ideal integrators.

Figure 4.28: Power spectrum of simulated output bit stream, input level -2 dB, for the modulator with ideal integrators.

Figure 4.29: Power spectrum of simulated output bit stream, input level +20 dB, for the modulator with ideal integrators.

Figure 4.30: Example input signal to modulator and input signal of quantizer, input level -6 dB, for the modulator with ideal integrators.

observation can be explained by looking at the time domain signal at the output signal of the second integrator or input to the quantizer. When the modulator is operating in its linear operating region, the output of the second integrator consists of the input signal component with the very high frequency quantization noise component (induced by the feedback loop of the Σ - Δ modulator) riding “piggyback” on it tracking the input signal as shown in Figure 4.30. As the input signal amplitude increases, the output levels of the integrators will increase proportionally. Furthermore, since ideal integrators are used for the simulation, the output of the integrators are allowed to grow to very large levels. But, the quantizing levels of the modulator and the feedback signal is only limited to $\pm\Delta$. As the output level of the integrator rises to try to track the increasing input signal, there will be a point when the output of the integrators together with the feedback signal loses its tracking ability of the input signal causing the structure to *saturate*. An example of this is shown in Figure 4.31. The integrators are not able to force their outputs to switch levels fast enough to follow the input signal more closely to accurately track the input signal. Eventually,

Figure 4.31: Example input signal to modulator and input signal of quantizer, input level +20 dB, for the modulator with ideal integrators.

the output of the second integrator or the input to the quantizer results in a large slow-varying-amplitude signal with the input signal appears to be “*beating*” on it. Quantizing this signal will produce a bit stream with very low frequency content as seen from spectrum of the output bit stream of the Σ - Δ modulator. The structure at this point experiences bit stream saturation where it erroneously “*assumes*” an input signal with a large low frequency content.

To gain further understanding of the physical implementation of the Σ - Δ modulator, the use of non-ideal integrators in the modulator are considered. A realistic saturation level which conforms to the power rails (0, +5V) of a typical CMOS device of 2.25 volts was chosen. The systems simulation observations of the non-ideal structure are summarized in the following. The modulator with non-ideal or clipped integrators behaves in a similar fashion as the modulator with ideal integrators for the idle channel and normal regions of operation. However, the modulator with non-ideal integrators depicts a different behavior as it is driven into its saturation region of operation. As the modulator is driven beyond the normal region of operation,

Figure 4.32: Power spectrum of simulated output bit stream, input level -3 dB, for the modulator with non-ideal integrators.

the integrators in the structure start to clip, introducing harmonic distortion to the signals within the structure as well as to the output bit stream of the $\Sigma\Delta$ modulator. This time, when the structure is driven into saturation the output level of the integrators are not allowed to exceed the saturation levels of the operational amplifiers used in the integrators. The frequency characteristic of the output bit stream of the simulated structure shows that as the input signal level grows larger and larger, the structure begins to lose its noise shaping characteristics at higher frequencies and odd harmonics of the input signal starts to appear with growing intensity at baseband frequencies. Eventually, the spectrum of the bit stream would just consist of the odd harmonics of the input signal with its fundamental component at the frequency of the input sinusoid. The preceding observation is shown in Figure 4.32 through 4.34. The rationalization of this phenomenon can be better explained by looking at the time domain signals of the modulator. It is understood that the output signal of the second integrator would typically consist of a component which is representative of the average value of the modulator input together with the quantization noise component. As

Figure 4.33: Power spectrum of simulated output bit stream, input level +6 dB, for the modulator with non-ideal integrators.

Figure 4.34: Power spectrum of simulated output bit stream, input level +30 dB, for the modulator with non-ideal integrators.

Figure 4.35: Example input signal to modulator and input signal of quantizer, input level +6dB, for the modulator with non-ideal integrators.

the input signal level gets progressively larger, the output of the non-ideal integrators are not allowed to grow to large levels and clipping of the integrator outputs sets in. This introduces harmonic distortion to the signal component within the modulator. Examples of the input signal of the quantizer when the modulator is operating in its overload region using non-ideal integrators are depicted in Figure 4.35 and 4.36. As the integrators try to track the input signal, and since its output is now limited, the output level of the integrators was observed to be clipped and switching at the same rate as the input signal, while it tries to maintain the signal content of the input within the modulator. Since the output levels of the integrators are clipped, the signal at the output of the second integrator will only be able to “represent” the frequency content of the input sinusoid. As a result a square wave looking signal is seen at the input of the quantizer, explaining the odd harmonics of the input sinusoid in the spectrum of the modulator’s bit stream.

A closer examination of the quantizer’s role in the modulator as a gain stage was confirmed by comparing the spectral bin corresponding to the input sinusoid’s

Figure 4.36: Example input signal to modulator and input signal of quantizer, input level +30 dB, for the modulator with non-ideal integrators.

frequency of the *Discrete Fourier Transform* computation of the input and output signals of the quantizer. The gain characteristics of the quantizer for a range of input signal amplitude and input signal frequencies are presented in Figure 4.37 to 4.39. The gain characteristic appears to be an increasing function of input signal amplitude for small input levels. At a certain point in the linear operating region of the modulator, the role of the quantizer then takes on a constant function of input signal amplitude. In this region of operation the modulator seems to obtain the highest degree of linearity. Suddenly as the input signal amplitude crosses the overload operating region threshold the gain characteristic of the quantizer drops drastically. It is also interesting to note from the graphs that the quantizer as a gain stage having a gain greater than unity doesn't exceed a large quantity. This could be attributed to the binary quantization and *limit cycle* process inherent within the modulator.

Figure 4.37: Quantization gain versus input amplitude characteristics of the quantizer for a range of input sinusoid frequencies (10 kHz – 100 kHz).

4.5 Practical Simulation Models of the Σ - Δ modulator

One method of incorporating the oversampled A/D structure into the systems level simulation of the ISDN *U*-interface transceiver environment would be to perform the complete structure simulation of converter at the oversampling rate. Due to the high oversampling rate DSL environment, this suggests that the resolution time step for the simulation of the converter would be very much smaller than that required to simulate the transceiver's architecture. As a result, a large portion of the execution time for the transceiver simulation will be dedicated to simulating the oversampling A/D converter which operates at typically several tenfolds the baud rate. This type of full blown simulation of the oversampling A/D converter, which may seem overwhelming, could be useful gauging the accuracy of simulation models developed. Using the knowledge of the operational behavior of the Σ - Δ modulator from the simulation results in the preceding section, we shall now discuss the practical issues of developing simulation

Figure 4.38: Quantization gain versus input amplitude (-100dB – 0 dB) characteristics of the quantizer for a range of input sinusoid frequencies (10 kHz – 100 kHz).

Figure 4.39: Quantization gain versus input amplitude (-30 dB – 0 dB) characteristics of the quantizer for a range of input sinusoid frequencies (10 kHz – 100 kHz).

models that could be used to predict the quantization process of the oversampling A/D converter²².

In the implementation of the ISDN *U*-interface transceiver, the most sensitive component of all the digital signal processing blocks to nonlinearities of the digital subscriber loop channel is the *echo canceller* block. Due to this, commonly the performance simulation of the analog interfaces for the ISDN *U*-interface transceiver is usually gauged by looking at the performance of the echo canceller. It may be beneficial to note the sensitivity of the echo canceller to the nonlinearities of the analog interface of the transceiver. The quantization noise of the oversampling analog-to-digital converter does have quite a significant effect on the *minimum mean squared error* (MMSE) convergence behavior of the echo canceller. The quantization noise effect on the MMSE convergence of the echo canceller can be seen from a simulation of an echo canceller with a oversampling A/D analog interface. A simulation of the 2B1Q transceiver's echo cancellation system was performed using a 33-tap baud-rate linear echo canceller operating in tandem with an oversampling A/D converter which consisted of a Σ - Δ modulator (shown in Figure 4.11) operating at an oversampling rate of 10.24 MHz followed by a 496-tap FIR digital decimation low-pass filter operating at 80 kHz for a trans-hybrid echo channel impulse response that spans 28 baud intervals. The impulse response of the trans-hybrid echo channel and the decimation low-pass is shown in Figure 4.40 and 4.41 respectively.

A comparison between the echo canceller's residual uncanceled echo convergence from a simulation with an the oversampling analog-to-digital converter and that with an ideal analog interface (Figure 4.42 and 4.43) reveals that the noise floor convergence of the echo canceller simulation with the oversampling analog-to-digital converter is approximately 35 dB higher than that of the ideal case analog interface. The

²²Unfortunately, due to time constraints, the development of the quasi-linear model of the Σ - Δ modulator's quantization process presented in the previous section could not be carried out. However, a conjecture of how a quasi-linear model for the simulation model of the Σ - Δ modulator is presented in Chapter 5.

Figure 4.40: Impulse response of trans-hybrid echo channel used for simulation.

Figure 4.41: Impulse response of FIR digital decimation low-pass filter used for simulation.

Figure 4.42: Simulation results of the residual uncanceled echo of an echo canceller with an ideal analog interface.

2B1Q transceiver echo canceller simulation with an oversampling analog-to-digital converter front-end operating at the oversampling rate as described previously was used as a gauge for the accuracy of the developed simulation models representing the oversampling analog-to-digital converter quantization noise.

4.5.1 Simple Additive White Noise Model

A simple simulation model could be derived by inducing a constant additive noise source which is input signal independent representing the maximum quantization noise error which is typically equal to half the quantization interval (2Δ). So, in the general case, we can simply say that the quantization noise is bounded in the interval $-\Delta < n(t) < \Delta$. Assuming that the quantization noise error is randomly distributed between these two limits and having a probability density function which is uniform between the interval. The maximum quantization noise power would be

Figure 4.43: Simulation results of the residual uncanceled echo of an echo canceller with an oversampling analog-to-digital converter.

$\sigma_n^2 = \frac{\Delta^2}{3}$. Clearly, this simulation model for the quantization noise would not be representative of the actual quantization noise produced by the oversampling analog-to-digital converter in all three regions of operation of the Σ - Δ modulator. Such a model, ideally, may be used for simulating the quantization noise when the Σ - Δ modulator is operating in its normal region where the in-band noise is pretty well constant in that region.

4.5.2 Varying Additive White Noise Power Model

A simulation model for the quantization noise that is dependent on the amplitude of the input signal could be derived through the characterization of the signal-to-noise ratio versus input amplitude function of the oversampling analog-to-digital converter. The signal-to-noise ratio versus input amplitude characteristic of the converter was obtained through computer simulation.

Figure 4.44: Simulation of echo canceller with oversampling analog-to-digital converter analog interface.

One method of acquiring the signal-to-noise versus input amplitude characteristic of the converter is through (Figure 4.44) the simulation of a 2B1Q fixed length finite word length echo canceller simulation with an oversampling analog-to-digital converter front end operating at the oversampling rate similar to that of the simulation used to show the sensitivity of the echo canceller to the quantization effects of the oversampling A/D converter for a range of input signals. In this approach, the signal-to-noise ratio considerations was done by identifying the residual uncanceled echo power as the quantization noise power²³ and the signal²⁴ power was computed from the output level of the of the decimation filter following the Σ - Δ modulator. The signal-to-noise could equivalently be obtained from Σ - Δ modulator simulations with sinusoidal inputs for different input amplitudes. For the sinusoidal input, the signal-to-noise ratio versus input amplitude characterization was performed by looking at the discrete fourier transform of the output bit stream of the Σ - Δ modulator where the signal component is identified as the component of the DFT computation in the frequency bin corresponding to the frequency of the input sinusoid, whereas

²³It is recognized that this noise consists of the residual uncanceled echo due to the fixed length and finite word length of the echo canceller. The noise component that is present is the in-band noise not filtered by the decimation filter.

²⁴The signal component consist of the input signal component and the filtered quantization noise component from the decimation filter.

the noise components were identified as the components of the DFT computation in the frequency bins within the baseband frequencies of 40 kHz other than that corresponding to the input. The signal-to-noise ratio versus input amplitude function of the converter obtained is very similar to that shown in Figure 4.21 for both methods mentioned in the above. A computer simulation model for the quantization noise of the converter can be derived from a polynomial curve fit of the collected signal-to-noise versus input amplitude data obtained through computer simulation. The curve fit of the data is used to produce a noise function which is used to vary the variance of an additive white noise source accordingly to the input signal levels of the converter.

The simulation model relied heavily on the signal-to-noise ratio versus input amplitude characteristic of the simulated device. The simulation model consisted of the quantization noise being simulated by an *additive white gaussian noise*²⁵ (AWGN) source whose variance is controlled by a variable gain stage which was derived from the signal-to-noise characteristic of the device. The gain function used to provide the gain to vary the noise variance was obtained from the polynomial curve fit of the signal-to-noise ratio versus input signal level characteristic of the converter. Sensing of the input signal amplitude of the model was performed at baud rate together with the noise variance update. A block diagram of the simulation model derived is presented in Figure 4.45. Verification of the model was done by including the quantization noise model into an echo canceller simulation with the input dependent noise injected at every baud instant. The quantization noise simulation model excluded the influence of the decimation filter of the oversampling analog-to-digital converter. The incorporation of the decimation filter impulse response of the oversampling analog-to-digital converter was through the simulated channel impulse response used to drive the simulation²⁶. The input waveform that was used in the simulation of the model

²⁵The injected noise spectrum was not noise shaped because the simulation model is intended to operate at the baud rate and not the oversampling rate. The emphasis of the noise model was the dependence of the quantization noise variance on the input signal amplitude.

²⁶This is assuming that the quantization process in the converter is modelled as a linear additive

Figure 4.45: Quantization noise simulation model.

was the response to the transmitted signal of the measured echo signal convolved with the impulse response of the decimation filter. The convergence characteristics of the residual uncanceled echo noise for a given input amplitude from the simulation of the model was compared to that of the full simulation of the echo canceller with the oversampling analog-to-digital converter operating at the oversampling rate.

The results from the simulation of the echo canceller with the quantization noise simulation model (Figure 4.45), showed that for input signal amplitudes near the high end of the normal operating region, the uncanceled echo noise floor convergence obtained from the model seems to behave in a similar fashion as that of the actual echo canceller with the oversampling analog-to-digital converter simulation. The approximate range of validity of such a model was restricted to the input signal amplitude range of -40 dB to -6 dB where the converter is operating in the linear region of operation of its Σ - Δ modulator. The simulation model, however, fails to show a similar noise floor convergence behavior for different input levels especially when the input levels are very small or when the oversampling analog-to-digital converter structure is driven into saturation. In these regions of operation, the minimum mean squared error convergence of the echo canceller simulation with the quantization noise model seems to be at a much lower level than that of the full simulation of the echo impairment.

Figure 4.46: Simulation of echo canceller with quantization noise model.

canceller and oversampling analog-to-digital converter, the difference of the minimum mean squared error between the two types of simulations was typically about 35 dB. The extrapolated noise function obtained from the signal-to-noise versus input signal amplitude function of the device was not able to provide the noise power that was sufficient to mimic the quantization noise process of the converter's Σ - Δ modulator.

From the results obtained thus far, it is suspected that the baud rate noise simulation model described above accurately represents the dynamics of quantization noise in the real structure operating at the oversampling rate over only a limited range of input amplitudes, primarily in the linear operating region of the converter's Σ - Δ modulator. As a consequence, an attempt to have the oversampling analog-to-digital converter model operate at a higher rate²⁷ and the inclusion of the decimation filter was made in the attempts to obtain a more accurate model. Instead of operating at the baud rate of T , a faster operating rate of $\frac{T}{16}$ was chosen for the noise simulation model. The tap spacing of the decimation filter was increased to $\frac{T}{16}$ instead of $\frac{T}{128}$ (the original oversampling rate of the converter). The coefficients of the decimation filter had to be increased by a factor of 16 to ensure that the overall gain response of the decimated decimation filter is identical to that of the original decimation filter. A block diagram of the simulation noise model operating at the $\frac{T}{16}$ is shown in

²⁷It is recognized that such a model is less computationally efficient than one which operates at the baud rate.

Figure 4.47: $\frac{T}{16}$ quantization simulation model.

Figure 4.47. The injection of the noise for the model should now correspond to the quantization noise introduced solely by the Σ - Δ modulator and the channel impulse response used for the echo canceller simulation. The function for the variable gain for the noise was derived from the signal-to-noise ratio versus input signal amplitude curves obtained from the simulation of the Σ - Δ modulator with the sinusoidal inputs of different amplitudes.

Verification of the modified noise simulation model was again performed by comparing the convergence behavior of the residual echo noise from the simulation of the model with that of the echo canceller and oversampling analog-to-digital converter. The simulation results obtained indicate the same problems as that of from the baud rate noise simulation model where the modified simulation model was able to model the actual quantization noise of the oversampling analog-to-digital converter at the high input amplitude end of the normal region of operation of the Σ - Δ modulator but fails to accurately represent the Σ - Δ modulator's quantization noise in both the idle channel and overload region. Again, the approximate range of validity of such a model was restricted to the input signal amplitude range of -40 dB to -6 dB where the converter is operating in the linear region of operation of its Σ - Δ modulator similar to that of the baud rate model. Painstaking fine tuning of the gain function that governs the noise variance was required to actually make the noise levels of the model conform to that of the actual oversampling analog-to-digital converter noise for any given input level.

From the simulation results of the simulation models presented, it appears that for the varying gain noise model to be useful, full characterization of the structure for each range of input amplitude to the structure will have to be performed. No advantage could be gained by running the quantization noise model higher than the baud rate. This could be due to the linear additive assumption of quantization noise process of the converter. Furthermore, the fully linear model does not reflect the behavior and stability of the highly nonlinear element in the actual structure when it is driven into saturation. As a result, we would require prior knowledge of the input levels to the model, and fine tuning the parameters of the model to the specific regions of operation of the oversampling analog-to-digital converter for each input level is necessary for such an approach to be used.

Chapter 5

System Simulation of a 2B1Q U-Interface Transceiver

For completeness, we shall discuss the issues of performing a complete systems simulation of a typical 2B1Q *U*-interface transceiver's for digital signal processing blocks¹. The discussion of the simulation system presented here is only for illustrative purposes, to show how the reported work in Chapters 3 and 4 could be used in a simulation environment.

The simulation of such a system can be used in analyzing the optimal performance, in the *minimum mean squared error*² (MMSE) sense, of the digital signal processing elements of such a transceiver. It can be used to answer questions that naturally surface during the design phase of such a system. For example, one may wish to investigate, how many taps is required by the echo canceller and decision

¹The architecture of the transmission system adopted for our purpose is based on the reported work in [ACCC87, CGH⁺89]. An existing simulation program of the digital signal processing elements of an *U*-interface transceiver for ISDN *basic access* obtained from Mitel Corporation [Lab] was modified to include an oversampling A/D converter as the analog-to-digital interface of the transceiver.

²The MMSE criterion is widely used in practice because of its simplicity and the existence of simple adaptive filtering algorithms which converge to the MMSE solution.

feedback equalizer (within the economical reach of current technology) to meet a certain criterion, or what would the system performance be for a different subscriber loop constitution or if a certain block on the transceiver or line interface circuit were modified or optimized.

5.1 Overview of the 2B1Q *U*-Interface Transceiver Simulation System

Figure 5.1 shows a block diagram of the digital signal processing elements of the transceiver and the transmission system [Lab]. The digital signal processing architecture of the transceiver includes the use of decision feedback equalization, and linear, jitter-compensated and nonlinear echo cancellation. The echo canceller and decision feedback equalizer are composed of finite precision (fixed word length), finite-length tapped-delay-line filters which are assumed to be jointly adapting and have a tap spacing equal to the symbol period. The zero-redundancy 4-level 2B1Q line code is used. The simulated transmission environment includes trans-hybrid echo, and intersymbol interference (ISI).

The 160 *kilo-bit-per-second* (kbit/s) line bit stream is first scrambled and then encoded into a 4-level, 80 *kilo-baud* (kbaud) signal before transmission via DSL channel consisting of a digital-to-analog (D/A) converter, low pass filter, line driver, hybrid coupler and line interface as previously described in Chapter 3. The nonlinearities of the D/A converter is simulated simply by mapping the four 2B1Q transmit-levels to their respective nonlinear transmit-levels. The DSL channel is simulated using the trans-hybrid line and echo pulse responses of the loop plant under study. On the receive side, after the DSL channel, the analog line signal is encoded into a 10.24 MHz bit stream by a noise shaping Σ - Δ modulator followed by a digital decimation filter which constitutes the oversampling analog-to-digital (A/D) converter. The decimation filter is used to remove the out-of-band noise introduced through course

Figure 5.1: Block diagram of 2B1Q *U*-interface transceiver.

quantization in the Σ - Δ modulator and downsamples the bit stream to produce an 80 *kilo-sample-per-second* (ksample/s) 20-bit representation output of the input to the A/D interface. The particular instant at which the samples are produced is controlled by a timing estimation (recovery) circuit which uses the samples to generate a timing function after echo and intersymbol interference have been removed by an echo canceller (EC) and a decision feedback equalizer (DFE) respectively. A 4-level quantizer follows to recover the data symbols for decoding.

5.1.1 Scrambler polynomials

At the network termination (NT) or local exchange end of the DSL the scrambler polynomials is $1 + x^{-5} + x^{-23}$ [Ame88]. At the line termination (LT) or subscriber's end the polynomial is $1 + x^{-18} + x^{-23}$ [Ame88]. These scramblers provide low intersymbol

correlation and between the two directions of data transmission to prevent errors in the adaptive echo canceller and DFE blocks, and a very low probability of adverse sequences causing false operation of timing extraction circuits [ACCC87].

5.1.2 Echo Canceller

The baud-rate linear adaptive transversal filter echo canceller is used to cancel the trans-hybrid echo signal. A 33-tap linear echo canceller is chosen, as the nonidealities of the DSL channel have significant effect on the echo response “tail”, as reported in [ACCC87]. Adaptation for the echo canceller is by the clipped *least mean squared* (LMS) algorithm [ACCC87].

The performance of the echo canceller can be further degraded by nonlinearity [AHM82b] and timing jitter [Fal85]. To circumvent the nonlinearity and timing jitter problem, the system incorporates adaptive compensators which consist of a jitter compensated echo canceller and a nonlinear echo canceller based on transpose distributed arithmetic. The algorithm employed in these compensators are described in detail in references [Cox85, CCA85] for the *jitter compensated* (JC) echo canceller and [CSA85, SCA88, CA84, Bur77] for the *nonlinear echo canceller* (NEC). Only a limited number of the echo canceller taps require the compensation algorithms due to the rapidly decaying nature of echo response and its derivative [ACCC87].

5.1.3 Decision Feedback Equalizer

The ISI introduced by the memory of the DSL channel is removed from the received signal by the *decision feedback equalizer* (DFE) [Pro83]. Adaptation of the coefficients of the DFE is also by the clipped LMS algorithm as in the case of the echo canceller [ACCC87].

5.1.4 Timing Estimator

A channel estimation type timing adaptation scheme [ACCC87, ACG84, MM76] used is based on the timing function

$$f(t) = h_0 - ph_{-1}$$

where h_0 and h_{-1} are the samples of the pulse response close to the pulse peak and the one baud precursor before the peak respectively, and p is a positive constant chosen to give a tolerable value of the ratio between the pulse peak and the precursor. The optimal sampling instant given by the timing function is one baud period after a predetermined value of the estimated precursor.

5.1.5 Digital Decimation Filter

The digital decimation filter implements a linear-phase *finite impulse response* (FIR) filter which removes the out-of-band quantization noise and downsamples the output of the Σ - Δ modulator to the line symbol rate of 80 kHz.

Besides, its primary functions of band limiting and downsampling, the decimation filter is also used for performing in-band spectral shaping, and a $(1 - z^{-1})$ fixed equalization. Figure 5.2 shows the frequency response of the basic filter. The filter calculates

$$Y_n = \sum_{i=0}^{495} x_{n-i} f_i$$

where x_k is the current bit output from the Σ - Δ modulator and f_i is the i th coefficient of the FIR filter.

5.2 Example Simulation Result

In this section, an example of the *mean squared error* (MSE) performance analysis of the transceiver system described in the previous section is presented. The simulation consists of a local transceiver which transmits as well as receives data from a

Figure 5.2: Decimation filter frequency response [Lab].

remote transmitter. Thus, at the receiver of the local transceiver there is an echo signal and a foreign signal present.

The simulation of the transceiver is executed in several phases. In the *first* phase of the simulation the local transmitter is turned on (with no transmission from the remote transmitter), transmitting at 4-levels. In this phase, the jitter compensated and linear echo canceller is trained to learn the impulse response of the echo channel. After the jitter compensated and linear echo canceller have adapted their tap coefficients to the trans-hybrid echo channel, the *second* phase is started where the nonlinear echo canceller is activated to cancel the nonlinearities introduced by the D/A converter and line drivers. During the training of the echo canceller the local transceiver's DFE is inactive and the step size of the clipped LMS algorithm during the training of the echo canceller is the same for first and second phases. Next, the *third* phase of the simulation is executed, whereby the local transmitter is turned off together with the echo canceller adaptation, and the remote transmitter starts transmitting at 2 levels. Now, we introduce a foreign signal at the input of the receiver allowing the DFE of the local transceiver to learn the memory of the transmission channel to cancel the ISI.

Figure 5.3: Pulse response of the line.

In this phase, the DFE is adapting its tap coefficients with a large step size to a two-level received symbol. The *fourth* phase of the simulation follows by the remote transmitter transmitting at 4 levels and the local DFE is adapting using a smaller step size than that in phase three. In the final phase of the simulation, *fifth* phase, both transmitters at both ends are turned on transmitting at 4 levels with the all adaptive signal processing blocks of the local transceiver operating simultaneously. The simulation of the transceiver was executed for a total of 8000 baud intervals. Phase one of the simulation was executed from baud intervals 1 through 9999, phase two was executed from baud intervals 1000 through 2499, phase three was executed from baud intervals 2500 through 4499, phase four was executed from baud intervals 4500 and 6499, and phase five was executed between baud intervals 6500 and 8000. The different operating phases of the transceiver are summarized in Table 5.1. The pulse response of the line trans-hybrid echo channels are depicted in Figure 5.3 and 5.4 respectively which are generated from the line and echo modelling program. Two simulations of the transceiver were performed, in one an oversampling A/D was used as the analog-to-digital interface of the transceiver while in the other an ideal

Figure 5.4: Pulse response of the trans-hybrid echo.

analog-to-digital interface was used. A comparison of the MSE convergence behavior of the two simulations mention above is given in Figure 5.5 shows that the simulation with the oversampling A/D converter as the analog-to-digital interface does have dramatic effects on the overall performance of the adaptive signal processing elements of the transceiver. The example shown includes the full algorithmic time domain representation of the oversampling A/D converter. Models such as that developed in the thesis will be more computationally efficient to simulate (faster execution) and should lead to similar results as well. Such a simulation may be performed prior to the actual hardware design and implementation of the transceiver. The signal processing architecture can be accurately verified and its performance estimated.

Figure 5.5: A comparison of the MSE convergence behavior of the transceiver simulation with oversampling A/D and that with ideal analog-to-digital interface.

operating phase	baud interval	transceiver operation
phase 1	1-9999	NT transmitter ON: 4-level symbol LT transmitter OFF Training EC + JC: slow adaptation NEC & DFE: INACTIVE
phase 2	1000-2499	NT transmitter ON: 4-level symbol LT transmitter OFF EC & JC adapting: slow adaptation Training NEC: slow adaptation DFE: INACTIVE
phase 3	2500-4499	NT transmitter OFF LT transmitter ON: 2-level symbol EC, JC & NEC: INACTIVE Training DFE: fast adaptation
phase 4	4500-6499	NT transmitter OFF LT transmitter ON: 4-level symbol EC, JC & NEC: INACTIVE Training DFE: slow adaptation
phase 5	6500-8000	NT transmitter ON: 4-level symbol LT transmitter ON: 4-level symbol EC, JC & NEC: slow adaptation DFE: slow adaptation

Table 5.1: Transceiver operating phases.

Chapter 6

Conclusions and Recommendations

6.1 Conclusions and Summary

The increasing demand for *high-rate* digital transmission services over subscriber loops has spawned-off new research efforts to achieve extremely high bandwidth transmission over twisted-pair copper media. This would imply the need for powerful signal processing strategies to be employed in a transceiver operating in such a medium to execute the complex signal transmission and detection of the signals. In designing such a transceiver, one will have to combine both systems and hardware optimization for the competitive implementations of such systems. To achieve optimal and efficient design of such transceivers a flexible and dynamic simulation tool for the verification and feasibility analysis for the system design of the transceiver is a necessity. The simulation of systems for the feasibility analysis has become a common application of the digital computer. Such studies of complex systems through simulation techniques has many merits. The simulation approach permits the evaluation of operating performance prior to the implementation of a system; it permits the comparison various implementation alternatives without actually having a working system hardware. The

short turn-around time to gauge a system through simulation allows for the timely policy decision to be easily made. Furthermore, simulation tools can be used by many people because of its readily comprehended structure and the availability of today's powerful digital computers. Once the simulation model is built, it can be used repeatedly to analyze new designs. It is usually the case that simulation data is much less costly to obtain than similar data from the real system. With simulation models, the data generated can be used to estimate any conceivable performance measure.

However, the results obtained from simulation should be interpreted with care, simulation can be easily misused, and simulation results taken with more confidence than is justified. It should not be seen as replacing the operations of the actual system. Simulation techniques cannot guarantee the exact performance of the real-life system. The accuracy of simulation results will depend on the verification and validity of the models used, proper collection and analysis of the data obtained, the choice of analytical methods, and the appropriate design of simulation experiments. As a result the development of the simulation models may be costly requiring large expenditures of time in their construction and validation. Simulation can only provide the answer to whether an idea is viable for implementation before the hardware for the system is constructed.

In view of the discussion above, the objective of this thesis has been to develop a simulation environment which provides a simulation model for the digital subscriber loop line interface for the optimization and performance analysis of the subscriber loop transceiver architecture. An efficient systems level simulation environment for the investigation for transceiver architecture optimization and algorithms is proposed.

In Chapter 2, an overview of the conditions in which a transceiver operating in the Digital Subscriber Loop channel were presented. The non-idealities, impairments of the channel, and noise sources indigenous to the channel were described together with the different possible transmission methods employed to achieve full duplex transmission over the twisted copper pair are presented for the reader to gain an

appreciation of the complexity of the system.

Following the introduction to the channel conditions of the digital subscriber loop, Chapter 3 described the methodology of obtaining an easily reconfigurable model for end-to-end loop channel and the trans-hybrid echo channel of the subscriber loop channel. It is common practice to use measured pulse responses of the line interface and trans-hybrid echo channels to drive a systems level simulation of the transceiver to obtain performance measure of the various digital signal processing block and study the interaction between each block. The process for obtaining the measured pulse responses is a cumbersome and difficult task, especially when there are several possible types loop configuration defined by the ANSI standards. These defined loops take into account only the major percentage of the actual population of the loop plant. Instead of using actual measured pulse responses of the line interface, attempts to model the trans-hybrid channel and transmission line through analytical means as described in the chapter. The impulse responses for the loop and trans-hybrid channels was computed from the derived models. By the method used, the impulse responses of the line and echo pulse responses for any loop configuration of the subscriber loop is obtainable. The computed pulse responses from the models develop show a close correspondence with the pulse responses obtained from measurements.

The natural progression in the attempts to model the line interface circuit of a digital subscriber loop transceiver would be to characterize the analog-to-digital interface of the transceiver which is the topic of discussion of Chapter 4.

An oversampling analog-to-digital converter type of architecture was considered for the modeling exercise. The characterization of the quantization noise in an oversampling analog-to-digital converter based on $\Sigma\Delta$ modulation is attempted. An overview of the $\Sigma\Delta$ modulation used in the oversampling analog-to-digital converter is presented together with a discussion of the performance characteristic of the $\Sigma\Delta$ modulator. A comparison of the different possible approaches for a model development is outlined.

From the different approaches discussed, the quasi-linear gain approach using describing functions from nonlinear control systems theory to model the quantizer in the Σ - Δ modulator seems to be the most viable technique for describing the nonlinear behavior of the structure. Unfortunately, the method of describing function cannot be employed directly for the derivation of the simulation model we are seeking because the technique requires long term averaging computation to obtain a description for the nonlinear behavior of the system. Nevertheless, the quasi-linear gain paradigm of looking at the nonlinearity appears to be an appropriate method to describe the nonlinear behavior of the system under study.

Subsequently, attempts to investigate the expediency of adopting a variation of the quasi-linear gain approach to characterize the quantization noise behavior of the Σ - Δ modulator was initiated. The analysis proceeded with the z -domain description of the system. Transfer functions for the signal and noise path as prescribed by the quasi-linear model were obtained. The derived signal and noise transfer functions which are functions of input signal level were analyzed by computing their respective spectra. The characteristic of the signal and noise transfer functions for varying gains corresponding to the different operating regions of the Σ - Δ modulator were noted. The analysis results obtained from the quasi-linear gain description of the modulator's nonlinearity was compared to the systems level simulation of actual Σ - Δ modulator.

The outcome of the simulations indicate that the description of the Σ - Δ modulation system decomposed into its signal and noise paths with the quasi-linear gain representation of the quantizer does in fact closely portray the the behavior of the nonlinear system for the most of the different operating regions of the modulator. An examination of the quantizer's role as a gain element was verified by inducing a sinusoidal signal of a known frequency into the modulator's and looking at the spectral frequency bin corresponding to the input signal frequency at the spectrum of the input and output of the quantizer. The behavior of the quantizer as a gain element as a function of input signal amplitude was found to be a function which

is constant for most part of the normal operating region of the modulator and is a decreasing function of input signal amplitude as we digress further away from the normal operating region. The gain characteristic appears to be an increasing function of input amplitude in the idle channel operating region and a decreasing function of input amplitude when the modulator is saturated by the input signal in the overload operating region.

From analysis of the simulation results and the theoretical understanding achieved through the quasi-linear gain view of the quantizer a proposal for a simulation model for the quantization noise of the Σ - Δ modulation system is presented. Unfortunately, due to time constraints of the thesis, verification of the proposed model was not possible. However, the ground work for a more accurate model obtained using both theoretical analysis and measurement based characterization of the quantization noise was laid. A discussion on practical simulation models for the oversampling A/D quantization noise is also presented.

Lastly, the issues of creating an overall systems simulation of a transceiver operating in the ISDN *U*-interface basic access was discussed. An example simulation of a transceiver with all its signal processing element working in tandem was presented. The simulation results indicated that the quantization noise in the oversampling A/D converter does adversely influence the overall performance of the transceiver system. As a result, an accurate representation of the quantization noise in the converter which is computationally efficient is of importance in building a fast and efficient simulation environment.

6.2 Recommendations for Future Work

For a more complete model of the Digital Subscriber Loop channel, the inclusion model of the other impairments of the channel, namely, the crosstalk noise and impulsive noise can be included into the DSL channel simulation environment.

Verification of the proposed quantization noise model for the oversampling analog-to-digital converter. A more realistic model of the quantization noise which accounts for the harmonic distortion introduced due to the clipping of the integrators when the modulator is driven into its overload operating region would provide a model which is closer to actual implementation of the converter.

6.2.1 Proposed Quasi-Linear Quantization Noise Model

The intent for the development of the following proposal is to obtain a simulation model which reflects the quantization noise characteristics in a Σ - Δ modulator by a model that is derived through a combination of the theoretical understanding and a measurement based characterization approaches of the system.

The simulation results from Section 4.4 of Chapter 4 indicate that the nonlinearity in the Σ - Δ modulation system may be suitably seen as a quasi-linear gain stage which is a function of the input signal amplitude to the modulator. From the observations obtained, we find that the quantizer as a gain element simply acts as a gain stage inhibiting the passage of the input signal when the modulator enters its overload region. And, for the noise it determines the noise shaping of the Σ - Δ modulator.

For the quasi-linear model the quantizer has been modeled as a structure shown in Figure 4.15. In multilevel quantization it is typical to model the the quantizer element simply as a unity gain stage. However, in order to model the noise at the output of a one-bit quantizer, it is more appropriate to include the gain influence attributed to the quantizer. One can rationalize that since the output of the modulator is always limited to the levels $\pm\Delta$ regardless of the input signal power, the output power of the modulator is fixed. It is shared between the signal component and the quantization noise component continually. We may therefore, assume that the output of the modulator is representative the output of two interlocking system of Figure 4.16. In one system, the input forcing function is the input signal $x(t)$. In the other system, the forcing function is an additive noise source $n(t)$ produced by the

quantization process.

At the baseband frequencies, the signal path contribution to the power of the signal component in the bit stream output may be approximated by the quasi-linear gains as a function of input amplitudes for the signal component in the bit stream as obtained from the simulation results in Figure 4.37. We may therefore assume power of the input signal content within the modulator's bit stream is

$$\sigma_s^2 = K_{x(t)}^2 \sigma_{x(t)}^2 \quad (6.1)$$

where $K_{x(t)}$ is the gain function of the quantizer for the signal component which is dependent on the input signal amplitude and $\sigma_{x(t)}^2$ is the modulator's input signal power.

The noise path contribution to the quantization noise power in the modulator's bit stream may be approximated by computing the noise path power spectrum obtained from the transfer function expressed in Equation 4.18. The noise power spectrum may be expressed as

$$\sigma_n^2 = |N(z)|^2 |H_n(z)|^2 \quad (6.2)$$

where $|N(z)|^2$ is the noise forcing function power for the noise path and $H_n(z)$ is the noise path transfer function. To simplify the computation, we shall assume that the noise forcing function $n(t)$ in the noise path having the following properties:

- The quantization noise is uniformly distributed over the range $-\Delta < n(t) \leq +\Delta$.
- $n(t)$ is a stationary white noise process.
- $n(t)$ is uncorrelated with the input signal of the quantizer.

From the assumptions above the noise injected by the single bit coder which represents the driving function for the noise path can be seen to have a quantizing step size of 2Δ with a variance of $\sigma_{N(t)}^2 = \frac{\Delta^2}{3}$. Using the simplifying assumptions, the noise path

power spectrum as a function of its quasi-linear gain K_n can be expressed in terms of angular frequency, ω as

$$\sigma_n^2(K_n) = \frac{\sigma_{N(t)}^2}{2\pi} \int_0^{\frac{\omega_A}{2}} \frac{1}{1 - K_n[H_f(\omega) + H_f^*(\omega)] + K_n^2|H_f(\omega)|^2} d\omega \quad (6.3)$$

Since the power of the output bit stream of the Σ - Δ modulator is constant and equal to Δ^2 , it follows that

$$K_{x(t)}^2 \sigma_{x(t)}^2 + \sigma_n^2(K_n) = \Delta^2 \quad (6.4)$$

The value of K_n can be found uniquely by solving Equation 6.4. The value of K_n and hence the noise shaping will depend on the input amplitude of the modulator.

The proposed simulation model will consist of an additive noise source which is a function of input signal amplitude. The variance of the additive noise source will be a function of the input signal dependent gain K_n . This noise source of the simulation model will have a Gaussian¹ probability distribution. The signal path in the simulation model is controlled by the input signal dependent gain K_x . A block diagram of the proposed Σ - Δ modulation quantization noise model is shown in Figure 6.1.

¹This assumption is adopted since the feedback quantization noise for higher order modulators are typically double- or triple-integrated before the quantizer input. The integration of a random variable tends to make its distribution approach a Gaussian distribution. Such assumptions are commonly made for the describing function analysis of nonlinear feedback systems which involve integration [GV68]. Justification of the Gaussian distribution assumption for the noise component present at the input of the quantizer can be found in [AP87].

Figure 6.1: Proposed simulation model for the $\Sigma\text{-}\Delta$ modulator.

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Appendix A

Program Segment for DSL Loop Constitution Definition

The following is an example program segment which defines the DSL loop constitution shown in Figure A.1 for the computation of the line and echo pulse responses in the DSL channel modelling program.

Figure A.1: Example DSL loop configuration.

Program segment defining sampling rate and number of impulse response points:

```
sampling_rate = 10.24e6; /* Hz */  
number_of_samples = 8192;
```

Program segment defining the example DSL loop constitution above:

```
/* Computation of ABCD parameters */  
  
/* trans-hybrid receive channel */  
ABCD = hybrid_loop_to_rx (xifreq);  
/* xifreq = frequency bin */  
  
/* section of line of 1500 ft, 24 AWG */  
ABCD = line (xifreq,1500,gamma24,Z24) * ABCD ;
```

```

/* section of an open-ended bridged tap
   of length 500 ft, 26 AWG */
ABCD = bt (xifreq,500,gamma26,Z26) * ABCD ;

/* section of line of 500 ft, 24 AWG */
ABCD = line (xifreq,500,gamma24,Z24) * ABCD ;

/* trans-hybrid transmit channel */
ABCD = hybrid_tx_to_loop (xifreq) * ABCD ;

/* ABCD parameters of equivalent DSL transmission channel */
/* for frequency bin xifreq */
a = ABCD [1,1];
b = ABCD [1,2];
c = ABCD [2,1];
d = ABCD [2,2];

```

END

1|2|0|4|9|1

FIN