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**A 1-Bit Superconductive Phase Shifter in Coplanar Waveguide at
Ka-band**

Walter Mycroft

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment
of the requirements for the degree of

Master of Electrical Engineering

**Ottawa-Carleton Institute of Electrical Engineering
Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada**

Jan 1999

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acceptance of the thesis,

**A 1-Bit Superconductive Phase Shifter in Coplanar Waveguide at
Ka-band**

submitted by

Walter A. Mycroft, B. Eng.

in partial fulfillment of the requirements for the degree of

Master of Electrical Engineering

Thesis Supervisor

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January 1999

Abstract

The maturation of high temperature superconductor technology has seen high temperature superconductors used in communication systems. The use of superconductors has mostly been limited to filters in cellular phone systems or satellite ground stations. The cooling systems for high temperature superconductors have also been developed, providing reliable operation. With cooling already included in a communications system, other superconductive components may be included.

One area that could benefit from the use of superconductors is phase shifters. Losses in most conventional phase shifters are approximately 2-3 dB per bit. Superconductors offer the possibility of reducing the losses in phase shifters due to their low loss properties. In addition the superconducting-normal phase transition can be used to make a switching element. A fully integrated phase shifter design would be possible. The fully integrated phase shifter would eliminate integration problems with the switching elements and the phase shifting networks.

This thesis presents the design and performance of a 180° bit superconductive phase shifter at Ka-band. The ability of such a circuit to function, providing the necessary phase shift, was demonstrated by the performance of the phase shifting sections. The expected advantages of the circuit were limited by the poor quality of the specific high temperature superconductor film that was tested. The performance advantages could be realized if the circuit were fabricated again with a high quality film.

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CHAPTER 1: INTRODUCTION

1.1 Overview

High-Temperature superconductor (HTS) materials were first discovered in 1986 [1].

Since then research has continued on these new materials and their possible applications.

Advances have been made in the superconductive materials themselves opening up new applications as the technology progressed. The major areas of research on HTS in Canada have been in bulk and thin film growth, microwave and power applications and other specialized applications.

The use of HTS materials for power applications relies on the ability to produce high quality bulk HTS ceramics. At present many problems remain with bulk HTS materials that limit the applicability of HTS to the proposed systems. Most notably, large scale power handling equipment requires the ability to handle large currents and magnetic fields. This ability has not been demonstrated in bulk HTS materials. The potential to handle the required currents exists and has been demonstrated in HTS thin-films. If the problems with bulk HTS materials can be overcome, then potential advantages for power systems exist. The major areas of research for power systems are in superconducting magnetic energy storage, fault current limiters, superconducting cables, generators and transformers. The most likely area for development is superconducting magnetic energy storage, for storage of excess energy generated at night and the subsequent return of that energy at peak periods in the day with little loss.

Major research occurs on HTS materials themselves, especially thin-films. This research includes determining appropriate substrates, addition of passivation layers and multilayer structures and improving the current carrying capabilities and high-power han-

dling [2-6]. Other research includes simulating the performance of HTS superconductors especially for high power levels where the series resistance of the material becomes non-linear.

An application of HTS materials is in superconducting quantum interference devices (SQUID). SQUID's are used in a variety of areas such as bolometers for radioastronomy, in nuclear magnetic resonance, magnetic resonance imaging, non-destructive imaging and microscopy. Non-destructive imaging allows the inspection of metals in a variety of industries, most notably aviation, for corrosion pits, fatigue cracks, voids, subsurface features and stress by the interruption of a current applied to the metal. All of these applications rely on the ability of SQUID's to detect and measure very small magnetic fields.

Another application of HTS materials is in digital circuits and systems. The systems make use of Josephson junctions. Josephson junctions are two terminal superconductive devices. Various circuits using high temperature and low temperature superconductors have been demonstrated with switching times as low as 1.5 ps per gate and demonstrated operation as high as 16 GHz [7].

One of the most promising areas for HTS is in thin films for microwave applications. A large body of research exists on developing various microwave circuits using HTS thin films [8,9,10,11]. The bulk of this research involves high Q filters and resonators at low frequencies. Superconductors are being used for these applications because they have clear advantages over other technologies. The use of HTS in a high Q filter allows for narrower bandwidths, sharper skirts, lower losses and lower noise figure as compared to a conventional filter. The outlined advantages are extremely useful in applications where

channels are very close together. Some proposed applications for these filters include cellular phone and personal communication system (PCS) base stations.

At the systems level, studies conducted have shown that the use of HTS in certain applications are beneficial, despite the higher costs and the need for cooling. One particular systems level report for a PCS system showed the use of HTS channel filters, tower-mounted at the antenna, could reduce the number of base stations required by 24%. With the high cost and difficulty involved in procuring base station sites, such a reduction in the number of required base stations quickly pays for the increased cost of the filters and cooling system required [12]. Other systems level examples of the use of HTS devices have been demonstrated for different applications [13,14]. Recent advances in cryocoolers have alleviated the reliability and maintenance concerns with regards to the cooling of HTS materials, with demonstrated life cycle testing of over 14,000 hours [12]. After a cryocooler has been included in a system it becomes possible to cool other components of the system. These components may include circuits that benefit from operating at lower temperatures or additional HTS circuits. Cooling a larger portion of the system requires a larger cooling capacity however the power and weight efficiency of cryocoolers improves with increasing capacity.

The need to cool a portion of a system allows the use of HTS circuits in other areas that are beneficial but may not justify the cost if they were the only components that would need to be cooled. Some examples of this are feed networks for large array antennas, long delay lines and phase shifters.

Four areas in antenna applications appear to offer performance advantages through the use of HTS. These areas are: low conduction losses in the feed networks, matching

electrically small antennas, matching moderately superdirective arrays and slow-wave structures for electronic scanning [15]. Various patch array antennas have been reported using HTS to reduce the losses in the feed networks [16,17,18]. Improved performance with respect to conventional patch array antennas are reported.

High temperature superconductors offer potential benefits in phase shifters and delay lines. Conventional delay lines are limited in the amount of delay they can provide due to the losses in the metal traces. HTS materials allow for very large delays with small losses. A reported 6 cm long yttrium barium copper oxide (YBCO) delay line had measured losses -0.12 dB at 30 K compared to an identical gold line with measured losses of -10.7 dB at 80 K [19]. A similar application of low loss lines was the design of a 40 ns chirp filter [20]. Various phase shifters using HTS have been fabricated, typically at frequencies below 5 GHz, with improved performance over conventional technologies in bandwidth and losses [21,22]. Other proposed phase shifters use SQUIDs or ferrites to provide continuous phase shifts over a large range of phase [23,24].

1.2 Thesis Objectives and Organization

The objective of this work is to investigate the suitability of HTS for use in phase shifters at high frequencies. Specifically, the design and testing of a 180° bit phase shifter in coplanar waveguide at Ka-band is presented. A fully integrated phase shifter design using HTS offers the promise of reduced losses, potentially up to 2 dB per bit. For a multiple bit phase shifter, the reduction in the losses can be significant. A fully integrated design eliminates the problem of integrating the switching elements with the phase shifter sections, as found in many conventional designs. Additionally, the use of coplanar waveguide lumped

elements are investigated at high frequencies. Such a phase shifter could potentially be used for a planar array antenna for a Local-Multipoint Communications System (LMCS).

The thesis is organized into five chapters covering the major topics of the thesis. The first chapter introduces the thesis and provides some basic background. Additional chapters provide more detail on the theory, design, testing and conclusions related to the design of a superconductive phase shifter.

Chapter 2 provides background material on superconductors and phase shifters in general. The history of superconductors and the basic properties that define superconductors are presented. The theory of operation of low temperature superconductors and speculation on the operation of high temperature superconductors are presented. Analytical models that are valid for both low temperature and high temperature superconductors are also presented. Details of various high temperature superconductors, their growth and patterning are covered. The theory of various types of planar phase shifters with their strengths, weaknesses and design equations are presented.

Chapter 3 provides details on the design of the phase shifter. Design goals and background for decisions on basic technologies selected are presented. The design of the phase shifter is presented from the ideal prototype network through simulations of the required elements, build up of the phase shifter and single-pole double-throw switch designs, to the final predicted results of the phase shifter.

Chapter 4 covers the fabrication, testing and measured results of the HTS phase shifter. Problems and solutions with the fabrication process are covered, as are problems with the test equipment. DC measurements of the quality of the HTS films are presented. Finally the measured performance of the phase shifter and various breakouts are covered.

Chapter 5 discusses the measured phase shifter results in relation to the design goals and simulated results. The suitability of this design for operation at Ka-band is addressed.

CHAPTER 2: SUPERCONDUCTOR AND PHASE SHIFTER BACKGROUND

2.1 Superconductors

Superconductive materials are materials that exhibit no measurable DC resistance and exhibit near perfect diamagnetism. Superconductors have been known of since 1911 but until recently have only been used in very specialized applications. In 1986 a new class of superconductive materials was discovered and much new research on superconductors has resulted.

This section will cover a brief overview of superconductive materials, their common properties and such theory as is known. The focus will then shift specifically to High-Temperature Superconductors (HTS) explaining in more detail the properties, technical issues for microwave applications and details on the type of film used in this thesis.

2.1.1 Superconductor History

Superconductive materials were first discovered by H. Kamerlingh Onnes in 1911 when he cooled a sample of mercury to 4K [25]. He noticed that the mercury at this temperature had no measurable DC resistance. Following this discovery various niobium-based alloys were discovered that exhibited the same properties at slightly higher temperatures. However none of these materials were superconductive above 23K. All of these materials exhibited no measurable DC resistance and near perfect diamagnetism. The near perfect diamagnetism, known as the Meissner effect, is the exclusion of magnetic flux from the interior of a superconductor, except within a thin region at the conductors surface.

The superconductive state is limited by three mechanisms, a maximum temperature T_c , a maximum current density j_c , and a maximum magnetic field H_c . These three

parameters combined are used to describe a boundary inside of which materials may superconduct. See Figure 2-1 for an example of this boundary.

FIGURE 2-1 Superconductive boundary as described by T_c , j_c and H_c . [1]

Various theories were proposed to explain the properties of superconductors, most notably the London theory [26], the Ginzberg-Landau theory [27] and the BCS theory [28]. The London theory, from 1935, gave reasonable predictions of the macroscopic properties of superconductors including the Meissner effect. The Ginzberg-Landau theory predicted high temperature superconductors in 1950. The BCS theory, from 1957, is the accepted theory on the fundamental causes of superconductivity in the materials discovered to that point.

Much research was performed with these superconductors, now called Low-Temperature Superconductors (LTS), however the need to cool them to 23K or below limited the practical applications. Some of the areas in which LTS materials have been used are in

nuclear magnetic resonance for chemical and pharmaceutical applications and in medicine for magnetic resonance imaging. LTS have also been used in astronomy for Superconducting Quantum Interference Devices (SQUIDS) to measure very small magnetic fields. LTS Josephson Junctions have been researched for digital circuits.

For more than 75 years materials that exhibited superconductive properties above 23K were unknown. In 1986 a new class of superconductive materials were discovered. This occurred when Bednorz and Müller [29] discovered a ceramic-based superconductor $\text{La}_{2-x}\text{Ba}_x\text{CuO}_4$ (LaBaCuO) that would superconduct at temperatures above 30K. This was quickly followed by the discovery of yttrium barium copper oxide (YBCO) by Paul Chu of the University of Houston and Mau-Ken Wu of the University of Alabama in Huntsville, which would superconduct up to 93K [30].

This discovery promised the possibility of using liquid nitrogen in order to cool the superconductive material. Liquid helium, which boils at 4K, was required to operate all previous superconductive materials. Liquid nitrogen, which boils at 77K, is ten times cheaper to produce and requires a much simpler refrigeration system than for liquid helium. Applications previously considered impractical for superconductors were now practical due to the lower cooling costs.

For the next few years many new superconductive materials were discovered. Currently the highest temperature material is $\text{Tl}_2\text{Ba}_2\text{Ca}_2\text{Cu}_3\text{O}_{10}$ (TBCCO) that has a T_c of 125K. This material promises operation at 77K, a large back off from its T_c , and thus should handle both larger currents and higher strength magnetic fields. Since the discovery of these high-temperature superconductors a large amount of research has focussed on new material development, the underlying physics responsible for these superconductors,

the electrical and physical properties of these materials and improvements in growing these materials in both bulk and thin-film form.

Over the last number of years, few new materials have been discovered and none have surpassed TBCCO in terms of its T_c . While little progress has been made in new material development, much progress has been made on the manufacturing of HTS materials mainly in thin-film form. The most common field for HTS materials to be applied is in electronics where high quality thin-films are available. In addition, while there are several theories on the mechanism of superconductivity in these HTS ceramics, presently there is no accepted explanation.

2.1.2 Properties of Superconductors

Superconductors possess two very remarkable macroscopic properties: immeasurably small DC resistance below T_c and near perfect diamagnetism. In 1956 Collins established an upper limit of $10^{-21} \Omega\text{-cm}$ for the resistivity of superconductors to DC currents. While superconductors have effectively no DC resistance this is not the case with AC currents. The resistance of a superconductor rises with the square of the frequency. The second property, near perfect diamagnetism, excludes magnetic fields from the interior of the superconductor. If a small magnetic field, below H_c , is applied to a superconductor, currents will be set up near the surface of the superconductor to exclude the magnetic field from the interior of the superconductor.

2.1.3 Superconductor Theory

Theory regarding the operation of superconductors is not complete. While the BCS theory is accepted as explaining the mechanism of superconductivity in LTS, there is not a theory presented that conclusively describes the mechanism of superconductivity in HTS materi-

als. There are accurate theoretical models for most LTS based on extensions of the BCS theory such as the Mattis and Bardeen equations [31] but these models cannot be rigorously applied to HTS. The most common model used for designing circuits using HTS is the Two-Fluid model or variations thereof.

Macroscopic theories of superconductivity apply well to both low temperature and high temperature superconductors. The two major macroscopic theories are the London theory and the two-fluid model. The Ginzberg-Landau theory applies to both low-temperature and high-temperature superconductors, actually predicting that high temperature superconductors exist.

The first model on the behaviour of superconductors that included both the lack of measurable DC resistance and the Meissener effect was proposed by London and London in 1935 [26], giving the now famous London equations. These equations can be derived from classical mechanics if it is assumed that there is no scattering.

$$\vec{F} = m \frac{d}{dt} \vec{v} = q \vec{E} \text{ and } \vec{J} = nq \vec{v} \quad (2-1)$$

$\vec{F}$ is a force acting on a charge in the presence of the electric field $\vec{E}$. The current density, $\vec{J}$, of a number of superconducting electrons n , is also defined. The mass, velocity and charge of the electrons are m , $\vec{v}$, and q respectively. Combining (2-1) yields

$$\frac{d}{dt} \vec{J} = \frac{nq^2}{m} \vec{E} \quad (2-2)$$

Now considering Maxwell's equations, relating electric field, current density and magnetic field as expressed by

$$\nabla \times \vec{E} = -\mu_o \frac{\partial}{\partial t} \vec{H} \text{ and } \nabla \times \vec{H} = \vec{J} + \frac{\partial}{\partial t} \vec{D} \quad (2-3)$$

Taking the curl of both side of (2-2) and inserting the first expression in (2-3) yields

$$\frac{\partial}{\partial t} \left(\nabla \times \vec{J} + \frac{1}{\lambda_L^2} \vec{H} \right) = 0 \text{ and } \lambda_L^2 = \frac{m}{\mu_o n q^2} \quad (2-4)$$

λ_L is called the London penetration depth and describes how far a magnetic field is able to penetrate into a superconductor before it is completely excluded. The London penetration depth is a property of the material but will vary with temperature according to the number of superconducting electrons, n .

The two London equations are

$$\text{London's 1st equation: } \frac{d\vec{J}}{dt} = \frac{1}{\mu_o \lambda_L^2} \vec{E} \quad (2-5)$$

$$\text{London's 2nd equation: } \nabla \times \vec{J} + \frac{1}{\lambda_L^2} \vec{H} = 0 \quad (2-6)$$

The first London equation, (2-5), is derived by inserting the London penetration depth into (2-2). The second London equation, (2-6), is derived from (2-4) using the Meissener effect to describe effect of the fields and currents inside the superconductor.

The London theory explains the operation of superconductors well for DC currents and very low frequencies. At higher frequencies there is loss in superconductive materials that increase with the square of the frequency. This has been explained by the Two-Fluid model. The Two-Fluid model assumes that there are two types of conducting electrons in the superconductor, both normal and superconducting. The London equations only account for the superconducting electrons and thus are only valid for DC. The total number of electrons n , is divided between normal n_n and superconducting n_s electrons. The ratio between n_s/n_n varies with temperature according to:

$$\frac{n_n}{n} = \left(\frac{T}{T_c}\right)^4 \text{ and } \frac{n_s}{n} = 1 - \left(\frac{T}{T_c}\right)^4 \quad (2-7)$$

The conductivity then becomes a complex value, see (2-8), where σ_1 is the conductivity of the normal electrons which cause losses and σ_2 is the conductivity of the superconducting electrons which cause the kinetic inductance effect.

$$\sigma = \sigma_1 - j\sigma_2 \quad (2-8)$$

The normal conductivity σ_1 is

$$\sigma_1 = \sigma_n \left[\frac{T}{T_c}\right]^4 \quad (2-9)$$

where σ_n is the normal state conductivity at $T = T_c$. The conductivity of the superconducting electrons, σ_2 , is

$$\sigma_2 = \frac{1}{\omega \mu_o \lambda_L^2} \quad (2-10)$$

To account for the temperature dependence of the London penetration depth λ_L , which varies with the fraction of superconducting electrons as in (2-7), the following equation is appropriate according to [34]

$$\lambda_L(T) = \frac{\lambda_L(0)}{\sqrt{1 - (T/T_c)^4}} \quad (2-11)$$

where $\lambda_L(0)$ is the effective London penetration depth as T approaches 0 K.

Substituting equations (2-9), (2-10) and (2-11) into (2-8) the complex conductivity is then

$$\sigma = \sigma_n \left[\frac{T}{T_c} \right] - j \left[\frac{1}{\omega \mu_o \lambda_L^2(0)} \right] \left[1 - \left(\frac{T}{T_c} \right)^4 \right] \quad (2-12)$$

With the complex conductivity now known the surface impedance can now be calculated. The surface resistance is an important figure of merit for a superconductor as the main reasons for using superconductors in electronics applications are their low losses and no dispersion up to very high frequencies [32]. The surface impedance of a material is defined as

$$Z_s = \frac{E_t}{\int_{-\infty}^0 J dx} = R_s + jX_s \quad (2-13)$$

and is measured in units of ohms per square. Equation (2-13) is strictly only true for a wave propagating in a planar conductor, however it is a close approximation for good conductors. Assuming that Ohm's law applies and that the electric fields decrease exponentially into the conductor then the surface impedance is given by

$$Z_s = (1 + j) \sqrt{\frac{\omega \mu_o}{2\sigma}} = R_s + j\omega L_s \quad (2-14)$$

For a normal conductor σ is real and constant, therefore the surface resistance and reactance are equal and depend on $\omega^{1/2}$. The surface impedance of a superconductive material can be calculated by substituting (2-12) into (2-14) giving the following expression

$$Z_s \approx \omega^2 \mu_o^2 \lambda_L^3(T) \sigma_1 / 2 + j\omega \mu_o \lambda_L(T) = R_s + j\omega L_s \quad (2-15)$$

Equation (2-15) assumes that $(\sigma_1/\sigma_2)^2 \ll 1$ which is true for temperature lower than $0.9 T_c$. From Equation (2-15) two major items of interest can be noted: Firstly the surface resistance of a superconductor rises with the square of the frequency rather than to the square root of the frequency as for normal conductors. Secondly the surface inductance is

directly proportional to the penetration depth and thus can be used to determine the penetration depth.

The Ginzberg-Landau theory [27] examines the London theory and finds faults in it, most notably that the surface tension between the normal and superconducting phases cannot be determined and does not allow for correct description of the destruction of superconductivity due to magnetic fields and currents. The Ginzberg-Landau theory is based on calculations of the free energy in the superconductor.

Ginzberg and Landau assume an effective wave function of the superconducting electrons and then evaluate the free energy in the absence of a magnetic field. The calculated free energy is shown to match with previously reported experiments. They then add the presence of a static magnetic field and again evaluate the free energy including the energy of the magnetic field and a potential gradient in the effective wave function for a one-dimensional case. Again evaluating the free energy and with a change of variable a new unitless term is introduced, κ . Their equations become formally identical to the London equations when $\kappa = 0$. However there are differences even for this case, the London penetration depth is a constant, independent of the applied magnetic field at a given temperature, while the actual penetration depth will vary so as to minimize the free energy. The value κ is a material property, the long range order parameter and is defined as $\kappa = \lambda/\xi$, the penetration depth divided by the coherence length. The coherence length is defined in the BCS theory. Ginzberg and Landau calculated that for mercury $\kappa \approx 0.165$.

The value of κ is used to distinguish between low temperature, Type I, and high temperature, Type II, superconductors. All low temperature superconductors have

$\kappa < 0.707$ and one critical magnetic field. For $\kappa \geq 0.707$ a mixed state of superconducting and normal portions of the material can exist with magnetic fields penetrating the superconductor at fixed points, called flux pinning. Type II superconductors have two critical magnetic fields, H_{c1} and H_{c2} . Up to the first critical magnetic field, H_{c1} , magnetic fields are completely excluded from the superconductor. Between H_{c1} and H_{c2} , the superconducting state is a mixed state with both superconducting and normal portions of the material. Above H_{c2} the superconductive state does not exist.

2.1.3.1 Low Temperature Superconductor Theory

The BCS theory of superconductivity [28] gives a detailed quantum mechanical explanation of low-temperature superconductivity. The BCS theory covers the five major points required to describe the causes of superconductivity: a second-order phase transition at T_c , an energy gap for particle-like excitations, the Meissener-Ochsenfeld effect, ($\vec{B} = 0$), infinite DC conductivity, ($\vec{E} = 0$), and that $T_c \sqrt{M} = \text{const.}$

The BCS theory states that for the appearance of the superconducting phase transition to occur, the transition must be such that the energy difference, $\Delta\epsilon$, between the electron states involved be less than $\hbar\omega$. The BCS theory starts from the Sommerfeld-Bloch individual particle model which gives a good description of normal metals and describes the normal state of a superconductor.

The Sommerfeld-Bloch model assumes that to a first approximation it is acceptable to neglect the positions of the electrons and to assume that the electrons move independently according to a self-consistent field determined by the other conduction electrons and the ions. The wave function of the metal as a whole is designated by the occupation of

Bloch individual particle states of energy, $\epsilon(\vec{k})$, defined by wave vector $\vec{k}$ and spin σ . In the ground state, all levels with energy below the Fermi energy are occupied while all those above the Fermi energy are empty. This theory doesn't include correlations between electrons to Coulomb forces or interactions between electrons and lattice vibrations, called phonons.

The electron-phonon interaction gives a scattering from the Bloch state defined by the wave vector $\vec{k}$ to $\vec{k}' = \vec{k} + \vec{k}$ by the emission or absorption of a phonon of wave vector $\vec{k}$, which is responsible for thermal scattering. The contribution to the energy of the electron-phonon interactions can be found by eliminating the linear electron-phonon interactions from the Hamiltonian. H_2 , a term of the second order Hamiltonian, gives the interaction between electrons independent of vibrational amplitude. The term H_2 is the interaction between electrons resulting from electron-phonon interactions.

When the change in energy is less than $\hbar \omega$, the attractive components of H_2 dominate the repulsive short-range screened Coulomb interaction between electrons, giving a net attraction. This attraction can allow a co-operative many particle state lower in energy than the normal state, this is the superconductive state.

The normal state of the superconductor is described by the Bloch model. The ground state wave function is a linear combination of low-lying normal state configurations where the Bloch states are virtually occupied in pairs of opposite spin and momentum. Excited states of the superconductor are formed by specifying certain occupied Bloch states and using the rest to form linear combinations of virtual pairs. A one to one correspondence exists between excited superconducting and normal states.

When a net current flows, paired states have a net momentum, q , that is the same for all virtual pairs within the coherence length ξ_o . The coherence length is given by Faber and Pippard [33] as $\xi_o = a \hbar v_o / (kT_c)$ where v_o is the average electron velocity at the Fermi surface and a is a dimensionless constant, for example 0.15 for Sn and Al. For each q there is a metastable state with a minimum of free energy and a unique current density. Individual electron scattering will not change q , common to all virtual pair states, but will simply cause fluctuations around the current determined by q . Most fluctuations will increase the free energy, only those fluctuations which effect most of the electrons so as to change q will reduce the free energy. There are many virtual pairs within the coherence length so such fluctuations are very rare, the metastable current carrying state can last indefinitely.

Normally conducting electrons exist along with superconducting virtual pairs (Cooper pairs) but at different energy levels. At $T = T_c$ this energy gap is reduced to zero and the normal state is the minimum of free energy. Below T_c this energy gap centered around the Fermi energy, which is the amount of energy that must be added to a Cooper pair to break it into individual electrons, is a real positive value. The electron density in the energy gap is zero, electrons either exist above this gap as individual electrons or as Cooper pairs below the energy gap. The density of states around the energy gap account for Josephson junctions but they shall not be covered here.

2.1.3.2 High-Temperature Superconductor Theory

There is no accepted theory explaining the causes of superconductivity in high-temperature superconductors. Many theories of the operation of high-temperature superconductors

use the BCS theory with different mechanisms for pair formation [35]. If the coupling mechanism is assumed to be through phonons as in the BCS model, then stronger coupling is required than found in low temperature superconductors. Another suggested coupling mechanism is through excitons, where the movement of a conduction electron along the main chain of the crystal causes a movement of charge in the side chains. The movement of charge in the side chains is such that when another conduction electron passes on the main chain, the charge is attractive causing electrons to travel in pairs on the main chain. Another coupling mechanism that has been considered is through plasmons, quantum of plasma oscillation. A final related theory suggests polarons, electron plus induced lattice polarization, as the coupling mechanism. Another main theory of the superconducting phenomenon in HTS is the resonating valence bond theory [36]. This theory uses the fact that the conduction mechanism lies in copper-oxide planes. When CuO_2 , an insulator, is mixed with other elements, (Y,Ba), the valence state of the copper changes from +2 to an average of +2.33. When in the superconducting state, the conduction band is filled with loose electrons, leaving positively charged holes in the lattice. The positively charged holes in the latter would be the primary charge carriers. Models using some form of the BCS theory or the resonating valence bond theory are the major proposed theories for high temperature superconductors.

A large number of papers on computational methods for predicting the performance of HTS exists. The most reported techniques are based on two-fluid models. The complexity of the techniques vary from calculation of the surface impedance for inclusion in commercial software to nonlinear 3-D finite difference time domain techniques for high-power operation [37,38,39].

2.1.4 High Temperature Superconductors

High temperature superconductors are a class of ceramic materials that were first discovered in 1986. They are called high temperature in that superconductivity is present at temperature as high as 125K, compared to a maximum of 23K in all previously known superconductors. HTS materials are different than LTS in that they are all copper-oxygen ceramics rather than metal conductors. These ceramics must be formed properly as different phases of the same family of ceramic have different superconductive properties. The three most common families of HTS are YBaCuO, BiSrCaCuO and TlBaCaCuO. Several HTS families, their various phases and transition temperatures can be found in Table 2-1.

TABLE 2-1 HTS Families, their Phases and Critical Temperature [40]

Material	Phase	T _c (K)
(LaSr)CuO	(LaSr) ₂ CuO ₄	40
YBaCuO	YBa ₂ Cu ₃ O ₄	95
	YBa ₂ Cu ₄ O ₈	80
TlBaCaCuO	Tl ₂ Ba ₂ CuO ₆	90
	Tl ₂ Ba ₂ CaCu ₂ O ₈	110
	Tl ₂ Ba ₂ Ca ₂ Cu ₃ O ₁₀	125
BiSrCaCuO	Bi ₂ Sr ₂ CuO ₆	12
	Bi ₂ Sr ₂ CaCu ₂ O ₈	90
	Bi ₂ Sr ₂ Ca ₂ Cu ₃ O ₁₀	110
HgBaCaCuO	HgBa ₂ CuO _x	85

All HTS materials are composed of a minimum of four elements. The elements must be deposited with close control on the ratio of the elements to obtain high quality films. Most of the elements of HTS materials are highly reactive, potentially leading to unwanted chemical reactions that can destroy the superconducting properties of the mate-

rial. All of the HTS compounds contain oxygen as an important element, however oxygen is incompatible with most processing techniques. Oxygen is also crucial in determining the properties of crystal imperfections such as grain boundaries.

The crystal structure of HTS ceramics is related to the perovskite unit cell. This structure is that of a metal ion (anion) surrounded in the center of a cube of cations, surrounded by an octahedral configuration of oxygen atoms. See Figure 2-2 for an example of a unit cell for YBCO. The superconducting properties of these materials are very anisotropic, they superconduct very well in the a-b plane but very poorly in the c direction. This is important in that structures that use these materials need to be planar both in crystal structure and in layout. Crossovers, where one HTS line crosses another without touching, are difficult to fabricate in HTS but have been accomplished by Pettiette-Hall et. al. at TRW [41]. Most crossovers for HTS circuits are fabricated using gold.

FIGURE 2-2 $\text{Y}_1\text{Ba}_2\text{Cu}_3\text{O}_7$ unit cell.

HTS ceramics are grown both in bulk and thin-film form. Thin-film HTS is the more developed technology having j_c 's orders of magnitude better than that found in the bulk form. This is related to the more uniform and controlled crystal structure of the thin-films than the bulk materials. The major limiting factors in the current carrying capacity of HTS lies in the grain boundaries and crystal orientation. Every grain boundary acts as a Josephson weak link and the supercurrent electrons must tunnel through this boundary. Forcing grain boundaries is one method of generating Josephson junctions for switching applications. The crystal orientation is important in that the supercurrent flows better in the a-b plane than in the c direction. Speculation is that the relatively weak connection between the Cu and O orbitals across the Y layer acts as a weak link in that direction. The thin-films are usually grown epitaxially on a substrate giving better grain alignments, fewer boundaries and good planarity. In the bulk ceramic, the crystal is more randomized with different crystal orientations and more grain boundaries, severely reducing the current carrying capabilities of the material. Applications of HTS thin-films is therefore much more advanced, being capable of meeting the needs for the electronics industry. Application of bulk films will have to wait until greater control of the crystal structure can be achieved.

The HTS materials are all Type II superconductors. Type II superconductors have two critical magnetic fields, a lower critical field H_{c1} and an upper critical field H_{c2} . When the applied field is lower than H_{c1} the material is entirely superconducting and no magnetic field penetrates. Above H_{c1} but below H_{c2} there is some flux penetration but it is fixed in position by circulating currents, known as flux pinning. The regions around the pinned flux lines is normal while the rest of the material is superconducting. This is also

known as the mixed state because parts of the material are superconducting while other parts are normal. Finally, above H_{c2} the entire material is normal.

2.1.4.1 Methods of Growing and Patterning HTS Thin films

There are three main techniques for growing HTS films; Molecular Beam Epitaxy, Sputtering and Laser Ablation. These methods all attempt to achieve the correct composition of the chemicals over the area of the substrate and throughout the thickness of the film. In addition there must be the correct oxygen content and crystal structure. The films can be formed with both in-situ and ex-situ processes. In the in-situ process the materials are deposited on the substrate above its crystallization temperature. In the ex-situ process the constitutive components are deposited on the substrate and then crystallized by annealing the wafer in an oxygen environment. All techniques require the substrate to be raised to a temperature greater than 800°C. The high temperature poses problems for integration with active devices and for substrate selection.

Molecular Beam Epitaxy uses separate sources for each element of the film, which allows for quick changes in the composition of the material but requires very strict control on the rate of deposition from each source. Sputtering uses a composite source to deposit the film on the substrate, and allows the inclusion of oxygen in the sputtering gas. Off-axis sputtering is the preferred method of sputtering but is very slow. In laser ablation a composite source is exposed to a focused laser beam from a high power source. A portion of the composite source is superheated and a fraction of the material will ablate off of the source onto the substrate. The National Research Center fabricated the YBCO films used in this thesis by pulsed laser ablation. A 248 nm excimer laser was used to target the source and the film was deposited on a LaAlO_3 substrate.

After the films have been grown they must be etched into useful shapes. All forms of etching the material will result in degrading the superconductive properties of the film. This is most noticeable at the edges of traces where good superconductive properties are essential, due to current crowding. The superconductive properties may be partially restored by annealing in oxygen after processing, but care must be taken to carefully clean the chip to limit the foreign chemicals that may destroy the superconductive properties of the HTS material.

The most common form of etching used with HTS are wet etching and ion milling. With wet etching care must be taken to insure that the HTS material does not contact any acids. Even a very weak acidic solution will very quickly etch away all of the HTS compounds. Ion milling is the least damaging method of etching HTS and gives very fine features with good resolution. The biggest problem with ion milling is that it is more expensive than wet etching. Patterning of the HTS films was performed at NRC using standard photolithography and ion beam milling. The ion beam consisted of Argon ions with an energy setting of 500 eV. Low resistance gold pads were also added to the HTS films at NRC. The patterned HTS films were prepared through an ion mill cleaning of the surface of the films. Gold was then evaporated onto the exposed areas of the film.

2.1.4.2 Substrates for HTS Thin films

Appropriate substrate selection is essential for proper operation of HTS microwave circuits. The substrate is generally assumed to be a passive component of the entire structure and is mostly ignored. With HTS thin-films the substrate cannot be ignored. Those substrates that one would be most tempted to use, such as Si, GaAs, MgO or Al_2O_3 are not well suited for HTS materials. High quality films are difficult or impossible to grow on

these substrates without buffer layers due to poor lattice matches, chemical incompatibility or poor crystal structure. See Table 2-2 on page 30 for various substrates that have been investigated and their properties.

This leads to a more fundamental look at the effects of the substrate on the film grown on the substrate. In the ideal case the substrate should provide mechanical support for the film but not interact with the film in any other way except for providing sufficient adhesion and in many instances providing a template for atomic ordering. In practice the substrate has a large effect on the film's properties. There is no ideal substrate for HTS films, specific applications require substrate materials that offer a suitable compromise for the application.

There are many issues involved in substrate selection that are important for film growth regardless of the film being produced. Julia M. Philips of AT&T Bell Labs [42] has covered them well. The most important global issues for substrate selection are: chemical compatibility, thermal-expansion match, surface quality, substrate cleanliness, substrate homogeneity, substrate thermodynamic stability and buffer layers.

Chemical compatibility is very important in the selection of a substrate especially for HTS films. There should be no chemical reaction between the film and the substrate. Many possible candidates for HTS films, such as Si, are highly reactive with all the current HTS materials. Another requirement specific to HTS is that the substrate must be unreactive to the oxygen rich environment required for film growth and processing.

Most substrates will have some thermal-expansion mismatch with any film grown on them. This can result in cracking or loss of adhesion of the film during thermal cycling, of particular importance to HTS with the wide range of temperatures encountered between

processing (approximately 1100K) and operation (usually 77K). HTS materials are rather brittle therefore are more likely to be subject to cracking. Cracking of HTS films introduces additional weak-links that reduce the current carrying capacity and increase the losses of the HTS film.

The surface quality of the substrate is critical since it is at the surface that the film and substrate interact. "A uniform surface is necessary (though not sufficient) to insure a uniform, homogeneous film." [42] There are many levels of surface defects that must be minimized to allow for high quality films to be produced. Of particular note for microwave applications of HTS is twinning boundaries. Twinning boundaries occur due to a phase transition of the substrate at various temperatures and affect the dielectric properties of the substrate, making highly accurate device modeling difficult if not impossible.

Substrate cleanliness is crucial for the growth of reproducible films. For the growth of HTS films the substrate is generally degreased in organic solvents followed by annealing in oxygen if the substrate is an oxide.

Substrate homogeneity is in many ways related to the surface quality. The substrate should be a single phase as much as possible because multiple phases cause grain boundaries that may affect the microstructure of the film. Also the film may not grow as well on one phase of the substrate as compared to others. Such defects, including twin boundaries, are potential nucleation sites for competing crystalline orientations of the film being grown.

Buffer layers are often used with HTS films to alleviate many of the problems associated with various substrates, most often for cases of chemical incompatibility. A buffer layer must be chemically compatible with both the substrate and the film. In addi-

tion, buffer layers must be reproducible with good surface qualities for the growth of a film on its surface. In addition to chemical compatibility, buffer layers can be used to alleviate thermal cracking and improve the epitaxial quality of the film.

The best HTS films grown to date are epitaxial on their substrates. This leads to further requirements for the substrate to support epitaxial growth. These further requirements include: lattice match, coincidence sites, surface and structural quality. The lattice match should be as good as possible, thereby improving the ability to obtain a singly oriented film. Coincidence sites are atomic positions that coincide on either side of the interface. This generally, though not exclusively, means that the film and substrate should have the same crystal structure. Surface and structural quality are important to minimize nucleation sites for misoriented grains. Single crystal films are essentially only possible when the substrate is single crystalline.

One further requirement on the selection of a suitable substrate is required, the suitability of the substrate for the intended application. For microwave circuits this would include: supporting high quality films, having low dielectric loss, available in large area wafers, being isotropic and supporting low surface resistance films. These requirements stem from the fact that HTS materials are used in microwave applications mainly for their low loss properties. The most common applications are filters and long delay lines. In these cases the losses in the film and the substrate are the major limiting factors. One additional requirement may be a reasonable dielectric constant of the substrate to limit the propagation of surface acoustic wave (SAW) modes.

The first major group of materials considered for HTS substrates are perovskite-structure oxides such as SrTiO_3 , LaGaO_3 and LaAlO_3 . These materials have the advantage

of having similar crystal structure to the HTS films, giving a large number of coincidence sites and in most cases similar lattice constants. In addition the substrates themselves are oxides and should have good chemical compatibility. These oxides have shown the ability to support high quality HTS films with the most common combination of all reported superconductors being YBCO on LaAlO_3 . These materials are not without their problems, the most common of which is a phase transition in the HTS processing range.

The search for suitable substrates has not been limited to perovskites. In order to reduce some of the problems with the perovskite substrates, including high substrate cost, high dielectric constant and twinning, other non-perovskite-structure oxides, eg. MgO and Al_2O_3 , have been considered. As these materials are oxides the chemical compatibility is still good, however coincidence sites and lattice match both suffer due to different crystal structures. The main advantage of these substrates is that many are already commercially available for use in other microwave applications so their electrical properties are well known and have good electrical performance. The use of these non-perovskite-structure oxides should allow for easy integration with existing technologies.

The most commonly used substrates from these materials are sapphire (Al_2O_3) and MgO . High quality films have been reported with MgO , but due to its large lattice mismatch such films are very sensitive to surface preparation. Sapphire is also of interest, though not as much for microwave application due to its anisotropic dielectric constant, that also precludes its use in most conventional microwave applications. In addition sapphire reacts with HTS materials so the use of buffer layers is generally required.

Research has also been conducted to grow HTS films on semiconductor substrates for direct integration with active devices. Attempts to grow HTS films on the same sub-

strate as active devices, both on Si and GaAs substrates, has met with at best limited success for a variety of reasons. Silicon has a good lattice match with HTS compounds but there is a variety of other problems. The most damaging problems are that Si is highly reactive with HTS compounds and has a coefficient of thermal expansion 3-4 times smaller. The use of buffer layers slightly reduces these problems without eliminating them. Even with a buffer layer the thickest HTS film that can be grown without cracking is only 50 nm. The best reported results use YSZ as a buffer giving a T_c of 86-88 K and a j_c at 77 K of $2.2 \times 10^6 \text{ A/cm}^2$ [43]. Growth of HTS films on GaAs has been even more difficult due to the lower temperature that the compound semiconductor can handle as compared to the required processing temperatures of HTS films.

The process available at the National Research Council where the HTS films were grown and patterned is YBCO grown on LaAlO_3 . This is the most reported combination and provides very good films and microwave properties, except for the second order phase transition in the LaAlO_3 .

Janus Konopka and Ingo Wolff [44] studied the dielectric properties of various substrates used for HTS over a range of frequencies and a range of temperatures. Their results show that the dielectric constant of LaAlO_3 is constant at 24.18 over the frequency range of 5-40 GHz when measured at 298 K. The dielectric constant decreases with temperature and is 23.85 at 80 K. The loss tangent of LaAlO_3 was measured with respect to temperature only and was found to be 5.2×10^{-4} at 80 K.

The dielectric properties of LaAlO_3 shall be looked at in more detail. As has been mentioned previously LaAlO_3 is anisotropic. Measurements of ϵ in the a-b and c planes

TABLE 2-2 Several Potential HTS Substrates

Substrate	ϵ	$\tan \delta$	Lattice Match	Phase Transition	Comments
SrTiO ₃	277	6×10^{-2}	Good	2nd Order	Excellent quality, poor ϵ and $\tan \delta$
LaGaO ₃	25	6×10^{-3}	Good	1rst Order	Severe twinning
LaAlO ₃	24	3×10^{-5}	Good	2nd Order	Most common
NdGaO ₃	20	3×10^{-4}	Good	None	Magnetic ions
YAlO ₃	16	1×10^{-5}	Fair	None	Possibly very good
MgO	9.6 5	5×10^{-4}	Poor	None	Sensitive to surface quality
Al ₂ O ₃	9.3 4	3×10^{-5}	Poor	None	Needs buffer layer, anisotropic
YSZ	25	8×10^{-3}	Fair	None	Excellent films, some chemical reaction

give results of ϵ_a (ϵ_b) averaging 23.99 and ϵ_c averaging 25.21 [45]. For the purposes of this thesis all simulations of LaAlO₃ assumed an isotropic dielectric constant of 23.85. This value was chosen from the paper by Janus Konopka and Ingo Wolff as the paper included changes in the dielectric constant for different frequencies and temperatures. The value of 23.99 from Reference [45] was measured at room temperature and expected operating temperatures of the HTS circuit are below 90 K.

2.2 Phase Shifters

Phase shifters are circuits that control the relative phase of a signal passing through it. The two main classes of phase shifters are digital and continuous. In a digital phase shifter there are several different selectable phase shifts allowing a broad range of phases, depending on the number of bits. In a continuous phase shifter, the phase through the circuit can be varied over as much as 180° by application of an external voltage to what is usually a ferrite material. In this thesis digital phase shifters shall be considered as they are

more commonly used for planar circuits than continuous phase shifters.

Most conventional phase shifters achieve a bandwidth of approximately 10% and losses of 1.5-3.0 dB / bit. Schindler et. al. [46] reported a 3 bit K/Ka band phase shifter with an octave bandwidth and losses of 3.0-3.3 dB per bit. The large bandwidth is possible due to using a higher order T-network for the 180° bit. Other reported phase shifters include a 4-bit Ka-band phase shifter with bits of 60°, 30°, 15° and 7.5° having total losses of 6.5 dB [47] and a W-band InP PIN diode phase shifter with losses of 3 dB per bit [48].

There are two major methods of creating the phase shift for digital phase shifters; through a time delay or a true phase difference. The application for which the phase shifter is intended will determine which type is most appropriate. Time delay phase shifters are either switched line or reflection phase shifters. True phase difference phase shifters are either loaded line or high-pass low-pass phase shifters.

For applications which require large instantaneous bandwidths or true time delays, a switched line or reflection type of phase shifter are most suited. Time delay phase shifters are usually used in phased array radars where large instantaneous bandwidth is essential. For phase comparators of any sort, the phase shifter that will give the required bandwidth and the least loss is most appropriate.

2.2.1 Switched Line Phase Shifters

A switched line phase shifter consists of two different lengths of line between two Single-Pole Double-Throw (SPDT) switches, see Figure 2-3. This type of phase shifter is a time delay device, the generated phase shift will be proportional to the frequency. One length of line l , is usually considered the reference and the other line $l + \Delta l$ is the delay line. The phase shift is accomplished through the difference in the lengths of the lines Δl .

The phase shift is given by $\Delta\phi = \frac{2\pi\Delta l}{\lambda}$. The choice of length l is important. The length must be chosen so that $l \neq \frac{n\lambda}{2}$ is true. If the electrical path length of $l_1 = l$ is multiple 180° then the phase shifter will go through 360° of phase error due to the resonant path. The switching elements used will contribute to the electrical path length. This resonance error also occurs when $l_2 = l + \Delta l$ is $\lambda/2$. For a 180° phase shift this error doesn't occur and the lines can be any reasonable length.

FIGURE 2-3 Switched Line Phase Shifter

The governing equation for a switched line phase shifter is [49]:

$$S_{21} = \frac{1}{1 + \frac{1}{Z_1 - j \cot\left(\frac{\pi l_1}{\lambda}\right)} + \frac{1}{Z_2 - j \cot\left(\frac{\pi l_2}{\lambda}\right)}} - \frac{1}{1 + \frac{1}{Z_1 - j \tan\left(\frac{\pi l_1}{\lambda}\right)} + \frac{1}{Z_2 + j \tan\left(\frac{\pi l_2}{\lambda}\right)}} \quad (2-16)$$

An estimate of the insertion loss, neglecting metal and dielectric losses is given by

$$\delta_\phi = 40 \log \left[1 + \frac{1}{2} \left(\frac{R_s}{Z_0} + \frac{Z_0}{R_p} \right) \right] \quad (2-17)$$

where R_s and R_p are the ON and OFF state resistances of the switching elements and Z_0 is the characteristic impedance.

To achieve a wider bandwidth than could normally be achieved with such a periodic structure a Schiffman phase shifter can be used [49]. In the standard case the phase shift produced is a linear function of frequency. A Schiffman coupled section is a linear function of frequency plus a sinusoidal function of frequency. By selecting l_1 parallel to the centre portion of the phase-frequency plot of the Schiffman curve, a wider bandwidth can be obtained at the cost greater losses and area. Again care must be taken so that no path is a multiple of 180° to avoid the resonant section and the associated phase error.

2.2.2 Reflection Phase Shifters

Reflection type phase shifters consist of a circulator or coupler terminated by the desired impedance [49]. The impedances come in two main forms, lumped elements or switched transmission line stubs. Lumped element terminations give larger bandwidths, an octave or more in most cases, while switched transmission line stubs give time delay devices suitable where large instantaneous bandwidths are required such as phased-array radars. Two reflection type phase shifters are shown in Figure 2-4.

FIGURE 2-4 Topologies of Reflection Phase Shifters

Reflection phase shifters suffer from one major source of error not present in other types of phase shifters. Mismatches between the circulator and the terminating impedance can contribute large errors. These errors are given by [49]:

$$\varepsilon_{\varnothing} = \pm \left(1 + 3|\Gamma_X| - \frac{1}{4} \sin \pi |\Gamma_X| \right) \text{asin} \left| \frac{\Gamma_M}{\Gamma_X} \right| \quad (2-18)$$

where $\varepsilon_{\varnothing}$ is the phase error, Γ_M is the mismatch between the circulator and the reflecting elements and Γ_X is the reflector. This can be simplified when there is little loss in the reflection elements or $|\Gamma_X| = 1$ to:

$$\varepsilon_{\varnothing} = \pm 4 \text{asin} |\Gamma_M| \quad (2-19)$$

and further approximated by

$$\varepsilon_{\varnothing} = \pm 100^\circ (\rho - 1) \quad (2-20)$$

where ρ is the voltage standing wave ratio (VSWR). For a VSWR of 1.2 this gives an error of approximately $\pm 20^\circ$. Therefore it is extremely important the circulator or coupler be very well matched to the reflection elements. The circulator or coupler must meet further requirements due to internal reflections. Isolation of only 20dB gives rise to maximum errors of $\pm 22.8^\circ$ while isolation of 40dB will reduce these errors to only $\pm 2.3^\circ$ [49].

Time delay reflection phase shifters, having either series or shunt switching elements terminated by either open or short circuit stubs respectively, have the instantaneous wide bandwidth needed for applications such as pulsed phased-array radars. In ideal operation with a shunt switching element, when the switching element is closed there will be infinite admittance and when the switch is open there will only be a line of length $\frac{\Delta l}{2}$. The

admittance of the length of line is $\frac{Y}{Y_o} = -j \cot \left[\frac{2\pi \frac{\Delta l}{2}}{\lambda} \right] = -j \cot \frac{\Delta \phi}{2}$ giving the governing

equation for time-delay reflection phase shifters of:

$$\Delta \phi = \frac{2\pi \Delta l}{\lambda} \quad (2-21)$$

Imperfect switching devices have parasitics changing the ideal open and closed admittances. By proper device selection the effects of these parasitics can cancel themselves out.

Lumped element reflection phase shifters operate in a different manner, in that they give a constant phase shift over a large bandwidth. For a 180° bit, only a switching element is required. A perfect switching element is 0Ω when closed and $\infty\Omega$ when open, giving a phase difference $\Delta \phi = 180^\circ$. The bandwidth of such a structure is limited only by the circulator or coupler used.

For other phase shifts the switching device forms a portion of the lumped elements needed to realize the phase shift, ordinarily contributing some shunt capacitance. See Figure 2-5 for design equations and parameters for various phase shifts. For $\pm 2^\circ$ all bandwidths are greater than one octave assuming that the bandwidth of the circulator or coupler is sufficient.

The average power that can be handled by a lumped element reflection phase shifter is given by [49]:

$$\overline{P}_i = \frac{\overline{P}_D}{4R_s Y_o} \left\{ k^2 \left(\frac{\omega}{\omega_o} \right)^2 + \left[1 - (1-a) \left(\frac{\omega}{\omega_o} \right)^2 \right]^2 \right\} \quad (2-22)$$

FIGURE 2-5 Performance of lumped element reflection phase shifter. [49]

where $\overline{P}_D$ is the maximum average device power, R_s is the device series resistance, Y_o is the characteristic admittance and k and α are given for various phase shifts in Figure 2-5.

The insertion loss is given by

$$\delta_{\phi} = 10 \log \left[\frac{1}{1 - \overline{P}_D / \overline{P}_i} \right] \quad (2-23)$$

with $\overline{P}_D / \overline{P}_i$ from (2-22).

2.2.3 Loaded Line Phase Shifters

A loaded line phase shifter is a line shunted by two susceptances a distance apart. The shunt susceptances can be either transmission line stubs or lumped elements. Loaded line phase shifters are only used for small phase shifts as the bandwidth becomes too small for larger phase bits. See Figure 2-6 for the topology of a loaded line phase shifter.

FIGURE 2-6 Topology of Loaded Line Phase Shifters

The governing equations for loaded line phase shifters, where $\theta = \frac{2\pi l}{\lambda}$ is the distance between the susceptances and B_N is the normalized shunt susceptances, are [49]:

$$S_{21} = \frac{1}{[\cos\theta - B_N \sin\theta] + j\left[B_N \cos\theta + \left(1 - \frac{B_N^2}{2}\right) \sin\theta\right]} \quad (2-24)$$

$$\varnothing = \text{atan} \left[\frac{B_N + \left(1 - \frac{1}{2} B_N^2\right) \tan\theta}{1 - B_N \tan\theta} \right] \quad (2-25)$$

Since the inverse tangent (atan) is normally taken between $\pm\pi/2$ the phase shift can be represented by:

$$\varnothing_D = \pi + \text{atan} \left[\frac{B_N + \left(1 - \frac{1}{2} B_N^2\right) \tan\theta}{1 - B_N \tan\theta} \right] \quad (2-26)$$

The phase error, assuming lossless circuits and that both phase bits have the same reflection coefficient is:

$$\varepsilon_\varnothing = \pm \text{asin}|\Gamma|^2 \quad \text{or} \quad |\Gamma| = \sqrt{\sin\varepsilon_\varnothing} \quad (2-27)$$

For widest bandwidth, the spacing between the shunt susceptances should be spaced $\theta = \lambda/4$ apart.

Using transmission line stubs the susceptances with the switching element open B_{NO} and closed B_{NS} are:

$$B_{NO} = K_S \tan K_\theta \theta \quad (2-28)$$

$$B_{NS} = K_S \tan K_\theta \theta \quad (2-29)$$

Putting (2-28) and (2-29) into (2-26) the phase difference $\Delta\phi$ can be calculated as:

$$\Delta\phi = \phi_{DO} - \phi_{DS} = 2 \operatorname{atan} \left[\frac{B_N}{1 - \frac{1}{2}B_N^2} \right] \quad (2-30)$$

The widest bandwidth using shunts stubs has $\theta = \lambda_o/4$ and stubs of length $\lambda_o/8$. The susceptances of the stubs is then $B_N = \pm jK_S Y_o$ where K_S is calculated using (2-30). To increase the bandwidth over an acceptable range of phase error and because the frequency response of the phase error is at a minimum at ω_o , the phase error is set to a non-zero negative amount. For the maximum allowable phase error of $\pm 2^\circ$ the values of K_S for 45° , 22.5° and 11.25° are 0.38, 0.178 and 0.082 respectively. Using these values of K_S for 22.5° and 11.25° will result in impractical characteristic impedances and therefore a smaller than optimum bandwidth may be required.

Using lumped elements the largest bandwidth again occurs when $l = \lambda/4$ and the lumped elements can be calculated using:

$$\frac{1}{\omega L Y_o} = \frac{4}{3} B_N \quad (2-31)$$

$$\frac{\omega C}{Y_o} = \frac{7}{9} B_N \quad (2-32)$$

where B_N can be calculated from (2-30) and ω is for the $\lambda/4$ spacing.

By sacrificing bandwidth it is possible to get phase shifts of greater than 45° through adjusting the spacing between the loads to other than $\lambda/4$. The spacing between the loads is adjusted so that the VSWR $\rho = 1.0$. Through substitution the design equations become:

$$\Delta\varnothing = \pi - 2 \operatorname{atan}\left[\frac{2}{B_N}\right] \quad (2-33)$$

or

$$B_N = 2 \tan\left(\frac{\Delta\varnothing}{2}\right) \quad (2-34)$$

which can be further reduced to

$$\Delta\varnothing = \pi - 2\theta \text{ or } \theta = \frac{\pi}{2} - \frac{\Delta\varnothing}{2} = \frac{2\pi l}{\lambda} \quad (2-35)$$

Finally the insertion loss at mid-band of a loaded-line phase shifter is

$$\delta_{\varnothing} = 20 \log \left[1 + \frac{4R_S Y_o}{1 + \frac{4}{K_S^2}} \right] \quad (2-36)$$

where R_S is the series resistance of the switching device and K_S is already defined.

2.2.4 High-Pass Low-Pass Phase Shifters

The high-pass low-pass phase shifter consists of series and shunt inductors and capacitors in either π or T configurations. This is a constant phase-shift device, whose major advantages are small size and large bandwidths. The most common configuration uses π or T networks connected with two SPDT switches, see Figure 2-7. Other topologies are possible and higher order π or T networks can be used for increased bandwidth if the increase in losses is acceptable.

The characteristic equations of a high-pass low-pass phase shifter can be demonstrated by choosing one of the topologies. The other topologies have the same form with some of the terms interchanged. For a low-pass T section the characteristic design equations are:

FIGURE 2-7 High-Pass Low-Pass Phase Shifter Topologies

$$S_{21} = \frac{2}{2(1 - B_N X_N) + j(B_N + 2X_N - B_N X_N^2)} \quad (2-37)$$

$$\Delta\phi = 2 \operatorname{atan} \left[\frac{B_N + 2X_N - B_N X_N^2}{2(1 - B_N X_N)} \right] \quad (2-38)$$

When the phase shifter is perfectly matched $|S_{11}| = 1$, (2-37) can be reduced to give

$$B_N = \frac{2X_N}{X_N^2 + 1} \quad (2-39)$$

which when substituted into (2-38) reduces that equation to

$$\Delta\phi = 2 \operatorname{atan} \left[\frac{2X_N}{X_N - 1} \right] \quad (2-40)$$

giving

$$X_N = \tan\left(\frac{\Delta\phi}{4}\right) \text{ and } B_N = \sin\left(\frac{\Delta\phi}{2}\right) \quad (2-41)$$

Equations (2-40) and (2-41) are then the equations used to design a high-pass low-pass phase shifter. If a π section were used instead of a T section then X_N and B_N would be exchanged in equation (2-41).

It is possible to get one octave bandwidth for a 90° bit with a phase error of 4° [49]. As mentioned previously, the bandwidth of the larger bits can be increased using higher order resonant section at the cost of increased losses.

The high-pass low-pass phase shifter is also susceptible to phase spikes due to 180° resonant sections and care must taken to avoid them. This is especially important at higher frequencies where the lumped elements may have a large distributed component.

CHAPTER 3: CIRCUIT DESIGN

The design of a one-bit superconductive phase shifter will be presented from the calculation of the initial ideal elements to the final layout and simulated results. The main goal of the design is to see what can be realized using HTS for phase shifting applications at high frequencies, specifically at Ka-band where there may be possible applications for Local Multi-point Communications Systems. The phase shifter will not be specifically designed for any given application, rather the phase shifter will be designed to demonstrate what is possible with HTS technology.

3.1 Design Goals

The initial design goals for the phase shifter are:

- A fully integrated phase shifter using HTS.
- One or more bits, beginning with the 180° bit.
- Losses of less than 1dB per bit.
- Operation at Ka-band, with the initial design goal of 30 GHz.
- As wide a bandwidth as possible while meeting other goals.
- Operation at or near 77 K.

The first design goal, of a fully integrated phase shifter using HTS is the basis of this thesis. Conventional phase shifters are usually hybrid-MIC, where the switching elements are MMICs and the phase shifting portion is conventional planar technology.

Hybrid-MIC techniques are used due to the high cost of chip area on MMIC, but hybrid techniques do lead to problems at higher frequencies when integrating the components.

HTS technology allows for the possibility of improving on conventional phase shifters in two ways, reduced losses and fully integrated fabrication. The second goal is that the

phase shifter is to have at least one bit, the 180° bit which is the most difficult to fabricate. More bits would have been added if time and chip space allowed. The third design goal is losses of less than one dB per bit. Lower losses is the major area where there is room for improvement of using HTS over conventional technology. Most reported phase shifters in the frequency band of this design have reported losses of 2-3dB per bit. The losses become very significant with a multi-bit phase shifter. The fourth design goal is that the phase shifter shall operate at Ka-band. Ka-band is a frequency range where there is little reported work with HTS phase shifters and the losses of conventional phase shifters become unacceptably high. The frequency of 30 GHz as the center frequency of the phase shifter is an initial working value, not an absolute goal. It is expected that the frequency of operation will shift down from this frequency due to parasitics and other effects as the design progresses. The fifth design goal is that the bandwidth of the phase shifter should be as large as possible. A bandwidth of 4 GHz would be sufficient to cover the entire LMCS band. The bandwidth is very dependent on the other design goals and is expected to be the most flexible. The sixth design goal is operation at or near 77 K. The temperature of operation was selected so that the phase shifter could be used with a commercial cryocoolers. The facilities at the Communications Research Centre promised potential operation to temperatures as low as 67 K by expanding the liquid nitrogen coolant into a near vacuum.

The design procedure followed was: select the basic technologies, select the phase shifter topology, create an ideal prototype network, simulate and model the lumped elements required, substitute the lumped element models into the prototype network and adjust the network to provide the required response, and finally using the geometry of the

selected lumped elements as a starting point conduct electromagnetic simulations adjusting the geometry to give the desired response.

3.2 Basic Technologies Selected

Before the initial design calculations were made some questions needed to be resolved. What HTS technologies are available and what sort of processes will they support? These questions influenced the design in many way and had to be answered even before the topology of the phase shifter was selected.

3.2.1 HTS Technology

The selection of the HTS material and process was very limited since Superconductor Technologies Inc., with a well developed commercial technology, no longer performs small lot jobs. This required the use of non-commercial superconductive technology from any partner available. The National Research Council (NRC) can fabricate and pattern HTS and their process was selected due to its availability.

The NRC process used $\text{YBa}_2\text{Cu}_3\text{O}_7$ (YBCO) on LaAl_2O_3 . The process at NRC was a single-sided process and did not include airbridges. It was believed that the airbridges could be added at the Communications Research Centre (CRC). YBCO is not the best HTS material available. This would affect the losses expected and the amount of back-off from its transition temperature that could be achieved. The process for fabrication at NRC was not specifically optimized for high T_c and low losses.

3.2.2 Microwave Transmission Line Technology

The two most common planar transmission line technologies are microstrip and coplanar waveguide. Microstrip is the most popular technology and is supported with a wide range of software packages for designing circuits. Microstrip is a two-sided technology and

requires via-holes for grounding. Since the NRC process provides YBCO on one side of the substrate, the ground plane for the microstrip line would have to be a normal metal. This would lead to increased losses in the HTS transmission line as compared to a two-sided HTS process [50].

Coplanar waveguide is a one-sided three conductor transmission line that allows for easy inclusion of series and shunt elements. At millimeter-wave frequencies, coplanar waveguide offers the potential of lower conductor and radiation losses as compared to microstrip lines [51]. Coplanar waveguide also allows for varying the dimensions of the transmission line without changing the characteristic impedance. Coplanar waveguide was selected for use in the phase shifter due to its single-sided nature and for allowing variations in the transmission line dimensions without changing the characteristic impedance.

3.3 Phase Shifter Topology

The phase shifter topology was selected with the various design goals in mind, as different topologies offer different advantages and disadvantages. The various types of phase shifters that were covered in Chapter 2 were considered for the design of the phase shifter. The advantages and disadvantages of each were considered and the High-pass Low-pass design was selected.

3.3.1 Selection of Phase Shifter Topology

The switched-line phase shifter is the simplest of the phase shifter topologies and the most frequently used. This is a time delay phase shifter and therefore gives a linear phase shift versus frequency response. The linear phase shift versus frequency response restricts the maximum possible bandwidth. The limited maximum bandwidth is the major disadvantage of a switched-line phase shifter and the reason that this design was not

selected. The switched-line phase shifter is the most conservative design and should be able to meet the other design goals.

The reflection-type phase shifter theoretically has the largest bandwidth for the 180° bit, however that is where its main advantages cease. The reflection phase shifter requires either a circulator or a coupler. Circulators are large and cannot be integrated onto a chip, violating the first design goal. Using a planar coupler such as a branch-line, rat-race or backward-wave coupler requires a very large structure and the coupler would limit the bandwidth of the phase shifter. The best possible result with a backward-wave coupler is a 35% bandwidth [52]. This topology was considered to be too large and too limited on the maximum potential bandwidth.

The loaded line phase shifter cannot offer both large phase shifts and large bandwidths simultaneously. For large bandwidths the phase shift is limited to less than 45° . For a multi-bit phase shifter the loaded-line topology might be considered for the smaller phase bits. As this thesis covers the design of a 180° bit phase shifter, this topology was unacceptable.

Finally, the high-pass low-pass phase shifter offers the possibility of large bandwidth, true phase shift, low losses and small size. The bandwidth of the high-pass low-pass design is smallest for the 180° bit, but can be increased by a higher order T or π network. The losses, compared to the other designs depend on the lumped elements and are potentially the smallest. Further, the high-pass low-pass topology is potentially the smallest topology, which could allow multiple bits on the same chip. This topology was selected for the 180° bit.

3.3.2 High-Pass Low-Pass Design Equations

From Chapter 2 the design equations for a high-pass low-pass phase shifter using T-networks, Equations (2-40) and (2-41), which assume a perfect match at the centre frequency, are reproduced here.

$$\Delta\phi = 2 \operatorname{atan} \left[\frac{2X_N}{X_N - 1} \right] \quad (3-1)$$

$$X_N = \tan \left(\frac{\Delta\phi}{4} \right) \text{ and } B_N = \sin \left(\frac{\Delta\phi}{2} \right) \quad (3-2)$$

Using π -networks instead of T-networks Equation (3-2) becomes:

$$X_N = \sin \left(\frac{\Delta\phi}{2} \right) \text{ and } B_N = \tan \left(\frac{\Delta\phi}{4} \right) \quad (3-3)$$

The layout of a three element T-network for the high-pass and low-pass case is shown in Figure 3-1. The ideal lumped elements, C_H and L_H , are for the high-pass network and elements C_L and L_L are for the low-pass network. The lowest order T or π -networks are three element networks. Three element networks were selected because they are the simplest networks and have the lowest losses. Higher-order networks could be used for increased bandwidth at the cost of increased losses. Low losses are a more important goal of this thesis than large bandwidth. Further work could investigate higher order networks for broader bandwidths if warranted.

FIGURE 3-1 Topology of Three Element T-Networks

Using Equation (3-2) the B_N and X_N values for the four largest bits were calculated for use with a T-network. From these values the ideal components for the high-pass and low-pass networks were calculated, including renormalization to a 50 Ω system as given by the following equations:

$$\text{Low-Pass } C_L = \frac{B_N}{2\pi\omega Z_o} \text{ and } L_L = \frac{Z_o X_N}{2\pi\omega} \quad (3-4)$$

$$\text{High-Pass } C_H = \frac{1}{2\pi\omega Z_o X_N} \text{ and } L_H = \frac{Z_o}{2\pi\omega B_N} \quad (3-5)$$

These values are listed in Table 3-1. These ideal components are the basis of the phase shifter design. The desired phase shift is divided between the high-pass and low-pass networks with each network providing half of the phase shift, ie. $\pm 90^\circ$ for the 180° bit. The actual phase shifter has the ideal components replaced with CPW lumped elements with their associated parasitics. Therefore the actual lumped elements differ significantly from these ideal values as the parasitics themselves form a portion of the T-network.

TABLE 3-1 Element Values for HP-LP T-network Phase Shifter

Phase Shift	T-network Section	Normalized X_N or B_N	Ideal Element Value
180°	Low-pass	$B_N = 1$	$C_L = 0.106$ pf
		$X_N = 1$	$L_L = 0.265$ nH
	High-pass	$B_N = 1$	$L_H = 0.265$ nH
		$X_N = 1$	$C_H = 0.106$ pf
90°	Low-pass	$B_N = 0.414$	$C_L = 0.075$ pf
		$X_N = 0.707$	$L_L = 0.110$ nH
	High-pass	$B_N = 0.414$	$L_H = 0.375$ nH
		$X_N = 0.707$	$C_H = 0.256$ pf

TABLE 3-1 Element Values for HP-LP T-network Phase Shifter

Phase Shift	T-network Section	Normalized X_N or B_N	Ideal Element Value
45°	Low-pass	$B_N = 0.382$	$C_L = 0.041$ pf
		$X_N = 0.199$	$L_L = 0.053$ nH
	High-pass	$B_N = 0.382$	$L_H = 0.694$ nH
		$X_N = 0.199$	$C_H = 0.533$ pf
22.5°	Low-pass	$B_N = 0.195$	$C_L = 0.021$ pf
		$X_N = 0.099$	$L_L = 0.026$ nH
	High-pass	$B_N = 0.195$	$L_H = 1.360$ nH
		$X_N = 0.099$	$C_H = 1.077$ pf

Table 3-1 shows, especially for the 45° and 22.5° bits, the calculated ideal lumped element values become very small for the low-pass T-network and become increasingly large for the high-pass T-network as the phase shift is reduced. It may be possible to fabricate the large lumped elements needed for the high-pass T-networks. However the required values for the low-pass networks are of the same magnitude as the parasitics found in lumped elements at Ka-band. The small lumped elements for the low-pass networks would be very difficult to design and would be very susceptible to process variation. It would not be suggested to attempt to fabricate the 45° and 22.5° bits using the high-pass low-pass technique. A better topology for the smallest two bits would have been required but it was decided to eliminate the 45° and 22.5° bits from the phase shifter.

In contrast, the 180° bit offers some excellent advantages, the lumped element values for the high-pass and low-pass T-networks are identical and of reasonable magnitude for fabrication at Ka-band. That the lumped elements are identical in both of the required T-networks offers the possibility of simpler design work as ideally the same lumped ele-

ments could be used in both networks. However the parasitics associated with actual lumped elements precluded this possibility.

Using the calculated ideal lumped element values, it was possible to calculate the maximum bandwidth of a three element T-network for various phase shifts. The maximum bandwidth was calculated specifically for operation at a centre frequency of 30 GHz. The calculation of the bandwidth was accomplished by creating T-networks for the high-pass and low-pass cases respectively using the ideal lumped element values listed in Table 3-1. The networks were then simulated separately and the phase difference between the calculated values of S_{21} were plotted. The phase differences for all four of the bits initially considered are shown in Figure 3-2.

FIGURE 3-2 Maximum Bandwidth of High-Pass Low-Pass Phase Shifter

The bandwidth for the various bits depends on the acceptable phase error. For this phase shifter design a phase error of 5.5% shall be considered acceptable. This corresponds to a phase of $180^\circ \pm 10^\circ$ for the largest bit. The bandwidths of the various bits assuming a maximum phase error of 5.5% are listed in Table 3-2.

TABLE 3-2 Bandwidths of High-Pass Low-Pass Phase Bits using Ideal Elements

Phase Bit	Phase Error (5.5%)	Upper Limit (GHz)	Lower Limit (GHz)	Bandwidth (GHz)
180°	10°	37.0	24.3	12.7
90°	5°	40.3	22.3	18.0
45°	2.5°	41.6	21.6	20.0
22.5°	1.2°	41.6	21.6	20.0

As can be noted from Figure 3-2 the phase difference versus frequency response is a minimum at the centre frequency and increases away from this frequency. The bandwidth can be increased by setting the phase at the centre frequency to the desired phase minus the maximum allowable phase error. This spreads the phase error across the entire acceptable range allowing more of the phase difference curve into the acceptable band. While possible, this was not incorporated into the design of the phase shifter in this thesis.

3.3.3 Ideal Phase Shifter Topology

There remains the selection of the final topology for the phase shifter. While a high-pass low-pass phase shifter topology was selected, the selection of π or T-networks remains. Since there is no difference in the theoretical performance of the phase shifter depending on the network other criteria must be used.

For this design, the deciding factor was the dc biasing of the switching element. The design of the superconductive switch will be covered later but it was originally based

on a series coplanar waveguide superconductive switch designed at McMaster University [53]. The switching element is turned on and off with a dc current passed through the center conductor of the coplanar waveguide. As the switch was being designed for this application it was decided that the dc biasing network could include the entire phase shifter, ideally compacting the design.

The basic concept was to place the switching elements as close to a T on the two branches as possible. The switching elements would place an open circuit on one of the branches near to the plane of the T, reflecting all of the energy down the other branch. This required that one of the elements have a dc current flowing through it while the other did not. To assure this, a dc ground was to be placed between the two switching elements either at the T or down the trunk path. Such a dc ground can be made very broad-band to exploit the broadband characteristics of the switching element.

With the dc ground positioned between the two branches, the dc feed for each switching element must be down their respective branches. To avoid the need for a dc blocking capacitor in either branch required that there be no dc path to ground in either branch. This required the use of T-networks. See Figure 3-3 for this initial topology.

3.4 Coplanar Waveguide Lumped Elements

The ideal topology for the phase shifter was presented in Figure 3-3. The next step was to replace the ideal components with actual lumped elements. The first step to replacing the ideal components with ideal lumped elements was to investigate the lumped elements themselves. This investigation was necessary for two main reasons; to ensure that the component values required could be achieved and to investigate the associated parasitics. Knowledge of the parasitics is especially important at high frequencies as the lumped ele-

FIGURE 3-3 Initial Phase Shifter Topology Including DC Biasing

ment structure could become self-resonant at the frequency of interest and the parasitics can overwhelm the main component of the lumped element.

3.4.1 Simulation of Coplanar Waveguide Lumped Elements

Coplanar waveguide is currently not as popular a technology as microstrip. There are not large design libraries of coplanar waveguide components that have been developed. As the number of fabrication runs would be limited and the lead time for each run was significant the best solution was to simulate the lumped elements and fit them to a model.

Large analytical models of coplanar waveguide components are not common in simulation programs such as Libra™. Some simple component models are available but not for lumped elements. The lack of analytical models meant that electromagnetic simu-

lations of the lumped elements were required. For coplanar waveguide the two electromagnetic packages that offered the best performance are Coplan™ and Sonnet™.

Coplan™ uses a quasi-static 3-D finite difference engine to calculate three dimensional coplanar structures [54]. The simulation is confined in a bounding box where the top and bottom walls and all walls without ports are perfect electric walls, and all the walls with ports are perfect magnetic walls. This 3-D package thus allows for the simulation of finite metal thickness and airbridges, which are essential to coplanar waveguide discontinuities.

Coplan™ was specifically designed for coplanar waveguide as an add-on to Libra™, a common microwave simulator. The program is parameter driven, where the geometry of the coplanar elements are determined by entering predetermined parameters, therefore allowing for easy optimization. In addition Coplan™ is seamlessly integrated into Libra™, allowing for direct comparisons between the coplanar waveguide components and other ideal networks. For this reason Coplan™ was selected for the initial investigation of the coplanar waveguide lumped elements. Coplan™ does suffer from one problem with respect to superconductive materials, there is no allowance for a complex conductivity to account for the kinetic inductance effect found in superconductors. Therefore all simulations using Coplan™ either assumed lossless or low-loss metals. This allows for the major design to be completed and then fine tuned with other software programs.

Sonnet™ is a stand-alone electromagnetic simulator which calculates S-parameters for arbitrary 3-D planar structures. Sonnet™ uses a “full wave” analysis where all coupling mechanisms are included in the simulation. The “full wave” analysis includes

dispersion, stray coupling discontinuities, surface waves, moding, metallization loss, dielectric loss and radiation loss [55]. Sonnet™ is a full three dimensional analysis in that both 2-D and 3-D currents are included in the analysis. As Sonnet™ allows only planar, multilayer structures it uses the Fast Fourier Transform to calculate the coupling between layers. Sonnet™ cannot simulate the effects of finite metal thickness. The main engine in Sonnet™ solves the 3-D planar circuits by solving for the current distribution in the circuit metallization using the Method of Moments.

Sonnet™ is based on a graphical interface, where the geometry being simulated must be manually entered through a graphics tool. The graphical interface is Sonnet™'s largest strength and weakness, the graphical interface allows for novel geometries that would not otherwise be possible to simulate, but becomes very tedious for very similar components. The version of Sonnet™ used at the beginning of this thesis did not have any allowance for optimization, however a later version did add that capability. Sonnet™ was used for simulating various novel geometries, and for final estimates of performance as Sonnet™ allows complex surface impedances.

Coplan™ was first tested to find approximate design rules on the accuracy of the simulations. While not possible to compare the results generated from Coplan™ with measured data it was possible to investigate the time-accuracy trade-off to some extent. A single spiral inductor was simulated. The maximum dimensions of the simulation were 250 μm by 250 μm and the smallest dimension was 5 μm . The spiral inductor was simulated with discretizations of 2.5 μm , 1.25 μm and 0.665 μm . For each discretization, the maximum iteration error allowed was varied between $1\text{e-}4$ and $1\text{e-}5$ to determine the effect of the iteration error on the results. The time required to complete the simulations and the

difference between the simulations were compared. The simulations with the smallest discretization were assumed to be the most accurate. The results of this experiment are covered in Table 3-3. The table shows that for a discretization of $1.25\ \mu\text{m}$, 4 cells to the

TABLE 3-3 Accuracy and Time for Coplan™ Simulations

Experiment	Iteration Error	Effect	Discretization	Effect Relative to $0.665\ \mu\text{m}$	Time
Test 1	$1\text{e-}4$	Not Noticeable	$2.5\ \mu\text{m}$	3 dB diff.	< 1min
Test 2	$1\text{e-}5$		$2.5\ \mu\text{m}$	3 dB diff	< 1min
Test 3	$1\text{e-}4$	Not Noticeable	$1.25\ \mu\text{m}$	1 dB diff.	~ 30 min
Test 4	$1\text{e-}5$		$1.25\ \mu\text{m}$	1 dB diff.	~ 30 min
Test 5	$1\text{e-}4$	Not Noticeable	$0.665\ \mu\text{m}$	Not applicable	4 hours +
Test 6	$1\text{e-}5$		$0.665\ \mu\text{m}$	Not applicable	4 hours +

smallest dimension, the simulations took approximately one-half hour. The corresponding error relative to the simulations with the smallest discretization was only 1 dB in $|S_{11}|$. Removing the error by reducing the discretization to $0.665\ \mu\text{m}$ increases the simulation time to more than four hours for the one component. A 1dB error was considered acceptable for a reasonable simulation time. Therefore there should be at least four discretization cells to the smallest dimension in each of the simulations.

For a guaranteed accuracy of $\pm 1\%$ Coplan™ requires that the discretization size be less than or equal to the smallest dimension divided by ten and that the iteration error be $1\text{e-}5$ or less. That accuracy would have a discretization of $0.5\ \mu\text{m}$ in the previous example. A $0.5\ \mu\text{m}$ discretization is smaller than all of the discretizations tested and would take longer to complete than the $0.665\ \mu\text{m}$ discretization simulation.

For most electromagnetic simulations the time required to complete a simulation is proportional to the number of subsections cubed, where the number of subsections is determined by the discretization size. Doubling of the circuit complexity can result in an increase in the required solution time by an order of magnitude or more. In addition, as the number of subsections is increased, the matrix size becomes very large and can become larger than the real memory available for simulation. Exceeding the available real memory leads to drastically increased simulation times, easily taking weeks to complete. It is therefore necessary to balance simulation accuracy with the time required to complete a simulation. As previously noted for CoplanTM, four divisions to the smallest dimension was the best compromise, but that value may vary depending on the time required for a specific simulation.

3.4.2 Coplanar Waveguide Lumped Element Models and Simulated Fits

As mentioned previously, it was expected that the CPW lumped-elements at Ka-band would have problems with self-resonance and large parasitics. It was necessary to simulate various lumped inductors and capacitors to ensure that the necessary components could be fabricated. While simulation of the lumped elements was necessary it was equally important to fit those simulations to models such that the parasitics could be incorporated into the phase shifter design. If the parasitics were ignored then there is very little possibility of the design working properly.

The first component to be designed was the 0.106 pf capacitor required for the 180° bit. The coplanar waveguide interdigital capacitor can be described by a few key parameters. These parameters are the width of the fingers WF , the spacing between the fingers SF , the length of the fingers LF , the number of fingers NF , the distance between the

edge of the capacitor and the ground plane S and the distance between the start of the capacitor and the ground plane G . Figure 3-4 shows an example of the CPW interdigital capacitor (IDC) with the dimensions labelled.

FIGURE 3-4 Layout of CPW Interdigital Capacitor

As a first approximation of the required dimensions it was assumed that the expressions from Ladbroke [56], derived for microstrip devices would be acceptable. From the figure on page 42 of Ladbroke for finger width and spacing of $10\text{ }\mu\text{m}$, the capacitance per unit area is 250 pf/cm^2 . For a 0.106 pf capacitor this requires an area of $4.24 \times 10^{-4}\text{ cm}^2$. For a square capacitor, this leads to 10 fingers with a length of $210\text{ }\mu\text{m}$ each. This capacitor was simulated as a series element with 50Ω source and load impedances using Coplan. The results of the simulation are shown in Figure 3-5. The ideal response of a series capacitor lies on the unit circle ($\bar{R} = 1$). The CPW interdigital capacitor differs quite significantly from the ideal response. As any size of ideal capacitor will remain on the unit circle, the difference can only be explained in terms of parasitics. The interdigital capacitor must be modeled to extract the desired capacitance and to discover the unwanted parasitics.

FIGURE 3-5 Simulated Results of Initial 0.106 pf Capacitor

The modeling began with the interdigital capacitors (IDCs). The simplest model of an interdigital capacitor is that of a π -network of capacitors. The center series capacitor is the desired capacitance and the shunt capacitors to ground are parasitics. The π -model is shown in Figure 3-6 with other more complex models. The π -model only accounts for the

FIGURE 3-6 Interdigital Capacitor Models

main capacitances and doesn't take into account any losses, inductances in the fingers of the interdigital capacitor or distributed effects. A more complete model, is given by Ladbroke on page 43 of his book. The Ladbroke model is similar to the π -model except the main series capacitance is replaced by a series combination of the main capacitance and

parasitic inductance and resistance. The most complex model adds series transmission lines to the Ladbroke model to account for distributed effects in the interdigital capacitor. The distributed effects are important at higher frequencies due to the small capacitance per unit area found in interdigital capacitors. To achieve the necessary capacitance an area large with respect to the wavelength may be required.

The fits for the 0.1 pf capacitor for the Ladbroke model and the model including transmission lines can be found in Figure 3-7 and Figure 3-8. The initial 0.106 pf capacitor

FIGURE 3-7 Fit of Ladbroke Model

whose simulated results can be seen in Figure 3-5 was the capacitor to which the models were fit. Comparing the simulated results to the models demonstrate that the distributed effects are essential for achieving a good match. The Ladbroke model, without the transmission line segments, was the correct shape but required rotation around the Smith Chart for a proper fit. The model that included the transmission line segments resulted in a very

FIGURE 3-8 Fit of Model Including Transmission Lines

good fit. The model values used to achieve the fit were $C = 0.14$ pf, $C_s = 0.06$ pf, $L = 0.08$ nH, $R = 1 \Omega$ and $E = 8^\circ$ at 30 GHz. From examining the model values the major model components are the main capacitance C , the shunt capacitances C_s , and the electrical lengths of the transmission line segments E . The parasitic inductance and resistance were removed from the model due to their small size. Removing the inductor and resistor lead to the final model used for the selection of the capacitors used in the phase shifter design. Figure 3-9 shows the final capacitor model.

FIGURE 3-9 Final Capacitor Model

After the model was selected further work was required in designing the 0.106 pF capacitor to be used for 180° bit. The initial fits to the Transmission Line model showed that the main capacitance was overestimated. Testing different geometries was necessary to achieve the desired capacitance.

To simplify fitting of the final model to the simulated results, it was decided to investigate the low frequency H_{11} measurements. A smaller capacitor was investigated as the initial attempt resulted in too large of a capacitance. The new interdigital capacitor had 8 fingers with a length of 175 μm . The smaller capacitor was simulated at low frequency and the capacitance calculated according to (3-6).

$$C_T = \frac{-1}{\text{Im}\{H_{11}\}2\pi f} \quad (3-6)$$

The capacitance C_T includes the main capacitance in addition to one of the shunt capacitances as seen in Figure 3-10.

FIGURE 3-10 Low Frequency Model for H_{11} Simulation of Interdigital Capacitors

The capacitor was simulated at both low and high frequencies using Coplan. The results were fit to both the final capacitor model and the low frequency model through tuning and optimization of the model parameters in Libra. The final capacitor model parame-

ters were $C = 0.16$ pf, $C_s = 0.05$ pf, $L = 0.06$ nH and $E = 8^\circ$ with $Z_0 = 50 \Omega$ and at 30 GHz.

The total capacitance from the low frequency model, C_T , equals $C + C_s$. The low frequency measurements should then provide a total capacitance of $C_T \approx 0.21$ pf. The results of the low frequency measurements are available in Table 3-4. The calculated values of C_T

TABLE 3-4 Low Frequency H_{11} Measurements

Frequency (GHz)	$\text{Im}\{Y_{11}\}$	C_T (pf)
0.01	1.28e-5	0.205
0.05	6.43e-5	0.205
0.10	1.29e-4	0.205

are 0.205 pf at all frequencies measured. That C_T is so close to $C + C_s$ confirms that the total capacitance equals the desired capacitance plus the parasitic capacitance. The difference between the values allowed for a quick check on the accuracy of the model fit.

Several different interdigital capacitor geometries were simulated and modeled in order to discover a geometry that would provide a capacitor with a main capacitance of 0.106pf. The modeled results are recorded in Table 3-5. The required capacitance for the

TABLE 3-5 Interdigital Capacitor Dimensions and Corresponding Capacitance

Physical Dimensions		Model Capacitances		Low Frequency Error Check			
NF	LF (μm)	C (pf)	C_s (pf)	f (GHz)	$\text{Im}\{H_{11}\}$	C_T (pf)	Error $C_T - (C + C_s)$
8	175	0.16	0.05	0.1	-7772	0.205	-0.005
7	175	0.157	0.051	0.1	-8354	0.191	-0.017
6	175	0.118	0.042	0.1	-10123	0.157	-0.003
5	175	0.109	0.042	0.1	-11112	0.143	-0.008

TABLE 3-5 Interdigital Capacitor Dimensions and Corresponding Capacitance

Physical Dimensions		Model Capacitances		Low Frequency Error Check			
NF	LF (μm)	C (pf)	C_s (pf)	f (GHz)	$\text{Im}\{H_{11}\}$	C_T (pf)	Error $C_T-(C+C_s)$
4	175	0.069	0.027	0.1	-14669	0.109	0.013
6	200	0.143	0.045	0.1	-9152	0.174	-0.014
6*	150	0.100	0.040	0.1	-11326	0.141	0.001
6	125	0.077	0.034	0.1	-12848	0.107	0.013
4	160	0.063	0.030	0.1	-15422	0.103	0.010
4	155	0.061	0.029	0.1	-15756	0.101	0.011
4	150	0.060	0.027	0.1	-16114	0.099	0.012
5	165	0.100	0.042	0.1	-11601	0.137	-0.005

* Highlighted row is for capacitor used in phase shifter

180° bit high-pass low-pass phase shifter can be realized by a capacitor with six fingers that are 150 μm long. This capacitor was selected due to its small parasitics.

After showing that it would be possible to fabricate a real interdigital capacitor for the 180° bit it was necessary to ensure that the inductors could be fabricated. With an inductance of 0.265 nH required for the 180° bit, a spiral inductor was selected to realize the required inductance. Large spiral inductors with many turns may suffer from self-resonance limiting the maximum inductance for a given frequency of operation.

The layout of the spiral inductors were controlled by several key parameters. These parameters included the number of turns N, the width of the center track WT, the spacing between the tracks ST, the inner diameter of the spiral inductor in both directions, I_DIA1 and I_DIA2, and the spacing between the outside of the spiral inductor and the ground plane S. The layout of a CPW spiral inductor is shown in Figure 3-11 with the relevant dimensions labelled. The initial design decisions for the spiral inductor were the use of 1.5

FIGURE 3-11 Layout of CPW Spiral Inductor

turns and a square topology. The number of turns was set to 1.5 to allow for a single air-bridge and for a straight-in straight-out design. A square spiral inductor topology is the most space efficient shape.

The simplest model of a spiral inductor is a π -network with the desired inductance and shunt parasitic capacitors. Simulations of H_{11} at low frequencies gave a good estimate of the inductance. The model used for these low frequency measurements is shown in Figure 3-12. At low frequencies the inductor approaches a short circuit and the shunt capaci-

FIGURE 3-12 Model for H_{11} Measurements of Spiral Inductors

tors an open. With one of the parasitic capacitors shunted across ground and the other connected in parallel with the inductance, the H_{11} measurement is almost completely determined by the desired inductance. The desired inductance, L , is determined by:

$$L = \frac{\text{Im}\{H_{11}\}}{2\pi f} \quad (3-7)$$

Using these low frequency measurements it is possible to size the desired inductance before matching the simulated results to more complicated models.

Several different geometries for the spiral inductor were tested and the results are displayed in Table 3-6. In all instances the spiral inductor maintains a square geometry so

TABLE 3-6 Low Frequency Sizing of Spiral Inductors

Physical Dimension (μm)			Frequency (GHz)	Electrical Parameters	
Inner Dia.	W	S		$\text{Im}\{H_{11}\}$	L (nH)
50	20	10	0.1	0.1933	0.308
40	20	10	0.1	0.1749	0.278
35*	20	10	0.1	0.1667	0.265
30	20	10	0.1	0.1590	0.253
35	20	20	0.1	0.1845	0.294
30	20	20	0.1	0.1765	0.281
25	20	20	0.1	0.1689	0.269
20	20	20	0.1	0.1615	0.257

* Highlighted rows are inductors with required value of inductance.

only one inner diameter is provided. The results of the low frequency simulations show that it should be possible to fabricate the desired 0.265 nH inductors required for the 180° bit.

The low frequency tests show that the spiral inductors are capable of meeting the size requirements for the inductance but do not provide estimates of the parasitics or other possible problems at high frequencies. High frequency problems and parasitics must be covered by modeling the spiral inductor. Three models of increasing complexity were used.

The first model, the π model, is shown in Figure 3-13. In the π model the desired

FIGURE 3-13 π Spiral Inductor Model

inductance, L , is shunted by a parasitic capacitance, C , with parasitic capacitances to ground, C_s . The shunt capacitances, C_s , are assumed to be identical but this assumption is not necessarily valid. The π model gives an approximate fit but large errors may be noted in Figure 3-14.

A more complete model is given in Ladbroke on page 37, shown in Figure 3-15, which adds series resistance, R , to the desired inductance and allows for dissimilar shunt capacitances to ground, C_{s1} and C_{s2} . This model was used for further design of the phase shifter as it provided acceptable results with only moderate complexity. The fit of the Ladbroke spiral inductor model is shown in Figure 3-16.

The final model, the Complex spiral inductor model, from CoplanTM, is shown in Figure 3-17. The complex spiral inductor model divides the desired inductance into two unequal portions, L and L_2 . These inductances are connected in series with the unequal capacitances shunting them to ground, C_{s1} , C_{s2} and C_{s3} , one at each of the nodes. The series resistance is divided into two equal portions, R , associated with the portions of series inductance. Finally there is a capacitance shunted across both of the inductances and

FIGURE 3-14 Fit of π Spiral Inductor Model

FIGURE 3-15 Ladbroke Spiral Inductor Model [56]

their associated resistances. This model provides a near perfect match to the CPW spiral inductor as can be seen in Figure 3-18. While the complex spiral inductor model provided a near perfect match to simulated CPW spiral inductor, it was too complex for practical use in circuit design.

FIGURE 3-16 Fit of Ladbroke Spiral Inductor Model

FIGURE 3-17 Complex Spiral Inductor Model [54]

The Ladbroke Spiral Inductor model was chosen for modeling of the CPW spiral inductors due to its relative simplicity and its acceptable match to simulated results. Those spiral inductors that were promising from the low frequency tests were fitted to the medium spiral inductor model for design use. The model data for various CPW spiral inductors are recorded in Table 3-7.

FIGURE 3-18 Fit of Complex Spiral Inductor Model

TABLE 3-7 Medium Spiral Inductor Model Data

Physical Dimensions (μm)			Model Data				
Inner Dia	W	S	L (nH)	C_{s1} (pf)	C_{s2} (pf)	C (pf)	R (Ω)
35	20	10	0.250	0.036	0.048	8.5e-9	0.50
25	20	20	0.243	0.035	0.049	1.3e-7	0.91
40*	20	10	0.262	0.038	0.050	3.0e-7	0.49
30	20	20	0.254	0.037	0.052	8.6e-11	0.92
35	20	20	0.265	0.039	0.054	1.6e-5	0.95

* Highlighted row is for inductor used in phase shifter

In all cases the capacitance shunted across the inductor is a very small and it was neglected in further design work. In addition the resistances were all very small and were neglected. From the preceding work it has been shown that suitable coplanar waveguide

lumped elements could be fabricated for the 180° bit. The inductor selected was a 1.5 turn square inductor with an inner diameter of $40\text{ }\mu\text{m}$, a track width of $20\text{ }\mu\text{m}$ and a track spacing of $10\text{ }\mu\text{m}$. This inductor was selected due to its small parasitics.

3.4.3 Reducing Coplanar Waveguide Lumped Element Parasitics

Simulation of CPW lumped elements showed that there are large parasitics related to these elements. There was an initial attempt at replacing the ideal components from the prototype networks directly with coplanar waveguide lumped elements. Direct substitution of the lumped elements was a dismal failure as the parasitics played a significant role in the lumped elements performance. The failure of direct substitution led to the modeling of the lumped elements covered in Section 3.4.2. The failure of direct substitution also led to attempts at reducing the parasitics in the lumped elements.

Attempts to reduce the parasitics in the CPW lumped elements could not affect the desired capacitance or inductance. Reducing the parasitics was possible in coplanar waveguide lumped elements by adjusting the spacing to the ground plane around the lumped element. Increasing the distance between the lumped element and the ground plane reduced the parasitic shunt capacitance while having little other affect on the lumped element. The layouts of the coplanar waveguide interdigital capacitor and the spiral inductor are shown in Figures 3-4 and 3-11 respectively, reproduced here in Figure 3-19. These layouts are for CoplanTM which was used for the initial simulation and modeling of the CPW lumped elements. The vertical separation between the interdigital capacitor and the ground plane is controlled by the parameter S and the horizontal separation is controlled by the parameter G. For the CPW spiral inductor the parameter S controls both of these

FIGURE 3-19 Layouts of CPW Interdigital Capacitor and Spiral Inductor

separations. Therefore the interdigital capacitor had two degrees of freedom for control the ground plane separation while the spiral inductor had only one.

To determine the effect of these values on the performance of the CPW lumped elements it was decided to run multiple simulations of the both an interdigital capacitor and a spiral inductor where the only variables allowed to change were S and G . The results were then examined to find the optimum values of S and G .

The results of these simulated tests for a CPW interdigital capacitor are shown in Figure 3-20. The simulated results shown are for increasing S and G simultaneously. Increasing S moved the simulated results towards the center of the Smith Chart. The benefit of increasing S decreases as S becomes large. Increasing G increased the distributed component of the interdigital capacitor. The increased distributed component is caused by the addition of a section of line equal to G to the interdigital capacitor.

From these findings it was decided to keep G as small as possible in order to have less of a distributed component in the CPW IDC. The vertical separation, S , was made as large as possible while taking into account chip area concerns.

FIGURE 3-20 Simulated Results of Varying Ground Plane Spacing for a CPW Interdigital Capacitor

For the CPW spiral inductor the decision was not so clear cut. Using CoplanTM, a parameter driven software package, it was not possible to separate the horizontal and vertical ground plane separation from one another. As the vertical separation is increased so does the horizontal separation. Increased horizontal separation adds to the distributed effects on the CPW spiral inductor because an additional length of line is added to both sides of the spiral inductor. After testing, a value of 30 μm was selected as the best compromise for reduced shunt capacitance to ground while keeping the additional lengths of line small.

Note when it was decided to move from CoplanTM to SonnetTM at a later point in the design process, it would have been possible to increase the vertical ground plane separation while keeping the horizontal ground plane separation constant. At that time the

design had progressed to a point where such changes, while possibly improving performance, would have require too much additional time for the potential performance gains.

3.5 Design of High-Pass and Low-Pass Sections

With enough evidence to show that it would be possible to realize the necessary coplanar waveguide lumped elements and that accurate models of those lumped elements had been assembled, the next step in the design process was replacing the ideal elements in the high-pass and low-pass prototype networks with actual coplanar waveguide lumped elements.

3.5.1 Substitution into Prototype Networks

The prototype networks for the 180° bit high-pass and low-pass sections shown in Figure 3-21 are ideal networks. The ideal capacitors and inductors must be replaced with models

FIGURE 3-21 Prototype 180° Bit T-Networks

of the CPW lumped elements. Direct substitution of the required CPW lumped element

models into the prototype network will not provide the same network as the prototype network. Figure 3-22 shows the direct substitution of the lumped element models into the prototype networks. The parasitic components must be incorporated into the design of the high-pass and low-pass sections in order to obtain similar responses to the ideal networks.

FIGURE 3-22 Substitution of CPW Lumped Element Models in Prototype Network

To incorporate the parasitics into the design of the high-pass and low-pass networks it was necessary to adjust at least one of the element values to include the excess shunt capacitances. As T-networks were used for the high-pass and low-pass sections of the phase shifter modifying only the shunt elements would minimize the components affected.

For the high-pass T-network changing only one of the CPW lumped elements required varying the shunt inductor to ground. Using models of the CPW lumped elements the network was simulated and optimized to provide a good input and output match to 50Ω . The prototype T-networks act as 50Ω to 50Ω transformers with a phase difference

between the two T-networks of 180° . By optimizing the high-pass network to act as a $50\ \Omega$ to $50\ \Omega$ transformer while not requiring exactly the same performance as the prototype high-pass network, it was believed that the performance of the complete phase shifter would be similar to the ideal performance. The only component allowed to change independently was the shunt inductor to ground. The corresponding parasitic shunt capacitance of the spiral inductor was varied in proportion to the change in the shunt inductor. The results of the optimization show a reasonable correspondence to ideal prototype network. The lumped element network has the same form as the prototype network but is rotated around the Smith Chart. Figure 3-23 shows the model of the high-pass network and the simulated results. As long as low-pass network differs from its prototype network in the same manner as the high-pass network then the required phase shift can still result. The phase difference between the high-pass and low-pass networks is important, not the exact performance of either of the T-networks.

The optimized results are shown in Figure 3-23. The shunt inductance needed to achieve the optimized results is only $0.14\ \text{nH}$. Such a small inductance is too small for a spiral inductor. The inductance would be better realized through a short section of high impedance line. Using a high impedance line also reduces or eliminates the parasitic shunt capacitance of the inductor.

The low-pass T-network was examined after the high-pass network was optimized for good performance. In the low-pass network the shunt capacitance to ground was the desired component to be changed. As the model of the CPW spiral inductor allows for two different parasitic shunt capacitances there are several combinations of the orientation of the spiral inductors. Examining these combinations, the best orientation of the spiral

FIGURE 3-23 Model and Simulated Results of High-Pass Network

inductors was such that the larger parasitic capacitances are on the same node as the desired shunt capacitance. This allowed the larger parasitic capacitances to be absorbed into the desired capacitance.

The model of the low-pass network was simulated and optimized to give a good 50Ω to 50Ω transformer by varying the shunt capacitance to ground. The simulated results of the model of the low-pass network were similar to the low-pass prototype network but again were rotated around the Smith Chart. The rotation was in the same direction as for the high-pass network. The model of the low-pass network and its simulated results are shown in Figure 3-24.

FIGURE 3-24 Model and Simulated Results of Low-Pass Network

The shunt capacitance required for the performance of the low-pass network was reduced from 0.106 pf in the prototype network to 0.015 pf in the model. Such a low capacitance is too small to be realized with an interdigital capacitor. Instead, a high impedance open circuit stub was used for this shunt capacitor.

The difference in the simulated angles of S_{21} between the models of the high-pass and low-pass T-networks was 187.1°. The phase difference was sufficiently close to the desired phase difference of 180° that the models of the CPW lumped elements had completed their purpose. The design was continued using electromagnetic simulations.

3.5.2 Electromagnetic Simulation and Design of T-Networks

From the previous work with the models for CPW lumped elements, circuits were designed that came close to satisfying the goals for the 180° bit high-pass and low-pass sections of the phase shifter. The high-pass network consisted of two identical series capacitors with a high impedance shunt short circuit stub separating them. The interdigital capacitors that fit the modeled elements had 6 fingers that were $10\text{ }\mu\text{m}$ wide, were separated by $10\text{ }\mu\text{m}$ and were $150\text{ }\mu\text{m}$ long. The low-pass network consisted of two identical series inductors that were mirror images of one another, separated by a high impedance open circuit stub. The spiral inductors were square inductors with 1.5 turns, track widths of $20\text{ }\mu\text{m}$, spacing between the tracks of $10\text{ }\mu\text{m}$ and an inner diameter of $40\text{ }\mu\text{m}$.

With this information the design was continued using electromagnetic simulations of the two networks. At this point a mistake was made in the layout of the low-pass T-network; the two spiral inductors were layed out in the same direction, instead of as mirror images of each other. This error was not noticed until the final mask had been fabricated, too late for correction. The performance of the low-pass T-network would likely have been improved if the spiral inductors had been layed out properly.

Electromagnetic simulations of the high-pass and low-pass networks using Coplan™ were performed and the shunt stubs approximately sized. The schematics and simulated results of the high-pass and low-pass networks, in addition to the ideal results from the prototype networks, are presented in Figure 3-25 and 3-26. The simulated phase difference between the two networks at 30 GHz is 182.3° , which is acceptable.

Limitations in the Coplan™ software were encountered with these simulations. The elements of a network in Coplan™ are simulated individually and must adhere to

FIGURE 3-25 Schematic and Simulated Results of High-Pass Network Using

Coplan™

strict rules within those elements. The required open circuit shunt stub for the low-pass network needed to be shorter than Coplan™ would allow. Through creative use of the software the previous results were obtained but they incorrectly modeled the effect of the

FIGURE 3-26 Schematic and Simulated Results of Low-Pass Network Using Coplan™

expected airbridges. In addition, there is assumed to be no coupling between adjacent but discrete components in Coplan™. By investigating the geometry in the area of the CPW Tee, this assumption could not be considered valid. For these reasons it was decided to continue further electromagnetic simulations using Sonnet™ instead of Coplan™.

The geometries of the high-pass and low-pass T-networks simulated using Coplan™ were laid out using the automatic layout generation package in Coplan™ / Libra™. At this point a mask of various test circuits was laid out including breakouts of various interdigital capacitors and spiral inductors, the simulated high-pass and low-pass networks and variations on the high-pass and low-pass networks and other test structures. This mask was created to provide confidence in the simulated results provided by the electromagnetic software. The test structures on the first mask are covered in greater detail later.

The geometry of the high-pass and low-pass networks generated by Coplan™ was exported as a GDS file and then imported into Sonnet™. The two geometries were then simulated over the frequency range of 28 to 32 GHz with 0.5 GHz frequency steps. The simulations of the two networks assumed perfect conductors, thus neglecting the conduction losses and the kinetic inductance effect. The layout and simulated results of the high-pass and low-pass networks are shown in Figures 3-27 and 3-28. The simulated results of the high-pass network showed a poor input and output match, only -11.5 dB at 30 GHz. The transmission losses were large, with a maximum of -0.42 dB. For the low-pass network the minimum of the input match was centered at 28.5 GHz, not at 30 GHz. The input match of the low-pass network was good, better than -20 dB across the band. The corresponding transmission losses were equally good, with less than 0.07 dB of loss. The simulated phase difference between the high-pass and low-pass networks was 145.9° at 30 GHz. The phase shift differs from the simulated results from Coplan™ by -36.4°, or 20%. That the two software packages differ in their simulated results was not unexpected,

FIGURE 3-27 Layout and Simulated Results of High-Pass Network Using

Sonnet™

especially as Coplan™ was not able to accurately portray the geometry around the Tee elements, in particular the airbridges.

Further Sonnet™ simulations were conducted on the high-pass and low-pass section of the phase shifter to optimize the results in order to provide the best possible input and output matches to 50 Ω and to provide a phase shift of 180° at 30 GHz. The simula-

FIGURE 3-28 Layout and Simulated Results of Low-Pass Network Using Sonnet™

tions included tapering the interdigital capacitors to reduce their shunt capacitance, adjusting the inner diameter of the spiral inductors, removing airbridges from the area of the Tee and adjusting the lengths of the shunt stubs. After all of these simulations were completed and input and output matches of better than -15 dB were achieved across the band, it was noticed that the phase difference between the high-pass and low-pass networks differed from 180° by 14° .

Adding a 14° length of ideal transmission line at 30 GHz to the low-pass network returned the phase difference to 180° at 30 GHz. A 14° length of line corresponds to $110\ \mu\text{m}$ of coplanar waveguide line at 30 GHz. After examining the layouts of the high-pass and low-pass sections it was found that the high-pass network had a length of $860\ \mu\text{m}$ while the low-pass network was only $770\ \mu\text{m}$ long. The difference in length of the two sections is $90\ \mu\text{m}$ long, very close to the $110\ \mu\text{m}$ length of line required to correct the phase error. This suggested that the phase error was due to distributed effects caused by the difference in length of the two sections. The addition of a length of line to the low-pass section had the additional advantage of allowing both networks to be exactly the same length, simplifying the design of the required single-pole double-throw switches. Having the high-pass and low-pass sections the same length also allowed for the possibility of using other SPDT switches. After the addition of the extra length of transmission line to the low-pass network, further simulations were conducted to give an optimum response.

3.5.3 Simulated High-Pass Low-Pass Results

The high-pass and low-pass networks were simulated and optimized to give a good input and output match and the proper phase shift. All of the simulations assumed lossless conductors, neglecting the surface resistance and kinetic inductance effects in the HTS. While it was expected that neglecting these effects would affect the simulated results, because there were no reliable estimates of these parameters, they were not used for design purposes.

The final layout of the high-pass T-networks that was submitted for the second mask is shown in Figure 3-29. The overall dimensions of the high-pass circuit are $700\ \mu\text{m}$ by $1170\ \mu\text{m}$ including the probe pads for measurement. The circuit consists of four layers,

the YBCO HTS ceramic, gold pads for various purposes, posts for the airbridges and the airbridges themselves.

FIGURE 3-29 Layout of High-Pass T-Network

The simulated results of this structure using Sonnet™ are shown in Figure 3-30. The input and output matches are better than -15 dB across the 28 to 32 GHz bandwidth except at the extreme lower end of the band. As the simulation is lossless the transmission losses are all less than 0.1 dB except at the lower end of the band. The phase of high-pass network varies from 24.5° to -25.5° across the bandwidth and is -2.7° at 30 GHz.

The final layout of the low-pass T-network that was submitted for the second mask is shown in Figure 3-31. The overall dimensions of the low-pass circuit are $700\ \mu\text{m}$ by $1170\ \mu\text{m}$ including the probe pads for measurement.

The simulated lossless performance of the low-pass T-network is shown in Figure 3-32. The input and output matches are better than -20 dB across the entire 28 to 32 GHz band. The transmission losses are again dependent solely on the input and output match as lossless conductors were assumed. The transmission losses are less than 0.04 dB across

FIGURE 3-30 Simulated Lossless Performance of High-Pass T-Network

FIGURE 3-31 Layout of Low-Pass T-Network

the entire band. The phase of the low-pass T-network varies from -165° to -192.1° across the 4 GHz bandwidth, and is -178.3° at 30 GHz.

FIGURE 3-32 Simulated Lossless Performance of Low-Pass T-Network

The phase difference between the high-pass and low-pass network is 189.5° at 28 GHz, 175.6° at 30 GHz and 166.6° at 33 GHz. A plot of the phase difference versus frequency of the two T-networks is shown in Figure 3-33. The acceptable bandwidth of $180^\circ \pm 10^\circ$ is from 28 to 31 GHz. The bandwidth was 3 GHz, only 23.6% of the predicted theoretical maximum.

3.6 Design of Single-Pole Double Throw Switch

The basis for the operation of all HTS switches is the superconducting-normal phase transition. In the superconducting state, the HTS has a small series resistance, while in the normal state the HTS has a large series resistance. The ratio between the normal to superconductive series resistance determines how good a switch the particular HTS material can provide. The ratio between the superconducting and normal resistance is typically on

FIGURE 3-33 Phase Difference of High-Pass and Low-Pass T-Networks

the order of 10^4 . This type of switching is unique to HTS in that they are ceramics with poor normal state conductivity. The LTS are metals, and their normal state conductivity is too high for the phase transition to act as a switch.

3.6.1 HTS Switching

All HTS switches utilize the superconducting-normal phase transition to accomplish the switching, but there are several different methods of achieving this phase change. A phase change in an HTS material can occur due to excessive current density, heating above the critical temperature or by applying a magnetic field. There are different methods of achieving each of these forms of switching. The most reported method of switching uses super-critical current pulses for fast switching [57,58,59]. Subnanosecond switching times were reported using this method [60]. Other reported switching elements use thermal heating to cause the phase transition. The switching times for thermal heating are greater than those for a supercritical current pulse due to the thermal time constants. The methods for

heating the substrate include resistive material at or near the switching element [61], an electron beam [62], self-heating hotspots from an applied current [63,64] and a laser aimed at the switching element.

The switching element in [53] was the basis of the initial switch design. The switching element is a section of coplanar line that narrows in the middle while maintaining the same impedance throughout its length. In the On state, the switch is simply a coplanar waveguide line. In the Off state a dc bias is applied to the center conductor. The current flowing through the narrow section of the line drives the center conductor normal in that region through the formation of localized hotspots. The switch was able to provide better than 20 db of isolation from 0-30 GHz with the highest applied dc bias. This series switch promised simple dc biasing for the phase shifter circuit with excellent bandwidth and no need for a dc block in the design. After more careful examination of the switching element it was realized that the switch acted as a variable attenuator and therefore was an absorptive switching element. For a single-pole double-throw switch design the losses would be greater than 3 dB. Losses of 3dB are greater than the total losses allowed for the entire phase shifter and therefore the switch design had to be rejected.

A new switching element design was then required that was reflective rather than absorptive. A reflective switch design was accomplished by the addition of two thin shunt stubs to a coplanar waveguide line. The shunt stubs short circuit the center conductor to the ground plane as seen in Figure 3-34. The shunt sections are 5 μm wide and 40 μm long, going from the center conductor to the ground planes. The stubs provide a short circuit, reflecting back incident rf signals in the Off state. Simulations predicted an isolation of 21 dB. In the On state, a dc bias is applied and the thin sections of line are driven nor-

FIGURE 3-34 HTS Switching Element and Simulated Results

mal by the dc current through the generation of hotspots. The losses in the On state depend on the rf resistance of the normal state of YBCO. Assuming that the shunt stubs have a total resistance of $1000\ \Omega$ the rf losses in the On state would be only 0.4 dB. With lower total resistance in the shunt stubs the losses in the On state would increase. The actual resistance of the normal superconductor depends on the temperature of the self-heating hotspot. This section needs to be tested to ensure proper operation because the size and resistance of the normal section cannot be accurately predicted.

3.6.2 SPDT Switch

The use of a shunt switching element required a dc block in the center conductor of the SPDT switch to isolate the switching elements. This was to be accomplished through a half-wavelength resonant section in the center conductor such that the dc block was transparent to rf signals at the center frequency. After simulation and optimization an input and output match of only -8.5 dB could be achieved across the 28 to 32 GHz band. For this

match the resonant section required a length of $2110\text{ }\mu\text{m}$, approximately $3\lambda/4$ at 30 GHz. The center conductor of the dc block was divided into two $7.5\text{ }\mu\text{m}$ wide sections with a gap of $5\text{ }\mu\text{m}$ separating them. At each end of the dc block, one of the sections of the center conductor stops, with a $5\text{ }\mu\text{m}$ gap between it and the continuation of the center conductor, while the other section continues into the center conductor. Such a long section of thin line could and did lead to fabrication problems. Replacing the long resonant section of line with a series interdigital capacitor would probably have been a better solution for the dc block but this was not considered at the time.

As the resonant section provided only a poor match, input and output matching networks were required. The output matching network was designed to allow for the input of the dc bias required for the shunt switching elements. With the addition of the input and output matching networks the simulated match was better than 15 dB across the band.

Shunt switching elements provide a short circuit and therefore they must be an odd multiple of $\lambda/4$ from the coplanar Tee. The initial design, where a series open circuit switch was expected, would have allowed for the switching elements to be placed directly at the Tee. This, in addition to not requiring a dc block, would have allowed for a very compact switch design.

The final layout of the SPDT switch is shown in Figure 3-35. The overall dimensions of the switch are $4430\text{ }\mu\text{m}$ long by $3515\text{ }\mu\text{m}$ wide. The design of the SPDT switch should be looked at further at a later date in order to reduce the size of the switch.

The final simulations of the SPDT switch predicted losses of 0.3 dB at 30 GHz and losses greater than 1.0 dB at the band edges. The simulated isolation provided by the SPDT switch was greater than 20 dB except at the lowest end of the band. The simulated

FIGURE 3-35 Layout of SPDT Switch

input and output matches were better than -10 dB for most of the band. The simulated results of the SPDT switch assuming a lossless conductor and a resistance of $1000\ \Omega$ in the shunt stubs are shown in Figures 3-36 and 3-37.

FIGURE 3-36 Simulated Losses and Isolation of SPDT Switch

FIGURE 3-37 Simulated Input and Output Matches of SPDT Switch

3.7 Layout and Simulated Results of Complete Phase Shifter

With all of the components of the phase shifter designed, the high-pass T-network, the low-pass T-network and the SPDT switches, it remained to combine the components to determine the overall phase shifter response. The final layout of the 180° bit phase shifter is shown in Figure 3-38. The overall dimensions of the phase shifter are $8360\ \mu\text{m}$ long by $3515\ \mu\text{m}$ wide, with the majority of the area being taken up by the two SPDT switches. A different SPDT switch design could save considerable chip area.

The simulated results of the phase shifter give the bandwidth for a phase difference of $180^\circ \pm 10^\circ$ as 28.5 to 31.5 GHz. The simulated losses are less than 0.78 dB and the sim-

FIGURE 3-38 Final Layout of 180° Bit Phase Shifter

ulated input and output matches are better than -11.6 dB. The results are shown in Figures 3-39 through 3-41.

FIGURE 3-39 Simulated Lossless Phase Difference of 180° Bit Phase Shifter

FIGURE 3-40 Simulated Mismatch Losses of 180° Bit Phase Shifter

FIGURE 3-41 Simulated Lossless Input and Output Match of Phase Shifter

3.7.1 Simulated Phase Shifter Results Including Estimated Superconductive Effects

All of the design work of the thesis was conducted assuming lossless conductors or conductors that had small losses. Nowhere in the design of the 180° bit phase shifter were kinetic inductance effects included. These effects were neglected in the design simulations for two main reasons. The first reason for neglecting these effects is that the reported surface resistances and kinetic inductances of HTS films vary greatly between films fabricated by the same process and even more greatly by films of different processes [65,66]. There are many reported values of the surface resistance for various HTS films at various frequencies and temperatures but they seldom agree. One paper, by Feng et. al. [67], provided measurements of the kinetic inductance in a YBCO film but the results for one film cannot necessarily be applied to another. The second reason for neglecting the losses and kinetic inductance in the superconductive material during the design was to save time while performing the electromagnetic simulations.

It had been hoped that the first mask, to test various circuit components and the fabrication of the circuit, could be used to estimate the series resistance and kinetic inductance of the YBCO films used in this thesis. Due to fabrication problems these tests were not conducted.

To estimate the effect of the surface resistance and kinetic inductance would have on the design of the phase shifter it was decided to use the published results in [67] as both the surface resistance and kinetic inductance for the same YBCO film were presented.

The measured R_s and X_s from [67] at 60 K and 10 GHz are: $R_s = 0.26 \times 10^{-3} \Omega$ and $X_s = 18 \times 10^{-3} \Omega$. The values were scaled to the appropriate frequency, with R_s scaled by the square of the frequency and X_s scaled proportional to the frequency, according to

Equation (2-15). The values at 30 GHz are: $R_s = 3.24 \times 10^{-3} \Omega$ and $X_s = 54.0 \times 10^{-3} \Omega$. These values were calculated for every frequency simulated between 24 and 32 GHz, and each frequency was simulated using its corresponding value of R_s and X_s . The results of these simulations are shown in Figures 3-42 through 3-44.

FIGURE 3-42 Simulated Phase Difference of 180° Bit Phase Shifter

The acceptable phase difference has been shifted in frequency from 28.5-31.5 GHz to 28-31 GHz, a downward shift in frequency of 0.5 GHz. For losses of less than 1.5 dB the usable bandwidth is only 28-30.5 GHz, as the losses at 31 GHz are 2.14 dB. The input and output match of the phase shifter is better than -10 dB for the range of 27.5 to 31 GHz. The inclusion of the surface resistance and kinetic inductance resulted in increased losses and a downward shift in frequency of 0.5 GHz. In addition there is a null in the SPDT switch at 26.5 GHz when these effects are included.

FIGURE 3-43 Simulated Losses of 180° Bit Phase Shifter

The simulations including the surface resistance and kinetic inductance concluded the design of a fully integrated superconductive phase shifter. The 180° bit was designed having a bandwidth of 3 GHz and losses of less than 1.5 dB. The predicted losses are 0.5 dB greater than the original goal but are considered acceptable. The bandwidth is only 23.6% of the theoretical maximum for a high-pass low-pass phase shifter operating at 30 GHz.

FIGURE 3-44 Simulated Input and Output Match of 180° Bit Phase Shifter

CHAPTER 4: FABRICATION, TESTING AND MEASURED RESULTS

This chapter covers the fabrication, testing, measured results and analysis of the 180° bit phase shifter that was designed. Problems with the fabrication and testing are presented with the solutions used to overcome these problems. The final measured results are presented.

4.1 Fabrication of YBCO Phase Shifter Circuit

The fabrication of the superconductive phase shifter was a three step process. First two different masks were layed out and fabricated at Nortel. The masks were then sent to NRC where the YBCO lines were patterned and gold pads were attached. The partially completed chips were then sent to CRC where the airbridges were added.

The masks consisted of four layers, three dark field layers and one light field layer. The light field layer was for patterning the YBCO lines while the three dark field layers were for adding gold pads, posts and airbridges. These various layers were all fabricated on one 4x4x0.060 inch low-expansion glass mask.

NRC provided the YBCO films on LaAlO_3 substrates and patterned the HTS films. The chip size was limited to 1 cm^2 as that was the largest chip size NRC could process. One copy of the first mask and two copies of the second mask were provided with the YBCO patterned and the gold pads added.

After receiving the partially completed chips from NRC, the addition of airbridges (the final stage in the fabrication) was carried out at CRC. Adding the airbridges involved modifying the standard airbridge process used at CRC to work with HTS materials. The firsts two attempts at the fabrication of the airbridges were unsuccessful, but the final copy of the second mask was properly fabricated.

4.1.1 First Fabrication

The first fabrication run consisted of test elements to verify the simulated results from Coplan™ and Sonnet™. These test elements included the highpass and lowpass networks and variations thereof, various spiral inductors and interdigital capacitors, three switching element designs and a Through-Reflect-Line (TRL) calibration standard for de-embedding. The initial run was conducted for two main purposes, to provide a comparison of the simulated and measured results and to test the airbridge fabrication process. The time required between the initial layout of the first mask and its return was eight months. The layout of the mask used in the first fabrication run is shown in Figure 4-1.

FIGURE 4-1 Layout of the First Mask

There were problems with the airbridge process on this run, large portions of the circuits were damaged, see Figure 4-2. The damage to the YBCO material occurred during the airbridge process, when HCl was used as a rinse after the photoresist was developed. All HTS materials react strongly with acids due to the high oxygen content of all HTS materials. It was believed that the photoresist would shield the YBCO from contact with

FIGURE 4-2 Damage to Chip of First Fabrication Run

the acid solution as the developed areas were all over gold pads. Due to slight misalignments of the mask, it is likely that portions of the developed photoresist were not properly aligned to the gold pads and the acid solution was able to come into contact with the YBCO. Large portions of the YBCO in the area of the posts for the airbridges were removed. All of the test structures with airbridges were damaged.

4.1.2 Second Fabrication

The second and third chips were fabricated using the second mask. These chip included the final phase shifter design, breakouts of the high-pass and low-pass networks, the SPDT switch, the interdigital capacitors and inductors used in the T-networks, the shunt stubs used in the T-networks, the switching element and a TRL calibration standard. The time required for the completion of the second and third chips from the initial layout of the second mask was four and six months respectively. The layout of the second mask used for the second and third chips is shown in Figure 4-3.

FIGURE 4-3 Layout of Second Mask

When the second and third chips were returned from NRC, there were problems with the patterning of the YBCO film. Many of the problems were minor, or unlikely to affect the circuit performance but in some instances the problems were potentially significant. These included breaks in one of the thin traces of the dc block, breaks in some of the switching elements and a break in a stub in the matching network for one of the SPDT switches. The second and third chips were the only chips available and no others could be fabricated, due to a lack of unpatterned YBCO films at NRC. The more damaged of the two chips was submitted for addition of the airbridges first, as the airbridge process had not yet been proven.

In the airbridge process for the second chip, NH_4OH , a basic solution was used for the rinse after the photoresist was developed instead of HCl . An adhesion agent, HMDS (hexamethyldisilazane) was used to ensure that the posts for the airbridges would properly adhere to the gold pads. When the fabrication was completed, the airbridges on all of the spiral inductors were missing, including the gold bonding pads that had been fabricated at

NRC. All of the other airbridges that had been required for mode suppression were present. This suggested that the process for fabricating the airbridges was almost correct and only minor changes were needed. The loss of the airbridges on the spiral inductors could have been due to poor adhesion of the gold pads to the YBCO film. A magnified view of the second chip showing the missing spiral inductor airbridges and some of the patterning problems in the YBCO film is shown in Figure 4-4.

FIGURE 4-4 Missing Airbridges and YBCO Patterning Problems of Second Chip

The third chip was submitted for the addition of the airbridges with only one change to the airbridge process, the adhesion agent HMDS was not used as the substance is slightly acidic. When fabrication was complete all of the airbridges were present. The only flaws in the third chip were those due to the poor patterning of the HTS. The third chip, finally presented a circuit in which the phase shifter and all of the sub-circuits could be tested. The circuits on the third chip are shown in Figures 4-5, 4-6 and 4-7.

FIGURE 4-5 Photograph of Complete Phase Shifter on Chip #3

FIGURE 4-6 Photograph of Single-Pole Double-Throw Switch on Chip #3

FIGURE 4-7 Photograph of Breakouts on Chip #3

4.2 Testing

It was originally planned to test the first chip before the second mask was fabricated. The measured results of the first chip were to be used to modify the design of the second mask as necessary. Due to the time lag between the layout of the first mask and its final return this was not possible. Instead the design of the second mask was completed and ready for layout before the first chip was returned. Time constraints required that the second mask be fabricated as soon as possible and was therefore completed before the first chip was tested.

4.2.1 DC Testing at NRC

The dc characteristics of the three YBCO chips fabricated at NRC were measured to determine the quality of the YBCO films. The quality of the film determines the transition temperature, the maximum current density and the maximum applied magnetic field that the superconductor can withstand while still superconducting. A four probe dc test circuit was added to the masks to allow for the dc tests.

The testing was conducted at NRC using their dc test setup. The setup allows for the measurement of the transition temperature and the maximum current density. The chips were mounted on carriers specially designed for the dc setup. The carriers were then attached to the dc measurement equipment and the chips were cooled by placing them in a container of liquid nitrogen. Measurements of the resistance were taken at one second intervals as the samples were cooled and warmed. The resistance measurements were also conducted for different current levels. The samples were placed in the liquid nitrogen were cooled as much as possible for the maximum current density tests. With the samples at liq-

uid nitrogen temperatures, the current was varied to determine when the material was driven normal by the current density.

The first chip was measured both after the initial patterning of the YBCO film at NRC and after airbridge processing. This was to examine the effect processing had on the YBCO film. Before and after processing the airbridges, T_c was 84.6 K. The maximum current carried by the 20 μm wide by 0.3 μm thick line was 70 mA, giving a maximum current density of $1.2 \times 10^6 \text{ A/cm}^2$ for the HTS film. After processing of the airbridges the maximum current density was not determined but the current carrying capability was better than 10 mA. The transition temperature of the film was poor, 5.4 K below the maximum reported T_c for a YBCO film but the maximum current density of the film was good.

The second chip was measured after the airbridges had been added. The transition temperature, T_c , was approximately 84.5 K. The maximum current carrying capability of the film was only 0.5 mA, giving a maximum current density of only $8.3 \times 10^3 \text{ A/cm}^2$. This maximum current density was so poor that an attempt was made to repair the YBCO film by annealing it in oxygen. The annealing in oxygen totally destroyed the superconductive properties of the film. Figure 4-8 shows the current carrying capabilities of the second chip before and after annealing. The annealing process probably failed due to impurities from the airbridges damaging the YBCO film.

The third chip was tested before the airbridges were put in place and was found to have a T_c of 85.3 K for an applied current of 1 μA . The maximum current carrying capability of the test line was 6 mA giving a maximum current density for the film of $1 \times 10^5 \text{ A/}$

FIGURE 4-8 Current Carrying Capability of Second Chip Before and After Annealing in Oxygen

cm^2 . This is a poor quality YBCO film but was assumed to be sufficient for small signal testing of the circuit.

4.2.2 Cryogenic Wafer Probing Station at CRC

The testing of the chips was to be conducted at CRC using a cryogenic wafer probing station available on site. The cryogenic wafer probing station had been shown to work with TBCCO circuits and was expected to work with YBCO circuits.

The cryogenic wafer probing station at CRC is a piece of equipment that allows circuits to be tested using rf probes at very low temperatures. The test circuit was placed on a cold head inside of a vacuum chamber and rf probes were used to measure the circuit. The cold head is cooled by liquid nitrogen providing an operating temperature on the cold head as low as 78 K under normal operating conditions. This temperature can be reduced by evaporating the liquid nitrogen into near vacuum and provided temperatures on the cold

head as low as 67.3 K for sustained periods of time. The vacuum is required to minimize thermal conduction by atmospheric gasses and condensation of atmospheric gasses on the cold head and circuit to be tested. The cryogenic wafer probing station has two rf probes available for testing circuits. The probes are aligned facing one another, allowing for two-port S-parameter measurements. There are also several dc bias lines that feed into the vacuum chamber.

The ability to directly probe a circuit allows for more accurate results as compared to testing with the device under test (DUT) being placed in a jig for connection to coaxial cables. Directly probing the circuits eliminates the need for bond wires in the rf path connecting the DUT to the jig. Direct probing also allows for calibration with no thermal cycling by using a calibration standard placed either on the chip to be measured or on another chip on the cold head.

The first chip contained only passive components or components for which the required dc biasing could be accomplished through the rf probes of the cryogenic wafer probing station. The second and third circuits had both passive components and circuits requiring separate dc biasing. Therefore the second and third chips had to be diced and placed on a jig before they were tested. The purpose of the jigs used for the second and third chips was to allow attachment points for the dc bias lines. These bias lines were expected to have no effect on the rf performance of the circuits.

4.2.2.1 Problems with Vacuum of the Cryogenic Wafer Probing Station

During the initial tests of the first chip with the cryogenic wafer probing station, thick crystalline films condensed onto the circuit as the probing station reached its operating temperature of 78-79 K. The condensed films interfered with making good contact

between the probe tips and the gold pads on the circuit. The condensed films had to be scratched off before good contact could be made. With increasing time the deposited film grew so thick and dark that seeing the circuit became difficult. These films were formed by gasses condensing on the cold head and the circuit at the extremely low temperature.

The vacuum in the vacuum chamber only reached 1.0×10^{-1} Torr with the vacuum pump running continuously. The pressure was too high for the proper operation of a cryogenic probing system, suggesting that there were serious gas leaks in the chamber. The pressure in the vacuum chamber should have been less than 1×10^{-2} Torr before the liquid nitrogen was turned on. The vacuum chamber should be isolated from the vacuum pump before the liquid nitrogen was turned on. The liquid nitrogen flowing through the cold head acts as a cryopump, condensing the residual gasses in the vacuum chamber onto the cold head. This method can produce pressures as low as 10^{-5} Torr in a well sealed vacuum chamber. While it was the condensation of gasses on the cold head and circuit that caused the initial problem, with a much lower initial pressure and with no leaks, the film of condensed gasses would be so thin as to not cause a problem.

Leaks were found in the vacuum chamber at the rf probe pass-throughs. Several of the joints were improperly sealed. These joints were then sealed with a silicon epoxy and the vacuum of the chamber was then tested. A pressures of 5.7×10^{-3} Torr was reached with the newly sealed joints. As a further check the vacuum pump was disconnected for 5 minutes and the pressure measured at the end of that period. The pressure had risen to only 8.4×10^{-3} Torr and was considered acceptable. After cooling the cold head in the vacuum chamber, only a very thin film of condensed gasses was deposited on the circuit, not enough to provide problems in making good contact between the rf probes and the circuit.

4.2.2.2 Thermal Problems with the Cryogenic Wafer Probing Station

The cryogenic wafer probing station at CRC had not previously been used to test YBCO circuits. It had been demonstrated that TBCCO circuits with T_c of 100 K or more could be tested using the system. YBCO has a T_c of only 90 K for very good films, and only 84.5-86 K for the films used in this thesis. After cooling the cryogenic probing station to 78 K the YBCO circuits were tested and found to be very lossy, indicating that the material was not superconducting.

That the YBCO circuits were not cold enough to superconduct was initially attributed to the jig design on which the circuits were mounted. As all of the Sonnet simulations had assumed an air gap below the substrate, jigs were designed with an air gap in place. The air gap under the circuit left a very poor thermal path between the chip and the jig itself. If the thermal path was too resistive, it would be impossible to cool the circuit to the necessary temperature. Simulations were performed with a lossy ground plane placed directly below the substrate to see the effects of removing the air gap. These simulations showed that the effect of a lossy ground plane on the circuit performance was negligible. The jigs were then redesigned where necessary and those circuits that didn't require an external dc bias line were placed directly on the cold head for testing. This reduced the thermal path allowing the circuits to reach lower temperatures.

The first chip was then placed directly on the cold head and large losses were still present in the rf measurements. As rf measurements are difficult to conduct it was decided to try dc measurements of chip number one placed directly on the cold head, and of chip number two on a jig. The results of the dc testing are recorded in Table 4-1.

TABLE 4-1 DC Measurements of YBCO films in Wafer Probing Station

Measured Device	Temperature of Cold Head	Voltage	Current	Resistance
Chip #1 on Cold Head	78.42 K	1.509 V	0.008 A	190 Ω
Chip #2 on Jig	78.35 K	4.896 V	0.009 A	550 Ω
Silvar Jig	78.40 K	0.030 V	0.024 A	1.25 Ω

The track that was measured on chip one and two was approximately 47.2 squares. Using R_{dc} of the superconductor at 100 K of 3.07 ohms per square, the resistance of the superconductors should be 144.8 Ω if the films were 100 K. The resistance of both films was greater than this value suggesting that the films were more than 100 K when they were measured. As a check on the dc test, the silvar jig was tested and it had a measured resistance of only 1.25 Ω .

The dc resistance experiment suggested that the films were over 100 K when they were being measured even though the cold head was approximately 78.5 K. There must have been some heat source that warmed the chips during measurement. It was noticed that underneath the rf probes, the thin films of condensed gas were not present. This suggested that the rf probe arms were the source of the heat, warming the YBCO chips. The rf probe arms were not actively cooled nor was there any thermal isolation between the probe head and the exterior of the vacuum chamber. No additional temperature sensors were available to measure the temperature of the rf probes to confirm this conclusion. Copper straps were attached from the rf probe arms to the cold head in an attempt to lower the temperature of the probe heads.

With the copper straps in place one final experiment was performed to determine if the YBCO chips could be tested with the available equipment. In this test, a YBCO chip was placed on the cold head with a TBCCO chip and Cascade calibration standard. The

cold head was then cooled to approximately 67.2 K by expanding the liquid nitrogen coolant into a vacuum. The system was then calibrated from 24 to 32 GHz using the Cascade standard. The calibration had an error of less than 0.015 dB in S_{21} and better than -30 dB in S_{11} . The YBCO line used in the dc test was then measured and found to have losses of 2.56 dB at 28 GHz. A short TBCCO line was also measured and found to have losses of 0.003 dB at 28 GHz, less than the calibration error. These tests indicate that the cryogenic wafer probing station at CRC is unable to cool YBCO sufficiently to superconduct, while it was able to cool TBCCO into a superconducting state. TBCCO has a higher T_c and it is this higher T_c that allows TBCCO to superconduct when the YBCO cannot. On heating the cold head back to room temperature the losses in the TBCCO line were measured. The loss in the TBCCO line reached 2.5 dB at 82 K. The TBCCO was already normal with a temperature reading 18 K below the T_c of TBCCO of 100 K.

The only methods of further cooling the YBCO films were to thermally isolate the rf probes or to use a different cryogenic liquid. Both of these methods would require significant redesign of the cryogenic wafer probing station and that was beyond the scope of this thesis. Instead, alternative methods of testing the YBCO circuits were investigated.

4.2.3 Final Testing Method

The National Institute of Standards and Technology (NIST) in Boulder, Colorado, has a cryogenic wafer probing station which uses liquid helium as the cryogen. The use of liquid helium allows for the circuits to be cooled far below the transition temperature of 85.3 K of the HTS material on the third chip. The probe arms are thermally connected to the cold head and their temperatures are individually measured. The test equipment available at NIST ensured that the circuits on the third chip could be tested.

A jig was designed to allow the third chip to be tested at NIST with provisions for dc biasing and thermal contact to the cold head. The chip was diced into three sections, two of which required dc biasing. The three sections included a section with the fully integrated phase shifter, a section with the single-pole double throw switch and a section with all of the passive breakouts. The sections of the chip were epoxied onto a kovar carrier with filtercon holders screwed into each end. Bond wires from the filtercons were connected to the chip capacitors on the phase shifter and the SPDT switch, and from the chip capacitors to the bond pads in the circuit to complete the dc bias network. Only four filtercons were used for the six chip capacitors because the switches in the phase shifter must be controlled together. The kovar carrier was attached to a large brass plate designed to mate up the cold head of the wafer probing station at NIST. The final jig used for testing is shown in Figure 4-9.

4.3 Results of Testing

The circuits on the third chip were tested using the equipment available at NIST. The testing of the circuits was conducted with the cold head at a temperature of 45 K and the probe arms with a temperature of 65 K. For two measurements the cold head was at 26 K. The cold head was cooled to 45 K and the intermediate stage was 47 K. The temperature was selected to ensure that the circuit would be entirely superconducting. The power level used for most of the testing was -5 dBm and in certain instances -20 dBm, the smallest power level that didn't require a complete recalibration. The on chip Thru-Reflect-Line (TRL) standard failed because the losses in the HTS lines were too small for accurate measurements. More and longer thru lines were required. After attempting to use the Thru-Reflect-Line (TRL) standard on the HTS chip to no avail, a Thru-Reflect-Match

FIGURE 4-9 Jig Set-up Used for Testing at NIST

(TRM) standard on GaAs was used instead. The use of different substrates for the calibration and testing can lead to errors. The TRM calibration standard on the GaAs substrate was the best option to complete the measurements of the HTS circuits in the time available. The calibration was conducted over the bandwidth of 0.1-40 GHz. Larger calibration errors occurred at the higher frequencies, especially above 35 GHz. Due to time constraints on the use of the equipment at NIST, no narrow band calibration was conducted. With the network analyzer calibrated the various circuits were tested. The measurements include averaging over eight sweeps.

4.3.1 Measured Results of Switching Element

The switching element used in the SPDT switch is shown in Figure 3-34 on page 91. The switching element was originally tested at 47 K and at a power level of -5 dBm. With no

applied dc bias, the Off state, the magnitude of the S21 measurement was between -1.0 and -1.4 dB. Simulations of the Off state predicted the magnitude of S21 to be lower than -20 dB. The measured switch provided almost no isolation between the input and output ports. When dc bias was added between the center conductor and the ground planes, with current levels up to 4 mA, no change in measured S21 was noticed. This suggested that the rf power level might be too large and that the rf signal was turning the switch on. The rf power was then reduced to -20 dBm and S21 was measured again. The magnitude of S21 in the Off state then varied between -3 dB to -1 dB across a band of 1 to 35 GHz. This amount of isolation was still unacceptable. When a dc bias of 2 mA was applied to the switching element, corresponding to the On state of the switching element, the losses were less than -0.5 dB across the same 1 to 35 GHz band. The On state of the switch performed better than predicted. The measurements are shown in Figure 4-10.

4.3.2 Measurement of Highpass and Lowpass Breakouts

The breakouts of the highpass and lowpass T-networks were measured at both 47 K and 26 K. The phase difference between the measured S21 of the two networks was calculated and phase shifts of $180^\circ \pm 10^\circ$ over the range of 26.3 GHz to 30.0 GHz at 47 K and 26.9 GHz to 34.5 GHz at 26 K were found. The phase differences versus frequency for the two operating temperatures are shown in Figure 4-11.

The corresponding transmission losses are higher than predicted, particularly with the lowpass T-network. At the operating temperature of 47 K the losses of the lowpass T-network in the range of 26.3 to 30.0 GHz, are -1.79 dB and -1.95 dB at the band edges respectively with maximum losses of -2.36 dB and minimum losses of -1.43 dB. For the highpass T-network at the same temperature and frequency range the losses are -0.32 dB

FIGURE 4-10 Measured Results of Switching Element

FIGURE 4-11 Measured Phase Shift between Highpass and Lowpass T-Networks

and -0.73 dB at the band edges with a maximum loss of -1.03 dB and a minimum loss of -0.29 dB within the band. Operating at 26 K, the bandwidth covers 26.9 to 34.5 GHz and the losses of the lowpass T-network are -1.68 dB and -2.94 dB at the band edges respectively with maximum losses at the upper band edge and minimum losses of -1.27 dB. For the highpass T-network operating at 27 K, over the frequency range of 26.9 to 34.5 GHz the losses are -0.40 dB at the band edges with a maximum loss of -1.64 dB in the band. The measured losses of the T-networks are higher than the desired -1.0 dB for the entire phase shifter. Figure 4-12 shows the measured transmission losses of the highpass and lowpass T-networks at both temperatures. Markers 1 and 2 delimit the bandwidth for the

FIGURE 4-12 Measured Transmission Losses of Highpass and Lowpass T-Networks

phase shifter at 47 K and markers 3 and 4 delimit the bandwidth at 26 K.

of the lumped elements agrees well with that predicted by the models and simulated results.

4.3.4 Measured Results of Single-Pole Double-Throw Switch

The SPDT switch was measured at 47 K with a power level of -5 dBm. A full 3-port measurement was impossible as the spacing between the ports was too narrow for two probes and not correct for a ground-signal-ground-signal-ground probe head. The measurements were all taken with one of the two ports on the selectable paths left open. If the SPDT switch provided good isolation between output ports then leaving one port open should cause little measurement error.

When the circuit was tested it was found that the input reflection coefficient was very poor, greater than -5 dB except for a narrow band around 38 GHz. The transmission losses in the range of interest, 26 to 35 GHz, were greater than -20 dB. These results apply to all combinations of applied bias and placement of the rf probes. Bias currents of up to 4 mA were used to no noticeable effect. At the time of testing reducing the power level, as was done for the switching element, was not considered. The SPDT switch did not work whatsoever, and no actual switching could be noticed. A representative example of the measured results is shown in Figure 4-14.

4.3.5 Measured Results of Fully Integrated Phase Shifter

After measuring the SPDT switch and finding that it didn't work, it was expected that the complete phase shifter would not work. In addition to having two SPDT switches, the bond wire for applying dc bias to one of the paths was broken during testing, allowing only one path to be measured. The circuit was tested at 47 K with a power level of -5 dBm and a dc bias of 2 mA to turn on the lowpass path.

FIGURE 4-14 Representative Measured Results of SPDT Switch

The losses in the complete phase shifter were greater than -26.9 dB across the entire range of measurements. There was nearly complete reflection at the input of the phase shifter while the output port was matched to better than -5 dB. As the phase shifter is nearly symmetric, this may suggest that the power level at the input was too large for the HTS film to operate properly. Therefore the phase shifter and the SPDT switch should have been tested at a lower power level. The measured results of the phase shifter are shown in Figure 4-15.

4.4 Analysis of Results

Large discrepancies existed between the simulations of the phase shifter components and the raw measured data. The differences between the simulated and measured results are due to three main factors: 1. The probe pads used for measurement were not de-embedded

FIGURE 4-15 Measured Results of Fully Integrated Phase Shifter

in the calibration. 2. The power level of the measurements was too large for the maximum current density of the HTS film. 3. The estimates of the material parameters of the HTS films were not accurate. Numerical analysis and further simulations were able to account for these effects and provide simulations that match-up well with the measured results.

4.4.1 Numerical De-embedding

All of the simulations used to design the phase shifter assumed that the effects of the probe pads would be de-embedded using the TRL calibration standard on the chip. When the TRM calibration standard had to be used instead, the effects of the probe pads were not removed. As part of the measurements the through and the line from the TRL calibration standard were measured. The through in the TRL standard consists of the probe pads for the left and right side of the components directly connected together.

The measurement of the through had to be divided into two components, one for the right side probe pad and the other for the left side probe pad. These components were used for de-embedding of the probe pads from the measured results. The probe pads are mirror images of one another and have identical S-parameters except that the ports are interchanged.

The procedure used to divide the S-parameters of the through into the S-parameters of the left and right side probe pads follows. The S-parameter matrix of the through was transformed into a Cascade matrix. The matrix square root of the Cascade matrix was taken, dividing the Cascade matrix into two equal components. The square root of the Cascade matrix was then transformed back into an S-parameter matrix. The complex conjugate of the elements of the S-parameter matrix was then taken, producing the S-parameter matrix for the left-side probe pads. The complex conjugate of the S-Parameter matrix was required to account for the effect of interchanging the ports of the S-parameter matrix for the right hand probe pad. The ports of the left side probe pad S-parameter matrix were interchanged producing the right side probe pad S-parameter matrix. Matlab™ was used to carry out these calculations for every frequency. The right side and left side probe pad S-parameter matrices were used to de-embed the through as a check on the accuracy of the matrices. The maximum error in the magnitude of S_{21} and S_{12} after de-embedding was ± 0.05 dB. Comparing the series connection of the left and right side probe pads to the measured data of the through showed that the S-Parameters were nearly identical. The S-parameters of the series connection lay between the measured S_{21} and S_{12} and the measured S_{11} and S_{22} . The small error confirmed that the procedure for de-embedding the probe pads was accurate.

The S-parameter matrices for the probe pads were used to de-embed the measured data files for the other elements. The de-embedding of the elements was accomplished using Libra™. The left and right side probe pad S-parameter data files were connected to the respective sides of the element being de-embedded as NEG2 (2-port negation) elements. The output was the de-embedded measured data.

4.4.2 HTS Film Quality and Power Handling

The measurements of the HTS circuits were to be conducted at small signal levels. Small signal levels mean a large back-off from the power level at which the superconductor would start becoming normal. Simulations of a straight, $50\ \Omega$, coplanar waveguide line identical to the $50\ \Omega$ lines used in the phase shifter were conducted to determine at what power level the edges of the line would become normal. The simulations to determine the maximum power handling were conducted using the critical current density of the YBCO thin-film on chip #1. The critical current density of the YBCO thin-film on chip #1 is $1.2 \times 10^6\ \text{A/cm}^2$. The maximum power level that the line could handle before the edges started to become normal was 14.0 dBm. A back-off of 20 dB from this value was considered to be acceptable for small signal operation. Therefore a power level of -5 dBm was chosen for conducting the measurements.

Problems with the measurements arose because the YBCO thin-film on chip #3, the chip that was measured, has a critical current density of only $1 \times 10^5\ \text{A/cm}^2$. The critical current density of chip #3 is approximately one-tenth that of chip #1, therefore the maximum power handling capability is only one-one hundredth of chip #1. The HTS film of chip #3 can handle only -7.5 dBm before the edges of a straight $50\ \Omega$ line start becoming

normal. The measurements taken at -5 dBm were high power levels, not small signal power levels.

Current crowding at discontinuities exacerbated the problem of current densities exceeding the critical current density of the YBCO thin-film. Regions with greater than the critical current density were not accounted for in the initial simulations, but had to be included for accurate simulation. An example of the current density exceeding the maximum current density of the HTS film at a power level of -5 dBm is presented in Figure 4-16. The lighter areas indicate where the current density is greater than the critical current

FIGURE 4-16 Current Density in Highpass T-Network

density of the HTS film. Similar results were found with the lowpass network, the SPDT

switch and the switching element. Accurate modeling of the circuits require that these areas have different material parameters than the rest of the HTS material.

4.4.3 YBCO Material Properties

Knowledge of the areas of excessive current density of the circuits was necessary but not sufficient to provide accurate simulations of the circuit. Appropriate material parameters of the YBCO films were required. The material parameters used for simulation needed to be consistent between various simulations and provide good matches to the measured results. For the highpass, lowpass and SPDT switch circuits one set of material parameters was able to meet these requirements.

In the regions where the current density was less than the critical current density the material parameters used are: $R_s = 0.00468$ ohms per square and $X_s = 0.424$ ohms per square at 30 GHz. The value of R_s is 1.4 times that used in the previous simulations. The value of X_s is 7.8 times the value used in the previous simulations. A large kinetic inductance corresponds to a large penetration depth which would be expected in a poor quality HTS film.

In the regions where the current density exceeded the critical current density the material parameters used are: $R_s = 0.15$ ohms per square and $X_s = 0.424$ ohms per square at 30 GHz. The values of R_s and X_s suggest that the HTS film is in a mixed state. If the film were completely normal, R_s would be expected to be much larger and X_s would be zero. Figures 4-17 to 4-20 show the initial simulations, measured results at 47 K and the final matched simulations of the highpass T-network, the lowpass T-network, the phase difference between the highpass and lowpass networks, and the SPDT switch respectively.

FIGURE 4-17 Measured and Simulated Results of Highpass T-Network

FIGURE 4-18 Measured and Simulated Results of Lowpass T-Network

FIGURE 4-19 Measured and Simulated Phase Shift

FIGURE 4-20 Measured and Simulated Results of SPDT Switch

The previous set of material parameters provided good matches between measured and simulated results, but didn't work with simulations of the switching element. The switching element was measured at -20 dBm in both the On and Off states.

In the On state the measured results of the switching element were better than originally expected. A dc current of 2 mA was used to drive the shunt stubs normal. The values for the superconducting regions used in the simulation are: $R_s = 0.00468$ ohms per square and $X_s = 0.424$ ohms per square at 30 GHz. For the normal regions, the shunt stubs, the material parameters required were $R_s = 200$ ohms per square and $X_s = 0$ ohms per square at 30 GHz. This shows that the HTS was completely driven normal in the shunt stubs by the applied current. The measured and simulated results of the switching element in the On state are shown in Figure 4-21.

FIGURE 4-21 Measured and Simulated Results of Switching Element in On State

In the Off state the measured results of the switching element were much worse than expected. The Off state of the switching element provided only 1-3 dB of isolation in the 5-35 GHz range. Better than 20 dB of isolation was expected. Simulations of the current density in the Off state with an input power level of -20 dBm predicted a maximum current density in the shunt switching element of half the critical current density. The circuit should have been entirely superconducting. In order to match the simulations to the measured results, the shunt stubs required a value for R_s of 33 ohms per square and X_s of 0 ohms per square at 30 GHz. Therefore the shunt stubs were normal. From the simulations it was expected that the entire circuit would be superconducting, suggesting that the HTS film was damaged in the region of the shunt stubs in some way. The measured and simulated results of the switching element in the Off state are shown in Figure 4-22.

FIGURE 4-22 Measured and Simulated Results of Switching Element in Off State

Knowledge of the current densities and selection of suitable material parameters allowed simulations of the various circuits to match the measured values. Accurate knowledge of the material parameters and maximum operating power level are required to design HTS circuits.

CHAPTER 5: CONCLUSIONS

5.1 Summary

A 180° superconductive phase shifter operating at Ka-band has been investigated. A phase shift of $180^\circ \pm 10^\circ$ was achieved over a bandwidth of 3.7 GHz at 47 K and 7.6 GHz at 27 K between the highpass and lowpass sections. This demonstrated that a high-pass low-pass superconductive phase shifter is capable of operation at Ka-band. The advantages of using superconductors as compared to conventional technologies was not demonstrated due to the poor quality of the YBCO films and the power levels of the measurements. With a high quality HTS film and operation at acceptable power levels, the simulations used for designing the phase shifter showed that losses of less than -1.5 dB for one bit are possible. Regardless of the quality of the HTS film the highpass lowpass design of the superconductive phase shifter will limit the maximum power handling of the circuit. The phase shifter designed in this thesis would be suitable only for the receive chain of an RF system.

With respect to the initial design goals, a fully integrated phase shifter was not achieved. The failure of the single-pole double-throw switch due to a poor quality YBCO film in conjunction with excessive power levels for that film, lead to the failure of the completely integrated phase shifter.

The 180° bit was successfully designed, as demonstrated by the highpass and low-pass breakouts. The measured phase difference between the breakouts was $180^\circ \pm 10^\circ$ over the ranges of 26.3 GHz to 30.0 GHz when measured at 47 K and 26.9 to 34.5 GHz when measured at 26 K.

The losses in the phase shifter sections were larger than the goal of less than 1 dB per bit for the complete phase shifter. The maximum losses in the range of operation were

-2.36 dB for the lowpass network and -1.03 dB for the highpass network at 47 K. When the breakouts were measured at 26 K, with the larger bandwidth, the maximum losses were -2.94 dB in the lowpass network and -1.64 dB in the highpass network. The higher than expected losses can be accounted for by the poor material properties of the YBCO film and the excessive power level for the YBCO film at which the circuits were measured. The power level was sufficient to drive portions of the circuits normal or into a mixed state. With peak currents flowing in the normal areas of the film the losses are significantly increased. In addition, the very large kinetic inductance shifted the frequency of operation of the lowpass network down in frequency, so that some filtering by the lowpass network increased the losses in that circuit.

The phase shifter was able to operate at Ka-band. Allowable phase shifts were present between 26.3 to 30 GHz and 26.9 to 34.5 GHz depending on the temperature of operation. Superconductive lumped element components were designed that operated over the range of measurements without resonances. Parasitics played a large role in the response of the circuits, as was expected.

The measured bandwidth of the phase shifter sections was better than expected. The bandwidth for the allowable phase shift of $180^\circ \pm 10^\circ$ was 3.7 GHz at 47 K and 7.6 GHz at 27 K between the highpass and lowpass sections. The bandwidths of operation would cover the entire local multi-point communication system band. The large change in the bandwidth between measurement at 47 K and 27 K shows that the bandwidth is affected by the kinetic inductance of the superconductor. The kinetic inductance varies with temperature, and is the only component that could account for such a large change in the bandwidth with temperature.

The phase shifter was measured at 47 K and 27 K to ensure that there would be no thermal problems with the measurements. The circuit should be able to operate at 77 K but the bandwidth of an acceptable phase shift would be open to question. As the operating temperature approaches the critical temperature of the superconductive film, the kinetic inductance increases. The closer the operating temperature is the critical temperature the greater this increase. The change in temperature from 47 K to 27 K would only slightly reduce the kinetic inductance. A change in temperature from 47 K to 77 K would greatly increase the kinetic inductance of the YBCO film and could have a significant impact on the performance of the circuits.

Chapter 2 presented background material on superconductors and phase shifters. The history of superconductors and some applications of low temperature superconductors were presented. Various macroscopic theories on the operation of superconductors, including the London Theory, Two-Fluid Models and the Ginzberg-Landau Theory were covered. The BCS theory describing the mechanism of superconductivity in low temperature superconductors was covered. Some of the theories on the mechanism in high temperature superconductors were covered. The various high temperature superconductors, their structure, fabrication, patterning an substrate selection were also presented.

The next portion of chapter 2 covered several planar digital phase shifters. The various types of phase shifters included switched line, reflection, loaded line and high-pass low-pass phase shifters. The design equations for these phase shifters were presented along with their advantages and limitations.

Chapter 3 reported the design of the superconductive phase shifter from the selection of technologies to the final layout. The selection of the phase shifter and its ideal pro-

prototype network was covered. The lumped elements required for the prototype networks were modeled and selected. The models of the lumped elements were then included into the prototype networks and modified to give the correct response. The highpass and low-pass networks were then laid out and electromagnetically simulated with the layout being modified until the desired results had been achieved. The design of the single-pole double-throw switch was then presented. Finally estimates of the circuit performance were presented using material properties from reported YBCO films. The predicted circuit performance for a phase shift of $180^\circ \pm 10^\circ$ was a bandwidth from 28 to 30.5 GHz with losses of less than 1.5 dB. The bandwidth was limited by the losses of the SPDT switch design.

Chapter 4 presented the fabrication, testing, measurement and analysis of the phase shifter circuit. The fabrication of the circuit by NRC and CRC and the problems with the fabrication were covered. Included was the poor quality of the YBCO films used in fabrication of the second and third chips. The YBCO film on the third chip has a maximum current density of only 1.0×10^5 A/cm², as compared to the maximum current density of the YBCO film on the first chip of 1.2×10^6 A/cm². The attempts to test the circuit using the cryogenic wafer probing station at CRC and the reasons for testing at NIST were presented. The measured results of the phase shifter and the assorted breakouts were then presented. The measured results of the highpass and lowpass sections were great with respect to the phase shift but the losses were too large. The complete phase shifter and the switches didn't operate as expected. The measured results were numerically de-embedded and then analyzed to explain the differences. The failure of the switches and the complete phase shifter can be attributed to the poor material properties of the YBCO film and the

power level at which the circuits were tested. The higher than expected losses in the high-pass and lowpass networks can also be explained in this manner.

5.2 Future Work

The present work has shown that a superconductive lumped element phase shifter can operate at Ka-band. The advantages of this circuit as compared to conventional Ka-band phase shifters were masked by the poor quality of the HTS film that was tested. To demonstrate the level of losses that can be achieved with such a circuit it would be beneficial to fabricate the circuit from a high quality YBCO film, such as the YBCO film on the first chip. The circuit could then be tested at a very low power level to demonstrate the low losses such circuits can have.

The design of the single-pole double-throw switch could also be looked at in more detail to increase the bandwidth, reduce the losses and increase the power handling capabilities of the circuit. The major factor limiting the current design of the switch is the dc block. The long thin sections of coupled line introduce large losses, limit the bandwidth and the power handling capability and introduce potential patterning problems. The switching elements themselves limit the power handling capability of the circuit. In the off state the current density in the shunt elements is very high as compared to the transmission line. By making the transmission line larger without changing the impedance of the line, which is possible in coplanar waveguide, the shunt stubs can be made wider without affecting the circuit. This would allow for greater power handling capability in the switching elements themselves.

The phase shifter designed in this thesis is limited to low power levels. The phase shifter would be suitable only for the receive chain of an RF system. The highpass lowpass

phase shifter design is limited in the maximum power handling of the circuit by the size and parasitics of the lumped elements. These elements cannot be scaled in size without affecting the frequency of operation. To include HTS phase shifters in high power applications at Ka-band some other topology of the phase shifter is required. Other topologies of phase shifters could be investigated to increase the power handling capabilities of the circuit.

References

- 1 Fitzgerald, K. "Superconductivity: Fact vs. Fancy", IEEE Spectrum, pp. 30-41, 1988.
- 2 Luo, J. and Li, Q. and Fenner, D.B. and Liu, S. and Hamblen, W.D. and Wu, X.D. "Pulsed Laser Deposition of $\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}/\text{BaTiO}_3/\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$ Multilayer Structure on Si(100) Substrates", IEEE Transactions on Applied Superconductivity, Vol. 5, No. 2, pt.2, pp. 1635-8, 1995.
- 3 Talvacchio, J. and Forrester, M.G. and Gavalier, J.R. "Properties of Passive Structures for Multilayer HTS Digital Circuits", Transactions on Applied Superconductivity, Vol. 5, No. 2, pt. 3, pp. 3139-42, 1995.
- 4 Booth, J.C. and Beall, J.A. and DeGroot, D.C. and Rudman, D.A. and Ono, R.H. and Miller, J.R. and Chen, M.L. and Hong, S.H. and Ma, Q.Y. "Microwave Characterization of Coplanar Waveguide Transmission Lines Fabricated by Ion Implantation Patterning of $\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$ ", IEEE Transactions on Applied Superconductivity, Vol. 7, No. 2, pt. 3, pp. 2780-3, 1997.
- 5 Zhi-Yuan Shen and Wilker, C. and Pang, P. and Face, D.W. and Carter, C.F., III and Harrington, C.M. "Power Handling Capability Improvement of High-Temperature Superconducting Microwave Circuits", IEEE Transactions on Applied Superconductivity, Vol. 7, No. 2, pt. 3, pp. 2446-53, 1997.
- 6 Pettiette-Hall, C.L. and Murduck, J. and Burch, J.F. and Sergant, M. and Hu, R. and Cordrump, J. and Luong, M. and Ellis, R.K. "Characterization and Improvement of a YBCO Multilayer Film Process for HTS Circuit Applications", IEEE Transactions on Applied Superconductivity, Vol. 7, No. 2, pt. 2, pp. 2057-62, 1997.

- 7 van Duzer, T. "Superconductor Electronics, 1986-1996", IEEE Transactions on Applied Superconductivity, Vol. 7, No. 2, pt. 1, pp. 98-111, 1996.
- 8 Avenhaus, B. and Porch, A. and Huang, F. and Lancaster, M.J. and Woodall, P. and Wellhofer, F. "Switched $\text{YBa}_2\text{Cu}_2\text{O}_7$ lumped element bandstop filter", Electronics Letters, Vol. 31, No. 12, pp. 985-6, 1995.
- 9 Vogt, A. and Jutzi, W. "An HTS Narrow Bandwidth Coplanar Shunt Inductively Coupled Microwave Bandpass Filter on LaAlO_3 ", IEEE Transactions on Microwave Theory and Techniques, Vol. 45, No. 4, pp. 492-7, 1997.
- 10 Jecha Kim and Seok-Kil Han and Kwang-Yong Kang. "Dependence of Microwave Properties of HTS Parallel Coupled-Line Type 4-Pole Bandpass Filters on Enhanced Electrodynamical Properties of Ag-Doped YBCO Films", 1997 SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference Proceedings, Vol. 1, pp. 165-70, 1997.
- 11 Shen Ye and Mansour, R.R. "An Innovative CAD Technique for Microstrip Filter Design", IEEE Transactions on Microwave Theory and Techniques, Vol. 45, No. 5, pt. 2, pp. 780-6, 1997.
- 12 Simmons, J.P., Jr. and Madden, J.M. "Practical HTS/Cryogenic Systems for Wireless Applications" Microwave Journal, Euro-Global Edition, Vol. 39, No. 10, pp. 124-36, 1996.
- 13 Romano, A. and Mansour, R.R. and Thomson, F. "A Hybrid Superconductive/Semiconductive Microwave Receiver", IEEE Transactions on Applied Superconductivity, Vol. 7, Iss. 2, pt. 3, pp. 3067-70, 1997.

- 14 Greed, R.B. and Hedges, S.J. "An Integrated High Temperature Superconductor Microwave System/Cryocooler Demonstrator", GEC Journal of Research, Vol. 12, No. 2, pp. 97-111, 1995.
- 15 Hanson, R.C. "Superconductive Antennas", IEEE Transactions on Aerospace and Electronic Systems, Vol. 26, No. 2, pp. 345-55, 1990.
- 16 Herd, J.S. and Hayes, D. and Kenney, J.P. and Poles, L.D. and Herd, K.G. and Lyons, W.G. "Experimental Results on a Scanned Beam Microstrip Antenna Array with a Proximity Coupled YBCO Feed Network", IEEE Transactions on Applied Superconductivity, Vol. 3, No. 1, pp. 2840-43, 1993.
- 17 Lewis, L.L. and Koepf, G. and Bhasin, K.B. and Richard, M.A. "Performance of TlCaBaCuO 30 GHz 64 Element Antenna Array", IEEE Transactions on Applied Superconductivity, Vol. 3, No. 1, pp. 2844-7, 1993.
- 18 Herd, J.S. and Poles, L.D. and Kenney, J.P. and Derov, J.S. and Champion, M.H. and Silva, J.H. and Davidovitz, M. and Herd, K.G. and Bocchi, W.J. and Mittleman, S.D. and Hayes, D.T. "Twenty-GHz Broadband Microstrip Array with Electromagnetically Coupled High T_c Superconducting Feed Network", IEEE Transactions on Microwave Theory and Techniques, Vol. 44, No. 7, pt. 2, pp. 1384-9, 1996.
- 19 Kruse, J. and Chang, W.H. and Scherrer, D. and Gao, F. and Feng, M. and Scharen, M. and Cardona, A. and Forse, R. "Scattering Parameter and Bit Error Rate Characterization of High Temperature Superconducting Coplanar Transmission Lines", IEEE Transactions on Applied Superconductivity, Vol. 5, No. 4, pp. 3518-21, 1995.

- 20 Lyons, W.G. and Arsenault, D.R. and Keast, C.L. and Shaver, D.C. and Berger, R. and Anderson, A.C. and Murphy, P.G. and Sollner, T.C.L.G. and Ralston, R.W. "Wideband Compressive Receiver Based on Advanced Superconductor and Semiconductor Circuits", IEEE Transactions on Applied Superconductivity, Vol. 7, No. 2, pt. 3, pp. 2462-7, 1997.
- 21 Subramayan, G. and Kapoor, V.J. and Bhasin, K.B. "A Hybrid Phase Shifter Circuit Based on TlCaBaCuO Superconducting Thin Films", IEEE Transactions on Microwave Theory and Technique, Vol. 43, No. 3, pp. 566-72, 1995.
- 22 Kaparkov, D. and Sherman, V. and Vendik, I. and Gaidukov, M. and Osadchiy, V. and Petrov, P. and Razumov, S. "Microwave digital phase shifter based on S-N-switching in HTS thin films", Proceeding of EUCAS 1995, Vol. 2, pp. 1139-42, 1995.
- 23 Jackson, C.M. and Kobayashi, J.H. and Durand, D. and Silver, A.H. "A High Temperature Superconductor Phase Shifter", Microwave Journal, Dec. 1992.
- 24 Jackson, C.M. "New Phase Shifters for Smart Systems", SPIE, Vol. 2448, pp. 218-25, 1995.
- 25 Onnes, H.K. "The resistance of pure mercury at helium temperatures", Lieden Comm., 120b, 1911.
- 26 London, F. and London, H. "The Electromagnetic Equations of the Supraconductor", Proceeding of the Royal Society London (A), Vol 149, pp. 71-88, 1935.
- 27 Ginzburg, V.L. and Landau, L.D. "On the Theory of Superconductivity", JETP, Vol. 20, pp 1064-86, 1950.

- 28 Bardeen, J. and Cooper L.N. and Schrieffer, J.R. "Theory of Superconductivity", Physical Review, Vol. 108, No. 5, pp. 1175-1204, 1957.
- 29 Bednorz, J.G. and Muller, K.A. "Possible high Tc superconductivity in the Ba-La-Cu-O system," Z. fur Phys., Vol. 64, pp. 189, 1986.
- 30 Wu, M.K. and Ashburn, J.R. and Torng, C.J. and Hor, P.H. and Meng, R.L. and Gao, L. and Huang, Z.J. and Wang, Y.Q. and Chu, C.W. "Superconductivity at 93K in a new mixed-phase Y-Ba-Cu-O compound system at ambient pressure," Physical Review Letters, Vol. 58, pp. 908, 1987.
- 31 Mattis, D.C. and Bardeen, J. "Theory of Anomalous Skin Effect in Normal and Superconducting Metals", Physical Review, Vol. 111, pp. 412-17, 1958
- 32 Barone, A. and Morini, A. and Frunzio, L. editors. "European Training on Technologies and Industrial Applications of Superconducting," World Scientific, Singapore, 1991.
- 33 Faber, T.E. and Pippard, A.B. Proc. Roy. Soc. (London) A231, 53, 1955.
- 34 Drabek, L. Gruner, G. Chang, J.J. Inam, A. Wu, X.D. Nazar, L. Venkatesan, T. and Scalapino, D.J. "Millimeter Wave Surface Impedance of $Y_1Ba_2Cu_3O_7$ Thin Films", Physical Review B, Vol. 40, pp. 7350-54, 1989.
- 35 Poole, C.P. and Datta, T. and Farach, H.A. "Copper Oxide Superconductors", John Wiley & Sons, Toronto, 1988.
- 36 Anderson, P.W. et. al. "Resonating-Valence-Bond Theory of Phase Transitions and Superconductivity in LaCuO-Based Compounds", Physical Review Letters, pp. 2790-3, June 1987.

- 37 Pond, J.M. "A Computationally Efficient Approach to Microwave Circuit Modeling of Complex High Temperature Superconductor Circuits", IEEE Transactions on Applied Superconductivity, Vol 7, Iss. 2, pt. 3, pp. 3052-5, 1997.
- 38 Dionne, G.F. "New Two-Fluid Superconduction Model Applied to Penetration Depth and Microwave Surface Resistance", IEEE Transactions on Applied Superconductivity, Vol. 3, No. 1, pp. 1465-7, 1993.
- 39 Megahed, M.A. and El-Ghazaly, S.M. "Nonlinear Analysis of Microwave Superconductor Devices using Full-Wave Electromagnetic Model", IEEE Transactions on Microwave Theory and Techniques, Vol. 43, No. 11, pp. 2590-9, 1995.
- 40 Long, Stuart A. and Williams Jeffery T. "High Temperature Superconductors and their Application in Passive Antenna Systems", IEEE Antennas and Propagation Magazine, pp. 7-18, 1990.
- 41 Pettiette-Hall, C.L. and Murdok, J. and Burch, J.F. and Sergeant, M. and Hu, R. and Cordrump, J. and Luong, M. and Ellis, R.K. "Characterization and improvement of a YBCO multilayer film process for HTS circuit applications", IEEE Transactions on Applied Superconductivity, Vol. 7, No. 2, pt. 2, pp. 2057-62, 1997.
- 42 Philips, Julia M. "Substrate selection for high-temperature superconducting thin films", Journal of Applied Physics, Vol. 79, No. 4, pp. 1829-48, 1996.
- 43 Fork, D.K. and Fenner, D.B. and Barton, R.W. and Phillips, J.M. and Connell, G.A.N. and Boyce, J.B. and Geballe, T.H. "High critical currents in strained epitaxial $\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$ on Si", Applied Physics Letters, Vol. 57, No. 11, pp. 1161-3, 1990.

- 44 Konopka, J. and Wolff, I. "Dielectric Properties of Substrates for Deposition of High- T_c Thin Films Up to 40 GHz". IEEE Transactions on Microwave Theory and Techniques, Vol. 40, No 12, pp. 2418-23, 1992.
- 45 Harrington, T.E. and Wosik, J. and Long, S.A. "Open Resonator Mode Patterns for Characterization of Anisotropic Dielectric Substrates for HTS Thin Films", IEEE Transactions on Applied Superconductivity, Vol. 7, No. 2, pp. 1861-64, 1997.
- 46 Schindler, M.J. and Miller, M.E. "A 3 Bit K/Ka Band MMIC Phase Shifter", IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, pp. 95-98, 1988.
- 47 Stenger, E. and Sarantos, M. and Niehenke, E. and Fudem, H. and Schwerdt, C. and Kuss, F. and Strack, D. and Hall, G. and Masti, J. "A Miniature, MMIC One Watt W-Band Solid-State Transmitter", 1997 IEEE MTT-S International Microwave Symposium Digest, Vol. 2, pp. 431-4, 1997.
- 48 Pavlidis, D. and Alekseev, E. and Kyushik Hong and Delong Cui. "InP-Based Millimeter-Wave PIN Diodes for Switching and Phase-Shifting Applications", Solid State Electronics, Vol. 41, No. 10, pp. 1635-9, 1997.
- 49 Garver, Robert V. "Broad-Band Diode Phase Shifters", IEEE Transactions on Microwave Theory and Techniques, Vol. 20, No. 5, pp. 314-23, 1972.
- 50 Lyons, W.G. and Bonetti, R.R. and Williams, A.E. and Mankiewich, P.M. and O'Malley, M.L. and Hamm, J.M. and Anderson, A.C. and Withers, R.S. and Meulengerg, A. and Howard, R.E. "High- T_c Superconductive Microwave Filters", IEEE Transactions on Magnetics, Vol. 27, No. 2, pp. 2537-39, 1991.
- 51 Jackson, R.W. "Coplanar Waveguide vs. Microstrip for Millimeter Wave Integrated Circuits", IEEE MTT-S Digest, pp. 699-702, 1986.

- 52 Koul, S.K. and Bhat, B. "Microwave and Millimeter Wave Phase Shifters Volume II", Artech House, Norwood, 1991.
- 53 Poulin, G.D. and Hegmann, F.A. and Lachapelle, J. and Moffat, S.H. and Preston, J.S. "A Superconductive Microwave Switch", IEEE Transactions on Applied Superconductivity, Vol. 5, No. 2, pt. 3, pp. 3046-8, 1995.
- 54 "COPLAN / Libra A Coplanar Design Tool within HP-EEsof Series IV", Argu-Mens GmbH, Version 2.0, 1996.
- 55 "Sonnet Users Manual Volume 1", Sonnet Software Inc, 1996.
- 56 Ladbroke, Peter H. "MMIC Design: GaAs FETs and HEMTs", Artech House, Boston, 1989.
- 57 Gaidukov, M.M. and Kozyrev, A.B. and Osadchy, V.N. "Microwave phase shifter based on high- T_C superconducting films", Electronics Letters, Vol.21, No. 12, pp. 983-85, 1995.
- 58 Karasik, B.S. and Milostnaya, I.I. and Zorin, M.A. and Elantev, A.I. and Gol'stman G.N. and Gershenzon, E.M. "High Speed Current Switching of Homogeneous YBaCuO Film Between Superconducting and Resistive States", IEEE Transactions on Applied Superconductivity, Vol. 5, No. 2, pp. 3042-45, 1995.
- 59 Kozyrev, A.B. and Osadchy, V.N. and Gaidukov, M.M. and Holmann, E.K. and Razumov, S. and Pavlov, A.S. "Fast high- T_c superconducting transmitter-reciever switch" Electronics Letters, Vol. 33, No. 15, pp.1344-5, 1997.
- 60 Barasik, B.S. and Zorin, M.A. and Milostnaya, I.I. and Elantev, A.I. and Gol'tsman, G.N. and Gershenzon, E.M. "Subnanosecond switching of YBaCuO

- films between superconducting and normal states induced by current pulse”, *Journal of Applied Physics*, Vol. 77, No. 8, pp. 4064-70, 1995.
- 61 Martens, J.S. and Hietala, V.M. and Ginley, D.S. and Tigges, C.P. and Plut, T.A. “HTS-Based Switched Filter Banks and Delay Lines”, *IEEE Transactions on Applied Superconductivity*, Vol. 3, No. 1, pp. 2824-27, 1993.
 - 62 Shkuratov, S.I. “A high- T_c superconducting thin-film switch controlled by a field-emitted electron beam”, *Journal of Physics D*, Vol. 27, No. 2, pp. 376-8, 1994.
 - 63 Peterson, T.L. and Maartense, I. and Biggers, R.R. “Self-Heating Hotspot Effects in HTS Thin Films”, *IEEE Transactions on Applied Superconductivity*, Vol. 5, No. 2, pp. 1436-9, 1995.
 - 64 Avenhaus, B. and Proch, A. and Huang, F. and Lancaster, M.J. “Switched $\text{YBa}_2\text{Cu}_3\text{O}_7$ lumped element bandstop filter”, *Electronics Letters*, Vol. 31, No. 12, pp. 985-6, 1995.
 - 65 Diete, W. and Getta, M. and Hein, M. and Kaiser, T. and Muller, G. and Piel, H. and Schlick, H. “Surface Resistance and Nonlinear Dynamic Microwave Losses of Epitaxial HTS Films”, *IEEE Transactions on Applied Superconductivity*, Vol. 7, No. 2, pt. 2, pp. 1236-9, 1997.
 - 66 Face, D.W. and Wilker, C. and Kingston, J.J. and Zhi-Yuan Shen and Pellicone, F.M. and Small, R.J. and McKenna, S.P. and Shiquan Sun and Martin, P.J. “Advances in HTS Films for High Power Microwave Applications”, *IEEE Transactions on Applied Superconductivity*, Vol. 7, No. 2, pt. 2, pp. 1283-6, 1997.
 - 67 Feng, M. and Gao, F. and Remillard, S. and Lithgow, R. and Scharen, M. and Cardona, A. and Forse, R. “High Temperature Superconducting Resonators and

Switches: Design, Fabrication and Characterization", IEEE Transactions on Microwave Theory and Techniques, Vol. 44, No. 7, pt. 2, pp. 1347-55, 1996.

IMAGE EVALUATION TEST TARGET (QA-3)

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