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**DEVELOPMENT AND CHARACTERIZATION OF
POLYSILICON EMITTER SOLAR CELLS**

by

George Papadopoulos, B.Sc.

**This thesis is submitted to the Faculty of Graduate Studies and Research
in partial fulfilment of the requirements for the degree of**

Master of Engineering

Ottawa-Carleton Institute for Electrical Engineering

Department of Electronics

Faculty of Engineering

Carleton University

Ottawa, Canada

April 1989

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The undersigned recommend to the Faculty of Graduate Studies
and Research the acceptance of the thesis:

**"Development and Characterization of
Polysilicon Emitter Solar Cells"**

submitted by George Papadopoulos in partial fulfilment of the
requirements for the degree of Master of Engineering.

Prof. N. G. Tarr
Thesis Supervisor

Prof. J. S. Wight
Chairman,
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April, 1989

**To my wife Denise,
and to my children,
Takis-Thallis and Maria**

ABSTRACT

The first portion of this research was concerned with the fundamental development and preliminary device characterization of a new poly-Si emitter solar cell structure whose emitter region consists of a thin n^+ poly-Si/ n^+ re-crystallized amorphous silicon (a-Si) bilayer film. The poly-Si bilayer emitter was formed by the sequential LPCVD deposition of a thin in-situ phosphorus doped polysilicon film, forming the junction of the device, followed by a thicker in-situ phosphorus doped a-Si layer that was recrystallized at 650°C to become a high-quality low-resistivity poly-Si film. The bilayer emitter proved capable of reducing the high emitter sheet resistance of earlier monolayer poly-Si emitter solar cells to acceptably low levels, without requiring undesirable high temperature annealing treatments. The bilayer emitter solar cells demonstrated excellent junction diode properties with diode ideality factors of approximately 1.05 over seven decades of current, and very low injection currents of $\sim 10^{-13}\text{A/cm}^2$. Emitter sheet resistances as low as $\sim 550\Omega/\square$ were obtained for films as thin as $\sim 1,000\text{\AA}$, demonstrating the advantage of the bilayer emitter over poly-Si monolayer-emitter solar cells in attaining high fill factors.

The second portion of this research was concerned with the design and optimization of an appropriate front metal contact grid structure to be implemented in conjunction with a reliable metalization scheme suited to poly-Si emitter solar cells. Various metalization schemes, metal deposition processes, and metal diffusion barriers were examined and compared, and an acceptable metallization scheme was identified. High temperature metal diffusion barriers were also investigated, and a very reliable TiWN_x -based barrier was developed for shallow poly-Si emitter devices.

Poly-Si/a-Si bilayer emitter solar cells with primitive single-layer SiO_x antireflection coating have demonstrated a conversion efficiency of $\sim 14\%$ (AM1.5) with the distinct possibility of attaining much higher values when state-of-the-art device design features are implemented. A very high open circuit voltage of 0.65Volts was obtained under one sun illumination conditions (AM1.5) at $\sim 30^\circ\text{C}$ with an uncoated poly-Si/a-Si emitter solar cell having a high-quality float-zone substrate, while fill factors as high as 0.80 were also demonstrated.

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LIST OF SYMBOLS AND ABBREVIATIONS

SYMBOL	DESCRIPTION	UNITS
$a(\lambda)$	Optical Absorption Coefficient	cm^{-1}
a-Si	Amorphous Silicon	
A	x-Dimensional Size of Solar Cell	cm
Al	Aluminum	
Au	Gold	
AM0(1,1.5)	Air Mass Zero (One, One point Five)	
ASEC	Applied Solar Energy Corporation	
ASR(λ)	Absolute Spectral Response	A/W
B	y-Dimensional Size of Solar Cell	cm
BSF	Back Surface Field	
c-Si	Crystalline Silicon	
C(λ)	Collection Efficiency	
E_g	Band Gap Energy	eV
$\mathcal{E}$	Built-in Electric Field	V/cm
FF	Fill Factor	
FZ	Float Zone	
GF	Grid Finger	
h	Plank's Constant 6.626×10^{-34}	J.sec
ITO	Indium-Tin-Oxide	
IR	Infra-Red	
J-V	Current Density - Voltage	
J_m	Current Density at the Maximum Power Point	A/cm^2
J_{ph}	Photogenerated Current Density	A/cm^2

J_{sc}	Short Circuit Current Density	A/cm^2
J_o	Dark Saturation Current Density	A/cm^2
$J_{o,bi}$	Diffusion Current Density of Back-Injected Holes into the Emitter	A/cm^2
$J_{o,e}$	Diffusion Current Density of Electrons Injected into the Base	A/cm^2
$J_{o,r}$	Space Charge ("Excess") Recombination Current Density	A/cm^2
k	Boltzmann's Constant 1.38×10^{-23}	J/K
λ	Wavelength	μm
LOTOX	Low Temperature Oxide	
LPCVD	Low Pressure Chemical Vapour Deposition	
m	Front Contact Grid Geometry Constant (3,4)	
μ	Minority Carrier mobility	$cm^2/V/sec$
n	Diode Ideality Factor	
n	Number of Grid Fingers	
η	Solar Cell Conversion Efficiency	
NRC	National Research Council of Canada	
$N(\lambda,0)$	Incident Photon Flux at the Front Surface of the Solar Cell	$m^{-2}/sec/\mu m$
$N(\lambda, x_{poly})$	Fraction of Photon Flux remaining at a distance x_{poly} from the top surface of the solar cell corresponding to the thickness of the poly-Si emitter layer	$m^{-2}/sec/\mu m$
$N(\lambda, W)$	Fraction of Photon Flux reaching the back surface of the solar, where W is the thickness of the solar cell	$m^{-2}/sec/\mu m$
P_{in}	Incident Solar Irradiance Density	W/cm^2
P_m	Maximum Output Power Density	W/cm^2

Poly-Si	Polycrystalline Silicon	
PR	Photo-Resist	
$P_{AM1.5(\lambda)}$	Spectral Power Density Distribution of the Standard AM1.5 Terrestrial Spectrum	$W/cm^2/\mu m$
P_b	Total Busbar Power Losses	%
P_{cf}	Grid Finger Contact Resistance Power Losses	%
P_f	Total Grid Finger Power Losses	%
P_{rb}	Busbar Resistance Power Losses	%
P_{rf}	Grid Finger Resistance Power Losses	%
P_{sb}	Busbar Shadowing Power Losses	%
P_{sf}	Grid Finger Shadowing Power Losses	%
P_{tl}	Lateral Current Flow Resistance Power Losses	%
P_{tot}	Total Front Surface Power Losses	%
q	Elementary Charge 1.6×10^{-19}	Cb
$R(\lambda)$	Reflection Coefficient	
RBS	Rutherford Backscattering Spectrometry	
R_s	Series Resistance	$\Omega \cdot cm^2$
R_{sh}	Shunt Resistance	$\Omega \cdot cm^2$
r	Emitter Sheet Resistance	$\Omega/\square$
r_{sm}	Metal Grid Sheet Resistance	$\Omega/\square$
ρ_c	Specific Contact Resistance	$\Omega \cdot cm^2$
ρ_{sm}	Metal Grid Resistivity	$\Omega \cdot cm$
S	Grid Finger Spacing	cm
SiO_x	Silicon-Oxide (Combination of Monoxide and Dioxide)	
SIMS	Secondary Ion Mass Spectroscopy	
σ	Photogenerated Carrier Drift Traveling Distance	V/cm
τ	Minority Carrier Lifetime	sec

t	Front Metal Grid Thickness	cm
T	Absolute Temperature	K
TEM	Transmission Electron Microscopy	
Ti	Titanium	
TiW	Titanium-Tungsten	
TiWN _x	Titanium-Tungsten-Nitride	
UV	Ultra-Violet	
u	Normalized Output Voltage	
V	Output Voltage of Solar Cell	Volts
V_m	Output Voltage at the Maximum Power Point	Volts
V_{oc}	Open Circuit Voltage of Solar Cell	Volts
VdP	Van der Pauw	
W_B	Average Width of Linearly Tapered Busbar	cm
W_{bb}	Full Width of Linearly Tapered Busbar	cm
W_f	Grid Finger Width	cm
$\Omega/\square$	ohms/square	

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Substantial improvements in solar cell performance have been achieved over the last decade. However, most of these improvements were attributed mostly to increases in short circuit currents and fill factors that have reached their fundamental limitations. More recently, approaches on further efficiency improvements emphasize open circuit voltage improvements rather than short circuit currents since the open circuit voltage has become the major limitation factor towards the attainment of very high efficiencies.

In order to maximize the open circuit voltage of a solar cell, injection currents have to be minimized first, followed by a reduction in both bulk and surface recombination effects. Polysilicon emitter contacts have been used in the early and mid 80's to reduce the back-injection current in bipolar transistors, improving substantially their performance [AsSo84]. However, it was not until the mid-80's that poly-Si contacts have been applied to solar cells. Green and Blakers [GrB183] have demonstrated enhancements in the open circuit voltage of MINP structure solar cells by incorporating polysilicon contacts on the front surface of such cells to reduce the front surface recombination velocity. Lindholm et al [LNAI85] have also demonstrated that both n^+ and p^+ polysilicon back surface fields can give further enhancements not only in the red spectral response but on the open circuit voltage of solar cells as well.

Recently, polysilicon emitter bipolar transistors have demonstrated very low back-injection currents that resulted in substantial improvements on the performance of such devices [RoTa85], [KeTa87]. It was the very low back-

injection current observed in these polysilicon emitter bipolar transistors that lead to the development of a new solar cell structure at Carleton U. [Tarr85], which employed a thin continuous layer of in-situ phosphorus doped polysilicon as the entire emitter region of the device. However, this work was aimed not at optimizing the device performance but rather in examining whether solar cells with this emitter structure would attain high open circuit voltages by exploiting the low back injection current of the poly-Si emitter structure. Even though a diode quality factor of ~ 1.1 over seven decades of current was observed and a high open circuit voltage of $\sim 650\text{mV}$ was attained, a low fill factor (FF) of ~ 0.62 , resulting from a high series resistance, restricted the efficiency of the device to relatively low levels for a crystalline silicon based solar cell.

The effect of series resistance on the fill factor and efficiency of a solar cell is shown in Figures 1.1.1 and 1.1.2 respectively. Numerical calculations were done using the following analytical expressions for the photogenerated power at the maximum power point and for the fill factor, derived by [Sing80], showing an explicit dependence on series resistance with an estimated error of less than 1%.

For $R_s \neq 0$, and assuming that the shunting resistance (R_{sh}) is very large, the maximum power point (P_m) is given by,

$$P_m = J_m V_m \quad (1.1.1)$$

where,

$$J_m = J_{ph} \left\{ 1 - \frac{1}{v+1-\ln v} - \frac{2R_s J_{ph}}{V_{oc}} \frac{v(v-\ln v)}{(v+1-\ln v)^3} \right\} \quad (1.1.2)$$

$$V_m = V_{oc} \left\{ 1 - \frac{1}{v} \ln(v+1-\ln v) + \frac{1}{v} \ln \left[1 + \frac{2R_s J_{ph}}{V_{oc}} \frac{v(v-\ln v)}{(v+1-\ln v)^2} \right] - \frac{R_s J_{ph}}{V_{oc}} \frac{v-\ln v}{v+1-\ln v} + \left(\frac{R_s J_{ph}}{V_{oc}} \right)^2 \frac{2v(v-\ln v)}{(v+1-\ln v)^3} \right\} \quad (1.1.3)$$

and,

$$v = \frac{V_{oc}}{n} \frac{q}{kT} \quad (1.1.4)$$

Figure 1.1.1 : Effect of series resistance on the fill factor of a solar cell

Figure 1.1.2 : Effect of series resistance on the efficiency of a solar cell

The fill factor (FF) can then be obtained from the maximum output power (P_m), the photogenerated current (J_{ph}) and the open circuit voltage (V_{oc}) using the following relationship,

$$FF = \frac{P_m}{J_{ph} V_{oc}} \quad (1.1.5)$$

while the solar cell efficiency (η) is obtained from the maximum output power (P_m) and the input power (P_{in}), where

$$\eta = \frac{P_m}{P_{in}} \quad (1.1.6)$$

An input total light power density of 83.18 mW/cm^2 [FaBu83] corresponding to 1.5 air mass factor, and a photogenerated current density (J_{ph}) of 30 mA/cm^2 , were assumed in the numerical calculations.

Figure 1.1.1 shows a ~5% increase in fill factor for every 1Ω decrease of R_s in the V_{oc}/n range between 500mV-600mV, while for the same rate of decrease in R_s the efficiency increases by ~1%, as shown in Figure 1.1.2, reaching a maximum value when R_s is zero. Therefore, in order to improve the fill factor and thus the efficiency of the solar cell, the series resistance of the device must be minimized. The principal series resistance losses come from the spreading resistance of the emitter and the voltage drop along the front metal grid contact. These two particular resistive components cannot be eliminated completely because they are involved in design compromises which determine the cell efficiency. Other factors which contribute to R_s , such as the metal-semiconductor contact resistance and the bulk resistance effects of the substrate can be made negligible by proper cell design [GrBl87] and fabrication methods which will not be dealt with here.

This thesis will deal with the evolution of a poly-Si/Recrystallized amorphous silicon (a-Si) bilayer emitter which reduces the high emitter sheet resistance of the original poly-Si emitter solar cells [Tarr85], while maintaining a good junction diode quality and a low dark saturation current.

1.2

THESIS OBJECTIVES

The main objective of this thesis was to investigate and implement various top layer processing and device design techniques that would improve the relatively poor fill factor and consequently the moderate photovoltaic performance of the original unoptimized in-situ phosphorus doped poly-Si monolayer-emitter solar cell reported in [Tarr85].

The first part of the device improvements was to reduce the high sheet resistance of the original poly-Si monolayer emitter to acceptably low levels without using high temperature furnace annealing treatments that could degrade both the advantageous low back injection properties associated with the poly-Si emitter and the lifetimes of the minority carriers in the substrate bulk. At the same time the poly-Si emitter had to be kept as thin as possible in order to avoid a loss in short wavelength response. To comply with the processing constraints and device performance compromises, an alternative LPCVD in-situ phosphorus doped poly-Si emitter processing approach, involving the sequential deposition of a very thin poly-Si layer followed by a thicker amorphous silicon film that could be recrystallized by a low temperature annealing treatment at a later step to form a high-quality low-resistivity poly-Si film, was investigated. To determine the best poly-Si emitter thickness, the sheet resistance of such bilayer films had to be determined and compared over a wide thickness range with poly-Si monolayer films and recrystallized a-Si films of similar thickness. In addition, the junction diode quality, particularly the back injection component of the dark saturation current, had to be examined in order to determine whether solar cells fabricated with such a processing approach could maintain the desirable high diode quality and low back-injection properties of the original poly-Si monolayer emitter. The

short wavelength response of poly-Si/a-Si bilayer emitter solar cells had also to be investigated for different bilayer film thicknesses in order to determine the severity of short wavelength photocurrent losses.

The second part of device improvement, aimed at increasing both the fill factor of the poly-Si emitter solar cells and their overall photovoltaic performance, required the design of a front metal current-collecting grid structure that could be implemented using available photolithographic techniques and which would minimize both the combined resistive effects associated with the top layer of the solar cells and the optical losses associated with shadowing effects. In addition, various front contact metallization schemes and metal deposition processes that could be implemented using available deposition equipment and materials had to be investigated in order to establish an acceptable and reliable front metal contact. The metal deposition processes had to yield a highly conducting metal layer of $\sim 5\mu\text{m}$ thickness in order to minimize grid-related parasitic resistive effects. The metallization scheme had to provide good adhesion to poly-Si, a relatively low contact resistivity, and most importantly it had to be thermally stable. The latter metallization requirement necessitated the investigation of acceptable metal diffusion barriers that could be implemented as part of the front metal contacts.

Finally, the magnitude of the total photocurrent losses associated with the poly-Si/a-Si bilayer emitter region of the solar cells had to be determined, while the general photovoltaic performance of the poly-Si/a-Si bilayer emitter cells had to be assessed and compared to that of a shallow phosphorus predeposited crystalline silicon (c-Si) emitter solar cell with a similar emitter thickness. Poly-Si/a-Si bilayer emitter solar cells with different quality substrates were also investigated to determine substrate effects on the photovoltaic performance.

1.3

THESIS OUTLINE

This thesis is divided into 5 chapters. The first chapter provides a brief background, and introduces the thesis objectives. Chapter 2 details the evolution of the poly-Si/a-Si bilayer emitter and describes the device structure and the processing procedure used to fabricate the poly-Si/a-Si emitter solar cells in this work. The dark saturation current characteristics and the junction diode quality of the poly-Si/a-Si emitter solar cells are presented and discussed in this chapter as well. A preliminary theoretical estimate of the magnitude of the total photocurrent losses expected with the utilization of such a poly-Si emitter is also presented along with the experimental short wavelength response of poly-Si/a-Si bilayer emitter solar cells with different emitter thicknesses, as obtained from absolute spectral response measurements. Chapter 3 details the design strategy used to optimize the front contact current collecting grid structure that was implemented in this work, while the front contact metallization schemes (Ti/Al, $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Au}$, $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Al}$), metal deposition processes (e-beam evaporation, sputtering, electroplating) and metal diffusion barriers (Ti, $\text{Ti}_{0.1}\text{W}_{0.9}$, $\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x$) examined, are also presented and compared in this chapter. Chapter 4 examines and evaluates the photovoltaic performance of the poly-Si/a-Si bilayer emitter solar cells under various illumination conditions, while an assesment of the total photocurrent losses associated with the emitter region of these devices is also presented based on experimental results obtained from natural sunlight photocurrent measurements as well as from absolute spectral response measurements covering the entire utilizeable solar spectrum. Finally, Chapter 5 contains a summary of the research, draws conclusions, and makes recommendations for future work.

CHAPTER 2

DEVELOPMENT OF THE POLY-Si/RECRYSTALLIZED a-Si BILAYER EMITTER SOLAR CELL AND PRELIMINARY CHARACTERISTICS

2.1 POLY-Si Emitter Sheet Resistance AND EVOLUTION OF THE POLY-Si/a-Si BILAYER Emitter

A high collection efficiency and good blue response demand a thin n^+ doped emitter layer which implies a high sheet resistance and a correspondingly high spreading resistance [Hall81]. The effect of spreading resistance can be minimized by careful design of the front grid contact, an issue which will be dealt with separately in Chapter 3. This subsection will deal with various techniques for improving the emitter's quality and sheet resistance.

Apart from the thickness of the emitter layer, the sheet resistance of the emitter is also affected by the structure of the deposited material, deposition parameters (i.e dopant concentration, dopant species, deposition rate, deposition temperature, etc.), post-deposition conditions and the actual fabrication method used. Learn et al [LeFo87] reported that poly-Si layers with lower resistivities were obtained with phosphorus in-situ doping by LPCVD as compared to post deposition doping from a $POCl_3$ source, because of the more uniform incorporation of phosphorus in the former case throughout the deposited layer which promotes enhanced grain growth and thus results in larger grain sizes. Regardless of the fabrication method used, the sheet resistance of the as-deposited phosphorus doped polysilicon is often relatively high unless it is subjected to high

temperature annealing [Waec87]. Although thermal annealing at 900°C has been found to reduce the resistivity of poly-Si by an order of magnitude [WaTa88], exposure to such high temperatures may degrade the effectiveness of the poly-Si layer in reducing the dark saturation current.

In initial work done on poly-Si emitter solar cells [Tarr85], poly-Si layers were grown to thicknesses between 500Å and 1,000Å in order to minimize the expected loss in blue response due to low lifetimes and short diffusion lengths of the photogenerated carriers in this region [GhFF80] that result from carrier trapping effects at the grain boundaries of the fine-grained poly-Si material. However, the sheet resistance values of these emitter layers were in the 2-6kΩ/□ range, and are believed to have been partially contributed to a high series resistance that limited the fill factor of the devices to low levels as explained in Subsection 1.1. Desirable emitter sheet resistances should lie in the 100-500Ω/□ range, and in conjunction with a good front grid contact high fill factors of ~0.82 can be attained [GBSK84]. For a poly-Si material to reach such levels of sheet resistance, a layer more than 2,000Å thick is required followed by a high temperature annealing [Weac87], both of which can have undesirable effects on the performance of the emitter by degrading the blue response and increasing the back injection current respectively. Therefore, it is necessary to utilize an alternative processing procedure or a different top layer device design that would reduce the emitter sheet resistance to acceptable levels while maintaining a low dark saturation current.

It is known that in-situ phosphorus doped silicon, deposited in the amorphous phase by LPCVD techniques and crystallized later to become poly-Si, has a better structural quality and lower resistivity than as-deposited poly-Si

[HKS83]. However, recently Keyes [Keye87] reported poor junction qualities for in-situ n^+ doped amorphous silicon emitter diodes recrystallized at 650°C , that showed a high depletion region recombination which improved only when the annealing temperature was increased to 900°C . Even though such a processing procedure would satisfy the low sheet resistance requirement, it could infer a decrease in the high open circuit voltage of the solar cell.

The constraints set by the high sheet resistance of the poly-Si material and the inadequacy of a-Si to form a good junction with the crystalline silicon substrate [Keye87] lead to the evolution of the poly-Si bilayer emitter structure shown in Figure 2.1.1, composed of a thin n^+ poly-Si layer forming the junction of the device, and followed by a layer of n^+ amorphous silicon which is recrystallized at 650°C to become high quality poly-Si. The purpose of this emitter structure is to exploit the best properties of both layers. The thin as-deposited n^+ poly-Si layer acts as a buffer impeding the injection of majority carriers to opposite sides of the junction while maintaining a low recombination rate in the depletion region, discussed in more detail in Subsection 2.3, and the top n^+ amorphous recrystallized layer providing low emitter sheet resistances, thus improving the fill factor of the device.

Besides the dopant concentration which is known to affect the sheet resistance of poly-Si films [Weac87], there is a thickness dependence of the sheet resistance in in-situ doped poly-Si films [LLLS84], [LeFo87], which becomes more pronounced at high levels of doping [LLLS84]. Figure 2.1.2 A),B) shows the sheet resistance and resistivity variation with film thickness respectively, for as-deposited n^+ poly-Si films, n^+ amorphous recrystallized poly-Si films, and n^+ poly-Si/ n^+ amorphous recrystallized poly-Si bilayer films. P-type $\langle 100 \rangle$ substrates were

Figure 2.1.1: Simplified schematic diagram of the n⁺ poly-Si bilayer emitter structure.

Figure 2.1.2: Measured sheet resistance (A) and resistivity (B) versus film thickness, for n^+ poly-Si, n^+ a-Si, and n^+ poly-Si/a-Si films. The thickness of the bilayer film is varied according to the a-Si film thickness while keeping the poly-Si film thickness fixed at $\sim 200\text{\AA}$.

used with a 1,000Å of thermally grown oxide to provide electrical isolation of the deposited films from the substrate. Depositions were carried out by in-situ phosphorus doping using a LPCVD reactor, with poly-Si films grown at 627°C from a 185/1 ratio of SiH₄/PH₃ mixture and a-Si films grown at 560°C from a 530/1 ratio of a SiH₄/PH₃ mixture. In the poly-Si/a-Si bilayer films approximately 200Å of poly-Si was first grown at 627°C followed immediately by an a-Si deposition at 560°C, while the bilayer film thickness was controlled by varying the a-Si deposition time. All the a-Si films and the poly-Si/a-Si films were recrystallized at 650°C in a N₂ ambient. Sheet resistance measurements were done using the Four Point Probe method, and an average value was taken from several measurements done across each wafer. Van der Pauw (VdP) crosses were also formed in some wafers by patterning half of each wafer so that both Four Point Probe and Van der Pauw (VdP) cross sheet resistance measurements could be taken on the same wafer. The results from the two methods were in very good agreement, having a difference of less than 5%. Thickness measurements were performed with a DEKTAK IIA surface profilometer and an average value was taken from several scans done on each wafer.

For all three poly-Si configurations shown in Figure 2.1.2 there is an increase in sheet resistance with decreasing film thickness which becomes sharp below a certain film thickness range that depends on the poly-Si configuration. It is known that for a given doping concentration the mobility of carriers in poly-Si films is a strong function of the grain size [NiIs80] with larger grain sizes associated with higher mobilities as well as longer effective lifetimes and diffusion lengths [GhFF80]. TEM micrographs [LLLS84] have shown a decrease in the grain size of poly-Si crystallites with poly-Si film thickness reduction, while a sharp increase in sheet resistance with decreasing grain size has also been

reported. It has been suggested that at a given dopant concentration level there is a critical grain size below which most of the poly-Si crystallites go from partial depletion to total depletion resulting in a drastic reduction of the free carriers available for conduction. For very high dopant concentration levels, 10^{20} - 10^{21} atoms/cm³, the poly-Si crystallites can only be partially depleted [MaSK81] and it is believed that instead of total grain depletion there is rather a partial grain depletion which increases with decreasing grain size. Such an effect could explain the exponential increase in sheet resistance with decreasing film thickness in all three poly-Si configurations. However, careful structural analysis and characterization of very thin n⁺ doped poly-Si films is lacking today and more work is required in this area for a better understanding of this effect.

It must be pointed out that due to a higher phosphorus incorporation in disordered a-Si films [WaTa88], even though the silane to phosphine ratio was three times lower in the a-Si depositions as compared to that used in the poly-Si depositions, the phosphorus concentration in the a-Si films has been found to be at the same level ($\sim 2.5 \times 10^{20}$ cm⁻³) with that of the in-situ phosphorus doped poly-Si films as deduced from SIMS measurements reported by Waechter [Waec87] in earlier similar work. Therefore, since the dopant concentration for the three poly-Si configurations are similar, their sheet resistance difference at a given film thickness is attributed mostly to the different grain structure pattern of the corresponding poly-Si configurations. X-ray diffractions and TEM studies [HKS83] have indicated that in-situ phosphorus doped recrystallized a-Si films have a <111> grain orientation and larger average grain sizes than as-deposited phosphorus doped poly-Si films which display a <311> grain orientation.

Sheet resistances less than 500 $\Omega/\square$ were obtained with the poly-Si/a-Si configuration for films thicker than 1,100Å. In the entire film thickness range

considered here, the sheet resistance of the bilayer films is lower by a factor of $\sim 4-5$ as compared to as-deposited poly-Si films, while it is only higher by a factor of $\sim 1.3-1.5$ for corresponding a-Si recrystallized films. The small deviation in sheet resistance of the bilayer films from the single a-Si films, as well as their similarity in the sheet resistance profile with respect to thickness, indicate that the utilization of the $\sim 200\text{\AA}$ thin poly-Si layer in the bilayer film configuration has a small effect in the determination of the sheet resistance of these films which is rather dominated by the adjacent recrystallized a-Si layer's structural properties. However, if the bilayer films utilize thicker as-deposited poly-Si layers it is expected that the bilayer sheet resistance deviation from the a-Si sheet resistance profile will increase.

Because of the sharp increase in sheet resistance below a certain film thickness in in-situ phosphorus doped poly-Si films, even though the poly-Si/a-Si bilayer films exhibit a significant reduction in sheet resistance especially for films thicker than $900\text{\AA}$, the utilization of a poorly chosen film thickness can critically affect the magnitude of the series resistance of the solar cell and consequently its fill factor. Considering the compromises that have to be made between the loss in blue response when utilizing a thick poly-Si layer and the high sheet resistance of a thin poly-Si film, a better top layer optimization can be made once the film thickness range where the sharp transition in sheet resistance takes place has been identified. For the poly-Si/a-Si configuration such a transition occurs in the vicinity of $\sim 900\text{\AA}$ where sheet resistances are in the $700\Omega/\square$ range and go as high as $4\text{k}\Omega/\square$ when the film thickness is reduced to $\sim 550\text{\AA}$. Thus, taking into consideration the sheet resistance variation with respect to film thickness, the solar cells fabricated in this work utilized poly-Si/recrystallized a-Si bilayer emitter layers with target thicknesses in excess of $900\text{\AA}$ achieving sheet resistances as low as $300\Omega/\square$ for emitter thicknesses less than $1,500\text{\AA}$.

2.2 STRUCTURAL DESIGN AND DEVICE FABRICATION OF LPCVD IN-SITU PHOSPHORUS DOPED POLY-SI/a-SI BILAYER EMITTER SOLAR CELLS

A simplified cross-sectional diagram of the Poly-Si/Recrystallized a-Si bilayer emitter solar cell structure is shown in Figure 2.2.1. All solar cells were fabricated on 5-cm diameter p-type single crystal silicon wafers of <100> orientation. The doping levels of the substrates were in the range of 10^{15} - 10^{16}cm^{-3} , and their thicknesses were approximately 300 μm . A wide range of different bulk resistivities - 0.07-0.135 $\Omega\cdot\text{cm}$ Float-Zone(FZ), 0.375-0.625 $\Omega\cdot\text{cm}$ (FZ), 1.8-2.6 $\Omega\cdot\text{cm}$, 3.2-4.2 $\Omega\cdot\text{cm}$ and 8.0-10.0 $\Omega\cdot\text{cm}$ - was selected in order to examine how the quality of the substrate itself affects individual output parameters of the solar cell. Low bulk resistivity high quality FZ substrates are known to give higher open circuit voltages [GBJK84] because they are associated with minimum bulk recombination rates, while high bulk resistivity substrates result in higher short circuit currents as they are usually associated with longer diffusion lengths.

The mask set used for the patterning of the wafers included a 2x2cm cell, two 0.5x0.5cm test cells, several diodes of different sizes, Van der Pauw crosses for emitter sheet resistance measurements, and Kelvin resistors for measurements of the emitter to metal contact resistivity. A metal mask layout showing all these patterns is shown in Figure 3.2.9 in the following Chapter.

The wafers were initially RCA cleaned to remove any organic and metal contaminants from the surface as well as any residual oxide. A Lotox deposition of $\sim 2000\text{\AA}$ of SiO_2 followed in order to provide some degree of surface passivation. After device wells were opened in this oxide, the wafers were RCA cleaned, flash

Figure 2.2.1: Cross sectional diagram of a typical n⁺poly-Si/n⁺recrystallized a-Si bilayer emitter solar cell.

dipped in 10% hydrofluoric acid (HF) until windows turned hydrophobic, and then spun dry and loaded as rapidly as possible into a (Low Pressure Chemical Vapour Deposition) LPCVD reactor in order to minimize growth of an interfacial native oxide.

The emitter layer was deposited in two consecutive steps without exposing the wafers to atmospheric conditions in between. The first deposition was carried out from a 185/1 silane to phosphine mixture at a temperature of 627°C and a pressure of ~0.3Torr growing a very thin polysilicon layer in the vicinity of 200Å. Then the reaction gases were shut off and pumped out of the system while a continuous N₂ flow was maintained until the tube temperature was reduced to 560°C. The second deposition was then carried out from a 530/1 silane to phosphine ratio at a pressure of ~0.3Torr growing an amorphous silicon (a-Si) layer with preselected target thickness varying from run to run in order to achieve a range of total emitter thicknesses between 900Å and 1,600Å. The chemical phosphorus concentration from SIMS measurements is estimated to be roughly in the $2-5 \times 10^{20} \text{cm}^{-3}$ range for both polysilicon and amorphous silicon layers.

A 60min annealing step at 650°C was performed in N₂ to recrystallize the amorphous silicon layer. It should be stressed here that no high temperature treatment was carried out after this step, so the highest temperature to which the wafers were exposed in the whole process sequence was 650°C. During patterning of the emitter area, many tiny pinholes were observed in isolated areas due to various imperfect processing conditions, and thus it was decided to retouch these areas with positive PR (Photo-Resist) using a fine brush. This method proved effective in reducing substantially the number of pinholes which otherwise would have resulted in a significant leakage current that would degrade the output characteristics of the solar cell.

Back contacts to the cells were made with a $\sim 2\mu\text{m}$ thick aluminum film deposited by e-beam evaporation after an initial brief etch of the back surface in 10% HF to remove any residual oxide. Sintering of the aluminum was performed at 450°C in a hydrogen ambient for 20min to ensure the contact was ohmic. Different metallization schemes were used for the front contact grid with most wafers receiving a $\sim 1,000\text{\AA}$ sputtered layer of TiW followed by either a $4\text{-}5\mu\text{m}$ e-beam Al or a $5\text{-}8\mu\text{m}$ thick layer of electroplated Au. Hydrogen annealing steps at $400\text{-}450^\circ\text{C}$ were performed to remove the damage created during the sputtering and e-beam metal depositions. More details about the front contact grid and metallization schemes will be presented in Chapter 3.

Finally, a single-layer antireflection coating of $\sim 750\text{\AA}$ SiO_x having a ~ 1.8 refractive index was deposited on some solar cells by thermal evaporation from a SiO_x powder source of 2.13gm/cm^3 density. Figure 2.2.2 shows the main processing steps involved in the fabrication of most of the $n^+\text{poly-Si}/n^+\text{a-Si}$ bilayer emitter cells, while a more detailed outline of the entire fabrication process is listed in Appendix 1.

A phosphorus predeposited crystalline silicon emitter control solar cell was also fabricated using a conventional diffusion furnace. The predeposition was performed at 850°C from a POCl_3 source with a 21/1 O_2 to POCl_3 concentration ratio [MaNS77], [NeNS75], [GBGW82] and a N_2 carrier gas flow of 1.7slpm. The predeposition time was kept very short (90sec) in order to create a shallow junction depth of $\sim 1,500\text{\AA}$ with a target sheet resistance of $\sim 400\Omega/\square$ that would be comparable with the poly-Si bilayer emitter solar cells of this work. The phosphorus concentration of the emitter layer was estimated to be $\sim 2 \times 10^{20}\text{cm}^{-3}$ from SUPREM III. A more detailed fabrication outline is listed in Appendix 2.

Figure 2.2.2: Main processing steps involved in the fabrication of a typical n^+ poly-Si/ n^+ a-Si bilayer emitter solar cell.

2.3 EMITTER DARK SATURATION CURRENT

Low emitter dark saturation currents have become one of the most critical requirements for the attainment of very high open circuit voltages in solar cells. The origin of the low dark saturation current associated with the n^+ poly-Si bilayer emitter implemented in the solar cells of this work will be examined in this subsection, while a correlation will be shown between the minority carrier transport and the bulk properties of the $\sim 200\text{\AA}$ n^+ poly-Si layer that forms the interface with the substrate.

Results from high quality $0.1\Omega\cdot\text{cm}$ FZ substrates show very high open circuit voltages ($\sim 650\text{mV}$) under AM1 conditions at $\sim 28^\circ\text{C}$ without the incorporation of an antireflection coating. This is one of the highest open circuit voltages reported for c-Si based solar cells and it is the result of two factors, one being the low recombination rate in the high quality substrate and the other being the emitter's low back-injection component of dark saturation current.

The magnitude of the n^+ poly-Si emitter's dark saturation current is determined by the hole diffusion current component injected from the p-type substrate into the poly-Si emitter, recombination effects that occur at the monosilicon/poly-Si junction interface, and the diffusion of electrons in the bulk substrate. Recombination effects at the front surface and under the top metal contact are negligible due to the very short diffusion lengths of the minority carriers in the highly doped and disordered poly-Si emitter bilayer configuration. Shunt resistance effects are usually negligible in large area ($\sim 4\text{cm}^2$) n^+/p solar cells and thus the total dark saturation current density J_0 can be written as:

$$J_0 = (J_{0,ei} + J_{0,bi})[\exp(qV/kT) - 1] + J_{0,r}[\exp(qV/nkT) - 1] \quad (2.3.1)$$

where $J_{0,ei}$ is the diffusion current density component due to electrons

injected into the base, $J_{0,bi}$ is the equivalent diffusion current density component due to back injection of holes into the emitter, and $J_{0,r}$ is a composite "excess" current density component due to recombination effects characterized by an ideality factor "n" where $1 < n < 2$.

Recombination at the grain boundaries of the poly-Si material is the major contribution to the "excess" current density and its magnitude can be a determining factor for the attainment of ultimate open circuit voltages. An increase of ~5mV was observed in the open circuit voltage of the n^+ bilayer emitter solar cells after a 20min hydrogen annealing at 450°C which was performed mainly to remove the damage introduced in the top recrystallized a-Si layer of the bilayer emitter during the e-beam/sputtering depositions involved in the metallization process. The increase in the open circuit voltage is associated with a reduction in the "excess" current density as shown from the dark J-V characteristics of a small diode in Figure 2.3.1, where a shift of the curve's reciprocal slope factor "n" from $n=1.67$ to $n=1.05$ takes place at low forward bias voltages after the hydrogen annealing treatment. An improvement in series resistance is also observed at high current levels believed to be attributed to a ~25% reduction in the emitter sheet resistance from a value of $\sim 480\Omega/\square$ to $\sim 360\Omega/\square$ in this particular case as indicated from Van der Pauw cross sheet resistance measurements before and after hydrogen annealing. Crystal regrowth, dopant activation or even passivation of dangling bonds due to phosphorus segregation at the grain boundaries is unlikely to occur at such low temperatures. A possible explanation may lie on hydrogen passivation of defect centers at the grain boundaries where the hydrogen may have preferentially diffused during the above mentioned heat treatment. Such an effect will reduce recombination at the grain boundaries explaining the reduction in the "excess" current density, while

Figure 2.3.1: Dark J-V characteristics of a 400x400μm n⁺ poly-Si bilayer emitter diode (A) before and (B) after hydrogen annealing at 450C° for 20min.

the reduction of the emitter's sheet resistance implies higher carriers mobilities associated with a possible reduction of the grain boundaries potential barriers as a consequence of defect passivation at the grain boundaries.

For a solar cell operating under one sun solar illumination, the injection current, being the dominant component of the dark saturation current at high current levels, will set an upper bound on the open circuit voltage of the device. The limitation of the open circuit voltage V_{oc} on the injection current density ($J_{o,ei}+J_{o,bi}$) can be described using the following simplified relationship,

$$V_{oc} \approx \frac{kT}{q} \ln\left(\frac{J_{ph}}{J_{o,ei}+J_{o,bi}}\right) \quad (2.3.2)$$

where J_{ph} is the photogenerated current density. From this expression it is straightforward that $J_{o,bi}$ needs to be as small as possible for maximum V_{oc} values to be attained.

Even though the use of a bipolar transistor is the most accurate method for measuring the back injection current, the dark J-V characteristics of a diode can also be used to deduce an upper bound on $J_{o,bi}$. Figure 2.3.2 shows a dark J-V characteristic for one of the diodes fabricated on a high quality substrate having an area of $400 \times 400 \mu m$. An almost ideal diode behavior is observed for approximately seven decades of current with an ideality factor of ~ 1.05 . An injection current density value of $\sim 2 \times 10^{-13} A/cm^2$ was estimated by linear extrapolation to zero forward bias from a J value of $\sim 20 mA/cm^2$ on the $\log(J)$ curve corresponding to 650mV using a slope of q/kT . This value correlates very well with findings from n^+ poly-Si emitter bipolar transistors [Keye87] fabricated with the same basic process used in this work, where high emitter Gummel numbers in the range of $10^{13} scm^{-4}$ to $10^{15} scm^{-4}$ observed in these devices

Figure 2.3.2: Dark J-V characteristics of a n^+ poly-Si bilayer emitter diode having an area of $400 \times 400 \mu\text{m}$, showing an almost ideal diode quality factor of ~ 1.05 and an injection current density of $2 \times 10^{-13} \text{ A/cm}^2$.

translate into very low back injection currents of 10^{-12} to 10^{-14} A/cm².

Reproducible device characteristics and back injection currents were successfully obtained in this work. However, it has to be noted here that during fabrication a changing offset value was observed in the phosphine mass flow controller of the LPCVD system prior to each poly-Si deposition which was taken into account in determining the actual phosphine flow in the reactor tube during deposition, thus having control over the as-deposited phosphorus doped poly-Si layer's structural and electrical properties. It is believed that the offset irregularity of the mass flow controller which passed unnoticed during previous work in n^+ poly-Si emitter bipolar transistors [Keye87] was the cause of the large variation on device characteristics observed on different deposition runs in that work, since apart from the dopant concentration level the amount of phosphine introduced during the in-situ deposition of poly-Si affects the nucleation, crystallization growth and thus the grain size of the poly-Si crystallites.

Several theories [DeDe79], [NiIs80], [NAKI85], [ElRo82], [AsSo84]] have been proposed to explain the very low back injection current in poly-Si contacted emitter devices. Among those theories it has been postulated [DeDe79] that the presence of an interfacial native oxide between the poly-Si and the single crystal silicon substrate acts as a tunnelling barrier to hole injection into the polysilicon, while an alternative theory [NiIs80] has suggested that the minority carrier transport is controlled by the bulk properties of the poly-Si layer itself characterized by a low minority carrier mobility that retards the transport of the injected minority carriers. Other theories have also included bandgap narrowing due to high doping effects [ChGG88] and quantum reflection of minority carriers at the interface [RoTa85]. The variety of interpretations given for the back injection current suppression mainly arises due to the different processing

techniques involved among various research groups including the poly-Si/Si interface treatment prior to poly-Si deposition, the processing method used to deposit and dope the poly-Si layer, as well as post heat treatment effects, all of which result in different poly-Si structural qualities.

As mentioned in Subsection 2.2, flash HF etching was performed prior to the polysilicon deposition for the devices fabricated in this work in order to remove any native oxide that might have been present on the surface of the p-type substrates. Despite this treatment an unintentional oxide may inevitably grow on the substrate surface as a consequence of the short exposure of the wafers in air during loading in the LPCVD system and the pump down cycle that follows prior to deposition. However, high resolution transmission electron microscopy (TEM) [BrPP85] has shown nearly oxide-free interfaces for specimens etched in HF prior to poly-Si deposition, while results from Auger electron spectroscopy [Duff82] indicate that the thickness of such an oxide layer is less than $2\text{\AA}$. Eltoukhy et al [ElRo82] examining the effect of various interfacial oxide layer thicknesses on the device characteristics of polysilicon contacted emitter transistors, reported that tunneling transport dominates for oxide thicknesses in excess of $20\text{\AA}$. Therefore, it is doubtful whether the presence of an ultra thin unintentional interfacial oxide in the devices fabricated in this work can act as a tunneling barrier in suppressing hole injection across the junction.

Neugroschel et al [NAKI85] have suggested that the minority carrier transport in in-situ doped poly-Si emitter devices is controlled by a highly disordered thin interfacial layer within $\sim 300\text{\AA}$ of the n^+ poly-Si/Si interface in the poly-Si layer. High resolution TEM studies [WoMI84] done by members of the same group showed that this thin layer consisted of grains with an average grain size of $\sim 40\text{\AA}$ as compared to $\sim 400\text{\AA}$ in the bulk of the poly-Si film. Such a poly-Si

disordered microstructure layer at the poly-Si/Si interface is believed to act as a very low mobility region where minority carriers are either blocked or recombine.

As-deposited poly-Si is composed of small crystallites of columnar structure joined together by grain boundaries. The grain boundaries are highly disordered regions containing large number of defects and dangling bonds due to incomplete bonding causing trapping states capable of immobilizing both dopant atoms and charge carriers. Carrier trapping at the grain boundaries result in partial grain depletion of doped poly-Si crystallites and the subsequent creation of potential barriers within the grains near the grain boundaries, while the grain boundaries themselves behave as potential barriers where the width of each of these potential barriers is approximately equal to the width of the grain boundary [MaSK81].

However, the grain boundary area and consequently its width is determined by the actual growth of the poly-Si crystallites. Crystal growth starts only after an incubation time that is required to establish a critical nucleus [KiSK83]. The initial nucleation is enhanced by the presence of defects on the substrate [BMZS85] such as vacancies and dangling bonds while Si atoms are heaped and crystallize on the nuclei during deposition. Large crystallites grow at the expense of small ones by crowding them out at the substrate interface as columnar grains develop while their grain size tends to increase as growth proceeds decreasing the grain boundary area between adjacent crystallites [FaBu83]. For complete crystallization of the poly-Si crystallites the crystallization growth rate must be faster than the deposition rate of the film while the deposition time must be long enough to take into account the incubation time of the nuclei. The short deposition time required for the bilayer emitter's thin interfacial n^+ poly-Si layer in this work can result

in incomplete crystallization with small grain size crystallites and wider grain boundaries. Such an effect can lead to an enhancement of the grain boundary potential barrier width which can act as an "artificial" blocking barrier to the transport of the back-injected hole majority carriers. In more detail, since the density of trapping states in the grain boundaries will be larger as a result of wider grain boundaries, thus immobilizing a greater amount of dopant atoms and charge carriers, in conjunction with an almost certain total depletion of the very small adjacent poly-Si crystallites a low-high-low junction can be created at the grain boundaries blocking the back-injected holes from reaching the defect centers in the grain boundaries where they can recombine. At the same time an extensive scattering mechanism of the back-injected holes is believed to be taking place within the very small depleted poly-Si grains that exist close to the junction interface, since the poly-Si grains in that particular region are rather believed to be spherical-like rather than columnar, thus being surrounded by grain boundaries whose blocking barrier capability can constrain and finally retard the diffusion motion of the back-injected carriers within these small depleted grains and within the very first atomic layers of poly-Si from the junction interface.

A sheet resistance of $\sim 10\text{k}\Omega/\square$ was measured for the $\sim 200\text{\AA}$ n^+ poly-Si film incorporated in the bilayer emitter that forms the interface with the p-Si substrate suggesting that the thin n^+ poly-Si interfacial film is composed of very small grains. This is further supported by the exponential sheet resistance increase with decreasing film thickness shown in Figure 2.1.2 of Subsection 2.1 which is believed to be attributable to grain size reduction with decreasing film thickness [LLLS84]. The existence of very small poly-Si grains at the poly-Si/Si interface implies very low carrier mobilities and extensive coulombic scattering,

both of which can lead to carrier diffusion suppression that would explain the low hole back injection current in the poly-Si emitter device configuration of the poly-Si/a-Si bilayer emitter solar cells.

2.4

SHORT WAVELENGTH RESPONSE

Recombination at the grain boundaries of the bilayer poly-Si emitter structure can be a potential source of serious carrier losses with corresponding reductions in the short circuit current. Substantial degradation in the short wavelength response is particularly expected since most of the high energy ultra-violet and blue radiation is absorbed very close to the top surface of the poly-Si bilayer emitter solar cell due to the very high absorption coefficient of poly-Si at short wavelengths.

In this subsection, in an attempt to predetermine the magnitude of short circuit current reductions that might occur with different implemented poly-Si/a-Si bilayer emitter thicknesses, initial theoretical short circuit current loss estimates that were made very early in this work are presented, considering a worst-case situation where complete emitter photocurrent losses take place with the utilization of a poly-Si/a-Si bilayer emitter. The severity of the actual short wavelength related photocurrent losses is also examined here based on absolute spectral response measurements of several poly-Si/a-Si bilayer emitter cells in the blue and ultra-violet range of the spectrum (ie $0.25\mu\text{m}$ - $0.5\mu\text{m}$). The absolute spectral response characteristics of the poly-Si/a-Si bilayer emitter cells in the entire utilizeable solar spectrum, as well as the determination of the actual total photocurrent losses of these devices from these measurements are presented separately in Chapter 4.3.

The minority carriers photogenerated in the bilayer poly-Si emitter will have to diffuse to the junction of the solar cell and fall through the built-in field in order to contribute to the photocurrent. However, the diffusive flow of the photogenerated minority carriers in the polycrystalline structure of the emitter

is expected to be largely retarded by excessive internal coulombic scattering and thus most of these carriers will either be neutralized by defects, or recombine before they reach the junction. To examine how critically the loss of short wavelength response in the bilayer poly-Si emitter may affect the short circuit current of the solar cell, a theoretical model is used to estimate the short circuit current density as a function of the emitter thickness assuming that all carriers generated in the emitter region recombine before reaching the junction while all carriers generated in the single crystal substrate are collected. The absorption coefficient of the poly-Si/a-Si bilayer is assumed to be similar to that of c-Si, based on relevant experimental results reported by Harbeke et al [HKS83] on recrystallized in-situ phosphorus doped a-Si films. The absorption coefficient of such films has been found to be very close to that of c-Si.

Considering a quantum efficiency of unity, the collected photocurrent can be found by:

$$J_{ph}(X_{poly}) = \int_0^{\lambda_{max}} q [1-R(\lambda)] [N(\lambda, X_{poly}) - N(\lambda, W)] d\lambda \quad (2.4.1)$$

where,

$$N(\lambda, X_{poly}) = N(\lambda, 0) \exp[-\alpha(\lambda) X_{poly}] \quad (2.4.2)$$

is the fraction of photon flux remaining at a distance from the surface corresponding to the thickness of the emitter layer, and

$$N(\lambda, W) = N(\lambda, 0) \exp[-\alpha(\lambda) W] \quad (2.4.3)$$

is the amount of photon flux reaching the back surface where W is the width of the solar cell and $N(\lambda, 0)$ is the incident photon flux at the front surface, while $\alpha(\lambda)$ is the absorption coefficient for silicon, and $R(\lambda)$ its reflection coefficient.

Figure 2.4.1: Schematic diagram showing the photocurrent contribution of the photon flux remaining in the substrate as a function of poly-Si emitter thickness.

The fraction of photon flux utilized by the substrate considering complete loss of photogenerated carriers in the emitter is determined from the difference between $N(\lambda, X_{\text{poly}})$ and $N(\lambda, W)$ and it is shown schematically in Figure 2.4.1.

Using the expressions for $N(\lambda, X_{\text{poly}})$ and $N(\lambda, W)$ given by equations (2.4.2) and (2.4.3) we may rewrite equation (2.4.1) as:

$$J_{\text{ph}}(X_{\text{poly}}) = \int_0^{\lambda_{\text{max}}} q [1-R(\lambda)] N(\lambda, 0) \{ \exp[-\alpha(\lambda) X_{\text{poly}}] - \exp[-\alpha(\lambda) W] \} d\lambda \quad (2.4.4)$$

The incident photon flux $N(\lambda, 0)$ is determined from the AM1.5 energy distribution obtained from Green [Gree82] by dividing by the energy of an individual photon (hc/λ) of this wavelength, while data for the absorption coefficient of silicon is obtained from [RaSS79]. Equation (2.4.4) is solved by numerical integration using Simpson's 1/3 rule with an upper wavelength limit of $1.128\mu\text{m}$ and a substrate thickness of $300\mu\text{m}$.

The calculated AM1.5 photocurrent density is shown in Figure 2.4.2 as a function of the bilayer poly-Si emitter thickness for both a perfect ($R=0$) and a single antireflection coating. A photocurrent loss of only 9 percent is estimated for a bilayer emitter thickness of 150nm while for a poly-Si/a-Si emitter thickness of 50nm the available AM1.5 photocurrent is reduced by less than 5 percent. However, under the mentioned assumptions that were made earlier, Figure 2.4.2 gives a worst estimate in this case for the photocurrent loss expected when using a poly-Si emitter since there is evidence that some minority carrier holes can diffuse across a thin poly-Si layer [SoTI79].

Figure 2.4.2: Calculated AM1.5 photocurrent as a function of the bilayer poly-Si emitter thickness for a perfect and a single antireflection coating, assuming complete loss of photogenerated carriers in the emitter and complete collection of photogenerated carriers in the single crystal substrate having a thickness of 300 μ m.

Absolute spectral response measurements carried out on some uncoated n^+ poly-Si emitter solar cells fabricated in this work as outlined in Appendix 1 indicate that indeed the blue response loss is not as severe as initially thought to be. Figure 2.4.3 shows the measured absolute responsivity in the ultra-violet and blue region of the spectrum for solar cells having poly-Si bilayer emitter thicknesses in the 900Å-1500Å range, while the absolute responsivity of an uncoated shallow (~1500Å) phosphorus predeposited crystalline silicon emitter solar cell with an enhanced blue response is also included for comparison purposes. The average blue response of the poly-Si bilayer emitter solar cells shown in Figure 2.4.3 is estimated to be between 40-60% (depending on the particular bilayer emitter thickness utilized in each cell) of the corresponding average response in the same region obtained for the crystalline silicon emitter solar cell indicating that there is a substantial collection of photogenerated minority carriers from the poly-Si emitter layer.

The photocurrent contribution of the blue response can be calculated by numerical analysis using the spectral power density distribution of the AM1.5 terrestrial standard spectrum $P_{AM1.5}(\lambda)$ [Gree82] and the experimental data of the measured absolute spectral response $ASR(\lambda)$ from Figure 2.4.3. An AM1.5 blue photocurrent density of 2.23mA/cm² was estimated for the crystalline silicon emitter while for the bilayer poly-Si emitter solar cells a photocurrent density of ~1.30mA/cm² was calculated for a 900Å poly-Si/a-Si emitter thickness and ~0.94mA/cm² correspondingly for poly-Si/a-Si emitter thicknesses in the 1250Å-1450Å range. Similarly, the AM1.5 photocurrent contribution of the ultra-violet response ($\lambda < 0.4\mu\text{m}$) was found to be 0.233mA/cm² for the crystalline silicon emitter and 0.013-0.028mA/cm² for the bilayer poly-Si emitter cells.

Figure 2.4.3: Measured absolute spectral response in the ultra-violet and blue region of the spectrum for n⁺poly-Si bilayer emitter solar cells with emitter thicknesses in the 900Å-1450Å range. A single crystal silicon emitter cell (c-Si; 1500Å) with enhanced blue response is also shown for comparison purposes.

Figure 2.4.4: AM1.5 input energy showing amount of energy contribution in the ultra-violet region.

Although the ultra-violet response of the bilayer poly-Si emitter cells is poor its effect on the short circuit current is insignificant since the input energy corresponding to the ultra-violet region is very small as seen in Figure 2.4.4 and its utilization will produce a very small amount of photocurrent as indicated from the result of the crystalline silicon emitter solar cell. On the other hand, the photocurrent loss of the bilayer poly-Si emitter cells in the blue region is slightly less than 1.3mA/cm^2 for a $1450\text{\AA}$ emitter thickness and only 0.9mA/cm^2 for the $900\text{\AA}$ bilayer poly-Si emitter as compared to the crystalline silicon emitter cell.

The increase in both the ultra-violet and blue response observed for the thinner bilayer poly-Si emitter cell in Figure 2.4.3 suggests that the photocurrent loss associated with the short wavelength response can become negligible if very thin poly-Si bilayer emitters below $500\text{\AA}$ are implemented. This is further supported from recent minority carrier diffusion length measurements in n^+ poly-Si reported by Chen et al [ChGG88] where a 40-50nm hole diffusion length was estimated for unpassivated n^+ poly-Si contacted emitter diodes. However, the use of very thin bilayer poly-Si emitters will restrict the attainment of high fill factors since a sharp increase of the emitter's sheet resistance occurs below $900\text{\AA}$, as shown in Figure 2.1.2. For an optimum solar cell efficiency a compromise must be made between the loss in blue response and the sheet resistance of the bilayer poly-Si emitter.

The incorporation of a transparent highly conducting oxide like indium-tin-oxide (ITO) on the top surface of the cell could be effectively used in conjunction with a very thin bilayer poly-Si emitter layer in reducing the emitter's high sheet resistance and thus obtaining an optimum blue response without compromising the fill factor of the device. However, this emitter configuration

could not be examined in this work due to lack of proper processing equipment for the deposition of such a highly conducting oxide layer.

Summarizing, it has been shown that the poly-Si/a-Si bilayer emitter solar cell developed in this work is a viable alternative to the poly-Si monolayer emitter developed in earlier work [Tarr85]. Acceptable low sheet resistances with values below $550\Omega/\square$ were obtained in the 1,000Å-1,500Å bilayer thickness range, while maintaining very good junction diode qualities and very low back injection currents. Although the ultra-violet response of the poly-Si/a-Si bilayer emitter cells is low, their blue response loss is not as severe, while it has been demonstrated that the entire short wavelength response can be improved with the implementation of poly-Si/a-Si emitter layers with thicknesses below 1,000Å.

CHAPTER 3

FRONT METAL GRID DESIGN AND METALLIZATION SCHEMES FOR POLY-SI EMITTER SOLAR CELLS

3.1 INTRODUCTION

One of the most important aspects to be considered in the design of a solar cell is the choice of a front metal current collecting grid structure that will minimize the lateral current flow resistance of the shallow emitter layer while covering as little as possible the active area of the device. These conflicting requirements can be satisfied through the use of regularly spaced narrow grid metal line conductors spread across the top surface and connected together by a wider grid line for current extraction. However, several power loss mechanisms are associated with the grid structure itself arising as a result of shadowing effects due to grid reflection, resistive voltage drops along the metal grid lines and the contact resistance between these lines and the semiconductor. Therefore, the design of the front grid pattern must be optimized so as to minimize the combined effect of all the power loss mechanisms related to the top layer of the solar cell.

Several studies have been made towards optimizing the front grid structure [Iles82], [FlMi79], [MaCC78], [Land79], [Baso84], [Scha79], [Saki80], [Serr78] under various constraints, and a variety of grid patterns have been developed depending mainly on the shape of the cell [Gree82], while their degree of complexity has been found to increase with increasing cell size and sunlight concentration levels [FlMi79].

Besides the design of the front grid structure, the metalization process to be selected to deposit the grid on the top surface of the solar cell must satisfy several requirements including the ability to deposit a thick layer of highly conducting metal that will provide a low resistance path to the collected current, while the metalization scheme to be used must provide good adhesion to silicon, must have a relatively low contact resistivity (ie $<0.01\Omega\cdot\text{cm}^2$), and it must be stable during subsequent thermal cycling.

In this Chapter the optimization procedure used to extract the design parameters for the front grid structure is presented, while three metallization processes are investigated involving electroplating, sputtering and e-beam deposition techniques. The metallization schemes examined include Ti/Al, TiW/Au, and TiW/Al configurations while TiW-based metal diffusion barriers on shallow n^+ poly-Si bilayer emitter diodes are also investigated.

3.2 FRONT CONTACT GRID DESIGN OPTIMIZATION

A 2x2cm square cell was used throughout this work since it is the most common geometry for experimental purposes and thus allows easy comparison with the results of other workers. For rectangular and square cells the most typical grid design consists of "n" parallel equally spaced fine grid fingers which are connected by a wide busbar usually at one edge. In such designs the lateral current flow resistance of the emitter layer decreases rapidly as the number of grid fingers "n" is increased since it is proportional to $1/n^2$ [Hove75], and it can practically become negligible if a large number of grid fingers is used. However, such a design will lead to substantial optical losses since most of the cell's active area will be covered. Therefore, a trade-off between resistive and optical losses is necessary and for an optimum grid design all separate power losses associated with the grid must be taken into account.

Once the general grid structure scheme suited to the particular cell shape has been selected, the next design criteria to be considered is the shape of both the grid fingers and the busbar. Grid fingers and busbars are usually either of constant width, linearly tapered or have step changes in width. Linearly tapered shapes have been proven the most efficient ones [Scha79] since they can minimize effectively grid ohmic losses by maintaining a constant current flux density in the grid lines. This is particularly important for the busbar since the current flowing through it will increase substantially towards the interconnect point depending on the number of grid fingers connected to it. On the other hand, for solar cells operating under one sun solar illumination there is no real benefit in making the width of the grid fingers any larger than its feasible minimum value as dictated by the technical limitations of the patterning process itself,

since their resistive losses can be reduced by decreasing the grid finger spacing, which also has the benefit of reducing the lateral emitter series resistance losses.

Figure 3.2.1 shows a schematic diagram with exaggerated grid dimensions of the starting grid design used for the optimization procedure, incorporating narrow parallel grid fingers of constant width connected by a linear tapered busbar at one edge while considering a single interconnection point at the center of the busbar. The symmetrical contacting scheme of the grid structure is broken into two identical "unit cells" and all the front contact power losses are expressed in terms of the "unit cell" dimensions shown in Figure 3.2.1, where "S" is the spacing between the centers of two adjacent grid fingers, " W_f " is the grid finger width, " W_B " is the average width of the linearly tapered busbar, and "AB" is the area of the "unit cell".

To estimate the losses in terms of cell efficiency, the power losses in the top layer of the cell are normalized to the maximum power output of the "unit cell" $ABJ_{mp}V_{mp}$, where " J_{mp} " and " V_{mp} " are the current density and voltage respectively at the maximum power point. Thus, the fractional power losses considered in the optimization of the grid structure in this work are calculated in their normalized form using the following equations given by Green [Gree82].

The shadowing power losses P_{sf} and P_{sb} due to grid finger and busbar shading respectively, are given by:

$$P_{sf} = W_f/S \quad (3.2.1)$$

$$P_{sb} = W_B/B \quad (3.2.2)$$

The resistive power losses P_{rf} and P_{rb} due to grid finger and busbar grid line

Figure 3.2.1: Schematic of the typical starting top grid contact structure used for the grid design optimization, showing the uniform parallel grid fingers and linear tapered busbar as well as the important dimensions for one of the two symmetrical "unit cells".

resistance respectively, are given by:

$$P_{rf} = (1/m) B^2 r_{sm} (J_{mp}/V_{mp}) (S/W_f) \quad (3.2.3)$$

$$P_{rb} = (1/m) A^2 B r_{sm} (J_{mp}/V_{mp}) (1/W_B) \quad (3.2.4)$$

where, $m=3$ for the constant width grid fingers;

$m=4$ for the linearly tapered busbar

and,

$$r_{sm} = \rho_{sm}/t \quad (3.2.5)$$

is the sheet resistance of the conducting metal layer which depends on the resistivity " ρ_{sm} " of the chosen metal element, and the thickness " t " of the deposited metal layer.

The resistive power loss P_{cf} due to grid finger contact resistance, is given by:

$$P_{cf} = \rho_c (J_{mp}/V_{mp}) (S/W_f) \quad (3.2.6)$$

where " ρ_c " is the specific contact resistance between the metal contact of the grid fingers and the semiconductor.

The resistive power loss P_{tl} due to lateral current flow in the emitter layer of the cell, is given by:

$$P_{tl} = (r/12) (J_{mp}/V_{mp}) S^2 \quad (3.2.7)$$

where " r " is the emitter's sheet resistance.

The total normalized front surface power loss P_{tot} is given by,

$$P_{tot} = P_b + P_f \quad (3.2.8)$$

where,

$$P_b = P_{sb} + P_{rb} \quad (3.2.9)$$

gives the total power loss associated with the busbar, and

$$P_f = P_{sf} + P_{rf} + P_{cf} + P_{tl} \quad (3.2.10)$$

gives the total power loss associated with the grid fingers. Thus, both the total busbar and the total grid finger power losses must be minimized respectively in order to achieve minimum total front surface power losses.

To minimize the total busbar power losses an optimum average busbar width is required in order to achieve an optimum trade-off between the shadowing and resistive power loss associated with the linear tapered busbar. Such an optimum average busbar width " W_B " is obtained when the resistive and shadowing busbar losses are equal. Using equations (3.2.2) and (3.2.4) this will occur when,

$$W_B = AB[(r_{sm}/m)(J_{mp}/V_{mp})]^{1/2} \quad (3.2.11)$$

On the other hand, to optimize the trade-off between the partial power losses associated with the grid fingers an optimum grid finger spacing is required such as to minimize the combined effect of these losses in order to result in a minimum total grid finger power loss. In this case, the optimum grid finger spacing " S " is given by the following iterative equation [Gree82],

$$S'' = S' \{ (3P_{sf} - P_{rf} - P_{cf}) / [2(P_{sf} + P_{tl})] \} \quad (3.2.12)$$

A simple computer program was written to extract the optimal values of the grid finger spacing " S " and the average busbar width " W_B " respectively using equations (3.2.1) through (3.2.12). The grid metal thickness " t " and the emitter

sheet resistance " r " are both treated as variable quantities in the optimization procedure and the importance of these two parameters towards minimizing the total power losses is emphasized. The consideration of a variable emitter sheet resistance in the grid design is especially important since in the poly-Si bilayer emitter structure the emitter sheet resistance can change drastically, as was shown in Figure 2.1.2, depending on the thickness utilized in the emitter layer, and thus its value can critically affect the lateral current flow resistive losses as well as the extraction of the proper optimized grid design parameters that will result in minimum total power losses.

The calculation assumes a specific contact resistance " ρ_c " value of $100\mu\Omega\cdot\text{cm}^2$ between the metal contact and the poly-Si emitter layer, while the bulk resistivity " r_{sm} " of the metal grid is taken as $2.214\mu\Omega\cdot\text{cm}$, a value that represents the resistivity of a gold metal conducting scheme for the electroplating technique used in this work. Although a minimum linewidth of 1λ ($6.35\mu\text{m}$) can be achieved with the available photolithographic process, a nominal grid finger linewidth of 3λ ($19.5\mu\text{m}$) was chosen instead and used in the optimization procedure to ensure a reliable metal continuity by the time the entire metallization process is completed. Finally the program calculates all the individual partial power loss components using the extracted optimized grid finger spacing and busbar width for a wide range of metal thicknesses ($1\mu\text{m}$ - $10\mu\text{m}$) and emitter sheet resistances ($100\Omega/\square$ - $5\text{K}\Omega/\square$), and then the minimum total power loss is determined for each separate case. From these results the optimum grid design parameters to be considered for the front grid pattern in conjunction with a suitable poly-Si bilayer emitter sheet resistance are selected such as to comply with the technological limitations of the available processing techniques.

The effect of increasing metal thickness on the total front surface power loss is shown in Figure 3.2.2 assuming a poly-Si bilayer emitter sheet resistance of $400\Omega/\square$ and considering grid metal layers in the $1\mu\text{m}$ - $10\mu\text{m}$ thickness range. The minimum of each curve, as seen in Figure 3.2.3 for the $5\mu\text{m}$ metal thickness case, gives the best compromise between all the partial power resistive and shadowing losses that result in a minimum total power loss at a corresponding optimum grid finger spacing. As the grid metal thickness increases it is apparent from equations (3.2.3), (3.2.4) and (3.2.5) that the resistive losses associated with the grid will be reduced, while as seen in Figure 3.2.2 the optimized value of the grid finger spacing can shift to higher allowable values with increasing metal thickness resulting in lower grid shadowing losses as well. From Figure 3.2.2 it is clear that the total front surface power loss can be reduced substantially with increasing metal thickness, where an 11% loss of the cell's intrinsic output for a contact grid design utilizing a metal layer of $1\mu\text{m}$ can be reduced to less than 6% when a $5\mu\text{m}$ thick metal layer is utilized instead, representing a ~50% reduction in total front surface power losses. On the other hand, the reduction of the total front surface power loss becomes less pronounced for every single micrometer increase in metal thickness and as seen in Figure 3.2.2 an increase from a $5\mu\text{m}$ to $10\mu\text{m}$ metal layer thickness will only result in a ~1% further loss reduction of the cell's intrinsic output from a ~6% loss to a ~5% loss in this particular case. In addition, for metal thicknesses in excess of $5\mu\text{m}$ the processing complexity increases considerably (especially when metal thicknesses tend to approach the $10\mu\text{m}$ range), and although this can be overlooked towards attaining ultimate experimental solar cell efficiencies it is usually not practical for commercial applications in terms of cost effectiveness.

Figure 3.2.2: Effect of increasing metal thickness on total front surface power loss and optimum grid finger spacing assuming a bilayer poly-Si emitter sheet resistance r of $400\Omega/\square$.

Figure 3.2.3: Fractional power losses for grid finger spacing values in the $300\mu\text{m}$ - $1300\mu\text{m}$ range showing the best compromise for a minimum total front surface power loss considering a poly-Si bilayer emitter sheet resistance r of $400\Omega/\square$ and assuming a grid metal thickness of $5\mu\text{m}$.

Figure 3.2.4 shows the combined effect on the total front surface power loss of decreasing emitter sheet resistances in conjunction with increasing grid metal thicknesses for emitter layers having sheet resistance values in the $100\Omega/\square$ - $5K\Omega/\square$ range. Every single point on each curve represents the minimum total power loss that can be attained with an optimum grid finger spacing at a corresponding grid metal thickness as was shown in Figure 3.2.3. For all emitter sheet resistance values considered here the minimum attainable total front surface power loss is greater than 10% when a metal layer of $1\mu\text{m}$ thickness is assumed, with a difference in total power loss of less than 1% for emitter sheet resistance values in the $100\Omega/\square$ - $1K\Omega/\square$ range, while for an emitter sheet resistance of $5K\Omega/\square$ the difference in total power loss, as compared to the other cases, shows an increase of more than 2% giving a minimum total front surface power loss of 13.5%.

Although the difference in total power loss for the sheet resistance values considered here doesn't seem significant when considering a $1\mu\text{m}$ thick metal layer, the effect of the emitter sheet resistance becomes more critical as the grid metal thickness increases, where steeper reductions of the minimum total front surface power loss are shown in Figure 3.2.4 with decreasing emitter sheet resistance values. This is a consequence of the much larger allowable optimum grid finger spacing values for lower emitter sheet resistances with increasing metal thickness, as seen in Figure 3.2.5, which results in lower shadowing losses. From the same figure it is seen that as the emitter sheet resistance increases from $100\Omega/\square$ to $5k\Omega/\square$, the increase of the optimum grid finger spacing with increasing metal thickness becomes less pronounced, being almost marginal in the $5K\Omega/\square$ case. This effect is due to the substantially increasing lateral current flow resistance power loss with increasing emitter sheet resistance and grid

Figure 3.2.4: Combined effect of emitter sheet resistance and grid metal thickness on total front surface power losses considering optimum grid finger spacing values. The effect of the emitter sheet resistance on the total front surface power losses becomes more pronounced with increasing metal thickness.

Figure 3.2.5: Effect of emitter sheet resistance on optimum grid finger spacing with increasing grid metal thickness. The increase of the optimum grid finger spacing with increasing metal thickness becomes less pronounced as the emitter sheet resistance r increases from $100\Omega/\square$ to $5K\Omega/\square$.

Figure 3.2.6: Effect of increasing emitter sheet resistance on the lateral current flow resistance power losses considering optimum grid finger spacings at corresponding grid metal thickness.

finger spacing, as shown in Figure 3.2.6, restricting the trade-off between the partial shadowing and resistive losses to correspondingly higher values due to a lower optimum grid finger spacing increase with increasing grid metal thickness. As a consequence, the difference in the total front surface power losses with decreasing emitter sheet resistance, shown in Figure 3.2.4, becomes more pronounced with increasing grid metal thickness and the emitter sheet resistance value becomes a determining factor for the attainment of an optimum total front surface power loss when utilizing thicker metal layers. As seen in Figure 3.2.4, for a grid metal thickness of $5\mu\text{m}$ the minimum total front surface power loss can be reduced to a range of 5-6% when considering an emitter layer having a sheet resistance value in the $100\Omega/\square$ - $500\Omega/\square$ range, while for an emitter layer with a $5\text{K}\Omega/\square$ sheet resistance the optimum total power loss will be close to ~10% for the same grid metal thickness. Thus, even though an optimum grid structure is used, the total front surface power loss will be quite substantial when utilizing emitter layers with very high sheet resistances, and since the sheet resistance of the bilayer poly-Si emitter has been found to increase drastically below a certain thickness range, as indicated in Chapter 2.1, the emitter layer thickness of most of the solar cells fabricated in this work was selected such as to give sheet resistances lower than $550\Omega/\square$.

Considering all the parameters analyzed above that affect the grid design optimization, an emitter layer sheet resistance in the proximity of $400\Omega/\square$ was selected to provide the basis for choosing the best grid structure to be utilized as the front grid metal contact on the solar cells of this work. Figure 3.2.7 shows the optimum grid dimensional parameters that give minimum total front surface power losses for corresponding grid metal layer thicknesses in the $1\mu\text{m}$ - $10\mu\text{m}$ range assuming an emitter layer having a $400\Omega/\square$ sheet resistance.

Figure 3.2.7: Optimum grid design parameters that result in a minimum total front surface power loss Plot for grid metal thicknesses in the $1\mu\text{m}$ - $10\mu\text{m}$ range considering a bilayer poly-Si emitter sheet resistance of $400\Omega/\square$. A metal thickness of $5\mu\text{m}$ is used to extract the optimum grid design parameters S , No. of GF, W_{bb} that correspond to the minimum total front surface power loss Plot at this metal thickness.

Considering a $5\mu\text{m}$ thick metal conducting layer that can be deposited with the current available processing techniques, the optimum grid dimensional parameters at this metal thickness, as extracted from Figure 3.2.7, give a grid finger spacing "S" of $711\mu\text{m}$, translating into ~ 28 grid fingers for the $2\times 2\text{cm}$ solar cell's active area utilized in this work, and for the linear tapered busbar a maximum fullwidth " W_{bb} " of $286\mu\text{m}$ (or $146\mu\text{m}$ for the average width W_B), while as mentioned in the beginning of this Subsection the grid fingers were considered uniform having a constant linewidth " W_f " of $19.5\mu\text{m}$.

The minimum total front surface power loss and its corresponding optimum fractional power losses for an emitter sheet resistance of $400\Omega/\square$ and grid metal layer thicknesses in the $1\mu\text{m}$ - $10\mu\text{m}$ range are shown in Figure 3.2.8. As seen in this figure, for a front metal contact grid structure implementing the extracted grid design parameters shown in Figure 3.2.7 at a metal layer thickness of $5\mu\text{m}$, the total front surface power loss " P_{tot} " at this metal thickness will be 5.924% with partial power losses accounting for 2.646% due to grid finger shading, 0.715% due to busbar shading, 1.031% due to grid finger resistive losses, 0.715% due to busbar resistive losses, 0.80% due to emitter lateral current flow resistive losses and 0.017% due to contact resistance losses when considering a moderate specific contact resistance of $100\mu\Omega\text{-cm}^2$. Thus, the total grid finger and busbar shadowing losses for such a grid structure will be 3.361%, while the total resistive losses will be 2.563%. However, because the pattern generator used to produce the optical mask of the front metal grid design requires integer " λ " units ($1\lambda = 6.35\mu\text{m}$) the busbar was linearly tapered from a width of 2λ ($12.7\mu\text{m}$) to a full width of 56λ ($355.6\mu\text{m}$) instead of the optimum value of $286\mu\text{m}$. Thus, the busbar shadowing losses increased slightly from 0.715% to 0.887%, which was though counter-

Figure 3.2.8: Minimum total front surface power loss and optimum partial power losses for grid metal thicknesses in the $1\mu\text{m}$ - $10\mu\text{m}$ range considering a bilayer poly-Si emitter sheet resistance of $400\Omega/\square$. For a metal thickness of $5\mu\text{m}$: $P_{tot}=5.924\%$, $P_{sf}=2.646\%$, $P_{bf}=0.715\%$, $P_{cf}=1.031\%$, $P_{bf}=0.80\%$, $P_{cf}=0.017\%$.

balanced by a corresponding slight reduction in the busbar resistive losses from 0.715% to 0.577%.

Figure 3.2.9 shows a 5X magnification of the actual top metal grid design layout implemented in this work with the above mentioned grid dimension parameters. The coverage of this grid structure accounts for ~3.5% power loss of the intrinsic cell's power output, while the total resistive power losses may vary from ~2.6% when utilizing a $5\mu\text{m}$ thick gold metal conducting scheme, to ~2.8% when utilizing a $5\mu\text{m}$ aluminum metal conducting scheme. However, the resistive losses may vary accordingly depending on the actual metal thickness deposited, the resistivity of the particular metal conducting element used and the emitter sheet resistance of the specific bilayer poly-Si emitter utilized, while a variation in the contact resistance usually has negligible effects as long as it is kept below $0.01\Omega\text{-cm}^2$. It has to be noted here that this grid design is comparable to state-of-the-art single metal level grid designs [GBSK84] used for crystalline silicon diffused emitter solar cells, while the total shading losses of the grid structure shown in Figure 3.2.9 are the lowest ever reported for a top contact grid.

As seen in Figure 3.2.9, the busbar is connected to a wide contact pad outside the active area of the solar cell which is used for probing purposes, while it can also serve as a bonding area for interconnections, or to attach external leads, without damaging the actual solar cell. Two smaller $0.5\times 0.5\text{cm}$ solar cells are also included, fitted symmetrically underneath the busbar of the main cell such as to provide working devices even if part of the wafer is damaged during fabrication. Finally, various test devices, from different sized diodes to Van der Pauw crosses for emitter sheet resistance measurements and Kelvin resistors for contact resistance measurements, were positioned around the main cell to provide access

Figure 3.2.9: Optimized front contact grid pattern and surrounding test devices in a 5X magnification of the original sized layout.

for individual characterization of the solar cell's properties in the same wafer with the actual device.

Due to unforeseen difficulties encountered during the mask aligning procedure, unavoidable multiple mask alignment trials had to be made in order to attain a desirable minimum mask alignment error. Thus, because of the actual physical contact that takes place between the patterned mask itself and the photoresist coating of the wafer's surface to be patterned during each alignment trial, undesirable photoresist removal from several isolated areas took place, leaving behind unprotected tiny spots in the solar cell area where the grid structure was later patterned, creating several isolated discontinuities in the resulted metal grid structure.

In order to minimize the negative effects of the isolated metal grid discontinuities (ie higher lateral current flow resistance for current collected from adjacent grid lines, and artificially higher voltage drops that would develop along these individual grid lines due to current overcrowding), a new metal grid pattern was designed and implemented at a later stage. Extra grid lines were added to the previous design in such a manner as to form a crossed "mesh" pattern with the already existing grid lines so that to provide a more flexible path for the collected current. The implemented improved "mesh" grid design is shown in Figure 3.2.10 having only marginal deviations from the previously determined resistive and optical losses of the original design. This grid pattern is believed to alleviate both the otherwise higher current flow resistances and the higher current densities that individual grid lines would have to carry in case of adjacent discontinuous grid lines, thus avoiding a possible increase in the series resistance and a consequent decrease in the fill factor of the solar cell due to these effects.

Figure 3.2.10: Improved front contact grid design showing the "mesh" pattern structure implemented. The shown size is a 5X magnification of the original sized layout.

3.3 FRONT CONTACT METALLIZATION SCHEMES / METAL DEPOSITION PROCESSES AND METAL DIFFUSION BARRIERS

A good front contact metallization scheme must satisfy several requirements. Because solar cells are required to have a long operating lifetime in order to be economically feasible for practical applications, the metal contact system must have good contact adhesion to the semiconductor, be corrosion resistant, and be thermally stable under subsequent temperature exposures. Finally, as mentioned in Subsection 3.2, it is important that the front contact be thick enough to provide a low resistance conduction path and thus minimize related parasitic resistance losses which can otherwise result in low fill factors and cell efficiencies.

For high efficiency cells the front metal grid is usually deposited in a high vacuum system by thermal evaporation, e-beam evaporation, or sputtering, while for low cost cells plating techniques or screen printing of metal inks (or pastes) are used instead. In this work, e-beam evaporation, sputtering and electroplating are the three metal deposition processes considered, while Ti/Al, TiW/Au and TiW/Al are the metallization schemes examined. The main purpose of the metallization experiments carried out was to establish a reliable metallization process capable of depositing metal thicknesses in the $5\mu\text{m}$ range in order to comply with the low front surface power loss grid design requirements discussed in Subsection 3.2, while on the other hand providing metal contact with good adhesion to the n^+ polysilicon bilayer emitter and good thermal stability.

The choice of the metallization scheme to be used as the grid contact on the top surface of the bilayer poly-Si emitter solar cells is very critical since the presence of grain boundaries and other extended defects in polysilicon through which metal atoms can rapidly diffuse across the very shallow poly-Si emitter

layers (1,000Å-1,500Å) utilized in this work even at room temperature. Aluminum is the most commonly used metal contact in various silicon semiconductor devices because it can provide relatively good ohmic contacts to both highly doped n-type and p-type silicon. However, aluminum will diffuse in polysilicon even at temperatures as low as 150°C [Nico78] causing substantial junction leakage and even most probably shorting of the device. Since post-metallization heat treatments are usually required to sinter the metal contact or anneal the radiation damage introduced on the top surface during the metal deposition when e-beam evaporation or sputtering is used, it is necessary to utilize a multilayer metallization scheme where the first metal layer must be thermally stable and act as a diffusion barrier between the highly conducting element used as the shallow polycrystalline silicon emitter.

i) TITANIUM/ALUMINUM METALLIZATION (Ti/Al)

In conventional solar cell technology a common multilayer front surface metallization scheme (for high efficiency solar cells) utilizes a thin layer of titanium (~1,000Å) as the first layer, mainly to obtain a low contact resistance and good adhesion to silicon, being followed by a thick layer of Ag or Al conductor, while a thin layer of palladium is often added between the titanium and the highly conducting metal to increase the moisture corrosion resistance of the contact. Titanium is an oxygen gettering material and besides its ability to break down the thin native oxide on the silicon surface by making strong Ti-O bonds that provide good adhesion to silicon, it is also thermally stable in contact with polysilicon at commonly used sintering temperatures of about 450°C [Nico78], [Keye87], thus making it attractive as a contact material for polysilicon emitter devices.

A Titanium/Aluminum metallization scheme was the first one implemented on the top surface of some poly-Si/a-Si emitter solar cells. Although both titanium and aluminum can be evaporated by resistive heating thus avoiding any possible radiation damage, the aluminum deposition thickness capability of the thermal evaporation system is constrained to $\sim 1\mu\text{m}$ and thus multiple aluminum thermal evaporations would be required by breaking vacuum in between for aluminum loadings in order to achieve a desirable aluminum thickness in the proximity of $5\mu\text{m}$. As an unavoidable consequence of the multiple aluminum loadings, the surfaces of the subsequent deposited aluminum layers can be oxidized in the short atmospheric exposures forming Al_2O_3 which can cause undesirable high parasitic metal resistance losses that can degrade the fill factor of the solar cell. On the other hand, even though the e-beam evaporation process can cause radiation damage to the front surface of the device, it has the flexibility of depositing metal layers in the desired $5\mu\text{m}$ range, while the radiation damage can be effectively annealed by a proper post heat treatment.

Titanium and aluminum were deposited sequentially on the top surface of the wafers by e-beam evaporation without breaking vacuum in between. The chamber was pumped down to a base pressure of $\sim 10^{-6}$ Torr before evaporation, while both titanium and aluminum films were deposited at a deposition rate of $15\text{\AA}/\text{sec}$ to thicknesses of $\sim 1,500\text{\AA}$ and $\sim 5\mu\text{m}$ respectively. Because titanium will act only as a sacrificial barrier in this case since it reacts with aluminum forming a TiAl_3 compound, considering that the thickness of the TiAl_3 compound will be equal to $(Dt)^{1/2}$ where "t" is the reaction time and "D" a diffusivity coefficient which as given by Nicolet [Nico78] is equal to $1.5 \times 10^{15} \exp(-1.8\text{eV}/kT) \text{ \AA}^2\text{sec}^{-1}$, the $1,500\text{\AA}$ target thickness selected for the titanium deposition was estimated to be

sufficient to leave some unreacted titanium ($\sim 700\text{\AA}$) after a 20min post-deposition heat treatment at 450°C .

The titanium/aluminum bimetal was patterned using an optical mask that defined the grid structure shown in Figure 3.2.9 using a positive photoresist. Some initial problems were encountered during the etching procedure of the thick aluminum layer on experimental wafers due to the long etching time ($\sim 6\text{min}$) required to etch the $\sim 5\mu\text{m}$ of aluminum in phosphoric acid. Severe undercutting was observed due to lateral etching, while the photoresist lifted off in several places along the narrow defined grid fingers creating discontinuities in the aluminum grid lines. However, this problem was resolved by performing the aluminum etching in two steps, where after a four minute initial etching the wafer was pulled out of the etching solution, rinsed in deionized water to stop the undergoing reaction and baked for 10 minutes at 130°C to reharden the predefined photoresist pattern. This method proved to be effective resulting in minimum undercutting ($\sim 15\%$ total on both sides), while the photoresist remained intact throughout the defined pattern by the end of the aluminum etching procedure. The remaining metal layer of titanium etched quickly ($\sim 30\text{sec}$) in a mixed solution of ammonium-hydroxide/hydrogen-peroxide/water (5:1:1) heated at 75°C , leaving a well defined metal pattern without any further observable undercutting and a clean poly-Si surface since the solution used is known to be a cleaning agent that can remove possible organic contaminants.

Although as-deposited titanium is known to make a very good ohmic contact to $n^+\text{poly-Si}$ [TiCr82], [Keye87] giving a low contact resistance and thus not requiring the otherwise necessary sintering step, a post heat treatment in this case was initially considered to be beneficial towards annealing the radiation damage introduced on the top surface of the device during the e-beam

evaporation of the Ti/Al metal layers. However, as illustrated in Figure 3.3.1 the junction integrity of a $400 \times 400 \mu\text{m}$ test diode starts degrading at annealing temperatures as low as 350°C showing an increasing leakage current at low forward bias voltages, while as shown in Figure 3.3.2 the diode characteristics degraded severely when a 400°C annealing was performed for 20 minutes giving a leakage current of $\sim 7\text{mA}/\text{cm}^2$ at 1V reverse bias. The fill factor of the solar cell annealed at 350°C showed a small decrease from a value of 0.79 before annealing to 0.77 after annealing, but the effect on the junction integrity degradation was more pronounced for the solar cell annealed at 400°C where the fill factor decreased from 0.79 before annealing to 0.49 after annealing.

Despite other reports [TiCr82], [Nico78], the results of this work indicate that titanium is not an effective barrier to material transport of Al even at low annealing temperatures. It is believed that besides the interaction between Al and Ti, Al diffused through the grain boundaries of the polycrystalline film structure of the Ti layer, and since Al cannot react with polysilicon it readily diffused through it once it reached the polysilicon layer's top surface. This can occur if the deposited titanium layer's structure consists of smaller polycrystalline grains than the corresponding overlaying aluminum layer's polycrystalline structure, since the grain size of a polycrystalline metal film is known to be a governing factor [Nico78], [CaCR77] in determining the atomic transport properties of a metal element, with a predominant migration of the material having larger grains into the material consisting of smaller grains. Since smaller grain materials have a much larger number of grain boundaries that can offer an easy path for material transport, considering the general trend of higher melting point elements to result in structurally smaller grain size films [CaCR77] with titanium having a

Figure 3.3.1: Dark J-V characteristics of a 400x400μm n⁺poly-Si bilayer emitter diode contacted by Ti/Al : A) before annealing and B) after H₂ annealing at 350°C for 15min.

Figure 3.3.2: Dark J-V characteristics of a 400x400 μm n⁺poly-Si bilayer emitter diode contacted by Ti/Al : A) before annealing and B) after H₂ annealing at 400°C for 20min.

melting point of 1668°C and aluminum a much smaller melting point of 660°C, a predominant migration of Al into Ti should normally be expected. However, it is suspected that the fabrication process itself could have been the critical factor towards the failure of the titanium sacrificial barrier in this case since its grain size depends on the deposition parameters selected (ie deposition rate). Thus, more experimentation is required to establish an effective titanium barrier, while TEM analysis and Rutherford Backscattering Spectrometry (RBS) which were not available in this work are necessary in determining the actual grain size of the metal films and their interaction respectively before and after annealing.

Although titanium failed as a diffusion barrier during annealing, the titanium/aluminum metallization scheme can provide a good ohmic contact to n⁺poly-Si even without post heat treatment. In this case a contact resistance of $55\mu\Omega.\text{cm}^2$ was measured before annealing. On the other hand, the inability to effectively anneal the radiation damages due to the e-beam evaporation process without degrading the junction integrity of the solar cell will degrade the performance of the device and consequently limit the possibility of attaining high efficiencies.

ii) TITANIUM-TUNGSTEN/GOLD METALLIZATION ($\text{Ti}_{0.1}\text{W}_{0.9}/\text{Au}$)

Titanium-tungsten ($\text{Ti}_x\text{W}_{1-x}$) has been widely used in the industry as part of bimetal and trimetal metallization schemes in IC interconnection systems [GBFM78] because of its well known corrosion resistance characteristics [CuFH70], its good adhesion to silica and highly conducting metals like gold and aluminum, and most importantly because of its adequate diffusion barrier properties [Nico78], [CuFH70], [GBFM78], [TiWI82] against gold and aluminum.

Titanium-tungsten ($\text{Ti}_x\text{W}_{1-x}$) is a pseudo-alloy whose useful composition varies over a range of 10 to 30 percent titanium in tungsten [GBFM78] with tungsten being practically insoluble in titanium below 700°C and titanium having a finite solubility in tungsten to about 10 percent at 600°C , where any excess titanium is not alloyed to tungsten but can nevertheless impart desirable characteristics to the film in terms of increasing corrosion resistance [CuFH70]. The superior corrosion resistance of $\text{Ti}_x\text{W}_{1-x}$ among other refractory metals is attributed to the formation of very stable and insoluble TiO_2 on exposed surface regions [CuFH70], while its good adhesion to silica is due to the strong readily formed Ti-O bonds with it, and its good electrical contact characteristics to gold and aluminum [GBFM78] is attributed to the formation of Ti-Au and Ti-Al interfacial compounds respectively.

Although $\text{Ti}_x\text{W}_{1-x}$ is unstable against silicon at temperatures in excess of 700°C forming a ternary $\text{Ti}_x\text{W}_{(1-x)}\text{Si}_2$ compound [HLNN76], it is thermodynamically stable at the much lower commonly used range of $400\text{-}450^\circ\text{C}$ annealing temperatures where it can act as an acceptable diffusion barrier between silicon and aluminum [GBFM78], and silicon and gold [Nico78], as long as the diffusivity of these metal elements in $\text{Ti}_x\text{W}_{1-x}$ is low ; a property which depends on the sputtering* deposition process of the $\text{Ti}_x\text{W}_{1-x}$ pseudo-alloy (ie ambient, base pressure) [NHNM78], [BBNE78].

Taking into account all the above mentioned characteristics of the $\text{Ti}_x\text{W}_{1-x}$ refractory compound, titanium-tungsten has been considered as an alternative refractory metal contact to titanium for the front contact grid of the poly-Si/a-Si

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* Sputtering of $\text{Ti}_x\text{W}_{1-x}$ films is used to avoid fractionation of the excess titanium during the deposition process.

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emitter solar cells. The implementation of a $\text{Ti}_x\text{W}_{1-x}/\text{Au}$ front metallization scheme is especially attractive for solar cell applications because it can combine the beneficial corrosion resistance, tight adherence, and diffusion barrier properties of $\text{Ti}_x\text{W}_{1-x}$ with the convenience of electroplating the gold conductor to any desired thickness at selected areas, thus making this metallization scheme economically viable for commercial applications. Having in mind all the above considerations, a $\text{Ti}_x\text{W}_{1-x}/\text{Au}$ bimetal metallization scheme was selected to be utilized as the front contact conducting grid in several bilayer poly-Si emitter solar cells using a deposition process that involves a combination of sputtering and electroplating techniques. It has to be noted here that for the first time such a metallization scheme finds application on solar cells, while for the first time the reliability of such a metal contact system stability is examined on sensitive shallow polysilicon emitter devices.

A multitarget sputtering system (MRC SEM-8620) having both sputter etch and r.f bias capabilities was used to deposit the titanium-tungsten as well as a thin gold film that is needed to be used as a "seed" layer in the gold electroplating procedure. The titanium-tungsten target used in this work had a 10:90wt% Ti:W composition while both the $\text{Ti}_{0.1}\text{W}_{0.9}$ and Au targets were of 99.99% purity. The targets were located 2.5 inches from the substrate. The deposition chamber was evacuated to a base pressure of $\sim 3 \times 10^{-7}$ Torr prior to the introduction of high purity (99.999%) argon to a partial pressure of about 8×10^{-3} Torr. Both the $\text{Ti}_{0.1}\text{W}_{0.9}$ and Au targets were sputter cleaned for 3 minutes at 1.4kV r.f peak voltage prior to each corresponding deposition, while a 100W r.f power was used throughout the sputtering process. The front surface of the wafers was sputter etched for 1 minute at 950V r.f peak voltage in order to remove the native oxide, and then the $\text{Ti}_{0.1}\text{W}_{0.9}$ and Au films were sputter-deposited sequentially on the

wafers without breaking vacuum. Both the $\text{Ti}_{0.1}\text{W}_{0.9}$ and Au were sputtered at 1.4kV r.f peak voltage for 6 minutes and 3 minutes respectively, depositing a $\sim 600\text{\AA}$ thick $\text{Ti}_{0.1}\text{W}_{0.9}$ film and a $\sim 300\text{\AA}$ Au film as measured by a Sloan Dektak profilometer on sample wafers.

For the electroplating process, a thick plating guide was used in order to avoid an undesirable "mushroom-shaped" gold build-up, due to lateral deposition during the Au electroplating, that could possibly lead to gold migration at the edges of the grid pattern and down the poly-Si emitter during annealing. The sputtered $\text{Ti}_{0.1}\text{W}_{0.9}$ /Au bilayer was coated with a dense positive photoresist (AZ-1375) that was spun at 2,500rpm for 30sec giving a photoresist thickness in the 3.5-4.0 μm range. Using an optical mask to define the grid pattern, the thick photoresist was purposely overexposed in UV light for $\sim 16\text{sec}$ to make certain it would develop properly leaving behind a clean surface that is necessary to provide good adhesion to the electroplated gold. Finally, the photoresist was developed for $\sim 100\text{sec}$ in a positive developer creating the desired thick plating guide that was needed.

The wafers were immersed in a gold solution that was heated in advance to a 48-50°C temperature range and with the aid of the resist plating guide-mask gold was electroplated at the open areas on the "gold seed" surface by applying a 1.7mA forward current. Gold layers in the 5-6 μm thickness range were built-up at a $\sim 1,300\text{\AA}/\text{min}$ deposition rate while gold films as thick as 8 μm were also obtained on several wafers showing the flexibility of the electroplating process. It has to be noted here though that after excessive use of the Au solution, the deposition rate of the electroplated film was found to have declined by as much as 500 $\text{\AA}/\text{min}$, while degradation of the deposited Au film quality was also observed with signs of a fading gold-brown film colour. However, when this effect was noticed fresh Au

solution was used and the problem was resolved. One of the possible reasons for this deteriorating effect may be attributed to the initial temperature stabilization process required to establish the recommended 48-50°C temperature range. The temperature of the solution on several occasions rose well beyond 50°C which may have reduced its useful active life.

After the electroplating process was completed, the resist plating guide-mask was stripped in J-100 and then the underlying thin "gold seed" layer was etched in a potassium-iodine solution for ~15sec with the aid of an ultrasonic agitator, while the remaining $\text{Ti}_{0.1}\text{W}_{0.9}$ layer was removed in a 30% hydrogen peroxide solution, leaving a well defined grid structure on the front surface.

The devices were given a 20 minute heat treatment at 400°C in a hydrogen ambient in order to anneal the radiation damage introduced on the front surface during the sputtering process. The junction integrity of the solar cells was preserved after the annealing, while as seen from the dark J-V characteristics shown in Figure 3.3.3 for a 400x400 μm diode before and after annealing respectively, a decrease in the dark saturation current is observed at low forward bias voltages after the annealing treatment due to a reduction in the recombination current component as a result of the effective hydrogen passivation of the sputtering radiation damage in the n^+ bilayer poly-Si emitter. However, in a few occasions the electroplated gold film peeled off the underlying "gold seed" surface during the annealing treatment indicating poor adhesion between the two corresponding layers in these cases. A possible explanation for this effect could be an insufficient UV exposure and/or development of the ~4 μm thick photoresist that might have left a very thin undetectable layer of the resist material on the "seed gold" layer surface area on which gold was electroplated.

Figure 3.3.3: Dark J-V characteristics of a 400x400 μ m n⁺poly-Si bilayer emitter diode contacted by Ti_{0.1}W_{0.9}/Au : A) before annealing and B) after H₂ annealing at 400°C for 20min.

Despite this effect no degradation was observed in the junction integrity of these devices after the annealing treatment, thus demonstrating the stability of the $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Au}$ metallization system at 400°C .

An improvement on the fill factor of the solar cells from ~ 0.78 to ~ 0.80 after annealing was observed mainly as a result of a $\sim 25\%$ reduction in the emitter sheet resistance, while very low leakage current densities in the $20\mu\text{A}/\text{cm}^2$ range were measured on the solar cells at 5V reverse bias voltage. The contact resistance of the $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Au}$ metal contact system to the n^+ bilayer poly-Si emitter was in the $100\text{--}150\mu\Omega\cdot\text{cm}^2$ range, as measured by Kelvin resistors on different wafers, without showing significant variation after the annealing treatment, while the resistivity of the $\text{Ti}_{0.1}\text{W}_{0.9}$ layer measured on sample wafers by the four point probe method was found to be in the $70\text{--}100\mu\Omega\cdot\text{cm}$ range, being in good agreement with results reported by Ghate et al [GBFM78]. Although the above reported contact resistance between the $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Au}$ bimetal and the n^+ poly-Si may seem high by integrated circuit standards, such contact resistance values have negligible effects on the solar cell performance.

The results of this work indicate that $\text{Ti}_{0.1}\text{W}_{0.9}$ is an effective diffusion barrier against gold at the 400°C temperature range since the improved diode characteristics and the negligible measured leakage currents after the annealing treatment imply that no metal migration takes place in the n^+ poly-Si bilayer emitter. Contrary to the results of this work, it has been reported by several workers [Nico78], [BBNE80], [NHNM78] that the commonly used $\text{Ti}_{0.3}\text{W}_{0.7}$ film exhibits marginal diffusion barrier properties against Au at 400°C when the $\text{Ti}_{0.3}\text{W}_{0.7}$ film is deposited in a pure state under high vacuum. Extensive indiffusion of Au in $\text{Ti}_{0.3}\text{W}_{0.7}$ has been reported at temperatures as low as 300°C [BBNE80] with severe pitting taking place at 400°C indicating intermixing of Au

and Si, while an improvement in the diffusion barrier properties of $\text{Ti}_{0.3}\text{W}_{0.7}$ occurs only when contaminant impurities like oxygen or nitrogen are introduced in the film during the deposition process [BBNE80], [NHNM78]. Based on the results of this work and the fact that the $\text{Ti}_{0.1}\text{W}_{0.9}$ film was deposited under high vacuum ($\sim 3 \times 10^{-7}$ Torr), it is believed that the diffusion barrier properties of $\text{Ti}_{0.1}\text{W}_{0.9}$ are superior to those of $\text{Ti}_{0.3}\text{W}_{0.7}$.

The ability to anneal the radiation damages in the n^+ bilayer poly-Si emitter without degrading the junction integrity of the solar cells, in conjunction with the grid metal thickness flexibility of the electroplating process that produced gold film layers as thick as $8\mu\text{m}$, proves that the $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Au}$ metallization scheme is a better candidate than the already examined Ti/Al scheme. However, although electroplating is convenient, it is not as reliable as the e-beam evaporation method since the metal deposition rate and the quality of the electroplated metal film can easily be altered by unavoidable small temperature fluctuations and applied current drift during electroplating, while aging of the electroplating solution itself is the most serious concern towards obtaining reproducible results. Furthermore, adhesion problems may occur due to insufficient U.V exposure and/or development of the thick resist plating-guide, a task that is not trivial since the thickness of the applied resist material has been found to vary by $\pm 10\%$ ($\pm 0.4\mu\text{m}$ in this case) depending on the corresponding room temperature, air humidity, and most importantly fluctuations in the angular velocity of the spinner during the photoresist spin coating. However, this problem can be avoided altogether if pulse plating with current reversal is used instead to build up the desired gold film, since this technique prevents lateral deposition of the electro-plated film, thus eliminating the need of a thick resist plating guide [GBSK84]. Lack of time however prevented experimental attempts with such a technique.

iii) TITANIUM-TUNGSTEN/ALUMINUM METALLIZATION ($\text{Ti}_{0.1}\text{W}_{0.9}/\text{Al}$)

A $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Al}$ bimetal system was examined as an alternative metallization scheme to $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Au}$, where a combination of sputtering and e-beam deposition processes are used to deposit the desired $\text{Ti}_{0.1}\text{W}_{0.9}$ and Al films on the front surface of the n^+ poly-Si bilayer solar cells in an attempt to establish a more reliable metal deposition process than the electroplating method used in the latter case. Once again, such a metallization scheme is implemented for the first time on solar cells and particularly on sensitive shallow poly-Si emitter devices like those fabricated in this work.

Using the same sputtering deposition procedure and deposition parameters as described on Subsection 3.3.ii, a $\sim 1000\text{\AA}$ thick layer of $\text{Ti}_{0.1}\text{W}_{0.9}$ film was deposited on the front surface of the solar cells. The aluminum deposition was carried out in a different vacuum system by e-beam evaporation, where a $\sim 5\mu\text{m}$ thick aluminum layer was deposited on top of the $\text{Ti}_{0.1}\text{W}_{0.9}$ film at a deposition rate of $\sim 15\text{\AA}/\text{sec}$ with the vacuum system having a $\sim 10^{-6}$ Torr base pressure. The surface of the $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Al}$ bimetal was then coated with a thin positive photoresist layer, and the desired grid pattern was defined using an optical mask. The excess aluminum was etched in phosphoric acid using the two step etching procedure discussed in Subsection 3.3.i, which is necessary in order to minimize undercutting and avoid a possible photoresist lift-off. The remaining $\text{Ti}_{0.1}\text{W}_{0.9}$ layer etched quickly ($\sim 5\text{sec}$) in an ammonium-hydroxide solution that was preheated to 75°C leaving a clean poly-Si surface and a well defined grid metal pattern with minimum undercutting. Further details on the complete metallization process and etching procedure are given in Appendix 1(8B).

In order to remove the radiation damage introduced on the front surface of the devices during the sputtering/e-beam metal deposition process, a 20 minute hydrogen annealing treatment was carried out at 450°C. No junction degradation effects were observed after the annealing in any of the $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Al}$ contacted shallow poly-Si emitter solar cells and their surrounding test diodes, while very low leakage currents were measured indicating that no metal migration took place in the n^+ poly-Si bilayer emitter during the 450°C heat treatment. Figure 3.3.4 shows the dark J-V characteristics of a $400 \times 400 \mu\text{m}$ diode before and after the annealing treatment, where a reduction in the dark saturation current density is observed at low forward bias voltages after the annealing as a result of the effective hydrogen passivation of the radiation damage and other defect centers in the poly-Si emitter layer. Fill factor improvements from ~ 0.78 to 0.80 and in some cases even to ~ 0.81 were attained after the annealing, mainly as a result of a 30-45% reduction in the n^+ poly-Si bilayer emitter sheet resistance.

The initial contact resistance of the n^+ poly-Si/ $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Al}$ configuration, as measured by Kelvin resistors on different wafers before annealing, was found to lie in the $250\text{-}300 \mu\Omega.\text{cm}^2$ range, while contact resistances in the $150\text{-}200 \mu\Omega.\text{cm}^2$ range were measured after the 450°C heat treatment. The apparent higher contact resistance values measured before annealing are attributed to the presence of a thin metal-oxide layer (most probably TiO_2) at the $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Al}$ interface that was formed on the $\text{Ti}_{0.1}\text{W}_{0.9}$ surface prior to the aluminum deposition in the short atmospheric exposure of the wafers during loading in the e-beam evaporation system. However, the reduction in the contact resistance after the 450°C annealing indicates that the thin metal-oxide broke down during the given heat treatment resulting in an increased adhesion between the $\text{Ti}_{0.1}\text{W}_{0.9}$ and Al films.

Figure 3.3.4: Dark J-V characteristics of a 400x400μm n⁺poly-Si bilayer emitter diode contacted by Ti_{0.1}W_{0.9}/Al : A) before annealing and B) after H₂ annealing at 450°C for 20min.

Although contact resistance values as high as $200\mu\Omega.\text{cm}^2$ were obtained after the annealing treatment, it must be emphasized that such contact resistances have negligible effects on the performance of the solar cells.

As expected, the e-beam evaporation method used to deposit the aluminum conductor proved to be more reliable than the Au electroplating process due to the more accurate control the former method provides over the metal deposition parameters and deposition conditions. On the other hand, although the maximum amount of metal film that can be deposited by e-beam evaporation with a single aluminum loading was constrained to $\sim 6\mu\text{m}$ in this case, experimental results in this work showed that fill factors as high as ~ 0.81 can be obtained with a $\sim 5\mu\text{m}$ thick aluminum front grid metal, demonstrating that such metal film thicknesses are more than adequate in minimizing the corresponding metal parasitic resistance of the front grid, and thus indicating that the e-beam evaporation method can easily comply with the front grid metal thickness requirements.

Concluding, among the metal deposition processes examined in this work, the sputtering/e-beam combination was found to give the most reliable and reproducible metal films, while the diffusion barrier capability of $\text{Ti}_{0.1}\text{W}_{0.9}$ against Al migration at 450°C in conjunction with the known good adhesion and corrosion resistance properties of $\text{Ti}_{0.1}\text{W}_{0.9}$, makes the $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Al}$ bimetal configuration the most suitable front metal contact for the sensitive shallow $n^+\text{poly-Si}$ bilayer emitter solar cells fabricated in this work.

3.4 DEVELOPMENT OF HIGH TEMPERATURE $Ti_{0.1}W_{0.9}$ -BASED DIFFUSION BARRIER CONTACTS FOR SHALLOW n^+ POLY-SI EMITTER DEVICES.

One of the main objectives in the metallization schemes examined so far was to implement a reliable metal diffusion barrier contact on the shallow n^+ poly-Si bilayer emitter devices of this work in order to avoid degradation of the solar cell performance that can be caused by diffusion of the primary metal conductor in the poly-Si emitter during subsequent heat treatments. Although the current experimental solar cells are not exposed to any further heat treatment after the post-metallization low temperature annealing at which $Ti_{0.1}W_{0.9}$ proved to be a reliable diffusion barrier against Au and Al, modern encapsulation methods of solar cells in a commercial production line may require a high temperature heat treatment where the metallization scheme can be exposed to temperatures as high as 600°C for ten minutes. Since the thermal stability and the diffusion barrier reliability of the metal contact layer in the metallization scheme is subject to the specific temperature level of the given heat treatment, further experimentation was carried out in this work to determine whether a $Ti_{0.1}W_{0.9}$ or even a $Ti_{0.1}W_{0.9}N_x$ -based metal contact film can be used as a high temperature diffusion barrier.

To avoid the lengthy processing procedure involved with the fabrication of solar cells, test diode devices were used instead since it was needed to evaluate only the junction integrity of the devices under various post-metallization heat treatments. Shallow n^+ poly-Si bilayer emitter diodes with emitter thicknesses in the 1250Å range were fabricated using the same poly-Si/a-Si fabrication sequence and LPCVD deposition parameters as described in Chapter 2.2, while a mask set containing different size diodes was used for patterning purposes.

A $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Al}$ bimetal configuration was used as the basic front metallization scheme, while variations based on this configuration included a $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Ti}/\text{Al}$, a $\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x/\text{Ti}/\text{Al}$, and a $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x/\text{Ti}_{0.1}\text{W}_{0.9}/\text{Al}$ metallization scheme. In the $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Ti}/\text{Al}$ and $\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x/\text{Ti}/\text{Al}$ configurations the sandwiched titanium layer was used to provide an increased adhesion between the Al and the $\text{Ti}_{0.1}\text{W}_{0.9}$ -based pseudo-alloy, while $\text{Ti}_{0.1}\text{W}_{0.9}$ was used alternatively in the $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x/\text{Ti}_{0.1}\text{W}_{0.9}/\text{Al}$ configuration for a better adhesion to both the overlying Al film and the underlaying n^+ poly-Si emitter surface.

The $\text{Ti}_{0.1}\text{W}_{0.9}$ and $\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x$ metal films were prepared in a multitarget r.f sputtering system with $\text{Ti}_{0.1}\text{W}_{0.9}$ being sputtered in pure argon (99.999%) or in a mixed N_2 -Ar (1:4) ambient accordingly, at $\sim 1.4\text{ kV}$ r.f bias with the system having a $(3-5)\times 10^{-7}$ Torr base pressure and a partial argon pressure of 8×10^{-3} Torr. A separate vacuum system was used to deposit the desired aluminum or titanium/aluminum films by e-beam evaporation, where in the case of titanium/aluminum the two corresponding films were deposited sequentially without breaking vacuum. Individual wafer processing details indicating the particular metal deposition parameters, deposition sequence and resultant metal film thicknesses for each separate configuration are presented in more detail in Table 3.4.1. Photolithography and chemical etching was used to define the desired diodes. Phosphoric acid was used to etch the excess aluminum, while the excess Ti, $\text{Ti}_{0.1}\text{W}_{0.9}$ and $\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x$ were all etched in a mixed solution of ammonium-hydroxide/hydrogen-peroxide/water (1:1:5) heated to 75°C .

To determine the reliability limit of the $\text{Ti}_{0.1}\text{W}_{0.9}$ -based diffusion barrier in each configuration, subsequent heat treatments were carried out in a hydrogen ambient by increasing the furnace temperature until degradation of the diode's

TABLE 3.4.1: INDIVIDUAL WAFER PROCESSING DETAILS OF METAL DIFFUSION BARRIERS ON POLY-Si/SILICON DIODES AND SUBSEQUENT POST-METALLIZATION HEAT TREATMENTS UNTIL DIODE JUNCTION INTEGRITY DEGRADATION.

Wafer No.	Poly-Si Emitter Thickness (Å)	Metal Target	Ar gas Flow (sccm)	N ₂ gas Flow (sccm)	Base Pressure (Torr)	Ar gas Partial Pressure (Torr)	RF Power (Watts)	RF Peak Voltage (kV)	Deposition Time (min)	Deposited Film Thickness (Å)	Resulted Metal Film	Ti (e-beam) Thickness (Å)	Al (e-beam) Thickness (μm)	Subsequent Heat Treatment Until Aluminum Spikethrough (°C)	Annealing Time (min)
GT-N-5	~1,250	TiW	92.3	-	3×10^{-7}	8×10^{-3}	100	1.4	10	~1,000	TiW	500	0.5	400 500	20 15
GT-N-6	~1,250	TiW	92.3	-	5×10^{-7}	8×10^{-3}	100	1.4	10	~1,000	TiW	-	1.0	450 500	20 15
GT-N-7	~1,250	TiW	40.0	10.0	4.4×10^{-7}	8×10^{-3}	105	1.45	13	~1,000	TiWN _x	500	1.0	500 600 650 700	15 15 10 10
GT-N-8	~1,250	TiW	40.0	10.0	4.4×10^{-7}	8×10^{-3}	105	1.45	13	~1,000	TiWN _x	500	0.5	400 500 550 600 650 700	20 15 15 15 10 10
GT-N-11	~1,250	TiW TiW TiW	92.3 40.0 92.3	- 10.0 -	3.4×10^{-7} 3.4×10^{-7} 3.4×10^{-7}	8×10^{-3} 8×10^{-3} 8×10^{-3}	100 100 100	1.4 1.45 1.4	4 10 4	~400 ~700 ~400	TiW / TiWN _x / TiW	-	1.0	450 500 600 650	20 15 15 15

junction integrity occurred. The applied heat treatment steps in each corresponding configuration are listed in Table 3.4.1.

Figure 3.4.1 presents the dark J-V characteristics of a $300 \times 300 \mu\text{m}$ n^+ poly-Si /Si diode contacted by $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Al}$ ($1000\text{\AA}/1.0\mu\text{m}$) after deposition and subsequent heat treatments at 450°C and 500°C respectively. As seen in this figure, the junction integrity of the diode was preserved after a 20 minute annealing at 450°C , while the diode was shorted after a subsequent 500°C annealing for 15 minutes. Similar results were also obtained with the $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Ti}/\text{Al}$ ($1000\text{\AA}/500\text{\AA}/0.5\mu\text{m}$) contact system, where severe pitting was observed after a 15 minute annealing at 500°C resulting in complete diode degradation. From these results, it is concluded that pure $\text{Ti}_{0.1}\text{W}_{0.9}$ can be used as a reliable diffusion barrier against Al only up to a 450°C heat treatment. Although other reports [TiWi82], [GBFM78] showed that TiW/Al is very stable up to 500°C for 30min, a lower vacuum ($\sim 0.5 \times 10^{-5}$ Torr) was used in these cases during the TiW deposition, and thus a higher oxygen concentration level could have attributed to the better diffusion barrier properties of the TiW film, as it was proved in a similar study done by Baker et.al [BBNE80].

However, the diffusion barrier properties of $\text{Ti}_{0.1}\text{W}_{0.9}$ were improved substantially when $\text{Ti}_{0.1}\text{W}_{0.9}$ was sputtered in a mixed N_2 -Ar (1:4) ambient, as can be deduced from the dark J-V characteristics of the $\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x/\text{Ti}/\text{Al}$ ($1000\text{\AA}/500\text{\AA}/1.0\mu\text{m}$) contacted n^+ poly-Si bilayer emitter diode shown in Figure 3.4.2, where the $\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x/\text{Ti}/\text{Al}$ contact system proved to be very stable up to a 650°C annealing for 10 minutes with very low leakage currents. Although a number of diodes were shorted after a subsequent annealing at 700°C for 10 minutes at isolated areas where pitting was observed, the junction integrity of several diodes was preserved indicating that even at this temperature range

Figure 3.4.1: Dark J-V characteristics of a $300 \times 300 \mu\text{m}$ n^+ poly-Si bilayer emitter diode contacted by $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Al}$: A) before annealing B) after H_2 annealing at 450°C for 20min and C) after H_2 annealing at 500°C for 20min.

Figure 3.4.2: Dark J-V characteristics of a $300 \times 300 \mu\text{m}$ n^+ poly-Si bilayer emitter diode contacted by $\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x/\text{Ti}/\text{Al}$: A) before annealing B) after subsequent H_2 annealings at 500°C for 15min ; 600°C for 15min ; 650°C for 10 min and C) after H_2 annealing at 700°C for 10min(—, --).

Figure 3.4.3: Dark J-V characteristics of a $300 \times 300 \mu\text{m}$ n^+ poly-Si bilayer emitter diode contacted by $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x/\text{Ti}_{0.1}\text{W}_{0.9}/\text{Al}$: A) before annealing B) after subsequent H_2 annealings at 450°C for 20min ; 500°C for 15min ; 600°C for 15min and C) after H_2 annealing at 650°C for 15min.

aluminum migration through the $\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x$ barrier is localized, occurring at weak spots in the $\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x$ film. Nevertheless, even for the diodes that remained intact after the 700°C heat treatment, an increase in the series resistance which is evident in Figure 3.4.2 from the early departure of the corresponding curve's slope (C-solid line) at lower current densities, indicates that intermixing takes place.

Finally, the $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x/\text{Ti}_{0.1}\text{W}_{0.9}/\text{Al}$ ($400\text{\AA}/700\text{\AA}/400\text{\AA}/1.0\mu\text{m}$) contact system was found to be stable up to 600°C annealing for 15 minutes, as deduced from Figure 3.4.3, while the diodes were shorted when a subsequent heat treatment step was performed at 650°C for 15 minutes. The better reliability performance of the $\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x/\text{Ti}/\text{Al}$ contact system as compared to $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x/\text{Ti}_{0.1}\text{W}_{0.9}/\text{Al}$ in this case, is believed to be attributed to the formation of an oxynitride layer at the $\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x$ film's surface prior to the deposition of the Ti/Al bimetal in the former system, that could have enhanced the barrier diffusion capability of the $\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x$ layer against Al.

Summarizing these results, it is concluded that although pure $\text{Ti}_{0.1}\text{W}_{0.9}$ failed as a diffusion barrier for heat treatments in excess of 450°C , the incorporation of nitrogen in the $\text{Ti}_{0.1}\text{W}_{0.9}$ film affects profoundly the diffusion barrier capabilities of $\text{Ti}_{0.1}\text{W}_{0.9}$ by increasing its blocking capabilities to Al migration through it, and thus enabling $\text{Ti}_{0.1}\text{W}_{0.9}\text{N}_x$ contacts to be used as high temperature diffusion barriers to heat treatments as high as 650°C .

CHAPTER 4

PHOTOVOLTAIC PERFORMANCE OF POLY-Si/a-Si BILAYER EMITTER SOLAR CELLS : EXPERIMENTAL RESULTS AND DISCUSSION

4.1 INTRODUCTION

The evaluation of the photovoltaic performance of the poly-Si/a-Si bilayer emitter solar cells fabricated in this work under the various guidelines set out in the past two chapters is the last step involved towards characterizing these devices and thus evaluating how well they work in comparison with other cells under illumination.

In this chapter, the illuminated characteristics of the poly-Si/a-Si bilayer emitter solar cells are examined and compared to those of a c-Si phosphorus predeposited emitter cell whose fabrication details are listed in Appendix 2. For reasons to be explained in the following subsection, the short circuit photocurrent I_{sc} of the solar cells was measured under natural sunlight, while absolute spectral response measurements carried out at the Radiometry and Photometry division of NRC (National Research Council) were used to estimate the amount of the photocurrent loss in the poly-Si/a-Si emitter layer. The fill factor FF and the open circuit voltage V_{oc} of the solar cells were determined from the illuminated J-V characteristics of the devices under AM1.5(100mW/cm²) conditions simulated with the aid of a solar simulator provided by TPK Solar Systems Inc.

In order to estimate the photocurrent loss in the poly-Si/a-Si bilayer emitter, uncoated cells were used for direct comparison of the short circuit current of the

poly-Si/a-Si bilayer emitter devices to that measured from the c-Si predeposited emitter cell, since variations in the properties of an applied antireflection coating from cell to cell (ie refractive index, absorbance, surface reflectance) can give misleading results. Poly-Si/a-Si bilayer emitter solar cells fabricated on a variety of substrates with different bulk resistivities were also examined in order to determine how the quality of the substrate itself affects individual output parameters of the solar cells.

A high accuracy ammeter (Keithley 177 DMM) was used to measure the short circuit photocurrent of the devices, while an HP4145A semiconductor parameter analyzer was used to obtain the illuminated J-V characteristics under simulated sunlight conditions. Most of the results are either presented in a tabular form or in the form of graphs followed by a corresponding discussion.

4.2 NATURAL SUNLIGHT PHOTOCURRENT MEASUREMENTS

One of the most important parameters for the determination of the short circuit photocurrent of a solar cell is the energy distribution of the illumination spectrum itself. For the purpose of getting reproducible results, light sources other than natural sunlight are commonly used in the laboratory to simulate the solar spectrum in order to avoid irradiance variations in the latter case due to changes in atmospheric conditions. However, regardless of the solar simulator used, the spectral irradiance distribution of simulated sunlight can only approximate that of the desired standard solar irradiance, while it varies considerably among different solar simulators [SADE80]. Thus, depending on the spectral response of the solar cell under examination and the spectral deviation of the simulator from the desired solar energy distribution, the short circuit photocurrent of the test cell will vary with the choice of the simulated

illumination spectrum [JeWo86], [SADE80]. Even though the illumination intensity of the selected light source can be adjusted to give the rated short circuit current under specified air mass conditions in a calibrated standard cell, it has been shown by Seaman et al [SADE80] that if spectral response mismatch exists between the standard cell and the test cell under examination, an error in the measured short circuit current will be induced being proportional to this mismatch and to the deviation of the simulator's spectral irradiance from the standard solar irradiance. Therefore, although simulated sunlight can be used to provide reproducible illuminated J-V characteristics, an error in the short circuit current will inevitably occur under the circumstances mentioned above.

Because the photocurrent loss of the poly-Si/a-Si bilayer emitter solar cells is mainly associated with a reduced short wavelength response, measurements of the short circuit current of these devices with the currently available 300W Tungsten filament light source (incandescent lamp), that has been used in the past by other workers at Carleton U. [Nort80], [Norm79], [Ther79], will not be very reliable in this case since such a light source exhibits very low short wavelength intensities while on the other hand it produces enhanced infra-red intensities, and consequently its use will result in an overestimate of the poly-Si/a-Si bilayer emitter cell's short circuit current. The spectral irradiance distribution of a characteristic 300W Tungsten filament incandescent lamp with its intensity set at 100mW/cm^2 is shown in figure 4.2.1, as taken from Seaman et al [SADE80], where it is compared along with standard AM1.5 and AM0 spectral irradiances. Comparison of the poly-Si/a-Si bilayer emitter cell's short circuit current to that of a c-Si phosphorus predeposited emitter cell will be meaningless if the tungsten source is used as a solar simulator. The very low short wavelength spectral

Figure 4.2.1: Spectral irradiance distribution of a 300W Tungsten filament light source with its intensity set at $100\text{mW}/\text{cm}^2$ take from reference [SADE80] as compared to standard AM1.5 and AM0 spectral irradiances.

irradiance of the tungsten source will be insufficient in producing appreciable photocurrents in the ultra-violet and blue spectral regions, that are of particular interest in this work, to observe any appreciable photocurrent difference between the two different structure cells despite the enhanced response of the c-Si predeposited emitter reference cell in the short wavelength regions. Furthermore, the very high infra-red irradiance of the tungsten source will more likely overshadow the utilization effects of the ultra-violet and blue irradiance.

On the other hand, despite the reproducibility problems associated with changing atmospheric conditions, natural sunlight can provide a realistic spectral irradiance distribution when outdoors measurements are carried out on a clear day, and if proper precautions are taken to avoid collection of light reflected from nearby objects (usually buildings) the measured short circuit photocurrent of the test cell under examination will represent the actual maximum possible short circuit current under the specific air mass conditions examined. Having in mind the above considerations, natural sunlight was considered to be the best currently available light source option in evaluating more accurately both the short circuit photocurrent of the poly-Si/a-Si bilayer emitter solar cells and that of the c-Si phosphorus predeposited emitter cell, from which measurements a meaningful comparison can be made between these two devices, and the photocurrent loss of the poly-Si/a-Si bilayer emitter cell can be estimated.

The short circuit photocurrent measurements in natural sunlight were carried out in Ottawa (45°N latitude) during the months of May and June, only on very clear days and within one hour from solar noon* with solar altitudes varying between 63° and 68° (28°-22° from Zenith) depending on the specific day

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* Solar noon in the months of May and June is 17min and 22min earlier than actual local noon respectively.

and time of the measurements. A portable chuck with a movable probe, along with a high accuracy ammeter (Keithley 177 DMM), were used for the short circuit current measurements, while measurements were done on the 2x2cm cells with the sun rays incident on a horizontal surface. A calibrated 2x2cm back-surface field space-cell provided by ASEC (Applied Solar Energy Corporation) with a AM1 rated photocurrent of 142mA was used as a standard reference cell for indirect indication of the level of the total incident solar irradiance intensity.

Preselected representative uncoated poly-Si/a-Si bilayer emitter solar cells with 1.8-2.6 Ω .cm substrates along with a high quality FZ 0.1 Ω .cm substrate were tested and compared to an uncoated c-Si phosphorus predeposited emitter cell with a 1.8-2.6 Ω .cm substrate. The results of these photocurrent measurements are shown in Table 4.2.1. Nearly identical short circuit photocurrents were measured with the standard cell just prior to and after each measurement was performed on the test cells under examination, indicating that there was no fluctuation on the incident solar irradiance during these measurements. However, a variation in the incident solar irradiance intensity was noted for the measurements that were carried out on different days, mainly as a result of a different solar altitude at the time of the corresponding measurements, and probably different water vapour content in the atmosphere as well, where in each case the short circuit photocurrent of the standard cell was found to be within 7% and 2.8% respectively of its AM1 rated value. Thus, in order to facilitate direct comparison among the results of the uncoated test cells, the tabulated measured photocurrents were normalized so as to give the corresponding AM1 values shown in Table 4.2.1, where the normalization constant used was the ratio of the standard cell's AM1 rated photocurrent over its measured photocurrent for each individual case.

Table 4.2.1: Estimated total area AM1 photocurrent density J_{sc} for 2x2cm poly-Si/a-Si emitter cells, calculated based on the measured photocurrent I_{sc} on uncoated cells in natural sunlight and the corresponding measured photocurrent I_{sc}^* of the (ASEC) control cell. The poly-Si/a-Si emitter cell's total photocurrent loss is also shown as calculated from the photocurrent difference with the c-Si predeposited emitter cell.

Solar Cell #	Emitter Thickness	Measured Photocurrent I_{sc}	Control Cell's Photocurrent I_{sc}^*	AM1 Conversion Factor I_{sc}^{**}/I_{sc}^*	Estimated AM1 Photocurrent Density $J_{sc} = I_{sc}(I_{sc}^{**}/I_{sc}^*)/4$	Poly-Si/a-Si Emitter Cell's Total Photocurrent Loss ΔJ_{sc} (AM1)
(Substrate Resistivity)	($\text{\AA}$)	(mA)	(mA)	-----	(mA/cm ²)	(mA/cm ²)
c-Si predep	1,500	88.8	132	142/132	23.88	---
11 (1.8 Ω .cm)	1,440	75.9	132	142/132	20.41	3.47
12 (1.8 Ω .cm)	1,400	77.2	132	142/132	20.76	3.12
110 (1.8 Ω .cm)	925	86.5	138	142/138	22.25	1.63
19 (0.1 Ω .cm)	1,400	76.3	138	142/138	19.63	4.25

I_{sc}^* : control cell's (ASEC) measured photocurrent.

I_{sc}^{**} : control cell's (ASEC) AM1 rated photocurrent.

As expected, all the estimated AM1 photocurrent densities of the poly-Si/a-Si bilayer emitter cells were lower than that of the c-Si emitter cell. A $\sim 23.9 \text{ mA/cm}^2$ value was estimated for the c-Si predeposited emitter cell while an increasing photocurrent density is noted with decreasing emitter thickness for the poly-Si/a-Si bilayer emitter cells with the $1.8\text{-}2.6 \Omega\cdot\text{cm}$ substrates, from a value of $\sim 20.4 \text{ mA/cm}^2$ for a $1,440 \text{ \AA}$ poly-Si/a-Si emitter thickness to a value of $\sim 22.3 \text{ mA/cm}^2$ for a $925 \text{ \AA}$ thick poly-Si/a-Si emitter layer. The lowest photocurrent density was obtained from the poly-Si/a-Si bilayer emitter cell with the $0.1 \Omega\cdot\text{cm}$ FZ substrate, whose estimated AM1 photocurrent density of 19.63 mA/cm^2 was found to be $\sim 1 \text{ mA/cm}^2$ lower from that of a poly-Si/a-Si bilayer emitter cell (#2) with the same emitter layer thickness but with a $1.8\text{-}2.6 \Omega\cdot\text{cm}$ substrate. This photocurrent difference is attributed to a lower substrate collection efficiency of minority carriers due to a shorter diffusion length of the photo-generated minority carriers in the $0.1 \Omega\cdot\text{cm}$ Wacker FZ substrate which as reported by Green et al [GBJK84] lies in the $150 \mu\text{m}$ range.

In order to justify that a meaningful estimate of the total photocurrent losses of the poly-Si/a-Si bilayer emitter cells can be made from the direct comparison of the short circuit photocurrents between the poly-Si/a-Si bilayer emitter cells and the c-Si predeposited emitter cell, some characteristic properties of the c-Si predeposited emitter cell will be first presented in order to show that the emitter layer of such a cell is characterized by a high collection efficiency which thus make it a valid realistic reference for photocurrent comparison purposes.

As seen from the simulated (SUPREM III) phosphorus active impurity profile of the c-Si predeposited emitter cell shown in figure 4.2.2, the active surface phosphorus concentration in the crystalline silicon emitter is $\sim 1.5 \times 10^{20} \text{ atoms/cm}^3$, while the phosphorus concentration falls off rapidly into the emitter.

Figure 4.2.2: Total phosphorus concentration profile of the c-Si predeposited emitter solar cell. The active impurity profile coincides with the chemical impurity profile in this case.

The phosphorus active impurity profile actually coincides in this case with the corresponding chemical profile, and the fact that the phosphorus surface concentration is below the solid solubility limit implies that a "dead" layer in the c-Si emitter is non-existent. Such a profile is known to result in an enhancement of the short wavelength response as a consequence of a reduction in both surface recombination rates and bulk emitter recombination effects [GBGW82], [GBSK84]. The reduction of the surface recombination rates is associated with the very high (but below the solid solubility limit) phosphorus surface concentration. It is believed [GBSK84] that in such a layer degeneracy dominates other heavy doping effects (ie bandgap narrowing and increased surface state densities), and effectively suppresses surface minority carrier concentrations. On the other hand, the reduction of the recombination effects in the bulk of the emitter is attributed to the rapid decrease of the phosphorus concentration near the top surface, as a consequence of which the doping levels across most of the shallow emitter are low enough to suppress Auger recombination [GBGW82], [Redf81].

Figure 4.2.3 shows the absolute spectral response of an uncoated c-Si predeposited emitter cell fabricated in this work as compared to that of a standard c-Si diffused emitter cell with an antireflection coating taken from reference [Norm79]. As seen in this figure, an enhanced short wavelength response is indeed obtained with the c-Si predeposited emitter cell despite the known high reflection losses associated with the bare surface of c-Si that account for as much as 70-40% of the non-utilized light in the $0.3\mu\text{m}$ to $0.5\mu\text{m}$ spectral range of interest as indicated from the reflectance curve shown. Using the absolute spectral response measurements of the c-Si predeposited emitter cell and the known AM1.5 spectral power density distribution [Curt77], the AM1.5 spectral photocurrent contribution of the actually collected photogenerated minority carriers was

Figure 4.2.3: Measured absolute spectral response of an uncoated c-Si predeposited emitter cell as compared to that of a standard c-Si diffused emitter cell with an antireflection coating taken from reference [Norm79]. An enhanced short wavelength response is obtained with the c-Si predeposited emitter cell despite the high reflectance of the bare c-Si surface in this region.

calculated and compared to that of the estimated photo-generated minority carriers that would be collected under AM1.5 conditions in the case of no recombination. Figure 4.2.4 shows the spectral collection efficiency $C(\lambda)$ of the photogenerated minority carriers in the c-Si predeposited emitter cell as was calculated from the ratio of the actually collected photogenerated minority carriers to the maximum possible collected photogenerated minority carriers in the case of no recombination, given by:

$$C(\lambda) = \frac{ASR(\lambda) P_{AM1.5}(\lambda)}{q[1-R(\lambda)] N(\lambda,0) (1-e^{-a(\lambda) \cdot x_s})} \quad (4.2.1)$$

where, $ASR(\lambda)$ is the measured absolute spectral response, $P_{AM1.5}(\lambda)$ is the AM1.5 spectral power density distribution, $R(\lambda)$ the surface reflectance of c-Si, $N(\lambda,0)$ the incident photon flux under AM1.5 conditions, $a(\lambda)$ the absorption coefficient of c-Si and x_s the distance from the top surface of the cell.

As seen in figure 4.2.4, the collection efficiency is very close to unity (98%) for most of the utilizeable spectrum of interest with an average collection efficiency of more than 90% noted for the minority carriers photogenerated from the blue spectral region. Thus, it is evident that the emitter layer of the c-Si predeposited emitter cell is characterized by a high minority carrier collection efficiency and consequently the total photocurrent losses of the poly-Si/a-Si bilayer emitter cells can be estimated in good approximation by comparing the short circuit photocurrent of these devices to that obtained from the c-Si predeposited emitter cell.

The estimated total photocurrent losses of the poly-Si/a-Si bilayer emitter cells are shown in Table 4.2.1, as were simply calculated from the photocurrent difference of the estimated AM1 short circuit photocurrent of the poly-Si/a-Si

Figure 4.2.4: Calculated spectral collection efficiency of the c-Si predeposited emitter cell.

emitter cells with respect to the c-Si predeposited emitter cell. A total photocurrent loss of 3.47mA/cm^2 was estimated for a solar cell (#1) with a $1,440\text{\AA}$ poly-Si/a-Si bilayer emitter thickness, while a solar cell (#10) with a $925\text{\AA}$ thick poly-Si/a-Si bilayer emitter shows a total photocurrent loss of only 1.63mA/cm^2 . Finally, the poly-Si/a-Si bilayer emitter cell with the $0.1\ \Omega\cdot\text{cm}$ FZ substrate (#9) exhibits the highest photocurrent loss of 4.25mA/cm^2 , part of which as explained earlier is believed to be attributed to a lower substrate collection efficiency.

Although the photocurrent loss associated with the poly-Si/a-Si bilayer emitter itself is expected to be very close to the values mentioned above, the total photocurrent losses reported here account also for small photocurrent differences associated with quality variations among the substrates themselves, and thus a better estimate of the emitter photocurrent losses cannot be made at this point from the natural sunlight results alone. Nevertheless, these results indicate that the photocurrent losses of the poly-Si/a-Si bilayer emitter cells are not severe, and that the losses can be reduced by decreasing the emitter thickness.

4.3 ABSOLUTE SPECTRAL RESPONSE CHARACTERISTICS AND DETERMINATION OF PHOTOCURRENT LOSSES

The most useful and detailed information concerning how effectively a solar cell structure collects photogenerated minority carriers can be obtained through the measurement of its spectral response over the entire utilizable solar spectrum. In this subsection, accurate estimates of the photocurrent losses associated with the emitter layer of the poly-Si/a-Si bilayer emitter cells are presented based on spectral response measurements.

The primary method that is commonly used to measure the spectral response of a test cell involves the direct comparison of the short circuit current per unit incident light power per unit wavelength of the test cell to that obtained from a calibrated cell when both cells are illuminated by the same narrow band source. However, for this method to be accurate it is required that both the test cell and the calibrated reference cell must have similar spectral responses within specified limits, dictating that they both be made from the same semiconductor material using similar processing techniques. Because the spectral response of the poly-Si/a-Si bilayer emitter cells is compared in this study to that of a c-Si phosphorus predeposited emitter cell, where the emitter layers of the two solar cell structures are formed from different material structures using different processing techniques, absolute spectral response measurements were performed in this work using instead a thermopile detector to indicate the intensity of the incident spectral irradiance, so that the measurements could be independent from specific material related calibration dependencies.

The absolute spectral response measurements were carried out at the Radiometry and Photometry Division of Physics at NRC, using a grating mono-

chromator and appropriate interference filters to select discrete wavelengths at 10nm intervals from the 250-450nm spectral range of a xenon light source's spectrum and from the 450-1200nm spectral range of a tungsten light source's spectrum respectively. Errors associated with the absolute thermopile detector calibrations were guaranteed to be within $\pm 5\%$ in the 250-350nm spectral range and within $\pm 3\%$ in the 350-1200nm range respectively. All solar cells under examination were found to be linear to increasing light intensity tests.

In order to estimate the photocurrent losses associated with the emitter layer of the poly-Si/a-Si bilayer emitter cell, the spectral range of the incident irradiance that is utilized in the emitter layer of these cells must be identified. Figure 4.3.1 shows the measured absolute spectral responses of two poly-Si/a-Si bilayer emitter cells whose emitter thicknesses lie within the 1,400-1,450Å range, with the poly-Si/a-Si bilayers being characterized by the same overall electrical and material properties due to their identical processing procedure, while having different c-Si substrates of similar thicknesses ($\sim 300\mu\text{m}$) which are however characterized by different electrical and material properties; one being a Ventron 1.8-2.6 $\Omega\cdot\text{cm}$ substrate and the other being a high quality 0.1 $\Omega\cdot\text{cm}$ Wacker FZ substrate. Since the collection of the photogenerated minority carriers in the solar cell depends mainly on their diffusion length which in turn is governed by the material properties and structural design of the cell itself, considering that the emitter layers of both cells are characterized by the same overall properties, the departure of the shown response curves at the starting edge of the infra-red region and their corresponding infra-red response difference is thus attributed to the different substrate material properties of the cells, with the 0.1 $\Omega\cdot\text{cm}$ Wacker FZ substrate characterized by a shorter diffusion length as implied from the corresponding lower infra-red response of that cell.

Figure 4.3.1: Comparison of measured absolute spectral responses of two uncoated poly-Si/a-Si bilayer emitter cells with similar poly-Si/a-Si bilayer emitter thicknesses, lying in the 1,400Å-1,450Å thickness range, and with similar thickness (~300μm) p-type c-Si substrates but of different electrical and material properties; one being a Ventron 1.8-2.6Ω.cm substrate (used in conjunction with the 1,450Å thick poly-Si/a-Si bilayer emitter), and the other being a 0.1Ω.cm Wacker FZ substrate (used in conjunction with the 1,400Å thick poly-Si/a-Si bilayer emitter).

Thus, since the structural design of the two cells is similar and their infra-red response difference is attributed to the different substrate material properties of the cells, the almost identical responsivities of the two cells in the short and intermediate wavelengths imply that poly-Si/a-Si bilayer emitters with emitter thicknesses in the proximity of $1,450\text{\AA}$ absorb strongly in, not only the ultra-violet and blue spectral regions of the incident irradiance, but also the entire visible spectral range as it is deduced from the departure of the two response curves at $\sim 0.75\mu\text{m}$. Furthermore, in order to account for spectral response differences due to the $\sim 50\text{\AA}$ emitter thickness difference of the two cells as well as due to the $\pm 3\%$ possible error in the measurements (due to NRC's calibrations), the spectral range of the $\sim 1,450\text{\AA}$ bilayer emitter's responsivity can be further slightly extended to include the $0.75\text{-}0.80\mu\text{m}$ part of the infra-red spectral range as well, in order to purposely represent a worst case situation.

This result came initially as a surprise because it was originally assumed that the absorption coefficient of the poly-Si/a-Si bilayer emitter would be very close to that of single crystal silicon, and thus only the ultra-violet and blue regions of the spectrum were expected to be absorbed strongly in a $\sim 1,500\text{\AA}$ thick front surface layer. The latter contention is clearly demonstrated in Figure 4.3.1.A) from the light penetration depth that is expected in a c-Si emitter cell according to the absorption coefficient of c-Si per given wavelength, both of which were calculated based on information taken from reference [RaSS79]. Although as grown in-situ doped a-Si, which forms the upper layer of the poly-Si/a-Si bilayer emitter cells and constitutes most of the emitter thickness ($\sim 85\%$ in this case), is associated with a much higher absorption coefficient than c-Si [HKS83], such films have been found to exhibit a very high structural perfection [WaTa88], [HKS83] and an absorption coefficient very close to that of c-Si [HKS83] when

Figure 4.3.1.A) : Light penetration depth in c-Si films as calculated from the absorption coefficient of c-Si in the 0.30-0.70 μm spectral range based on relevant information taken from [RaSS79]. It is evident that only the ultra-violet spectrum of the incoming light is strongly absorbed in a $\sim 1,500\text{\AA}$ c-Si film, while at least a $\sim 5,000\text{\AA}$ thick film of c-Si is needed to absorb strongly in both the ultra-violet and blue spectral range of the incoming light.

they are recrystallized by thermal annealing as in the present case. Nevertheless, after scrutinizing the reported results of those references, it was noticed that the results on the absorption coefficient of the in-situ doped recrystallized a-Si reported by Harbeke et al [HKS83] have been obtained on much thicker as-grown a-Si films of $\sim 5,000\text{\AA}$ thickness that have been recrystallized under a high temperature annealing treatment of $900\text{--}1000^\circ\text{C}$ resulting in average grain sizes in the order of $\sim 2,700\text{\AA}$, while the Raman scattering experiments, that determined the structural quality of the low temperature annealed films in the work performed by Waechter et al [WaTa88] was carried out on films with thicknesses in the proximity of $\sim 7,000\text{\AA}$.

Since grains grow during deposition with increasing deposition time minimizing the amount of grain boundaries per unit volume [FaBu83], [KiSK83], [BMZS85], when considering films deposited using similar overall deposition parameters, thicker films will consist of grains with larger average grain sizes while the overall structural quality of the films is expected to improve as the grains grow larger. The as-grown in-situ doped a-Si films of the poly-Si bilayer emitter cells examined here were only $\sim 1,200\text{\AA}$ thick in this case, and thus their average grain sizes are expected to be much smaller than those of the corresponding films examined by the other workers [WaTa88], [HKS83], incorporating a larger amount of grains per unit volume and consequently a larger amount of grain boundaries per unit volume. Because of these properties of the as-grown a-Si films, it is believed that after the low temperature annealing that was performed in this work at 650°C , the resultant recrystallized a-Si films were of lower structural quality than those reported by [WaTa88], [HKS83] having smaller grains and thus maintaining a larger amount of grain boundaries per unit volume. Any combination of these structural effects could have resulted

in a higher absorption coefficient of these films, since grain boundaries can act as light scattering regions, while on the other hand the higher the disorder and the amount of defects in the structural quality of the films the lower will be its optical gap and consequently the higher will be its absorption coefficient [ie $\alpha(hf) \propto (hf - E_g)^{1/2}$] [OvMe86]. However, although the absorption coefficient of the recrystallized a-Si film of these poly-Si/a-Si bilayer emitter cells could have been higher than expected, it is believed that it is rather the very thin ($\sim 200\text{\AA}$) underlying as-grown poly-Si layer that absorbs the greater part of the visible spectral range, since such a thin poly-Si film would consist of highly disordered regions composed of very small grains and a large amount of (wider) grain boundaries per unit volume that could have given rise to a large amount of internal light scattering resulting in an increased absorption coefficient. This trend is also in agreement with Harbeke et al [HKS83] who report that even the $\sim 5,000\text{\AA}$ thick as-grown in-situ doped poly-Si films when annealed at high temperatures ($900-1000^\circ\text{C}$) exhibit an absorption coefficient almost twice of that of c-Si, while the average grain size of these films have been found to be half the average grain size of recrystallized a-Si films with the same thickness that were annealed under the same conditions. Unfortunately, reflectance and transmittance measurements of the poly-Si/a-Si bilayer films and/or their individual sublayers, that would have otherwise determined their absorption coefficient, were not made due to the unavailability of proper optical set-ups.

Because the absorption coefficient of the poly-Si/a-Si bilayer films is unknown, the exact actual photocurrent loss associated with the emitter layer of the poly-Si/a-Si bilayer emitter solar cells examined in this work could not be calculated directly from the absolute spectral response measurements. The best alternative method to get the closest estimate of the actual photocurrent losses

associated with these devices was to compare the absolute spectral response of the poly-Si/a-Si bilayer emitter cells to that of a c-Si phosphorus predeposited emitter cell with an enhanced blue response. Although the c-Si emitter cell itself suffers some photocurrent losses from its emitter layer, the collection efficiency of that cell has been found to be very high in most of the utilizable spectrum of interest (0.3-0.8 μ m), being close to unity in the visible spectral range and very high in the blue region (82-97%), while being lower (40-82%) but nevertheless high enough in the ultra-violet region (to contribute some measurable photocurrent) as was shown in Figure 4.2.4. Even though the collection efficiency of the photogenerated minority carriers in the c-Si emitter cell associated with the utilization of the ultra-violet spectral range is not very high, since incoming photons from that region are very energetic (>6eV) with most of their energy that is larger than the band gap of c-Si (~1.12eV) being dissipated as heat rather than creating excess electron-hole pairs, the sensitivity of any solar cell to that spectral region will be very small and therefore the utilization of this spectral range will result in a very small photocurrent contribution even under ideal conditions with no recombination effects. Thus, although the photocurrent loss associated with the photogenerated minority carriers induced from the utilized ultra-violet spectral range in the emitter layer of the uncoated c-Si emitter cell is moderate as compared to the overall ideal photocurrent contribution from that spectral range, it is very small in magnitude having an estimated value of ~0.2mA/cm² at AM1.5 under ideal conditions (no recombination effects). The estimated corresponding photocurrent losses associated with the utilization of the blue and visible spectral regions respectively are similarly small, with ~0.2mA/cm² in photocurrent loss accounted for by the non-collected minority carriers photo-induced from the blue region and ~0.3mA/cm² respectively from the visible region. Consequently, a comparison of the absolute spectral responses

of the two different solar cell structures will give a very good, almost accurate, indication of the amount of photocurrent losses associated with the emitter of the poly-Si/a-Si bilayer emitter cells, while at the same time it will make an excellent comparison of the photovoltaic conversion performance of the poly-Si/a-Si bilayer emitter cells to a very shallow c-Si emitter cell structure with minimum realistic photocurrent losses that has been used as a basic standard design on recent developments of very high efficiency state-of-the-art c-Si emitter cells [GBSK84], [GBWJ87].

Figure 4.3.2 shows the measured absolute spectral response of an uncoated poly-Si/a-Si bilayer emitter cell with a bilayer emitter thickness of $\sim 1,450\text{\AA}$, as compared to that of an uncoated c-Si phosphorus predeposited emitter cell with a $\sim 1,500\text{\AA}$ shallow c-Si emitter. As seen in this figure, the absolute spectral response of the poly-Si/a-Si bilayer emitter cell in the $0.25\text{-}0.90\mu\text{m}$ spectral range is lower than that of the c-Si emitter cell, with its average responsivity being estimated as $\sim 82\%$ of the corresponding c-Si emitter cell's average responsivity. The absolute spectral responses of the two different solar cell structures in the $0.90\text{-}1.20\mu\text{m}$ spectral range are almost identical with the poly-Si/a-Si bilayer emitter cell exhibiting a slightly higher (1%) average responsivity. However, as explained earlier based on evidence shown in Figure 4.3.1, only the part of the poly-Si/a-Si bilayer emitter cell's absolute spectral response curve that corresponds to wavelengths less than or equal to $0.80\mu\text{m}$ is mainly absorbed in the poly-Si/a-Si bilayer emitter itself, whose average responsivity is estimated to be $\sim 78\%$ of that corresponding to the c-Si emitter cell in the same spectral range. Similarly, the part of the absolute spectral response curve in the $0.80\text{-}0.90\mu\text{m}$ spectral range (as well as that in the $0.90\text{-}1.20\mu\text{m}$ spectral range) is believed to be part of the substrate responsivity of that device, whose average responsivity in that spectral

Figure 4.3.2: Measured absolute spectral response of an uncoated in-situ phosphorus doped poly-Si/a-Si bilayer emitter cell with a $\sim 1,450\text{\AA}$ thick poly-Si/a-Si bilayer emitter as compared to that of an uncoated shallow predeposited phosphorus doped c-Si emitter cell with a $\sim 1,500\text{\AA}$ thick emitter layer.

range is ~98% of the corresponding c-Si emitter cell's average responsivity.

Although the average responsivity of the 1,450Å thick poly-Si/a-Si bilayer emitter itself is as high as ~78% of the corresponding c-Si emitter cell's average responsivity in the same spectral range (0.29μm-0.80μm), its overall absolute spectral response in the ultra-violet region (<0.4μm) is very poor with its average responsivity being as low as ~5.5% of the c-Si emitter cell's average responsivity, indicating that most of the minority carriers photogenerated from the ultra-violet spectrum either recombine or are neutralized by defects before they have a chance to be collected. However, the poly-Si/a-Si bilayer emitter's responsivity shows a substantial increase for incident irradiances with wavelengths beyond the ultra-violet spectral range, where its moderate average responsivity in the blue spectral range (0.4-0.5μm), being ~42.5% of that corresponding to the c-Si emitter cell, indicates that a rather substantial amount of the photogenerated carriers induced from the blue spectrum are being collected. A much higher responsivity in the 0.5-0.8μm spectral range (visible and part of infra-red) with an overall average responsivity of as high as ~86.5% of that corresponding to the c-Si emitter cell is indicative of the very high collection probability associated with the photogenerated carriers induced from that spectral range. Since the intrinsic diffusion length of the photogenerated minority carriers in the poly-Si/a-Si bilayer emitter is believed to be very short due to the inherent high degree of defects associated with the polycrystalline structure of the recrystallized a-Si and poly-Si films, the steady substantial increase observed in the absolute spectral response of the 1,450Å poly-Si/a-Si bilayer emitter in the blue and the rest of the visible spectral region can not be accounted alone from the expected reduction in surface reflectivity with increasing wavelengths of incident light. It may be due to the growing magnitude of the built-in electric

field towards the junction, whose drifting influence on minority carriers becomes stronger as minority carriers are photogenerated closer to the junction. Thus, even though much of the utilizable light spectrum ($0.25\text{-}0.80\mu\text{m}$ in this case) is strongly absorbed in the $1,450\text{\AA}$ poly-Si/a-Si bilayer emitter itself where most of the photogenerated carriers would normally be expected to be lost by recombination or by defect neutralization, it is believed that the built-in electric field extends far enough into the $1,450\text{\AA}$ bilayer emitter towards the top surface, and since the drift distance " σ " that the photo-generated minority carriers can travel is proportional to the magnitude of the built-in electric field " $\mathcal{E}$ " (ie $\sigma = \mu \mathcal{E} \tau$, where μ is the minority carrier mobility and τ is its corresponding lifetime respectively) the collection probability of the photogenerated minority carriers will become larger as these minority carriers are photogenerated closer to the junction, thus resulting in the observed steady responsivity increase of the poly-Si/a-Si bilayer emitter associated with the blue and visible regions of the spectrum.

On the other hand, the lower observed substrate responsivity of the poly-Si/a-Si bilayer emitter cell in the $0.80\text{-}0.90\mu\text{m}$ spectral range, as compared to that corresponding to the c-Si emitter cell in the same spectral range, indicates that the collection probability of the photogenerated minority carriers induced from the above mentioned spectral range is smaller in the former case. This can be explained considering that the incident light irradiance from the $0.80\text{-}0.90\mu\text{m}$ spectral range is not absorbed as deep into the substrate of the poly-Si/a-Si bilayer emitter cell as in the case of the c-Si emitter cell's substrate but rather closer to the junction interface, and even though the diffusion length of the photogenerated carriers in the substrate of the poly-Si/a-Si bilayer emitter cell is the same as in the c-Si emitter cell's substrate, although a small difference may

exist due to substrate quality variations from cell to cell, the minority carriers induced from the $0.80\mu\text{m}$ - $0.90\mu\text{m}$ spectral range will have to travel a further distance in the former case in order to be collected and thus they will be characterized by a lower collection probability.

The measured absolute spectral response of another uncoated poly-Si/a-Si bilayer emitter cell having a thinner bilayer emitter of $\sim 925\text{\AA}$ thickness is shown in Figure 4.3.3 as compared to that of the uncoated phosphorus predeposited c-Si emitter cell with the $\sim 1,500\text{\AA}$ shallow c-Si emitter, while the measured absolute spectral response of the poly-Si/a-Si bilayer emitter cell with the $\sim 1,450\text{\AA}$ thick bilayer emitter is also shown for comparison purposes. As seen in this figure, the absolute spectral response of the $\sim 925\text{\AA}$ poly-Si/a-Si bilayer emitter cell is higher throughout the entire utilizeable light spectrum than that of the cell with the $\sim 1,450\text{\AA}$ thick poly-Si/a-Si emitter, exhibiting a more pronounced responsivity increase particularly in the visible and blue spectral regions as compared to that of the cell with the thicker emitter. This responsivity increase is mainly associated with the decrease in the poly-Si/a-Si emitter thickness in the former case, while its higher infra-red responsivity throughout the $0.75\mu\text{m}$ - $1.20\mu\text{m}$ is presumably the result of a slightly better quality substrate than that of the other cells. With its responsivity approaching closer to that of the c-Si emitter cell in the intermediate and short wavelengths, the overall average responsivity of the poly-Si/a-Si bilayer emitter cell with the $\sim 925\text{\AA}$ thick emitter in the 0.25 - $0.80\mu\text{m}$ spectral range has been estimated to be as high as $\sim 86.5\%$ of that corresponding to the c-Si emitter cell in that spectral range, being $\sim 10\%$ higher than that obtained with the $\sim 1,450\text{\AA}$ thick poly-Si/a-Si emitter in the same spectral range. In more details, in the visible spectral region the average responsivity of the poly-Si/a-Si bilayer emitter cell with the $\sim 925\text{\AA}$ thick bilayer emitter is $\sim 9.0\%$ higher of that

Figure 4.3.3: Measured absolute spectral response of an uncoated in-situ phosphorus doped poly-Si/a-Si bilayer emitter cell with a $\sim 925\text{\AA}$ thick poly-Si/a-Si bilayer emitter, as compared to that of an uncoated shallow predeposited phosphorus doped c-Si emitter cell with a $\sim 1,500\text{\AA}$ thick emitter layer. The measured absolute spectral response of the uncoated in-situ phosphorus doped poly-Si/a-Si bilayer emitter cell with the $\sim 1,450\text{\AA}$ thick poly-Si/a-Si bilayer emitter is also shown for comparison purposes.

obtained with the 1,450Å thick bilayer emitter, being as high as ~95% of that corresponding to the c-Si emitter cell in the same spectral range, indicating that most of the photogenerated carriers induced from that spectral range are being collected, while its average responsivity in the blue spectral region is estimated to be ~59% of the c-Si emitter's cell average responsivity in the same spectral region, being ~27.5% higher of that obtained with the thicker bilayer emitter in the blue spectral region, thus indicating that a substantially larger amount of photogenerated carriers induced from the blue spectral region is collected by this cell as compared to that of the thicker bilayer emitter. Finally, although its ultra-violet response is slightly higher than that of the cell with the thicker bilayer emitter, its responsivity in that region is very poor having an average value that has been estimated to be ~8.2% of that obtained with the c-Si emitter cell, indicating that still most of the photogenerated minority carriers induced from that region are either neutralized by defects or recombine before they have a chance to be collected.

Although the exact spectral range of the incident irradiance that is utilized in the ~925Å poly-Si/a-Si bilayer emitter is not known, since a comparison of such cells with different c-Si substrates but with similar poly-Si/a-Si bilayer emitter thicknesses (as in the case of the thicker poly-Si/a-Si bilayer emitter cells) was not made here, it is evident from the absolute spectral response comparison between the poly-Si/a-Si bilayer emitter cell with the ~925Å thick poly-Si/a-Si bilayer emitter and the c-Si emitter cell, that the upper wavelength of the utilized spectrum in the thinner bilayer emitter will be less than or equal to 0.8μm. In the case the absorption coefficient of the recrystallized a-Si layer itself is the same as that of the thicker bilayer emitter (the thickness of the poly-Si layer is the same in both cases), then more light is expected to penetrate the thinner bilayer

emitter that will consequently be absorbed in the substrate, and thus the bilayer emitter's utilizeable spectrum will be reduced to wavelengths less than $0.8\mu\text{m}$. However, the absorption coefficient of the recrystallized a-Si film may be slightly higher in this case since its as-grown a-Si film was only $\sim 700\text{\AA}$ thick, being $\sim 550\text{\AA}$ thinner than that of the thicker bilayer emitter examined previously, and thus its final grain structure may not be as perfect as that of the thicker film, in which case the upper wavelength limit of the bilayer emitter's utilizeable spectrum will be higher.

Nevertheless, in either case the drift influence of the built-in electric field on the minority carriers photogenerated in the thinner bilayer emitter is expected to have grown stronger, since the junction of the cell has been practically shifted closer to the top surface as a consequence of the decrease in the bilayer emitter thickness, and thus an enhanced drift travelling distance " σ " ($\sigma \propto E$) of these minority carriers can translate into a higher collection probability that could explain the observed higher responsivities obtained in the visible and blue regions of the spectrum with the implementation of the thinner bilayer emitter.

Knowing the absolute spectral responses of both the poly-Si/a-Si bilayer emitter cells and that of the "reference" phosphorus predeposited c-Si emitter cell in the entire utilizeable spectral range of the solar spectrum, it is now possible to accurately determine the total photocurrent losses of the poly-Si/a-Si bilayer emitter cells as well as the actual part of these photocurrent losses that are associated with the poly-Si/a-Si bilayer emitters themselves in each individual case.

Using the measured absolute spectral response $ASR(\lambda)$ of the previously examined solar cells and the spectral power density distribution of the standard AM1.5 terrestrial spectrum $P_{AM1.5}(\lambda)$ [Curt77], the AM1.5 short circuit current density J_{sc} , as well as the corresponding partial photocurrent densities associated with the utilization of each separate spectral region (ie ultra-violet, blue, visible and infra-red) of the AM1.5 spectrum, were all calculated by numerical analysis using the following equation,

$$J_{sc} = \sum_{\lambda=\lambda_1}^{\lambda=\lambda_2} ASR(\lambda) \cdot P_{AM1.5}(\lambda) \cdot \Delta\lambda \quad (4.3.1)$$

where λ_1 and λ_2 are the lower and upper wavelength limits respectively applied for either the entire utilizeable AM1.5 solar terrestrial spectrum ($0.29\mu\text{m}$ - $1.12\mu\text{m}$), or for the individual spectral regions considered in each case respectively.

Once the short circuit current densities of the poly-Si/a-Si bilayer emitter cells and that of the c-Si emitter cell were calculated, the total photocurrent losses of the poly-Si/a-Si bilayer emitter cells were estimated by simply subtracting the obtained values of the short circuit current densities of the poly-Si/a-Si bilayer emitter cells from the corresponding values obtained for the c-Si emitter cell. Similarly, the individual partial photocurrent losses of the poly-Si/a-Si bilayer emitter cells associated with each separate spectral region were calculated using the same technique. From these estimates the magnitude of the actual contribution of each individual spectral-related photocurrent loss to the total photocurrent losses is determined, while the dominant spectral-related photocurrent loss is identified in each case, thus giving a better understanding on how

the total photocurrent losses of these devices are affected with the utilization of a specific poly-Si/a-Si bilayer emitter thickness.

Finally, the photocurrent losses associated with the poly-Si/a-Si bilayer emitters themselves as well as those that may be associated with the individual substrates, as in the case of the $0.1\Omega\cdot\text{cm}$ FZ substrate, were calculated based on the obtained partial photocurrent losses associated with each spectral region. These calculations took also into account related information obtained from the spectral response characteristics of each individual solar cell in determining the upper wavelength limit of the utilized spectrum in each region of the cell structure.

Part of the results from the above mentioned calculations are tabulated in Table 4.3.1 showing the partial photocurrent contribution from each spectral region of the AM1.5 spectrum as well as the total AM1.5 short circuit density of the "reference" c-Si emitter cell, the poly-Si/a-Si bilayer emitter cell with the $1,450\text{\AA}$ bilayer emitter (#1) whose absolute spectral response was shown in Figure 4.3.1, the poly-Si/a-Si bilayer emitter cell with the thinner ($\sim 925\text{\AA}$) bilayer emitter (#10) whose absolute spectral response was shown in Figure 4.3.3, as well as that of the poly-Si/a-Si bilayer emitter cell with the $0.1\Omega\cdot\text{cm}$ FZ substrate (#9) whose absolute spectral response was shown in Figure 4.3.1 and which is included in this table mainly because of its substrate photocurrent losses that are associated with the infra-red region of the spectrum. The corresponding photocurrent losses of the poly-Si/a-Si bilayer emitter cells associated with each individual spectral region as well as their total short circuit current losses are also shown in mA/cm^2 in parentheses under the columns labeled as $\Delta J_{(\dots)}$ and besides the columns that show the actual photocurrents obtained in each spectral region so that to allow

Table 4.3.1: Estimated AM1.5 short circuit current densities as calculated from absolute spectral response measurements. Photocurrent contribution from U.V, Blue, Visible, and I.R spectral regions are shown separately indicating also the photocurrent losses of the uncoated poly-Si/a-Si emitter cells in each corresponding region.

		Estimated AM1.5 Photocurrent Densities from Absolute Spectral Response Measurements									
Solar	Emitter	(0.29-0.4 μ m)	(0.4-0.5 μ m)	(0.5-0.8 μ m)	(0.8-1.12 μ m)	(1.12-1.2 μ m)	(1.2-1.4 μ m)	(1.4-1.6 μ m)	(1.6-1.8 μ m)	(1.8-2.0 μ m)	(2.0-2.2 μ m)
Cell #	Thickness	J_{uv}	ΔJ_{uv}	J_{blue}	ΔJ_{blue}	$J_{visible}$	$\Delta J_{visible}$	J_{ir}	ΔJ_{ir}	J_{sc}	ΔJ_{sc}
/ (Substrate)	(Å)	(mA/cm ²)	(Loss)	(mA/cm ²)	(Loss)	(mA/cm ²)	(Loss)	(mA/cm ²)	(Loss)	(mA/cm ²)	(Loss)
c-Si / (1.8 Ω cm)	1,500	0.233	(---)	2.20	(---)	11.527	(---)	6.222†	(---)	20.182	(---)
#1 / (1.8 Ω cm)	1,450	0.013	(0.220)	0.938	(1.262)	9.965	(1.562)	6.18††	(0.042)*	17.096	(3.086)
#10 / (1.8 Ω cm)	925	0.019	(0.214)	1.293	(0.907)	10.993	(0.534)	6.409	(-0.187)*	18.714	(1.468)
#9 / (0.1 Ω cm FZ)	1,400	0.013	(0.220)	0.937	(1.263)	9.960	(1.567)	5.486	(0.736)	16.396	(3.786)

* The minus sign indicates that the infra-red photocurrent contribution from the substrate of this device shows a gain with respect to the corresponding photocurrent contribution from the predeposited c-Si emitter device.

†c-Si predep. : (0.8-0.9 μ m) $J_{ir,1}$ = 3.45 (mA/cm²)
(0.9-1.12 μ m) $J_{ir,2}$ = 2.772 (mA/cm²)

†† #1 (poly-Si/a-Si): (0.8-0.9 μ m) $J_{ir,1}$ = 3.38 (mA/cm²)
(0.9-1.12 μ m) $J_{ir,2}$ = 2.80 (mA/cm²)

** #1 poly-Si/a-Si emitter's cell substrate loss: (0.8-0.9 μ m) $\Delta J_{ir,1}$ = 0.07 (mA/cm²)
substrate gain: (0.9-1.12 μ m) $\Delta J_{ir,2}$ = -0.028 (mA/cm²)

easy visualization of the magnitude of the photocurrent loss in each spectral region. For the c-Si emitter cell the corresponding parentheses are left blank to indicate that this cell has been used as a "reference cell". In this table the spectral range shown corresponding to the labeled "visible" region has been purposely extended to include the 0.75-0.80 μm part of the infra-red region for practical reasons, since this spectral range is only at the starting edge of the infra-red region where all three poly-Si/a-Si bilayer emitter cells show only a marginal photocurrent difference with the c-Si emitter cell, as is deduced from the previously shown spectral response curves, that may as well be attributed to the $\pm 3\%$ allowable measurement error margins quoted by NRC's callibrations in that spectral range.

For all the solar cells included in Table 4.3.1, the largest contribution to short circuit current comes from the visible spectral range, which in these cells accounts for as much as 57-60% of the corresponding short circuit current. This results from the high average responsivities of these cells in that spectral range in conjunction with the very high incoming photon flux associated with the visible spectral region (ie 0.50 μm -0.75 μm) of the AM1.5 spectrum that is shown in Figure 4.3.4. On the other hand however, because the incoming photon flux from the visible spectral range is much higher than that from the shorter wavelength spectral regions, although the average responsivities of the poly-Si/a-Si bilayer emitter cells have been found to be very high, being 86.5% - 95% of the average responsivity obtained with the c-Si emitter cell in the same spectral range depending on the thickness of the poly-Si/a-Si bilayer emitter, their corresponding photocurrent losses that are associated with the visible spectral range are rather quite substantial when they are compared to the photocurrent losses associated with the shorter wavelength spectral regions where the

Figure 4.3.4: Photon flux in the incident utilizeable sunlight spectrum corresponding to the AM1.5 standard terrestrial irradiance spectral distribution as calculated based on the data taken from NASA [Curt77].

corresponding average responsivities of these cells have been found to be much lower than that of the c-Si emitter cell. Particularly, for the poly-Si/a-Si bilayer emitter cells with the thicker poly-Si/a-Si bilayer emitters (ie #1; 1,450Å, #9; 1,400Å), the photocurrent losses associated with the visible spectral range are the dominant photocurrent losses. In the case of the poly-Si/a-Si bilayer emitter cell with the 1,450Å thick poly-Si/a-Si bilayer emitter (#1) the estimated $\sim 1.56 \text{ mA/cm}^2$ photocurrent loss associated with the visible spectral region accounts for as much as $\sim 50.6\%$ of the total photocurrent losses of this cell. For the same cell, although its average responsivity in the blue spectral region has been estimated to be only 42.5% of that corresponding to the c-Si emitter cell, the photocurrent loss of this cell associated with the blue spectral range has been found to be lower than that associated with the visible spectral region, being estimated at $\sim 1.26 \text{ mA/cm}^2$ and accounting for $\sim 41\%$ of the total photocurrent losses of this cell. On the other hand, although the average responsivity of this cell (#1) in the ultra-violet region is very low ($\sim 5.6\%$ of that corresponding to the c-Si emitter cell), its estimated 0.22 mA/cm^2 photocurrent loss associated with that spectral region is rather insignificant, accounting for only $\sim 7\%$ of the total photocurrent losses of this cell.

Even though for the cell with the 1,450Å poly-Si/a-Si emitter thickness (#1) there is evidence that much of the visible region is absorbed in the emitter, and thus when considering a theoretical complete photocurrent loss of the photogenerated minority carriers in the poly-Si/a-Si bilayer emitter it would rather result in much higher photocurrent losses than those initially estimated in Chapter 3.5, that could be as high as $\sim 70\%$ of the maximum obtainable short circuit current in the case of no recombination effects, the actual losses have only reduced by $\sim 15\%$ the amount of the otherwise maximum obtainable short

circuit current as is deduced from the $\sim 3.1 \text{ mA/cm}^2$ photocurrent loss calculated for this cell at AM1.5 irradiance conditions. Furthermore, in this case (#1) the AM1.5 photocurrent contribution of the poly-Si/a-Si bilayer emitter itself to the total short circuit current of this cell is as high as $\sim 10.9 \text{ mA/cm}^2$, accounting for $\sim 64\%$ of the total obtainable short circuit current of this cell (#1), and this indicating that even a $\sim 1,450 \text{ \AA}$ thick poly-Si/a-Si bilayer emitter, as in this case, can actually contribute a very substantial amount of photocurrent.

On the other hand, in the case of the cell with the thinner poly-Si/a-Si bilayer emitter (#10), although there is evidence that most, if not all, of the visible region of the incident irradiance is absorbed in the $\sim 925 \text{ \AA}$ thin poly-Si/a-Si bilayer emitter, its total photocurrent losses were found to be only $\sim 1.47 \text{ mA/cm}^2$, as seen in Table 4.3.1, reducing by only $\sim 7\%$ the amount of the otherwise maximum obtainable short circuit current in the case of no recombination effects, being $\sim 53\%$ lower than that of the poly-Si/a-Si bilayer emitter cell with the $\sim 1,450 \text{ \AA}$ thick poly-Si/a-Si bilayer emitter. As seen in Table 4.3.1, this drastic decrease in the total photocurrent losses of this cell (#10), as compared to the cell with the $\sim 1,450 \text{ \AA}$ poly-Si/a-Si bilayer emitter, is mostly attributed to the substantial decrease in photocurrent losses associated with the visible spectral region in this case, where its $\sim 0.53 \text{ mA/cm}^2$ photocurrent loss in this spectral range is estimated to be $\sim 66\%$ lower than the corresponding photocurrent loss in the same spectral range obtained with the thicker poly-Si/a-Si bilayer emitter (#1), while accounting for only $\sim 22\%$ of the total photocurrent losses of this cell (#10).

In this poly-Si/a-Si bilayer emitter cell (#10), the dominant photocurrent losses are those associated with the blue region of the spectrum. Although these account for $\sim 55\%$ of the total photocurrent losses in this cell, the calculated

~0.91mA/cm² photocurrent loss which is associated with this spectral range, as seen in Table 4.3.1, is ~28% lower than that obtained with the ~1,450Å poly-Si/a-Si bilayer emitter (#1) in the same spectral range. This photocurrent loss reduction in this spectral range obtained with the utilization of the thinner (~925Å) poly-Si/a-Si bilayer emitter is the next major contributor towards the lower total photocurrent losses in this case. On the other hand, although substantial reductions in the photocurrent losses associated with the visible and blue spectral regions have been obtained with the utilization of a thinner poly-Si/a-Si bilayer emitter (#10), the reduction of the photocurrent losses associated with the ultra-violet region have been found to be only marginal in this case, being ~3% lower than that corresponding to the ~1,450Å poly-Si/a-Si bilayer emitter, and accounting for ~8.2% of the total photocurrent losses of this cell (#10), but nevertheless being insignificant as they were calculated to be only ~0.214mA/cm². In this particular cell (#10), the substrate photocurrent contribution that is associated with the infra-red spectral region has been found to be higher than all the other cells, where the negative calculated 0.187mA/cm² value, that is shown in Table 4.3.1 under the photocurrent losses, actually indicates the amount of excess photocurrent contribution (gain) of this substrate as compared to that obtained with the substrate of the c-Si emitter cell, which have actually boosted by ~11% the reduction of the total photocurrent losses obtained for the poly-Si/a-Si bilayer emitter cell with the ~925Å poly-Si/a-Si bilayer emitter.

Finally, it is evident from the calculated values shown in Table 4.3.1 for this cell (#10), that with the utilization of an even thinner poly-Si/a-Si bilayer emitter the total photocurrent losses of poly-Si/a-Si bilayer emitter cells can be further reduced to very low values (<1mA/cm²) or they can even be eliminated

altogether, since as explained earlier even in the case the absorption coefficient of a very thin utilized poly-Si/a-Si bilayer emitter ($<500\text{\AA}$) becomes high enough to absorb most of the utilizeable solar spectrum, the junction of the cell will be shifted very close to the top surface and consequently the built-in electric field will be much stronger in the entire poly-Si/a-Si bilayer emitter, whose influence on the drift distance of the photogenerated minority carriers can be enhance to the point where almost all the photogenerated minority carriers in the poly-Si/a-Si bilayer emitter can be pulled through into the substrate before they have a chance to recombine or even be neutralized by inherent defects in the polycrystalline structure of the poly-Si/a-Si bilayer emitters. Nevertheless, such a thin poly-Si/a-Si bilayer emitter will be characterized by a very high sheet resistance ($>10\text{k}\Omega/\square$), as it was shown in Figure 3.2.2, and unless a highly conducting transparent oxide like ITO is utilized on top of the poly-Si/a-Si bilayer emitter, a degradation in the fill factor of the device will be inevitable. Another solution of course is to reoptimize the front contact grid structure in order to minimize the lateral current flow related resistance in the ultra-thin poly-Si/a-Si bilayer emitter film, but only at the expense of optical losses. However, actually in either case there will no longer be an advantage in using the recrystallized a-Si layer anymore since its original purpose was to reduce the otherwise high sheet resistance of the poly-Si emitter itself.

The last poly-Si/a-Si bilayer emitter cell (#9) with the $\sim 1,400\text{\AA}$ thick poly-Si/a-Si bilayer emitter that is included in Table 4.3.1 exhibits similar photocurrent losses in almost all the indicated spectral regions as those of the cell with the $\sim 1,450\text{\AA}$ poly-Si/a-Si bilayer emitter (#1), except in the infra-red spectral range where a $0.736\text{mA}/\text{cm}^2$ substrate photocurrent loss, attributed to the shorter diffusion lengths of the minority carriers photogenerated in the $0.1\Omega\cdot\text{cm}$ FZ

substrate and accounting for ~19.5% of the total photocurrent losses in this cell, has increased the total photocurrent losses of this cell by ~18.5% compared to those obtained with the latter cell (#1) to a value of ~3.8mA/cm². However, although the substrate photocurrent loss in this particular case may be crippling the short circuit current of this device, the utilization of such a high quality substrate can boost the open circuit voltage of a solar cell by ~60mV as will be shown in the following subsection. If a thinner (~150μm) substrate is used instead with an appropriate back surface design (ie back surface field and back surface reflector) to enhance the photocurrent, the collection probability of the infra-red light induced photogenerated minority carriers in the substrate would be increased. The utilization of such a substrate in conjunction with the utilization of an optimized ultra-thin poly-Si/a-Si bilayer emitter covered with a highly conducting transparent oxide have the potential of producing very high efficiency solar cells.

Finally, Table 4.3.2 shows separately the AM1.5 photocurrent losses associated with the poly-Si/a-Si bilayer emitters themselves in each individual case for the poly-Si/a-Si bilayer emitter cells that were analyzed in Table 4.3.1, while their corresponding AM1.5 substrate photocurrent losses (or gains) as well as their total AM1.5 photocurrent losses are shown in the same table in order to give a complete visualization on the magnitude of the regional photocurrent losses of these cells. Since there is evidence for all three poly-Si/a-Si bilayer emitter cells (judging from their corresponding measured absolute spectral responses) that, if not all, most of the visible region is absorbed in the poly-Si/a-Si bilayer emitter in each particular case, the emitter photocurrent losses of these cells were thus calculated based on the separate AM1.5 spectral related photocurrent losses associated with the ultra-violet region, the blue region, and the entire visible

Table 4.3.2: Estimated AM1.5 and AM1 poly-Si/a-Si emitter photocurrent losses calculated based on NRC's absolute spectral response measurements of the poly-Si/a-Si emitter cells as compared to that of the c-Si emitter cell. Substrate photocurrent losses (or gains) calculated with the same procedure are also listed, while both natural sunlight and NRC's estimated total photocurrent losses are shown as well for comparison purposes.

SOLAR	CELL	#	Thickness (Å)	Poly-Si/a-Si emitter photocurrent loss		Substrate photocurrent loss		Total photocurrent loss		
				AM1.5 (Calculated)	AM1 (Estimated)	AM1.5 (Calculated)	AM1 (Estimated)	AM1.5 (Calculated)	AM1 (Estimated)	AM1 (Natural sunlight)
				$\Delta J_{\text{emitter}} = \Delta J_{\text{uv}} + \Delta J_{\text{blue}} + \Delta J_{\text{visible}}$ (mA/cm ²)		$\Delta J_{\text{substrate}} = \Delta J_{\text{ir}}$ (mA/cm ²)		ΔJ_{sc} (mA/cm ²)		
1	1	1	1,450	3.044	3.658	0.042	0.050	3.086	3.709	3.47
10	1	1	925	1.655	1.989	-0.187†	-0.224†	1.468	1.765	1.63
9 (0.1 FZ)*	1	1	1,400	3.05	3.666	0.736	0.885	3.786	4.550	4.25

* The (0.1 FZ) indicates that this solar cell has a high quality 0.1 Ω.cm Float-Zone substrate.

† The minus sign indicates gain with respect to the corresponding photocurrent contribution from the predep. c-Si emitter cell's substrate.

region inclusive such as to rather give a worst case estimate. Similarly, the corresponding shown AM1.5 substrate losses (or gains) of these cells were calculated based on the AM1.5 spectral related photocurrent losses associated with the infra-red region of the AM1.5 spectrum. Based on these calculations, the corresponding shown AM1 regional and total photocurrent losses were estimated by multiplying the shown AM1.5 photocurrent losses by a factor of $100/83.18$ (~ 1.2022), where $100 \text{ (mW/cm}^2\text{)}$ is the total maximum power density that is received at the earth's surface under AM1 irradiance conditions and $83.18 \text{ (mW/cm}^2\text{)}$ is the corresponding maximum total AM1.5 standard terrestrial irradiance power density. The AM1 total photocurrent losses of these cells, that were estimated accordingly from the natural sunlight short circuit measurements discussed in the previous subsection, are also included in this table for comparison purposes.

As seen in Table 4.3.2, the poly-Si/a-Si bilayer emitter photocurrent losses of the cell with the $\sim 1,450\text{\AA}$ thick poly-Si/a-Si bilayer emitter (#1) are slightly lower from the calculated total photocurrent losses of this cell by $\sim 1.3\%$, with the AM1.5 poly-Si/a-Si bilayer emitter photocurrent losses calculated to be $\sim 3.04\text{mA/cm}^2$ and the corresponding AM1 emitter photocurrent losses estimated to be at $\sim 3.66\text{mA/cm}^2$, while the very small substrate photocurrent losses of this cell, being $\sim 0.04\text{mA/cm}^2$ as calculated at AM1.5 conditions and $\sim 0.05\text{mA/cm}^2$ as estimated for AM1 conditions, make up for the rest of the total calculated photocurrent losses in this case. On the other hand, the actual emitter photocurrent losses of the cell with the $\sim 925\text{\AA}$ thick poly-Si/a-Si bilayer emitter (#10) are found to be higher than the total calculated photocurrent losses of this cell by $\sim 11.3\%$, with its AM1.5 poly-Si/a-Si bilayer emitter photocurrent loss being calculated at $\sim 1.65\text{mA/cm}^2$ and its corresponding AM1 emitter photocurrent loss estimated to be

at $\sim 1.99 \text{ mA/cm}^2$. The reason the total photocurrent losses in this case are lower than the poly-Si/a-Si bilayer emitter's photocurrent losses is due to the fact that the substrate photocurrent contribution of this cell was found to be higher than the corresponding photocurrent contribution of the c-Si emitter cell in the same spectral range (infra-red region) by $\sim 0.19 \text{ mA/cm}^2$ at AM1.5 irradiance conditions and by $\sim 0.22 \text{ mA/cm}^2$ respectively at AM1 conditions, indicating rather a gain in this spectral range instead of a loss as symbolized with the corresponding shown minus sign of these values in Table 4.3.2, and thus the total photocurrent losses of this cell were found to be lower by these amounts since they are calculated based on the total short circuit current difference between this cell and that corresponding to the c-Si emitter cell.

For the poly-Si/a-Si bilayer emitter cell with the $0.1 \Omega \cdot \text{cm}$ FZ substrate (#9), the poly-Si/a-Si bilayer emitter photocurrent losses of this cell are similar to those found for the cell with the $\sim 1,450 \text{ \AA}$ poly-Si/a-Si bilayer emitter, as they were calculated to be $\sim 3.05 \text{ mA/cm}^2$ at AM1.5 irradiance conditions and $\sim 3.66 \text{ mA/cm}^2$ as estimated correspondingly at AM1 conditions. Nevertheless, in this case the substrate photocurrent losses are calculated to be $\sim 0.736 \text{ mA/cm}^2$ at AM1.5 conditions and $\sim 0.885 \text{ mA/cm}^2$ at AM1 conditions, which as was explained earlier are mainly attributed to the shorter diffusion lengths of the minority carriers photogenerated in this substrate which are consequently characterized by a lower collection probability.

In Table 4.3.2, it can also be seen that there is a very good correlation between the estimated AM1 total photocurrent losses that were calculated based on the measured absolute spectral responses of these cells and the estimated AM1 total photocurrent losses deduced from the natural sunlight measurements, thus

indicating that the results from the natural sunlight measurements that were shown in the previous subsection were indeed quite accurate.

Summarizing, these results indicate that the actual photocurrent losses associated with the poly-Si/a-Si bilayer emitters themselves are not severe considering that most of the utilizeable spectrum is absorbed in the emitter layer of these devices. The poly-Si/a-Si bilayer emitter photocurrent losses have been found to decrease with the utilization of thinner emitters, indicating that there is room for further emitter photocurrent loss reductions to the point where these losses can have a negligible effect on the overall photovoltaic performance of these devices.

4.4 ILLUMINATED CELL CHARACTERISTICS UNDER AM1.5(100mW/cm²) SIMULATED SUNLIGHT CONDITIONS

AM1.5 simulated sunlight was used in this work mainly to obtain the illuminated J-V characteristics of the devices under a controlled environment, from which measurements the fill-factor (FF) and open circuit voltage (V_{oc}) could be accurately determined. Although the short circuit current density (J_{sc}) and the maximum output power density (P_{max}) of the solar cells examined are also presented here as they were extracted from the corresponding obtained illuminated J-V characteristics of these cells under the AM1.5 simulated sunlight conditions, the degree of accuracy of these particular parameters is highly dependent on the spectral irradiance distribution accuracy of the AM1.5 solar simulator used. For reasons cited earlier in Subsection 4.2 the extracted values of these parameters may not necessarily reflect the true J_{sc} and P_{max} values of the poly-Si/a-Si bilayer emitter cells, especially because the actual spectral irradiance distribution of the particular AM1.5 simulator used was unknown at the time of the measurements*. Nevertheless, although a conscientious effort is made in this work not to misrepresent the AM1.5 J_{sc} and P_{max} results obtained with the aid of this AM1.5 solar simulator as the actual AM1.5 illuminated characteristic parameters of the poly-Si/a-Si bilayer emitter cells fabricated in this work, it has to be noted here that experimental results taken under similar simulated sunlight conditions are commonly used in the photovoltaic community for comparison purposes. The AM1.5 J_{sc} and P_{max} values presented here are

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* The spectral irradiance distribution of simulator lamps have been found to vary after extensive use of the lamp [SADE80], and thus a simulator lamp at its late lifetime may exhibit a different spectral irradiance distribution from its original one at its early lifetime, that in the first place would only approximate that of a standard sunlight irradiance distribution.

believed to comply with the internationally recognized $\pm 10\%$ allowed uncertainty error limits (due to the $\pm 10\%$ maximum allowed deviation of the simulated sunlight's spectral irradiance distribution from that of natural sunlight at any wavelength of the spectrum [FaBu83]) of such simulated photovoltaic results.

The experimental test set-up that was used to obtain the illuminated J-V characteristics of the examined solar cells under the AM1.5(100mW/cm²) simulated sunlight conditions is shown in Figure 4.4.1. A "Kratos" AM1.5 xenon arc solar simulator, that was made available by TPK Solar Systems Inc., was used to obtain the AM1.5(100mW/cm²) simulated sunlight. The intensity of the AM1.5 simulated sunlight's irradiance was adjusted by a computer control unit so as to give $\sim 100\text{mW/cm}^2$ of total incident irradiance on the surface of the solar cells, as it was indirectly deduced from measurement of the short circuit photocurrent of an ASEC calibrated control cell. The solar cells were positioned on a portable vacuum chuck below the solar simulator so as to receive the simulated sunlight on a horizontal surface at normal incidence. The operating temperature of the solar cell is monitored by a temperature sensor imbedded on the chuck, and is adjusted by a temperature control unit so as to maintain an operating cell temperature in the proximity of 28°C. The illuminated J-V characteristics of the solar cells were obtained with the aid of an HP4145A semiconductor parameter analyzer, by applying and varying a forward bias voltage on the cells from zero to one volts. However, because the current compliance of the HP4145A semiconductor parameter analyzer unit was constrained to $\sim 105\text{mA}$, being lower than the short circuit photocurrent capability of the 2x2cm control solar cell used and of that of the 2x2cm poly-Si/a-Si emitter cells that were covered with an antireflection coating, the illuminated J-V characteristics reported here were obtained from the

Figure 4.4.1: Experimental test set-up used to obtain the simulated AM1.5 illuminated J-V characteristics of the solar cells.

smaller (0.5x0.5cm) test cell devices instead, while the AM1(100mW/cm²) rated short circuit current and open circuit voltage of the 2x2cm control solar cell were monitored by a high accuracy Keithley multimeter just prior to and after each measurement in order to check and adjust, if necessary, the intensity of the incident irradiance and/or the operating temperature of the solar cell.

Nevertheless, it has to be noted here that the vacuum suction of the portable chuck was not operatable at the time of the measurements, and thus even though the temperature control unit was set so as to maintain 28°C at the chuck's top surface, the measured open circuit voltage of the ASEC control cell was found to be ~5mV below its 28°C rated value throughout the entire experiment, implying that the test cells were rather operating at ~2°C higher temperature* than 28°C as a consequence of poor thermal contact to the chuck.

Table 4.4.1 shows the AM1.5(100mW/cm²) illuminated characteristic parameters (ie J_{sc} , V_{oc} , FF, P_{max}) of the solar cells examined, as extracted from the J-V characteristic curves obtained under the simulated sunlight conditions. Most of the parameter values shown refer to uncoated solar cells unless otherwise noted in this table. Although the efficiencies of these devices are not shown due to lack of space, the total area efficiency (ie taking into account the top metal grid's contact covering area as well) is percentagewise equal to the corresponding maximum output power density (P_{max}) magnitude, since the incident AM1.5 irradiance used was equal to 100mW/cm². As seen in this table, poly-Si/a-Si bilayer emitter solar cells with various substrates of different resistivities were tested, while related device and processing parameters, like the bimetal composition of the top contact grid and the corresponding post-metal hydrogen

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* The dV_{oc}/dT decrease in V_{oc} with increasing temperature is ~2.3mV/°C as given by Green [Gree82 (pg.92)].

Table 4.4.1: Illuminated output parameters of uncoated 0.5x0.5cm poly-Si/a-Si emitter solar cells measured at TPK Solar Systems Inc. using a AM1.5 (100mW/cm²) xenon arc solar simulator. An ASEC 2x2cm control solar cell rated for I_{sc} :142mA; V_{oc} =0.600 Volts & 28°C at AM1 (100mW/cm²) illuminated conditions, was used for calibration purposes. Substrates with various resistivities are included, while related device and processing parameters are shown for comparison purposes.

Solar Cell #	Substrate	Front Metal	H ₂ Annealing Temp. (°C)	Time (min)	Emitter Thickness (Å)	Emitter Sheet Resistance (Ω/□)	I_{sc} (mA/cm ²)	V_{oc} (Volts)	FF	P_{max} (mW/cm ²)
Control Cell	---	---	---	---	---	---	35.5	0.595	---	---
c-Si predep	1.8-2.6	Al	---	---	1,500	400	23.4	0.514	0.686	8.26
1	1.8-2.6	ITiW/Al	450	20	1,440	270	23.1	0.584	0.80	10.8
2	1.8-2.6	ITiW/Al	450	20	1,400	395	23.2	0.583	0.792	10.7
3	1.8-2.6	ITiW/Al	350	15	1,260	450	24.0	0.584	0.770	10.8
4	1.8-2.6	ITiW/Al	400	15	1,080	900	22.0	0.583	0.767	9.84
5A**	1.8-2.6	ITiW/Al	450	20	1,550	330	30.0	0.588	0.795	14.0
5B**	1.8-2.6	ITiW/Al	450	20	1,100	900	29.6	0.590	0.772	13.48
6	3.2-4.3	ITiW/Al	450	20	1,350	540	19.3	0.558	0.780	8.40
7	8.0-10.0	ITiW/Al	400	15	1,440	465	22.5	0.540	0.760	9.24
8	0.5 (FZ)	ITiW/Al	450	20	1,360	450	19.6	0.610	0.795	9.50
9	0.1 (FZ)	ITiW/Al	450	20	1,400	360	19.2	0.648	0.790	9.83

* ASEC control cell with double antireflection coating

** These cells are coated with a single SiO_x antireflection coating:

SiO_x thickness:750Å ; SiO_x refractive index:1.77 (as deduced from ellipsometry measurements)

annealing treatments, as well as the measured emitter thicknesses of these cells and their corresponding measured emitter sheet resistances, are also shown in the table for each individual cell, since these parameters affect most of the illuminated output characteristics of these devices (ie FF, V_{oc} , P_{max}).

The emitter sheet resistances of most of the poly-Si/a-Si bilayer emitter cells, and especially of those with thinner emitter thicknesses, were found to be higher than those that were shown in Figure 3.2.2 for corresponding poly-Si/a-Si bilayer emitter film thicknesses, indicating that the post-hydrogen annealing treatments were not fully effective in removing all the damages introduced during the deposition of the top metal contacts. This resulted in slightly lower fill factors than expected. Nevertheless, all the fill factors of these devices were found to be higher than 0.76, while most of these devices exhibited fill factors higher than 0.78 and some even as high as ~0.80, showing a dramatic improvement from the ~0.60 fill factors of the original poly-Si monolayer emitter cells reported by Tarr [Tarr85] in earlier work. The 0.76-0.77 fill factors of the poly-Si/a-Si bilayer emitter cells with the TiW/Au front metal contact are slightly lower than those obtained with the TiW/Al front contacts (ie 0.78-0.80), mainly due to artificially higher voltage drops developed along most of the grid lines in the former case as a result of current overcrowding effects that were created due to the several unavoidable discontinuities formed in the grid lines during the mask aligning process of the original grid design (Figure 4.2.9) that was implemented in these cells, as explained earlier in more detail in Chapter 4.2. However, besides these isolated effects in these cells, it can be seen in that for those poly-Si/a-Si emitter cells for which the new "mesh" grid design (shown in Figure 4.2.10) was implemented (ie the cells with the TiW/Al bimetal configuration), the observed variation in the fill factor is mainly attributable to variations in the emitter sheet

resistance. It can be clearly seen that as the emitter sheet resistance of the poly-Si/a-Si bilayer emitter cells increases with thinner poly-Si/a-Si emitter thicknesses, the fill factor decreases slightly as a consequence of higher lateral current flow resistances. On the other hand, the lower value of the c-Si emitter cell's fill factor is believed to be attributable to space-charge recombination effects in the depletion region of this device, the occurrence of which is supported by the relatively low open-circuit voltage of this cell (~ 0.51 Volts), as compared to the open circuit voltages obtained with the poly-Si/a-Si bilayer emitter cells that have a similar substrate ($1.8\text{-}2.6\ \Omega\cdot\text{cm}$). The lower obtained open circuit voltage can not be entirely attributed to the higher back injection current that is associated with such a c-Si emitter cell. To substantiate the above reasoning, the dark $\log J$ - V characteristic curve of the ($0.5\times 0.5\text{cm}$) examined c-Si emitter cell is shown in Figure 4.4.2, where the "excess" current density component of the dark saturation current ($J_{0,r}$) that is associated with such recombination effects is found to be $\sim 2\times 10^{-8}\ \text{A/cm}^2$, as deduced from the shown extrapolation of the curve's slope taken at low forward bias voltages, being two orders of magnitude higher than the injection current component ($J_{0,ei}+J_{0,bi}$) of the dark saturation current, that was found to be $\sim 2\times 10^{-10}\ \text{A/cm}^2$ as deduced from the shown extrapolation of the curve's q/kT slope taken at a point corresponding to ~ 0.51 Volts.

The high fill factors of the poly-Si/a-Si bilayer emitter cells indicate that the series resistance of these devices is very small. To verify that the series resistance of the poly-Si/a-Si bilayer emitter cells is indeed negligible, a common experimental technique introduced by Handy [Hand67], incorporating a family of several illuminated J - V characteristic curves that are obtained under several different light intensities from each individual cell, was used to find the actual

Figure 4.4.2: Dark logJ-V characteristics of the 0.5x0.5cm c-Si emitter cell. A recombination "excess" current density ($J_{0,r}$) value of $\sim 2 \times 10^{-8} \text{ A/cm}^2$ is obtained from the shown extrapolation of the curve's slope at low forward bias voltages, while an injection current density ($J_{0,ei} + J_{0,bi}$) value of $\sim 2 \times 10^{-10} \text{ A/cm}^2$ is obtained from the shown extrapolation of the curve's q/kT slope taken at high forward bias voltages.

series resistance of these devices. Figure 4.4.3 shows such a family of illuminated J-V curves for a typical poly-Si/a-Si bilayer emitter cell with an emitter thickness in the proximity of $1,400\text{\AA}$. It can be readily demonstrated that the absolute value of the slope of the line joining the marked points on these curves, that correspond to a J value of $J=J_{sc}-\Delta J$, will be equal to the reciprocal value of the series resistance R_s [Handy] of the solar cell, for any reasonable chosen value of ΔJ that is fixed for all J-V curves ($\Delta J=5\text{mA/cm}^2$ in this case). The series resistance value obtained by this method was $\sim 0.46\Omega\cdot\text{cm}^2$, thus confirming that the series resistance of the poly-Si/a-Si bilayer emitter solar cells fabricated in this work is indeed very small, a result that is highly desirable for the attainment of a highly efficient cell operation.

The open circuit voltage of all the poly-Si/a-Si bilayer emitter solar cells was found to be much higher than that of the "reference" c-Si emitter cell. In the case of the poly-Si/a-Si bilayer emitter cells that have a similar substrate ($1.8\text{-}2.6\Omega\cdot\text{cm}$) as that of the c-Si emitter cell, open circuit voltages were found to be $\sim 584\text{mV}$ (at 30°C), $\sim 70\text{mV}$ higher than that of the c-Si emitter cell. The open circuit voltage superiority of phosphorus in-situ doped poly-Si emitter cells, is mainly achieved as a result of the very low injection component of the dark saturation current (being $\sim 10^{-13}\text{ A/cm}^2$) associated with the device structure of such poly-Si emitter devices.

It is quite evident from the open circuit voltage values listed in Table 4.4.1 that the resistivity and consequently the quality of the various substrates used in this work have a profound effect on the open circuit voltage of the poly-Si/a-Si bilayer emitter cell devices, which effects nonetheless can extend to other solar cell structures as well since they are solely associated with the bulk properties of the individual substrates used. From Table 4.4.1, it can be seen that the cells with

Figure 4.4.3: Family of illuminated J-V curves of a typical poly-Si/a-Si bilayer emitter cell obtained at different light intensities that were used for the determination of the series resistance of the solar cells. The series resistance (R_s) of the solar cell is equal to the reciprocal absolute value of the slope of the line joining the marked points of these curves that correspond to a J value of $J = J_{sc} - \Delta J$, where ΔJ is 5 mA/cm^2 in this case.

the higher resistivity substrates (ie #6; 3.2-4.3 $\Omega\cdot\text{cm}$, #7; 8.0-10.0 $\Omega\cdot\text{cm}$) exhibit lower open circuit voltages, with cell #6, whose substrate is characterized by a 3.2-4.3 $\Omega\cdot\text{cm}$ resistivity, exhibiting an open circuit voltage of $\sim 0.56\text{Volts}$, being $\sim 22\text{mV}$ lower than that obtained with corresponding poly-Si/a-Si bilayer emitter cells with 1.8-2.6 $\Omega\cdot\text{cm}$ resistivity substrates, and with cell #7, that has a substrate characterized by a 8.0-10.0 $\Omega\cdot\text{cm}$ resistivity, exhibiting an even lower open circuit voltage of $\sim 0.54\text{Volts}$, being $\sim 44\text{mV}$ lower respectively than that obtained with corresponding poly-Si/a-Si bilayer emitter cells with 1.8-2.6 $\Omega\cdot\text{cm}$ resistivity substrates. These lower open circuit voltages are indicative of the higher recombination rates associated with higher resistivity substrates. High recombination rates in the substrate can result into a subsequent undesirable constraint of the open circuit voltage capability of solar cells to lower values, that can consequently restrain the attainment of very high efficiencies.

On the other hand, of particular interest are the open circuit voltage results obtained with the use of lower resistivity float-zone (FZ) substrates (ie #8; 0.5 $\Omega\cdot\text{cm}$ FZ, #9; 0.1 $\Omega\cdot\text{cm}$ FZ), that have been widely used in the mid 80's by other workers [GBGW82], [GBJK84], [GBWJ87] towards attaining both open circuit voltage and efficiency records. The poly-Si/a-Si bilayer emitter cell with the 0.5 $\Omega\cdot\text{cm}$ FZ substrate (#8) exhibited an open circuit voltage of 0.610Volts, while the cell with the 0.1 $\Omega\cdot\text{cm}$ FZ substrate (#9) exhibited the highest open circuit voltage among the devices examined, giving an open circuit voltage value of as high as $\sim 0.65\text{Volts}$. This is the highest open circuit voltage ever reported, to be obtained under one sun AM1.5 ($100\text{mW}/\text{cm}^2$) illuminating conditions, for an uncoated solar cell having a $\sim 300\mu\text{m}$ thick substrate and an overall simple cell structure. It has to be remarked here that the operating temperature of that cell was more likely $\sim 30^\circ\text{C}$ at the time of these measurements for the reasons cited earlier. Considering

that the open circuit voltage of a solar cell can be reduced by as much as $\sim 2.3 \text{ mV}/^\circ\text{C}$ for each additional increase in temperature by 1°C [Gree82], then the open circuit voltage obtained with the poly-Si/a-Si bilayer emitter cell having the $0.1\Omega\cdot\text{cm}$ resistivity FZ substrate (#9) can translate into ~ 0.653 Volts for a 28°C operating temperature, and into ~ 0.660 Volts respectively for a 25°C operating temperature*. The utilization of a back surface field, that was not implemented in the devices of this work, can further increase the open circuit voltage of the poly-Si/a-Si bilayer emitter solar cells by virtue of a further reduction in the dark saturation current due to corresponding reductions in back surface recombination effects, while even further open circuit voltage enhancements can be achieved with the utilization of thinner substrates ($50\text{-}150\mu\text{m}$ thick) by virtue of reduced Auger bulk recombination effects. Such thin substrates implemented in conjunction with cell light trapping design features have been originally introduced during the development of very high efficiency concentrator solar cells [GBWJ87], [VWSF87], [SKGS85].

Furthermore, considering that the open circuit voltage of a solar cell will further increase with the attainment of higher short circuit current densities [i.e. $V_{OC} \propto \ln(J_{SC}/J_0)$], that can be simply obtained with the utilization of a good antireflection coating in conjunction with a front texturized surface, and the implementation of a back surface field, poly-Si/a-Si bilayer emitter cells with high quality $0.1\Omega\cdot\text{cm}$ FZ substrates have the potential of achieving very high open circuit voltage records. In order to justify this statement, an experiment was carried out in which the illumination intensity of an incandescent lamp was

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* 25°C is actually the most recent revised cell operating temperature standard adapted by SERI (Solar Energy Research Institute) in September '85 for comparison of experimental photovoltaic results [GBWJ87].

adjusted such as to obtain a $\sim 32 \text{ mA/cm}^2$ short circuit current density on several poly-Si/a-Si bilayer emitter cells including one with a $0.1 \Omega \cdot \text{cm}$ FZ substrate. The magnitude of this selected short circuit current density is within the short circuit current density capability projections of these cells if just a good double antireflection coating is applied on the top surface of the poly-Si/a-Si bilayer emitter. Table 4.4.2 shows both the open circuit voltage and fill factors obtained from these cells under these illuminating conditions, with the cell operating temperature of these devices being adjusted to $\sim 28^\circ \text{C}$. As seen from this table, an open circuit voltage of ~ 0.67 Volts was measured for the poly-Si/a-Si bilayer emitter cell with the $0.1 \Omega \cdot \text{cm}$ FZ substrate, while an increased open circuit voltage is also observed for the rest of the solar cells examined. It can also be seen from this table that the fill factors of all the solar cells have increased to values in the 0.80-0.81 range, as a consequence of the higher open circuit voltages obtained and the corresponding simulated higher short circuit current density of the cells.

Although the short circuit current density of solar cells utilizing $0.1 \Omega \cdot \text{cm}$ FZ substrates is expected to be lower than that of cells with higher resistivity substrates (considering substrate thicknesses in the $\sim 300 \mu\text{m}$ range) due to the shorter intrinsic diffusion length associated with such low resistivity substrates, recent studies have shown that thinner substrates when implemented in conjunction with cell light trapping designs will not only eliminate such negative effects (ie shorter diffusion lengths than the thickness of the substrate), but in fact can give a further short circuit current enhancement [GrCa87]. Thus, it is believed that an optimized poly-Si/a-Si bilayer emitter cell structure utilizing a very thin poly-Si/a-Si bilayer emitter covered by a highly conducting transparent oxide like ITO, and having a thin $0.1 \Omega \cdot \text{cm}$ FZ substrate with a proper

Table 4.4.2: Measured open circuit voltage (V_{oc}) and fill factor (FF) for cells illuminated to give a photocurrent density of 32mA/cm^2 at a controlled temperature of 28°C .

Solar Cell #	Substrate Resistivity ($\Omega\cdot\text{cm}$)	Emitter Thickness ($\text{\AA}$)	Emitter Sheet Resistance ($\Omega/\square$)	V_{oc} (Volts)	FF
c-Si predep	1.8-2.6	1,500	400	0.526	0.690
1	1.8-2.6	1,440	270	0.595	0.808
2	1.8-2.6	1,400	395	0.597	0.806
8	0.5 (FZ)	1,360	450	0.625	0.800
9	0.1 (FZ)	1,400	360	0.669	0.798

implemented light trapping design (ie texturized front and back surfaces), and a back surface field, not only has the potential of achieving very high open circuit voltage records, but has also the potential of attaining very high efficiencies in the 20% range under one-sun illuminated conditions. This trend can be substantiated by the fact that the poly-Si/a-Si bilayer emitter cell #5A shown in Table 4.4.1, whose overall structural design is a very simple basic one, having a $\sim 300\mu\text{m}$ thick substrate of $1.8\text{-}2.6\Omega\cdot\text{cm}$ resistivity instead of a high quality FZ low resistivity substrate, and a primitive single layer SiO_x anti-reflection coating, is characterized by a total area efficiency of as high as 14.0%. The corresponding illuminated J-V characteristic curve of this device is shown in Figure 4.4.4 as was obtained under the AM1.5 ($100\text{mW}/\text{cm}^2$) simulated sunlight conditions, where its extracted photovoltaic parameters give a short circuit current density of $30.0\text{mA}/\text{cm}^2$, an open circuit voltage of $\sim 0.59\text{Volts}$ (at $\sim 30^\circ\text{C}$), a fill factor of ~ 0.80 and a maximum output power density of $14.0\text{mW}/\text{cm}^2$.

The illuminated J-V characteristic curve of a corresponding uncoated poly-Si/a-Si bilayer emitter cell (#1), having a $1.8\text{-}2.6\Omega\cdot\text{cm}$ substrate and a poly-Si/a-Si bilayer emitter thickness in the proximity of $1,450\text{\AA}$, is shown in Figure 4.4.5 as was obtained under the same AM1.5 ($100\text{mW}/\text{cm}^2$) simulated sunlight conditions. This solar cell exhibit a short circuit current density of $\sim 23.0\text{mA}/\text{cm}^2$, an open circuit voltage of $\sim 0.595\text{Volts}$, a fill factor of ~ 0.80 , and a maximum power density of $\sim 11.0\text{mW}/\text{cm}^2$. Figure 4.4.6 shows the AM1.5 (simulated) illuminated J-V characteristics of another uncoated poly-Si/a-Si bilayer emitter cell (#9) having a similar poly-Si/a-Si bilayer emitter thickness as that of the cell (#1) shown in the previous figure, but having a high quality $0.1\Omega\cdot\text{cm}$ FZ substrate. As seen in this figure, this cell exhibits a lower short circuit current density of $\sim 19.0\text{mA}/\text{cm}^2$, but a higher open circuit voltage of $\sim 0.65\text{Volts}$ (at $\sim 30^\circ\text{C}$), a fill factor

Figure 4.4.4: Illuminated J-V characteristic curve of a poly-Si/a-Si bilayer emitter cell (#5A) with a primitive single layer SiO_x antireflection coating, as obtained under AM1.5(100mW/cm²) simulated sunlight conditions.

Figure 4.4.5: Illuminated J-V characteristic curve of an uncoated poly-Si/a-Si bilayer emitter cell (#1) having a $\sim 1,450\text{\AA}$ poly-Si/a-Si emitter thickness and a substrate characterized by a $1.8\text{-}2.6\Omega\cdot\text{cm}$ resistivity, as obtained under AM1.5(100mW/cm^2) simulated sunlight conditions.

Figure 4.4.6: Illuminated J-V characteristic curve of an uncoated poly-Si/a-Si bilayer emitter cell (#9) having a $\sim 1,400\text{\AA}$ poly-Si/a-Si emitter thickness and a high quality float-zone substrate characterized by a low resistivity of $0.1\Omega\cdot\text{cm}$, as obtained under AM1.5(100mW/cm^2) simulated sunlight conditions.

of ~ 0.79 , and a maximum output power density of $\sim 9.8 \text{ mW/cm}^2$. The maximum output power densities of these two poly-Si/a-Si bilayer emitter solar cells (ie #1, #9) are quite high considering that these values were obtained from uncoated cells with non-optimized structures. For comparison purposes, Figure 4.4.7 shows both the AM1.5(100 mW/cm^2) illuminated J-V characteristic curves of the same two uncoated poly-Si/a-Si bilayer emitter cells as compared to that obtained with the c-Si emitter cell. For the cells with the similar substrates ($1.8\text{-}2.6 \Omega\cdot\text{cm}$), the poly-Si/a-Si bilayer emitter cell's open circuit voltage superiority over with the c-Si emitter cell is clearly evident in this figure, while the further open circuit voltage enhancement that can be attained with the utilization of a high quality $0.1 \Omega\cdot\text{cm}$ FZ substrate is clearly demonstrated as well. Although the short circuit current densities of both poly-Si/a-Si bilayer emitter cells shown in this figure are lower than that of the c-Si emitter cell, if proper optimized cell structure designs like the ones proposed earlier are implemented in these cells (ie a very thin poly-Si/a-Si emitter covered by ITO, thinner substrates in conjunction with light trapping design features, and a back surface field), then it is believed that poly-Si/a-Si bilayer emitter cells with such state-of-the-art structural design feature configurations can outperform in all aspects similar state-of-the-art c-Si emitter cells.

Finally, going back to Table 4.4.1, an attempt is made in the following paragraphs to analyze the short circuit current results obtained under the specific simulated AM1.5(100 mW/cm^2) illuminating conditions used in this work. The AM1.5 short circuit current densities of several poly-Si/a-Si bilayer emitter cells (#1, #2, #3, #7), shown in Table 4.4.1, are $\sim 10\%$ higher than expected (by $2.0\text{-}2.5 \text{ mA/cm}^2$) as compared to both the AM1(100 mW/cm^2) normalized values of the natural sunlight short circuit photocurrent density measurements of these cells,

Figure 4.4.7: Comparison of the AM1.5(100mW/cm²) illuminated J-V characteristic curves of an uncoated c-Si emitter cell with a 1.8-2.6 $\Omega\cdot\text{cm}$ resistivity substrate, an uncoated poly-Si/a-Si bilayer emitter cell (#1) with a similar 1.8-2.6 $\Omega\cdot\text{cm}$ resistivity substrate, and an uncoated poly-Si/a-Si bilayer emitter cell (#9) with a high quality 0.1 $\Omega\cdot\text{cm}$ float-zone substrate.

and the corresponding AM1(100mW/cm²) short circuit current density projections of such cells with similar poly-Si/a-Si bilayer emitter thicknesses, as deduced from the AM1.5(83.18 mW/cm²) calculated short circuit current results obtained from the absolute spectral response measurements. The short circuit current densities of these particular solar cells (ie #1, #2, #3, #7) were carefully re-measured under the same illuminated conditions (ie AM1.5; 100mW/cm²) giving almost identical results, and thus indicating that the increased short circuit current densities could not be accounted for due to the quoted $\pm 5\%$ variation in the illumination uniformity of the simulator used, or due to higher total irradiance intensity shifts that may have occurred during these measurements.

Although related information about the actual spectral power density distribution of the particular Xenon arc solar simulator used was unavailable, after examining the spectral power distribution of the Xenon arc's emitted light produced by several different manufacturers, it was noticed that if appropriate filters are not used, then apart from an enhanced ultra-violet irradiance that the unfiltered xenon spectrum exhibits, there are also two pronounced irradiance peaks in the 0.8 μ m-1.0 μ m spectral range of the unfiltered xenon's spectrum. These two peaks are common in all cases, exhibiting an irradiance intensity of more than twice of that of the standard AM1.5 spectrum in that spectral range (ie 0.8 μ m-1.0 μ m) when the intensity of the xenon's irradiance distribution is adjusted to approximate that of the standard AM1.5 spectrum. The general unfiltered spectral irradiance distribution trend of a typical xenon arc source is shown in Figure 4.4.8, where the pronounced irradiance peaks in the 0.8 μ m-1.0 μ m spectral range of the xenon's arc infra-red spectrum are clearly visible. Even though, it is unknown whether there was any special built-in filter in the "Kratos" solar simulator fixture used at the time of the measurements, the higher short circuit

Figure 4.4.8: General unfiltered spectral irradiance distribution trends of a typical xenon arc light source, showing the pronounced infra-red irradiance peaks associated with such simulated sunlight sources.

current density results obtained with the #1, #2, #3 and #7 poly-Si/a-Si bilayer emitter cells can only be explained if a higher infra-red irradiance than that of the standard AM1.5 spectrum was absorbed and consequently utilized in the substrate of these cells, thus implying that either the xenon's infra-red ($0.8\mu\text{m}$ - $1.0\mu\text{m}$) spectral irradiance was not filtered properly or not at all. This is further supported by the fact that the magnitudes of the short circuit current densities of the cells with the low resistivity FZ substrates (#8, #9) are within the expected short circuit current densities that would normally be obtained under standard AM1.5($100\text{mW}/\text{cm}^2$) illuminated conditions. These particular results are believed to be attributed to the insensitivity of the FZ substrates of these cells to such an enhanced infra-red irradiance due to the lower intrinsic diffusion length that is associated with such substrates.

On the other hand, although the c-Si emitter cell has a similar substrate as that of those poly-Si/a-Si bilayer emitter cells that exhibited higher AM1.5 short circuit current densities than expected (ie #1, #2, #3, #7), its AM1.5 short circuit current density was found to be within the expected short circuit current range that would normally be obtained under standard AM1.5($100\text{mW}/\text{cm}^2$) illumination conditions. However, since the c-Si emitter cell and the poly-Si/a-Si bilayer emitter cells in the latter case were uncoated at the time of the measurements, the light reflectance and transmittance properties of the two different emitter structure cells may differ significantly. This is supported by relevant findings reported by Harbeke [Harb85] comparing the reflectance properties of phosphorus in-situ doped polycrystalline silicon films and c-Si films, where it was shown that uncoated poly-Si films exhibit substantially lower surface reflectances than bare c-Si films for the entire range of the solar spectrum examined, due to the rough top film's surface associated with poly-Si layers in the

former case. It is also quite possible that such polycrystalline silicon films with film thicknesses in the same thickness range as the ones implemented in this work ($t \leq 1,500 \text{ \AA}$) may exhibit higher infra-red transmittance properties than corresponding c-Si films, because of the inherent grain structure of the poly-Si/a-Si bilayer emitter films that could promote infra-red light transmission due to multiple random internal light scattering effects in the polycrystalline film. A combination of such optical properties (ie light reflectance and transmittance) that may be associated with films of poly-crystalline structure, would explain the correspondingly higher short circuit currents obtained with the poly-Si/a-Si bilayer emitter cells under these specific simulated AM1.5(100mW/cm²) illuminating conditions. Finally, the uncertainty error of the short circuit current density results of the solar cells listed in Table 4.4.1 is estimated to be ~10% in most cases, and as high as ~13% in several occasions, of the corresponding expected short circuit current density values that could be obtained under standard AM1.5(100mW/cm²) illuminating conditions, thus indicating that although reproducible illuminated J-V cell characteristics can be obtained with the aid of a solar simulator, short circuit current errors are bound to occur for the reasons cited earlier in Subsection 4.2.

CHAPTER 5

SUMMARY AND RECOMMENDATIONS

5.1 SUMMARY AND CONCLUSIONS

The main objective of this thesis was to investigate various top layer processing and device design techniques that could be applied to the original unoptimized in-situ phosphorus doped monolayer emitter solar cells developed at Carleton U. [Tarr85] in earlier work, with the goal of improving both the initial low fill factors of these devices and their moderate photovoltaic performance.

In an attempt to reduce the high sheet resistance ($\sim 5\text{k}\Omega/\square$ for $\pm 1,000\text{\AA}$ thick layer) of the original poly-Si monolayer emitter, without using undesirable high temperature furnace annealing treatments, a new solar cell structure incorporating an LPCVD in-situ phosphorus doped poly-Si/recrystallized a-Si bilayer film as the emitter was developed. The sheet resistance of poly-Si/recrystallized a-Si bilayer films was examined over a wide thickness range, and although it was found to be slightly higher than that of corresponding recrystallized a-Si films by a factor of ~ 1.4 , it was still substantially lower than that of corresponding poly-Si films by a factor of ~ 5 in most of the film thickness range examined. Acceptably low sheet resistances of $\sim 550\Omega/\square$ and $\sim 300\Omega/\square$ were obtained with poly-Si/a-Si bilayer films as thin as $\sim 1,000\text{\AA}$ and $1,500\text{\AA}$ thick respectively, thus overcoming one of the obstacles towards attaining higher fill factors. Examination of the dark characteristics of poly-Si/a-Si bilayer emitter solar cells showed injection current densities as low as $\sim 10^{-13}\text{A/cm}^2$, allowing open circuit voltages of as high as $\sim 0.65\text{Volts}$ to be obtained at $\sim 30^\circ\text{C}$ under $\text{AM1.5}(100\text{mW/cm}^2)$ illumination conditions. Diode ideality factors of ~ 1.05 over

nearly seven decades of current have been demonstrated, showing the excellent diode quality characteristics of the poly-Si/a-Si emitter solar cells developed in this work. Reproducible dark characteristics were obtained by taking into account the offset irregularity of the phosphine mass flow controller that had passed unnoticed in previous work, and which is believed to have created the reproducibility problems cited in the past on similar poly-Si emitter devices [Keye87].

A strong sheet resistance dependence on film thickness was found in thin poly-Si/a-Si bilayer films, as well as in poly-Si and recrystallized a-Si films. In the case of poly-Si/a-Si bilayer films a sharp increase in the sheet resistance was observed for film thicknesses beyond $\sim 900\text{\AA}$. This abrupt transition in the sheet resistance with film thickness dictated the emitter layer thickness of $900\text{\AA}$ - $1,500\text{\AA}$ used in this work, considering that a compromise had to be made between higher short wavelength photocurrent losses expected with thicker utilized poly-Si layers, and the much higher sheet resistances associated with thinner poly-Si films.

The abrupt increase in sheet resistance that was observed as film thickness decreased in all different polycrystalline film structures examined implies that thin poly-Si films are composed of very small grains and wider grain boundaries due to incomplete crystallization. Such an effect would support Neugroschel's [NAKI85] suggestion that hole diffusion current suppression takes place within a thin disordered layer of poly-Si at the poly-Si/Si interface resulting in the very small back injection current associated with poly-Si contacted devices. It is suggested that wider grain boundaries can immobilize a greater amount of dopant atoms and charge carriers, while in conjunction with an almost certain total depletion of the very small adjacent crystallites that are believed to exist at the

poly-Si/Si junction interface, a low-high-low junction can be created at the grain boundaries acting as an artificial blocking barrier to the diffusion of back-injected carriers. However, cross-sectional XTEM studies of such thin poly-Si films are lacking today and thus the existence of such a disordered poly-Si region is not certain. It is also possible that more than one effect may be taking place at the same time, including a quantum reflection of hole waves at the poly-Si/Si interface as has been suggested by Tarr [Tarr85], due to the abrupt transition from the $\langle 100 \rangle$ c-Si lattice to the predominant $\langle 111 \rangle$ orientation of the polycrystalline silicon grains. Nevertheless, the low back-injection properties associated with poly-Si emitter devices are not well understood and more work has to be done in this area.

Preliminary investigation of short wavelength photocurrent losses associated with the implementation of poly-Si/a-Si bilayer emitter thicknesses in the 900Å-1,500Å range, have shown that the average blue response of the poly-Si/a-Si emitter solar cells is as high as ~50% of that obtained with a shallow (1500Å) phosphorus predeposited c-Si emitter cell with an enhanced blue response, indicating that there is a substantial collection of photogenerated minority carriers from the poly-Si/a-Si emitter layer. The short wavelength related photocurrent losses were calculated for AM1.5(83.13mW/cm²) illuminated conditions to be ~1.3mA/cm² for poly-Si/a-Si bilayer emitter cells with emitter thicknesses in the 1,250-1,450Å range, while they were found to be only ~0.9mA/cm² for corresponding cells with bilayer emitter thicknesses in the proximity of ~900Å. The increase in short wavelength response observed for cells utilizing thinner poly-Si/a-Si emitter layers suggests that short wavelength related photocurrent losses can become negligible if very thin poly-Si/a-Si bilayer emitters are implemented.

A suitable front contact current collecting grid geometry was selected and optimized, based on known device parameters and the processing requirements of the top layer. The optimized front contact grid structure implemented allowed for 28 grid fingers (14 grid-fingers/cm) spaced $\sim 700\mu\text{m}$ apart, minimizing the combined total front surface power loss mechanisms of the solar cells to $\sim 3.5\%$. The combined resistive power loss effects accounted for as little as $\sim 2.5\%$ of the total efficiency losses respectively for a $\sim 5\mu\text{m}$ thick metal grid and a poly-Si/a-Si bilayer emitter with sheet resistance less than $500\Omega/\square$. The importance of the utilization of a low emitter sheet resistance and the necessity for a thick front grid metal, towards achieving optimal minimum total front surface power losses, was demonstrated during the front grid optimization study. It was shown that the minimum total front surface power losses can be reduced by as much as $\sim 50\%$ when an emitter layer of $\sim 500\Omega/\square$ sheet resistance is implemented in conjunction with a $\sim 5\mu\text{m}$ thick front grid metal, as compared to that of a $\sim 5\text{ k}\Omega/\square$ emitter layer implemented in conjunction with a $\sim 5\mu\text{m}$ thick front grid metal, as in the case of a poly-Si monolayer emitter cell. This demonstrates the profound advantage of the low emitter sheet resistance that poly-Si/a-Si bilayer emitter solar cells have over poly-Si monolayer emitter cells in attaining high conversion efficiencies.

Investigating different front contact metallization processes, it was shown that although electroplating is a flexible cheap metal deposition process having the ability to deposit very thick highly conducting metal films in excess of $5\mu\text{m}$, it is not as reliable as e-beam evaporation. On the other hand, although the e-beam metal deposition process was capable of depositing metal films in the $5\mu\text{m}$ range, the main disadvantage of this process is that it is not as cost effective as the electroplating process for industrial applications.

Among the metal diffusion barriers examined, the $\text{Ti}_{0.1}\text{W}_{0.9}$ refractory metal proved to be the most reliable, demonstrating its diffusion barrier capabilities against Al and Au migration at 450°C , thus making possible the necessary post-hydrogen annealing and sintering treatments required to obtain both a good quality cell and good front and back metal contacts. The proven diffusion barrier properties of $\text{Ti}_{0.1}\text{W}_{0.9}$ in conjunction with its well known adhesion and corrosion resistant properties [CuFH70] makes this refractory metal very attractive, not only for poly-Si emitter solar cells, but for other types of low cost commercial polycrystalline silicon solar cells as well. The most reliable and acceptable metallization scheme was the $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Al}$ bimetal configuration, exhibiting a contact resistance of $\sim 200\mu\Omega/\text{cm}^2$, which is relatively low for solar cell applications, while aluminum thicknesses as high as $5\mu\text{m}$ were made possible by e-beam evaporation, thus fulfilling the metallization requirement objectives. High temperature $\text{Ti}_{0.1}\text{W}_{0.9}$ -based metal diffusion barrier configurations were also developed withstanding heat treatments as high as 650°C for 10 min, having industrial application capabilities in modern encapsulation methods of solar cell modules on commercial production lines.

Fill factors as high as ~ 0.80 and total series resistances as low as $\sim 0.46\Omega\cdot\text{cm}^2$ have been demonstrated for poly-Si/a-Si bilayer emitter cells utilizing the optimized front contact grid structure design and the metallization schemes developed in this work, fulfilling the main objective of this thesis. Conversion efficiencies as high as 14% have been demonstrated under $\text{AM1.5}(100\text{mW}/\text{cm}^2)$ simulated sunlight conditions for poly-Si/a-Si bilayer emitter cells with a primitive SiO_x antireflection coating, while poly-Si/a-Si emitter solar cells with state-of-the-art device design features should be able to attain much higher conversion efficiency values. The open circuit voltage superiority of poly-Si/a-Si

bilayer emitter cells over that obtained with c-Si emitter cell has been demonstrated. It has also been shown that different quality substrates have a profound effect on the open-circuit voltage of poly-Si/a-Si bilayer emitter devices, where cells with lower resistivity substrates have the capability of achieving higher open circuit voltages. An open circuit voltage of as high as ~ 0.65 volts at $\sim 30^\circ\text{C}$ was obtained with an uncoated poly-Si/a-Si emitter cell having a low resistivity ($0.1\Omega\cdot\text{cm}$) high quality float-zone substrate, while a very high open circuit voltage of ~ 0.67 volts was obtained with a poly-Si/a-Si bilayer emitter cell illuminated to give a photocurrent density of $\sim 32\text{mA}/\text{cm}^2$ at $\sim 28^\circ\text{C}$, indicating the distinct capability of poly-Si/a-Si bilayer emitter solar cells of setting high open circuit voltage records if optimized state-of-the-art structural design features such as back surface fields are implemented.

Although an attempt was made early in this work to predetermine the photocurrent losses associated with different poly-Si/a-Si bilayer emitter thicknesses, assuming that the absorption coefficient of the poly-Si/a-Si bilayer would be close to that of c-Si, experimental absolute spectral response results obtained later implied that the absorption coefficient of the poly-Si/a-Si emitter films was higher than expected. Absolute spectral response measurements have provided strong indications that much of the ultra-violet, blue and visible irradiance is strongly absorbed in the poly-Si/a-Si bilayer emitter region of the solar cells. Nevertheless, despite this effect the total photocurrent losses of the poly-Si/a-Si bilayer emitter cells associated with the response loss in the ultra-violet, blue and visible region of the solar spectrum were not severe. An AM1.5 ($83.18\text{mW}/\text{cm}^2$) total emitter photocurrent loss of $\sim 3\text{mA}/\text{cm}^2$ was estimated for cells utilizing poly-Si/a-Si bilayer emitter thicknesses in the $1,400\text{--}1,500\text{\AA}$ range, while for cells with poly-Si/a-Si emitter thicknesses in the proximity of $900\text{\AA}$, a

50% reduction in the photocurrent losses was determined with a $\sim 1.5 \text{ mA/cm}^2$ total emitter related photocurrent loss.

Photocurrent densities as high as 30 mA/cm^2 were obtained under AM1.5 (100 mW/cm^2) simulated illuminated conditions with a poly-Si/a-Si bilayer emitter cell having a $\sim 1500 \text{ \AA}$ emitter thickness and covered with a primitive single layer SiO_x antireflection coating, demonstrating the distinct possibility of attaining much higher short-circuit current densities if state-of-the-art device design structures are implemented (i.e good double antireflection coating, light trapping design, and a back surface field).

Finally, in-situ phosphorus doped poly-Si/a-Si bilayer emitter cells with state-of-the-art design features should be able to outperform in all aspects c Si emitter cells with similar design features, if very thin poly-Si emitter layers are utilized in conjunction with a highly conducting transparent oxide like ITO.

5.2

RECOMMENDATIONS FOR FUTURE WORK

There are several aspects that have to be investigated for further improvements on the performance of poly-Si emitter solar cells.

Poly-Si/a-Si bilayer emitter solar cells with thinner emitters have already exhibited a reduction of the total emitter related photocurrent losses to acceptable low levels. It is suggested that if a very thin n^+ poly-Si emitter layer is utilized ($<500\text{\AA}$), the built-in electric field in the entire emitter region will be strong enough to enhance the drift of the photogenerated minority carriers in the emitter to the point where almost all of these minority carriers will be collected by the junction. Therefore, the following recommendations are suggested:

- Ultra-thin poly-Si monolayer emitters ($100\text{-}300\text{\AA}$) must be investigated towards determining the emitter-related photocurrent losses of such solar cell devices using absolute spectral response measurements.
- Rapid thermal annealing must also be investigated as a means of reducing the very high sheet resistance of such ultra-thin films.
- A high conductive transparent oxide like ITO should be implemented in conjunction with such thin poly-Si emitter layers. Further investigation is needed in evaluating the feasibility of this approach.
- Silver electroplating should be investigated as a means of depositing the thick metal grid contact, since silver makes also a very good contact to ITO.
- State-of-the-art device design trends use thinner low resistivity c-Si substrates with light trapping design features which are not hard to implement and they can easily be adapted to these cells.

- An in-situ boron doped poly-Si back surface field should also be implemented in addition to the previous suggested design features, since it has already been shown by Lindholm et al [LNAI85] that such a BSF is superior to conventional back surface fields formed by Al-paste alloying techniques resulting in higher open circuit voltages and enhanced red spectral responses.
- Apart from the poly-Si emitter device improvements that can be made, optical measurements will be very helpful in evaluating the reflectance and transmittance properties of in-situ phosphorus doped poly-Si films, thus making possible the determination of the absorption coefficient of such films.
- Cross-sectional XTEM studies are also necessary to determine the grain structure of poly-Si films close to the poly-Si/Si junction interface, and may give some possible answers to the low-back injection current.
- SIMS measurements are also necessary for the determination of the actual dopant concentration of in-situ phosphorus doped poly-Si films.

Suggested basic processing steps and fabrication details required to develop a state-of-the-art poly-Si emitter solar cell capable of reaching very high efficiencies (~20%), and very high open circuit voltage records (>700mV), are shown in the following schematic diagrams under the heading "ITO/ULTRA-THIN n^+ POLY-Si EMITTER SOLAR CELL WITH p^+ POLY-Si BSF AND LIGHT TRAPPING DESIGN". A detailed suggested processing runsheet for such a state-of-the-art poly-Si emitter solar cell is given in Appendix 3. The development and fabrication details of such a solar cell are currently under investigation at Carleton U.

ITO/ ULTRA-THIN n^+ POLY-SI EMITTER SOLAR CELL WITH p^+ POLY-SI BSF AND LIGHT TRAPPING DESIGN
(SCHEMATIC DIAGRAMS OF SUGGESTED PROCESSING STEPS, AND RELEVANT FABRICATION DETAIL CONSIDERATIONS)

1)

i) THINNING OF SUBSTRATE FROM $\sim 300\mu\text{m}$ TO $100\mu\text{m}$ - $150\mu\text{m}$
 $35\% \text{ KOH} @ 95^\circ\text{C}$

ii) REMOVE POTASSIUM CONTAMINATION FROM SI-SURFACE WITH:
 $\text{HNO}_3\text{-HF-CH}_3\text{COOH (95:5:10)}$ AT ROOM TEMPERATURE FOR 1min

2)

DEPOSIT LOTOX: $\sim 3000\text{\AA} \text{ SiO}_2 @ 400^\circ\text{C}$

3)

DEFINE ACTIVE AREA

i) PATTERN FRONT SURFACE

ii) REMOVE EXCESS OXIDE FROM FRONT AND BACK SURFACE

4)

TEXTURIZE FRONT AND BACK SURFACE: (FORM V-GROOVES)

- $\text{KOH (135 gm) : ISOPROPYL ALCOHOL (40 ml) : H}_2\text{O (400 ml) @ } 70^\circ\text{C}$ FOR 14 min
 (NEED TO REMOVE POTASSIUM CONTAMINATION IN THIS CASE)

OTHER CHEMICAL ETCHANTS FOR TEXTURIZING SURFACES (V-GROOVES):

- $\text{KOH (23.4%) : NORMAL PROPYL ALCOHOL (13.3%) : H}_2\text{O (23.4%) @ } 82^\circ\text{C}$
 - $\text{ETHYLENE DIAMINE : H}_2\text{O (1:3) BOIL FOR 10min}$

- $\text{N}_2\text{H}_4 : \text{H}_2\text{O (60:40) @ } 110^\circ\text{C}$ FOR 10min
 - $\text{N}_2\text{H}_4 : \text{H}_2\text{O (65:35) @ } 100^\circ\text{C}$ FOR 15min

5)

DEPOSIT $\sim 200\text{\AA}$, $\sim 300\text{\AA} \text{ } n^+ \text{ POLY-Si @ } 627^\circ\text{C}$

PH_3 : 13.5% + OFFSET
 SiH_4 : 20.0%

$T=627^\circ\text{C}$
 $t=5\text{min, } 10\text{min}$

* DURING SPUTTER ETCHING IN THE TIW DEPOSITION PROCESS
 $\sim 100\text{\AA}$ OF THE INITIAL DEPOSITED POLY-Si WILL BE LOST

6)

i) PROTECT FRONT SURFACE WITH P.R

ii) ETCH $n^+ \text{ POLY-Si}$ FROM BACK SURFACE

7)

DEPOSIT LOTOX: $\sim 300\text{\AA} \text{ SiO}_2 @ 400^\circ\text{C}$

i) PROTECT FRONT SURFACE WITH P.R

ii) ETCH OXIDE FROM BACK SURFACE UNTIL p-Si SUBSTRATE IS EXPOSED

B₂H₆: 31.0%
SiH₄: 36.0%

T=560°C
t=20min

DEPOSIT ~1000Å p⁺ (BORON DOPED) POLY-Si @ 560°C

i) PROTECT BACK SURFACE WITH P.R

ii) ETCH p⁺ POLY-Si FROM FRONT SURFACE UNTIL THE OXIDE IS EXPOSED

iii) ETCH OXIDE FROM FRONT SURFACE UNTIL n⁺ POLY-Si IS EXPOSED

i) PROTECT BACK SURFACE WITH P.R

ii) PATTERN n⁺ POLY-Si EMITTER

iii) ETCH EXCESS n⁺ POLY-Si FROM FRONT SURFACE UNTIL OXIDE IS EXPOSED

iv) USE RTA @ 900°C FOR 6sec ON BOTH FRONT + BACK SURFACE

i) DEPOSIT ~1500Å TiW (SPUTTERED) ON FRONT SURFACE

ii) DEPOSIT ~1500Å TiW (SPUTTERED) ON BACK SURFACE

i) DEPOSIT ~5μm ALUMINUM (e-beam) ON FRONT SURFACE

ii) DEPOSIT ~2μm ALUMINUM (e-beam) ON BACK SURFACE

i) PATTERN FRONT BIMETAL

ii) PROTECT BACK WITH P.R

iii) ETCH EXCESS ALUMINUM AND TITANIUM-TUNGSTEN FROM FRONT SURFACE

iv) HYDROGEN ANNEALING AT 125°C FOR 20min

3

OF/DE

3

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APPENDIX 1: RUN SHEET FOR POLY-Si/RECRYSTALLIZED μ -Si EMITTER SOLAR CELLS

Starting Material:	Ventron	p-type <100>	1.8-2.6 Ω .cm
	Semimetals	p-type <100>	3.2-4.3 Ω .cm ; 8.0-10.0 Ω .cm
	Wacker FZ	p-type <100>	0.375-0.625 Ω .cm
	Wacker FZ	p-type <100>	0.07-0.135 Ω .cm

1) RCA Clean**2) Lotox Deposition**

- Deposition temperature: 405°C
- Pressure: 0.3 Torr
- Si₂H₄ flow setting: 25% (50.0 sccm)
- O₂ flow setting: 27.5% (55.0 sccm)
- Deposition time: 12min
- Expected thickness: 2,000Å

3) Open Device Wells**a) Mask: CU-106-01-0A**

- Apply HMDS and NEGATIVE PR (Waycoat HNR-80) on front surface
- Spin at 5,000 RPM for 30sec
- Prebake at 80-85°C for 25min
- Expose in UV light for 3sec
- Develop in Waycoat Negative Resist Developer for 90sec continue developing in thinner developer (Waycoat PF) for 20sec
- Rinse in two baskets of Propanol for 20sec
- Blow dry with N₂
- Inspect under microscope
- Postbake at 130°C for 30min

b) Etch SiO₂ in Silox etchant at 20°C until bare silicon is exposed

Expected etch time: ~150sec
 Rinse in DI H₂O for 10min
 Blow dry with N₂

c) Strip PR in Caro's acid at 110°C for 10min

Rinse in DI H₂O for 10min
 Blow dry with N₂

4) Poly-Si/a-Si Emitter Deposition

- a) RCA Clean
- b) Immediately before deposition, dip wafers in 10% HF for 2sec to ensure windows are hydrophobic ; Rinse for 5min and then spin dry at 2,400 RPM in N₂ for 5min
- c) Poly-Si Deposition
  - Deposition temperature: 627°C
  - Pressure: 0.28 Torr
  - PH₃ flow setting: 13.5% + Offset (0.2229 sccm)
  - SiH₄ flow setting: 20% (41.120 sccm)
  - Deposition time: 5min
  - Expected thickness of deposited layer: ≈200Å

Lower the temperature to 560°C and proceed to next step

- d) a-Si Deposition
  - Deposition temperature: 560°C
  - Pressure: 0.28 Torr
  - PH₃ flow setting: 6.0% + Offset (0.0991 sccm)
  - SiH₄ flow setting: 26.0% (52.498 sccm)
  - Deposition times: 60min - 110min
  - Expected thickness of deposited layers: 900Å - 1,600Å

5) Recrystallization Anneal

- Furnace temperature: 650°C

10min	preheat	in N ₂
2min	push	in N ₂
60min	anneal	in N ₂
2min	pull	in N ₂
5min	cool	in N ₂

6) Pattern Poly-Si

- a) Mask: CU-106-02-0A
  - Apply HMDS and POSITIVE PR (Waycoat HPR-204) on front surface
  - Spin at 4,700 RPM for 30sec
  - Prebake at 100°C for 30min
  - Expose in UV light for 6-7sec
  - Develop in 50% Waycoat Positive Developer + 50% H₂O for 60-90sec
  - Rinse in DI H₂O for 2-5min
  - Blow dry with N₂
  - Postbake at 130°C for 30min
- b) Etch Poly-Si in HNO₃+H₃PO₄+HF+DI H₂O (30:10:1:15) at 20°C until the oxide is exposed
  - Rinse in DI H₂O for 10min
  - Blow dry with N₂
- c) Strip PR in Caro's acid at 110°C for 10min
  - Rinse in DI H₂O for 10min
  - Blow dry with N₂

7) Back Contact Metallization

- a) Dip wafers in 10% HF for 2sec to remove native oxide on back surface
  - Rinse in DI H₂O for 10min
  - Blow dry with N₂
- b) Deposit 2μm Al by e-beam on back surface
  - Density of Al: 2.7gm/cm³
  - Base pressure: 1x10⁻⁶ Torr
  - Deposition rate: 15Å/min
- c) Sintering
  - Furnace temperature: 450°C

5min	preheat	in N ₂
5min	preheat	in H ₂
20sec	push	in H ₂
20min	anneal	in H ₂
20sec	pull	in H ₂
5min	cool	in H ₂
5min	cool	in N ₂

8) Front Contact Metallization Schemes

A) $\text{Ti}_{0.1}\text{W}_{0.9}/\text{Au}$ Sputtering followed by Au Electroplating

a) RF Sputtering

Diameter of targets: 5"

Distance of target from substrate: 2.5"

Base pressure: $3\text{-}5 \times 10^{-7}$ Torr

Ar partial pressure: 8×10^{-3} Torr

Ar flow: 92.3 sccm

- Sputter etch front surface for 1min to remove native oxide
RF Power: 100W
RF Peak Voltage: 950V
- Sputter 600Å $\text{Ti}_{0.1}\text{W}_{0.9}$
RF Power: 100W
RF Peak Voltage: 1.4kV
Deposition Rate: 100Å/min
- Sputter 300Å Au
RF Power: 100W
RF Peak Voltage: 1.4kV
Deposition Rate: 100Å/min

b) Pattern Front Metal

- Mask: CU-106-03-0A (0B)
- Apply HMDS and POSITIVE PR (Waycoat HPR-204) on back surface
- Spin at 4,700 RPM for 30sec
- Coat front surface with HMDS and POSITIVE PR (AZ-1375)
- Spin at 2,500 RPM for 30sec
- Expected PR thickness: 3.5 - 4.0µm
- Prebake at 100°C for 30min
- Expose in UV light for ~16sec
- Develop in 50% Waycoat Positive Developer + 50% H_2O for ~100sec
Rinse in DI H_2O for 2-5min
Blow dry with N_2

- c) **Au Electroplating**
- Raise temperature of Au Solution to 48-50°C
  - Immerse wafers in Au Solution
  - Apply forward current of 1.7mA to front surface
  - Target thickness: 5µm
  - Expected time: 40min
- d) **Strip PR in J-100 at 100-110°C for 10min**
Rinse in DI H₂O for 30min
Blow dry with N₂
- e) **Etching of Sputtered Au Seed Layer**
- Protect the back surface with POSITIVE PR (Waycoat HPR-204)
  - Etch in KI+I₂+DI H₂O (4:1:10) at room temperature with the aid of the ULTRASONIC AGITATOR
  - Expected etch time: 10-15sec
Rinse in DI H₂O for 10min
Blow dry with N₂
- f) **Etching of Sputtered Ti_{0.1}W_{0.9} Layer**
- Etch in 30% H₂O₂ at room temperature
  - Expected etch time: ≈10min
Rinse in DI H₂O for 10min
Blow dry with N₂
- g) **Strip PR in J-100 at 100-110°C for 10min**
Rinse in DI H₂O for 30min
Blow dry with N₂
- h) **Annealing of Sputtering Radiation and Ion Bombardment Damage**
- Furnace temperature: 400°C

5min	preheat	in N ₂
5min	preheat	in H ₂
20sec	push	in H ₂
20min	anneal	in H ₂
20sec	pull	in H ₂
5min	cool	in H ₂
5min	cool	in N ₂

B) $\text{Ti}_{0.1}\text{W}_{0.9}$ Sputtering followed by Al Evaporation

a) RF Sputtering

- Base pressure: $3\text{-}5 \times 10^{-7}$ Torr
- Ar partial pressure: 8×10^{-3} Torr
- Ar flow: 92.3 sccm
- Sputter etch front surface for 1min to remove native oxide
RF Power: 100W
RF Peak Voltage: 950V
- Sputter $1,000\text{\AA}$ $\text{Ti}_{0.1}\text{W}_{0.9}$
RF Power: 100W
RF Peak Voltage: 1.4kV
Deposition Rate: $100\text{\AA}/\text{min}$

b) Al Evaporation

- Deposit $4\text{-}5\mu\text{m}$ Al by e-beam
Density of Al: $2.7\text{gm}/\text{cm}^3$
Base pressure: 1×10^{-6} Torr
Deposition rate: $15\text{\AA}/\text{min}$

c) Pattern Front Metal

- Mask: CU-106-04-0A
- Apply HMDS and POSITIVE PR (Waycoat HPR-204) on front surface
- Spin at 4,700 RPM for 30sec
- Prebake at 100°C for 30min
- Expose in UV light for 6-7sec
- Develop in 50% Waycoat Positive Developer + 50% H_2O for 60-90sec
Rinse in DI H_2O for 5min ; blow dry with N_2
- Postbake at 130°C for 30min

d) Etching of Al

- Protect the back surface with POSITIVE PR (Waycoat HPR-204)
- Etch Al in H_3PO_4 at 60°C
- Expected total etch time: $\approx 6\text{min}$

Etching steps to avoid PR lift off and to minimize pattern undercutting:

4min etch		2min etch
5min rinse in DI H_2O	+	5min rinse in DI H_2O
10min bake at 130°C		10min bake at 130°C

e) Etch $\text{Ti}_{0.1}\text{W}_{0.9}$ in $\text{DI H}_2\text{O} + \text{NH}_4\text{OH} + \text{H}_2\text{O}_2$ (5:1:1) at 75°C

- Expected etch time: $\approx 5\text{sec}$
- Rinse in $\text{DI H}_2\text{O}$ for 10 min
- Blow dry with N_2

f) Strip PR in J-100 at $100\text{--}110^\circ\text{C}$ for 10min, or in MICROSTRIP-2001 at 75°C for 10min

- Rinse 15min in $\text{DI H}_2\text{O}$
- Blow dry with N_2

g) Annealing of Sputtering and e-beam Radiation Damage

- Furnace temperature: 450°C
  - 5min preheat in N_2
  - 5min preheat in H_2
  - 20sec push in H_2
  - 20min anneal in H_2
  - 20sec pull in H_2
  - 5min cool in H_2
  - 5min cool in N_2

9) Antireflection Coating

- Deposit $740\text{\AA}$ SiO_x by thermal evaporation

Density of SiO_x : 2.13gm/cm^3

Base pressure: 3×10^{-6} Torr

Back fill with N_2 3-4 times to minimize moisture in the chamber

Deposition rate: $5\text{\AA}/\text{sec}$

NOTES

- 1) **RCA Clean**
  - a) Etch in DI H₂O+NH₄OH+H₂O₂ (5:1:1) at 80°C for 10min
(To remove organic contaminants)
(Rinse 10min in DI H₂O)
  - b) Etch in DI H₂O+HCl+H₂O₂ (6:1:1) at 80°C for 10 min
(To remove metal contaminants)
Rinse 10min in DI H₂O
  - c) Etch in 10% HF for 2min
(To remove residual oxide)
Rinse 10min in DI H₂O
Blow dry with N₂
- 2) **Silox Etchant** is a modified buffered HF solution
- 3) **Caro's Acid**: H₂SO₄+H₂O₂ (25:1)
Heat 500ml H₂SO₄ to 95°C, add 20ml H₂O₂ and heat solution to 110°C
The solution will be active for ~15min
- 4) Most of the chemicals used are toxic or corrosive. Appropriate safety precautions should be followed (ie. use of rubber gloves, fume hood, wash hands, etc.)

APPENDIX 2: RUN SHEET FOR PREDEPOSITED PHOSPHORUS EMITTER SOLAR CELLS

* FOLLOW PROCEDURE AS DESCRIBED IN APPENDIX 1 WITH THE BELOW LISTED MODIFICATIONS

Starting Material: Semimetals p-type <100> 1.8-2.6 Ω .cm with a 1,000Å thermally grown oxide

- OMIT steps 1) through 2)

3) Open Device Wells

a) Mask: CU-106-01-0A

- **Apply HMDS and NEGATIVE PR (Waycoat HNR-80) on front surface; COATBACKS**
- **Spin at 5,000 RPM for 30sec**
- **Prebake at 80-85°C for 25min**
- **Expose in UV light for 3sec**
- **Develop in Waycoat Negative Resist Developer for 90sec ; continue developing in thinner developer (Waycoat PF) for 20sec**
- **Rinse in two baskets of Propanol for 20sec**
Blow dry with N₂
Inspect under microscope
- **Postbake at 130°C for 30min**

b) Etch SiO₂ in Buffered HF at 20°C until bare silicon is exposed
Expected etch time: 80-90sec
Blow dry with N₂

c) Strip PR in Caro's acid at 110°C for 10min
Rinse in DI H₂O for 10min
Blow dry with N₂

4) Emitter Predeposition

a) RCA Clean

b) Phosphorus Predeposition Process

i) Predeposition Parameters

- Source: POCl_3 @ 20°C
- Tube temperature: 850°C
- N_2 carrier gas flow: 1.7slpm
- N_2 /dopant gas flow: $\sim 10\text{sccm}$ (2.5mg/min POCl_3)
- O_2 gas flow: $\sim 40\text{sccm}$ (53.25mg/min)

ii) Establish Steady-State Conditions

- Pre-saturate the Quartz tube with $\text{N}_2+\text{O}_2+\text{N}_2/\text{dopant}$ for 60min in order to get a STEADY-STATE of dopant level

Flushing time: 60min

iii) Predeposition Steps

5min	preheat	in N_2+O_2
30sec	push	in N_2+O_2
5min	warm-up	in N_2+O_2
90sec	dope	in $\text{N}_2+\text{O}_2+\text{N}_2/\text{dopant}$
10min	hold	in N_2+O_2
5sec	pull	in N_2+O_2
5min	cool	in N_2+O_2

- Expected Junction Depth: $\sim 1,500\text{\AA}$
- Expected Sheet Resistance: $\sim 400\Omega/\square$

* There are no Phosphosilicate Glass Removal and Drive-in steps

- OMIT steps 5) through 6)

7) Back Contact Metallization

- a) Etch SiO_2 on back surface in concentrated HF until bare silicon is exposed

Rinse in DI H_2O for 10min

Blow dry with N_2

- b) Deposit $2\mu\text{m}$ Al by e-beam on back surface

Density of Al: 2.7gm/cm^3

Base pressure: 1×10^{-6} Torr

Deposition rate: $15\text{\AA}/\text{min}$

- c) Sintering

- Furnace temperature: 450°C

5min preheat in N_2

5min preheat in H_2

20sec push in H_2 /

20min anneal in H_2

20sec pull in H_2

5min cool in H_2

5min cool in N_2

- OMIT step 8A)
- Steps 8B)a) through 8B)f) remain the SAME
- OMIT steps 8B)g) through 9)

**APPENDIX 3: SUGGESTED RUN SHEET FOR ITO/ n^+ POLY-Si EMITTER SOLAR CELLS
WITH p^+ POLY-Si BSF AND LIGHT TRAPPING DESIGN**

Starting Material: 4 Ventron p -type $\langle 100 \rangle$ 1.8-2.6 $\Omega \cdot \text{cm}$

2 Wacker FZ p -type $\langle 100 \rangle$ 0.1 $\Omega \cdot \text{cm}$

1) Substrate Thinning

a) Etch substrate in 35% KOH @ 95°C down to $\sim 140\mu\text{m}$ (130-150 μm)

Expected etching time: _____ min

Rinse in DI H_2O for 10min

b) Etch clean substrate in $\text{HNO}_3 + \text{HF} + \text{CH}_3\text{COOH}$ (85:5:10) at room temperature for 1min to remove potassium contamination

Rinse in DI H_2O for 10min

2) RCA Clean

3) Lotox Deposition (First)

- Deposition temperature: 405°C
- Pressure: 0.3 Torr
- Si_2H_4 flow setting: 25% (50.0 sccm)
- O_2 flow setting: 27.5% (55.0 sccm)
- Deposition time: 18min
- Expected thickness: 3,000Å

4) Open Device Wells

a) Mask: CU-106-01-0A

- Apply HMDS and NEGATIVE PR (Waycoat HNR-80) on front surface
- Spin at 5,000 RPM for 30sec
- Prebake at 80-85°C for 25min
- Expose in UV light for 3sec
- Develop in Waycoat Negative Resist Developer for 90sec continue developing in thinner developer (Waycoat PF) for 20sec
- Rinse in two baskets of Propanol for 20sec
- Blow dry with N_2
- Inspect under microscope
- Postbake at 130°C for 30min

- b) Etch SiO_2 in Lotox etchant at 20°C until bare silicon is exposed

Expected etch time: $\approx 150\text{sec}$

Rinse in DI H_2O for 10min

Blow dry with N_2

- c) Strip PR in Caro's acid at 110°C for 10min

Rinse in DI H_2O for 10min

Blow dry with N_2

5) Texturize Front and Back Surface (V-Grooves)

- a) Texturize wafers in $\text{KOH}(135\text{gm}) + \text{ISOPROPYL ALCOHOL}(40\text{ml}) + \text{H}_2\text{O}(400\text{ml})$

@ 70°C for 14min

Rinse 10min in DI H_2O

- b) RCA Clean (It may be necessary to repeat step 1b to remove potassium residues)

6) Phosphorus doped Poly-Si Emitter Deposition

- a) Immediately before deposition, dip wafers in 10% HF for 2sec to ensure windows are hydrophobic ; Rinse for 5min and then spin dry at 2,400 RPM in N_2 for 5min

- b) Poly-Si Deposition

- Deposition temperature: 627°C
- Pressure: 0.28 Torr
- PH_3 flow setting: 13.5% + Offset (0.2229 sccm)
- SiH_4 flow setting: 20% (41.120 sccm)

Wafer No.	Deposition time	Expected thickness
(2 Ventron; 1 FZ)_____	<u>5 min</u>	<u>150-250 Å</u>
(2 Ventron; 1 FZ)_____	<u>10 min</u>	<u>250-350 Å</u>

7) Etch Strip Back Surface from Poly-Si (Protect Front Surface)

- a) • Apply HMDS and POSITIVE PR (Waycoat HPR-204) on front surface
- Spin at 4,700 RPM for 30sec
  - Bake at 130°C for 30min
- b) Etch Poly-Si from back surface in $\text{HNO}_3 + \text{H}_3\text{PO}_4 + \text{HF} + \text{DI H}_2\text{O}$ (30:10:1:15) at room temperature until the entire substrate surface (bare silicon) is exposed
- Rinse in DI H_2O for 10min
- Blow dry with N_2

- c) Strip PR in Caro's acid at 110°C for 10min
 Rinse in DI H₂O for 10min
 Blow dry with N₂

8) Lotox Deposition (Second)

- Deposition temperature: 405°C
- Pressure: 0.3 Torr
- Si₂H₄ flow setting: 25% (50.0 sccm)
- O₂ flow setting: 27.5% (55.0 sccm)
- Deposition time: 4min
- Expected thickness: 500Å

9) Etch Strip Back Surface from Lotox (Protect Front Surface)

- a) • Apply HMDS and POSITIVE PR (Waycoat HPR-204) on front surface
- Spin at 4,700 RPM for 30sec
  - Bake at 130°C for 30min
- b) Etch Lotox from back surface in Lotox etchant at room temperature until the entire substrate surface (bare silicon) is exposed
 Rinse in DI H₂O for 10min
 Blow dry with N₂
- c) Strip PR in Caro's acid at 110°C for 10min
 Rinse in DI H₂O for 10min
 Blow dry with N₂

10) Boron doped Poly-Si Back Surface Deposition

- a) Immediately before deposition, dip wafers in 10% HF for ~2sec to remove native oxide; Rinse for 5min and then spin dry at 2,400 RPM in N₂ for 5min
- b) Poly-Si Deposition
- Deposition temperature: 560°C
  - Pressure: ____ Torr
  - B₂H₆ flow setting: 31.0%
  - SiH₄ flow setting: 36.0%%

Wafer No.	Deposition time	Expected thickness
(4 Ventron; 2 FZ) _____	20 min _____	950-1050 Å _____
_____	min _____	Å _____

11) Etch Boron Doped Poly-Si and Lotox from Front Surface (Protect Back)

- a) • Apply HMDS and POSITIVE PR (Waycoat HPR-204) on back surface
  - Spin at 4,700 RPM for 30sec
  - Bake at 130°C for 30min
- b) Etch Boron doped Poly-Si in $\text{HNO}_3+\text{H}_3\text{PO}_4+\text{HF}+\text{DI H}_2\text{O}$ (30:10:1:15) at 20°C until the underneath oxide is exposed completely
Rinse in DI H_2O for 10min
Blow dry with N_2
- c) Etch Lotox in Lotox etchant at room temperature until the Phosphorus doped Poly-Si is exposed completely
Rinse in DI H_2O for 10min
Blow dry with N_2
- d) Strip PR in Caro's acid at 110°C for 10min
Rinse in DI H_2O for 10min
Blow dry with N_2

12) Pattern Phosphorus Doped Poly-Si Emitter (Front Surface)

- a) Mask: CU-106-02-0A
  - Apply HMDS and POSITIVE PR (Waycoat HPR-204) on front surface ;
(COAT PROTECT BACK SURFACE WITH POSITIVE P.R)
  - Spin at 4,700 RPM for 30sec
  - Prebake at 100°C for 30min
  - Expose in UV light for 6-7sec
  - Develop in 50% Waycoat Positive Developer + 50% DI H_2O for 60-90sec
Rinse in DI H_2O for 2-5min
Blow dry with N_2
  - Postbake at 130°C for 30min
- b) Etch Poly-Si in $\text{HNO}_3+\text{H}_3\text{PO}_4+\text{HF}+\text{DI H}_2\text{O}$ (30:10:1:15) at 20°C until the oxide is exposed; (REMINDER: BACK SURFACE MUST BE COATED WITH P.R)
Rinse in DI H_2O for 10min
Blow dry with N_2
- c) Strip PR in Caro's acid at 110°C for 10min
Rinse in DI H_2O for 10min
Blow dry with N_2

13) Rapid Thermal Annealing (OPTIONAL)

RTA @ 900°C for 6sec in N₂ both front and back surface

14) Metallization: Ti_{0.1}W_{0.9} Sputtering followed by Al Evaporation

a) RF Sputtering (Front Surface)

- Base pressure: $3\text{-}5 \times 10^{-7}$ Torr
- Ar partial pressure: 8×10^{-3} Torr
- Ar flow: 92.3sccm
- Sputter etch front surface for 30sec (ONLY) to remove native oxide
RF Power: 100W
RF Peak Voltage: 950V
- Sputter 1,500Å Ti_{0.1}W_{0.9} on front surface
RF Power: 100W
RF Peak Voltage: 1.4kV
Deposition Rate: 100Å/min (Deposition time:~15min)

b) RF Sputtering (Back Surface)

- Base pressure: $3\text{-}5 \times 10^{-7}$ Torr
- Ar partial pressure: 8×10^{-3} Torr
- Ar flow: 92.3sccm
- Sputter etch back surface for 30sec (ONLY) to remove native oxide
RF Power: 100W
RF Peak Voltage: 950V
- Sputter 1,500Å Ti_{0.1}W_{0.9} on back surface
RF Power: 100W
RF Peak Voltage: 1.4kV
Deposition Rate: 100Å/min (Deposition time:~15min)

c) Al Evaporation

- Deposit 4μm Al by e-beam on front surface
Density of Al: 2.7gm/cm³
Base pressure: 1×10^{-6} Torr
Deposition rate: 15Å/min

d) Deposit 2μm Al by e-beam on back surface

Density of Al: 2.7gm/cm³
Base pressure: 1×10^{-6} Torr
Deposition rate: 15Å/min

15) Pattern Front Metal (Protect Back Surface)

- Mask: CU-106-04-0A
- Apply HMDS and POSITIVE PR (Waycoat HPR-204) on front surface;
(COAT PROTECT BACK SURFACE WITH POSITIVE P.R)
- Spin at 4,700 RPM for 30sec
- Prebake at 100°C for 30min
- Expose in UV light for 6-7sec
- Develop in 50% Waycoat Positive Developer + 50% DI H₂O for 60-90sec
Rinse in DI H₂O for 5min ; blow dry with N₂
- Postbake at 130°C for 30min

d) Etching of Al

- Etch Al in H₃PO₄ at 60°C from front surface; (REMINDER: BACK SURFACE MUST BE COATED WITH POSITIVE PR)
- Expected total etch time: ~6min

Etching steps to avoid PR lift off and to minimize pattern undercutting:

4min etch	2min etch (MAXIMUM 3min)
5min rinse in DI H ₂ O	+ 5min rinse in DI H ₂ O
10min bake at 130°C	10min bake at 130°C

e) Etch Ti_{0.1}W_{0.9} in DI H₂O+NH₄OH+H₂O₂ (5:1:1) at 75°C

- Expected etch time: ~5sec
Rinse in DI H₂O for 10 min
Blow dry with N₂

f) Strip PR in J-100 at 100-110°C for 10min, or in MICROSTRIP-2001 at 75°C for 10min

Rinse 15min in DI H₂O
Blow dry with N₂

16) Annealing of Sputtering and e-beam Radiation Damage
(OPTIONAL DEPENDING ON SUCCESS OF DIODE EXPERIMENTS)

- Furnace temperature: 450°C

5min	preheat	in N ₂
5min	preheat	in H ₂
20sec	push	in H ₂
20min	anneal	in H ₂
20sec	pull	in H ₂
5min	cool	in H ₂
5min	cool	in N ₂

END

1 3|0 9|9 0

FIN