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A NOVEL 19 to 38GHz MMIC CPW BALANCED FREQUENCY MULTIPLIER

Kevin So

A Thesis Submitted to the School of Graduate Studies in Partial
Fulfillment of the Requirements for the Degree Master of Applied
Science

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Abstract

This thesis demonstrates the analysis, design and fabrication of a 19 to 38GHz MMIC balanced frequency multiplier with a potential for Local Multipoint Distribution System (LMDS) applications. The circuit is designed in coplanar waveguide (CPW) and utilizes planar transitions (CPW to slot) and a T-junction to achieve a balanced topology. In addition, a new class of compact CPW structures is implemented in the circuit to demonstrate their usefulness. Strong correlation is found between the measured and simulated results. The doubler circuit achieves a maximum conversion gain of -10.37dB at an input power of 15.52dBm.

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CHAPTER 1 *Introduction*

1.1 MMIC

Modern high frequency electronic communication systems require high performance and low cost microwave circuits. Monolithic Microwave Integrated Circuits (MMICs) have provided a solution to these requirements for the last two decades. MMICs allow the integration of components such as transmission lines, resistors, inductors, capacitors, diodes and transistors on a single chip on gallium-arsenide (GaAs) substrate measuring a few millimeters per side. Traditionally, MMICs utilized microstrip technology due to its maturity and the availability of sophisticated models. However, increasingly, MMIC designers are using coplanar waveguide (CPW) technology to develop highly integrated circuits. In CPW, the ground is located on the same plane as the signal, all sitting on top of the substrate. Coplanar technology has the obvious advantages of lower dispersion and lower coupling between adjacent lines, thus allowing higher levels of integration and leading to a reduction in cost. Despite the advantages, coplanar technology is still not generally used in the MMIC design industry.

1.2 LMDS

Emerging commercial wireless applications at the quasi-millimeter and millimeter-wave frequency bands have produced a significant increase in the demand of high performance and low cost MMICs. The applications include fixed satellite, digital point-to-point radio services and local multipoint distribution service (LMDS) [1, 2].

With the significant increase in high speed voice and data demand over the last few years, LMDS broadband wireless promises to be an effective last mile solution for service providers to deliver high capacity services to end users. A LMDS system employs a host microwave radio at a base station, and a network of client radios within a cell site. Currently, in North America, the LMDS band occupies frequencies at 28, 31 and the recently available 38-39GHz.

1.3 Frequency Multipliers

In communication systems such as LMDS, signal generation is very important. The signal must have a high level of stability and low phase noise performance. To achieve these requirements in modern high frequency communication systems, a signal is generated with a low frequency oscillator (VCO) or phase-locked-loops (PLL) and is multiplied by a nonlinear device

through harmonic generation to achieve the desired high frequency. The phase noise added by the frequency multiplier is usually less than what an oscillator or a PLL at the higher frequency would give. As a result, MMIC frequency multipliers are used extensively in microwave transmitters and receivers [3, 4]. Active multipliers have the advantage over diode type for lower conversion loss and are typically configured for frequency doubling yielding good performance [5, 6]. Frequency doublers can be made single ended [7] or balanced [8]. Single ended transistor based doublers have the advantage of allowing a compact size. However, compared to single ended designs, a balanced or push-push (antiseriess) topology offers the potential of superior odd harmonics suppression, but at an increase in size.

A balanced multiplier consists of a pair of identical transistors being driven by signals having 180° phase difference. Due to the phase relation, the fundamental and subsequent odd harmonics are cancelled, while the desired second harmonic signals are constructively combined.

To reduce the size of balanced frequency doublers, coplanar waveguide technology could be employed. Research has been previously published on the design of coplanar frequency doublers. However, with recent developments in novel coplanar passive structures [9], higher levels of integration can be achieved. This thesis investigates the design of a 19 to 38GHz frequency doubler

using CPW technology and incorporating novel coplanar structures to achieve maximum integration.

1.4 Objectives

The objective of this thesis is to design a coplanar 19 to 38GHz balanced multiplier for the possible use in a LMDS application. To achieve a balanced topology, an 180° phase shifting structure is designed using planar transitions. In addition, a new class of novel coplanar structures will be incorporated into the design to achieve a high level of integration. To generate harmonics, a pair of identical Pseudo High-Electron Mobility Transistor (pHEMT) is employed. The performance of the frequency multiplier is simulated, measured and discussed.

This thesis is arranged as follows: Chapter Two details the types of frequency multipliers and reviews published work in this area. Chapter Three examines transmission lines and the advantages of coplanar waveguides. Chapter Four presents the design analysis of the frequency multiplier circuit. Chapter Five reviews the measurements of the fabricated multiplier and compare the results with the simulations of Chapter Four. And finally, Chapter Six concludes the findings and describes future work.

CHAPTER 2 *Frequency Multipliers*

2.1 Introduction

Frequency multiplier circuits are essential components to modern communications equipment. In this chapter, general frequency multiplication theory will be presented. In Section 2.2, passive multipliers will be briefly highlighted while Section 2.3 will describe multipliers employing active devices including the pHEMT. In Section 2.4, expressions will be presented to describe the nonlinear properties to attribute to frequency multiplication. In addition, different design topologies will be covered. In Section 2.5, biasing of the active device in doubler circuits will be discussed. Finally, in Section 2.6, a review of literature relevant to frequency doublers and their performance will be highlighted.

2.2 Passive Frequency Multipliers

Diode circuits are commonly used as harmonic generators at microwave frequencies. They generate higher order harmonics effectively by making use of the diode's nonlinear properties. The major advantage the diode frequency multiplier has over other types of multipliers is that it generates a minimal

amount of noise. Low noise is a desirable property in applications where low phase noise is required, as in phase modulated communication systems and local oscillator (LO) sources for use in radar.

There are primarily three types of diode based frequency multipliers.

Table 2-1 illustrates the properties of each type:

Table 2-1: Types of diode frequency multipliers

Diode Type	Advantages	Disadvantages	Note
Varactors	Low noise Good efficiency	Narrowband	For low harmonics
Step Recovery Diodes (SRD)	Low noise Good efficiency	Narrowband	For very high harmonics in UHF or low microwave frequency range
Resistive Diodes	Broadband	Less efficient	For low order harmonics

Despite the low noise advantage that diode based multipliers have, in contrast to active frequency multipliers, they always exhibit loss (less than unity gain).

2.3 Active Frequency Multipliers

Active frequency multiplying circuits employ the use of transistors instead of diodes to achieve harmonic generation. By using transistors like field-effect transistors (FETs), active frequency multipliers have significant advantages over passive types: they can achieve broad bandwidths and frequency conversion gain greater than unity.

2.3.1 High Electron Mobility Transistors

For MMIC applications, the use of GaAs based pseudomorphic high electron-mobility transistors (pHEMTs) in multiplying circuits allow for high gain up to millimeter wavelengths of operation. The high electron mobility transistor (HEMT) is essentially a field-effect transistor having current carrying electrons densely confined in a thin layer of order 100Å thickness [10]. The basic principles of their operation are similar to those of metal-semiconductor field effect transistors (MESFETs) [11]. The main difference between FETs and HEMTs are their epitaxial layer structures. Table 2-1 outlines the difference in device structure between the GaAs MESFET, HEMT and pHEMT. In a HEMT device, the structure is

Table 2-2: Epitaxial compositions of basic MESFET, HEMT and pHEMT devices.

Device Layer	MESFET	HEMT	pHEMT
Ohmic Contact	n ⁺ GaAs	n ⁺ GaAs	n ⁺ GaAs
Schottky Contact	n GaAs	n AlGaAs	n AlGaAs
Donor		n ⁺ AlGaAs	n ⁺ AlGaAs
Spacer		Un-doped AlGaAs	Un-doped AlGaAs
Channel	n ⁺ GaAs	Un-doped GaAs	Un-doped InGaAs
Buffer	p- GaAs	p- GaAs	p- GaAs
Substrate	GaAs	GaAs	GaAs

composed of different layers that are grown to optimize and to extend the performance of the FET. Figure 2.1 illustrates the cross-sectional epitaxial structure of the basic GaAs pHEMT.

$$NF_{\min} \approx 1 + \frac{2\omega C_{gc}}{g_m} \left(\frac{R_s + R_g}{R_i} \right)^{\frac{1}{2}} \quad (2.3.1)$$

where C_{gc} is the gate channel capacitance, and R_s , R_g and R_i are the source, gate and intrinsic resistances respectively, the pHEMT noise figure is minimized.

In terms of power amplification, Figure 2.2 illustrates power performance of MESFET and pHEMTs examined by [12]. It can be seen that pHEMTs have higher power performance compared to MESFETs, especially at the higher frequencies.

Figure 2.2: Power performance of the MESFET vs. pHEMT as a function of frequency [12].

Finally, for high frequency operation, pHEMTs offer the best choice due to high gain up to millimeter-wavelengths and good noise and power performance at those frequencies [12]. It should be also noted that for this thesis, the only device available based on the fabrication process was the pHEMT.

2.4 Frequency Multiplication

2.4.1 Nonlinear circuits

In order to understand frequency multiplication, we must examine some frequency generation properties of nonlinear microwave circuits. Circuits that are said to be linear are simply circuits that behave with very weak nonlinearity and therefore are treated as if they were linear for only an approximation. For example, small signal amplifiers are used and treated in systems as if they were linear. In these systems, the nonlinear phenomenon generates unwanted harmonics that degrade system performance.

On the other hand, circuits like frequency multipliers, maximize the nonlinear properties of devices to generate desired harmonics. To understand the basic concept of frequency multiplication, we need to simplify the process by ignoring nonlinearities due to device reactance and any higher order mixing effects. With these assumptions, we can begin to analyze the multiplication

process. Figure 2.3 shows a basic circuit with excitation V_s , a resulting current I and a two terminal nonlinear device. With no source impedance, the voltage of

Figure 2.3: Basic circuit with a two terminal nonlinear device.

the nonlinear device is simply V_s and the current can therefore be found by expansion of a Taylor series. The nonlinear device has a transfer characteristic function g . Therefore the output current I can be described by:

$$I = g(V_s) \quad (2.4.1)$$

and where V_s is given by:

$$V_s = v_s(t) = V \cos(\omega t) \quad (2.4.2)$$

As stated earlier, by expansion of the current as a Taylor series, the output current can be written as:

$$\begin{aligned}
 I = i(t) &= g(v_s(t)) = g_0 + g_1 V \cos(\omega t) + g_1 (V \cos(\omega t))^2 + \dots & (2.4.3) \\
 &= g_0 + [g_1 V \cos(\omega t)] + \left[g_2 V^2 \left(\frac{1}{2} + \frac{\cos(2\omega t)}{2} \right) \right] + \dots \\
 &= g_0 + \frac{g_2 V^2}{2} + g_1 V^2 \cos(\omega t) + \frac{g_2 V^2}{2} \cos(2\omega t) + \dots
 \end{aligned}$$

From the Taylor series, the output current I consists of a DC component, a fundamental component of magnitude $g_1 V^2$ at frequency ω radians, and a second harmonic of magnitude $g_2 V^2/2$. In general, the Taylor series can be extended to the n^{th} power, with harmonics up to $n\omega$ radians due to terms like $\cos(\omega t)^n$ that can be further expanded. It can be seen that the output current can consist of a remarkable number of new frequency components.

The main objective of a frequency multiplier is to maximize the desired harmonic component while eliminating the undesired frequencies of the output current. In the case of a frequency doubler, the harmonic components of 2ω radians should be maximized while eliminating the components of ω radians.

2.4.2 Multiplier Topologies

In many ways, the basic concept behind a frequency multiplier is very similar to that of a power amplifier, except that the input and output of the circuit relate to different frequencies.

The most basic frequency multiplier design is the single-ended topology, consisting of harmonic reflectors as proposed by Rauscher [7]. Figure 2.4

Figure 2.4: Single ended frequency multiplier block diagram.

illustrates a block diagram of the second harmonic reflector type active frequency doubler. The input matching network is designed to conjugately match the input at the fundamental frequency. The input reflector block provides a short circuit for the second harmonic. This can be achieved with the use of an open-circuited quarter-wavelength stub at the doubling frequency, which blocks any second harmonic components propagating back from the gate port of the active device by short-circuiting. At the drain port of the active device, an output current will consist of both the fundamental and harmonic frequency components. To suppress the fundamental frequency component, an output reflector block is employed. This block acts to terminate the active device by presenting an open

circuit load at the fundamental frequency shifted by the conjugate of the output capacitive impedance to the drain, as proposed by Standcliff [13]. Finally, the output matching block is designed to maximize the second harmonic output power to the circuit's load. Using this design method, the desired second harmonic output can be maximized with proper matching while suppressing the fundamental frequency component with the use of reflectors.

Frequency multipliers can also be designed with a balanced approach. By far the most practical and commonly used balanced topology is the antiseriess or "push-push" multiplier, requiring two nonlinear active elements. The major advantage of this type of circuit is its ability to achieve a broadband fundamental frequency short circuit at the drain. Figure 2.5 illustrates the basic topology of an antiseriess circuit. From equation (2.4.1), we can describe the I/V characteristic of a nonlinear resistive device A as:

$$I_A = g(V_A) = g(V_S) = g_0 + g_1V + g_2V^2 + g_3V^3 + g_4V^4 + \dots \quad (2.4.4)$$

In an antiseriess circuit, the applied voltage to an identical device B is reversed, giving device B a current of:

$$I_B = g(V_B) = g(-V_S) = -g_0 - g_1V + g_2V^2 - g_3V^3 + g_4V^4 - \dots \quad (2.4.5)$$

It can be seen from equation (2.4.5) that the DC and the odd-order terms of the

Figure 2.5: Even and odd-order voltages and currents in the antiseries (balanced) circuit.

power series are negative. Adding these two current equations give the output current across R_L :

$$I_L = I_A + I_B = 2g_2V^2 + 2g_4V^4 + \dots \quad (2.4.6)$$

Thus, under sinusoidal excitation, the load current contains only even-order harmonics. Taking the antiseries concept, a balanced frequency multiplier can be designed accordingly. Figure 2.6 illustrates the basic building blocks of a balanced antiseries active frequency multiplier. The two active devices are connected via individual input matching circuits and are mutually connected to a

Figure 2.6: Balanced push-push (antiseriess) active frequency multiplier.

180-degree coupler. As a result, the gates of the two active devices are driven by input signals that have a 180-degree phase difference. Therefore, the output current from the drains will have fundamental components that are out of phase, so each device effectively short circuits each other at the fundamental frequency and creating a virtual ground. The second harmonics of the drain currents will have no phase difference and will combine constructively at the output. There are several advantages to this configuration over a single-ended multiplier circuit. By eliminating the use of filters at the output, parasitic effects can be minimized, allowing the balanced multiplier to have greater bandwidth than would a single-ended device. Secondly, a balanced active multiplier has 3dB greater output power advantage due to an additional nonlinear device. This can be a very

desirable property at high frequencies where smaller active devices have low output power.

2.5 Device Biasing and termination

To design a frequency doubler, determining the pHEMT bias condition is crucial. The objective is to generate a distorted drain current or voltage waveform by means of proper bias. The most effective way to employ the pHEMT in a doubler circuit is to use it as a half-wave rectifier [7]. There are two regions of bias that will result in this optimum nonlinear operation: vicinity of forward conduction and pinch-off (or referred to as Class B in some literature [7]).

2.5.1 Region I: Forward Conduction

In this region, the gate voltage of the pHEMT is biased near zero volts (wide open channel, maximum current conduction) with a drain current bias close to I_{DSS} . This bias point will allow the gate voltage to swing from zero to pinch-off, as illustrated in Figure 2.7. This region of operation has been shown [7, 11, 14] to have similar performance as that of a doubler operating in pinch-off. However, due to a high gate voltage bias, the doubler circuit will be involved with higher dc drain current which yields lower DC to RF

Figure 2.7: I_{DSS} bias (region I, forward conduction) [14].

efficiencies. As well, there is a higher risk of device failure due to current spikes at the gate [7, 14]. Based on these drawbacks, the present design discussed in this thesis will focus on device bias in the pinch-off region for frequency doubling.

2.5.2 Region II: Pinch-off

The proper bias point for a class B multiplier is in the vicinity of pinch-off which generates an approximate half-wave sinusoidal current rich in even harmonics. Figure 2.8 illustrates the pinch-off bias waveforms. The pHEMT turn-on voltage is defined by the threshold voltage, V_t , which allows the transistor's channel to conduct during the positive half of the gate excitation

Figure 2.8: Pinch-off bias (region II) [14].

cycle. As a result, the drain conducts in pulses with the shape of a rectified cosine as shown in Figure 2.8. The amount of time a pHEMT is turned-on is referred to as duty cycle. The duty cycle of the drain current pulses varies with the gate bias voltage, V_{gg} . If the gate is biased at the threshold voltage V_t , the duty cycle is 50 percent, but if $V_{gg} < V_t$ the device is turned off over most of the excitation cycle, therefore the duty cycle is less than 50 percent.

Figure 2.9 shows that from gate excitation, the drain current peaks at the value I_{max} . Based on the theory by [11], the current pulses have a period of T and time duration of t_0 , where t_0 is $< T/2$. Therefore, when the drain current is maximum, $t=0$, and can be represented by the Fourier-series containing only cosine components:

$$I_d(t) = I_0 + I_1 \cos(\omega_p t) + I_2 \cos(\omega_p t) + I_3 \cos(\omega_p t) + \dots \quad (2.5.1)$$

where I_n is the n^{th} harmonic current. For $n \geq 1$, the current can be written as:

$$I_n(t_0) = I_{\max} \frac{4t_0}{\pi T} \left| \frac{\cos(n\pi t_0 / T)}{1 - (2nt_0 / T)^2} \right| \quad (2.5.2)$$

In order for the frequency doubler to achieve optimum performance, the second harmonic output current I_2 must be maximized. Equation (2.5.2) shows that I_2

Figure 2.9: Voltage and current waveforms in the ideal active frequency multiplier [11].

can be maximized by varying t_0/T or known as the conduction period. Figure 2.10 shows a plot of I_n/I_{max} as a function of conduction period for $n=2$ to 4 based on (2.5.2). It appears that for $n=2$, the optimum conduction period is 0.35. This can be achieved by adjusting the gate bias voltage V_{gg} below the threshold voltage V_t so that the drain current has the desired short period of conduction.

Figure 2.10: Harmonic drain current components as a function of conduction period [11].

However, two problems exist when attempting to achieve a short conduction period. According to [11, 14], the first problem arises when V_{gg} is made much below V_t . This creates a large magnitude of the peak reverse gate voltage that maybe much greater than the avalanche voltage of the device, causing breakdown. Secondly, by biasing it below the threshold voltage, greater

input power is required to produce a wide gate voltage variation which leads to poor multiplier conversion gain. Therefore, it is necessary to use a conduction period that is greater than the optimum. As part of the design process of a frequency doubler, it will be necessary to select the proper bias to achieve an acceptable trade-off between conversion gain and second harmonic output power.

The minimum conduction period for a given device is given by:

$$\theta_t = 2 \cos^{-1} \left(\frac{2V_t - V_{g \max} - V_{g \min}}{V_{g \max} - V_{g \min}} \right) \quad (2.5.3)$$

where $V_{g \max}$ and $V_{g \min}$ are the maximum and minimum peak gate voltages of the device respectively. The maximum and minimum voltages establish limits of conduction. The bias voltage that achieves this conduction period θ_t is:

$$V_{gg} = \frac{V_{g \min} + V_{g \max}}{2} \quad (2.5.4)$$

2.5.3 Gate and Drain Terminations

For a frequency doubler, the input circuit should be matched to the active device at $f_0 = \omega_0/2\pi$ so that maximum input power is delivered. The output circuit should be matched to deliver maximum output power at $2f_0$. By using a balanced topology, the fundamental frequency at the output should be mostly

rejected with only a minimal level of fundamental RF power in the drain current. In addition, since the balanced topology creates a virtual ground at f_0 at the output as seen in Figure 2.6, independent matching conditions can be established for odd and even harmonics. The matching requirements for a frequency doubler is similar those of a power amplifier with the exception that the desired output component is at $2f_0$ instead of f_0 .

Figure 2.11: Small input voltage swing resulting in a large distorted output swing with open circuit load line [13].

In addition to ensuring that the matching circuits are designed to deliver maximum input and output power to and from the device, consideration should also be made to maximize the desired second harmonic component. It has been demonstrated and reported by [13, 15] that the optimum output load at the fundamental frequency (f_0) that should be presented to the drain of the device is an open circuit shifted by the conjugate of the device's output capacitive

reactance. This was determined through a load-pull characterization of the device. The open circuit load line is demonstrated by [13] in Figure 2.11 where a small input voltage swing results in a very large distorted output swing.

Figure 2.12: Findings by [7] concluding that conversion gain is dependent on fundamental frequency load reactance.

The distortion is further enhanced when the device is biased near pinch-off. Further studies into output terminations by [7] conclude that the maximum possible second harmonic output power that can be produced is independent of fundamental frequency termination presented to the drain of the device. Figure

2.12 illustrates these findings that i) the RF conversion gain is dramatically dependent on fundamental frequency load reactance, and ii) the maximum second harmonic output power is relatively invariant. The observed dependence of conversion gain on fundamental frequency load reactance was concluded by [7] as a linear circuit effect due to parasitic feedback within the device, giving rise to conversion gain values that shoot off towards infinity as instability is approached at the fundamental frequency shown in Figure 2.13. Therefore it is obviously undesirable to achieve high gain at the expense of device instability. A similar device analysis will need to be performed for this thesis's doubler circuit so that the proper drain termination at the fundamental frequency can be appropriately designed to minimize this effect.

Figure 2.13: Findings by [7] show that high conversion gain is at the expense of circuit stability.

The choice of proper second harmonic input termination at the gate is also crucial to the optimum frequency conversion ability of the doubler circuit. Since the pHEMT is a bi-lateral device, a second harmonic RF signal can be fed back through the transistor and be re-amplified to destructively interfere at the output. It has been shown in works by [7, 11, 13, 14, 16] that the appropriate termination at the gate should be a short circuit at the second harmonic ($2f_0$). This can be achieved with the use of a quarter wavelength open circuited stub at $2f_0$.

2.6 Frequency Doubling Research

Many successful MMIC frequency doublers have been designed and their results published. These works include diode, FET and HEMT based multipliers, single-ended and balanced topologies, and microstrip and CPW implementations. Single-ended frequency doublers have been well described in literature [7, 13]. Balanced frequency doublers have also been well explored in literature [5, 17, 18, 19, 20], and they all incorporate the use of novel structure to establish a three-port network to achieve 180° input phase difference. Of the active frequency doublers reviewed thus far, all except one [5] achieves a conversion loss. As well, the doublers in [15, 17, 18, 19, 20] are implemented in CPW as hybrid or MMICs. Typical conversion loss in these works range from -0.5 to -12dB depending on the input frequency and have fundamental output signal rejection between 25-40dB. Of particular interest is the technique proposed by [17, 18] to achieve phase split using the properties of the CPW to slotline T-junction. Further discussion regarding the 180° coupler structure will be discussed in Chapter 3.

CHAPTER 3 *Transmission Line Technology*

3.1 Introduction

The selection of transmission line technology used in MMIC is an essential part of the design process. Early in this chapter, traditional microstrip technology is briefly discussed while the rest of the chapter is devoted to CPW. In Section 3.2, the advantages of CPW are highlighted. In Section 3.3, basic CPW and slotline theory are presented with suggested references for further detail analysis. In Section 3.4, CPW and slotline discontinuities like short and open circuits are reviewed while Section 3.5 presents traditional CPW stubs. In Section 3.6, a novel class of folded CPW shunt stubs is discussed. Finally, Section 3.7 reviews CPW transitions and T-junctions that are relevant to the balanced frequency doubler design.

3.2 Transmission Lines for MMIC

Traditionally, microstrip transmission lines are the preferred medium for MMIC circuits. Microstrip technology is one of the most popular types of planar transmission lines due to the ease of fabrication by photolithographic processes and they can be easily integrated with other passive and active microwave

devices. In addition, the electromagnetic behaviour of microstrip is well understood and many models have been developed [21]. Figure 3.1 illustrates the geometry and electromagnetic field lines of a microstrip line. The geometry of a microstrip line consists of a conductor of width W , which is printed on a thin grounded dielectric substrate with a thickness d and relative permittivity ϵ_r .

Figure 3.1: Microstrip geometry with electromagnetic field lines [21].

Increasingly, MMIC designers have been adopting the use of coplanar waveguide (CPW) technology to develop integrated circuits with higher degrees of integration. CPW was first proposed by [22], and it has even been suggested as an alternate to microstrip [24]. CPW is a planar transmission line, similar to a slotline structure with an additional third conductor centered in the slot region. Its principal advantage is that it is well suited for use with field effect transistors (ie. pHEMT) where RF grounding close to the device can be made. [24]

3.3 Uniplanar Waveguide

Transmission line structures where the ground is located on the same plane as the conductor are considered to be uniplanar. Both slotline and CPW fall into this category. The design of the frequency multiplier employs both of these types of transmission line structures and they will be examined in this section.

3.3.1 Coplanar

Coplanar waveguides are a type of planar transmission line, which are uniplanar in construction. Figure 3.2 illustrates the geometry of a CPW structure. This structure consists of a center strip conductor with semi-infinite ground planes on either side, all on a dielectric substrate with finite thickness. Note that a conventional CPW does not have a conductor underneath the substrate, and those that do are known as conductor-backed CPW (CBCPW). In a practical MMIC, the coplanar ground planes are made of finite extent. The use of CPW at microwave and millimeter wave frequencies in MMIC offers several advantages over traditional microstrip:

- The uniplanar structure offers simplified fabrication [25]
- Eliminates the need for via holes and the inherent parasitic inductance [26, 27]

- Reduces dielectric and radiation loss [26, 28]

Furthermore, since a ground plane exists between any two adjacent lines (center conductors), cross talk effects are very weak [26]. This beneficial property allows MMICs to have higher density than those designed using microstrip, thus reducing overall production costs [29].

Figure 3.2: Coplanar wave guide transmission line, with a center strip conductor and two ground planes on either side [21].

Compared to microstrip, CPW does have some disadvantages. They include: poor thermal handling properties due to the lack of via-holes and a backside process that contributes significantly to heat removal of active devices [30], and the possible excitation of unwanted modes at asymmetric discontinuities [28]. But due to the technical advantages of CPW over microstrip, especially at microwave and millimeter wave frequencies, this thesis will focus on the use of CPW for its design.

3.3.2 Conventional Coplanar Waveguide (CPW)

Like microstrip, a CPW structure supports a quasi-TEM mode of wave propagation. Transverse electromagnetic (TEM) waves exist on transmission lines that consist of two or more conductors and are characterized by the lack of

Figure 3.3: CPW field components: (a) magnetic-field distribution, (b) electric field distribution [25].

longitudinal field components. Figure 3.3a and 3.3b illustrates the quasi-static electric and magnetic field components that exist in a CPW structure. A CPW has most of its field lines in the dielectric region, concentrated between the center conductor and the ground planes on either side. However, some fraction of the fields will be in the air region above the substrate. For this reason, a pure TEM wave cannot be supported since the phase velocity, given by:

$$v_{ph} = \frac{c}{\sqrt{\epsilon_{eff}}}, \quad (3.2.1)$$

of the TEM fields in the dielectric region would be different from the phase velocity of the TEM fields in the air region (where $v_{ph}=c$ since $\epsilon_{eff}=1$).

The quasi-TEM mode of propagation supported by CPW has low dispersion, which allows for the potential of wide-band circuits [25]. In addition, CPW has lower dielectric loss compared to microstrip since the fields are mostly split between air and the dielectric, as opposed to microstrip where the fields are mostly contained within the dielectric below the line [31].

The characteristic impedance (Z_0) of CPW can be found using techniques and formulas found in [32]. The analytical expressions for ϵ_{eff} and Z_0 presented in [32] are:

$$\epsilon_{eff} = \frac{C}{C_0}, \quad (3.2.2)$$

$$Z_0 = \frac{1}{Cv_{ph}}, \quad (3.2.3)$$

where C is the capacitance per unit length of the CPW line and C_0 is the capacitance per unit length of the line in the absence of dielectric substrates. It can be seen from these expressions that the characteristic impedance is governed by the substrate dielectric constant and the unit capacitance of the line. Furthermore, [32] has shown that the unit length capacitance is dependent on the geometry of the CPW line, governed by the following two arguments:

$$k = \frac{c}{b} \sqrt{\frac{b^2 - a^2}{c^2 - a^2}}, \quad (3.2.4)$$

$$k' = \sqrt{1 - k^2} = \frac{a}{b} \sqrt{\frac{c^2 - b^2}{c^2 - a^2}}, \quad (3.2.5)$$

where the variables a , b , and c are geometric dimensions shown in Figure 3.4. It can be seen that multiple geometric CPW dimensions can yield the same characteristic impedance, which gives a circuit designer great flexibility when using CPW. The theory and formulas behind determining CPW characteristic impedance are all incorporated into a design software program called "Linecalc".

3.3.3 CPW Coupling

An advantage of using CPW is the ability to design lower cost MMICs. Small chip area contributes to one aspect of this cost saving. CPW allows circuits to achieve higher density because coupling between neighbouring transmission

Figure 3.4: Geometric dimension of finite ground plane CPW [25].

lines is much lower than that of microstrip. However, this coupling between neighbouring lines can contribute to losses in the circuit. Therefore, it is important for this coupling to be minimized when using CPW. An analysis of CPW coupling in MMIC's was performed by [34] which determined the minimum distance requirements between neighbouring CPW transmission lines for the best performance. The spacing between center conductors versus coupling from the study is summarized below:

- $a/d=0.5$ $k < -16\text{dB}$
- $a/d=1$ $k < -22\text{dB}$
- $a/d=2$ $k < -30\text{dB},$

where a is the distance between neighbouring lines, $d = w + 2s$ ground to ground spacing as shown in Figure 3.5 and k represents the maximum coupling coefficient defined in classical directional-coupler theory [21]. The conclusions from this study will be further discussed in Chapter 4 where detail doubler circuit design will be examined.

Figure 3.5: Coupling between adjacent CPW lines [34].

3.3.4 CPW Analysis

The objective of this thesis is to incorporate the use of CPW transmission lines in its design with an understanding of CPW behaviour and limitations. For further detail analysis of CPW impedance, dispersion, and losses using different numerical techniques, they can be found in works by [22, 34, 35, 24, 36, 37, 38, 39, 40, 41, 42, 43].

3.3.5 Slotline

The basic slotline configuration is shown in Figure 3.6 and it consists of a narrow slot etched in the metallization on one side of the dielectric substrate. Like CPW, the other side of the substrate is without metallization. Figure 3.7 illustrates the approximate field distribution in a slotline.

Various slotline analysis methods have been proposed and are discussed in [44]. As well, slotline characteristic impedance is examined in [44]. Like CPW, the objective of this thesis requires an understanding of slotline behaviour and limitations. Detail analysis can be found in works highlighted by [44].

Figure 3.6: Slotline geometry [44].

Figure 3.8: Field distribution of slotline [44].

3.4 Discontinuities

The use of discontinuities is an integral part of practical CPW MMIC circuits. It is essential to have a good understanding of their circuit behaviour for successful designs. Discontinuities can cause signal power loss due to the conversion of the desired CPW mode to other parasitic modes. For the frequency doubler, we will examine open ended, short ended, step change, right angle bend and T-junctions CPW discontinuities. In addition, we will also examine two slotline discontinuities employed in the design.

3.4.1 CPW Open Circuit

A CPW open circuit is shown in Figure 3.8a, and is formed by terminating the center conductor a short distance before the slot ends. The gap formed by the center conductor and the ground plane conductor creates an electric field that gives rise to a capacitive reactance, and is shown in Figure 3.8b. The formulas to determine the open circuit capacitance are discussed in [25]. Guidelines for an open circuit discontinuity can be found in [45].

3.4.2 CPW Short Circuit

A CPW short circuit is shown in Figure 3.9a, and is formed by ending the slots abruptly. An inductive reactance is formed by stored energy due to the RF currents that flows around the end of the slots. This inductance, shown in

Figure 3.8: CPW Open: (a) layout of open discontinuity, (b) capacitance representing open gap [25].

Figure 3.9b, is analytically examined in [25]. Guidelines for a short circuit discontinuity can be found in [45].

Figure 3.9: CPW Short: (a) layout of CPW short circuit discontinuity, (b) inductance representing the discontinuity at the short [25].

3.4.3 Air-Bridges and Right Angle Bend

CPW circuits with discontinuities give rise to mode conversion which is a serious problem that results in additional insertion/return loss [25]. Air-bridges are a simple method to alleviate this problem. An air-bridge is formed by an elevated metal strip that connects the ground planes on either side of the center conductor, therefore maintaining electrical continuity between the ground planes of the circuit. By placing air-bridges very close to the discontinuities, parasitic modes (i.e. slot line) can be suppressed.

Figure 3.10 illustrates a right angle CPW bend employing the use of air-bridges. According to [25], the 90° right angle bend will suffer in performance degradation caused by parasitic reactance from the bend itself and parasitic capacitance from the addition of air-bridges. To compensate, it has been suggested by [46] that the corners can be chamfered by an optimal amount. However, studies performed by [47] suggest that better performance can be achieved by optimizing the air-bridge itself than mitering the corners.

Figure 3.10: CPW Right angle bend with the use of air-bridges [25].

For the foundry process used in this thesis, conducting tunnels are used instead of air-bridges. The OMMIC process consists of many different metal layers. By utilizing a second metal layer (BE) beneath the main conducting layer (IN), conducting bridge crossings can be formed. Examples of this can be found

in Chapter 4. The BE and IN metal layers are separated and isolated by a $1\mu\text{m}$ thick dielectric.

3.4.4 CPW T-junctions

The use of T-junctions is necessary in most CPW circuits. Since a T-junction contains several discontinuities, the simplest way to suppress mode conversion is to employ the use of air-bridges as shown in Figure 3.11. T-junction equivalent circuit models and transmission coefficients can be found in [25].

Figure 3.11: CPW T-junction with air-bridges [25].

3.4.5 Slotline Short End

A slotline short end is shown in Figure 3.12. The short circuit end is created by terminating the slot by filling the slot (with a conducting surface lying

in the slot plane). The end result of the short end is an equivalent dominant inductive reactance. A detail analysis can be found in [44].

Figure 3.12: Slotline short circuited end [25].

3.4.6 Slotline Open End

Two different slotline open ends are shown in Figure 3.13. The most practical open end is obtained by means of a circular disc type opening. Since the slotline termination is an open circuit, it is capacitive in nature [44]. In the circular open end shown in Figure 3.13a, the larger the radius the better the open circuit is. Similar open circuit performance can be achieved with the open end shown in Figure 3.13b. However, the main advantage of this combination of a flared slot and half disc is that it requires less surface area to achieve the same open circuit performance [48].

Figure 3.13: Slotline open ends: (a) Circular open circuit, (b) flare/half disc open circuit [44].

3.5 CPW Stubs

Series and shunt CPW stubs are essential transmission line elements in MMIC circuit design. Stubs provide capacitive and inductive reactances as a function of length and geometry.

3.5.1 Open Circuited CPW Series Stub

Based on the open circuit discontinuity described in Section 3.4.1, an open circuited CPW series stub is formed by an inter-digital structure in the center conductor shown in Figure 3.12a. An open circuited series stub can be modeled as a series capacitance, shown in Figure 3.12b. It has been shown by [25] that the capacitance increases linearly with the length of the stub, and decreases when the width of the stub increases. There are limitations to this series equivalent model and are further discussed in [49].

Figure 3.12: (a) CPW series open circuit stub, (b) stub equivalent circuit [25].

3.5.2 Short Circuited CPW Series Stub

Similarly, the a short circuited CPW series stub consists of an inter-digital structure terminated in a short circuit discontinuity as described in Section 3.4.2. Figure 3.13a illustrates a short circuited series stub. According to [50], the stub can be characterized by a series resistance and a series inductance as shown in Figure 3.13b. Limitations to this equivalent circuit model are discussed further in [25]. Experimentally, it has been shown by [50] that the resistance and inductance is a function of the length, and they increase as the length of the stub increases. Also, the resistance and inductance decrease as the width of the stub increases.

Figure 3.13: (a) CPW series short circuit stub, (b) stub equivalent circuit [25].

3.5.3 Open Circuited CPW Shunt Stub

An open circuited CPW shunt stub is shown in Figure 3.14a, where an asymmetric stub is printed in the CPW ground plane. Additional air-bridges are required to suppress the parasitic coupled slotline mode. To maintain coplanar symmetry, the stubs can be printed on each side of the ground plane as shown in Figure 3.14b. Air-bridges are employed to suppress undesired modes. When the lengths of the stubs are electrically small [25], they can be modeled as a shunt capacitor, shown in Figure 3.14c. Full analysis of this structure can be found in [51, 52].

Figure 3.14: CPW Shunt Open Stubs: (a) asymmetric, (b) symmetric, (c) equivalent shunt capacitance representing the open stub [25].

3.5.4 Short Circuited CPW Shunt Stub

Similarly, a short circuited CPW shunt stub is shown in Figure 3.15a, where the stub is printed in the CPW ground plane. When the lengths of the stubs are electrically small [25], they can be modeled as shunt inductance, as shown in Figure 3.15b. Full analysis of this structure can be found in [51, 52].

Figure 3.15: CPW Shunt Short Stubs: (a) asymmetric, (b) symmetric, (c) equivalent shunt capacitance representing the short stub [25].

3.6 Novel CPW Shunt Stubs

It has been shown so far that CPW allows for great flexibility and offers wide scope of innovation in uniplanar technology. One of the main objectives of this thesis is to incorporate innovative coplanar techniques into the frequency doubler's design. In recent years, a new class of novel and compact CPW shunt stubs patterned into the center conductor has been developed by [52] at the Communications Research Centre (CRC) in Kanata, ON. These structures have been demonstrated to improve the performance and increase the flexibility of the existing CPW elements. Therefore, this thesis attempts to incorporate these innovations in its design.

3.6.1 Center Patterned CPW Shunt Stubs

Until [52] proposed these innovative structures, only CPW series stubs have been implemented in the center or coplanar ground conductor [49]. As shown in Section 3.5, CPW shunt stubs have been typically formed in the ground conductor. A new class of CPW shunt open and short circuited stubs folded into the center conductor is shown in Figure 3.16 and Figure 3.17 respectively. The analogous stubs formed in the ground plane are also shown in the figures. The folded structure is formed by introducing a thin strip of ground across the CPW and the inner conductor is connected across this ground with the use of air-bridges. Stubs are then formed inside the center conductor using the

Figure 3.16: Novel center patterned open shunt stub [25].

Figure 3.17: Novel center patterned short shunt stub [25].

new virtual ground. These new proposed stubs by [52] offer several advantages over conventional shunt stubs:

- greater field confinement due to the stubs printed in the center conductor which leads to lower radiation loss
- compactness
- reduction of the number of air-bridges in the case of an asymmetric CPW shunt stub which are expensive to build

Testing of these center patterned CPW shunt stubs have been performed by [52] to show strong agreement with conventional CPW shunt stubs.

3.6.2 Multi-Stubs Configuration

Building on the concepts introduced in [52], a new miniaturizing technique has been proposed in [53] to integrate CPW series stubs within the center conductor of the same CPW section as shown in Figure 3.18. The ideal

equivalent circuit of two open circuit series CPW stubs is illustrated in Figure 3.18a. Normally, cascading two conventional CPW open circuit series stubs is very large in configuration as shown in Figure 3.18b. Therefore, by applying a miniaturizing technique to such a structure is highly desirable. Figure 3.18c illustrates both open circuit CPW series stubs integrated within the center strip. The proposed overlapping by [53] is entirely responsible for major size reduction.

Figure 3.18: Novel multi-series open stubs: (a) equivalent transmission line circuit, (b) traditional implementation of CPW multi-series open stubs, (c) compact structure with series stubs folded into the center conductor [53].

In addition, [53] expands on the overlapping series stub configuration by applying the same concept to CPW shunt stubs. Figure 3.19a illustrates the ideal equivalent short circuit CPW shunt stubs, while Figure 3.19b shows how these stubs are implemented conventionally. Finally, Figure 3.19c shows the overlapping technique being applied to achieve major size reduction.

This attractive technique increases design freedom and allows for CPW structures to be implemented in MMICs with higher integration densities.

Further novel structures based on this concept can be found in works by [52, 53].

Figure 3.19: Novel multi-series shorted stubs: (a) equivalent transmission line circuit, (b) traditional implementation of CPW multi-series shorted stubs, (c) compact structure with series shorted stubs folded into the center conductor [53].

3.7 Transitions and Junctions

A major advantage of using CPW in MMICs is the ability to integrate with other uniplanar transmission lines. Therefore it is essential to have suitable transitions. One of the most common transitions is from an unbalanced CPW to a balanced slotline. Comprehensive studies of this type of transition have been previously published [17, 54], and will be discussed in the following section. In addition, slotline-CPW junctions are examined and their application to this thesis will be discussed.

3.7.1 Slotline-CPW Junctions

Figure 3.20 illustrates the four types of T-junctions that can be realized between CPW and slotline. In addition, the electric fields are shown to illustrate the mode transformation. Of interest to this thesis is the T-junction shown in Figure 3.20c proposed by [55]. The figure illustrates a three-port network structure with a slotline transmission line as input and CPW transmission line as

Figure 3.20: Different types of CPW and Slotline T-junctions: (a) CPW to CPW, (b) CPW to slot, (c) slot to CPW, (d) slot to slot [44].

outputs. In addition, a quarter-wave short circuit slotline stub is placed in the middle to provide an open circuit at the frequency of interest, while shorting out other frequencies. Due to the configuration of slotline-to-CPW, the unbalanced

electric fields of the CPW lines are 180-degrees out of phase. The equivalent transmission line circuit for this configuration is shown in Figure 3.21, which shows a slotline input in series with the CPW outputs. Further analysis of this T-junction and its equivalent circuit can be found in Chapter 4.

Figure 3.21: Equivalent transmission model of slotline to CPW T-junction [44].

An objective of this thesis was to design a frequency doubler using the balanced topology discussed in Chapter 2. Therefore, by incorporating a slotline-CPW T-junction into the circuit design, a balanced (180-degrees out of phase) input signal can be achieved. The next section will examine how a slotline transmission line can be implemented in conjunction with CPW technology.

3.7.2 CPW to Slotline

Various transitions have been proposed and examined by [17, 54, 56, 57, 58, 59] and are illustrated in Figure 3.22. Details of each transition design can

be found in [44]. The general theory for these transitions is based on the fact that there needs to be a complete transfer of current from the unbalanced end (CPW) to the balanced end (Slotline). Using Figure 3.22c as an example, the currents at the CPW end have equal magnitude but opposite in direction and flow along the center conductor and the CPW ground planes on both sides. By placing a short circuit a quarter-wave length away between the center strip and the ground plane, an open circuit is presented at the transition. This forces all the currents of the unbalanced end (CPW) to flow between the center conductor and the remaining ground plane. In addition, an air-bridge is employed across the transition to allow the backward current on the CPW ground planes to flow from one conductor to the other conductor of the slotline. The combination of an open circuit and the air-bridge help transform the CPW mode into the slotline mode.

The CPW to slotline transition is a fundamental passive component in MMICs. It is imperative for the transition to have good topology so that it does not degrade the overall performance of the circuit. The properties of this transition have been a topic of considerable interest and applications in antenna, balanced mixer and multiplier circuits highlighting the use of this transition can be found in [55, 58, 60, 61]. Furthermore, new research into increasing the bandwidth of CPW to slotline configurations has been the subject of many papers [54, 56, 62]. The challenge is to design compact transition topologies while

achieving low loss that can be integrated into MMIC applications. Further analysis into the use of the CPW-to-slotline transition in combination with the slotline-CPW T-junction discussed in the previous section will be discussed in Chapter 4.

Figure 3.22: Various CPW to slotline transitions [44].

CHAPTER 4 *Design and Analysis of the Multiplier Circuit*

4.1 *Introduction*

A successful frequency doubler circuit will require careful design considerations. The use of circuit design tools and electromagnetic simulators will assist the design process. This chapter will cover the entire balanced frequency doubler circuit design analysis. In Section 4.2, the fabrication process used by the foundry for the circuit will be briefly discussed. In addition, the software used for the design analysis is highlighted. In Section 4.3, an analysis on pHEMT size is presented. Section 4.4 describes the use of a load-pull analysis to determine optimal loads. Device and circuit stability are analyzed in Section 4.5. In Section 4.6, termination at the gate of the pHEMT is discussed. In Section 4.7, an ideal balanced frequency doubler is presented and the performance results are shown. In Section 4.8, CPW circuits are analyzed and simulated. Finally, in Section 4.9, the design of the CPW 180° coupler is discussed and complete CPW simulation results of the doubler circuit are presented.

4.2 Fabrication Technology and Models

The 19 to 38GHz balanced frequency doubler was designed with the assistance and resources of the MMIC group at the Communications Research Centre (CRC), in Kanata, Ontario. In addition to technical and computing support, CRC provided access to the OMMIC foundry's ED02AH fabrication process technology, which was developed specifically for microwave applications up to millimeter wave frequencies. The main features of this technology include:

- Hetero-epitaxy with a pseudomorphic (GaInAs) active layer
- Enhancement and depletion mode transistors
- 0.2 μm gate length

Similar to the epitaxial layer structures described for a generic pHEMT in Chapter 2, Figure 4.1 illustrates the active layer profile of the OMMIC pHEMT device. From here on, all design analysis of the frequency doubler circuit including transmission lines, active and passive device elements are based on the OMMIC process technology and models.

Figure 4.1: Epitaxial structure of OMMIC's ED02AH fabrication process [68].

4.2.1 ADS and Momentum

For the design analysis of the doubler, Agilent Technologies' Advanced Design System (ADS) was used as the primary circuit simulation design tool. ADS transistor models of the ED02AH process were provided by OMMIC for this purpose. In addition, all coplanar structures were simulated with the aid of the ADS electromagnetic simulation software Momentum. Momentum is a two-dimensional electromagnetic field analysis simulator that solves for s-parameters using the Method of Moment. Since conventional CPW models of passive structures do not exist, and due to the custom nature of the circuit, it was necessary to perform design analysis using Momentum.

4.3 Device Selection

An objective of the frequency doubler design is to maximize second harmonic generation output at 38GHz. Therefore, proper pHEMT device selection was necessary. Based on the frequency multiplication theory outlined in Chapter 2, simulations were performed to determine the optimal number of gate fingers, unit width of gate fingers and the bias points.

4.3.1 Gate Bias

Since the frequency doubler will be biased in the vicinity of pinch-off, the depletion type pHEMT will be selected for purposes of this design. A depletion type device has a channel that gets smaller or is pinched-off when a reverse gate bias is applied and will conduct maximum current with a zero bias. Based on data provided by the foundry, the pHEMT threshold voltage is $V_t = -0.9V$. Using the large signal nonlinear transistor model "fED2ONI2" with default gate width $w_g = 15\mu m$ and gate fingers $n_{bf} = 6$, the DC characteristics of the device is plotted in Figure 4.2 and 4.3. The device was arbitrary biased with a drain voltage $V_d = 3V$. From simulation results, the threshold voltage $V_t = -0.9V$ was verified to have almost zero current (device pinch-off). Using equation 2.5.3 and the device limitations provided by the foundry, the minimum conduction angle was determined to be:

$$\theta_i = 2 \cos^{-1} \left(\frac{2V_i - V_{g \max} - V_{g \min}}{V_{g \max} - V_{g \min}} \right) = 2 \cos^{-1} \left(\frac{2(-0.9) - 1 - (-6)}{1 - (-6)} \right) = 125.6^\circ \text{ (or 0.35)}$$

Figure 4.2: DC Characteristics of 6x15 μ m pHEMT, Drain current vs. Drain Voltage.

Figure 4.3: DC Characteristics of pHEMT. Drain current vs. Gate Voltage.

From Figure 2.9, a conduction period of 0.35 is optimal for maximum second harmonic current. According to equation 2.5.4, to achieve a conduction angle $\theta_t = 125.6^\circ$, the gate must be biased at:

$$V_{gg} = \frac{V_{g \min} + V_{g \max}}{2} = \frac{-6 + 1}{2} = -2.5V$$

Biasing the pHEMT at a voltage much below the threshold will encounter the problems discussed in Chapter 2, in this case, mainly a requiring a large gate voltage variation which leads to poor multiplier conversion gain. Therefore, in order to determine the optimal bias point, we must investigate the device's ability to generate second harmonic output power at 38GHz.

The circuit shown in Figure 4.4 consists of a common source pHEMT with ideal RF chokes at the gate and drain bias lines and ideal DC blocks at the input and output. The device is terminated with a 50Ω load. The input consists of a swept power source at a fundamental frequency of 19GHz. A simulation was performed to measure the maximum conversion gain and maximum output power at 38GHz with gate bias voltage $V_{gs} = -1.4$ to -0.3 V. Conversion gain is defined as the ratio between second harmonic output power and fundamental input power. Figure 4.5 and 4.6 illustrate the results obtained. It can be seen that the conversion gain reaches a maximum at $V_{gs} = -0.6$, while output power at 38GHz decreases as the gate bias is increased. Therefore, improving conversion gain comes at the expense of a decrease in second

Figure 4.4: Common source pHEMT circuit in Harmonic Balance testbench.

Figure 4.5: Maximum conversion gain vs. gate bias for default pHEMT at 38GHz.

Figure 4.6: Second harmonic output power vs. gate bias for default pHEMT at 38GHz.

harmonic output power. According to foundry data, the pHEMT model is valid for DC gate bias voltages $-1.2\text{V} < V_{gs} < 0.6\text{V}$. Using $V_{gs}=-1.4\text{V}$ as the baseline for comparison, the improvement in conversion gain (in dB) is greater than the loss of second harmonic power until $V_{gs}=-0.8\text{V}$. For example, at $V_{gs}=-1.1\text{V}$, conversion gain is improved by 0.805dB while second harmonic output power decreases by 0.634dB. Therefore, it is reasonable to increase the gate bias voltage until the increase in gain is approximately equal to the loss in output power. For $V_{gs} > -0.8\text{V}$, the loss of power at 38GHz is greater than the improvement in conversion gain. Note that the input and output s-parameters were observed while changes were made to V_{gs} . Although changes in gate bias voltage will change the device parasitics which could affect gain and power output, it was observed that the s-parameters varied very slightly, approximately by 0.2dB for $-1.2\text{V} < V_{gs} < 0.6\text{V}$. In addition, $V_{gs}=-0.8\text{V}$ is a bias in the vicinity of pinch-off ($V_t=-0.9\text{V}$), which agrees with findings by [7, 11, 14]. However, the design tradeoff is that the conduction period shown in Figure 2.9 is no longer 0.35, but slightly greater than 0.5. From this analysis, the gate bias voltage was determined to be optimal at $V_{gs}=-0.8\text{V}$.

4.3.2 Drain Bias

The design of the 19 to 38GHz frequency multiplier is based on Class B operation as discussed in Chapter 2. In addition, a reactive load will be

presented to the drain of the pHEMT. According to [63], the drain supply voltage for Class B operation is:

$$V_s = \frac{V_{dgB} - 2|V_t| + V_k - V_\Phi}{2}, \quad (4.2.1)$$

where V_{dgB} is the maximum drain voltage before breakdown, V_k is the knee voltage and V_Φ is the diode voltage. From the device limits provided by the foundry in Appendix A and using equation 4.2.1, the drain bias voltage was determined to be $V_s=3V$.

4.3.3 pHEMT Size

In addition to proper biasing, the pHEMT itself should be selected for optimal second harmonic generation. The device can have $n_{bd}=2, 4, 6$ or 10 fingers and a gatewidth $10\mu m \leq w_u \leq 50\mu m$. Outside of these limitations will yield the following effects according to the foundry:

- sources in the middle of the pHEMT are not correctly grounded
- drain and gate accesses are long
- there is a phase shift between the gate fingers

With these guidelines in mind and based on the previous analysis for gate biasing, simulations were performed to determine the optimal number of gate fingers and gate width. Figure 4.7 and 4.8 illustrate the conversion gain and

Figure 4.7: Conversion gain vs. pHEMT gate width.

Figure 4.8: Second harmonic output power vs. pHEMT gate width.

Figure 4.9: Layout of 4x33 pHEMT device with dual sources.

second harmonic output power with an input RF signal of 8dBm at 19GHz (where maximum conversion gain occurred for the given bias in Figure 4.5). It can be seen in Figure 4.7 that maximum conversion gain occurs at $n_{bd}=2$ and 4 with a gate width of $w_g=55\mu\text{m}$ and $33\mu\text{m}$ respectively. Since $w_g=50\mu\text{m}$ is at the limit of the device model, it is desirable select a pHEMT size of $n_{bd}=4$ fingers and $w_g=33\mu\text{m}$ gate width. In addition, a device with shorter unit gatewidth will have less signal loss at 19GHz and lower gate parasitic resistance [63]. The same trends can be observed for second harmonic output power shown in Figure 4.8.

In summary, based on the above analysis for optimal second harmonic generation, the OMMIC pHEMT device will be biased at $V_{gs}=-0.8V$ and $V_{ds}=3V$, and have $n_{bd}=4$ fingers with $w_u=33\mu m$ unit gatewidth. In addition, all OMMIC pHEMT devices have two sources as illustrated by the layout in Figure 4.9.

4.3.4 Output Capacitance

From the theory presented in Chapter 2, the optimum load that should be presented to the drain is an open circuit shifted by the conjugate of the device's output capacitive impedance at $f_0=19GHz$. To determine the output capacitance of the pHEMT, the $4 \times 33\mu m$ small signal model was used and the bias was set to $V_g=-0.8V$ and $V_{ds}=3V$. Figure 4.10a illustrates the circuit and Figure 4.10b illustrates the S_{22} measurement on a Smith chart at 19GHz. From the Smith chart, the conjugate reactance would be $+j3.047 \bullet Z_0$. This will be used later to determine the necessary length of transmission line required to connect the outputs of the two pHEMTs.

Figure 4.10: Output capacitance: (a) small signal circuit, (b) S₂₂ measurement of the circuit.

4.4 Harmonic Load-Pull

As part of the design process, it was necessary to characterize the pHEMT. A harmonic load-pull was performed in ADS based on the 4x33um large-signal pHEMT model. The bias conditions were set to $V_{gs}=-0.8V$ and $V_{ds}=3V$ with $Z_0=50\Omega$. Normally, a load-pull is performed and the maximum deliverable power is extracted through 50Ω at the fundamental frequency. However, in the design of the frequency doubler, we wanted to determine the maximum deliverable power at the second harmonic, $2f_0=38GHz$. Figure 4.11a illustrates the load-pull circuit setup and Figure 4.11b illustrates the load-pull results. The simulation results indicated that for the given pHEMT and bias and in an input power of 8dBm, the maximum second harmonic output power was -5.45dBm and required a load reactance of $+j2.108 \bullet Z_0$ at $f_0=19GHz$. Note that the load reactance was slightly different from the conjugate of the output capacitive impedance as discussed in Section 4.3.4. From the load-pull results, if the load impedance was made to be $+j3.047 \bullet Z_0$, then the output power at 38GHz would be -11.269dBm.

From the harmonic load-pull simulation, it can be concluded that the drain should be presented with a load reactance of $+j2.108 \bullet Z_0$ to achieve maximum second harmonic output power.

Figure 4.11: Load-pull analysis: (a) circuit setup, (b) load results for maximum 2nd harmonic output power.

4.4.1 Equivalent Transmission Line

The 19 to 38GHz frequency doubler was designed in a balanced topology as discussed in Chapter 2. At the output combining point, there will be a virtual ground at 19GHz. Therefore it is necessary to rotate the virtual ground through a length of CPW transmission line to achieve the pure normalized reactance of $+j2.108$. Figure 4.12a illustrates the test circuit consisting of the output impedance of the device at terminal 1, followed by an ideal lossless transmission line and a ground. The S_{11} result from the S-parameter simulation at 19GHz is presented in Figure 4.12b. It shows the impedance seen by the device to have a pure reactance of $+j2.15$ normalized to 50Ω , which is approximately the desired reactance from the harmonic load-pull simulation. Therefore, a transmission line of 75Ω with an electrical degree of 71 at 19GHz will yield the desired fundamental load for maximum output power at 38GHz.

Figure 4.12: Equivalent transmission line: (a) simulation setup with ideal lossless transmission line, (b) S_{11} results to achieve the reactance desired.

4.5 Stability

The same theory relating to stability developed for amplifiers is applicable to analyze frequency multipliers. Positive intrinsic feedback in a pHEMT can occur, due to negative real impedance, and causing oscillations when associated with an external impedance and frequency. As a result, the circuit's stability and terminating impedances can be greatly affected. From the stability theory discussed in [11, 14, 21], a device's stability can be divided into two categories: unconditionally ($K > 1$ and $B > 0$) and conditionally ($K < 1$ or $B < 0$) stable.

4.5.1 Small Signal pHEMT Stability

Initial device stability was determined using the $4 \times 33 \mu\text{m}$ pHEMT small signal model at $V_{gs} = -0.8\text{V}$ and $V_{ds} = 3\text{V}$ with ideal DC blocks and RF chokes. The stability factor and measure were calculated for frequencies from 0 to 40GHz in ADS. Equations for the stability factor and measure can be found in [21]. Figure 4.13a shows the circuit setup and Figure 4.13b shows a plot of stability factor (K) and stability measure (B) versus frequency. From the plot, it appears that the device is unconditionally stable for frequencies greater than 15GHz.

In a balanced frequency doubler circuit topology, the drain bias line is connected to the circuit after the virtual ground at the output. Therefore, the

Figure 4.13: Stability analysis: (a) simulation setup of small signal pHEMT, (b) stability factor and measure plotted from 0 to 40GHz.

transmission line discussed in Section 4.4.2 should be included as part of the stability simulation. Figure 4.14a shows the device with an ideal transmission line of electrical length 71° and an impedance of 75Ω at the drain. Figure 4.14b shows the simulated stability results. The simulation shows no change in stability with the addition of the transmission line at the drain.

4.5.2 Gate and Drain Bias Line

In the small signal stability simulation, the bias lines are assumed to have ideal RF chokes. In addition, no DC blocks were included in the circuit setup. However, in the design of the frequency doubler, realistic RF chokes and DC blocks will be required.

Based on initial Momentum simulation of a 50Ω CPW transmission line on OMMIC's substrate, a quarter-wavelength at 19GHz was determined to be approximately $1800\mu\text{m}$ while at 38GHz was approximately $900\mu\text{m}$.

The balanced frequency doubler circuit should have almost zero RF signal at 19GHz after the drain connection point. Therefore, based on the quarter-wavelength results and factoring potential MMIC chip area, it was feasible to implement a RF choke at the drain line using a $\lambda/4$ transmission line of length $900\mu\text{m}$ at 38GHz. This would be followed by a capacitor of reasonable size to ground such that at 38GHz, it was seen as a short and an open after the $\lambda/4$

transmission line. Using the capacitor size calculator provided by the foundry, 6pF of capacitance can be achieved by using two 3pF SiN capacitors of $75\mu\text{m} \times 140\mu\text{m}$. This would be equal to approximately 0.52Ω at 38GHz, which is sufficient for the desired short. The implementation of the drain bias line is shown in Figure 4.14a.

At the gate bias line, it would be convenient to apply the same idea to create a choke for RF signals at 19GHz. However, a quarter-wavelength transmission line at 19GHz is too long to be practical. Therefore, an inductance of 6nH was used. At 19GHz, the inductance represents an impedance of approximately 716Ω , which would be sufficient to stop most RF signals leaking into the gate bias line. In addition, a 3pF capacitor was placed after the inductor to provide a short to any RF signals that manage to leak into the bias line. The implementation of the gate bias line is shown in Figure 4.14a.

DC blocking in the circuit is provided by the use of 5pF SiN capacitors at the gate input and drain output. Capacitance of this size can be achieved in a compact area, and providing a good short at RF and an open at DC.

4.5.3 Large Signal pHEMT Model Stability

Since the frequency doubler will be designed using the large signal pHEMT model, it was necessary to compare it against the small signal model in terms of

stability. In addition, ideal DC blocks were replaced with realistically sized capacitors and RF chokes. At the input and output, a 5pF SiN capacitor was used for DC blocking, which represented an impedance of 1.67Ω at 19GHz and 0.83Ω at 38GHz. The impedances represented a near short circuit to RF signals and an open circuit to DC signals.

Small signal conditions were initially simulated using the large signal pHEMT model as shown in the circuit in Figure 4.14a. The stability factor and measure were determined with an input RF power of -50dBm. The results are plotted in Figure 4.14b. It can be seen that the K and B values across the frequencies are different than those plotted in Figure 4.14b using the small signal pHEMT model. From the plot in Figure 4.14b, the circuit is unconditionally stable for frequencies greater than 33GHz. Therefore, it was necessary to implement stability structures to ensure unconditional stability at the desired frequencies of 19GHz and 38GHz.

4.5.4 Stability Structures

Based on the results shown in Figure 4.14b, stability must be improved at low to mid-band frequencies. To increase stability in low-band frequencies, a structure parallel to the drain and gate power can be added. This structure will consist of a resistor in series with a capacitor [64]. For mid band frequencies, a small amount of inductance can be added at the source to improve stability [65].

However, this is undesirable since any inductance at the source will dramatically decrease the gain performance of the pHEMT.

Figure 4.15: Unit circuit with drain stability structure.

Figure 4.15 illustrates the stability structure at the drain bias in parallel with the supply voltage. In the stability structure shown, it consists of a resistor R_d in series with a capacitor C_d , which provide input loading and impedance respectively at low frequencies [64]. With initial values of $R_d=50\Omega$ and $C_d=1\text{pF}$, the stability factor and measure were simulated under small signal conditions (RF input power of -50dBm) and plotted in Figure 4.16a and Figure 4.16b

respectively. Both values of K and B can be seen to have increased between 0 to 6GHz compared to the results without the stability structure.

Figure 4.16: Stability results with and without drain stability structure: (a) Stability Factor (K) plot, (b) Stability Measure (B) plot.

Further simulations were performed and the values of R_d and C_d were optimized to be 80Ω and 4pF respectively. Figure 4.17 shows the results of the stability factor and measure. Although improvements have been made at the low band frequencies, the circuit is still only conditionally stable at 19GHz .

Figure 4.17: Stability results with optimized drain stability structure.

Further stability improvement was examined and Figure 4.18 illustrates the addition of a stability structure at the gate bias in parallel with the gate supply voltage. The structure consists of a resistor R_g in series with a capacitor C_g . Stability simulations were performed and the values of R_g and C_d were optimized. Figure 4.20 shows a plot of K and B with optimized $R_g=80\Omega$ and $C_g=4\text{pF}$. From the results, the structures implemented at the gate and drain

have improved stability at the low frequencies. However, stability is still of concern at 19GHz.

Figure 4.18: Unit circuit with drain and gate stability structures.

At 19GHz, the device unit is conditionally stable, where $K < 1$ and $B > 0$.

Further analysis was performed by measuring the S_{11} and S_{22} at 19GHz and plotting the source and load stability circles. Figure 4.19a illustrates the value of S_{11} and the source stability circle on a Smith chart at 19GHz. Since S_{11} is greater than zero, the center region of the Smith chart is stable and all impedances presented to the drain would be stable up to the circular boundary of the source stability circle on the Smith chart. Similarly, Figure 4.19b illustrates the value of S_{22} and the load stability circle on a Smith chart at 19GHz. Since S_{22} is greater

Figure 4.19: Source and Load stability circles at 19GHz.

than zero, and the load stability circle lies outside the unit radius of the Smith chart, the circuit device is considered stable at 19GHz. Therefore, the gate can be matched with any positive impedance while the drain can be presented with the virtual short circuit of a balanced topology.

From Figure 4.20, $K > 1$ and $B > 0$ at 38GHz, therefore the device unit is unconditionally stable at the second harmonic output frequency.

4.5.5 Large Signal Stability Effects

So far, the stability analysis performed have been based on small signal conditions where RF input power was equal to -50dBm. Since the frequency doubler circuit will be operating with a large signal input, it was necessary to perform stability simulations with larger RF input powers. Figure 4.20a and Figure 4.20b show plots of stability factor and measure respectively. It should be noted that as RF input power increased, so did the values of K and B . From Figure 4.20, at RF input power greater than 0dBm, the circuit device unit is unconditionally stable across all frequencies.

From the above analysis, stability for the unit device circuit has been considered for both small and large signal conditions and stability structures were implemented to ensure stability at the frequencies of interest.

(a)

(b)

Figure 4.20: Large signal stability simulation results: (a) stability factor (K), (b) stability measure (B)

4.6 Reflected Second Harmonic Power

In a frequency doubling circuit, it is necessary to properly terminate second harmonic RF signals that are reflected back through the gate of the pHEMT. From the theory presented in Chapter 2, a short circuit should be presented to 38GHz at the gate. To achieve this short circuit, an open circuited quarter-wave length shunt stub could be employed. Figure 4.21a illustrates the circuit setup with power samplers to measure reflected RF power at 38GHz at the gate of the pHEMT. Figure 4.21b shows the reflected power at 38GHz versus input power at 19GHz. It can be seen from the results that at large input power levels, the reflected second harmonic power can be quite significant. As a result, the second harmonic RF signal can be amplified back through the pHEMT and potentially decrease the gain and power output performance of the doubling circuit.

To minimize the amount of reflected power, an ideal open circuited quarter-wavelength shunt stub at 38GHz was placed at the gate of the pHEMT. Figure 4.22 shows the amount of reflected second harmonic power can be reduced to below -180dBm (nothing) with the use of the shunt stub.

(a)

Reflected RF Power @ 38GHz

(b)

Figure 4.21: Measuring reflected power (38GHz) at the gate: (a) circuit setup, (b) reflected RF power at 38GHz vs. input power.

Figure 4.22: Reflected power plot with open shunt stub termination at the gate of the pHEMT.

4.6.1 Compact CPW Shunt Stubs

Based on the CPW shunt stub miniaturization concepts presented in Chapter 3, we can utilize a similar CPW topology to create the proper termination at the gate for reflected second harmonic power.

Figure 4.23a illustrates a typical shunt $\lambda/4$ open circuit CPW stub implemented in the ground plane along with its equivalent circuit model. As suggested by [52], the shunt stub can be folded into the center conductor to maintain symmetry transversely as shown Figure 4.23b. However, the

Figure 4.23: CPW open circuit shunt stubs: (a) traditional stub printed in ground plane, (b) new class of shunt stub folded in the center conductor [25].

amount of space taken up by the stub is still $\lambda/4$ at 38GHz. To reduce the shunt structure further, loading techniques proposed in [66, 67] can be applied. By applying a series inductive loading to one end of the stub, the stub's length can be reduced. Figure 4.24 illustrates the ideal $\lambda/4$ open circuited stub. Figure 4.25 illustrates the shortened open circuited stub with a series short circuit stub to provide inductive loading. It can be seen that similar s-parameter performance can be achieved.

By applying the overlapping multiple CPW stub topology proposed by [53], a novel compact structure can be employed at the gate to suppress second harmonic reflected power. The series $\lambda/8$ short (series inductive loading) and open stubs can be folded into the center conductor to create a compact shunt CPW structure as shown in Figure 4.26a. Figure 4.26b shows the S_{21} and S_{11} Momentum results of the compact CPW structure implemented on the OMMIC

substrate. Note that it was only simulated up to 40GHz. The results of the compact CPW structure agrees well with the circuit structure created with ideal stub elements.

Figure 4.24: Ideal $\lambda/4$ open shunt stub at 38GHz: (a) circuit setup, (b) s-parameter results.

Figure 4.25: Reduced shunt stub with series inductive loading by series short circuited stub at 38GHz: (a) circuit setup, (b) s-parameter results.

(a)

CPW Shunt Multi-series Stubs

(b)

Figure 4.26: Compact CPW multi-series shunt stub: (a) design layout, (b) Momentum s-parameter simulation results.

Figure 4.27 shows the suppression results of the compact CPW structure inserted into the gate circuit shown in Figure 4.21a. The compact CPW structure manages to short RF power at 38GHz below -20dBm.

4.7 Ideal Balanced Frequency Doubler

At this point, a single ended frequency doubler has been considered. One objective of this thesis is to implement frequency multiplication in a balanced topology. Two single ended pHEMT circuits will be combined and appropriate matching networks will be designed. Conversion gain will be examined and novel designs for achieving out of phase input signals will be considered.

4.7.1 Balanced Topology

From the theory discussed in Chapter 2, a balanced frequency doubler consists of two single ended multiplying circuits in parallel. At the input, the circuits are connected by a 180° coupler such that the phase of the RF input signals at the gates of the pHEMT are 180° apart. At the output, the drains are connected to create a virtual short at the fundamental frequency, while constructively combining at the second harmonic. Figure 4.28a illustrates the balanced circuit based on the circuit described in the previous sections and the

Figure 4.27: Reflected power (38GHz) at the gate of the pHEMT with CPW multi-series shunt stub.

use of an ideal 180° hybrid coupler with 3dB loss. With no matching networks, a harmonic balance simulation was performed with input RF levels from -20dBm to +20dBm at 19GHz. Figure 4.28b and 4.30c show plots of conversion gain and output power respectively. From the conversion gain plot, it can be seen that a maximum is achieved at approximately 14dBm of input power with a conversion gain of -13dB. In addition, the virtual short at the output at the fundamental frequency created by the balanced topology suppresses the 19GHz output signal by >80dB below the second harmonic.

Figure 4.28: Ideal Balanced Frequency doubler circuit: (a) circuit schematic, (b) conversion gain and (c) fundamental and 2nd harmonic output power levels.

4.7.2 Load at Fundamental Frequency

From the load-pull analysis performed earlier, it was seen that the ideal load at the drain would be a transmission line of electrical length 71° at 19GHz. In an attempt to fine tune the load impedance, conversion gain was measured against the electrical line length at the drain with an input power of 15dBm as shown in Figure 4.29. It was interesting to see that higher conversion gain can be achieved with much shorter or longer transmission line lengths. In fact, it

Figure 4.29: Conversion Gain vs. load reactance provided by transmission line length at the drain.

appeared from the plot that the worst conversion gain was obtained at the determined electrical length of 71° . However, Figure 4.30 illustrates the problem with implementing the other loads. The figure illustrates a plot of the S_{11} at 19GHz looking into the pHEMT device after the 180° coupler and S_{22} at 38GHz at the output of the doubler circuit. When the transmission line at the drain is at certain electrical angles, the s-parameters are greater than 0dB. This indicates instability in the circuit due to positive impedance. Although stability was examined in Section 4.5, it was only of the unit device circuit consisting of the single ended doubler. By placing the two circuits together to form the balanced topology, feedback was potentially introduced. Similar results were examined in

[7] where depending on the fundamental load reactance presented to the output of the device, the conversion gain values shoot off as instability is approached. Therefore, the fundamental load reactance must be chosen carefully to ensure circuit stability while maximizing conversion gain.

To ensure stability at all input power levels, the original electrical length of 71° was decreased to 69° at 19GHz. Figure 4.31 plots the conversion gain using the 69° transmission line at 19GHz. The results show that the maximum conversion gain occurs at an input RF power of 13dBm.

Figure 4.30: S-parameters of pHEMT while varying the length of transmission lines at the drains.

Figure 4.31: Conversion gain results with drain transmission line length of 69° at 19GHz.

4.7.3 Matching networks

The next step in the analysis was to design the input and output matching networks. Input matching networks will be required on each of the two RF signal paths after the 180° coupler. The matching networks will transform the input impedance of the device at 19GHz to match for the coupler. At the output, the matching network will be placed after the DC blocking capacitor and will be matched for RF signals at 38GHz. Since the objective of the thesis was not for wideband operation, simple and compact inductive and capacitive networks were employed for matching.

The initial value of S_{11} measured after the coupler was determined and Figure 4.32a illustrates the L and C network employed for matching at an input RF power of 13dBm. Since the ideal 180° hybrid coupler was designed for 50Ω matching, the matching network was synthesized to match the pHEMT to that impedance. Figure 4.32b plots the overall circuit input matching (S_{11}) results incorporating the matching networks.

Figure 4.32: Input matching network: (a) L and C matching circuit, (b) overall S_{11} measured from the input.

Similarly, output matching was measured initially. The S_{22} parameter was measured in the harmonic balance simulation by using a second small signal source with an frequency offset at the output as seen in Figure 4.28a. Figure 4.33a illustrates the inductor used for matching. The output matching results at 38GHz are shown in Figure 4.33b.

Figure 4.33: Output matching circuit: (a) inductor for matching at 38GHz, (b) S_{22} measured at the output at 38GHz

The above design analysis has shown the use of simple matching networks to ensure maximum RF power is delivered to and from the doubler circuit. The matching networks were implemented with ideal components.

However, these matching networks will change slightly once non-ideal components are incorporated into the circuit, but a similar analysis will be performed to ensure good matching at input and output frequencies.

4.7.4 Ideal Circuit Performance

With the input and output matching networks incorporated into the balanced circuit, the ideal 19 to 38GHz balanced frequency multiplier circuit was complete. Table 4-1 outlines the ideal circuit performance results obtained in a harmonic balanced simulation.

Table 4-1: Ideal balanced frequency doubler performance.

Performance	Simulated Result
Maximum Conversion Gain	-7.582dB @ 11dBm input power
Fundamental Frequency Output Power (19GHz)	< -80dBm @ 11dBm input power
Second Harmonic Output Power (38GHz)	3.418dBm @ 11dBm input power
S_{11}	< -30dB @ 11dBm input power
S_{22}	< -20dB @ 11dBm input power

4.8 Momentum CPW Circuit Analysis

The ideal circuit presented in the previous section provided a foundation to develop the circuit in CPW with the foundry's substrate data using the Momentum simulator. Using Momentum, passive CPW structures can be created and simulated as a complete circuit to obtain performance results.

4.8.1 Drain Connection

From the ideal circuit, the drains of the pHEMT are connected by 75Ω transmission lines of electrical length 69° at 19GHz. Using Momentum, the dimensions for a 75Ω CPW were determined and the drain connection structure is shown in Figure 4.34. A $1250\mu\text{m}$ CPW was simulated and was shown to represent 69° at 19GHz. The line was bent as shown in Figure 4.34 for compactness. By bending the CPW, additional losses were introduced through parasitics and a purely reactive load seen by the output of the pHEMT could not be achieved. A three-port s-parameter network was created from the momentum simulation and was compared to the equivalent ideal transmission lines in the overall doubler circuit. Figure 4.35 shows the load seen by the pHEMT at 19GHz with the ideal transmission lines while Figure 4.36 shows the load seen with the momentum three-port s-parameter network. Once the ideal matching networks were re-adjusted, the performance results obtained were slightly lower than those from the ideal circuit. The conversion gain decreased

by 0.2dB to -7.7dB. This was to be expected due to the losses that are included in the Momentum simulation.

Figure 4.34: CPW layout for drain connection.

Figure 4.35: Reactive Load seen by the drains of each pHEMT with ideal transmission line length.

Figure 4.36: Load seen by the drains of each pHEMT with CPW connection.

4.8.2 Gate Bias Line

As discussed earlier in this chapter, the gate bias structure will consist of a 6nH inductor, 3pF capacitor, 80 Ω resistor and 4pF capacitor. In keeping with CPW design, symmetry was maintained by creating the same required impedance or capacitance through parallel structures. Since the gate will have virtually zero DC current, CPW line widths were not of concern.

In order to achieve approximately 6nH of inductance, three 2nH spiral inductors were connected in series such to ensure that the minimum resonance frequency of each inductor was greater than 19GHz. At the minimum resonance frequency, an inductor no longer behaves like an inductor and has a quality factor Q of zero. From the theory presented in [10], the minimum resonance frequency is inversely proportional to the inductance. At 6nH, a single OMMIC process spiral inductor has a resonance frequency of 8.7GHz. Therefore it was necessary to split the inductance into three 2nH spiral inductors. Upon further investigation and test simulations, it was realized that 4nH was sufficient to provide RF choking and no difference was made to the ideal circuit performance presented previously. Therefore, two 2nH spiral inductors were connected in series to obtain 4nH as shown in Figure 4.37.

OMMIC's SiN capacitors were selected to achieve the large capacitance values. Two 1.5pF capacitors in parallel were used to achieve 3pF. Similarly,

two 2pF capacitors in parallel were used to achieve 4pF. The capacitors are shown in Figure 4.37. To achieve the net capacitance, a parallel capacitance circuit was employed to maintain coplanar symmetry as described in Chapter 3. In addition, by maintaining coplanar symmetry, no air-bridges were necessary to suppress undesired modes.

To achieve 80Ω , two 160Ω GaAs resistors in parallel were used. Again, it was necessary to use a parallel structure to maintain coplanar symmetry. Since the gate voltage is at -0.8V , the maximum voltage handling capability of each resistor was not of concern. Figure 4.37 illustrates the GaAs resistors implemented in the gate bias line.

Figure 4.37: Gate structure including input matching network, DC blocking capacitor, gate biasing structure and folded multi-series shunt stub.

4.8.3 Gate Junction

A CPW t-junction was designed which combined the gate bias line, the CPW multi-shunt stub structure and a 5pF SiN DC blocking capacitor as shown in Figure 4.37. The CPW t-junction and the passive components were simulated in Momentum and a three-port s-parameter network was created.

4.8.4 Drain Bias Line

Similar to the gate bias, SiN capacitors and GaAs resistors were employed in the drain bias line. Since the drain bias line will have DC current and 3V, it was important to ensure that the GaAs resistors could handle the voltage and that the CPW could support the amount of current. However, since the pHEMT is biased at pinch-off, the DC current at the drain is much less than 1mA. According to the foundry's process guidelines, the metal layer (IN) used can support 6mA/ μm . A 70 Ω CPW of length $\lambda/4$ at 38GHz was simulated in Momentum and has a center conductor width of 8 μm which allows the CPW to support up to 24mA of current. S-parameter results of this structure show good RF suppression below -30dB from 5GHz to 40GHz. Figure 4.38 illustrates the drain bias line structure along with the SiN capacitor for DC blocking and the drain connection lines.

4.8.5 Matching Networks

With Momentum s-parameter networks created for most of the passive structures, it was necessary to re-adjust the input and output matching networks to account for the differences between ideal and non-ideal elements.

For the input matching network, inductance was provided through the length of CPW that was used for the series DC blocking SiN capacitor. Symmetric SiN+SiO₂ capacitors were connected in parallel to the ground plane as shown in Figure 4.35 to achieve a match to a resistive load of 39 Ω for a simple matching network at 19GHz.

Similarly, for the output matching network, it was designed with all the Momentum s-parameter networks in place, including the input matching network. Since the pHEMTs are bi-lateral devices, the input and output matching networks were tuned continuously to achieve the best matching. Spiral inductors could not be used at the output for matching at 38GHz due to their low resonance frequencies. Instead, to achieve larger inductances, a shorted CPW series stub was incorporated into the center conductor as shown in Figure 4.38. The impedance and length of the series stub was optimized such that two SiN+SiO₂ capacitors in parallel brought the output matching to 50 Ω .

Figure 4.38: Drain passive CPW structure incorporating the drain connection lines, drain bias and stability structures and output matching network.

4.8.6 Performance Results

Table 4-2 highlights the performance results simulated with CPW components and an ideal three-port balun model:

Table 4-2: CPW balanced frequency doubler performance with ideal coupler at the input.

Performance	Simulated Result
Maximum Conversion Gain	-8.085dB @ 17.5dBm input power
Fundamental Frequency Output Power (19GHz)	< -30dBm @ 17.5dBm input power
Second Harmonic Output Power (38GHz)	8.932dBm @ 17.5dBm input power
S_{11}	-13dB @ 17.5dBm input power
S_{22}	< -20dB @ 17.5dBm input power

Note that the maximum conversion gain has shifted from an input power of 11dBm to 17.5dBm once ideal elements were replaced with CPW Momentum components. Also, the conversion gain has decreased to approximately -8.0dB due to further losses accounted for by the Momentum simulation of CPW structures.

4.9 180° Three-port Coupler

As discussed in Chapter 2 and Chapter 3, the balanced frequency multiplier requires a circuit to successfully split the input RF signal into two separate signals that are 180° out of phase. By incorporating the balanced and unbalanced behaviours of slotline to CPW transitions and the phase properties of slot to CPW T-junctions, a simple three-port passive network was incorporated into the multiplier circuit.

4.9.1 Ideal Circuit Equivalent

From the transmission line theory presented in Chapter 3, it was shown that a slotline to CPW T-junction creates a three port network structure such that the unbalanced electric fields at the CPW ports are 180-degrees out of phase. In addition, it was also shown that a transition can be designed such that an unbalanced CPW mode can be transformed into the balanced slotline mode. Figure 4.39 illustrates the basics of such a structure, where the CPW ground and center conductors are label by numbers. Figure 4.40 illustrates the equivalent transmission line circuit with each transmission line number corresponding to the labels in Figure 4.39. The equivalent circuit shows that the transmission lines are in a series configuration.

Figure 4.39: Basic three-port CPW structure with CPW input to a slot line transition and a slotline to CPW T-junction.

Figure 4.40: Equivalent transmission line model of the CPW structure shown in Figure 4.39.

Due to the inherent properties and the nature of the series configuration, it is impossible for a three-port network to be reciprocal, lossless and matched all at the same time [21]. The proposed three-port network is characterized by the fact that a change in the terminal conditions at any one port affects the conditions at the other ports. An insertion of a matching network at one port changes the impedance characteristics at the other two ports. That is why typical 180° hybrid couplers [44] are four-port networks, which provide isolation [21]. However, these four-port structures are large in size, therefore reducing the compactness of MMIC circuits. To meet the objective of this thesis, a simple three-port network will be implemented to achieve 180° phase difference with a trade-off in matching at all ports.

By developing an equivalent circuit model for the 180° coupler structure, we can simulate the behaviour of transmission line lengths and impedance to ensure optimal performance. In the circuit show in Figure 4.41, each transmission line has an impedance and electrical length at 19GHz. By default, all impedances were initially made to 50Ω and electrical line lengths were set to 90° . The output terminal impedances were set 39Ω , which is the load that the input matching networks have been designed to present as discussed in Section 4.8.5. Figure 4.42 illustrates the S-parameter results of the structure at the initial values.

Figure 4.41: Equivalent circuit schematic of CPW coupler structure.

Figure 4.42: Equivalent circuit results with initial impedance and line length values.

The main design objectives of this structure were to provide 180° phase difference at the outputs, low loss and good input matching. In order to meet the design objectives in terms of S-parameters, it would mean that the phase difference between S_{21} and S_{31} should be 180° at 19GHz, to have maximum S_{21} and S_{31} values at 19GHz, and to have a minimum S_{11} ($<-10\text{dB}$) value at 19GHz. In addition, the 180° coupler should be designed as compact as possible while meeting all the objectives.

From simulation of different line lengths, it was determined to be critical for the short circuit stubs $L2$ and $L5$ to be 90° ($\lambda/4$) at 19GHz which provide the appropriate open circuits. In addition, it was critical to ensure that the output line lengths $L4$ and $L6$ were equal in order to achieve 180° phase difference at the outputs.

Figure 4.43 plots the S-parameter results of the structure when the length of $L1$ was varied from 10° to 90° . It can be seen from Figure 4.43b that by changing $L1$, there were corresponding transformations of impedance and phase in S_{11} . Similar changes to S_{22} and S_{33} were observed when the lengths $L4$ and $L6$ were varied.

Figure 4.43: S-parameter results of coupler based, while sweeping length of L1. Notice the impedance transformation seen (b).

With the objectives in mind, the 180° coupler structure was optimized and the impedances and dimensions of the transmission lines are shown in Table 4-3. The S-parameter results are shown in Figure 4.44. It can be seen from the

Table 4-3: Ideal transmission lines for 180° coupler.

Transmission Line Impedance		Transmission Line Electrical Length (at 19GHz)	
Z1	54 Ω	L1	5 $^\circ$
Z2	54 Ω	L2	90 $^\circ$
Z3	45 Ω	L3	8 $^\circ$
Z4	35 Ω	L4	90 $^\circ$
Z5	35 Ω	L5	90 $^\circ$
Z6	35 Ω	L6	90 $^\circ$

dimensions that the input CPW to slotline transition has been shortened to minimize on overall size. In addition, from Figure 4.43b, the structure provides good input matching. The ideal, no loss structure offers good input matching (less than -20dB), minimum loss at 19GHz (S_{21} and S_{31} at -3dB), over 6dB of isolation between the two output arms, and exactly 180° phase difference between the outputs at 19GHz. The next step is to implement the ideal circuit in CPW and comparing the Momentum results.

Figure 4.44: Ideal lossless transmission line model simulation results of 180-degrees coupler.

4.9.2 Momentum Analysis

By using Momentum, the actual CPW structure was implemented with the substrate data provided by the foundry. In order to layout the CPW dimensions and impedances of Table 4-3, it was necessary to simulate CPW lines to obtain the desired impedances. Table 4-4 outlines the CPW dimensions required to obtain the correct impedances at 19GHz.

Table 4-4: Momentum simulated transmission line dimensions

Transmission Line	Impedance	Dimensions (gap/cond/gap)	Length
Z1	54 Ω	10/14/10 μm	90 μm
Z2	54 Ω	10/14/10 μm	1600 μm
Z3	45 Ω	10/22/10 μm	144 μm
Z4	35 Ω	10/52/10 μm	1580 μm
Z5	35 Ω	10/52/10 μm	1580 μm
Z6	35 Ω	10/52/10 μm	1580 μm

To implement the short circuit slotline stubs, a few design choices were considered. Various short circuit termination options are presented in [44]. In addition, [62] outlines three different pseudo short circuit slotline resonators as shown in Figure 4.45. Of particular interest is the slotline ring resonator shown in Figure 4.45c which provides a virtual short. A slotline ring resonator is a fundamental passive component in MMIC circuits and is a topic of considerable interest [Chang]. Compared to conventional slotline linear resonating stubs, the ring resonator does not suffer from open or short-end

Figure 4.45: Various types of slotline short circuits: (a) & (b) pseudo shorts, (c) ring virtual short [62].

effects. As a result, a more accurate resonance frequency can be achieved. In addition, ring resonators can provide a highly localized zero point.

For comparison, a CPW 180° coupler was initially designed and simulated based on the dimensions in Table 4-4 and with conventional slotline linear resonating stubs as shown in Figure 4.46. The Momentum simulation results from Figure 4.47 shows strong agreement with the ideal equivalent circuit. Next, a similar coupler was simulated with the use of slotline ring resonator as shown in Figure 4.48. The simulation results are shown in Figure 4.49. Building on the compactness of the slotline ring resonator, a new design was conceived to accommodate the rest of the doubler circuit as shown in Figure 4.50 and the simulation results of the coupler are shown in Figure 4.51. Instead of a perfect ring, the resonator has a diamond shape design to achieve the virtual short. As well, to maintain compactness, the conventional slotline linear stub was employed at the input. The new coupler design achieves good input matching

($S_{11}=-21\text{dB}$ @ 19GHz), low loss (S_{21} and S_{31} of -3.8dB) and output matching where S_{22} and $S_{33}=-6.3\text{dB}$. In addition, a 181-degree phase difference at the output ports was achieved.

Figure 4.46: Coupler with linear slotline shorts.

Figure 4.47: Momentum results of coupler with linear slotline terminations.

Figure 4.48: Coupler with slotline ring virtual short.

Figure 4.49: Momentum results of coupler with slotline ring termination.

Figure 4.50: Compact coupler with slotline diamond shaped virtual short.

Figure 4.51: Momentum s-parameter results of coupler with diamond shaped slotline virtual short.

4.10 Final CPW Momentum Circuit Results

The three-port network was inserted into the CPW circuit and good performance results were achieved with minor adjustments to the input and output matching networks. Figure 4.52 illustrates the final layout of the entire balanced frequency doubler circuit. The Table 4.5 summarizes the performance results of the 19 to 38GHz frequency multiplier:

Table 4-5: Summary of doubler performance results.

Performance	Ideal Circuit	CPW Circuit
Maximum Conversion Gain	-7.582dB @ 11dBm input power	-8.539dB @ 17dBm input power
Fundamental Frequency Output Power (19GHz)	< -80dBm @ 11dBm input	-22dBm @ 17dBm input
Second Harmonic Output Power (38GHz)	3.418dBm @ 11dBm input	8.942dBm @ 17dBm input
S_{11}	< -30dB @ 11dBm input power	< -20dB @ 17dBm input power
S_{22}	< -20dB @ 11dBm input power	< -20dB @ 17dBm input power

Figure 4.52: Final layout of 19-38GHz Balanced CPW Frequency Doubler circuit, size 2.5x2.5mm.

CHAPTER 5 *On Wafer Measurements of the Multiplier Circuit*

5.1 Introduction

From the results obtained in Chapter 4, the design was submitted and reviewed by the MMIC group at CRC. DC and RF input pads were added to the layout and was sent to the foundry for fabrication. This chapter reviews the measurements performed and the results obtained. All measurements were taken at the MMIC wafer testing facility at CRC. In Section 5.2, power measurements were obtained and the best circuit across the wafer was determined. In Section 5.3, small signal s-parameters of active and passive test circuits were measured. In Section 5.4, simulated and measured results were compared and a summary of results were provided. Finally Section 5.5 presents a discussion on the results observed.

5.2 Power Measurements

Output power measurements were measured on wafer with the use of a HP437B Power Meter, which provided more accurate power measurements than the HP8565E Spectrum Analyzer. DC drain voltage was provided by a Kikusui Regulated DC Power Supply model PAB18-18A and the two gate voltages were

provided by two Kikusui models PMC35-2. In addition, RF cables and probes were measured for losses at various frequencies and were factored into the final measurements. Figure 5.1 illustrates the measurement setup.

Figure 5.1: Wafer measurement setup.

For an accurate comparison between measured and simulated results, a plastic donut shaped disc of height $635\mu\text{m}$ was placed underneath the wafer as shown in Figure 5.2. This creates a pocket of air underneath the circuit under test. Momentum simulation results from Chapter 4 were based a substrate configuration in which the layers were on air. Without the plastic donut, the wafer would be sitting directly on the metallic measurement table, giving the appearance of a conductor-backed CPW circuit.

Figure 5.2: Plastic donut shaped disc underneath wafer during test to simulate pocket of air.

Note that it was determined that spurious frequencies were well suppressed below that of 38GHz, therefore allowing the use of a power meter to measure second harmonic output power.

5.2.1 Designed Bias and Frequency

To confirm the performance of the frequency doubler, power output measurements were performed on wafer at reticle R17C17 with the bias at $V_g = -0.8V$ and $V_d = 3V$. Figure 5.3 shows the measured power outputs at 19GHz and 38GHz. Due to the frequency limitation of the power meter, the third harmonic could not be measured. From the plot, it can be seen that the

Figure 5.3: Output power versus input power measurements where the fundamental output power is at 19GHz and the second harmonic at 38GHz.

fundamental output power is suppressed below the second harmonic by 25 to 36dB. Figure 5.4 shows a plot of the conversion gain of the circuit. It can be seen that the maximum conversion gain obtained was -10.55dB at an input

power of 15.5dBm. At this input power, the drain current was 25mA. The power measurements obtained were within range of the simulated performance results discussed in Chapter 4. Direct comparisons with simulated results will be made in Section 5.4.

Figure 5.4: Conversion gain measurements.

5.2.2 Bandwidth

To determine the best conversion gain that could be obtained with the fabricated circuit, output power measurements were taken across an input frequency range that spanned from 18.5 to 21GHz. Figure 5.5 illustrates a plot of the maximum conversion gain versus input frequency. The figure shows that the frequency doubler operates at 1.25dB higher conversion gain when the input

frequency is at 19.9GHz. At 19.9GHz, the maximum conversion gain obtained at an output frequency of 39.9GHz was at -9.16dB with an input power of 16.97dBm. The measured results indicate a potential frequency shift of approximately 900MHz in the circuit.

Figure 5.5: Maximum conversion gain measured with input frequency ranging from 18.5GHz to 21GHz.

5.2.3 Power Variations across Wafer

Due the nature of the MMIC fabrication process, output power variations were observed in each frequency doubler circuit across the entire wafer. A test was performed to determine three reticles that produced the best performance in terms of output second harmonic power. With an input power of 15.5dBm at 19GHz, Figure 5.6 illustrates the mapping of output powers at 38GHz measured

at each reticle across the wafer. It can be seen that the range of output powers varies from -0.26 to 1.83dBm.

Two other reticles were selected on the wafer to obtain three sets of data such that the frequency shift trend observed in the previous section could be verified. Based on the output powers observed in Figure 5.6, reticles R27C13 with a second harmonic output power of 1.66dBm and R32C17 with 1.83dBm were selected based on their high output power.

Figure 5.6: Wafer map of doubler circuit with output power at 38GHz of each reticle as illustrated. The darkened reticles were selected for final measurements.

5.2.4 Optimal Frequency and Performance

Figure 5.7 illustrates a plot of the maximum frequency conversion gain versus input frequency for the three selected reticles across the wafer. It can be

seen that the same trends were observed. The measurements conclude that the circuit achieves the best conversion gain performance when operated as a 19.9 to 39.9GHz frequency doubler.

Figure 5.7: Maximum conversion gain plotted against input frequency for the three reticles selected in Section 5.23.

In addition, the best performance results were obtained on reticle R32C17, with a conversion gain of -9.07dB at 19.9GHz. Figure 5.8 shows the measured output powers with an input frequency of 19GHz. Figure 5.9 shows the conversion gain at 19GHz. At an input frequency of 19.9GHz, Figure 5.10 illustrates the measured output powers while Figure 5.11 shows the conversion gain. It can be observed from the figures that for both sets of input frequencies,

the fundamental output power was suppressed below the second harmonic by at least 20dB and as much as 40dB at the region of interest.

Figure 5.8: Second harmonic and fundamental output power plotted for the doubler circuit on reticle R32C17.

Figure 5.9: Conversion gain for doubler circuit on reticle R32C17.

Figure 5.10: Output power plot with input frequency at 19.9GHz.

Figure 5.11: Conversion gain plot with input frequency at 19.9GHz.

5.3 Small Signal S-parameters

Since large signal s-parameters measurements were not possible, small signal s-parameters were measured instead. By comparing the measured and simulated s-parameters, we can get an indication as to what could be contributing to the frequency shift.

5.3.1 Doubler Circuit

At the designed bias, two port s-parameter measurements were obtained and are shown against simulated results in Figure 5.12. It can be seen that the

simulated results very closely match the measured s-parameters. The only difference was in the dB levels of the measurements which were generally higher than simulated. The strong agreement in s-parameter trends between the simulated and measured results can only indicate that the circuit is performing as designed.

Figure 5.12: Small signal s-parameter measurements for entire doubler circuit with bias.

5.3.2 180 Degrees Coupler

Test circuits of individual sections of the frequency doubler circuit were fabricated on the wafer. These circuits allow each stage of the overall circuit to be analyzed. The 180° three-port coupler was selected as a test circuit. Figure 5.13 shows the fabricated coupler test circuit. Since the measurement facility at CRC is capable of only measuring one port per axis, the third port of the coupler test circuit was designed with a 50Ω GaAs resistor termination. This allowed limited verification of the coupler. Figure 5.14 illustrates the s-parameter measurements obtained for the coupler. It can be seen that all the s-parameters closely matched the simulated results, except for S_{11} . Figure 5.14a shows the measured S_{11} to be slightly different compared to the simulated results in the region between 15 to 30GHz. However, at 19GHz, the measured value was still quite acceptable with $S_{11} < -10\text{dB}$.

5.3.3 Gate Structure

A gate structure consisting of the input matching network, gate bias line and the multi-series shunt stub was fabricated on wafer as a test structure as shown in Figure 5.15. Figure 5.16 illustrates the three-port s-parameter measurements. It can be seen that the measured and simulate results are almost identical. This verified that the matching network could not be

contributing to the frequency shift observed in the previous power measurements.

Figure 5.13: 180° three-port coupler test circuit with one output port terminated with 50 Ω GaAs resistor.

Figure 5.14: Measured s-parameter results of coupler test circuit.

Figure 5.15: Gate structure test circuit.

Figure 5.16: Three-port s-parameter measurements of the gate structure test circuit.

Figure 5.16 (cont'd): Three-port s-parameter measurements of the gate structure test circuit.

Figure 5.17: Phase measurements of the gate structure test circuit.

5.3.4 Drain Structure

A drain structure consisting of the drain bias line, t-junction, and output matching network was fabricated separately as a test structure as shown in Figure 5.18. Figure 5.19 illustrates the three-port s-parameter measurements. Strong s-parameter agreement between measured and simulated results can be observed. Variations in dB levels can be seen at different frequency ranges. Large differences (5 to 10dB) in magnitude levels at 38GHz were observed in S_{11} and S_{21} . These differences could be the result of variations in the fabricated capacitors where the distance between substrate layers is critical. The phase measurements are shown in Figure 5.20. From the results, there is a difference in the phase seen at port 2, where the simulated and measured phases are opposite.

Figure 5.18: Drain structure test circuit.

(a)

(b)

(c)

(d)

(e)

(f)

Figure 5.19: S-parameter measurements of drain structure test circuit.

Figure 5.20: Phase measurements of drain structure test circuit.

5.3.5 Multi-Series Shunt Stub

Figure 5.21 illustrates the multi-series shunt stub as a test structure. The two-port s-parameter measurements are shown in Figure 5.22. It can be seen that the stub is performing as simulated by shorting signals at 38GHz. The only difference lies in the magnitude of the s-parameters at 38GHz. The measured structure suppresses signals at 38GHz by 8dB while the simulated structure suppresses by almost 25dB. The difference in suppression would allow a greater amount of 38GHz RF signal to be reflected back through the pHEMT. This could explain for the lower output power measurements leading to an overall lower conversion gain. The phase results are shown in Figure 5.23.

Figure 5.21: CPW Multi-series shunt stub test circuit.

Figure 5.22: S-parameter measurements of multi-series shunt stub test structure.

Figure 5.23: Phase measurements of multi-series shunt stub test structure.

5.4 Design Comparison

From Section 5.2, it was found that the power performance varies from circuit to circuit across the wafer. Therefore, this thesis has chosen to highlight the best performing doubler circuit, which was determined in Section 5.2 to be at reticle R32C17. The following sections will highlight the measured results at reticle R32C17 and be compared against simulated data.

5.4.1 Power Output

Figure 5.24 shows the simulated and measured output powers at an input frequency of 19GHz. It can be seen that the second harmonic power output at 38GHz follows the simulated output power quite closely. The measured fundamental power output is lower than simulated by 10 to 20dB. In fact, the fabricated circuit suppresses fundamental power much better than predicted.

Figure 5.24: Comparison of simulated and measured output power results at 19GHz.

5.4.2 Conversion Gain

Figure 5.25 compares the simulated against the measured conversion gain. It can be seen that the conversion gain measured is approximately 2dB lower than the simulated. This could be due to a higher substrate loss than simulated, as observed in the power output levels in Figure 5.24. However, the general trend of the measured gain agrees with the simulated.

Figure 5.25: Comparison between simulated and measured 19 to 38GHz conversion gains.

5.4.3 Bandwidth

Although a wide bandwidth was not an objective of this thesis, it was interesting to observe the range of input frequencies that could be used with the frequency doubler circuit. The bandwidth is defined as the range of frequencies in which the conversion gain varies no more than 3dB from its maximum. Figure 5.26 illustrates the measured maximum conversion gain versus input frequency. It can be seen that the measured results are a 1 to 2dB lower than the simulated conversion gain. From Figure 5.26, the measured bandwidth is

It can be seen from Figure 5.26 that the maximum conversion gain occurs at 19.9GHz as discussed in Section 5.4.2. However, the same trend was also seen in the simulated data. During the design analysis, we did not examine the bandwidth of the doubler. It was assumed that since the coupler, matching networks and bias structures were all designed at 19GHz, there was no reason why the best performance was not obtained at the design frequency. It can be seen from Figure 5.26 that the measured conversion gain at 19GHz and 19.9GHz differs by 1.3dB.

Figure 5.26: Comparison between simulated and measured bandwidth results.

5.4.4 Performance Summary

Table 5-1 summarizes the simulated and measured performance of the frequency doubler design at 19GHz.

Table 5-1: Summary of best doubler performance with an input frequency of 19GHz.

Performance	Simulated (at 15.52dBm input)	Measured (at 15.52dBm input)
Maximum Conversion Gain	-8.623dB	-10.37dB
Fundamental Frequency Output Power (19GHz)	-24.981dBm	-34.07dBm
Second Harmonic Output Power (38GHz)	6.897dBm	5.15dBm
S_{11}	< -28dB	n/a
S_{22}	< -28dB	n/a

5.5 Discussion

From the measurements, it can be concluded that the objectives of the frequency doubler were satisfied. The design achieved moderate conversion loss at 19 to 38GHz, employed a novel three-port network to achieve phase balance and incorporated the use of a new class of compact CPW structures.

The passive structures were found to perform as designed. Without large signal s-parameter measurement capabilities, there was no way to verify the input and output matching of the circuit at the desired input power level. However, we can assume that the matching networks were adequate since the output power levels were only a few decibels lower than simulated and that the maximum conversion gain versus input frequency trends were similar to simulation results.

In addition, although initial results suggested that there was a frequency shift, further investigation revealed that the frequency shift measured was also contained in the simulation data. During design analysis, we failed to examine the bandwidth of the doubler circuit and it was assumed due to the nature of the matching networks and resonant structures that frequency multiplication was optimal at 19GHz. If input frequency was swept and maximum conversion gain was measured, it would have revealed during design analysis that optimal

operation occurred at 19.9GHz. The reason for the 900MHz shift is uncertain, but a potential reason could be that some of the resonant structures were not tuned precisely enough for 19GHz operation.

Finally, the balanced topology yielded excellent fundamental output power suppression. The 19GHz output signal is over 35dB below the 38GHz signal when maximum conversion gain occurs.

Figure 5.27: Actual fabricated MMIC CPW Balanced Multiplier.

CHAPTER 6 *Discussion and Recommendations*

6.1 Synopsis

6.1.1 Summary of Work

This thesis has successfully demonstrated the design of a 19 to 38GHz coplanar balanced frequency multiplier incorporating novel CPW structures.

A detailed characterization of the pHEMT active device was presented and second harmonic generation was optimized during the design analysis. CPW design considerations were taken into account and all passive structures were simulated fully. A novel coplanar-to-slotline-to-coplanar three port structure was designed to achieve 180° phase separation. Based on a set of acceptable simulation results, the circuit was fabricated and measurements were taken. The measurements show strong correlation with the simulated data, with a slightly higher loss than simulated. The decrease in second harmonic output power led to 1.8dB lower conversion gain compared to simulation. Further investigation revealed that the optimal conversion gain could be obtained with an input frequency of 19.9GHz.

6.1.2 Major Thesis Accomplishments

This work into CPW balanced frequency multiplier has demonstrated the potential of CPW as a suitable technology for MMIC design. In addition, it has highlighted the use of novel CPW structures to achieve higher levels of integration. The major results of this work are the following:

- A -10.37dB of conversion gain from 19 to 38GHz at 15.52dBm of input power.
- A successful design of a CPW-Slotline-CPW three port 180° coupler for use in a balanced topology.
- Incorporating a CPW multi-series shunt stub for harmonic rejection.
- Over 34dB of fundamental output power suppression.

The frequency doubler was designed over a 2.6x2.6mm dimension.

6.2 Discussion of Future Work

Although the design of frequency multipliers is a matured research area, there is a need to utilize more novel CPW structures to achieve higher levels of integration and better conversion efficient at high frequencies. Future work might include the following:

- To reduce the size of the current design by investigating other novel CPW structures that can be incorporated.
- To further reduce the loss through the 180° coupler by investigating other designs.
- Using another to simulation software to design the passive CPW structures to determine if it might be more accurate.

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