A Delta-Sigma Frequency Discriminator
with Fractional-N Divider
and 3-Bit Quantizer

Jian-Hong Fang

M.A.Sc, B.Eng

A Thesis Submitted To The Faculty Of
Graduate Studies And Research
In Partial Fulfilment Of The Requirements
For The Degree Of M.A.Sc
Department of Electronics
Carleton University, Ottawa, Canada
© Jian-Hong Fang, 2007

Library and
Archives Canada

Bibliothèque et
Archives Canada

Published Heritage
Branch

Direction du
Patrimoine de l'édition

395 Wellington Street
Ottawa ON K1A 0N4
Canada

395, rue Wellington
Ottawa ON K1A 0N4
Canada

Your file Votre référence

ISBN: 978-0-494-26986-2

Our file Notre référence

ISBN: 978-0-494-26986-2

NOTICE:

The author has granted a non-exclusive license allowing Library and Archives Canada to reproduce, publish, archive, preserve, conserve, communicate to the public by telecommunication or on the Internet, loan, distribute and sell theses worldwide, for commercial or non-commercial purposes, in microform, paper, electronic and/or any other formats.

The author retains copyright ownership and moral rights in this thesis. Neither the thesis nor substantial extracts from it may be printed or otherwise reproduced without the author's permission.

AVIS:

L'auteur a accordé une licence non exclusive permettant à la Bibliothèque et Archives Canada de reproduire, publier, archiver, sauvegarder, conserver, transmettre au public par télécommunication ou par l'Internet, prêter, distribuer et vendre des thèses partout dans le monde, à des fins commerciales ou autres, sur support microforme, papier, électronique et/ou autres formats.

L'auteur conserve la propriété du droit d'auteur et des droits moraux qui protègent cette thèse. Ni la thèse ni des extraits substantiels de celle-ci ne doivent être imprimés ou autrement reproduits sans son autorisation.

In compliance with the Canadian Privacy Act some supporting forms may have been removed from this thesis.

Conformément à la loi canadienne sur la protection de la vie privée, quelques formulaires secondaires ont été enlevés de cette thèse.

While these forms may be included in the document page count, their removal does not represent any loss of content from the thesis.

Bien que ces formulaires aient inclus dans la pagination, il n'y aura aucun contenu manquant.

Canada

Abstract

The design and implementation of a new Frequency Discriminator (FD) architecture is presented in this thesis. This architecture has finer frequency resolution and lower frequency noise compared to existing architectures. This superior performance is achieved by incorporating a fractional-N divider and a multi-bit quantizer. The new architecture is based on Delta-Sigma ($\Delta\Sigma$) Modulation techniques and converts instantaneous frequency directly to digital form.

Simulation models were developed in Matlab Simulink to explore the effect of various parameters on performance. The models then were transformed into circuit blocks. The circuit blocks were simulated both at the behavioural and the transistor level. The design was fabricated in 0.18 μm TSMC CMOS process.

This FD architecture is suitable for use in high resolution frequency synthesis and frequency demodulation applications.

Acknowledgements

I would like to thank Prof. Miles Copeland and Dr. Norm Filiol for their encouragement and guidance over the course of this research and Mr. Tom Riley of Kaben Research Inc. for technical and financial support. This research was funded by CITO and Kaben Research through the Student Internship Program.

Special thanks go to Dr. John Hulse from Institute for Microstructural Science in National Research Council Canada for generously lending his hands on fault analysis and for turning a designer's nightmare to a enjoyable and learning experience.

I also owe thanks to the following individuals for their help in different areas:

Gordon Allan: Digital Design Flow. Yunle Sun: Analog Layout. Mary Ann Riley: Administration of Research Funding.

Finally, I want to thank my lovely wife, Ni Liu, for her continuous and selfless support. As a former world champion in sports acrobatics, she appreciates the hard work and determination both in sports and academic world.

Contents

1	Introduction	1
1.1	Motivation	1
1.2	Objectives	3
1.3	Contributions	4
1.4	Thesis Outline	5
2	Background	7
2.1	Frequency Discriminators	7
2.1.1	Analog Frequency Discriminators	8
2.1.2	PLL Based FDs	9
2.1.3	$\Delta\Sigma$ FDs	11
2.1.4	Comparison of Different Types of Frequency Discriminators	12
2.2	$\Delta\Sigma$ Modulation	13
2.2.1	Over-Sampling	14
2.2.2	Noise-Shaping	16
2.3	First-Order $\Delta\Sigma$ Modulators	18
2.4	Second-Order $\Delta\Sigma$ Modulators	20
2.5	Higher-Order $\Delta\Sigma$ Modulators	22

3	Analysis of a Second-Order $\Delta\Sigma$ FD Having a Fractional-N Divider and a Multi-Bit Quantizer	23
3.1	First-Order $\Delta\Sigma$ FD	25
3.1.1	Linear Model for Dual-Modulus Divider	27
3.1.2	Linear Model for a First Order $\Delta\Sigma$ FD	29
3.1.3	Performance Evaluation	30
3.2	Second-Order $\Delta\Sigma$ FD with Integer-N Divider and Single-Bit Quantizer . . .	33
3.3	Second-Order FD with Fractional-N Divider	37
3.4	A Second-Order $\Delta\Sigma$ FD Using a Fractional-N divider and a Three-Bit Quantizer (Proposed Architecture)	42
3.5	Comparison	44
3.6	Effects Of System Parameters on Performance	46
3.7	System Noise Analysis	48
3.7.1	Quantization Noise Transfer Function	50
3.7.2	f_{in} Noise Transfer Function	50
3.7.3	f_{ref} Noise Transfer Function	50
3.7.4	Divider Noise Transfer Function	50
3.7.5	PFD and CP Noise Transfer Function	51
3.7.6	Integrator Noise Transfer Function	51
3.7.7	Quantizer Noise Transfer Function	51
3.8	Circuit Performance Improvement Techniques	52
3.9	Summary	56
4	Circuit Design and Simulation Results	57
4.1	f_{in} and f_{ref} Input Buffers	60
4.1.1	Simulation Results	61

4.1.2	Phase Noise Performance	62
4.2	Programmable Multi-Modulus Divider	64
4.2.1	Prescaler	65
4.2.2	M-Counter	66
4.2.3	A-Counter	68
4.2.4	Decoding of M-Counter States	68
4.2.5	Simulation of MMD	71
4.3	Phase-Frequency Detector	72
4.3.1	PFD Noise Performance	75
4.4	Charge Pump	76
4.4.1	PFD/CP Noise Performance	80
4.5	Integrator	81
4.5.1	Noise Performance	84
4.6	3-Bit Quantizer	85
4.6.1	Comparator Design	86
4.6.2	Simulation Results	88
4.6.3	Noise Performance	90
4.7	Digital Feedback Block (DFB)	91
4.7.1	Encoder	91
4.7.2	$2 - Z^{-1}$ block	91
4.7.3	Residual Accumulator	92
4.7.4	Data Weighted Averaging Block	92
4.7.5	Simulation Result	94
4.8	Serial Interface	95
4.9	Overall Performance	99

5	Measurements	104
5.1	Chip Layout and Test Setup	104
5.2	Fabrication and Fault Analysis	107
6	Conclusions and Future Work	116
6.1	Conclusions	116
6.1.1	Summary	116
6.1.2	Advantages Over Existing $\Delta\Sigma$ FD Designs	119
6.2	Future Work	119

List of Figures

1.1	A Conventional PLL Based Frequency Synthesizer	1
1.2	A Frequency Discriminator Based Frequency Synthesizer	2
2.1	Narrow Bandpass Filter Used as a FD	8
2.2	FD with Improved Linearity	9
2.3	Slope Demodulator	9
2.4	PLL Used as a FD	10
2.5	Model of a First-Order PLL Frequency Discriminator	11
2.6	Block Diagram of First-Order $\Delta\Sigma$ FD	11
2.7	A Block Diagram for a First-Order DSM	13
2.8	Illustration of Sampling and Quantization	14
2.9	Quantizer Linear Model	15
2.10	In-band Noise Decreases with Increasing Sampling Frequency	16
2.11	Noise Spectral Density before and after Shaping	17
2.12	Linear Model of a First Order DSM	18
2.13	Linear Model of a Second Order DSM	20
3.1	Block Diagram for a First-Order $\Delta\Sigma$ FD	25
3.2	Timing Diagram for a First-Order $\Delta\Sigma$ FD	25

3.3	Phase Ramps for f_{ref} and f_{div}	27
3.4	Linear Model for Dual-Modulus Divider	29
3.5	Linear Model for a First-Order $\Delta\Sigma$ FD	29
3.6	Simulation of First Order $\Delta\Sigma$ FD	32
3.7	Second Order $\Delta\Sigma$ FD Block Diagram	33
3.8	Second Order $\Delta\Sigma$ FD Linear Model	33
3.9	Matlab Simulation Result for the Second Order $\Delta\Sigma$ FD	35
3.10	An Example of Phase Error Cancellation in Fractional-N Frequency Synthesis	37
3.11	Block Diagram for a Second-Order $\Delta\Sigma$ FD With Fractional-N Divider . . .	38
3.12	Linear Model of Second Order $\Delta\Sigma$ FD with Fractional-N Divider	39
3.13	Integer-N versus Fractional-N Divider Comparison	41
3.14	Second-Order $\Delta\Sigma$ FD with Fractional-N Divider and Multi-Bit Quantizer . .	42
3.15	Linear Model for Figure 3.14	43
3.16	SNR vs Input Frequency Deviation	45
3.17	Linear Model of 2nd-Order Fractional-N $\Delta\Sigma$ FD	48
3.18	Noise Transfer Function at Various Circuit Nodes	52
3.19	CP Output with (a) no DWA, and (b) DWA	53
3.20	DWA for Eight Elements - Input Sequence: 011, 100 and 010	54
3.21	Comparison between no CP Mismatch, CP Mismatch with and without DWA	56
4.1	System Block Diagram	57
4.2	$\Delta\Sigma$ FD Design Flow and Tools Used	59
4.3	Input Buffer	60
4.4	f_{ref} Input Buffer Operation	61
4.5	f_{in} Input Buffer	62
4.6	Output Phase Noise of f_{ref} Buffer	63

4.7	Output Phase Noise of f_{in} Buffer	63
4.8	Programmable Multi-Modulus Divider	64
4.9	Programmable MMD Timing	65
4.10	Schematic for Prescaler	66
4.11	Schematic for M-Counter	67
4.12	Schematic for A-Counter	68
4.13	Mapping of M-counter States to MMD Timing Signals	70
4.14	RTL Test Bench Simulation Results	71
4.15	A schematic for a PFD	72
4.16	PFD with DC offset	73
4.17	PFD Transition Simulation: Fref Leading Fdiv	74
4.18	PFD Transition Simulation: Fref Lagging Fdiv	75
4.19	Schematic for one Charge Pump element	77
4.20	Charge Pump Operation	79
4.21	PFD/CP Output-Referred Noise	80
4.22	(a) a Passive Integrator and (b) an Active Integrator	81
4.23	Schematic for a Active Integrator	82
4.24	Integrator Transient Response	83
4.25	Integrator Output Referred Noise for Lock Condition	84
4.26	An Array of Eight Comparators Used as a 3-bit Quantizer	85
4.27	Comparator Schematic	87
4.28	Quantizer Simulation	89
4.29	Quantizer Input-Referred Noise	90
4.30	The Digital Feed Back Block	91
4.31	Residual Accumulator	92

4.32	Block Diagram for DWA implementation	93
4.33	DFB RTL Simulation Result	94
4.34	Implementation of Serial Interface	95
4.35	Serial Interface Timing	97
4.36	Serial Interface RTL Simulation	98
4.37	System Simulation with Verilog-A and Verilog	99
4.38	System Simulation (PFD Modelled at the Transistor Level)	100
4.39	System Simulation (CP Modelled at the Transistor Level)	100
4.40	System Simulation (Quantizer Modelled at the Transistor Level)	101
4.41	System Frequency Noise Performance	102
4.42	System Phase Noises Performance	103
5.1	Chip Layout	105
5.2	Test Setup	106
5.3	Block Diagram for a DEI System [HFSN04]	108
5.4	Test setup with DEI System	109
5.5	Locations for DEI Measurements	110
5.6	DEI Images. Left: RESET is inactive and Right: RESET is active	111
5.7	Time-Related Waveform When RESET is active	112
5.8	Time-Related Waveform When RESET is inactive	112
5.9	Divider Waveform	114
5.10	Time-Related Waveform When RESET=OFF	115

List of Tables

2.1	Comparison of Different Types of Frequency Discriminators	12
3.1	$\Delta\Sigma$ FD Architecture Performance Comparison	44
3.2	Simulation Result for Different Combinations of f_{ref} and n	47
4.1	Prescaler State Table	66
4.2	Decoder Outputs	69
4.3	CP Output Current vs Control Bits	78
4.4	Static Control Signals	95
4.5	Serial Interface Signals	96
4.6	System SpectreVerilog Simulations	99
5.1	External Pin DC Bias Level Measurement	107

Chapter 1

Introduction

1.1 Motivation

Frequency synthesizers are an essential component in wireless communication devices. It is very difficult to find a transceiver today that does not employ at least one if not several frequency synthesizers.

Phase Locked Loop (PLL) based frequency synthesis is the most commonly used method of generating stable high frequencies. The architecture of a conventional PLL based frequency synthesizer is shown in Fig.1.1.

Figure 1.1: A Conventional PLL Based Frequency Synthesizer

The system compares the frequencies of two signals (one is the reference clock, f_{ref} , the other one is the divided-down version of VCO output frequency, f_{out}) and produces an error signal which is proportional to the difference between the phases of these two signals. The error signal, after being processed, is used to drive the Voltage-Controlled Oscillator (VCO). The output frequency from the VCO passes through a frequency divider back to the input of the phase comparator, producing a negative feedback loop. If the reference clock or the division ratio, N , changes, the error signal will increase, driving the VCO frequency in the opposite direction to reduce the error. Thus, the VCO frequency is always locked to N times the reference clock.

A second generation synthesizer architecture [Bax94] is shown in Fig.1.2.

Figure 1.2: A Frequency Discriminator Based Frequency Synthesizer

The architecture shown in Fig.1.2 is based on an FD in the feedback path, which measures the VCO frequency and produces results in digital form. The FD functions as a frequency demodulator and analog-to-digital converter, and replaces the divider and phase detector in a conventional PLL synthesizer. Early conversion of the VCO frequency into digital form permits much of the remaining loop to be realized using Digital Signal Pro-

cessing (DSP) techniques. Since most of the loop is digital, the loop dynamics can be changed by re-programming the loop filter on the fly to suit different application needs. Such flexibility is the key to multi-mode transceivers.

Operation of this synthesizer architecture is similar to conventional PLL based ones. The FD bit-stream is decimated and scaled to give a measure of the VCO frequency. This digital value is compared to the desired reference frequency word to produce an error signal. The error signal is digitally filtered and converted to an analog signal to drive the VCO.

The FD is the key component in this architecture. The remainder of this thesis focuses on the analysis, design and implementation of an improved version of the second-order $\Delta\Sigma$ FD first introduced in [Bax94]. It is hoped that the knowledge gained will allow for further improvements to high performance frequency synthesis.

1.2 Objectives

The objectives of this thesis are:

1. To analyze the $\Delta\Sigma$ frequency discriminator presented in [Bax94] and propose improvements.
2. Incorporate a fractional-N divider into the architecture presented in [Bax94]. This fractional divider should not require highly precise analog circuits and have a fractionality of $1/8$. Inclusion of this divider should result in 18 dB decrease in quantization noise compared to [Bax94].
3. Replace the single-bit quantizer with a multi-bit quantizer in order to maintain the full-scale input range of the discriminator.
4. Analyze the new architecture using Matlab/Simulink.

5. Implement and test the architecture at the transistor level in a 0.18 μm CMOS process.

1.3 Contributions

The contributions made in this thesis, to the research area of high performance frequency measurement and frequency synthesis, are the following:

1. The design and analysis of a new architecture for a $\Delta\Sigma$ frequency discriminator that makes use of a novel fractional divider. This discriminator measures the instantaneous frequency of an input signal and converts it directly into digital form. Use of a fractional divider with a step size of $1/8$ results in 18 dB less total quantization noise power in the output bitstream, compared to previous implementations. This reduces the decimation filter requirements after the discriminator and improves the SNR for small deviation FM signals. The fractional divider makes use of a Data Weighted Averaging (DWA) algorithm to apply first order noise shaping to mismatch errors introduced in the divider elements. The end result is a second-order $\Delta\Sigma$ Frequency Discriminator with greatly improved dynamic range compared to previous architectures, providing higher sensitivity to low deviation frequency modulated signals.
2. A Matlab/Simulink model for the discriminator was designed and used to predict performance and to validate the concept of the new architecture. A linear analysis of the architecture was performed in order to create a model for analysis purposes. The model was used to determine the transfer function of the signal and various noise sources to the output of the discriminator. These results are summarized in [FFRC07] and will be presented at ISCAS 2007, in New Orleans, USA.
3. A transistor level design for the new discriminator architecture was created, simu-

lated and fabricated in the TSMC 0.18 μm CMOS process. Simulations were performed, at the transistor level, for each block. The noise predictions from these simulations were applied to the transfer functions determined in 2, and used to predict the SNR of the final design. Phase noise performance indicates a state of the art in-band BFM of -200 at 20 kHz offset. In order to help ensure functionality of the final design, each block was either modelled as a Verilog, Verilog-A or a transistor level circuit. This allowed for SpectreVerilog simulations of the architecture in closed loop, something which would not have been practical at full transistor level.

4. Due to an error in the Output Drivers, provided by the foundry, it was not possible to observe many of the key outputs of the fabricated circuit in the laboratory. As a result of this fault, a research relationship was formed with John Hulse of the NRC and MuAnalysis Inc. to prove the validity of using Dynamic Electroluminescence Imaging (DEI) measurements to debug high performance CMOS circuits. DEI is non-invasive, non-destructive and has a bandwidth approaching 100 GHz. This means that very fast signals can be observed without unduly loading or otherwise interfering with the circuitry under test. Using this technique, the feedback divider operation was confirmed. Results of this collaborative research effort have been submitted for publication at CSTC 2007.

1.4 Thesis Outline

The remainder of this thesis is organized as follows:

In Chapter 2, several different types of frequency discriminators are reviewed. $\Delta\Sigma$ Modulation techniques are briefly described. Analysis methods for $\Delta\Sigma$ Modulators are also presented. Finally, the $\Delta\Sigma$ FD is introduced: first-order $\Delta\Sigma$ FD, followed by the exten-

sion to second-order, and finally, second-order with a fractional-N divider and a multi-bit quantizer.

In Chapter 3, the detailed architecture design of the new $\Delta\Sigma$ FD is presented. The various design parameters and their effects on performance are examined closely. Some techniques used to overcome potential circuit imperfections are also explained. Matlab Simulink simulations are performed at this level.

Chapter 4 explains the partitioning of the system at the circuit level. The different design methods/flows for the analog and digital parts of circuits are described. The functionality and specifications for each block are verified through simulation at the behavioural level as well as at the transistor level.

Chapter 5 presents the measurement data from the fabricated chip and the results of DEI testing.

Chapter 6 presents conclusions and suggestions for further work in this area.

Chapter 2

Background

In this chapter, a brief review of FDs and DSM techniques is presented.

2.1 Frequency Discriminators

Frequency Discriminators (FDs) convert instantaneous frequency, taking the form of a sum of carrier and modulation components, as expressed in Eq.2.1, into a proportional voltage. The voltage amplitude at the output of a FD may take either analog or digital form, but its changes always follow, in direct proportion, those of the input frequency.

$$f_{in}(t) = f_{nom} + k_f s(t) \quad (2.1)$$

where $f_{in}(t)$ is the instantaneous frequency of the input frequency, f_{nom} the constant nominal carrier frequency, and k_f is the proportionality constant relating frequency changes to amplitude values of $s(t)$.

2.1.1 Analog Frequency Discriminators

A simple analog frequency discriminator can be built using a narrow band filter as shown in Fig.2.1.

Figure 2.1: Narrow Bandpass Filter Used as a FD

Within a limited range, the voltage is linearly proportional to the frequency. This range of linearity may be improved by subtracting a shifted version of the narrow-band filter's output from the non-shifted version [Rod96], as illustrated in Fig.2.2.

A slope demodulator, depicted in Fig.2.3, is used to implement the improved linearity. It is designed in such way that the even powers in the Taylor series expansion of the filter roll-off function are eliminated and it becomes an odd function of input frequency. The upper half of the output winding of the transformer and C_1 are tuned to f_a , and the lower half of the winding and C_2 are tuned to f_b .

Figure 2.2: FD with Improved Linearity

Figure 2.3: Slope Demodulator

2.1.2 PLL Based FDs

A PLL can also be used as a frequency discriminator. When the input signal is frequency modulated, the loop-generated error signal will, under certain conditions, be a duplicate of the input modulating signal. The first-order analogue PLL, shown in Fig 2.4, provides an example of this method.

Figure 2.4: PLL Used as a FD

The input signal, $y_i(t)$, is frequency modulated by a sinusoidal signal of frequency Ω and maximum deviation Δf_i . The instantaneous frequency of $y_i(t)$ is:

$$f(t) = f_c + \Delta f \sin(\Omega t + \theta) \quad (2.2)$$

$y_i(t)$ is given by:

$$y_i(t) = A \sin\left(2\pi f_c t + \frac{2\pi \Delta f}{\Omega} \cos(\Omega t + \theta)\right) \quad (2.3)$$

When the phase detector is operating in its linear region, its output is given by:

$$u_1(t) = K_1 \frac{2\pi \Delta f}{\sqrt{(K_1 K_2 K_3)^2 + \Omega^2}} \sin\left(\Omega t + \theta + \frac{\pi}{2} - \text{Arctan} \frac{\Omega}{K_1 K_2 K_3}\right) \quad (2.4)$$

$u_1(t)$ is a duplicate of the modulating signal of Eq 2.2, differing only by a multiplicative constant and low-pass filtering with the time constant $1/(K_1 K_2 K_3)$. A model which corresponds to this functionality is shown in Fig.2.5.

Figure 2.5: Model of a First-Order PLL Frequency Discriminator

2.1.3 $\Delta\Sigma$ FDs

A $\Delta\Sigma$ FD architecture introduced in [BC94] converts the instantaneous frequency of an input signal into a digital bit stream having a high SNR in the band of interest. The block diagram for a first-order $\Delta\Sigma$ FD is shown in Fig.2.6.

Figure 2.6: Block Diagram of First-Order $\Delta\Sigma$ FD

The term $\Delta\Sigma$ is used here because what this FD does for input *frequency* is what a $\Delta\Sigma$ A/D modulator does for input *voltage*. Therefore, all of the knowledge accumulated about conventional DSMs can be applied to the analysis of $\Delta\Sigma$ FDs. In the next section, a review of conventional DSMs is presented. A detailed analysis of $\Delta\Sigma$ FDs is presented in Chapter 3.

2.1.4 Comparison of Different Types of Frequency Discriminators

A comparison of the main performance parameters for the three different types of FDs presented in the previous sections is given in Table. 2.1. It can be seen from the table that the $\Delta\Sigma$ -based discriminator performs well for the parameters listed.

Parameter	Bandpass Filter	PLL-Based	$\Delta\Sigma$ -Based
Frequency Input Range	poor	fair	good
Frequency Resolution	poor	good	good
Linearity	poor	good	good
Dynamic Range	poor	fair	good
Output Format	analog	analog	digital
Phase Continuity	no	yes	yes

Table 2.1: Comparison of Different Types of Frequency Discriminators

2.2 $\Delta\Sigma$ Modulation

$\Delta\Sigma$ Modulation (DSM) was first introduced in 1962 [IM62] and has been used in applications such as digital phones, digital audio, instrumentation and frequency synthesis [NST96]. The block diagram for an A/D converter using first-order DSM is shown in Fig.2.7.

Figure 2.7: A Block Diagram for a First-Order DSM

This type of modulator exploits over-sampling and noise-shaping techniques. Over-sampling compensates for coarse quantization with faster sampling speeds and converts a requirement for precise analogue components to one for high speed digital signal processing, thus easing the designer's burden. Noise-shaping is a method for shifting quantization noise to higher frequencies where it is easily suppressed by simple low-pass filtering. The resulting output is an accurate replica of the original analog input with the addition of shaped and filtered quantization noise.

An important difference between a conventional A/D converter and a $\Delta\Sigma$ A/D converter lies in the correspondence between the input and output sample values. With a conventional A/D, there is a one-to-one correspondence between the input and output sample values. In contrast, no such correspondence exists in the case of $\Delta\Sigma$ A/D converter: for any given point in time, the output sample values doesn't represent the input value at that point, but

rather it is the time-averaged value of the output that represents the input value.

2.2.1 Over-Sampling

Sampling and Quantization are used to convert a continuous analog signal into series of digital words. The Nyquist Sampling Theorem requires the sampling frequency, f_s , to be at least twice the maximum signal frequency, f_{max} , in order for the original analogue signal be faithfully recovered from the series of samples.

When converting from an analog signal to a digital signal, error is unavoidable. An analog signal is continuous, with ideally infinite precision, while the digital signal's precision is dependent upon the quantization resolution. The series of differences between actual analog values and their approximated digital values makes up what is called quantization noise. Quantization noise, e , is illustrated in Fig.2.8. The linear model for a quantizer is shown in Fig.2.9.

Figure 2.8: Illustration of Sampling and Quantization

Figure 2.9: Quantizer Linear Model

If e is regarded as having equal probability of lying anywhere in the range $\pm \frac{\Delta}{2}$, where Δ is the quantization step, the value of the total error power is given by

$$e_{rms}^2 = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \quad (2.5)$$

For a given sampling frequency f_s , the spectral density of the sampled noise is

$$E(f) = \sqrt{\frac{e_{rms}^2}{f_s/2}} = \sqrt{2} \frac{e_{rms}}{\sqrt{f_s}} \quad (2.6)$$

The quantization noise power that falls into a signal band $0 \leq f < f_{max}$ is given by

$$n_o^2 = \int_0^{f_{max}} E^2(f) df = e_{rms}^2 \frac{2f_{max}}{f_s} \quad (2.7)$$

Oversampling, the situation where $f_s > 2f_{max}$, has the effect of spreading a fixed amount of quantization noise power over a broader range of frequencies which is above the Nyquist frequency. The consequence of this is a reduction in the noise power in a given fixed bandwidth. In fact, each doubling of the sampling frequency halves the noise power appearing in this band. That is, it reduces the noise power available to contaminate the reconstructed analogue signal by one half. A graphical illustration is shown in Fig.2.10.

Figure 2.10: In-band Noise Decreases with Increasing Sampling Frequency

2.2.2 Noise-Shaping

Noise Shaping distributes noise energy unevenly over a frequency range. It is a technique that also can be used to shift noise to higher frequencies, outside of the band of interest.

First-order noise shaping in the frequency domain is equivalent to time domain differentiation of the quantization noise:

$$n_i = e_i - e_{i-1} \quad (2.8)$$

$$N(f) = E(f) \left| 1 - e^{-j\frac{2\pi f}{f_s}} \right| = 2e_{rms} \sqrt{\frac{2}{f_s}} \sin\left(\frac{\pi f}{f_s}\right) \quad (2.9)$$

The spectral density, before and after shaping, is shown in Fig.2.11. Noise within the band of interest is shifted to higher frequencies.

Figure 2.11: Noise Spectral Density before and after Shaping

2.3 First-Order $\Delta\Sigma$ Modulators

The block diagram for a typical first-order $\Delta\Sigma$ Modulator is shown in Fig 2.7, and the corresponding linear model in Fig 2.12 [NST96].

Figure 2.12: Linear Model of a First Order DSM

The addition of a quantizer to such a system makes it non-linear and its analytical solution very difficult if not impossible to obtain. In fact, to fully characterize the system in analytical form, one must make use of chaos theory.

The behaviour of the system can, however, be predicted using time-domain simulation methods.

The frequency domain linear model can provide us with some important system characteristics and usually can also provide adequate performance estimates for a wide variety of DSM architectures. In this thesis, both time-domain simulation and frequency domain linear approximation are used.

The output of the linear model (Fig.2.12) can be written:

$$y[n] = x[n-1] + e[n] - e[n-1] \quad (2.10)$$

The frequency-domain equivalent of this is:

$$Y(z) = z^{-1}X(z) + E(z)(1 - z^{-1}) \quad (2.11)$$

In the frequency domain, the output is the sum of an undistorted input and the first-order shaped quantization noise.

The total noise power in the band of interest is given by:

$$n_o^2 = \int_0^{f_o} |N(f)|^2 df = e_{rms}^2 \frac{\pi^2}{3} \left(2 \frac{f_o}{f_s}\right)^3, \quad f_s^2 \gg f_o^2 \quad (2.12)$$

In this case, it is seen that each doubling of the sampling frequency f_s reduces the in-band noise power to one eighth (9 dB) of the original value.

2.4 Second-Order $\Delta\Sigma$ Modulators

The in-band noise can be further reduced by increasing DSM order.

There are two ways to achieve higher order DSMs, namely Multi Stage Noise Shaping (MASH), and single-loop multi-order. These methods differ only at the circuit implementation level. They have identical system transfer functions which can be derived from the linear model. The pros and cons of these two approaches are described in [NST96].

A typical single-loop, second-order, DSM is shown in Fig.2.13.

Figure 2.13: Linear Model of a Second Order DSM

The output of this modulator can be written as:

$$y[n] = x[n-1] + (e[n] - 2e[n-1] + e[n-2]) \quad (2.13)$$

where the quantization noise is twice differentiated. The spectral density of the noise is given by:

$$N(f) = E(f)(1 - e^{-j2\pi f/f_s})^2 \quad (2.14)$$

The in-band noise power is given by

$$n_o^2 = \int_0^{f_o} |N(f)|^2 df = e_{rms}^2 \frac{\pi^4}{5} (2 \frac{f_o}{f_s})^5 \quad f_s^2 \gg f_o^2 \quad (2.15)$$

In this second-order case, the noise decreases by a factor of 32 (15 dB) for every doubling of f_s , compared to the factor of 8 (9 dB) which was obtained with the previously-discussed first-order DSM.

2.5 Higher-Order $\Delta\Sigma$ Modulators

Higher-order $\Delta\Sigma$ Modulators for even better in-band noise reduction are possible. In general, for an L-order system, the noise spectral density and power figures are:

$$N_L(f) = E(f)(1 - e^{-j2\pi\frac{f}{f_s}})^L \quad (2.16)$$

$$n_{oL}^2 = \int_0^{f_o} |N(f)|^2 df = e_{rms}^2 \frac{\pi^{2L}}{2L+1} \left(2\frac{f_o}{f_s}\right)^{2L+1} f_s^2 \gg f_o^2 \quad (2.17)$$

In the order-L case, the noise decreases by $3(2L+1)$ dB for every doubling of the sampling frequency. Tonal behaviour can be a problem in lower order modulators, especially first-order. Use of higher order significantly reduces this problem.

Although higher order DSMs can give superior performance, their use is discouraged by the difficulties in implementing circuits containing more than two integrators. Detailed discussions of the problem can be found in [NST96] and [CT92].

Chapter 3

Analysis of a Second-Order $\Delta\Sigma$ FD Having a Fractional-N Divider and a Multi-Bit Quantizer

In this chapter, the architecture of the new $\Delta\Sigma$ FD will be developed from a first-order $\Delta\Sigma$ FD design. Further refinements to this design result in the final device. The improvements on the starting first-order $\Delta\Sigma$ FD are:

- Second-order $\Delta\Sigma$ FD with integer-N divider and single-bit quantizer.

The slope of the noise shaping is increased from 20 dB/dec in the first-order circuit to 40 dB/dec in the second-order one. The increase in the amount of quantization noise power shifted to higher frequencies results in a higher in-band SNR.

- Second-order $\Delta\Sigma$ FD with fractional-N divider and single-bit quantizer.

The use of a fractional-N divider to reduce *total* quantization noise power will also bring about improved in-band SNR. Total quantization noise power is directly related

to the quantizer's minimum step size. The replacement of the integer-N divider with a fractional-N divider enables one to use smaller minimum quantizer step sizes. A $\frac{1}{8}$ fractional-N divider is used for the work described in this thesis, so that the minimum step size is reduced to $\frac{1}{8}th$ of that of the original, and the total noise power is reduced to $\frac{1}{64}th$ of the original.

- Second-order $\Delta\Sigma$ FD with fractional-N divider and multi-bit quantizer (the proposed architecture).

While a fractional-N divider reduces quantization noise and increases in-band SNR and frequency resolution, it does have a serious drawback: the input frequency range is reduced to $\frac{1}{8}th$ of the original one. This reduction in frequency range can be compensated by using a multi-bit quantizer (three bits in the present case).

3.1 First-Order $\Delta\Sigma$ FD

The block diagram for a first-order $\Delta\Sigma$ FD is shown in Fig.3.1 and its timing diagram is shown in Fig.3.2.

Figure 3.1: Block Diagram for a First-Order $\Delta\Sigma$ FD

Figure 3.2: Timing Diagram for a First-Order $\Delta\Sigma$ FD

In the block diagram shown in Fig.3.1, the divisor for the next f_{ref} cycle is controlled by the output of a D-type Flip Flop (DFF) functioning as a phase comparator: when the rising edge of the divided input signal f_{div} leads that of the reference signal f_{ref} , the DFF

output is high. This will cause the input signal, f_{in} , to be divided by $n + 1$ during the next cycle, and the rising edge of f_{div} to be delayed by one f_{in} period, T_{in} . Eventually, f_{div} will come to lag f_{ref} and the DFF output will go low. The input signal f_{in} will once again be divided by n , a situation that will persist until f_{div} eventually comes to lead f_{in} again.

For the system to work, f_{in} must satisfy:

$$nf_{ref} < f_{in} < (n+1)f_{ref} \quad (3.1)$$

If f_{in} is less than nf_{ref} , the DFF output will always be low. If f_{in} is greater than $(n+1)f_{ref}$, the output will be permanently high. These frequency restrictions of the $\Delta\Sigma$ FD are analogous to the voltage amplitude constraints to which a conventional $\Delta\Sigma$ modulator is subject to.

The first-order $\Delta\Sigma$ FD's output bit-stream corresponds to the instantaneous input frequency plus quantization noise.

3.1.1 Linear Model for Dual-Modulus Divider

Linearization of the dual modulus divider is the key to analyzing the behaviour of the first order $\Delta\Sigma$ FD . Phase information can be extracted from the timing diagram shown in Fig.3.2. An example of phase ramps for f_{ref} and f_{div} is illustrated in Fig.3.3.

Figure 3.3: Phase Ramps for f_{ref} and f_{div}

Where, t_k denotes the end of the k_{th} divider cycle.

The phase of f_{div} with respect to f_{ref} is given by:

$$\phi_{f_{div}} = 2\pi \frac{t_k}{T_{ref}} \quad (3.2)$$

$$t_k = \sum_{i=1}^k (n + b_i) T_{in}(k), \quad (3.3)$$

Where $T_{in}(k)$ is the average period of the input frequency during the k_{th} divider cycle, n is the base divisor (At any instant of time, the divider is dividing by n or by $n - 1$), and b_i may be either '0' or '1'.

The average frequency is

$$f_{in}(k) = \frac{1}{T_{in}(k)} = f_{nom} + f_{mod}(k), \quad (3.4)$$

Where f_{nom} is the nominal carrier frequency and $f_{mod}(k)$ the average modulating frequency added to f_{nom} during the k_{th} divider cycle.

The nominal divisor is the ratio

$$N = \frac{f_{nom}}{f_{ref}}, \quad (3.5)$$

Substitution of Eq(3.3), Eq(3.4) and Eq(3.5) into Eq(3.2) gives

$$\begin{aligned} \phi_{f_{ref}} &= 2\pi \frac{\sum_{i=1}^k (n + b_i) \frac{1}{f_{in}(k)}}{T_{ref}} \\ &= 2\pi \sum_{i=1}^k \left[\frac{1}{N} (n + b_i) \frac{f_{nom}}{f_{in}(k)} \right] \end{aligned} \quad (3.6)$$

A block diagram for the linearized circuit model is shown in Fig.3.4.

Figure 3.4: Linear Model for Dual-Modulus Divider

3.1.2 Linear Model for a First Order $\Delta\Sigma$ FD

The complete model for a first-order $\Delta\Sigma$ FD can now be obtained through the inclusion of a divider, a phase detector and a one-bit quantizer.

Figure 3.5: Linear Model for a First-Order $\Delta\Sigma$ FD

If the input instantaneous frequency is given as in Eq.3.7 (a special case of the generic

form in Eq.2.1).

$$f_{in} = f_{nom} + \Delta f \sin(\Omega t) \quad (3.7)$$

Where f_{nom} is the nominal carrier frequency, Δf the maximum frequency deviation, and Ω the modulating frequency.

The output of the system in Fig.3.5 is

$$Y_{out} = N - n + \frac{\Delta f}{f_{ref}} \sin(\Omega t + \theta) + (1 - z^{-1})E_n \quad (3.8)$$

Where $N = \frac{f_{nom}}{f_{ref}}$, the ratio of nominal carrier frequency to reference frequency, n is the base divisor and E_n is the quantization noise spectral density. The output contains a DC offset $(N - n)$ proportional to the center frequency offset, an undistorted and scaled version of the modulation signal, and first-order differentiated quantization noise.

3.1.3 Performance Evaluation

When the input frequency to a first-order $\Delta\Sigma$ FD is constant, the quantization noise will not be white, as previously assumed in Chapter 2. In this case, the linear model fails to describe the operation of the system accurately.

To sidestep this problem and evaluate the performance, a sinusoidally-modulated input frequency (Eq.3.7) is used.

Signal-To-Noise Ratio(SNR), the ratio of Signal Power to Noise Power within a prescribed band, is the performance metric of interest.

If f_{low} and f_{high} are the band boundaries, the total in-band noise power is:

$$S_{noise} = E_n^2 \int_{f_{low}}^{f_{high}} |1 - e^{-j\frac{2\pi f}{f_{ref}}}|^2 df, \quad (3.9)$$

Where

$$E_n^2 = \frac{\Delta^2}{12f_s} \quad (3.10)$$

$$\Delta = f_{ref} \quad (3.11)$$

$$f_s = f_{ref} \quad (3.12)$$

The signal power is given by

$$S_{sig} = \frac{\Delta f^2}{2} \quad (3.13)$$

Where Δf is the maximum frequency deviation, as expressed in Eq.3.7.

In order to compare analytical results with simulation results, numbers are substituted into the equations.

Δf , the maximum frequency deviation, has to be $< \frac{f_{ref}}{2}$ in order for the system not to saturate, as described in Eq.3.1.

Because the reference clock, f_{ref} , is also the sampling frequency in the system, Ω , the modulating frequency, has to be $< \frac{f_{ref}}{2}$ to satisfy Nyquist's Law.

Let $f_{ref} = 10 \text{ MHz}$, $\Delta f = -10 \text{ dB}$ of full range $\frac{f_{ref}}{2}$, $f_{low} = 10 \text{ kHz}$, $f_{high} = 200 \text{ kHz}$, and $\Omega = 50 \text{ kHz}$

The SNR predicted by theory (Eq.3.9) is compared to that computed by simulation shown in Fig.3.6 over the bandwidth from $f_{low} = 10 \text{ kHz}$ to $f_{high} = 200 \text{ kHz}$.

The equation predicts that SNR in the band will be 31.54 dB .

The Matlab simulation result finds the SNR to be 31.7 dB using Eq.3.14.

$$SNR = \frac{\sum(\text{SignalPowerat } 50 \text{ kHz FFTbin})}{\sum(\text{FFTbins from } 10 \text{ kHz to } 200 \text{ kHz}) - \sum(\text{SignalPowerat } 50 \text{ kHz FFTbin})} \quad (3.14)$$

Figure 3.6: Simulation of First Order $\Delta\Sigma$ FD

This is a rather good agreement, and the SNR calculated by simulation will henceforth be used as a benchmark.

The diagram illustrates the proposed PLL architecture. It consists of the following blocks and signal flow:

- Inputs:** f_{in} and f_{ref} .
- MMD Block:** Receives f_{in} and the output of the summing junction. Its output is fed into the PFD block.
- PFD Block:** Receives the output of the MMD block and f_{ref} . Its output is fed into the CP block.
- CP Block:** Receives the output of the PFD block. Its output is fed into the integrator block.
- Integrator:** Represented by an integral symbol $\int$. Its output is fed into the quantizer block.
- Quantizer:** Represented by a square wave symbol. Its output is Y_{out} .
- Feedback Path:** Y_{out} is fed into a delay block $2-Z^{-1}$. The output of this block is added to a noise signal n at a summing junction (represented by a circle with a plus sign).

The block diagram illustrates a closed-loop control system with a feedforward path. The input f_{in} is processed by a block $F_{nom}/()^{-1}$ and then multiplied by the output of a summing junction. This summing junction also receives a disturbance n and a feedback signal from a delay block $2-Z^{-1}$. The resulting signal passes through a block $\frac{1}{N}$ and then a block $\frac{2\pi}{1-Z^{-1}}$. This signal is added to the output of a feedforward path, which consists of a block $\frac{2\pi}{1-Z^{-1}}$ receiving a reference input of 1. The sum of these two paths then passes through a block $\frac{1}{1-Z^{-1}}$. Finally, the output Y_{out} is added to a noise signal $E_n(z)$ at a summing junction. The output Y_{out} is also fed back through the delay block $2-Z^{-1}$ to the disturbance summing junction.

Reproduced with permission of the copyright owner. Further reproduction prohibited without permission.

The output of the system is given by:

$$Y_{out} = N - n + \frac{\Delta f}{f_{ref}} \sin(\Omega t) + (1 - z^{-1})^2 E_n, \quad (3.15)$$

and the system noise power is

$$S_{noise} = E_n^2 \int_{f_{low}}^{f_{high}} |1 - e^{-j \frac{2\pi f}{f_{ref}}}|^4 df \quad (3.16)$$

The quantization noise, as shown in Eq.3.15, is second-order differentiated, so that more noise will be shifted upwards in frequency and out of the band of interest.

The theoretical performance of the second order system was compared to simulation results and the SNR calculated with E_n^2 , Δ and f_s retaining their values from the first-order example.

The Matlab simulation result is shown in Fig.3.9.

Figure 3.9: Matlab Simulation Result for the Second Order $\Delta\Sigma$ FD

The theoretically-predicted SNR was 51.73 dB, a figure nearly 20 dB greater than that of the first-order $\Delta\Sigma$ FD. The difference can be attributed to decreased in-band quantization noise.

The *SNR* found by simulation was about 4 dB lower than the theoretical result. The main reason for the difference is the linear model's inability to account for the non-linear nature of the system.

3.3 Second-Order FD with Fractional-N Divider

Further reduction in overall quantization noise power may be had if the quantization step size is reduced.

In the systems described previously, the divisor is restricted to integer values (n and $n + 1$), and the minimum quantization step size is correspondingly restricted. If, however, a non-integer divisor was available, finer control over this step size could be achieved and the quantization noise power would be reduced to a fraction of what it would be otherwise. This has been done, with the divider being implemented by an accumulator-based circuit.

In the past, this approach to fractional-N division has been beset by truncation-related discrete spurs [Cra94]. The many ways of suppressing these spurs proposed to date have all involved the use of difficult-to-implement precision analog circuits. One example is shown in Fig.3.10 [Roh83]. It is very difficult to create a precise match between the D/A output and phase error signal.

Figure 3.10: An Example of Phase Error Cancellation in Fractional-N Frequency Synthesis

A novel approach to implement a spur-free fractional-N divider is illustrated in Fig.3.11. The multi-modulus divider has two outputs: f_{d0} and f_{d1} , f_{d0} is one T_{in} ahead of f_{d1} . These two signals, along with the Selector and the Phase Frequency Detector (PFD)/Charge Pump (CP) array, form a D/A for cancelling out the truncation error from the accumulator.

Figure 3.11: Block Diagram for a Second-Order $\Delta\Sigma$ FD With Fractional-N Divider

Other architectures incorporating a separate D/A in the feedback path focus on techniques to match the D/A output charge with the charge transferred through the PFD and CP. In the architecture shown in Fig.3.11, the components making up the D/A are actually the Selector, the PFDs and CPs. Therefore no separate D/A is needed and no mismatch between the D/A and the charge pump exists. The mismatch errors that cannot be eliminated (except through careful layout techniques) include those due to f_{d1} not being delayed by exactly one T_{in} cycle, delay mismatches in the selector, and mismatches in the PFD/CP

elements. This approach anticipates advantages of applying dynamic element matching techniques to those mismatches.

A linear model for the system is shown in Fig.3.12.

Figure 3.12: Linear Model of Second Order $\Delta\Sigma$ FD with Fractional-N Divider

Referring to the linear model, a proof that the accumulator truncation error (ϵ_i) is cancelled and does not appear at the Charge Pump output proceeds as follows:

$$\phi_{fd0} = \frac{2\pi}{N} \frac{1}{1-Z^{-1}} \frac{f_{nom}}{f_{in}} (n + C_i) \quad (3.17)$$

$$\phi_{fd1} = \frac{2\pi}{N} \left(\frac{1}{1-Z^{-1}} \frac{f_{nom}}{f_{in}} (n + C_i) + \frac{f_{nom}}{f_{in}} \right) \quad (3.18)$$

$$C_i = \frac{X_i}{8} - (1-Z^{-1})\epsilon_i \quad (3.19)$$

$$R_i = 8\epsilon_i \quad (3.20)$$

$$\phi_{sum} = (8 - R_i)(\phi_{fref} - \phi_{fd0}) + R_i(\phi_{fref} - \phi_{fd0}), \quad (3.21)$$

Where X_i is the output of the $2 - Z^{-1}$ block, C_i and R_i the accumulator carry and remainder outputs, respectively.

Some substitutions put Eq.3.21 into the form:

$$\begin{aligned}\phi_{sum} &= \frac{2\pi}{1-Z^{-1}} \left\{ 8 \left[1 - \frac{1}{N} \frac{f_{nom}}{f_{in}} \left[n + \frac{x_i}{8} + (1-Z^{-1})\varepsilon_i \right] \right. \right. \\ &\quad \left. \left. - \frac{1}{N} (1-Z^{-1}) 8\varepsilon_i \right] \right\} \\ &= \frac{2\pi}{1-Z^{-1}} 8 \left\{ 1 - \frac{1}{N} \frac{f_{nom}}{f_{in}} \left[n + \frac{x_i}{8} \right] \right\}\end{aligned}\quad (3.22)$$

ϕ_{sum} is independent of ε_i , as was to be shown.

The output of the system derived from the linear model is given by:

$$Y_{out} = N - n + \frac{\Delta f}{f_{ref}} \sin(\Omega t + \theta) + (1 - Z^{-1})^2 E_n \quad (3.23)$$

This is the same expression as Eq.3.15, except that now the value of E_n is $\frac{1}{8}$ of that in Eq.3.15.

This method of reducing noise power also causes the full scale frequency deviation f_{mod} to be reduced to one eighth of the original, from $\pm \frac{f_{ref}}{2}$ to $\pm \frac{f_{ref}}{16}$. This drawback can be compensated through the use of a multi-bit quantizer, as will be shown in next section.

The results of simulating both types of second-order FDs are plotted in Fig.3.13. In each case, the same input was used: the modulating frequency was $\Omega = 50 \text{ kHz}$ and frequency deviation $f_{mod} = -10 \text{ dB}$ of $\frac{f_{ref}}{16}$.

Analysis indicates that the SNR of an FD using a fractional-N divider is better than that obtained with an integer-N architecture by $20 \log_{10} 8 = 18 \text{ dB}$, in agreement with time-domain simulation results.

Figure 3.13: Integer-N versus Fractional-N Divider Comparison

3.4 A Second-Order $\Delta\Sigma$ FD Using a Fractional-N divider and a Three-Bit Quantizer (Proposed Architecture)

As described in the previous section, the use of a fractional-N divider is accompanied by a reduced input frequency range. This drawback is overcome when the single-bit quantizer is replaced with a multi-bit quantizer. In particular, a 3-bit quantizer can restore the input frequency range to $\pm \frac{f_{ref}}{2}$. This is a feature of the proposed architecture. A block diagram is shown in Fig.3.14. This block diagram is identical to Fig.3.11, except that now the single-bit quantizer is replaced by a 3-bit quantizer. The corresponding linear model is that shown in Fig.3.15.

Figure 3.14: Second-Order $\Delta\Sigma$ FD with Fractional-N Divider and Multi-Bit Quantizer

The expression for Y_{out} is the same as for the single-bit case, but the input frequency

Figure 3.15: Linear Model for Figure 3.14

range is now $\pm \frac{f_{ref}}{2}$. The size of the input step corresponds to $\frac{1}{8}$ of an input frequency period at the PFD input.

3.5 Comparison

The comparison of the different $\Delta\Sigma$ FD architectures described in the previous sections is presented in Table.3.1.

System Type	Input Range	Quantization Step	SNR @ $\Omega = 50 \text{ kHz}$ $\Delta f = -10 \text{ dB}$ of $\frac{f_{ref}}{16}$ 10 kHz – 200 kHz Bandwidth
1st Order	$\pm \frac{f_{ref}}{2}$	f_{ref}	13.71 dB
2nd Order Integer-N	$\pm \frac{f_{ref}}{2}$	f_{ref}	29.15 dB
2nd Order Fractional-N	$\pm \frac{f_{ref}}{16}$	$\frac{f_{ref}}{8}$	46.68 dB
2nd Order Fractional-N Multi-Bit	$\pm \frac{f_{ref}}{2}$	$\frac{f_{ref}}{8}$	46.68 dB

Table 3.1: $\Delta\Sigma$ FD Architecture Performance Comparison

Fig.3.16 shows SNR versus input frequency deviation for cases 2,3 and 4 in Table.3.1.

From table.3.1 and Fig.3.16, it can be seen that the second-order $\Delta\Sigma$ FD with fractional-N divider has higher SNR (about 18 dB) than the one with integer-N divider for the same input. By using a 3-bit quantizer, the second-order $\Delta\Sigma$ FD with fractional-N divider has the same full scale input range as the one with integer-N divider.

Figure 3.16: SNR vs Input Frequency Deviation

3.6 Effects Of System Parameters on Performance

The system parameters: f_{ref} (reference clock), f_{nom} (carrier frequency), Δf (maximum frequency deviation), Ω (modulating frequency) and n (base division ratio) are related. Once the application-dependent values of f_{nom} , Δf and Ω have been specified, f_{ref} and n can be determined:

f_{ref} and n must be chosen so as to satisfy the input range requirement:

$$nf_{ref} < f_{nom} \pm \Delta f < (n+1)f_{ref}, \quad (3.24)$$

and f_{ref} must not violate the Nyquist criterion:

$$\Omega < \frac{f_{ref}}{2} \quad (3.25)$$

In this thesis, typical values of $f_{nom} = 1 \text{ GHz}$, $\Delta f = 1 \text{ MHz}$ and $\Omega = 50 \text{ kHz}$ are chosen as an example. For any given values of f_{nom} , Δf and Ω , there are many f_{ref}, n combinations that can satisfy Eq.3.24 and Eq.3.25. Four sets of the combinations are chosen to evaluate their influence on system performance. The results are shown in Table.3.2.

#	f_{ref}	n	SNR (simulation)
	Hz		10 kHz 200 kHz Bandwidth dB
1	5 M	200	56.40
2	10 M	100	61.57
3	20 M	50	69.87
4	40 M	25	75.05

Table 3.2: Simulation Result for Different Combinations of f_{ref} and n

With each doubling of f_{ref} , the quantization noise PSD $E_n^2 = \frac{\Delta^2}{12f_s}$ doubles, but the effects of this doubling are outweighed by the simultaneous doubling of the sampling frequency (see Eq.2.15). The total noise in the band of interest decreases. Therefore, the net effect of increasing f_{ref} is to improve the SNR.

3.7 System Noise Analysis

System noise is an important performance determinant and a careful analysis is essential to an evaluation of the new architecture's feasibility. Such an analysis will allow noise sources and their relative importance to be identified so that design efforts can be appropriately focused.

The noise generated in each block of this architecture is modified by a characteristic transfer function, such as a high-pass or a low-pass one. In preparation to analyzing the effects of noise in different blocks, the new architecture's linear model (Fig.3.15) is redrawn as Fig.3.17.

Figure 3.17: Linear Model of 2nd-Order Fractional-N $\Delta\Sigma$ FD

In the interest of clarity, the original figure has been condensed, with the functions of the circuit blocks being depicted mathematically.

In each block, information is carried in different formats. The input to the $\Delta\Sigma$ FD (in particular, the divider) takes the form of frequency in units of hertz. The divider functions as a perfect integrator whose output is in units of radians. The PFD generates pulses with their widths, in units of seconds, proportional to the phase difference at the input of the PFD. The charge pump produces a current pulse, with units of amperes, that has a duration

that is proportional to the width of the pulse from the PFD. At the output of the integrator, the information is carried in the form of voltage, in units of volts, which is proportional to the current produced by the charge pumps. The quantizer digitizes the voltage and represents the information in discrete numbers. The feedback loop converts the number back to frequency. The system compares the feedback output with the input frequency and tries to minimize the error.

The system output in Fig.3.17 is given by:

$$f_{out} = \left(\frac{f_{in}}{n} - f_{ref} \right) \frac{K_{div} K_{pfd} K_{cp} F(z) K_{quan}}{1 + K_{div} K_{pfd} K_{cp} F(z) K_{quan} B(z)} = 8n \left(\frac{f_{in}}{nf_{ref}} - 1 \right) \quad (3.26)$$

Where,

- $K_{div} = \frac{2\pi}{1-z^{-1}} T_{ref}$ is the transfer function of divider, in units of radians/hertz.
- $K_{PFD} = \frac{T_{ref}}{2\pi}$ is the gain of the PFD, in units of seconds/radian.
- $K_{CP} = \frac{I_p}{T_{ref}}$ is the gain of the CP, in units of amperes/second.
- $F(z) = \frac{z^{-1}}{C(1-z^{-1})} T_{ref}$ is the transfer function of integrator, in units of volts/ampere.
- $K_q = \frac{1}{\frac{T_{in}}{8} \frac{I_p}{C}}$ is the gain of the quantizer, in units of numbers/volt.
- $B(z) = \frac{f_{in}}{8n} (2 - z^{-1})$ is the transfer function of the feedback block, in units of hertz/number.
- I_p is the source current of the charge pump, in unit of ampere.
- C is the integrator capacitor value, in units of farads.

The output f_{out} is in form of discrete numbers from 0 to 7 representing the actual frequency deviation from 0 to f_{ref} .

The transfer functions seen by noise signals at various points in the system will now be developed.

3.7.1 Quantization Noise Transfer Function

Letting n_o be the output noise power, and n_{quan} the quantizer noise power, we have

$$\frac{n_o}{n_{quan}} = \frac{1}{1 + A_{ol}} \quad (3.27)$$

Where A_{ol} is the open loop gain:

$$A_{ol} = K_{div}K_{pfd}K_{cp}F(z)K_qB(z) = \frac{(2 - z^{-1})z^{-1}}{(1 - z^{-1})^2}$$

Thus,

$$\frac{n_o}{n_{quan}} = (1 - z^{-1})^2 \quad (3.28)$$

3.7.2 f_{in} Noise Transfer Function

$$\frac{n_o}{n_{f_{in}}} = \frac{1}{n} \frac{K_{div}K_{pfd}K_{cp}F(z)K_q}{1 + A_{ol}} = \frac{8}{f_{ref}} z^{-1} \quad (3.29)$$

3.7.3 f_{ref} Noise Transfer Function

$$\frac{n_o}{n_{f_{ref}}} = \frac{K_{div}K_{pfd}K_{cp}F(z)K_q}{1 + A_{ol}} = \frac{8n}{f_{ref}} z^{-1} \quad (3.30)$$

3.7.4 Divider Noise Transfer Function

$$\frac{n_o}{n_{div}} = \frac{K_{pfd}K_{cp}F(z)K_q}{1 + A_{ol}} = \frac{8n}{2\pi} (1 - z^{-1}) z^{-1} \quad (3.31)$$

3.7.5 PFD and CP Noise Transfer Function

The noise originating in the PFD and CP blocks is combined, as measurement or simulation of the noise at the phase detector output is difficult.

$$\frac{n_o}{n_{PFD_CP}} = \frac{F(z)K_q}{1 + A_{ol}} = \frac{8n}{I_p}(1 - z^{-1})z^{-1} \quad (3.32)$$

3.7.6 Integrator Noise Transfer Function

$$\frac{n_o}{n_{int}} = \frac{K_q}{1 + A_{ol}} = \frac{8n}{\frac{I_p}{c}T_{ref}}(1 - z^{-1})^2 \quad (3.33)$$

3.7.7 Quantizer Noise Transfer Function

The quantizer circuit noise is treated in the same manner as quantization noise, as shown in Eq.3.27.

All of the NTFs (Noise Transfer Functions) are plotted in Fig.3.18. The system parameters used to obtain these are:

$$n = 100, f_{ref} = 10 \text{ MHz}, I_p = 200 \text{ uA}, C = 1 \text{ pF}$$

Fig.3.18 shows that noise from f_{in} and f_{ref} has no shaping. Noise from the divider, PFD and CP are subject to first-order shaping, and those from the integrator and quantizer are subject to second-order shaping.

Later, in Chapter 4, these transfer functions will be used to predict the effect of simulated circuit noise on the system.

Figure 3.18: Noise Transfer Function at Various Circuit Nodes

3.8 Circuit Performance Improvement Techniques

In this section, some system level approaches to minimize the adverse affects of circuit non-idealities are described.

CMOS VLSI processes are typically optimized for high-density digital design and not high precision analog design. Mismatches between the charge pumps and PFDs is inevitable, and can lead to increased in-band noise levels and reduced SNR.

A technique called Data Weighted Averaging (DWA) has been exploited in this design

to lessen these mismatch effects. This technique [BF95] [NH96] performs a first-order shaping of the mismatch caused distortion, and moves noise to higher frequencies where it can be removed by filtering.

Figure 3.19 shows the fundamental principle behind this technique, using the simple case of a 2-element CP array. To represent the effect of CP output error, each of the two CPs has an output 10% above or below the desired current. The output current errors will average to zero when both CPs contribute to the output, but if only one contributes, a net 10% error will appear in the output as illustrated in Fig.3.19. This suggests that errors resulting from the non-ideal implementation of analog circuits can be reduced if the outputs of several CPs are averaged to produce the final output.

Figure 3.19: CP Output with (a) no DWA, and (b) DWA

The element selection process used in DWA must ensure that the work is apportioned equally among the CPs in the array. This is done by a cyclic element selection process whose concept of operation is illustrated in Fig.3.20 [BF95] [NH96].

Figure 3.20: DWA for Eight Elements - Input Sequence: 011, 100 and 010

In the figure above, an array of eight CPs is used. For each new input sequence, the elements that are adjacent to those used in the previous input sequence will be selected. To express this algorithm mathematically, one can begin by imagining an infinite element array and a pointer $ptr(k)$ containing the address of the first cell of the $(k+1)_{th}$ selection. At each clock cycle, this pointer is incremented by the input code $x(k)$:

$$ptr(k) = ptr(k-1) + x(k) \quad (3.34)$$

The mismatch error at cycle k is

$$y_{mis}(k) = \sum_{i=ptr(k-1)}^{ptr(k)-1} w_i - x(k)w_{mean} \quad (3.35)$$

Where the w_i are the ‘weights’ of the elements and w_{mean} their average

$$w_{mean} = \frac{1}{N} \sum_{i=0}^{N-1} w_i$$

In the absence of mismatches, $w_0 = w_1 = \dots = w_{N-1}$.

Eq(3.35) can be re-written in the form:

$$y_{mis}(k) = IM(ptr(k)) - IM(ptr(k-1)) \quad (3.36)$$

Where $IM(ptr)$ is the Integral Mismatch Function [BF95] [NH96].

$$IM(ptr) = \sum_{i=0}^{ptr-1} (w_i - w_{mean}) \quad (3.37)$$

$y_{mis}(k)$ is obtained by first-order differentiation of the function $IM(ptr)$ and so benefits from first-order noise shaping. It has been proven that for random input signals, $IM(ptr)$ has a white spectrum [NH96].

The circuit implementation for the DWA block is described in Chapter 4.

Simulations of the second-order $\Delta\Sigma$ FD with fractional-N divider and multi-bit quantizer were run with three cases: no CP mismatch, CP mismatch 10% with DWA and CP mismatch without DWA. The results are captured in Fig.3.21. The in-band first-order shaping on noise from the CP mismatch reduces the total in-band noise, and therefore increases SNR.

Figure 3.21: Comparison between no CP Mismatch, CP Mismatch with and without DWA

3.9 Summary

In this chapter, a system level analysis of different $\Delta\Sigma$ FD architectures was presented. In the next chapter, the circuit level implementation of the new architecture is presented.

Chapter 4

Circuit Design and Simulation Results

This chapter describes the $\Delta\Sigma$ FD design at the circuit level using a TSMC 0.18 μm CMOS process. The design goal is validation of the system architecture discussed in Chapter 3, and not to create a circuit optimized for lowest power consumption, lowest noise, or smallest area.

The partitioning of the system into circuit blocks is shown in Fig.4.1.

Figure 4.1: System Block Diagram

The system has two inputs: f_{in} , a frequency-modulated carrier and f_{ref} , a 10MHz ref-

erence clock. f_{in} is chosen to fall in the range $nf_{ref} < f_{in} < (n+1)f_{ref}$, where n is the base divisor of the MMD.

The circuit operates as follows: The PFD compares the phase of f_{div} , the divided down version of f_{in} , to that of f_{ref} and generates two pulses, PU and PD , which are used as inputs to the CP. The difference between the width of these two pulses is proportional to the phase difference between f_{div} and f_{ref} . The CP acts as a current source when PU is high and a current sink when PD is high. The net current is converted to a voltage by the integrator, whose output is sampled by the 3-Bit Quantizer. The quantizer's 3-Bit output, which is also the $\Delta\Sigma$ FD's output, is used by the Digital Feedback block to generate the next MMD divisor. The feedback loop is closed by sending the new N to the MMD.

The output of the system is the 3-Bit data stream from the Quantizer and represents the deviation of f_{in} from its nominal constant carrier frequency.

This system is a mixed-signal system with digital and analog components working together to perform the overall system function. The relationship between the analog and digital design flows is illustrated in Fig.4.2. The design tools used at each of the indicated stages are also named.

Implementation details of each circuit block are described in the following sections.

Figure 4.2: $\Delta\Sigma$ FD Design Flow and Tools Used

4.1 f_{in} and f_{ref} Input Buffers

These input buffers convert applied analog sinusoidal waveforms to digital (CMOS) levels. The simplified schematic used for both buffers is shown in Fig.4.3.

Figure 4.3: Input Buffer

Feedback is used to linearize the first stage and so reduce the input noise gain. Furthermore, a larger $\frac{W}{L}$ was used in the first stage to reduce the circuit-generated noise. In principle, greater channel area means less $\frac{1}{f}$ noise and thermal noise, but requires more current for speed,

The design of the f_{in} input buffer differs from that of the f_{ref} buffer only in transistor sizing. Device sizes need to be scaled down because of the higher frequencies involved.

4.1.1 Simulation Results

Operation of the f_{ref} and the f_{in} input buffers was simulated using Spectre. The simulation results are shown in Fig.4.4 and Fig.4.5.

Figure 4.4: f_{ref} Input Buffer Operation

Figure 4.5: f_{in} Input Buffer

4.1.2 Phase Noise Performance

The phase noise seen at the buffers' output has two sources – one source is the phase noise already present in the input signal, about which nothing can be done, and the second source is that generated internally by the buffer. A design goal is that phase noise added by the input buffer must be 3 dB below the specified input phase noise. A typical low noise 10 MHz reference clock produced by a signal generator, HP8663A for example, has a phase noise of -147 dBc/Hz@10 kHz.

Spectre PSS simulation was used to predict the phase noise spectra at the f_{ref} (10 MHz) and f_{in} (1 GHz) buffer outputs. The results are shown in Fig.4.6 and Fig.4.7, respectively.

Fig.4.6 shows that noise added by the f_{ref} input buffer is much less than that present in the input signal.

The relative importance of the phase noise present in the f_{ref} and f_{in} input signals will be evaluated later in this chapter.

Figure 4.6: Output Phase Noise of f_{ref} Buffer

Figure 4.7: Output Phase Noise of f_{in} Buffer

4.2 Programmable Multi-Modulus Divider

The programmable Multi-Modulus Divider (MMD) divides the input frequency by a divisor determined by the output of the Digital Feedback block. The MMD structure used in this work, one consisting of a Prescaler and two down-counters, is shown in Fig.4.8.

Figure 4.8: Programmable Multi-Modulus Divider

The MMD works by dividing f_{in} by a number $P + 1$ for a period of time and then by P for a period of time. The total time for these operations is one cycle of the output frequency, f_{div} .

Let the first period of time be equal to A periods of a waveform whose frequency is $\frac{f_{in}}{P+1}$ and the second be ' $M-A$ ' periods of a waveform with frequency $\frac{f_{in}}{P}$.

The total time required for the two-modulus division is $T_{div} = \frac{A}{f_{in}/(P+1)} + \frac{M-A}{f_{in}/P}$ seconds, or $T_{div} = \frac{A+MP}{f_{in}}$ seconds. The output frequency of the divider can be given by:

$$f_{div} = \frac{f_{in}}{N} \quad (4.1)$$

Where $N = A + MP$, $f_{div} = \frac{1}{T_{div}}$.

In this thesis, a 5-bit M-counter and a 2-bit A-counter are used. A value of 4 for P was chosen so that the divisor components can be expressed in the simple binary format ($N = M_4M_3M_2M_1M_0A_1A_0 = 4M + A$).

4.2.1 Prescaler

The prescaler divides f_{in} by either 4 (P) or 5 ($P+1$). The divisor is determined by the state of the div_p input: $div_p = 0[1] \rightarrow \text{divide by 4}[5]$

Figure 4.10: Schematic for Prescaler

Present state	Next state divide by 4	Present state	Next State divide by 5	Invalid state	Next State divide by 4	Next State divide by 5
000	001	000	001	010	000	100
001	011	001	011	101	010	010
011	110	011	110	111	110	110
110	000	110	100	100	000	
		100	000			

Table 4.1: Prescaler State Table

4.2.2 M-Counter

After the M-counter's initial value, M , has been loaded, the counter proceeds to decrement.

On reaching zero, the M-counter generates the load signal, ld , which causes the MMD to return to its initial state, where both counters are reloaded and div_p reset to zero. During

counting, the M-counter's changing output states are decoded to produce timing signals needed by other parts of the FD. The schematic for the M-counter is shown in Fig.4.11.

Figure 4.11: Schematic for M-Counter

4.2.3 A-Counter

After the initial value of A is loaded, this counter decrements to zero. When zero ($Q_1Q_0 = '00'$) is reached, div_p goes high. The counter is 'frozen' in this last state until ld is activated at the end of the state sequence. The schematic for the A-counter is shown in Fig.4.12.

Figure 4.12: Schematic for A-Counter

4.2.4 Decoding of M-Counter States

As mentioned previously, timing signals needed by other FD components are derived from the M-counter's output states.

There are four outputs from the M-counter decoding circuit:

- f_{div} : input to the PFD for phase comparison with f_{ref} .

- $Quan_{clk}$: clock signal to the Quantizer.
- $Digblk_{clk}$: clock signal to the Digital Feedback Block.
- ld : load signal to initialize the MMD and reload the M-counter and the A-counter.

The timing relationships between those outputs are as follows:

Even when the loop is locked, f_{ref} leads f_{div} by a fixed time period because of the way PFD is designed, which is to be described in the next section. As a result, PU and PD have nearly equal durations when the loop is locked. The integrator converts the net transferred charge to a voltage which is sampled by the 3-bit quantizer after a settling time. There is , therefore, a time gap between the divider output f_{div} and the clock $Quan_{clk}$ that triggers the sampling.

The 3-bit digitized signal is fed to the Digital Feedback Block which uses it to generate a new divisor in time for the next cycle. The clock $Digblk_{clk}$ to the Digital Feedback Block must be delayed somewhat so that the quantizer data will be the most-recent.

The relationships between these outputs is illustrated in Fig.4.13.

Table.4.2 shows the relation between M-counter states and the four timing signals generated.

Decoder Output	Corresponding States
f_{div}	$\bar{Q}_4 Q_3 Q_2 \bar{Q}_1 \bar{Q}_0$
f_{quan}	$Q_4 Q_3 Q_2 \bar{Q}_1 \bar{Q}_0$
f_{fdb}	$Q_4 Q_3 Q_2 \bar{Q}_1 Q_0$
ld	$Q_4 Q_3 Q_2 Q_1 \bar{Q}_0$

Table 4.2: Decoder Outputs

Figure 4.13: Mapping of M-counter States to MMD Timing Signals

4.3 Phase-Frequency Detector

The PFD converts the phase error to pump-up and pump-down pulse signals (PU and PD), the difference in widths of these being proportional to the phase error. The difference is positive when f_{ref} leads f_{div} and negative when f_{ref} lags f_{div} . The detector is such that a phase error of $+2\pi$ occurs when the PU pulse width is T_{ref} and the PD width is zero, so the PFD gain is $K_{PFD} = \frac{T_{ref}}{2\pi}$.

The schematic for the PFD is shown in Fig.4.15.

Figure 4.15: A schematic for a PFD

The circuit functions as follows:

If f_{ref} leads f_{div} , the rising edge of f_{ref} sets PU high, where it remains until the rising edge of f_{div} arrives and sets PD high. PU and PD are logically 'and'ed to form a short reset pulse to clear both outputs. The width of the PU pulse is proportional to the phase difference between f_{ref} and f_{div} .

If f_{div} leads f_{ref} , the rising edge of f_{div} sets PD high, where it remains until the rising edge of f_{ref} arrives and sets PU high. PU and PD are logically 'and'ed to form a short

reset pulse to clear both outputs. The width of the PD pulse is proportional to the phase difference between f_{div} and f_{ref} .

The above circuit has a dead-zone problem when the widths of the PU and the PD pulses are comparable to their transition rising/falling times, as may happen when the phase error is close to zero. A solution to this problem, which also improves PFD linearity, is to introduce a fixed DC phase offset to move the lock point away from the zero phase error point, as illustrated in Fig.4.16.

Figure 4.16: PFD with DC offset

When the loop is locked, f_{ref} will always lead f_{div} for a fixed time period, thus establishing a minimum PU pulse width. The circuit is designed to emit a PD pulse of exactly the same length. The charge transferred to the integrator during the minimum PU time is

removed during the PD time and the net effect on the integrator output (the error voltage) will be zero. The loop will remain locked in spite of the introduction of the phase offset.

The downside of this approach is that since the duty cycle of PU and PD is no longer zero at the lock point, the charge pump will always operate for a minimum time equal to double the PD pulse width in each f_{ref} cycle. The system noise contribution will increase. The reference feed-through will also increase.

Fig.4.17 and Fig.4.18 show simulations of the PFD with offset in the cases where f_{ref} leads and lags f_{div} :

Figure 4.17: PFD Transition Simulation: Fref Leading Fdiv

Figure 4.18: PFD Transition Simulation: Fref Lagging Fdiv

There are eight such PFDs used in this design, forming an array of eight PFDs. This array of eight PFDs is a part of the truncation error suppression scheme used in the new architecture for the fractional-N divider, as described in Chapter 3.

4.3.1 PFD Noise Performance

The PFD noise will be analyzed together with the CP noise as described in the next section.

4.4 Charge Pump

The Charge Pump (CP) converts the difference between the PU and the PD pulse widths to an average current output during one f_{ref} cycle. If the widths are t_{PU} and t_{PD} , the average current will be $I = \frac{I_p}{T_{ref}}(t_{PU} - t_{PD})$. The gain of the CP can be given by:

$$K_{CP} = \frac{I_p}{T_{ref}} \quad (4.2)$$

Where I_p is the constant current flow during a pump up or a pump down interval.

The schematic for one CP used in this design is shown in Fig.4.19.

The CP has three sections:

- Band Gap: provides an accurate current reference that is robust with regard to process, voltage and temperature variations.
- Mirror : forces source and sink currents to be equal and equal-to the band gap reference current.
- Charge Pump Element : generates a source or a sink current depending on state of PU or PD signals.

Figure 4.19: Schematic for one Charge Pump element

The CP output current is programmable by enabling or disabling parallel charge pump elements using two control bits, A_1 and A_0 , as shown in Table.4.3. Control over the CP output current allows the designer a way of adjusting the system loop gain.

Control Bits	# of CP element enabled	CP Output Current (μA)	Array Output (μA)
$A_1A_0 = 11$	8	25	200
$A_1A_0 = 10$	7	21.875	175
$A_1A_0 = 01$	6	18.75	150
$A_1A_0 = 00$	5	15.625	125

Table 4.3: CP Output Current vs Control Bits

There are eight such CPs used in this design, forming an array of eight CPs. This array of eight CPs is a part of the truncation error suppression scheme used in the new architecture for the fractional-N divider, as described in Chapter 3.

The maximum output current of the array, which is $200 \mu A$, is the sum of the maximum output of each CP. The behaviour of the array of eight CPs at its maximum current output has been simulated. The result is shown in Fig.4.20.

Figure 4.20: Charge Pump Operation

4.4.1 PFD/CP Noise Performance

PFD and CP noise performance was simulated using the Spectre PSS and Pnoise packages. This simulation was done with an array of eight CPs and their associated PFDs. The eight PFDs are supplied with the same input. The total output current is $200\ \mu\text{A}$. The output-referred noise, in units of $\text{amperes}/\sqrt{\text{Hz}}$, is shown in Fig.4.21.

Figure 4.21: PFD/CP Output-Referred Noise

4.5 Integrator

The integrator is a current to voltage converter which transforms CP array output current to a voltage which can be sampled by the Quantizer. An integrator may be passive or active. From the system analysis point of view, there is no difference between the two, but the choice of one over the other is significant for the circuit design.

Figure 4.22: (a) a Passive Integrator and (b) an Active Integrator

If a passive integrator, as shown in part a of Fig.4.22, were used, the requirement of voltage compliance would make CP design more challenging. That is, a CP feeding a passive integrator must be capable of producing a constant source or sink current over a wide output voltage range. This problem does not occur when an active integrator, as shown in part b of Fig.4.22, is used because the virtual ground at the (+) input holds the (–) input to V_{ref} . Another benefit of using an active integrator is the reduction of kickback noise from the comparators used in the Quantizer [FV04].

The schematic for the active integrator chosen for this design is shown in Fig.4.23.

Figure 4.23: Schematic for a Active Integrator

The OP-AMP uses a differential input stage having an active load followed by a common source stage also driving an active load. It has a small number of transistors, high open loop gain, rail to rail output range and a large input range with only one frequency compensation capacitor being needed [HBL01].

The RC filter in the OP-AMP's input path eliminates the effects of op-amp slew rate limitations which could cause non-linear operation.

The integrator's response to CP output pulses is shown in Fig.4.24.

Figure 4.24: Integrator Transient Response

4.5.1 Noise Performance

The integrator's noise performance was simulated using the Spectre PSS and Pnoise packages. The output-referred noise, in units of $\text{volts}/\sqrt{\text{Hz}}$, is shown in Fig.4.25.

Figure 4.25: Integrator Output Referred Noise for Lock Condition

4.6 3-Bit Quantizer

Quantizers are essentially A/D converters. In this thesis, an array of eight comparators, as shown in Fig.4.26, is used to implement a 3-bit quantizer.

Figure 4.26: An Array of Eight Comparators Used as a 3-bit Quantizer

The quantizer's input resolution, voltage step size ΔV , must be the same as the voltage swing at the integrator's output caused by a $T_{in}/8$ phase error at the input of the CP. In this case, ΔV is given by:

$$\Delta V = \frac{T_{in} I_{pump}}{8 C_{loop}} \quad (4.3)$$

Where $T_{in} = 1 \text{ ns}$, $I_{pump} = 200 \text{ } \mu\text{A}$ and $C_{loop} = 1 \text{ pF}$. (C_{loop} is the capacitor used in the integrator, as shown in Fig.4.23.) Thus:

$$\Delta V = \frac{1 \text{ ns} \cdot 200 \text{ } \mu\text{A}}{8 \cdot 1 \text{ pF}} = 25 \text{ mV} \quad (4.4)$$

The total range of the quantizer is therefore $V_{ref_high} - V_{ref_low} = 8\Delta V = 200 \text{ mV}$.

When the loop is locked, the PFD's DC offset will cause the quantizer's input voltage to first decrease and then to increase by an amount given by:

$$V_{offset} = T_{offset} I_{pump} / C_{loop} = \frac{4 \text{ ns} \times 200 \text{ } \mu\text{A}}{1 \text{ pF}} = 800 \text{ mV} \quad (4.5)$$

As an RC filter is used in the integrator's input path, the voltage decrease/increase is reduced to somewhere near 200 mV , as shown in Fig.4.24.

For testing purposes, external pins are available for adjusting V_{ref_high} and V_{ref_low} .

4.6.1 Comparator Design

The schematic for the comparator is shown in Fig.4.27.

Figure 4.27: Comparator Schematic

The comparator has a differential input stage followed by two regenerative flip-flops and an S-R latch [YES92] [Yuk85].

A cycle of operation of this circuit consists of a settling period followed by a regeneration period:

Settling Period:

This is the period when the clock is low. Switches $M1$ and $M2$ are off, the n-channel flip-flops disconnected from the p-channel flip-flops, and a voltage proportional to the input voltage difference ($V_{in} - V_{ref}$) is established between nodes a and b . This voltage will act as the initial imbalance for the following regeneration period.

Regeneration Period:

When the clock goes high, switches $M1$ and $M2$ are turned on and the n- and p-channel flip-flops regenerate the voltage difference between nodes a and b and also between nodes c and d . This latter voltage difference (between c and d) is soon amplified to a voltage nearly equal to the power supply. The following S-R latch drives the complementary digital output levels at the end of the regeneration period.

4.6.2 Simulation Results

The integrator and quantizer combination was simulated. The simulation results are shown in Fig.4.28. The input current to the integrator simulates a phase error of $T_{in}/8$ by making the width of the sink current pulse $T_{in}/8$ longer than the source pulse. During each f_{ref} cycle, the integrator output voltage is reduced by $\Delta V = 25 \text{ mV}$, which is sampled by the quantizer at the end of the cycle.

Figure 4.28: Quantizer Simulation

4.6.3 Noise Performance

Fig.4.29 shows the results of the quantizer noise simulation. Since the quantizer is a non-linear device, the noise measurement is performed on the differential input stage only.

Figure 4.29: Quantizer Input-Referred Noise

4.7 Digital Feedback Block (DFB)

The main function of the DFB is to process the quantizer output and generate the divisor for the divider in Fig.3.14. The all-digital nature of the DFB means that the design can be implemented using Hardware Description Language (HDL).

The DFB consists of five blocks. The block diagram is shown in Fig.4.30.

Figure 4.30: The Digital Feed Back Block

4.7.1 Encoder

This encodes the quantizer output into a 3-bit binary data.

4.7.2 $2 - Z^{-1}$ block

Here, the operation $2X_n - X_{n-1}$ is performed, where X_n and X_{n-1} are the current and previous Encoder outputs. Since the quantizer's output is in the range from 0 to 7, the range of $2 - Z^{-1}$ is from -7 to 14. To avoid negative numbers, an offset of 8 is added.

4.7.3 Residual Accumulator

Fig.4.31 presents the block diagram for the Residual Accumulator.

Figure 4.31: Residual Accumulator

4.7.4 Data Weighted Averaging Block

The circuit implementation of the DWA function, described in section 3.8 of Chapter 3, is shown in Fig.4.32. It performs the cyclic selection process as described in section 3.8.

Figure 4.32: Block Diagram for DWA implementation

4.7.5 Simulation Result

The RTL simulation result for the DFB is shown in Fig.4.33. Each row of the RTL simulation result corresponds to a node in the block diagram of Fig.4.30.

Figure 4.33: DFB RTL Simulation Result

In this simulation, for example at 600 ns, when the Quantizer output changes from $h'01$ to $h'03$, the output of the Encoder changes from $d'1$ (X_{n-1}) to $d'2$ (X_n) (number of '1's in the Quantizer output). The $2 - Z^{-1}$ block then produces $2X_n - X_{n-1} + d'8 = d'11$. The Accumulator splits $d'11$ into carry over $C = d'1$ and the residual $R = d'3$. C is used to add on the base divisor $int_N = d'99$ to generate the divisor $div_N = d'100$ for the next cycle. R is used to determine the selection of f_{d0} or f_{d1} , as shown in Fig.3.11. In this example, 3 f_{d0} and 5 f_{d1} will be selected as the inputs to the PFD.

4.8 Serial Interface

Some of the circuit blocks have static control signals, as listed in Table.4.4.

Signal Name	Description	Width	Default Value
$int_N < 6 : 0 >$	Base division ratio for the N-divider	7	7b'1100010
$inoise < 2 : 0 >$	Noise control on Charge Pump	3	3b'111
$ipump < 1 : 0 >$	Current control on Charge Pump	2	2b'11
$multi_bit$	Switch between single-bit mode and multi-bit mode	1	1'b1
dwa_enable	Enable or disable DWA capability	1	1'b1

Table 4.4: Static Control Signals

Because there is a limited number of pads, it is impossible to assign a pad for each of the control signals. A Serial Interface (SIF) is used to overcome this problem. A simple and straight-forward method to implement serial-to-parallel conversion is shown in Fig.4.34.

Figure 4.34: Implementation of Serial Interface

A two-stage approach is taken. In stage one, the data is shifted into a register chain at the rising edge of the clock. After fourteen of these clock cycles, the old set of control signals will have been replaced by a new set. In stage two, the output parallel register is triggered and the new set becomes available.

When the *Reset* signal is active, all outputs are reset to their default values. (Default values which are determined by wiring the *Reset* signal to the appropriate *Clear* and *Set* inputs of the register).

Table.4.5 describes each of the block terminals:

Name	Description	I/O
Reset	when high, initializes interface	Input
Clock	common FF clock	Input
Load	strokes shift register contents to output register	Input
DataIn	Serial data input	Input
DataOut	Serial data output (for testing)	Output

Table 4.5: Serial Interface Signals

The number of signal inputs needed for the items of Table.4.4 is four.

The timing diagram for the SIF is shown in Fig.4.35.

Figure 4.35: Serial Interface Timing

An RTL simulation of the SIF was performed, with results shown in Fig.4.36.

Figure 4.36: Serial Interface RTL Simulation

The SIF outputs are set to their initial values when the *Reset* is active, further SIF operation is inhibited until *Reset* is inactive. Data is then shifted in with each rising edge of the clock and after fourteen clock cycles, the data pattern 01010101010101, for example, is present at the shift-register outputs. The *Load* clock can then be used to transfer the data pattern to the output registers.

4.9 Overall Performance

The entire system was simulated using SpectreVerilog with each circuit block modelled with Verilog-A, Verilog, or at the transistor level. The results are summarized in Table.4.6.

Fig#	MMD	PFD	CP	Quantizer	Integrator	DFB
Fig.4.37	Verilog	Verilog	Verilog-A	Verilog-A	Verilog-A	Verilog
Fig.4.38	Verilog	Transistor Level	Verilog-A	Verilog-A	Verilog-A	Verilog
Fig.4.39	Verilog	Verilog	Transistor Level	Verilog-A	Verilog-A	Verilog
Fig.4.40	Verilog	Verilog	Verilog-A	Transistor Level	Verilog-A	Verilog

Table 4.6: System SpectreVerilog Simulations

Figure 4.37: System Simulation with Verilog-A and Verilog

Figure 4.38: System Simulation (PFD Modelled at the Transistor Level)

Figure 4.39: System Simulation (CP Modelled at the Transistor Level)

Figure 4.40: System Simulation (Quantizer Modelled at the Transistor Level)

The noise data collected from transistor level simulations of each of the blocks was applied to the appropriate transfer function as described in Section 3.7. The frequency noise performance is shown in Fig.4.41.

Simulations with the PFD or CP modelled at the transistor level show a significant increase in the noise floor at lower frequencies (Fig.4.38 and Fig.4.39). This is most likely caused by non-linearity in the PFD and CP folding high frequency noise back to lower frequencies [RFDK03]. The input referred frequency noise performance is shown in Fig.4.41. This is obtained by multiplying the output binary data by $\frac{f_{ref}}{8}$.

The in-band (10 kHz to 200 kHz) SNR figure calculated with the addition of the simulated noise is 42.46 dB, down from 46.68 dB when only quantization noise was considered.

The phase noise can be obtained using:

$$S_{\delta\phi}(f) = \frac{1}{f^2} S_{\delta f}(f) \quad (4.6)$$

Figure 4.41: System Frequency Noise Performance

Where $S_{\delta\phi}(f)$ is the spectral density of the phase noise and $S_{\delta f}(f)$ is the spectral density of the frequency noise shown in Fig.4.41.

The phase noise is plotted in Fig.4.42. These results indicate that if the discriminator were used as part of frequency synthesizer with a closed loop bandwidth of 100 kHz, the in band phase noise, due to the discriminator, would be -90 dBc/Hz @ 20 kHz offset for an output frequency of 1 GHz and a reference frequency of 10 MHz. This indicates a BFM [RFDK03] of $-90 \text{ dBc/Hz} - 20\log_{10}(N=100) - 10\log_{10}(F_{\text{ref}}=10 \text{ MHz}) = -200$.

Figure 4.42: System Phase Noises Performance

At low frequencies, the noise from the CP and the PFD is dominant. Improvement of the CP and PFD noise performance is listed as an item for future work.

Chapter 5

Measurements

5.1 Chip Layout and Test Setup

The chip is housed in an 80-pin Ceramic Flat Package (CFP), with the test fixture being provided by the Canadian Microelectronics Company: (<http://www.cmc.ca>).

A plot of the chip layout is shown in Figure. 5.1.

Figure 5.1: Chip Layout

The proposed test setup is shown in Figure 5.2. An RF signal generator is used to provide both the f_{in} input frequency and the 10 MHz reference clock (the latter from the generator's clock reference output). A digital pattern generator provides a serial data stream to the Serial Interface, and the 3-bit output stream is sent to a logic analyzer. An oscilloscope is connected to the output of the Multi-Modulus Divider for debugging purposes.

Figure 5.2: Test Setup

5.2 Fabrication and Fault Analysis

Due to various implementation problems, three designs were fabricated and tested. The details for each fabrication run are given in the following paragraphs.

First fabrication:

A design error was found after the layout was submitted: the CP input polarity was reversed, resulting in positive, rather than negative feedback, in the system loop. This prevented the loop from locking and it was decided to submit a second design for fabrication.

Second fabrication:

For the second submission, transistor level simulations showed correct operation. The measurement results on DC bias levels of the external pins were very close to those obtained from simulations, as shown in Table.5.1.

Signal Name	Description	Simulation Result	Measurement Result
f_{in}	Input Clock	0.78 v	0.75 v
f_{ref}	Reference Clock	0.80 v	0.76 v
$bias_n$	CP NMOS bias	0.45 v	0.43 v
$bias_p$	CP PMOS bias	1.27 v	1.30 v
lf_{ref}	Integrator Ref	0.53 v	0.51 v

Table 5.1: External Pin DC Bias Level Measurement

However, f_{div} , the 10 MHz output signal, from the Multi-Modulus Divider was not detected during testing. The vendor-supplied ‘Standcell’ output drivers were thought to be at fault, but verification of the suspicion was necessary. In particular, it had to be shown that the 10 MHz f_{div} signal is present at the output of the Multi-Modulus Divider.

For monetary reasons, it was decided to forgo a ‘Micro-Surgery’ procedure in favor of

the noninvasive Dynamic Electroluminescence Imaging (DEI) technique [HFSN04]. This method is based upon the fact that passage of current through *any* semiconductor (it doesn't have to be a material expressly designed to emit photons, as in LEDs) is accompanied by the emission of detectable amounts of light. By observing an operating chip with a microscope and a high-gain photo-detector it is possible to display, both spatially and temporally, the current flow at the circuit nodes of interest.

A block diagram for a DEI system is shown in Fig.5.3

Figure 5.3: Block Diagram for a DEI System [HFSN04]

The light collection is performed with a conventional microscope and imaged onto the photo-cathode of a position dissecting photomultiplier tube called a Mepsicron IITM [HFSN04].

The tube is configured for single photon counting so that each detected photon can be processed separately. The Mepsicron provides five output signals, four for a position computer and one to start the Time to Pulse Height Converter (TPHC). The outputs of the Position Computer and the TPHC are captured by a multi-parameter analyzer and stored as a stream of events with X, Y, T signatures.

The test setup using the DEI system is shown in Fig.5.4

Figure 5.4: Test setup with DEI System

The RF signal generator provides the 1 GHz input signal, f_{in} , to the Device Under Test (DUT). The 1 GHz signal is also divided down to 2.5 MHz to give a STOP signal for the TPHC. If the DUT is working properly, four cycles of the waveform for the expected 10 MHz f_{div} output can be captured in the 40 ns long window.

The area of the Multi-Modulus Divider on the die was searched for signs of the 10 MHz f_{div} signal. In that area, the 10 MHz f_{div} signal is mixed with signals of various frequencies

$(f_{in}/3, f_{in}/4, \dots, f_{in}/N)$. The DEI technique has the ability of detecting the 10 MHz f_{div} signal among the others, as will be shown later. The location of the Multi-Modulus Divider is illustrated in Fig.5.5.

Figure 5.5: Locations for DEI Measurements

When *Reset* is inactive, the Multi-Modulus Divider is operating, with divider transistors switching at various fractions of f_{in} Hz, that is, at $f_{in}/3$, $f_{in}/4$, ..., f_{in}/N . The electroluminescence of the transistors will form a 'cloud' in the DEI image as shown at the bottom of the left part of Figure 5.6. On the other hand, when *Reset* is active, the Multi-Modulus Divider only has the f_{in} input present, and a bright spot is shown in the captured image (bottom of the right part of Figure 5.6).

Figure 5.6: DEI Images. Left: RESET is inactive and Right: RESET is active

The above images were processed to produce the time-correlated waveforms, shown in Fig.5.7 and Fig.5.8.

Figure 5.7: Time-Correlated Waveform When RESET is active

Figure 5.8: Time-Correlated Waveform When RESET is inactive

The only visible difference between Fig.5.7 and Fig.5.8 is the amount of the electroluminescence (photo counts). In both cases, only 1 GHz and its harmonics were seen, although the intensity patterns were different. With RESET active, the overall intensity was weaker. Although the difference between when RESET was active and inactive suggested the Multi-Modulus Divider was operating, no 10 MHz signal could be identified from the signals shown in Fig.5.8. (Later with the third fabrication, and extra information obtained from electrical testing, it was determined the reason no 10 MHz was detected is that the wrong trigger frequency was used: The Multi-Modulus Divider was dividing by 101, not 100, which makes $f_{div} = 9.9 \text{ MHz}$, not synchronous with the trigger frequency 2.5 MHz.)

As the 10 MHz f_{div} signal couldn't be identified, the DEI measurement results were not conclusive for the second fabrication.

Third fabrication:

For the third fabrication, the presumably defective ‘Standcell’ output drivers were replaced with custom-designed drivers consisting of cascaded CMOS inverters [WE02]. The 10 MHz f_{div} output signal from the Multi-Modulus Divider was detected using an electrical oscilloscope.

Figure 5.9 shows that the duration of the *high* state of the divider output is four f_{in} cycles as expected.

Figure 5.9: Divider Waveform

Unfortunately, two bonding wires were mistakenly interchanged by the bonding facility and full testing will be impossible until this defect is repaired.

DEI measurements were performed again on the third fabrication. With the extra information obtained from the electrical testing, the right trigger frequency was used. The waveform from the Multi-Modulus Divider area when RESET is inactive is shown in Fig.5.10.

Figure 5.10: Time-Correlated Waveform When RESET=OFF

It is shown that the 10 MHz output signal exists among the other signals. Had the correct division ratio been used in earlier testing, the same waveform would have been measured for the second fabrication.

More DEI measurements are planned for the second and the third fabrication. Signals will be traced along different paths using the DEI technique. Those measurements will show the internal circuits are operating without unduly loading the circuits.

Full electrical testing of the system will be done when the bonding wires are repaired. However, such testing is beyond the scope of this thesis. The results from previous measurements and the co-operation test work with the NRC and MuAnalysis Inc. have resulted in a submission to CSTC 2007[HSF⁺07].

Chapter 6

Conclusions and Future Work

6.1 Conclusions

6.1.1 Summary

The motivation for this thesis was to look at a new architecture for a $\Delta\Sigma$ FD that would be suitable for second-generation frequency synthesis applications. Such synthesizers allow the loop filter to be implemented on chip in the digital domain while maintaining low phase noise. Digital implementation allows the loop filter to be programmed on the fly enabling multi-mode wireless.

A brief review of different types of frequency discriminators was presented, and then the thesis focused on the development of a $\Delta\Sigma$ FD. Different existing architectures for $\Delta\Sigma$ FD were examined closely. Performance of each of the $\Delta\Sigma$ FDs was compared. The results were provided as the benchmark for a new design for a $\Delta\Sigma$ FD that is the first known to employ a fractional-N divider.

This new design uses a fractional-N divider in order to reduce quantization noise and

to achieve finer frequency resolution and higher in-band SNR. In a $\Delta\Sigma$ FD that uses an integer-N divider, the quantization step size, Δ , is F_{ref} . By using a 1/8 fractional-N divider, the quantization step is reduced to $F_{ref}/8$. As quantization noise is directly proportional to the quantization step, reducing Δ by eight results in an 18 dB total quantization noise power reduction. In this new design, the fractional-N divider is implemented in a novel way: The multi-modulus divider has two outputs: f_{d_0} and f_{d_1} . f_{d_0} is one input frequency cycle ahead of f_{d_1} . These two signals, along with the PFD and CP array, form a D/A for cancelling out the truncation error remaining in the Accumulator. Other existing architectures for fractional-N dividers incorporate a dedicated high precision D/A at the output of the accumulator in the feedback path and focus on techniques to match the D/A charge transfer with the charge transferred through the PFD and CP (see Fig. 3.10). In this novel architecture, most of the components making up the D/A are in the PFD and CP array so that charge transfer mismatch from these components is eliminated. The mismatches that cannot be eliminated (except through careful layout techniques) result from f_{d_1} not being exactly one cycle delay or from delay mismatches in the different paths. This approach takes advantage of the ability to apply Dynamic Element Matching techniques to the mismatches between the eight parallel paths (each path consists of a Selector element, PFD and CP). The elimination of the precision D/A circuit makes the system more suitable for implementation in a CMOS process. A 3-bit quantizer is used to restore the input range.

Matlab simulations of this new $\Delta\Sigma$ FD were conducted to predict performance and validate the architecture. A linear model of the system was created. The transfer functions from each block in the system to the system output were derived from the linear model. The impact on performance from different choices of system parameters was evaluated both analytically and experimentally (by simulation). Several system level techniques were introduced to mitigate circuit level non-idealities. The analysis and simulations prove the

concept of the new $\Delta\Sigma$ FD works. The results from the system analysis and simulation were captured in a conference paper [FFRC07] that was accepted by ISCAS (International Symposium on Circuits and Systems) 2007.

Circuits for each block in the system were designed in TSMC 0.18 μm CMOS process. The system was simulated using SpectreVerilog with different blocks simulated at the Verilog, Verilog-A or transistor level as appropriate. In each block, transistor level simulations were conducted to verify the functionality of the block and to collect noise data. The noise data was plugged into the transfer functions developed in the linear analysis in order to predict the total noise output of the system. The design was fabricated three times. The first one was not successful due to a design error. The second one was difficult to test due to a non-functional "Standcell" output driver. The third chip is currently under testing. Due to a bonding error at the packaging facility, only a small part of the system has been tested and shown to be working.

DEI analysis techniques were used to do fault analysis on the second fabrication. Microsurgery and micro-probing were considered initially, but the protracted and costly test cycles of those techniques made them less attractive. DEI is a low-cost, noninvasive, non-destructive optical approach and it has bandwidth approaching 100 GHz. Even with the circuits under six-layer metal masks, DEI was able to successfully detect the light emitted by the transistor gates when switching. Light was collected with a conventional microscope and imaged on to the photo-cathode of an imaging photomultiplier tube where each single photon was counted. After time and space correlation, the waveform of the exciting signals can be displayed on a screen similar to a conventional electrical oscilloscope. Collaborative DEI fault analysis was conducted at MuAnalysis Inc. in cooperation with the NRC (National Research Council) and has resulted in one paper submitted to CSTC.

6.1.2 Advantages Over Existing $\Delta\Sigma$ FD Designs

When used alone as a frequency demodulator, the new design has increased sensitivity to small deviation FM signals and superior SNR compared to previous $\Delta\Sigma$ FDs.

When used in a frequency synthesizer as shown in Fig.1.2, the $\Delta\Sigma$ FD enables the loop filter to be implemented digitally and made programmable. This makes the transfer function of the filter well defined and eliminates the need for large passive components.

Phase noise performance indicates a state of the art in-band BFM of -200 @ 20 kHz offset.

6.2 Future Work

Full testing of the third fabrication is currently underway. A custom-made PCB (Printed Circuit Board) will be manufactured to facilitate the testing.

DEI measurements will be continued on the third fabrication. The results from the third fabrication will be compared against those from the second fabrication in order to improve the technique.

The PFD and the CP are the dominant contributors to low frequency noise limiting the achievable SNR. Future work could be done to reduce the noise of these components. Once performance is optimized, the discriminator could be incorporated into a frequency synthesizer.

References

- [Bax94] W. Bax, "A sigma-delta frequency discriminator based synthesizer," Master's thesis, Carleton University, Ottawa ON, Canada, 1994.
- [BC94] R. Beards and M. Copeland, "An oversampling delta-sigma frequency discriminator," *Circuits and Systems -II: Analog and Digital Signal Processing, IEEE Transactions On*, vol. 41, Jan 1994.
- [BF95] R. Baird and T. Fiez, "Linearity enhancement of multi-bit delta-sigma a/d and d/a converters using data weighted averaging," *Circuits and Systems-II: Analog and Digital Signal Processing, IEEE Transactions On*, vol. 42, December 1995.
- [Cra94] J. A. Crawford, *Frequency synthesizer design handbook*. Artech House, INC, 1994.
- [CT92] J. Candy and G. Temes, *Oversampling Delta-Sigma Data Converters*. IEEE Press, 1992.
- [FFRC07] J. Fang, N. Filiol, T. Riley, and M. Copeland, "A delta-sigma frequency discriminator with fractional-n divider and three-bit quantizer," in *Circuit and Sys-*

-
- tems, ISCAS'2007, 2007 IEEE International Symposium On*, vol. TBD, 28-31 May 2007.
- [FV04] P. Figueiredo and J. Vital, "Low kickback noise techniques for cmos latched comparators," *Circuits and Systems, 2004. ISCAS'04 Proceedings of the 2004 International Symposium on*, vol. 1, May 2004.
- [HBL01] M. Hershenson, S. Boyd, and T. Lee, "Optimal design of a cmos op-amp via geometric programming," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 20, Jan 2001.
- [HFSN04] J. Hulse, J. Frank, and M. Simard-Normandin, "Dei as a performance and defect analysis tool," in *Circuit and Systems, NEWCAS 2004. The 2nd Annual IEEE Northeast Workshop on*, vol. 1, 20 June - 23 June 2004.
- [HSF⁺07] J. Hulse, K. Sarault, J. Fang, N. Filiol, and M. Simard-Normandin, "Dynamic electroluminescence imaging (dei) debugging of 0.18 μm circuitry," in *Canadian Semiconductor Technology Conference*, 14 Aug - 17 Aug 2007.
- [IM62] H. Inose and J. Murakami, "A telemereing system by code modulation - delta-sigma modulation," in *Space Electron. Telemetry. IEEE Transaction On*, vol. SET-8, Sep 1962.
- [NH96] O. Nys and R. Henderson, "An analysis of dynamic element matching techniques in sigma-delta modulation," *Circuit and Systems, ISCAS'96 IEEE International Symposium On*, vol. 1, May 1996.
- [NST96] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data Converters: Theory, Design, and Simulation*. Wiley-IEEE Press, Oct 1996.

-
- [RFDK03] T. A. Riley, N. M. Filiol, Q. Du, and J. Kostamovaara, "Techniques for in-band phase noise reduction in delta-sigma synthesizers," *Circuits and Systems -II: Analog and Digital Signal Processing, IEEE Transactions On*, vol. 50, Nov 2003.
- [Rod96] M. S. Roden, *Analog And Digital Communication Systems*. Prentice-Hall, Inc., 1996.
- [Roh83] U. L. Rohde, *Digital PLL Frequency Synthesizers, Theory and Design*. Prentice-Hall, Inc., 1983.
- [WE02] N. H. Weste and K. Eshraghian, *Principles of CMOS VLSI Design*, 2nd ed. Addison-Wesley Publishing Company, 2002.
- [YES92] G. Yin, F. Eynde, and W. Sansen, "A high-speed cmos comparator with 8-b resolution," *Solid-State Circuits, IEEE Journal of*, vol. 27, Feb 1992.
- [Yuk85] A. Yukawa, "A cmos 8-bit high-speed a/d converter ic," *Solid-State Circuits, IEEE Journal of*, vol. sc-20, June 1985.