A 20-GHz Bipolar Varactor-Tuned VCO using Switched Capacitors to Add Tuning Range

by
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A 20-GHz Bipolar Varactor-Tuned VCO using Switched Capacitors to Add Tuning Range

Submitted by Malcolm Stewart, B.Eng. in partial fulfillment of the
requirements for the degree of

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Abstract

The increasing demand for telecommunication bandwidth has driven data rates increasingly higher. To meet the eventual demand for more bandwidth next generation systems are slated to run at 40GB/s. Although, it may be possible to implement 40GB/s data rates in advanced materials such as GaAs or InP eventually the clock and data recovery (CDR) circuits for these systems will have to be designed in a silicon (Si) technology.

In this thesis, the affects of various noise sources on the phase-locked loop (PLL) of a CDR circuit are simulated and discussed. Drawing from the simulation results, suggestions for the selection of CDR PLL loop parameters are given. As well, a dual-rate (10/20GHz) CDR PLL is discussed.

The most difficult block to design in a CDR PLL is the oscillator. If a VCO is used, it must be designed so that it has a large enough tuning range ($\pm 10\%$) to make up for variations in manufacturing. To accomplish this, a 20-GHz voltage-controlled oscillator (VCO) with on-chip inductors is presented. Wide-band tuning is accomplished in this VCO using a combination of switched capacitors and varactor diodes. Design guidelines for the oscillator and guidelines for switched-capacitor circuit design are given.

Finally, the VCO in simulation had a worst case phase noise performance of -73.5dBc/Hz at a 100kHz offset from a 20GHz carrier. Measurement results were not able to corroborate the simulation results. The reasons for the measurement failure is analysed.

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Chapter 1: Introduction

1.1 Motivation

Until the 1990's the forecasts for a telecommunication networks bandwidth capacity was calculated employing concentration ratios derived from classical engineering formulas such as Poisson and Reeling. It was assumed when doing these calculations that a given individual would only use the network for six minutes per hour. This was sufficient for voice only traffic, however, because of the exponential increase in data traffic generated by high-speed internet access, faxes, multiple phone lines, modems, and teleconferencing people today use the network an average of 180 minutes per hour (relative to the standard voice bandwidth) [1]. Assuming that the demand for data bandwidth continues to grow, much more bandwidth will be needed.

Tremendous strides have already been made to increase the bandwidth of the telecommunication networks. In 1997 the most advanced technology could operate at 1.2Gbps over a single fibre; today, companies have demonstrated systems capable of operating up to 1.2Tbps. These 1.2Tbps systems will adequately meet the data demands of the next few years, however, we must design and prepare for the future. As the internet matures a major portion of the data traffic will result from streaming video. Assuming that consumers will

eventually demand high resolution HDTV format video even these 1.2Tbps systems will be inadequate. Today many carriers' fibre optic systems are closing in on one hundred-percent utilization across portions of their networks[2]. When the projected growth of the internet is taken into account it becomes obvious that solutions are required to supply the necessary bandwidth. To increase its bandwidth a carrier currently has three choices: to lay more fibre, to transmit more data in parallel using dense wavelength division multiplexing (DWDM), or to increase the bit rate using time division multiplexing (TDM).

Current leading edge TDM systems operate at the OC-192 (STM-64 outside North America) rate of 10Gbps, and next generation systems will be required to operate at the OC-768 (STM-256) rate of 40Gbps. The first OC-768 systems will be designed using expensive processes based on indium-phosphide, or gallium-arsenide. Eventually companies will attempt to move out of these expensive technologies and into a less expensive silicon process. A great deal of research is currently being done to generate silicon germanium (SiGe) processes capable of running clock and data recovery circuits (CDR) at 40GHz.

1.2 Thesis Goals

One of the most difficult components to design at 40GHz is the voltage controlled oscillator (VCO). A typical "rule of thumb" when choosing a process in which to design a VCO, is that the VCO should oscillate up to approximately 1/3 of the process f_T . At the time of this thesis the best SiGe technology available was NT70 (SiGe2) with a process f_T of about 70GHz. By taking into account this "rule of thumb" an oscillator in NT70 should be able to be designed up to about 23GHz.

Until SiGe matures to a point where it is feasible to design oscillators reliably at 40 GHz, it may be possible to use two 20GHz oscillators mixed together to generate the 40GHz signal. This thesis focuses on the design of a 20-GHz VCO in the NT70 process flow.

In addition to developing oscillators at higher frequency, new methods for increasing the tuning range of these oscillators are required. A wide tuning range is needed to cover fabrication and process variations, as process error can give rise to a 10-20% variation in the oscillation frequency. For this reason, two flavours of VCO are discussed: the first uses a varactor for tuning, and the second uses the combination of a varactor and a switched capacitor for tuning.

Finally it will be shown that using switched tuning techniques, the VCO sensitivity (K_{VCO}) can be set to allow a single PLL to be used for CDR in two different frequency bands with approximately the same PLL characteristics.

1.3 Thesis Outline

Chapter 2 focuses on the circuitry surrounding a typical VCO in a phase-locked loop, or PLL. A general overview of a clock and data recovery (CDR) system is given to give the reader an idea of where the VCO fits into the modern communication network. PLL theory is discussed, followed by an analysis of noise in the PLL.

In Chapter 3, CDR circuits are analysed using Matlab to get an understanding of the effects of phase noise generated outside and inside of the CDR PLL. With the understanding of how noise propagates through the PLL this chapter ends with a discussion of using the same PLL in two different frequency bands.

The performance parameters and the mathematical theory of VCOs is presented in Chapter 4. Next, a discussion of the LC tank circuit is given with an emphasis on methods for varying the capacitance by using varactors and/or accumulation MOS transistors. This chapter also includes a discussion of the Colpitts, Hartley and Negative resistance oscillator architectures and the typical circuit components needed to build them. This chapter

ends with a literature review concerning current methods for building high-frequency and wideband oscillators.

In Chapter 5 the design and implementation of a VCO is described. A more in depth analysis of the negative resistance oscillator structure is given, followed by an explanation of the design choices made to improve performance. Following this a discussion of the LC tank design is given with particular emphasis on the addition of a switched capacitor element to the tank circuit. This chapter concludes with a discussion of the layout and the measurement results.

The last chapter, Chapter 6, summarizes the work of this thesis. Contributions of this thesis are outlined, followed by a discussion of areas that require further research.

Chapter 2: Background

2.1 The Optical Network

Optical networking is the technology of choice in today's networking marketplace. In an optical system, information is beamed point to point in the form of light. Using light as a carrier and an optical fiber as the medium vast distances can be covered with very little latency. This technology allows people to make phone calls from one side of the earth to the other without a significant delay.

Current optical networks use time-division multiplexing (TDM) in conjunction with dense wavelength division multiplexing (DWDM) which can achieve multiples of the TDM frequency. A visual description of this system is given in Figure 2.1.

FIGURE 2.1 A visual description of TDM/DWDM multiplexing.

Further discussions of DWDM, TDM, and SONET are given in the following sections.

2.1.1 DWDM -- Dense Wavelength Division Multiplexing

The main concept of DWDM is the parallel streaming of information on a fibre. Different wavelengths of light are utilized for different channels of data. This system is able to transmit asynchronous transfer mode (ATM), SONET, internet protocol traffic, or any other digital data form over the same optical fibre by assigning the data streams to different wavelengths.

State of the art systems using C-band (1520 to 1565nm), and L-band (1570-1603nm) light frequencies are able to transmit up to 160 different wavelengths at 10Gb/s for a total of 1.6Tb/s on a single fibre. Further exploration of DWDM work is beyond the scope of this thesis, however, additional information and references to literature concerning this topic can be found in [1].

2.1.2 TDM - Time Division Multiplexing

Before DWDM, TDM was the main method for increasing the capacity of a communication network. The idea behind TDM, is that the capacity of the data stream can be increased by using smaller time intervals, allowing more data can be transmitted per second. Through the use of a demultiplexer, Figure 2.2 describes how TDM signals are multiplexed together. In this diagram, an incoming interleaved TDM signal represented by triangles, hexagons, and parallelograms is demultiplexed into 3 separate data streams at $1/3$ of the incoming frequency.

FIGURE 2.2 Visual description of a TDM demultiplexer

There are currently two industry standards that dictate TDM parameters: the Synchronous Optical Network (SONET) standard, and the Synchronous Digital Hierarchy (SDH) network standard. Both SONET and SDH provide standard rates, formats, and optical interfaces for their systems and each outline a migratory path to meet future bandwidth requirements. Because of the similarity of these systems only SONET will be discussed.

2.1.3 SONET - The Synchronous Optical NETwork [2], [3]

The SONET standard describes the current TDM optical network system from the virtual tributary (VT) signal, all the way up to STS-768 (Synchronous transport signal) or OC-768 (optical carrier) level signal. The SONET hierarchy is described by Figure 2.3.

FIGURE 2.3 Depiction of the SONET multiplexing hierarchy.

A synchronous system, means that the average frequency of the clocks in the system are the same. In SONET, every clock in this system can be traced back to a highly stable reference supply. Because STS signal frequency is stable, these signals can be multiplexed together without any bit stuffing. This means that each of the SONET levels is an integer multiple of levels below it. The benefit of using integer multiples, is that even at very high frequencies the lower level data signals can be extracted.

The current frequency limiting component in SONET or SDH systems is the integrated fibre-optic receiver. For this reason, the focus of the remainder of this chapter will be on fibre optic receiver design.

2.2 Non-return to zero (NRZ) data formatting [4], [9]

Data can be transmitted on the SONET system using a any type of data format. Figure 2.4a,b shows two common data formats that may be used: the first is NRZ format and the second is return to zero (RZ) format. In both data formats, successive bits are statistically independent of their neighbouring bits and are measured using the bit rate: $1 / T_b$ (bits/s). Figure 2.4a,b depicts how the bit period is measured for both data formats: in NRZ T_b is equal to the period of the bit, and in RZ T_b is equal to the bit period plus the following zero period. Because RZ data goes to zero in between data bits, half of the information transmitted contains no information and is simply using up bandwidth.

FIGURE 2.4 (a) NRZ data; (b) RZ data; (c) CLK waveform

There are two attributes to NRZ data that make clock recovery difficult. The first is that the data may contain long sequences of 1's and 0's. During the time that the data is inactive, the clock recovery circuit must be able to maintain its oscillation and it must not drift in frequency.

The second attribute that makes clock recovery difficult is that NRZ data does not produce any spectral energy at the data rate. The fastest waveform that is possible using NRZ, shown in Figure 2.4c, is a square wave with a period of $2T_b$ or one-half of the bit rate. Even though there is a chance of spectral component occurring at one-half of the bit rate, because of random phase reversals in the data there will not be a visible spectral component there. The derived power spectral density of NRZ data is given in Equation 2.1 [4],

$$P_x(\omega) = T_b \cdot \left[\frac{\sin(\omega T_b / 2)}{(\omega T_b) / 2} \right]^2, \quad (2.1)$$

and is illustrated in Figure 2.5:

FIGURE 2.5 A Normalized depiction of a NRZ data spectrum (power spectral density)

Because there is no spectral component at the bit rate in the NRZ data, a circuit component that generates a frequency component at $1/T_b$ is required. This can be accomplished by detecting each data transition and generating a corresponding pulse. If this method is

applied to the square wave illustrated in Figure 2.4c a clock signal at the bit rate is generated. Edge detection on random data is illustrated in Figure 2.6

FIGURE 2.6 A depiction of an edge detected output from a NRZ data input

The average power per harmonic of an edge detected signal has been derived previously in [6], Figure 2.7 illustrates the harmonic power for a periodic data signal of length $N=16$. In later sections, a simulation on edge detected data will be performed which agrees with these calculated results. The simulated results will show nulls at even harmonics, and spikes at odd harmonics.

2.2.1 Edge detection circuitry

To generate a clock at the bit rate, the edge detection circuit must create an output at both positive and negative data edges. The simplest way to achieve edge detection is to use an XOR gate having a delayed input as illustrated in Figure 2.8.

FIGURE 2.8 Edge detection using an XOR gate.

In CDR circuits that use a PLL, edge detection is performed as one of the functions of the phase detector block.

2.3 Fibre-optic receivers [6]

A typical fiber-optic SONET receiver architecture is illustrated in Figure 2.9. This receiver is made up of a pin-diode (PD) with transimpedance amplifier (TZ), an automatic gain control circuit (AGC), and a clock and data recovery (CDR) circuit with demultiplexer (Demux).

FIGURE 2.9 10GB/s optical receiver architecture

2.3.1 The photo-detector (PD) and transimpedance amplifier (TGZ) circuitry

The photo-detector, labelled PD in Figure 2.9, absorbs and converts the light pulses into electron hole pairs. These electron-hole pairs get swept across the diodes depletion region and result in a current that is proportional to the light energy hitting the diode. The signal size coming out of the photo-diode is very small and needs to be amplified by a low-noise preamplifier (TZ). The TZ converts the PD current into a voltage for subsequent processing. This is one of the most important stages of the design because the sensitivity of the receiver and the signal-to-noise ratio are determined within this stage. Typically, the TZ is integrated on the same die as the PD in order to shift interconnect problems from the interface between the PD and TZ to the interface between the TZ and the AGC where impedance levels are easier to control.

2.3.2 The automatic gain control (AGC) circuit

The AGC is used to buffer the circuit from process variations and from changes in signal strength. This block must be able to automatically adjust its output to provide the proper signal amplitude, and the appropriate dc levels to the CDR regardless of the output power of the TZ circuit. Also in this block, the signal from the TZ is converted into a differential signal. Differential circuits are employed throughout the remainder of the receiver because of their superior noise rejection properties.

2.3.3 The clock and data recovery (CDR) circuitry

In today's receivers, the CDR circuitry limits the obtainable data rate. This hard to design block has been implemented at data rates up to 10Gb/s. In the future, as better integrated circuit technologies are developed, data rates of 40Gb/s will be obtainable.

Clock and data recovery circuits come in two varieties: open loop filters, and closed loop synchronizers. These two synchronizers are discussed in greater detail in the following sections.

2.3.3.1 .Open loop synchronizers

FIGURE 2.10 Block diagram of an open loop bandpass filter CDR circuit.

The open loop synchronizer, depicted in Figure 2.10, used to be the implementation of choice for high bit-rate receivers. In this architecture, periodic timing information is extracted from NRZ data using a nonlinear edge-enhancement circuit to generate a spectral line at the bit rate. After the edge detect circuit, a narrowband, high-Q, surface-acoustic-wave (SAW) filter centered at the bit-rate was used. SAW filters ring in response to an input pulse. If the input signal is at the proper frequency, acoustic waves are created in the SAW filter that constructively interfere at each edge detected input. This constructive interference gradually builds up into a large enough acoustic wave to be detected by the output transducer. Input signals that are not at the proper frequency will interfere destructively, and no signal at these destructive frequencies will be output. Because of the acoustical properties of the SAW filter, the open loop synchronizer is able to output a clock even during a long string of data without a level change.

Because it does not suffer from instabilities and nonlinear problems, such as frequency acquisition and cycle slipping, the open-loop synchronizer is a very attractive solution. The problem with the open loop synchronizer, however, is that it must be manually adjusted using the delay element to centre the clock-edge in the bit interval and because it is unable to track phase offsets due to temperature, or component aging. Also, the saw filter and delay element are external to the receiver electronics which result in added bulk, and interconnect problems. Finally, a circuit of this architecture is limited in frequency to around 2.5Gb/s because next generation rates of 10Gb/s and higher are not attainable using current SAW filter technology.

2.3.3.2 Closed loop synchronizers

FIGURE 2.11 Block diagram of a closed loop CDR circuit using a PLL

Because SAW filter technology did not progress as fast as integrated circuit technology, at frequencies of 10Gb/s or higher the closed loop synchronizer architecture is necessary. A block diagram of the closed loop synchronizer is given in Figure 2.11. Unlike the open loop synchronizer, this architecture is completely integratable and is able to compensate for changes in the environment and input bit rate. The problem with the closed-loop synchronizer is that it is difficult to design because its frequency acquisition and tracking abilities are nonlinear.

The main component of the closed loop synchronizer is the PLL. Technology limitations on the PLL circuit design is the main reason why closed loop CDR circuits have not been demonstrated at 40GB/s frequencies or higher. The PLL circuit is made up of three parts: the phase detector, the loop filter, and the VCO. The goal of the PLL is to reduce the phase difference between the input signal, and the output of the VCO. To do this, the output of the phase detector drives the VCO in a direction that reduces the phase difference. When the loop has achieved lock, the phase of the VCO and the input reference will have a fixed phase difference. For the rest of this chapter, PLLs are discussed in more detail.

2.4 Phase-locked loops - PLLs [5], [6], [7]

As mentioned previously, the main component in the next generation of CDR circuit will be the PLL. The PLL circuit typically limits the frequency of CDR. In this section the basic operation of the PLL is explained

A PLL is a feedback system used to average out excess phase noise acting on a periodic signal. A depiction of a simplified PLL is shown in Figure 2.12. This first order PLL is made up of a phase detector and a VCO. In this circuit, the phase detector produces an output voltage that is a function of the phase difference between input to the circuit and the output of the VCO. The loop is considered to be in lock when the phase difference, between the input and output signals remains constant with time. Phase lock can only occur when the input and output frequencies are equal. The VCO output frequency is a function of the phase detector output voltage.

FIGURE 2.12 Basic PLL architecture (first order)

The PLL synchronizes the frequency generated by an oscillator with the frequency of a reference signal by minimizing the phase difference. Figure 2.12 can be used to describe the operation of the PLL. The phase detector compares the phase difference between the input reference signal and the oscillator's output signal. The output of the phase detector is a function of the phase difference between the reference and the output signal. The phase detector output is used to drive the VCO output frequency in a direction that reduces the phase difference between the reference signal and the VCO output. When the loop has achieved lock, the phase of the VCO and the input reference will have a fixed phase difference.

The description of the VCO having a fixed phase difference can be accurate in simulation, but not in an actual implementation. A problem every implementation of a VCO encounters is phase noise. Phase noise causes slight deviations from the expected fixed phase difference. Phase noise is the sum of the input signal phase noise, with the phase noise of all of the loop components. The time domain counterpart to phase noise is jitter. Jitter can be described as the phase difference between the waveform and a periodic signal at the same frequency. All PLLs are susceptible to phase noise and jitter because they operate on the phase of signals. Phase noise and indirectly jitter will be revisited in later sections.

The PLL has four basic regions of operation as shown in Figure 2.13. These four regions starting from the outside and moving in are: the hold range, the pull-in range, the pull-out range, and the lock range. The PLL is called dynamic when the output signal is not locked

or synchronized with the reference frequency in frequency and phase. The PLL is called static when the output signal is locked with the reference frequency.

FIGURE 2.13 Regions of PLL operation

The hold range, $\Delta\omega_H$, describes the frequency range in which a PLL can statically maintain phase tracking. If the reference signal is increased above or below the boundaries of this range the PLL will lose lock.

The pull-in range, $\Delta\omega_{PI}$, describes the PLL in a dynamic state or when it is attempting to acquire lock. Inside the pull-in range the PLL will always be able to achieve lock. Outside of the pull-in range the PLL will not be able to lock onto the reference signal. Toward the edges of the pull-in range the PLL may take a long time to acquire lock, whereas, inside a subset of the pull-in range called the lock-in range, $\Delta\omega_L$, the PLL will be able to achieve lock very rapidly. The lock-in range is the normal operating frequency range for the loop. Acquisition inside of the lock-in range is a phase acquisition process, while acquisition outside of this range also requires frequency acquisition.

The pull-out, $\Delta\omega_{PO}$, range describes the size of frequency step that if applied to a locked PLL will cause it to lose lock. If the PLL is initially in a locked state and a frequency is applied that is less than the pull-out range, the PLL will remain in lock; if it is greater than the pull-out range, the PLL will lose lock. If the frequency exceeds the pull-out range and does not quickly return to the lock-in range the PLL will have to reacquire lock.

2.4.1 Second Order PLLs

Unlike the first-order PLL described above, most PLL implementations are made up of three parts: the phase detector, a low-pass filter (LPF), and the VCO. A second-order PLL circuit diagram is shown in Figure 2.14. The addition of the LPF between the output of the phase detector and the VCO helps to reduce the effect of high frequency noise on the control line of the VCO.

FIGURE 2.14 A second-order PLL circuit.

Even though a PLL is a highly non-linear system, when the loop is in lock it can be described using a linear model [7]. A loop is locked when output signal frequency matches that of the input, and the phase detector output has settled to a constant value. A fixed

phase difference between the reference and output signal may exist depending on the type of PLL used.

FIGURE 2.15 2nd order PLL in frequency domain

Figure 2.15 shows the PLL represented in the frequency domain. This loop can be described by the following equation:

$$H(s) = \frac{\Phi_o(s)}{\Phi_i(s)} = \frac{K_{vco}K_{pd}F(s)}{s + K_{vco}K_{pd}F(s)} = \frac{KF(s)}{s + KF(s)}, \text{ where } K = K_{vco}K_{pd} \quad (2.2)$$

Equation 2.2 is the general linearized transfer function of a phase-locked loop [7],[14]. This function is only applicable to the PLL when it is in a locked state.

The dynamics of the PLL are dependant on the type of loop filter used. To illustrate the effect of the loop filter, a low-pass filter (LPF) with phase lead correction will be analysed. A depiction of this type of filter is given in Figure 2.16.

FIGURE 2.16 LPF with Phase lead correction

The transfer function for this filter is:

$$F(j\omega) = \frac{R_2 + 1/jC\omega}{R_1 + R_2 + 1/jC\omega} = \frac{1 + j\omega R_2 C}{1 + j\omega(R_1 + R_2)C} \quad (2.3)$$

Simplifying things:

$$F(j\omega) = \frac{1 + j\omega\tau_2}{1 + j\omega\tau_1} \text{ with } \tau_2 = R_2 C \text{ and } \tau_1 = (R_1 + R_2)C \quad (2.4)$$

Figure 2.17 describes the output characteristics of this LPF filter.

FIGURE 2.17 Output characteristics of filter depicted in Figure 2.16

Substituting Equation 2.4 into Equation 2.2 we get the transfer function for the PLL using a LPF with phase lead correction:

$$H(s) = \frac{K \cdot \frac{1 + s\tau_2}{1 + s\tau_1}}{s + K \cdot \frac{1 + s\tau_2}{1 + s\tau_1}} = \frac{K \cdot \frac{s\tau_2 + 1}{\tau_1}}{s^2 + s \cdot \frac{K\tau_2 + 1}{\tau_1} + \frac{K}{\tau_1}} \quad (2.5)$$

From Equation 2.5 it can be seen that the use of a first order filter in the loop results in a second order PLL loop transfer function. The order of a PLL can be determined by the loop filter order plus one.

This transfer function can be expressed in the standard control theory format as follows:

$$H(s) = \frac{s \left(2\zeta\omega_n - \frac{\omega_n^2}{K} \right) + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (2.6)$$

Where the parameters ζ and ω_n , representing the damping constant and natural frequency of the loop. These can be found using:

$$\omega_n^2 = \frac{K}{\tau_1} \quad (2.7)$$

$$2\zeta\omega_n = \frac{1 + K\tau_2}{\tau_1} \quad (2.8)$$

An s-plane plot, shown in Figure 2.18, can be used to explain the parameters ζ and ω_n ,

FIGURE 2.18 A pair of complex poles on an S-Plane plot

From Figure 2.18 it can be seen that the poles are at a distance ω_n from the origin, at an angle of $\theta = \sin^{-1} \zeta$. The damping factor is used to measure the stability of the system. If the poles of the system lie on the imaginary axis, or $\theta = 0$, then the system will oscillate. As the ζ is increased, and the poles move into the left hand plane of the plot and the system becomes stable. A matlab plot of the second order PLL frequency response, described by Equation 2.6, for various damping factors is given in Figure 2.19

FIGURE 2.19 2nd order PLL frequency response

Figure 2.19 shows that the PLL transfer function describes a low-pass filter with a pass band from zero to ω_n . This plot assumes that the input noise can be treated as the input signal to the PLL, and that the same PLL transfer function described in Equation 2.6 can be used. If the input excess phase varies slowly the output excess phase follows, whereas, if the input excess phase varies quickly it will be filtered out - noise at frequencies above ω_n will be filtered, and whereas noise at frequencies below ω_n will be passed through.

A major problem with circuits having a low damping factor, ζ , is that the phase noise around ω_n gets amplified. This effect can be seen in Figure 2.19 where for signals less

than $\zeta = 1$ the noise gain at ω_n peaks. The problem of phase noise peaking is compounded in PLL circuits that are used in a string of regenerative repeaters because the timing jitter of the clock will be increased exponentially. In practice, CDR circuits will use an overdamped PLL with a damping constant in the range of 4 to 6 to minimize the effect of noise peaking [10], [11].

2.4.1.1 2nd order PLL phase step response

This section describes how the PLL reacts to a shift of phase on the input signal. A depiction of a shift in phase is given in Figure 2.20.

FIGURE 2.20 Phase step depiction.

The phase error of the loop is found from:

$$He(s) = \frac{\Phi_e(s)}{\Phi_i(s)} = 1 - H(s) = \frac{s^2 + \frac{\omega_n^2}{K}s}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (2.9)$$

and the phase step is given by:

$$\Phi_i(s) = \frac{\theta}{s} \quad (2.10)$$

combining the previous two equations yields:

$$\Phi_e(s) = \frac{\theta}{s} \cdot \frac{s^2 + \frac{\omega_n^2}{K}s}{s^2 + 2\xi\omega_n s + \omega_n^2} = \theta \cdot \frac{s + \frac{\omega_n^2}{K}}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (2.11)$$

A depiction of the unit phase step transient response is given in Figure 2.21.

FIGURE 2.21 Transient Phase error of Second-order loop for a phase step of the input signal.(copied from [8])

If a phase step is applied to a PLL oscillating at the natural frequency of the loop, a phase error between the reference and the output will result. A phase step will not cause the PLL to leave the lock range, and the loop dynamics will quickly force the phase error back to zero.

Waveforms corresponding to higher damping factors settle before those corresponding to lower damping factors. A phase step will cause the VCO to speed up (or slow down depending on the size of the phase step) in order to align the reference and output signals.

2.4.1.2 2nd order PLL frequency step response

This section describes how the PLL reacts to a frequency step on the reference signal. A depiction of a frequency step is given in Figure 2.22.

FIGURE 2.22 Depiction of a frequency step

A frequency step can be modelled using:

$$\Phi_i(s) = \frac{\Delta\omega}{s^2} \quad (2.12)$$

Which combined with Equation 2.9 yields:

$$\Phi_e(s) = \Delta\omega \cdot \frac{s + \frac{\omega_n^2}{K}}{s(s^2 + 2\xi\omega_n s + \omega_n^2)} \quad (2.13)$$

A depiction of the PLLs response to a step in frequency is given in Figure 2.23:

FIGURE 2.23 2nd order PLL frequency step response. (copied from [8])

From the transient response of the phase error it can be seen that the phase error is initially zero because the loop is locked at the VCO centre frequency. As the input reference frequency experiences a frequency step a phase error develops. This phase error decreases as the new frequency is acquired, and the phase of the PLL is aligned. Once again, waveforms corresponding to higher damping constants settle the faster.

Unlike after a phase step, the resultant phase offset between the reference and output signal does not settle to zero. The phase error eventually dies down to the following value:

$$\phi_e(t \rightarrow \infty) = \frac{\Delta\omega}{K} \quad (2.14)$$

The static phase error is necessary for the loop to remain in lock. This offset value is used by the loop to tell the VCO how far from the centre frequency the reference signal can be found. PLLs with higher loop gains will result in lower static phase errors.

The static phase difference at frequency offsets presents a problem in loops that have a low overall loop gain such as CDR circuits. In CDR circuits that are part of a series of data

repeaters this offset jitter can accumulate to significant levels. CDR circuits operate at very high frequencies which mean they cannot take advantage of active filters which could otherwise be used to increase the loop gain. Another problem with a static phase offset in these circuits is that it has been found to increase jitter at the output signal and to cause the data stream to be sampled at a sub-optimum point [12].

2.4.2 2nd order PLL using a charge pump

The charge pump (CP) PLL is a digital PLL that uses a charge pump attached to the output of the phase/frequency detector as shown in Figure 2.24. The CP PLL is popular for integrated circuit applications because of its ease of implementation, because of the fact that it allows the PLL to have a PULL-IN range that is only limited by the VCOs tuning range [12], and because it does not require a static phase error offset between the reference and the output to operate.

FIGURE 2.24 A charge pump PLL

In the PLL shown in Figure 2.24, the phase detector generates an UP or DOWN signal by comparing the reference signal with the feedback signal. The UP and DOWN signal tells the VCO to either speed up or slow down. A depiction of the phase detector output is given in Figure 2.25. As shown in Figure 2.25a, if the reference signal arrives before the feedback signal then the phase detector generates an UP pulse to increase the VCOs fre-

quency. Secondly if the reference signal arrives after the feedback signal, as shown in Figure 2.25b, then a down pulse is generated to slow the VCO.

FIGURE 2.25 Example of a UP/DOWN phase detector output

Using Figure 2.25a and Figure 2.26 as a reference, when the loop feedback lags the reference signal the UP signal turns on causing an injection of charge I_p into the lowpass filter. I_p flows until the loop feedback goes high and the UP signal is deasserted. The additional charge stored on C can be quantified by:

$$\Delta V_{ctrl} = \frac{I_p \Delta t}{C}, \text{ where } \Delta t \text{ is the time that UP is on} \quad (2.15)$$

The additional charge injected into the LPF increases the filter's output voltage and speeds up the VCO. The increased VCO frequency causes the feedback to become more in phase with the reference signal. When the feedback and the reference signals become locked in

frequency and phase, the control signals should not turn on any more and the control voltage should remain constant.

FIGURE 2.26 Charge pump and low pass filter

It should be noted, that the charge pump in Figure 2.26 requires that the resistor R_2 be present in the circuit. Without this resistor the PLL will have two poles on the imaginary axis and a damping factor of zero. What this means is that this system would have a phase oscillation at the natural frequency of the system. By inserting the resistor into the circuit this phase oscillation will not occur because the resistor causes a zero to be added to the system and the poles to be placed in the left plane.

The CP PLL has the same transfer function, and response to a phase step as a second-order PLL that uses a loop filter. Where the CP PLL differs from the second-order PLL with only a LPF is that when it is in lock the static phase error will be theoretically zero. In the case of the charge pump PLL the voltage offset that is supplied to the VCO in order to tune the PLL is decoupled from the phase detector. What is meant by this is that when the loop is in lock the phase detector does not need to output a signal in order to maintain the voltage offset.

The switching interaction between the phase detector and the charge pump make the charge pump PLL a discrete time system, however, as long as the loop bandwidth is much less than the input reference frequency and there are only small phase variations a linear analysis can be used. Linear analysis can be applied to CDR PLLs because they are typically designed with a narrow loop bandwidth in order to minimize the noise introduced by external sources.

2.4.2.1 Dynamic Phase Error

Dynamic phase error is the sum of the input noise referred to the output and the VCO noise referred to the output. Any noise generated inside of the loop that is outside of the loop bandwidth cannot be reduced by negative feedback action. All of the loop components contribute in some manner to the noise of the system. The following equation describes the phase jitter at the output of the PLL:

$$\Phi_o(s) = \Phi_{ov}(s) + \Phi_{oi}(s) \quad (2.16)$$

This equation represents the sum of the input spectral density referred to the output, plus the spectral density due to the VCO [5]. The reason for including only the VCO spectral density into this equation is because in monolithic implementations the VCO is the most significant contributor of the loop components to the phase noise [9].

2.5 PLL Circuit Component Descriptions

The following sections focus on specific circuit blocks that could be used in a CDR PLL. For more information concerning these blocks, or for examples of other circuits that could be used see: [12], [13], [14].

2.5.1 The Phase Detector

An UP/DOWN PD shown in Figure 2.27. This PD can be used to control a charge-pump circuit (Section 2.5.2) using its UP and DOWN pulses to activate the charge pump switches.

FIGURE 2.27 UP/DOWN PD

The rising edge of the REF signal causes UP to be asserted, UP gets cleared when FB goes high. Likewise, a rising edge on the FB input causes DOWN to go high, DOWN is cleared when REF subsequently goes high. The operation of this PD is depicted in Figure 2.28.

FIGURE 2.28 UP/DOWN PD outputs

The UP/DOWN PD circuit takes the average difference between the UP and DOWN outputs, which behave as shown in Figure 2.29. This circuit's input range is 4π radians, and it has a gain constant described by:

$$K_D = \frac{V_{DD}}{2\pi} \quad (2.17)$$

In order to maximize the range of this PD the equilibrium point is set to 0 degrees.

FIGURE 2.29 UP/DOWN PD characteristics

For the sequential PD the following equation describes the phase error:

$$t_p = \left| \frac{\theta_e}{\omega_{REF}} \right| \quad (2.18)$$

where t_p is the duration of the UP or DOWN pulse, θ_e , is the phase error between the REF and FB signals, and ω_{REF} is the frequency of the REF signal.

2.5.2 The Charge Pump (CP)

As mentioned previously, CPs [12] are commonly used in the place of an active filter in a PLL. Filter characteristics can be achieved by applying the charge pump output to a RC network as depicted in Figure 2.30. The CP controls the magnitude of charge stored in the loop filter thus converting the PD output to a control voltage that is usable by the VCO. A main advantage of the CP is that it can be implemented with only a few transistors, saving the area, complexity, and power compared to an active filter.

FIGURE 2.30 Charge-pump loop filter

A CP requires the PD to control one or more of the current sources while the RC network provides the necessary transfer function characteristics. The depicted CP, Figure 2.30, acts as a 3-pole switch having states UP, DOWN, and OFF. When the loop feedback (FB) leads the loop input, the VCO has to slow down so the charge pump is switched into the DOWN position to remove charge from the capacitor, see Figure 2.28b. When the PLL is locked the switch is in the OFF position and the VCO frequency stays the same. This charge pump is designed to work with a sequential phase detector as shown in Figure 2.27.

From Figure 2.28a, when the loop feedback lags the reference, at each leading edge of the reference UP turns on causing an injection of charge I_p into the LP filter. I_p flows until the loop feedback goes high. The additional charge stored on C can be quantified by:

$$\Delta V_{ctrl} = \frac{I_p \Delta t}{C}, \text{ where } \Delta t \text{ is the time that UP is on} \quad (2.19)$$

The additional charge increases the loop filter's output voltage and speeds up the VCO. The increased VCO frequency causes the feedback to become more in phase with the reference signal. When the feedback and the reference signals become locked in phase and frequency, the control signals will not turn on any more and the control voltage should remain constant.

In an actual design it is possible for both PD outputs, UP and DOWN, to go high for a few gate delays when the input waveforms are aligned. The time of a few gate delays is very short (in ns) and this would have very little effect on the dc output of the loop filter. For

such a case, the CP depicted in Figure 2.31 has an additional capacitor, C_2 , which would largely eliminate the effect of this glitch.

FIGURE 2.31 Charge-pump loop filter with extra pole

The reason that an extra pole is added to the CP circuit using C_2 , is to eliminate the voltage glitch that occurs because of the loop stabilizing zero, resistor R , every time a switch is turned on. C_2 is also useful in circuits where the input comes from a multiplier type PD, because C_2 will remove the higher frequency mixing components. If C_2 is chosen sufficiently smaller than C , loop dynamics will not be effected other than a slight decrease in the loop damping. When the loop is designed, the damping factor is usually chosen slightly higher to compensate for C_2 .

Finally, differential charge-pump circuits will have better noise immunity, and improved matching compared to most other circuit choices [12].

2.5.3 The VCO

This section gives a brief overview of a few VCO parameters [15]. VCO architecture and design is covered in greater detail in Chapter 3.

If the PLL system is given no input signal, the output of the phase detector will be the same as the input from the VCO. This signal will be filtered out by the LPF so the DC amplifier will have nothing to amplify. This means that the signal applied to the VCO will be zero volts. At zero volts, the VCO will operate at the free running frequency, f_{nom} . An ideal VCO can be described by the following equation:

$$\omega_t = \omega_{nom} + K_{vco} V_c \quad (2.20)$$

The VCO generates a periodic waveform that is a linear function of the control voltage V_c . For a sinusoidal waveform the output of the VCO is:

$$v_o(t) = B \cos(\omega_{nom}t + \phi_o(t)) \quad (2.21)$$

where phase error, $\phi_o(t)$, is described by:

$$K_{vco} \int v_c dt = \phi_o(t) \quad (2.22)$$

This equation shows that phase at the output of the VCO is adjusted by changing the frequency of the VCO in a way that reduces the phase error. It also shows that the output phase is dependant on the history of v_c , not just the current value.

Finally, the input/output transfer function for the VCO is:

$$\frac{\Phi_o(s)}{v_c(s)} = \frac{K_{vco}}{s} \quad (2.23)$$

In monolithic implementations the VCO is the most significant contributor of the loop components to the phase noise.

2.6 Summary

This chapter gave a brief overview of the modern optical network to help give a better perspective of how this circuit fits into the telecommunication network. Optical transceiver circuitry was briefly discussed, followed by a quick overview of PLL circuit theory. A discussion of phase error in the PLL was given with an emphasis on the phase error in a second-order loop. Finally, the chapter concluded with a brief overview of typical PLL components to give the reader an idea of how the VCO would interface to the rest of the PLL.

In the next chapter, a CDR system is modelled in Matlab. Building on this foundation an explanation of VCO band switching is given, and how it affects the CDR PLL output.

Chapter 3: CDR Simulation

This chapter makes use of the theory described in Chapter 2 to take a closer look at CDR PLL. The simulations described in this chapter were performed in Matlab.

3.1 NRZ Data

As described previously, NRZ data has a null point at the transmitted data frequency. To illustrate this fact the FFT of a NRZ data stream was taken in matlab for 20000 bits of random data (oversampled by 10). The plot of this FFT is given in Figure 3.1. It is clear from this plot that there is no frequency component at the data rate, and there is no other outstanding frequency component. The reason for this is that the adjacent data transitions are equally likely to be negative as positive at any time. This random phase reversal would prevent the accumulation of a steady-state resonance if the signal were applied to band-pass filter [6].

FIGURE 3.1 FFT of a Random NRZ data stream, normalized to the data frequency.

When performing an FFT the number of data points determine the frequency step size, Equation 3.1, and the oversample rate determines the overall bandwidth of the FFT, Equation 3.2.

$$f_s = 2 \times \text{data frequency} \times \text{oversample rate} \quad (3.1)$$

$$f_{\text{nyquist}} = \text{data frequency} \times \text{oversample rate} \quad (3.2)$$

$$f_{\text{step}} = \frac{\text{data frequency}}{\text{N number of points} \times \text{oversample rate}} \quad (3.3)$$

The total number of points is an exact power of 2 so that a Fast-Fourier Transform, FFT, can be used rather than a Discrete Fourier Transform. It was also found through simulation that simulations progress much faster if you generate an array before you fill it. If the array isn't generated before the simulations (eg. the Edge-detected array) are done, it was found that for very long data streams the majority of the simulation time was spent just building

the array. A similar plot as that performed for Figure 3.1 is given in Figure 3.2 showing a much higher resolution using these principles.

FIGURE 3.2 2^{22} point simulation using 2X oversampling on NRZ data. Normalized to the data frequency.

As mentioned above the NRZ data does not have a discernable frequency component. One might expect to find a frequency component at 1/2 the frequency rate, however, because of the data's random phase fluctuations, illustrated in Figure 3.3, this frequency component is not distinguishable.

FIGURE 3.3 Depiction of Random Phase Reversal in NRZ data

Figure 3.4 illustrates the effect of creating a positive pulse at every bit transition. Now, every bit transition is in phase with a resonant signal at the bit rate. Using Edge detected data one would expect to find a strong frequency component at the bit rate.

FIGURE 3.4 Depiction of Edge Triggered Data

A simulation of edge-triggered data was performed using the same 20000 points of NRZ data as were used in the generation of Figure 3.1. The results of this simulation can be seen in Figure 3.5. From this diagram the strong frequency component at the bit rate is clearly evident, as are the null points at the even harmonics. The harmonics in this figure agree with the expected harmonics described by NRZ theory in Figure 2.7.

FIGURE 3.5 Simulated harmonics of a normalized edge detected NRZ data signal

Figure 3.6 shows a NRZ edge detected data stream. Noise is scaled by the bin width ($20 \cdot 10^9 / 2^{21}$) but the tone is not. Note that this is comparable to adjusting the resolution bandwidth on a spectrum analyser from 9.537kHz to 1Hz resulting in a reduction of noise of 39.79dB. The reason that the tone is not scaled with the noise is because an infinitesimally narrow tone is not affected by the resolution bandwidth.

FIGURE 3.6 2^{23} point simulation using 2X oversampling on NRZ edge detected data, normalized to the data frequency.

Having generated a frequency component at the bit rate, it can be recovered using the methods discussed in Chapter 2.

3.2 PLL Output Phase Noise

In this chapter we will only analyse two sources of noise at the output of the PLL: the input phase noise, and the VCO phase noise. The reason that the other sources of noise in the PLL are ignored, is because the VCO noise source dominates over all of the other internal noise sources [9]. Using this assumption, and because the noise components are

from independent sources, the spectral density at the output of the PLL can be summarized as:

$$\Phi_o(f) = \Phi_{ov}(f) + \Phi_{oi}(f) \quad (3.4)$$

Where the vco's contribution at the PLL output can be calculated by,

$$\Phi_{ov}(f) = \Phi_v(f) \cdot |H_n(j2\pi f)|^2 \quad (3.5)$$

and the input noise referred to the output can be calculated by:

$$\Phi_{oi}(f) = \Phi_i(f) \cdot |H(j2\pi f)|^2 \quad (3.6)$$

In the following sections we will use these equations as the basis for the analysis.

3.3 VCO Noise at the Output of the PLL

The analysis described in this section pertains to Equation 3.5. The phase noise at a certain offset from the carrier is described by Leeson's equation given in Equation 3.7. A more thorough analysis of Leeson's equation is given in Chapter 4.

$$\Phi_v(f) = \left(\frac{A\omega_0}{2Q\Delta\omega} \right)^2 \cdot \frac{FkT}{2P_s} \quad (3.7)$$

The transfer function for the output phase noise due to VCO noise and $\frac{\theta_o}{\theta_n}$ can be derived

from control theory using Figure 3.7:

FIGURE 3.7 Transfer Function from θ_{vco} to θ_o

Therefore, the output phase noise due to VCO noise is:

$$\frac{\theta_o}{\theta_n} = \frac{1}{1 + G(s)}, \quad (3.8)$$

which is the PLL error transfer function (Chapter 2), described by:

$$H_n(s) = \frac{\theta_o}{\theta_n} = \frac{s^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (3.9)$$

Using this equation we get:

$$|H_n(j2\pi f)|^2 = \frac{(2\pi f)^4}{(2\pi f)^4 + 2 \cdot (2\xi\omega_n)^2 (2\pi f)^2 + \omega_n^2 (2\pi f)^2 + \omega_n^4} \quad (3.10)$$

Figure 3.8 shows the results of this theory with $\omega_n = 2\pi \cdot 100k$, and $\zeta = 5$. The results show very low noise results for the bandwidth chosen. Further discussion on PLL parame-

ter selection will be done later. The VCO phase noise used in this simulation were scaled to match the simulation results given in Chapter 5.

FIGURE 3.8 Simulation of the output phase noise of a PLL due to the VCO using ω_n of 100kHz

3.4 Input Noise at the Output of the PLL

The PLL in some ways can be seen as an adaptable Band-Pass Filter (BPF), where the centre frequency is automatically tuned to the bit rate. For instance, the phase-detector in the frequency domain can be likened to a mixer that mixes the edge detected signal down to the baseband.

The PLL tracks the phase of the edge-detected signal and mixes the signal energy from the clock frequency down to dc where it can be suppressed by the loop filter. When the loop is in lock, the clock signal of the VCO will be in quadrature with the clock component of the input edge detected signal and the resulting dc component will be zero. The resulting phase error signal is subsequently sent through a LPF filter and then used to adjust the fre-

quency of the oscillator. This baseband tuning signal frequency modulates the VCO, thus shifting the filtered noise spectrum up to the clock frequency.

In this section we will be looking at the PLL as a Low Pass Filter (LPF). Unlike the VCO noise analysis there is no equation that describes the input noise to the PLL of edge-detected NRZ data; therefore, the numerical results of Section 3.1 will be used.

The transfer function for the PLL is:

$$H(j2\pi f) = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (3.11)$$

The magnitude squared of this equation is:

$$|H(j2\pi f)|^2 = \frac{(2\xi\omega_n)^2 (2\pi f)^2 + \omega_n^4}{(2\pi f)^4 + 2 \cdot (2\xi\omega_n)^2 (2\pi f)^2 + \omega_n^2 (2\pi f)^2 + \omega_n^4} \quad (3.12)$$

which is plotted in Figure 3.9:

FIGURE 3.9 PLL Transfer function for a PLL using a w_n of 100kHz

As can be seen in Figure 3.9, even though the PLL has been designed to have a ω_n of 100kHz, the bandwidth appears to be closer to 1MHz than 100kHz. The reason for this is that a large damping constant was chosen to minimize jitter peaking. Figure 2.19 in Chapter 2, illustrated the effect of the damping constant on the effective loop bandwidth.

Figure 3.10 shows the filtered result at the output of the VCO in the loop. After filtering the noise is now filtered relative to the reference tone. The data in this plot was generated using 2^{22} data points, with 2X oversampling for a total 2^{23} data points.

FIGURE 3.10 Simulation of the output phase noise of a PLL due to an edge detected input signal using a 100kHz ω_n . (normalized to the data frequency)

A plot zoomed into to show noise close into the clock signal is shown in Figure 3.11. As can be seen from this plot the phase noise close to the carrier is approximately -70dB. At frequencies greater than 1MHz offset the phase noise drops off at approximately -20db/

decade. It is obvious, from this plot that the PLL designer should make the loop bandwidth as small as possible to minimize the transfer of phase-noise to the PLL output.

The FFT was performed using an input having $\pm 1V$. A more realistic input level would have been $\pm 200mV$, or about the same as the VCO output power level. Because Figure 3.11 shows the output power relative to carrier no scaling is required, and we can directly compare these values to the phase noise of the VCO. A dashed line is drawn on Figure 3.11 to represent the output phase noise curve. From 10^4 to 10^6 the line is drawn near the top of the data points shown because Figure 3.6 clearly shows the phase noise around the carrier at around $-71dBc/Hz$.

FIGURE 3.11 Phase noise offset from the carrier. The dashed line is an approximation of the phase noise curve.

The above phase-noise simulations for the VCO and input data stream are summarized in Figure 3.12. This figure shows that for a 1MHz bandwidth the phase-noise at the output of

the PLL is mainly due to random modulations in the data, and additive noise. This being the case, the bandwidth of the noise-suppression filter is the most critical parameter in determining the phase-noise of the recovered clock. For PLLs having a large loop bandwidth it may be possible to use a ring oscillator.

Figure 3.12 shows that for a larger loop bandwidth the input noise will easily dominate. However, Figure 3.13 shows that if the loop bandwidth is narrowed to 100kHz the VCO becomes a significant contributor to the total noise of the system. For a narrow enough bandwidth, the VCO will dominate the output phase noise. It is obvious that there will be a point somewhere around 100kHz at which the noise performance of the loop will be optimized.

FIGURE 3.12 Calculated output PLL phase noise for a 1MHz PLL bandwidth

FIGURE 3.13 Calculated output PLL phase noise for a 100kHz PLL bandwidth

One must also take into account other parameters of the PLL such as acquisition speed. For example, if the loop bandwidth is made too small then the acquisition speed of the PLL may not be high enough for the application. There are many solutions, some are discussed in [9], that attempt to solve these problems. For example, one might use two loop bandwidth settings: a wide bandwidth for fast acquisition and a narrow bandwidth for its noise rejection properties. In the following chapters methods of selecting and adjusting K_{VCO} of the oscillator will be discussed for just such applications.

3.5 Dual Band Tuning

This section assumes that the PLL used is capable of operating in one of two frequency bands: for example, performing clock and data recovery at 10GHz or at 20GHz. To

accomplish this task the PLL can switch between a 20GHz and a 10GHz VCO. A description of this VCO is give in Figure 3.14:

FIGURE 3.14 Transfer function from $\theta_i(s)$ to $\theta_o(s)$

The reason that the 20GHz VCO in Figure 3.14 has a K_{VCO} (measured in Hz/V) that is twice that of 10GHz VCO, is because we are assuming that the two VCOs require a tuning range of about 10% of their frequency.

The problem with having a different K_{VCO} at the higher frequency is that the loop gain will be twice as large and more noise will be passed through near the clock frequency. To remove this problem a method is required to decrease the effective K_{VCO} of the 20GHz VCO without decreasing its tuning range. This can be achieved by using an oscillator with two bands of operation each with a 2GHz range. A switch can be used to jump between adjacent frequency bands, for example, from the 18-20GHz band to the 20-22GHz

Figure 3.15 illustrates the difference between using a regular VCO (dotted line) at the 20GHz frequency and the switch tuned VCO (solid lines) at 20GHz. The 10GHz VCO fre-

quency range is also shown to illustrate that it will have the same K_{VCO} value as the switch-tuned oscillator at 20GHz.

FIGURE 3.15 Comparison between a switched tuned VCO and a regular VCO at 20GHz

The design and discussion of oscillators with switched tuning will be given in later chapters.

3.6 Summary

In this chapter the contribution of input and VCO noise to the output of the CDR PLL output was explored. The relationship between the PLL bandwidth and each of these noise sources was found and discussed.

Methods for tuning the PLL are discussed, followed by the description of a dual-band tuning architecture that makes use of a switched-tuned oscillator circuit to control the gain of the high-frequency VCO.

The focus of the following chapters will be on the design of the VCO. Methods for switched tuning inside an oscillator will be discussed along with other methods for wide-band tuning.

Chapter 4: VCO Design Principles

As mentioned at the end of Chapter 3, this chapter focuses on voltage-controlled oscillator (VCO) design. This chapter starts with a discussion of the various performance parameters that a VCO must meet. Following this, a discussion of the various components that make up a VCO is given. Thirdly, VCO architectures will also be discussed. Finally, current high-speed and wideband oscillator designs will be reviewed.

4.1 VCO Performance Parameters

VCOs are typically designed as part of a system, such as a PLL. The output and input requirements of this system are known and the different elements of the system, including the VCO are budgeted to meet this requirement. This section will discuss the various specifications that a VCO is typically designed for.

The *centre frequency* is the value in the middle of the VCOs tuning range. The range of the VCO is determined by the application that the VCO is designed for. Typically the larger the tuning range the noisier the VCO. Careful trade-offs must be made when deciding how much tuning range is really necessary.

Closely related to the centre frequency is the VCOs **tuning range**. The tuning range is determined by taking the frequency range required by the application, and by adding in some margin to account for process and temperature variations.

Tuning linearity describes the non-linear tuning characteristics of the VCO. Because the VCO gain, K_{VCO} , is not linear across the tuning range some areas in the tuning range will exhibit higher sensitivity to voltage variations than others. It is important to try and minimize the variation of K_{VCO} because non-linearity can degrade the settling behaviour of the PLL.

The **output amplitude** of the VCO must be traded off with power dissipation, supply voltage, and tuning range. A large output amplitude will make the waveform less sensitive to noise, however, a VCO with a large output amplitude may have a large amplitude variation across the tuning range which is undesirable.

Just like any other circuit the VCO must be constrained in terms of **Power dissipation**. The optimum power dissipation for a VCO is determined by application the VCO is intended for. If the optimum power dissipation is not achievable then the designer must trade-off speed, and noise sensitivity to lower the power numbers for the VCO.

The **output signal purity** of a VCO refers to the allowable phase noise or jitter at the VCOs output.

Finally, the oscillator's **supply and common mode noise rejection** requirements must be met. Oscillators are very sensitive to noise, in a poorly designed oscillator both supply and common mode noise will be coupled through to the VCOs output as phase noise. Typically, oscillators are designed in a fashion that minimizes the amount of noise that can be coupled to its output: for example, making the VCO differential.

4.2 The Tank Circuit[14]

The LC tank oscillates using the properties of the inductor and capacitor. Consider a circuit that consists of a perfect inductor in series with a perfect capacitor. When the capacitor is fully charged, the total energy of the system is stored in the electric field of the capacitor, there is no current flow through the inductor and hence no charge stored by it. As the capacitor discharges and current begins to flow, the energy that was stored in the capacitor's electric field is transferred into the magnetic field of the inductor. When the capacitor is fully discharged and the current is at its maximum value, all of the energy is stored by the inductor. In an ideal situation the energy will continue to transfer between the inductor and the capacitor indefinitely. The rate at which energy is transferred back and forth between the capacitor and the inductor is called the frequency of operation.

An LC tank circuit is typically used to determine the oscillation frequency of an LC VCO. An ideal LC tank circuit is depicted in Figure 4.1, and its transfer function is given by Equation 4.1. At high frequencies the capacitor, C , acts like a short, and at low frequencies the inductor, L , acts like a short. Maximum gain occurs at the frequency of minimum admittance, or maximum impedance.

FIGURE 4.1 LC tank circuit

$$\frac{V_{out}}{I_{in}} = \frac{1}{sC + \frac{1}{sL}} = \frac{1}{C} \cdot \left(\frac{1}{s^2 + \frac{1}{LC}} \right) \quad (4.1)$$

The frequency at which the inductive and capacitive admittance cancel is known as the resonant frequency and is given by:

$$\left(\omega_0 C - \frac{1}{\omega_0 L} \right) = 0 \quad (4.2)$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (4.3)$$

If perfect components were used, in a simulation the above circuit will oscillate forever. In reality, resistive losses will exist in the tank circuit that will cause the oscillations to reduce in amplitude, or to be damped. These resistive losses come from many different places in the circuit. To simplify the calculations an equivalent parallel resistance can be used to represent them as shown in Figure 4.2.

FIGURE 4.2 RLC Tank Circuit

The transfer function for the circuit in Figure 4.2 is:

$$\frac{V_{out}}{I_{in}} = \frac{1}{sC + \frac{1}{R} + \frac{1}{sL}} = \frac{1}{C} \cdot \left(\frac{1}{s^2 + \frac{s}{RC} + \frac{1}{LC}} \right) \quad (4.4)$$

which means the resonant frequency is now given by:

$$\omega_0 = \sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}} \quad (4.5)$$

Typically $R \gg \sqrt{\frac{L}{4C}}$ which means that Equation 4.5 can be approximated by Equation 4.3.

4.2.1 Quality Factor, Q

An important descriptive factor of a RLC tank circuit is its Q, or quality factor. Tank Q is a measure of the rate of energy loss. The fundamental description of Q is:

$$Q = \omega \frac{\text{energy stored}}{\text{average power dissipated}} \quad (4.6)$$

Q is a dimensionless quantity, and is as the above equation states proportional to the ratio of energy stored to the energy lost per unit time.

To derive the energy stored in the RLC tank we must note that the peak energy stored in the capacitor or the inductor is equal to total energy stored in the tank. If at resonance the peak capacitor voltage is $(I_{pk}R)$ then the total energy stored is:

$$E = \frac{1}{2}C(I_{pk}R)^2 \quad (4.7)$$

At resonance the RLC tank circuit acts like a simple resistance. Therefore, the average power dissipated in this resistance can be given by:

$$P_{avg} = \frac{1}{2}I_{pk}^2R \quad (4.8)$$

And so, the Q of the network can be derived using Equation 4.6 as:

$$Q = \omega_0 \frac{E}{P_{avg}} = \frac{1}{\sqrt{LC}} \frac{\frac{1}{2} C (I_{pk} R)^2}{\frac{1}{2} I_{pk}^2 R} = \frac{R}{\sqrt{L/C}} \quad (4.9)$$

from which we can get:

$$Q = \frac{R}{\omega_0 L} = \omega_0 RC \quad (4.10)$$

Another definition of Q, called the “open-loop Q”, gives the following equation for the simple LC circuit shown in Figure 4.1:

$$Q = 0.5 \omega_0 \left| \frac{d\phi}{d\omega} \right| \quad (4.11)$$

This definition gives a better idea of how Q effects the circuit. This equation can be described using Figure 4.3. The higher the Q of the circuit, the flatter the slope in the phase versus frequency transfer function.

FIGURE 4.3 Phase response of the RLC network depicted in Figure 4.2

According to the Barkhausen criteria for oscillation the total phase shift around the loop must be an integer multiple of 2π to sustain oscillations. Any extra phase shifts in the circuit must be compensated for by a change in the instantaneous frequency. Oscillators with a large Q have better frequency stability because the required instantaneous change in frequency for a given phase shift is smaller.

4.2.2 Inductors

The inductor is probably the hardest semiconductor passive device to model and build. The classical inductor is a coil in the shape of a spring. Ideally designers would like to use a similar structure built on top of silicon substrate. However, because of current processing restrictions we must settle for simple planar spiral inductors as shown in Figure 4.4:

FIGURE 4.4 On-chip inductor shapes: a. square, and b. octagon

Other typical inductor shapes not shown in Figure 4.4 are the hexagonal and circular. Square spiral inductors are the most popular because of the ease of their layout and because all layout tools support them. Where allowed, inductors with more than four sides are preferred because of their improved performance. The problem with oscillators having more than 4 sides is that they require angles other than 90 degrees. The problem with using angles other 90 degrees is that some technologies don't support them. When other

angles are allowed, careful design procedures must be followed to keep the inductor on the design grid to avoid generating a huge number of design rule violations. Where allowed, optimum inductor performance can be accomplished using a circular inductor.

4.2.2.1 Inductor Q

The efficiency of an inductor is measured by its Q, and can be defined by:

$$Q = 2\pi \cdot \frac{\text{peak energy stored}}{\text{energy loss in one oscillation cycle}} \quad (4.12)$$

When referring to an inductor, only the energy stored in the magnetic field is of interest. Energy that is stored in the inductor's electric field is considered a loss. A simplification of the inductor model shown in Figure 4.5 is shown in Figure 4.5, where R_p and C_p represent the effects of C_{si} , C_{ox} and R_{si} .

FIGURE 4.5 Simplified model of an inductor. Note that: $C_o = C_p + C_s$

From this model the following equation can be derived using the energy equation physical model for planar spiral inductors, as present by C. Patrick Yue in [18].

$$Q = \frac{\omega L_s}{R_s} \times \frac{R_p}{R_p + \left[\left(\frac{\omega L_s}{R_s} \right)^2 + 1 \right] \cdot R_s} \times \left(1 - \frac{R_s^2 C_o}{L_s} - \omega^2 L_s C_o \right) \quad (4.13)$$

In the above equation, the first term accounts for the magnetic energy stored and the series resistance losses, the second term accounts for the substrate losses, and the last term represents the decrease in Q due to the increase in peak electric energy with frequency and the vanishing of Q at self-resonance.

Equation 4.13 can be interpreted as follows: at low frequencies inductor Q increases with frequency because term one dominates and series resistive loss are fairly constant. After an optimum point the inductor Q will start to decrease as the second and third terms in Equation 4.13 start to dominate. The reasons that inductor Q now gets lower are:

- because the skin effect causes the series resistance to increase,
- because eddy currents in the substrate cause the effective resistance of the substrate to increase,
- and because of the effects of self-resonance.

The self resonance frequency occurs at the point where the reactance of the inductor balances the reactance of its parasitic capacitances. After this point the inductor appears more capacitive than inductive. The self-resonance frequency can be approximated using the following equation:

$$f_o = \frac{1}{2\pi\sqrt{LC_o}} \quad (4.14)$$

Taking only self-resonance into account, the Q of the inductor can be approximated by:

$$Q_{ind} = \frac{\omega L_s}{R_s} \left[1 - \left(\frac{f}{f_o} \right)^2 \right] \quad (4.15)$$

As we can see from this equation when the self-resonance frequency is reached the Q of the inductor will go to zero. At this point the VCO will not oscillate no matter how much negative resistance is added in parallel to the tank. This suggests that the inductor has a finite useable bandwidth above which it cannot be used. In order for the VCO to work the

circuit should be conservatively designed well back from the self-resonance frequency to ensure a decent Q value [20].

4.2.2.2 Patterned Ground Shields

A conductive patterned ground shield reduces the substrate energy losses by terminating the inductor's electric field before it reaches the substrate. The reason for the patterning is to stop the formation of an image current in the ground shield. The image current would flow in a direction opposite to that of the current in the spiral inductor causing a negative self-inductance which would lead to a reduction in the total inductance and Q. Patterned ground shields have been shown to increase the Q by more than 30% at 2GHz [19].

The problem with patterned ground shields is that they add additional capacitance to the inductor causing the self-resonance frequency to be lower. In high-frequency designs such as that described in this thesis the inclusion of a patterned ground shield is disadvantageous. For lower frequency designs where the self-resonant frequency is much higher than the operating frequency a patterned ground shield can be used. For the best performance the ground shield should be placed as far from the inductor, and as close to the substrate as possible - in most technologies this means using the polysilicon layer.

4.2.3 Varactors [14],

Equation 4.3 shows that the oscillators' frequency of oscillation is determined by the tank's resonant frequency as described. However, this equation does not take into account process variation. A more correct equation for the resonant frequency of a oscillator would be:

$$\omega_{osc} = 1 / (\sqrt{(L \pm \Delta L_x)(C \pm \Delta C_x)}) = \omega_0 \pm \Delta \omega_x \quad (4.16)$$

In order to make up for process variations a variable capacitor, called a varactor, is used instead of, or in combination with a capacitor. A varactor is created using a reverse biased

P-N junction. Under reverse bias, the carriers in each region (holes in the P region, and electrons in the N-region) move away from the junction, leaving an area depleted of carriers. This depleted region is essentially an insulator that can be compared to a parallel plate capacitor. As the reverse bias increases, the effective width of this depletion region is increased. The depletion capacitance can be written as:

$$C_j = \frac{C_{j0}}{\left(1 + \frac{V}{\Phi}\right)^m} \quad (4.17)$$

where C_{j0} is the zero bias capacitance, V is the applied voltage, Φ is the contact potential (0.6 for Si), and m is the diode law ($m=0.5$ for an abrupt junction, and $m=0.33$ for a graded junction).

In a bipolar process varactors can be made using one, or both of the junction capacitances, C_μ or C_π , as shown in Figure 4.6.

FIGURE 4.6 Different kinds of varactors in a Bipolar process

In the technology used, NT70, the type of varactor available makes use of the base-collector junction as shown in Figure 4.7.

FIGURE 4.7 A cross section of a base-collector junction varactor

It can be seen in Figure 4.7, that a parasitic diode exists between the collector and the substrate. Care must be taken in order to minimize or remove the effects of this parasitic component so that it does not reduce the quality of the varactor [20].

The varactor can be modelled as a variable capacitance in series with a resistance (R_s) as shown in Figure 4.8.

FIGURE 4.8 Common model for the varactor diode

The resistance, R_s , comes from the undepleted semiconductor resistance and from the die substrate. The quality factor, Q , of the varactor is given by:

$$Q_{var} = \frac{1}{2\pi f C_j R_s} \quad (4.18)$$

In order to maximize Q , R_s must be minimized. To minimize R_s the varactor should be designed so that the distance between the cathode and anode is minimized. Referring to Figure 4.7 you will notice that the collector (cathode) region surrounds the base (anode) region of the varactor. Since the diode is formed over the entire surface area of the base-collector junction, the distance between the anode and cathode will be minimized using a long narrow anode in parallel with a long and narrow cathode. Taking this to the next logical step, the resistance can be reduced further by placing a cathode strip on both sides of the anode. An alternative layout, technology permitting, would have the anodes and cathodes layed out in a grid pattern - anode surrounded by cathode. The author leaves the comparison of diode layout as a topic of further study.

FIGURE 4.9 Basic Tuned Circuits

Two ways that a typical tuned circuit uses varactors are shown in Figure 4.9. In Figure 4.9a the series capacitor $C1$ is inserted to isolate the DC bias. The choice of varactor tuned circuit is made depending on your tuned circuit implementation.

4.2.3.1 Accumulation-Mode MOSFET Varactors [21], [22]

In standard CMOS processes conventional varactors typically have very low Q values. In such processes it is advantageous to use an accumulation-mode MOSFET varactor (A-MOS). A-MOS varactors are created by using a p-channel MOSFET in a P-well/substrate or a n-channel MOSFET in an n-well. This description will take into account the n-chan-

nel MOSFET in an n-well only as it is more commonly used. A cross-sectional view of the n-channel A-MOS varactor is given in Figure 4.10.

FIGURE 4.10 Cross-sectional view of the n-channel A-MOS varactor.

Referring to Figure 4.11, the capacitance of the n-channel A-MOS varactor is at a maximum when the applied voltage is far above the devices flatband voltage, V_{FB} . In this region of operation, the silicon surface is accumulated with electrons provided by the n+ regions and the capacitance seen from the gate is related only to the oxide thickness. As the control voltage, V_g , is decreased the accumulated charge on the surface of the silicon decreases. At $V_g = V_{FB}$ the device becomes charge free and below this level the surface of the device undergoes depletion. The formation of the depletion layer results in an additional capacitance in series with the oxide capacitance. This additional capacitance causes the A-MOS transistors overall capacitance to decrease. From deep accumulation to strong depletion the capacitance goes from a maximum to a minimum value.

FIGURE 4.11 Sketch of a typical voltage versus capacitance curve for an A-MOS varactor

The A-MOS varactor can be modelled in a similar manner as the conventional varactor. The model for the A-MOS varactor is given in Figure 4.12. The main difference between the A-MOS varactor and the conventional varactor is that the resistance across the tuning range also varies with the tuning voltage. The resistance of the A-MOS varactor peaks at V_{FB} and is minimized at the high and low tuning voltages - unless the A-MOS is pushed into deep depletion.

If the device is pushed into deep depletion, the formation and widening of an inversion layer adds additional resistance between the capacitor and ground. Designers should refrain from pushing the device into deep depletion because there is little reason for doing so - the additional reduction in the A-MOS's capacitance moving from depletion to deep depletion is small.

FIGURE 4.12 Common model for the varactor diode

The quality factor, Q , of the A-MOS varactor is given by:

$$Q_{var} = \frac{1}{2\pi f C_j R_s} \quad (4.19)$$

An A-MOS varactor's Q varies significantly across its tuning range due to the variability of its resistance value. However, even with this high variation in Q the A-MOS transistor's worst case Q will typically be better than that of a conventional varactor in a CMOS process. A conventional varactors Q does not vary significantly across its tuning range.

Because of the variance of slope in voltage versus capacitance curve shown in Figure 4.11 it is obvious that the K_{VCO} of the A-MOS device will vary greatly across the tuning range.

Knowing this the VCO designer should make sure that the noise on the tuning node is optimized with the highest K_{VCO} in mind. Also, the PLL that uses this VCO must take into account the worst case K_{VCO} .

The advantages of the A-MOS varactor increases as process feature size is scaled down because decreased channel length will lower the overall resistance of the device. In the future A-MOS varactors will continue to take the place of conventional varactors in CMOS, and perhaps Bi-CMOS process VCOs.

4.3 Making the circuit resonate [20]

As mentioned previously, a tank circuit will not be able to keep oscillating indefinitely with anything less than perfect components. Higher Q components will only make the ringing of the circuit more persistent. In the time domain the output of the resonant tank can be approximated by:

$$V(t) \propto V_0 e^{-t/(2RC)} \quad (4.20)$$

or,

$$V(t) \propto V_0 e^{-(t/T)(\pi/Q)} \quad (4.21)$$

From this equation we can see that the amplitude will go to $1/e$ of its initial value in Q/π cycles. Because we can not create a tank circuit with an infinite Q out of passive components, we must add feedback circuitry to generate a “negative resistance” to cancel out the

tank resistor and make it appear as if the circuit has an infinite Q . Figure 4.13 shows three methods of generating this negative resistance.

FIGURE 4.13 LC resonators with feedback: a. the Colpitts oscillator, b. the Hartley oscillator, and c. the negative resistance oscillator (Biasing not shown) [20]

In each case depicted in Figure 4.13 active components have been added to generate a gain greater than one around the loop to maintain oscillations. As shown, transistors are used to generate the amplification that an oscillator needs. At small amplitudes the loop gain will be greater than unity, however, as the amplitude of the VCO increases inherent nonlinearities of the active devices will provide amplitude limiting in each of these cases. Amplitude limiting factors are: a finite output swing, and at higher frequencies a finite slew rate.

4.3.1 The Negative Resistance Oscillator

A negative resistance oscillator with MOS transistors is depicted in Figure 4.13c. The small signal equivalent of this circuit is given in Figure 4.14:

FIGURE 4.14 Negative resistance oscillator small signal equivalent circuit

Summing the currents at node X gives:

$$I_i + g_{m1} V_{\pi 1} + g_{m2} V_{\pi 2} - \frac{V_i}{r_{e2} + r_{e1}} = 0 \quad (4.22)$$

Assuming that both transistors are biased in the same way, that:

$$g_{m1} = g_{m2}, r_{e1} = r_{e2}, V_{\pi 1} = V_{\pi 2} \quad (4.23)$$

$$I_i = \frac{V_i}{2r_e} - g_m V_i = -\frac{g_m V_i}{2} \quad (4.24)$$

Calculating the input impedance gives:

$$Z_i = \frac{V_i}{I_i} = -\frac{2}{g_m} \quad (4.25)$$

Thus in order to oscillate the equivalent parallel resistance of the tank must be:

$$r_p = \frac{2}{g_m}. \quad (4.26)$$

4.4 Linear Feedback Model of an Oscillator

Oscillators can be viewed as a linear feedback system [23]. A conventional feedback system is shown in Figure 4.15. The Barkhausen oscillation criteria for this system requires that gain of the loop be unity and that the total phase shift through the system is $n \cdot 360$ degrees ($n=0,1,2,\dots$).

FIGURE 4.15 Linear Feedback model

The transfer function for this system is:

$$\frac{v_{out}(t)}{v_n(t)} = \frac{A(s)}{1 - A(s)H(s)} \quad (4.27)$$

Which means that the loop will oscillate as long as:

$$A(s)H(s) = 1 \quad (4.28)$$

Oscillators are typically designed with a loop-gain greater than one and rely on nonlinearities in the amplifier to reduce the magnitude to exactly one in steady-state operation. The designer must ensure that the total phase shift around the loop is a multiple of 360 degrees.

4.5 Oscillator Frequency Instability

The output of an ideal oscillator is given by:

$$V_{out}(t) = V_0 \cdot \cos(\omega_0 t + \phi_0) \quad (4.29)$$

where the amplitude V_0 , the frequency ω_0 , and the phase ϕ_0 are all constants. The spectrum of the ideal oscillator consists only of an impulse at the desired frequency ω_0 . In reality, however, the output of the oscillator will exhibit a “skirt” caused by phase error or jitter. For this reason, a real oscillator is better represented by the equation:

$$V_{out}(t) = V_0[1 + A(t)] \cdot f[\omega_0 t + \phi(t)] \quad (4.30)$$

where $A(t)$ and $\phi(t)$ are functions of time, and f is a periodic function which represents the slope of the oscillator [24]. Figure 4.16 depicts the output characteristics of an ideal oscillator versus a real oscillator.

FIGURE 4.16 Output spectrum of a. the ideal oscillator, and b. depiction of the output of a real oscillator (notice the skirt on the oscillator output)

In the time domain, the time between transitions on the ideal oscillator is constant. In a practical oscillator the time between transitions will vary because of $\phi(t)$. The uncertainty between edge transitions is called the *timing jitter*.

Not taking into account timing jitter, a synchronous digital circuits data needs to be stable only $t_{setup} + t_{hold}$ for it to be captured—the black line on Figure 4.17. When a peak-to-peak

timing jitter on the clock of $\tau_{\max}$ is taken into account, the data needs to be stable for: $t_{\text{setup}} + t_{\text{hold}} + 2 \cdot \tau_{\max}$, the grey line on Figure 4.17. Therefore, jitter causes a decrease in timing margin which results in a reduction of the maximum achievable clock frequency.

FIGURE 4.17 The effect of timing jitter on timing margin

The following equation is used to describe the single sideband noise spectral density:

$$L_{\text{total}}\{\Delta\omega\} = 10 \cdot \log \left[\frac{P_{\text{sideband}}(\omega_0 + \Delta\omega, 1\text{Hz})}{P_{\text{carrier}}} \right] \quad (4.31)$$

where $P_{\text{sideband}}(\omega_0 + \Delta\omega, 1\text{Hz})$ represents the single sideband power at a frequency offset $\Delta\omega$, from the carrier in a bandwidth of 1Hz as shown in Figure 4.18. P_{carrier} is the total power under the spectrum.

FIGURE 4.18 Visualization of phase noise per unit bandwidth

The problem with Equation 4.31 is that it takes into account both amplitude and phase noise. Amplitude noise can be reduced by amplitude limiting, while there is no method to reduce phase noise. Because amplitude noise can be limited, in most practical oscillators $L_{total}\{\Delta\omega\}$ is dominated by its phase portion, $L_{phase}\{\Delta\omega\}$, which is known as phase noise.

4.5.1 Derivation of Phase Noise

In order to derive oscillator phase noise the linear feedback model of the oscillator shown in Figure 4.15 will be used. Using this model it can be determined how much the feedback system rejects, or amplifies the various noise components [25].

The transfer function for this model:

$$\frac{v_{out}(j\omega)}{v_n(j\omega)} = \frac{A(j\omega)}{1 - A(j\omega)H(j\omega)} \quad (4.32)$$

This system will oscillates at $\omega = \omega_0$: this is the point at which the transfer function goes to infinity ($A(j\omega_0)H(j\omega_0)=1$). For small deviations from ω_0 , the open-loop transfer function can be written as:

$$H(j\omega) \approx H(j\omega_0) + \Delta\omega \frac{dH}{d\omega} \quad (4.33)$$

If we assume that $A(j\omega)=A$ is a constant, we get the noise transfer function:

$$\frac{v_{out}(j(\omega_0 + \Delta\omega))}{v_n(j(\omega_0 + \Delta\omega))} = -\frac{A}{\Delta\omega \frac{dH}{d\omega}} \quad (4.34)$$

and so, the noise power spectral density is shaped by:

$$\left| \frac{v_{out}(j(\omega_0 + \Delta\omega))}{v_n(j(\omega_0 + \Delta\omega))} \right|^2 = \frac{A^2}{(\Delta\omega)^2 \left| \frac{dH}{d\omega} \right|^2} \quad (4.35)$$

Now if we use:

$$H(j\omega) = Y(\omega) e^{j\phi(\omega)} \quad (4.36)$$

which means:

$$\frac{dH}{d\omega} = \left(\frac{dY}{d\omega} + jY \frac{d\phi}{d\omega} \right) e^{j\phi} \quad (4.37)$$

For $\omega \approx \omega_0$, $Y \approx 1$, Equation 4.35 can be rewritten as:

$$\left| \frac{v_{out}(j(\omega_0 + \Delta\omega))}{v_n(j(\omega_0 + \Delta\omega))} \right|^2 = \frac{A^2}{(\Delta\omega)^2 \left[\left(\frac{dY}{d\omega} \right)^2 + \left(\frac{d\phi}{d\omega} \right)^2 \right]} \quad (4.38)$$

Noting that for an LC tank at resonance $\frac{dY}{d\omega}=0$, and taking into account the definition of Q given by Equation 4.11 yields:

$$\left| \frac{v_{out}(j(\omega_0 + \Delta\omega))}{v_n(j(\omega_0 + \Delta\omega))} \right|^2 = \frac{A^2 \omega_0^2}{4Q^2(\Delta\omega)^2} \quad (4.39)$$

which describes the noise shaping function of the oscillator.

Typically, phase noise is quoted in the form of Leeson's equation as an absolute noise referenced to the carrier power. Rewriting Equation 4.39 in this form yields:

$$PN = \frac{|v_{out}(j(\omega_0 + \Delta\omega))|^2}{2P_s} = \frac{A^2 \omega_0^2}{4Q^2(\Delta\omega)^2} \cdot \frac{|v_n(j(\omega_0 + \Delta\omega))|^2}{2P_s} \quad (4.40)$$

where P_s is the signal power. This equation is divided by 2 because amplitude noise is of less interest and the effects of AM to PM conversion are currently being ignored. $|v_n(j(\omega_0 + \Delta\omega))|$ represents the amount of noise present in the system before being shaped by the noise shaping function of the oscillator. Since the total resonator losses can be represented by a finite resistor, then:

$$|v_n(j(\omega_0 + \Delta\omega))|^2 = kT \quad (4.41)$$

Which means that Equation 4.40 can be rewritten as:

$$PN = \left(\frac{A\omega_0}{2Q\Delta\omega} \right)^2 \cdot \frac{FkT}{2P_s} \quad (4.42)$$

Where the F term is a multiplicative factor known as the device excess noise number.

4.5.1.1 Noise in the Control Path

The previous description describes the phase noise of a closed loop oscillator system. When a tuning node is added to an oscillator, this equation must be modified to take into account noise injected into the system through this node [23]. The frequency of this VCO can be described by:

$$\omega_{osc} = \omega_0 + K_{VCO}V_{cont} \quad (4.43)$$

where K_{VCO} and V_{cont} are the VCO gain and control line voltages. As discussed in the previous chapter, the input to the VCO is typically fed by some form of low-pass filter. Therefore, we can assume that the V_{cont} is a low frequency sine wave of amplitude V_m at frequency $\Delta\omega$. Using the narrowband FM approximation yields:

$$v_{out}(t) \approx A \cos(\omega_0 t) + \frac{AV_m K_{VCO}}{2\Delta\omega} [\cos(\omega_0 + \Delta\omega)t - \cos(\omega_0 - \Delta\omega)t] \quad (4.44)$$

where A is the carrier power.

Assuming that the low frequency sine wave is a noise source then the phase noise resulting from this is represented by:

$$PN = \left(\frac{V_m K_{VCO}}{2\Delta\omega} \right)^2 \quad (4.45)$$

Combining Equation 4.42 with Equation 4.45 and reporting in decibels yields:

$$L(\Delta\omega) = 10 \cdot \log \left(\left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \cdot \frac{FkT}{2P_s} + \left(\frac{V_m K_{VCO}}{2\Delta\omega} \right)^2 \right) \quad (4.46)$$

4.5.1.2 Phase Noise in Oscillators

Phase noise that originates in the VCO comes from many different sources. The components of the VCO such as the resonator and the varactor diode contribute noise to the circuit that is related to the quality factor, or Q , of the component. A component with a higher Q will contribute less noise to the oscillator output than one with a lower Q . The phase noise of the VCO is primarily determined by the overall Q of the circuit.

The active components, or transistors, in the circuit also add to the noise of the VCO. The noise contribution of these components can be minimized by careful device size selection. If careful device sizing does not provide the required performance then it may be necessary to switch design processes.

Other sources of phase noise in the oscillator are the power supply, and the external tuning voltage supply noise which can only be minimized by the careful choice of power supply.

4.6 Techniques for High-Frequency and Wideband Operation

The following sections give a brief summary of recent work in the literature relating to high-frequency oscillators and high-frequency Wideband oscillators. The sections are organized according to the tuning method employed.

4.6.1 Current Tuning

H. Knapp et al. discuss in [26] a 19.5-22GHz implemented in a SiGe bipolar process with an f_T of 50GHz. This circuit achieved a phase-noise of -91dBc/Hz at a 1MHz offset. The circuit diagram for this oscillator structure is depicted in Figure 4.19:

FIGURE 4.19 Oscillator structure

As can be seen in Figure 4.19 this oscillator does not utilize a varactor for tuning. Because this oscillator is operated at such a high frequency it makes use of the diffusion capacitance of its emitter follower transistors for tuning. The amplitude of the oscillator is large enough to cause the base-emitter junction of the emitter followers to become forward biased for a short time each cycle. During this time the diffusion capacitance in parallel with the tank circuit is increased. By increasing the gain of the circuit, and hence the amount of time that the circuit emitter followers spend in the forward biased condition the circuit can be tuned. As shown in Figure 4.19, the gain of the circuit is varied via an external control signal which controls the amount of current flowing through the current source.

A similar design presented by Klaus Ettinger et al. in [27] uses bias current to tune the parasitic capacitance of the transistors to achieve frequency. The novel element described by this paper is the stripline inductor that is used rather than a spiral inductor. This circuit achieves a tuning range from 14 to 21.5GHz and a phase noise of -85dBc/Hz at 1MHz at a bias current of 7mA.

4.6.2 Switch Tuning

A. Kral, F. Behbahani, and A. Abidi suggest in [28] two methods for switch tuning a VCO. In the first method, a switch is used to select a tuning element out of an array of tuning elements. The frequency characteristics of these tuning elements overlap such that a wide tuning range is obtained. Tuning is accomplished using a mixed analog-digital PLL which must first digitally select the appropriate tuning element and then fine tune the frequency with the analog control. A depiction of this oscillator is given in Figure 4.20.

FIGURE 4.20 Switched array of oscillators with a combined output

Two techniques for switching the tuning elements were investigated. The first technique suggested uses a MOSFET in series with the inductor. As suggested by the authors, this technique was found to greatly decrease the Q of the LC tank because of the addition of larger relative losses. The second technique solves this problem by using a MOSFET switch (the inverter) connected to a common-mode point outside the oscillator loop as illustrated in Figure 4.20.

Using this switched oscillator methodology the resultant VCO had a tuning range of 26%. This oscillator has a very good tuning range but this extra tuning range comes at the expense of an excessive amount of die area. The majority of this extra die area can be attributed to the extra inductors that are required for each of the extra tuning elements. In most practical designs, alternative methods for extending the tuning range would most likely be used.

The second method for switched tuning uses a weighted array of MOS capacitors in parallel with the inductor. This method is depicted in Figure 4.21.

FIGURE 4.21 Switched capacitor oscillator

Through simulation the authors showed that as long as the switch is turned completely ON or OFF, the switch will not degrade the Q of the capacitor. The results of the switched

capacitor measurements were incomplete so they could not be directly compared to the results obtained for the switched tuning elements.

Using this topology and technology a 26.5% tuning range is accomplished with a worst case phase noise of -117dBc/Hz at 600kHz offset in the middle of the tuning range around where we would expect to find V_{FB} for this device.

4.6.3 A-MOS tuning

A-MOS tuning is currently one of the preferred methods of tuning in a CMOS VCO. A great deal of literature has appeared recently on this topic, and a few of the more interesting papers are discussed here.

In [32], Jakub Kucera et al. implement a 2GHz wide band VCO in a Bipolar process using switched A-MOS varactors for coarse tuning and varactors for fine tuning. Bond wire inductors are used to take advantage of their high Q-factor rather than integrated spiral inductors.

The A-MOS varactors are used in the regions where their Q-factor is at its highest: in the area of weak depletion and in the region of deep accumulation. The varactor is used because its Q does not vary significantly across its tuning range, and because a varactor produces a more linear K_{VCO} curve than the A-MOS. By using a combination of varactor and A-MOS this oscillator produces a phase noise of -128.5dBc/Hz at a 600kHz offset. Because the A-MOS transistors are implemented only as switched capacitors, the phase

used in this implementation rather than integrated spiral inductors. A depiction of the circuit is given in Figure 4.23.

FIGURE 4.23 Diagram of the LC CMOS VCO. Bondwire inductors and MOS varactors realize the tank.

Two recent papers by Neric Fong et al., [30] and [31], explore the use of A-MOS varactors even further. In both of these papers the work was done using an SOI CMOS process. The first paper [30], illustrated in Figure 4.24a, deals with the differential tuning of A-MOS varactors. This paper shows that by differential tuning the A-MOS at v_c^- and v_c^+ , common-mode noise such as flicker and shot noise can be rejected. Using this topology the oscillator has a 40% tuning range and a phase noise of -121.67dBc/Hz at 3.8GHz and -111.67dBc/Hz at 5.7GHz.

The second paper [31], illustrated in Figure 4.24b, shows a band switching L-C VCO. The band-switching topology consists of two sets of varactors: a bank of switching varactors (ON/OFF only) ($C_1, C_2, \dots, C_N$), and a tuning varactor (C_t). This paper demonstrates that band switching can be used to limit K_{VCO} while maintaining the oscillators overall tuning

range. Because of the decrease in K_{VCO} , phase noise performance at the output of the oscillator was improved. This VCO had a 58% tuning range: it was tunable from 3-5.6GHz and had a phase noise performance of -120dBc/Hz to -114dBc/Hz in this range.

FIGURE 4.24 A-MOS oscillator structures where a.) single frequency band but uses differential tuning, and b.) Tunes over multiple frequency bands using Switch-tuning

4.7 Summary

In this chapter VCO design was reviewed in greater detail. Typical parameters of the VCO that might be found in a specification were described to give the user an idea of what is important to a VCO design.

Following this, general oscillator theory was reviewed. Particular emphasis was placed on the description of phase noise and its various sources in the oscillator.

In Section 4.2 the workings of the VCOs tank circuit were discussed. Instruction on the design of the LC tank and its various components were given.

The active portion of the VCO was described in Section 4.3. Various VCO architectures were presented and analysed to determine the amount of negative resistance required to make them oscillate.

Finally, recently documented techniques for high frequency operation and wideband tuning were discussed. Particular emphasis was placed on methods of switched tuning using A-MOS transistors and switched capacitors.

In the next chapter, the results of this oscillator design will be given. In addition to this, a method for switch tuning the oscillator between frequency bands will be presented along with results from simulation.

Chapter 5: Circuit Design

A pair of 20GHz VCOs have been designed. The first, a 20GHz negative-resistance VCO, was designed and implemented with varactor tuning; and the second was designed and implemented using both varactor tuning and switch tuning. This chapter covers the design process of these two oscillators.

5.1 Selected Topology, [33]

A differential Negative-Gm oscillator implementation was chosen for two reasons: because a lot of recent work had been done at Carleton using the Colpitt's oscillator configuration, and because of industrial interest in the circuit. The reason for choosing to do the oscillator differentially was because differential oscillators are less sensitive to supply and common mode noise. A basic differential Negative-Gm oscillator is shown in Figure 5.1.

FIGURE 5.1 Basic Differential Negative-Gm oscillator without Biasing

As discussed in previous sections the oscillator is broken up into two basic blocks: the active circuit and the resonant tank. In the following sections design details will be given for each of these blocks.

5.1.1 The Active Circuit

A modified version of the circuit shown in Figure 5.1 was implemented and can be seen in Figure 5.2. Transistors Q1 and Q3 were added as level shifters to increase the output swing of the circuit. Similar VCO implementations have been done before in [10] and [26], however, this is the first time that their implementation has been given in detail. A discussion of level shifting is included in Section 5.1.1.1. The output of this circuit is taken at nodes Y and Z.

FIGURE 5.2 Differential Negative-Gm Oscillator with level shifters. Biasing is not shown.

5.1.1.1 Why add the level shifters?

Figure 5.3 shows what the output should look like at nodes A and B for the basic -Gm oscillator shown in Figure 5.1. Node A connects to the base of Q5, and node B connects to its collector. When node A is about 0.6V above node B, the Collector-Base junction will be forward biased. Therefore the peak output voltage is:

$$V_{max} = \frac{V_{CB}}{2} \cong 0.3V \quad (5.1)$$

FIGURE 5.3 Oscillation at Nodes A and B for the -Gm oscillator shown in Figure .

FIGURE 5.4 Oscillation at Nodes A, B, C, and D for the -Gm oscillator shown in Figure

Similarly, Figure 5.4 shows what the output should look like at nodes W, X, Y, and Z for the -Gm oscillator shown Figure 5.2. For this circuit V_{max} is derived:

$$V_{CB} = \left(V_{CC} - V_{BE} + \frac{V_Z}{V_X} \cdot V_{max} \right) - (V_{CC} - V_{max}) \quad (5.2)$$

$$\therefore V_{max} = \frac{V_{CB} + V_{BE}}{1 + \frac{V_Z}{V_X}} \quad (5.3)$$

Assuming that V_{CB} is forward biased by 0.6V, V_{BE} equals 0.8V, and the gain is equal to one, then $V_{max} \cong 0.7V$.

Therefore, as is obvious from the explanation above, the reason for adding the level shifters is to increase output amplitude of the circuit.

5.1.1.2 Equivalent Negative Resistance

A similar analysis to that done Section 4.3.1 is now done to the differential -Gm oscillator that was shown in Figure 5.2. The small signal equivalent model of this circuit is given in Figure 5.5:

FIGURE 5.5 Small signal model of Differential Negative-Gm oscillator.

Assuming that the like transistors are biased and sized in the same way this analysis can be simplified by assuming:

$$g_{m1} = g_{m3}, g_{m4} = g_{m2}, r_{e1} = r_{e3}, r_{\pi2} = r_{\pi4} \quad (5.4)$$

Summing the currents at the output gives:

$$I_o = g_{m1} v_1 + g_{m3} v_3 + g_{m4} v_4 + \frac{V_1}{r_{e1}} \quad (5.5)$$

$$I_o = g_{m1} v_1 + g_{m3} v_3 + g_{m4} v_4 + \frac{V_o}{2(r_{e1} + r_{\pi2})} \quad (5.6)$$

$$I_o = 2g_{m1}v_1 + g_{m4}v_4 + \frac{V_o}{2(r_{e1} + r_{\pi2})} \quad (5.7)$$

which means Z_o can be derived:

$$Z_o = \frac{V_o}{I_o} = \frac{V_o}{V_o \left[-\frac{2 \cdot g_{m1} \cdot r_{e1}}{2(r_{e1} + r_{\pi2})} - \frac{g_{m4} \cdot r_{\pi2}}{2(r_{e1} + r_{\pi2})} + \frac{1}{2(r_{e1} + r_{\pi2})} \right]} \quad (5.8)$$

$$Z_o = \frac{2(r_{e1} + r_{\pi2})}{-2 \cdot g_{m1} \cdot r_{e1} - g_{m4} \cdot r_{\pi2} + 1} \quad (5.9)$$

to get to the next step, the following equations are used:

$$g_m \cdot r_e = \frac{\beta}{\beta + 1} \text{ and} \quad (5.10)$$

$$r_e = \frac{r_{\pi}}{\beta + 1} \quad (5.11)$$

From these equations, Equation 5.9 can be simplified to:

$$Z_o = \frac{2(r_{e1} + r_{\pi2})}{-(\beta + 1)} \quad (5.12)$$

$$Z_o = -2 \left(\frac{r_{e1}}{\beta + 1} + \frac{r_{\pi2}}{\beta + 1} \right) \quad (5.13)$$

Which can be approximated to:

$$Z_o \approx -2 \cdot r_{e2} \quad (5.14)$$

Thus in order to oscillate the equivalent parallel negative resistance must be $-2 \cdot r_{e2}$.

5.1.2 Resonant Tank Analysis

As mentioned previously, the LC tank is used to set the frequency of oscillation. In general the frequency of oscillation can be approximated by:

$$\omega_{osc} = \frac{1}{\sqrt{LC}} \quad (5.15)$$

This equation however does not take into account the effective parasitic capacitances added by the transistors which at the frequency of interest, 20GHz, are significant.

The schematic representation of the tank circuit in Figure 5.6 takes into account the different parasitic capacitances of the transistors.

FIGURE 5.6 The LC-tank of Figure 5.2 circuit drawn with parasitic capacitances of transistors.

The parasitic capacitances can be simplified to form two equivalent parasitic components, one is shown in Figure 5.7, on nodes A and B:

FIGURE 5.7 Parasitic capacitance on Node A or B

From Figure 5.7 the parasitic capacitance on Node A (or B) is derived as:

$$C_A \approx C_{\mu 2} + \frac{C_{\pi 1} \cdot (C_{\pi 2} + C_{\mu 1})}{C_{\pi 1} + C_{\pi 2} + C_{\mu 1}} \quad (5.16)$$

which means the equivalent parallel capacitance of the parasitic capacitances is:

$$C_{parasitic} \approx \frac{1}{2} \left[C_{\mu 2} + \frac{C_{\pi 1} \cdot (C_{\pi 2} + C_{\mu 1})}{C_{\pi 1} + C_{\pi 2} + C_{\mu 1}} \right] \quad (5.17)$$

Therefore, a more accurate equation for the frequency of oscillation taking into account the transistor parasitics is given by:

$$\omega_{osc} \approx \frac{1}{\sqrt{L \left(C + \frac{C_{\mu 2}}{2} + \frac{1}{2} \cdot \frac{C_{\pi 1} \cdot (C_{\pi 2} + C_{\mu 1})}{C_{\pi 1} + C_{\pi 2} + C_{\mu 1}} \right)}} \quad (5.18)$$

This equation is compared to the frequency of oscillation for the basic -Gm oscillator, shown in Figure 5.1, whose frequency of oscillation can be worked out to be:

$$\omega_{osc} = \frac{1}{\sqrt{L\left(C + 2C_{\mu} + \frac{C_{\pi}}{2}\right)}} \quad (5.19)$$

By comparing these two equations a second advantage of the level shifting transistors becomes apparent: they decrease the parasitic capacitance that is seen in parallel to the tank circuit.

In general the parasitic capacitances of the transistors are taken care of by the simulator. Designers usually calculate the inductor and capacitor sizes according to Equation 5.15 and then tweak the transistor and capacitor sizes after simulations are done to meet the specifications. If the parasitic capacitance of the transistors is too large they can be resized and the circuit will be simulated again.

5.1.3 Basic circuit schematic

The actual design implemented, shown in Figure 5.8, sources current from *vcc* to the transistors through its inductors. Because both sides of the inductor are at *vcc* the circuit

shown in Figure 5.2 a would require a DC bias above the voltage rail in order for the varactors to operate. The solution, as shown in Figure 5.8, was to turn the varactors around.

FIGURE 5.8 Differential -Gm oscillator with varactor diode tuning

Using the diode configuration shown in Figure 5.8 it is possible to tune the circuit while remaining within the voltage rails. A back-to-back diode configuration was not used because in order to tune the diodes within the voltage rails the cathodes of the diodes would have to be pointed at nodes 'a' and 'b' which would mean that the parasitic varactor diode would be present at these nodes. By using the configuration depicted above, the parasitic diode is effectively removed from the circuit by grounding it to the voltage rail. Also, by using a series MIM capacitor the overall Q of the capacitor is increased because the Q of the varactor (low) is averaged out with the Q of the capacitor (high). The use of large resistors on the tuning node makes sure that ac current goes through the diode to Vcc rather than to V_{bias} .

5.2 LC tank Component Sizes

The inductive and capacitive tank elements are critical components in the VCO design as their properties determine the frequency of operation as discussed in the previous chapter. Even though NT70 was a new process, the properties of its metalization process are well known because the process is shared with previous versions of the technology. This enabled the use of previously characterized inductors in the VCO design. By using previously characterized inductors from the cell library, the chance of error in the final design was reduced.

Two of these inductor structures were used: the first used separate inductors for each tank, and the second used a single centre tapped inductor that was shared between the tank circuits. The two structures are shown in Equation 5.9. The equivalent tank inductance works out to be approximately 250pH for both inductor structures.

FIGURE 5.9 a.) Centre-tapped 496pH inductor, b.) 250pH inductor

Having chosen the inductors from the library, it was necessary to determine the capacitance required to oscillate at 20GHz. The required tank capacitance can be determined using Equation 5.20.

$$C_0 = \frac{1}{(2\pi f)^2 \cdot L} = 253.3fF \quad (5.20)$$

In the capacitive structure chosen, see Figure 5.10, both a capacitor and a varactor are used to make up the total capacitance, C_0 .

FIGURE 5.10 Capacitor-varactor configuration

As shown in Figure 5.10 the varactor's cathode is connected to vcc and the anode is connected to a tuning node A. The capacitor is present to act as a dc block between the tuning node and the rest of the circuit. If a voltage source is hooked straight to Node A then the varactor would be ac shorted on both the anode and cathode side. In order not to have this short, a relatively large resistor ($1k\Omega$) was added between node A and the tuner. This configuration allows a dc path to Node A, while allowing very little ac current loss because the varactor path has a lower impedance. If it is assumed that node A is open circuit the following approximation can be made to determine the varactor and capacitor sizes:

$$C_0 = \frac{C_{var} \cdot C_{cap}}{C_{var} + C_{cap}} \quad (5.21)$$

From this equation it can be seen that in order to maximize the effect of C_{var} the series capacitor, C_{cap} , must be made as large as possible. The following table illustrates the effect of the varactor and different capacitor sizes on the tuning range of the circuit.

Cser	Cvar	Cparasitic	Ctot	Frequency	Tuning Range
6.00E-13	6.00E-13	1.00E-13	4.00E-13	1.5915E+10	7.4421E+09
6.00E-13	3.00E-13	1.00E-13	3.00E-13	1.8378E+10	
6.00E-13	1.00E-13	1.00E-13	1.86E-13	2.3358E+10	
3.00E-13	6.00E-13	1.00E-13	3.00E-13	1.8378E+10	5.6843E+09
3.00E-13	3.00E-13	1.00E-13	2.50E-13	2.0132E+10	
3.00E-13	1.00E-13	1.00E-13	1.75E-13	2.4062E+10	
1.50E-13	6.00E-13	1.00E-13	2.20E-13	2.1460E+10	3.7042E+09
1.50E-13	3.00E-13	1.00E-13	2.00E-13	2.2508E+10	
1.50E-13	1.00E-13	1.00E-13	1.60E-13	2.5165E+10	

Table 5.1 Varactor and capacitor sizing comparison

From Table 5.1 it can be seen that the value of the capacitor should be maximized, if it were possible the 600fF would have been used, however, the theory does not take into account the size of the capacitor and the area limitations that were imposed on the layout of the circuit. Because of these limitations a 300fF capacitor was used instead. Although the frequency range attained using a 300fF varactor is not as large as that of a 600fF varactor, it still allowed for a large tuning range - and it could be fit into the area available.

In Table 5.1 a fairly large parasitic capacitance component, $C_{parasitic}$, is included in the calculations. This parasitic component was quantified using post layout extraction in the Cadence Virtuoso environment (Table 5.1 rounds this value up from 96fF to 100fF). In the Virtuoso environment parasitic capacitances and resistances are extracted using scripts provided by the technology provider.

The parasitic capacitance in Table 5.1 is the sum of all the metal, and transistor capacitances on the tank circuit. The inclusion of this parasitic component into Equation 5.21 yields:

$$C_{tot} = \frac{C_{var} \cdot C_{cap}}{C_{var} + C_{cap}} + C_{parasitic} \quad (5.22)$$

A plot of the varactor's capacitive characteristics is shown in Figure 5.11. In NT70 over a tuning voltage range of 0 to 5V the variation in the capacitance of the varactor is approximately 6X. (This sounds very unrealistic - a designer should expect to get up to a 2-3X tuning range)

FIGURE 5.11 The varactor's capacitance variation due to input voltage

5.3 Switched Capacitance

The second oscillator designed uses the same negative-Gm oscillator structure and tank circuit, however, it also includes a method for switch tuning the frequency range to try and increase the circuits tuning range.

5.3.1 Switched Capacitor Design

Another way to change the frequency of a VCO is to switch in a capacitive element. The switchable capacitance can be used to add an additional capacitive element in parallel with

the LC tank circuit to decrease the frequency of oscillation. This circuit can be theoretically used to make short frequency band hops to increase the tuning range or it could be used to make a larger jump to tune in a different frequency band.

In order to add and remove a capacitor to the LC tank circuit a device is needed to act as a switch. In this technology the best device available is the npn BJT. In most analog type applications the BJT is used almost exclusively in the active mode of operation either as a current source or as an amplifier. When the BJT is used as part of a switch it is operated in the cutoff and saturated regions of operation. An example circuit and its transfer characteristics are shown in Figure 5.12 and Figure 5.13.

FIGURE 5.12 BJT inverter

As depicted in Figure 5.13, when the circuit is operated in the active region as an amplifier, the voltage gain is quite high and is equal to the slope of the transfer function. How-

ever, when the circuit is operated as a switch, in cutoff or saturation, the voltage gain is negligible- in these regions the voltages and currents do not depend on β .

FIGURE 5.13 Transfer characteristics for a BJT inverter(Figure 5.12).

The cutoff region of the transistor occurs when V_I is approximately 0.5V or less. Here, the emitter-base junction is reverse-biased and will not be conducting appreciable current. In the cutoff region the currents and voltages for the circuit in Figure 5.12 will be:

$$i_B = 0; i_E = 0; i_C = 0; v_C = V_{CC} \quad (5.23)$$

Saturation occurs when we attempt to force more current into the collector than the collector can support. At approximately $I_C = (V_{CC} - 0.7)/R_C$, the voltage difference between the base and the collector(v_{CB}) will be equal to zero. If the current into the base is increased further, the collector current will increase and v_{CB} will go negative. When the collector-base junction becomes forward biased($\sim 0.5V$), any further increase in I_B will result in a very small increase in I_C . Assuming that the collector-base junction is forward biased by 0.5V, we can find the value for I_{Csat} :

$$I_{Csat} = \frac{V_{CC} - V_{CEsat}}{R_C} = \frac{V_{CC} - 0.7}{R_C} \quad (5.24)$$

Using the minimum β for the transistor we can calculate the base current required to ensure saturation of the transistor:

$$I_{Bsat} = \frac{I_{Csat}}{\beta_{min}} \quad (5.25)$$

Past I_{Bsat} any further increase in base current will result in a decrease in the effective β of the transistor. The ratio of I_{Csat} to β can be set at will and is called the forced β :

$$\beta_{forced} = \frac{I_{Csat}}{I_B} \quad (5.26)$$

5.3.2 The Switched Capacitor Circuit

A picture depicting the switched capacitor circuit component in parallel with the LC tank is shown in Figure 5.14.

FIGURE 5.14 LC tank with switched component

Assuming this circuit were ideal, when V_{switch} is ON the capacitor C_{switch} would appear in parallel with the tank, and when V_{switch} is OFF C_{switch} will be open circuit. The equations for capacitance for this ideal case are:

$$\text{Switch = ON: } C_{tot} = \frac{C_{var} \cdot C_{cap}}{C_{var} + C_{cap}} + C_{switch} \quad (5.27)$$

$$\text{Switch = OFF: } C_{tot} = \frac{C_{var} \cdot C_{cap}}{C_{var} + C_{cap}} \quad (5.28)$$

What actually happens is that when V_{switch} is ON, C_{switch} appears in parallel with the tank having a small resistive component in series with it due to the transistor; and when V_{switch} is OFF, a parasitic capacitance appears in parallel with the tank due to the capacitance between the plate of the capacitor attached to the tank and the substrate. The effective value that the circuit sees is described by the following equation:

$$C_{switch} = \frac{C}{1 + sCR} \quad (5.29)$$

Initially the switched tuning was used to switch from 20GHz down to 10GHz, however, after some simulation this was found to be impractical because the switched capacitor dramatically reduces the tuning range at 10GHz. Using Equation 5.20 it can be seen that at 20GHz the tank circuit requires a 250fF capacitor, and at 10GHz a capacitance of 1pF is needed. To illustrate the effect of switching in the C_{switch} , let us assume C_{cap} is very large compared to C_{var} so that Equation 5.27, and Equation 5.28 can be simplified to:

$$\text{Switch = ON: } C_{tot} = C_{var} + C_{switch} \quad (5.30)$$

$$\text{Switch} = \text{OFF: } C_{tot} = C_{var} \quad (5.31)$$

Switch	Cswitch	Cvar	Ctot	Frequency	Tuning Range
ON	7.50E-13	6.00E-13	1.35E-12	8.6633E+09	2.2546E+09
	7.50E-13	3.00E-13	1.05E-12	9.8233E+09	
	7.50E-13	1.00E-13	8.50E-13	1.0918E+10	
OFF	0.00E+00	6.00E-13	6.00E-13	1.2995E+10	1.8836E+10
	0.00E+00	3.00E-13	3.00E-13	1.8378E+10	
	0.00E+00	1.00E-13	1.00E-13	3.1831E+10	

Table 5.2 Effect of switch capacitance on the oscillators tuning range, 20GHz to 10GHz.

Table 5.2, although only an approximation, shows us why switching in a capacitor to change frequency from 20GHz to 10GHz will not work. At 20GHz (C_{switch} is OFF) the circuit has plenty of tuning range; however, at 10GHz (C_{switch} is ON) the tuning range is about 1/8 of what it was at 20GHz. In reality when parasitic capacitance is taken into account the difference in tuning range between the two frequencies is closer to 4X.

The switched capacitor was now used to increase the tuning range of the inductor at the higher frequency, 20GHz.

Table 5.3 predicts how C_{switch} can extend the tuning range of an oscillator. Capacitance numbers come from the post-layout extraction and simulation. $C_{\text{parasitic}}$ is the total parasitic capacitance when the switch is OFF (the parasitic component of C_{switch} has been sub-

tracted from C_{switch} ON). Notice that the size of the varactor (C_{var}) and the capacitor (C_{cap}) have been decreased so that the oscillator frequency is in the desired range.

Switch	Tuning Voltage	Cswitch	Cparasitic	Ccap	Cvar	Ctot	Frequency	Tuning Range
ON	0	7.20E-14	1.18E-13	2.00E-13	8.60E-14	2.50E-13	2.0126E+10	6.4441E+09
	1	7.20E-14	1.18E-13	2.00E-13	1.16E-13	2.63E-13	1.9612E+10	
	2	7.20E-14	1.18E-13	2.00E-13	1.61E-13	2.79E-13	1.9050E+10	
	3	7.20E-14	1.18E-13	2.00E-13	2.54E-13	3.02E-13	1.8320E+10	
	4	7.20E-14	1.18E-13	2.00E-13	3.68E-13	3.20E-13	1.7806E+10	
	5	7.20E-14	1.18E-13	2.00E-13	5.20E-13	3.34E-13	1.7405E+10	
OFF	0	0.00E+00	1.18E-13	2.00E-13	8.60E-14	1.78E-13	2.3849E+10	
	1	0.00E+00	1.18E-13	2.00E-13	1.16E-13	1.91E-13	2.3007E+10	
	2	0.00E+00	1.18E-13	2.00E-13	1.61E-13	2.07E-13	2.2114E+10	
	3	0.00E+00	1.18E-13	2.00E-13	2.54E-13	2.30E-13	2.0994E+10	
	4	0.00E+00	1.18E-13	2.00E-13	3.68E-13	2.48E-13	2.0230E+10	
	5	0.00E+00	1.18E-13	2.00E-13	5.20E-13	2.62E-13	1.9648E+10	

Table 5.3 Tuning range of a 20GHz oscillator with switched capacitor tuning.

Note: it was a mistake to decrease the size of the capacitor, C_{cap} . If the capacitor had been left the same size it would have made a better comparison to the more generic 20GHz oscillator presented in the last section. The reduction of the size of this capacitor also caused a reduction in the circuits tuning range.

5.3.3 Switch-capacitance component guidelines

Switched capacitive components are particularly difficult to design at very high frequencies (tens of GHz). At these frequencies the parasitic components on the tank circuit make up a significant portion of the overall tank capacitance. In fact, in the 20GHz oscillator described in this thesis the parasitic component made up 1/2 to 1/3 of the total capacitance depending on which part of the capacitor tuning range is being used. To minimize the capacitance of the additional capacitor when the switch is OFF, the top plate of the capacitor used should be attached to the tank circuit of the oscillator.

The additional capacitors and transistors required to operate at this frequency increase the overall parasitic capacitance decreasing the effect of the switched capacitor. In fact at 20 GHz the addition of 72fF of capacitance through a switched capacitor came with 18fF of

additional parasitic capacitance. If this switched capacitor is decreased in size the amount of usable switch capacitance to additional parasitic capacitance due to the switch circuitry will decrease. Likewise, if the size of the switch were increased the amount of usable switch capacitance will increase.

Table 5.4 illustrates what happens as more switched capacitors are added to the circuit. As can be seen from this table, the greatest increase in tuning range occurs when a single switched capacitor is added. The reason for this is that as more switched capacitances are added the effect of varactor tuning on the overall capacitance is diminished. As can be seen, the effect of additional switched capacitances diminishes very quickly. When the number of switches increased from zero to one the range of the oscillator is increased by approximately 2003MHz. If the number of switches is incremented from one to two, an additional 800MHz of tuning range becomes available. Continuing to add switches to a total of three, four, and five causes the tuning range to grow by 325MHz, 100MHz, and -14MHz respectively. As can be seen, by the addition of the fifth switch actually causes the tuning range to decrease.

# Switches	Csw	Cpar	Cpar_sw	Ccap	Cvar min	Cvar max	Freq_max	Freq_min	Range
0	1.00E-13	1.00E-13	0.00E+00	2.00E-13	8.60E-14	5.20E-13	2.5154E+10	2.0358E+10	4.7955E+09
1	1.00E-13	1.00E-13	2.50E-14	2.00E-13	8.60E-14	5.20E-13	2.3394E+10	1.6560E+10	6.8338E+09
2	1.00E-13	1.00E-13	5.00E-14	2.00E-13	8.60E-14	5.20E-13	2.1958E+10	1.4315E+10	7.6435E+09
3	1.00E-13	1.00E-13	7.50E-14	2.00E-13	8.60E-14	5.20E-13	2.0758E+10	1.2789E+10	7.9690E+09
4	1.00E-13	1.00E-13	1.00E-13	2.00E-13	8.60E-14	5.20E-13	1.9735E+10	1.1666E+10	8.0693E+09
5	1.00E-13	1.00E-13	1.25E-13	2.00E-13	8.60E-14	5.20E-13	1.8850E+10	1.0795E+10	8.0554E+09

Table 5.4 Number of Switches versus tuning range

The analysis given in Table 5.4 does not take the whole picture into account. As the number of switches is increased and the effect of the varactor is decreased the amount of overlap between the tuning ranges at different switch settings will decrease. The designer must ensure a continuous tuning range from the top of the tuning range to the bottom. As can be seen in Figure 5.15, at 5 switches the tuning ranges at different switch settings do

not overlap, and the tuning range at different switch settings is very small. As a comparison, Figure 5.28 shows the overlap of the tuning ranges for a single switch oscillator.

FIGURE 5.15 Tuning range for a five switch oscillator. All switched capacitors are the same size.

The five switch oscillator that is described by Figure 5.15 is a poor oscillator design because of its discontinuous tuning range. This oscillator could have been made continuous by decreasing the size of the switched capacitors, however, even in this case the amount of tuning overlap between adjacent switches would be too small. The designer must ensure that the overlap of the tuning ranges between adjacent switch totals is large enough so that jitter and frequency drift on the input data stream does not cause the oscillator switch settings to change when the PLL is in lock. If the tuning range overlap is too small to compensate for jitter and frequency drift then the oscillator might be continuously bumped out of lock as a switch is toggled on and off.

Because of the required overlap between switch levels and the diminished tuning range return as more switches are added, the optimum number of switches for the design out-

lined in this thesis was found to be one switch. At lower frequencies, as the effects of parasitic capacitance on the overall tank circuit capacitance decrease, the number of switches attached to the circuit can be increased. At high frequencies it was necessary to make all of the switched capacitors minimum size; however, at lower frequencies it is possible to vary the sizes of the switched capacitors. A simple example of this is to have 4 switch capacitors of the same size and one that is half size - this configuration would give 10 tuning ranges to choose from.

In summary, the switched tune circuit can only be used if it increases the tuning range enough to warrant increased circuit complexity. Using the negative-Gm oscillator architecture at 20GHz, the use of a switch to increase the tuning range of the oscillator is limited (in the NT70 process). At lower frequencies, where the parasitic capacitances make up a much smaller piece of the overall capacitance, the switched tuned oscillator can be used effectively. In these cases, the number of switches used should be chosen such that the tuning range is maximized, and a large enough overlap between adjacent frequency bands maintained so that frequency drift and jitter (within circuit tolerances) do not cause the oscillator to change switch levels.

5.4 Results

This section describes the completed circuit, as well as tuning and phase noise results of the varactor tuned oscillator, and the varactor and switch tuned oscillator.

5.4.1 Final Circuit

The completed core oscillator circuit with component values is given in Figure 5.16. As shown in Figure 5.16, the current sources are implemented using bipolar transistors with a 150Ω series resistor. The resistor is used to provide better matching between the current sources. The reason that the supplies are labelled differently in Figure 5.16 is because they are tied to separate power pads. By not attaching these supplies the current going through the oscillator can be varied by adjusting the level of V_{cc1} .

FIGURE 5.16 Complete oscillator schematic. The location of the switched capacitor is shown with a dotted line because not all of the designs implemented it.

The 40Ω degeneration resistors in Figure 5.16 were added to improve the noise of the oscillator. The best noise improvement occurred when the degeneration was made as large as possible. The problem with adding emitter degeneration is that it degraded the gain around the oscillator. If too much emitter degeneration is added an oscillator won't start up. Figure 5.17 shows the open loop gain of the oscillator as the emitter degeneration resistor is swept.

FIGURE 5.17 Open Loop Gain

From this simulation it can be seen that the loop has a gain of one with an emitter degeneration resistor of around 50Ω . In later sections the closed loop gain of the oscillator is analysed and a discussion on how to select the amount of emitter degeneration is given.

5.4.1.1 Design Guidelines

At very high frequencies, such as those used in this thesis the selection of the tank circuit component sizes in an oscillator becomes a very important part of the circuit design. At

these frequencies the design of every portion of the oscillator is critical to its operation. In the following paragraphs guidelines are given concerning the different aspects of the oscillator design.

By reading this section the reader will obtain a better understanding about how to design a VCO. It is hoped that by reading this section the reader will be able to avoid some of the mistakes that were made as part of the learning process in this design.

1. Don't trust a pre-layout simulation. It was found that for designs at GHz frequencies every little parasitic capacitance was important: this included transistor parasitic capacitors, metal to metal parasitics, metal to substrate parasitics, etc. Pre-layout simulations did not adequately simulate the overall capacitance of the circuit. It was necessary to resimulate everything post-layout to get accurate results. Because of the effect of parasitic capacitance on the overall circuit characteristics, a designer should start layout of the circuit as soon as possible.
 2. From the required frequency the necessary tuning range required of your oscillator can be determined. This tuning range should be able to compensate for temperature, voltage, and process variation. Although it may not be academically critical to be able to compensate for all of these variations, in industry it is very important that all of these parameters are taken into account to maximize process yield.
 3. Before designing the tank circuit for your oscillator, a designer should get a feel for the various components available in their technology. If varactors and/or accumulation MOS transistors are to be used for tuning, then various simulations should be run to understand their tuning characteristics. As mentioned in the first point, it is helpful to simulate these components using an extracted netlist.
 4. Determine an oscillator architecture. This is best done by doing a literature search. When looking through different papers at frequencies similar to yours, take particular
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note as to why they chose their oscillator architecture, and whether or not it performed as expected.

5. Understand the inductor model used by the simulator. If this model does not accurately model the inductor that you are using (pay particular attention to the parasitic capacitances it attempts to model), then you should create your own inductor model to use. If possible fabricate and characterize various inductive structures.
 6. Determine the best L and C sizes for your design. At lower frequencies where parasitic capacitances are an insignificant portion of the overall tank capacitance, inductors can simply be chosen to minimize the phase noise of the design. At higher frequencies where parasitic capacitances make up a significant portion of the overall tank capacitance, the size of inductor used becomes a compromise between phase noise performance and tuning range. To minimize the effects of parasitic capacitances the inductor should be made as small as possible, and the capacitive elements as large as possible; whereas, to minimize phase noise it has been found that larger inductors perform better. The compromise between tuning range and phase noise performance is best determined using post-layout simulations.
 7. The sizing of the active components and the currents through them in the circuit is also a compromise between gain around the loop and overall noise in the oscillator. Increasing the current will increase the output power and the gain of the loop however, it may also increase shot noise leading to poorer phase noise performance. Transistor sizes must also be determined such that the effect of their parasitic capacitances on the tank are minimized. If adequate loop gain is available, emitter degeneration can be added to increase the linearity of the transistors amplifiers at the cost of some additional noise. The optimum point for the circuit described by this thesis was to use small transistors with a current slightly below that which provided maximum transistor f_T ($\sim 1.5\text{mA}/\mu\text{m}^2$).
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8. To ensure maximum testability be sure to use as many voltage supplies as is feasible: ideally, every separate path from source to ground could have its own individually tunable supply. Therefore, when selecting the probe pads for testing your circuit make sure that the selected pad has lots of test ports.
9. Finally, tape out as many designs as you can - especially if this is your first design in a new technology. By taping out an array of designs you minimize your chances of not getting any results. In these designs, be sure to vary the loop gain, oscillator test points, and whatever other devices or parameters that you are interested in.
10. Emitter degeneration is useful for improving the phase-noise performance of the circuit. However, too much emitter degeneration will not allow your circuit to oscillate. Whenever possible, run a monte-carlo or a corner simulation to get an idea of how your circuit will perform as the process is varied. If an uncharacteristic process is being used make sure that your emitter degeneration resistors are 25% or more below the point where the circuit stops oscillating in closed loop simulation.
11. Pay careful attention to all aspects of your circuit. A very well designed oscillator attached to a poorly designed output buffer results in a poorly designed oscillator.
12. Pay attention to the voltages that appear across each transistor. Make sure that the voltage across the transistors does not exceed their breakdown voltage.

5.4.2 Layout Description

The layout of the oscillator circuit is a very important part of its design. At high frequencies, like 20GHz, tank components are small and parasitic capacitances can make up a large component of the tank capacitance. To decrease the effect of parasitic capacitances the designer should layout the design as small and compact as possible. If the design is differential, the designer should also make sure that the parasitics are balanced for both signal paths. A close-up of the oscillator layout is given in Figure 5.18. The layout of the

design was done so that there is a line of symmetry down through the centre of the design. Where the design is not perfectly symmetrical, identical lengths and areas of metal were used to balance the differential signal paths.

FIGURE 5.18 Close-up of oscillator layout

Figure 5.19, Figure 5.20 and Figure 5.21 show the layouts of the three oscillators that were fabricated. As these pictures show, a guard ring of substrate contacts was placed

around the entire circuit. In addition to this, the inductors were isolated from the rest of the circuit to ensure good performance. These circuits passed both LVS and DRC checks. Because the LVS checker was unable to identify inductor structures it was necessary to create a new schematic in which the inductors were replaced with a short across the two nodes to vcc.

FIGURE 5.19 The layout of a regular varactor tuned oscillator using a shared centre tapped inductor.

FIGURE 5.20 The layout of a regular varactor-tuned oscillator with 2 inductors

FIGURE 5.21 Switched capacitor oscillator layout using a centre tapped inductor.

Three designs were taped out in order to vary the results. Figure 5.19 and Figure 5.20 are layouts for the varactor tuned oscillator. The only difference between these layouts are the inductive structures used: Figure 5.19 uses a shared centre-tapped inductors for the tank circuits, whereas Figure 5.20 uses a separate inductor for each tank. Figure 5.21 layout is similar to that in Figure 5.19 except this layout incorporates the switched capacitors.

5.4.2.1 Layout Guidelines

The oscillator should be layed out so that it is symmetrical down the middle of the design as shown in Figure 5.18. If it is not possible to lay a structure out symmetrically, then identical metal line lengths and areas should be used to keep parasitic resistances and capacitances as balanced as possible.

The higher the frequency the greater effect of parasitic capacitances. To minimize these parasitics the design should be made as compact as possible. Devices should be spaced a minimum distance apart, and the metal lines kept as far apart as possible to minimize metal to metal capacitances. When metal over metal crossovers are necessary they should be made to cross at 90 degrees, and if design rules permit the use of metal tracks at 45 degree angles can be used to decrease the distance between two points. Further parasitic capacitance savings can be had by combining devices together: for example, when using a CMOS technology transistors of the same type can be layed out to share drain/source nodes.

Because inductors couple signals into the substrate, care must be taken to isolate the inductor from the rest of the circuitry. Isolation around the inductor can be seen in Figure 5.21. The area immediately around it is left free of all types of circuitry, the width of this free space is approximately 5 line widths from the outside turn of the inductor [20]. To isolate the inductor and the rest of the oscillator from surrounding circuitry, a ring of substrate tie downs can be added around the entire oscillator. This ring of tie downs should

be connected to a grounding potential so that as little signal as possible can be passed in or out through the substrate.

Varactors are another device that should be layed out carefully. To minimize the parasitic resistance in the varactor, it should be designed so that the distance between the cathode and anode is minimized. Since the diode is formed over the entire surface area of the base-collector junction, the diode resistance is minimized by using a long narrow anode in parallel with a long and narrow cathode. Taking this to the next logical step, the resistance can be reduced further by placing a cathode strip on both sides of the anode. Alternatively, if the technology permits, the anodes and cathodes layed out in a grid pattern - anode surrounded by cathode.

5.4.3 Bipolar Switch Analysis

An ac analysis of the switch was performed to derive its capacitance and Q for when it is on and when it is off. The device under test is illustrated in Figure 5.22. The switch is formed by an npn transistor having two emitter stripes. The reason for using two stripes instead of one is to reduce the ON resistance of the transistor.

FIGURE 5.22 Switch Capacitor circuit

Figure 5.23 shows the capacitance versus current curve for transistors measuring 5-25μm in size. It is obvious from this diagram that all of the transistors when turned ON act as very good switches - the capacitance looking into the switch capacitor circuit when they are on is approximately equal to the capacitor value. When the switch is OFF, however,

circuit works better when the switch is smaller. The reason for this is that the parasitic capacitances due to the switch increase the overall OFF capacitance. Typically in a switched capacitor design we want to maximize the ratio of ON to OFF capacitance.

FIGURE 5.23 Switch capacitor capacitance versus current curve.

The next figure, Figure 5.24, shows the Q of the switched capacitor circuit versus the input current for transistors varying in size from $5\mu\text{m}$ to $25\mu\text{m}$. What this diagram shows is that in order to maximize the Q of the switch capacitor, the switch transistor size should be maximized. It also shows that by driving the switch harder we can increase the Q of the circuit by decreasing the series resistance of the transistor.

FIGURE 5.24 Switch Capacitor Q versus current curve

What both Figure 5.23 and Figure 5.24 show is that in order to design a good switch four things must be considered: the transistors size, the desired Q, the power it consumes, and the ratio between ON and OFF capacitance. In addition to these criteria one must take into account that this capacitance is actually being placed in parallel with a larger capacitor having a much higher Q. What this means is that even if the switched capacitor has a lower Q, the overall Q of the tank circuit will be much higher because the low Q in the switch will be averaged out with the higher-Q component in parallel with it. Also, it should be noted that this same switch at 5GHz instead of 20GHz will have a Q that is 4 times as high.

5.4.4 Varactor tuned Oscillator Results

An oscillator was built using the structure described in Figure 5.2, and the derived tank parameters from this section. The following diagram, Figure 5.25, describes this oscillator's frequency versus voltage characteristics:

FIGURE 5.25 20GHz Negative-Gm oscillator frequency versus tuning voltage characteristics

Because of the use of a capacitor in series with the varactor the tuning curve shown in Figure 5.21 is unexpectedly flat. Figure 5.26 plots the varactor capacitance, C_{var} ; the total capacitance, C_{tot} , and the output frequency on the same graph. Even though C_{cap} effectively lowered the tuning range it also had a linearizing effect on frequency versus voltage curve and hence it minimized the variation of the K_{vco} parameter. K_{vco} for this circuit varies only from 1.22GHz/volt to 2.05GHz/volt. Therefore, if you have excess tuning range - you can decrease C_{cap} , which will decrease and linearize K_{vco} and decrease the effect of control line noise on the oscillation frequency.

FIGURE 5.26 Capacitance, Frequency curve comparison

Using SPECTRE the phase noise for this oscillator, plotted from a 100KHz offset, is shown in Figure 5.27.

FIGURE 5.27 Phase noise response for the varactor tuned oscillator (spectre PSS simulation).

5.4.5 Varactor and Switch-tuned Oscillator Results

Figure 5.28 shows the simulated results for frequency when the switch is ON, and OFF. The tuning range of the oscillator was 6.4GHz: from 17.5GHz (switch OFF) to 23.8GHz (switch ON). This is a small improvement over the 5.96GHz tuning range that was seen using the oscillator presented in Section 5.2. As mentioned previously Ccap should be made as large as possible; had Ccap been made as large as the oscillator presented in Section 5.2, the range of the oscillator should have been about 7GHz. Finally, take note that the linearizing affect of the capacitor in series with the varactor is also evident here.

FIGURE 5.28 Frequency versus tuning voltage characteristics for a 20GHz switch tunable VCO

The phase noise for the switch tuned oscillator is given in Figure 5.29. When the switch is OFF the results are very close to the results for the varactor tuned oscillator, shown previously in Figure 5.27, and when the switch is ON the phase noise increases by a few dB. The reason for this is that when the switch is OFF the tank sees just a small capacitor to the substrate, however, when the switch is ON it will see a larger capacitance in series with the

effective resistance of the saturated transistor. The extra noise of the saturated transistor causes the increase in phase noise.

FIGURE 5.29 Phase Noise for the switch tuned oscillator (spectre PSS simulation)

The simulation results for the switch-tuned VCO are summarized in Table 5.5.

Simulation Summary	
Tuning Range	
Band 1	17.2-20GHz
Band 2	19.6-23.8GHz
Phase Noise (@2.5V)	
Band 1 (18.9GHz)	-73.5dBc/Hz
Band 2 (21.5GHz)	-75dBc/Hz
Output Power	-16dBm
Current	
Buffer	24.3mA
VCO	30.2mA

Table 5.5 Simulation Results for the Switch-tuned Oscillator

5.5 Measurements

Measurements were attempted on the oscillators when they were received from the fabrication facility. Various attempts were made to coax a signal out of the oscillator to no avail. During measurements, the circuits were visually inspected using a microscope, and the layouts were reinspected in cadence to verify that the VCO was not missing any attachments.

The test setup is described in Figure 5.30. As shown, an 80GHz spectrum analyser and five voltage sources were used to test the circuit. After attempting to get measurements on the spectrum analyser, the circuit was hooked up to an oscilloscope to see if there was a spectrum analyser problem. The oscilloscope also did not show any output, even when a high voltage sinusoidal signals were applied to the various input nodes of the circuit.

FIGURE 5.30 Test Setup

Overall DC current to the oscillator appeared to be in the proper range. However, because of limitations resulting from the circuit layout it was impossible to tell which path the current belonged to. Had the power to ground paths been sub-divided further it might have been possible to determine if the circuit was properly functioning. A larger pad ring should have been used to allow for more voltage source input and outputs.

It was not possible to come up with a definitive reason for the failure because we were unable to properly test the circuit, and because the process does not exist any longer. The following explanations are given to try and explain the failure of the circuit: the first is that there was too much emitter degeneration added to the circuit, and the second is that the output buffer for the circuit was poorly designed.

5.5.1 Problems with the Emitter degeneration

After a review of simulation data it is believed that the circuit failure could have resulted from the circuit having too little gain, or negative resistance. Too much emitter degeneration may have been added to the circuit, so that even in simulation the gain in the loop was small. The reason that this is a problem is that the process had not been qualified and that it was constantly being modified and tweaked. This was evident through the constant flow of model updates - there were 4 or 5 during the design process. The process may even have been updated even after the design was submitted.

Because NT70 was a new process it did not have simulation corner models available. In order to show the effect of process variation on an oscillator circuit, an identical oscillator structure was designed in IBM6HP which has similar process properties. The IBM6HP process is mature and very well characterized. Figure 5.31 shows a Monte Carlo simulation of this oscillator. This simulation shows that there is a 5% chance that it the oscillator

will not work. Considering that NT70 was a new process one can only surmise that he results would come out worse than this.

FIGURE 5.31 Monte-Carlo simulation of oscillator using IBM6HP

The results of a closed loop simulation, in IBM6HP, showing the oscillator output swing versus the degeneration resistance are shown in Figure 5.32. As you can see from this plot, for typical devices the oscillator works well up with up to 73Ω of emitter degeneration. This graph also shows that for worst case process conditions this device will stop oscillating with an emitter degeneration resistance of about 55Ω . It is obvious from this graph that the designer must consider worst case process parameters when designing his circuit - especially when the process is new. If the process does not supply corner models than a

designer should probably design his degeneration resistors 25-30% below the highest degeneration that can be supported using typical process corner.

FIGURE 5.32 Closed loop output swing versus degeneration resistance, for typical and worst case process parameters.

Had this been the only design that failed in this process the reason for failure could have been placed on a poor design, however, to the knowledge of the designer no other devices manufactured in this process lot have been found to be operational. Other devices produced in this technology included phase detectors, amplifiers, and VCO circuits. Having neither seen nor heard of a working device in this technology, one can assume that there may have been an error in the device fabrication process or in the process technology itself.

It was impossible to make further iterations of this circuit because of the large window of time between design tapeouts and because at the time there was a great deal of uncertainty around whether the fabrication facility would still be around. In fact, the fabrication facility was sold and closed soon after this work was finished.

5.5.2 Problems in the output buffer circuit

The output buffer circuit was used between the oscillator and the pads to isolate the oscillator. This circuit was also used to decrease the amplitude of the oscillator output to a signal level that was more appropriate for the circuitry that would have been attached to the oscillator (the phase detector). The first problem is that both circuit isolation and amplitude limiting should not have both been attempted with this circuit. In a real application the amplitude limiting would have been tied directly to the circuit following the oscillator - not to the test pads. Because this oscillator was not meant to drive any other circuit block, the design of this buffer circuit should have only focused on buffering the circuit from the pads.

The circuit described in Figure 5.33 accomplishes both the stepping down in output amplitude and buffering. However, it does so in a rather unconventional, and unplanned for way. In the design submitted the R2 and R1 resistors were made the same size. Assuming that M5 and M4 are biased in the active region, this would mean that the DC voltage between the R1 resistors and M2/M3 would be approximately 5V. This is not possible and the result is that the M5 and M4 transistors are operated in the saturation region.

Note: the reason the current source M4 and M5 uses two transistors is that it was easier to make the layout symmetrical using two instead of one transistors.

FIGURE 5.33 Output buffer circuit architecture

Because the M4 transistors are operated in saturation mode the circuit becomes very difficult to debug without having separate power supplies for the different paths through the transistor. In the active mode of operation the majority of current passes from the collector to the emitter, in saturation mode there is significant base current which complicates the analysis, and makes the circuit sensitive to process variations. As an example, in saturation the emitter of M4 has two sources through R2 or R1a, since there was only 1 Vcc pin it was not easy to isolate this buffer and force the transistors to operate in the active region.

Although this circuit performed correctly in simulation, as mentioned previously, the models provided for the transistors may have been inaccurate. If this is the case then the difficulty in debugging this circuit is compounded. Depending on the inaccuracy of the models it may be possible that transistors were not biased in the saturation region, but

were instead put into the cutoff region which would have result in the appearance of the oscillator not working when in fact it was the buffer circuit that was not able to pass on the signal. It is possible that simulation over process corners would have uncovered this problem, however, models for such corners were not available.

Finally, it came to the attention of the author after the thesis defence that devices in the same technology were found to blow up if they were biased with more than 3.3V across them. All circuits have series components so none of the circuits will directly have 3.3V across the. However, the possibility of breakdown deserves greater attention.

5.6 Summary

A pair of oscillators were designed and the results presented in this chapter. A method for switch tuning an oscillator is presented, as are the simulation results confirming that this type of frequency tuning works is given.

Lessons learned in the design of this circuit are summarized in sets of guidelines given for the design, and layout of the circuit. Following this, a guideline for the design and use of switched capacitor circuits is given.

Unfortunately neither of the oscillator circuits worked in measurements. Possible explanations for the failure of these circuits have been presented.

Chapter 6: Conclusions

6.1 Summary of Work

In this thesis the phase noise at the output of a CDR PLL has been explored and analysed. It was found that the phase-noise at the output of the PLL is largely dependant on the PLL bandwidth. For large bandwidths the phase noise of the input data stream dominates, whereas, for smaller bandwidths the phase noise of the oscillator will become a significant contributor. A 20GHz PLL incorporating an oscillator which has approximately the same phase noise performance as those described in this thesis, a bandwidth in the range of 100kHz was found to be close to the ideal. Based on these results, a suggestion on how to use a switch-tunable oscillator was made to accomplish dual-band (20 or 10GHz) CDR. The CDR PLL uses switched-tuning to balance the K_{VCO} of the high and low frequency oscillators.

Secondly, a dual-band switch tunable oscillator was designed having a worst case phase noise performance of -73.5dBc/Hz at a 100kHz offset from a 20GHz carrier when the switch was on (lower frequency band) and a -75dBc/Hz at a 100kHz offset when the switch was off (higher frequency band). The phase noise of the oscillator when the switch was off, was found to be comparable to the phase noise of an oscillator designed without a

switch which had a phase noise of: -76.5dBc/Hz . It was concluded that at 20GHz a single switched capacitor can be used to increase the tuning range effectively. It was also concluded that at lower frequencies, where parasitic capacitances are less critical to the design of the circuit, additional switched capacitors could be used to increase the tuning range even further. Both oscillator designs discussed here were fabricated, however, neither of the two designs were functional enough to generate measurement results.

6.2 Thesis Contributions

1. The effect of CDR PLL input noise and VCO noise was simulated and analysed.
 2. It was found that switched tuning could be used to adjust the K_{VCO} of an oscillator making a dual-band (20-10GHz) CDR PLL circuit feasible.
 3. A bipolar switched capacitor circuit was designed and analyzed.
 4. A 20GHz oscillator with varactor tuning was designed and fabricated.
 5. The linearizing effect on the K_{VCO} of a VCO by a varactor in series with a capacitor was documented and analysed.
 6. A 20GHz oscillator with combined switch and varactor tuning oscillator was designed and fabricated.
 7. The effect of switch noise on the oscillator phase noise output was explored.
 8. Design guidelines are given on how to design a switched-capacitor tuning circuit. Topics discussed include how to choose the number of switches, and the choice of capacitor values.
 9. Layout guidelines and techniques are documented to minimize parasitic capacitances, and to maximize matching between differential circuit paths.
 10. The effect of emitter degeneration on the oscillator across process parameters was simulated and discussed.
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6.3 Future work

There is still work left to do in the area of switched oscillator design, for example:

1. Find new applications, and configurations for the bipolar switch.
 2. Explore how to increase the quality of the bipolar switch even further.
 3. Integrate an entire CDR PLL using a switched tuned oscillator.
 4. Integrate a dual-mode switch-tuned oscillator at 40GHz/10GHz using switched tuned oscillators to match the K_{VCO} s of the two frequency bands.
 5. Do a comparison of switched capacitor and switched A-MOS design performance. It would be interesting to see how the two techniques compare against each other using the same process technology.
 6. Develop better methods for K_{VCO} tuning, and verify these methods in the design of a dual-mode PLL that can meet two different standards.
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