6GHz Active-Inductor Matched Duplexer-less LNA/PA Design Incorporated with a Bondwire-Antenna

by

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Abstract

A design technique and detailed design equations for a high frequency (above 6GHz), high-Q, active inductor (AI) is discussed using non-minimal-length CMOS technologies, such as 130nm CMOS, which can be attractive because of the bias controls available in the discussed novel topology can regulate its performance over process variations. The design is achieved via a parasitic cancellation technique. An inductance of 1.9nH is acheived at 6.75GHz with a Q of 38. The active inductor is then used to obtain a high-gain, narrowband, tuning and a output-matching element at or above 6.5GHz.

Also discussed is a design procedure for designing low-power narrowband high-gain CMOS LNAs for wireless applications at frequencies greater than 6GHz, with considerations for process variations. This procedure, used to design the LNA and test the AI, is not based on detailed derivations of equations; rather it is based on a simulation procedure and methodology that converges quickly to a practical optimized solution for LNA designs. As a result, it requires minimal time and resources from the designer. It takes a holistic design approach where all factors, including manufacturing costs, technology choice and applications are considered. The procedure conveys how to design the appropriate topology from the "ground up", and then gives the designer the option to match the ports or not; depending on if it is necessary or appropriate. The inductorless LNA specifications at 6.5GHz are: a S_{21} of 14.7dB, a NFmin of 3.3dB, a NF of 6.2dB and a S_{22} less than -15dB with only 6.4mW (plus 2.5mW for narrow-band output match) power consumption for a 1.2V supply. It should be noted that the use of the AI severely reduces the linearity of the circuit to a 1-dB compression point of -26dBm. This limits the range of operation of the LNA when used in a transceiver, but saves chip area and production costs.

The last part of this thesis discusses the design of a bondwire antenna with detailed equations showing the derivation of the radiated power, radiation pattern, and the transmitter to receiver link-budget for a bondwire-antenna for short-range radio communications in the 6.5GHz frequency range. The bondwire antenna is then used to design a high-gain, narrowband duplexer-less LNA/PA block for a transceiver with the LNA input and PA output automatically matched to the bondwire-antenna. Besides the inductive bondwire antenna, the LNA and PA are designed to be inductor-less, thus saving silicon chip area. The transceiver range is calculated to be about 4.86m, ideal for applications such as remote controls, biomedical monitoring equipment, or RFID tags. Both front end blocks are designed with low-power, low cost and high yield considerations. The inductorless LNA parameters at 6.5GHz are a S_{21} of 14.7dB, a NF of 4.9dB, S_{11} and a S_{22} less than -10dB. Also, a S_{21} of 14.4dB is achieved for the PA. A power consumption of 9.8mW for the transmit (TX) and 14.6mW for the receive (RX) is achieved using a 1.2V supply.

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1.0 Introduction

1.1 Motivation

1.1.1 Active Inductors

There are many uses for inductors, especially for filters, RF chokes, and magnetic storage devices for L-C tanks. Inductors are useful because their electronic behaviour is complimentary to capacitors since their impedance increases with frequency. With real inductors implemented using coiled wires, the impedance increases with frequency till the self-resonance frequency (SRF) is reached after which the inductor no longer behaves like an inductor, but like a capacitor. This behaviour is due to the capacitance present between the coils of the wires which become transparent to alternating currents and resonate with the inductors at the SRF. Inductors made with large coiled wires over ferrite rods (not surface-mount) have their SRF under 1 GHz, and are thus not useful beyond that frequency. In order to use the inductors at higher frequencies the coil radius needs to be decreased to the micrometer-range so as to reduce the parasitic capacitance between the coils. This is usually done on the silicon chip where the coil is "flattened" and re-shaped into either a square or an octogonal spiral with increasing radius. For frequencies under 10GHz, implementable passive inductors occupy a square area with 100μm to 300μm in width for a high Q, depending on the value of the inductance required. The capacitance to the silicon substrate can be reduced by creating perpendicular resistive ground planes which prevent Eddy-currents from flowing in the substrate and creating a "transformer-effect" which drains energy from the inductor.

With most of today's electronics technology manufactured on the silicon chip, and the length of the transistors being used decreased to a few tens of nanometers, $10000\mu m^2$ and $90000\mu m^2$ areas occupied by passive inductors are quite large and could otherwise be used for several essential RF,

analog or digital circuits in a system-on-chip (SoC) design. Additionally, silicon-chip area is costly and therefore companies generally try to minimize their total silicon-chip area used for their product. Active RC bandpass filters were first designed with feedback in 1969 [1] using operational amplifiers. As silicon technology was miniaturized, these filters were integrated onto the SoC design making active-inductor design possible. Now, with the CMOS technology within the tens of nanometers, it is sufficient to use the transistor itself as transconductance amplifier (i.e. voltage to current converter). This reduces the area of the (active) inductor to about $400\mu m^2$, which is only 4% of the silicon area occupied by a 100μm x 100μm passive inductor, saving costs and increasing functionality of the SoC. Still, as the frequencies for telecommunications increase beyond 6 GHz for everyday use, the parasitic capacitances of the transistors used reduce the SRF of the active inductors to below 6 GHz. So, the first part of this thesis is about cancelling those parasitics and increasing the usage frequency without using the transistor technology with the smallest gate length, which is, again, costly. It should be noted that beyond 15 or 20 GHz, the on-chip traces behave like transmission lines (TLs) and thus inductances can be easily generated as TLs of various lengths. Also, active inductors present operation limits to the signal amplitude for which they are used. If the signal amplitude increases beyond a certain limit, then the biasing of the transistors in the AI is no longer in the linear range and therefore this severely limits the linearity of the circuit using the active inductor. This fact has to be taken into account when designing a SoC circuit.

1.1.2 Low Noise Amplifier Design Procedure

Another component in the RF-front-end of the SoC circuit is the low noise amplifier (LNA). The second part of this thesis explains how to obtain transistor length, width and biasing parameters in order to design an LNA, considering various practical problems faced in industry.

These problems and limitations such as design topology and technology were encountered during work in various companies. Although this expertise is well-known to many RF designers, it has never been actually summarized in a paper before. The active inductor (AI) is then used to match the output of the LNA to the 50-ohm port of the network or spectrum analyzer for measurement. This was done to test the AI and the LNA design procedure.

1.1.3 Bondwire Antenna and Duplexer-less LNA/PA Design

Laboratory testing during work was the source of the bondwire-antenna concept. During the measurement of a VCO's phase noise at work, it was observed that a pencil-probe picked up the 400 MHz VCO frequency and displayed it on the Spectrum analyzer, even without touching the VCO inductor. This was achievable up to a distance of 20cm. The VCO's inductor was off-chip and was connected with bondwires to the on-chip VCO circuit. The inductor was a surface-mount component. It was deduced that the bondwires connecting the inductor to the VCO were radiating electromagnetic (EM) waves and they were being picked up by the Spectrum Analyzer's probe. Thus the idea of the bondwire-antenna was developed to be used at the same frequency range as the active inductor, i.e. 6 GHz, increasing the communication distance. It was later found that bondwire-antennas were already being used at frequencies above 30 GHz. However, the bondwire-antenna have not previously been used as a direct connection to the LNA without using antenna feed traces.

The antenna can be used for both the tranmitter and receiver. In order to obtain both functionalities, a topology was invented that allowed the LNA and power amplifier (PA) to simulteneously use the bondwire both as an antenna and as an inductor for the LC-tank for the PA. Although both uses are not an invention, their simulteneous usage has never been reported before. This dual use would be useful for RFID or medical monitoring devices, where the SoC package

uses bondwires and uses Time-Domain Duplexing (TDD) or Frequency Domain Duplexing (FDD). The duplexer-less topology is only useful for FDD if the half-duplex functionality is switched fast enough to mimic full-duplex operation. This switching is done through a single bias control TX_RXb for the design discussed in Chapter 5. This topology allows for the full integration of the LNA/PA and the antenna without losses in a feed or a duplexer. The losses due to the mismatch between the PA output and the antenna impedance are far greater due to the small size of the antenna. However, the benefits of costs savings due to full package integration may outweigh this loss.

In summary, the motivation for this thesis is the miniaturization of integrated circuits via the frequency- and Q- enhancement of an active inductor, and the integration of the LNA/PA and antenna together in a the bondwire-type package.

1.2 Contributions

This thesis includes 4 major contributions: a novel active inductor design technique, an LNA design procedure, the design of a bondwire antenna, and duplexer-less LNA/PA design for the front-end of a transceiver. The motivation for this thesis is the miniaturization of integrated circuits, and the integration of the antenna together with the bondwire-type package. The circuits discussed in this thesis are targeted for low-power, low-voltage, short-range applications like RFID-tags, remote controls or medical monitoring equipment. In the Master's Thesis, a method was developed to miniaturize the LC-tank, resulting in the U.S. patent #11/299,969 titled "On-chip tunable artificial tank circuit," which was obtained courtesy of Carleton University and Prof. J. S. Wight. The following IEEE papers and IET journal were published for the PhD (oldest first, journal is last):

1. "A Q- and bandwidth-enhancing design technique for active inductors using parasitic cancellation," *EDSSC-2008*, 8-10 Dec. 2008 (also published in SCS-2008, 7-9 Nov. 2008, co-sponsored by IEEE).
2. "High frequency low cost CMOS LNA design procedure for the wireless industry," *EDSSC-2008*, 8-10 Dec. 2008.
3. "Bondwire-antenna and duplexer-less LNA/PA design for wireless transceivers," *ISCAS-2009*, pp. 1044 - 1047, 24-27 May 2009 ("Duplexer-less LNA/PA design for wireless transceivers with bondwire-antenna" published in DTIS-2009, 6-9 April 2009, co-sponsored by IEEE).
4. "6.7 GHz high-Q active inductor design using parasitic cancellation with process variation control," *Electronics Letters*, Vol. 46, no. 7, pp.486 - 487, April 1st 2010.

1.3 Organization

In this chapter, the motivation describes how the ideas for the circuits in thesis were initially conceived and developed. Section 1.2 describes the contributions in this thesis while this section gives the organizational details of this thesis. In the next chapter, sections 2.1 to 2.4 give a literature review and background of the circuits discussed in this thesis, stating previous works in their respective subjects. Chapter 3 details the design of the active inductor, Chapter 4 gives the LNA design procedure, and Chapter 5 details the bondwire antenna design together with the duplexer-less LNA/PA design. The simulation results are given at the ends of Chapters 3, 4, and 5 for the respective designs. Chapter 6 details the measurement method, and gives a comparison between measured and simulated results. Finally, Chapter 7 provides the conclusion obtained from the simulations and measurements of the various designs, and gives recommendations and future work.

1.4 Summary

This chapter introduces the general concept of the active inductor, the LNA and the bondwire-antenna to the reader. It shows how and why these ideas were conceived and developed. It then lists the contributions. Finally it shows how the chapters in this thesis are organized. The next chapter gives the background and literature review of the circuits discussed in this thesis.

2.0 Background

This chapter gives a detailed literature review of 4 major ideas presented this thesis, namely: the active inductor (AI), LNA design procedure, bondwire/in-package antenna design and the duplexer-less LNA/PA design.

2.1 Active Inductors

Active inductors (AIs) have long been used for output filtering and image rejection at frequencies under 6GHz. They also play an important role in inductor-less LNA design, whether it is narrow-band or ultra-wide-band (UWB). LNAs that use off-chip passive inductors, or off-chip transmission lines, bias Ts [2], bondwire, or baluns for input matching are not truely inductorless, because all these passive elements have an associated inductance in them. Some designs implement the LNA stage itself with an AI-topology incorporating a passive inductor at the output [3], or use feedback in addition to the passive input matching [4] to obtain low NF. These topologies have the advantage of providing a broadband match and low NF, but are not inductorless. The advantages of using active inductors are that no off-chip components are necessary, and the technique reduces chip area since inductors are large (over 100μm square) on silicon. The disadvantage of using an AI is that it provides poor linearity since the input/output swings are limited due to MOSFET biasing requirements (to ensure the correct DC operation range).

Active inductors (AIs) have recently largely been used for loading [5] and for image rejection [6] of high-frequencies (above 6GHz), in narrowband LNAs and UWB LNAs, to increase their BW performance [5]. However, some published papers on UWB or high-frequency LNAs have not reported the performance of their AI at these frequencies [5]. They only mention optimization of

the AI with the LNA for best performance. There is no doubt this is necessary due to the number of parameters involved. Others report insufficient data on the AI performance, such as S_{11}, without a frequency range on the Smith-chart, and do not provide the equations that show the Q-enhancement [7], leaving the reader to wonder if the performace is acheived simply by the common gate input or the feedback design [8]. Yet others claim to have capacitive peaking, but fail to provide S-parameter versus frequency plots for their design [9]. There are some excellent UWB LNA design like [10, 11] that do not use active or passive inductors; however they consume 19mW or 25mW which is too much power for only an S21 of 10dB, which is in any event insufficient gain for wireless applications. Other designs which are also truely inductorless have been published, but use minimal-length CMOS technology [12, 2] which is expensive. Some papers that do report the AI performance [13] show the maximum Q at frequencies below 6GHz (lower frequencies).

Recent active GaAs technologies provide excellent transistors for high-frequency AI design [14]. However, these technologies are not currently used for volume production in industry, and are expensive.

Reference [5] uses Laplace domain equations and ω_i for various C_{gs} and g_m in the equation for deriving the AI impedance. However, it does not include the biasing parasitics of each transistor which have a profound effect on the AI's performance. It is important to note that it may be misleading to express the frequencies in the transfer functions in Laplace domain, since the s^2-term results in $-\omega^2$ in Fourier domain, revealing that the circuit may oscillate at frequencies beyond the pole frequency ω_p. Reference [5] uses the same topology as [15], but uses a sub-micron process which gives a faster performance than the GaAs MESFET technology of [15], so nothing novel is presented. Reference [5] shows nothing about the AI performance in terms of inductance and Q, or at which frequencies it provides the peaking for the UWB performance. Thus the UWB

performance could perhaps be acheived with the mentioned input-feedback and buffered-output matching.

Reference [15] has plots which show UWB performance with the regulated cascode, but only up to frequencies of 1MHz. The LNA presented in [18] shows S_{21} gain plot peaks similar to that of an oscillator, having abrupt changes in the magnitude of S_{11} and S_{22} in the vicinity of the input/ output match, bringing into question the stability of the LNA. It uses multiple simple AI topologies for band-selection, which is not suitable for high-frequency AI design.

Some topologies like [6, 16] use AI for image reject for frequencies lower than 6GHz. This AI topology is not suitable for high-frequency AI design, since the bandwidth (BW) is limited by C_{gs} and C_{gd}. If the effect of C_{gs} is removed, then the BW can be extended.

Reference [13] uses passive input narrowband transmission-line matching circuits and offset frequency S11 and S22 performances of the input and output matching between 3 stages to obtain UWB performance. Other papers like [17] use passive inductors for narrowband input-matching circuits. The need for AIs in these kind of circuits is redundant since the tuned frequency response and voltage gain have already been acheived by the input matching network. However, after several LNA stages, the RC loading of the stages produce a broadband response, increasing the output noise and the possibility of desensitization. Thus, at this point, it is useful to re-tune the signal using narrowband filter which may consist of an AI.

Recently, a paper [19] has been published detailing a method for high-frequency LNA design beyond 6GHz. In that work, the output was matched using an active inductor. In [19], the AI provides both the output match and the narrowband filtering and high-gain. Most published papers either use 1/gm=1/50 ohms buffers or passive inductors for output matching [2]. The output match converts the voltage gain to power gain, thereby reducing the NF. Other researchers use bias-Ts or

output baluns for output matching for measurement purposes [20]; this is done only so that the output voltage gain can be converted to power gain, which can in turn be measured by the Network Analyzer. In practice, the output is usually taken from the mixer and then buffered through a test-buffer in order not to load the LNA output.

The technique described in this thesis, of using an active inductor for narrowband tuning, high-gain, and output matching has never previously been used for high frequency LNAs, because the performance of active inductors is limited by the transistor parasitics and therefore the technology. If the parasitics present in the AI transistors can somehow be cancelled instead of being "halved" using differential topology [21, 18], then the AI frequency performance can be enhanced together with its Q as in [22]. This is the concept that is presented in this work. Table 1 shows the AI performance parameters obtained in this thesis.

Type	Desired	Measured
Inductance	1.2nH to 4nH	1.9nH at 6.8GHz
Power Consumption	<2.5mA	2mA
Q	>25	38
Peak Q frequency	>6GHz	>6.5 GHz (depending on bias)

Table 1: Active Inductor Specifications

2.2 LNA Design

Although some texts give a detailed explanation of the LNA function and its importance in a transciever, including what are the main noise sources and how to calculate them [23], and other books give LNA matching techniques for low noise figure (NF) and maximum gain for an already biased and sized transistor (from which S-parameters have been extracted [24]), they do not give a

transistor-level circuit design technique that results in a low noise amplifying CMOS transistor. Reference [25] gives an excellent procedure to obtain simulteneous noise and power gain matching for Bipolar transistors, but not for CMOS transistors. The final topology and CMOS transistor-level circuit design technique is left for the designer to explore. Standard topologies like common source or common gate are discussed, but the selection of current, and of transistor parameters such as length and width are left for the designer to decide.

While papers like [26] present simulators as the solution, and provide complicated flow charts to design the simulators, accurate simulators such as Eldo and Spectre already exist and are extensively used in industry. Also, while papers like [3, 27, 5, 10] give excellent theoretical analysis of the inductorless LNA using active inductors and capacitive peaking, they do not provide the exact simulation procedures they used in order to arrive at the solution for their transistor parameters (length, width and biasing). Other papers like [12] show excellent performance with simulated and measured results, but give no procedure by which they arrived at the solution for their LNA transistors.

This thesis provides a step-by-step "ground-up" procedure by which a solution can be reached for the LNA transistor parameters. Large and fast computing power enables quick simulations, thus making lengthy hand-calculations redundant for optimized LNA design. In particular, the transistor noise can now be accurately modelled. Table 2 shows the LNA specifications obtained in this work.

It should be noted that the input of the LNA was purposely left unmatched so as to obtain its NF, because it will be later seen that the LNA will be matched using a bondwire antenna, and the NF of that LNA cannot be directly measured, therefore measuring the NF of the input-unmatched

LNA and comparing to simulated results would then give the actual NF of the wireless LNA whose NF cannot be measured, but can be simulated.

Type	Desired	Measured
S11	<0dB	-2.4dB
S22	<-10dB	-28dB
S21	>10dB	14dB
NFmin	<4dB	3.4dB
NF	<7dB	6.2dB
Power Consumption	<12mA, 1.2 supply	8.2mA, 1.2V supply

Table 2: LNA Specifications

2.3 Antenna Design

On-chip antennas (OCAs) have been widely researched and used in several applications for frequency ranges above 1GHz [28]. Chip area is expensive, and therefore there is a constant push to minimize it, thus reducing production costs. At low frequencies, OCAs need to be large to provide sufficient signal to the LNA input (above the transceiver sensitivity [29]). OCAs efficiency at frequencies above 10GHz is high, and drops for frequencies lower than 10GHz since the wavelength increases, lowering the effective area of the antenna. This is especially true for low-Q inductive OCAs [28]. The large area occupied by the antenna in [28] could be useful for other components in a full SoC design.

The dielectric formed by the passivation layers in system on chip (SoC) designs introduces a loss to the incoming electromagnetic (EM) wave, thus reducing antenna gain. A further disadvantage of using non-looped on-chip antennas such as patch antennas is that although their

performance is remarkable at high frequencies, integrated circuits cannot be formed underneath the top metal layer which is usually used for the antenna [30].

The idea of using a single bondwire as an antenna in this work [31] is not completely new. Reference [32] uses the bondwires in a semi-helix antenna design. However, [32] does not provide the derivation of the antenna radiated power. Also, [32] has multiple traces on-chip as part of the semi-helix antenna, and these are resistive and therefore reduce the Q of the antenna.

There have been other designs similar to the bondwire-antenna. Reference [33] describes a half-loop antenna above a ground plane, which is effectively a circular loop antenna due to image theory [24]. Other bondwires have been used as antennas as shown in [34-36], but in applications above 30GHz, where these antennas have a much higher gain and efficiency. Authors of [37] and [28] claim a radiation efficiency of 8% at 5.2GHz for their antenna, but do not show how the radiation resistance was derived, except that it is a simulation and measured result. Therefore there is no comparison between a theoretical analysis of antenna gain (or directivity) and the simulated and measured results.

2.4 Transceivers and Duplexers

The design of transceivers has been published extensively. Most SoC or system in package (SiP) designs mention use of duplexers that can switch the signal path either from the PA to the antenna, or from the antenna to the LNA [38, 39]. However, some references neither mention the duplexer (or a similar switch), nor an appropriate antenna which would drive the receiver [40]. Reference [41] claims only a 0.6dB loss through the duplexer but does not show its design. Other designs such as [37] have the transmiter (TX) and receiver (RX) and their respective antennas on separate chips, and thus do not require duplexers. A few designs like [28] give the link budget and

operational range of the transceivers. Many designs, like [42], show excellent performance but do not show the duplexer design or give the power link budget between the transceivers. Designs like [43] show how to overcome PA leakage to the LNA via feedback cancellation of the leakage signal, but this approach requires several extra circuit blocks and has a higher power consumption. Many transceiver designs automatically assume a 50-ohm antenna source/load for the LNA/PA designs. This approach is sub-optimal unless the design is meant for SiP, since it either requires an off-chip antenna or an on-chip antenna matched to 50-ohms by components which are costly in mass production. In other words, LNA/PA design without considering the duplexer (or a similar switch), and the antenna is not useful for complete SoC or SiP integration.

Reference [44] shows an excellent topology to ground the input of the common gate LNA via an NMOS switch, thus rendering the large PA output swings null at the LNA input. Although this thesis work [31] is original, it uses a topology similar to [44] in that the signal to the input to the LNA is also grounded in the transmit mode.

2.5 Summary

This chapter gives a background and literature review of AIs, LNA, OCAs, bondwire-antennas, and transceiver designs. It describes the usage of the designs, their advantages, disadvantages, and performance limitations. It identifies a problem and presents a method for the solution to overcome some of the disadvantages of known AI designs. It considers the design procedure of the LNAs in various publications and identifies what part of the procedures have been omitted in literature, and describes briefly how this thesis offers a practical solution for the omitted procedures. It gives tables of specifications that were obtained from simulations and measured for the AI and LNA, and compares how other works on OCAs, bondwire antennas and transceivers are related to the work in

this thesis. Finally, this chapter discusses the published transceiver designs, and the importance of looking at the transceiver as a complete system in order to properly understand the functioning of the individual blocks. The next chapter gives detailed design analysis of the active inductor.

3.0 Active Inductor Design and Analysis

3.1 Initial Analysis: Developing the Concept of Parasitic Cancellation

Fig. 1 (left) shows the standard AI topology [15]. Equations (1-3) give a close form version of the equations given in [15] in jω-terms. Equations (1-3) show that the impedance reaches a peak at a certain frequency when $\left(g_{m2}g_1 - \omega^2 C_2 C_{gd2}\right) = 0$. The imaginary part of this impedance, Z_{in} is negative at this peak frequency. If it was possible to get this peaking to occur while $Im(Z_{in})$ is positive, then a high-Q active inductor or gyrator would be obtained. The equations also show that the imaginary part contains a $-\omega^2$ term that quickly decreases to become negative, resulting in the circuit behaving capacitively rather than inductively, thus making this design dependant on the transistor parasitics.

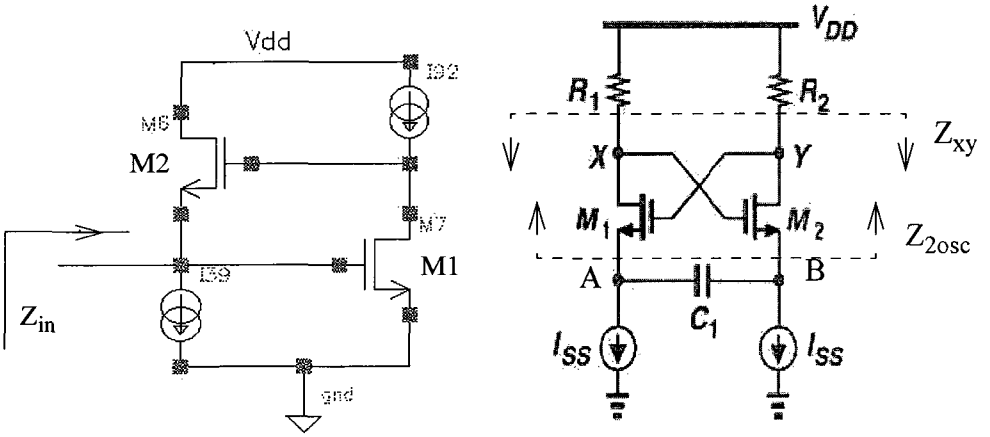

Figure 1: Basic active inductor (left) and relaxation oscillator [23].

$$Re(Z_{in}) = \frac{g_{ds1}g_1g_{m2} + \omega^2 C_1(g_{m2}C_{gd2} + g_1C_2)}{A} \quad (1)$$

$$Im(Z_{in}) = j\omega\left[\frac{C_1\left(g_{m2}g_1 - \omega^2 C_2 C_{gd2}\right) - g_{ds1}\left(g_{m2}C_{gd2} + g_1 C_2\right)}{A}\right] \tag{2}$$

$$A = \left(g_{m2}g_1 - \omega^2 C_2 C_{gd2}\right)^2 + \omega^2\left(g_{m2}C_{gd2} - g_1 C_2\right) \tag{3}$$

where $g_1=g_{m1}+g_{ds1}$, $C_1=C_{gs2}+C_{gd1}+C_{gd2}$, and $C_2= C_{gs2}+C_{gd1}$.

The new AI topology is derived from the concept of a relaxation oscillator given in [23], and shown in Fig. 1 (right). The impedance Z_{xy} is given in [23] as:

$$Z_{xy} = -\frac{2}{g_m} + \frac{j}{\omega C_1} \tag{4}$$

Reference [45] uses (4) to resonate C_1 and cancel-out the load capacitances of a quartz crystal connected between points X and Y in the design of the crystal oscillator. This means the capacitive element C_1 now presents a positive imaginary impedance similar to that of an inductor but inversely proportional to frequency. This fact can also be used "in reverse": if C_1 is removed, and the resistors R1 and R2 are both renamed R_L, the resulting circuit is shown in Fig. 2. The equivalent very basic small signal diagram of the upper cross-coupled pair of Fig. 2 is shown in Fig. 3, ignoring g_{ds1}, g_{ds2}, C_{gd1}, C_{gd2} and many other parasitics for simplification of calculation. Now the admittance Y_2 as seen differentially from points A and B is given by (5).

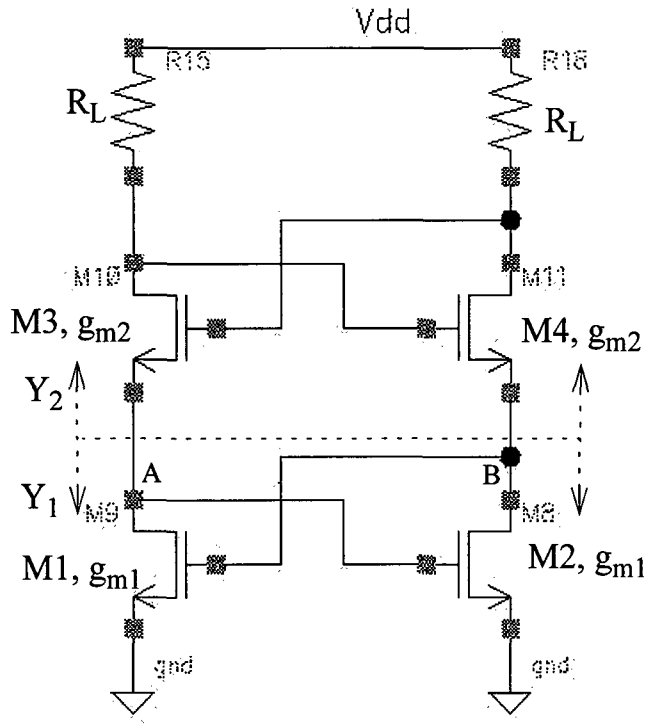

Figure 2: Basic schematic of the new active inductor.

$$Y_2 = \frac{I_{in}}{V_{in}} = \frac{Y_L(g_{m2} + j\omega C_{gs2})}{2Y_L - g_{m2} + j\omega C_{gs2}} \tag{5}$$

Here, $Y_L=1/Z_L$. The impedance represented by (5) is real with the condition that $2Y_L>g_{m2}$. This condition disappears once more parasitics are considered. The impedance $Z_2=1/Y_2$ is given by (6). The real part of impedance Z_2 increases with $(\omega C_{gs2})^2$. This means that the equivalent Q of the inductance presented by the circuit in Fig. 2 is very small at high frequency. Now consider the admittance, Y_1, of a minus-g_m-cell formed by M1 and M2 shown in Fig. 2 and given by (7). When Y_2 is put in parallel with Y_1, the resulting differential impedance $Z_{in}=1/(Y_1+Y_2)$ is given by (8).

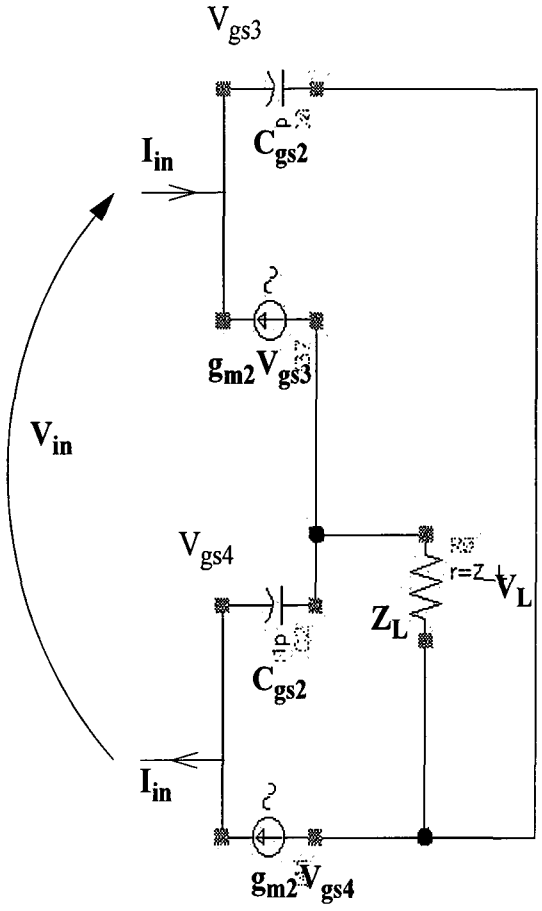

Figure 3: The small signal equivalent circuit to calculate Y_2.

$$Z_2 = \frac{g_{m2}(Y_L - g_{m2}) + \omega^2 C_{gs2}^2 + 2j\omega C_{gs2}(g_{m2} - Y_L)}{Y_L\left(g_{m2}^2 + \omega^2 C_{gs2}^2\right)} \tag{6}$$

$$Y_1 = -\frac{g_{m1} + j\omega C_{gs1}}{2} \tag{7}$$

$$Z_{in} = \frac{2(2Y_L - g_{m2}) + j\omega C_{gs2}}{2Y_L(g_{m2} - g_{m1}) + g_{m1}g_{m2} + \omega^2 C_{gs1}C_{gs2} + j\omega[2Y_L(C_{gs2} - C_{gs1}) + g_{m2}C_{gs1} - g_{m1}C_{gs2}]} \tag{8}$$

Equation (8) shows that if $C_{gs1}=C_{gs2}$ and $g_{m1}=g_{m2}$, the parasitic cancellation of the active inductor occurs, and then (8) reduces to (9), showing no dependance on the $(\omega C_{gs2})^2$-term for its real part. This ensures that the Q increases with frequency. This gives the basis for the design of a high-Q high frequency active inductor using parasitic cancellation.

$$Z_{in} = \frac{2(2Y_L - g_{m2}) + j\omega C_{gs2}}{g_{m1}g_{m2} + \omega^2 C_{gs1}C_{gs2}} \tag{9}$$

At first glance, (6) shows that if $Y_L > g_{m2}$ (the condition required for stability), then the imaginary part is actually negative, giving a capacitive frequency response. However, when Y_L is properly defined as $Y_L=g_L+j\omega C_L$, the resulting impedance given by (10) shows that the imaginary part is indeed positive.

$$Z_{in} = \frac{g_L g_{m2}(g_L - g_{m2}) + \omega^2\left(g_L C_{gs2}^2 + g_{m2}C_L^2 + 2g_{m2}C_L C_{gs2}\right) + j\omega\left(2g_L g_{m2}C_{gs2} + g_{m2}^2 C_L\right)}{\left(g_{m2}^2 + \omega^2 C_{gs2}^2\right)\left(g_L^2 + \omega^2 C_L^2\right)} \tag{10}$$

However, (10) still has the $\omega^2 C_{gs2}^2$ dependance in the real part. This would be appropriately cancelled by the minus-g_m-cell. It is important to note that (10) implies that a larger g_m is required for a smaller inductance, since the imaginary part of (10) is approximately proportional to $1/g_m$ and since the g_m for the upper M1, M2, M3 and M4 is designed to be the same to ensure parasitic cancellation.

3.2 More Detailed Analysis: Differential verses Single-Ended Operation

Differential analysis of the AI is relatively simple as voltages and currents at points A and B in Fig. 2 are taken to be 180^o out of phase. The impedance of the AI (Z_{in}) in Section 3.1 was derived

differentially, but the g_{ds} of the MOSFETs in the AI were not included. Figure 4 shows the small signal diagram of the AI that includes g_{ds} of the lower differential pair.

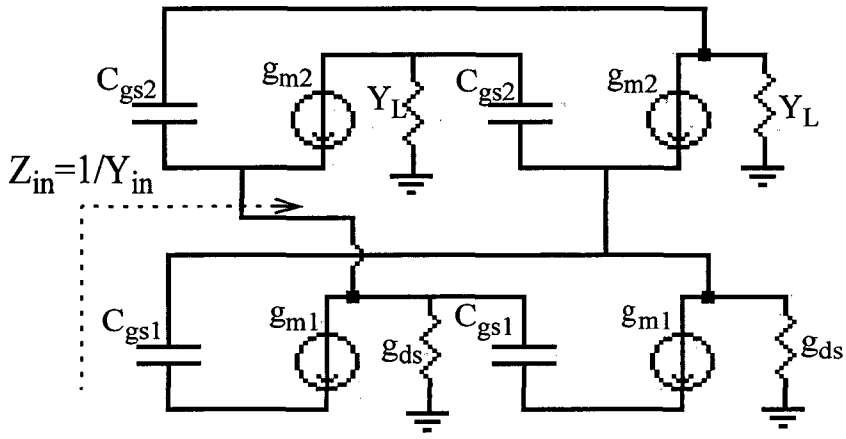

Figure 4: The small signal diagram of the Active Inductor including g_{ds}.

When g_{ds} is included in the derivation, the total admittance is given by (11).

$$Y_{in} = Y_1 + Y_2 \tag{11}$$

where $Y_1 = \frac{g_{m1} + g_{ds1} + j\omega C_{gs1}}{2}$ and $Y_2 = \frac{Y_L(g_{m2} + g_{ds2}) + j\omega C_{gs2}(2g_{ds2} + Y_L)}{g_{ds2} + 2Y_L - g_{m2} + j\omega C_{gs2}}$

When the admittance is inverted to give $Z_{in}=1/Y_{in}$, and the parasitics (i.e. $g_{m1}=g_{m2}=g_m$, $g_{ds1}=g_{ds2}=g_{ds}$ and $C_{gs1}=C_{gs2}=C_{gs}$) are cancelled assuming they are almost equal, the resulting impedance is given by (12).

$$Z_T = \frac{Z_R + j\omega Z_I}{\left(g_m^2 - g_{ds}^2\right)^2 + (2\omega C_{gs} g_{ds})^2} \tag{12}$$

where

$$Z_R = 2[2Y_L - g_m + g_{ds}]\left[g_m^2 - g_{ds}^2\right] - \omega^2 4C_{gs}^2 g_{ds},$$

and

$$Z_I = C_{gs}\left(g_m^2 - g_{ds}^2\right) + 2C_{gs}g_{ds}(2Y_L - g_m + g_{ds})$$

In (12), the negative ω^2–term in Z_R implies that Z_{in} becomes negative as ω increases. This means that at a certain frequency the circuit becomes unstable if it is driven differentially and therefore cannot be used differentially. So, although this circuit is not suitable for differential operation, it functions exceptionally well in single-ended operation. The hand-derived equation of the single-ended AI obtain from Fig. 4 is given by (13).

$$\begin{aligned}
Y_{in} &= g_{ds} + j\omega C_{gs1} + Y_1 + Y_2 + Y_3 - Y_4 \\
\text{where: } Y_1 &= \frac{g_{m1}g_{m2}(B_1 - g_{m1}g_{m2}g_1)}{B_1(Y_L + j\omega C_{gs2})} \\
Y_2 &= \frac{g_{m1}^2 g_1(Y_L + j\omega C_{gs2})}{B_1}, \quad Y_3 = \frac{Y_L(g_{m2} + j\omega C_{gs2})}{Y_L + j\omega C_{gs2}} \\
Y_4 &= \frac{g_{m1}g_{m2}g_1 Y_L(g_{m2} + j\omega C_{gs2})}{B_1(Y_L + j\omega C_{gs2})} \\
g_1 &= g_{ds} + Y_L + j\omega(C_{gs1} + C_{gs2}) \\
B_1 &= g_{m2}^2(g_{ds} + j\omega C_{gs1}) - (Y_L + j\omega C_{gs2})B_2 \\
B_2 &= (Y_L + j\omega C_{gs2})(g_{ds} + j\omega C_{gs1}) + g_{m1}Y_L(Y_L + j\omega C_{gs2})
\end{aligned} \tag{13}$$

3.3 Active Inductor Design Method and Simulation Results

The single-ended admittance Y_{in} in (13) becomes too combersome to visually analyze or simplify to show how the parasitic cancellation occurs. In order to visualize the parasitic cancellation, the hand derived equations and values of the parasitics obtained from Cadence DC simulation results were entered and plotted in Matlab. The Matlab simulation results in Fig. 5 show the parasitic cancellation effect.

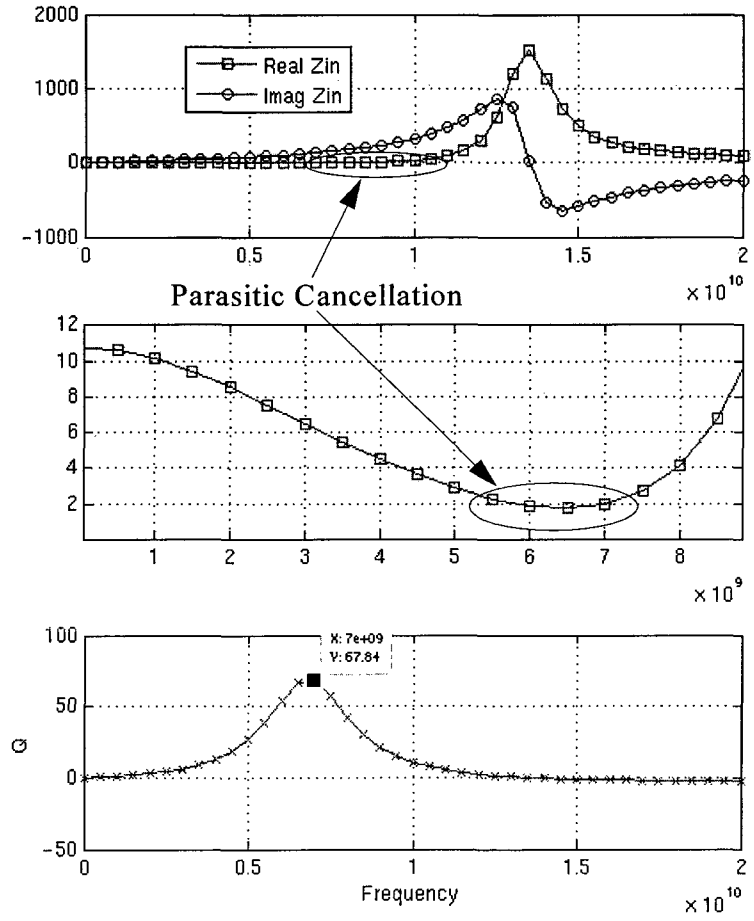

Figure 5: Matlab simulation result of the single-ended Active Inductor from the hand-derived equations.

The basic circuit that was realized for the AI is shown in Fig. 6. The biasing is controlled via the biasing resistors R_B and the circuit is loaded with a resistor R_L. Choosing the appropriate values for Y_L gives parasitic cancellation yielding a high-Q, high-frequency active inductor. These biasing controls can be adjusted to ensure that the circuit will operate over process variations. The coupling capacitors with the bias resistors also provide a phase shift necessary to ensure the circuit is stable over all frequencies.

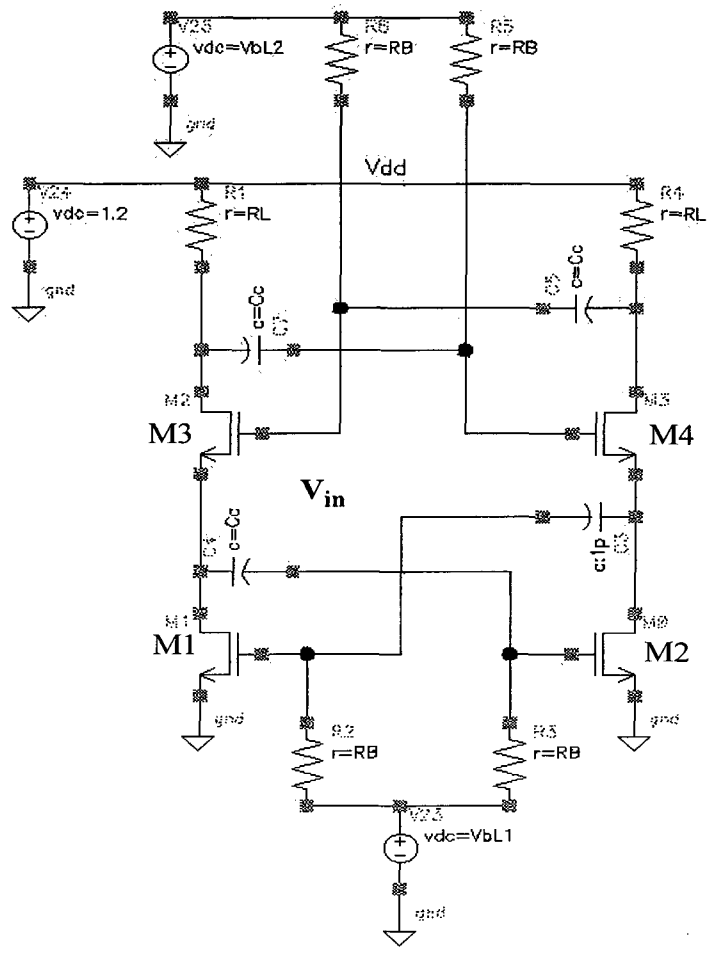

Figure 6: Schematic of the Active Inductor with Resistive loading.

The AI design topology was entered and simulated in Cadence using Spectre. The widths of all NMOS transistors were chosen to be the same to ensure parasitic cancellation. The transistor widths were increased to provide the g_m and C_{gs} values obtained from the Matlab simulation that gave the inductive response at the desired frequencies, while the load resistors were decreased to allow for correct biasing conditions for the transistors. The resistors were increased to obtain high-Q and decreased to provide stability. VbL1 was increased to obtain high frequency operation while VbL2 was kept constant at 1V. The final transistor parameters used were determined by the low-noise widths and number of fingers as obtained in the procedure detailed in the chapter 4, since the AI was to be used at the output of the LNA, and it was required to keep the noise output of the AI to a minimum.

It should be noted that the load resistors R_L have a minimum of 10% process variation. For this reason, the load resistors were replaced with PMOS transistors in triode region of operation, where their g_{ds} (gate to drain conductance) provides the equivalent resistance of $1/R_L$. The PMOS output resistance can be controlled with the gate bias voltage, which can track process variation. The Cadence schematic and layout was created are shown in Fig. 7 and Fig. 8. Although this circuit is similar to the one in [46], the PMOS transistors are in triode region instead of saturation, and are not acting as current sources. Since the PMOS transistors present a larger load to the amplifying NMOS transistors, the current consumption of the AI was increased from 600uA to 2mA. The Cadence simulation result showing the real and imaginary impedance together with the Q of the AI is shown in Fig. 9. Although this frequency response shown in Fig. 9 is comparable to the result in Fig. 1 in [47], the high-Q AI in [47] is susceptible to process variation.

Comparing the frequency response of the AI in Fig. 9 with the one obtained from Matlab in Fig. 5, it can be seen that the self-resonance frequency is lower by 5 GHz since not all the parasitics

were taken into account in generating the Matlab plot. In order to demonstrate the advantage of the bias controls over process variation, five corner simulations were done to obtain the similar inductance and Q. Table 3 shows the corner simulation results with bias voltages for an inductance of approximately 2.6nH inductor with a Q of 40, where VbL2 was maintained at 1V for the simulations.

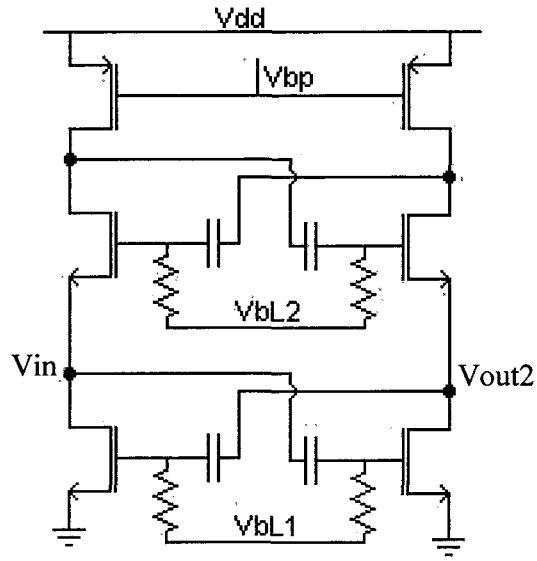

Figure 7: Basic schematic of the novel active inductor with resistive load replaced by PMOS transistors in triode region of operation.

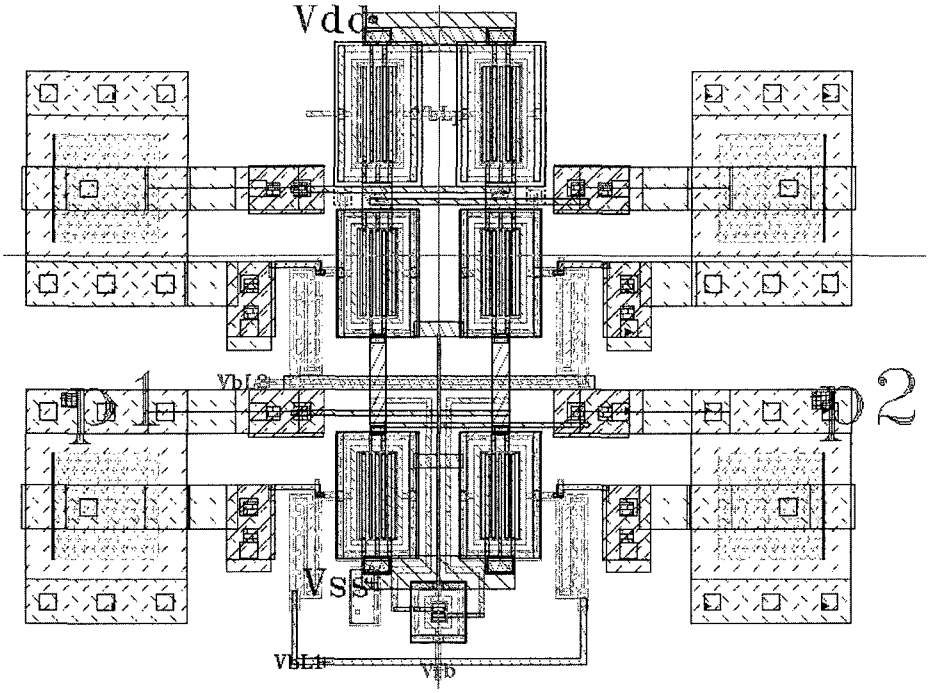

Figure 8: Layout of the new active inductor.

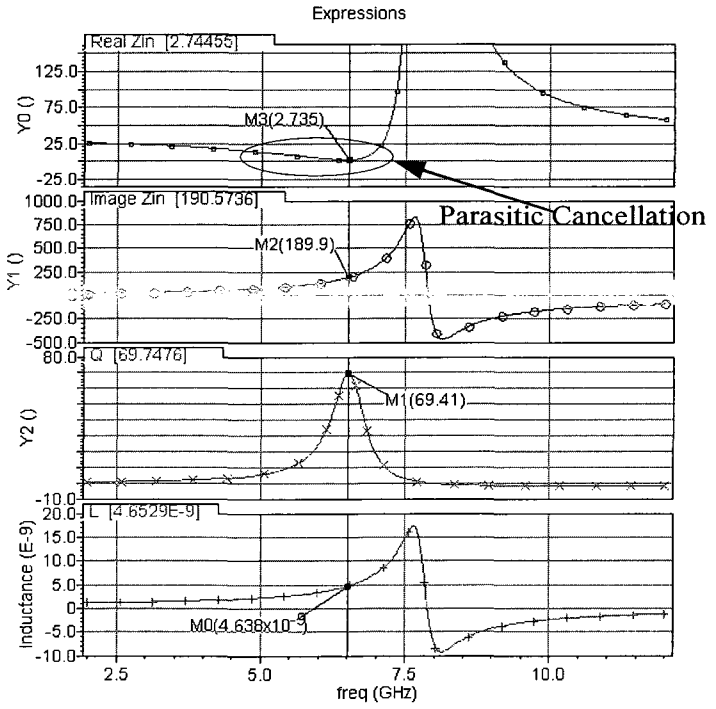

Figure 9: Post layout simulation plot from Cadence showing the Impedance and Q of the active inductor.

Corner	VbL1 (mV)	Vbp (mV)	inductance (nH)	Q	% Deviation of inductance from typical
tt	530	436	2.6567	41.78	
ss	570	379	3.6424	30	37%
ff	480	517	2.7096	40.4	1.9%
sf	570	439	2.6949	41.12	1.44%
fs	504	413	2.47	40.27	-7.17%

Table 3: Post Layout Corner Simulation Results of the Active Inductor.

As mentioned in the abstract, the AI presents a limitation to linearity. In order to explore this fact, transient simulations were done by applying a small sinusoidal voltage at the input node of the AI at point A in Fig. 2, and plotting the output voltage amplitude at point B. The input voltage was increased in a parametric simulation and the result is shown in Fig. 10. This result shows that the maximum input voltage before the AI enters compression is 75mV.

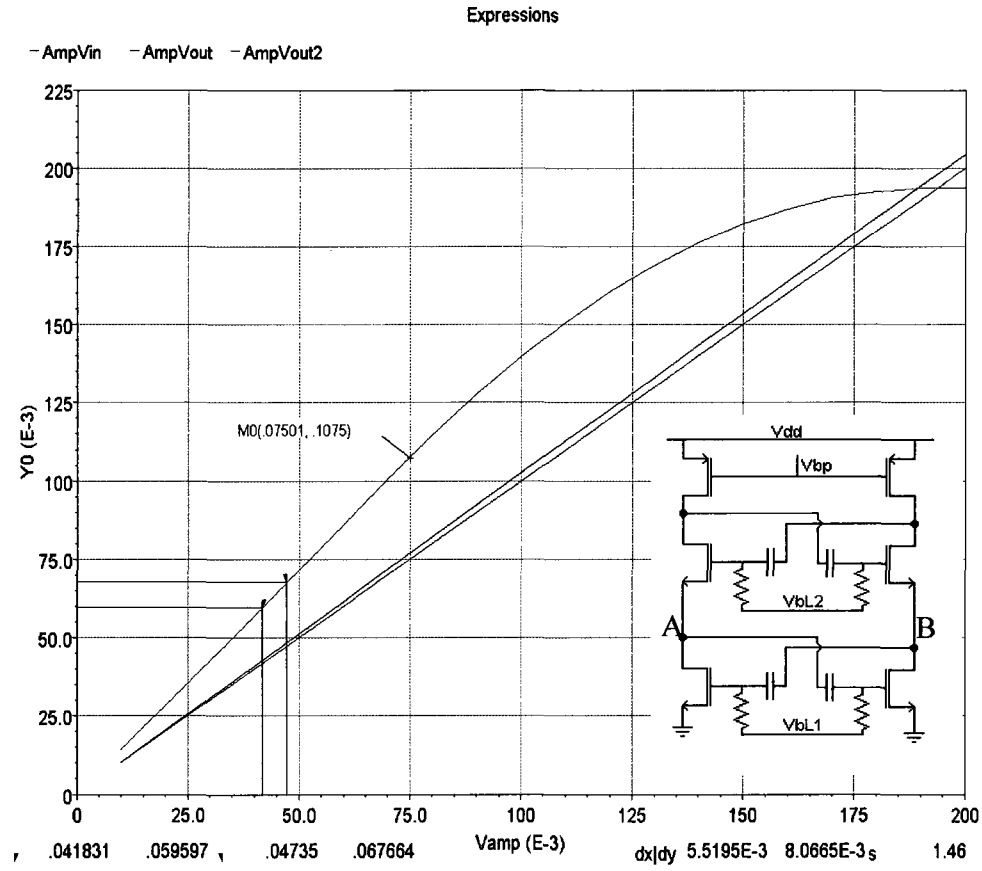

Figure 10: Post layout simulation of the active inductor showing compression of Vout2 at point B when Vin is at point A is increased.

3.4 Active Inductor Application

As mentioned in Chapter 2, AIs have most commonly been used as output loads for tuned narrowband circuits, for image reject circuits, and for peaking near the bandwidth edge of a broadband or UWB circuit. There is another application for which the AIs can be, but are not commonly used; in an output matching network as shown in Figure 11. In order to test the AIs capabilities, an LNA was designed for a wireless application, considering factors such as process

variation, simplicity, yield, measurability, and usability in industry. The following chapter describes the LNA design methodology.

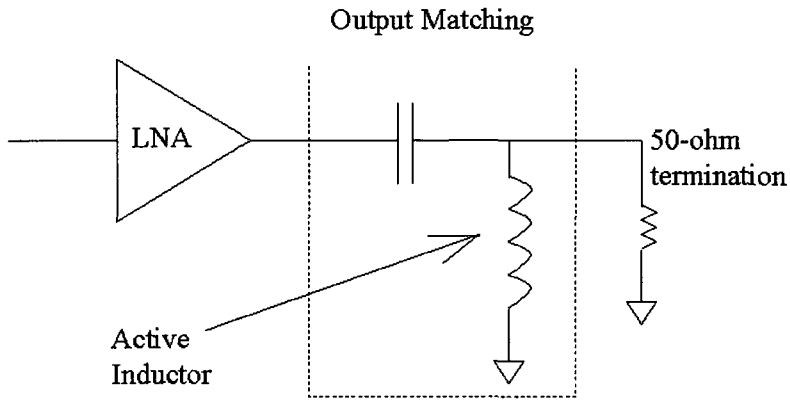

Figure 11: Active inductor usage for LNA output matching.

3.5 Summary

This chapter analyzes the equations of the input impedance of the standard AI topology and describes the development of a new AI. It shows why the AI can only be used single-endedly and not differentially. It gives detailed hand-derived equations, which can be used with a program like Matlab, to show how parasitic cancellation can be acheived using the new AI topology and simple transistor models. It shows how the biasing components can be used for process tracking. It also shows the small signal limitations in which the AI is utilizable. It gives the simulation results and final AI topology and layout that was submitted for manufacturing. Finally this chapter presents a possible use of the AI that is not commonly considered: as an output matching network for an LNA. The next chapter gives the LNA design procedure used to design the LNA that will to be used to test the AI.

4.0 LNA Design Procedure

This chapter discusses general issues concerning LNA design procedures. The procedure assumes the basic graphs from literature are available to designer and can be used as a starting point. It also assumes that the simulation tools generally used in industry are also available to the designer, and that the designer will be designing an LNA for a whole system-on-chip rather than the LNA as a block-component by itself.

4.1 Deriving LNA Specifications

The available Bit Error Rate (BER) versus Signal to Noise Ratio (SNR) graphs for various modulation schemes determine the minimum system SNR that a system requires in order to correctly demodulate the signal. The minimum system noise figure (NF) (not to be confused with NFmin - the NF that the LNA exhibits with both its input and output ports matched to the port impedances) that is required is calculated from the minimum power that is available from the antenna to the LNA, using the sensitivity equation given in [9]. A good approximation of the total NF added by the components after the LNA is 3 to 7dB, depending on the image-reject architecture and the down conversion architecture used. Thus, in general, an LNA design with a NF below 7dB is usually sufficient for short range applications using basic modulation schemes like FM, FSK, BPSK and QPSK. Other more complex modulation schemes like 16-QAM require a NF of less than 4dB from the LNA.

4.2 Determining Technology

There is a continuous push in industry for low voltage and low power consumption for mobile units. This means that, for example, designs in technologies such as 0.18μm using 1.8V may have to be implemented using a 1V supply. This reduces other parameters like linearity, gain per stage,

and the ability to provide a fully differential circuit design in order to reduce second-order intermodulation (IP2). Since CMOS has excellent performance in digital circuits, and since the technology used for the digital core is usually the same as that used for the front-end receiver, this requires a compromise in performance. Current CMOS technologies available are: 0.35μm using 3.3V supply, 0.18μm using 1.8V supply, 0.13μm using 1.5V supply, 90nm using 1.2V supply, 65nm using 1.2V supply, 45nm, and 32nm. Many designs use supply voltages lower than those given by the manufacturer, but care must be taken not to push the transistors into the triode region of operation, where the gain is diminished. Smaller technology means lower voltage and higher gain at higher frequency of operation, but the resulting low R_{ds} requires a larger g_m for higher gain.

4.3 Determining Topology

4.3.1 Gain, Bandwidth and NF

Several papers on UWB low-noise amplifiers have recently been published using active inductors (AIs) that extend the bandwidth and provide larger gains. However, these papers fail to mention the fact that transistor parameters in the AIs are subject to process variation, and this greatly affects the performance of the active inductors. LNA/AI performance dependancy on process variation is not mentioned in any published paper known to the author. Also, current consumption of greater than 10mA results in battery drainage, requiring frequent recharge of the appliance. Thus there is lack of use of active inductors for LNA loads in industry at high-frequencies.

Some high frequency or UWB circuits require the smallest transistor lengths and this is dependant on process technology as discussed in [2, 12]. These technologies are costly for mass-production and have more process variation than their larger counterparts. Thus, the use of UWB LNAs based on small geometry transistors is impractical in low-power wireless systems since

transmitted signals in wireless transceivers are usually narrow band, and are vulnerable to desensitization from interferers.

Input matching via feedback causes a reduction of gain, requiring more DC power consumption for a required SNR. Low gain implies that more amplifier stages would be required before the analog to digital converters (ADCs), which ultimately increases the total NF. Therefore S_{21}=6dB [2] to 11dB [10, 11] is insufficient to increase system SNR and lower NF requirements, especially when lossy, high NF blocks are used for signal down conversion or image rejection. Thus a minimum S_{21} of 20dB is often required to amplify the miniature voltages, of the order of a few sub-micro-volts, to the sub-millivolt or millivolt range.

Common gate LNAs provide 1/gm=50 ohm matching but do not provide the isolation that is required from the output to input. In this topology, the V_{gs} and V_{ds} change at the same time as V_s changes with the input voltage, thus reducing the isolation. This is needed to ensure isolation from supply noise, the frequency domain duplexing (FDD) or time domain duplexing (TDD) switch leakage, and LO leakage in the case of direct conversion. The NF is also higher for this topology. For these reasons common gate LNAs are seldom used in industry.

Cascode LNAs provide excellent gain for low NF and reverse isolation. However the headroom required to ensure both the common source and cascode transistors are in saturation is not always available in the case of low-voltage circuit designs, or in the case where the passive inductive load is not used (e.g. the case of packaging without bondwires for LNA designs that do not use bondwires as inductive loads).

Differential common source or cascode is desirable only if the antenna is itself differential, e.g. a dipole. Most antennas designed in industry are single-ended and therefore the LNAs are single-ended as well. Later amplifier stages can be made differential.

Thus, if voltage supply headroom is available, a cascode topology should be used, and if not, then the simple common source is sufficient. It should noted be that common source topology gives a slightly lower NF than the cascode due to the number of transistors in the cascode.

4.3.2 Linearity, Chip Area and Biasing

In addition to NF, the LNA must exhibit excellent linearity so that interferers do not easily desensitize the LNA, unless the transceiver is designed for short-range applications where it is well known that the desired signal level has a high probability of being larger than any interferer. Interferers at the LNA input are unavoidable except by having a high-Q band pass filter at the input, which usually is part of the matching network. The series resistance of low-Q inductors injects noise into the gate of the LNA increasing the LNA's NF. Many topologies have the output loaded with an inductor. This is usually not necessary as band pass filtering is already done via the input matching network. Resistive degeneration increases linearity but also increases NF and reduces gain. Increasing the current can also increase linearity, but comes as a cost to the customer in terms of the number of recharges that are required. It is greatly advantageous to use bondwires as inductors for load, or source degeneration, however this is limited to the type of packaging used by the System On Chip (SoC).

Many packages do not use bondwires to connect the integrated circuit (IC) to the PCB, but use solder balls, PCB traces, and bumps on the IC to connect it to external inputs, outputs and controls. Thus in many cases using the bondwires as an input matching inductor, load inductor and/or source degeneration is not always possible. Since the LNA is a crucial but very small part of the total circuit, packaging requirements are not determined by its chip area, but rather the whole system and its power consumption. For cases such as base stations where power is readily available, packages that easily dissipate heat are used. In these cases bondwires are not used since power requirements could melt the bondwires. Many modern packages have several layers (usually 7), in

which resistor, capacitor, and inductor components are inserted. These components save total IC area and cost, since the packaging costs are usually much lower than IC fabrication costs.

Thus, if one is designing for a mobile unit, then one uses bondwires for matching, loading, and source degeneration; and if the circuit being designed is for the base station, then larger current consumption can be used to obtain a lower NF and higher linearity. However, since there are far fewer base stations than mobile units, the LNA design for the base station can afford the increase in chip area for on-chip inductors.

In many cases the antenna is usually on the PCB or the package, and the antenna itself provides the bandpass filtering required to suppress the interferering frequencies. This is usually the case in which the image reject transceiver architecture is used.

Although passive inductive loads provide extra headroom for low-voltage LNA topologies, they are not necessary for tuning if a passive inductive/bondwire matching network is already used. Also, inductive loads can cause oscillations due to feedback through C_{gd}. They can also cause device breakdowns since they allow the output voltage to swing larger than Vdd. Thus, in many cases a small resistor is used in series with the bondwire load to reduce its Q. Also, in many cases resistor-only loading is used, or a current source is used. In the case of resistive loading, the current of the LNA first stage is controlled via a bias voltage that is set to track the process variations of both the resistor and the g_m of the LNA transistor, which can be due to the variations in its length and width, in order to give a low NF and high yield.

In the case of the current source, the g_m is controlled via the current, and the bias voltage is also varied with the bandgap and regulator supplies. PMOS current sources used for biasing at lower frequencies as in [20, 48], are rarely used for biasing at high frequency, due to the excess capacitive loading that PMOS transistors present at the output. This is because a larger current is

required from the LNA transistor for the same gain, unless the technology being used to design the LNA is such that the PMOS current source presents minimal loading at the LNA output, as in [12]. Also, the resistors chosen for loading are normally sized with larger than minimum width that is required for the LNA current density in order to increase their tolerance (i.e. obtain a lower percentage tolerance). In this thesis, high-precision metal resistors were used for LNA loads, and large poly-resistor arrays were used to provide matching ratios for voltage biasing. Although resistor arrays would never be used in industry except to generate a process variant voltage that can be compared against a reference, it is sufficient to provide the correct bias voltages for the LNA transistors for this testcase. In industry, the resistor ratios would be used to provide a reference voltage to a regulator, from which a separate bias voltage would be generated via current mirrors. The current mirrors not only provide matching in this case, but also provide sufficient supply to signal isolation via the capacitive dividers that are formed by Cgd and Cds of the current mirror transistors. Figure 12 shows a process tracking architecture that could be used in industry.

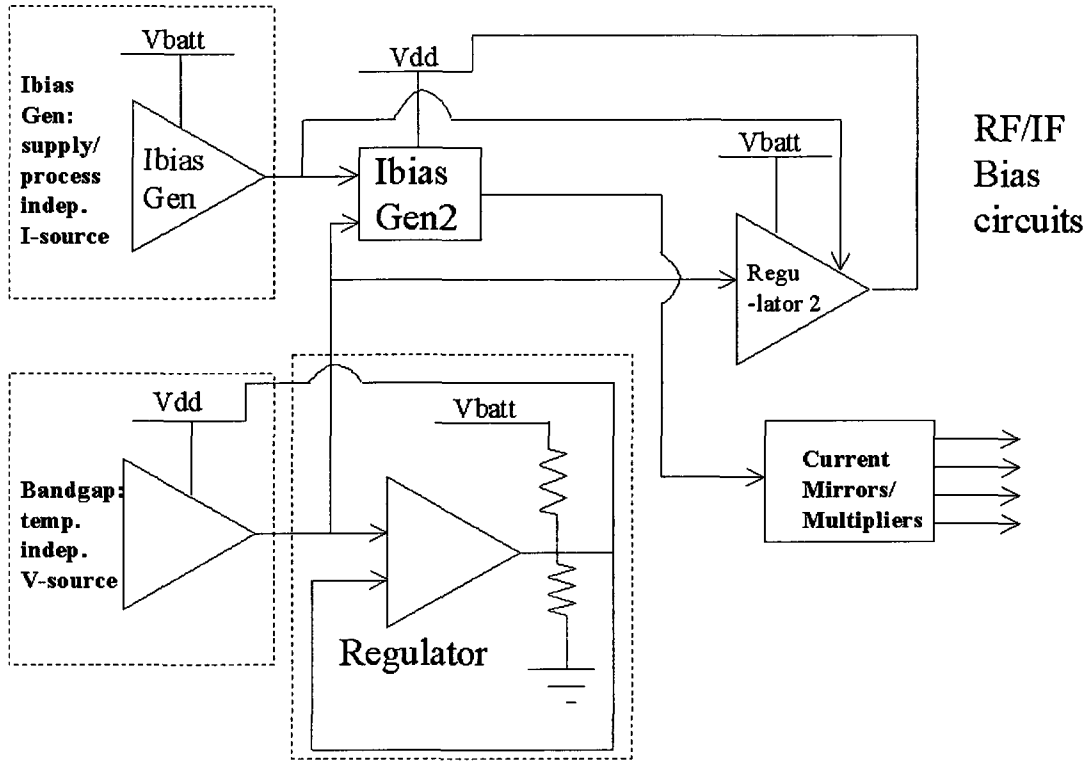

Figure 12: Possible process tracking architecture used in industry.

4.3.3 Image Rejection

In many systems, image rejection is done by the transceiver architectures [23]. Active inductors have been published to give sufficient image rejection for high frequencies [6]. However, again, care must be taken in the biasing of the active inductor and how this biasing needs to track the process variation in order to provide maximum yield in production. Although image rejection should be performed as early in the receiver-chain as possible, it is important to note that active inductors are a source of large noise, and thus they should be used towards the end of the LNA cascade, but before the mixer. Therefore self-biased topologies used in [6] are usually not desirable for industry.

4.4 Including Parasitics

The peripheral parasitics must be included in the schematic before simulating an LNA in order to optimize the width of the transistor, the number of fingers and the exact gate bias voltage. These peripherals include ESD protection diodes (usually 2 back-to-back reverse biased diodes connected in series from ground to Vdd, with the signal running between the 2 diodes), input pad capacitances, equivalent bondwire models (inductance + resistance) for both source bias and gate input match, and PCB trace on the package plus any through-via equivalent capacitance and inductance. The antenna equivalent circuit should also be included in order to ensure a more accurate source impedance. In the case of fully differential LNAs, the bondwire mutual inductance should also be included. Figure 13 shows the main parasitics that need to be included before LNA transistor parameter determination. These parasitics cause a phase and voltage gain change in the signal input from the source voltage, and thus present a very small real impedance, and a more capacitive impedance at the gate of the LNA transistor, than the 50 ohms that is normally assumed.

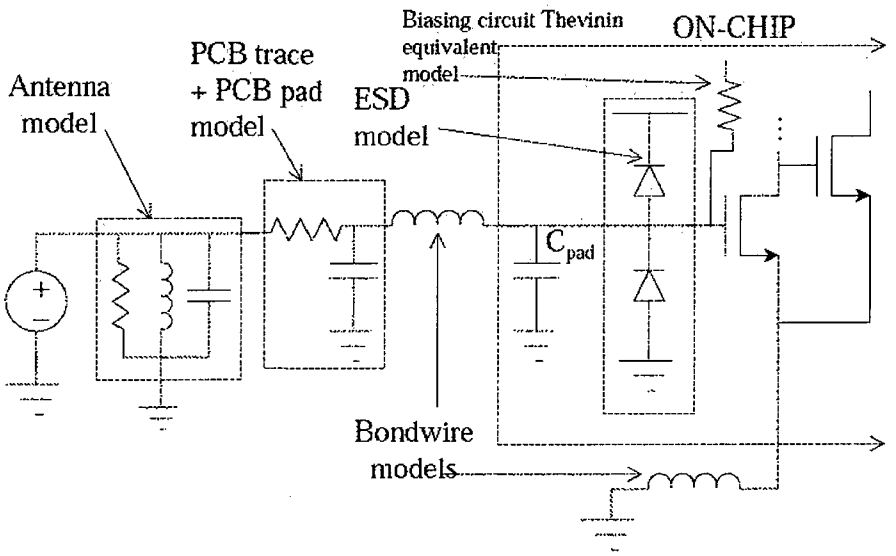

Figure 13: Peripheral transistor parasitics.

4.5 Bias and Transistor Parameter Determination

The current density in CMOS that gives a low NF depends on the channel inversion controlled by the gate bias voltage, and the length and width of the transistor, as well as the number of fingers. Most designs in industry use PMOS current sources to determine the amount of current flowing through each transistor and then vary the gate bias voltage, transistor width and number of fingers to obtain the correct current density in order to obtain minimum NFmin before the circuit is matched. The reason for the PMOS current sources is that the gain of the LNA has to track with the process variation of the full SoC in order to provide maximum yield. However, in order to determine the correct current density that gives minimum NFmin, the topology has to be first determined. Once the topology has been determined, then quick parametric simulations can be performed in software like CADENCE or ADS to obtain the correct transistor size.

As an example, the topology of a simple common source amplifier is considered. The gate of the transistor is biased via a large resistor (e.g. 40K ohms) connected in series with an ideal voltage to ground. This resistor should emulate the R_{ds} of a current source biasing the transistor as shown in [41]. The drain is biased at a supply voltage Vdd/2 via a hypothetical ideal inductor of value 1H, which acts as RF choke, providing the transistor drain voltage to be set at mid-rail (Vdd/2) in order to obtain maximum linearity. The input port impedance is set to the value of the equivalent parallel resistor of the antenna (which could be 50 ohms, but is not in most cases). The equivalent parallel inductance and capacitance of the antenna are then put in parallel with the input port. The output port impedance is set to a large value (e.g. 50Mohms), and placed in parallel with a small capacitor, (from 5fF to 20fF) to emulate the input impedance of the next low-noise transistor. After all the parasitics are included as mentioned above, the circuit should look like the one shown on the left of Figure 14. Now the following steps should be followed to obtain the LNA transistor parameters:

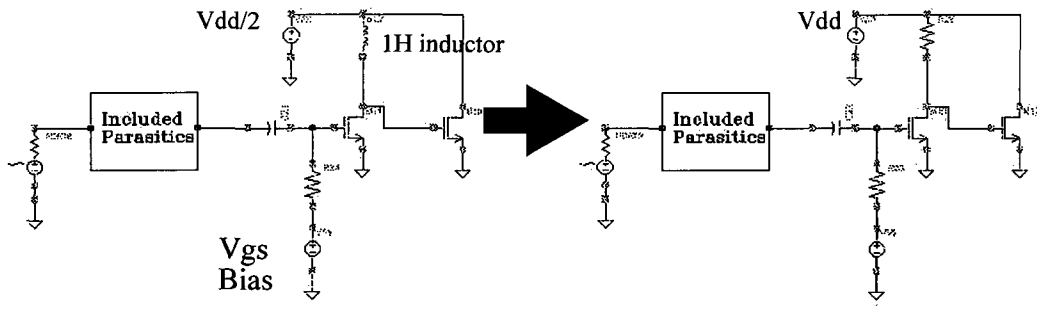

Figure 14: Transformation of LNA circuit from ideal to actual.

4.5.1 Step 1: First parametric simulation

The width of the transistor, the number of fingers (N, in increments of 2 for symmetric layout), and the bias voltage in the vicinity of the threshold voltage of the transistor, are swept in a parametric S-parameter simulation at the desired frequency of operation. At this point the step size of the total transistor width should be kept to 1μm to enable quick simulations. This step size can later be reduced to 0.01μm for a more accurate width. The width per finger would then be the width divided by N. A series of plots showing NF should be plotted. For the smallest NF, the minimum of these curves is chosen as the starting point of the current and transistor size required for low NF. The gate bias voltage for the minimum NF is recorded. If the system can handle a larger NF for reasons of lower current, and smaller width or smaller number of fingers, then the appropriate parameters are chosen for the application. From this point on, the number of fingers will be fixed, so only V_{gs} and transistor width will be swept in the following parametric simulations.

4.5.2 Step 2: Determine Ibias

DC simulation is run to determine the current, Ibias, with the gate bias voltage and transistor width obtained in Step 1.

4.5.3 Step 3: Calculate R_L

The 1H ideal inductor is now replaced with a resistor of value R_L=Vdd/(2*Ibias). This will slightly increase the NF since the resistor has an output noise voltage contribution that is divided by the the square of the transistor voltage gain, resulting in an additional small input noise voltage.

4.5.4 Step 4: Replace Supply Voltage

The supply voltage is replaced with Vdd, since the resistor will cause a drop of Vdd/2, leaving the drain of the transistor at the voltage Vdd/2 (at which it was first biased). The circuit should now look like the one showed on the right of Figure 14.

4.5.5 Step 5: Re-adjust for Early-Voltage Effects

The first step 1 is re-simulated to find the transistor width which gives the new minimum NF transistor width, and replace this as the new width. Also, the gate bias voltage is re-adjusted for the minimum NF curve.

4.5.6 Step 6: Re-determine Ibias

The DC the simulation is re-run to find if the transistor is in saturation or the triode region. Usually, at this point the transistor is in saturation. However, the DC current consumption will be reduced due to the fact that the magnitude of Early voltage is smaller in recent sub-micron devices, so the I_{ds} verses V_{ds} curve is not flat in the saturation region of operation (and thus gives a smaller R_{ds}). If the transistor is found to be in the triode region of operation, then proceed to Step 7, otherwise proceed to Step 8.

4.5.7 Step 7: Iteration

If the transistor is in triode region of operation, then a new resistor is found that will give mid-rail operation: RL=(Vdd/(2*Ibias)), resulting in a new current, Ibias, through the transistor. Steps 5 to 7 are repeated until a solution is converged on. First the voltage bias will converge to a certain value, and then a resistor value and transistor width that gives low NF.

4.5.8 Step 8: LNA transistor parameter determination is complete

The transistor design is now complete. If the bondwire is being used for input matching, then a capacitor is placed between the gate and ground, and its value is swept till the S_{11} becomes a minimum. At this point, the circuit input is matched to the source. Now an S-parameter frequency sweep can be run to ensure the design is stable, and yields a NF that is close to NFmin at the desired frequency.

4.6 Cascading Stages

Since power saving is necessary in industry, LNAs are rarely designed as single stages. Multiple stage LNAs give large gain and low NF, but decreased linearity. This increases the output SNR and thus reduces the bit jitter when the analog sinusoidal signal is limited (in the case of FM, or FSK), or is converted to a digital signal via an ADC. The amplifier stages immediately after the LNA should also be designed and biased in the low noise configuration in order to keep the system NF to a minimum, again to obtain a minimum bit error rate (BER) upon demodulation. The procedure to realize this is the same as the one given in Section 4.5, except that the input port impedance is now changed to the value of the output resistance, R_L of the first stage, in parallel with the drain-to-source capacitance, C_{ds}, of the first stage transistor. Steps 1 to 7 are now repeated, and step 8 is ignored since it is not feasible to match the input of the second stage to R_L of the first stage.

4.7 Matching Techniques

Although a simultaneous power gain and NF match is desirable, in most cases it is not practical due to current limitations of the transceiver. Thus, the technique mentioned in [25] is often not used, but its variations are used. The use of off-chip matching components such as inductors or baluns, as mentioned in [9], proves expensive in volume-production. Square or octagonal on-chip inductors at high frequencies occupy between 100μm to 200μm large silicon area [49], and are therefore costly for volume-production. Use of on-chip inductors for matching is also process dependant, and is thus not always recommended for input matching. Special thick metal layers are available in recent technologies. If the process allows for the fabrication of thick metal layers, like IBM's 130nm and ST's 65nm CMOS technologies, then input matching using on-chip inductors is feasible. But these technologies are expensive in industry. Some cheaper technologies, like 180nm, do not provide the thick metal layers and are thus not attractive for on-chip inductor designs. In addition to this, on-chip inductors have Q-values of less than 16, which do not give sufficient input filtering to maintain linearity while providing a proper match.

As mentioned earlier, input matching via feedback causes a reduction of gain, thereby requiring more DC power consumption for larger SNR. In addition to this, the input source impedance presented to the LNA is much smaller than 50-ohms, due to the presence of pad and trace capacitances above 200fF. Also, some technologies cannot provide high-gain at these frequencies, requiring multiple stages for sufficient gain in order to use feedback, and this can possibly result in instability over process variation. Thus these feedback-matching techniques are not commonly used in industry.

Stacked inductors give a low-Q response [3]. Using a passive inductive load with feedback in an active-inductor circuit configuration is equivalent to increasing the Q of the passive inductor, resulting in a low noise input match [3].

Output match increases power gain, thus reducing the NF. Since the output of the LNA is connected to another amplifying stage or a Mixer, it is best to ensure the output port impedance is the same as, or similar to, that of the stage that the LNA is driving. Most published papers either use 1/gm=1/50 ohms buffers or inductors for output matching. This is done only so that the output voltage gain can be converted to the power gain, which can in turn be measured by a Network Analyzer. Thus, these output matching techniques are not necessary in a System On Chip (SoC) receiver. In industry, the output is usually taken from the Mixer and then buffered through a test-buffer, in order not to excessively load the LNA output.

Bondwires used as inductors are structure-variant, and may change from package to package, requiring trimming after packaging [2]. However the resonating capacitance can be digitally switched in or out during the foundry testing. This limits the degree of the freedom for the input matching available to the designer. In fact, if the chip package is already chosen, the only components that the designer can change for the input match are the matching capacitors in parallel with the C_{gs} of the common source LNA transistor, and the width and the number of fingers of the transistor. A low NF can also be obtained by having low noise devices in multiple stages to increase gain and SNR. If the technology, packaging, and chip area costs do not allow for bondwire parasitics, or on-chip inductors, then the input is left unmatched, but the transistors are still designed to provide a low NF. Ball grid array packages do not have bondwires, but have a 50 ohm trace impedance from the bump on the IC to the solder ball. Thus a 50-ohm source can be assumed before the pad with ESD parasitics in this case.

4.8 LNA Simulation Results.

A 3-stage cascaded LNA was designed in Cadence using the method described in section 4.5. The schematic is shown in Fig. 15 and the layout is shown in Fig. 16. The post layout S-parameter simulation result shows a gain of 14dB, a NF of 6.23dB and an NFmin of 3.3dB at 6.5 GHz with the output properly matched and the input unmatched as shown in Fig. 17. Figure 18 shows that the LNA's 1dB-compression is -26dBm, which is low, as expected. Of course, if the AI matching was removed and the LNA was connected to a mixer to down-convert the RF signal, the linearity of the LNA would be higher, because the linearity limitation presented by the feedback topology of the AI would no longer affect the output signal, since the LNA would consist of simple inverter stages. When comparing the simulation results shown in Fig. 17 with the S-parameter simulation result shown in chapter 5, the NF of the LNA is shown to be within the simulated range, since the NF of the wireless LNA cannot be measured directly, unless a full system is designed and the BER is measured from the back-plane.

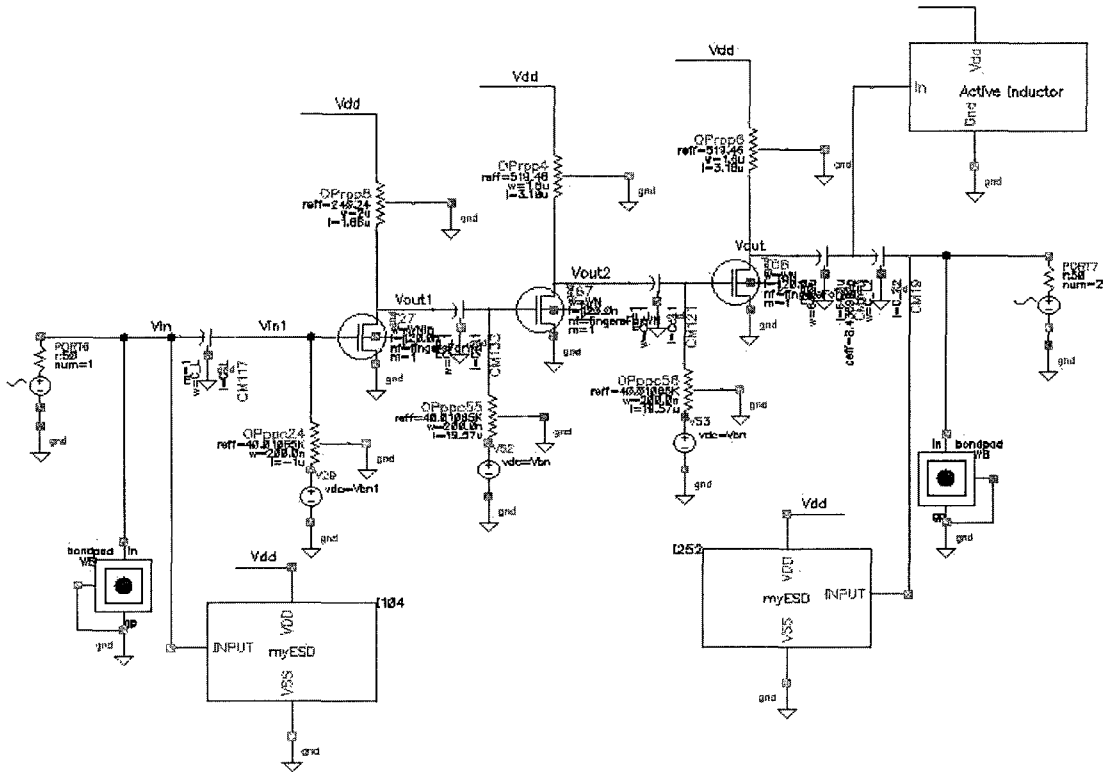

Figure 15: Schematic of the 3-stage unmatched LNA.

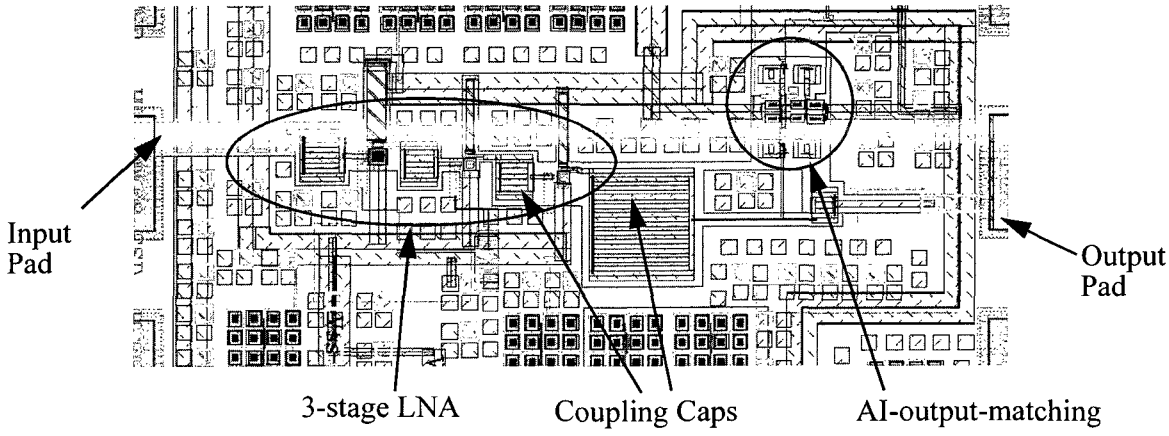

Figure 16: Layout of the 3-stage unmatched LNA.

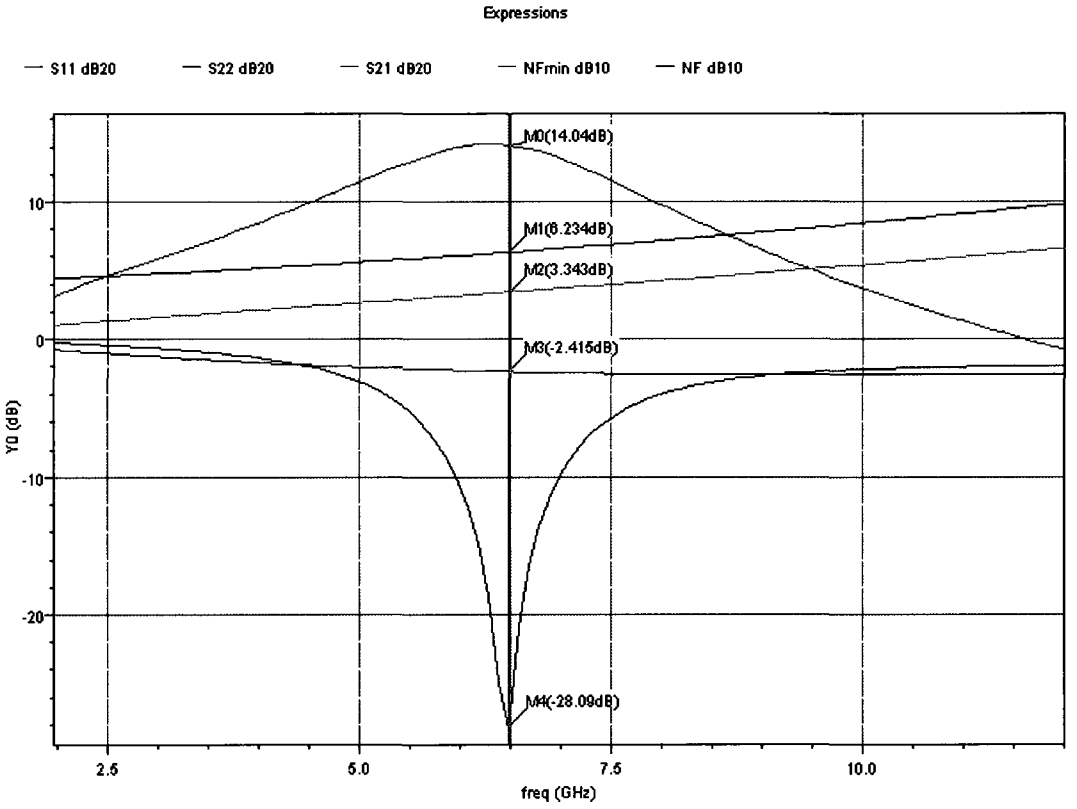

Figure 17: Post layout S-parameter simulation result of the 3-stage unmatched LNA.

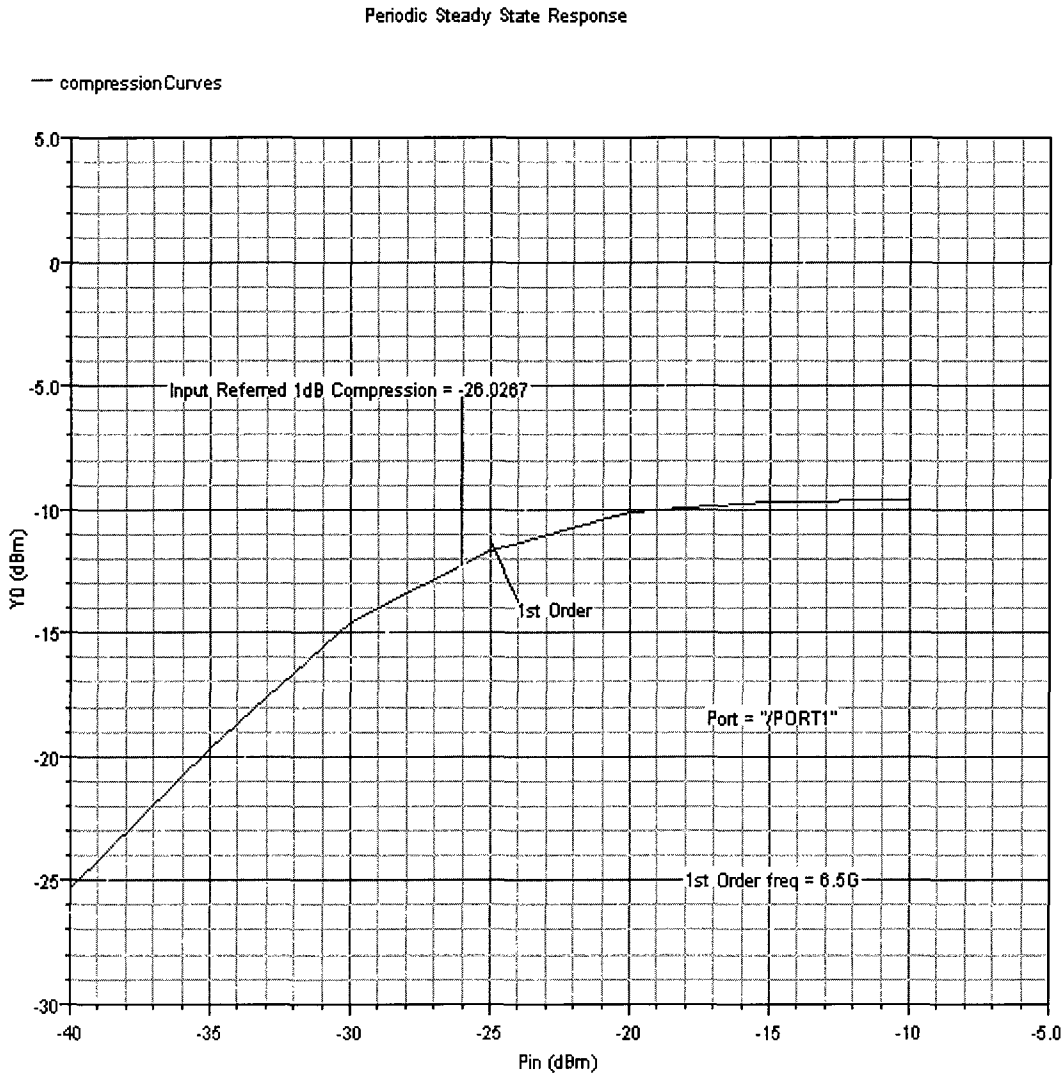

Figure 18: 1-dB compression point post layout simulation result of the 3-stage unmatched LNA.

4.9 Summary

This chapter gives the LNA design procedure. It begins by showing how the LNA specifications can be derived from the system specificaitons, and what technology should be used. It then discusses the pros and cons of the common LNA topologies, which topologies give best performance parameters (e.g. gain, bandwidth, noise figure, linearity, chip area and biasing) and

what are the practical trade-offs faced in the industry that affect the various performance parameters. It discusses the various methods used in biasing an LNA, and the advantages of using these methods. It also discusses what methods are used for image rejection and which ones are insufficient. It describes what parasitics should be included before the transistor parameters (i.e. length, width and bias voltage) are determined, and as an example, what exact simulation steps should be taken in order to determine these parameters. It highlights which method to follow for designing the amplifier stages following the LNA, and the advantages of having multiple stages verses a single stage LNA. Finally, it presents the practical LNA matching techniques available and used in industry, and their limitations. The next chapter shows how this LNA design procedure is used to design a duplexer-less LNA/PA pair that uses a bondwire antenna.

5.0 Bondwire Antenna with Duplexer-less LNA/PA Design

5.1 Bondwire Antenna Design

In order to overcome the problem of lossy on-chip dielectric and low-Q on-chip antennas (OCAs) resulting from the planar dimensions of the System on Chip (SoC) in silicon, the idea of using a bondwire as an antenna was considered. Bondwires have a high-Q due to the low resistivity of gold, and the fact that the bondwire is connected above the substrate gives an advantage to the design compared to the OCA in [32] which has a relatively lower Q. A bondwire antenna has to be placed physically orthogonal to the other bondwires in the package in order to ensure that there is minimal cross-talk between the bondwires. Also, the circuits under the antenna must be shielded by a grounded metal shield so that the radiation does not interfere with the circuit functions on the chip. Reference [50] gives series solution to half-loop antenna, while [51] describes a loop antenna tilted an an angle to the cartesian axes. In this thesis, approximations are used to obtain hand-derived equations for the theoretical near and far-field patterns in spherical coordinates. The approximations will be mentioned during the derivations.

In order to simplify the calculation of the radiation pattern for the bondwire antenna, the profile of the bondwire is assumed to be an infinitesimal half circular loop. Since the circuit below it will be shielded but not a full sheet of metal, it cannot be approximated to be a ground-plane as in [52], and thus the radiation pattern will be different from the approximations of a circular loop antenna resulting from image theory. Therefore its radiation pattern must be calculated from first principles. The first variable to calculate in order to obtain the antenna radiation pattern is the Magnetic Vector Potential **A**. The primes (annotated with ') will be used for coordinate values of the current element and the non-primes for the coordinate values of the observer. In general **A** is calculated from (14), since the current element $\mathbf{J}dV$ reduces to $\mathrm{I}ad\phi'$ as shown in Figure. 19 in the

spherical coordinate system, assuming constant current in the bondwire at any particular point in time.

$$\vec{A} = \frac{\mu}{4\pi}\iiint_V \vec{J}\frac{e^{-jkR}}{R}dV = \frac{\mu}{4\pi}\int_0^{\pi} Ia\hat{\phi}'\frac{e^{-jkR}}{R}d\phi' \tag{14}$$

In (14) R is magnitude of the vector between the current element and the observer, i.e. $R = |r - r'|$, where |r'| = a.

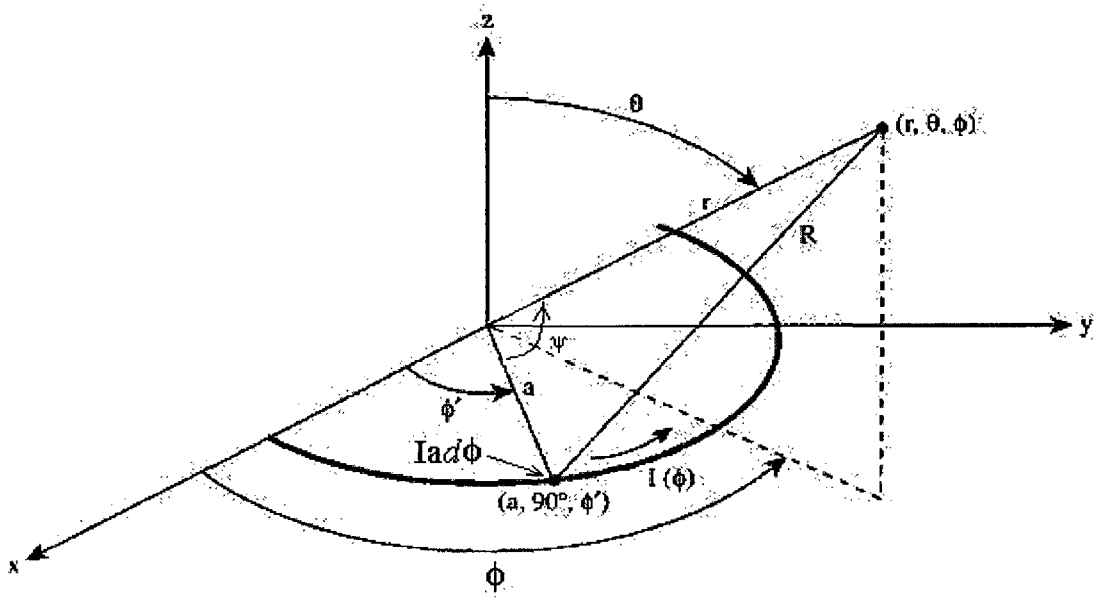

Figure 19: Bondwire antenna current element in spherical coordinates.

Also, there is a angle, ψ, between vector coordinates of the current element and the observer that can be expressed in terms of $(\phi - \phi')$ that causes a phase difference in **A**, which affects the radiation pattern and thus needs to be taken into account in determining the value of R, as shown in Fig 19. Thus, for large values of R for which |r| and |r'| are almost the same, R can be approximated as shown in (15) where $\cos\psi = \sin\theta\cos(\phi - \phi')$.

$$R = |r - r'| = r - r'\cos\psi = r - a\sin\theta\cos(\phi - \phi') \tag{15}$$

Equation (15) can be used to split the exponential in (14) in the integral into 2 parts: one that is constant and contains "r", and another part that varies with the current element and contains " r' ", as shown in (16). Integration of functions like (16) result in Bessel functions and the integrals get too complicated to analyze, so (16) is can be approximated as (17) since the value "ka" is small (about 0.06) for the operational frequency range. The R in the denominator of the integral can be approximated by (18) as described in [53]. Furthermore, the coordinate unit angle ϕ' of the current element has to be expressed in terms of the unit angle ϕ of the observer, as expressed in (19), in order to carry out the integral of **A**.

$$e^{-jkR} = e^{-jk(r - a\cos\psi)} = e^{-jkr}\{\cos[ka\sin\theta\cos(\phi - \phi')] + j\sin[ka\sin\theta\cos(\phi - \phi')]\} \tag{16}$$

$$e^{-jkR} = e^{-jkr}(1 + j\sin[ka\sin\theta\cos(\phi - \phi')]) \tag{17}$$

$$\frac{1}{R} = \frac{1}{r}\left(1 + \frac{a}{r}\sin\theta\cos(\phi - \phi')\right) \tag{18}$$

$$\hat{\phi}' = \hat{\phi}\cos(\phi - \phi') + [\hat{\theta}\cos\theta + \hat{r}\sin\theta]\sin(\phi - \phi') \tag{19}$$

The resulting integral used to calculate **A** is obtained by substituting (17-19) into (14) which becomes too large to fit on this page. It should be mentioned that the term containing "ka^2" was neglected in the integral since $ka^2 << 1$. The calculated **A** is shown in (20). The E- and H-field expression are obtained from **A** using the well known Maxwell's equations, and are given in (21) and (22) respectively.

$$\vec{A} = \frac{\mu_o Iae^{-jkr}}{4\pi r}\left[\hat{\phi}(2\sin\phi) + \left(\frac{\pi}{2}\right)\left(\frac{a}{r} + jka\right)\sin\theta - (\hat{\theta}\cos\theta + \hat{r}\sin\theta)2\cos\phi\right] \tag{20}$$

$$\vec{H} = \frac{1}{\mu}\nabla\times\vec{A} = \frac{Iae^{-jkr}}{4\pi r}\left[\left\{\hat{r}\frac{r}{a}\pi\cos\theta\left(jk + \frac{1}{r}\right) + \hat{\theta}\left[\left(jk + \frac{1}{r}\right)\left(2\sin\phi + \frac{\pi a\sin\theta}{2r}\right) + k^2 a\frac{\pi\sin\theta}{2}\right] + \hat{\phi}2\cos\phi\cos\theta\right\}\right] \tag{21}$$

$$\vec{E} = -j\omega\vec{A} - \frac{j}{\omega\mu\varepsilon}\nabla(\nabla\bullet A) = -\frac{Iae^{-jkr}}{4\pi r}[\hat{\phi}E_\phi + \hat{\theta}E_\theta + \hat{r}E_r] \tag{22}$$

where

$$\vec{E}_\phi = j\omega\left\{2\sin\phi + \frac{\pi}{2}a\left(\frac{1}{r} + jk\right)\sin\theta\right\} - \frac{j}{\omega\mu\varepsilon}\frac{2}{r}\left(\frac{1}{r} + jk\right)\sin\phi$$

$$\vec{E}_\theta = 2\cos\theta\cos\phi\left[j\omega + \frac{j}{\omega\mu\varepsilon}\frac{2}{r}\left(\frac{1}{r} + jk\right)\right]$$

$$\vec{E}_r = 2\sin\theta\cos\phi\left[j\omega + \frac{j}{\omega\mu\varepsilon}\frac{4}{r}\left(\frac{1}{r} + jk - \frac{k^2 r}{2}\right)\right]$$

Now the radiated power is given by (23), yielding a radiation resistance given by (24).

$$P_{rad} = \int_0^{\pi}\int_0^{2\pi}\left\{\frac{\vec{E}\times\vec{H}^*}{2}\bullet\hat{r}\right\}r^2\sin\theta\, d\theta\, d\phi = \frac{8\pi}{3}\frac{\mu}{2c}\left(\frac{Ia\omega}{4\pi}\right)^2\left[2 + \left(\frac{k\pi a}{2}\right)^2\right] \tag{23}$$

$$R_{rad} = \frac{8\pi}{3}\frac{\mu}{2c}\left(\frac{a\omega}{4\pi}\right)^2\left[2 + \left(\frac{k\pi a}{2}\right)^2\right] \tag{24}$$

In order to obtain the gain of the antenna, its radiation intensity U must be calculated as given by (25), which results in U_{max} as given by (26), and the directivity D given by (27), assuming the

maximum radiation intensity U_{max} occurs at $\theta = \phi = \pi/2$. Then the gain G of the antenna is given by $e_r D$ from (27), where $e_r = R_{rad}/(R_{rad}+R_L)$ is the radiation efficiency. The results from these equations allow the use of the Friis equation, from which a range of signal sensitivity can be derived given the radiated power, without the need for simulation results.

$$U = \frac{r^2}{2} \times Real(\vec{E} \times \vec{H}) = \frac{\mu}{c}\left(\frac{Ia\omega}{4\pi}\right)^2 [\hat{r}U_r + \hat{\theta}U_\theta + \hat{\phi}U_\phi] \tag{25}$$

where

$$U_r = -2(\cos\theta\cos\phi)^2 + 2(\sin\phi)^2 + \frac{3\pi a}{2r}\sin\theta\sin\phi + \left(\frac{k\pi a\sin\theta}{2\sqrt{2}}\right)^2$$

$$U_\theta = -\frac{\pi a}{r}\cos\theta\sin\phi \text{ and } U_\phi = \frac{\pi a}{r}\cos\phi .$$

$$U_{max} = \frac{\mu}{2c}\left(\frac{a\omega}{4\pi}\right)^2\left\{2 + \frac{3\pi a}{2r} + \left(\frac{k\pi a}{2\sqrt{2}}\right)^2\right\} \tag{26}$$

Assuming the TX/RX antennas are in the far-field region from each other with kr>>1, or equivalently $r>>\lambda/2\pi$, and taking into account that the last term is small, the second and third terms can be ignored in U_{max}.

$$D = \frac{4\pi U_{max}}{P_{rad}} = \frac{3}{2} \tag{27}$$

This shows that the directivity of the bondwire (infinitesimal half-loop) antenna is almost the same as the infinitesimal full-circular-loop. Figure 20 shows the normalized radiation intensity U_r of the bondwire antenna where the last two terms in U_r approach zero in the far-field region. This plot was obtained from Mathematica using the first 2 terms of U_r.

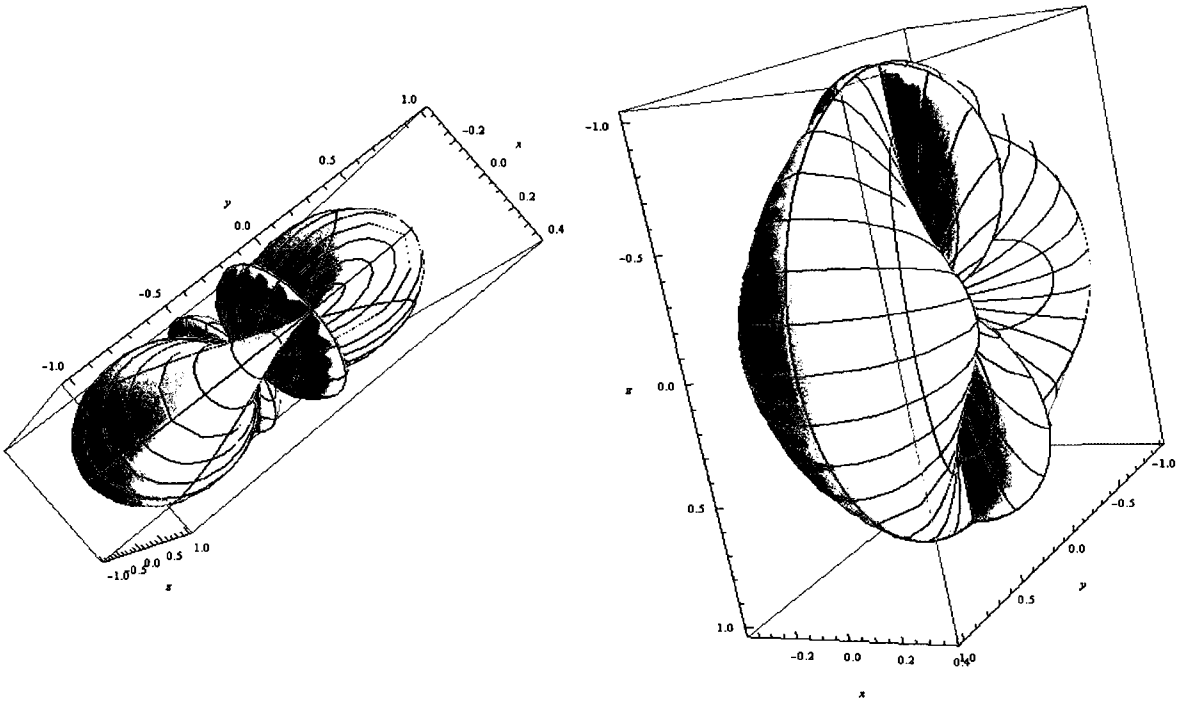

Figure 20: Plot of bondwire antenna radiation intensity.

In order to prove that the above calculations are correct, the bondwire-antenna was drawn as a semi-circle of 1-mil thick gold wire with the diameter of 1mm in HFSS and simulated with a lumped port between its 2 ends and simulated in HFSS. The HFSS bondwire drawing in Fig. 21 shows the bondwire in the X-Y-plane, and Fig. 22 shows the HFSS Gain plot in θ and ϕ directions, and the plots match the ones obtained from Mathematica in Fig. 20.

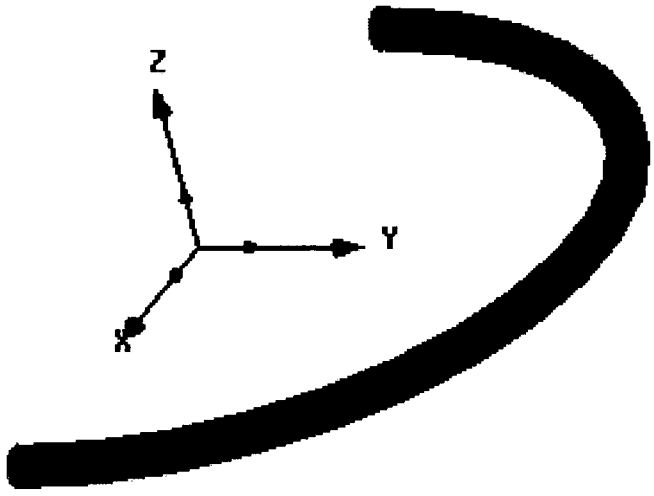

Figure 21: Drawing of half-circular bondwire in HFSS.

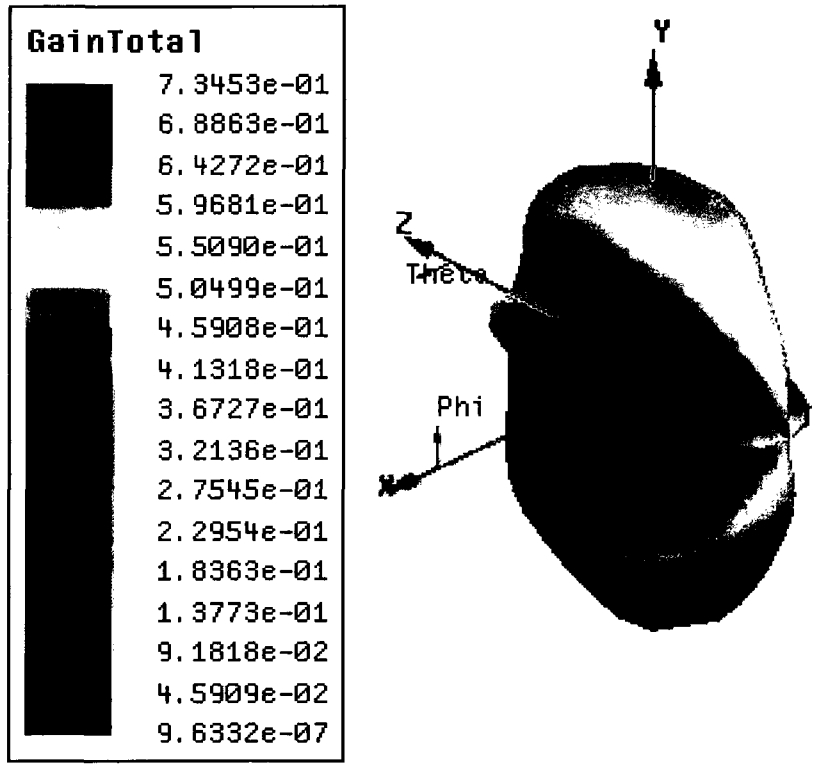

Figure 22: Radiation Intensity pattern obtain from HFSS simulation.

5.2 Determining LNA and PA Topology

5.2.1 Gain, Bandwidth, Linear, NF and Power Consumption

Considerations mentioned in section 4.3, as discussed in [19], were taken into account in designing the LNA/PA pair. Although the circuit in [19] was designed for inductor-less LNA, the same issues apply for the PA since it is important not to transmit a noisy signal. Three cascading stages were used for the LNA and PA to increase gain and isolation in both TX and RX modes.

5.2.2 Combining the LNA and PA

The unique duplexer-less design avoids active devices in the signal path to the LNA and from the PA, and thus provides a lossless signal path from the antenna to the LNA and from the PA to the antenna. The LNA/PA are both common source to be usable for low voltage applications. The bondwire antenna forms the load for the LC-tank output of the PA and forms part of the matching network for the LNA, as shown in Fig. 23, which shows the combination of the LNA/PA topology. The cascading stages provide isolation between TX and RX. This design is different compared to [44] where the inductors (bondwires) were used as loads and then matched to the antenna. The approach of this work saves extra matching components required for the antenna. However, the mismatch between the PA output and the bondwire equivalent parallel resistance greatly limits and lowers the output power. The LNA/PA were designed single-endedly to simplify testing since the measurement instruments available are also single-ended, and also because the AI that was used for matching was single-ended. This topology is only useful for time domain duplexing (TDD) because only the TX or RX can be on at one time. In frequency domain duplexing (FDD), the TX and RX have separate antennas because the TX and RX are turned on at the same time. TDD can emulate the full-duplexing functionality by fast switching between the TX and RX, allowing this circuit to be duplexer-less.

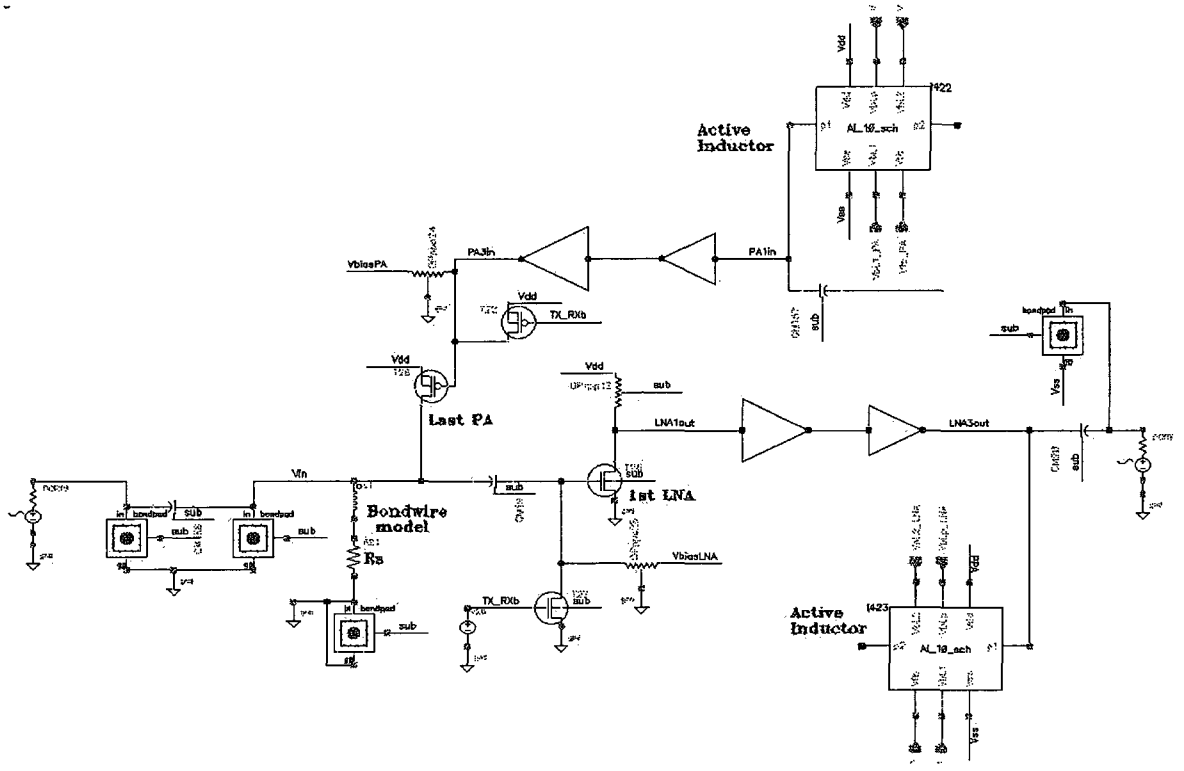

Figure 23: Simplified schematic of the LNA/PA/Bondwire-Antenna Interface with the bondpad loading, not showing all the biasing.

5.3 LNA and PA Transistor Bias and Parameter Determination

The method used in section 4.5, as described in [19], was used to determine the transistor parameters of the LNA and PA as well as the cascading stages following the LNA and preceding the PA. The PA transistor parameters were also designed in the same way as those of the LNA to minimize the noise contribution of the PA. The PA design was chosen as simple class A because the purpose of this design was not to optimize the PA or to present a new PA design, but to demonstrate and test the functionality of the bondwire antenna when fed with a certain current available from the PA.

5.4 LNA/PA Matching, Layout, and Simulation Results

In this thesis, the antenna is inductive and the input and output of the LNA and PA are capacitive respectively, thus enabling the bondwire antenna to present a conjugate match. Reference [54] gives derivations of the antenna Q and shows how the antenna, together with the gate-source parasitics of the LNA and the drain-source parasitics of the PA, behaves as an RLC circuit at the resonant frequency. This presents a high impedance to the gate of the LNA and to the load of the PA, which is ideal for low power transceivers. Both the input of the PA and the output of the LNA are matched using an active inductor described in [22], since the signal levels at these points are small and do not drastically offset the bias and operating conditions of either the PA or the LNA.

After the circuits were designed, the layout of the LNA/PA combination was done in Cadence as shown in Fig. 24. The full chip layout is shown in Fig. 25. Figure 26 shows the post layout S-parameter simulation result of the LNA with the PA off. The input port resistance of the LNA was set to 153-ohms as it would be seen by the incoming EM wave, which is the total parallel resistance of the bondwire in parallel with the resonating pads and coupling capacitors.

The post-layout S-parameter simulation results of the PA are shown in Fig. 27. It should be noted that even though the PA operates in the large signal mode, the S-parameter S_{21} small-signal gain is a good approximation to the actual large-signal gain, because the output of the PA is almost a pure sinusoid, since the output load is an LC-tank.

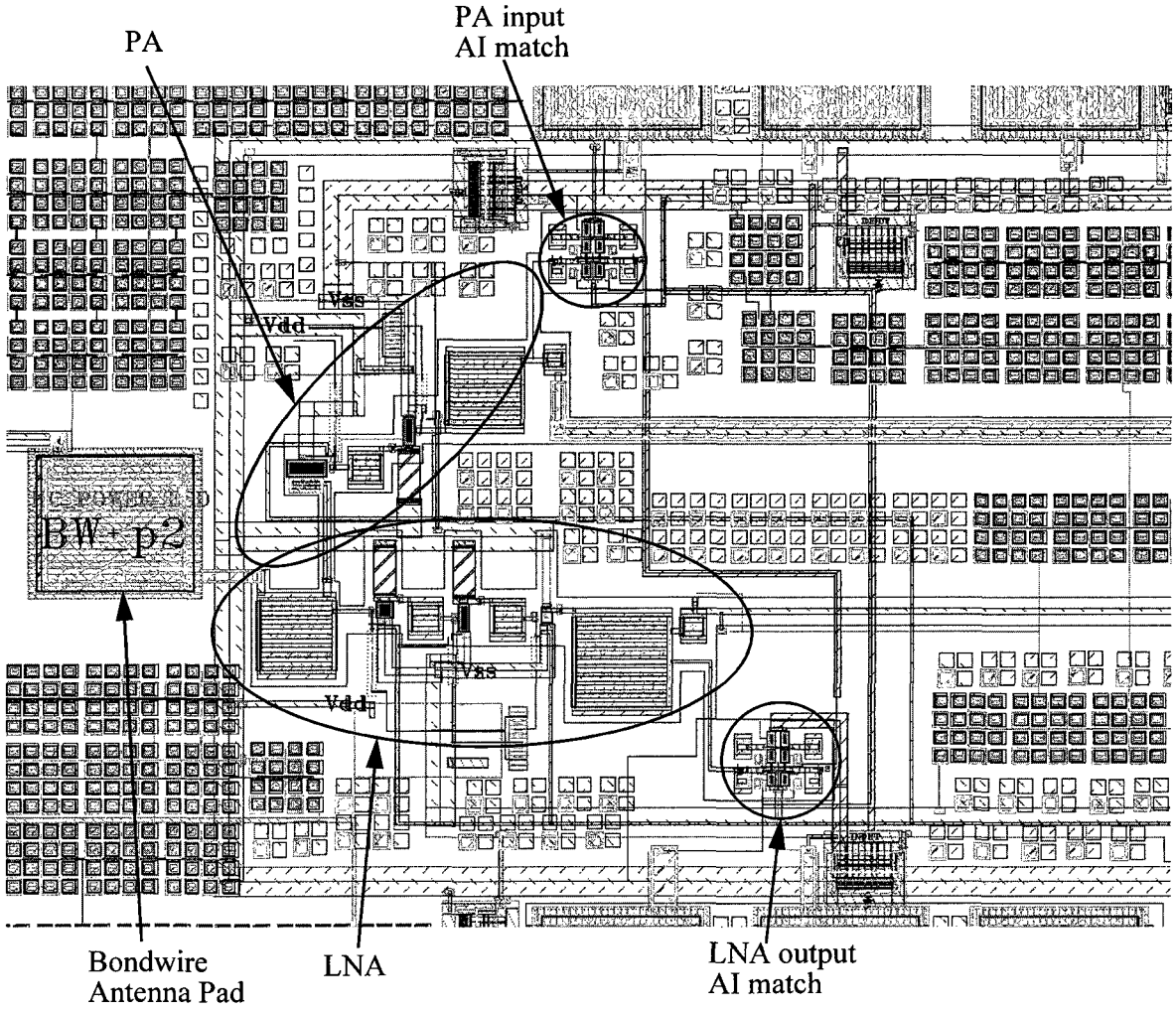

Figure 24: Layout of active inductor and LNA/PA with pad for the bondwire antenna.

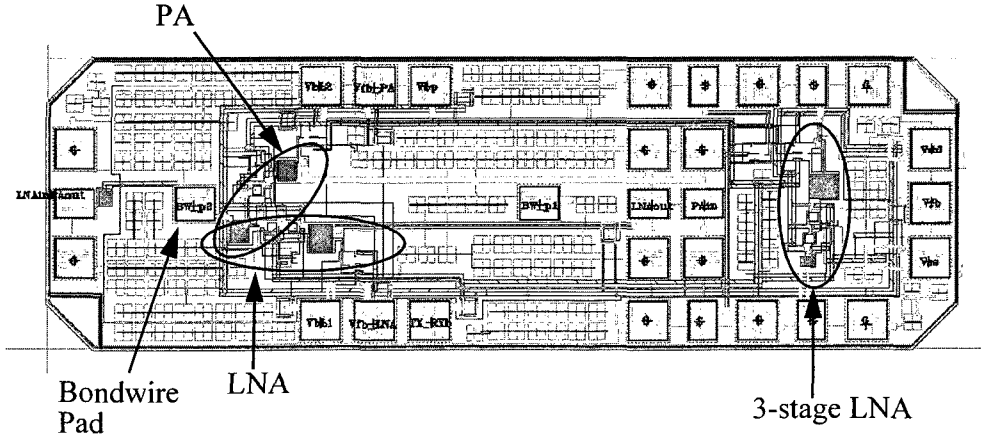

Figure 25: Layout of the full chip as fabricated in IBM's CMOS 0.13μm technology.

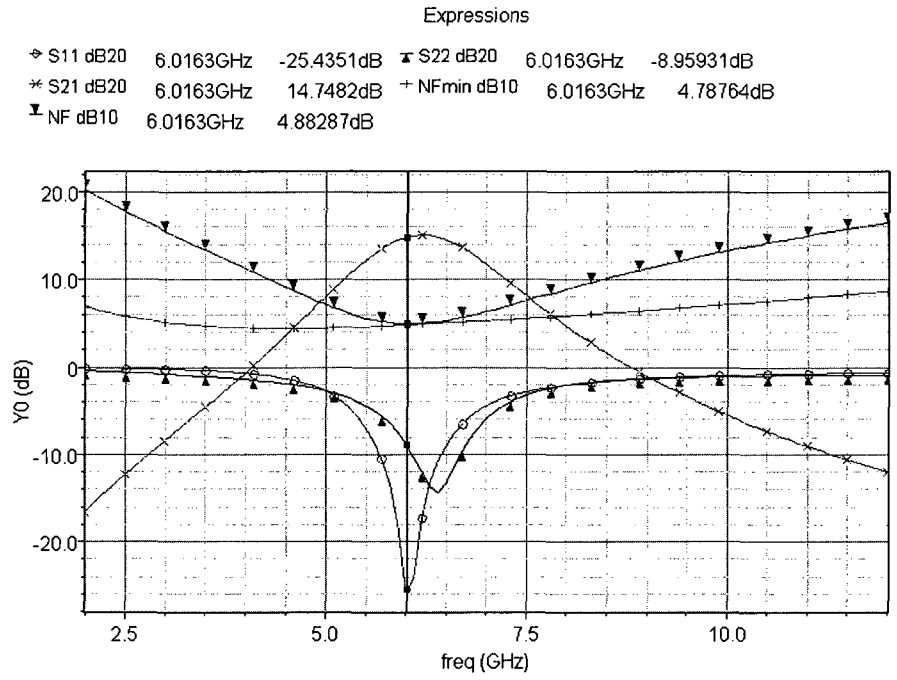

Figure 26: S-parameters of front-end block with the PA off and LNA on.

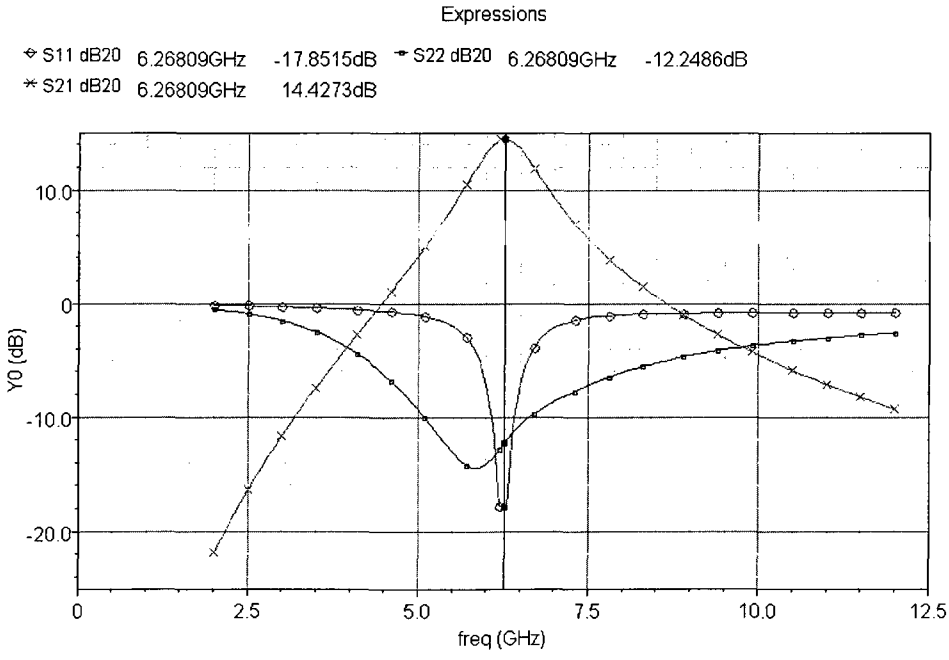

Figure 27: S-parameters of front-end block with the PA on and LNA off.

5.5 Bondwire Antenna Integrated with Chip and PCB

The HFSS simulation result shown in Fig. 22 is insufficient for practical applications, since the bondwire antenna has to be excited by an A.C. voltage source above a real ground plane. In order to obtain a more accurate simulation result, and ensure that the bondwire antenna will work correctly as intended, the layout of the PCB was created in ADS and then imported into HFSS. The layout of the PCB is shown in Fig. 28. A close up of the area of the PCB where the chip was placed and bondwired is shown in Fig. 29.

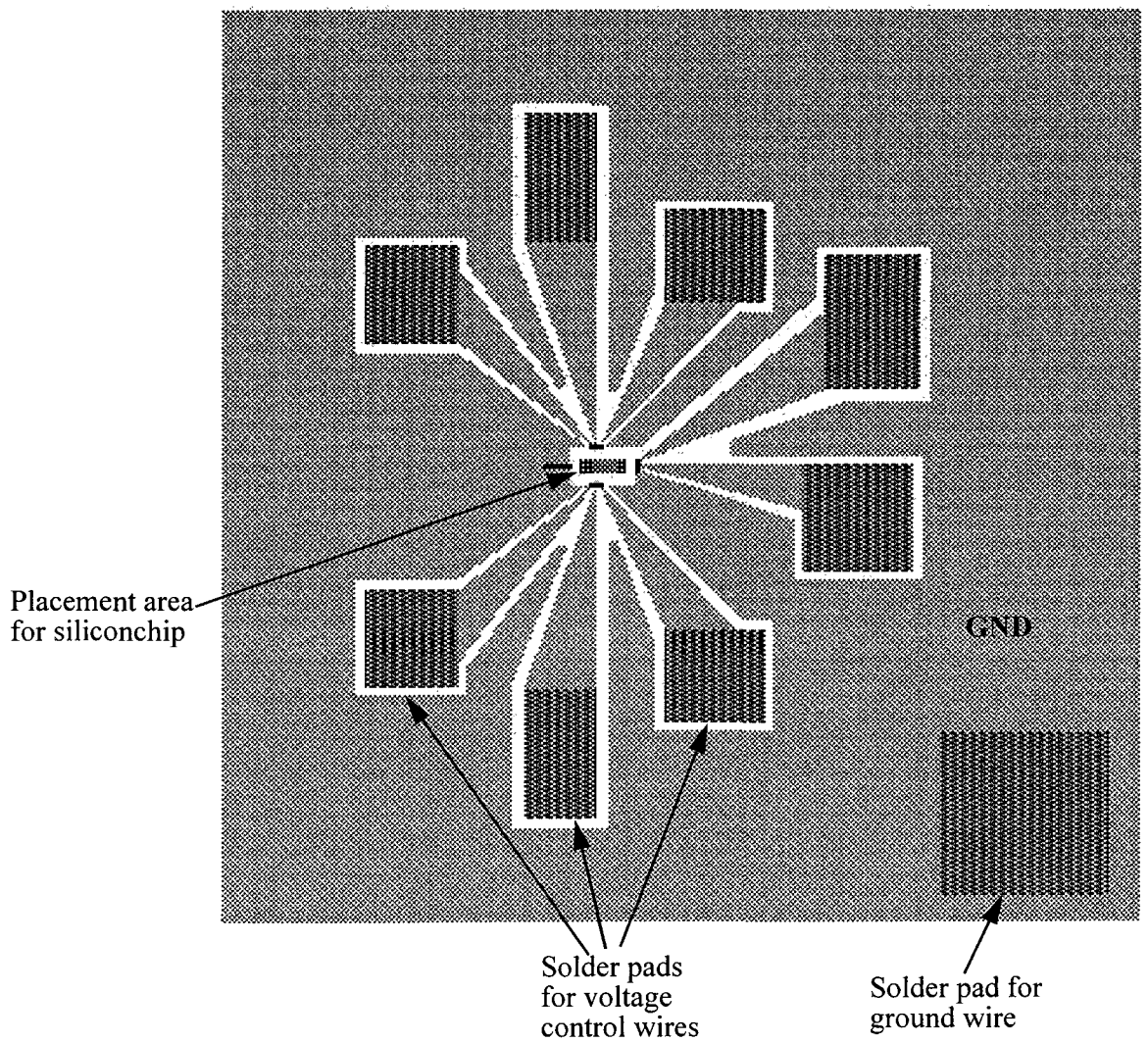

Figure 28: Layout of the PCB as created in ADS sent to SpeedyPCB

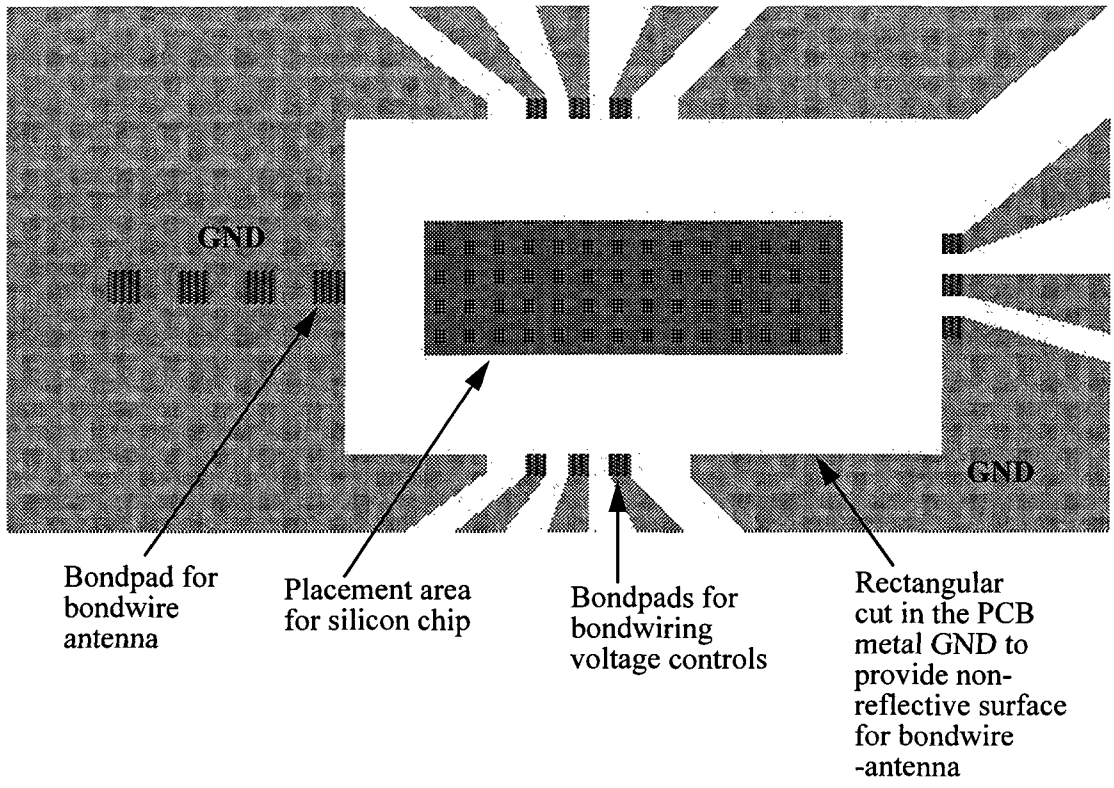

Figure 29: Layout area of the PCB showing the chip placement area.

A 3-dimensional layout of the chip, together with the power-rails, the bondwires that provide the DC voltages, the silicon substrate, the silicon dioxide layers between the metals, an approximation of the metal fill on the top metal, the exact PCB layers and substrate was created in HFSS as shown in Fig. 30. Actually, several versions were created as a step-by-step analysis to find which PCB configuration is appropriate to test the bondwire antenna together with the chip. The PCB chosen was one with 23mil FR4 and 1oz copper (35μm thickness), which gave the best performance with the available funds. The gain obtained from the HFSS simulation result of the full structure is shown in Fig. 31. This result shows that the gain is reduced to 80% its original value of 0.551 to 0.4425. The loss in gain is due to the EM losses in the metal fill, silicon-substrate, PCB substrate, and single-ended usage.

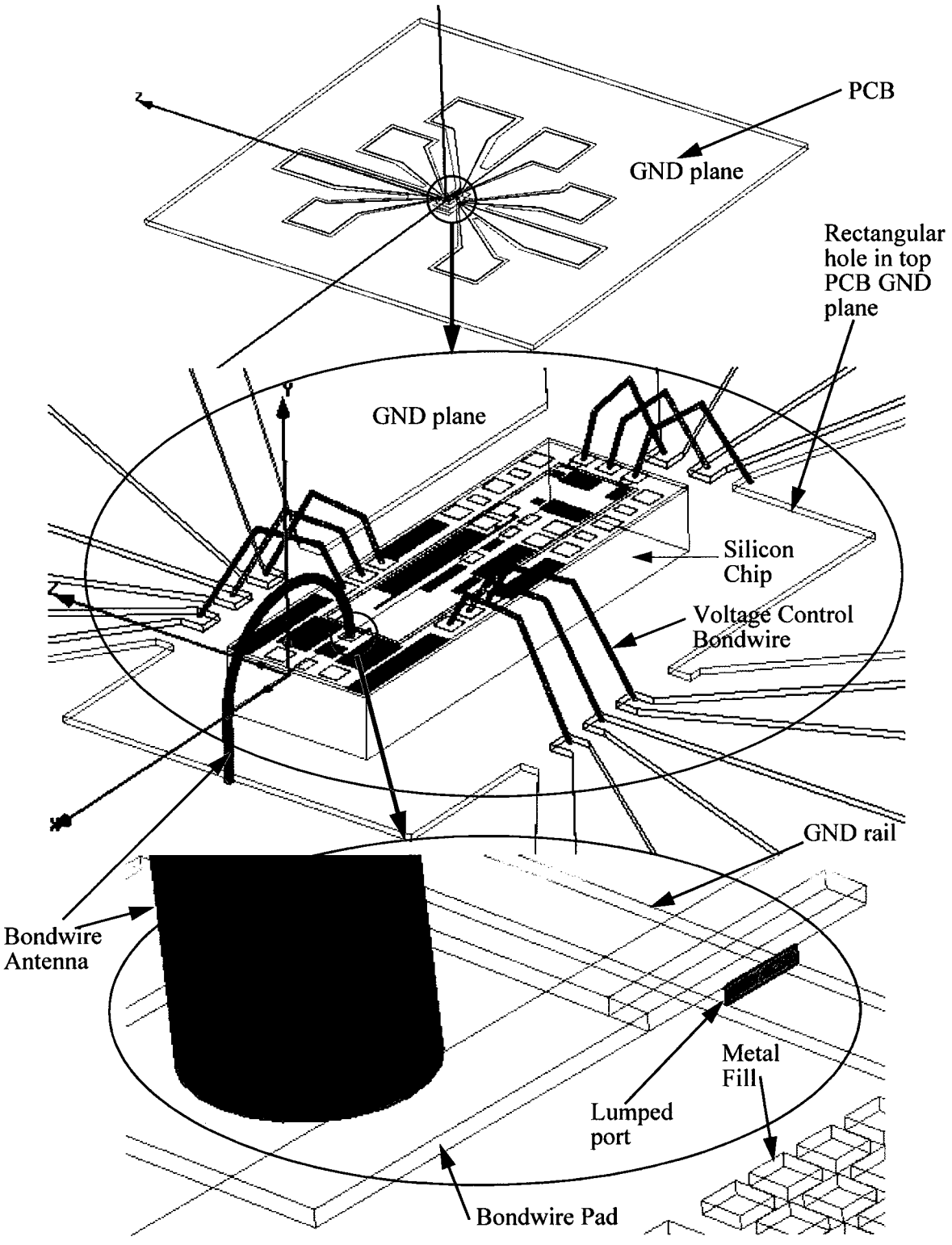

Figure 30: Complete layout of PCB plus silicon-chip in HFSS with bondwire antenna.

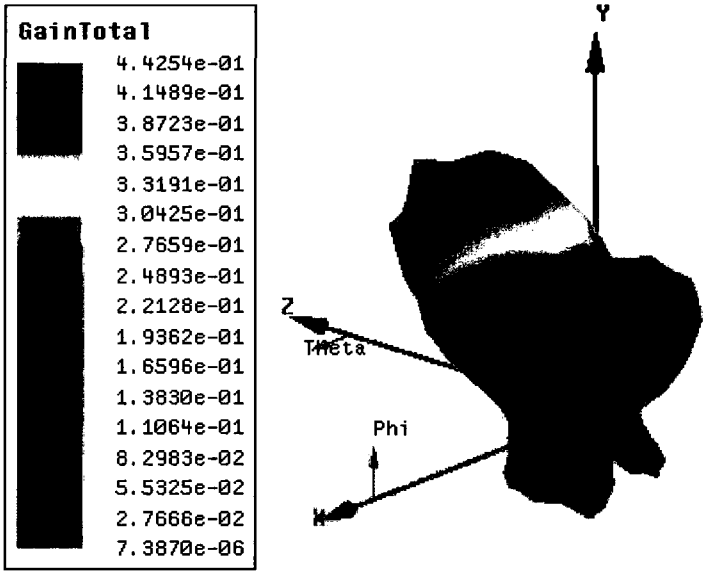

Figure 31: The gain of the bondwire antenna as simulated together with the structure shown in Fig. 30.

This simulation result shown in Fig. 31 also shows the deviation of the radiation pattern towards the x-axis. This is due to the combination of the half-loop radiation pattern and the pattern of the extension of the straight part of the bondwire that connects it to the PCB. Thus the broadside is now at a 45^{o} angle to the x-axis in both the x-y and the x-z plane, however it maintains the basic "flat" shape of the result shown in Fig. 22. Also the radiation in the negative-y direction is greatly reduced by the bottom ground plane of the PCB. The HFSS simulation result shows the radiation efficiency is decreased from 41% in the ideal case to 10.3% with the parasitics, while directivity is increased from 1.5 to 4.3 due to the large ground-plane provided by the PCB as described in [55]. Thus, the gain of 0.4425, which is 80% of the gain of the ideal bondwire antenna without any parasitics, is not due to the bondwire maintaining its radiation efficiency, but due to the increased directivity of the larger ground plane. This means that were the PCB ground plane not present, the gain of the antenna would be much lower.

5.6 Transceiver Link Budget from Analytical Model

ADS was used to simulate the series resistance of a bondwire with a diameter of the formed semi-circle equal to 1.069mm, giving the antenna a circuit impedence of $Z_A = 0.42 + j36.76\Omega$, and thus a loss resistance $R_L = 420m\Omega$. The bondwire R_{rad} has a value of $106.6m\Omega$ at 6.5GHz. This can be compared to a full-circular-loop antenna which has a $R_{rad} = 5m\Omega$, which means R_{rad} of the half-loop is more than 20 times larger. This means that the bondwire antenna can transmit to a further distance, or receive from a further distance than a complete loop antenna, because of the larger R_{rad}, increasing the sensitivity of the receiver. This gives an antenna radiation efficiency of $e_r = R_{rad}/(R_{rad} + R_L) = 20.24\%$. This is 12% greater than the value of the antenna described in [28]. However, this efficiency had been hand-calculated, and the diameter of the bondwire (25.4μm) and the skin-depth had not been taken into account, since the half-loop was assumed to be infinitely thin. Thus, simulation result shown in Fig. 22 gives a radiation efficiency of 41.6%. This efficiency will drop to a quarter of this value once all parasitics are considered. For a gain of 0.551, the directivity is calculated to be 1.32 in the broadside direction, which is close to the analytically derived approximation of 1.5. In order to achieve a larger R_{rad} and e_r, the thickness of the bondwire could be increased. Also, the Q of the antenna is 36.76/0.42 = 87.52, and this has a profoundly positive effect on the communication range of a transceiver which would use this antenna.

Since the antenna is not embedded in any dielectric, its dielectric efficiency is almost 100%. The hand-calculated gain G is therefore $e_rD = 1.5*0.2024 = 0.3036$, which is equal to -5.177dBi. This is 17dB greater than the gain reported in [37]. Now consider the PA output, V_{out}, swinging from Vdd(1.2V) to Vss(0V). Fig. 32 shows the small-signal circuit diagram of the PA output and its integration with the bondwire antenna. The R_{ds} of the PA obtained from the Cadence simulation was 437 ohms. This is in parallel with the equivalent series resistance of the bondwire antenna

given by $R_S = R_L + R_{rad}$. Due to the large Q of the bondwire, this R_S translates to an R_p=2566.1 ohms according to (28). Since the current through R_p, $I_{Rp} = 1.2V/R_p$, and the fraction of R_p that is R_{rad} is $e_r = 0.2024$, the power radiated is given by (29).

$$R_p = R_s + \frac{\omega^2 L_p^2}{R_s} \tag{28}$$

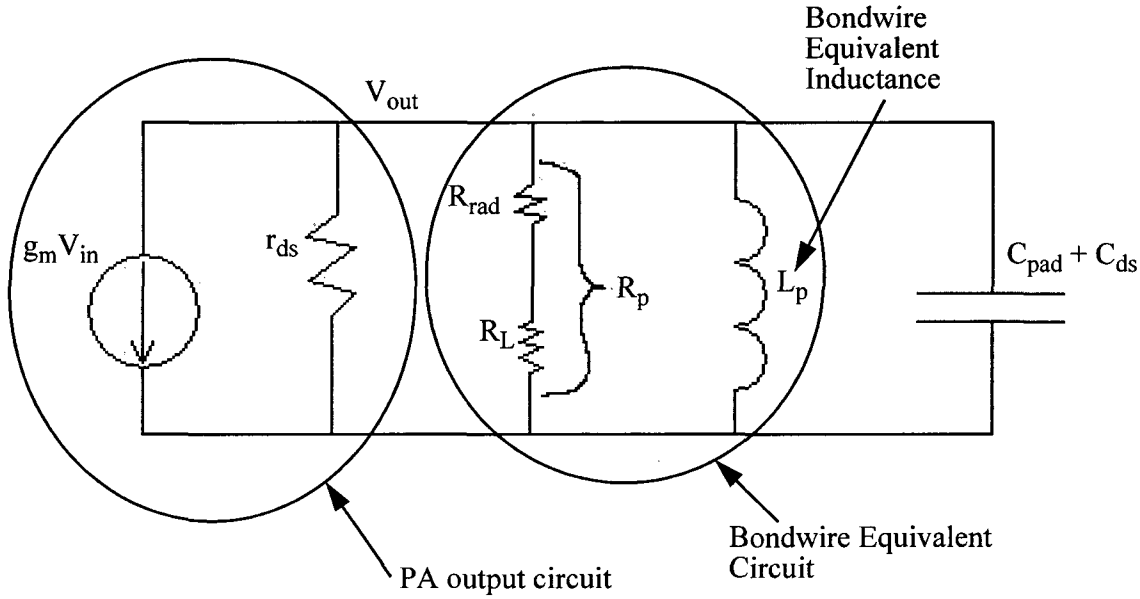

Figure 32: Small signal diagram of the PA output together with the equivalent circuit of the bondwire antenna.

$$P_{rad} = \left(\frac{V_{out}}{R_p}\right)^2 R_p \times 0.2024 = 0.114mW \equiv -9.43dBm \tag{29}$$

Now it is clearly seen how the Q of the antenna really contributes to the transmitted/received power. The effective area of the antenna is given by (30).

$$A_e = \frac{\lambda^2 G}{4\pi} = 5.1464\times10^{-5}\ \mathrm{m}^2 \tag{30}.$$

Given that the LNA post-layout simulated bandwidth is 1.32GHz, its noise floor is equal to −174dBm/Hz + 10log(1.32GHz) = −82.8dBm. Assuming the signal needs to be 10dB above the noise floor for the LNA to detect it, the minimum signal power required at the input to the LNA is $10^{(-82.8+10)/10}$ = 5.248e-8 mW = 52.48pW. Since the transmitted power was calculated as 0.114mW, the power density W_D is 0.114e-3/($4\pi R^2$). Equation (31) can be used to relate the received power, P_R, to the power density at the receive antenna, given a certain separation distance R between the transmittor and receiver via the Friis equation.

$$P_R = W_D \times A_e = \frac{0.4669 \times 10^{-9}}{R^2} \text{ Watts} \tag{31}$$

If the minimum signal power is now taken as P_R, then the maximum analytically derived range R between the TX and RX is 2.98m, which is more than that obtained in [37]. If the gain obtained from the HFSS simulation result from Fig. 31 is used, then the range reduces to 2.67m. This shows the advantage of using a high-Q bondwire antenna.

5.7 Summary

This chapter presents the idea of a bondwire antenna along with its advantages. It gives a detailed method how to analytically derive the equations for the antenna's radiation pattern, power, resistance, and directivity in spherical coordinates. It compares the plot obtained from the derivations and HFSS simulations to verify the validity of the analysis. It shows the effect the silicon-chip, metal-fill, and PCB layers have on the bondwire antenna performance, and how they change the antenna parameters through detailed HFSS simulations. It gives the small-signal circuit diagram of the power amplifier and shows how exactly the radiated power is calculated. It also gives a transceiver link-budget by taking into account the power transmitted, the antenna's

effective area and the power received by the same antenna on the receive side. It also describes a unique duplexer-less LNA/PA pair topology that will test the bondwire as an antenna. The next chapter describes the measurement strategy, method, and experimental results.

6.0 Measurement Methods, Procedures, and Results

6.1 Chip Fabrication and PCB Assembly

The AI, the input-unmatched LNA, and the duplexer-less LNA/PA designs were fabricated using IBM's CMOS 0.13μm technology available through CMC at Carleton Unviersity, and simulated using Spectre in Cadence. The PCB was designed in ADS as shown in Chapter 5 and fabricated by SpeedyPCB. The chip was glued to its place on the PCB with epoxy. Then the voltage controls and the voltage supply pads were bondwired to the PCB by Zhan Xu, a fellow PhD student. Stripped wires were soldered to the solder pads on the PCB for the voltage controls and supply.

6.2 Active Inductor

6.2.1 Measurement procedure:

First, the horizontally angled (bent) Picoprobe #51799 and #42712 available in the Faraday cage were used to do a full 2-port calibration on the 8722ES Network Analyzer from 2 GHz to 12 GHz using Picoprobe calibration substrate Part #CS-5 3681 available in the cage. The calibration substrates were not actually for the probes, but were sufficient to obtain an acceptable calibration. Normally, the on-chip de-embedding would be done using the silicon substrate and pads on the silicon chip itself, and not on a separate substrate. But there was not sufficient chip area available for both the 3 circuits, the pads for probing and the pads for voltage controls and supplies, and de-embedding as well, so the Picoprobe calibration substrate had to suffice. Once the calibration was complete, the 50-ohm calibration and open were re-probed to ensure calibration was correct. This calibration was saved for the later measurement of the duplexer-less LNA/PA with the bondwire antenna as discussed in section 6.4.

After calibration, the probes were lifted and the PCB was placed in the center of the probe-station. The station pump was turned on to keep the PCB in place so it could not move while it was being probed, in order not to damage the probes. Then the voltage supplies and controls were connected to the Keithley and other voltage sources available in the lab. Once the expected current consumption was shown on the voltage supplies, the voltage supplies and controls were turned off, and the bent probe was then carefully lowered to the pads of the chip. The microscope on the probe-station was used to view the probes as they landed on the chip pads.

6.2.2 Measurement strategy and results:

The strategy of measuring the active inductor is similar to that of measuring the velocity or position of an electron: the act of measurement itself offsets the result in such a way as to change the state of the electron. This means that the process of measuring the AI changes the AI's value and frequency response, so it does not behave as expected. If the AI is used in an application such as a filter or a matching network, as it is for the LNA/PA, its effect is clearly visible from the output signal. Thus, the technique used here was to first measure the S_{11} of the AI when the voltage controls and supplies to the AI were off, in order to measure the effect of the probes and pads alone. This is shown in Fig. 33 as an equivalent capacitance of 535.84fF at 6.5GHz. Then the S_{11} was measured when the the voltage controls and supplies to the AI were on and recorded in a Touchstone S1P file. This S_{11} included the frequency response of the AI, the probes and pads as shown in Fig. 34. Finally, the S1P file was imported into ADS as a Data Item. The effect of the pads and probes were de-embedded in ADS using a negative capacitance in parallel with the port as shown in Fig. 35. This negative capacitance is of the same value of 535.84fF at 6.5GHz given in Fig. 33 when the AI was off. The AI's impedance and S_{11} resulting from simulation of the measured S_{11} Data Item with the de-embedded capacitor is shown in Fig. 36 and Fig. 37.

It can be seen from Fig. 36 that the real part of the AI decreases just as predicted by the simulation as the AI reaches its self-resonance frequency. This demonstrates the effect of parasitic cancellation in the AI. It should be noted that the de-embedding effect of the negative capacitor does not cover the entire range of the measured frequency, but is sufficiently broad to cover the operational range of the AI. Comparing Fig. 36 to Fig. 5 and Fig. 9 of the Matlab and Cadence simulation plots, it can be concluded that parasitic cancellation occurs as expected in the novel active inductor. Fig. 37 shows the shifting of the impedance as the effects of the probes and pads are de-embedded.

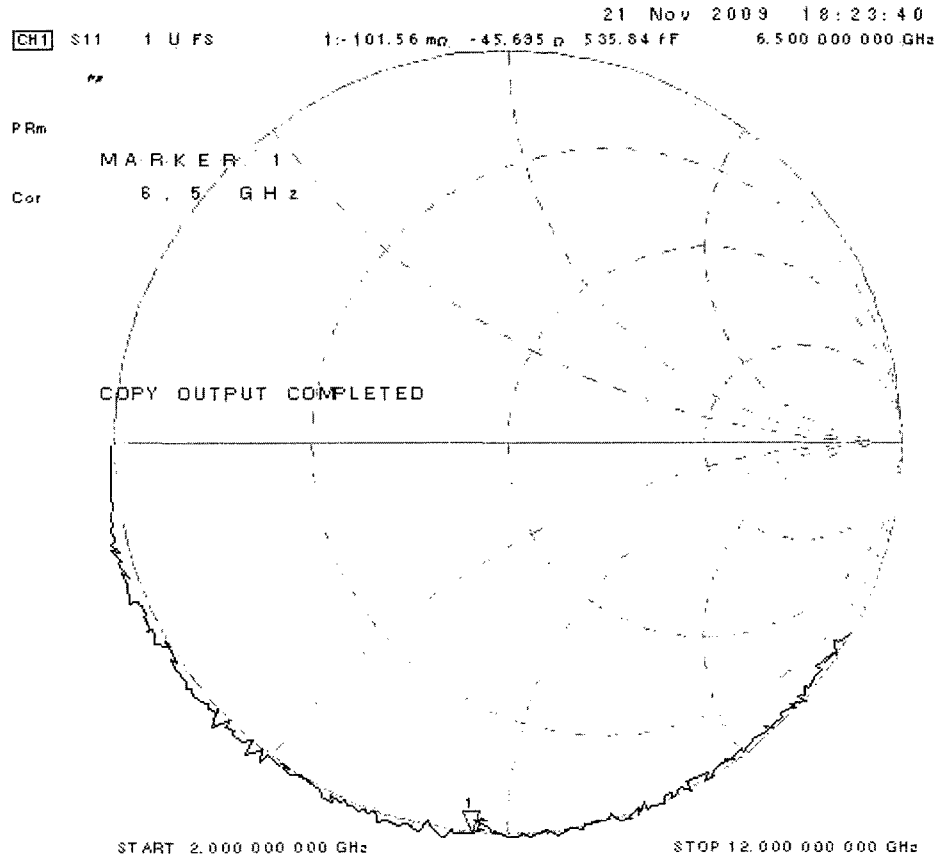

Figure 33: S11 plot obtained from the VNA with the probes landed on the chip pads but with AI turned off.

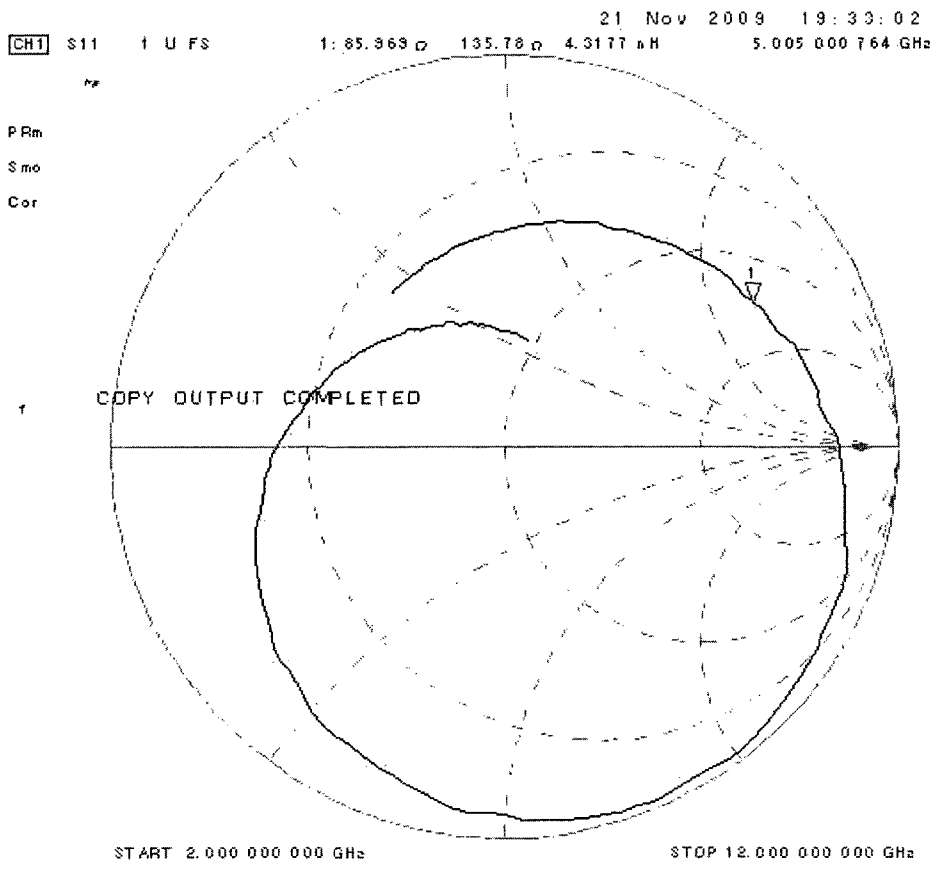

Figure 34: S11 plot obtained from the VNA with the probes landed on the chip and with AI turned on.

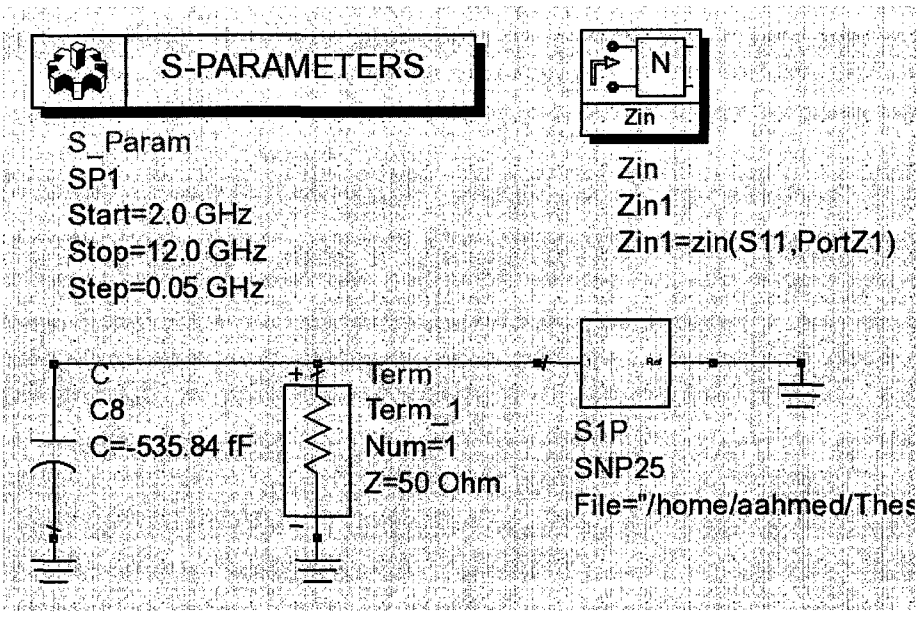

Figure 35: ADS simulation setup with the de-embedding negative capacitance in parallel with the port.

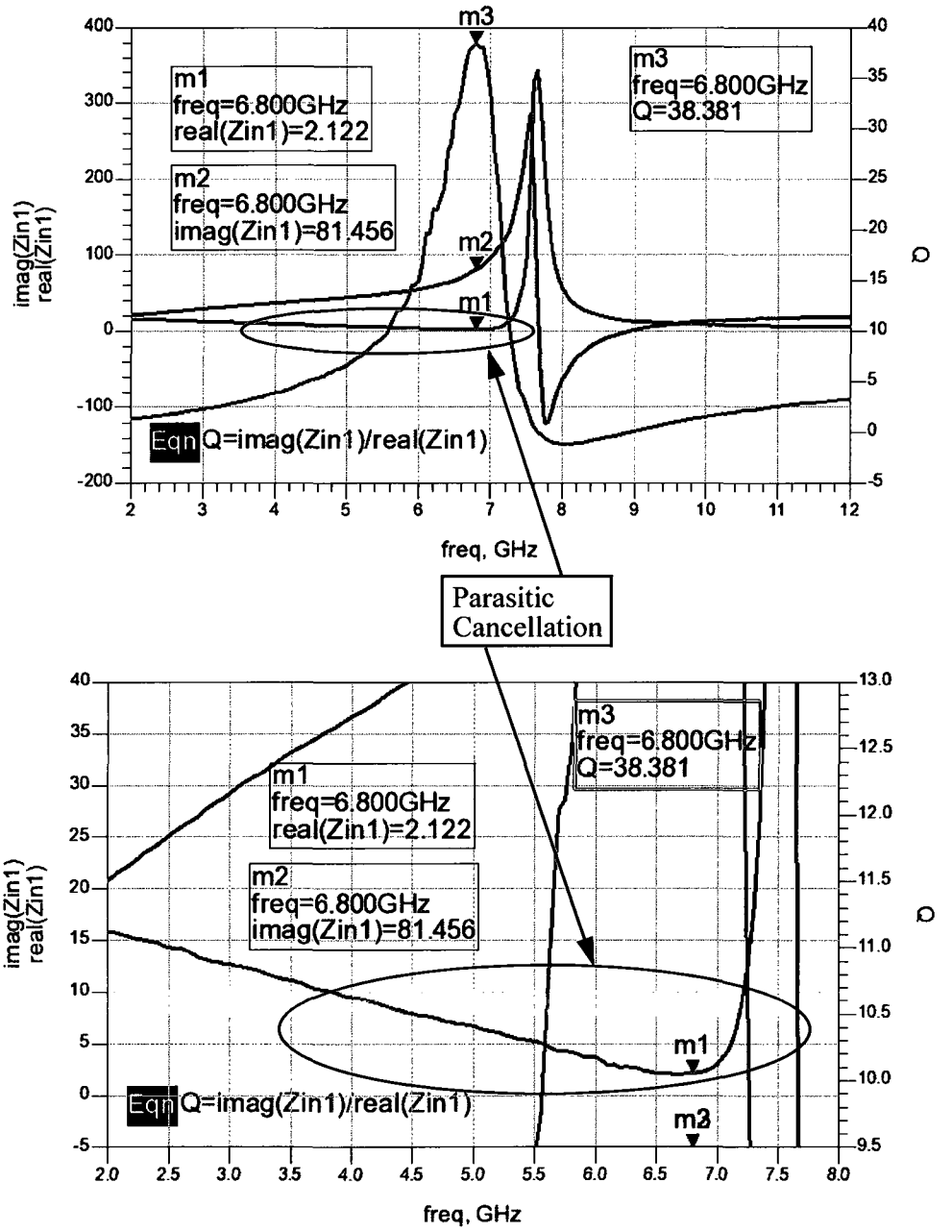

Figure 36: Impedance of the AI obtained after de-embedding the probes and pads in ADS.

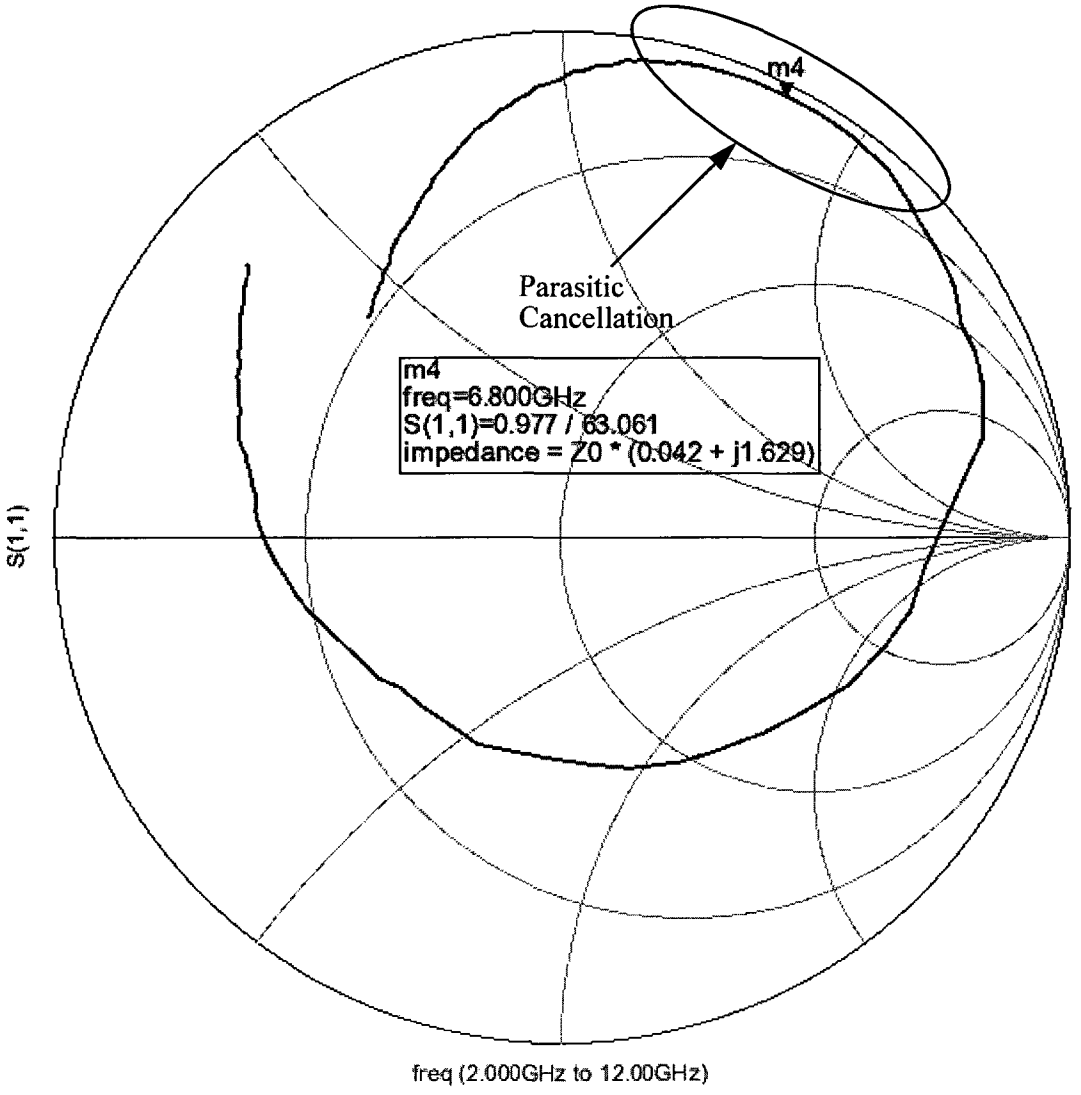

Figure 37: S_{11} of the AI obtained after de-embedding the probes and pads in ADS.

6.3 Input-Unmatched LNA

Horizontally angled (bent) probes were required to measure the 4 S-parameters of the LNA via the VNA, so that the probes did not touch the PCB and soldered wires. Since "bent" probes with 150μm pitch were not available, probes with 100μm pitch were obtained as a courtesy from ST

Microelectronics. The same calibration substrate that was used in the AI measurement was used to perform a full 2-port calibration of the VNA. Once the calibration was complete, the 50-ohm calibration and open was re-probed to ensure the calibration was correct.

After calibration, the probes were lifted and the PCB was placed in the center of the probe-station. The station pump was turned on to keep the PCB in place so it could not move while being probed, (in order not to damage the probes). Then the voltage supplies and controls were connected to the Keithley and other voltage sources available in the lab. Once the expected current consumption was shown on the voltage supplies, the voltage supplies and controls were turned off, and the probes were then carefully lowered to the pads of the chip. The microscope on the probe-station was used to view the probes as they landed on the chip pads. The power supplies and the voltage controls were then turned back on. The voltage controls of the AI that was part of the output matching network of the input-unmatched LNA were tuned to obtain the proper 50-ohm output matching as shown by the S_{22} plot in Fig. 38. Then the S_{21} and S_{11} were measured as shown in Fig. 39 and Fig. 40 respectively. The S_{11} shows clearly that the input is unmatched.

Comparing Fig 39 to Fig. 17 of the post-layout simulation result obtained in section 4.8, the gain is 1.2dB lower in the measured results. This loss is expected due to connecting cables and calibration mismatch.

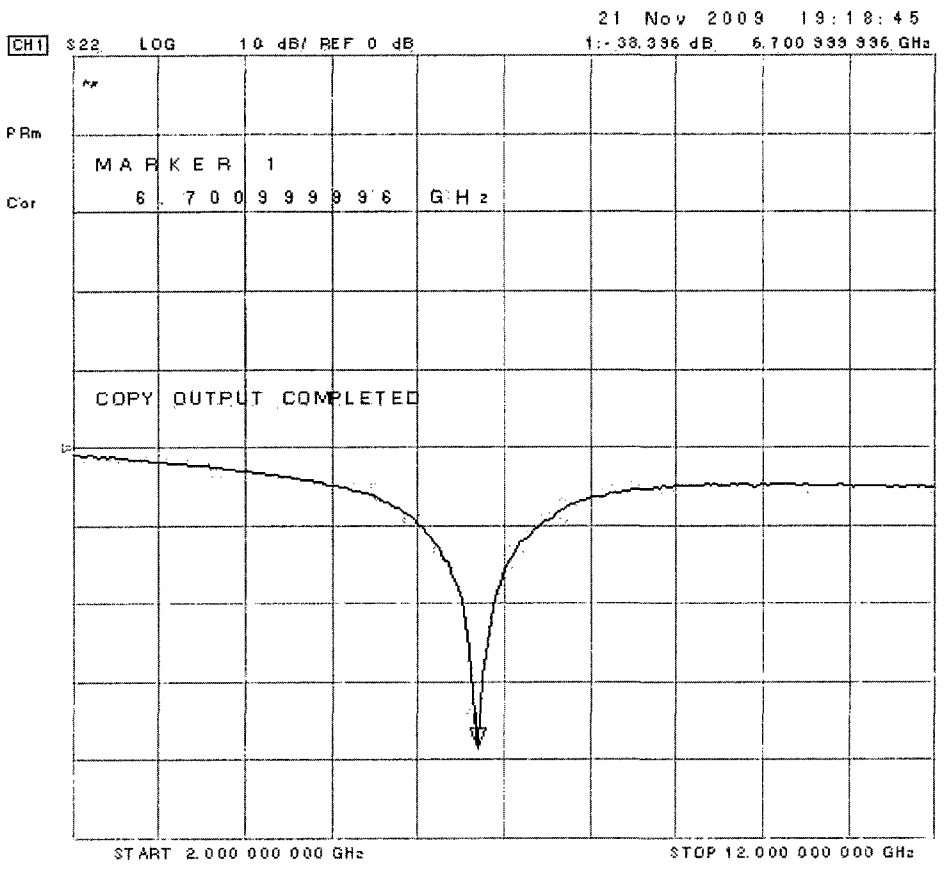

Figure 38: The measured S_{22} of the input-unmatched LNA after correctly tuning the output matching AI.

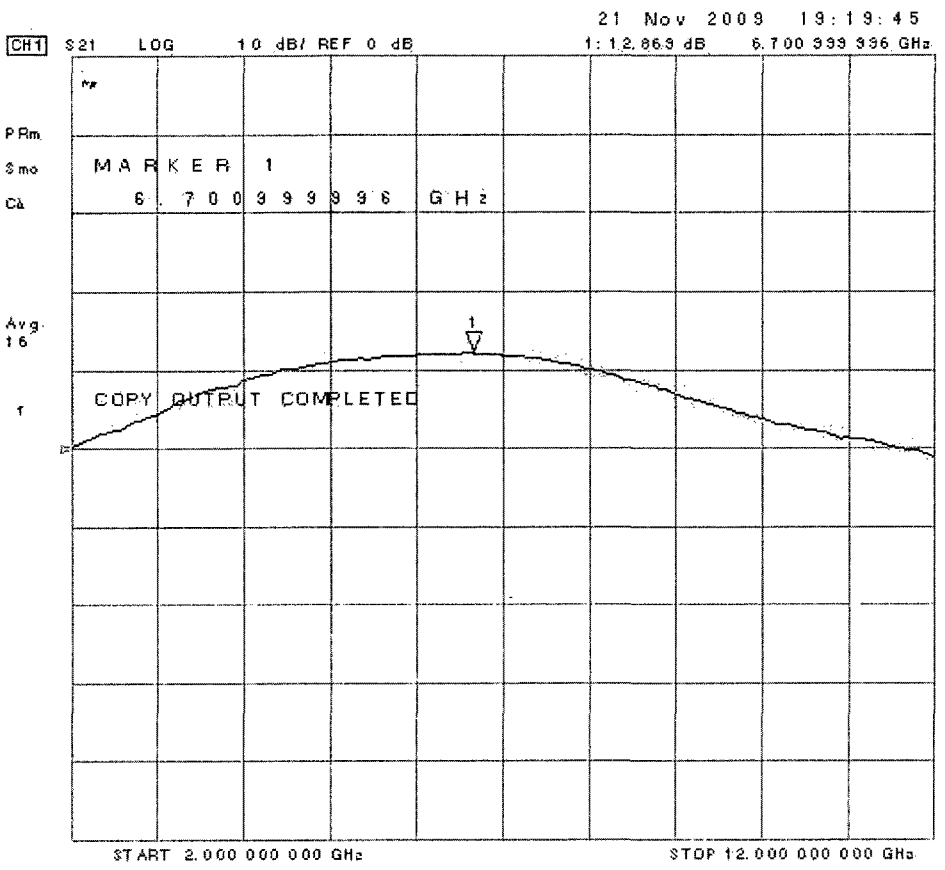

Figure 39: The measured S_{21} of the input-unmatched LNA.

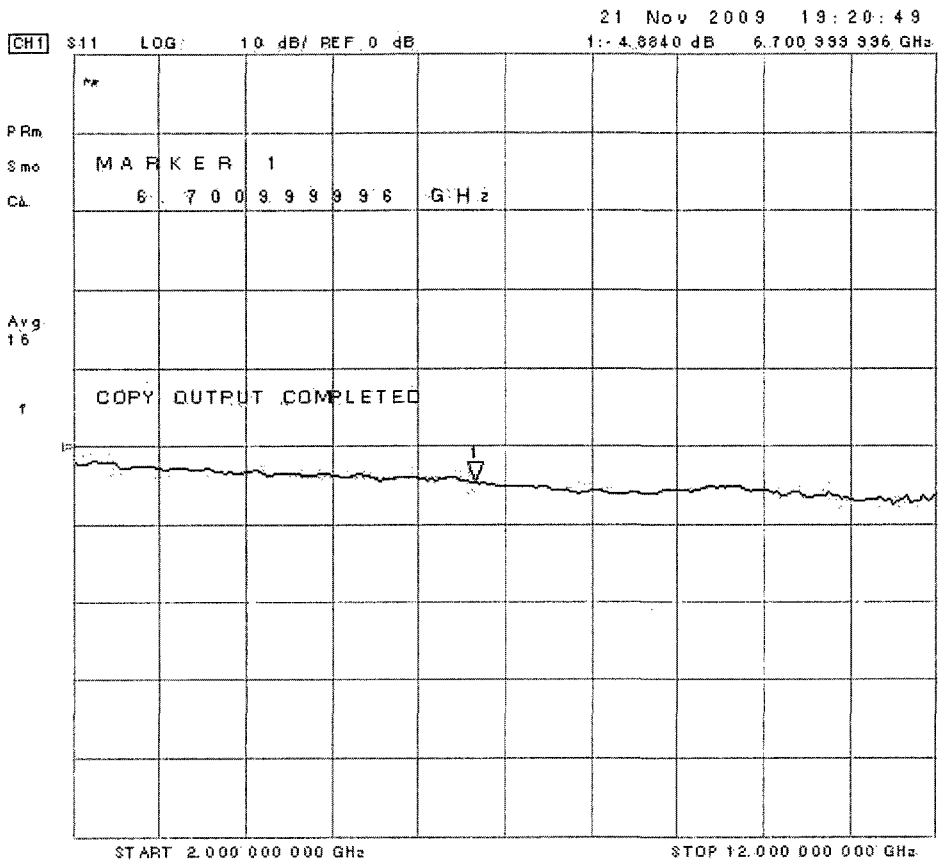

Figure 40: The measured S_{11} of the LNA showing its input is unmatched.

After measuring the S-parameters, the probes were lifted and the HP 8975A Noise Figure Analyzer was calibrated using a series noise source (SNS) connected together with all the 50-ohm cables and connecters except the 3-pin Picoprobes. The calibrated NF is shown in Fig. 41. Then the 50-ohm cables were connected to the 3-pin 50-ohm probes and the probes were carefully lowered and landed onto the chip pads to measure the LNA noise figure and gain. The measured LNA noise figure and gain are shown simulatenously in Fig. 42. The bandwidth of the gain in Fig. 42 can be compared to the bandwidth of the gain in Fig. 39. Both figures show a bandwidth of about 3.5GHz. This bandwidth can and will be reduced with a narrowband matching network or with a narrowband RF antenna. The gain of the LNA compared to the measured S-parameter is degraded

further by 0.76dB due to the longer cables required for the connection in the NF measurement. The gain has peaked at 6.7GHz instead of the simulated 6.5GHz, and the higher frequency of operation is also another source of slight loss.

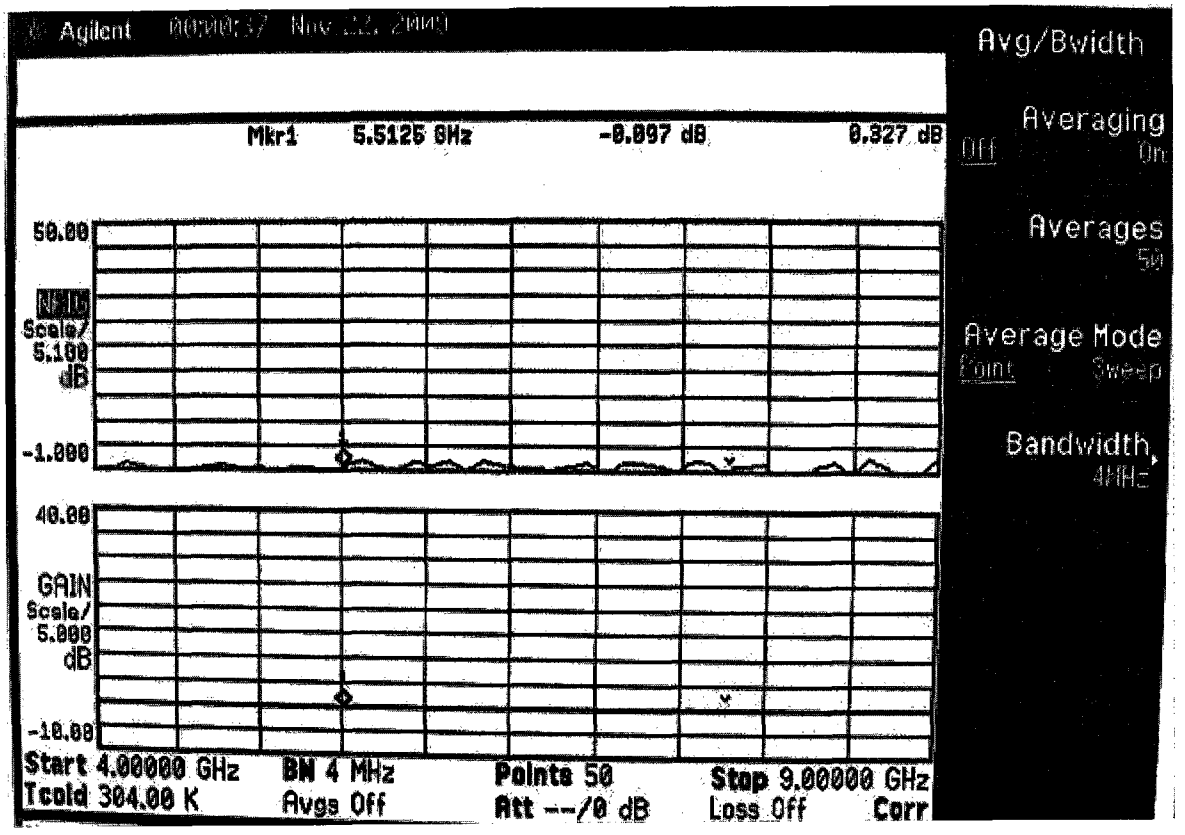

Figure 41: The calibrated output of the Noise Figure Analyzer.

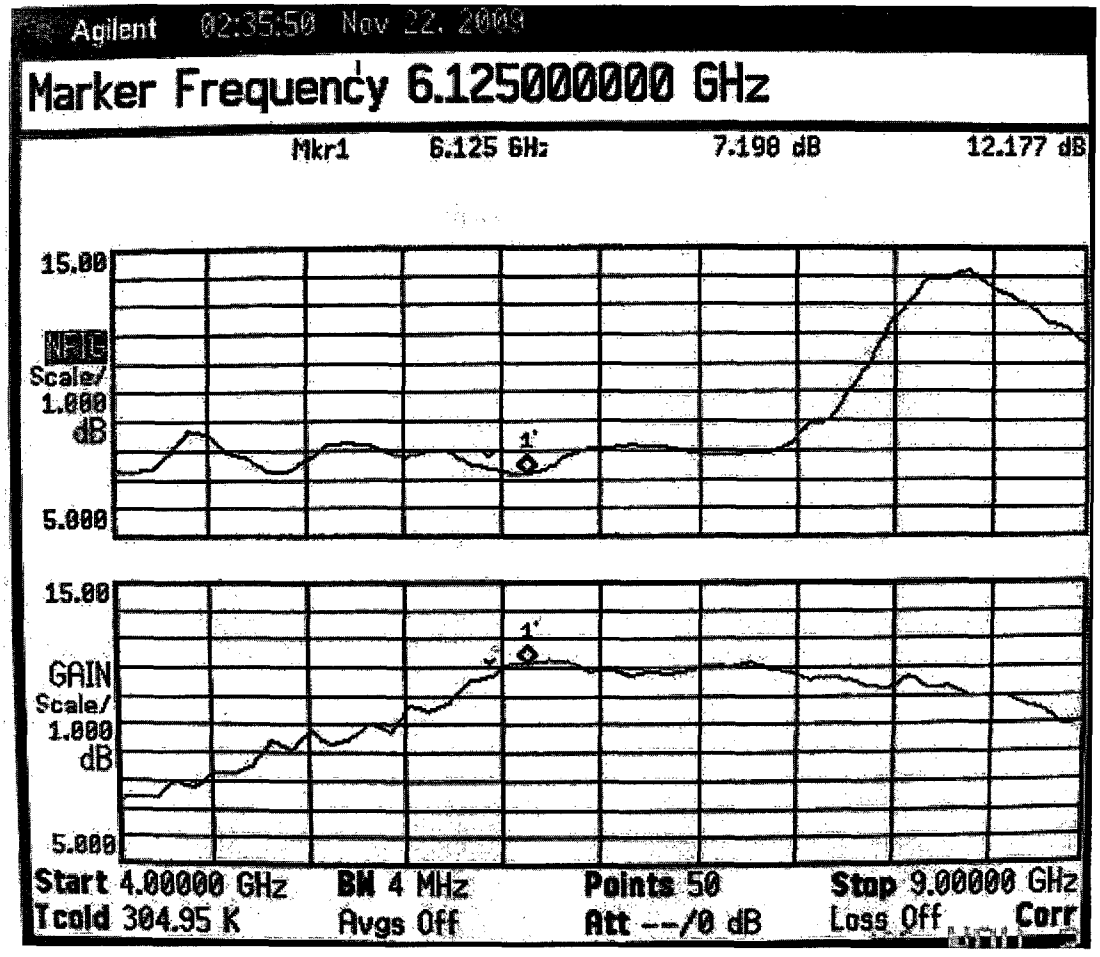

Figure 42: The output of the Noise Figure Analyzer showing the NF of the input-unmatched LNA and its gain.

6.4 Duplexer-less LNA/PA with Bondwire Antenna

6.4.1 LNA/PA and Antenna Measurement strategy:

In many designs, the antenna is a separate part of the circuit and can be simulated and tested separately. In this design, the bondwire antenna is integrated as part of the LNA/PA system together with the chip, so it cannot be tested alone in an anachoic chamber. This was because a full receiver chip was not designed, and the RF signals had to be applied through probes on pads, and not through SMA connecters. If RF signals were applied to the pads through SMA connecters and

tranmission lines (TL) on the PCB, which would be larger than the bondwire antenna, then the signal from the TL would interfere with the EM waves produced by the antenna. This would change the radiation pattern of the PCB to the extent where it could not be reconciled with the radiation pattern of the bondwire antenna. So the bondwire antenna was tested in conjunction with the LNA/PA circuit.

6.4.2 LNA Measurement procedure, results and analysis:

The same 2-port calibraton files saved as described in section 6.2.2, was re-loaded into the VNA. The PCB was placed in the center of the probe-station. The station pump was turned on to keep the PCB in place so it could not move while it is being probed, again in order not to damage the probes. Then the voltage supplies and controls were connected to the Keithley and other voltage sources available in the lab. Once the expected current consumption was shown on the voltage supplies, the voltage supplies and controls were turned off, and the probes were then carefully lowered to the pads of the chip. The microscope on the probe-station was used to view the probes as they landed on the chip pads. Now the power supplies and the voltage controls were turned back on. The switch "TX_RXb" was set to 0V to simultaneously turn on the biasing of the LNA and turn off the biasing of the PA. The voltage controls of the AI that was part of the output matching network of the LNA were tuned to obtain the proper 50-ohm output matching as shown by the S_{22} plot in Fig. 43.

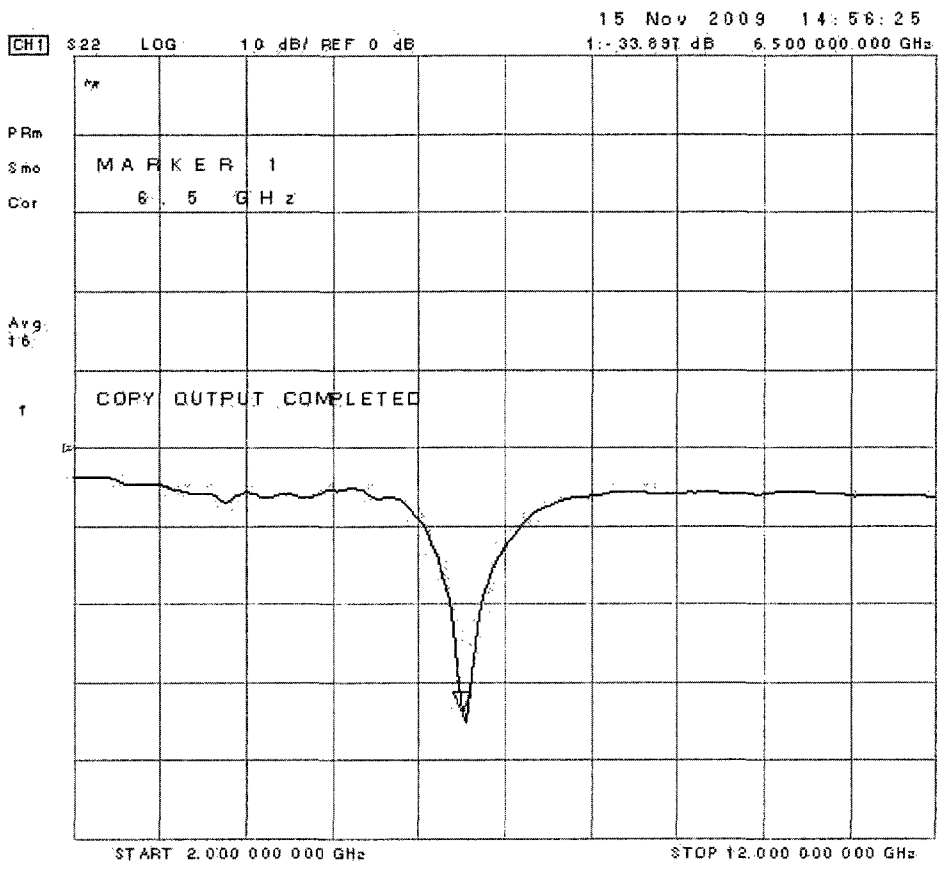

Figure 43: The S_{22} of the duplexer-less LNA/PA with its LNA turned on and PA turned off.

Now the probe was lifted and connected to the HP 8564E Spectrum Analyzer, via a 50-ohm cable to its 50-ohm input port. In a real application, this would be the input to the RX mixer and usually not 50-ohms. A broadband horn antenna H1498 from BAE Systems with a boresight gain of 10dBi was connected via a long 50-ohm cable to an HP E8257C Signal Generator (SG). The SG was set to 10dBm output power at 6.5 GHz, and was used as the transmitter. The probe was then lowered and re-landed on the LNA output pads. A meter rule was used to measure the distance of the horn antenna to the chip, with the small distance of the width of the chip 0.8mm being ignored. The antenna's H-plane was positioned parallel to the bondwire-antenna's H-plane and the measurements of the spectrum analyzer output was recorded as shown in Table 4. In this table, the

PCB rests on the X-Z plane, the Y-axis points towards the ceiling, X-axis points to the right, while the Z-axis comes out of the page towards the reader. The ϕ-direction is in the X-Y plane. Next the frequency of the SG was swept from 2 GHz to 12 GHz. The antenna was then positioned at the point of maximum gain (i.e. at ϕ=45 and θ=45) and the SA plot was set to hold the maximum value of the display. The resulting plot from the Spectrum Analyzer is shown in Fig. 44.

ϕ	θ	**SA read-out (dBm)**	**Calculated Value (dBm)**	**Difference (Loss) (dB)**
45	90	-23	-21.43	1.57
45	45	-19.4	-17.84	1.56
45	0	-21.9	-20.34	1.56
45	-45	-22.5	-20.85	1.65

Table 4: LNA Antenna Measurement: spectrum analyzer (SA) readout versus and calculated results

Table 4 shows the calculated and maximum measured Spectrum Analyzer readout for the LNA in RX mode. The measurements taken in Table 4 were taken at ϕ=45-degrees because that is direction in which the bondwire antenna has considerable gain as observed from the HFSS simulation in Fig. 31 in section 5.5, and during measurement. The power at the antenna terminals is given by (32). Applying (32) for the spectrum analyzer readout given in Table 4, where the power transmitted (P_t) is 10dBm, the horn antenna gain (G_t) is 10dB, and the bondwire antenna gain (G_r) is 0.44254 (HFSS simulated value), gives an LNA gain of 12.84dB. Comparing this to the Cadence simulated result in Fig 26 in section 5.4, this is almost 2dB smaller. Considering the consistent 1.64dB loss due to cables or bondwire deformation, the actual LNA gain would be

12.84+1.64=14.48dB, which is 0.22dB less than the result obtained from the Cadence post layout simulation. This shows the HFSS simulation results are very accurate.

$$P_{received} = \frac{P_t G_t G_r \lambda^2}{(4\pi R)^2}(dBm),\ G_{LNA} = P_{measured} - P_{received}(dB) \qquad (32)$$
$$\text{similarly, } G_{PA} = P_{measured} - P_{received}(dB)$$

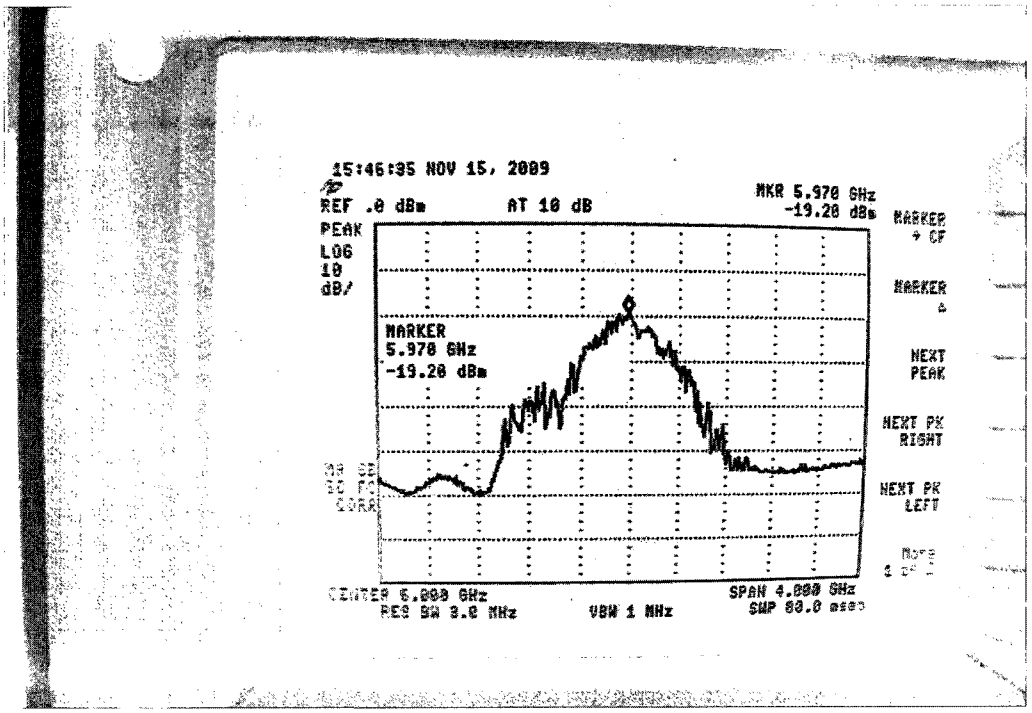

Figure 44: LNA output with signal generator frequency sweep from 2 GHz to 12 GHz with power level at 10dBm.

6.4.3 PA Measurement procedure, results and analysis:

After the measurements for the LNA, the probes were lifted and the voltage control TX_RXb was set to 1.2V to turn on the PA and turn off the LNA simultaneously. The voltage controls of the AI that was part of the input matching network of the PA were tuned to obtain the proper 50-ohm input matching as shown by the S_{11} plot in Fig. 45.

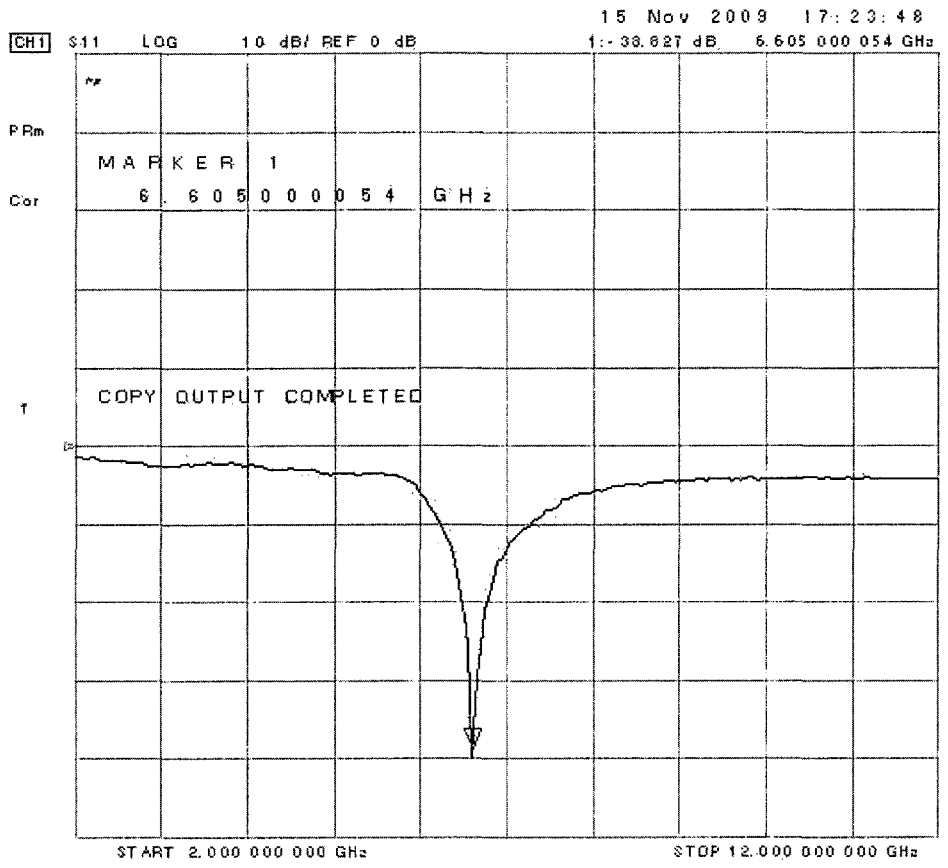

Figure 45: The S_{11} of the duplexer-less LNA/PA with its PA turned on and LNA turned off.

Now the probe was lifted and connected to HP E8257C Signal Generator (SG), via a 50-ohm cable to its 50-ohm output port. The SG was used as a signal source. In a complete application of SoC design, this would be the output of the TX mixer. The broadband horn antenna H1498 from BAE Systems with a boresight gain of 10dBi was connected via a long 50-ohm cable to the HP 8564E Spectrum Analyzer. The output resistance of the PA transistor was 437 ohms. In parallel with the equivalent bondwire parallel resistance of 2566 ohms, this results in a total resistance seen at the output of the PA of 373 ohms at resonance (when the bondwire inductance resonates with the pads and output capacitance of the bondwire-antenna). To ensure the output of the PA swings rail-to-rail for Vdd=1.2V and Vss=0V, the PA output power should be $(1.2)^2/373 = 5.9$dBm. Since the

gain of the PA obtained from the post layout simulation shown in Fig. 27 is 14.4dB, the input power to the PA should be -8.5dBm. To ensure the PA output does not clip and the PA remains in Class-A operation, an input power of -10dBm was chosen.

The SG was set to −10dBm output power to ensure the PA output was rail-to-rail at 6.5 GHz, and was used as the input to the PA. The probe was then lowered onto the PA input pads. A meter rule was used to measure a distance of 0.5m from the horn antenna to the chip, with the small distance of the width of the chip 0.8mm being ignored. Any distance larger than 0.5m did not give an output sufficiently large to be viewed on the Spectrum Analyzer display. The antenna's H-plane was positioned parallel to the bondwire-antenna's H-plane and the measurements of the spectrum analyzer output was recorded as shown in Table 5. Next the horn antenna was brought 10cm closer to the chip so the plot is more visible and the SG frequency was swept from 2 GHz to 12 GHz. The antenna was then positioned at the point of maximum gain (i.e. at ϕ=45 and θ=45) and the SA plot was set to hold the maximum value of the display. The resulting plot from the Spectrum Analyzer is shown in Fig. 46.

Since the power transmitted is given by (29) as -9.43dBm in section 5.6, the power received by the Horn is calculated by (32) to give -43.72dBm at the 40cm distance, and -45.67dBm at 50cm. The output of -45.2dBm and -47.3dBm at a distance of 40cm and 50cm respectively was read from the SA giving a loss of 1.48dB and 1.63dB respectively due to cables and interference from surrounding metals. This shows again that the HFSS simulations were extremely accurate.

ϕ	θ	SA read-out (dBm)	Calculated Value (dBm)	Difference (Loss) (dB)
45	90	-50.9	-49.26	1.64
45	45	-47.3	-45.67	1.63
45	0	-49.8	-48.17	1.63
45	-45	-50.3	-48.68	1.62

Table 5: PA Antenna Measurement: spectrum analyzer (SA) readout versus and calculated results

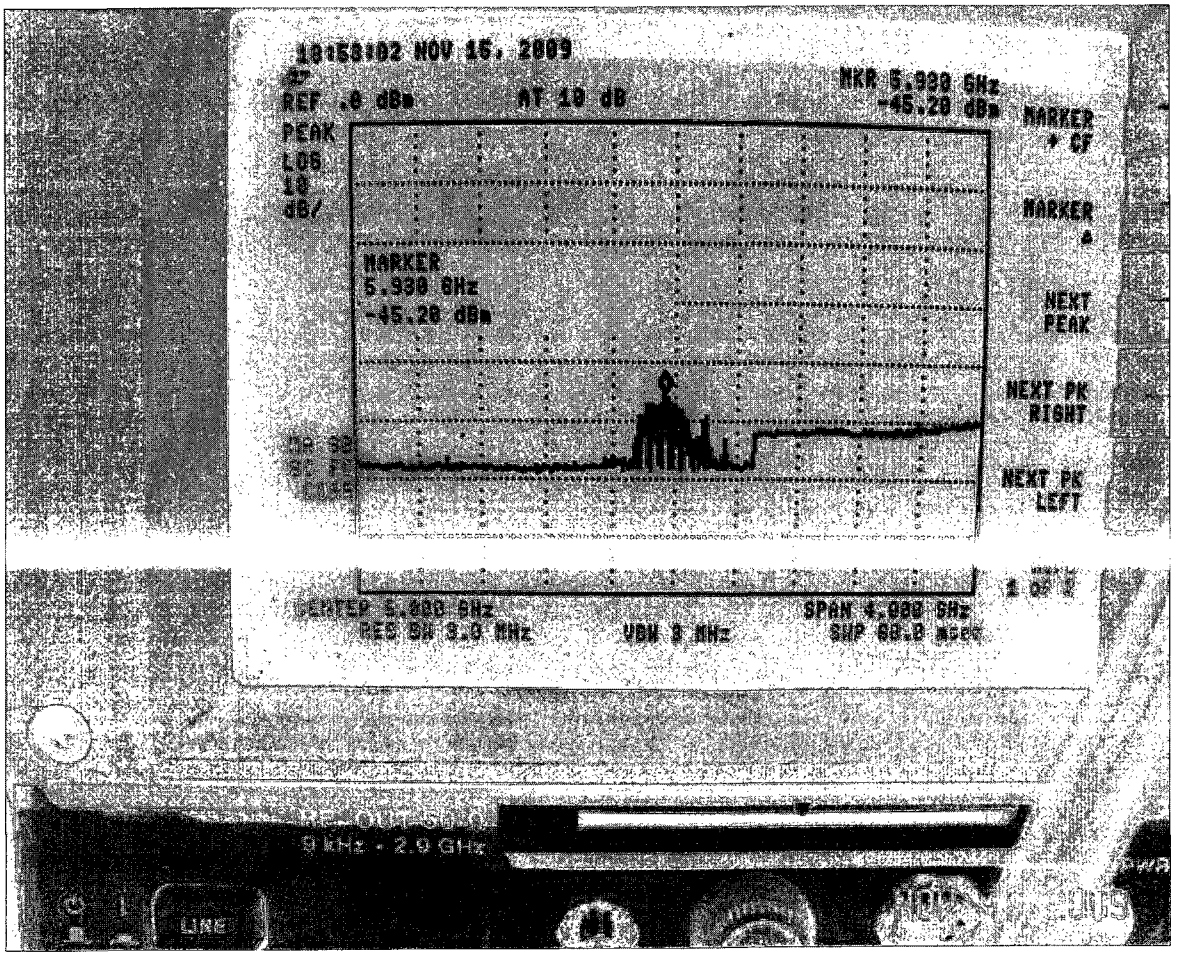

Figure 46: PA output with signal generator frequency sweep from 2 GHz to 12 GHz with power level at -10dBm.

Given that the measured LNA/PA bandwidth is 400MHz, its noise floor is equal to -174dBm/Hz + 10log(400MHz) = -88dBm. Assuming the signal needs to be 10dB above the noise floor for the LNA to detect it, the minimum signal power required at the input to the LNA is $10^{(-88+10)/10}$ = 1.585e-8 mW = 15.85 pW. Since the transmitted power was calculated as 0.114mW, the power density W_D of the incoming wave from a transmitting PA to the receiving LNA of the same chips is 0.114e-3/($4\pi R^2$). Now (31) can be used again to relate the received power, P_R, to the power density at the receive antenna, given a certain separation distance R between the transmittor and receiver via the Friis equation. If the minimum signal power is now taken as P_R, then the maximum measured range R between the TX and RX is 4.86m, which is 2.7 times the result obtained in [37]. This again shows the advantage of using a high-Q bondwire antenna.

6.6 Summary

This chapter describes the measurement procedure used for the measurement of the Active Inductor, the input-unmatched LNA, and the duplexer-less LNA/PA with the bondwire antenna, and presents the measurement results of these circuits. In the case of the AI, it shows how the probe and pad parasitics were de-embedded using the results from the network analyzer, the S1P file and the ADS simulation. It compares the S-parameter and the Noise Figure results of the input-unmatched LNA (IULNA) to the S-parameters and gain of the duplexer-less LNA/PA (DLP) with the bondwire antenna in TX and RX mode to show how the noise figure of the DLP circuit can be deduced from the measured result of the IULNA and the simulated result of the DLP. It compares the measured radiated power from bondwire-antenna in the TX mode of the DLP to the simulated value, deducing the PA and antenna gain from it, including the path loss. Similarly, it compares the LNA output power in the receive path to the simulated value of the bondwire-antenna and LNA gain, including the path loss. Finally it gives the maximum communication distance that can be

obtained if the PA was transmitting and the LNA was receiving simultaneously. The next chapter presents the conclusion of this thesis.

7.0 Conclusion

7.1 Thesis Summary and Contributions

A new active inductor (AI) topology was designed and its small-signal impedance was analytically derived and simulated in both Matlab and Cadence using IBM's CMOS 0.13μm available from CMC at Carleton University. Both simulation results match even though not all parasitics were taken into account in the Matlab simulation. The active inductor was measured using picoprobes and a network analyzer. Here the touchstone ".s1p" file was saved and re-simulated in ADS with the equivalent negative capacitance in parallel with the S-parameter ports, to de-embed the RF pads and probes. The resulting impedance shows almost exactly the same behaviour as the Matlab and Cadence simulations, with similar values for inductance and Q as simulated in the corner simulations. This AI consumes only 2mA. At its highest Q point, an inductor of 1.9nH is achieved. Larger inductances can be obtained with lower current and thus a lower g_{m2}, as indicated by (10) (since $\mathrm{Im}[Z_2]$ is approximately proportional to $1/g_m$). Table 6 shows the active inductor in comparison with one of recently reported in literature.

REF	Process	L (nH)	Q	NF	Chip Area (mm^2)
[3]	0.18μm	?	?	4.75-6.7	0.05
This Work	0.13μm	1.9	38.8	2.6-4 (NFmin)	0.0026

Table 6: Active Inductor Comparison.

On the same chip as the active inductor, a 3-stage common source LNA was designed with its input unmatched to the 50-ohm port. The active inductor was used to match the output of an input-unmatched LNA to the 50-ohm input of a network analyzer, and then the NF of the LNA was

measured. Both simulation and measurement show a NF of 6.2 and 7.2dB respectively, showing a loss of 1dB. Since the NFmin of the Cadence post-layout simulation result was 3.34dB, this leads to the conclusion that, if the LNA input was matched to the 50 ohms, then the LNA NF would be about 3.3dB to 4.3dB. Table 7 shows the comparison of the LNA with similar reported results. As can be seen from table 7, [12] and [2] obtain their performance from the smallest sub-micron technology available, while [3] uses stacked inductors in a feedback configuration similar to that of an active inductor topology, resulting in a high-Q low noise input match. Reference [5] uses feedback input matching, but the power consumption is 5mW larger, and the gain is about half of that obtained in this work.

Reference	**Tech**	**S_{21} (dB)**	**NF (dB)**	**Power**
12	90nm	14dB	3.2dB	9.7mW
2	65nm	4dB	4dB	21mW
3	130nm	16.8dB	2.2dB at 3.4GHz	8.16mW
5	130nm	11.2dB	2.5dB	13.5mW
This Work	130nm	14.4dB	3.4dB (NFmin)	8.16mW

Table 7: LNA Comparisions

Again on the same chip, the same LNA design was integrated with a class-A PA design and a bondwire antenna to form a duplexer-less LNA/PA circuit as shown in Fig. 47. The bondwire was used as a load for the PA, and used simultaneously as a resonating-and-matching antenna for the LNA, with TX and RX controlled by the biasing of the LNA and PA. The PA design was similar to the LNA. The full design was simulated in Cadence. The antenna was simulated in HFSS together with the chip and its top metal layers including power-rails and metal-fill, and the exact PCB layout that was sent for manufacture at SpeedyPCB.

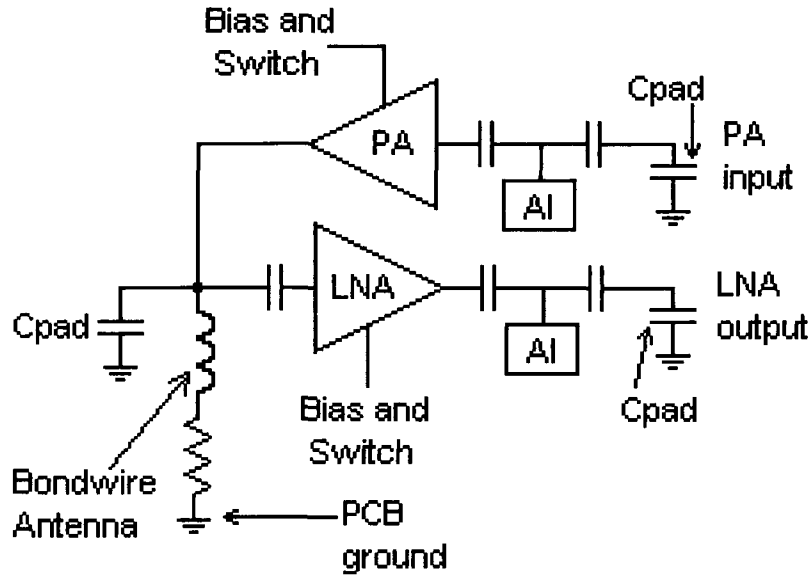

Figure 47: Simplified schematic of the duplexer-less LNA/PA with bondwire antenna.

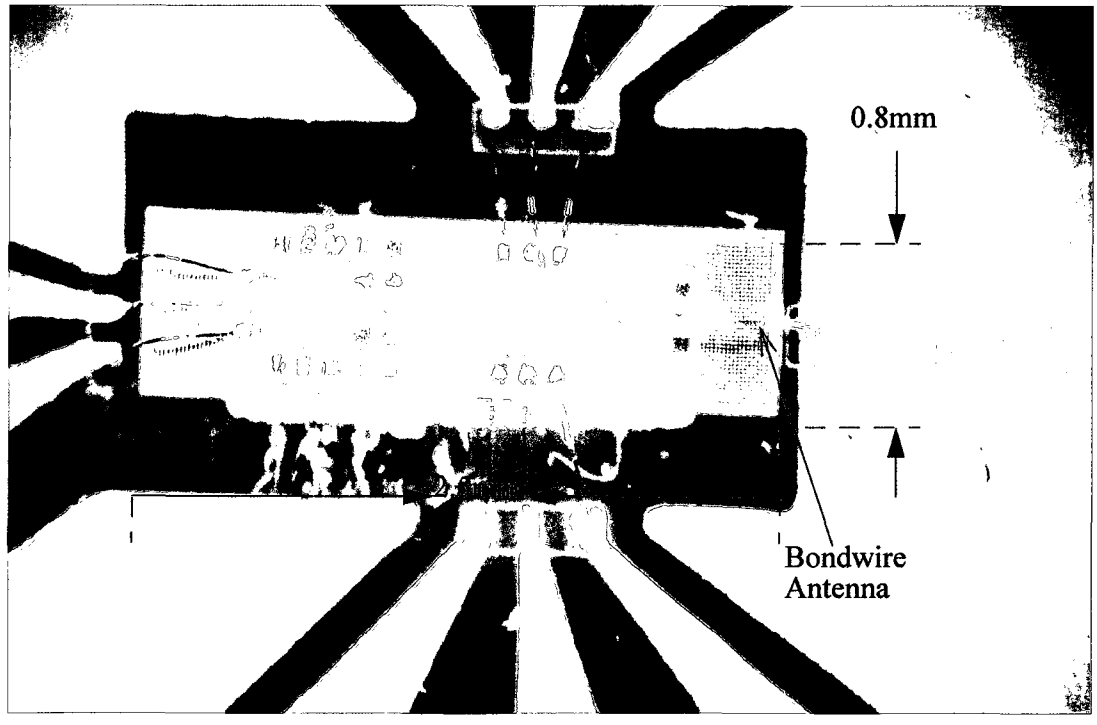

Figure 48: Photograph of the chip bondwired to the PCB showing the bondwire-antenna.

The silicon chip, containing the AI, input-unmatched LNA, and the duplexer-less LNA/PA was attached to the PCB with epoxy and then bondwired to the PCB pads as shown in Fig. 48. The LNA/PA performance was measured in conjunction with the antenna as discussed in section 6.4. The HFSS simulations show the bondwire antenna gain of -3.54dBi at 6 GHz. The Cadence and HFSS simulation results were compared to the measured results and showed only a 1.6dB loss due to cable connections. This indicates that the LNA performance is close to the simulated gain of 14.7dB and therefore should have a NF of a value close to 4.9dB as simulated, since the NF of the input un-matched LNA was measured to be within 1dB of error. This reasoning was employed because the NF cannot be directly measured for an LNA in a wireless link, unless a full system on chip radio is designed, and the resulting jitter and BER is measured, which was beyond the scope of this work. Table 8 shows the comparison of this research on LNA/PA designs with recently published transceivers in the same frequency range.

Reference	Tech	S_{21} (dB)	NF (dB)	Power
56	90nm	?	?	33mW
40	250nm	13dB/7.27dB	2.9dB	26.1mW
This Work	130nm	14.7dB/14.4dB	4.9dB	10.2mW

Table 8: LNA/PA Comparison

7.2 Future Works and Recommendations

As mentioned in this section 3.3, the biasing controls of the active inductor can be used for process tracking. A custom circuit could be designed to track the process variation of the AI components. In addition to that, Monte-Carlo simulations could be done together with that circuit to evaluate the exact limitations and yield of this AI design. Also, an important parameter to obtain would be the sensitivity of the AI value to the variations in the bias voltages, and this should be

simulated and calculated in addition to process variations in Monte-Carlo simulations. Although the performance of this AI is exceptional, it is recommended that this AI not be used for volume-production unless the Monte-Carlo simulation is re-done and a process tracking circuit is designed.

In order to speed up simulations, the AI can be modeled as 2 coupled passive inductors connected to ground with points A and B shown in Fig. 2 as the inputs of the inductors. This model can be cross-checked with post-layout simulation results, and the correct coupling factor with parasitic capacitances can be used in the model. Although it is clear from the analytical equations that this AI cannot be used differentially, it could be used "in-line" with the points A and B shown in Fig. 2 as the 2 ends of an inductor. The loss of using it as such could be investigated. Also, this AI can be used as a single-ended transformer with point A as its input and point B as an output, if the ratio between the sizes of the transistors M1:M2 and M3:M4 were increased. The limitations of this circuit could also be investigated.

The LNA design procedure is given for a simple common-source LNA. A similar procedure could also be formulated for other topologies like cascode, common-gate or feedback topologies for UWB LNAs.

Various bondwire antenna topologies could be investigated. Also, instead of using the bondwire as an antenna, two bondwires could be used to differentially carry the signal from the chip to a PCB antenna which would be more efficient. Instead of using a single bondwire antenna on the chip, several PAs together with bondwire antennas could be strategically placed in a full SoC circuit to provide both a larger transmit gain and a wider broadside angle for chip-to-chip or PCB to PCB communication, and to eliminate polarization loss, especially on large SoC circuits which are thousands of micrometers in dimensions.

7.3 Summary

This chapter summarizes the research undertaken in this thesis, and presents the measurement results of the AI, the input-unmatched LNA and the duplexer-less LNA/PA with the bondwire antenna. It concludes that the measurement results match closely to the calculated and simulated values of all the circuits within experimental measurement errors. It provides tables of comparisons with published AI, LNA and LNA/PA designs with similar frequency ranges to demonstrate the advantages of the work presented in this thesis. Finally, it mentions the future work that could be done to further investigate or improve the circuits in this thesis, and gives recommendations on the usage of the AI.

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