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Superconductive Analog-to-Digital Converters in Wireless Radio Applications

By

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Dipl. Eng., Electrical and Computer Engineering (2001)

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for the partial fulfillment
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Abstract

Requirements for lowpass and bandpass sampling operation for wideband radio are extracted and special focus is given on the time jitter specification. The effect of clock jitter on QPSK and IS-95 systems is analyzed and specifications are extracted. A new type of analog-to-digital converter is presented and its performance is evaluated. The superconductive ADC is based on the Rapid Single Flux Quantum digital logic, which is a promising technology employing Josephson junctions. The applicability of the device is investigated under wireless radio systems. Specifications under bandpass sampling operation of the superconductive phase modulation ADC are proposed. Finally, test results are presented for the superconductive ADC in comparison to the state-of-the-art semiconductor ADC.

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Glossary

3GPP	3 rd Generation Partnership Project
ADC	Analog-to-Digital Converter
BCS	Bardeen Cooper Schrieffer
BER	Bit Error Rate
CDMA	Code Division Multiple Access
CRSJ	Capacitor Resistor Shunted Junction
DEC	Decoder
DG	Diversity Gain
ENBW	Effective Noise Bandwidth
ENOB	Effective Number Of Bits
FER	Frame Error Rate
FSR	Full Scale Range
HTS	High Temperature Superconductivity
IS-95	Interim Standard 95
JJ	Josephson Junction
LO	Local Oscillator
LSB	Least Significant Bit
LTS	Low Temperature Superconductivity
NF	Noise Figure
PG	Processing Gain
PM-ADC	Phase Modulation Analog-to-Digital Converter

PPJ	Peak Percent Jitter
PSD	Power Spectral Density
RSJ	Resistor Shunted Junction
RSFQ	Rapid Single Flux Quantum
SDR	Software Defined Radio
SFDR	Spurious Free Dynamic Range
SFQ	Single Flux Quantum
SNR	Signal-to-Noise Ratio
SQUID	Superconductive Quantum Interference Device
SYNC	Synchronizer

Chapter 1

Introduction

The progress in wireless radio systems in the recent years has changed the way circuits are designed and built. New ideas have been implemented and traditional transceiver structures have changed through time. The most widely used architecture, the superheterodyne receiver, is steadily being replaced by more sophisticated circuits that operate at higher data rates. A typical radio receiver consists of two parts: the analog front-end and the digital back-end. Until recently, the focus of the design was on the analog part having many discrete components many of which were placed off chip (e.g. filters). Advances in VLSI technology enabled the use of fast and low cost digital circuits that can perform many of the functions previously done in the analog part of the circuit. For example we could employ digital downconversion and filtering, thus eliminating the need for expensive off-chip filters, mixers and VCOs. The ultimate goal is reduce the overall cost of wireless basestation by allowing flexibility to the receiver to support many different standards. This calls for higher performance receiver. The evolution in the design of receivers is shown in Fig. 1.1. Modern wireless standards are designed in such a way that high data rates are supported at a minimum cost. That implies the allocation of extra bandwidth to a user and the simultaneous processing of more than one channel by the receiver. Wideband radio is becoming a popular approach and is considered the intermediate stage before the advent of Software Defined Radio (SDR). The two terms describe similar concepts but there exist certain differences. Wideband radio is a more

generic term that describes architectures that can support increased bandwidths such as WCDMA or 3-channel IS-95. On the other hand, SDR remains a concept rather than an implementation and refers to a receiver that performs most of the processing in the digital domain. This implies that the receiver can handle signals from different standards using the same hardware equipment.

Figure 1.1: Receiver architectures (a) Superheterodyne, (b) Direct conversion (Quadrature sampling) and (c) Direct sampling (Digital IF).

The first receiver architecture, the superheterodyne (Fig. 1.1a) is the most popular and is made up of many discrete components. The signal is downconverted from the Radio Frequency (RF) to an Intermediate Frequency (IF). In order to reduce the presence of the

image frequency and reject interference signals that could saturate the receiver thus reducing Signal-to-Noise Ratio (SNR), filters are required before each mixer. The signal is converted from analog to digital after the IF stage and further processed in the baseband portion of the circuit. The advantage of this design is the high selectivity but the cost is not optimum due to the analog filters and the downconversion stage (mixer and local oscillator). Overall, the superheterodyne receiver offers little flexibility.

In the direct conversion receiver (Fig. 1.1b), only one downconversion stage is used in order to reduce the cost. The signal is mixed from RF directly to baseband or very low IF. It is further split to In-phase and Quadrature components by a quadrature demodulator. The main problem is the existence of a DC frequency component and the I/Q imbalance of the demodulator [1].

Since the cost of a system is proportional to the number of off-chip components and downconversion stages, it is reasonable to remove those costly components and place the Analog-to-Digital Converter (ADC) as close to the antenna as possible. In this case, the signal is sampled directly from RF and the high data rate digital signal is digitally downconverted to baseband frequency. The requirements for analog parts are reduced to two RF filters and a Low-Noise Amplifier (LNA) only. Signal processing takes place in the digital part the receiver which can be either an Application Specific Integrated Circuit (ASIC) or a Field Programmable Gate Array (FPGA). Current technology offers many solutions for digital processing of high data rate signals.

As can be seen from the block diagram of the direct sampling or digital IF receiver (Fig. 1.1c), the most important component is the ADC. Its exposure to strong blocking tones under operation at high sampling rates impose linearity and dynamic range

limitations. Thereby, it has to meet stiff requirements making its design a hard task but simultaneously a prosperous field of research. The purpose of this work is to provide an analysis to the specifications of an ADC for wireless radio systems such as IS-95 and WCDMA and investigate the effect of specific non-idealities in the overall performance of the system.

Chapter 2 presents an analysis on requirements for ADCs used in wideband radio. It deals with the issue of undersampling (sampling at rates below the Nyquist rate), the dynamic range needed for operation under wireless standards, the relationship between spectral purity of the clock and total performance and the immunity of the receiver to blocking signals and noise.

Clock jitter is further discussed in Chapter 3 where simulations of sampling systems are shown. Clock jitter or equivalently clock phase noise is a major limitation in wideband radio making the ADC a 'bottleneck' of the system. The figure of merit is the Signal-to-Noise Ratio (SNR) since it is more appropriate for wireless standards rather than Bit Error Rate (BER).

A new type of high speed ADC is presented in Chapter 4. The superconductive Phase Modulation ADC offers many advantages against typical ADCs due to the physical characteristics of the Josephson junction.

The superconductive device is characterized under continuous wave signals and results are presented in Chapter 5. In addition, the state-of-the-art semiconductor ADC is characterized under the same testing conditions and results are directly compared.

Chapter 2

ADC Requirements for wideband radio systems

2.1 ADC Fundamental Concepts

If the ADC is assumed as an ideal device, there is a theoretical limit in the SNR. The SNR is proportional to the number of bits B according to the following equation:

$$SNR = 6.02B + 1.76 \text{ (dB)} \quad (2.1.1)$$

for Nyquist rate sampling. In many applications, the ADC operates under oversampling scheme, which increases the SNR by the oversampling ratio:

$$SNR = 6.02B + 1.76 + 10 \log \left(\frac{f_s}{2f_{\max}} \right) \text{ (dB)} \quad (2.1.2)$$

where $f_{\max}$ is the maximum frequency of the analog input signal. A proof of these equations can be found in [2]. Table 2.1 shows the theoretical limits in SNR as a function of number of bits B when $f_s = 2f_{\max}$. It should be noted that the above equations are derived under the assumption that the only source of noise is quantization.

Table 2.1: Theoretical SNR of an ideal ADC.

SNR (dB)	Number of Bits
74	12
80	13
86	14
92	15
98	16

An ADC has two major types of noise. The first is the thermal noise of the circuit and the other is due to the quantization of the input signal. Quantization inherently means loss of information; otherwise, the ADC would require an infinite number of bits. The difference between the analog and the digital signal is referred as quantization noise. It is present in all ADCs and is inversely proportional to the number of bits. Equations (2.1.1) and (2.1.2) are based on an ADC model having wideband flat quantization noise that can be considered as an additive white noise signal uncorrelated to the input. They are also valid for sinusoidal inputs at Full Scale Range (FSR). The FSR is the difference between the maximum and minimum analog input voltages. For signals having different peak-to-rms ratios these equations do not hold but can be regarded as an upper limit of performance. The mean square quantization noise power with respect to input is:

$$P_{QN} = \frac{q^2}{12R}$$

where q is the quantization step size and R is the input resistance of the ADC. The quantization step size equals the FSR over 2^B (number of different states). Commercial ADCs have FSR varying from 1 to 20V.

For example, a 16-bit ADC with $FSR = 5V_{rms}$ and input impedance of $R = 50\Omega$ would have:

$$q = \frac{FSR}{2^B} = \frac{5V}{2^{16}} = 0.076mV$$

and

$$P_{QN} = \frac{(0.076mV)^2}{12 \times 50\Omega} = 9.7pW$$

or

$$P_{QN} = -80.13dBm.$$

This quantization noise power corresponds to the minimum input signal that can be detected by the ADC. If the signal power is less than the quantization noise, an amplification stage is necessary. In theory, it is desired to have the signal power 3 dB above the quantization noise. In practice, the signal power must be 10-15 dB above to reduce noise contribution to 0.1-0.4 dB.

2.2 Theory of Undersampling

It is well known from the Nyquist theorem that the sampling rate, f_s , of an analog signal must be at least twice the maximum frequency, $f_{\max}$, in order to avoid aliasing:

$$f_s \geq 2 \cdot f_{\max} \quad (2.2.1)$$

In a direct sampling receiver design, it would mean that we need an ADC sampling at twice the maximum frequency of the incoming signal. For the CDMA Band Class 1, the sampling rate would have to be:

$$f_s \geq 2 \cdot f_{\max} = 2 \times 1910 \text{ MHz} = 3820 \text{ MS} / \text{s}$$

Such a high frequency is practically not realizable if high resolution is also required. Fortunately, this is not the only available option. The signal can be sampled at a rate lower than the Nyquist frequency and reconstructed without loss of information. The technique is called undersampling or bandpass sampling and is derived from the Nyquist theory. Undersampling is essentially intentional aliasing and if used under some conditions the aliased version of the sampled signal contains all the spectral components of the original band.

Similarly to [3] we can show that when a bandpass signal is sampled at a rate lower than the Nyquist rate, its spectrum is repeated in the frequency domain at multiples of the sampling rate f_s . Throughout this presentation the following conventions are used:

F, Ω continuous frequency

f, ω discrete frequency

Let's assume a baseband signal $s(t)$ with a spectral representation $S(F)$.

The bandpass representation can be written as: $s_{BP}(t) = s(t)e^{j2\pi F_o t}$ and

$S_{BP}(F) = S(F - F_o)$ respectively, from the Fourier Transform properties.

By definition, the sampled versions of $s(t)$ and $s_{BP}(t)$ are:

$$s(n) = \frac{1}{2\pi} \int_{-\pi}^{+\pi} S(\omega) e^{j\omega n} d\omega = \int_{-1/2}^{1/2} S(f) e^{j2\pi f n} df \quad (2.2.2)$$

and

$$s_{BP}(n) = \frac{1}{2\pi} \int_{-\pi}^{+\pi} S(\omega - \omega_o) e^{j\omega n} d\omega = \int_{-1/2}^{+1/2} S(f - f_o) e^{j2\pi f n} df \quad (2.2.3)$$

Also,

$$s_{BP}(n) \equiv s_{BP}(nT) = \int_{-\infty}^{+\infty} S(F - F_o) e^{j2\pi n F / F_s} dF \quad (2.2.4)$$

$$\text{since } t = nT = \frac{n}{F_s}.$$

From (2.2.3) and (2.2.4) we have,

$$\int_{-1/2}^{+1/2} S(f - f_o) e^{j2\pi f n} df = \int_{-\infty}^{+\infty} S(F - F_o) e^{j2\pi n F / F_s} dF \quad (2.2.5)$$

The discrete frequency is $f = \frac{F}{F_s}$ and (2.2.3) can be written as

$$\begin{aligned} \int_{-1/2}^{1/2} S(f - f_o) e^{j2\pi f n} df &= \frac{1}{F_s} \int_{-F_s/2}^{+F_s/2} S\left(\frac{F - F_o}{F_s}\right) e^{j2\pi n F / F_s} dF \\ &= \int_{-\infty}^{+\infty} S(F - F_o) e^{j2\pi n F / F_s} dF \end{aligned} \quad (2.2.6)$$

The last equation can be written in a different way. Instead of having one integral from $-\infty$ to $+\infty$, we can have a sum of smaller integrals over a range of F_s .

$$\int_{-\infty}^{+\infty} S(F - F_o) e^{j2\pi n F / F_s} dF = \sum_{k=-\infty}^{+\infty} \int_{(k-1/2)F_s}^{(k+1/2)F_s} S(F - F_o) e^{j2\pi n F / F_s} dF \quad (2.2.7)$$

From (2.2.6) and (2.2.7) we see that $S(F)$ (spectrum of $s(t)$) in the interval $(k-1/2)F_s$ to $(k+1/2)F_s$ is identical to $S(F-kF_s)$ in the interval $-F_s/2$ to $F_s/2$. Hence,

$$\begin{aligned} \sum_{k=-\infty}^{+\infty} \int_{(k-1/2)F_s}^{(k+1/2)F_s} S(F-F_o) e^{j2\pi nF/F_s} dF &= \sum_{k=-\infty}^{+\infty} \int_{-F_s/2}^{+F_s/2} S((F-F_o)-kF_s) e^{j2\pi nF/F_s} dF \\ &= \int_{-F_s/2}^{+F_s/2} \left[\sum_{k=-\infty}^{\infty} S((F-F_o)-kF_s) \right] e^{j2\pi nF/F_s} dF \quad (2.2.8) \end{aligned}$$

Equations (2.2.6), (2.2.7) and (2.2.8) yield

$$\begin{aligned} S\left(\frac{F-F_o}{F_s}\right) &= F_s \sum_{k=-\infty}^{\infty} S((F-F_o)-kF_s) \text{ or,} \\ S(f-f_o) &= F_s \sum_{k=-\infty}^{\infty} S[(f-f_o)-kF_s] \quad (2.2.9) \end{aligned}$$

The last equation shows clearly that the spectrum of a bandpass signal sampled at a rate lower than twice its maximum frequency is repeated periodically in the frequency domain.

2.3 Sampling Frequency Allocation in Undersampling Scenario

Suppose we have a bandlimited signal of bandwidth B centered at frequency F_O . The choice of sampling frequency F_S depends on B and F_O . After sampling, F_O will be translated to F_{IF} , which is in the first Nyquist zone. From Nyquist theory we know that:

$$F_{IF} > \frac{B}{2}$$

Folding can be avoided if:

$$F_{IF} + \frac{B}{2} < \frac{F_S}{2}$$

If these two conditions are met, a signal can be sampled at a rate lower than twice its maximum frequency but higher than its bandwidth. Bandpass sampling is depicted in Fig. 2.1, where aliasing triangles are repeated every F_S . The signal band has to fall in the range:

$$\left[(n+1)\frac{F_S}{2}, n\frac{F_S}{2} \right] \text{ or } \left[n\frac{F_S}{2}, (n+1)\frac{F_S}{2} \right], n \in \mathbb{Z}$$

Figure 2.1: Bandpass sampling aliasing zones.

When the signal is spread over two or more Nyquist zones, folding occurs and information is lost. Sampling with and without folding is shown in Fig. 2.2.

Figure 2.2: Examples of bandpass sampling (a) without folding and (b) with folding.

Mathematically the conditions can be summarized in the following algorithm [4]:

$$\text{If } \text{fix}\left(\frac{F_o}{\frac{F_s}{2}}\right) \text{ is even then } f_{IF} = \text{rem}(F_o, F_s)$$

else (odd) $f_{IF} = F_s - \text{rem}(F_o, F_s)$,

where $\text{fix}(x)$ gives the truncated part of x and $\text{rem}(F_o, F_s)$ gives the remainder of F_o/F_s .

The implementation of this algorithm in Matlab can be found in Appendix A. For CDMA Band Class 1 (1850-1910 MHz), all the valid frequencies between $2 \times B = 120\text{MHz}$ and 300MHz are shown in Fig. 2.3.

Figure 2.3: Allowable sampling frequencies for CDMA Band Class 1.

The first possible sampling frequency is $F_s=132$ MS/s.

It must be noted that the frequencies shown above correspond to a receiver that accommodates the full receive band (e.g. 60 MHz). Alternative designs are possible with smaller receive bandwidths and F_s obviously will vary. The choice of bandwidth and consequently F_s is related to the RF preselect filter. Selectivity and roll-off are important in the final decision. For example, if $B=60$ MHz and $F_s=132$ MS/s we need a filter with sharp roll-off since the edge of the Nyquist zone is 1 MHz off the signal bandwidth. Such stiff requirements are needless if F_s is higher e.g. $F_s=202$ MHz. A state-of-the-art conventional preselect filter would hardly meet the selectivity requirement. Typical

cavity resonator filters used in basestations provide 2dB/100KHz of attenuation. A High Temperature Superconductive (HTS) filter however, can have steeper characteristic and satisfy the requirement. Selectivity in HTS filters can be as high as 20dB/100KHz [5], having approximately 70-90 dB minimum at 1 MHz offset from the Nyquist zone edge [6]. If a cryogenic LNA is collocated with the filter, further reduction of sensitivity is possible as will be shown in Section 2.4.

The input bandwidth of the ADC is also a concern. Even when the ADC operates under bandpass sampling scheme, its analog input bandwidth must be larger than the input signal frequency. Consequently, one downconversion stage may not be avoided in the end.

2.4 General Specifications for Direct Sampling Receivers

For basestation application, an ADC must meet certain specifications derived from wireless standards such as IS-95 and 3GPP2 to enable the direct sampling receiver. A typical circuit of this kind would comprise an antenna, a Band-Pass Filter (BPF), a LNA and a second optional BPF, as shown in Fig. 2.4.

Figure 2.4: RF Frontend of a direct sampling receiver.

One can investigate required performance under a spread spectrum system e.g. IS-95. Minimum performance of a Base Station receiver is described in TIA/EIA-97-D, which covers the recommended minimum performance standards for Base Stations supporting dual mode spread spectrum systems [7]. The band of interest is the CDMA Band Class 1 ranging from 1850 to 1910 MHz. The received signal must have a Frame Error Rate (FER) less than 1% with 95% confidence. This corresponds to an equivalent output SNR of $E_b/N_o = 6.7\text{dB}$. The data rate is at 9.6 Kbps and the Equivalent Noise Bandwidth (ENBW) equals the channel bandwidth $ENBW = 1.2288\text{ MHz}$. The Processing Gain (PG) in a spread spectrum system is defined as the ratio between the chip rate and the data rate:

$$\text{Processing Gain} = 10\log\left(\frac{\text{ChipRate}}{\text{DataRate}}\right) = 10\log\left(\frac{1.2288 \cdot 10^6}{9600}\right) = 21\text{dB}$$

At this point, one has to select the bandwidth of the system. The full receive bandwidth is $B = 1910 - 1850 = 60\text{MHz}$ and if the BPF bandwidth equals this, then all channels are selected and the cost is minimized. However, this results in increasing the system noise power. The thermal noise power N at the antenna input becomes:

$$N_{ant} = kTB = -174\text{dBm/Hz} + 10\log(60 \cdot 10^6) = -96.2\text{dBm}$$

According to the standard, the maximum receiver sensitivity is $S_r = -119\text{ dBm}$ across the ENBW of 1.2288MHz or -179.9 dBm/Hz for Spreading Rate=1.

For the given sensitivity, the receiver NF can be derived by the following expression:

$$\frac{E_b}{N_o} = S_r - 10\log(kT) - NF + PG + DG$$

where DG is the antenna diversity gain, k is Boltzmann's constant ($=1.38 \times 10^{-23}\text{ J/K}$) and $T = 20^\circ\text{C}$ or 293K .

As stated earlier, $E_b / N_o \geq 6.7\text{dB}$ and $PG = 21\text{dB}$. Assuming $DG=0$, NF is:

$$6.7\text{dB} \leq -179.9\text{dBm/Hz} - (-173.9\text{dBm/Hz}) - NF + 21\text{dB} \text{ or}$$

$$NF \leq 8.3\text{dB}$$

Typical basestations have the advantage of antenna diversity that increases received signal power by combining non-fading signals [8]. Diversity Gain in such basestations is

$$DG = 2.4\text{dB}$$

Therefore, the NF specification in a receiver becomes:

$$NF \leq 10.7\text{dB}$$

The signal is below the noise floor in a spread spectrum signal. In order to be sampled and digitized by the ADC, the signal power has to be raised at least to the noise floor of the ADC. We can assume that the only source of noise in the ADC is quantization noise

(P_{QN}). Practically, P_{QN} needs to be several dB below thermal noise in such a way that it has negligible contribution to the overall NF. In the following calculations, P_{QN} is kept 15 dB below noise floor.

A 16-bit superconductive ADC would have $P_{QN} = -80.13$ dBm, as shown previously. For a receive bandwidth of 60 MHz, the analog gain G_{RF} that ensures P_{QN} adds less than 0.2 dB to the total noise is:

$$-174 \text{ dBm/Hz} + G_{RF} + NF_{RF} = -161.34 \text{ dBm/Hz} + 15 \text{ dB or}$$

$$G_{RF} = 27.66 \text{ dB} - NF_{RF}$$

For a typical receiver at room temperature with $NF_{RF} \leq 2 \text{ dB}$, the analog frontend amplifies by $G_{RF} = 25.66 \text{ dB}$. A receiver employing a cryogenic filter/LNA structure [9], [10] can have $NF_{RF} \leq 1.3 \text{ dB}$ with low HTS filter insertion loss of 0.3 dB, thus $G_{RF} = 26.36 \text{ dB}$.

This amount of gain corresponds to the minimum IS-97D requirements regarding sensitivity. Better sensitivity values are feasible for lower NF, provided P_{QN} stays at low levels. It may seem desirable to relax P_{QN} requirements (i.e. ENOB) with higher NF, but the performance would degrade since designers aim at lower sensitivity. Low sensitivity basestations allow for greater cell coverage at reduced cost. Therefore, the gain stage must be chosen such that maximum amplification is applied to the signal. However, there are trade-offs between gain-NF and gain-linearity that must be taken into consideration for the optimization.

Calculations for a CDMA direct RF sampling receiver can be summarized in Table 2.2.

Table 2.2: Software Radio Receiver Budget.

Software Radio Rx Budget for CDMA applications			
Signal bandwidth	1.23	[MHz]	
Modem data rate	9.60	[kbps]	
Sensitivity	-119.00	[dBm]	
Sensitivity over signal bandwidth	-179.89	[dBm/Hz]	
Eb/No requirements	6.70	[dB]	
Rx band	1850.00	[MHz]	
	1910.00	[MHz]	
Sampling frequency	132.00	[MS/s]	
Nyquist zone of operation	14.00		
A/D bits of resolution	16.00	[bits]	
A/D SNR	98.08	[dB]	
Quantization noise	-80.13	[dBm]	
Quantization noise density	-161.34	[dBm/Hz]	
RF Frontend Input Bandwidth	60.00	[MHz]	
Thermal noise @ antenna	-96.22	[dBm]	
SNR @ antenna	-5.89	[dB]	(due to thermal noise across the signal BW)
Antenna Diversity Gain	2.40	[dB]	
Processing Gain	21.07	[dB]	(1.2288Mc/s signal --> 9.6kbps data rate)
Receiver Noise Figure	10.78	[dB]	
RF block gain & Noise figure			
Rx filter noise figure	0.30	[dB]	(typ. For HTS filter)
RF block Noise Figure	1.30	[dB]	(typ. At cryogenic temp.)
RF block gain	26.26	[dB]	
LNA gain	26.56	[dB]	

One of the most important aspects of the system is the single tone desensitization requirement, as it dictates the dynamic range and selectivity of the receiver. It describes the receiver capability of operating in the presence of a high power signal (blocker). The continuous wave (CW) blocker should not saturate the ADC, as no valid conversion would be possible. In a superheterodyne receiver, blocking signals are rejected by successive filtering stages and the high selectivity of the design ensures that the ADC is not subject to this interference. In a direct RF sampling however, that filtering is minimal across a wide frequency range, the ADC must handle the interferer. Specifically, [7] states that $FER < 1\%$ with 95% confidence ($SR=1$ or $SR=3$) when the interferer is at 1.25 MHz offset from the desired signal and its power $P=80$ dB above the signal of interest. This is illustrated in Fig. 2.5 where the blocker is located at a lower frequency than the band of interest. Blocker power at the antenna is 80 dB above the sensitivity.

Figure 2.5: Single Tone Desensitization.

The required SNR can be calculated:

$$P_{bl} = -119dBm + 80dB = -39dBm$$

This is the rms value of the blocker. The peak level is 3 dB higher:

$$P_{bl} = -39dBm + 3dB = -36dBm$$

To avoid clipping at the ADC, saturation power must be at least (3 dB headroom):

$$P_{ADC} = P_{bl} + G_{RF} = -36dBm + 26.36dB + 3dB = -6.64dBm$$

For the 16-bit ADC presented previously with $P_{QN} = -80.13dBm$:

$$SNR_{ADC} = P_{ADC} - P_{QN} = -6.64dBm - (-80.13dBm) = 73.49dB \text{ or}$$

$$ENOB = 12$$

If the interference signal is not a sinusoid, the peak-to-rms ratio can be higher than 3 dB.

For a IS-95 reverse link signal the crest factor is 6 dB whereas for a 1xRTT reverse link signal it is 9 dB. Therefore,

$$SNR_{ADC} = 73.49dB + 6dB = 79.49dB \text{ or}$$

$$ENOB = 13$$

In addition, spurious signals generated by the ADC must be 25 dB below noise floor or 10 dB below quantization noise.

$$SFDR = 0dBm - (-P_{QN} - 10dB) = 90.13dB$$

Except for the single tone desensitization requirement, a receiver must be able to handle two out of band blockers. The two-tone desensitization test relates to the linearity of the ADC in a direct RF sampling receiver. In the presence of two tones, 3rd order intermodulation products are generated due to the nonlinearity of the device. According to [7], the BS receiver has to operate in the presence of the interference tones presented in

Table 2.3. The offset frequencies are measured from the center of the channel band.

For $SR=1$ the spur is located in band at $f = 2 \times f_2 - f_1 = 2 \times 1.25 - 2.05 = 0.45 \text{ MHz}$. For

$SR=3$ we get $f = 2 \times f_2 - f_1 = 2 \times 2.5 - 3.3 = 1.7 \text{ MHz}$. These are the offset frequencies from the center of the band.

Applying the same method for the calculation of interferer power as in the single tone case, blocker powers $P_{bl,1}$ and $P_{bl,2}$ are:

$$P_{bl,1} = P_{bl,2} = -46 \text{ dBm}$$

All 3rd order products must be 10 dB below quantization noise, therefore

$$P_3 = -80.13 \text{ dBm} - 10 \text{ dB} = -90.13 \text{ dBm}$$

which means that spurs must be

$$P_{bl,1} - P_3 = -46 \text{ dBm} + 90.13 \text{ dBm} = 44.13 \text{ dB} \text{ below blocker power. This requirement can be}$$

tested in a two-tone test of the ADC.

Table 2.3: Two Tone Desensitization Test Case.

Interferer Frequency (MHz)	Interferer Power (dB)	Spreading Rate (SR)
1 st Tone @ $ f-f_0 = 1.25$	70	1
2 nd Tone @ $ f-f_0 = 2.05$	70	1
1 st Tone @ $ f-f_0 = 2.50$	70	3
2 nd Tone @ $ f-f_0 = 3.30$	70	3

2.5 Clock Jitter Requirements for Wideband Radio

Another key factor in Analog-to-Digital Conversion is the clock that drives the ADC. The spectral purity of the clock plays an important role in the performance of high frequency data sampling and wideband radio systems because it contributes to the total noise power. Noise is described mostly in the time domain as clock jitter, another way of expressing phase noise. Other terms can be found in literature such as aperture uncertainty, aperture jitter and clock uncertainty. In sampling systems, jitter becomes significant when the sampling rate increases and high resolution is necessary. Requirements regarding jitter performance in wideband radio can be extracted after the jitter effect is quantified.

Figure 2.6: Clock jitter of a sampling system.

The concept of clock jitter is better illustrated in Fig. 2.6. In an ideal sampling system the sampling instants are equally spaced in the time domain. Every T_s sec an analog sample is taken and converted to a digital word. In the presence of jitter, the intervals between the sampling points are not equal. The uncertainty between each sampling point is the

clock jitter. Jitter is a random process and treated in statistical terms such as the standard deviation σ .

There are various definitions of jitter depending on the way it is measured. These include period, cycle, cycle-to-cycle, accumulated and long-term jitter. Each of them can be expressed in terms of rms (σ), 3-sigma (3σ), peak and peak-to-peak value. The most widely used definitions are:

- Period jitter: the time variation between consecutive clock edges. It is a measure of the time displacement of one clock edge relative to the preceding edge.
- Accumulated jitter: the elapsed time between a triggering clock event and a certain edge of the clock. Obviously, it is a function of the number of periods between the two events.
- Long-term jitter: the limit value of the accumulated jitter for a large number of clock pulses.

Each of the above is usually expressed in terms of rms value.

The impact of jitter on a sampling system can be evaluated by a simple approximation found widely in literature [11]. Let's assume a perfect sinusoid

$$x(t) = A \sin(2\pi ft)$$

If the sampling rate f_s is much higher than f (oversampling) we can assume that the signal is piecewise linear between two sampling instants. The rate of change is given by the slew rate, which represents how fast the signal varies (Fig. 2.7). The slew rate is

$$\frac{dx}{dt} = \frac{d}{dt}(A \sin(2\pi ft)) = A2\pi f \cos(2\pi ft) \quad (2.5.1)$$

It is maximum at the zero crossings of the sinewave or,

$$\left. \frac{dx}{dt} \right|_{\max} = \left. \frac{dx}{dt} \right|_{t=0} = A2\pi f \quad (2.5.2)$$

The resulting error voltage caused by the uncertainty in the clock pulse is [12], [13]:

$$e_j(kT_s) = y(kT_s) - x(kT_s) = (\text{SlewRate}) \cdot \sigma_{ij}$$

or,

$$e_j(kT_s) = \left. \frac{dx}{dt} \right|_{rms} \cdot \sigma_{ij} = \sqrt{\frac{1}{T} \int_0^T \left(\frac{dx}{dt} \right)^2 dt} \cdot \sigma_{ij} = \sqrt{2\pi} f A \sigma_{ij}$$

where $T=1/f$.

Consequently the SNR of the sampling system is

$$SNR = 10 \log \left(\frac{\text{SignalPower}}{\text{NoisePower}} \right) = 10 \log \left(\frac{\left(\frac{A}{\sqrt{2}} \right)^2}{(\sqrt{2\pi} f A \sigma_{ij})^2} \right)$$

$$SNR = 20 \log \left(\frac{1}{2\pi f \sigma_{ij}} \right) \quad (2.5.3)$$

It should be noted that σ_{ij} is the rms value of jitter. The last expression is well known as an approximation of the SNR in sampling systems.

Figure 2.7: Error voltage induced by time jitter.

A general expression can be found if more effects are taken into consideration.

Including thermal noise and differential nonlinearity, we have [11]:

$$SNR = -10 \log \left[(2\pi f \sigma_{ij})^2 + \left(\frac{1+\varepsilon}{2^N} \right)^2 + \left(\frac{V_{noise}}{2^N} \right)^2 \right] \quad (2.5.4)$$

where N is the Number of Bits, ε the average Differential NonLinearity of the converter (e.g. 0.5 LSB), and V_{noise} the thermal noise in LSBs.

Equation (2.5.3) is the upper limit of SNR because in a real system more effects will limit its performance, such as internally generated noise and nonlinearities. The plot of the SNR vs. analog input frequency for different values of jitter based on (2.5.3) is shown in Fig. 2.8, which gives an insight into the clock requirement for an IF sampling receiver.

Figure 2.8: SNR vs. input frequency of a sampling system with jitter based on (2.5.3).

For example, if the requirement is $SNR > 79.49 \text{ dB}$ at $f = 1850 \text{ MHz}$, as derived before, we need $\sigma_{ij} < 9.12 \text{ fs}$ rms. Therefore, a low jitter clock is needed, making the design of the receiver a challenging task. The Matlab code simulating the theoretical SNR equation (2.5.3) can be found in Appendix A.

Since the clock is a PLL circuit, the corresponding phase noise characteristic (phase noise mask) must be determined. The relation between the clock time jitter $\sigma_{ij}^2 \text{ (sec}^2\text{)}$ and the clock phase noise $\sigma_\phi^2 \text{ (rad}^2\text{)}$ is provided below.

The equation relating these two physical quantities is:

$$\sigma_\phi^2 = \omega_{clk}^2 \sigma_{ij}^2 \quad (2.5.5)$$

as can be easily seen if the time domain equation of a phase modulated signal is written:

$$\begin{aligned} V(t) &= A \cos(\omega t + \phi(t)) \\ &= A \cos[\omega(t + t_j(t))] \end{aligned} \quad (2.5.6)$$

Hence, the rms values of phase and time components can be expressed in the form:

$$\sigma_\phi = \omega \sigma_{ij}$$

$$\text{or } \sigma_\phi^2 = \omega_{clk}^2 \sigma_{ij}^2$$

Using the approximation of Fig. 2.6, the output signal $y(t)$ can be approximated in a first order Taylor series.

$$y(kT_s) = x(kT_s) + \frac{d}{dt}(x(kT_s))t_j(kT_s) = x(kT_s) + x'(kT_s)t_j(kT_s) \quad (2.5.7)$$

The difference between the approximated signal $y(t)$ and the real signal $x(t)$ is

$$e_j(kT_s) = y(kT_s) - x(kT_s) = x'(kT_s)t_j(kT_s) \quad (2.5.8)$$

It is known in signal theory that the average power of a stationary random signal is given by the autocorrelation function evaluated at zero shift in the time origin.

$$E[x^2(t)] = \sigma_x^2 = r_{xx}(0) = \int_{-\infty}^{+\infty} S_x(f) df$$

with $r_{xx}(\tau) = E[x(t)x(t+\tau)]$ and $S_x(f)$ the Power Spectral Density (PSD) of the signal.

The autocorrelation function $r_y(mT_s)$ of the discrete sampled signal y is by definition

$$r_y(mT_s) = E[y(kT_s + mT_s)y(kT_s)] \quad (2.5.9)$$

where $E(.)$ is the expected value.

Substituting (2.5.7) in (2.5.9)

$$r_y(mT_s) = r_x(mT_s) + r_{x'}(mT_s) \cdot r_{ij}(mT_s) \quad (2.5.10)$$

A proof of (2.5.10) can be found in Appendix B1.

The autocorrelation function of the first derivative has the following property as shown in [14] and Appendix B1:

$$r_{x'}(mT_s) = -r_x''(mT_s) \quad (2.5.11)$$

Equations (2.5.8), (2.5.10) become

$$r_y(mT_s) = r_x(mT_s) - r_x''(mT_s) \cdot r_{ij}(mT_s) \quad (2.5.12)$$

$$r_{ej}(mT_s) = -r_x''(mT_s) \cdot r_{ij}(mT_s) \quad (2.5.13)$$

The Fourier Transform of (2.5.12) gives an equation describing the relationship between the output signal power spectral density, $S_y(f)$, the input signal power spectral density, $S_x(f)$, and the random jitter power spectral density $S_{ij}(f)$

$$S_y(f) = S_x(f) + [(2\pi f)^2 S_x(f)] * S_{ij}(f) \quad (2.5.14)$$

because the multiplication in time domain is equivalent to convolution in the frequency domain and vice versa.

Although (2.5.14) contains the two inputs and the output of a sampling system it is not very useful in the calculation of SNR. Instead, it is more practical to derive an expression in the time domain. Knowing that the power equals the autocorrelation at zero we get

$$SNR = 10 \log \left(\frac{r_x(0)}{-r_x''(0) \cdot r_{ij}(0)} \right) \quad (2.5.15)$$

The SNR of a sampling system is inversely proportional to the second derivative of the autocorrelation function and the jitter total average power or variance ($r_{ij}(0) = \sigma_{ij}^2$ because $\mu_{ij} = 0$). Thus, it is independent of the clock phase noise profile as long as its total average power remains constant. This makes the simulation of communication systems in the presence of ADCs less complicated since we can first select noise power levels that meet requirements and then translate them to phase noise masks.

Equation (2.5.15) shows another interesting property of the sampler. The autocorrelation function of low frequency signals is approximately flat around zero. Consequently, the second derivative takes small values and the SNR increases. On the other hand, high frequency signals are more susceptible to jitter and have lower SNR due to high autocorrelation function slope.

Three examples below illustrate the efficiency of (2.5.15) in calculating SNR [11]. The first example shows another way of finding the SNR of a sinusoidal input and the result is the same as in (2.5.3). In the second example, the input is a baseband random signal with flat power spectrum as depicted in Fig. 2.9. In the last example, the input has raised cosine power spectral density.

Figure 2.9: Rectangular power spectrum.

The power spectral density can be written as:

$$S_x(f) = \text{rect}\left(\frac{f}{2f_c}\right) \quad (2.5.16)$$

Applying the SNR formula yields

$$SNR = 10 \cdot \log\left(\frac{3}{\omega_c^2 \cdot \sigma_{ij}^2}\right) \quad (2.5.17)$$

If the signal is bandpass the SNR formula becomes

$$SNR = 10 \cdot \log\left(\frac{1}{\sigma_{ij}^2 \left(f_o^2 + \frac{BW^2}{12}\right)}\right) \quad (2.5.18)$$

where f_o is the carrier frequency and $BW=2f_c$.

A proof of (2.5.17) and (2.5.18) can be found in Appendix B.

In a more practical scenario of an IS-95 system, data undergo raised cosine pulse shaping.

Generally, a square root raised cosine filter is used in the transmitter and another one in the receiver. As shown in Appendix B, when the sampled signal has raised cosine PSD and (2.5.15) can be applied.

The SNR of a signal with baseband raised cosine PSD is

$$SNR = 10 \log \left(\frac{1}{\left(\frac{\omega_b^2}{12} + W^2(\pi^2 - 8) \right) \sigma_{ij}^2} \right) \quad (2.5.19)$$

When the signal is modulated on carrier f_o we have a bandpass raised cosine PSD with the following SNR

$$SNR = 10 \log \left(\frac{1}{\left(\frac{\omega_b^2}{12} + W^2(\pi^2 - 8) + \omega_o^2 \right) \sigma_{ij}^2} \right) \quad (2.5.20)$$

The proof of (2.5.19) and (2.5.20) is provided in Appendix B.

Chapter 3

Clock Jitter and ADC Performance

3.1 Limitations of Sampling Systems

Clock jitter plays a major role in the performance of a wideband radio receiver, as previously advocated. A theoretical approach to the jitter effect on a generic sampling system in terms of SNR was shown. In wideband radio systems however, design gets more complicated in consideration of the spectrum characteristics of the information signal and the sampling scheme (e.g. undersampling).

For the system of interest, i.e. IS-95, the modulation scheme is OQPSK and the baseband signal is shaped with root-raised cosine filters. Apparently, the clock jitter impact on the received signal is related to the spectrum distribution. This holds in the case of baseband signals sampled at rates higher than the Nyquist rate. For signals modulated on a carrier, the frequency plays the most important role in the SNR degradation. As will be shown in this chapter, the effect of jitter on signals having different modulation schemes but positioned at the same frequency can be approximated by the same formula under the same sampling scheme.

Different sampling scenarios change the behavior of the system against jitter. First, performance is degraded with increasing frequency according to the SNR formula of lowpass sampling:

$$SNR = 6.02B + 1.76 + 10 \log \left(\frac{f_s}{2f_{\max}} \right) \text{ (dB)}$$

For the undersampling scenario, the SNR is degraded by the ratio of clock to signal frequency. The higher the ratio the less likely the receiver is to meet the requirements. For a given SNR, the total noise power in the band of interest can be calculated. This number can be used to find the maximum noise caused by the clock source e.g. a PLL circuit. The PLL phase noise must be chosen based on this assessment.

The relationship between time jitter and phase noise power was shown in (2.5.5) to be:

$$\sigma_{\phi}^2 = \omega_{clk}^2 \sigma_{ij}^2$$

or in terms of total average power

$$S_{ij}(f) = \frac{1}{\omega_{clk}^2} S_{\phi}(f) \quad (3.1.1)$$

Substituting (2.5.5) in the basic SNR formula (2.5.3) we get:

$$SNR = \left(\frac{\omega_{clk}}{\sigma_{\phi} \omega_{sig}} \right)^2 \quad (3.1.2)$$

or

$$SNR = 20 \cdot \log \left(\frac{\omega_{clk}}{\sigma_{\phi} \omega_{sig}} \right) \text{ (dB)}$$

Equation (3.1.2) shows that when the analog signal is sampled, the SNR is not only dependent on phase noise σ_ϕ , but on the ratio of clock to signal frequency as well. An undersampling system would perform worse than an oversampling one despite having the same ADC clock. The choice of Nyquist zone for undersampling is limited by the total noise in the band. A receiver where the signal would be digitally downconverted from RF would be impractical even for the state of the art oscillator performance.

This was clearly demonstrated in Chapter 2 for the case of a signal at $f=1850$ MHz. The clock jitter using (2.5.3) must be $\sigma_{tj}=9.12$ fs (*rms*) in order to have minimum $SNR=79.49$ dB. Inversely, (3.1.2) can provide the required sampling rate under bandpass sampling for a given SNR. For the same SNR and typical clock phase noise of $\sigma_\phi=0.01$ mrad *rms*, the clock frequency can be

$$SNR = 20 \cdot \log \left(\frac{\omega_{clk}}{\sigma_\phi \omega_{sig}} \right) \text{ or}$$

$$f_{clk} = 10^{7.949/2} \cdot 10^{-5} \cdot 1.85 \cdot 10^9 \text{ or}$$

$$f_{clk} = 174.5 \text{ MHz}$$

A valid sampling frequency for CDMA Band Class 1 is $f_s=192$ MS/s. A sample phase noise power calculation from phase noise data giving $\sigma_\phi=0.01$ mrad *rms* can be found in Appendix C.

3.2 Signal-to-Noise Ratio Performance of Sampling Systems

The relationship between SNR and clock jitter was shown in Chapter 2 for three different cases. Specifically, theoretical equations were derived for a single sinusoid, a signal having flat power spectral density and a signal with raised cosine power spectral density. For the flat and raised cosine PSD, equations were derived both for baseband and bandpass spectrum. Equations (2.5.3), (2.5.17), (2.5.18), (2.5.19) and (2.5.20) are repeated below for convenience

$$SNR = 10 \cdot \log \left(\frac{1}{4\pi^2 f_o^2 \sigma_{ij}^2} \right) \text{ sinusoid} \quad (3.2.1)$$

$$SNR = 10 \cdot \log \left(\frac{3}{4\pi^2 f_c^2 \sigma_{ij}^2} \right) \text{ rectangular PSD baseband} \quad (3.2.2)$$

$$SNR = 10 \cdot \log \left(\frac{1}{4\pi^2 \sigma_{ij}^2 \left(f_o^2 + \frac{BW^2}{12} \right)} \right) \text{ rectangular PSD bandpass} \quad (3.2.3)$$

$$SNR = 10 \cdot \log \left(\frac{1}{\left(\frac{\omega_b^2}{12} + W^2(\pi^2 - 8) \right) \sigma_{ij}^2} \right) \text{ raised cosine PSD baseband} \quad (3.2.4)$$

$$SNR = 10 \cdot \log \left(\frac{1}{\left(\frac{\omega_b^2}{12} + W^2(\pi^2 - 8) + \omega_o^2 \right) \sigma_{ij}^2} \right) \text{ raised cosine PSD bandpass} \quad (3.2.5)$$

where σ_{tj} is the rms value of clock jitter, f_0 the carrier frequency, f_c the cutoff frequency of the baseband signal, BW the bandwidth of the signal centered at f_0 , ω_b the oversampling frequency of the root raised cosine filter and $W = 1/2T_b$.

All three systems were simulated in Matlab Simulink and mathematical formulas were evaluated with satisfactory accuracy. The sampling system used is not a full ADC model but a Sample-and-Hold block. The purpose of the simulations is to demonstrate the effect of jitter on baseband and bandpass signals under oversampling scenario but not to investigate the behavior of a specific type of ADC. In such a case, the SNR would depend on the architecture of the ADC and the interface between the clock and the device. Another assumption governs the sampling scheme. Equations (3.2.1)-(3.2.5) are derived under the simplification that the oversampling ratio f_s/f_0 is so high that the duration of the sampling pulse is negligible compared to the signal period T . In reality, this does not hold although simulation results converge to the theoretical values.

3.2.1 Single Sinusoid

A simulation testbed was first developed for the simple case of a sinewave signal sampled with a high frequency clock. The model is depicted in Fig. 3.1. The signal is generated in the “Sinewave” block and processed through “Sample & Hold”. Two discrete S&H blocks exist in the design but are clocked from different sources: a noiseless clock for the upper path and a jittered clock for the lower path. Calculation of SNR is carried out by calculating the signal and noise powers in the time domain.

Signal power is found by calculating the power of the noiseless sampled signal (upper path). If this signal is subtracted from the jittered sampled signal (lower path), the difference equals the error due to jitter. The error power equals total noise power. The only source of noise in the system is jitter from the “Clock with Jitter” block. Consequently, subtracting noise from signal power yields the SNR due to clock jitter.

The power calculation is performed by the variance block. It calculates the variance y of the input vector u of length M according to the following formula:

$$y = \sigma^2 = \frac{\sum_{i=1}^M |u_i - \mu|^2}{M - 1}$$

where μ is the mean value of the input signal.

The signal and noise powers are converted in dB before calculating the SNR. Apart from time domain calculation, SNR was also calculated in the frequency domain by performing a FFT on the two signals. Results were identical as in the time domain.

The clock is a square wave generator with variable period duration. This block is available in [15] and few modifications were made to the initial design. As can be seen in Fig. 3.2, random Gaussian noise modulates a sinewave generator, which is hard-limited by a hysteresis loop block. Jitter variance is one of the variables of the “Clock with Jitter” block and is expressed in terms of Peak Percent Jitter (PPJ), or $\sigma_{ij} / 3$ (%):

$$\sigma_{ij}^2 = \left(\frac{PPJ}{300 \cdot f_{clk}} \right)^2 \quad (3.2.6)$$

The factor of 3 implies that the 3σ definition of jitter is used.

Figure 3.1: MATLAB model for sampling system of a sinewave signal.

The jitter definition of (3.2.6) is consistent with the relationship between time jitter and phase noise described in (2.5.5). Indeed, the output of the sinewave block is:

$$\begin{aligned}
 y(t) &= \sin(2\pi f_{clk}(t + \Delta t)) \\
 &= \sin(2\pi f_{clk}t + 2\pi f_{clk}\Delta t) \\
 &= \sin(2\pi f_{clk}t + \Delta\phi)
 \end{aligned}$$

$$\text{where } \text{Var}[\Delta t] = \sigma_{tj}^2 = \left(\frac{PPJ}{3 \cdot 100 \cdot f_{clk}} \right)^2$$

$$\text{and } \text{Var}[\Delta\phi] = \sigma_{\phi}^2 = (2\pi f_{clk})^2 \left(\frac{PPJ}{3 \cdot 100 \cdot f_{clk}} \right)^2 = \left(\frac{2\pi}{3} \frac{PPJ}{100} \right)^2$$

or

$$\sigma_{\phi}^2 = \omega_{clk}^2 \sigma_{tj}^2 \quad (3.2.7)$$

Dividing the PPJ over f_{clk} ensures that the jitter is scaled with frequency as in a real clock.

Figure 3.2: Model for clock with jitter.

Simulation results are summarized in Table 3.1 for three frequencies of the single tone. The clock frequency was kept constant at $f_{clk}=1000$ Hz and the sampling time of the tool at $\text{SampleTime}=1\text{e-}4$ sec. It is obvious that the simulated SNR approaches the theoretical SNR for high oversampling ratios, as previously explained.

Table 3.1: Simulation results for sampling system of a sinewave signal.

f_o (Hz)	Sample Time (sec)	f_{clk} (Hz)	Jitter Power (sec^2)	SNR Theory (dB)	SNR Simulation (dB)
1	1e-4	1000	1e-10	84.036	84.08
10	1e-4	1000	1e-10	64.036	63.34
100	1e-4	1000	1e-10	44.036	43.01

Sampling the analog signal with the “Sample & Hold” block is essentially a zero-order hold operation with variable hold time. Alternatively, it can be viewed as a filtering operation. The impulse response of S&H is presented in [16] as:

$$h(t) = \begin{cases} 1, & 0 \leq t \leq T_s \\ 0, & \text{otherwise} \end{cases}$$

where T_s is the hold time.

The frequency response is:

$$H(F) = T_s \left(\frac{\sin \pi F T_s}{\pi F T_s} \right) e^{-j\pi F T_s}$$

The frequency response of S&H is plotted in Fig. 3.3. The sampling frequency $1/T_s$ corresponds to the first zero in the magnitude characteristic of $|H(f)|$. Low frequency input signals to the S&H filter are not attenuated as much as those near $1/2T_s = f_s/2$. At $f = f_s/2$ we have 3 dB drop in gain. Throughout simulations, the oversampling ratio was kept high to avoid this loss due to the nature of the S&H block.

Figure 3.3: Frequency response of the S&H system as a linear filter.

3.2.2 White Bandlimited Power Spectral Density

The second Matlab simulation evaluated (3.2.2) and (3.2.3). A signal with flat power spectral density (white noise) is filtered by a 10th-order Butterworth lowpass filter. The cutoff (passband-edge) frequency is $f_c=1/20$ Hz and an approximate flat power spectrum is created. This signal is sampled by two clocks as in the sinusoid simulation case and the SNR is calculated for 2^{15} samples. All frequencies are normalized to clock frequency f_{clk} in order to reduce simulation time. This does not affect simulation results since the ratio between the frequencies remains the same. The simulation model is shown in Fig. 3.4. Simulation results are shown in Table 3.2.

Table 3.2: Simulation results for a baseband signal with flat PSD.

f_c (Hz)	Sample Time (sec)	f_{clk} (Hz)	Jitter Power (sec ²)	SNR Theory (dB)	SNR Simulation (dB)
0.05	1	1	1.778×10^{-4}	52.33	51.18
0.15	1	1	1.778×10^{-4}	42.79	41.66
0.2	1	1	1.778×10^{-4}	40.29	39.08

Simulation numbers correlate with the theoretical equation described before. Any discrepancies can be attributed to the finite sampling frequency f_{clk} and the S&H block. All equations were derived under the assumption that sampling rate f_s is much higher than the maximum frequency of the signal. As f_c increases, the input signal is attenuated because the oversampling ratio is reduced. For $f_c=0.2$, the edge of the spectrum is attenuated by $20 \cdot \log(\text{sinc}(0.2/1)) = -0.5$ dB.

In the bandpass case, the signal is upconverted before being sampled. This is done by multiplying the baseband portion by a cosine signal. The remaining part of the model is identical to the baseband one. This model is illustrated in Fig. 3.5 and simulation results are summarized in Table 3.3. The cut-off frequency of the baseband signal is f_c and the carrier frequency f_0 .

Table 3.3: Simulation results for a bandpass signal with flat PSD.

f_c (Hz)	f_0 (Hz)	Sample Time (sec)	f_{clk} (Hz)	Jitter Power (sec^2)	SNR Theory (dB)	SNR Simulation (dB)
0.05	0.5	1	10	1.78×10^{-6}	47.39	47.87
0.05	1	1	10	1.78×10^{-6}	41.49	41.77
0.4	2	1	15	9.68×10^{-6}	27.51	27.09

Simulation results validate (3.2.3) showing clearly the effect of sampling a bandpass signal. The SNR is mainly determined by the carrier frequency rather than the signal bandwidth.

Figure 3.4: Sampling of a baseband signal with flat PSD.

Figure 3.5: Sampling of a bandpass signal with flat PSD.

3.2.3 Raised Cosine Power Spectral Density

The third simulation testbed covers the raised cosine PSD. Random integers are generated and used as the input to a QPSK baseband modulation block. Data are in NRZ format. The QPSK pulses are shaped with a square root raised cosine filter. The filtered signal has raised cosine PSD. The 'Raised Cosine Interpolator' filter oversamples the input data by a factor of 2. The sampling time of random integer data is $T_d=1$ sec and the output sampling time from the filter is $T_s=1/2$ sec. The SNR is calculated for 2^{15} samples. Any InterSymbol Interference (ISI) between pulses is neglected for this simulation. Simulation results are presented in Table 3.4. The simulation testbed is shown in Fig. 3.6.

Table 3.4: Simulation results for a baseband signal with raised cosine PSD.

f_d (Hz)	f_{ov} (Hz)	f_{clk} (Hz)	a	Jitter Power (sec^2)	SNR Theory (dB)	SNR Simulation (dB)
1	2	10	0.5	1.6×10^{-5}	36.19	36.06
1	2	10	0.22	1.6×10^{-5}	36.64	36.57
1	2	10	0.1	1.6×10^{-5}	36.74	36.85

Data are generated at rate f_d and upsampled at rate f_{ov} by the raised cosine filter-interpolator. The data rate at the S&H input is therefore f_{ov} . Simulation results prove the validity of (3.2.4) with respect to the roll-off factor a . It should be noted that $a=0.22$ is used in IS-95 systems.

Figure 3.6: Sampling of a baseband signal with raised cosine PSD.

A simulation testbed is also developed for a bandpass QPSK signal. The signal is generated in a similar manner to the baseband case but is upconverted at the carrier frequency f_0 by a mixing process. The same parameters are used as in the baseband example. The clock frequency though is $f_{clk}=15$ Hz. Simulation results are presented in Table 3.5. The simulation model is shown in Fig. 3.7.

Table 3.5: Simulation results for a bandpass signal with raised cosine PSD.

f_d (Hz)	f_{ov} (Hz)	f_0 (Hz)	f_{clk} (Hz)	a	Jitter Power (sec ²)	SNR Theory (dB)	SNR Simulation (dB)
1	2	3	15	0.5	6×10^{-6}	26.55	26.17
1	2	4	15	0.5	6×10^{-6}	24.13	22.13
1	2	5	15	0.5	6×10^{-6}	22.23	20.4

Figure 3.7: Sampling of a bandpass signal with raised cosine PSD.

The results in Table 3.5 prove that (3.2.5) is correct and as in the flat PSD case, the SNR is dependent on the carrier frequency. The discrepancy between theoretical and simulated SNR can be attributed to the S&H filtering. For $f_{\text{clk}}=15$ Hz, the signal is attenuated by the sinc characteristic. At $f_0=3, 4, 5$ Hz the attenuation is $20 \cdot \log(\text{sinc}(f/f_{\text{clk}}))$ or $-0.58, -1.1$ and -1.65 dB respectively.

3.3 Clock Requirements in IS-95 Systems

The simulation example of bandpass signals shows clearly that the carrier frequency sets the limits in IF and RF sampling. When the signal bandwidth is small compared to the carrier frequency, its effect can be neglected. The SNR in each case can be approximated by (3.2.1) with sufficient precision, despite the shape of PSD. The impact of the modulation scheme on the SNR is not as important as the carrier frequency to sampling rate ratio is under IF and direct RF sampling scenario.

Apart from the general case when a signal is sampled at IF or RF, it is interesting to see the behavior of the sampling system in the presence of an interferer. Single tone desensitization requirements for wideband radio with respect to dynamic range were derived in Chapter 2. However, a blocker can affect the system performance in another way. The blocker tone acquires the clock phase noise profile and extra noise falls in band. This is because sampling can be viewed as a multiplication or a mixing process. In a similar manner to downconversion when the signal is multiplied by the local oscillator tone, the sampled signal has the spectral characteristics of the clock. This situation is illustrated in Fig. 3.8, where the blocker tone phase noise adds to the total in band noise.

If the SNR requirement is known, we can budget the allowed amount of noise caused by the blocker tone. Let's assume a direct RF sampling receiver with $f_s=132$ MS/s and signal bandwidth $BW = f_H - f_L = (1910-1850)MHz = 60MHz$. The ADC SNR must be at least 79.5 dB according to the theoretical derivation presented in Chapter 2. Substituting (3.2.7) into (3.2.1) and assuming a signal located at the center of the band ($f=1880$ MHz)

$$\sigma_{\phi}^2 = \omega_{clk}^2 \sigma_{ij}^2$$

$$SNR = \frac{1}{4\pi^2 f_o^2 \sigma_{ij}^2} = \frac{\omega_{clk}^2}{4\pi^2 f_o^2 \sigma_{\phi}^2} \text{ or}$$

$$10^{7.95} = \frac{(132 \text{ MS/s})^2}{(1880 \text{ MHz})^2 \sigma_{\phi}^2} \text{ or}$$

$$\sigma_{\phi} = 7.45 \mu\text{rad (rms)}$$

This number represents the required total phase noise power of the LO driving the ADC. It is difficult to achieve such performance from an oscillator using existing technology. A more realistic scenario would include a downconversion stage to relax the phase noise requirement by increasing the scaling factor f_{clk}/f_o . The signal can be downconverted to the third Nyquist zone (134-194 MHz).

Figure 3.8: Degradation of SNR due to blocker phase noise.

The SNR derivation in Chapter 2 yielded $SNR_{ADC}=79.49$ dB measured across $[0, f_s]$ or $[-f_s/2, +f_s/2]$. The quantization noise of the ADC is distributed across this range therefore all power calculations are done for the same frequency interval. The SNR must not be degraded by the phase noise introduced by the blocker. The blocker will have the same phase noise profile as the clock. In the quantization noise case, P_{QN} was kept 15 dB below thermal noise so that its contribution to total noise is less than 0.2 dB. As far as jitter is concerned, the same assumption regarding noise contribution holds (less than 0.2 dB). The allocation to each source of noise is 0.1 dB.

Let's assume the blocker power is $P_{bl}=0$ dBFS. Hence, the total noise in the band is $N_{bl}=-79.49$ dBFS. After the phase noise is added, the SNR becomes $SNR=79.39$ dB or -79.39 dBFS (degradation by 0.1 dB).

Such degradation is met if the phase noise introduced by the blocker is

$$\sigma_{\phi, bl}^2 = -95.8 \text{ dBFS or dBc}$$

$$\text{since } 10^{-79.49/10} + 10^{-95.8/10} = 10^{-79.39/10}$$

For a signal at the center of the band and a blocker at 900KHz offset or $f_{bl}=164$ MHz, the clock phase noise that meets the above requirement can be found.

Equation (3.1.2) can be written as

$$SNR = \left(\frac{1}{\sigma_{\phi}} \right)^2 \left(\frac{f_{clk}}{f_{bl}} \right)^2 \text{ or}$$

$$\sigma_{\phi, bl}^2 = \left(\frac{1}{\sigma_{\phi}} \right)^2 + 10 \log \left(\frac{f_{clk}}{f_{bl}} \right)^2 \text{ or}$$

$$\left(\frac{1}{\sigma_{\phi}} \right)^2 = -95.8 \text{ dBc} - 20 \log \left(\frac{132 \cdot 10^6}{164 \cdot 10^6} \right) \text{ or}$$

$$\left(\frac{1}{\sigma_{\phi}} \right)^2 = -93.61 dBc \text{ or}$$

$$\sigma_{\phi} = 2.086 \cdot 10^{-5} \text{ rad (rms)}$$

The corresponding time jitter is

$$\sigma_{ij} = 20.24 \text{ fs (rms)}$$

The phase noise equation represents the total phase noise allowed for 0.1 dB degradation in SNR by the blocker. For a flat phase noise profile this corresponds to

$$\left(\frac{1}{\sigma_{\phi}} \right)^2 = -154.5 \text{ dBc / Hz across the channel bandwidth of 1.2288 MHz.}$$

The system designer has to choose a clock that satisfies the phase noise requirement. The phase noise power spectral density of the LO should not exceed -154.5 dBc/Hz at 900 KHz offset. In a LO, the phase noise at such offset is dominated by the VCO performance. A typical VCO has -145 dBc/Hz at 100 KHz offset from the carrier [17]. The requirement can be met by raising the clock frequency or relaxing the NF specification. For a specific clock, the total phase noise can be calculated by noise integration in the channel bandwidth.

Chapter 4

Josephson Junction and A/D Converters

4.1 Physical Properties of the Josephson Junction

In the previous chapters, the significance of the ADC in the design of a wideband radio receiver was shown. Dynamic range and linearity set the performance limits of the receiver, as stated in Chapter 2. Apart from the typical semiconductor ADCs, a special type of superconductive device can potentially meet these requirements. The properties of the superconductive material make the technology a candidate for software radio due to its linearity, high switching speed and dynamic range. This chapter deals with the physical properties of a superconductive electronic circuit using the Josephson Junction (JJ) as a switch. The switching logic (Rapid Single Flux Quantum Logic – RSFQ) is described and the superconductive ADC is introduced. The design and fabrication of the ADC studied in this work are also analyzed.

In the semiconductor electronics world the major device is the transistor. On the other hand, in superconductor electronics the most important component is the JJ. The JJ is a two-terminal device of two superconductive materials (Nb - Niobium) separated by a thin insulator layer (Aluminum Oxide - AlO_x). The junction and its circuit symbol are shown in Fig. 4.1.

Figure 4.1: The Josephson Junction.

When the insulating material is placed between the two superconductors interesting phenomena occur. If the thickness of the insulating material is small ($\sim 1\text{nm}$), electron tunneling takes place.

In superconductors, the charge carriers are Cooper pairs, which are described by the BCS (Bardeen, Cooper, Schrieffer) theory of superconductivity. Their formation occurs when the interaction between the electrons and the ionic lattice is strong. A fast moving electron distorts the lattice by attracting positive charged ions. This mechanism creates a positive charge behind the electron. If a second electron is moving in the opposite direction, it is attracted to the positive charge and a weak bound is formed between the two electrons. The first electron transfers its momentum to the lattice in the form of phonon (quantized lattice vibration) emission. The second electron absorbs this phonon thus the momentum is transferred to it. Such a behavior is possible due to the low temperature that reduces thermal phonons. It should be noted that each pair has a total linear momentum, $\vec{p}$, equal to zero and each electron of the pair has opposite spin. A Cooper pair is the result of momentum transfer between two electrons through the emission and absorption of a phonon with the lattice.

The properties of the junction are described through the DC and AC Josephson effects.

4.1.1 DC Josephson Effect

The DC Josephson effect describes the behavior of the JJ when no external voltage is applied to it. The current flowing through the insulating layer depends on the Cooper pairs' phase between the two superconductive materials. Electron pairs in each superconductor are characterized by a wave function, which takes the form

$$\Psi(\vec{r}, t) = |\Psi(\vec{r}, t)| e^{j\left(\Theta(\vec{r}) - \frac{2E_F t}{\hbar}\right)} \quad (4.1.1)$$

where $\Theta(\vec{r})$ is the phase of the wavefunction for each electron pair and E_F the Fermi energy. This energy is the uppermost level occupied at $T=0$ K. If $V=0$, (4.1.1) becomes

$$\Psi(\vec{r}, t) = |\Psi(\vec{r}, t)| e^{j\Theta(\vec{r})} \quad (4.1.2)$$

The wavefunction amplitude of the Cooper pair is constant at $T=0$ (ground state), since the electrons are bound and independent of the crystal lattice potential. The magnitude square is typically defined as the effective Cooper pair density $|\Psi|^2 = n_s$. In addition, the phase can be considered coherent between the electrons such that (4.1.2) is valid over the whole superconductor. If the two superconductors are close enough (Fig. 4.1), the wavefunctions of each material can penetrate the barrier. The coupling energy increases and when it exceeds thermal fluctuation energy, the phases become locked and Cooper pairs can flow through the barrier, forming a supercurrent.

According to the DC Josephson effect the current through the insulator is

$$I_s = I_c \sin(\theta_1 - \theta_2) = I_c \sin \phi \quad (4.1.3)$$

where I_c is the maximum supercurrent (the critical current of the junction) and $\phi = \theta_1 - \theta_2$ is constant for $V=0$. A proof of (4.1.3) based on quantum mechanic theory can be found in [18] and [19]. A more simplified approach is presented in [20].

From a physical point of view, (4.1.3) is a link between phase and coupling energy. When the phase difference between the two superconductive layers is zero, the current is zero and the coupling energy is maximum. When $\phi = \pi / 2$ the current is maximum and the coupling energy becomes zero.

The phase ϕ is related to the applied voltage across the junction via the relationship

$$\frac{\partial \phi}{\partial t} = \frac{2e}{\hbar} V \quad (4.1.4)$$

which is derived in Section 4.1.2. If $V = 0$, the phase is constant since $\frac{\partial \phi}{\partial t} = 0$. On the

other hand, if $V \neq 0$ the junction oscillates as described by the AC Josephson effect.

The energy of a Cooper pair that crosses the junction is

$$\Delta E = qV = -2eV = E_1 - E_2 \quad (4.1.5)$$

In the general case, (4.1.3) shows that the supercurrent flowing through the JJ is dependent on the phase drop ϕ across the junction. This dependence of current to phase is due to the quantum mechanical nature of the superconductive state. When the particle is below the critical temperature of the material, it can be viewed as a wavefunction having a probability density $|\Psi\Psi^*|$. This particle, the Cooper pair, can be transferred across a very thin insulating material with a high-energy barrier, as previously mentioned.

4.1.2 AC Josephson Effect

If a DC voltage $V \neq 0$ is applied to the junction, then the phase is no longer constant. The junction will oscillate at frequency f_J .

The phase is given by

$$\frac{d\phi}{dt} = 2\pi f_J = 2\pi \frac{E}{h} = 2\pi \frac{2eV}{h} = \frac{2eV}{h} \quad (4.1.6)$$

or

$$\frac{d\phi}{dt} = \frac{2\pi V}{\Phi_o} \quad (4.1.7)$$

where $\Phi_o = \frac{h}{2e}$ is defined as the magnetic flux quantum ($\Phi_o = 2.07 \cdot 10^{-15} \text{ Wb}$).

Thus, the oscillating frequency is $f_J = \frac{V}{\Phi_o}$ and the current becomes:

$$I_s = I_C \sin(\omega_J t) \quad (4.1.8)$$

The JJ behaves as a voltage control oscillator with constant I_C for frequencies below

$$f_{\max} = \frac{V_{\max}}{\Phi_o} = \frac{2e}{h} \left(\frac{2\Delta}{e} \right)$$

where $\frac{2\Delta}{e}$ is the gap voltage when Cooper pairs can break with $f_{\max} \cong 1 \text{ THz}$ for Nb.

Maximum operating frequency of JJ circuits that has been demonstrated is in the range of 200 GHz. The I-V characteristic of the JJ is shown in Fig. 4.2. Above the Cooper pair breaking voltage, current exceeds I_C and becomes resistive across the junction resistance. Resistance R represents normal state resistance. The corresponding voltage to the critical current I_C is predicted by the BCS theory.

Figure 4.2: I-V characteristic of the JJ.

4.2 Josephson Junction Electrical Model

4.2.1 Lumped Element Equivalent Circuit

For small variations of the current ($I_s \ll I_c$), the JJ behaves as a non-linear inductance.

From (4.1.3), (4.1.7) and the definition of inductance we have:

$$L_J \equiv \frac{V}{\left(\frac{dI}{dt}\right)} = \frac{V}{I_c \cos \phi \frac{d\phi}{dt}} = \frac{V}{I_c \cos \phi \frac{2e}{\hbar} V} = \frac{\hbar}{2eI_c} \cdot \frac{1}{\cos \phi}$$

or

$$L_J = \frac{L_{J0}}{\cos \phi} \quad (4.2.1)$$

$$\text{where } L_{J0} = \frac{\hbar}{2eI_c}.$$

Equation (4.2.1) gives the effective AC inductance with DC bias current and a small AC current applied to the JJ.

However, for large signals, the dynamics of the JJ become more complicated. There is a quasiparticle (single electron) current across the junction and parasitic capacitance, which leads to an RLC equivalent circuit [20]:

$$I = I_s + I_n + I_d = I_c \sin \phi + \frac{V}{R} + C \frac{dV}{dt} = I_c \sin \phi + \frac{\hbar}{2eR} \frac{d\phi}{dt} + \frac{\hbar C}{2e} \frac{d^2\phi}{dt^2} \quad (4.2.2)$$

where I_s is the JJ supercurrent, I_n the quasiparticle current flowing through a resistive path, I_d the displacement current due to the parasitic capacitance formed by the two layers of superconductive material and $V = \frac{\hbar}{2e} \frac{d\phi}{dt}$.

Equation (4.2.2) is a second order nonlinear differential equation that can be solved though numerical analysis.

For simplicity let's assume a small phase difference such that $\sin \phi \cong \phi$, then (4.2.2) reduces to

$$I = \frac{\Phi}{L_{JO}} + \frac{V}{R} + C \frac{dV}{dt} \quad (4.2.3)$$

because

$$\Phi = L_{JO} I_s = L_{JO} I_c \Phi \text{ or}$$

$$I_c \phi = \frac{\Phi}{L_{JO}}$$

This equation describes a parallel RLC circuit with a natural resonant frequency

$$\omega = 2\pi f = \frac{1}{\sqrt{L_{JO} C}},$$

bandwidth

$$\Delta\omega = \frac{1}{RC} = \frac{\omega_o}{Q} \text{ where } Q = \omega_o RC = \left(\frac{R^2 C}{L_{Jo}} \right)^{1/2}$$

and a damping factor

$$\zeta = \sqrt{\frac{L_{Jo}}{4R^2 C}}$$

Usually the junction is characterized by $\beta_C = Q^2$ also known as Stuart-McCumber parameter.

Using the above equations, one can have two models: the RSJ (Resistor Shunted Junction) model and the CRSJ (Capacitor Resistor Shunted Junction) model. The RSJ is overdamped because of the resistor and does not have hysteretic characteristic as the CRSJ.

4.2.2 Voltage State Logic in Josephson Junction Circuits

According to the theory presented previously, the JJ can have two different states when biased at $I = I_B < |I_C|$. The first is the superconductive, which corresponds to the dynamic inductance model. The second occurs when the junction current exceeds the critical quantity I_C and the current in excess is carried through a resistive path. The superconductive state represents binary “0” and the resistive binary “1”. The voltage in the “1” state corresponds to the gap voltage $V_g = 2\Delta / e$ ($V_g = 2.8\text{mV}$ for Nb JJ).

The current-voltage characteristic of two JJ is shown in Fig. 4.3. Both junctions are biased at DC current I_B . Although the input to this type of circuits is typically voltage, it is transformed to current to facilitate the operation of the JJ.

In the first attempts to implement superconductor digital circuits, designers employed a switching logic named latching or voltage-state. The main disadvantage of this technology lies in the switching between the states. Although switching from “0” to “1” can be achieved quite fast, the opposite (“1” to “0”) is done at a lower speed. The reason can be seen in Fig. 4.3a, where the voltage remains at “1” despite input current is zero. The only way to return to “0” state is switching off the bias current I_B , which requires extra time. Another approach for implementing digital circuits with JJ makes better use of the JJ physics by encoding flux rather than voltage. This approach is named Single Flux Quantum (SFQ) logic and employs shunted JJ as the one shown in Fig. 4.3.

4.3 Rapid Single Flux Quantum (RSFQ) Logic

The previous section described the voltage-state switching logic in superconductors. If the fundamental property of superconductors to quantize magnetic flux is used, a new digital logic technique is feasible. The supercurrent, I_s , can also be expressed in terms of magnetic flux. If the junction is not used as a radiation source but as a receiver of electromagnetic energy, the sensitivity of this device can be expressed in magnetic flux units. The magnetic flux is the time integral of the voltage (Faraday's law)

$$\Phi = \int V dt = \frac{\Phi_o}{2\pi} \phi \quad (4.3.1)$$

since from (4.1.7)

$$V = \frac{\Phi_o}{2\pi} \frac{d\phi}{dt}.$$

Substituting (4.3.1) into (4.1.8) the supercurrent is now, $I_s = I_c \sin(2\pi \frac{\Phi}{\Phi_o})$ which shows

the dependence of the current on the applied flux or the quantized phase $\phi = 2\pi \frac{\Phi}{\Phi_o}$. In a

superconductive loop, this implies that the flux exists in integer multiples of Φ_o . If we close the ends of the loop, the wavefunctions in those two points should have a phase difference corresponding to integer multiples of 2π , thus

$$\Phi = n\Phi_o \quad n = 0, \pm 1, \pm 2, \dots$$

Digital information can be coded in two states, for example $n=0$ and $n=1$. Instead of discrete voltage states, binary information is coded in flux states. This logic is called Rapid Single Flux Quantum (RSFQ) and dominates in modern digital superconductive circuits. An extensive presentation of the technology can be found in [21], [22] and [23].

The simplest SFQ circuit having one JJ is the RF SQUID (Superconductive Quantum Interference Device) and is used for magnetic detection (Fig. 4.4).

Figure 4.4: (a) The RF SQUID and (b) its characteristic response in time. Voltage is in units of $I_C R$, time in units of τ_o (Eq. (4.4.8)) and phase in rad. The graph shows the voltage and phase when the junction switches and a single flux quantum pulse is released.

The loop comprises only one JJ and no bias current is necessary for its operation. In principle, the RF SQUID measures flux in multiples of Φ_0 so it has high sensitivity to input signals.

The flux in the RF SQUID is

$$\Phi = \Phi_{ex} - LI \text{ or}$$

$$\Phi_{ex} = \Phi + LI_C \sin\left(2\pi \frac{\Phi}{\Phi_0}\right) \quad (4.3.2)$$

Equation (4.3.2) is plotted in Fig. 4.5 where the transitions from one state to another are shown. External flux is induced to the loop by the current I_{ex} , which creates $\Phi_{ex} = MI_{ex}$, M being the mutual inductance of the coupling circuit. It must be noted that (4.3.2) has the solution plotted in Fig. 4.5 when $LI_C > 1$ that is for junctions with large critical current.

If $LI_C < 1$, $\Phi \cong \Phi_{ex}$ and the phase difference across the junction is mainly due to the applied flux, or $\phi = 2\pi \frac{\Phi_{ex}}{\Phi_o}$ thus no quantization is possible. If $LI_C > 1$, quantization states are allowed. In general, for $LI_C > 1$ there are more than two stable states for the same external flux Φ_{ex} in a JJ loop but the proper choice of LI_C product facilitates the operation around two flux states, representing digital “1” and “0” respectively.

Figure 4.5: Total magnetic flux Φ as a function of applied flux Φ_{ex} in the RF SQUID. The DC bias flux is set to $\Phi_o / 2$ (dashed line).

Switching between flux states means a phase rotation or leap by 2π as the current increases and exceeds the critical value I_C . When I_S reaches I_C the phase difference reaches also the critical point of $\pi/2$ but beyond this point I_S decreases. More current flows through the shunt resistor thus producing a voltage across the junction. This voltage causes a further increase in phase until it reaches 2π . After the phase has rotated by 2π , the junction releases a pulse with constant area proportional to the flux quantum Φ_o .

$$\int V dt = \Phi_o = 2mV \cdot ps$$

Special care must be given to the selection of the junction characteristics because the dynamics of the model (RSJ or CRSJ) determine the switching speed of the RF SQUID.

As any second order system, there is a trade-off between switching speed and allowable oscillations. In order to avoid oscillation of the loop, the system must be underdamped which leads to $\beta_c \leq 1$:

$$\beta_c = Q^2 \text{ or}$$

$$\beta_c \leq \frac{R^2 C}{L_{JO}} \text{ or}$$

$$\beta_c \leq \frac{2\pi}{\Phi_o} I_c R^2 C \text{ or}$$

$$R \leq \left(\frac{\Phi_o}{2\pi I_c C} \right)^{1/2} \quad (4.3.3)$$

For a typical JJ, the inequality (4.3.3) is not met and a resistor that decreases the total resistance of the circuit is connected externally in parallel to the JJ. However, an

underdamped loop $R \ll \left(\frac{\Phi_o}{2\pi I_c C} \right)^{1/2}$ would make the circuit slow, so the resistor should

not be too large. A good compromise between these two conflicting requirements is

$\beta_c \cong 1$. For this value, the time constant of the loop is:

$$\tau_o = RC = \left(\frac{\Phi_o C}{2\pi I_c} \right)^{1/2} \quad (4.3.4)$$

It is clear from (4.3.4) that the switching speed of a JJ depends on C and I_c . Those two parameters are related to the process technology. Currently there are two competing fabrication technologies in superconductive electronics, which are by Hypres Inc. and TRW Inc. (now part of Northrop Grumman Inc.). Current and future scaling of the JJ characteristics are summarized in Table 4.1 [22].

Table 4.1: Current and future superconductive technology features ($\beta_c = 1$).

Fabrication technology	HYPRES [24]	TRW [25], [26]	COOL design [27]	Deep submicron [22]
Minimum junction size $F = \sqrt{A_{\min}} \text{ (}\mu\text{m)}$	3	1.75	0.8	0.3
Critical current density $j_c \text{ (kA/cm}^2\text{)}$	1	4	20	150
Specific capacitance $C_o \text{ (}\mu\text{F/cm}^2\text{)}$	5	6	7	8
$I_c R$ product (mV)	0.3	0.5	1.1	2.0
Time scale $\tau_o = (\Phi_o C_o / 2\pi j_c)^{1/2} \text{ (ps)}$	1.28	0.7	0.3	0.17
Power scale $I_u^2 R \text{ (}\mu\text{W)}$	0.04	0.07	0.14	0.25

The critical current density is $j_c = I_u / A_{\min}$ where I_u is the value of the critical current and $A_{\min}$ the minimum junction size. Typically, I_u is selected to be $100\mu\text{A} < I_u < 200\mu\text{A}$ as a trade-off between noise immunity and power consumption. A junction biased at low current is susceptible to thermal fluctuations and it is likely that it switches in the absence of external signals. On the other hand, a high bias current would mean excessive power dissipation. A good trade-off is $I_u = 0.125\text{mA}$ which calculations in Table 4.1 are based on. The specific capacitance C_o equals the total capacitance of the JJ per unit area or $C_o = C/A$. For AlO_x junctions with $\epsilon_r \cong 10$ and thickness $d = 2 - 5 \text{ nm}$, C_o is calculated from the equation

$$C_o = \frac{C}{A} = \frac{\frac{\epsilon_0 \epsilon_r A}{d}}{A} = \frac{\epsilon_0 \epsilon_r}{d}$$

The minimum pulse width $\tau = \pi\tau_0$, which determines the bandwidth of RSFQ technology, is determined by the critical current density j_c and the specific capacitance C_0 . Therefore, the switching speed of the RSFQ circuit is a function of the minimum junction size.

The RF SQUID as described in this section along with the single JJ are the core of most digital superconductive circuits. Based on the physics of these subcircuits, all digital components found in silicon technology have been built in LTS. Flip-flops, memory cells, gates both synchronous and asynchronous have been successfully demonstrated in SFQ. In the beginning of SFQ technology, the major problem that had to be solved was how the pulses would be transferred from one element to another. The solution was the propagation of pulses through dynamic SFQ circuits that can reproduce and in some cases amplify the input pulses.

A typical layout of the externally shunted JJ is illustrated in Fig. 4.6.

Figure 4.6: Layout of an externally shunted JJ. Figure courtesy of Hypres Inc.

4.4 Phase Modulation Superconductive ADC

One of the numerous applications of RSFQ circuits lies in the A/D conversion field. The switching speed of the JJ makes superconductive ADCs a good candidate for wideband radio [28], [29]. The Phase Modulation ADC (PM-ADC) studied here was designed and fabricated by Hypres Inc. in collaboration with State University of New York (SUNY) at Stony Brook. Design and fabrication of the device are covered in [30], [31] and [32]. The circuit block diagram is shown in Fig. 4.7 and comprises the quantizer front-end (Modulator, SYNC and DEC) and the decimation digital filter. The key component of the ADC is the modulator, a standard RF SQUID, having two inputs: a clock source and an analog input signal.

Figure 4.7: Phase modulation ADC block diagram.

The clock is generated externally by a signal generator and connected to the modulator loop (RF SQUID) through the clock generation module, which divides the frequency by 2.

The JJ is thus clocked at a rate of $f_{clk}/2$ by the DC voltage source. The input signal is inductively coupled to the loop, which operates as a phase modulator of the total magnetic flux.

The phase modulator circuit schematic is depicted in Fig. 4.8. The clock frequency is divided by two by a T flip-flop implemented in RSFQ technology. The junction J_0 generates the SFQ pulse train that modulates the analog signal. A LPF formed by L_0 and R_0 attenuates the higher frequency components of the pulses so that the modulator junction J_1 is not affected by harmonics and is biased at a stable DC voltage generating a quantum flux at a rate of $\Phi_o/2$ every clock cycle. Since one flux quantum Φ_o is generated every two periods, from (4.3.3) the DC voltage input to the modulator is:

$$V = \frac{\Phi_o f_{clk}}{2}$$

Figure 4.8: Phase modulator of the PM-ADC.

The modulator core is formed by the junction J_1 and the transformer L_1 that couples the analog input current into the loop. As the voltage source pumps magnetic flux at a constant rate of $f_{clk}/2$ the JJ switches at the same rate. As discussed in the previous section, the JJ releases a flux quantum Φ_0 pulse when the current across the junction exceeds the critical current. In the presence of an analog signal, the time when the transition occurs differs. If the input current increases, the quantum flux is released before the clock instant. Inversely, a decreasing input makes the JJ switching later. Consequently, the loop performs phase modulation on the input signal.

The phase of the output stream is proportional to the total flux applied to the loop i.e. the flux of the clock pulse train plus the flux of the analog signal. An SFQ pulse produced by J_1 corresponds to 2π rad in phase difference across the junction. Equivalently, an input signal variation corresponding to a SFQ in flux units produces a phase difference of 2π .

The modulated signal passes through a Josephson Transmission Line prior to the synchronizer. The synchronizer or “race arbiter” is another important component of the front-end as it demodulates the flux pulse train. It consists of RSFQ shift registers that synchronize the delayed inputs. The pulse train is delayed in N delay cells or channels of the synchronizer ($N=2$ for the ADC studied in this work). The purpose of the synchronizer is to convert the pulse train to a parallel bit differential code. It also stores the incoming pulses and releases them at the clock edge. Each delay element introduces time delay of $\tau = 1/Nf_{clk}$ to the pulse train so that the inputs to the synchronizer are identical but shifted in time. The achieved phase resolution is in the order of π/N and constitutes the LSB resolution of the ADC. The theoretical minimum detectable signal is

$\Phi_o/2N$ because the clock pumps $\Phi_o/2$ flux in the loop per period $1/f_{\text{clk}}$. For each channel, the required input signal flux for switching J1 is $\Phi_o/2$ or π rad in phase. The remaining portion $\Phi_o/2$ of the flux is provided by the clock flux bias. The number N of synchronizer delay cells determines the loop components' values. Based on the process parameters, the relationship between the loop components [30] can be derived.

Following the synchronizer there is the decoder circuit, which is the last component of the front-end quantizer. It converts the binary thermometer code of the SYNC to a differential code for further processing.

The last block of the ADC is the digital decimation filter. Its main task is downsampling (decimating) the data rate. It is implemented using a typical CIC (Cascaded Integrator Comb) architecture found in [33] and [34]. It performs integration of the differential code and low-pass filtering removing any unnecessary components, like the clock flux bias.

A detailed analysis of phase modulation-demodulation for a PM-ADC having a 4-channel synchronizer is presented in [30].

The output bit stream of the ADC is in differential JJ logic format and has to be converted to a standard electronic logic if it is to be processed by semiconductor circuits. Section 5.6.2 will further discuss the interface. It should be noted that the whole device is at Low Temperature of 4.9K submerged in liquid Helium.

The ADC under test has 15 physical bits and a 2-channel synchronizer. It was fabricated at Hypres foundry using the Nb process of 1 kA cm^{-2} critical current density. It contains 6000 JJ and occupies 1 cm^2 chip area. The digital decimation filter is tunable via a programmable clock controller at 1:128, 1:64 and 1:16 decimation ratio. The ADC chip is optimized for clock frequency of $f_{\text{clk}}=18.6 \text{ GHz}$ which is provided by an external source.

More information on the hardware setup will be presented in Chapter 5. Finally, the circuit photomicrograph is shown in Fig. 4.9. The enlarged portion of the picture illustrates the phase modulator.

Figure 4.9: Circuit photomicrograph of the 15-bit PM-ADC. Picture courtesy of Hypres Inc.

Chapter 5

Superconductive ADC Measurements

5.1 Introduction

The superconductive ADC was tested under single and two-tone signals in both lowpass and bandpass sampling schemes. The CW signal was sampled at IF and the resulting bit stream was processed using Hypres custom software. The testbed consists of an analog signal generator, the ADC, the JJ to ECL interface and the software code. The receiver chain is shown in Fig. 5.1.

Figure 5.1: Receiver test-bed for the superconductive ADC characterization.

5.2 Signal Generator

The signal was generated at IF, thus a downconversion stage was not necessary. However, the receiver setup is similar to that of a superheterodyne one, where the image noise and LO leakage are attenuated several dB below noise floor. The IF was chosen after simulations so that the SNR at the output of the ADC is satisfactory. This frequency

was tunable in order to investigate the performance over a wide frequency range.

Simulation has shown that an IF between 10-70 MHz is necessary for an acceptable SNR.

The sampling rate will be at least twice the maximum frequency for the lowpass sampling scheme or less than twice the maximum frequency for the undersampling scheme.

5.3 Superconductive Analog to Digital Converter

The Device Under Test (DUT) was the Phase Modulation ADC provided by Hypres Inc. and described in Section 4.4. Device characteristics can be found in [32]. The ADC operated mostly under lowpass sampling scheme. As already mentioned, an intermediate frequency of 70 MHz maximum will give an SNR of at least 50 dB. The clock source of the ADC was set to 18.6 GHz (clock input) and the decimation ratio to 128:1, which is the maximum on chip decimation. This ratio reduces the output sampling rate to 145.3 MS/s. The JJ logic bit stream is then transformed to complementary standard ECL format (-0.9V to -1.7V). The digital output is available on standard two-row, 10 pin DIP connectors. The ADC has 15 physical bits but maximum 12 were used in the test. The other 3 contained no information, only noise.

5.4 Post-Process

The digital signal could be further decimated (up to 64:1) using Hypres custom software (Digitest), if necessary. After digital data was collected, a 16384-point FFT was performed, using “Blackman-2” windowing. SNR (Signal-to-Noise Ratio), SFDR (Spurious

Free Dynamic Range) and ENOB (Effective Number of Bits) were calculated and saved in postscript format files.

5.5 Test Results

5.5.1 Single Tone Test

A single tone signal was applied to the ADC as shown in Fig. 5.2. The sinewave frequency varied from 2 to 200 MHz. Two of these values (10 and 50MHz) are the same as in the published paper by Hypres that describes the performance of the device under single tone test [32].

Figure 5.2: Single-tone evaluation setup.

The clock frequency was set to 18.6 GHz while the decimation ratio was 1:128. This resulted in an output sampling rate of 145.3 MS/s. Having the same frequency helped validate Hypres' results. The broad range of frequencies was chosen so as to evaluate the performance of the ADC in two different scenarios: oversampling and undersampling.

The test results are presented in Table 5.1. The input power level chosen gave the maximum SNR and SFDR, which did not correspond, to the FS (Full Scale) level. Since this type of ADC is limited by the maximum slew rate, the input power was increased by 3 dB and the degradation of SNR and SFDR was recorded. Results are presented in Table 5.2. In both cases, the input signal was either lowpass or bandpass filtered and attenuated by 30dB before entering the ADC (Fig. 5.3). The SNR and SFDR graphs versus analog input frequency (no slew rate limit) are depicted in Fig. 5.4. The FFT of a 10 MHz single tone is shown in Fig. 5.6.

Table 5.1: Single Tone Results.

f_{in} (MHz)	P_{in}* (dBFS)	P_{in}* (dBm)	SNR (dBc)	SFDR (dBc)	ENOB
2.0	-13.67	-9	75.18	-98.17	12.20
5.0	-14.22	-17.5	67.1	-90.95	10.86
10.0	-10.70	-20	61.37	-84.56	9.90
15.5	-14.89	-28	57.2	-81.9	9.21
29.5	-8.80	-27.5	51.46	-76.32	8.26
50.0	-11.22	-34.5	45.86	-70.32	7.33
69.1	-11.91	-38	41.27	-66.39	6.56
150.0	-11.17	-44	13.81	-39.09	2.01
200.0	-12.67	-48	22.84	-48.75	3.50

* P_{in} corresponds to the optimum power level for maximum SNR and SFDR.

Table 5.2: Single Tone Results (Slew Rate Limitation).

f_{in} (MHz)	P_{in} (dBFS)	P_{in} (dBm)	SNR (dBc)	SFDR (dBc)	ENOB
2.0	-10.67	-6	36.15	-38.79	5.55
5.0	-11.22	-14.5	46.23	-55.32	7.39
10.0	-6.70	-16	50.52	-60.08	8.10
15.5	-11.89	-25	47.33	-55.93	7.57
29.5	-5.80	-24.5	31.95	-37.39	5.50
50.0	-8.22	-31.5	31.51	-40.27	4.94
69.1	-8.91	-35	34.71	-51.81	5.47
150.0	-8.17	-41	9.66	-29.99	1.31
200.0	-9.67	-45	20.67	-44.09	3.14

Figure 5.3: Input attenuation to ADC.

Figure 5.4: SNR and SFDR vs. input frequency for the single tone test.

Slew Rate Limitation

The slew rate is the dominant limitation in this ADC when the signal frequency increases as can be seen in Table 5.2. The ADC must track the signal and account for the steep changes in amplitude. The current architecture supports a clock generator that produces $\Phi_o/2$ fluxons per clock period [30], where Φ_o is the magnetic flux quantum ($\Phi_o = h/2e = 2.07 \cdot 10^{-15} \text{ Wb}$) as shown in Chapter 4. For a sinewave input $y(t) = A \sin \omega t$ this means that the rate of change must not exceed $\Phi_o/(2f_{clk})$. The maximum signal amplitude in multiples of Φ_o is:

$$A_{\max} = (\Phi_o/2) \cdot f_{clk} / 2\pi f$$

Assuming a typical JJ single loop with mutual inductance M, the current flowing through the junction is:

$$I_{\max} = A_{\max} / M$$

The above equations describe the slew rate limitation in the modulator of the ADC. The maximum input power can be found by assuming a 50Ω system.

$$P_{\max} = (I_{\max}^2 / 2) \cdot 50$$

For $f_{clk}=18.6 \text{ GHz}$ and $f=10 \text{ MHz}$ the maximum input signal (peak) is $148 \Phi_o$. A typical value for the mutual inductance of a single loop is $M=200 \text{ pH}$ resulting in $I_{\max}=1.53 \text{ mA}$.

The max input power is -12.3 dBm for a 50Ω system.

SNR and SFDR dependence on input frequency

It has been mentioned that the device is a lowpass delta ADC and the output is decimated. The output filter is a major limitation if the input is at high IF. The effect of the sinc characteristic of the output filter is evident in Fig. 5.5. Although the frequency increased from 150 to 200 MHz, the SNR increased as well. It was 13.81 at 150 MHz and 22.84 at 200 MHz. The decimated signal is multiplied by a sinc function in the time domain:

$$\text{sinc}(f/f_s/2) = \text{sinc}(f/72.65),$$

where f is the signal frequency and f_s the sampling frequency. The values at 150 and 200 MHz are $\text{sinc}(150/72.65) = 0.0311$ and $\text{sinc}(200/72.65) = 0.081$ or $20 \cdot \log(0.081/0.0311) = 8.31$ dB

This explains the difference in SNR between the two frequencies.

Figure 5.5: Sinc filter characteristic.

Figure 5.6: 16K FFT for a 10 MHz single tone.

5.5.2 Two-Tone Test

This test case is useful for the determination of third order intermodulation products. Two signal sources were used and three frequency sets were chosen. The first set is 9 and 10MHz, the second is 30.5 and 31.5MHz and the third is 49.5 and 50.5MHz. The test setup is shown in Fig. 5.7. The output of each signal generator was filtered by lowpass filters and then connected to a combiner. The combiner's output was either lowpass or bandpass filtered before feeding the ADC. It must be noted that the signal was attenuated by 30dB before being sampled as in the single-tone test case.

Figure 5.7: Two-tone evaluation setup.

For each frequency set, higher order intermodulation products are generated. Third and fifth order intermodulation products are of interest in our case in order to examine the linearity of the ADC. No second order IM2 products ($|f_1-f_2|, |f_1+f_2|$) were observed. All frequencies are shown in Table 5.3 and test results are presented in Tables 5.4, 5.5 and 5.6. The FFT of $f_1=30.5$ and $f_2=31.5$ MHz for $P_1=P_2=-31$ dBm can be found in Fig. 5.8.

Table 5.3: Fundamental and odd order intermodulation frequency components.

f_1 (MHz)	f_2 (MHz)	$2f_1-f_2$ (MHz)	$2f_2-f_1$ (MHz)	$3f_1-2f_2$ (MHz)	$3f_2-2f_1$ (MHz)
9	10	8	11	7	13
30.5	31.5	29.5	32.5	28.5	33.5
49.5	50.5	48.5	51.5	47.5	52.5

Table 5.4: Input and output power for 9 and 10 MHz input.

P_1 (dBm)	P_2 (dBm)	$P_{2f_1-f_2}$ (dBc)	$P_{2f_2-f_1}$ (dBc)	$P_{3f_1-2f_2}$ * (dBc)	$P_{3f_2-2f_1}$ * (dBc)
-30	-27	-74.9	-75	-	-
-29	-26	-73.6	-72.6	-	-
-27.5	-24.5	-56.4	-74.2	-	-

* Fifth order intermodulation products below noise floor.

Table 5.5: Input and output power for 30.5 and 31.5 MHz input.

P_1 (dBm)	P_2 (dBm)	$P_{2f_1-f_2}$ (dBc)	$P_{2f_2-f_1}$ (dBc)	$P_{3f_1-2f_2}$ (dBc)	$P_{3f_2-2f_1}$ (dBc)
-33	-33	-71.2	-71.7	-72	-77
-32	-32	-67.4	-71.7	-72.1	-72
-31	-31	-63	-65.8	-68.8	-68.2

Table 5.6: Input and output power for 49.5 and 50.5 MHz input.

P_1 (dBm)	P_2 (dBm)	$P_{2f_1-f_2}$ (dBc)	$P_{2f_2-f_1}$ (dBc)	$P_{3f_1-2f_2}$ (dBc)	$P_{3f_2-2f_1}$ (dBc)
-33	-33	-68	-70	-67	-69
-32	-32	-65.3	-63.4	-65.6	-67.1
-31	-31	-52.5	-52.4	-58.1	-59.8
-30	-30	-42.7	-42.8	-49.7	-49.8

Power of third and fifth order products (dBc) is shown relatively to P_1 and P_2 , which were equal at the FTT output in all three cases. This is not true for 9 and 10 MHz signals because the input power of the second tone was twice the power of the first one, although the FFT showed equal power levels. The generator output was not at the desired power level but deviated when switched to high scale close to saturation.

The two-tone test involved problems that had not been anticipated. When two signals were present the ADC was not the only source of error. As can be seen from Table 5.4, the third order intermodulation product power was much higher ($>20\text{dB}$) for the $2*f_1-f_2$ than the $2*f_2-f_1$ product, when the power exceeds 2.5 dBm. This occurred only for this frequency since for the rest of the test the intermodulation products were symmetrical. This behavior was attributed to the signal generators' not being sufficiently isolated. For example when a BPF was used at the output of the combiner the spectrum was still asymmetrical but not as much as in the LPF case. Furthermore, when two 10 dB attenuators were placed at the outputs of the generators the difference was reduced to 4 dB ($P_{2f_1-f_2}=-59.9\text{dBc}$ and $P_{2f_2-f_1}=-64\text{dBc}$ for $P_1=-27.2\text{dBm}$ and $P_2=-26.5\text{dBm}$). The lack of proper equipment (spectrum analyzer, network analyzer) made the testing more challenging.

The presence of fifth order intermodulation products was stronger at 30.5, 31.5 MHz and 49.5, 50.5 MHz than at 9, 10 MHz as a result of filtering. The LPF's with 10% 3dB bandwidth used in the test attenuate more the 5th order signals at low frequencies where the frequency falls out of the passband. At higher frequencies, the 5th order frequencies fall in the passband.

Figure 5.8: 16K FFT for the two-tone test $f_1=30.5$ and $f_2=31.5$ MHz ($P_1=P_2=-31$ dBm).

5.5.3 Comparison to Hypres' Results

The superconductive ADC chip has been tested by Hypres in the past and results have been presented in published papers [30], [31]. Compared to [30] the results of Nortel test seem to be slightly worse in terms of SNR. The small difference in SNR can be attributed to the higher oversampling ratio. Unfortunately, no information is provided for the test setup in [30]. Although the ADC in [31] is a previous version of the chip used in this test (1G as opposed to 2G), it is useful to show the performance of both. The 1G chip is optimized for clock frequency $f_{\text{clk}}=12.8$ GHz and has 14 physical bits, compared to $f_{\text{clk}}=19.6$ GHz and 15 bits of 2G. The following tables summarize results taken during the tests.

Table 5.7: Comparison between Hypres' published results and Nortel test results.

F=10MHz	Hypres' [30]	Hypres' [31]	Nortel
SNR (dBc)	63	78	61.37
SFDR (dBc)	-76.5	-90	-84.56
ENOB	10.2	12.6	9.9
fs (MS/s)	153.1	25	145.3
fclk (GHz)	19.6	12.8	18.6

Table 5.8: Comparison between Hypres' [31] and Nortel test.

F=50 MHz	Hypres' [31]	Nortel
SNR (dBc)	58	45.86
SFDR (dBc)	-80	-70.32
ENOB	9.4	7.33
fs (MS/s)	100	145.3
fclk (GHz)	12.8	18.6

5.5.4 Superconductive ADC Performance vs. IS-95 Specifications

The current ADC operation is degraded as the input frequency increases. High values of SNR cannot be achieved when the signal exceeds a few MHz. Therefore, the device can be used only for low IF sampling, making direct sampling not feasible at the moment. In the case of wideband radio operating at IF, the SNR of the ADC would have to be greater than 80 dB under IS-95, as derived in Chapter 2. The SFDR would have to be at least 90 dB. These numbers are derived from the single and two-tone desensitization test case and can be achieved using a heterodyne or superheterodyne receiver. However, in a wideband radio or direct sampling receiver (3 channel IS-95 or 3GPP) these numbers are not met unless the signal is in the sub megahertz range. This is also the reason for not testing the ADC under CDMA signal since no useful results would be available. However, the ADC shows very good linearity due to the inherent characteristics of the JJ. The FFT's saved during the test show that all higher harmonics of the signal generator are suppressed (below noise floor) for a single tone input or minimized for the two tone test.

5.5.5 Superconductive ADC vs. state-of-the-art Semiconductor ADC (AD6645)

It would be useful at this point to present a comparison between the phase modulation superconductive ADC and the state-of-the-art semiconductor ADC which is described in [35]. The Analog Devices AD6645 employs a subranging architecture and is fabricated on a 0.8 μ m complementary bipolar process. It was tested in Nortel labs and further information on the architecture of the ADC and the evaluation board can be found in [36]. The maximum sampling rate is limited to 105MS/s but undersampling is possible since the analog input bandwidth is at 270MHz. For single-tone inputs the SNR is relatively stable and above 65 dB for frequencies up to 200 MHz. The sampling frequency was constant at $f_s=80$ MS/s. Table 5.9 summarizes SNR and SFDR single-tone test results in both cases.

Table 5.9: Superconductive Phase Modulation vs. AD6645 ADC.

f_{in} (MHz)	PM-ADC SNR (dBc)	AD6645 SNR (dB)	PM-ADC SFDR (dBc)	AD6645 SFDR (dB)
2.0	75.18	68.56	98.17	53.87
5.0	67.1	68.54	90.95	61.88
10.0	61.37	73.23	84.56	62.22
15.5	57.2	67.84	81.9	55.5
29.5	51.46	71.78	76.32	73.48
50.0	45.86	72.35	70.32	73.93
69.1	41.27	67.10	66.39	76.74
150.0	13.81	71.99	39.09	69.61
200.0	22.84	61.88	48.75	61.51

The AD6645 seems to be more suitable for IF sampling applications because the SNR is stable with frequency. The lowpass nature of the PM-ADC is obvious in this table, too. On the other hand, the AD6645 seems to be less linear than the PM-ADC according to SFDR values. Because of different filtering used, the true SFDR of AD6645 should have been higher than the one shown but still lower than the PM-ADC. In the two-tone test, the FFT spectrum of AD6645 contains more second and third order intermodulation products. Also, its fifth order IM products are below the noise floor. In all three frequency sets second order IM ($|f_1-f_2|$, $|f_1+f_2|$) power levels were higher than third order ones.

The FFT for $f=29.5$ MHz is presented in Fig. 5.9. The FFT of two tones at $f_1=30.5$ and $f_2=31.5$ MHz is shown in Fig. 5.10.

Figure 5.9: 16K FFT for a single tone at $f=29.5$ MHz (AD6645).

Figure 5.10: 16K FFT for a two tone at $f_1=30.5$ and $f_2=31.5$ MHz (AD6645).

5.6 Hardware Used

5.6.1 Signal Sources

Two different signal sources were used for the characterization of the device. One source generated the analog signal, which was digitized, and a second source generated the clock signal driving the ADC. The devices' characteristics are summarized in Tables 5.10 and 5.11.

Table 5.10: Signal Generators.

Model	Frequency Range	Quantity
HP 8640B	0.5 MHz to 1.024 GHz	2
HP 83712A	10 MHz to 40 GHz	1

Table 5.11: SSB (dBc/Hz) Phase Noise Characteristics of HP 83712A.

Carrier Frequency	100Hz Offset	1 KHz Offset	10 KHz Offset	100 KHz Offset
500 MHz	-70	-86	-103	-119
2 GHz	-66	-74	-91	-107
10 GHz	-69	-75	-79	-101
18 GHz	-63	-70	-73	-99

5.6.2 Josephson Junction to ECL Interface

The digital bitstream of the ADC is transformed from JJ to ECL logic in order to be connected to a logic analyzer and processed by the software [37]. The interface between the ADC and the logic analyzer consists of a clock module and four data modules (Fig. 5.11). The clock module processes the ADC output clock and distributes it to the data modules.

Data bits are then latched and converted to ECL. The clock and data modules did not operate ideally throughout the test. As a result, data acquired by the software might have been affected by noise. The threshold voltage of the data modules had to be constantly tuned in a way that accounted for any deviation from normal performance.

Figure 5.11: Interface circuit.

5.6.3 Cooling Process

Another point of interest during the test was the cooling process of the ADC chip. The test was performed using a “dewar”. The “dewar” is a metal flask containing liquid He which is replaced after a few days. The ADC is attached at the edge of a probe and immersed into the liquid He. Cooling takes place in an electromagnetically shielded environment to protect the chip from external interference. If magnetic flux is trapped in the superconductive loops due to external magnetic fields, the switching capabilities of the JJ will change. The procedure must be slow and takes more than 1/2 hour in order for the chip to reach smoothly the point where Nb becomes superconductive. Currently, there

are two options for the packaging: The cryocooler package or the “dewar”. The second option is cheaper and more flexible for test purposes only. Commercial applications require a more sophisticated cryogenic packaging system, which would be smaller in size and reliable for a long period of time. Further information on packaging technology can be found in [38] and [39].

5.6.4 Filters

Two types of filters were used during the experiment: lowpass and bandpass. Filtering is necessary in order to minimize the effect of harmonics from signal sources. Filters are shown in Table 5.12.

Table 5.12: Filters.

Manufacturer	Type	Part #	Frequency (MHz)	Quantity
Trilithic Inc.	LPF	X5ELX2-1.1-KK	2.0	1
Trilithic Inc.	LPF	X5ELMD5-1-KK	5.0	1
Trilithic Inc.	LPF	X5ELM10-1-KK	10.0	2
TTE	LPF	J4003-10M-50-720A	10.0	2
Trilithic Inc.	BPF	7BMD10/X1.0-3-KK	10.0	1
Mini-Circuits	LPF	SLP-30 9010 12	30.0	1
Trilithic Inc.	LPF	X5ELM50-1-KK	50.0	2
TTE	LPF	X5ELX100-1-KK	50.0	1
Trilithic Inc.	BPF	7BMD50/X5-3-KK	50.0	1
Mini-Circuits	LPF	SLP-70 9339 15	70.0	1
K&L Microwave Ltd	BPF	5BT-63/125-5-0/0	63-125	1
K&L Microwave Ltd	BPF	5BT-125/250-5-0/0	125-250	1

5.6.5 Power Combiners/Splitters, Connectors

The power combiner was needed for the two-tone test when signals from the two generators were combined. The combiner's model was: KDI D293S 64537. All connections were implemented with SMA cables. The following cable connections were used: Clock Source - Filter, Filter - ADC, Analog Source - Filter, Filter - Combiner. Also, the following connectors were used where necessary: N-Type to BNC, BNC to SMA.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

This work presented an analysis on wideband radio requirements related to the ADC. The system level approach quantified the specifications for a IS-95 direct RF sampling receiver with respect to SNR, SFDR and clock jitter. An ADC with such performance in SNR and SFDR can be used in a wideband radio receiver. Degradation of SNR due to clock jitter was also investigated. The importance of low jitter clock in wideband sampling systems operating under bandpass sampling scheme was shown.

Moreover, theoretical formulas were derived for signals sampled by a generic sampling system. The theoretical equation uses the autocorrelation function of the input signal for the derivation of the SNR expression when the only noise source stems from the clock. Cases covered involve sampling a single sinusoid, a baseband and bandpass signal with flat and raised cosine power spectral density. The last simulation model can be used to investigate the effect of jitter on IS-95 systems and derive theoretical requirements, since the same modulation scheme and pulse shaping are employed here. The three examples were simulated in Matlab Simulink using a Sample and Hold block as a sampler. Simulation results correlate with theory for high oversampling ratios.

The phase modulation superconductive ADC, provided by Hypres Inc. was tested under single and two tone signals and compared to the state-of-the-art semiconductor ADC (AD6645). Test results were as expected and proved the lowpass nature of the device. It is obvious that the current ADC cannot meet the requirements for software defined radio. Performance is mostly affected by the slew rate limitation as discussed previously. This is apparent in the dynamic range (SNR), which decreases with frequency. The superconductive ADC shows better linearity but SFDR degrades when frequency enters the IF range. Overall, the AD6645 maintains high SNR for a wider range of frequencies than the PM-ADC but with decreased linearity.

6.2 Future Work

From the theoretical point of view, an ADC model is necessary for the evaluation of SNR expressions. This model would show the impact of other non-idealities on system performance but allow undersampling as well. A bandpass modulator would demonstrate clock jitter scaling with sampling to signal frequency ratio, as explained in Chapter 3.

Future work on the Phase Modulation Superconductive ADC would involve replacing the high jitter clock with an on-chip solution and changing the modulator with a bandpass sigma-delta structure [40]. In general, superconductive ADCs have great potential due to the physics of the JJ but many challenges still lie ahead such as clock generation, packaging and process variations.

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Appendix A

A1. Matlab Code for Direct RF Sampling Frequency

The algorithm for the selection of the sampling frequency F_s is implemented in the following Matlab code.

```
%bandpass_sampling.m

%This MATLAB script calculates the allowable sampling frequencies
%for direct bandpass sampling of a CDMA signal

fl=1850; %CDMA lower band in MHz

fh=1910; %CDMA upper band in MHz

BW=fh-fl; %CDMA band allocation

BWchannel=1.25; %CDMA channel bandwidth in MHz

fc=fl+BW/2;

n=0;

%Minimum sampling rate fs=2*BW

for fs=(2*BW):300

    n=n+1;

    if rem(fix(fc/(fs/2)),2)==0 %if even/odd Nyquist zone

        fIF=rem(fc,fs);
```

```
else

    flF=fs-rem(fc,fs);

end

if ((flF-BW/2)>0 & ((fs/2-flF-BW/2)>0))

    %fs

    freq(n)=fs;

else

    freq(n)=0;

end

end

freq

figure;

stem(freq);

ylabel('Sampling frequency fs');
```

A2. Matlab code for SNR Calculation of a Sinewave Signal

Equation (2.4.3) is verified against a time domain simulation. The simulated SNR correlates very well with the theoretical SNR for a sinewave signal. The Matlab script is given below.

```
%
%sample_sinewave.m
%Script for simulation of sinewave sampling formula
%Sample-and-Hold is assumed ideal and modeled by a Dirac delta function
%

Ts=1e-4; %sets the sampling frequency
fo=1; %Sinewave frequency
t=0:Ts:1;

jitter_var_matrix=[1e-10 1e-9 1e-8 1e-7 1e-6 1e-5 1e-4]; %sets the clock jitter power
sigma1=randn(1,length(t)); %Random signal with variance=1
fprintf('\nVariance sigma1^2 is %f',var_sigma1);

for i=1:length(jitter_var_matrix)
jitter_var=jitter_var_matrix(i);
sigmatj=sqrt(jitter_var)*sigma1; %Random signal with variance=sigma_tj
var_sigmatj=var(sigmatj);
fprintf('\nVariance sigmatj is %f',var_sigmatj);
```

```

Dt=sigmatj; %clock jitter Delta t

x=sin(2*pi*fo*t);

x_j=sin(2*pi*fo*(t+Dt)); %Phase modulate the sinewave with random noise


etj=x_j-x; %Noise equals the error signal


SNR_sim=10*log10(var(x)/var(etj)); %SNR calculated in the time domain

SNR_theor=-20*log10(2*pi*fo*sqrt(jitter_var)); %Theoretical SNR formula

                                %given by equation (2.4.3)

SNR_sim_matrix(i)=SNR_sim;

SNR_theor_matrix(i)=SNR_theor;

fprintf('\nSimulation SNR is %f dB',SNR_sim);

fprintf('\nTheoretical SNR is %f dB',SNR_theor);

end


figure;

semilogx(sqrt(jitter_var_matrix),SNR_sim_matrix,sqrt(jitter_var_matrix),SNR_theor_ma
trix);

title('SNR of sinewave sampling due to clock jitter contribution')

xlabel('RMS Jitter (sec)')

ylabel('SNR (dB)')

```

Table A.1: SNR results from theory and simulation.

RMS Jitter (sec)	SNR Theory (dB)	SNR Simulation (dB)
1.00e-5	84.023141	84.036403
3.16e-5	74.023139	74.036403
1.00e-4	64.023133	64.036403
3.16e-4	54.023118	54.036403
1.00e-3	44.023097	44.036403
3.16e-3	34.023308	34.036403
1.00e-2	24.026741	24.036403

This validates (2.4.3) for a sinewave input signal.

Figure A.1: SNR of sinewave sampling due to clock jitter contribution.

Appendix B

B1. Theoretical Derivation of Some Autocorrelation Properties

This section proves

$$r_y(mT_s) = r_x(mT_s) + r_{x'}(mT_s) \cdot r_{t_j}(mT_s) \quad (2.5.10)$$

and

$$r_{x'}(mT_s) = -r_x''(mT_s) \quad (2.5.13)$$

First, we derive (2.5.10) from (2.5.8).

$$e_j(kT_s) = y(kT_s) - x(kT_s) = x'(kT_s)t_j(kT_s)$$

or

$$y(kT_s) = x(kT_s) + x'(kT_s)t_j(kT_s) \quad (2.5.8)$$

and

$$r_y(mT_s) = r_x(mT_s) + r_{x'}(mT_s) \cdot r_{t_j}(mT_s) \quad (2.5.10)$$

The autocorrelation of the discrete signal y is

$$r_y(mT_s) = E[y(kT_s + mT_s)y(kT_s)] \quad (B.1.1)$$

The autocorrelation of $y(kT_s)$ can be also written as

$$\begin{aligned} r_y(mT_s) &= E[y(kT_s + mT_s)y(kT_s)] \\ &= E\left[\left(x(kT_s + mT_s) + x'(kT_s + mT_s)t_j(kT_s + mT_s)\right)\left(x(kT_s) + x'(kT_s)t_j(kT_s)\right)\right] \end{aligned}$$

$$\begin{aligned}
&= E[x(kT_s)x(kT_s + mT_s) + x(kT_s + mT_s)x'(kT_s)t_j(kT_s) + \\
&\quad x'(kT_s + mT_s)t_j(kT_s + mT_s)x(kT_s) + \\
&\quad x'(kT_s)x'(kT_s + mT_s)t_j(kT_s)t_j(kT_s + mT_s)] \tag{B.1.2}
\end{aligned}$$

Let's set $u_1 = x(kT_s + mT_s)x'(kT_s)$, $u_2 = x'(kT_s)x'(kT_s + mT_s)$, $u_3 = x'(kT_s + mT_s)x(kT_s)$, $v_1 = t_j(kT_s)$ and $v_2 = t_j(kT_s)t_j(kT_s + mT_s)$. The variables u_1 and v_1 are uncorrelated because the random process t_j is independent of the input signal. The same holds for variables u_3 and v_1 , u_2 and v_2 . Two uncorrelated variables have zero covariance and therefore

$$E[u_1 \cdot v_1] = E[u_1] \cdot E[v_1] \text{ because } \text{Cov}[u, v] = 0.$$

A proof can be found in A. Papoulis, S. Pillai, *Probability, Random Variables and Stochastic Processes*, McGraw-Hill, 4th Ed., 2002, pp. 210-211.

Also the mean value of the jitter process is zero or $E[t_j(kT_s)] = 0$

Equation (B.1.2) becomes

$$\begin{aligned}
r_y(mT_s) &= E[x(kT_s + mT_s)x(kT_s)] + E[x(kT_s + mT_s)x'(kT_s)t_j(kT_s)] + \\
&\quad E[x'(kT_s + mT_s)t_j(kT_s + mT_s)x(kT_s)] + \\
&\quad E[x'(kT_s)x'(kT_s + mT_s)t_j(kT_s)t_j(kT_s + mT_s)] \\
&= r_x(mT_s) + E[x(kT_s + mT_s)x'(kT_s)] \cdot E[t_j(kT_s)] + \\
&\quad E[x'(kT_s + mT_s)x(kT_s)] \cdot E[t_j(kT_s + mT_s)] + \\
&\quad E[x'(kT_s)x'(kT_s + mT_s)] \cdot E[t_j(kT_s)t_j(kT_s + mT_s)] \\
&= r_x(mT_s) + r_x(mT_s) \cdot r_{tj}(mT_s) \tag{B.1.3}
\end{aligned}$$

The autocorrelation property of (2.5.13) is shown below.

The time derivative of signal $x(t)$ is

$$x'(t) = \lim_{\Delta t \rightarrow 0} \frac{x(t + \Delta t) - x(t)}{\Delta t}$$

The autocorrelation of $x'(t)$ is

$$\begin{aligned} r_{x'}(mT_s) &= E \left[\lim_{\Delta t_1 \rightarrow 0} \frac{x(kT_s + mT_s + \Delta t_1) - x(kT_s + mT_s)}{\Delta t_1} \cdot \lim_{\Delta t_2 \rightarrow 0} \frac{x(kT_s + \Delta t_2) - x(kT_s)}{\Delta t_2} \right] \\ &= \lim_{\Delta t_1, \Delta t_2 \rightarrow 0} \frac{1}{\Delta t_1 \cdot \Delta t_2} E \left[(x(kT_s + mT_s + \Delta t_1) - x(kT_s + mT_s)) \cdot (x(kT_s + \Delta t_2) - x(kT_s)) \right] \end{aligned}$$

After all necessary algebraic manipulations we have

$$r_{x'}(mT_s) = \lim_{\Delta t_1, \Delta t_2 \rightarrow 0} \frac{1}{\Delta t_1 \cdot \Delta t_2} [r_x(mT_s + \Delta t_1 - \Delta t_2) - r_x(mT_s + \Delta t_1) - r_x(mT_s - \Delta t_2) + r_x(mT_s)]$$

Taking the limit with respect to Δt_2 , the first derivative of the autocorrelation becomes

$$r_{x'}(mT_s) = \lim_{\Delta t_1 \rightarrow 0} \frac{1}{\Delta t_1} [-r_x'(mT_s + \Delta t_1) + r_x'(mT_s)]$$

The last equation is just the negative time derivative of $r_x'(mT_s)$, which leads to

$$r_{x'}(mT_s) = -r_x''(mT_s) \tag{B.1.4}$$

B2. Derivations of SNR Formulas

The SNR expressions of a sampling system are derived for four different power spectral densities (PSD):

- A. Baseband rectangular PSD.
- B. Bandpass rectangular PSD.
- C. Baseband raised cosine PSD.
- D. Bandpass raised cosine PSD.

The SNR is found using (2.5.15), which is repeated below.

$$SNR = 10 \log \left(\frac{r_x(0)}{-r_x''(0) \cdot r_{ij}(0)} \right) \quad (\text{B.2.1})$$

A. Baseband Rectangular PSD.

A baseband rectangular PSD is illustrated in Fig. 2.9. The spectrum is bandlimited at f_c and is described by the following equation

$$S_x(f) = \text{rect} \left(\frac{f}{2f_c} \right) \quad (\text{B.2.2})$$

The autocorrelation $r_x(t)$ must be calculated and its second time derivative $r_x''(t)$ at $t=0$.

The remaining term is the sampling clock jitter $r_{ij}(0) = \sigma_{ij}$. The inverse Fourier

Transform of the PSD equals the autocorrelation function. Therefore

$$r_x(t) = 2f_c \cdot \frac{\sin(\omega_c t)}{\omega_c t} \quad (\text{B.2.3})$$

and

$$r_x(0) = 2f_c \quad (\text{B.2.4})$$

The second derivative of (B.2.3) is

$$r_x''(t) = -\frac{\sin(\omega_c t)(\omega_c^2 t^2 - 2) + 2\omega_c t \cos(\omega_c t)}{\pi t^3} \quad (\text{B.2.5})$$

If (B.2.5) is evaluated at $t=0$, an indeterminate form of $0/0$ is obtained. Applying L'

Hopital's rule can remove the indetermination

$$\begin{aligned} \lim_{t \rightarrow 0} r_x''(t) &= \lim_{t \rightarrow 0} \left[-\frac{\frac{d}{dt}(\sin(\omega_c t)(\omega_c^2 t^2 - 2) + 2\omega_c t \cos(\omega_c t))}{\frac{d}{dt}(\pi t^3)} \right] \\ &= \lim_{t \rightarrow 0} \left[-\frac{\omega_c^3 \cos \omega_c t}{3\pi} \right] = -\frac{\omega_c^3}{3\pi} \end{aligned} \quad (\text{B.2.6})$$

Substituting (B.2.4) and (B.2.6) into (B.2.1) the following SNR expression is obtained

$$SNR = 10 \log \left(\frac{2f_c}{\frac{\omega_c^3}{3} \cdot r_{ij}(0)} \right)$$

or

$$SNR = 10 \log \left(\frac{3}{\omega_c^2 \cdot \sigma_{ij}^2} \right) \quad (\text{B.2.7})$$

B. Bandpass Rectangular PSD.

A signal with baseband rectangular PSD is modulated on a carrier at frequency f_0 . The PSD of the modulated signal becomes

$$S_x(f) = \frac{1}{2} \text{rect}\left(\frac{f - f_0}{2f_c}\right) + \frac{1}{2} \text{rect}\left(\frac{f + f_0}{2f_c}\right) \quad (\text{B.2.8})$$

The PSD is shown in Fig. B.1. The bandwidth of the signal is $\text{BW} = 2f_c$.

Figure B.1: Bandpass rectangular Power Spectral Density.

The inverse Fourier Transform of PSD (B.2.8) equals the autocorrelation function $r_x(t)$.

Using the modulation property of the Fourier Transform the autocorrelation is expressed

$$r_x(t) = 2f_c \cdot \frac{\sin(\omega_c t)}{\omega_c t} \cos(\omega_0 t) \quad (\text{B.2.9})$$

and

$$r_x(0) = 2f_c \quad (\text{B.2.10})$$

The second derivative of $r_x(t)$ is

$$\begin{aligned}
 r_x''(t) = & -\frac{\sin(\omega_c t)(\omega_c^2 t^2 - 2) + 2\omega_c t \cos(\omega_c t)}{\pi t^3} \cos(\omega_o t) \\
 & - 2\omega_o \frac{\omega_c t \cos(\omega_c t) - \sin(\omega_c t)}{\pi t^2} \sin(\omega_o t) \\
 & - 2f_c \omega_o^2 \frac{\sin(\omega_c t)}{\omega_c t} \cos(\omega_o t)
 \end{aligned} \tag{B.2.11}$$

The limit of $r_x''(t)$ can be found using L'Hopital's rule for the first two terms of (B.2.11).

$$\lim_{t \rightarrow 0} r_x''(t) = -\frac{\omega_c^3}{3\pi} - 2f_c \omega_o^2 \tag{B.2.12}$$

Substituting (B.2.10) and (B.2.12) into (B.2.1) we get

$$\begin{aligned}
 SNR &= 10 \log \left(\frac{2f_c}{\left(\frac{\omega_c^3}{3\pi} + 2f_c \omega_o^2 \right) \sigma_{ij}^2} \right) \text{ or} \\
 SNR &= 10 \log \left(\frac{1}{\sigma_{ij}^2 \left(f_o^2 + \frac{BW^2}{12} \right)} \right)
 \end{aligned} \tag{B.2.13}$$

or

$$SNR = 10 \log \left(\frac{3}{\sigma_{ij}^2 (f_H^2 + f_L^2 + f_L f_H)} \right) \tag{B.2.14}$$

where $f_H = f_o + f_c$ and $f_L = f_o - f_c$.

C. Baseband Raised Cosine PSD.

Before being transmitted, data are pulse shaped to minimize the effect of InterSymbol Interference (ISI). Usually data are in a non-return to zero (NRZ) format and a pulse shaping filter reduces the spectrum sidelobes. The raised cosine filter is widely used for this purpose and particularly in CDMA. Pulse shaping is split between the receiver and transmitter in such a way that each one has a square root raised cosine filter. When a signal is filtered with a root raised cosine filter the output has a raised cosine PSD. The PSD is thus

$$S_x(f) = \begin{cases} \frac{1}{2W}, & 0 \leq |f| < f_1 \\ \frac{1}{4W} \left[1 - \sin \left(\frac{\pi(|f| - W)}{2W - 2f_1} \right) \right], & f_1 \leq f < 2W - f_1 \\ 0, & \text{otherwise} \end{cases} \quad (\text{B.2.15})$$

where a is the roll-off factor, $W = \frac{1}{2T_b}$ and $f_1 = W - a$. Variable T_b is the chip rate and

$\omega_b = 2\pi R_b$, where $R_b = 1/T_b$ is the data rate after root raised cosine interpolation.

The autocorrelation function $r_x(t)$ equals the inverse Fourier Transform of (B.2.15)

$$r_x(t) = \sin c(2Wt) \frac{\cos(2\pi a W t)}{1 - 4a^2 W^2 t^2} \quad (\text{B.2.16})$$

In order to simplify calculation the value of a is assumed to be $a=0.5$.

The value of (B.2.16) at $t=0$ is

$$r_x(0) = \lim_{t \rightarrow 0} r_x(t) = 1 \quad (\text{B.2.17})$$

The first derivative of (B.2.16) takes the form

$$r_x'(t) = \frac{\omega_b t \cos\left(\frac{\omega_s t}{2}\right) - 2 \sin\left(\frac{\omega_b t}{2}\right)}{\omega_b t^2} \cdot \frac{\cos(\pi W t)}{1 - 4W^2 t^2} + \frac{\sin\left(\frac{\pi t}{T_b}\right)}{\frac{\pi t}{T_b}} \cdot \frac{-\pi W \sin(\pi W t)(1 - 4W^2 t^2) + 8W^2 t \cos(\pi W t)}{1 - 4W^2 t^2} \quad (\text{B.2.18})$$

After performing necessary manipulations the second derivative is

$$r_x''(t) = \frac{-\frac{\omega_b^2 t^2}{2} \sin\left(\frac{\omega_b t}{2}\right) - 2\omega_b t \cos\left(\frac{\omega_b t}{2}\right) - 4 \sin\left(\frac{\omega_b t}{2}\right)}{\omega_b t^3} \cdot \frac{\cos(\pi W t)}{1 - 4W^2 t^2} + 2 \frac{\omega_b t \cos\left(\frac{\omega_b t}{2}\right) - 2 \sin\left(\frac{\omega_b t}{2}\right)}{\omega_b t^2} \cdot \frac{-\pi W \sin(\pi W t)(1 - 4W^2 t^2) + 8W^2 t \cos(\pi W t)}{(1 - 4W^2 t^2)^2} - \pi W \frac{\pi W \cos(\pi W t)(1 - 4W^2 t^2) - 8W^2 t \sin(\pi W t)}{(1 - 4W^2 t^2)^2} + 8W^2 \frac{(1 - 4W^2 t^2)[\cos(\pi W t) - \pi W t \sin(\pi W t)] + 16W^2 t^2 \cos(\pi W t)}{(1 - 4W^2 t^2)^3} \quad (\text{B.2.19})$$

The value of (B.2.19) at zero is found by taking the limit and using L'Hopital's rule when necessary.

$$\lim_{t \rightarrow 0} r_x''(t) = -\frac{\omega_b^2}{12} - W^2(\pi^2 - 8) \quad (\text{B.2.20})$$

Substituting (B.2.17) and (B.2.20) into (B.2.1) we get the SNR expression

$$SNR = 10 \log \left(\frac{1}{\left(\frac{\omega_b^2}{12} + W^2 (\pi^2 - 8) \right) \sigma_{ij}^2} \right) \quad (B.2.21)$$

D. Bandpass Raised Cosine PSD.

As in the bandpass rectangular PSD, the bandpass raised cosine PSD can be represented as

$$S_{x,BP}(f) = \frac{1}{2} S_x(f - f_o) + \frac{1}{2} S_x(f + f_o) \quad (B.2.22)$$

with

$$r_{x,BP}(t) = \sin c(2Wt) \frac{\cos(2\pi a W t)}{1 - 4a^2 W^2 t^2} \cos(\omega_o t) \quad (B.2.23)$$

The same assumption concerning the value of a is made here as well $a=0.5$.

Equation (B.2.23) gives

$$r_{x,BP}(0) = \lim_{t \rightarrow 0} r_{x,BP}(t) = 1 \quad (B.2.24)$$

Obviously, the second derivative changes since we account for the modulation factor of the cosine function.

$$\begin{aligned}
r_{x,BP}''(t) = & \frac{-\frac{\omega_b^2 t^2}{2} \sin\left(\frac{\omega_b t}{2}\right) - 2\omega_b t \cos\left(\frac{\omega_b t}{2}\right) - 4 \sin\left(\frac{\omega_b t}{2}\right)}{\omega_b t^3} \cdot \frac{\cos(\pi W t)}{1 - 4W^2 t^2} \cdot \cos(\omega_o t) + \\
& 2 \frac{\omega_b t \cos\left(\frac{\omega_b t}{2}\right) - 2 \sin\left(\frac{\omega_b t}{2}\right)}{\omega_b t^2} \cdot \\
& \left[\frac{-\pi W \sin(\pi W t)(1 - 4W^2 t^2) + 8W^2 t \cos(\pi W t)}{(1 - 4W^2 t^2)^2} \cos(\omega_o t) - \omega_o \frac{\cos(\pi W t)}{1 - 4W^2 t^2} \sin(\omega_o t) \right] + \\
& \left[-\pi W \frac{\pi W \cos(\pi W t)(1 - 4W^2 t^2) - 8W^2 t \sin(\pi W t)}{(1 - 4W^2 t^2)^2} + \right. \\
& \left. 8W^2 \frac{(1 - 4W^2 t^2) [\cos(\pi W t) - \pi W t \sin(\pi W t)] + 16W^2 t^2 \cos(\pi W t)}{(1 - 4W^2 t^2)^3} \right] \cos(\omega_o t) - \\
& 2\omega_o \sin(\omega_o t) \frac{-\pi W \sin(\pi W t)(1 - 4W^2 t^2) + 8W^2 t \cos(\pi W t)}{(1 - 4W^2 t^2)^2} - \\
& \omega_o^2 \frac{\cos(\pi W t)}{1 - 4W^2 t^2} \cos(\omega_o t)
\end{aligned} \tag{B.2.25}$$

The limit of (B.2.25) as t approaches zero is

$$\lim_{t \rightarrow 0} r_{x,BP}''(t) = -\frac{\omega_b^2}{12} - W^2(\pi^2 - 8) - \omega_o^2 \tag{B.2.26}$$

Substituting (B.2.24) and (B.2.26) into (B.2.1) we get the SNR expression for bandpass raised cosine PSD.

$$SNR = 10 \log \left(\frac{1}{\left(\frac{\omega_b^2}{12} + W^2(\pi^2 - 8) + \omega_o^2 \right) \sigma_{ij}^2} \right) \tag{B.2.27}$$

Appendic C

C1. Phase Noise Power Calculation

The spectral purity of a Local Oscillator (LO) is characterized by phase noise data at certain frequency offsets from the carrier frequency. The power is expressed in dBc relative to the carrier power.

Let's assume a LO with the following phase noise profile (Fig. C.1).

Figure C.1: Phase noise profile of a LO.

The total noise can be found by integrating the power spectral density $S(f)$ over the bandwidth of interest B .

For the example shown in Fig. C.1 the total power is

$$\sigma_{\phi}^2 = \int_1^{10^6} S(f) df$$

The integral is calculated in each region separately because the shape of the curve changes. Before integrating phase noise density, values must be converted to linear.

$$-77 \text{ dBc} \rightarrow 1.995 \cdot 10^{-8}$$

$$-95 \text{ dBc} \rightarrow 3.162 \cdot 10^{-10}$$

$$-135 \text{ dBc} \rightarrow 3.162 \cdot 10^{-14}$$

The integral is

$$P_1 = 1.995 \cdot 10^{-8} \int_{10}^{10^3} \frac{1}{f^3} df = 9.98 \cdot 10^{-11} \text{ rad}^2$$

$$P_2 = 3.162 \cdot 10^{-10} \int_{10^3}^{10^4} \frac{1}{f^2} df = 2.85 \cdot 10^{-13} \text{ rad}^2$$

$$P_3 = 3.162 \cdot 10^{-14} \int_{10^4}^{10^6} df = 3.13 \cdot 10^{-18} \text{ rad}^2$$

Hence,

$$\sigma_\phi^2 = P_1 + P_2 + P_3 = 10^{-10} \text{ rad}^2 \text{ or}$$

$$\sigma_\phi^2 = -100 \text{ dBc}$$

The rms value of phase noise is

$$\sigma_\phi = 1.05 \cdot 10^{-5} \text{ rad (rms)}$$

For a LO frequency of $f=132 \text{ MHz}$, the time jitter is

$$\sigma_{ij} = \frac{\sigma_\phi}{2\pi f} = 0.012 \text{ ps (rms)}$$