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A $3\mu\text{m}$ Σ - Δ MODULATOR
AND DUAL MODULUS DIVIDER FOR USE
IN Σ - Δ MODULATED FRACTIONAL-N
FREQUENCY SYNTHESIS

MING ZHONG, M. ENG.

A thesis submitted to the Faculty of
Graduate Studies and Research in partial fulfillment
of the requirements for the degree of
Master of Engineering

Faculty of Engineering
Department of Electronics
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Ottawa, Ontario

April 22, 1991
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The undersigned recommend to the Faculty of Graduate Studies and Research acceptance of the thesis, "A $3\mu\text{m}$ Σ - Δ Modulator and Dual Modulus Divider for Use in Σ - Δ Modulated Fractional-N Frequency Synthesis" submitted by Ming Zhong in partial fulfillment of the requirements for the degree of Master of Engineering.

A handwritten signature in cursive script, reading "David J. Walkey". The signature is written in dark ink on a white background.

David J. Walkey, Thesis Supervisor

A handwritten signature in cursive script, reading "J. S. Wight". The signature is written in dark ink on a white background.

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April 22, 1991

Abstract

This thesis describes the logic circuit design, theoretical analysis, computer simulation, standard cell layout and testing of a noise shaping CMOS fractional N frequency divider. The complete circuit has been integrated on two chips using the Northern Telecom CMOS3 3 μm double metal process.

Measured results on the dual modulus divider chip indicate that the circuit is capable of dividing input signals at frequencies up to 250 MHz. When used in conjunction with the digital Σ - Δ bitstream generator chip, the dual modulus divider provides noise shaping to suppress noise around the divided frequency, making it suitable for use in phase locked loop frequency synthesizer applications.

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Chapter 1

INTRODUCTION

Practically all modern signal generators and radio communication equipment make heavy use of frequency synthesizers. Most of the new frequency synthesizers utilize the phase locked loop (PLL). Integrating the PLL on a VLSI chip can greatly reduce the cost of frequency synthesizers.

A basic PLL is shown in Fig.1.1. It includes a phase detector, a low-pass filter, a voltage-controlled oscillator (VCO) and a frequency divider. The function of a PLL is to track small differences in phase between the input and feedback signal. The phase detector measures the phase difference between its two inputs. The phase detector output is then filtered by the low-pass filter and applied to the VCO. The VCO input voltage changes the VCO frequency in a direction that reduces the phase difference between the input signal and the output of the VCO.

The loop comes to equilibrium at a fixed phase error (this error is zero for a second order loop) only when the relation between output frequency f_{out} and reference frequency f_{ref} is:

$$f_{out} = N \cdot f_{ref} \quad (1.1)$$

Under this condition, the loop is said to be locked to the reference. It can be seen from Eq-1.1 that we can achieve a variable output frequency from a single reference

Figure 1.1: Block diagram of a basic PLL.

frequency by changing N . Since N is an integer, the step size of frequency equals f_{ref} . In order to obtain fine frequency resolution the reference frequency must be small. Since the loop settling time is directly proportional to the reference period, the decrease of reference frequency means an increase of settling time.

If N can be made to assume fractional values, the frequency resolution of f_{out} can be made arbitrarily small and the settling time problem is solved. In the case of high frequency telecommunication, the ratio between carrier frequency and channel bandwidth is very large, so fractional division PLL synthesizers are especially useful.

According to [4] the basic requirements for a frequency divider are:

1. A high frequency of operation.
2. A broadband operation.
3. A variable division ratio.
4. Zero rf (radio frequency) output in the absence of an rf input signal.
5. Low cost.

There are various ways to realize a variable ratio divider. Several examples have been given in [10]. Since $3\ \mu\text{m}$ CMOS digital circuits typically operate at clock speeds of up to 30MHz, higher frequencies bipolar devices are usually used. In this thesis the design, implementation and testing of a novel high speed digital CMOS fractional N divider, shown in block diagram form in Fig.1.2, is described.

Figure 1.2: Block diagram of a digital fractional N divider.

The divider includes one clocked inverter ring oscillator as the prescaler (the divide-by-3,4 block, which divides either by 3 or 4 depending on its input state), one digital Σ - Δ modulator as modulus controller and some control blocks. A digital Σ - Δ modulator has the characteristic of noise shaping and it can generate a pseudo random bit stream, this bit stream (the overflow of the Σ - Δ modulator) is used as the control command to make the division ratio of the prescaler switch between three and four. Thus, after the Divide-by-16 block, the division ratio N can vary from 48 to 64. The second function of the Divide-by-16 block is to generate some control signals for the Σ - Δ modulator. Since the overflow probability of the digital Σ - Δ modulator is a fractional number, by changing the value of the input data the division ratio N can

be a fractional number. This fractional N divider (Fig.1.2) has been implemented on two chips. One is the dual modulus divider, the other is the digital Σ - Δ modulator and the Divide-by-16 block. Simulation and chip testing show that the input clock frequency (f_{ref}) can be higher than 190MHz. In a PLL, with the exception of the VCO and the frequency divider, all devices are working at the frequency lower than or equal to $\frac{f_{ref}}{N}$. For the sake of power consumption, those devices are usually implemented in CMOS. Since the fractional N divider shown in Fig.1.2 is also in CMOS, it has the advantages of lower power consumption and lower complexity than that of bipolar devices, and easier interface with other CMOS parts. In addition, the characteristic of the Σ - Δ bitstream provides noise shaping of the divided down signal, which is an important advantage of the $\Sigma \Delta M$ system for frequency synthesizer application.

The design in this thesis is based on the ideas given in [1,2]. The thesis includes five chapters. Chapter 1 is the introduction. Chapter 2 presents some examples of divide-by- n , $(n+1)$ counters and background about analog Σ - Δ modulators. Chapter 3 describes a high speed dual modulus divider, its logic design, timing analysis, simulation, chip layout and testing results. Chapter 4 gives the design of a second order digital Σ - Δ modulator. Its logic is verified first by using a Logic Cell Array (LCA) and then chip testing. At the end of Chapter 4, the two chips are connected together to form a fractional N frequency divider system and the system is then tested. In order to distinguish from the chip testing, this system level testing is defined as joint testing. The conclusions and some suggestions for future work are then presented in Chapter 5.

Chapter 2

BACKGROUND OF $N, (N+1)$ DIVISION AND SIGMA-DELTA MODULATION

This chapter reviews dual modulus division and Σ - Δ modulation. Since a divide by $n, (n+1)$ counter is necessary in a fractional N divider, sections 2.1 and 2.2 introduce some known methods to realize the divide by $n, (n+1)$, which provide a comparison and a better understanding of the new method which will be described in the next chapter. Sections 2.3 to 2.5 present the basic principles of analog delta modulation and first and second order Σ - Δ modulation. The development of an equivalent digital second order Σ - Δ modulator (Chapter 4) is based on those principles.

2.1 Presettable Counter

Fig.2.1 (a) shows a presettable divide-by- N counter, where N is the modulus of the counter. Its value can be changed, depending on the input *Data* signal. Table 2.1 gives the relation between N and *Data* signal.

J_1 to J_5 are the preset data inputs. If *PRESET* signal is 'high', J_i controls D *Flip - Flop* (DFF_i), where $i = 1, \dots, 5$. If *PRESET* signal is 'low', the working

Figure 2.1: RCA-CD4018B CMOS presettable divide-by-N counter. (a) Logic diagram. (b) Waveform of divide by 8,9.

N	2	4	6	8	10
Data	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	$\overline{Q_4}$	$\overline{Q_5}$
N	3	5	7	9	
Data	$\overline{Q_2} \cdot \overline{Q_1}$	$\overline{Q_3} \cdot \overline{Q_2}$	$\overline{Q_4} \cdot \overline{Q_3}$	$\overline{Q_5} \cdot \overline{Q_4}$	

Table 2.1: The relationship between N and $Data$ in RCA-CD4018B.

states of DFFs will not be affected by the value of J_i .

Assuming $DATA = \overline{Q_5} \cdot \overline{Q_4}$, the counter will divide with a modulus of nine. Usually each output $\overline{Q_i}$ is a pulse signal and its frequency equals one ninth of the clock frequency. One can control the counter to occasionally divide by a modulus of eight by presetting J_i . For example, if at one cycle of $\overline{Q_1}$, setting J_1 'low' at the eighth clock pulse will result in $\overline{Q_1}$ changing to 'low' one pulse earlier. Thus, this period of $\overline{Q_1}$ will be eight times that of the clock period. This is a modulus eight division. Fig.2.1 (b) shows the waveforms of the divide by 8,9 operation.

2.2 Cycle Swallower

A cycle swallower is shown in Fig.2.2(a). The swallow trigger input is a control signal. If it is 'high', the output will be the same as the clock signal. If it is 'low', one pulse will be removed from the output, Fig.2.2(b). Assuming a divide-by-two counter is connected to the cycle swallower and the cycle swallower output is used as a clock

(a) Logic diagram.

(b) Waveforms.

Figure 2.2: A cycle swallower.

signal, one can get divide-by-2,3 output.

Another example is the SP8720 ECL divide-by-3,4 counter, which is shown in Fig.2.3. From its truth table (Table 2.2), it can be seen that if both $\overline{PE_1}$ and $\overline{PE_2}$ are 'low', the division ratio is four, while in any other case the ratio is three.

A high speed CMOS dual modulus frequency divider, which can work at up to 165 MHz, has been reported in [32,33]. Fig.2.4 (a) shows its logic diagram. The first stage, Fig.2.4 (b), implements a memory-cell-like D-latch configuration and works on

Figure 2.3: SP8720 ECL divide-by-3,4 counter.

$\overline{PE}_1$	$\overline{PE}_2$	Division Ratio
L	L	4
H	L	3
L	H	3
H	H	3

Table 2.2: Truth table for control inputs of SP8720.

(a) Logic diagram

(b) The first Stage

Figure 2.4: A high speed CMOS divide by 15,16 frequency divider [32,33].

a single phase clock, which does not have clock skew problem. The simplicity of the structure allows high frequency operation. The frequency divider modules can be switched between 15 and 16 by varying the 15-16 control signal. This example also belongs to the family of pulse swallowers.

2.3 Delta Modulation System

A delta modulation system can be thought of as a Differential Pulse Code Modulation (DPCM) system with a one bit quantizer. Its basic scheme is shown in Fig.2.5.

Figure 2.5: Delta modulator [26].

The quantizer output, Q , is 'high' if the difference between the input signal, $X(t)$, and feedback signal, $Y(t)$, is positive, and Q is 'low' if the difference is negative [26]. The high oversampling ratio and loop gain enables the feedback signal, $Y(t)$, to "track" the input signal, $X(t)$. The decoding of the binary pulses of Q' at receiver is accomplished simply by using an integrator (accumulator) to produce a waveform, $Y'(t)$, which differs from the original signal by the error signal, $E(t)$, in the encoder. The final decoded signal, $O(t)$, is obtained by low-pass filtering $Y'(t)$ to remove any noise due to quantization effects in the encoder which lie outside the message band.

The appeal of delta modulation is its simplicity and stability. According to [22], the noise in this system can be classified into three categories

1. *Slope overload noise* occurs when the slope of the input signal is too great to be tracked by the encoder.

2. *Idling noise* happens when there is no input signal and the output Q of the encoder consists of a sequence of alternate local ones and zeros.
3. *Quantization noise* occurs when the encoder is tracking correctly and arises from the voltage and fine quantization used in the encoding process.

An important parameter in describing the performance of the delta modulation system is the decoded Signal to Noise Ratio (SNR). The dynamic range and SNR of the delta modulator are inversely proportional to the input signal frequency, since there is an integrator at the receiving end which can cause error accumulation when the system is subjected to transmission disturbances [17]. By inserting another integrator into the delta modulator encoder, the disadvantages can be eliminated. The new configuration is called a sigma-delta modulation system.

2.4 First Order Sigma-Delta Modulation

The first order Σ - Δ modulator is a modification of the delta modulator discussed in section 2.3. It consists of a delta modulator preceded by an integrator. Fig.2.6 (a) and (b) show the encoder and the decoder respectively.

From Fig.2.6 (a), one can write:

$$E(t) = \int X(t) dt - Y(t) = \int X(t) dt - \int Q dt = \int [X(t) - Q] dt.$$

Therefore, Fig.2.6 (a) and Fig.2.6 (c) are equivalent. Fig.2.6 (d) is the discrete-time model of a Σ - Δ modulator, whereas $e(Z)$ stands for the quantization noise. $Q(Z)$ is the encoder output which includes signal component, $S(Z)$, and noise component, $n(Z)$. $H(Z)$ is the transfer function of the integrator,

$$H(Z) = \frac{1}{1 - Z^{-1}} \quad (2.1)$$

Figure 2.6: First order Σ - Δ modulator.

In order to obtain the transfer function of both signal and noise, it is assumed that the input signal $X(Z)$, and quantization noise $e(Z)$, are uncorrelated. $Q(Z)$ and $e(Z)$ are both normalized signals. Based on these assumptions and using the standard result for a feedback system, the Signal Transfer Function (STF) is:

$$\frac{S(Z)}{X(Z)} = \frac{H(Z)}{1 + H(Z)}. \quad (2.2)$$

The Noise Transfer Function (NTF) is given by:

$$\frac{e(Z)}{n(Z)} = \frac{1}{1 + H(Z)}. \quad (2.3)$$

Substituting $H(Z)$ from Eq-2.1 into Eq-2.2 and Eq-2.3,

$$\frac{S(Z)}{X(Z)} = \frac{H(Z)}{1 + H(Z)} = \frac{1}{2 - Z^{-1}}, \quad (2.4)$$

and

$$\frac{e(Z)}{n(Z)} = \frac{1}{1 + H(Z)} = \frac{1 - Z^{-1}}{2 - Z^{-1}}, \quad (2.5)$$

From Eq-2.4 and Eq-2.5, it can be seen that the STF has a low-pass filter response, and the NTS has a high-pass filter response. This means that the encoder discriminates noise from signal or the noise contribution in the signal band is reduced. This effect is often called "noise shaping".

Σ - Δ modulation exhibits improved performance over Delta modulation in several ways:

1. The overload characteristic is independent of the frequency of the input signal [22].
2. Since an integrator functions as a low-pass filter (Fig.2.7 shows typical frequency responses of a integrator and a LPF), the integrator in the encoder adds a high gain to the low frequency signal. Meanwhile, the quantization noise is distributed outside the signal band by the noise shaping integration. The higher the oversampling ratio, the better the noise shaping performance [27].
3. Since the integration and differentiation in a decoder cancel each other, there is no integration process involved in the demodulation. There will therefore be no accumulative error due to transmission disturbances [17].

Based upon the above discussion of the first order Σ - Δ modulator, it can be understood that increasing the oversampling ratio will achieve better noise shaping and higher resolution A/D conversion. However, small oversampling ratios are generally desirable, since for a given maximum bandwidth of VLSI technology, smaller oversampling ratios allow one to handle signals of wider spectra. This limitation can be overcome by implementing higher order Σ - Δ modulation systems [21].

Figure 2.7: The frequency responses of Integrator and LPF.

2.5 Second Order Sigma-Delta Modulation

A double integration or second order Σ - Δ modulation encoder is shown in Fig.2.8 (a). Fig.2.8 (b) shows its Z domain block diagram. Since the additional integrator moves the quantization noise further out of band, the resolution or SNR is enhanced and the requirement for high oversampling ratios is relaxed. The cost of this architecture is the increased complexity and tighter requirement of circuit accuracy to ensure system stability and good performance. The saturation problem of integrators may introduce additional noise and decrease the SNR. However, for a double loop system, this additional cost is generally moderate. By carefully selecting circuit parameters, the zeros and poles of the system can lie in a suitable position and the function of the system can meet the expected specification.

Further improving the SNR versus bit-rate can be achieved by implementing the N th order Σ - Δ modulation, where $N > 2$, but stability is a major problem associated with higher order Σ - Δ modulation. These issues are not the subject of this thesis. For more details, one can refer to [23-31].

Figure 2.8: Second Order Sigma-Delta Modulator.

Chapter 3

DESIGN AND ANALYSIS OF THE FREQUENCY DIVIDER

Chapter 2 has discussed a few examples of dual modulus dividers which all rely on standard digital operation to perform the division. Chapter 3 will present a new topology for the dual modulus divider which uses a modified ring oscillator clocked by the incoming signal to perform the first division. This allows full advantage to be taken of the inherent high speed of inverters.

Fig.3.1 is the block diagram of the frequency divider which includes four parts. The input signal of the Clocked Ring Oscillator (Clock) is a high frequency signal, usually from the VCO in Fig.1.1. The function of the Clocked Ring Oscillator block is to divide the clock frequency by a factor of three or four. The frequency of the output signal (Test) is then decreased by a factor of four by the Divide-by-4 block. Since the digital Σ - Δ modulator in Fig.1.2 is absent in Fig.3.1, it is needed that an alternate way to obtain the division ratio control signal. The U Signal Generator block in Fig.3.1 is used for this purpose. The U Signal Generator constructs a control signal from the output of the Divide-by-4 block and an input signal Y , which then controls the division ratio through the logic block. In Fig.3.1, only the Clocked Ring Oscillator, Switches and Logic block belong to the dual modulus frequency divider.

Figure 3.1: Block diagram of the frequency divider.

The Divide-by-4 block is used to obtain a lower frequency signal, which is easier to test than the high frequency output from the ring oscillator. The Divide-by-4 block is equivalent to the Divide-by-16 block in Fig.1.2. After the Divide-by-4 block, instead of from 48 to 64, the division ratio N can be from 12 to 16. The function of a Divide-by-4 block and U Signal Generator can be replaced by the Divide-by-16 block and the digital Σ - Δ modulator in Fig.1.2 and which will be discussed in next chapter. The design and work of each block in Fig.3.1 is discussed in the following sections.

3.1 Ring Oscillator and Switches

The clocked inverter consists of two $PMOS$ transistors and two $NMOS$ transistors, connected as shown in Fig.3.2. The clocked inverter is the basic element in the ring oscillator block and it is also used as a switch in the switches block.

When the clocked inverter is used as an inverter, the two inputs $V_{p\text{clock}}$ and $V_{n\text{clock}}$

Figure 3.2: Clocked inverter circuit.

are connected together (V_{clock}). The output V_{out} depends on both input V_{in} and the clock signal V_{clock} . If both V_{in} and V_{clock} are 'low', the output is 'high'. If both V_{in} and V_{clock} are 'high', the output is 'low'. In other cases, the output will be in a high impedance state and will remain unchanged. The reason for these and a more detailed discussion will be given in Section 3.5.

When the clocked inverter is used as a switch, the $V_{p\text{clock}}$ and $V_{n\text{clock}}$ will remain as separate inputs. The truth table for the switch is in Table 3.1 [1], where ‘Z’ means the high impedance state. If V_{out} is ‘Z’, the switch is ‘off’. Otherwise the switch is ‘on’.

V_{in}	V_{pclock}	V_{nclock}	V_{out}
0	0	0	1
0	0	1	1
0	1	0	Z
0	1	1	Z
1	0	0	Z
1	0	1	0
1	1	0	Z
1	1	1	0

Table 3.1: Truth table of a clocked inverter switch.

Fig.3.3 shows a ring oscillator and switches circuit. The ring oscillator consists of three clocked inverters. The output of each stage is also connected to a clocked inverter which is used as a switch. The clock input of the ring oscillator is a high frequency signal which is also the output of the VCO, and the output of each stage of the clocked ring oscillator is this frequency divided by three. The clock input of the three switches is controlled by the phase control circuit. The outputs of the three switches are connected together and only one switch is on at any time.

Although the ring oscillator does have a stable operating point with all outputs at $V_{DD}/2$, in practice noise and other nonidealities such as transistor mismatch will force the circuit out of this state and oscillation will build up.

Fig.3.4 shows the expected waveform of each output. It can be seen that the three inverter outputs can have only one of the following six states at each half clock cycle:

Figure 3.3: Clocked inverter ring oscillator.

	1	2	3	4	5	6	1
A:	0	0	0	1	1	1	0
B:	0	1	1	1	0	0	0
C:	1	1	0	0	0	1	1

At the beginning of the oscillation, the three inverters are allowed to enter one of the six states. Then the six states are repeated in order. It can be seen from Fig.3.4 that the total time length of the six states equals one period of a inverter's output or three periods of clock signal. Assuming that T_1 is the period of the clock signal and T_2 is the period of each inverter's output, then

$$T_2 = 3 \times T_1, \quad (3.1)$$

which is a *divide-by-3* function.

The relation between the output of the three inverters are that the transition of B occurs after C, and the transition of A occurs after B.

Figure 3.4: Waveform of ring oscillator outputs.

Fig.3.4 also shows the waveform of the three switch outputs. One can control the switches to make the output sequence C, B, A, C. When the output is switching from one phase to another, the period of the output is T_3 instead of T_2 and

$$T_3 = 4 \times T_1. \quad (3.2)$$

This is the function *divide-by-4*. Thus the relation between the frequency of clock signal and the frequency of the output signal is *divide-by-3* or *4*.

One also can control the switches to make the output sequence C, A, B, C. During this time, when the output switches from one phase to another, the period of the output is T_4 and $T_4 = 2 \times T_1$. This is the function *divide-by-2*. Thus the relation between the frequency of clock signal and the frequency of the output signal also can be *divide-by-3* or *2*.

It can be seen from the above discussion that the function of the ring oscillator

and switches circuit is a frequency divider whose division ratio can be three or four (or two or three alternately).

The output signal of this circuit is used as the clock signal for all latches and D-flip-flops in the logic block, *Divide-by-4* circuit and *U* Signal Generator circuit shown in Fig.3.1. Fig.3.3 shows that to accommodate the large loading on the output, three stages of inverter drivers have been used.

3.2 Control Logic Block

The control logic block (Fig.3.1) uses the output of the *U* signal generator as its input signal, and its output is used to control the on/off state of the three switches. It includes two parts: Latches and Decoder. The Latches block uses the control information from the *U* Signal Generator to give a series of control codes. The Decoder block changes this code into the control signals which are used to set the division ratio to be three or four in the Ring Oscillator block.

The function of the latches circuit is to generate the code (T_0 , T_1) which is used as the input of the decoder circuit. It is formed by four latches and two logic blocks, as shown in Fig.3.5.

As shown in [1], in order to guarantee that the ring oscillator will switch phases at the proper time, thereby preventing glitches in the output waveform, Latch-1 and latch-3 are triggered by a falling-edge, and latch-2 and latch-4 are triggered by a rising-edge. The states of output T_0 , T_1 should be only '00', '01' or '10', i.e., state '11' is not allowed. The signal *U* which comes from the *U* Signal Generator block controls the time when T_0 and T_1 are allowed to switch states. If *U* is '1', T_0 and T_1 can change, but if *U* is '0', T_0 and T_1 must not change. Based on these requirements, the logic equations of D_0 and D_1 are as following:

Figure 3.5: Circuit diagram of Latches block.

$$D_0 = \overline{T_1} \cdot T_0 U + T_0 \overline{U} = \overline{\overline{\overline{T_1} \cdot T_0 U} \cdot \overline{T_0 \overline{U}}} \quad (3.3)$$

$$D_1 = \overline{T_1} T_0 U + T_1 \overline{U} = \overline{\overline{\overline{\overline{T_1} T_0 U} \cdot \overline{T_1 \overline{U}}}} \quad (3.4)$$

These logic equations can be realized using two 2 input NAND and one 3 input NAND gates. Since T_0 , T_1 are triggered by the falling-edge of clock, it is required that D_0 , D_1 should change one step before T_0 , T_1 . In other words, D_0 , D_1 should be triggered by the rising-edge of clock. To achieve this, the output T'_0 of latch-2 is used as the T_0 in D_0 , D_1 and the $\overline{T_1}$ is replaced by the output $\overline{T'_1}$ of latch-4. Thus, Eq-3.3 and Eq-3.4 become:

$$D_0 = \overline{\overline{\overline{\overline{T'_1} \cdot T'_0 U} \cdot \overline{T_0 \overline{U}}}}, \quad (3.5)$$

$$D_1 = \overline{T_1' T_0' U} \cdot \overline{T_1 U}. \quad (3.6)$$

Fig.3.6 shows the SPICE simulation result of Latches block with a clock frequency of 50MHZ.

Figure 3.6: Simulation result of Latches block.

As mentioned in Section 3.1, there are three switches in the ring oscillator block, each one controlling one phase of the ring oscillator. They work alternately to change the frequency division ratio of the output signal from N to $N + 1$. In our case N equals three.

A decoder circuit is used to translate the output code of the latches circuit (T_0 , T_1) into the appropriate switch signals. The inputs of the decoder are therefore the outputs of latches (T_0 , T_1) and the decoder outputs are the switch-control signals $P_i, \overline{P_i}$ ($i = 1, \dots, 3$). The relation between T_i and P_i are:

$T_0 T_1$	$P_1 \overline{P_1}$	$P_2 \overline{P_2}$	$P_3 \overline{P_3}$
0 0	1 0	0 1	0 1
1 0	0 1	1 0	0 1
0 1	0 1	0 1	1 0

If $P_i = '1'$ and $\overline{P_i} = '0'$, the switch is 'on'. If $P_i = '0'$ and $\overline{P_i} = '1'$, the switch is 'off'. Thus, if T_0, T_1 are '00', only switch-1 is on. If T_0, T_1 are '10', only switch-2 is on. If T_0, T_1 are '01', only switch-3 is on.

To ensure that the output of the Ring Oscillator block ($Test_0$ in Fig.3.3) switches from one phase to another phase only when it is 'low', the switches should finish turning 'on' or 'off' after the falling edge of the $Test_0$ signal and before its rising edge [1]. However, the phase control block introduces a delay between the falling edge of $Test_0$ and P_i which can cause failure of the circuit. The solution is to make the switch start turning earlier. If the turning begins at the rising edge of $Test_0$ and finishes at its falling edge, as long as the delay is less than three input clock periods (T_2 in Fig.3.4) the switches can change state in time and glitches in $Test_0$ signal can

Figure 3.7: Decoder circuit.

be avoided. Based on this analysis, all P_i signals must change at a falling edge and all $\overline{P}_i$ must change at a rising edge. Therefore:

$$P_1 = \overline{T_0} + T_1 \quad \overline{P_1} = \overline{T_0} \cdot \overline{T_1} \quad (3.7)$$

$$P_2 = \overline{T_0} + T_1 \quad \overline{P_2} = \overline{T_0} \cdot \overline{T_1} \quad (3.8)$$

$$P_3 = \overline{T_0} + \overline{T_1} \quad \overline{P_3} = \overline{T_0} \cdot T_1 \quad (3.9)$$

Fig. 3.7 is the circuit diagram of the Decoder.

Notice that the latches are clocked by $Test_3$ and those with falling edges which come before its rising edge relative to $Test_0$. Since P_i signals control the NMOS

transistors in the switches, the $\overline{P_i}$ signals control the PMOS transistors, which means NMOS transistors should change state before the PMOS transistors. But an NMOS transistor needs a logic 'H' to turn it on, and a PMOS transistor needs a logic 'L' to turn it on, while in this circuit, the signal change from 'low' to 'high' is slower than that from 'high' to 'low'. Hence, the two control signals can arrive at almost the same time. This means the PMOS transistor and the NMOS transistor in a switch can be turned on at the same time. But, for the same reason, they can not be turned off at the same time. This means it is possible that there are two or even three switches on for a short period of time. In this case, since the three phases are connected together, for two reasons the relation between them is equivalent to Line-AND. The two reasons are:

1. The switch is in fact a clocked inverter, so its output is the compliment of its input .
2. If the outputs of two inverters are connected together, and the input of inverter-1 V_{in1} becomes low and the input of inverter-2 V_{in2} becomes high at the same time, the output voltage level depends on the turning speed of NMOS and PMOS transistors. If the NMOS and PMOS transistors have the same width to length ratio, NMOS transistor will turn on first, thus the output will be low. If the size of the PMOS transistor is more than two times larger than the NMOS transistor, PMOS transistor will turn on first, thus the output will be high.

Also, since at any time at least one phase is 'H', the output of Ring Oscillator block ' $Test_0$ ' should stay at 'low'.

After the switches have finished turning, only one switch becomes 'on', the signal $Test_0$ goes to 'high' but adjusts to the next phase.

From the above analysis, it can be concluded that the switch control signal triggered by different edges makes the circuit work in proper logic as long as the delay of the Phase Control block is less than three input clock periods (T_2 in Fig.3.4). Fig.3.8 shows the simulation results of the Decoder circuit.

Figure 3.8: Waveforms of decoder circuit.

3.3 Divide-by-Four and U Signal Generator Circuit

Fig.3.9 shows the Divide-by-4 circuit (see Fig.3.1), which is formed by two D-flip-flops and one exclusive NOR (EXNOR) gate.

Figure 3.9: Divide-by-4 circuit.

The working sequence of Q_1 , Q_2 and D_2 are:

Clock	1	0	1	0	1	0	1	0	1	0	1	0
Q_1	1	1	0	0	1	1	0	0	1	1	0	0
Q_2	1	1	1	1	0	0	0	0	1	1	1	1
D_2	1	1	0	0	0	0	1	1	1	1	0	0

It can be seen from the table that D_2 should be '1' if Q_1 and Q_2 are the same, and D_2 should be '0' if Q_1 and Q_2 are different. An EXNOR gate has this function.

Simulation results show that there is a spike when D_2 equals '1', caused by Q_1 and Q_2 not becoming '1' at exactly the same time. But since the spike appears when clock equals '1', while for a rising edge triggered D-flip-flop the value of Q depends

only on the value of D when clock equals '0', the spike does not affect the value of Q_2 . In fact the Divide-by-4 block is also a modulus 4 counter.

SPICE simulation shows that the circuit can work with a clock frequency of 75MHz .

The U and $\bar{U}$ signals in the Latches block are generated from the output of Divide-by-4 block and an off-chip input signal Y . A D-flip-flop and a three input AND gate are used. The AND gate includes a three input NAND gate and a inverter in order to create both U and $\bar{U}$ signal, Fig.3.10.

Figure 3.10: Circuit Diagram of U Signal Generator.

Since latch-1 and latch-3 are falling-edge-triggered devices, while all D-flip-flops in the U signal generator block and divide-by-4 block are rising-edge-triggered, $Test_3$ is used as the clock of latches and $Test_2$ is used as the clock of D-flip-flops (Fig.3.3) in order to provide enough setup time for the input signal D_i ($i = 0, 1$) of latch-1 and latch-3. The input of the D-flip-flop in the U signal generator block is the output of the divide-by-4 block (Q_2), which is a pulse with two clock cycle width. The output signal of this D-flip-flop (Q) is the same as its input but with one clock cycle delay. Since the U and $\bar{U}$ signal should be a one clock cycle width pulse, a three input AND gate is used to generate such a pulse by connecting one of its inputs to the input

D and another to the output Q of the D-flip-flop. Another input of the three input AND gate is an off-chip control signal Y . Fig.3.11 is the SPICE simulation result of the Divided-by-4 block and U Signal Generator block.

Figure 3.11: SPICE simulation result of Divide-by-4 block and U Signal Generator block.

It has been stated in Section 3.1 that the Ring Oscillator block will divide the input clock frequency by three or four. After the output of the Ring Oscillator block passes through the Divide-by-4 block, the division ratio N becomes twelve or sixteen. The division ratio N can be set to between 12 and 16 by controlling the signal U . For example, if $Y = '0'$, then $U = '0'$, and the phase control signal will not change. Thus, only one switch is on all the time. the Ring Oscillator block will work on divide-by three and N will be twelve. If $Y = '1'$, U is controlled by the output of the Divide-by-4 block. Since in every period of the Divide-by-4 block U becomes '1' once, this

m_1	m_2	N
4	0	12
3	1	13
2	2	14
1	3	15
0	4	16

Table 3.2: The division ratio N change with m_1 and m_2 . ($n_1 = 3$, $n_2 = 4$, $N_c = 4$)

results in the change of phase control signals and, in turn, the output of the Ring Oscillator block switches from one phase to the other. Therefore after dividing by three 3 times, it divides by four once. In this case N is thirteen. If Y changes between 'low' and 'high' at a different time, N can change between twelve and sixteen.

Assume n_1 and n_2 are the two division ratios of the Ring Oscillator, in our case $n_1 = 3$, $n_2 = 4$. m_1 is the number of times to divide by n_1 , where $m_1 \leq N_c$, and m_2 is the number of times to divide by n_2 , where $m_2 \leq N_c$. N_c is the modulus of the counter block, so $m_1 + m_2 = N_c$. Since there is a modulus four counter in our circuit, $N_c = 4$. Table 3.2 shows that for the different values of m_1 and m_2 , the division ratio N changes from twelve to sixteen.

In general,

$$\begin{aligned}
 N &= N_c \cdot \frac{\text{Total number of input pulses in one period of Ring Oscillator block}}{\text{Total number of output pulses in one period of Ring Oscillator block}} \\
 &= \frac{N_c(m_1 n_1 + m_2 n_2)}{m_1 + m_2}
 \end{aligned} \tag{3.10}$$

By controlling the signal Y , the value of m_1 and m_2 can be changed, thus, the value of N can be changed. In fact the use of Divide-by-4 block and U signal generator block is for the convenience of chip testing. In the actual circuit shown in Fig.1.2, a divide-by-sixteen block and a Σ - Δ modulator are used. An output of the Σ - Δ modulator U' will replace the U signal here and it can make N change even continually, as discussed in the next chapter.

3.4 Simulation

Fig.3.12 shows the entire divider circuit diagram. This circuit has been simulated by SPICE. Most of the node capacitors used are extracted from standard cell gate circuits. Since the clocked ring Oscillator block is a custom design cell, two 50fF and one 80fF capacitor are added on the three outputs of the ring oscillator. Fig.3.13 (a), (b) are the SPICE simulation results of the dual modulus divider. The input clock frequency is 120 MHz. It can be seen that the signal *Test* divides clock frequency by 3 three times and by 4 one time. The *Odiv4* signal divides the clock frequency by thirteen.

Table 3.3 lists the maximum clock frequency and the minimum clock frequency obtained from simulation. In this table 'Ring Oscillator' means the clocked inverter ring part only, and 'Divider' means the circuit shown in Fig.3.12.

For the purpose of timing analysis in Section 3.6, Table 3.3 gives the results where the input signal to the ring oscillator is either a square-wave or sine-wave. It can be seen from Table 3.3 that at high frequency, since there is no much difference between sine-wave and square-wave, the results are close. For the simulation of the divider only a sine-wave has been used because the output of VCO is a sine-wave signal, and also because in practical testing a high frequency square wave is difficult to obtain.

Figure 3.12: Circuit diagram of the fractional N divider.

	Max. F_{clock} (Sine-wave)	Max. F_{clock} (Square-wave)	Min. F_{clock} (Sine-wave)	Min. F_{clock} (Square-wave)
Ring Oscillator	245 MHz	250 MHz	75 MHz	80 MHz
Divider	190 MHz	–	75 MHz	–

Table 3.3: The simulated maximum/minimum clock frequencies.

Comparing the two maximum clock frequencies of the ring and the divider, the latter is 55 MHz lower. This is because the delay introduced by the control circuit limits the speed of the entire divider circuit. Thus simplifying the control circuit to make the delay as small as possible might improve the circuit performance. Since the control circuit adds no affect on the speed of divider at low frequency, the minimum clock frequency of the divider circuit depends only on the ring oscillator. This is proved by the results in Table 3.3 where the two minimum clock frequencies are the same.

Figure 3.13: SPICE simulation result of the fractional N divider at $F_{clock} = 130 \text{ MHz}$.

3.5 Timing Analysis of a Clocked Inverter

As mentioned in Section 3.1, a clocked inverter is the basic component in the Ring Oscillator. It is necessary to take a look at how the clocked inverter works before discussing the Ring Oscillator.

Fig. 3.14 shows a clocked inverter. It can be seen that the clocked inverter includes two PMOS transistors and two NMOS transistors. The voltage of its output V_{out} depends on its input signal V_{in} , clock signal V_{clock} and its initial state. In this section, the different combinations of inputs and output are classified into eight cases, and each of them will be discussed in detail. For the convenience of description, first of all, let's define the 'on' and 'off' of a transistor.

Figure 3.14: Clocked inverter circuit with parasitic capacitors.

The Definition of 'On' and 'Off'

Generally speaking, from the view of digital operation, the 'on' or 'off' of a MOS transistor is according to the comparison between its gate-source voltage V_{GS} and its threshold voltage V_T . For NMOS transistor, if $V_{GS} \leq V_{Tn}$, there is no channel formed under gate, the transistor is in cut-off region and no current flows from its drain to source. The transistor is 'off'. If $V_{GS} > V_{Tn}$, there is a channel formed under gate, for the drain-source voltage $V_{DS} > 0$, there can be a current which is a function of voltages flowing from drain to source and the transistor is in linear or saturation region. If there is no current or $V_{DS} = 0$, the channel is still there, the transistor is also 'on'.

For better understanding of above definitions, according to [3], one can think a NMOS transistor is a voltage controlled switch. If the control voltage is 'low', which

is equivalent to $V_{GS} \leq V_{Tn}$, the switch is 'off'. If the control voltage is 'high', which is equivalent to $V_{GS} > V_{Tn}$, the switch is 'on', regardless of the amount of current passing through the switch.

For PMOS transistor, its threshold voltage V_{Tp} is a negative value, the condition of 'on' is changed to $|V_{GS}| > |V_{Tp}|$ and the condition of 'off' is $|V_{GS}| \leq |V_{Tp}|$.

In the following discussion, the concept of 'on' and 'off' will be used without further explanation.

Case A: V_{clock} Is 'L', V_{in} Changes from 'H' to 'L'

When V_{clock} is 'low', since M_4 is 'on', there is a low impedance between its drain and source, node c is in positive potential. The gate-source voltage of M_1 is zero hence M_1 is cut-off. Assuming the output is initially at ground potential, node e stays at zero. In this case, if input is 'high', M_2 is 'on' and M_3 is 'off'.

During the transition of input changing from 'high' to 'low', the gate-source capacitance of M_2 (C_{GS2}) which is initially charged to high voltage will now discharge. Since the voltage across the capacitor cannot change suddenly the voltage on node e (V_e) will be pulled below ground, then C_{GS2} will discharge and the capacitor across the drain-gate of M_1 (C_{GD1}), which will be parallel with C_{GS2} , is charged. One can say this is the effect of charge redistribution between C_{GS2} and C_{GD1} . At the same time, since M_2 turns from 'on' to 'off' and M_3 turns from 'off' to 'on', there is a short time when both M_2 and M_3 are 'on', a charge current can flow from V_{DD} through M_4 , M_3 , M_2 , C_5 , C_{GS2} and C_{GD1} to ground. This current can cancel some charge stored on C_{GS2} and in turn cancel some negative voltage of V_e . As soon as the charge on C_{GS2} and C_{GD1} get to equilibrium the voltage V_e stays at a value slightly below ground. This condition is stable if the voltage does not fall more than either an

n-channel threshold voltage drop or one diode drop below ground.

With the V_{in} moving to ground, M_4 is still 'on' and M_3 turns to 'on', the load capacitor C_L can charge through M_3 and M_4 . At the same time the voltage on node c (V_c) will drop to allow the charging current to flow through M_3 and M_4 . As the output voltage rises to 'high', the voltage V_c is forced to return to V_{DD} . Finally the circuit is changed to a new stable state, that is V_{clock} and V_{in} are both 'low', V_{out} is 'high', M_1 , M_2 are 'off' and M_3 , M_4 are 'on'.

Fig. 3.15 is the simulated result of case A.

Figure 3.15: Voltage transitions for V_{clock} 'L', V_{in} from 'H' to 'L'.

Case B: V_{clock} Is 'L', V_{in} Changes from 'L' to 'H'

When V_{clock} and V_{in} are both 'low', M_1 and M_2 are 'off', M_3 and M_4 are 'on'. Assuming V_{out} is initially 'high', the same as the final state of case A, V_c is in power supply

potential and V_e is in ground potential.

During the transition of V_{in} change from 'low' to 'high', M_3 from 'on' turns to 'off'. Since the voltage across the gate-source capacitor of M_3 (C_{GS3}) can not change suddenly the voltage on node c will follow the change of V_{in} . This pushes V_e slightly higher than V_{DD} . At the same time since M_4 is 'on', the initially charged high voltage on C_{GS3} can be discharged through M_4 and V_e can return to V_{DD} after transition. Since there is a capacitance between output and node c, V_{out} also follows the voltage change on node c.

With the input moving to 'high', M_2 from 'off' turns to 'on', there is a low impedance between the drain-source of M_2 . While M_1 is still 'off', there is a high impedance between the drain-source of M_1 . Hence, V_e should stay at a voltage value higher than half V_{DD} . The final stable state is V_{clock} is 'low', V_{in} and V_{out} are both 'high', M_1 and M_3 are 'off', M_2 and M_4 are 'on'.

Fig. 3.16 is the simulated result of case B.

Case C: V_{clock} Is 'H', V_{in} Changes from 'L' to 'H'

When V_{clock} is 'high' and V_{in} is 'low', M_1 is 'on', M_2 is 'off'. V_e is at zero potential. M_3 is 'on', M_4 is 'off'. Assuming output voltage is initially 'high', the voltage on node c is forced to stay at high potential.

During the transition of input change from 'low' to 'high', for the same reason as mentioned in case A, the voltage on node c is pushed slightly above V_{DD} . The difference here is the charge redistribution happens between the gate-source capacitor of M_3 (C_{GS3}) and the capacitance from drain to gate of M_4 .

With the V_{in} moving to 'high', M_2 from 'off' turns to 'on' and M_3 from 'on' turns to 'off'. Thus, both M_1 and M_2 are 'on', C_L can discharge through M_1 and M_2 .

Figure 3.16: Voltage transitions for V_{clock} 'L', V_{in} from 'L' to 'H'.

At the same time the voltage on node e will increase to allow the discharge current passing through M_1 and M_2 . As the output voltage drops to zero, V_e is forced return to zero. The final new stable state is V_{clock} and V_{in} are 'high', V_{out} is 'low', M_1 and M_2 are 'on', M_3 and M_4 are 'off'.

Fig. 3.17 is the simulation result of case C.

Case D: V_{clock} Is 'H', V_{in} Changes from 'H' to 'L'

When V_{clock} and V_{in} are both 'high', M_1 and M_2 are 'on', M_3 and M_4 are 'off'. Assuming V_{out} is initially 'low', same as the final state of case C, V_e is in power supply potential and V_e is in ground potential.

During the transition of V_{in} change from 'high' to 'low', M_2 from 'on' turns to 'off'. Since the voltage across the gate-source capacitor of M_2 (C_{GS2}) can not change

Figure 3.17: Voltage transitions for V_{clock} 'H', V_{in} from 'L' to 'H'.

suddenly V_e will follow the change of V_{in} . This makes the voltage on node e is pulled slightly lower than zero. At the same time since M_1 is 'on', the initially charged high voltage on C_{GS2} can be discharged through M_1 and V_e can return to zero after transition. Since there is a capacitance between output and node e, V_{out} also follows the voltage change on node e and stays at a voltage a little lower than zero because M_2 is 'off'.

With the input moving to 'low', M_3 from 'off' turns to 'on', there is a low impedance between the drain-source of M_3 . While M_4 is still off, there is a high impedance between the drain-source of M_4 . Hence, V_e should stay at a voltage value lower than half V_{DD} . The final stable state is V_{clock} is 'high', V_{in} and V_{out} are both 'low', M_1 and M_3 are 'on', M_2 and M_4 are 'off'.

Fig. 3.18 is the simulated result of case D.

Figure 3.18: Voltage transitions for V_{clock} 'H', V_{in} from 'H' to 'L'.

So far the discussion has considered the transitions of the circuit under the condition of keeping V_{clock} as a constant and letting V_{in} change from one level to another level. When a clocked inverter is used in a ring oscillator, as mentioned in Section 3.1, the frequency of clock signal is three times that of the input signal. In this case the output is only allowed to change after the edge of clock signal, meanwhile the value of V_{out} depends on the value of V_{in} during the transition of clock signal. This is equivalent to keeping V_{in} constant and changing V_{clock} , as in the following cases.

Case E: V_{in} Is 'L', V_{clock} Changes from 'H' to 'L'

When V_{in} is 'low', V_{clock} is 'high', M_1 and M_3 are 'on', M_2 and M_4 are 'off'. Assuming V_{out} is initially 'low', the voltage on node e is forced to stay at a low potential. Since

there is a low impedance across the source-drain of M_3 and a high impedance across the source-drain of M_4 , the voltage on node c should be a value lower than half V_{DD} .

During the transition of V_{clock} moving to 'low', M_1 from 'on' turns to 'off', M_4 from 'off' turns to 'on', M_2 is still 'off' and M_3 is still 'on'. The voltage on node e is pulled slightly below zero by the charge redistribution between the gate-drain capacitor of M_1 (C_{GD1}) and the capacitance across the gate-source of M_1 . Since both M_3 and M_4 are 'on', C_L can charge through M_3 and M_4 . This results in the output voltage increasing to V_{DD} and V_c is also pushed to V_{DD} . The final stable state is V_{in} is 'low', V_{clock} and V_{out} are 'high', M_1, M_2 are 'off' and M_3, M_4 are 'on'.

Fig. 3.19 is the simulation result of case E.

Figure 3.19: Voltage transitions for V_{in} 'L', V_{clock} from 'H' to 'L'.

From the discussion of case E, one can see that if V_{out} is initially 'high', after the transition of V_{clock} changing from 'high' to 'low', V_{out} should keep unchanged because

both M_1 and M_2 are 'off', C_L can not find a discharge path.

Case F: V_{in} Is 'L', V_{clock} Changes from 'L' to 'H'

When both V_{in} and V_{clock} are 'low', M_1 and M_2 are 'off', M_3 and M_4 are 'on'. Assuming V_{out} is initially 'high', the same as the final state of case E. V_c is in power supply potential and V_e is in ground potential.

During the transition of V_{clock} change from 'low' to 'high', M_4 from 'on' turns to 'off'. Since the voltage across the gate-drain capacitor of M_4 (C_{GD4}) can not change suddenly the voltage on node c will follow the change of V_{clock} . This makes the voltage on node c being pushed slightly higher than V_{DD} . At the same time the capacitors C_{GS4} and C_{GD4} are discharged. Since M_4 is turning 'off', V_c stays at the value a little higher than V_{DD} . V_{out} also follows the voltage change on node c because of the capacitance between the output and node c.

With V_{clock} moving to 'high', M_1 from 'off' turns to 'on', V_e stays at zero because M_2 are still 'off'. The final stable state is V_{in} equals 'low', V_{clock} is 'high', M_1 and M_3 are 'on', M_2 and M_4 are 'off', V_{out} keeps on 'high' because C_L is unable to discharge.

Fig. 3.20 is the simulated result of case F.

Figure 3.20: Voltage transitions for V_{in} 'L', V_{clock} from 'L' to 'H'.

Case G: V_{in} Is 'H', V_{clock} Changes from 'L' to 'H'

When V_{in} is 'high', V_{clock} is 'low', M_1 and M_3 are 'off', M_2 and M_4 are 'on'. Assuming V_{out} is initially 'high', V_c is forced stay at high potential. Since there is a low impedance across the drain-source of M_2 and a high impedance across the drain-source of M_1 , V_e should be a value higher than half V_{DD} .

During the transition of V_{clock} moving to 'high', M_1 turns 'on', M_4 turns 'off', M_2 is still 'on' and M_3 is still 'off'. The voltage on node c is pushed slightly above V_{DD} by the charge redistribution between the gate-drain and gate-source capacitance of M_4 . Since both M_1 and M_2 are 'on', C_L can discharge through M_1 and M_2 . This results in the output voltage drop to zero and the voltage on node e is also pushed to ground potential. The final stable state is V_{in} and V_{clock} are 'high', V_{out} is 'low', M_1 , M_2 are 'on' and M_3 , M_4 are 'off'. Fig. 3.21 is the simulation result of case G.

Figure 3.21: Voltage transitions for V_{in} 'H', V_{clock} from 'L' to 'H'.

From the discussion of case G, it can be seen that if V_{out} is initially 'low', after the transition of V_{clock} change from 'low' to 'high', V_{out} should keep unchanged because both M_3 and M_4 are 'off', C_L can not find a path to charge.

Case H: V_{in} Is 'H', V_{clock} Changes from 'H' to 'L'

When both V_{in} and V_{clock} are 'high', M_1 and M_2 are 'on', M_3 and M_4 are 'off'. Assuming V_{out} is initially 'high', same as the final state of case G, V_c is in power supply potential and V_e is in ground potential.

During the transition of V_{clock} changing from 'high' to 'low', M_1 from 'on' turns to 'off'. Since the voltage across the gate-drain capacitor of M_1 (C_{GD1}) can not be changed suddenly V_e will follow the change of V_{clock} . This makes the voltage on node e being pulled slightly lower than zero. At the same time the capacitor C_{GD1} and C_{GS1}

are discharged. Since M_1 turns to 'off', the voltage V_e stays at a value a little differ from zero. V_{out} also follows the voltage change on node e because of the capacitance between the output and node e.

With V_{clock} moving to 'low', M_4 from 'off' turns to 'on', V_c stays at V_{DD} because M_3 are still 'off'. The final stable state is V_{in} equals 'high', V_{clock} is 'low', M_1 and M_3 are 'off', M_2 and M_4 are 'on', V_{out} keeps on low potential because C_L is unable to be charged.

Fig. 3.22 is the simulated result of case H.

Figure 3.22: Voltage transitions for V_{in} 'H', V_{clock} from 'H' to 'L'.

3.6 Timing Analysis of Ring Oscillator

In this section, the Ring Oscillator shown in Fig. 3.3 is analysed. Its *maximum/minimum clock frequency* F_{clock} , and *self-oscillation frequency* F_{self} , are calculated analytically.

According to [12], in a ring oscillator, most nodes are either in 'high' or in 'low' state, but there is at least one transition node which is neither in 'high' nor 'low' state because the number of stages is odd. The oscillation is a propagation of the transition state from one node to the next.

Fig.3.23 shows the three output waveforms of the Ring Oscillator at $F_{clock} = 95 \text{ MHz}$. From Fig.3.23, one can draw the following conclusions:

Figure 3.23: Output waveform of the Ring Oscillator, $F_{clock} = 95 \text{ MHz}$.

1. Since the voltage of node C, $V(C)$, is the input of one clocked inverter and the voltage of node A, $V(A)$, is its output, if $V(C)$ changes from "H" to "L" on the rising edge of clock signal, $V(A)$ does not change from "L" to "H" at the same edge of clock signal but the falling edge.
2. The three outputs have the same waveforms. The period of each output is exactly equal to three times of clock period. i.e. the speed of the ring is

controlled by F_{clock} as long as each output of the ring working on *divide-by-3* mode.

3. The phase difference of two outputs is one clock period or 120 degrees, including a half clock period plus the rising time t_r of one output plus the half falling time t_f of another output. Therefore:

$$T_{clock} \geq \frac{1}{2}T_{clock} + t_r + \frac{1}{2}t_f \quad (3.11)$$

hence,

$$T_{clock} \geq 2 \times t_r + t_f \quad (3.12)$$

It can be seen that T_{clock} has a minimum value if the two sides of Eq-3.12 are equal. Thus, the maximum of F_{clock} can be obtained from Eq-3.12. If the clock frequency is higher than the maximum F_{clock} , the output of the ring can not follow the change and the ring can not work in the *divide-by-3* mode.

4. The output waveforms are not ideal square-waves. After V_{out} (Fig. 3.14) increasing to "H" on the falling edge of clock, it drops a little with the rising of clock and remains at the value $V_{DD} - \Delta V_{oh}$, then increases to "H" again with the next clock falling edge. Ideally when V_{in} is 'low', V_{clock} changes from 'low' to 'high', M_1 , M_3 are 'on' and M_2 , M_4 are cut-off, there is no path for C_L discharging, and V_{out} should hold on high voltage level. But since V_{in} is not a square-wave in a ring oscillator, C_L can find a discharging path during and after V_{clock} changing. That is the reason of V_{out} dropping. This will be discussed in more detail later.

If F_{clock} is very low, which means the period of clock is very long, it is possible that V_{out} keeps decreasing until the next clock falling edge, one can get $\Delta V_{oh} =$

$V_{DD} - V_{out} > 2.5 V$. This may cause a wrong output in the next stage and the ring will not work at *divide-by-3* mode.

From above discussion, it can be seen that the minimum clock frequency depends on the time t_d during which V_{out} decreases from "H" to half the value of V_{DD} . As mentioned earlier, the decreasing of V_{out} can take half clock period, thus the relation of t_d and maximum T_{clock} can be:

$$t_d = \frac{\max\{T_{clock}\}}{2} \quad (3.13)$$

3.6.1 Maximum Clock Frequency of the Ring Oscillator

Calculation of t_r

To simplify the problem, assume that in a clocked inverter (Fig-3.14), both V_{in} and V_{clock} are square-wave. Fig-3.24 shows the waveforms under this condition.

The conditions for V_{out} changing from 'low' to 'high' are $V_{in} = 'L'$ and V_{clock} changing from 'high' to 'low'. Under these conditions M_4 works in the linear region, M_3 is first in saturation region and, then, linear region, both M_1 and M_2 are cut-off. During t_r , load capacitor C_L is charged through M_3 and M_4 . It is clear that t_r includes two parts:

- t_{r1} : M_3 works in saturation region, V_{out} increases from 10 % of V_{DD} to $|V_{T3}|$.
- t_{r2} : M_3 works in linear region, V_{out} increases from $|V_{T3}|$ to 90 % of V_{DD} .

One can get:

$$t_r = t_{r1} + t_{r2} \quad (3.14)$$

V_{T3} is the threshold voltage of M_3 . Since the source of M_3 is not connected to V_{DD} , body effect has to be considered. From [3],

$$V_{T3} \approx V_{T0p} - \gamma\sqrt{V_{sb}}, \quad (3.15)$$

Figure 3.24: Waveform of clocked inverter with both V_{in} and V_{clock} are square-wave.

where γ is the body effect coefficient (for PMOS transistor in $3\ \mu\text{m}$ CMOS process $\gamma = 0.6V^{0.5}$) [15], V_{sb} is the source-substrate voltage (for M_3 , $V_{sb} = |V_c - V_{DD}|$).

During t_{r1} , since M_3 is in saturation, it is equivalent to a constant current source:

$$I_{DS3} = -\frac{\beta_3}{2}(V_{GS3} - V_{T3})^2 = -C_L \left(\frac{dV_{out}}{dt} \right),$$

Where V_{GS3} is the gate-source voltage of M_3 and $V_{GS3} = V_{in} - V_c$. Therefore:

$$\begin{aligned} t_{r1} &= \frac{2C_L}{\beta_3} \int_{0.1V_{DD}}^{|V_{T3}|} \frac{dV_{out}}{(V_{in} - V_c - V_{T3})^2} \\ &= \frac{2C_L}{\beta_3} \left(\frac{|V_{T3}| - 0.1V_{DD}}{(V_{in} - V_c - V_{T3})^2} \right), \end{aligned} \quad (3.16)$$

where $\beta = k \frac{W}{L}$, L and W are the length and width of transistor channel, and k is the transconductance parameter μC_{ox} .

In Eq-3.16, $V_{in} = 0$, V_c is not a constant, but since M_4 is in linear region, simulation shows that assuming the average value of its source-drain voltage V_{SD4} is a constant

and equals 1V is reasonable. Thus, for $V_{DD} = 5V$, $V_c = V_{DD} - V_{SD4} = 4V$. C_L is the sum of the input capacitance of two clocked inverter loads and layout capacitance, $C_L \approx 0.45 pF$. $W_3 = 54 \mu m$ and for PMOS transistor K_p equals $16 \times 10^{-6} A/V^2$, $V_{T0p} = -0.8V$ [15]. Substituting those values and Eq-3.15 into Eq-3.16, $t_{r1} \approx 0.42 ns$.

During t_{r1} , both M_3 and M_4 are in the linear region, V_{out} increases from $|V_{T3}|$ to 90 % V_{DD} . Since $V_{in} = V_{clock} = "L"$, the two series transistors can be equated to one transistor and the equivalent channel width is

$$W_{eqp} = \frac{W_3 \times W_4}{W_3 + W_4} \quad (3.17)$$

From [3], The current passing through M_3 and M_4 (I_{DS34}) should be:

$$I_{DS34} = -\beta_{eqp}((V_{GS34} - V_{T0p})V_{DS34} - \frac{V_{DS34}^2}{2}) = -C_L \cdot \frac{dV_{out}}{dt}$$

Where V_{GS34} is the equivalent gate source voltage. Since V_{in} is 'low', $V_{GS34} = V_{in} - V_{DD} = -V_{DD}$. V_{DS34} is the equivalent drain-source voltage and $V_{DS34} = V_{out} - V_{DD}$. Therefore:

$$\begin{aligned} t_{r2} &= \frac{C_L}{\beta_{eqp}} \int_{|V_{T3}|}^{0.9V_{DD}} \frac{dV_{out}}{(V_{GS34} - V_{T0p})V_{DS34} - \frac{V_{DS34}^2}{2}} \\ &= \frac{C_L}{\beta_{eqp}} \int_{|V_{T3}|}^{0.9V_{DD}} \frac{dV_{out}}{(-V_{DD} - V_{T0p})(V_{out} - V_{DD}) - \frac{(V_{out} - V_{DD})^2}{2}} \\ &= \frac{-C_L}{\beta_{eqp}(V_{DD} + V_{T0p})} \left(\ln(V_{out} - V_{DD}) - \ln\left(1 + \frac{V_{out} - V_{DD}}{2(V_{DD} + V_{T0p})}\right) \right) \Big|_{|V_{T3}|}^{0.9V_{DD}} \\ &= \frac{C_L}{\beta_{eqp}(V_{DD} + V_{T0p})} \left(\ln \frac{1.9V_{DD} + 2V_{T0p}}{V_{DD} + 2V_{T0p} + |V_{T3}|} - \ln \frac{0.1V_{DD}}{V_{DD} - |V_{T3}|} \right) \end{aligned} \quad (3.18)$$

Substituting $W_3 = 54 \mu m$, $W_4 = 78 \mu m$ and Eq-3.15, Eq-3.17 into Eq-3.18, $t_{r2} \approx 1.55 ns$. From Eq-3.14, $t_r \approx 1.97 ns$.

Calculation of t_f

The condition for V_{out} changing from 'high' to 'low' are V_{in} ="H" and V_{clock} changing from 'low' to 'high'. During and after the transition of V_{clock} , M_1 , M_2 saturate for a very short time. Assuming both M_1 and M_2 work in the linear region during t_f makes little difference but it simplifies the problem substantially. In this case M_1 , M_2 also can be equated to one transistor through which the load capacitor C_L discharged. Since the NMOS transistor is faster than the PMOS transistor, t_f should be less than t_r . The equivalent channel width is

$$W_{eqn} = \frac{W_1 \times W_2}{W_1 + W_2} \quad (3.19)$$

from [3], the discharge current pass through M_1 , M_2 (I_{DS12}) is:

$$I_{DS12} = \beta_{eqn}((V_{GS12} - V_{T0n})V_{DS12} - \frac{V_{DS12}^2}{2}) = -C_L \frac{dV_{out}}{dt}$$

$$\beta_{eqn}((V_{DD} - V_{T0n})V_{out} - \frac{V_{out}^2}{2}) = -C_L \frac{dV_{out}}{dt}$$

Where V_{GS12} is the equivalent gate-source voltage. Since V_{in} is high, $V_{GS12} = V_{in} = V_{DD}$. V_{DS12} is the equivalent drain-source voltage and $V_{DS12} = V_{out}$. One can get:

$$t_f = \frac{-C_L}{\beta_{eqn}(V_{DD} - V_{T0n})} \int_{0.9V_{DD}}^{0.1V_{DD}} \frac{dV_{out}}{V_{out} - \frac{V_{out}^2}{2(V_{DD} - V_{T0n})}} \quad (3.20)$$

$$= \frac{C_L}{\beta_{eqn}(V_{DD} - V_{T0n})} \ln \left(\frac{180V_{T0n} - 171V_{DD}}{20V_{T0n} - 11V_{DD}} \right)$$

If $V_{DD} = 5V$, $W_1 = 72\mu m$, $W_2 = 48\mu m$, for NMOS transistor K_n equals $50 \times 10^{-6} A/V^2$, $V_{T0n} = 0.7V$. Substituting those values and Eq-3.19 to Eq-3.20, $t_f \approx 0.63 ns$.

Calculation of the maximum clock frequency

From Eq-3.12 the minimum clock period is 4.57ns, thus the maximum clock frequency can be up to 218MHz.

3.6.2 Minimum Frequency of the Ring Oscillator

Fig-3.25 shows the waveform of ring oscillator at minimum F_{clock} . As mentioned earlier, t_d exists because V_{in} is not a square-wave. But, according to the simulation results and the discussion in Section 3.4, assuming V_{clock} is square-wave is still reasonable. When $V_{clock} = 'L'$, C_L is already charged to V_{DD} . During the transition of V_{clock} changing from 'low' to 'high', four transistors are all 'on'. M_1 , M_2 , M_3 work in the linear region and M_2 in saturation. Since C_L can discharge through M_1 , M_2 , V_{out} starts dropping. At the same time V_{in} drops. The reason for V_{in} dropping is similar to V_{out} increasing which will be discussed soon. After V_{clock} reaches 'high', M_4 is cut-off, M_1 is in linear region and M_2 stays at saturation region until $V_{in} - V_e - V_{T2} = 0$. During this time t_d , a constant discharging current I_{DS2} flows from C_L through M_2 , M_1 to ground, and

$$I_{DS2} = \frac{\beta_2}{2}(V_{in} - V_e - V_{T2})^2 = -C_L \frac{dV_{out}}{dt}, \quad (3.31)$$

which makes $V_{out}(t_d) = V_{DD} - \Delta V_{oh}$ (region A in Fig-3.25). After t_d , M_2 is cut-off and V_{out} holds on $V_{out}(t_d)$ until V_{clock} starts falling. At the falling edge of V_{clock} , M_4 changes from cut-off to linear, and M_3 is also in the linear region. This allows C_L to be charged through M_3 , M_4 and hence V_{out} becomes high again. The same thing happens when V_{out} is 'low', but in this case C_L charges through M_3 , M_4 which results in a increase of V_{out} (region C in Fig-3.25). Since NMOS is faster than PMOS, the dropping of V_{out} is faster than its rising, in other words V_{out} drops to the dangerous value at higher

clock frequency rather than increases to that value. This clock frequency should be the minimum clock frequency. Based on this reason, to calculate the minimum F_{clock} , only the case when V_{out} is high is considered (region A in Fig-3.25). From Eq-3.21,

$$\begin{aligned} t_d &= -2 \frac{C_L}{\beta_2} \int_{V_{DD}}^{V_{out}(t_d)} \frac{dV_{out}}{(V_{inA} - V_e - V_{T2})^2} \\ &= \frac{2C_L(V_{DD} - V_{out}(t_d))}{\beta_2(V_{inA} - V_e - V_{T2})^2}. \end{aligned} \quad (3.22)$$

To calculate t_d , V_{in} is a important condition. Since it is not a constant, its average value V_{inA} is used. Also the input delay is small enough to be ignored. It can be seen from Fig-3.25 that the waveform of V_{in} in region A is the same as V_{out} in region B, while the calculation of the latter is easier than the former. In region B, V_{clock} changes from 'low' to 'high' and V_{in} changes from 'high' to 'low'. There is a short period during which M_2 works in the saturation region and M_1 in the linear region, thus V_{out} decreases rapidly. During this period,

$$I_{DS1} = \beta_1((V_{clock} - V_{T1})V_e - \frac{V_e^2}{2}), \quad (3.23)$$

$$I_{DS2} = \frac{\beta_2}{2}(V_{in} - V_e - V_{T2})^2. \quad (3.24)$$

Where I_{DS1} is the drain-source current of M_1 , I_{DS2} is the drain-source current of M_2 and

$$I_{DS1} = I_{DS2}. \quad (3.25)$$

From Fig-3.25 it can be seen that in region B there is a point at which V_{in} equals V_{out} . At this point, M_2 is still in saturation and after this point M_2 turns to cut-off. V_{out} keeps almost unchanged. This value of V_{outB} can be used as the average V_{in} in region A. It also can be seen from Fig-3.25 that at this point V_e is very low and one can assume V_e equals 20mV, which means the body effect in M_2 can be ignored and

Figure 3.25: Waveforms of Ring Oscillator at minimum F_{clock} .

the V_e^2 term in Eq-3.23 can also be ignored. Based on these considerations one can solve V_{out} from Eq-3.23, Eq-3.24 and Eq-3.25,

$$V_{outB} = V_{inA} = V_{T0n} + \sqrt{\frac{2\beta_1}{\beta_2}(V_{clock} - V_{T0n})V_e}. \quad (3.26)$$

Substituting $V_{clock} = 5V$ and all other values to Eq-3.26, V_{inA} is about 1.21V. In region A, V_e is also very low in the most time. Thus the body effect in M_2 can be ignored. Eq-3.22 becomes:

$$t_d = \frac{2C_L(V_{DD} - V_{out}(t_d))}{\beta_2(V_{inA} - V_e - V_{T0n})^2}. \quad (3.27)$$

Since the maximum clock period defined is when $V_{out}(t_d) = 2.5V$, the value of T_{clock} , from Eq-3.27, $t_d \approx 10.9ns$. Substituting t_d into Eq-3.13, the maximum of T_{clock} is 21.8ns. Therefore, the minimum of F_{clock} is about 45.87 MHz.

3.6.3 Calculation of the Self-Oscillation Frequency F_{self}

Although the dual modulus divider presented in this thesis uses a digitally clocked inverter ring, preliminary work has suggested that the circuit can also operate in a quasi injection-locked mode where the ring is constrained to oscillate at a third of the frequency of an incoming sinusoidal waveform. This mode of operation has the potential to allow division signals with lower amplitude and degraded digital character, thus relaxing the requirements on a high frequency component such as a VCO.

Although a complete discussion of this mode of operation is outside the scope of this thesis, as part of the testing procedure some preliminary results on the oscillation frequency were obtained. This section therefore provides a starting point for the analysis of the circuit as an oscillator. Section 3.8 will show the test results.

Self-oscillation occurs when the clock signal is replaced by two suitable DC voltage sources (refer to Fig.3.2). To simplify the problem, the delay of a clocked inverter t_{di} with square-wave at V_{in} and DC at V_{clock} is considered, Fig-3.26. Since M_1 , M_4 are DC biased, their effect to the circuit depends on the value of bias voltage, and so does the value of t_{di} .

Calculation of the falling edge delay t_{fd}

During the falling of V_{out} , from V_{DD} to half V_{DD} , M_1 is in saturation, M_4 in linear region, M_3 is cut-off and M_2 first in saturation, then turns to linear region. Thus the load capacitor C_L can discharge through M_1 , M_2 . The falling edge delay t_{fd} is defined as V_{out} dropping from V_{DD} to $0.5V_{DD}$. Since M_1 is in saturation,

$$I_{DS1} = \frac{\beta_1}{2}(V_{nclock} - V_{T1})^2 = -C_L \frac{dV_{out}}{dt}.$$

Figure 3.26: Waveforms of the Clocked Inverter at $V_{nlock} = 1.5V$, $V_{plock} = 3.5V$ and V_{in} is square-wave.

Therefore,

$$t_{fd} = \frac{2C_L}{\beta_1} \int_{V_{DD}}^{V_{DD}} \frac{dV_{out}}{(V_{nlock} - V_{T1})^2} = \frac{C_L V_{DD}}{\beta_1 (V_{nlock} - V_{T0n})^2}. \quad (3.28)$$

For $V_{DD} = 5V$, if $V_{nlock} = 1.5V$, $t_{fd} = 2.93ns$.

Calculation of the rising edge delay t_{rd}

During the rising of V_o , from zero to half V_{DD} , M_4 is in saturation, M_1 in linear region, M_2 is cut-off and M_3 first in saturation, then turns to linear region. Thus C_L can charge throu M_3 , M_4 . The rising edge delay t_{rd} is defined as V_{out} increasing from zero to $0.5V_{DD}$. Since M_4 is in saturation,

$$I_{DS4} = -\frac{\beta_4}{2} (V_{plock} - V_{DD} - V_{T4})^2 = -C_L \frac{dV_{out}}{dt}.$$

Thus

$$t_{rd} = \frac{2C_L}{\beta_4} \int_0^{\frac{V_{DD}}{2}} \frac{dV_{out}}{(V_{plock} - V_{DD} - V_{T4})^2} = \frac{C_L V_{DD}}{\beta_4 (V_{plock} - V_{DD} - V_{T0p})^2}. \quad (3.29)$$

If $V_{plock} = 3.5V$, $t_{rd} \approx 11 \text{ ns}$.

Self-oscillation frequency

The delay of the inverter should be the average of t_{fd} and t_{rd} :

$$t_{di} = \frac{t_{fd} + t_{rd}}{2}. \quad (3.30)$$

The period of the self-oscillation is three times of t_{di} . Therefore, F_{self} is:

$$F_{self} = \frac{1}{3t_{di}}. \quad (3.31)$$

Substituting the value of t_{fd} and t_{rd} into Eq-3.30, $t_{di} \approx 7 \text{ ns}$. From Eq-3.31, $F_{self} \approx 47.6 \text{ MHz}$, while the tested result is 48 MHz (Fig.3.33) and HSPICE simulation result is 45.45 MHz .

In the above calculations, the clock signal is assumed to be an ideal square-wave. However, practically it is impossible to obtain a good square-wave at high frequency. Instead, sine-wave is used in testing. This is one reason of the difference among calculation, simulation (Table 3.3) and testing (Section 3.11) results. Meanwhile, during calculation some assumptions and approximations have been used which also introduce distortions.

3.7 Chip layout

The layout of the dual modulus frequency divider was done manually using *Electric*, a VLSI design CAD system developed by *Schlumberger Palo Alto Research*, Palo

Alto, California. The design rules used were for *NTE CMOS3 DLM*, which is $3\mu\text{m}$ single polysilicon double metal process. The gate level devices come from Carleton University CMOS3 standard cell library.

There are eight pads on the chip: one V_{DD} pad, one V_{SS} pad, four input pads, and two output pads. The chip size is $3133 \times 1866 \mu\text{m}^2$.

Fig.3.27 is the diagram of layout. For the sake of memory size, only five layers are shown.

Figure 3.27: Layout of the dual modulus frequency divider (chip CU051).

The design implementation was submitted to *Canadian Microelectronics Corporation* (CMC) twice and manufactured by *Northern Telecom Electronics* (NTE). The first version did not work properly. Since there was one wrong connection in the layout, the Ring Oscillator only worked in divide-by-3 mode. This mistake could be

avoided if using an automatic layout tool such as *EDGE*, a powerful VLSI design CAD system developed by *Cadence Design Systems Inc.*, San Jose, California. Unfortunately at that time no such tool was available. After correcting the mistake, the second version works correctly.

3.8 Testing Results

Fig.3.28 shows the chip test equipment setup. The DC Source is an ANATEK Dual Regulated DC Power Supply, the value of V_{SS} is $-2.5V$ and V_{DD} , $+2.5V$. The two clock inputs V_{pclock} and V_{nclock} are biased separately, each of them can vary from $-2V$ to $+2V$. The AC component of clock signal is a high frequency sine-wave generated by a HP4195A Network/Spectrum Analyzer. The outputs are fed to a HITACHI Digital Storage Oscilloscope.

Figure 3.28: Dual modulus divider chip (CU051) testing environment.

Fig.3.29 is the waveform of *Test* and *Odiv4* signals. Fig.3.30 (a) and Fig.3.30 (b) show their relations to *Clock* signal. Each of them was measured at 83.75MHz clock frequency and $\pm 1V$ bias voltages. It can be seen that *Test* signal divides clock

frequency by three or four, and *Odiv4* signal divides clock frequency by thirteen.

Figure 3.29: Waveform of 'Test' and 'Odiv4'.

It was found from testing that the maximum and minimum clock frequencies are changed by varying the bias voltage. This is due to the change of working points of PMOS and NMOS transistors, and thus, their dynamic range is changed. Table 3.4 shows the relation between bias voltage and maximum clock frequency. Table 3.5 shows the relation between bias voltage and minimum clock frequency. From Table 3.4 one can find that the maximum clock frequency can be up to 203.5 MHz at bias voltage of $V_{p\text{clock}} = V_{n\text{clock}} = 0.75V$. The results of zero bias can be used to compare with SPICE simulation results given by Table 3.3 in Section 3.4.

Fig.3.31 is the contour plot of Table 3.4, and Fig.3.32 is the contour plot of Table 3.5. One can find that the largest working frequency range lays in the area of

(a)

(b)

Figure 3.30: (a) 'Test' vs. 'Clock'. (b) 'Odiv4' vs. 'Clock'.

V_{pclock}	-0.75	-0.5	-0.25	0	0.25	0.5	0.75	1	1.25	1.5	1.75
V_{nclock}											
-2			76	78.5	81.5	93	97	103	101.5	95.5	
-1.75	80.5	85.5	92	96.5	103.5	110.5	116	118.5	120.5	97.5	
-1.5	79	89.5	96.5	99.5	108	118.5	120.5	122.5	124	94.5	81.5
-1.25		93.5	100	107.5	116	120	123	125	127	92.5	79
-1		79.5	107.5	116.5	120	123	123.5	128	131.5	100	
-0.75			107.5	120	122.5	125.5	127.5	131	143	87.5	
-0.5			109	122	125.5	128	131	134	143	85.5	
-0.25				123.5	126.5	130.5	133.5	149.5	143	89.5	
0			123	127	129.5	133	149.5	150.5	143.5	138.5	
0.25			124.5	129	134.5	149.5	191.5	151.5	104.5		
0.5				134.5	144.5	160	200	153.5	144.5	135.5	
0.75				135.5	141.5	150.5	203.5	155.5	146	137	
1					134.5	140	151.5	176	147.5	137	
1.25						135	138	144	149.5	138.5	
1.5								134.5	150	138	
1.75										136	

Table 3.4: Maximum clock frequency (MHz) vs. bias voltage (V) (CU051).

V_{pclock}	-0.75	-0.5	-0.25	0	0.25	0.5	0.75	1	1.25	1.5	1.75
V_{nclock}											
-2			73	73	73	73	72.5	73	72.5	71.5	
-1.75	72	74	7.5	74.5	74.5	74	73.5	72.5	72	72	
-1.5	71.5	73	73.5	73.5	73	72.5	72	71.5	71.5	72	72
-1.25		71	71.5	72.5	72.5	72.5	72	71	72	71	75
-1		70	70	71.5	70.5	70.5	70.5	71	71.5	92	
-0.75			71	71.5	72.5	71.5	71.5	71	72	74	
-0.5			100.5	71	71	71	71	72	72.5	80.5	
-0.25				96.5	71.5	70.5	72	72	75	89	
0			117	112	97	70.5	71.5	74	111.5	117.5	
0.25			123	116	111	100	73	81	86		
0.5				122.5	118.5	112.5	102.5	83.5	112.5	121	
0.75				124.5	118	120	113.5	110.5	112	117.5	
1					124	119.5	117	169	116	118.5	
1.25						127.5	122.5	150	118	120	
1.5								126	122.5	120.5	
1.75										125	

Table 3.5: Minimum clock frequency (MHz) vs. bias voltage (V) (CU051).

From testing, it was also found that at some bias voltage range, self oscillation may happen and the self oscillation frequency F_{self} differs from different bias voltage. This agrees with the conclusion obtained from Section 3.6, timing analysis of Ring Oscillator. Fig.3.33 is the spectrum of self oscillation at $\pm 1V$ bias voltage. The spectrum is obtained from the 4195A. In Fig.3.33, F_{self} is 48.11 MHz. The spurs are introduced by testing equipment and environment noise.

Figure 3.32: Contour graph of minimum clock frequency vs. bias voltage (CU051).

Figure 3.33: Self Oscillation spectrum of frequency divider. ($V_{plock} = +1V$, $V_{nlock} = -1V$)

3.9 Problems and Improvements

In testing, it was found that the circuit was unstable. At the beginning, it was dividing the input clock frequency by three or four properly. After a while, it switched automatically to divide by three only. After carefully checking the SPICE simulation input net list, another connection error was found.

Simulation also shows that the control circuit determines the maximum working frequency. Since the pulse width of $Test_3$ is larger than that of $Test_2$, especially at high frequency, (Fig.3.13 (a) and (b)), and $Test_3$ has the same waveform as $Test_1$ but with two stage delay, changing the clock of all D-Flip-Flops from $Test_2$ to $Test_1$ can increase the maximum working frequency (See Fig.3.12).

The second version of layout was modified manually by using EDGE. The new version or the third version of layout have been submitted to NTE through CMC. Fig.3.34 is the diagram of layout. To ensure circuit stability the power supply of the Ring Oscillator is separated from the whole circuit. There is also a test circuit on the chip, which includes a Ring Oscillator and its bias circuit. This chip has the size of $1866 \times 4300 \mu m^2$.

The test environment is the same as Fig.3.28. Table 3.6 and Table 3.7 are the tested results. Comparing with the results given by Table 3.4 and Table 3.5, it can be seen that at some bias voltages the maximum clock frequency of chip CU055 can be up to 250 MHz and the frequency range is larger than that of chip CU051. Testing also shows that chip CU055 is stable.

Vpclock(V) Vnclock(V)	2	1.75	1.5	1.25	1	0.75	0.5	0.25	0
-2	94	135.5	142	145	146	181.5	187	189.5	189.5
-1.75	93.5	138	144.5	180.5	185	189	205	207.5	243.5
-1.5	93.5	138.5	145	152.5	185.5	191.5	241.5	244	246
-1.25	93.5	138.5	144.5	151.5	176.5	193	240.5	243.5	245
-1	93.5	138	144	151.5	163.5	194	238	241.5	244.5
-0.75	93	137.5	143	149.5	162	186	236.5	241	243.5
-0.5	93	137	142.5	148	160.5	182.5	235	140	243
-0.25	92.5	111.5	142	147.5	153	181	234.5	239	242.5
0	92.5	110	141.5	146.5	153	179.5	233	149.5	241.5
0.25	92.5	110	141	146	152	178	232.5	149.5	241
0.5	92.5	109.5	140	145	151	159.5	231.5	149.5	240
0.75	92.5	109.5	139.5	144.5	150	155.5	164	149.5	239.5
1	92.5	110	138.5	143.5	149	153.5	149.5	149.5	238.5
1.25	92.5	110	137.5	142	148.5	152.5	149.5	140.5	237.5
1.5	93	111	135.5	140.5	147	151.5	175.5		237
1.75	92.5	109.5	132.5	139	145.5	152	142		236
2		102.5	116	131.5	140.5	151			240

Vpclock(V) Vnclock(V)	-0.25	-0.5	-0.75	-1	-1.25	-1.5	-1.75	-2
-2	189.5	155.5	188	159	158	186	158.5	152.5
-1.75	246.5	245	246.5	242.5	197.5	195.5	193.5	191
-1.5	247.5	249.5	251	248	237.5	238.5	231	198.5
-1.25	247.5	249.5	251	251.5	243	241	133.5	218.5
-1	247	249.5	251.5	251.5	248	242.5	234.5	218.5
-0.75	246	248	254.5	251	248	244	236	217.5
-0.5	246.5	248.5	253.5	251	250	224.5	236	218
-0.25	245	248.5	253.5	251	250.5	248	195	
0	243	248.5	252.5	251	250.5	244	189	
0.25	244	249	252.5	250.5	250	242.5	183.5	
0.5	242.5	248.5	251	250.5	250	241.5		
0.75	242.5	144	252	250.5	251	239.5		
1	243	139	252.5	251.5	251	237.5		
1.25	243	133.5	251	251.5	246.5			
1.5	243.5		251	244.5	242			
1.75	243		243.5					
2								

Table 3.6: Maximum clock frequency (MHz) vs. bias voltage (V) (chip CU055).

Vpclock(V) Vnclock(V)	2	1.75	1.5	1.25	1	0.75	0.5	0.25	0
-2	51	51	51	51	49	51	52	51.5	51
-1.75	51	51	51	51.5	49	51	52	51.5	51
-1.5	51.5	51	51	51	49	51	51.5	51.5	50.5
-1.25	51.5	51	50	51	49	50.5	51.5	51	50.5
-1	51.5	51	50	51	50	50.5	51	50.5	50.5
-0.75	52	51	49	50.5	50	50.5	50.5	50.5	55.5
-0.5	52	51	51	50.5	50.5	52	50.5	54	61
-0.25	52	51	49	50.5	52.5	55	54.5	60.5	68.5
0	52.5	50.5	50.5	52.5	55.5	59	61	68.5	150
0.25	52	50	52.5	56.5	61	67.5	69	74.5	150
0.5	51.5	51.5	57.5	62.5	70	75.5	150	78.5	150
0.75	49.5	58	65	71.5	76.5	82.5	116.5	112.5	150
1	57.5	66.5	72	77	83	85.5	116.5	118.5	160.5
1.25	68	72.5	76.5	81	114	117.5	120.5	133.5	166
1.5	78.5	77.5	108	115.5	119.5	121.5	124		210.5
1.75	89.5	104.5	114.5	122	124.5	127	129.5		215.5
2		101.5	111	124	134.5	149			222.5

Vpclock(V) Vnclock(V)	-0.25	-0.5	-0.75	-1	-1.25	-1.5	-1.75	-2
-2	51	50.5	50.5	50	66.5	74.5	81.5	109.5
-1.75	51	50.5	50.5	51	69.5	74.5	78.5	123
-1.5	50.5	50.5	56	68	73	77	115	127.5
-1.25	50.5	57.5	66.5	72.5	76	80	118	160.5
-1	56.5	64.5	71.5	75.5	78.5	115	155.5	169
-0.75	62.5	70.5	75	78.5	150	117.5	164.5	175
-0.5	69	74	78.5	107	150	162.5	167.5	204
-0.25	74	77.5	150	115	160.5	165.5	170	
0	150	150	150	158.5	164.5	210	172.5	
0.25	150	150	155.5	164	209.5	214	176	
0.5	115.5	119.5	163.5	209	213.5	217.5		
0.75	156	123	209.5	213.5	216.5	220		
1	164	134	214	216.5	219.5	222.5		
1.25	210.5	130.5	217	219.5	246.5			
1.5	215		220	222	221.5			
1.75	225		223.5					
2								

Table 3.7: Minimum clock frequency (MHz) vs. bias voltage (V) (chip CU055).

Figure 3.34: A new layout of the two modulus frequency divider (chip CU055).

Chapter 4

DESIGN AND LOGIC VERIFICATION OF A DIGITAL SIGMA-DELTA MODULATOR

In order to implement the complete noise shaping fractional N divider, a Σ - Δ modulator is required to provide a modulus control bit-stream with the necessary spectral properties.

A digital version of the sigma delta modulator was constructed rather than using existing analog realizations or finite length simulated and clocked streams because the analog system has noise sources which are not present in the digital version (and it was felt that the simulation should be idealized to the greatest extent possible), and the finite sequence simulated stream could not be output fast enough to run the 3,4 divides at its highest operating speed. This chapter will describe the design and implementation of a second order Σ - Δ modulator which generates the “U” signal in Fig.3.1. Fig.4.1(a) shows the block diagram and Fig.4.1(b) shows the Z-domain model of the system [2].

The following terminologies are used in this chapter:

1. *Bit cycle and word cycle:* In the operation of the digital Σ - Δ modulator, each

Figure 4.1: (a) Block diagram of a second order digital Σ - Δ modulator and an U' Signal Generator; (b) Z domain model of the Σ - Δ modulator.

word is a 16-bit binary digit. There are two clock signals in the circuit. The fast clock is an input signal (the 'Test' in Fig.3.12), the length of whose period (T_2 or T_3 in Fig.3.4) is equivalent to one bit. Thus it is called bit cycle. The slow clock is generated by the control block in Fig.4.1 (a), the length of whose period equals sixteen 'bit cycles' or a 'word'.

2. *The order of bit:* From Fig.4.1 (a) it can be seen that the circuit includes one adder and two accumulators. Since each accumulator includes one adder (Section 4.2), actually there are three adders in the second order digital Σ Δ modulator, each of which is a 16-bit serial adder. Since each addition of two sixteen-bit digits takes sixteen bit cycles or one adder cycle, the adder cycle is

the same as the word cycle. Assuming the adder in the Adder block is called *adder₁*, the adders in *Accumulator₁* and *Accumulator₂* will be called *adder₂* and *adder₃* respectively. The adder cycle of *adder₁* should begin with the zeroth bit, and end with the fifteenth bit. The adder cycle of *adder₂* should begin with the first bit and end with the sixteenth bit or the zeroth bit of the second word. The adder cycle of *adder₃* should begin with the second bit and end with the seventeenth bit or the first bit of the second word. When talking about the order of bits, *adder₁* is used as the reference. In the following sections, the bit sequence always refers to that of *adder₁*'s.

4.1 Adder

The Adder block in Fig.4.1 (a) is a 16-bit serial adder [37,38]. It consists of a full adder and a D-Flip-Flop which feeds back the carry of previous bit, as shown in Fig.4.2.

Figure 4.2: A 16 bit serial adder.

It should be noted that for the fifteenth bit of an input digit, the next bit is the

zeroth bit of the next input digit. In this case, the carry of the fifteenth bit should not be feedback. An AND gate and a carry removing signal $C'R_1$ are used to clear the fifteenth carry. The signal comes from the control block in Fig.4.1 (a) and will be discussed in Section 4.6.

4.2 Accumulator

The function of an accumulator is equivalent to an analog integrator. There are a 16-bit serial adder and a 16-bit shift register in an accumulator. One input of the adder is the sum of previous adder and the other input is the output loop back. Thus, the sum keeps accumulating until overflow. Since the addition has to be done serially, a shift register with 16 D-Flip-Flops connected in serial is adopted to store the 16 bit sum and feed this value back to the input bit by bit. Fig.4.3 is the circuit diagram of an accumulator.

There are two accumulator blocks in Fig.4.1 (a) which have the same configuration but different inputs and outputs. The relationship between them will be explained in Section 4.6, circuit synchronization.

4.3 The Selecting Switch

The function of the selecting switch circuit is defined by Table 4.1, where A, B are two inputs and C is the output of the circuit, Therefore,

$$C = (-M)(A\bar{B} + B\bar{A}) + (-2M)AB = \overline{(A \oplus B)(-M)} \cdot \overline{AB(-2M)} \quad (4.1)$$

It can be seen from Eq-4.1 that the circuit should include an exclusive OR gate, two 2-input-NAND gates and one 3-input-NAND gate. $-M$ is an input number with sixteen bits and $-2M$ can be obtained by adding one bit delay to $-M$, which means

Figure 4.3: Circuit diagram of an accumulator.

shifting $-M$ one bit left. A D-Flip-Flop is used for this purpose. Its input is $-M$ and output, $-2M$. Fig-4.4 shows the logic diagram of Selecting Switch block.

AB	00	10	01	11
C	0	-M	-M	-2M

Table 4.1: The relation among the inputs and output of the Selecting Switch block.

Figure 4.4: Logic diagram of Selecting Switch block.

4.4 The Control Circuit

The Control Circuit block is used to generate all control signals. It consists of a divide-by-sixteen counter and some logic units. A five bit synchronize counter can be used. The working sequence of the input D_i and output Q_i ($i = 0, \dots, 4$) of the five D-Flip-Flops in the counter is defined in Table 4.2, from which one can get following logic functions :

$$D_0 = \overline{Q_0} \quad (4.2)$$

$$D_1 = Q_0\overline{Q_1} + \overline{Q_0}Q_1 = Q_0 \oplus Q_1 \quad (4.3)$$

$$D_2 = Q_0Q_1\overline{Q_2} + \overline{Q_0}\overline{Q_1}Q_2 = \overline{\overline{Q_0Q_1Q_2} \cdot \overline{Q_0Q_1Q_2}} \quad (4.4)$$

$$D_3 = Q_0Q_1Q_2\overline{Q_3} + \overline{Q_0}\overline{Q_1}\overline{Q_2}Q_3 = \overline{\overline{Q_0Q_1Q_2Q_3} \cdot \overline{Q_0Q_1Q_2Q_3}} \quad (4.5)$$

$$D_4 = Q_0Q_1Q_2Q_3\overline{Q_4} + \overline{Q_0}\overline{Q_1}\overline{Q_2}\overline{Q_3}Q_4 = \overline{\overline{Q_0Q_1Q_2Q_3Q_4} \cdot \overline{Q_0Q_1Q_2Q_3Q_4}} \quad (4.6)$$

Since the working period of *adder*₁ is from the zeroth bit to the fifteenth bit, *adder*₂ has one bit more delay than *adder*₁ and *adder*₃ has two bit more delay than *adder*₁. Therefore the carry removing signal stated in Section 2.1 should come at the beginning of each adder cycle, in other words, the least significant bit of each adder or the zeroth bit for *adder*₁, the first bit for the *adder*₂ and the second bit for *adder*₃. Since *adder*₃ starts at the second adder cycle, a control signal *R*₀ is required to latch the sixteen D-Flip-Flops of *Accumulator*₂ block to zero before the eighteenth bit from the beginning. This is a reset signal, its value should be “low” before the eighteenth bit and “high” thereafter.

The fifth D-Flip-Flop and a two bit counter can be used to generate the reset control signal *R*₀, Fig.4.5. At the sixteenth bit, *Q*₄ becomes ‘high’, while *Q*_B stays ‘low’ until the eighteenth bit, which results in *R*₀ changing to ‘high’. *R*₀ is fed back to the inputs of the *DDF*₄ and *DDF*_B in Fig.4.5 to keep their outputs “high”. Hence, after the eighteenth bit, *R*₀ will stay at ‘high’.

Order of bit	Q_0	Q_1	Q_2	Q_3	Q_4	D_0	D_1	D_2	D_3	D_4
0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	1	0	0	0
2	0	1	0	0	0	1	1	0	0	0
3	1	1	0	0	0	0	0	1	0	0
4	0	0	1	0	0	1	0	1	0	0
5	1	0	1	0	0	0	1	1	0	0
6	0	1	1	0	0	1	1	1	0	0
7	1	1	1	0	0	0	0	0	1	0
8	0	0	0	1	0	1	0	0	1	0
9	1	0	0	1	0	0	1	0	1	0
10	0	1	0	1	0	1	1	0	1	0
11	1	1	0	1	0	0	0	1	1	0
12	0	0	1	1	0	1	0	1	1	0
13	1	0	1	1	0	0	1	1	1	0
14	0	1	1	1	0	1	1	1	1	0
15	1	1	1	1	0	0	0	0	0	1
16	0	0	0	0	1	1	0	0	0	1
17	1	0	0	0	1	0	1	0	0	1
18	0	1	0	0	1	1	1	0	0	1
19	1	1	0	0	1	0	0	1	0	1

Table 4.2: The working sequence of a five bit counter.

Figure 4.5: Reset control signal (R_0) generator.

The three carry removing signals CR_1 , CR_2 and CR_3 can be derived by using three 4-input-NAND gates. One of them should be 'low' at the zeroth, first or second bit, while 'high' at other bits.

This counter can generate control signals, but can not work at high frequency, because of the delay introduced by the large number of gates. To solve this problem a much simpler four bit counter is designed, Fig-4.6 (a). This circuit works faster than the previous one but still not fast enough (Max. clock frequency is 35.7 MHz).

A half synchronize counter can be used to further reduce the complexity. Fig-4.6 (b). Since it is not a fully synchronized counter, the delay between the two synchronized parts makes the width of the first carry removing signal CR_1 narrower. To solve the problem only one four input NAND gate is used to obtain a word clock and two D-Flip-Flops are adopted to obtain the carry removing signals with one or two bit delay. Since the outputs Q_i ($i = 0, \dots, 3$) of the four bit counter do not become "high" at the same time, the word clock is obtained from the fifteenth bit and then delayed one bit by DFF_{05} to get CR_1 . In Fig-4.6 (b), the reset control signal (R_0) generator is moved after DFF_4 . After CR_3 becomes "low" and Q_B becomes

“high”, R_0 toggles to “high”. The logic equation of D_{R0} is:

$$D_{R0} = \overline{C} \overline{R_3} Q_B + R_0 = \overline{\overline{\overline{C} \overline{R_3} Q_B} \cdot \overline{R_0}} \quad (4.7)$$

(Note: so far, all DFFs are initially set to zero.)

If DFF_{05} , DFF_4 and DFF_5 are set to “high” initially, the two bit counter can be removed. Fig.4.6 (c) shows the final circuit diagram of control block. Comparing Fig.4.6 (c) with the previous configurations, one can see the former is much simpler, which requires less area and works faster (Max. frequency is 41.6 MHz).

2 of/de 2

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS
STANDARD REFERENCE MATERIAL 1010a
(ANSI and ISO TEST CHART No. 2)

Figure 4.6: Circuit diagram of the control block.

4.5 U' Signal Generator

U' is the signal which is used to replace the U in Fig.3.12. The value of U' shown in Table 4.3 is defined to be A for the first bit, B for the second bit, and I any other time, where I is an input signal. The logic equation is:

$$\begin{aligned} U' &= ICR_2CR_3 + A\overline{CR_2}CR_3 + BCR_2\overline{CR_3} \\ &= \overline{ICR_2\overline{CR_3} \cdot BCR_2\overline{CR_3} \cdot A\overline{CR_2}CR_3} \end{aligned} \quad (4.8)$$

According to Eq-4.8, four 3-input-NAND gates and a D-Flip-Flop are used, Fig.4.7. The D-Flip-Flop is used to prevent spikes.

Figure 4.7: Logic diagram of the U' Signal Generator block.

Chapter 3 described the process for obtaining the division ratio N from Eq-3.10. By substituting $m_1 = N_c - m_2$ in Eq-3.10, one can get:

$$N = N_c n_1 + m_2 \quad (4.9)$$

Where m_1 is the number of times divided by n_1 and N_c is the modulus of the counter. Since m_2 is the number of times divide by $n_1 + 1$ in a repeat period, now it should be:

$$m_2 = I_n + 2P \quad (4.10)$$

$\overline{CR_2}$	$\overline{CR_3}$	U'
0	0	I
1	0	A
0	1	B

Table 4.3: The relation among inputs and output of the U' Signal Generator block.

P is the possibility of either the first bit or the second bit of U' is 'high', in other words P is the average bit stream density of overflow. It depends on the value of K and M, $P = \frac{K}{M}$. By $\frac{M}{2} \leq K \leq \frac{3M}{2}$, one can get $0.25 \leq P \leq 0.75$ and $0.5 \leq 2P \leq 1.5$. I_n is the number of "1"s in the other fourteen bits and it is an integer. Therefore,

$$N = N_c n_1 + I_n + 2P \quad (4.11)$$

Since $N_c n_1 + I_n$ is an integer and $2P = \frac{2K}{M}$ is a number varying from 0.5 to 1.5, by fixing M and varying the value of K, N can be changed continuously.

4.6 Circuit Synchronization

Fig.4.8 shows the circuit diagram of Fig.4.1 (a). In Fig.4.8, the fast clock should be connected to the clock inputs of all D-Flip-Flops unless otherwise specified. The reset signal should go to the Reset or Set inputs of all D-Flip-Flops except the shift register in *Accumulator*₂. These two signals are not shown entirely for the sake of clarity.

As stated at the beginning of this chapter, the three adder cycles are delayed one bit delay from each other. *DDF*₃₆ is connected between *adder*₁ and *adder*₂ to get the one bit delay. The output *V*₀₁ of *adder*₂ is passed through *DDF*₁₁ for the same reason.

The overflow of the *adder*₃ is the carry of its most significant bit, which is feedback to control A and B in the selecting switch circuit. This function is the same as a analog feedback loop. Generally speaking, in a feedback loop, the feedback signal is proportional to the output signal. Here if there is no overflow (*A* = *B* = 'low'), the output of selecting switch is zero, i.e., zero feedback. If there is only one adder cycle with overflow (*A* = 'high' or *B* = 'high'), the output of the selecting switch is -*M*. If there are two or more adder cycles with overflow, the output of the selecting switch should be -2*M*. *DDF*₁, *DDF*₂ and *DDF*₁₄ are used to obtain A and B. Among the three D-Flip-Flops *DDF*₁₄ is used to pick up the overflow, its clock can be the third carry removing signal *CR*₃. Since the Data input of a D-Flip-Flop is a large load, two inverters must be connected to the overflow signal to prevent the delay of the feedback signal from becoming too large to catch the overflow. Another method to pick up the overflow is using a logic multiplexer controlled by *CR*₃. If *CR*₃ is "low", the input of *DDF*₁₄ *D*₁₄ equals the value of feedback signal, otherwise *D*₁₄ equals the output *Q*₁₄ of *DDF*₁₄. In this way *DDF*₁₄ can use the common clock. It can be seen that the latter is less time sensitive than the former. Once *DDF*₁₄ catches a overflow,

Figure 4.8: Circuit diagram of a Second Order Digital Σ - Δ Modulator and U' Signal Generator.

B becomes 'high' at the beginning of the next word cycle and A becomes 'high' at the beginning of the third word cycle. Hence, DDF_1 and DDF_2 should be clocked by the first carry removing signal CR_1 .

Since there are many stages from the inputs of the selecting switch (-M, A, B) to the output of $adder_1$ S_1 , introduces a long delay for the signal going through this path in one bit cycle, and it is possible for this delay to cause error in high frequency operation. DDF_{37} is used to prevent the accumulation of delay by cutting this path into two bit cycles.

Since $-2M$ is obtained by shifting $-M$ one bit left (Section 4.3), the zeroth bit of $-2M$ should be always 'low'. But if the fifteenth bit of $-M$ is 'high', this '1' can be the sixteenth bit of $-2M$, which means the zeroth bit of $-2M$. This is an error. It can be seen that the DDF_3 should be reset to zero at fifteenth bit of $-M$ to ensure the output of DDF_{37} equals 'low' at the zeroth bit of $-2M$ when the output of selecting switch block C is $-2M$. The first carry removing signal CR_1 can be used as this reset signal. But since the pulse width of CR_1 is too wide to catch the next bit, a narrow pulse generator can be used to get a more narrow pulse as the reset signal. Fig.4.9. Another approach to make the output of D-Flip-Flop 3 zero at the zeroth bit of $-2M$ is to control its input. Since the m_{94} signal is one bit earlier than CR_1 , it can be used as the control signal. If m_{94} is "low", D equals "low", otherwise D equals $-M$. This relation can be expressed as:

$$D = -M \cdot m_{94} = \overline{\overline{-M} + \overline{m_{94}}}, \quad (4.12)$$

where D is the Data input of DDF_3 .

An AND gate or two inverters and a 2-input-NOR gate can be used to obtain D. Since m_{94} is a key signal to generate all control signals in the circuit, and heavier loading may result in the signal arriving too late and causing wrong operation, two

Figure 4.9: A narrow pulse generator.

inverters and a 2-input-NOR gate are chosen because the inverter is a smaller load than an AND gate.

4.7 Simulation

The circuit of Fig.4.8 is simulated by *SILOS*, a logic simulation program developed by SIMUCAD Inc., Menlo Park, California. The fast clock is a square-wave with 10 MHz frequency. Four groups of K and M values have been tested, Table 4.4. Since errors occur most frequently at the beginning and end of a digit, the four groups of numbers try to consider as many possibilities as possible at the two ends.

Fig.4.10 is the flow chart of the second order digital Σ - Δ modulator. A software simulation program written in "C" was developed to simulate the flow chart. The four groups of K and M in Table 4.4 have been used.

The two sets of simulation results are compared bit by bit and they are the same as expected. Fig.4.11 is the FFT result of the bit stream of overflow obtained from logic simulation results. It is clear from Fig.4.11 that the quantization noise has been suppressed around the clock frequency, which indicates proper operation as a Σ Δ bit-stream generator. The spectrum will be used to compare with the chip testing

Group No.	K (decimal)	K (binary)	M (decimal)	-M (binary)
1	12817	0011001000010001	12800	1100111000000000
2	34850	1000100000100010	62943	0000101000100001
3	20865	0101000110000001	48891	0100000100000101
4	33308	1000001000011100	29166	1000111000010010

Table 4.4: Testing values of K and M.

result in Section 4.9.

Figure 4.10: A flow chart of the Second Order Digital Σ - Δ Modulator.

Figure 4.11: FFT result of the overflow bit stream.

4.8 Logic Verification Before Layout by LCA

A Logic Cell Array (LCA) is a user-software-programmable gate array. It is manufactured with a matrix of user-configurable logic blocks and a ring of input-output blocks. The channels between blocks are occupied by segmented metal interconnects and programmable switching points. The user's program defines the state of switching points through a nearby SRAM cell, and in this way groups and interconnects the logic blocks into useful functions — logic gates, flip-flops, multiplexers, buffers, and so on. It can be seen that LCA device is a very flexible tool to speed up the circuit design, logic verification, and design optimization.

The circuit in Fig.4.8 has been down loaded to a 48 pin M2064 LCA chip by using LCA design software packages including SCHEMA, SCH2SILO, PCSILOS, P&R, XACT. Among them SCHEMA is used for circuit diagram drawing. SCH2SILO can

generate a net list for logic simulation and layout. PCSILOS is a logic simulator available on the PC. P&R can give the bit code or the interconnection commands of LCA, and by running XACT one can down load the bit code to a LCA chip. The down loaded 48 pin M2064 LCA chip has been tested to verify the logic circuit before layout.

Fig.4.12 shows the testing equipment setting. The DC source is a 0-5 volt DC voltage from a HP6216A Power Supply. the clock is a square-wave generated by a HP3325B Data Signal Generator, which also gives a synchronize signal used to control a HP8180A Data Generator. The input data K, -M, I and Reset signal are obtained from 8180A. The output signals Word Clock, O_{D16} , S_1 , V_{01} , V_{02} and CV_{02} are fed into HP8182A Data Analyzer; thus they can be compared with the simulation result bit by bit. The overflow of the Σ - Δ modulator CV_{02} is fed into a HP4195A Network/Spectrum Analyzer and a KEITHLEY 196 system DMM at the same time. The latter is used for testing the DC component of CV_{02} . The spectrum of CV_{02} is the same as Fig.4.17 in Section 4.9. The waveform of CV_{02} and U' is displayed on a HITACHI Digital Storage Oscilloscope. Fig.4.13 (a) and (b) show the waveforms of U' and CV_{02} . Since CV_{02} is the same as B (Fig.4.8), A is delayed than B one word cycle, which means the value of B_{n-1} should be the same as the Value of A_n , where X_n is the value of X at n'th word cycle and X stands for A or B. From Fig.4.13 it can be seen that the first and the second bit of U' varies with the value of A, B, Table 4.5, while the other fourteen bits are the same as the input data I.

As stated in Chapter 2, the output pulse density of an analog Σ - Δ modulator should be proportional to the value of the input signal. In a digital Σ - Δ modulator, for a certain value of M, the pulse density of the overflow signal has this same relationship to the input signal. In other words the relation between the DC voltage of

Figure 4.12: LCA chip testing environment.

the overflow signal CV_{02} and input data K should be linear,

$$V_{DC} = V_{DD} \frac{K}{2M}. \quad (4.13)$$

A problem found in simulations and testing was that for the values of $M=12800$, $529 \leq K \leq 15889$, a nonlinear relationship was obtained when $K \leq 5649$. The reason is that plus $-M$ is used instead minus $+M$ which generates many false overflows during addition and accumulation. The false overflows are caused by the sign change in binary operation.

There can be two solutions: the first is to modify the circuit. Simulation shows that under certain conditions one can obtain a linear relationship at CV_{02} . The conditions are:

(a)

(b)

Figure 4.13: Waveforms of U' and CV_{02} from LCA testing.

$A_n=B_{n-1}$	B_n	1'st bit of U'	2'nd bit of U'	Position on Fig.4.13
0	1	0	1	1 (a)
1	1	1	1	2 (a)
1	0	1	0	3 (a)
0	0	0	0	4 (b)

Table 4.5: The relation among A, B and U'.

If the most significant bit of V_{01} is 'high', $K \leq 5649$ and carry overflow is 'high' then CV_{02} should be 'low' (The overflow is not true).

One more input signal IK is needed. If $K \leq 5649$, IK is 'high'. If $K > 5649$, IK is 'low'. From above discussion, three 2-input-NAND gates and two inverters can be used, Fig.4.14.

Figure 4.14: Proposed modification of the Digital Σ - Δ Modulator.

The second approach is to keep the circuit unchanged but to reduce the value of M. This will reduce the slop and the linear range of the DC values at CV_{02} but still meet the requirements. In the test, $M = 8192$ and $4113 \leq K \leq 12305$ are used.

No.	K (binary)	K (decimal)	V_{DC} (f=1MHz)	V_{DC} (f=10.2MHz)
1	000100000010001	4113	1.19V	1.18V
2	0001010000010001	5131	1.49V	1.47V
3	0001100000010001	6161	1.79V	1.77V
4	0001110000010001	7185	2.09V	2.06V
5	0010000000010001	8209	2.39V	2.35V
6	0010010000010001	9233	2.68V	2.65V
7	0010100000010001	10257	2.98V	2.94V
8	0010110000010001	11281	3.28V	3.24V
9	0011000000010001	12305	3.58V	3.53V

Table 4.6: Testing results of the V_{DC} at CV_{02} .

A linearly changed DC voltage has been obtained from both simulation and testing, Tabel 4.6 is the testing results at 1 MHz and 10.2 MHz clock frequency.

4.9 Chip Testing Results

An integrated circuit version of the digital Σ - Δ modulator was carried out after the above design and verification process. Fig.4.15 shows the layout of Fig.4.8, which is done manually using *VALE*, a physical layout editor developed by METHEUS corporation Inc., Hillaboro, Oregon. The chip size is $4607 \times 3756 \mu m^2$. This chip is also fabricated by NTE through CMC in a $3\mu m$ CMOS process.

The testing environment is the same as Fig.4.12 excepting the LCA chip is replaced by the one shown in Fig.4.15. The bit string of CV_{02} obtained from the 8182A is compared with the simulation result bit by bit and they are identical. The maximum operating frequency is 29.5 MHz. Fig.4.16 (a) and (b) are the waveforms of U' and CV_{02} , where one can find that the relation between the values of the first and second bit of U' and the values of A, B are the same as in Table 4.5, while the waveform is much less noisy than Fig.4.13. This may be due to the reduced length of

interconnection in the IC chip compared to those of the LCA chip.

Figure 4.15: Layout of the Second Order Digital Σ - Δ Modulator and U' Signal Generator (chip CU049).

Fig.4.17 shows the spectrum of CV_{02} obtained from the 4195A at 16 MHz clock frequency. Comparing Fig.4.17 with Fig.4.11 in Section 4.7, one can see that they are quite similar. Since the frequency of the word clock is 1 MHz, one can see the noise shaping around the 1 MHz frequency.

(a)

(b)

Figure 4.16: Waveforms of U' and CV_{02} from chip testing.

Figure 4.17: Tested spectrum of CV_{02} .

4.10 Joint Testing of Two Chips

Since both chips (CU051 and CU049) have been tested, it is possible to connect them together to form a fractional N frequency divider system. In this system, the chip CU051 is equivalent to a divide by 12,13 divider. Its output is used as the bit clock of the Σ - Δ modulator (chip CU049), and the word clock of the Σ - Δ modulator is the output of the fractional N divider. Fig.4.18 (a) shows the block diagram of such a system.

The test equipment setup is shown in Fig.4.18 (b). The $\pm 2.5V$ DC supply voltage and the bias voltages are given by a general purpose test board. The input clock of chip CU051 obtained from a HP4195A Network/Spectrum Analyzer is a 150 MHz sine-wave. The bit clock (*Odiv4* on CU051) is a square-wave with 11.5 MHz to 12.5 MHz frequency, which is used as the synchronization signal of HP8180A Data Generator. A high speed TTL buffer is connected between *Odiv4* and the 8180A in order to increase the driving ability of the *Odiv4* signal. The input signals of chip CU049 (*Clock*, *K*, *M*, *I* and *Reset*) are generated by the 8180A. The output signal *U'* of CU049 is used as the input signal *Y* of CU051 in order to control the switching between two division ratios. The output signal *Word Clock* is fed into HP3585A Spectrum Analyzer. Other outputs are connected to HP8182A Data Analyzer. Since *K* is set to 8209 and *M* = 8192, in Eq-4.11, $N_c = 4 \times 16$, $n_1 = 3$, $I_n = 2$, thus *N* is about 196. Therefore, the frequency of *Word Clock* signal should be around 765 KHz. Fig.4.19 shows the spectrum of this signal. One can see that the marked frequency is 769 KHz, which agrees with the calculated results. The theoretical phase noise power spectrum is also shown in Fig.4.19 to compare with the measured result. The equations used to calculate the ideal phase noise spectral density $S_\phi(f)$ of such a system are given by [2]:

(a) Block diagram of the tested system.

(b) Test equipment setup.

Figure 4.18: Test environment of the fractional N divider system.

$$S_{\phi}(f) = \left(\frac{f_d Q(f)}{(f - f_d) \cdot N} \right)^2 \quad (4.14)$$

and

$$Q(f) = 2\pi \sqrt{\frac{2N}{3f_{clock}}} \left(1 - \cos\left(2\pi \frac{(f - f_d) \cdot N}{f_{clock}}\right) \right) \quad (4.15)$$

where f_d is the carrier frequency, N is the fractional division ratio and f_{clock} is the

Figure 4.19: Tested spectrum of the fractional N frequency divider output (CU051) and comparison with theoretical result.

input clock frequency, f_{ref} in Fig.4.18 (a). One can see from Fig.4.19 that there is more noise around the carrier frequency. The noise may come from the testing equipment, TTL buffer and other noise sources. (In Fig.4.19, the theoretical result, $S_{\phi}(f)$, is the phase noise spectral density, the carrier frequency is not shown. The

accuracy of Eq-4.14 and Eq-4.15 is reduced as the frequency is far away from the carrier frequency due to the approximation used in the equations.)

After replacing chip CU051 by CU055, the system is tested again. The equipment setup is the same as Fig.4.18 (b) but the 150 MHz clock signal is given by HP8663 Synthesized Signal Generator and the *Word Clock* signal of CU049 is fed into 4195A. Fig.4.20 shows the spectrum obtained from 4195A. Comparing with Fig.4.19, one can find the two tested results are similar on the property of noise shaping.

Figure 4.20: Tested spectrum of the fractional N frequency divider output (CU055).

Chapter 5

CONCLUSIONS

5.1 Summary

A high speed CMOS fractional N frequency divider has been designed and tested. The divider can be used in a fractional division PLL synthesizer for application in high frequency telecommunication systems.

After the introduction to the thesis, some background and known examples of dual modulus divider techniques have been reviewed. The design of the fractional N divider was then described in detail. Two parts have been discussed: The design of a dual modulus frequency divider and the design of a second order digital Σ - Δ modulator.

After logic design and HSPICE simulation of the dual modulus frequency divider, a chip layout has been done manually by ELECTRIC. The timing analysis has also been done by theoretical calculation. Chip testing shows that at certain bias voltages, the input clock frequency can be up to 250 MHz.

The logic design of a second order digital Σ - Δ modulator has been verified by SILOS simulation, 'C' language program simulation, Logic Cell Array testing before layout and chip testing after layout. The four results have been compared bit by bit

and no bit error among them was found. The maximum bit clock frequency can be up to 29.5 MHz.

Finally, joint testing has been taken and the spectrum of the output of the fractional N divider shows a good noise shaping behavior.

Since the implementation of the high speed dual modulus frequency divider and the digital second order Σ - Δ modulator are both first time achieved, the contribution of this thesis should be emphasized on VLSI design aspect.

5.2 Future Work

Future work can focus on increasing speed and flexibility of the fractional N divider. Since the present chips are implemented in $3\mu m$ CMOS, it can be migrated into $2\mu m$ CMOS, $1\mu m$ CMOS or BICMOS process so that higher speed can be achieved.

As stated in Chapter 3, the speed of the two modulus frequency divider is limited by the control blocks. To simplify the control circuit is another possibility of increasing speed.

The two chips (CU055 and CU049) can be integrated into one single chip, the Divide-by-4 block and the U signal generator block in Fig.3.1 should be removed. Fig.5.1 shows the block diagram of this chip. In Fig.5.1, the Control Logic block includes the Phase Control block in Fig.3.1 and the U' Signal Generator in Fig.4.1 (a). Since the maximum operating frequency of the Σ - Δ modulator is 29.5 MHz, it is possible at high f_{ref} , to have the bit clock frequency higher than the maximum operating frequency of the Σ - Δ modulator (29.5 MHz). In other words the fractional N divider may be disabled at high frequency. There are two solutions: to improve the speed of the Σ - Δ modulator or to increase the division ratio of the dual modulus divider.

Figure 5.1: Block diagram of an integrated digital fractional N divider.

The ring oscillator can be made with $2n+1$ stages ($n = 1, 2, 3, \dots$) and the division ratio can be changed from 3,4 into 5,6, 7,8, etc. by making different connections between available pads on the chip. In this way the fractional N divider will become more flexible.

Appendix A

CHIP BONDING DIAGRAMS

Figure A.1: Two modulus divider chip (CU051) bonding diagram.

Pin Number	Type	Signal
7	Input	Vnclock
8	Input	Vpclock
9	Input	Y
10	Output	Odiv4
20	Power	V_{DD}
21	Power	V_{SS}
30	Input	Reset
31	Output	Test

Table A.1: CU051 Pad number and name.

CMC MULTIPROJECT BONDING DIAGRAM

RETICLE CODE U41MBRAND ID LABEL IC3

OTHER IDENTIFICATION FEATURES _____

CU055

WAFER NUMBERS _____

DESIGN FILE REFERENCE _____

PACKAGE		IDK40F1-192G	L10		C-493-175-35M	
WIRE ALLOY	99% Al/1% Si	DIA.	.001"	ELONG.	1.5 - 4%	T.S.
	99% Al/1% Si		.00125"		1.5 - 4%	
D/A PREFORM		ALLOY 98% Au/2% Si		RECOMMENDED SIZE		W/B METHOD U.S.

BONDING DIAGRAM

- NOTES: 1. DIE ATTACH PAD SIZE: .400 X .400
2. ZERO GROUND

Figure A.2: Two modulus divider chip (CU055) bonding diagram.

Pin Number	Type	Signal
1	Power	VSS_2
2	Power	VDD_2
7	Input	NCLK_2
8	Input	PCLK_2
9	Power	VDD_1
10	Input	NCLK_1
11	Input	PCLK_1
12	Input	Y
13	Output	ODIV4
19	Power	VDD_3
20	Power	VSS_3
29	Input	Reset
30	Output	Test
31	Power	VSS_1
32	Input	IN
40	Output	OUT

Table A.2: CU055 Pad number and name.

SMC MULTI-PROJECT BONDING DIAGRAM
RETICLE CODE 136A2
OTHER IDENTIFICATION FEATURES _____
WAFER NUMBERS _____
DESIGN FILE REFERENCE _____

BRAND ID LABEL TC3
CU049

PACKAGE		IDK40F1-192G		LID		C-493-175-35M	
WIRE ALLOY		99% Al/1% Si		DIA.		.001"	
		99% Al/1% Si				.00125"	
				ELONG.		1.5 - 4%	
						1.5 - 4%	
				T.S.		14-16 Gms	
						18-22 Gms	
D/A PREFORM		ALLOY 98% Au/2% Si		RECOMMENDED SIZE		W/B METHOD U.S.	

BONDING DIAGRAM NOTES: 1. DIE ATTACH PAD SIZE: .400 x .400
2. ZERO GROUND

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Figure A.3: Σ - Δ Modulator and U' Signal Generator chip (CU049) bonding diagram.

Pin Number	Type	Signal
1	Input	K
9	Power	V_{DD}
10	Output	U'
11	Input	I
12	Output	CVO2
19	Input	M
20	Output	QD16
21	Output	Word Clock
22	Input	Clock
23	Input	Reset
31	Output	VO2
32	Output	VO1
37	Power	V_{SS}
40	Output	S1

Table A.3: CU049 Pad number and name.

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4.5 U' Signal Generator

U' is the signal which is used to replace the U in Fig.3.12. The value of U' shown in Table 4.3 is defined to be A for the first bit, B for the second bit, and I any other time, where I is an input signal. The logic equation is:

$$\begin{aligned} U' &= ICR_2CR_3 + A\overline{CR_2}CR_3 + BCR_2\overline{CR_3} \\ &= \overline{ICR_2\overline{CR_3} \cdot BCR_2\overline{CR_3} \cdot A\overline{CR_2}CR_3} \end{aligned} \quad (4.8)$$

According to Eq-4.8, four 3-input-NAND gates and a D-Flip-Flop are used, Fig.4.7. The D-Flip-Flop is used to prevent spikes.

Figure 4.7: Logic diagram of the U' Signal Generator block.

Chapter 3 described the process for obtaining the division ratio N from Eq-3.10. By substituting $m_1 = N_c - m_2$ in Eq-3.10, one can get:

$$N = N_c n_1 + m_2 \quad (4.9)$$

Where m_1 is the number of times divided by n_1 and N_c is the modulus of the counter. Since m_2 is the number of times divide by $n_1 + 1$ in a repeat period, now it should be:

$$m_2 = I_n + 2P \quad (4.10)$$