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Title of Thesis — Titre de la thèse

"DESIGN AND CHARACTERIZATION OF A
MICROPROCESSOR-CONTROLLED DIGITAL WAVEFORM
RECORDER"

University — Université

CARLETON UNIVERSITY, OTTAWA, CANADA

Degree for which thesis was presented — Grade pour lequel cette thèse fut présentée

Master of Engineering

Year this degree conferred — Année d'obtention de ce grade

1984

Name of Supervisor — Nom du directeur de thèse

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DESIGN AND CHARACTERIZATION OF A MICROPROCESSOR-CONTROLLED
DIGITAL WAVEFORM RECORDER

by

© Carlos Roberto Pon, B. of Tech.

A thesis submitted to the Faculty of Graduate
Studies and Research in partial fulfillment
of the requirements for the degree of

Master of Engineering

Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada
April 1984

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ABSTRACT

This thesis describes the design and performance of a digital waveform recorder which digitizes and stores single-shot signals with a real time sampling rate of 500 KHz using a 12 bit ADC. In addition to the real time capabilities, two other sampling schemes, sequential and random sampling are included in the system to digitize and store repetitive signals with a virtual sampling rate of 25 MHz or higher, subject to the limitations of digital hardware.

The system is characterized in the time and frequency domain for each sampling scheme. Finally applications are included such as the evaluation of transfer functions for linear systems.

ACKNOWLEDGEMENTS

The author wishes to thank with deep appreciation his program supervisors, Prof. C. H. Chan, and Prof. M. A. Copeland for the professional guidance, financial and moral support through the extent of this thesis.

The author is also indebted to Dr. E. Samson for his collaboration in the software support of the system, and to N. Mikhail for his contribution in the hardware.

Last but not least. I would like to thank my family, and especially my wife Sonia for her strong support during this study. This thesis is especially dedicated to my little daughter Chantal.

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LIST OF SYMBOLS

A	Peak Amplitude
AC	Alternating Current
A/D	Analog to Digital
ADC	Analog to Digital Converter
B	Full scale range of the ADC
BM	Buffer Memory
C	Offset in volts
C ₁ , C ₂	Capacitors
CMOS	Complementary Metal Oxide Semiconductor
CRT	Cathode Ray Tube
D	Harmonic Distortion
dB	Decibels
DAC	Digital to Analog Converter
DC	Direct Current
Δf	Discrete frequency resolution in Hz
Δt	Aperture Uncertainty
DFT	Discrete Fourier Transform
D.S.O.	Digital Storage Oscilloscope
D.P.O.	Digital Processing Oscilloscope
ΔV	Analog interval in the ADC
EOC	End of Conversion
ENB	Effective Number of bits
f	Frequency
f _c	Nyquist Frequency

LIST OF SYMBOLS (cont.)

FF1 to FF5	Flip Flop 1 to 5
FFT	Fast Fourier Transform
f_s	Sampling Frequency
FS	Full Scale
FSR	Full Scale Analog Range of the ADC
GHz	Gigahertz
HMD	Hold Mode Droop
HW	Hanning Window
I/O	Input/Output port
K	Scale factor for displaying sampled data in a CRT
KHz	Kilohertz
LSB	Least Significant Bit
MHz	Megahertz
mV	Millivolts
MF	Memory Full
MSB	Most Significant Bit
N	Number of bits for ADC
NMOS	N-Channel Metal Oxide Semiconductor
nsec	Nanoseconds
P	Phase in radians
P(nth Code)	Probability of occurrence for code bin N
PDF	Probability Density Function
P ² CCD	Profiled Peristaltic Charge-Coupled Device
PIA	Peripheral Interface Adapter
ppm	Part per million
PRNG	Pseudo Random Number Generator

LIST OF SYMBOLS (cont.)

psec	Picoseconds
Q	Minimum step size for an ADC
Q_1 to Q_5	Outputs of a D flip flop from 1 to 5
RAM	Random Access Memory
rms	Root Mean Square
S	Least Square Function
S/H	Sample and Hold
S/N	Signal to Noise ratio
T	Sampling Interval
T_A	Aperture time
T_C	Conversion time for the ADC
T_D	Time delay
t_0	Time of trigger recognition
t_1, t_2, t_3	Sampling instant of time
t_Q	Quantization time
t_W	Time window
U.S.B.	Useful Storage bandwidth
μA	Microamperes
usec	Microseconds
V	Volts
VDT	Video Display Terminal
VLSI	Very Large Scale Integration
v_1, v_2, v_3	Voltage instant of time
W	Write pulse
ω	Frequency in rad/sec

LIST OF SYMBOLS (cont.)

$ W(f) $	Magnitude spectrum of a rectangular or a Hanning window
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CHAPTER I

INTRODUCTION

1.1 Motivation for thesis

The motivation for this thesis is to develop and build a prototype of a digital signal acquisition unit which, coupled with an inexpensive oscilloscope and a microcomputer will provide some of the capabilities of a digital storage oscilloscope (D.S.O.) and digital processing oscilloscope (D.P.O.). Although such instruments have existed previously as complete units, they have been expensive and fairly specific in purpose. With the development of a modular unit as described in this thesis, it is possible to adapt to the needs of the user readily and, more importantly, at a lower cost. This should supply the Department of Electronics with a tool to support the work of other graduate students, as well as a possible introduction of some experiments in undergraduate laboratories.

1.2 Background

For the last three decades, oscilloscopes have been among the most versatile and widely used tools by engineers. Technology over the years has brought power to this instrument by increasing bandwidth and sensitivity, and improving triggering circuitry and even adding storage capability. Now, with digital technology reaching the point where a microprocessor is a common component in many systems today, it is appropriate to bring digital signal processing capabilities into the oscilloscope.

Like a conventional instrument, the digital storage oscilloscope (D.S.O.) contains a signal acquisition unit and a

display unit (figure 1.1a). In addition, the oscilloscope in this thesis contains a third section, called a processor, which has the ability to digitize an acquired waveform, to provide an interface with a minicomputer, and to store digital data and convert it to analog form for display (figure 1.1b), [1]. The total apparatus is capable of performing the functions of a Digital Processing Oscilloscope (D.P.O.). The applications of this instrument, complete with a minicomputer, are limited only by the imagination of the user. A few of the more obvious ones are:

- Signal averaging to extract signals from noise.
- Viewing of a signal after passing it through an arbitrarily constructed digital filter, including one that may not even be realizable in conventional circuitry.
- Display of a signal in the frequency domain by calculating its Fourier transform.
- Automatic scaling of a displayed waveform in any convenient form (a logarithmic frequency scale, for example).

The final unit that will be developed will be that labelled as the "Digital Waveform Recorder" in figure 1.2. The major design decision that will be necessary in the design of this unit is in the approach used for acquisition of the signal.

Essentially, three sampling approaches exist, which will be described in more detail in chapter 2. These are: sequential, random and real time sampling. The real time sampling technique is the only method that can acquire single event signals and to accomplish that it takes samples of the input signal continuously for a finite time [2].

Fig. 1a. Conventional oscilloscope contains an acquisition and display unit.

Fig. 1b. Digital processing oscilloscope also contains a processor for linking scope to a computer.

Fig. 1.2 Final unit diagram and its interface.

Random and sequential sampling techniques only work for repetitive events. Both techniques work well for high frequency signals. Random sampling shows the pulse leading edge without a delay line but the acquisition rate is not equal to the signal occurrence rate, and does not work well with smoothing. Sequential or repetitive sampling works well with smoothing techniques, because of feedback methods, but the CRT will not show the pulse leading edge without a delay line or pretriggering [3,4].

1.3 Thesis Objective

One of the main goals for this waveform recorder unit is to have flexibility in the acquisition of the input signal. In this thesis the objective is to incorporate the three signal acquisition techniques named in the previous section, although the random technique is a modified one, plus additional features to allow common measurements including instantaneous, maximum, minimum, peak to peak, rms and mean values of the signal.

Averaging of the signal is also included to reduce random noise in the input signal, and additional functions such as differentiation, integration, linear interpolation, and expansion can be added. This unit should also include a standard form for interfacing with an external minicomputer, such that complex signal processing can be performed.

1.4 Thesis Format

Chapter 2 of this thesis discusses the three techniques found in most digital sampling oscilloscopes for the acquisition of signals, giving advantages and drawbacks of the different schemes.

In chapter 3 the hardware architecture and software development of the waveform recorder are presented. Chapter 4 is devoted to the dynamic test performance of the unit, in the time and frequency domain.

Finally applications and conclusions are summarized in chapter 5, including some recommendations for future work.

CHAPTER II

BACKGROUND INFORMATION

2.1 Introduction

There are five elements that are common to any digitizing scheme. These are: One or more ADC, a digital memory, timing circuits, display circuitry, and control circuitry. The control circuitry may be either very elementary or quite sophisticated, incorporating microprocessors with extensive firmware. The difference between various approaches resides in the techniques used in the signal acquisition. There are three schemes that have been used in digital sampling oscilloscopes, which will be described in this chapter.

2.2 Real Time Sampling

This is the most common technique that has been used for most instruments, with analog signals being sampled on a periodic basis as illustrated in figure 2.1a. The train of sampling pulses in figure 2.1b represents a fast acting switch which connects to the analog signal for a very short period of time and then disconnects for the remainder of the sampling period. The result of the fast acting sampler is identical with multiplying the analog signal by a train of sampling pulses of unity amplitude, giving the modulated signal of figure 2.1c.

For a signal which is bandwidth limited and contains no frequency components higher than f_c , the signal can be recovered without distortion if it is sampled at a rate of at least $2f_c$ samples per second. Frequency f_c is called the Nyquist frequency for this sampling frequency.

Fig. 2.1a Original input signal.

Fig. 2.1b Sampling pulses.

Fig. 2.1c Sampled signal.

Any sampling rate less than twice of Nyquist frequency will result in aliasing (figure 2.2), therefore the folded part of the spectrum causes distortion in the recovered signal, which cannot be eliminated by filtering the recovered signal.

In practice, because of nonideal bandlimiting of the signal, one should take at least $2.5f_c$ samples per second. Even then there is no complete recovery of information. For display uses, if the samples are not taken very frequently, the waveform that appears on the screen becomes a discontinuous sequence of dots. A demand for a continuous waveform display seems entirely valid. This can be accomplished if the digitized information is passed through an interpolator, in which a continuous signal can be re-created from the samples.

The more frequently samples are taken, the more accurate is the representation of the signal. This implies that the Useful Storage Bandwidth (U.S.B.) of a digital storage oscilloscope is related to both sampling rate and display technique.

The U.S.B. of a D.S.O. can be defined with the following equation.

$$\text{U.S.B. (MHz)} = \text{Digitizing Rate (MHz)} / K \quad (2.1)$$

where K is typically 25 for dot display, 10 for vector display, and 2.5 for a sine wave interpolator. Thus for sine waves, approximately 25 samples per cycle are necessary for a dot display to give an accurate representation of the signal. Joining the dots with vectors improves this ratio to only 10 samples per cycle. By internally processing the sinusoidal signal, it

Fig. 2.2a Continuous signal spectrum.

Fig. 2.2b Sampled signal spectrum.

requires only 2.5 samples per cycle to display sinusoidal signals.

A typical D.S.O. using real time sampling can be represented by the block diagram of figure 2.3, in which the signal after being conditioned is ready to be digitized, and then is stored in memory. Assuming real time sampling, a finite number of samples is taken. After the complete memory space has been filled, the signal is ready for being processed or displayed on the screen. The important thing about this is that there is a limited time to acquire the sample signal, quantize it and store it in memory. This time is shown in figure 2.1b as T . Then

$$T = t_Q \quad (2.2)$$

where t_Q = quantization time.

This indicates that the performance of this technique is limited by the digitizer, not by the front end analog or triggering circuitry, as is the case with analog scopes. D.S.O. today are limited to a maximum sampling rate of about 100 MHz at a resolution of 8 bits. Resolutions as high as 15 bits are available, but at 100KHz. Increasing these numbers is one of the key problems facing scope designers today. Faster, more precise ADC and faster, lower power Random Access Memories (RAM) are required.

Solutions to the performance problem are being sought both with conventional silicon technology, which is probably capable of providing digitizing rates in the range of 200 to 500 MHz, and with Gallium Arsenide, which should be able to reach 1GHz. In contrast, scan converters, which are CRT like devices, repla-

Fig. 2.3 Typical block diagram of a D.S.O. for real time sampling.

cing the scope face with an electronically-read storage matrix, have long been used for the most demanding applications, and can probably reach sampling rates of 2 to 5 GHz (Figure 2.4), [5].

In using silicon technology the only alternative for maximum speed is the flash ADC. However, here the effective resolution drops off significantly with sampling rate. For an 8 bit flash ADC, typically performance is equivalent to 7.1 bits of effective resolution for a 1 MHz signal; 6.1 bits at 10 MHz; and 5.1 bits at 35 MHz (the top end).

A different approach for storage of analog signals in real time before A/D conversion has been carried out using a fast analog shift register called a profiled peristaltic charge-coupled device (P²CCD) [6,7] as a sort of sample and hold circuit that stores signal samples in analog form at very high frequencies at one end and shift them down its length until it is full. It then holds the samples while the ADC digitizes them. Since that the ADC can read out a much lower rate, it allows the use of an inexpensive, compact low power ADC, and the resolution of the instrument does not decrease as the sampling rate increases. The drawback of this scheme is that signal inaccuracies are incurred in the long analog delays due to charge-transfer inefficiency and charge leakage. Today 256 analog signals values can be stored. It should be possible to increase this number in the future and make this approach more practical.

Acquisition in real time can also be manipulated by adjusting the sampling rate, in the same way as the sweep speed of the analog scope does it, specially for pulses, the sampling

Fig. 2.4 Cost versus speed for A/D converters using three different technologies.

rate is set in such a way as to take several samples on the transitions. The newer digitizer with programmable sample rate switching prove particularly well suited to the latter approach; setting them for dense sampling on fast transitions and for sparser sampling over the remainder of the waveform (figure 2.5) [8].

2.3 Sequential Sampling

This technique can deal with extremely high bandwidth signals as long as they are repetitive.

The implementation consist of taking one data point per sweep, and sampling the input signal at a slightly advanced point on each sweep (figure 2.6). Also, to reduce noise, the scope can perform averaging for repetition of the same signal, as long as the noise is uncorrelated with the input signal [9,10,11].

The disadvantage of the repetitive sampling is that it is not applicable for viewing single shot events. The advantage is that only one part of the circuit, the sampling head which takes the samples, has to have the full bandwidth. The other circuits work at a relatively low speed. By this means it is possible to avoid the fast ADC and fast memory needed in the real time technique.

With this technique the virtual sampling rate can be extended to a maximum. The bandwidth capability, depends on the narrow aperture time T_A of the sample and hold (S/H) circuit and in the time delay T_d (figure 2.6). Thus if T_A is choosen properly,

$$\text{Virtual Sampling Rate(MHz)} = 1/T_d(\text{usec}) \quad (2.3)$$

SEQUENTIAL SAMPLING

Fig. 2.6 Arbitrary waveform sampled sequentially.

A typical block diagram using this scheme is shown in Fig. 2.7.

A repetitive waveform and a synchronous trigger is presented to the acquisition system. At precisely the selected moment, the S/H gate opens for a very short selected period (aperture time), and the portion of the waveform existing during this time is digitized and stored in memory. By increasing the time delay, segments occurring further into the waveform are sampled, converted and continuously stored in memory. The process continues until sufficient points are captured, before the reconstruction of the original input signal. The variable delay time in Fig. 2.7 typically is accomplished with the circuit shown in Fig. 2.8.

The repetitive input signal is applied to the input of a S/H circuit and to the trigger input of a fast sweep generator. The fast sweep generator is adjusted to be triggered by the feature of the signal which is to be recorded and is set to complete its sweep in the period of interest after the trigger. A slow sweep generator which is slow enough to obtain sufficient samples is also started (Fig. 2.9). The sampling instant occurs when the two sweep generators are of equal amplitude as determined by a fast comparator circuit. There will thus be one sample taken each time the fast sweep generator is triggered. Since the sampling instant occurs a little later in the fast sweep each time, the sampled point is taken at increasing times in the signal waveform. The time between the fast sweep trigger and the sampling instant is called the sampling delay time.

Fig. 2.7 Simplified block diagram for a sequential sampling scheme.

Fig. 2.8 Variable delay for sequential sampling scheme.

Fig. 2.9 Timing diagram for the block circuit in Fig. 2.8.

2.4 Random Sampling

In this sampling system the sampling pulses are not held in a synchronized relation with the signal [4,12,13]. This scheme also requires a repetitive signal for a successful acquisition. A typical block diagram that represents random sampling is shown in Fig. 2.10.

The basic principle is demonstrated in conjunction with Fig. 2.11. Consider that we are interested in observing a time window t_w framed around an input signal. The point in time at which the input signal is of sufficient amplitude to cause a trigger recognition is at $t=t_0$. At this instant, t_0 , a step pulse called start is generated. The start pulse is applied to the linear timing ramp generator (Fig. 2.10). This allows the ramp voltage to begin its run up. Meanwhile a free running oscillator has been generating a train of strobe pulses that are completely unsynchronized with the input signal repetition rate. Thus the occurrence of a strobe pulse within the time window of interest t_w is a purely random coincidence. The strobe pulse is the command to the vertical sampling gate to take a sample of the input signal. Assume now that a strobe has occurred at time t_1 within the time window. The vertical channel now has a valid data point in the region of interest. At the same time the strobe t_1 stops the ramp at a voltage level which is thus proportional to the instant in time t_1 at which a vertical sample was taken. This voltage level is applied to a second S/H.

After converting both S/H signals to digital format through respective ADC, the number of bits that result from digitizing

Fig. 2.10 Simplified block diagram for a random sampling scheme.

Fig. 2.11 Basic random sampling timing diagram.

the horizontal signal are used to form part of the storage address. To this address, the number of bits of the vertical signal conversion is written.

The cycle may now be repeated with another randomly occurring coincidence between the signal and the strobe, say at t_2 , again within the time window but after t_1 ; then the stop occurs later in time, thus the ramp is allowed to run up to a much larger voltage v_2 , which corresponds to an increased address.

After each address is filled, a flag is set to indicate this. The process continues, many times until sufficient data are obtained to permit a relatively complete representation of the input signal. In those cases where the sampled signal instant time has occurred before, then average of the signal is done for that particular address. A good representation of the input signal is obtained when 99% of the allocated waveform memory locations are filled. Remaining unfilled points are then interpolated. The memory now contains the vertical values of the waveform in the horizontal sequence in which they were displayed.

With this technique the sampling rate will not depend on the speed of the ADC. The only limitation will depend on the aperture time of the S/H which is able to capture the instant of time of the signal.

$$\text{Virtual Sampling Rate (MHz)} = 1/T_A(\text{usec}) \quad (2.4)$$

where T_A = aperture time of the S/H

There are some disadvantages. Random sampling is like everything else in actual practice, i.e., compromises and

tradeoffs must be made. The major disadvantage of random sampling is the larger data acquisition time to obtain sufficient samples to adequately represent the input signal. The probability of a coincidence within the time window of the free running strobe and the input signal is quite low particularly if the time window is narrow and the signal repetition rate is low. This is the case used for observing an aperiodic recurrent signal.

2.5 Summary

Three sampling schemes were described, showing advantages and drawbacks between them. Although these methods are not of direct value for signal processing purposes, there are advantages in sampling in a random manner to overcome aliasing effects and aliasing noise.

In the next chapter the three schemes are implemented showing the design consideration of the hardware elements involved in the digital acquisition of signals.

CHAPTER III

HARDWARE AND SOFTWARE DESCRIPTION

3.1 Introduction

In this chapter the hardware and software of the acquisition system are described. The hardware possesses several novel features to allow data capture at virtual speeds of up to 25 MHz, using digital techniques and relatively inexpensive integrated circuits.

Two methods of sampling are described using this virtual 25 MHz sampling rate, Sequential and a novel Pseudo Random sampling technique.

For a more general purpose data acquisition system, the real time sampling scheme is also included, which will be capable of the simultaneous collection and storage of data. This technique will provide a tool to look at single shot events.

One of the most expensive elements in a real time acquisition unit is the ADC especially when the unit tries to reach its maximum speed and resolution. A relatively inexpensive ADC was chosen with 12 bit resolution and 2 usec conversion time. This converter uses a successive approximation 12 bit method. The ADC speed will allow measurement in real time with a maximum sampling rate of 500 KHz, assuming that memory write time is less than conversion time of the ADC. The 12 bit resolution will give a very wide dynamic range of the order of 72 dB, very well suited for applications found in many areas of science and technology.

3.2 Basic System Configuration

The basic system is based on an acquisition unit supported by a 6800 microprocessor. This processor performs two major operations, one as the controller of the acquisition system (figure 3.1), and second as the serial interface to a more powerful post-processor. In this particular project, a 16 bit MC68000 based microcomputer, the Omninet Corvus system was chosen to perform further digital signal processing.

This system will give the user the option of computer augmentation for data acquisition, data analysis, display, or interactive experimental control [1,14].

The software which is developed in 6800 assembler code allows the user to perform the following operations, some of which may be optional.

1. Different methods of acquisition

- Real time
- Non-real-time: Sequential
- Non-real-time: Random

2. Select sampling rate in the real time mode from 500 KHz down to 50 Hz.

3. Select trigger mode. Pre-trigger or Post-trigger.

4. Choice of averaging for repetitive signals.

5. Display the stored waveform in any analog scope.

6. Option of transferring the stored waveform through an RS-232C serial port to another computer (The Corvus Concept) for further data analysis.

Once the information is in the Corvus Concept, further

Fig. 3.1 Basic system configuration.

data analysis can be performed with a network station that offers the speed and computing power of a 16 bit microprocessor.

Since the station includes medium resolution graphics, visualization of the waveform can be done in the time and/or frequency domain on the VDT. In addition to the display capabilities, other operations such as interpolation, smoothing, addition or subtraction of waveforms, etc, can be easily incorporated through software control.

3.3 Hardware Consideration for Real Time Acquisition

This section introduces the constructed real time acquisition unit. The complete block diagram of this unit is shown in figure 3.2. Complete details will be given in the subsequent sections of this chapter.

The analog input signal is fed into the vertical preamplifier which boosts the amplitude to the desired level, up to the maximum of 10 V peak to peak. This output drives the trigger generator which provides the trigger signal for the control logic. The amplified signal then goes into a S/H which acquires the signal voltage when the trigger signal arrives and then holds its value while a 12 bit ADC converts the value into digital form. At the end of conversion the digital information is written into the Buffer Memory (BM) for temporary storage.

The address of the BM is controlled by a 12 bit synchronous counter, but only 11 bits are used to give access to 2048 locations in memory. The 12th bit is used as a flag for memory full.

A 2Kx12 Random Access Memory (RAM) is required to store

2048 ADC output samples of 12 bit each. The converter, memory and address counter are synchronized by the control logic circuit. The same signal clocks both the counter and the ADC.

After the BM completes the storage of 2048 samples of digital data (representing the analog signal), the system switches to the Read or Display mode. Data stored in BM are read and transferred sequentially through a parallel port to the microprocessor control system, which has a high density memory for data analysis. At the end of data transfer, the BM output is directed to a 12 bit DAC at a repetitive rate by continuously clocking the 12 bit BM address counter. The DAC output is a reconstruction of the analog signal sample by sample. By letting the clock run continuously, the repetitive output signal is suitable for oscilloscope display.

It is important to notice that in the block diagram of figure 3.2 several units are common to the three sampling schemes which will be described in details later.

3.3.1 Front End Signal Conditioning

The front end amplifier and the trigger generator are not included in this thesis. The vertical preamplifier which typically is variable in gain is replaced by a waveform generator for experimental purposes, and the synchronous output substitutes the main trigger generator. The important thing to note about real time digital acquisition units is that its performance is limited by the digitizer and the memory, not by the front end or the triggering circuitry. However the analog bandwidth of the input circuitry should ideally remain equal to the

Nyquist frequency; this procedure would reduce aliasing errors by attenuating frequency components above the Nyquist frequency before undersampling could alias them.

A 2 usec conversion time is required for A/D conversion, hence the maximum sampling frequency is 500 KHz. Consequently the bandwidth of the amplifier (including low pass filtering) for real time applications should be less than 250 KHz.

In the other two sampling schemes the 25 MHz virtual sampling rate will require a higher bandwidth of the order of 10 MHz. For the sequential sampling scheme an antialiasing filter should be carefully chosen to prevent "aliasing" high frequency noise down into the base-band region. For the random sampling scheme the implications of the Nyquist sampling theorem are not critical, therefore the front end for this scheme is free of low pass filtering.

3.3.2 The Sample and Hold

There are several parameters in the selection of the S/H which will meet the necessary accuracy requirement of the system.

The most critical part of sample-and-hold operation is during the short sample to hold transition when the sampling switch opens, which is called the aperture time. If the sampling process is consistent, aperture time becomes unimportant. The principal source of timing error is the aperture uncertainty, since too much uncertainty can create amplitude errors in digitizing. These errors, in turn, have an effect similar to reducing the effective digitizer bits [15,16].

Figure 3.3 illustrate the relationship between a clock pulse and a sampling window; noise prevents the strict maintenance of this relationship in practice, by jittering the window in time relative to the clock. Since an uncertainty curve associated with this jitter arises from noise, one can assume that the curve is Gaussian in shape. Thus, the maximum aperture uncertainty (Δt) can be defined at the 2-sigma point on the curve in figure 3.3.

Now an error analysis can be performed to determine the maximum aperture uncertainty (Δt) allowed for 1/2 LSB (least significant bit) of error when an n-bit system digitizes a sine wave in the area of its zero crossing (area of greatest slope, dV/dt). Using a sine wave of frequency f and of amplitude sufficient to exercise the full range of the digitizer, the analysis results in the following equation: (see Appendix A)

$$\Delta t = 1/\pi \cdot f \cdot 2^{N+1} \quad (3.1)$$

or, rearranging for frequency,

$$f = 1/\pi \cdot \Delta t \cdot 2^{N+1} \quad (3.2)$$

Employing this latter relationship and stipulating a total uncertainty of 100 psec, for example, enables the computation of the frequencies of full amplitude sine waves that an n-bit digitizer can process with no more than 1/2 LSB of error. The results are tabulated in table 3.1.

Fig. 3.3 Noise jitter alters the window aperture creating uncertainty in the digital conversion.

$\Delta t(\text{psec})$	n(number of bits)	f(KHz)
100	7	12,430
100	8	6,210
100	9	3,100
100	10	1,550
100	11	777
100	12	388
100	13	194
100	14	97
100	15	48
100	16	24

TABLE 3.1

Number of bits of the ADC versus frequency with
a constant aperture uncertainty of 100 psec.

Using again equation 3.2, by maintaining n constant as
a 12 bit resolution enables the computation of the frequencies
at full amplitude sine waves at different uncertainty times. The
results are shown in table 3.2

n(number of bits)	Δt (psec)	f(KHz)
12	400	97
12	300	129
12	200	194
12	100	388
12	90	431
12	80	485
12	70	555
12	60	647
12	50	777
12	40	971
12	30	1290
12	20	1940
12	10	3880

TABLE 3.2

Aperture uncertainty versus frequency with a
12 bit resolution.

Since the highest frequency in real time sampling that can be achieved with a 12 bit resolution is approximately 250 KHz, the use of 100 psec uncertainty is then the key parameter for the selection of the S/H as evident in table 3.2.

Another important parameter is the hold mode droop, which is defined as the output voltage change per unit of time while in the hold mode. This originates from the leakage current of the hold capacitor, the off-state leakage of the S/H, and the input bias current of the voltage follower in the S/H. For the 2 usec conversion time of the 12 bit ADC the hold mode droop (HMD) should be better than,

$$\text{HMD} = V_{FS} / 2^N \cdot T_C = 10 / 2^{12} \cdot 2 \cdot 10^{-6} = 1.22 \text{ (mV/usec)} \quad (3.3)$$

where T_C = conversion time of the ADC.

In addition hold mode droop changes exponentially with temperature. Most of the leakage that causes this droop comes from silicon devices. Since a device's leakage approximately doubles for every 10 °C increase in temperature, hold mode droop shares this characteristic.

Then if we want to operate the equipment between +25 °C to +55 °C, there is a 30 °C change, which means the HMD should be improved to better than 0.15 (mV/usec).

Another source of error in the hold mode droop is feedthrough. This parameter is the percentage of an input sinusoidal signal that is measured at the output of the S/H in the hold mode. A greatly attenuated version of the input shows up at the output, passing through switch capacitance and stray coupling capacitance. Values of feedthrough are expressed in % or in dB of attenuation. Then for a 12 bit resolution, it is required at least 72 dB or 0.01% feedthrough rejection.

Having decided the main parameters, a S/H HTC-0300 is selected (Appendix K).

3.3.3 The Analog to Digital Converter

The analog input signal is digitized by a 12 bit ADC (EH12B3) which uses a successive approximation algorithm for signal conversion. The selection of this converter was a tradeoff between speed and cost. A parallel converter would be very expensive and not feasible with 12 bit resolution, and a dual slope integrator is very slow for the application. Input signals for this converter must be within the range of -5 V to +5 V (bipolar mode). The output of the ADC is coded in offset binary format where the MSB indicates the sign of the input signal. Code 1 represents a positive input and a code 0 represents a negative one.

Sampling starts immediately after the first triggering signal, being synchronized with the programmable clock, which initiates the sampling pulse of 300 nsec duration necessary to obtain a 0.01% settling accuracy. The trailing edge of the sampling pulse triggers another monostable of 100 nsec which initiates the conversion of the ADC. The converter will put out an End of Conversion (EOC) pulse indicating that conversion is complete (figure 3.4). At this instant the digitizer signal has been latched in a 12 bit register ready to be stored in the buffer RAM. A Write (W) pulse of 90 nsec follows for data storage, whose address has been settled by the 11 LSB address counter. This sampling process continues at the rate of the programmable clock, until 2048 points have been obtained.

Figure 3.5 shows the S/H and the ADC with the power supply

Fig. 3.4 Timing diagram of a real time acquisition.

Fig. 3.5 The analog to digital converter.

connections. Two separate power supplies are used for the analog and digital sections. A dual supply with ± 15 V provides power to all the analog components of the circuit, and a +5 V supply with separate ground supplies the power to all the digital circuitry. The connection between the analog and digital grounds is internal to the ADC. This connection minimizes the introduction of digital noise into the analog circuitry.

3.3.4 Buffer Memory Storage

After the sampled signal is encoded through the ADC, the digitized signal is ready for storage. NMOS static Random Access Memories (RAM) 4802 are used to store 2048 points of the waveform on a 12 bit data bus, whose access time is less than the conversion time of the ADC. With RAM organization of $2K \times 8$ bits, 2 RAM chips are arranged in parallel with common address and control bus, as shown in figure 3.6, with one RAM for the lower byte and the other one for the next higher 4 bits. Since data input and data output in the RAM have common bus, it is necessary to use 3-state latches at the output of the ADC as well as the input of the DAC. This will make it possible to transfer data between RAM and the I/O parallel port without producing bus contention and interference with the DAC.

The system can be easily upgraded to 16 bits by just changing the ADC and DAC along with better and faster S/H part.

3.3.5 The Digital to Analog Converter (DAC)

For display purposes in an analog scope, the digitized signal stored in the BM is sent through a 12 bit DAC. To view a waveform with flicker free display, 20 msec per raster is

Fig. 3.6 Bus interconnection between ADC, DAC, EM, and I/O ports.

required on the CRT screen. If the waveform contains 2048 points, this gives a budget less than 10 usec per point. This requires that each digital step on the screen settle within 10 usec.

A DAC-69-12B is chosen with 5 usec settling time.

To reconstruct the original signal stored in the BM, the system switches to the READ mode, enabling only the latch at the input of the DAC. In this particular mode the address counter is incremented sequentially at a rate of 100 KHz. Since the counter output represents the address of the RAM then data output will represent the reconstructed analog signal. Because of the cyclic output of the counter, the analog output from the DAC becomes repetitive which can be displayed on any CRT oscilloscope. A trigger signal can be derived from the address counter (see figure 3.7).

Latches are used in the parallel inputs of the DAC to avoid interference when the system is operating in the sampling and transferring mode.

Also a smoothing low pass filter is provided at the analog output of the DAC to remove sampling frequency components for better quality display.

3.3.6 The Control Logic

The control logic provides the timing and control signals to coordinate the S/H, ADC, BM, DAC, Address Counter and Input/Output latches. There are three timing modes in this real time scheme.

- Sampling Mode
- Transferring Mode

Fig. 3.7 The digital to analog converter.

- Read Mode

In the sampling mode the input analog signal is stored sequentially in the BM. The input signal can be triggered in two different ways: Post or Pre-trigger.

When Post-trigger is selected, 2048 points are stored in memory immediately after the first trigger signal. Fig. 3.8 shows the control logic diagram. First an arming pulse is supplied to reset FF2. Q_2 will then enable FF1, which becomes ready for the trigger signal. Once the trigger arrives, $\bar{Q}_1$ starts a clear pulse for the address counter. This will initiate the storage from location zero in the BM. At the same time it will enable the output latch of the ADC, and the programmable clock, which runs the sampling cycle. Simultaneously Q_1 enables the write pulses for the RAM which are produced by the EOC signal from the ADC. The sampling process continues until the MSB of the address counter generates a Memory Full (MF) signal for the system, setting FF2, which then reset FF1. This MF pulse disables the following circuits: FF1, programmable clock, output latch, and write pulses (see Fig. 3.9 for timing diagram).

In the Pre-trigger selection, the system acquires the signal continuously until the trigger arrives. The BM then stores 2048 points before triggering, implying that we can see events 100 percent preceding the trigger signal. An arming pulse is produced to reset FF2. $\bar{Q}_2$ will then enable FF1, which simultaneously with the arming pulse set Q_1 and initiate the sampling process. This process finishes when the trigger signal arrives.

The system resumes control to the transferring mode. The

Fig. 3.9 Timing diagram for sampling mode in real time.

data stored in the BM is sent to the microprocessor memory, through a parallel port. Both input and output latches are disabled during this mode. The BM is read through a PIA (Parallel Interface Adapter) controlled by the microprocessor. This transfer of 2048 points to the microprocessor memory provides a temporary storage to perform instant signal processing, like averaging, which improves S/N ratio for repetitive signals; or it can be transported to a more powerful computer through a serial port (RS-232C) to perform further data analysis. All this is under software control.

At the end of transferring period, the system switches to the read mode. Only the output latches are enabled and data are read from BM to the DAC. The 11 stage binary address counter is clocked continuously at 100 KHz through all 2048 stages, and this provides the scanning of the entire captured waveform.

3.4 Repetitive Sampling

This sampling process can be accomplished in two different ways. Sequential or Random sequence.

Both sampling schemes are only valid for repetitive signals, which were discussed in chapter II.

This section shows the hardware implementation for both schemes.

3.4.1 Sequential Sampling

As in the real time sampling scheme, there are three timing modes, which are in the same sequence.

In the sampling mode, the signal to be digitized is sampled at different times during successive occurrences of

the signal..

Each of the repetitions in the waveform is referenced with respect to time, as indicated by points R in Fig. 3.10b. In this example, there are six repetitive cycles. Notice that each sample is delayed by T_d seconds plus a full period with respect to the previous sample. So sample 1 is taken T_d time away from the reference point, sample 2 is $2T_d$ from R, and so on.

Then by displaying these sampled values, we obtain the reconstructed input signal, as shown in Fig. 3.10a.

It is clear from both figures in 3.10 that the smaller the time interval, T_d , the better the resolution of the reconstructed waveform.

For this, the waveform and the sampling circuitry must have certain characteristics.

1. The waveform to be displayed has to be repetitive.
2. A circuit producing the time reference is needed.
3. A circuit to produce T_d and NT_d is required.
4. A very fast switch is needed as the sampling gate.

The first requirement is clear and needs no further explanation. The second point can be satisfied by using a triggering circuit. Whenever the waveform crosses a certain amplitude and slope, a trigger pulse is produced that can be used as a time reference. The third requirement T_d , $2T_d$, $3T_d$ and so on, can be obtained by using a programmable counter, which start to count down when the sample reference occurs. The microprocessor programs the counter to count down starting from the

Fig. 3.10a Reconstructed waveform. Fig. 3.10b Sampled waveform.

value of the next time increment between data points. Each time the counter reaches zero, a sample is taken. This is shown in Fig. 3.11.

A synchronous high speed counter with parallel load is used for this application. Since 2048 points are required to fill the BM, then an 11 bit counter is required. Three 74S163 have been connected as shown in Fig. 3.12, to form the 11 bit counter. With a 25 MHz clock a minimum T_d is 40 nsec. This will allow an equivalent sampling rate of 25 million samples/second.

The next limitation is how fast the S/H will sample without loosing resolution.

Recalling equation 3.1:

$$\Delta t = 1 / \pi \cdot f \cdot 2^{N+1}$$

Then for a 12 bit resolution and a maximum frequency of 12.5 MHz, the required aperture uncertainty is 3.1 psec. A S/H with this requirement becomes prohibitively expensive. Using the same S/H as the one being used for real time sampling, one can only attain 7 bit resolution.

Putting all together, the system for repetitive sampling is shown in Fig. 3.13.

After a control signal disconnect the timing logic used for real time sampling, the sequence of events are as follow:

1. A microprocessor program stores a number N in the output port.
2. A load signal stores this number N in the high speed counter.

Fig. 3.11 Microprocessor programmable digital delay.

Fig. 3.12 Hardware implementation of a digital delay using synchronous counters.

Fig. 3.13 System architecture for sequential and random sampling.

3. The trigger synchronized signal is enabled to start the counting.
4. At the end of counting, the carry output of the last stage will trigger a monostable to produce the sample. This sample is delayed by NT_d seconds with respect to the synchronized trigger signal.
5. At the end of the sampling pulse, the S/H switches to the hold position. Then the sampled signal is quantized by the ADC.
6. At the End Of Conversion (EOC) the digitized signal is latched, and sent through the I/O parallel port and to be stored sequentially in the microprocessor memory.

This complete sequence from 1 to 6 is repeated again for a number $N+1$, until 2048 points have been obtained.

The trigger enable circuit allows a trigger output only when the microprocessor has stored the preceding digitized signal in memory. This acknowledgement is done in the following manner, as shown in Fig. 3.14.

Timing signals are shown in Fig. 3.15. The enable signal from the microprocessor control set FF3. This FF3 absorbs the time difference between the arrival of the enable signal and the synchronized trigger signal. FF4 generates a one clock period output pulse and reset FF3.

The Q_4 output will set the last flip-flop to start the counting. Q_5 stays high until the end of counting, when the sampling pulse resets FF5.

With this method the equivalent sampling rate is not

Fig. 3.14 Circuit synchronizer.

Fig. 3.15 Timing diagram for the synchronizer.

limited by A/D conversion rate or computer speeds, since any number of cycles of the input signal may be ignored between data taking events.

After the sampling mode, the system switches to the transferring mode. The digitized data is transferred from the microprocessor memory to the BM. In this mode both input and output latches are disabled, and the parallel port is programmed as output. After all the digitized data is in the BM, this switches in the read mode, by enabling the output latches and setting the parallel port as input.

3.4.2 Random Sampling

This technique requires the same hardware as sequential sampling. The only modification is in the software.

As shown in Fig. 3.11, the input number N is incremented, under software control to obtain sequential sampling.

In the random sampling scheme, this number is given in a random order. Thus the digitized value is stored at the address given by the random number. This is shown diagrammatically in Fig. 3.16.

This sequence of numbers is generated by a random number generator, in which the sequence is initiated by a seed number. Since the sequence is always the same for a given seed number, the numbers generated are predictable and reproducible. Therefore, the sequences generated by these algorithms are more correctly called pseudorandom sequences and the algorithm used is called a Pseudo Random Number Generator (PRNG). This algorithm uses the mixed congruential method [17]. It generates a se-

Fig. 3.16a Reconstructed waveform. Fig. 3.16b Sampled waveform.

quence of random numbers by always calculating the next random number from the last one obtained given an initial seed. The formula for the congruential method is:

$$X(n+1) = ((A X(n)) + C) \text{ Modulo } M \quad (3.4)$$

where Modulo is the remainder function. In other words, $X(n+1)$ is the remainder of $((A X(n)) + C)$ divided by M .

This formula yields a pseudorandom sequence of length M (i.e. has period M) if and only if:

1. C is relatively prime of M .
2. $B = A - 1$ is a multiple of P for every prime P which evenly divides M .
3. If M is a multiple of 4, then B is also a multiple of 4.

The possible values of $X(n+1)$ are $0, 1, 2, \dots, M-1$, so that M represent the desired number of different values that could be generated. Thus M is equal to 2048, since this number represents the address space in the BM.

Then A and C must be chosen properly to guarantee that each number in the sequence occur only once. Since 2 is the only prime P that divides M , B can be any even number, and therefore A must be odd. Since B must be a multiple of 4, choosing $B=12$ gives the value of $A=13$. In this case, C can be any prime number other than 2. Using $C=13$ the above formula becomes:

$$X(n+1) = ((13 X(n) + 13) \text{ MOD } 2048) \quad (3.5)$$

In order to increase acquisition speed the random numbers are stored sequentially in a look up table.

CHAPTER IV

SYSTEM PERFORMANCE

4.1 Introduction

In this chapter, complete system performance is studied, including factors such as aperture uncertainty, quantization noise, resolution, offset, gain, and linearity errors. These are measured over a wide range of frequencies.

In the first section of this chapter a systematic error analysis of the waveform recorder is carried out. The remainder of the chapter is devoted to dynamic test methods and specifications under realistic operating conditions, for the three sampling schemes. These dynamic tests give the user a model of resolution versus frequency for the recorder.

All of the dynamic tests used for the waveform recorder use sinewaves as stimuli. These were chosen because they are easier to generate with adequate fidelity at the frequencies of interest. Also sine waves have a very predictable dV/dt and are bidirectional. At the same time a sine wave as a stimulus is the simple mathematical model a sine function provides for analysis. This benefit greatly simplifies the algorithms used for data analysis.

Three dynamic test for waveform recorder characterizations are presented here: sine wave curve fitting, histogram analysis, and discrete finite Fourier Transform. All these tests operate in the same way. A sine wave source is supplied to the waveform recorder and one or more records of data are taken. A computer is then used to analyze the data. The test differ primarily in

the analysis algorithms and consequently in the sort of errors brought to light. Critical to the success of these tests is the purity of the sine wave source. A synthesized source generator HP3320A is used to provide the short term and long term stability required by the dynamic range of the ADC.

Figure 4.1 shows the basic configuration for the dynamic tests. The output from the signal generator may contain nonlinearities and harmonics which are not desirable, in which case a filter may be inserted, reducing their amplitude to levels below which they cannot affect the test results. A KROHN-HITE model 3550 filter was used for these tests.

These tests provide the most stressful conditions for the ADC with the input signal amplitude at full scale. In general, nonlinear effects increase more quickly than the signal level increases because of the nonideal large-signal DC behaviour of the ADC components and the higher slew rates large amplitudes imply.

4.2 System Error Budget

The number of resolution bits of the ADC does not determine the relative accuracy of a data acquisition system. In fact, achievable relative accuracy is likely to be far different from the implied resolution, depending on the converter and S/H specifications and operating conditions. This means that the last few resolution bits may be meaningless in terms of realizable accuracy.

The best way to attack this problem is with a systematic error budget [18,19]. In a given system, this must be done not

Fig. 4.1 - Set up for the curve fit, histogram, and the FFT test.

only for the S/H and ADC, but also for other components in the front end, if they are included such as analog multiplexer, amplifier, etc.

In this particular waveform recorder, there are two major considerations in this budget, the S/H and the ADC.

The error budget for this system is determined based on the following assumptions: Operating temperature range between 25 °C to 55 °C, maximum power supply voltage change of 1 percent with time and temperature, and maximum input source impedance of 50 Ohms.

Given the specifications of the S/H and the ADC in table 4.1 and 4.2 respectively, the error analysis is as follow:

TABLE 4.1

Specifications for the S/H HTC-0300	
Nonlinearity	0.01 % maximum
Bias current	15 uA maximum
Offset versus temperature	40 uV/°C
Offset versus power supply	10 mV/V

TABLE 4.2

Specifications for the 12 bit ADC EH12B3	
Resolution	12 bits
Accuracy at 25 °C	$\pm .012\%$ of FS or $\pm 1/2$ LSB
Nonlinearity	$\pm 1/2$ LSB maximum
Differential Nonlinearity	$\pm 1/2$ LSB maximum
Differential Nonlinearity T.C.	± 3 ppm/°C maximum
Temp. Coeff. of Gain	± 30 ppm/°C maximum
Temp. Coeff. of Zero, Bipolar	± 15 ppm of FS/°C maximum
Power supply rejection	.01% FS/% supply maximum

Sample and Hold error analysis:

1. Nonlinearity is 0.01 %
2. Input bias current of 15 uA causes an offset error voltage in the source resistance.

Source resistance = 50 Ohms

Offset error = $50 \times 15 \times 10^{-6} = 750$ uV or 0.0075%

3. Offset versus temperature = 40 uV/°C

Since the temperature inside the housing may change by as much as 30 °C, the total change over the range will be: $40 \times 30 = 1200$ uV or 0.012%

4. Offset versus Power supply = 10mV/v

Since the supply may vary by 150 mV or 1% of 15V, the error contribution is 1.5 mV or 0.015%.

ADC error analysis:

1. Specified linearity error (relative accuracy) 1/2 LSB, or 0.0125%.
2. Quantizing uncertainty: 1/2 LSB, or 0.0125%.
3. Temperature errors:
 - a. Gain temperature coefficient= 30 ppm/°C.
For 30 °C change= 30x30= 900 ppm, or 0.09%
 - b. Zero temperature coefficient= 15 ppm/°C
For 30 °C change= 15x30= 450 ppm, or 0.045%
4. Power supply sensitivity error= 0.01%
5. Differential nonlinearity temperature coeff. = 3 ppm/ °C
For 30 °C change= 3x30 = 90 ppm, or 0.009%

The worst case arithmetic sum of all these errors is 0.2235% or equivalent to 8.8 useful number of bits. It is improbable that the errors will add in one direction. Statistical (RMS) addition of the errors yield a lower value, which uses the following formula:

$$\text{RMS}_{\text{error}} = \sqrt{E^2(1) + E^2(2) + \dots + E^2(n)} \quad (4.1)$$

where $E(i)$ is the respective error for $i = 1$ to n .

Substituting the values in formula 4.1, gives a $\text{RMS}_{\text{error}}$ equal to 0.1% or equivalent to 10 useful bits. This on the other hand, may be too optimistic since the number of error sources is small. At any rate, the maximum error will be somewhere between 0.22% and 0.1%, a significant difference from

what might be assumed as a 12 bit or 0.024% converter. The ideal relative accuracy has been degraded between 2 or 3.2 resolution bits.

This system error budget in conjunction with the S/H analysis shown in table 3.1 gives the overall theoretical performance of the system as plotted in Fig. 4.2.

4.3 Sine Wave Curve Fitting Test

This test gives a global description of the ADC. This means that the errors measured by the test are averaged to give a general measurement of the ADC transfer function. The result of this test is a figure of merit called the Effective Number of Bits (ENB) for the ADC. The effective bit number is a general measure of how much an ADC's nonlinearity has reduced its usefulness at a given frequency [8,16,20].

The number of effective bits is obtained by analyzing a record of data taken from a sinewave source. When the high purity sine wave has been converted and stored in digital form, the computer (post-processor) can begin its analysis. The first step is to fit a computer generated ideal sine wave of the form $[A \sin(Wt+P)+C]$ to the digital signal, where:

A= Amplitude in volts

W= Frequency in rad/sec

P= Phase in rad

C= Offset in volts.

Any difference between the data record and the best fit sine wave is assumed to be an error. (Fig. 4.3).

The standard deviation of the error is then calculated

Fig. 4.2 Theoretical system performance. Top line is the ideal one, and the shaded area correspond to the hardware limitation using the systematic analysis.

Fig. 4.3 Fitting a sine wave to the sampled signal under test.

and compared with the error of an ideal ADC of the same number of bits might generate. If the actual error calculated exceeds the ideal error, the number of effective bits exhibited by the ADC is less than the number of bits it digitizes. Errors that cause degradation in this test are nonlinear effects such as harmonic distortion, noise, and aperture uncertainty. Gain, offset, and phase errors do not affect the results since they are ignored by the curve-fitting process.

The effective number of bits (ENB) is computed using the following formula:

$$\text{ENB} = N - \log_2(\text{actual RMS error} / \text{ideal RMS error}) \quad (4.2),$$

where N is the number of ADC bits.

The ideal RMS error is assumed to be the quantization noise exhibited by an ideal ADC with a Uniform-Probability-Density (PDF) input such as a perfect ramp signal. Quantization noise from an ideal conversion is therefore a triangular waveform with a peak-to-peak value of Q. (See Appendix B). As with most noise sources, the average value is zero, but the RMS value is determined from the triangular shape to be:

$$\text{Ideal RMS Error} = Q / \sqrt{12} \quad (4.3)$$

where Q is the ideal code bin width, and is equal to:

$$Q = \text{FSR} / 2^N \quad (4.4)$$

where FSR= full scale analog range of the ADC.

The actual RMS error is simply the square root of the

sum of the squared errors of the data points from the fitted sine wave over the number of points.

$$\text{Actual RMS Error} = \sqrt{\frac{\sum_{k=1}^N [X_k - A \cos(Wt_k + P) - C]^2}{N}} \quad (4.5)$$

where X_k and t_k are the data points, N is the number of points in the record.

The algorithm used to perform the fitting operation is a variation of the least-squares routine, known as quasi-Newton algorithm. This algorithm consist in to find the best-fit sine wave to the data record by minimizing the error. The error is minimized by adjusting the fit parameters: frequency, phase, gain, and offset. The great pitfall of this algorithm is the lack of convergence, especially when the data record is very poor or computational resolution is inadequate, unless the guesses for the four parameters are within small error.

Since the initial guesses are very important factor, the solution of the minimization error equation is required. This is done by taking the partial derivative of the least square function with respect to each of the four parameters. The minimum error occurs when all of the derivatives are equal to zero. Then having:

$$S = \sum_{k=1}^N [X_k - A \cos(Wt_k + P) - C]^2 \quad (4.6)$$

where S = least square function, and taking the partial derivatives $\partial S / \partial A$, $\partial S / \partial C$, $\partial S / \partial W$, and $\partial S / \partial P$ gives the four simultaneous equations:

$$\sum_{k=1}^N X_k \cos(Wt_k + P) - A \sum_{k=1}^N \cos(Wt_k + P) - C \sum_{k=1}^N \cos(Wt_k + P) = 0 \quad (4.7)$$

$$\sum_{k=1}^N X_k - A \sum_{k=1}^N \cos(Wt_k + P) - CxN = 0 \quad (4.8)$$

$$\sum_{k=1}^N X_k t_k \sin(Wt_k + P) - A \sum_{k=1}^N t_k \cos(Wt_k + P) \times \sin(Wt_k + P) - C \sum_{k=1}^N t_k \sin(Wt_k + P) = 0 \quad (4.9)$$

$$\sum_{k=1}^N X_k \sin(Wt_k + P) - A \sum_{k=1}^N \cos(Wt_k + P) \times \sin(Wt_k + P) - C \sum_{k=1}^N \sin(Wt_k + P) = 0 \quad (4.10)$$

Substituting eq. (4.7) and (4.8) into (4.9) and (4.10), gives us the following two nonlinear equations (Appendix C):

$$\frac{\sum (X_k - \bar{X}) t_k \sin(Wt_k + P)}{\sum (X_k - \bar{X}) \cos(Wt_k + P)} = \frac{\sum [\cos(Wt_k + P) - \bar{X}] t_k \sin(Wt_k + P)}{\sum [\cos(Wt_k + P) - \bar{X}] \cos(Wt_k + P)} \quad (4.11)$$

$$\frac{\sum (X_k - \bar{X}) \sin(Wt_k + P)}{\sum (X_k - \bar{X}) \cos(Wt_k + P)} = \frac{\sum [\cos(Wt_k + P) - \bar{X}] \sin(Wt_k + P)}{\sum [\cos(Wt_k + P) - \bar{X}] \cos(Wt_k + P)} \quad (4.12)$$

where:

$$\bar{X} = \frac{1}{N} \sum_{k=1}^N X_k \quad (4.13)$$

and;

$$\bar{X} = \frac{1}{N} \sum_{k=1}^N \cos(Wt_k + P) \quad (4.14)$$

Equations (4.11) and (4.12) are solved iteratively, with only two fit parameters. Calling these equations R and S respectively, these errors parameters are minimized by adjusting the frequency and the phase. Since the frequency is known from the synthesizer generator, it is used as a good guess, leaving only the phase to be adjusted until R and S converge to a minimum. Once the frequency and phase are found, they are substituted in eq. (4.7) and (4.8); solving them for amplitude and offset. After these four parameters are found, they are fed into the Quasi-New-

ton routine, which calculates the final minimum error. This program was written in FORTRAN called Fitting (see Appendix C).

An HP7221 plotter was used to plot the data record and the error residue for different frequencies. This test was done for all three sampling schemes.

In Fig. 4.4 six examples are shown for sine waves from 1KHz to 224KHz, using real time sampling. The error residues are magnified 10 times. The amplitude of these errors are of the same level for all frequencies. The error is produced mostly from clock noise, and short term stability in the clock called jitter. This shows that the stability of the clock is not good enough, since the timing was derived from asynchronous counters, therefore one or more of the least significant bits of the digitized result will be in error. The effective number of bits in this test went from 9.05 to 8.5 bits, indicating not much variation over frequency.

Fig. 4.5 to 4.8 show sine waves from 100KHz up to 10MHz using the sequential and random schemes. In these figures, aperture uncertainty is identifiable because it generates an error that is a function of input slew rate. This error is mostly noticeable in the zero crossing, where sine waves change more rapidly. This error become dominant causing a low number of effective bits at higher frequencies. The ENB vary linearly with both input frequency and amplitude. A complete plot of ENB versus frequency is shown in Fig 4.9. Although sequential sampling seem to be the best, random sampling becomes better at the frequency rolloff of 400 KHz. For comparison the performance of two commercial waveform digitizers are shown in the

Fig 4.4
First 250 points in real time sampling of the curve fit data and the error residue from a fitted sine wave. a) For a 1112 Hz sine wave the ENB= 9.05 bits. b) For a 5.6 KHz the ENB= 8.85 bits.

c) For a 11.2 KHz sine wave the ENB = 8.75 bits. d) For a 56 KHz sine wave the ENB = 8.65 bits.

e) For a 112 KHz sine wave the ENB = 8.6 bits. f) For a sine wave of 224 KHz the ENB = 8.5 bits.

Fig 4.5
First 250 points of a sine wave at 100.75 KHz. a) For sequential sampling the ENB = 10.6 bits. b) For random sampling the ENB = 9.05 bits.

2

Fig 4.6

First 250 points of a sine wave at 1.03 MHz. a) For sequential sampling the ENB = 7.55 bits. b) For random sampling the ENB = 8 bits.

Fig 4.7

First 40 points of a sine wave at 5.123 MHz. a) For sequential sampling the ENB = 5.45 bits. b) For random sampling the ENB = 5.8 bits

Fig 4.8

First 40 points of a sine wave at 10.789 MHz. a) For sequential sampling the ENB = 4.7 bits. b) For random sampling the ENB = 5.04 bits.

Fig. 4.9 System performance of the waveform recorder. Lines with dots are experimental, remainder are theoretical.

graph of Fig. 4.10 with an 8 bit, 200 MHz unit (top), and a 6 bit device (bottom).

Another useful error measurement is the harmonic distortion. This error is usually a nonlinear function of amplitude and frequency. The distinguishing characteristic of this error is the presence of the harmonics (or aliased harmonics if the fundamental is close to the Nyquist frequency).

The usual method of measuring distortion involves tuning a notch filter to remove the fundamental frequency from the signal under test, so that the power in the harmonics can be compared to the power in the fundamental. This ratio is the percent of harmonic distortion [21].

Let us call the distorted signal under test as:

$$X(t) = f(t) + d(t) \quad (4.15)$$

where $f(t)$ is the pure sine wave (undistorted portion of $X(t)$), and $d(t)$ is the distortion. Conceptually, if the signal $X(t)$ is expanded in a Fourier series:

$$X(t) = \sum_{k=1}^N a_k \sin(K\omega t) \quad (4.16)$$

Then equation 4.16 represents the decomposition:

$$X(t) = a_1 \sin(\omega t) + \sum_{k=2}^N a_k \sin(K\omega t) \quad (4.17)$$

into the fundamental plus the harmonics (distortion). The harmonic distortion is defined as the ratio of the power in the distortion to the power in the fundamental,

Fig. 4.10 This graph plots examples of dynamic performance for two commercial waveform digitizers - an 8 bit, 200 MHz unit (top) and a 6 bit instrument with the same sampling rate (bottom).

$$D = \frac{\frac{1}{T} \int_0^T d^2(t) dt}{\frac{1}{T} \int_0^T f^2(t) dt} \quad (4.18)$$

where $f(t)$ and $d(t)$ have period T .

The numerator of Eq. (4.18) is simply $\Delta T/T$ times the least square function S of Eq. 4.5.

$$\frac{1}{T} \int_0^T d^2(t) dt = \frac{\Delta T}{T} \times S \quad (4.19)$$

The denominator is just the average power in the best fit sine wave, $f(t) = A \sin(Wt)$, which is:

$$\frac{A^2}{T} \int_0^T \sin^2(Wt) dt = \frac{A^2}{2} \quad (4.20)$$

Substituting 4.19 and 4.20 into 4.18, we have:

$$D = \frac{\frac{\Delta T}{T} \times S}{\frac{A^2}{2}} = \frac{2 \times \Delta T \times S}{T \times A^2} \quad (4.21)$$

Since $T = N \times \Delta T$, then,

$$D = \frac{2 \times S}{N \times A^2} \quad (4.22)$$

where N is the number of samples of the data record.

Then from equation 4.22 we can find the harmonic distortion versus frequency, which is shown plotted at Fig. 4.11. This plot show clearly that harmonic distortion increases with frequency for both schemes, although random sampling is less affected as indicated in the graph.

4.4 Histogram Testing

This test provides both a localized error description and

Fig. 4.11 Harmonic distortion versus frequency.

some global description of the ADC. Using the histogram test, it is possible to obtain the differential nonlinearity of the ADC, to see whether any missing codes exist [20,22]. Such an error is introduced if the ranges of analog values, represented by the same digital codeword, are not constant for all codewords. Conversely, the output codeword should occur with the same frequency if all analog amplitudes are equally frequent. However, in real ADCs, a systematic variation in the size of the analog ranges corresponding to different digital codewords will rapidly cause large errors in the frequencies of occurrence of the different codewords.

The ideal characteristic transfer function of a 3 bit ADC is shown in Fig. 4.12a. The analog intervals ΔV which are represented each by a specific digital code have all the same size (except for 000 = $1/2 \Delta V$), so that every digital number has the same probability of occurrence, when an equally distributed analog signal is applied to the input. The quantizing error of $\pm 1/2$ LSB is inherent also in the ideal ADC as represented in Fig. 4.12a.

In Fig. 4.12b an ADC having nonideal positions of the transitions is shown. To simplify, it is assumed here that all bit transitions except that for the LSB are ideally positioned, only the transition of the LSB are out of place by $1/2$ LSB. These position errors are very common with ADCs with feedback techniques and result from a nonideal adjustment of the internal DAC resistor network. The incorrect transition of the LSB has two major effects. First, the quantization error of the ADC in the example of Fig. 4.12b goes from $+1/2$ LSB to -1 LSB and differs,

Fig. 4.12a Ideal conversion relationship in 3 bit ADC.

Fig. 4.12b Conversion relationship in 3 bit ADC at boundary of $\pm 1/2$ LSB error tolerance.

therefore, by $1/2$ LSB from that of the ideal ADC (this being in accordance with specifications of most ADC manufacturers). Second, as a consequence of this, there is a large difference in the occurrences of certain digital values, when an equally distributed analog signal is at the input. For instance, in the example of Fig. 4.12b state 010 has a field of $3/2 \Delta V$ and state 001 only $1/2 \Delta V$, this means that state 010 occurs 3 times more often than state 001. In this example, each even number 2, 4, 6, ... has a frequency of occurrence which is 150 percent and each odd number 1, 3, 5, ... one which is 50 percent of the real value. The result is a dither in the probability distribution. In real ADCs, not only the transitions of the LSB are out of place but also those of the higher order bits so that dither appears not only between neighboring digits, but also between every 4th, 8th, 16th, 32th, ... amplitude number.

To test the ADC for a uniform probability distribution a ramp voltage is necessary to sweep all digital codewords. Since there is no equipment available to supply ramp voltages at frequencies of 10 MHz (for maximum frequency), a sine wave-based-histogram test is used.

The same setup of Fig. 4.1 is used where a statistically significant number of samples of the input sinusoid are taken and stored as a record. The frequency of code occurrence in the record is then plotted as a function of code. For an ideal ADC, the shape of the plot would be the PDF of a sine wave (Fig. 4.13) provided that the input and sample frequencies are relatively independent. The PDF of a sine wave is given by: (See Appendix E)

Fig. 4.13 Sine wave probability density function.

$$P(V) = \frac{1}{\pi\sqrt{A^2 - V^2}} \quad (4.23)$$

where A is the sine wave amplitude and V is the independent variable (voltage). For a real ADC, fewer than the expected number of occurrences for a given code bin indicates that the effective code bin width is smaller than ideal at the input frequency. No occurrences indicates that the code bin width is zero for that input. A greater than expected number of occurrences implies a larger than ideal code bin width.

It has been shown [20] that 100,000 samples would give 99.9 percent confidence that the peak deviation is less than 0.5 LSB. The notion of confidence relies on the input's being a random process. We can model the sine wave input as random process only if the input and sample frequencies are relatively independent.

The specification of greatest interest that can be calculated using the histogram test is differential nonlinearity. Differential nonlinearity is a measure of how each bit varies in size with respect to the ideal, which is calculated as:

$$\text{Differential Nonlinearity} = \frac{\text{Actual } P(\text{nth code})}{\text{Ideal } P(\text{nth code})} - 1 \quad (4.24)$$

where Actual P(nth code) is the measured probability of occurrence for code bin n, and Ideal P(nth code) is the ideal probability of occurrence for code bin n. The code bin number n goes from 1 to 2^N , where N is the number of ADC bits. To calculate the probability for each code in the actual data record, the number of occurrences for each code is divided by the number of samples in the record. The ideal probability of occurrences is what an ideal ADC would generate with a sine wave input. For

each code bin, this is the integral of the probability density function of a sine wave over the bin defined as:

$$\text{Ideal } P(V) = \int \frac{1}{\pi \sqrt{A^2 - V^2}} dV \quad (4.25)$$

for an ideal ADC,

$$V = \frac{X \times B}{2^N} \quad (4.26)$$

where B is the full scale range of the ADC in volts, and X is a particular code bin which can take values between -2^{N-1} to $+2^{N-1}$.

Substituting 4.26 in 4.25, and inserting the limits for two consecutive codes, it becomes:

$$\text{Ideal } P(n) = \frac{1}{\pi} \int_{n-1-2^{N-1}}^{n-2^{N-1}} \frac{dX}{\sqrt{\frac{A^2 2^{2N}}{B^2} - X^2}} \quad (4.27)$$

The solution of the integral becomes:

$$\text{Ideal } P(n) = \frac{1}{\pi} \text{SIN}^{-1} \left(\frac{X \times B}{A \times 2^N} \right) \Bigg|_{n-1-2^{N-1}}^{n-2^{N-1}} \quad (4.28)$$

substituting the limits,

$$\text{Ideal } P(n) = \frac{1}{\pi} \left[\text{SIN}^{-1} \left(\frac{(n-2^{N-1}) \times B}{A \times 2^N} \right) - \text{SIN}^{-1} \left(\frac{(n-1-2^{N-1}) \times B}{A \times 2^N} \right) \right] \quad (4.29)$$

A program called Histogram (Appendix F) is used to calculate the histogram for different sine waves. This program collects data until 100,000 points are reached, when they are displayed on the VDT screen. Fig. 4.14 shows the histogram for a sine wave of 1.789 MHz using sequential and random sampling. A judicious

choice of the frequency for the input sinusoid is necessary for realistic test results. An input frequency that is submultiple of the sample frequency violates the relative independence criterion and will result in sampling of the same few codes each input cycle. Fig. 4.14 shows very much similarity for both samples schemes. Fig. 4.15 shows the correspondent differential nonlinearity errors in LSB, although sequential sampling shows lower discontinuities, both schemes have the same amount of average error, approximate about 1.1 LSB. A program called PDF (Appendix G) is used to calculate the differential nonlinearity from an histogram record. Fig. 4.16 shows the histogram for a sine wave of 10.789 MHz. It is clear on the figure the reduction of the amplitude which is affected by the roll-off gain response in the S/H. Notice also the offset error which is shown by the shift of the complete curve from the 2048 output code. Fig. 4.17 shows the correspondent differential nonlinearity indicating an improvement of the discontinuities by the random sampling. Again for both schemes, the average error is the same, about 1.34 LSB.

Finally an histogram for a real time application of 11.2 KHz sine wave is shown in Fig. 4.18, with the respective DNL error. The average DNL is equal to 1.08 LSB.

For comparison Fig. 4.19a shows data from a commercially available, 8 bit 20 MHz ADC for an input sine wave at 9.85 MHz, while Fig. 4.19b shows data from an 8 bit, 100 MHz ADC taken at 9.85 MHz. In both figures large differential nonlinearities and numerous missed codes are apparent.

Fig. 4.14. A 100,000 sample histogram with a 1.789 MHz sine wave input.
a) For sequential sampling. b) For random sampling.

Fig. 4.15. Differential Nonlinearity errors in LSB, taken from the histogram record 4.14. a) For sequential sampling the average DNL= 1.11 LSB. b) For random sampling the average DNL= 1.13 LSB.

Fig. 4.16. A 50,000 sample histogram with a 10.789 MHz sinewave input.
a) For sequential sampling. b) For random sampling.

Fig. 4.17. Differential Nonlinearity error in LSB. a) For sequential sampling DNL= 1.34 LSB. b) For random sampling DNL= 1.34 LSB.

Fig. 4.18. a) A 100,000 sample histogram with a 11.2 KHz sinewave input for a real time sampling. b) Differential Nonlinearity = 1.08 LSB.

Fig. 4.19a A 100,000-sample histogram plot for a commercially available 20 MHz, 8 bit ADC with a 9.85 MHz input. Large differential nonlinearities and numerous missed codes are apparent.

Fig. 4.19b A 100,000-sample histogram plot for a 100-MHz, 8 bit ADC with a 9.85 MHz input sampled at 20 MHz. Extremely large differential nonlinearities and numerous missed codes are apparent.

4.5 FFT Testing

The Fast Fourier Transform (FFT) is used to characterize an ADC in the frequency domain in much the same way that a spectrum analyzer is used to determine the linearity of an analog circuit. The data output for both techniques is a presentation of the magnitude of the Fourier spectrum for the circuit under test. Ideally the spectrum is a single line that represents the pure sine wave input and is free of distortion components generated by the circuit under test. There are, however, significant differences between the spectrum analyzer and ADC spectra because of the sampling operation of the ADC, [23,24,25,26].

Let's first recall the integral Fourier transform:

$$X(f) = \int_{-\infty}^{+\infty} x(t) e^{-j2\pi f t} dt \quad (4.30)$$

where $x(t)$ is a continuous time domain function, and $X(f)$ is the corresponding frequency domain function for which the integral transform is to be evaluated. The equation 4.30 includes the amplitude and phase of every frequency in $x(t)$. The Fourier transform cannot be used in this form for an ADC, because $x(t)$ is only digitized at a finite number of points, N , spaced Δt seconds apart. Instead, the Discrete Fourier Transform (DFT) must be used. It is defined as:

$$X(k\Delta f) = \Delta t \sum_{n=0}^{N-1} x(n\Delta t) e^{-j(2\pi/N)nk} \quad (4.31)$$

where k and $n=0,1,2,\dots,N-1$; Δt is the time domain sampling interval, and N is the number of samples taken over the interval of $(N-1)\Delta t$.

There are significant differences between $X(f)$ and $X(k\Delta f)$. While $X(f)$ has infinite spectral resolution, $X(k\Delta f)$ has a discrete frequency resolution of $\Delta f = 1/N\Delta t$ because of the finite number of points in the data record.

Now the Fast Fourier Transform is nothing more than a time saving computer algorithm for evaluation of the DFT, so its mathematical properties are completely analogous to the DFT's. Similarly, the errors associated with the FFT derive from the DFT, known as leakage and aliasing.

Leakage arises from the fact that the waveform is studied over only a short period (or window) of time. So whenever a nonintegral number of cycles of $x(t)$ is contained in the record, sharp discontinuities will exist at the points where the start of one record joins the end of the preceding record. Since sharp phenomena in one domain are spread out in the other domain, we would expect the spectrum of a sine wave to be spread out through the frequency domain.

The spectrum smearing can be explained as follows. The finite record size of $x(t)$ can be considered the consequence of multiplying $x(t)$ by a rectangular function having unity amplitude during the time period $N\Delta t$ that the record is acquired and zero amplitude elsewhere. Since multiplication of two functions in one domain (time, in this case) is equivalent to convolution in the other, the spectrum of $X(k\Delta f)$ is derived by convolving $X(f)$ with $W(f)$, the Fourier transform of the rectangular window. $W(f)$ is the familiar $\text{sinc}X/X$ function (see Fig. 4.20a for $|W(f)|$), consisting of a main lobe surrounded by a series of sidelobes whose

Fig. 4.20 Time domain and frequency domain representations of rectangular and Hanning windows.

amplitudes decay at a 6 dB per octave rate. It is these sidelobes that are responsible for leakage. Even if the spectrum of $X(f)$ is a single line, the sidelobes of $W(f)$ during convolution smear the energy in the single line into a series of spectral lines spaced $1/N\Delta t$ apart whenever the frequency of $x(t)$ is not an integral multiple of $1/N\Delta t$.

Leakage can be reduced by multiplying the data in the record by a windowing function that weights the points in the center of the record heavily while smoothly suppressing the points near the end. Many different windowing functions exist that offer various tradeoffs of amplitude resolution versus frequency resolution. A function commonly used with sine waves is the Hanning window, defined by:

$$HW = \frac{1}{2}(1 - \cos(2\pi t/N\Delta t)) \quad (4.32)$$

Notice in Fig. 4.20b that both the window and its derivative approach zero at the two end of the record and that the transform's main lobe is twice as wide as that of the rectangular window, while the amplitudes of the sidelobes decay by an additional 12 dB per octave. The reduced level of the sidelobes reduces leakage, but the wider main lobe limits the ability to resolve closely spaced frequencies. Furthermore, the shape of the main lobe can attenuate the spectral amplitudes of $X(f)$ by as much as 1.5 dB. However, for the FFT testing to be described here, the Hanning window was selected as a good compromise between frequency and amplitude resolution.

The second error introduced by sampling is called aliasing. This arises if the waveform is sampled at too slow a rate. The

sampling process causes the two-sided spectrum of $X(f)$, symmetrical about the origin, to be replicated at the sampling frequency f_s and at all of its harmonics. If $X(f)$ contains components that exceed $f_s/2$, then these components are folded back, or aliased, onto spectral lines below f_s , causing aliasing errors. The frequency $f_s/2$ is sometimes called the Nyquist frequency, referring to the Nyquist criterion, which requires the sampling rate to be twice the highest frequency present in the input signal to define the waveform uniquely. The result is that the spectrum of $X(k\Delta f)$ is displayed only from DC to $f_s/2$ and the maximum input frequency must be limited to be less than $f_s/2$ to avoid aliasing.

The FFT test set up is the same as in Fig 4.1. The low pass filter was used only up to the maximum frequency of 200 KHz. A full scale sinewave of properly chosen frequency is applied to the waveform recorder under test. A 1024 points record sampled at the maximum frequency rate is then taken and given to the computer, which calculates the DFT using an FFT algorithm. The spectral magnitude is then plotted as a function of frequency in the screen of the VDT or, for a hard copy, the data points are sent to the HP7221 plotter.

Useful information about the ADC's performance can be derived from three features of the spectra: the noise floor, the harmonic level, and the spurious level.

Two classes of noise sources determine the level of the noise floor. The first is called quantization noise. This is the error, bounded by $\pm 1/2$ LSB, that is inherent in the quantization of the input amplitude into discrete levels. The higher the number

of bits, the smaller the error bound and, therefore, the lower the noise floor. For an ideal N bit ADC the quantization noise is theoretically known to have a signal to noise ratio equal to: (see Appendix H).

$$S/N = (6N + 1.8) \text{ dB} \quad (4.33)$$

Fig. 4.21 presents the magnitude of the spectra derived from the FFT for a sine wave of 11.2 KHz used with a 12 bit and 8 bit resolution converter in a real time sampling scheme. S/N ratio was measured with respect to noise floor since the others peaks correspond to harmonic components. This show a signal to noise ratio below the ideal limit which is indicative of errors of all types that the ADC produces.

The second class of noise source includes wideband noise generated within the ADC, along with other sources. In a successive approximation ADC, for example, the internal function of the comparator is critical to conversion accuracy, particularly when high precision, high speed conversions is to take place [27]. However, there are other major sources of noise which affect the ADC performance. These include noise generated in the signal and reference source resistances, noise in the reference generator itself, noise in switched constant current sources or voltage sources, power supply generated noise (including ground loop currents), etc. Furthermore, aperture jitter is another major source of wideband noise, originated in the sample and hold. The magnitude of this localized code error is dependent upon the slew rate of the input at the time of sampling. This is shown clearly on next figures when the noise floor raise with an

Fig. 4.21 FFT plot for a 11.2 KHz input frequency using 12 bit(top) and 8 bit (bottom) ADC with a real time sampling scheme.

increase in frequency.

Each of these localized code errors can be modeled as a sharp discontinuity in the time domain that when transformed into the frequency domain results in a broad spectrum that rises the height of the noise floor above that caused by quantization noise alone.

The second feature of the FFT derived spectrum that indicates an ADC's level of dynamic performance is the harmonic content. Static and dynamic integral nonlinearities cause curvature in the ADC's transfer function. If the input frequency f_{in} is much lower than the Nyquist frequency ($f_s/2$), then the harmonic components will be in the expected locations $2f_{in}, 3f_{in}$, etc. If, on the other hand the harmonics of f_{in} are greater than $f_s/2$, then these frequencies will be aliased onto components below $f_s/2$. Take for instance in Fig. 4.22a, a 500,000 sample per second (f_s) ADC with an input sinewave of 112 KHz. The second harmonic at 224 KHz falls in the frequency spectrum, the third harmonic at 336 KHz is aliased to 164 KHz, the fourth harmonic at 448 KHz is aliased at 52 KHz, the fifth at 560 KHz is aliased to 60 KHz, and so on. An antialiasing filter used at the input of the waveform recorder shows a reduction of the harmonic level, Fig. 4.22b, giving an improvement of more than 5dB.

The input frequency was carefully selected for the FFT test, since an incorrectly chosen frequency can alias one of its harmonic components onto the fundamental and thereby understate the harmonic distortion (in the example above, an input frequency of 125 KHz would place the third harmonic at the fundamental

Fig. 4.22 FFT plot for a 112 KHz input frequency without an antialiasing filter (top), and with the filter (bottom), using the real time sampling scheme.

frequency)). The input frequency should be chosen so that the harmonics are far enough away to be easily resolvable from the fundamental.

The third feature of the FFT based spectrum that is indicative of the ADC's level of dynamic performance is the spurious content. Spurious components are spectral components that are not harmonically related to the input. For example, a strong signal near the ADC such as transient electrostatic or electromagnetic coupling of noise signals from other circuits (internal or external to the converter), may contaminate the ADC's analog ground somehow and thereby appear in the spectrum. The nearby signal will not only appear as itself, but because of nonlinearities within the ADC and S/H, can combine with the input signal to form sum and difference terms resulting in intermodulation distortion. Fig 4.23 to 4.27 shows the spectral outputs for full scale sine waves inputs from 512 KHz to 10.789 MHz. Sequential sampling shows a severe intermodulation distortion which is an indication of large integral nonlinearities. For the random sampling scheme since the samples are not correlated with the input frequency, intermodulation distortion is averaged out over the frequency spectrum, giving a much better performance in the frequency domain. Also, as might be expected, the distortion increases with increasing frequency. Harmonic and spurious components are typically better for sequential sampling below 400 KHz. Above this frequency random sampling is the winner. At 10.789 MHz the random sampling scheme show -52 dB at the spurious level, and -46 dB at the harmonic level. Since the fundamental is at -10 dB, the S/N ratio is 36 dB equivalent to 6 bits of

Fig. 4.23 FFT plots for a 512 KHz input frequency using sequential sampling (top), and random sampling (bottom).

Fig. 4.24 FFT plots for a 1.12 MHz input frequency using sequential sampling (top), and random sampling (bottom).

Fig. 4.25 FFT plots for a 2.24 MHz input frequency using sequential sampling (top), and random sampling (bottom).

Fig. 4.26 FFT plots for a 5.13 MHz input frequency using sequential sampling (top), and random sampling (bottom).

Fig. 4.27 FFT plots for a 10.789 MHz input frequency using sequential sampling (top), and random sampling (bottom).

accuracy. With an antialiasing filter this number should increase to 7 bits.

Fig. 4.28 presents, for comparison, the test results for commercially available digitizers: a 20 megasample per second, 8 bit ADC and a 100 megasample per second, 8 bit ADC with a full scale, 9.85 MHz sine wave input, sampled at 20 megasample per second. The numerous large harmonic components, both odd and even are indicative of severe harmonic distortion errors, resulting from integral nonlinearity in the transfer function of both of these ADCs.

Finally, a complete overall performance is graphically plotted in Fig. 4.29, showing bit accuracy versus frequency, for all the sampling schemes. Notice the similarity of these curves with respect to the performance in the time domain shown in Fig. 4.9. To convert S/N ratio into bit accuracy just subtract 1.8 and divide by 6, as shown in equation 4.33.

4.6 Summary

The three tests described in this chapter were sine-wave-based ADC tests which provide information about the quality of the waveform recorder. The test may be used to isolate specific failures, even at high speed and fine resolution. A final summary given in table 4.3 shows the enlightenment of different errors found in the capture of sine waves exposed by the dynamic tests. These tests were simple to run, requiring only a generator

Fig. 4.28 FFT plots for a 20 MHz, 8 bit ADC (top) and a 100 MHz, 8 bit ADC (bottom). Full scale input sine waves at 9.85 MHz were sampled at a rate of 20 MHz. The high levels of harmonic distortion indicate severe integral nonlinearities.

Fig. 4.29 Overall system performance in the frequency domain using the FFT plots for all the sampling schemes.

ERROR	SINE WAVE CURVE-FIT	HISTOGRAM	FFT
Differential nonlinearity	Yes-part of RMS error	Yes-shows up as spikes	Yes-shows up as elevated noise floor
missing codes	Yes-part of RMS error	Yes-shows up as bins with 0 counts	Yes-shows up as elevated noise floor
Integral nonlinearity	Yes-part of RMS error	Yes (could be measured with a highly linear ramp waveform)	Yes-shows up as harmonics of fundamental aliased in to baseband.
Aperture uncertainty	Yes-part of RMS error	No-averaged out	Yes-shows up as elevated noise floor
Noise	Yes-part of RMS error	No-averaged out	Yes-shows up as elevated noise floor
Gain errors	No	Yes-shows up in peak to peak spread of distribution	No
Offset errors	No	Yes-shows up in offset of distribution average	No

TABLE 4.3

Summary of the errors exposed by the dynamic tests in the waveform recorder

CHAPTER V

APPLICATIONS AND FUTURE WORK

5.1 Summary

In this thesis a general data acquisition system has been developed which allows the digital storage of either repetitive, or single shot signals. Whether measuring RMS, AC or DC voltages, or performing waveform analysis or algorithms using fast Fourier transforms (FFT), all measurements are made with sampling techniques. Obviously trade-offs exist in the selection of sampling schemes, depending on the nature of the input analog signal. Three types of sampled data measurements were performed: Real time, non-real-time-sequential, and non-real-time-random. The last sampling technique is a novel one called pseudo-random sampling. The advantage of this scheme is that the samples are equi-spaced after signal reconstruction. Therefore spectral analysis is still applicable using the FFT algorithm [28,29]. Another advantage of this scheme is that it can be used to extract information from signals not amenable to real time or sequential sampling. Also, some waveform characteristics are more accurately evaluated (i.e., undesirable phenomena are more effectively eliminated from the measurement) when the samples are taken at random intervals, as in the instance of statistical parameters evaluation.- RMS voltage, peak or peak to peak information, etc.

5.2 Application of the System

After the signal is digitized and stored, the computer or

post processor play the major role in the measurement evaluation process [30]. For display purposes, a CRT or any ordinary scope can be used. (Fig. 5.1 shows sine and triangular waveforms of 400 KHz displayed on a Tektronik 465 scope). Results can also be displayed on the VDT or in hard copy form, on the digital plotter.

The second function of the system is waveform analysis, in which comprehensive measurements of the signal characteristics, such as rise and fall times, pulse width, time difference and voltage at a given point are taken.

The third type of application is called statistical analysis. Measurements such as DC offset, average value, peak to peak, RMS, histogram records, and correlation, are made.

Finally, the system can be used for spectrum analysis, to study frequency components, modulation, distortion and digital filtering [31,32,33,34,35].

The spectra shown in Fig. 5.2 and 5.3 are some examples of filter transfer functions for low pass and band pass filtering, respectively, as determined by the system.

Those above are the result of averaging 64 times using the 3582A spectrum analyzer. Those shown below correspond to a one-time determination using the FFT algorithm on the CORVUS computer.

5.3 Conclusions

In this thesis, a waveform recorder has been designed, using cost effective components. The system acquire signals in real time with a maximum sampling rate of 500 KHz with a resolution of

Fig. 5.1 Oscilloscope displays for a 400 KHz sine wave (top), and a triangular wave (bottom).

Fig. 5.2 Low pass filter characterization using the spectrum analyzer 3582A (top), and the constructed recorder (bottom).

Fig. 5.3 Band pass filter characterization using the spectrum analyzer 3582A (top), and the constructed recorder (bottom).

12 bits. The sampling rate is increased for repetitive signals using sequential or random sampling schemes up to 25 MHz or higher, subject to the limitation of digital hardware. The system was characterized in the time and frequency domains. A comparison between schemes shows that at low frequencies, the sequential sampling gives a better resolution, but above 400 KHz random sampling is the winner. Finally an application of the system was performed, such as determination of the transfer function characteristic of a linear system.

5.4 Recommendations for future work

There are two major limitations in this hardware system. One of them is the drop out of accuracy bits as frequency increases. This limitation can be overcome by using an expensive sample and hold with much lower aperture uncertainty, or by use of a sample and hold in a feedback loop, as shown in Fig. 5.4 [11,18,36]. Two amplifiers are needed with two different hold capacitors. The advantage of this configuration is that when switch S_1 is closed, capacitor C_1 is only charged up to 5 percent of the input voltage, reducing the slew rate limitation of the system. The AC amplifier, which has a gain of 20, will bring the 5 percent value up to 20x5 percent or 100 percent. Note switch S_2 , which closes at the same time as S_1 , remains closed much longer, by about 500 times. This allows capacitor C_2 (stretcher capacitor) to charge to the full value of the signal. The DC amplifier, having a gain of 1, will simply isolate C_2 from the ADC input. Thus, C_2 will not discharge, and it will send the actual signal value to the ADC input. Note that if 100 percent of the signal is applied to

Fig. 5.4 A feedback arrangement for vertical sampling system problem.

the sampling capacitor, C_1 , via the feedback loop, C_1 will charge fully.

All the above happens before sample 3 is taken, and then finally sample 3 is taken. When switch S_1 closes, capacitor C_1 is not charged or discharged. The AC amplifier, being AC coupled, will not see a change and therefore will not alter the system. As a result, the output voltage to the ADC remain at the correct value. Capacitor C_2 must have very low droop rate since it is not allowed to lose its charge.

The second limitation in this system is due to the curvature of the ADC transfer characteristic, which shows up as harmonic distortion in the frequency spectrum. This was shown clearly in the frequency test for sequential sampling. The distortion can be decreased by using automatic calibration routines. This auto-calibration process can improve stability and accuracy, in which the microprocessor automatically calibrates the sample and hold and ADC circuit each time data is taken on a waveform, using compensation techniques [11,18,21,32].

Finally with the advent of VLSI, the system architecture of the waveform recorder is very feasible for integration on a chip using CMOS technology, especially the control and timing logic circuits.

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APPENDIX A

Analysis of the S/H Aperture Time Uncertainty

A sinusoidal input signal $V_{in}(t)$ can be described as:

$$V_{in}(t) = A \sin(2\pi ft) \quad (A.1)$$

where A is equal to one-half the full scale dynamic range of the ADC. The maximum amplitude error occurs when sampling the input signal at the zero crossings, when its slope is maximum.

The slope of the input signal is given by:

$$dV_{in}(t)/dt = 2\pi f A \cos(2\pi ft) \quad (A.2)$$

The maximum value corresponds at $t=0$, and the slope of $V_{in}(t)$ is $A2\pi f$ [volts/sec].

Thus the amplitude error in volts is:

$$\Delta V_{in}(t) = \Delta t A 2\pi f \quad (A.3)$$

Since the peak to peak amplitude of the input signal is $2A$ and is equal to the full dynamic range of the N bit ADC, the maximum allowable voltage error of $1/2$ LSB is:

$$\Delta V_{in}(t)_{\text{maximum}} = 1/2 \text{ LSB} = 2A/2^{N+1} \quad (A.4)$$

Equating the last two equations above and solving for t yield an expression for the aperture uncertainty.

$$\Delta t = 1/\pi f 2^{N+1} \text{ [seconds]} \quad (A.5)$$

APPENDIX B

Analysis of the Quantization Noise in the ADC

Figure B.1 shows an ideal ADC and ideal DAC that digitize and then reconstruct an analog slow voltage ramp signal.

The ADC and output register are both triggered together so that the DAC is updated in synchronism with the A-D conversions. The DAC output ramp is identical with the analog input ramp except for the discrete steps in its output. If the output ramp is subtracted from the input ramp as shown, the difference is the quantization noise. Therefore this ideal quantization noise is triangular in shape with a peak to peak value of Q .

The RMS value of this noise is determined from the triangular shape using the RMS formula:

$$\text{RMS} = \sqrt{\frac{1}{T} \int_0^T f^2(t) dt} \quad (\text{B.1})$$

$$\text{where } f(t) = \frac{Q}{T} \left(t - \frac{T}{2} \right) \quad 0 < t < T \quad (\text{B.2})$$

Then:

$$f^2(t) = Q^2/T^2 (t^2 - tT + T^2/4) \quad (\text{B.3})$$

applying integral on both sides, we obtain:

$$\int f^2(t) dt = Q^2/T^2 \left[\int_0^T t^2 dt - T \int_0^T t dt + T^2/4 \int_0^T dt \right] \quad (\text{B.4})$$

The integration becomes:

$$\int f^2(t) dt = Q^2/T^2 [T^3/3 - T^3/2 + T^3/4] \quad (\text{B.5})$$

Finally, substituting (B.5) in (B.1), it becomes:

$$\text{RMS}(\text{noise}) = \sqrt{Q^2[(4-6+3)/12]} = Q/\sqrt{12} \quad (\text{B.6})$$

Fig. B.1 a) Signal digitization and reconstruction b) and quantization noise. Quantization noise is shown as difference between input and output for ideal data conversion system.

APPENDIX C

Development of the Curve Fitting Equations

Dividing eq. (4.8) by N, we obtain:

$$\frac{1}{N} \sum_{k=1}^N X_k - \frac{A}{N} \sum_{k=1}^N \cos(Wt_k + P) - C = 0 \quad (C.1)$$

$$\text{Defining } \bar{X} = \frac{1}{N} \sum_{k=1}^N X_k \quad (C.2)$$

$$\text{and, } \bar{A} = \frac{1}{N} \sum_{k=1}^N \cos(Wt_k + P) \quad (C.3)$$

and substituting back in (C.1), it becomes:

$$\bar{X} - A\bar{A} = C \quad (C.4)$$

multiplying (C.4) by $\sum_{k=1}^N t_k \sin(Wt_k + P)$, we obtain:

$$\sum_{k=1}^N \bar{X} t_k \sin(Wt_k + P) - A \sum_{k=1}^N \bar{A} t_k \sin(Wt_k + P) = C \sum_{k=1}^N t_k \sin(Wt_k + P) \quad (C.5)$$

Substituting (C.5) in eq. (4.9) and factoring, it becomes:

$$\sum_{k=1}^N (X_k - \bar{X}) t_k \sin(Wt_k + P) = A \sum_{k=1}^N [\cos(Wt_k + P) - \bar{A}] t_k \sin(Wt_k + P) \quad (C.6)$$

multiplying (C.4) by $\sum_{k=1}^N \sin(Wt_k + P)$, we obtain:

$$\sum_{k=1}^N \bar{X} \sin(Wt_k + P) - A \sum_{k=1}^N \bar{A} \sin(Wt_k + P) = C \sum_{k=1}^N \sin(Wt_k + P) \quad (C.7)$$

Substituting (C.7) in eq. (4.10) and factoring, it becomes:

$$\sum_{k=1}^N (X_k - \bar{X}) \sin(Wt_k + P) = A \sum_{k=1}^N [\cos(Wt_k + P) - \bar{A}] \sin(Wt_k + P) \quad (C.8)$$

Finally, multiplying (C.4) by $\sum_{k=1}^N \cos(Wt_k + P)$, we obtain:

$$\sum_{k=1}^N \bar{x} \cos(Wt_k + P) - A \sum_{k=1}^N \bar{a} \cos(Wt_k + P) = C \sum_{k=1}^N \cos(Wt_k + P) \quad (C.9)$$

substituting (C.9) in eq. (4.7) and factoring, it becomes:

$$\sum_{k=1}^N (X_k - \bar{x}) \cos(Wt_k + P) = A \sum_{k=1}^N [\cos(Wt_k + P) - \bar{a}] \cos(Wt_k + P) \quad (C.10)$$

Then dividing (C.6) over (C.10) and (C.8) over (C.10), we obtain the final two nonlinear equations, as shown in (4.11) and (4.12) respectively.

$$\frac{\sum_{k=1}^N (X_k - \bar{x}) t_k \sin(Wt_k + P)}{\sum_{k=1}^N (X_k - \bar{x}) \cos(Wt_k + P)} = \frac{\sum_{k=1}^N [\cos(Wt_k + P) - \bar{a}] t_k \sin(Wt_k + P)}{\sum_{k=1}^N [\cos(Wt_k + P) - \bar{a}] \cos(Wt_k + P)} \quad (C.11)$$

$$\frac{\sum_{k=1}^N (X_k - \bar{x}) \sin(Wt_k + P)}{\sum_{k=1}^N (X_k - \bar{x}) \cos(Wt_k + P)} = \frac{\sum_{k=1}^N [\cos(Wt_k + P) - \bar{a}] \sin(Wt_k + P)}{\sum_{k=1}^N [\cos(Wt_k + P) - \bar{a}] \cos(Wt_k + P)} \quad (C.12)$$

APPENDIX D

Program "FITTING"

```
*      This program calculate the fitting parameters of a sine
*      wave function that best fit in a sampled data record, by
*      minimizing its function, using the quasi-Newton algorithm
      DOUBLE PRECISION X(4),F,W(62),DATA(60)
      INTEGER IFAIL,LIW,LW,N,IW(6)
      COMMON /LAB1/DATA
      N=4
      WRITE(108,50)
*      read the amplitude, frequency, phase, and offset respec-
*      tively
      READ(105,*),(X(I),I=1,N)
      PI=3.14159265358979323846
      X(3)=X(3)*(PI/180)
      X(2)=X(2)/1E6
      LIW=6
      LW=62
      IFAIL=1
      WRITE(108,80)
*      enter the number of data points
      READ(105,150)NP
      WRITE(108,90)
*      read the data record
      READ(105,*),(DATA(I),I=1,60)
      DO 10 I=1,60
```

```

DATA(I)=DATA(I)*(5.0/2048.0)

10  CONTINUE

*   call the quasi-Newton routine in the CP6 library
CALL E04CGF(N,X,F,IW,LIW,W,LW,IFAIL)
IF(IFAIL.NE.0)WRITE(108,99998)IFAIL
IF(IFAIL.EQ.1)GO TO 20

*   print the minimum function value
WRITE(108,200)F

*   print the fit parameters
WRITE(108,300),(X(I),I=1,N)

20  STOP

50  FORMAT(21H ENTER THE PARAMETERS)
80  FORMAT(32H ENTER THE NUMBER OF DATA POINTS)
90  FORMAT(22H ENTER THE DATA POINTS)
200  FORMAT(27H FUNCTION VALUE ON EXIT IS,D15.5)
300  FORMAT(13H AT THE POINT,4D15.5)
150  FORMAT(13)
99998 FORMAT(16H ERROR EXIT TYPE,13)

END.

*   This subroutine calculate the actual RMS error which is
*   used for the main program to find the minimum function
*   value

SUBROUTINE FUNCT1(N,XC,FC)
INTEGER N
DOUBLE PRECISION FC,XC(N),DATA(60),A,W,P,C,ARG,PI,E
COMMON /RAB1/DATA
PI=3.14159265358979323846
A=XC(1)

```

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```

W=XC(2)
P=XC(3)
C=XC(4)
FC=0
DO 1000 I=1,60
  T=(40E-3)*I
  ARG=2*PI*W*T+P
  * rms error calculation
  E=(DATA(I)-A*DCOS(ARG)-C)**2
  FC=FC+E
1000 CONTINUE
  WRITE(108,99)A,W,P,C,FC
99  FORMAT(1X,5D15.5)
  RETURN
END

```

APPENDIX E

Analysis of Probability Density Function for a Sine Wave

By definition, the probability density function, (PDF) describes the probability that the signal will be found within a given range, v and $v+dv$, and is normalized by dv to give a density function.

For a sine wave,

$$v(t) = Ax \sin(Wt) \quad (E.1)$$

taking the derivative

$$dv(t) = AWx \cos(Wt) dt \quad (E.2)$$

where

$$dt = \frac{dv}{AWx \cos(Wt)} \quad (E.3)$$

$$\text{Since } A^2 \cos^2(Wt) + A^2 \sin^2(Wt) = A^2 \quad (E.4)$$

$$A^2 \cos^2(Wt) = A^2 - A^2 \sin^2(Wt) \quad (E.5)$$

$$\text{or } A^2 \cos^2(Wt) = A^2 - v^2 \quad (E.6)$$

$$\text{and } \cos(Wt) = \pm \sqrt{A^2 - v^2} / A \quad (E.7)$$

substituting (E.7) in (E.3)

$$dt = \frac{\pm dv}{W \sqrt{A^2 - v^2}} \quad (E.8)$$

Over half a cycle,

$$\frac{dt}{T/2} = \frac{dv}{WT/2 \sqrt{A^2 - v^2}} \quad (E.9)$$

finally normalizing by dv , it becomes the PDF of a sine wave,

$$P(v) = \frac{1}{WT/2 \sqrt{A^2 - v^2}} \quad (E.10)$$

substituting $\omega = 2\pi f = 2\pi/T$

$$P(v) = \frac{1}{\pi \sqrt{A^2 - v^2}} \quad (E.11)$$

APPENDIX F

Program "HISTOGRAM"

{THIS PROGRAM READ A FILE OF 2048 POINTS FROM A RECORD SENT BY THE WAVEFORM RECORDER CONTROLLER. THIS IS CONVERTED INTO A TEXT FILE FROM WHICH IS PROCESSED. IT CONSIST IN INCREMENT THE CORRESPONDENT DIGITAL CODE WORD EVERY TIME IT APPEARS IN THE DATA RECORD. A STATISTICAL NUMBER OF SAMPLES IS REQUIRED TO HAVE SOME CONFIDENCE IN THE OCCURRENCES OF ALL DIFFERENT CODES (TIPICALLY 100,000). THEN IT REQUIRES TO READ ABOUT 50 FILES. THE FREQUENCY OF CODE OCCURRENCE IN THE RECORD IS THEN PLOTTED AS A FUNCTION OF CODE.]

PROGRAM HISTOGRAM;

VAR

IN_NAME:	STRING[30];
IN_FILE:	INTERACTIVE;
OUT_FILE:	INTERACTIVE;
N,K,I,P:	INTEGER;
ANS:	CHAR;

BEGIN

FOR I:=0 TO 4095 DO

BEGIN

HISTO[I]:=0

END;

WRITELN('DO YOU WANT TO USE AN EXISTING HISTO DATA FILE?');

READLN(ANS);

IF (ANS = 'Y')

```
THEN
  BEGIN
    RESET(IN_FILE,'HISTO.TEXT');
    FOR I:=0 TO 4095 DO
      BEGIN
        READLN(IN_FILE,HISTO[I]);
      END;
    CLOSE(IN_FILE,LOCK);
  END;
  {READ FILE RECORD, AS SENT FROM THE RECORDER}
  WRITE('DATA FILE NAME: ');
  READLN (IN_NAME);
  REWRITE(OUT_FILE,'HISTO.TEXT');
  N:=0;
  RESET(IN_FILE,IN_NAME);
  GET (IN_FILE);
  WHILE NOT EOF (IN_FILE) DO
    BEGIN
      FOR I:=1 TO 16 DO
        BEGIN
          FOR K:= 1 TO 5 DO
            BEGIN
              IF NOT EOF (IN_FILE) THEN
                BEGIN
                  DATA[K]:=ORD(IN_FILE^)-ORD('0');
                  IF DATA[K]>9 THEN DATA[K]:=DATA[K]-7;
                  GET(IN_FILE)
```

```
END  
END;  
N:=N+1;  
DECIMALDATA[N]:=DATA[2]*16*16+DATA[3]*16+DATA[4];  
P:=-DECIMALDATA[N];  
IF (P<0) OR (P>4100)  
THEN  
ELSE  
{INCREMENT THE CORRESPONDENT DIGITAL CODE WORD  
OCCURRENCE}  
HISTO[P]:=HISTO[P]+1;  
END;  
IF NOT EOF (IN_FILE) THEN GET (IN_FILE)  
END;  
BEGIN  
FOR I:=0 TO 4095 DO  
    WRITELN(OUT_FILE,HISTO[I]);  
END;  
CLOSE(OUT_FILE,LOCK);  
END.
```

APPENDIX G

Program "PDF"

{THIS PROGRAM CALCULATES THE PROBABILITY DENSITY FUNCTION FOR A PARTICULAR CODE BIN, USING EQ. (4.29). THEN FROM AN HISTOGRAM RECORD, THE CORRESPONDENT DIFFERENTIAL NONLINEARITY ERROR IS COMPUTED USING EQ. (4.24) AND STORED IT IN AN OUTPUT FILE CALLED P.TEXT}

```

program pdf;
  var
    in_file:          interactive;
    out_file:         interactive;
    i:                integer;
    u,v,NS:           real;
    histo:            array [0..4095] of integer;
    m,sum:            real;
    p,dn:             array [0..4095] of real;
  begin
    WRITE('ENTER THE NUMBER OF SAMPLES: ');
    READLN(NS);
    reset(in_file,'histo.text');
    rewrite(out_file,'p');
    for i:=0 to 4095 do
      begin
        {CALCULATION OF THE IDEAL PROBABILITY DENSITY FUNCTION
        FOR A PARTICULAR CODE BIN}

```

```

u:=abs((1-2048)/4096);
v:=abs((1-2049)/4096);
u:=arctan(u/sqrt(-u*u+1.0));
v:=arctan(v/sqrt(-v*v+1.0));
p[i]:=(u-v)/3.14159;
{GET ACTUAL OUTPUT CODE FROM THE HISTOGRAM RECORD}
readln(in_file,histo[i]);
{CALCULATION OF ACTUAL PDF}
m:=histo[i]/NS;
{CALCULATION OF THE DIFFERENTIAL NONLINEARITY FOR A
PARTICULAR CODE BIN}
dn[i]:=m/abs(p[i])-1;
{AND STORE THIS VALUE IN THE OUTPUT FILE "P.TEXT"}
writeln(out_file,dn[i]);
end;
close(out_file,lock);
begin
{CALCULATION OF THE AVERAGE DIFFERENTIAL NONLINEARITY}
sum:=0;
for i:=1024 TO 3071 DO
    sum:=dn[i]+sum;
end;
begin
    sum:=sum/2048;
    writeln(sum);
end;
end.

```

APPENDIX H

Analysis of the S/N for an ADC with N bits

The signal to noise ratio (S/N), which is a power ratio expressed in decibels, it can be found from the ratio of RMS signal to RMS noise as follow.

If the minimum quantization step of the ADC with N bits is Q, then the maximum peak-to-peak signal is $2^N Q$ volts.

The the RMS signal is given by:

$$\text{RMS}(\text{signal}) = 2^N Q / 2\sqrt{2} \quad (\text{H.1})$$

$$\text{since the RMS}(\text{noise}) = Q/\sqrt{12} \quad (\text{H.2})$$

therefore,

$$\text{S/N}(\text{ratio}) = \frac{2^N Q / 2\sqrt{2}}{Q/\sqrt{12}} = 2^N \sqrt{6}/2 \quad (\text{H.3})$$

in decibels,

$$\text{S/N}(\text{ratio}) = 20 \log(2^N \sqrt{6}/2) \quad (\text{H.4})$$

$$\text{S/N}(\text{ratio}) = N \times 20 \log 2 + 20 \log(\sqrt{6}/2) \quad (\text{H.5})$$

$$\text{S/N}(\text{ratio}) = 6.02N + 1.76 \text{ [decibels]} \quad (\text{H.6})$$

$$\text{S/N}(\text{ratio}) \approx 6N + 1.8 \text{ [dB]} \quad (\text{H.7})$$

APPENDIX I

Schematics for the Waveform Recorder

Sheet 1 of 1

1000

1000

1000

1000

1000

APPENDIX 3

Software Support for the 6800 Controller

```

1      * THIS IS THE SOFTWARE FOR THE LINK
2      * BETWEEN THE 6800 MICROCOMPUTER AND
3      * THE CORVUS COMPUTER
4      OPT      PAG
5      NAM      E DATA TRANSMISSION TO THE CORVUS
6      8009     SERBUF EQU $8009
7      8008     SERCSR EQU $8008
8      8017     P3ACRB EQU $8017
9      8015     P3ADRB EQU $8015
10     0200     TEMP EQU $0200
11     0202     MEMPNT EQU $0202
12     0204     COUNT EQU $0204
13     0206     TEMPO EQU $0206
14     0208     BUFFER EQU $0208
15     1000     ORG $1000
16     1000 7F 80 17 CLR P3ACRB SET PORT 3B AS OUTPUT
17     1003 86 FF LDA A #$FF
18     1005 B7 80 15 STA A P3ADRB
19     1008 86 06 LDA A #$06
20     100A B7 80 17 STA A P3ACRB
21     100D 86 03 LDA A #$03 DO MASTER RESET
22     100F B7 80 08 STA A SERCSR
23     1011 86 11 LDA A #$11 8 BITS, NO PARITY
24     1014 B7 80 08 STA A SERCSR 2 STOP BITS
25     1017 86 00 LDA A #$00 SEND A CR
26     1019 BD 12 D6 JSR OUTPUT AND
27     101C 86 0A LDA A #$0A LF
28     101E BD 12 D6 JSR OUTPUT
29     1021 CE 10 E4 LDX $MESS-1 SEND INITIALIZATION
30     1024 FF 02 02 STX MEMPNT MESSAGE
31     1027 FE 02 02 FRTMOR LDX MEMPNT
32     102A 08 INX
33     102B FF 02 02 STX MEMPNT
34     102E A6 00 LDA A 0,X
35     1030 27 05 BEQ ADQUI
36     1032 BD 12 D6 JSR OUTPUT
37     1035 20 F0 BRA FRTMOR
38     1037 B6 80 08 ADQUI LDA A SERCSR IS DATA READY?
39     103A B4 01 AND A #$01
40     103C 27 F9 BEQ ADQUI
41     103E B6 80 09 LDA A SERBUF YES, READ DATA IDENT.
42     1041 B1 31 CMP A #$31 IF 1, THEN DO
43     1043 27 0E BEQ REAL REAL TIME SAMPLING
44     1045 B1 32 CMP A #$32 IF 2, THEN DO
45     1047 27 02 BEQ NOREAL REPETITIVE SAMPLING
46     1049 20 EC BRA ADQUI
47     104B 86 00 NOREAL LDA A #$00 GET SAMPLING RATE
48     104D B7 02 0B STA A BUFFER IDENTIFICATION
49     1050 7E 10 BE JMP CONT GO TO REPET. ROUTINE
50     1053 B6 80 REAL LDA A #$80 REAL TIME ROUTINE
51     1055 B7 02 0B STA A BUFFER
52     1058 CE 11 9D LDX $MESS3-1 SEND MESSAGE FOR DIFFERENT
53     105B FF 02 02 STX MEMPNT SAMPLING RATES
54     105E FE 02 02 SAM LDX MEMPNT
55     1061 08 INX
56     1062 FF 02 02 STX MEMPNT
57     1065 A6 00 LDA A 0,X

```

58	1067	27	05		BEQ	SAMM	
59	1069	1D	12	D6	JSR	OUTPUT	
60	106C	20	F0		BRA	SAM	
61	106E	B6	80	08	LDA A	SERCSR	IS SAMPLING RATE SELECTED?
62	1071	84	01		AND A	#01	
63	1073	27	F9		BEQ	SAMM	
64	1075	B6	80	09	LDA A	SERBUF	YES, GET DATA
65	1078	81	33		CMP A	#33	IDENTIFY SAMPLING
66	107A	27	2E		BEQ	QST	SELECTION
67	107C	81	34		CMP A	#34	
68	107E	27	2A		BEQ	QST	
69	1080	81	35		CMP A	#35	
70	1082	27	26		BEQ	QST	
71	1084	81	36		CMP A	#36	
72	1086	27	22		BEQ	QST	
73	1088	81	37		CMP A	#37	
74	108A	27	1E		BEQ	QST	
75	108C	81	38		CMP A	#38	
76	108E	27	1A		BEQ	QST	
77	1090	81	39		CMP A	#39	
78	1092	27	16		BEQ	QST	
79	1094	81	41		CMP A	#41	
80	1096	27	1C		BEQ	LETT	
81	1098	81	42		CMP A	#42	
82	109A	27	18		BEQ	LETT	
83	109C	81	43		CMP A	#43	
84	109E	27	14		BEQ	LETT	
85	10A0	81	44		CMP A	#44	
86	10A2	27	10		BEQ	LETT	
87	10A4	81	45		CMP A	#45	
88	10A6	27	0C		BEQ	LETT	
89	10A8	20	C4		BRA	SAMM	
90	10AA	B4	0F		AND A	#0F	SET PROG. COUNTER
91	10AC	B7	02	06	STA A	TEMPO	FOR CORRECT SAMPL. FREQ.
92	10AF	B7	80	15	STA A	F3ADRB	
93	10B2	20	0A		BRA	CONT	
94	10B4	84	0F		AND A	#0F	
95	10B6	8B	09		ADD A	#09	
96	10B8	B7	02	06	STA A	TEMPO	
97	10BB	B7	80	15	STA A	F3ADRB	
98	10BE	CE	11	48	LIX	#MESS5-1	SEND MESSAGE FOR STORAGE
99	10C1	FF	02	02	STX	MEMFNT	IN THE CORVUS COMPUTER
100	10C4	FE	02	02	LIX	MEMFNT	
101	10C7	08			INX		
102	10CB	FF	02	02	STX	MEMFNT	
103	10CB	A6	00		LDA A	0,X	
104	10CD	27	05		BEQ	CONT1	
105	10CF	BD	12	D6	JSR	OUTPUT	
106	10D2	20	F0		BRA	PTMR	
107	10D4	B6	80	08	LDA A	SERCSR	IS DATA READY?
108	10D7	84	01		AND A	#01	
109	10D9	27	F9		BEQ	CONT1	
110	10DB	B6	80	09	LDA A	SERBUF	YES, GET DATA AND
111	10DE	81	33		CMP A	#33	COMPARE WITH REF. VAL.

DATA TRANSMISSION TO THE CORVUS

112	10E0 26 DC	BNE	CONT	
113	10E2 7E 12 1E	JMP	ALLIUN	YES, THEN GO TO CORRESP.
114	10E5 52	FCC	/READY/	SUBROUTINE
	10E6 45 41			
	10E8 44 59			
115	10EA 0D	FCB	\$0D,\$0A	
	10EB 0A			
116	10EC 57	FCC	/WELCOME TO THE STORAGE OSCILLOSCOPE/	
	10ED 45 4C			
	10EF 43 4F			
	10F1 4D 45			
	10F3 20 54			
	10F5 4F 20			
	10F7 54 48			
	10F9 45 20			
	10FB 53 54			
	10FD 4F 52			
	10FF 41 47			
	1101 45 20			
	1103 4F 53			
	1105 43 49			
	1107 4C 4C			
	1109 4F 53			
	110B 43 4F			
	110D 50 45			
117	110F 0D	FCB	\$0D,\$0A	
	1110 0A			
118	1111 53	FCC	/SELECT SAMPLING MODE:/	
	1112 45 4C			
	1114 45 43			
	1116 54 20			
	1118 53 41			
	111A 4D 50			
	111C 4C 49			
	111E 4E 47			
	1120 20 4D			
	1122 4F 44			
	1124 45 3A			
119	1126 0D	FCB	\$0D,\$0A	
	1127 0A			
120	1128 31	FCC	/1. REAL TIME/	
	1129 2E 20			
	112B 52 45			
	112D 41 4C			
	112F 20 54			
	1131 49 4D			
	1133 45			
121	1134 0D	FCB	\$0D,\$0A	
	1135 0A			
122	1136 32	FCC	/2. NON REAL TIME/	
	1137 2E 20			
	1139 4E 4F			
	113B 4E 20			
	113D 51 45			

DATA TRANSMISSION TO THE CORVUS

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```

113F 41 4C
1141 20 54
1143 49 4D
1145 45
123 1146 0D          FCB      $0D,$0A,$00
    1147 0A 00
124 1149 50          MESS5    FCC      /PRESS FUNCTION KEY "FILE=F1"/
    114A 52 45
    114C 53 53
    114E 20 46
    1150 55 4E
    1152 43 54
    1154 49 4F
    1156 4E 20
    1158 4B 45
    115A 59 20
    115C 22 46
    115E 49 4C
    1160 45 3D
    1162 46 31
    1164 22
125 1165 41          FCC      /AND ENTER FILENAME FOLLOWED BY RETUR
ND A PERIOD/
    1166 4E 44
    1168 20 45
    116A 4E 54
    116C 45 52
    116E 20 46
    1170 49 4C
    1172 45 4E
    1174 41 4D
    1176 45 20
    1178 46 4F
    117A 4C 4C
    117C 4F 57
    117E 45 44
    1180 20 42
    1182 59 20
    1184 52 45
    1186 54 55
    1188 52 4E
    118A 20 4B
    118C 45 59
    118E 20 41
    1190 4E 44
    1192 20 41
    1194 20 50
    1196 45 52
    1198 49 4F
    119A 44
126 119B 0D          FCB      $0D,$0A,$00
    119C 0A 00
127 119E 53          MESS3    FCC      /SELECT SAMPLING RATE (KHZ):/
    119F 45 4C
    11A1 45 45

```

DATA TRANSMISSION TO THE CORVUS

	11A3 54 20		
	11A5 53 41		
	11A7 4D 50		
	11A9 4C 49		
	11AB 4E 47		
	11AD 20 52		
	11AF 41 54		
	11B1 45 20		
	11B3 28 4B		
	11B5 48 5A		
	11B7 29 3A		
128	11B9 0D	FCB	\$0D,\$0A
	11BA 0A		
129	11BB 33	FCC	/3. 500/
	11BC 2E 20		
	11BE 35 30		
	11C0 30		
130	11C1 0D	FCB	\$0D,\$0A
	11C2 0A		
131	11C3 34	FCC	/4. 100/
	11C4 2E 20		
	11C6 31 30		
	11C8 30		
132	11C9 0D	FCB	\$0D,\$0A
	11CA 0A		
133	11CB 35	FCC	/5. 50/
	11CC 2E 20		
	11CE 20 35		
	11D0 30		
134	11D1 0D	FCB	\$0D,\$0A
	11D2 0A		
135	11D3 36	FCC	/6. 20/
	11D4 2E 20		
	11D6 20 32		
	11D8 30		
136	11D9 0D	FCB	\$0D,\$0A
	11DA 0A		
137	11DB 37	FCC	/7. 10/
	11DC 2E 20		
	11DE 20 31		
	11E0 30		
138	11E1 0D	FCB	\$0D,\$0A
	11E2 0A		
139	11E3 38	FCC	/8. 5/
	11E4 2E 20		
	11E6 20 20		
	11E8 35		
140	11E9 0D	FCB	\$0D,\$0A
	11EA 0A		
141	11EB 39	FCC	/9. 2/
	11EC 2E 20		
	11EE 20 20		
	11F0 32		
142	11F1 0D	FCB	\$0D,\$0A

DATA TRANSMISSION TO THE CORVUS

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143	11F2 0A				
	11F3 41	FCB	/A.	1/	
	11F4 2E 20				
	11F6 20 20				
	11F8 31				
144	11F9 0D	FCB	\$0D,\$0A		
	11FA 0A				
145	11FB 42	FCC	/B.	.5/	
	11FC 2E 20				
	11FE 20 2E				
	1200 35				
146	1201 0A	FCC	\$0D,\$0A		
	1202 0A				
147	1203 43	FCC	/C.	.2	
	1204 2E 20				
	1206 20 2E				
	1208 32				
148	1209 0D	FCB	\$0D,\$0A		
	120A 0A				
149	120B 44	FCC	/D.	.1/	
	120C 2E 20				
	120E 2E 2E				
	1210 31				
150	1211 0D	FCB	\$0D,\$0A		
	1212 0A				
151	1213 45	FCC	/E.	.05/	
	1214 2E 20				
	1216 2E 30				
	1218 35				
152	1219 0D	FCB	\$0D,\$0A,\$00		
	121A 0A 00				
153	121C 0D	MESS4	FCB	\$0D,\$0A	
	121D 0A				
154	121E 8D 20 00	ALLDUN	JSR	\$2000	
155	1221 CE 5F FE		LDX	\$\$5FFE	
156	1224 FF 02 02		STX	MEMFNT	
157	1227 86 10	NEXT	LDA A	\$\$10	
158	1229 B7 02 04		STA A	COUNTR	
159	122C FE 02 02	SEND	LDX	MEMFNT	
160	122F 8C 6F FE		CPX	\$\$6FFE	
161	1232 27 56		BEQ	FIN	
162	1234 08		INX		
163	1235 08		INX		
164	1236 FF 02 02		STX	MEMFNT	
165	1239 A6 01		LDA A	1,X	
166	123B B7 02 00		STA A	TEMP	
167	123E 84 F0		AND A	\$\$F0	
168	1240 44		LSR A		
169	1241 44		LSR A		
170	1242 44		LSR A		
171	1243 44		LSR A		
172	1244 8D 12 E1		JSR	ASCII	
173	1247 FF 12 D6		JSR	OUTPUT	
174	1248 8D 12 E1		LDA A	TEMP	

NOW, SEND THE 2048 SAMPLED
POINTS THROUGH AN RS-232C
LINE TO THE CORVUS COMPUTER
(16 DATA POINTS PER LINE)

DATA TRANSMISSION TO THE CORVUS

175	124D 84 0F		AND A	##0F	
176	124F BD 12 E1		JSR	ASCII	
177	1252 BD 12 D6		JSR	OUTPUT	
178	1255 A6 00		LDA A	0,X	
179	1257 B7 02 00		STA A	TEMP	
180	125A 84 F0		AND A	##F0	
181	125C 44		LSR A		
182	125D 44		LSR A		
183	125E 44		LSR A		
184	125F 44		LSR A		
185	1260 BD 12 E1		JSR	ASCII	
186	1263 BD 12 D6		JSR	OUTPUT	
187	1266 B6 02 00		LDA A	TEMP	
188	1269 84 0F		AND A	##0F	
189	126B BD 12 E1		JSR	ASCII	
190	126E BD 12 D6		JSR	OUTPUT	
191	1271 86 2E		LDA A	##2E	
192	1273 BD 12 D6		JSR	OUTPUT	
193	1276 7A 02 04		DEC	COUNTR	
194	1279 27 02		BEQ	ROUND	
195	127B 20 AF		BRA	SEND	
196	127D 86 0D	ROUND	LDA A	##0D	
197	127F BD 12 D6		JSR	OUTPUT	
198	1282 86 0A		LDA A	##0A	
199	1284 BD 12 D6		JSR	OUTPUT	
200	1287 7E 12 27		JMP	NEXT	
201	128A 86 30	FIN	LDA A	##30	SEND SAMPLING IDENT.
202	128C BD 12 D6		JSR	OUTPUT	TO THE CORVUS
203	128F 86 30		LDA A	##30	
204	1291 BD 12 D6		JSR	OUTPUT	
205	1294 86 30		LDA A	##30	
206	1296 BD 12 D6		JSR	OUTPUT	
207	1299 B6 02 06		LDA A	TEMP0	
208	129C BD 12 E1		JSR	ASCII	
209	129F BD 12 D6		JSR	OUTPUT	
210	12A2 CE 12 BE		LDX	##MESS1-1	SEND MESSAGE OF
211	12A5 FF 02 02		STX	MEMPNT	COMPLETE OPERATION
212	12AB FE 02 02	PRINT	LDX	MEMPNT	
213	12AB 08		INX		
214	12AC FF 02 02		STX	MEMPNT	
215	12AF A6 00		LDA A	0,X	
216	12B1 27 22		BEQ	COMPL	
217	12B3 F6 80 08	OUT	LDA B	SERCSR	
218	12B6 C4 02		AND B	##02	
219	12B8 27 F9		BEQ	OUT	
220	12BA B7 80 09		STA A	SERBUF	
221	12BD 20 E9		BRA	PRINT	
222	12BF 4F	MESS1	FCC	/OPERATION COMPLETED/	
	12C0 50 45				
	12C2 52 41				
	12C4 54 49				
	12C6 4F 4E				
	12C8 20 43				
	12CA 4F 4D				

DATA TRANSMISSION TO THE CORVUS

12CC	50	4C			
12CE	45	54			
12D0	45	44			
223	12D2	0D		FCB	10D,10A,100
	12D3	0A	00		
224	12D5	3F	COMPL	SWI	
225	12D6	F6	80	00	OUTPUT
226	12D9	C4	02		
227	12DB	27	F9		
228	12DD	B7	80	09	
229	12E0	39			
230	12E1	81	09	ASCII	
231	12E3	23	02		
232	12E5	8B	07		
233	12E7	8B	30	ASCZ	
234	12E9	39			
235	12EA	B6	80	08	ECHO
236	12ED	84	01		
237	12EF	27	F9		
238	12F1	B6	80	09	
239	12F4	F6	80	08	DO1
240	12F7	C4	02		
241	12F9	27	F9		
242	12FB	B7	80	09	
243	12FE	39			
244					

0 ERROR(S) DETECTED

DATA TRANSMISSION TO THE CORVUS

SYMBOL TABLE:

IQUI	1037	ALLDUN	121E	ASCII	12E1	ASCZ	12E7	BUFFER	0208
OMPL	12D5	CONT	10BE	CONT1	10D4	COUNTR	0204	DO1	12F4
CHO	12EA	FIN	128A	LETT	10B4	MEMFNT	0202	MESS	10E5
ESS1	12BF	MESS3	119E	MESS4	121C	MESS5	1149	NEXT	1227
OREAL	104B	OUT	12E3	OUTPUT	12D6	F3ACRB	8017	F3ADRB	8015
RINT	12A8	PRTHOR	1027	PTMR	10C4	QST	10AA	REAL	1053
OUND	127D	SAM	105E	SAMM	106E	SEND	122C	SERBUF	8009
ERCSK	8008	TEMP	0200	TEMFO	0206				

	OFF	FAG	
	NAM	REAL TIME SAMPLING (MAX 500 KHz)	
	* REAL TIME SAMPLING (MAX 500 KHz)		
801A	F1ACRA EQU	\$801A	
801B	F1ADRA EQU	\$801B	
801C	F1ACRB EQU	\$801C	
801D	F1ADRB EQU	\$801D	
801E	F2ACRA EQU	\$801E	
801F	F2ADRA EQU	\$801F	
801G	F2ACRB EQU	\$801G	
801H	F2ADRB EQU	\$801H	
801I	F3ACRA EQU	\$801I	
801J	F3ADRA EQU	\$801J	
801K	F3ACRB EQU	\$801K	
801L	F3ADRB EQU	\$801L	
0200	COUNTR EQU	\$0200	
0202	HIDEST EQU	\$0202	
2000	ORG	\$2000	
2000 7F 80 1F	CLR	F2ACRB	SET PORT 2B AS OUTPUT
2003 86 FF	LDA A	#\$FF	
2005 B7 80 1D	STA A	F2ADRB	
2008 86 04	LDA A	#\$04	
200A B7 80 1F	STA A	F2ACRB	
200D 7F 80 1A	CLR	F1ACRA	SET PORT 1A AS INPUT
2010 7F 80 1B	CLR	F1ADRA	
2013 86 04	LDA A	#\$04	
2015 B7 80 1A	STA A	F1ACRA	
2018 7F 80 16	CLR	F3ACRA	SET PORT 3A AS INPUT
201B 7F 80 14	CLR	F3ADRA	
201E 86 06	LDA A	#\$06	
2020 B7 80 16	STA A	F3ACRA	
2023 86 04	LDA A	#\$04	SET CA2
2025 B7 80 1E	STA A	F2ACRA	
2028 86 EF	REPEAT LDA A	#\$EF	ENABLE BMV A/D'S OUTPUT LATCHES
202A B7 80 1D	STA A	F2ADRB	
202D CE 08 00	LDX	#\$0800	INITIALIZE SOFTWARE COUNTER
2030 FF 02 00	STX	COUNTR	
2033 CE 60 00	LDX	#\$6000	INITIALIZE DESTINATION REGISTER
2036 FF 02 02	STX	HIDEST	
2039 86 30	LDA A	#\$30	SET CLOCK FOR ADDRESS COUNTER TO LOW
203B B7 80 1E	STA A	F2ACRA	
203E 86 30	LDA A	#\$30	PRODUCE ARMING PULSE TO START SAMPLING
2040 B7 80 17	STA A	F3ACRB	
2043 86 38	LDA A	#\$38	
2045 B7 80 17	STA A	F3ACRB	
2048 86 30	LDA A	#\$30	
204A B7 80 17	STA A	F3ACRB	
204D 86 80 1A	WAIT LDA A	F1ACRA	CHECK FOR END OF SAMPLING
2050 2A FF	BPL	WAIT	
2052 86 0F	LDA A	#\$0F	YES, DISABLE A/D'S AND D/A'S LATCHES
2054 B7 80 1D	STA A	F2ADRB	
2057 FE 02 00	LDX	COUNTR	
205A FF 02 00	AGAIN STX	COUNTR	
205D 86 80 18	LDA A	F1ADRA	GET DATA (LO BYTE)
2060 F6 80 14	LDA B	F3ADRA	GET DATA (HI BYTE)
2063 0A 0F	AND B	#\$0F	
2065 10 02 02	LDA	HIDEST	STORE DATA

REAL TIME SAMPLING (MAX 500 KHZ)

2068 A7 00	STA A 0.X	IN DESTINATION REGISTERS
206A E7 01	STA B 1.X	
206C 08	INX	
206D 08	INX	
206E FF 02 02	CTI HIDEST	INCREMENT DESTINATION
2071 B6 80 1E	LDA A F2ACRA	REGISTER
2074 84 38	ORA A \$38	
2076 B7 80 1E	STA A F2ACRA	
2078 B6 80 1E	LDA A F2ACRA	INCREMENT THE ADDRESS
207C 84 F7	AND A \$F7	COUNTER
207E B7 80 1E	STA A F2ACRA	
2081 FE 02 00	LDX COUNTER	
2084 09	DEX	DECREMENT THE SOFTWARE CTR
2085 26 D3	BNE AGAIN	MORE SAMPLES?
2087 B6 87	LDA A \$87	NO, ENABLE THE D/A'S COUNTER
2089 B7 80 1D	STA A F2ADRB	AND D/A'S INPUT LATCH
208C 37	RTS	
	END	

NO ERRORS DETECTED

REAL TIME SAMPLING (MAX 500 KHZ)

SYMBOL TABLE:

AGAIN 205A	COUNTR 0200	HIDEST 0202	F1ACRA 801A	F1ACRB 801B
F1ADRA 8018	F1ADRB 8019	F2ACRA 801E	F2ACRB 801F	F2ADRA 801C
F2ADRB 801D	F3ACRA 8016	F3ACRB 8017	F3ADRA 8014	F3ADRB 8015
REPEAT 2028	WAIT 204D			

	MEM	REG	SEQUENTIAL SAMPLING (MAX 25 MHZ)	
3			* SEQUENTIAL SAMPLING (MAX 25 MHZ)	161
4	801A	F1ACRA	EQU	\$801A
5	8018	F1ADRA	EQU	\$8018
6	801B	F1ACRB	EQU	\$801B
7	8019	F1ADRB	EQU	\$8019
8	801E	F2ACRA	EQU	\$801E
9	801C	F2ADRA	EQU	\$801C
10	801F	F2ACRB	EQU	\$801F
11	801D	F2ADRB	EQU	\$801D
12	8016	F3ACRA	EQU	\$8016
13	8014	F3ADRA	EQU	\$8014
14	8017	F3ACRB	EQU	\$8017
15	8015	F3ADRB	EQU	\$8015
16	0200	COUNTR	EQU	\$0200
17	0202	HIDEST	EQU	\$0202
18	0204	LODEST	EQU	\$0204
19	0206	HISOUR	EQU	\$0206
20	0208	LOSOUR	EQU	\$0208
21	020A	MILCNT	EQU	\$020A
22	020C	AVR	EQU	\$020C
23	020E	AVRG	EQU	\$020E
24	0210	TIME	EQU	\$0210
25	0212	FLAG	EQU	\$0212
26	2000		ORG	\$2000
27	2000 CE 40 00	LIX		\$\$\$4000
28	2003 4F	CLR A		
29	2004 A7 00	BACK STA A	0,X	
30	2006 08	INX		
31	2007 8C 70 00	CFX	\$\$\$7000	
32	200A 26 F8	BNE	BACK	
33	200C 86 01	LDA A	\$\$\$01	
34	200E 87 02 06	STA A	HISOUR	
35	2011 7F 80 1A	CLR	F1ACRA	SET PORT 1A AS INPUT
36	2014 7F 80 18	CLR	F1ADRA	
37	2017 86 06	LDA A	\$\$\$06	
38	2019 87 80 1A	STA A	F1ACRA	
39	201C 7F 80 1B	CLR	F1ACRB	SET PORT 1B AS OUTPUT
40	201F 86 FF	LDA A	\$\$\$FF	
41	2021 87 80 19	STA A	F1ADRB	
42	2024 86 06	LDA A	\$\$\$06	
43	2026 87 80 1B	STA A	F1ACRB	
44	2029 7F 80 1F	CLR	F2ACRB	SET PORT 2B AS OUTPUT
45	202C 86 FF	LDA A	\$\$\$FF	
46	202E 87 80 1D	STA A	F2ADRB	
47	2031 86 04	LDA A	\$\$\$04	
48	2033 87 80 1F	STA A	F2ACRB	
49	2036 7F 80 16	CLR	F3ACRA	SET PORT 3A AS INPUT
50	2039 7F 80 14	CLR	F3ADRA	
51	203C 86 06	LDA A	\$\$\$06	
52	203E 87 80 16	STA A	F3ACRA	
53	2041 86 10	START LDA A	\$\$\$10	STORE NUMBER OF AVERAGES (MAXIMUM 16)
54	2043 87 02 0C	STA A	AVR	
55	2046 87 02 0E	STA A	AVRG	
56	2049 86 80 1B	LDA A	F1ACRB	SET LOAD LINE HIGH
57	204C 84 F7	AND A	\$\$\$F7	

58	204E	B7 80 1B	STA A	F1ACRB	
59	2051	B6 80 1A	LDA A	F1ACRA	DISABLE ACKNOWLEDGE CONTR
60	2054	8A 38	ORA A	#138	SIGNAL MICROPROCESSOR
61	2056	B7 80 1A	STA A	F1ACRA	
62	2059	CE 08 00	LDX	#10800	INITIALIZE SOFTWARE
63	205C	FF 02 00	STX	COUNTR	COUNTER
64	205F	CE 40 00	LDX	#14000	INITIALIZE DESTINATION
65	2062	FF 02 04	STX	LODEST	REGISTER (LO BYTE)
66	2065	CE 50 00	LDX	#15000	AND
67	2068	FF 02 02	STX	HIDEST	(HI BYTE)
68	206B	86 FF	LDA A	#FF	ENABLE AND'S OUTPUT
69	206D	B7 80 1B	STA A	F2ADRB	LATCHES
70	2070	FE 02 00	LDX	COUNTR	GET DELAY NUMBER
71	2073	FF 02 00	STX	COUNTR	
72	2076	F6 02 00	LDA B	COUNTR	
73	2079	B6 02 01	LDA A	COUNTR+1	
74	207C	CA FB	ORA B	#FB	
75	207E	B7 80 19	STA A	F1ADRB	STORE DELAY NUMBER
76	2081	F7 80 1D	STA B	F2ADRB	
77	2084	B6 80 1B	LDA A	F1ACRB	LOAD THE NUMBER IN THE
78	2087	8A 38	ORA A	#38	HIGH SPEED COUNTER
79	2089	B7 80 1B	STA A	F1ACRB	
80	208C	B6 80 1B	LDA A	F1ACRB	
81	208F	84 F7	AND A	#F7	
82	2091	B7 80 1B	STA A	F1ACRB	
83	2094	B6 80 1A	LDA A	F1ACRA	READY TO START SAMPLING
84	2097	84 F7	AND A	#F7	
85	2099	B7 80 1A	STA A	F1ACRA	
86	209C	B6 80 1A	LDA A	F1ACRA	
87	209F	8A 38	ORA A	#38	
88	20A1	B7 80 1A	STA A	F1ACRA	
89	20A4	BD 22 80	JSR	DELAY	
90	20A7	B6 80 1A	LDA A	F1ACRA	WAIT FOR END OF ACQUI-
91	20AA	2A FB	BPL	WAIT	SITION
92	20AC	B6 80 18	LDA A	F1ADRA	GET LO BYTE
93	20AF	F6 80 14	LDA B	F3ADRA	GET HI BYTE
94	20B2	97 51	STA A	#51	STORE THEM IN TEMP
95	20B4	C4 0F	AND B	#0F	REGISTERS FOR SUM
96	20B6	D7 52	STA B	#52	
97	20B8	7F 00 53	CLR	#53	
98	20BB	7F 00 54	CLR	#54	
99	20BE	FE 02 04	LDX	LODEST	GET OLD DATA
100	20C1	A6 00	LDA A	0,X	
101	20C3	E6 01	LDA B	1,X	
102	20C5	97 41	STA A	#41	AND STORE THEM IN THE
103	20C7	D7 42	STA B	#42	SUM REGISTERS
104	20C9	FE 02 02	LDX	HIDEST	
105	20CC	A6 00	LDA A	0,X	
106	20CE	E6 01	LDA B	1,X	
107	20D0	97 43	STA A	#43	
108	20D2	D7 44	STA B	#44	
109	20D4	BD 22 66	JSR	SUM	SUM OLD DATA WITH NEW
110	20D7	96 41	LDA A	#41	DATA
111	20D9	D6 42	LDA I	142	

111	2018	FE	02	04	LDX	LODEST
112	2019	A			STX A	1.0
113	2020	FE	01		STA F	1.0
114	2021	08			INX	
115	2022	08			INX	
116	2023	FF	02	04	STX	LODEST
117	2024	96	43		LDA A	\$43
118	2025	D6	44		LDA B	\$44
119	2026	FE	02	00	LDX	HIDEST
120	2027	A7	00		STA A	0.0
121	2028	EF	01		STA F	1.0
122	2029	08			INX	
123	2030	08			INX	
124	2031	FF	02	00	STX	HIDEST
125	2032	FE	02	00	LDX	COUNT
126	2033	09			DEX	
127	2034	26	32		BNE	GO1
128	2035	7A	02	0E	DEC	AVRG
129	2036	26	30		BNE	GO2
130	2100	CE	40	00	LDX	\$4000
131	2101	FF	02	04	STX	LODEST
132	2102	CE	50	00	LDX	\$5000
133	2103	FF	02	02	STX	HIDEST
134	2104	CE	08	00	LDX	\$0800
135	2105	FF	02	00	STX	COUNT
136	2106	B6	02	0C	LDA A	AVR
137	2107	B7	02	10	STA A	TIME
138	2108	74	02	10	LSR	TIME
139	2109	25	16		RCS	YES
140	2110	FE	02	02	LDX	HIDEST
141	2111	64	01		LSR	1.0
142	2112	66	00		ROR	0.0
143	2113	FE	02	04	LDX	LODEST
144	2114	66	01		ROR	1.0
145	2115	66	00		ROR	0.0
146	2116	20	EF		BRA	RUN
147	2117	7E	20	73	JMP	AGAIN
148	2118	7E	20	59	JMP	MORE
149	2119	FE	02	04	LDX	LODEST
150	2120	08			INX	
151	2121	08			INX	
152	2122	FF	02	04	STX	LODEST
153	2123	FE	02	02	LDX	HIDEST
154	2124	08			INX	
155	2125	08			INX	
156	2126	FF	02	02	STX	HIDEST
157	2127	FE	02	00	LDX	COUNT
158	2128	09			DEX	
159	2129	26	C6		BNE	LOOP
160	2130	86	01		LDA A	\$01
161	2131	B7	02	12	STA A	FLAG
162	2132	CE	40	00	LDX	\$4000
163	2133	FF	02	04	STX	LODEST
164	2134	CE	60	00	LDX	\$6000

STATE OF INDICATED IN
THE POINTS

DECREMENT SOFTWARE
COUNTER
FINISH THE 2048 SAMPLES
YES, DECREMENT AVERG. C
FINISH AVERAGING?
YES, THEN DIVIDE BY TH
NUMBER OF AVERAGE

LOOP

RUN

GO1
GO2
YES

CONTINUE SAMPLING
DO MORE AVERAGES

INCREMENT
DESTINATION
REGISTERS

ANY MORE POINTS?

NO

166	2154	FF			LOSQU
167	2155	FE			\$100
168	2156	FF	10 10	TRAN	COUNTY
169	2157	FE	02 10		TRANSER THE
170	2158	FE	02 11		BAJA POINTS
171	2159	FE	02 04		FOR PERMANENT
172	2160	FE	02 04		STORAGE
173	2161	FE	02 04		
174	2162	FE	02 04		
175	2163	FE	02 04		
176	2164	FE	02 04		
177	2165	FE	02 04		
178	2166	FE	02 04		
179	2167	FE	02 04		
180	2168	FE	02 04		
181	2169	FE	02 04		
182	2170	FE	02 04		
183	2171	FE	02 04		
184	2172	FE	02 04		
185	2173	FE	02 04		
186	2174	FE	02 04		
187	2175	FE	02 04		
188	2176	FE	02 04		
189	2177	FE	02 04		
190	2178	FE	02 04		
191	2179	FE	02 04		
192	2180	FE	02 04		
193	2181	FE	02 04		
194	2182	FE	02 04		
195	2183	FE	02 04		
196	2184	FE	02 04		
197	2185	FE	02 04		
198	2186	FE	02 04		
199	2187	FE	02 04		
200	2188	FE	02 04		
201	2189	FE	02 04		
202	2190	FE	02 04		
203	2191	FE	02 04		
204	2192	FE	02 04		
205	2193	FE	02 04		
206	2194	FE	02 04		
207	2195	FE	02 04		
208	2196	FE	02 04		
209	2197	FE	02 04		
210	2198	FE	02 04		
211	2199	FE	02 04		
212	2200	FE	02 04		
213	2201	FE	02 04		
214	2202	FE	02 04		
215	2203	FE	02 04		
216	2204	FE	02 04		
217	2205	FE	02 04		
218	2206	FE	02 04		
219	2207	FE	02 04		

211	2181	FE	01	01
212	218A	09		
213	2184	18	80	
223	218F	CE	60	00
224	21DE	FF	02	08
225	21E1	86	6F	
226	21E3	B7	80	1A
227	21E6	7F	80	1A
228	21E9	86	FF	
229	21EF	B7	80	1E
230	21EE	86	06	
231	21FC	F7	80	1A
232	21FE	7F	80	1E
233	21F6	86	FF	
234	21F8	B7	80	1A
235	21FB	86	06	
236	21FD	F7	80	1E
237	2200	86	2F	
238	2203	F7	80	1E
239	2205	86	6F	
240	2207	F7	80	1E
241	220A	CE	00	
242	220E	FE	02	08
243	2210	FE	02	08
244	2213	A6	00	
245	2215	E6	01	
246	2217	F7	80	1E
247	221A	F7	80	1A
248	221E	06		
249	221B	06		
250	221F	FF	02	10
251	2222	06	4F	
252	2224	F7	80	1D
253	2227	06	6F	
254	2229	F7	80	1E
255	222C	86	6F	1E
256	222F	8A	3E	
257	2231	F7	80	1E
258	2234	86	80	1E
259	2237	8A	F7	
260	2239	F7	80	1E
261	223C	FE	02	00
262	223F	09		
263	2240	26	CF	
264	2242	7F	80	1A
265	2245	7F	80	18
266	2248	86	06	
267	224A	B7	80	1A
268	224D	7F	80	16
269	2250	7F	80	1A
270	2253	86	06	
271	2255	B7	80	16
272	2258	86	E7	
273	225A	B7	80	1D

END	
LDA A	\$B6C
STA	LOSOUR
LDA A	\$B6F
STA A	F2ADRE
CLR	F1ACRA
LDA A	\$BFF
STA A	F1ADRA
LDA A	\$B0A
STA A	F1A77
CLR	F3ACRA
LDA A	\$B
STA A	F3AEFA
LDA A	\$B0E
STA A	F3ACRA
LDA A	\$B2F
STA A	F2ADRE
LDA A	\$B6F
STA A	F2ADRE
IND	\$B
STA	LOSOUR
LDA A	\$B
LDA B	\$B
STA A	F1AEFA
STA B	F2IAA
IND	
IND	
STA	LOSOUR
LDA E	\$B4F
STA E	F2ADRE
LDA E	\$B6F
STA :	F2ADRE
LDA A	F2ACRA
ORA A	\$B3E
STA A	F2ACRA
LDA A	F2ACRA
AND A	\$BF7
STA A	F2ACRA
LIX	COUNT
DIX	
RNE	NEW
CLR	F1ACRA
CLR	F1ADRA
LDA A	\$B06
STA A	F1ACRA
CLR	F3ACRA
CLR	F3ADRA
LDA A	\$B06
STA A	F3ACRA
LDA A	\$BE7
STA A	F2ADRE

ENRILE RM. 120111
A T E AMI L A C
CE T 1007 10 05 00

SEND A CLEAR PULSE
FOR THE ADDRESS
COUNTER

WRITE IN THE IN-

INCREMENT THE
ADDRESS COUNTER

DECREMENT SOFTWARE.CT:
ANY MORE POINTS?
NO, SET FORT 1A AS
INPUT

SET PORT 3A AS INPUT

DISABLE A/D. ENAB

	OFF	FLAG	
	NAME	RANDOM LABELING (MAX 15 MHz)	
	* RANDOM LABELING (MAX 15 MHz)		
4	801A	F1ACRA EQU	\$801A
5	801B	F1ADRA EQU	\$801B
6	801C	F1ACRB EQU	\$801C
7	801D	F1ADRB EQU	\$801D
8	801E	F2ACRA EQU	\$801E
9	801C	F2ADRA EQU	\$801C
10	801F	F2ACRB EQU	\$801F
11	801D	F2ADRB EQU	\$801D
12	8016	F3ACRA EQU	\$8016
13	8014	F3ADRA EQU	\$8014
14	8017	F3ACRB EQU	\$8017
15	8015	F3ADRB EQU	\$8015
16	0200	COUNTN EQU	\$0200
17	0202	HIDEST EQU	\$0202
18	0204	LODEST EQU	\$0204
19	0206	HISOUR EQU	\$0206
20	0208	LOSOUR EQU	\$0208
21	020A	MILCNT EQU	\$020A
22	020C	AVR EQU	\$020C
23	020E	AVRG EQU	\$020E
24	0210	TIME EQU	\$0210
25	0212	FLAG EQU	\$0212
26	0214	ADRESS EQU	\$0214
27	0216	AVRCNT EQU	\$0216
28	0218	TEMP4 EQU	\$0218
29	021A	TEMP5 EQU	\$021A
30	021C	TEMP6 EQU	\$021C
31	021E	TEMP7 EQU	\$021E
32	2000	ORG	\$2000
33	2000 CE 40 00	LDX	\$\$4000
34	2003 4F	CLR A	
35	2004 A7 00	STA A 0,X	
36	2006 08	INX	
37	2007 86 70 00	CPX	\$\$7000
38	200A 26 F8	BNE	BACK
39	200C 86 01	LDA A	\$\$01
40	200E B7 02 16	STA A	AVRCNT
41	2011 7F 80 1A	CLR	F1ACRA
42	2014 7F 80 18	CLR	F1ADRA
43	2017 86 06	LDA A	\$\$06
44	2019 B7 80 1A	STA A	F1ACRA
45	201C 7F 80 1B	CLR	F1ACRB
46	201F 86 FF	LDA A	\$\$FF
47	2021 B7 80 19	STA A	F1ADRB
48	2024 86 06	LDA A	\$\$06
49	2026 B7 80 1B	STA A	F1ACRB
50	2029 7F 80 1F	CLR	F2ACRB
51	202C 86 FF	LDA A	\$\$FF
52	202E B7 80 1D	STA A	F2ADRB
53	2031 86 04	LDA A	\$\$04
54	2033 B7 80 1F	STA A	F2ACRB
55	2036 7F 80 16	CLR	F3ACRA
56	2039 7F 80 14	CLR	F3ADRA
57	203C 86 06	LDA A	\$\$06

CLEAR MEMORY LOCATIONS FOR STORAGE

SET PORT 1A AS INPUT

SET PORT 1B AS OUTPUT

SET PORT 2B AS OUTPUT

SET PORT 3A AS INPUT

55	203E	B7	80	1A	STA A	P1ACRA	
56	2041	B7	1		LDA A	111	STORE NUMBER IN ADDRESS
57	2043	B7	02	00	STA A	AVI	MAXIMUM 10
58	2046	B7	02	0E	STA A	AVR0	
59	2049	B6	80	1B	LDA A	P1ACR1	SET LOAD LINE HIGH
60	204C	B4	F7		AND A	00F7	
61	204E	B7	80	1B	STA A	P1ACR1	
62	2051	B6	80	1A	LDA A	P1ACRA	DISABLE ACKNOWLEDGE CONTROL
63	2054	BA	38		ORA A	0038	SIGNAL OF MICROPROCESSOR
64	2056	B7	80	1A	STA A	P1ACRA	
65	2059	CE	08	00	LDX	000800	INITIALIZE SOFTWARE
66	205C	FF	02	00	STX	COUNT1	COUNTER
67	205F	CE	30	00	LDX	003000	INITIALIZE ADDRESS
68	2062	FF	02	14	STX	ADDRESS	REGISTER
69	2065	CE	40	00	LDX	004000	INITIALIZE DESTINATION
70	2068	FF	02	04	STX	LODEST	REGISTER (LO BYTE)
71	206B	CE	50	00	LDX	005000	AND (HI BYTE)
72	206E	FF	02	02	STX	HIDEST	
73	2071	B6	FF		LDA A	00FF	ENABLE A/D'S OUTPUT
74	2073	B7	80	1D	STA A	P2ADRB	LATCHES
75	2076	FE	02	00	LDX	COUNT1	
76	2079	FF	02	00	STX	COUNT1	
77	207C	FE	02	14	LDX	ADDRESS	GET RANDOM NUMBER
78	207F	E6	00		LDA B	00X	FROM THE LOOK UP
79	2081	A6	01		LDA A	10X	TABLE
80	2083	08			INX		
81	2084	08			INX		
82	2085	FF	02	14	STX	ADDRESS	
83	2088	CA	F8		ORA B	00F8	
84	208A	B7	80	19	STA A	P1ADRB	STORE DELAY NUMBER
85	208D	F7	80	1D	STA B	P2ADRB	
86	2090	C4	47		AND B	0047	
87	2092	F7	02	18	STA B	TEMP4	
88	2095	B7	02	19	STA A	TEMP4+1	
89	2098	CA	10		ORA B	0010	
90	209A	F7	02	1A	STA B	TEMP5	
91	209D	B7	02	1B	STA A	TEMP5+1	
92	20A0	CA	20		ORA B	0020	
93	20A2	F7	02	1E	STA B	TEMP7	
94	20A5	B7	02	1F	STA A	TEMP7+1	
95	20A8	C4	67		AND B	0067	
96	20AA	F7	02	1C	STA B	TEMP6	
97	20AD	B7	02	1D	STA A	TEMP6+1	
98	20B0	B6	80	1B	LDA A	P1ACRB	LOAD THE NUMBER IN THE
99	20B3	BA	38		ORA A	0038	HIGH SPEED COUNTER
100	20B5	B7	80	1B	STA A	P1ACRB	
101	20B8	B6	80	1B	LDA A	P1ACRB	
102	20BB	B4	F7		AND A	00F7	
103	20BD	B7	80	1B	STA A	P1ACRB	
104	20C0	B6	80	1A	LDA A	P1ACRA	READY TO START SAMPLING
105	20C3	B4	F7		AND A	00F7	
106	20C5	B7	80	1A	STA A	P1ACRA	
107	20C8	B6	80	1A	LDA A	P1ACRA	
108	20CB	BA	38		ORA A	0038	

111	200F 17 80 1A	STA A	F1ACRA	
112	2010 F5 22 6E	JSR	DELAY	
114	2013 B6 80 1A	LDA A	F1ACRA	WAIT FOR END OF ACQUI
115	2016 2A FB	BFL	WAIT	SITION
116	2018 B6 80 18	LDA A	F1ADRA	GET LO BYTE
117	201B F6 80 1A	LDA B	F3ADRA	GET HI BYTE
118	201E 97 51	STA A	\$51	STORE THE IN TEMP
119	20E0 D7 52	STA B	\$52	REGISTER FOR SUM
120	20E2 7F 00 53	CLF	\$53	
121	20E5 7F 00 54	CLF	\$54	
122	20E8 FE 02 18	LDR	TEMP4	GET OLD DATA
123	20EB A6 00	LDA A	0x	
124	20ED 97 41	STA A	\$41	AND STORE THEM IN THE
125	20EF FE 02 1A	LDR	TEMP5	DATA REGISTERS
126	20F2 A6 00	LDA A	0x	
127	20F4 97 42	STA A	\$42	
128	20F6 FE 02 1C	LDR	TEMP6	
129	20F9 A6 00	LDA A	0x	
130	20FB 97 43	STA A	\$43	
131	20FD FE 02 1E	LDR	TEMP7	
132	2100 A6 00	LDA A	0x	
133	2102 97 44	STA A	\$44	
134	2104 BD 22 54	JSR	UM	SUM OLD DATA WITH
135	2107 96 41	LDA A	\$41	NEW DATA
136	2109 FE 02 18	LDR	TEMP4	
137	210C A7 00	STA A	0x	STORE SUM AS INDICATED
138	210E 96 42	LDA A	\$42	BY THE POINTER
139	2110 FE 02 1A	LDR	TEMP5	
140	2113 A7 00	STA A	0x	
141	2115 96 43	LDA A	\$43	
142	2117 FE 02 1C	LDR	TEMP6	
143	211A A7 00	STA A	0x	
144	211C 96 44	LDA A	\$44	
145	211E FE 02 1E	LDR	TEMP7	
146	2121 A7 00	STA A	0x	
147	2123 FE 02 00	LDR	COUNTN	DECREMENT SOFTWARE
148	2126 09	DEX		COUNTER
149	2127 26 44	BNE	G01	FINISH THE 2048 SAMPLES
150	2129 7A 02 0E	DEC	AVERG	YES, DECREMENT AVERG. CTR
151	212C 26 42	BNE	G02	FINISH AVERAGING?
152	212E CE 40 00	LDR	\$4000	YES, THEN DIVIDE BY THE
153	2131 FF 02 18	STX	TEMP4	NUMBER OF AVERAGES
154	2134 CE 50 00	LDR	\$5000	
155	2137 FF 02 1A	STX	TEMP5	
156	213A CE 60 00	LDR	\$6000	
157	213D FF 02 1C	STX	TEMP6	
158	2140 CE 70 00	LDR	\$7000	
159	2143 FF 02 1E	STX	TEMP7	
160	2146 CE 08 00	LDR	\$8000	
161	2149 FF 02 00	STX	COUNTN	
162	214C B6 02 0C	LDA A	AVER	
163	214F B7 02 10	STA A	TIME	
164	2152 74 02 10	LSR	TIME	
165	2155 25 1C	BCS	YES	

166	2117	FE	02	11		LDX	TEMP 1	
167	215A	64	00			LDA	0,X	
168	2150	FE	02	10		LDX	TEMP 2	
169	215F	66	00			ROR	0,X	
170	2161	FE	02	1A		LDX	TEMP 5	
171	2164	66	00			ROR	0,X	
172	2166	FE	02	18		LDX	TEMP 4	
173	2169	66	00			ROR	0,X	
174	216B	20	E5			BRA	RUN	
175	216D	7E	20	79	G01	JMP	AGAIN	CONTINUE SAMPLING
176	2170	7E	20	59	G02	JMP	MORE	DO MORE AVERAGES
177	2173	FE	02	18	YES	LDX	TEMP 4	
178	2176	08				INX		
179	2177	FF	02	18		STX	TEMP 4	
180	217A	FE	02	1A		LDX	TEMP 5	INCREMENT DESTINATION
181	217D	08				INX		REGISTERS
182	217E	FF	02	1A		STX	TEMP 5	
183	2181	FE	02	1C		LDX	TEMP 6	
184	2184	08				INX		
185	2185	FF	02	1C		STX	TEMP 6	
186	2188	FE	02	1E		LDX	TEMP 7	
187	218B	08				INX		
188	218C	FF	02	1F		STX	TEMP 7	
189	218F	FE	02	00		LDX	COUNTA	ANY MORE POINTS?
190	2192	09				DEX		
191	2193	26	B4			BNE	LOOP	
192	2195	CE	40	00		LDX	##4000	NO
193	2198	FF	02	04		STX	LODEST	
194	219B	CE	50	00		LDX	##5000	
195	219E	FF	02	02		STX	HIDEST	
196	21A1	CE	60	00		LDX	##6000	
197	21A4	FF	02	08		STX	LOSOUR	
198	21A7	CE	08	00		LDX	##0800	
199	21AA	FF	02	00	TRAN	STX	COUNTR	TRANSFER THE
200	21AD	FE	02	04		LDX	LODEST	DATA POINTS
201	21B0	A6	00			LDA	0,X	FOR PERMANENT
202	21B2	08				INX		STORAGE
203	21B3	FF	02	04		STX	LODEST	
204	21B6	FE	02	02		LDX	HIDEST	
205	21B9	E6	00			LDA B	0,X	
206	21BB	08				INX		
207	21BC	FF	02	02		STX	HIDEST	
208	21BF	FE	02	08		LDX	LOSOUR	
209	21C2	A7	00			STA A	0,X	
210	21C4	E7	01			STA B	1,X	
211	21C6	08				INX		
212	21C7	08				INX		
213	21C8	FF	02	08		STX	LOSOUR	
214	21CB	FE	02	00		LDX	COUNTR	
215	21CE	09				DEX		
216	21CF	26	D9			BNE	TRAN	
217	21D1	CE	60	00		LDX	##6000	
218	21D4	FF	02	08		STX	LOSOUR	
219	21D7	B6	6F			LDA A	##6F	ENABLE BM. DISABLE

220	21D9	B7 80 1D	STA A	P2ADRI	ADDS AND DECS
221	21DC	7F 80 1A	CLR	P1ACRA	SET PORT 1A AS OUTPUT
222	21D9	86 FF	LDA A	##FF	
223	21E1	B7 80 18	STA A	P1ADRA	
224	21E4	86 06	LDA A	##06	
225	21E6	B7 80 1A	STA A	P1ACRA	
226	21E9	7F 80 16	CLR	P3ACRA	SET PORT 3A AS OUTPUT
227	21EC	86 FF	LDA A	##FF	
228	21EE	B7 80 14	STA A	P3ADRA	
229	21F1	86 06	LDA A	##06	
230	21F3	B7 80 16	STA A	P3ACRA	
231	21F6	86 2F	LDA A	##2F	SEND A CLEAR PULSE
232	21F8	B7 80 1D	STA A	P2ADRI	FOR THE ADDRESS
233	21FB	86 6F	LDA A	##6F	COUNTER
234	21FD	B7 80 1D	STA A	P2ADRB	
235	2200	CE 06 00	LDX	##0800	
236	2203	FF 02 00	STX	COUNTR	
237	2206	FE 02 08	LDX	LOSOUR	
238	2209	A6 00	LDA A	0,X	
239	220B	E6 01	LDA B	1,X	
240	220D	B7 80 18	STA A	P1ADRA	
241	2210	F7 80 14	STA B	P3ADRA	
242	2213	08	INX		
243	2214	08	INX		
244	2215	FF 02 08	STX	LOSOUR	
245	2218	C6 4F	LDA B	##4F	WRITE IN THE BM
246	221A	F7 80 1D	STA B	P2ADRB	
247	221D	C6 6F	LDA B	##6F	
248	221F	F7 80 1D	STA B	P2ADRB	
249	2222	86 80 1E	LDA A	P2ACRA	INCREMENT THE
250	2225	8A 38	ORA A	##38	ADDRESS COUNTER
251	2227	B7 80 1E	STA A	P2ACRA	
252	222A	86 80 1E	LDA A	P2ACRA	
253	222D	84 F7	AND A	##F7	
254	222F	B7 80 1E	STA A	P2ACRA	
255	2232	FE 02 00	LDX	COUNTR	DECREMENT SOFTWARE
256	2235	09	DEX		COUNTER
257	2236	26 CB	BNE	NEW	ANY MORE POINTS?
258	2238	7F 80 1A	CLR	P1ACRA	NO, SET PORT 1A
259	223B	7F 80 18	CLR	P1ADRA	AS INPUT
260	223E	86 06	LDA A	##06	
261	2240	B7 80 1A	STA A	P1ACRA	
262	2243	7F 80 16	CLR	P3ACRA	SET PORT 3A AS INPUT
263	2246	7F 80 14	CLR	P3ADRA	
264	2249	86 06	LDA A	##06	
265	224B	B7 80 16	STA A	P3ACRA	
266	224E	86 E7	LDA A	##E7	DISABLE A/D. ENABLE D/A
267	2250	B7 80 1D	STA A	P2ADRB	
268	2253	39	RTS		
269	2254	0C	CLC		SUBROUTINE FOR 16 BIT
270	2255	96 41	LDA A	##41	ADDITION
271	2257	99 51	ADC A	##51	
272	2259	97 41	STA A	##41	
273	225B	96 42	LDA A	##42	

NEW

SUM

RANDOM SAMPLING (MAX 25 MHz)

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274	225D	99	52		ADC A	\$52	
275	225F	97	42		STA A	\$42	
276	2261	96	43		LDA A	\$43	
277	2263	99	53		ADC A	\$53	
278	2265	97	43		STA A	\$43	
279	2267	96	44		LDA A	\$44	
280	2269	99	54		ADC A	\$54	
281	226B	97	44		STA A	\$44	
282	226D	39			RTS		
283	226E	86	11	DELAY	LDA A	\$11	SUBROUTINE DELAY
284	2270	87	02	0A	STA A	MILCNT	
285	2273	7A	02	0A	DEC	MILCNT	
286	2275	26	FB	MORDEC	BNE	MORDEC	
287	2278	39			RTS		
288					END		

NO ERROR(S) DETECTED

RANDOM SAMPLING (MAX 25 MHz)

SYMBOL TABLE:

ADRESS	0214	AGAIN	2079	AVR	020C	AVRCNT	0216	AVRG	020E
BACK	2004	COUNTR	0200	DELAY	226E	FLAG	0212	G01	216D
G02	2170	HIDEST	0202	HISOUR	0206	LODEST	0204	LOOP	2149
LOSOUR	0208	MILCNT	020A	MURDEC	2273	MORE	2059	NEW	2203
F1ACRA	801A	F1ACRB	801B	F1ADRA	801B	F1ADRB	8019	F2ACRA	801E
F2ACRB	801F	F2ADRA	801C	F2ADRB	801D	F3ACRA	8016	F3ACRB	8017
F3ADRA	8014	F3ADRB	8015	RUN	2152	START	2041	SUM	2254
TEMP4	0218	TEMP5	021A	TEMP6	021C	TEMP7	021E	TIME	0210
TRAN	21AA	WAIT	20D3	YES	2173				

APPENDIX K

SPECIFICATIONS FOR THE SAMPLE AND HOLD, AND THE
ANALOG TO DIGITAL CONVERTER

SPECIFICATIONS

Typical at 25°C and nominal power supply voltages unless otherwise noted.

MODEL	UNITS	HTS-002*	HTS-0025M	HTC-0100
DYNAMIC CHARACTERISTICS				
Acquisition Time (See Figure 1) to 100 mV Output Step	ns typ (max)	20 (30)	*	N/A
to 100 mV Output Step	ns typ (max)	N/A	*	170 (200)
Sample Rate	MHz max	10	*	5
Aperture Time	ns min (typ) (max)	6 (10) (20)	*	*
Settling Time	ns typ (max)	20 (30)	*	100 (120)
Bandwidth - 0 dB 1 V p-p Input	MHz min	10	20	N/A
Bandwidth - 0 dB Small Signal Input	MHz min	N/A	*	8
Slew Rate	V/μs typ (min)	400 (200)	*	250 (120)
Aperture Uncertainty	ps (rms) max	20	*	100
Harmonic Distortion (See Figure 6 and Output Loading)	dB typ (max)	65 (60)	*	75 (62)
Feedthrough Rejection (2V p-p, 10MHz Input)	dB min	70	**	N/A
(dc to 2.5MHz)	dB min	N/A	*	70
Drop Rate	mV/μs typ (max)	0.2 (4)	0.2 (30)	0.005 (0.007)
Process Drifts (Hold) (See Figure 1)	mV typ (max)	2 (20)	*	5 (50)
Transients (See Figure 1)	mV typ (max)	10 (100)	*	N/A
ACCURACY/STABILITY DC				
*Gain	V/V	+0.92 min	*	-1.00 ± 0.1%
Gain vs. Temperature	ppm/°C typ (max)	20 (40)	*	10 (50)
Zero Offset Voltage	mV typ (max)	2 (20)	*	2 (20)
Offset vs. Temperature	typ (max)	30 (150) μV/°C	*	40 (75) ppm/°C
Linearity	% max	0.01	*	*
INPUT				
Voltage Range	V max	12	*	±10
60dB Feedthrough Rejection	V p-p max	1	*	N/A
Impedance	Ω typ min	10 ¹⁰ 10 ⁸	10 ¹⁰ 10 ⁸	10K [†]
Bias Current	nA max	1.5	10K	15 μA
OUTPUT				
Voltage	V max	12	*	±10
Current (not short circuit protected)	mA max	±50	*	*
Impedance	Ω typ (max)	5 10	*	0.1 (dc)
Load - Harmonic				
Distortion for 2V p-p	Ω min	50	*	N/A
Signal and Specified R _L	Ω min	100	*	N/A
60dB	Ω min	200	*	N/A
85dB	mV rms	0.1 (max)	0.2 (max)	0.1
HOLD COMMAND/DIGITAL INPUT				
Logic Compatible		ECL	*	TTL
0 = Track 1 = Hold [‡]	V	-1.5 to -1.4/-0.7 to -1.05	*	N/A
Hold Input 0 = Track 1 = Hold	V	N/A	*	0 to +0.4/+2.4 to +5
Hold Input 0 = Hold 1 = Track	V	N/A	*	0 to +0.4/+2.4 to +5
POWER REQUIREMENTS - HTS				
V ₊ = +15V ±0.5V (Pins 8 and 22)	mA max	40	*	N/A
V ₋ = -15V ±0.5V (Pins 1 and 12)	mA max	40	*	N/A
V _{CC} = +4.4V to +15.5V (Pins 1 and 9) [§]	mA max	15	*	N/A
V _{CC} = +4.9V to +15.5V (Pins 2 and 10) [§]	mA max	15	*	N/A
V _{EE} = -5.2V to -25V (Pin 4)	mA max	40	*	N/A
POWER REQUIREMENTS - HTC				
±12V to ±18V	mA max	N/A	*	25
+5V to ±0.25V	mA max	N/A	*	25
Power Supply Rejection Ratio	mV/V	N/A	*	10
TEMPERATURE RANGE				
Operating (Case)	°C	0 to +70	-55 to +100	0 to +70
Storage	°C	-55 to +125	*	*

NOTES

* Sample rates shown are a guide only, and are based on system acquisition times - see logic speed. These rates can be exceeded with acquisition time trade-offs.

† Drop rate for case temperatures up to 50°C is 1mV/μs max.

‡ Noise level measured in track mode at 5MHz bandwidth. Noise level increases when high duty cycle repetitive hold command is applied. A 50% duty cycle hold command results in approximately 0.5mV (rms) signal source output.

§ One ECL 10m Gate on pull-down resistor.

¶ V_{CC} may be tied to V₊. V_{CC} may be tied to V₋ or V_{EE}. However, for proper operation, V_{CC} and V_{EE} must have the same nominal value.

* Specifications same as model HTS-0025.

** Specifications same as model HTC-0100.

Specifications subject to change without notice.

Specifications in parentheses indicate max. min. over entire specified operating temperature range.

SPECIFICATIONS ADC-EH12B3

(Typical at 25°C, ±5V, 500 Hz)

Analog Input Range
Input Impedance
Input Overvoltage
Start Conversion

0V to +10V FS or ±5V FS
1.15k ohms ±0.1%
20V, no damage
2V min. to 5V max. positive pulse
with duration of 100 nsec. min. Rise
and fall times <500 nsec.
Logic 1: resets converter
Logic 0: initiates conversion
Loading: 1 TTL load

Parallel Output Data

12 parallel lines of data held until
next conversion command
V_{out} (10¹¹) < +0.4V
V_{out} (1¹¹) > +2.4V
Each output capable of driving up to
2 TTL loads

Coding: Unipolar operation
Bipolar operation

Straight Binary: positive true
Offset Binary: positive true
Two's complement: positive true
NRZ successive decision pulse output
generated during conversion with
MSB first

Serial Output Data

Straight binary or offset binary,
positive true coding
Loading: 4 TTL loads

End of Conversion (EOC)

Conversion Status Signal
V_{out} (1⁰) < +0.4V indicates con-
version completed
V_{out} (1⁰) > +2.4V during reset and
conversion
Loading: 4 TTL loads
Internal clock pulse train of negative
going pulses from +5V to 0V gated on
during conversion time
Loading: 6 TTL loads

Clock Output

Resolution

12 Bits (1 part in 4096)

Accuracy at 25°C

±0.12% of FS ±1/2 LSB

Nonlinearity

±1/2 LSB max

Differential Nonlinearity

±1/2 LSB max

Differential Nonlinearity T.C.

±3ppm/°C max

Temp. Coeff. of Gain

±30ppm/°C max

Temp. Coeff. of Zero unipolar

±150 μV/°C max

Temp. Coeff. of Offset bipolar

±15ppm of F.S./°C max

Power Supply Rejection

0.1% FS/supply max

Conversion Time

2.0 μsec maximum

+15VDC ±0.5V @ 80mA max

-15VDC ±0.5V @ 20mA max

+5VDC ±0.25V @ 150mA max

Operating Temp. Range

0°C to 70°C

Storage Temp. Range

-25°C to +85°C

Relative Humidity

Up to 100% non-condensing

Case Size

4 x 2 x 0.6 inches

(101.6 x 50.8 x 10.2mm)

Case Material

Black DuPont Phthalate per MIL M 14

Finish

020: round, gold plated

Weight

200: long min

4 oz max (114 g)

TIMING DIAGRAM FOR ADC-EH12B3 Output 101010101010 **OUTPUT CODING****UNIPOLAR 10V to +10V¹**

SCALE	INPUT VOLTAGE	STRAIGHT BINARY
+FS - 1 LSB	+9.9976V	1111 1111 1111
+7/8 FS	+8.7500V	1110 0000 0000
+3/4 FS	+7.5000V	1100 0000 0000
+1/2 FS	+5.0000V	1000 0000 0000
+1/4 FS	+2.5000V	0100 0000 0000
+1 LSB	+0.0024V	0000 0000 0001
0	0.0000V	0000 0000 0000

BIPOLAR (-5V to +5V)

SCALE	INPUT VOLTAGE	OFFSET BINARY	TWO'S COMPLEMENT ²
+FS - 1 LSB	+4.9976V	1111 1111 1111	0111 1111 1111
+3/4 FS	+3.7500V	1110 0000 0000	0110 0000 0000
+1/2 FS	+2.5000V	1100 0000 0000	0100 0000 0000
0	0.0000V	1000 0000 0000	0000 0000 0000
-1/2 FS	-2.5000V	0100 0000 0000	1100 0000 0000
-3/4 FS	-3.7500V	0010 0000 0000	1010 0000 0000
-FS + 1 LSB	-4.9976V	0000 0000 0001	1000 0000 0001
-FS	-5.0000V	0000 0000 0000	1000 0000 0000

¹Using MSB output for Bit 1

GAIN & OFFSET ADJUSTMENTS **UNIPOLAR OPERATION**

1. Apply START CONVERT pulse to pin 24 (see pin 14 timing and timing diagram).
2. Apply a first data reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to zero (±1/2 LSB (±1.2mV)). Adjust the gain to ensure the output code is the same as the input code (the code is the same between 0000 0000 0000 and 0000 0000 0001).
3. Adjust the output of the voltage reference to +FS (±1/2 LSB (±4.9976V)). Adjust the GAIN to ensure the output code is the same as the input code (the code is the same between 1111 1111 1110 and 1111 1111 1111).

BIPOLAR OPERATION

1. Apply START CONVERT pulse to pin 24 (see pin 14 timing and timing diagram).
2. Apply a first data reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to zero (±1/2 LSB (±1.2mV)). Adjust the offset to ensure the output code is the same as the input code (the code is the same between 0000 0000 0000 and 0000 0000 0001).
3. Adjust the output of the voltage reference to +FS (±1/2 LSB (±4.9976V)). Adjust the GAIN to ensure the output code is the same as the input code (the code is the same between 1111 1111 1110 and 1111 1111 1111).

ORDERING INFORMATION**PRICES (1-8)**

ADC-EH12B3 \$249.00

MATING SOCKETS

DILS-2 (2/MODULE) \$5.00/PAIR

TRIMMING POTENTIOMETERS

TP20, TP200, TP20K \$3.00 EACH

For extended temperature range operation, the following suffixes are added to the model number. Consult factory for pricing.

- EX -25°C to +85°C operation
- EXX-HS -55°C to +85°C operation with hermetically sealed semiconductor components

THE ADC-EH12B3 CONVERTER IS COVERED UNDER GSA CONTRACT.

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