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A CMOS LOW NOISE AMPLIFIER FOR IMPULSE RADIO ULTRA-WIDEBAND APPLICATIONS

By
Yasser Khairat Soliman

A thesis
presented to Carleton University
in fulfilment of the
thesis requirement for the degree of
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in
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Abstract

The design and implementation of an Ultra-wideband (UWB) low noise amplifier (LNA) in $0.18\mu\text{m}$ CMOS technology is presented in this thesis. A 3.1-10.6 GHz, single-stage, low noise amplifier (LNA) design employing a frequency dependant feedback network is reported. Post-layout simulations of the LNA demonstrated a power gain of 8 dB, an input matching of -13 dB, a minimum spot noise figure (NF) of 3.5 dB and an average NF of 4.4 dB. The amplifier exploits a combination of negative and positive feedback to attain a flat gain across the entire bandwidth with an input-referred 1 dB compression at -2.48 dBm, an input-referred second- and third-order intermodulation intercept points (IIP_2 , IIP_3) at 10.71 dBm and 20.76 dBm, respectively. An ultra-wideband noise and power matching technique utilizing frequency dependent Miller's multiplication factors is presented.

The transient response to the fifth order derivative of a Gaussian monopulse input occupying a bandwidth of 6.6 GHz was demonstrated in simulations. The correlation coefficient between the input and the output monopulses is above 99 % emphasizing the minimum distortion introduced by the amplifier.

The measured LNA demonstrated a voltage gain of 9.53 ± 0.86 dB with a 3 dB bandwidth of 7.3 GHz, a minimum $|S_{11}|$ of -9.1 dB, a minimum NF of 6.4 dB, an IIP₃ of 10.67 dBm while drawing 12 mA of current from a 1.8 V supply. It was observed during measurements and verified by electromagnetic (EM) simulations that the performance of the load inductor was degraded due to its increased parasitics to substrate which resulted in a degradation in the measured power gain performance compared to post-layout simulations. With the demonstrated voltage gain performance, the LNA is suitable for direct sequence (DS) UWB applications that operate in the lower band (i.e. 3.1-5.15 GHz).

The main contributions of this work include: i) the implementation of a single stage frequency-controlled feedback LNA in the CMOS technology that spans the entire UWB spectrum; ii) the analysis of Miller's multiplication factors and their variation with frequency which was exploited to facilitate the wideband power and noise matching with minimum passive components added at the input of the amplifier; iii) the analysis for the equivalent two-port noise representation of the amplifier which illustrated how the optimum signal source susceptance needed for ultra-wideband noise matching has been modified by the proposed topology and how it could be approximated by a single passive component.

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to Tay and Joy

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Chapter 1

Introduction

1.1 Motivation

Wireless telecommunication integrated circuits have been gaining substantial attention from both academia and industry. High-speed wireless communication is becoming common in the context of data transfer schemes.

Ultra-wideband (UWB) wireless technology uses low-power ultra-short pulses to convey information. These sub-nano-second pulses cover a large absolute bandwidth that directly translates into high transfer data-rates that vary between 110 Mbps and 1 Gbps within ranges of 10 meters and 1 meter, respectively. The robustness against multipath fading, the centimeter-range detection resolution and the low-complexity transceiver made UWB technology a potential candidate for applications that range from military-oriented (e.g. Radars and localizers) to indoor consumer electronics' applications (e.g. Wireless Personal Area Networks).

In designing UWB radio receiver front-ends that operate near the noise floor of narrow-band receivers, focus is put on the low noise amplifier (LNA) because it is the first stage that follows the antenna and hence has a strong influence on the signal-to-noise

ratio (SNR) propagating through the subsequent receiver stages. While considerable research into narrow-band LNA design techniques exists, development of UWB LNA design techniques is still underway, especially for designs targeting low-cost processes like CMOS. Achieving a flat gain and a constant group delay while maintaining simultaneous optimum noise and power matching over an ultra-wide bandwidth are the main design challenges. Successful designs that cover the whole band have been reported in GaAs MESFETs [9–11] and more recently in SiGe BiCMOS [12] and CMOS [13]. In [12] and [13], LC ladder structures were exploited to achieve near optimum power and noise matching. The number of lossy passive elements used in high order ladder structures at the input of an amplifier can severely degrade the noise figure. They can also degrade the settling time and the damping behaviour when responding to sub-nanosecond monopulse-based UWB systems. This degradation imposes a challenge on time-domain based correlation and on the reliability of the decision circuit. In [9–11], a controlled feedback technique has been utilized to maintain a flat gain and obtain acceptable input and output matching, but the use of GaAs MESFETs implies a rather expensive process that is not suitable for low-cost consumer electronics [14].

1.2 Thesis Goals

The goal of this research is to explore the design and implementation of an UWB LNA in CMOS $0.18\,\mu\text{m}$ technology. The LNA is desired to have a flat gain, near optimum power and noise matching and constant group delay over the UWB operating bandwidth (i.e. 3.1-10.6 GHz).

1.3 Thesis Outline

The first part of Chapter 2 provides some background information on UWB emission regulations, signal structures and various receiver architectures. The second part provides a literature review of different wide-band amplifier topologies.

Chapter 3 discusses the feedback topology proposed. Transistor noise figure characteristics and trade offs are presented. A graphical design approach is then discussed and applied to design the LNA feedback network. A UWB power matching technique utilizing Miller's effect is explained. Two-port noise analysis and simulations are then presented. The LNA transient response, stability and biasing circuitry are discussed. A transfer function for the amplifier is derived using a two-port network approach to identify open- and closed-loop quantities pertaining to the performance of the LNA.

The LNA layout and implementation details are discussed in Chapter 5. Chapter 6 discusses the DC and RF measurement results of the LNA. The results are correlated with simulations from Chapter 3.

Chapter 7 summarizes the thesis conclusions, research contributions and provides some proposed topics for future work.

A derivation for the relationship between the LNA gain and transconductance utilizing a small-signal transistor model is provided in Appendix A. The derived relationship is used to design for the transistor transconductance in Chapter 3.

The equivalent two-port noise parameters for the LNA are derived in Appendix C. These parameters are used in the noise analysis in Chapter 3 to identify trends and to

describe how the proposed topology transformed the characteristics of the equivalent noisy two-port network of the transistor circuit and how this resulted in minimum additional components needed to achieve UWB simultaneous noise and power matching.

Chapter 2

Ultra-Wideband Technologies

This chapter provides a brief overview of the UWB specifications and emission regulations, modulation schemes and signal structures. It also discusses an example of an impulse radio UWB receiver architecture and the signal power level required at the input for reliable detection.

2.1 Fractional Bandwidth and Ultra-Wideband Systems

The fractional bandwidth of an electromagnetic waveform is given by [1]:

$$\text{Fractional Bandwidth} = \frac{(f_H - f_L)}{(f_H + f_L)/2}, \quad (2.1.1)$$

where, f_H and f_L are the upper and lower frequencies of the -10 dB bandwidth of the emitting source.

The terminology, “Ultra-wideband”, has been used by the Defense Advanced Research Projects Agency (DARPA), and later by the radar community, to refer to a family of radar apparatus. This family of radars adopted carrier-free baseband pulse structures of fractional bandwidths greater than 0.25. The advantages behind the use of these

baseband signals were due to their sharp definition in time and the resulting accuracy in range resolution and enhanced target recognition applications [15]. More recently, devices that operate on signal structures of fractional bandwidths greater than 0.2 or, a minimum bandwidth of 500 MHz have been, generally, designated as ultra-wideband (UWB) devices [1]. The frequency spectrum between 3.1-10.6 GHz has been allocated by the Federal Communications Commission (FCC) [1] to enable indoor wireless transceivers to achieve data rates on the order of 480 Mbps or higher [16]. At the same time, these transceivers will co-exist with narrow band devices that operate within the same bandwidth. The UWB radiators emissions mask as defined by the FCC across this ultra-wide bandwidth in [1] is shown in Fig. 2.1.

Figure 2.1: FCC's emissions mask for radiators up to 12 GHz [1].

Shannon's channel capacity formula is given by [17],

$$C = B \log_2 \left(1 + \frac{S}{N} \right) \quad (2.1.2)$$

where C is the channel capacity in bits per second (bps), B is the transmission bandwidth in Hertz (Hz), S is the signal power in watts, N is the noise power in watts. In (2.1.2), increasing the signal to noise ratio results in an increase in the channel capacity in a logarithmic fashion. On the other hand, wider bandwidths result in a linear increase in the channel capacity and a linear increase in data rates is thus achievable. This is considered one of the strongest motivations behind the use of a wide bandwidth in wireless systems.

2.2 Modulation Schemes and Signal Structures

By generalizing the UWB terminology and not restricting it to a specific transceiver implementation, several techniques were adopted by the UWB community. One approach was to divide the allocated frequency spectrum into sub-bands and to employ orthogonal multi-carrier techniques (e.g. orthogonal frequency division multiplexing (OFDM)) within each sub-band. This technique had the advantage of benefiting from the well-established frequency-domain system- and circuit-level design concepts and implementations.

Another approach adopted the time-domain short-pulse or impulse technique from the UWB radar community. In this technique, a train of pulses is utilized to convey the information symbols. The pulse amplitude, position (in a determined time window) or polarity could be modulated by the information symbols. Also, a combination of any number of these pulse characteristics could be adopted for modulation to increase the number of bits per symbol. This technique also has several advantages including:

- The shorter the duration of the pulse, the wider its bandwidth. For a constant pulse energy, the wider the bandwidth is, the less signal to noise power ratio (SNR)

per frequency [18]. This fact enables the impulse UWB transceivers to successfully coexist with narrow band transceivers while operating at their noise floor.

- Since the pulse can be designed to be sharply defined in time, its energy can be concentrated within a chosen bandwidth. This eliminates the need for a spectrum up/down conversion unlike the narrow band transceivers case. Therefore, the transmitter and the receiver chain could be greatly simplified. This simple architecture eventually translates into low-complexity transceiver and lower power operation [18,19].
- Despite the low transmitted power levels operation regulated by FCC, the short-pulse UWB transceiver inherent robustness against multipath fading in indoor environments was reported in [20]. The experiment was performed in a modern office environment where multipath fading is a known challenge for narrow band transceivers. It was found that for UWB pulses, the received signal energy for every received multipath waveform had a maximum variation of 5 dB upon varying the receiver position within a room. This greatly simplifies the required fading margin in link budgets compared to the narrow-band case. [20].

Several impulse types were adopted in the literature as the underlying signal structure for short-pulse based UWB systems. Examples of such waveforms were root raised cosine RRC [16], chirp signals [21], Hermitian polynomials [22] and Gaussian pulses [23].

In this thesis work, the focus is on the time-domain impulse-based UWB approach due to its low complexity transceiver architecture and reliable performance given low signal

power levels [19].

2.3 Power spectral density (PSD) and Impulses

Among the several signal structures presented, the n^{th} order derivative of the Gaussian monopulse have been suggested for use as the underlying signal structure [19,24,25]. The time domain expression for this family of pulses is given by [24],

$$v^{(n)}(t) = -\frac{n-1}{\sigma^2}v^{(n-2)}(t) - \frac{t}{\sigma^2}v^{(n-1)}(t), \quad (2.3.1)$$

with PSD [24],

$$|P_n(f)| = A_{max} \frac{(2\pi f\sigma)^2 \exp(-(2\pi f\sigma)^2)}{n^n \exp(-n)}. \quad (2.3.2)$$

In (2.3.1) and (2.3.2), n is the order of the derivative of the Gaussian monopulse, σ is the standard deviation and A_{max} is the peak value of the PSD allowed by the FCC (i.e. -41.3 dBm/MHz).

Moreover, it was suggested in [24] that the 5^{th} order derivative of the Gaussian pulse can be adjusted to meet the FCC emissions mask requirements by fixing f in (2.3.2) to be equal to one of the FCC mask corner frequencies (e.g. $f = 10.6$ GHz) and manipulating both σ and n in (2.3.1). As a result, it was adopted here for PSD analysis and its expression has the form [24],

$$v(t) = K \left(-\frac{t^5}{\sqrt{2\pi}\sigma^{11}} + \frac{10t^3}{\sqrt{2\pi}\sigma^9} - \frac{15t}{\sqrt{2\pi}\sigma^7} \right) \exp\left(-\frac{t^2}{2\sigma^2}\right), \quad (2.3.3)$$

with PSD,

$$|Y(f)| = K(2\pi f)^5 \exp\left[-\frac{(2\pi f\sigma)^2}{2}\right], \quad (2.3.4)$$

where, K is a constant used to determine the amplitude of the Gaussian pulse such that its PSD meets the FCC indoor emissions spectral mask in Fig. 2.1. The 5th order derivative of the Gaussian pulse using $\sigma = 51$ ps [24] is shown in Fig. 2.2.

By choosing K and estimating the corresponding PSD of the impulse, an impulse am-

Figure 2.2: A Gaussian monopulse of the fifth order derivative.

plitude of 120 mV peak to peak was found to satisfy the FCC emissions mask when ideal antenna performance and normalized impedances are assumed. The PSD of the 5th derivative of the Gaussian pulse was then plotted against the FCC mask in Fig. 2.3. In Fig. 2.3, the power spectral density of both, the Gaussian pulse and the FCC power emissions mask, were normalized to the peak UWB indoor emission allowed by the FCC, i.e. -41.3 dBm/MHz [1, 24].

The other pulse types, including the lower order Gaussian pulses could also be used however, a frequency shift is needed so that the spectrum of these pulses fits between

Figure 2.3: Normalized PSD of a single Gaussian monopulse of the 5th order derivative versus the FCC emission mask for indoor wireless transceivers.

3.1 GHz and 10.6 GHz. This implied the need for a carrier frequency to perform frequency shifting of the pulse spectrum content. Therefore, traditional heterodyning would still be required negating the trend of less complex, carrierless transceivers. The advantage behind the 5th order derivative is that it covers the entire bandwidth between 3.1 GHz to 10.6 GHz allocated for indoor communication [24]. This eliminated the need for any frequency shifting. This advantage preserved the carrierless principle behind the use of pulse-based signal structure UWB transceivers.

The information will be conveyed by using a sequence of modulated Gaussian impulses with a certain pulse repetition frequency (PRF). The PSD of an unmodulated train of impulses is shown in Fig. 2.5 where the normalized power density exceeded the FCC emissions mask. Furthermore, the spikes made the impulses appear as narrow band interferers to other narrow band systems that share the spectrum (e.g. 802.11a,b). This

Figure 2.4: A portion of a train of gaussian monopulses (5^{th} order derivative) with randomly reversing polarity.

means that despite the fact that the PSD of a single impulse satisfies the FCC emissions mask, it is not a sufficient condition to guarantee that the train of impulses meet the FCC emission mask requirements. However, a polarity modulated impulse train can satisfy the FCC indoor emissions mask. This emphasizes that the type of modulation, the pulse repetition frequency (PRF) and the pulse amplitude influence the PSD of the train of pulses. A portion of the polarity modulated pulse train is shown in Fig. 2.4 and the PSD is plotted against the FCC emissions mask in Fig. 2.6. It was found that modulating the polarity of the pulses by a random sequence had the greatest effect on reducing the magnitude of the spikes in the PSD plot giving rise to a more “noiselike” spectrum as shown in Fig. 2.6.

2.4 An Impulse Radio UWB Receiver Architecture

The low SNR per frequency positions the UWB transceiver operating power levels at the noise floor of the narrow band transceivers that share part of the frequency spectrum [18].

Figure 2.5: Normalized PSD of a unmodulated train of Gaussian impulses (5th derivative) and a single impulse versus the FCC emission mask for indoor wireless transceivers.

While this is an advantage from the coexistence point view point, it is a challenge to design receivers that possess suitable signal power sensitivity levels.

For uncoded information symbols, the symbol energy to noise spectral density ratio is given by:

$$\frac{E_s}{N_0} = \frac{P_{av} T_p}{N_0} \left(\frac{\text{watt} \cdot \text{second}}{\text{watt/Hz}} \right) = \frac{P_{sd}}{N_0} \cdot \frac{B_s}{B_p}, \quad (2.4.1)$$

where, E_s is the energy per symbol, N_0 is the noise power spectral density, P_{av} is the average transmitted power, P_{sd} is the power spectral density limit specified by the FCC, B_s is the symbol bandwidth and B_p is pulse repetition frequency (PRF). In (2.4.1), for a fixed P_{av} , the SNR for an information symbol can be increased in two ways. One way is to decrease the B_p which can be done by lowering the PRF. This means that the pulse rate is traded for more SNR. Another way to increase the SNR is to make B_s larger. This

Figure 2.6: Normalized PSD of a train of Gaussian monopulses (5th derivative) with a randomly reversing polarity versus the FCC emission mask for indoor wireless transceivers.

can be accomplished by increasing the frequency content of an impulse [19].

The ratio B_s/B_p can be interpreted as the pulse processing gain [19]. The larger the pulse processing gain is, the higher the SNR that can be achieved for a fixed average transmitted power spectral density. This is the main advantage behind adopting the impulse UWB technique. This advantage enables transceivers to operate at a low power level relative to the channel noise and the front-end components self noise [19, 24].

2.5 Correlation Receiver Theory

The correlation type receiver is used to detect impulses in an additive white Gaussian noise (AWGN) channel. Signals or vectors correlation is an operation by which the degree of similarity between two signals (or vectors) is evaluated. The degree of similarity between two signals $x(t)$ and $y(t)$, can be evaluated by a measure named *correlation coefficient*,

c_n , given by [26],

$$c_n = \frac{1}{\sqrt{\mathcal{E}_x}\sqrt{\mathcal{E}_y}} \int_{\tau_1}^{\tau_2} x(t)y(t)dt, \quad (2.5.1)$$

where, $\mathcal{E}_x$ and $\mathcal{E}_y$ are the corresponding signal energies for $x(t)$ and $y(t)$, respectively. In (2.5.1), the correlation integral is normalized by the respective signal energies so that the computed degree of similarity, c_n is independent of the magnitude of the two signals under comparison. By using the Schwarz inequality, the correlation coefficient values is bounded to [21,26]

$$-1 \leq c_n \leq 1. \quad (2.5.2)$$

In (2.5.2), $c_n = 1$ corresponds to a full similarity between the two signals or impulses under comparison. $c_n = -1$ indicates a similarity with phase reversal. $c_n = 0$ indicates complete irrelevance over the time of observation.

Fig. 2.7 shows a high level block diagram of a correlation based receiver. The signal energy received by the antenna is filtered by a bandpass filter (BPF) to limit the noise bandwidth and the interference from other emitters. The received signal is then amplified by a low-noise amplifier (LNA). The LNA is designed to amplify the signal while adding the minimum possible noise. The output of the LNA is then fed into a correlation demodulator and a decision circuit.

A single stage correlation demodulator consists of a multiplier followed by an integrator. One of the multiplier inputs is a coherent reference signal to be supplied locally at the receiver by means of a pulse train generator synchronized with the transmitter. The received signal, $r(t)$, is then multiplied by the locally generated pulse template and the

Figure 2.7: A high level architecture of an impulse UWB style receiver.

output gets integrated over the impulse period, T .

In Fig. 2.7, a bank of correlators is used. The total number of correlators required depends on the modulation scheme chosen (e.g. Binary or M-ary PSK or FSK ...etc). In a system where a set of M bi-orthogonal signals are to be sent, a bank of $(M/2)$ correlators (i.e. half the number of signals) is required. The set of coherent impulses to be supplied locally to the correlators are chosen to be a set of $M/2$ out of the M bi-orthogonal signals. If $r(t)$ is the input to the bank of $M/2$ correlators in Fig. 2.7 and $s_j(t)$, where $j = 0, 1, \dots, (M/2) - 1$, are the set of bi-orthogonal coherent impulses, the outputs of the impulse correlators, r_j , where $j = 0, 1, \dots, (M/2) - 1$, are given by,

$$r_j = \int_0^t r(t)s_j(t)dt; \quad 0 \leq t \leq T, \quad j = 0, 1, \dots, (M/2) - 1. \quad (2.5.3)$$

Since the received signal is

$$r(t) = s_i(t) + n(t); \quad 0 \leq t \leq T, \quad j = 0, 1, \dots, (M/2) - 1, \quad (2.5.4)$$

we have

$$\begin{aligned} \mathbf{r}_j &= \int_0^T s_i(t)s_j(t)dt + \int_0^T n(t)s_j(t)dt; \quad i = 0, 1, \dots, M-1, j = 0, 1, \dots, (M/2)-1, \\ &= \begin{cases} \int_0^T s^2(t)dt + n_j; & i = j \\ n_j; & i \neq j, |i-j| \neq \frac{M}{2} \\ -\int_0^T s^2(t)dt - n_j; & |i-j| = \frac{M}{2} \end{cases} \end{aligned} \quad (2.5.5)$$

$$= \begin{cases} \mathcal{E} + n_j; & i = j \\ n_j; & i \neq j, |i-j| \neq \frac{M}{2} \\ -(\mathcal{E} + n_j); & |i-j| = \frac{M}{2} \end{cases} \quad (2.5.6)$$

where,

$$n_j = \int_0^T n(t)s_j(t)dt; \quad j = 0, 1, \dots, (M/2)-1 \quad (2.5.7)$$

$$\begin{aligned} \mathcal{E} &= \int_0^T s_i(t)s_j(t)dt; \quad i = j = 0, 1, \dots, M/2-1 \\ &= \int_0^T s^2(t)dt. \end{aligned} \quad (2.5.8)$$

In (2.5.6) and (2.5.7), $\mathcal{E}$ denotes the energy of a single impulse. From (2.5.6), it is noted that when the i^{th} correlator correlates a template with its corresponding received impulse buried in noise, its output will be the energy of that template plus noise. The output of all the other $(M/2) - 1$ correlators will be only noise. The noise components at the output of the correlators are Gaussian with zero mean and variance [27]

$$\sigma^2 = \frac{\mathcal{E}N_0}{2}. \quad (2.5.9)$$

The outputs of the correlators, $\mathbf{r}_j$, are then fed into a detector stage. The detector stage observes the correlator outputs and decides which symbol was transmitted. First, the detector compares the $(M/2)$ correlators outputs based upon their absolute values, $|\mathbf{r}_j|$, and the largest is selected. The detector then decides upon which symbol was transmitted

according to the sign of the selected correlator output, r_j . $s_j(t)$ is selected if $r_j > 0$ and $-s_j(t)$ is selected if $r_j < 0$. [27, 28].

The signal-to-noise-power ratio (SNR) presented at the input of a single correlator stage directly influences its output and consequently the symbol error rate. Therefore, for a complete transceiver, it is useful to have an estimate of the minimum required input SNR for a reliable correlation operation. In [27, 28], the bit signal-to-noise ratio, E_b/N_0 , required to achieve a probability of symbol error around 10^{-3} in a 4 bi-orthogonal system is approximately 7.5 dB. In this case, an ideal mathematical correlation operation is assumed where the correlator circuit non-idealities are ignored.

Given the theoretical bit SNR of 7.5 dB required to achieve 10^{-3} probability of symbol error in [27, 28], the output SNR required for a bit rate, R_b , of 110 Mbps with an impulse bandwidth, B , of 6.6 GHz is given by [24],

$$SNR_{required} = \frac{E_s/T_s}{N_0 B} = \frac{E_s R_s}{N_0 B} = \frac{E_b}{N_0} \cdot \frac{R_b}{B}. \quad (2.5.10)$$

And assuming a link margin, LM , of 5 dB [19, 24],

$$\begin{aligned} SNR_{dB} &= SNR_{required} + LM, \\ &= 7.5 + 10 \log_{10}(110 \times 10^6) - 10 \log_{10}(6.6 \times 10^9) + 5 \text{ dB} \\ &\approx -5.3 \text{ dB}. \end{aligned} \quad (2.5.11)$$

A minimum correlator output SNR of -5.3 dB is used in the calculations presented later.

Given this theoretical lower bound on the SNR that should be presented at the correlator output and assuming a specific total noise figure for the combined front-end building blocks, i.e. BPF, LNA and correlator stages in Fig. 2.7, the relation between the SNR at the output of the correlator, $(S/N)_{\text{correlator}_{\text{out}}}$, and the SNR at the input of the BPF, $(S/N)_{\text{BPF}_{\text{in}}}$ is given by,

$$\frac{S}{N}_{\text{correlator}_{\text{out}}} = \frac{S}{N}_{\text{BPF}_{\text{in}}} - NF_{\text{total}}, \quad (2.5.12)$$

where, NF_{total} is the combined noise figure of the BPF, the LNA and the correlator in dB and it is given by [29],

$$NF_{\text{total}} = F_{\text{BPF}} + \frac{F_{\text{LNA}} - 1}{G_{\text{BPF}}} + \frac{F_{\text{correlator}} - 1}{G_{\text{BPF}}G_{\text{LNA}}}. \quad (2.5.13)$$

In (2.5.13), F_{BPF} , F_{LNA} and $F_{\text{correlator}}$ are the noise figures of the BPF, the LNA and the correlator. G_{BPF} , G_{LNA} are the power gains (or attenuations) of the BPF and the LNA, respectively. It is noted that the noise figure of the BPF can be interpreted as a signal power loss [30]. Assuming a -3 dB for the BPF attenuation, an LNA with a gain of 10 dB and an average noise figure of 2.5 (4 dB) [16], a correlator with a noise figure of 10 dB [31] and a bandwidth of 6.6 GHz, expression (2.5.13) gives,

$$NF_{\text{total}} = 2 + \frac{2.5 - 1}{0.5} + \frac{10 - 1}{0.5 \times 3.16} \approx 10.7. \quad (2.5.14)$$

The required signal power level at the input of the BPF, $S_{\text{BPF}_{\text{in}}}$, such that the theoretical minimum SNR is available at the correlator output is given by:

$$S_{\text{BPF}_{\text{in}}} = \text{Noise Floor} + \frac{S}{N}_{\text{correlator}_{\text{out}}} + NF_{\text{total}}, \quad (2.5.15)$$

where,

$$\text{Noise Floor} = 10 \log_{10}(KT) + 10 \log_{10} B. \quad (2.5.16)$$

In (2.5.16), K is the Boltzmann's constant, T is the room temperature in Kelvin and B is the impulse -10 dB-bandwidth (4 - 10.6 GHz) [1]. We have,

$$\begin{aligned} \text{Noise Floor} &= -173.8 \text{ dBm} + 10 \log_{10}(6.6 \times 10^9) \\ &= -75.6 \text{ dBm}. \end{aligned} \quad (2.5.17)$$

Substituting from (2.5.14) and (2.5.17) in (2.5.15) we have:

$$S_{BPF_{in}} = \text{Noise Floor} + \frac{S}{N_{correlator_{out}}} + NF_{total}, \quad (2.5.18)$$

$$= -75.6 \text{ dBm} - 5.3 \text{ dB} + 10.3 \text{ dB} \approx -70.6 \text{ dBm}. \quad (2.5.19)$$

Therefore, a minimum theoretical signal power level of -70.6 dBm should be represented at the input of the BPF. This power level should, in theory, guarantee that the correlation stage delivers higher output SNR than required to guarantee a probability of symbol error on the order of 10^{-3} .

2.6 Non-Linearity Effects on Correlation Coefficient

The effects of the total non-linearity in the receiver building blocks up to the correlator on the output correlation coefficient were investigated in this section. A fifth-order derivative of a Gaussian monopulse was fed into a nonlinear block represented by a power series with constant and real coefficients:

$$i_o = k_0 + k_1 v_{in} + k_2 v_{in}^2 - |k_3| v_{in}^3, \quad (2.6.1)$$

where v_{in} is the Gaussian monopulse input voltage. k_1 was assumed constant and equivalent to a nominal transistor transconductance (e.g. 0.067 A/V). A typical range for the input-referred intercept points IIP_2 and IIP_3 due to harmonic distortion was chosen (e.g. -15 to 5 dBm). For each value of IIP_2 and IIP_3 , k_2 and k_3 values were generated for a $Z_0 \Omega$ system based expressions (2.6.2)-(2.6.5).

$$k_2 = \alpha_1 \frac{k_1}{IIP_2} \quad (2.6.2)$$

$$k_3 = \alpha_2 \frac{k_1}{IIP_3^2} \quad (2.6.3)$$

Where,

$$IIP_2 = 10 \log \frac{v_{in,IIP_2}^2 / Z_0}{1 \text{ mW}} \quad (2.6.4)$$

$$IIP_3 = 10 \log \frac{v_{in,IIP_3}^2 / Z_0}{1 \text{ mW}} \quad (2.6.5)$$

It is noted that IIP_2 and IIP_3 in (2.6.4) and (2.6.5) are in dBm units. α_1 and α_2 are 2 and 4, respectively [32]. The output of the non-linear block was correlated with the input ideal Gaussian monopulse. The output correlation coefficient is plotted versus IIP_2 and IIP_3 in Fig. 2.8. It is noted that the correlation coefficient output is more sensitive to degradation in IIP_3 than it is for IIP_2 beyond -10 dBm.

2.7 Wideband Amplifiers

The function of a wideband LNA is to provide flat gain and constant group delay while possessing a low noise figure over a wide bandwidth. Depending on the application, the amplifier may be required to have its input and output impedances matched to 50Ω . This section discusses the various topologies of UWB LNA circuits.

Figure 2.8: The effect of input-referred second and third order intercept power levels due to harmonic distortion on the correlation coefficient. The correlation coefficient output is shown to be more sensitive to degradation in IIP_3 than IIP_2 for IIP_3 power levels less than -10 dBm

Wideband amplifier topologies include: i) Balanced amplifiers [33], ii) lossy matched [34], iii) Actively matched amplifiers [35,36], iv) Reactively matched amplifiers [34], v) Feedback amplifiers [4,37], vi) Additive gain or distributed amplifiers (DA) [34,38,39] and vii) Multiplicative gain or cascaded amplifiers [3,40].

2.8 Balanced Amplifiers

Balanced amplifiers are generally known for their flat gain and good input and output matching across a bandwidth close to two octaves [33,41,42]. A balanced low noise amplifier topology employs two 90° couplers to split the input power between, and combine the output power from, two theoretically-identical amplifiers connected as shown in Fig. 2.9. Each amplifier is mismatched for constant gain and low noise performance. The remaining, in-phase, input and output reflections are absorbed at the input and output couplers resistive terminations, respectively. While the couplers bandwidths limit the broadband performance and integration, the resistive termination degrades the noise performance. The redundant structure also translates into double the power consumption and the area.

Figure 2.9: A balanced amplifier arrangement. Input and output couplers with resistive terminations are used at the input and at the output to absorb the input and output reflections. The two dotted boxes represent the two 90° couplers used in this configuration.

Lossy matched amplifiers employ a resistive termination at the input of the network so that a frequency independent matching is obtained. This technique is not preferred in low noise amplifiers due to its direct impact on the noise figure performance. This impact has two aspects; first is the equivalent noise generator of the resistive load that appears at the input of the amplifier. Second is the resulting input signal division which counts

as a signal attenuation and hence a signal-to-noise ratio degradation [43].

2.9 Actively Matched Amplifiers

Successful actively matched amplifier designs employing the common gate topology have been reported in the literature [35,36]. The absence of Miller's multiplication effect on C_{gd} gives this topology the potential for wideband performance. Impedance matching could be achieved by designing for $1/g_m = 50\Omega$. However, the parasitic capacitances, C_{gs} , C_{sb} , C_{db} and C_{dg} have to be resonated out. Source and drain inductors of a common gate transistor were used to resonate out the parasitic capacitances at the transistor source and drain areas, respectively in [35,36]. The noise performance of a common gate topology ignoring the induced gate noise has a lower bound given by $F \geq 1 + \gamma/\alpha$ [35, 36, 38] where, γ is 0.67-1.1 [44] and α is g_m/g_{d0} . Under perfect input matching condition, this lower bound in the short channel regime ($\alpha < 1$) is 4.8 dB [38] and it is expected to degrade further if the induced gate noise is taken into consideration [38,45]. A resistive feedthrough topology between the source and drain was exploited [35] in an effort to create a new lower bound than $1 + \gamma/\alpha$ at a single operating frequency. It has also been noted that the capacitive coupling between the source and drain terminals through the substrate coupling network degrades the noise and stability performance for this topology [35]. A shunt inductance between the transistor source and drain terminals has been proposed to mitigate this problem at a single operating frequency (i.e. narrowband) [35, 46]. The resulting noise figure was 6 dB at 24 GHz. Therefore, despite the potential for a wideband power matching performance (if wideband resonance techniques are introduced

to counteract the parasitics), the wideband noise performance can still be a significant drawback.

2.10 Reactively Matched Amplifiers

Wideband reactively matched amplifiers employ input and output impedance matching networks to attain acceptable power and noise matching as well as constant gain and group delay across a predetermined bandwidth. Due to the classical intrinsic gain roll-off of a transistor at high frequencies, i.e. ($|S_{21}|^2$), the employed matching networks are expected to possess complementary transfer functions across the usable bandwidth [34]. Simultaneously achieving broadband power and noise matching and gain roll-off compensation is not theoretically possible by a single matching network [34]. This is due to the fact that a gain roll-off compensation network reflects power at lower frequencies to achieve gain leveling. This, in turn, comes at the expense of higher input reflections. In [2], a com-

Figure 2.10: A tuned lossy matched broadband amplifier [2]

bination of lossy and lossless matching networks were simultaneously utilized. The lossy matching network was introduced at low frequencies to reflect power and hence achieve gain leveling. At microwave frequencies, the lossy networks were transformed to high impedances to become theoretically negligible and the lossless matching network becomes dominant as shown in 2.10. A constant gain of 19 dB with 50 ps step response across a

bandwidth between 0.8 MHz and 8.5 GHz (13.5 Octaves) from a two stage amplifier [2]. The reported noise figure in [2] was between 7.5-10 dB due to the same reasons argued in the lossy matched amplifier case. The amplifier draws a 60 mA of current from a 3 V supply making this topology not attractive for low power applications.

In [13], an LC ladder input matching structure employing the input impedance of the active device as part of the structure was exploited to achieve near optimum power and noise matching. The gain leveling in this case was achieved via an output shunt peaking approach. The losses associated with the passive elements in high order ladder structures at the input of an amplifier can severely degrade the noise figure [13, 34]. LC ladder networks may also degrade the settling time and the damping behaviour when responding to sub-nanosecond monopulse-based UWB systems. This degradation imposes a challenge on time-domain based correlation and on the reliability of the back-end decision circuit.

2.11 Feedback Amplifiers

Feedback design techniques that cover wide bandwidths have been previously reported in GaAs MESFETs [9–11]. In [9–11], a controlled feedback technique has been utilized to maintain a flat gain and obtain acceptable input and output matching, but the use of GaAs MESFETs implies a rather expensive process that is not suitable for low-cost consumer electronics. Feedback amplifiers are discussed in more details in chapter 3.

A multi-stage amplifier with global feedback is reported in [37]. The open-loop gain becomes less than unity for a perfect matching condition i.e. $Z_{in} = R_{FB}/(1 + A_v)$ [4]. This resulted in a poor closed-loop linearity performance especially if the gain of the

first stage is made large enough to achieve good noise performance [4, 37]. Stability was another major concern due to the global feedback around multiple gain stages. Power consumption is a penalty by the choice of the multi-stage topology.

2.12 Distributed Amplifiers

In a constant gain-bandwidth product system, favoring the gain comes at the expense of the bandwidth [34, 38, 39]. For a common source amplifier topology, increasing the size of the transistor gate width to realize more gain would augment the size of gate-source and gate-drain, source and drain junction capacitances. This effect will influence the location of the dominant poles rendering a narrower bandwidth amplifier. Splitting the required transistor gate width into several transistors, the gain can be achieved in an additive manner. Artificial transmission lines (ATL) can be built around the input and the output parasitic capacitances of the smaller transistor sections. The RF input signal travels down the input ATL (i.e. the gate line) exciting the gates of the transistors. The RF output from all transistors travel on the drain line while adding constructively toward the load termination and destructively toward a dummy load as is shown in Fig. 2.11. The operating power gain of a DA with N gain stages and a transconductance g_{m0} per stage is given by [34]:

$$G_p = \frac{g_{m0}^2 Z_{0G} Z_{0D}}{4} \frac{[\exp(-\alpha_G N l_g) - \exp(-\alpha_D N l_d)]^2}{(\alpha_D l_d - \alpha_G l_g)^2} \quad (2.12.1)$$

$$\begin{aligned} G_p|_{(\alpha_G N l_g) \ll 1} &\approx \frac{1}{4} (N g_{m0})^2 Z_{0G} Z_{0D} \\ G_p|_{(\alpha_D N l_d) \ll 1} &\approx \frac{1}{4} (N g_{m0})^2 Z_{0G} Z_{0D} \end{aligned} \quad (2.12.2)$$

In (2.12.1) and (2.12.2), Z_{0G} and Z_{0D} are the characteristic impedances, α_G and α_D are the attenuation constants per unit length, l_d and l_g are the electrical lengths of the microstrip

Figure 2.11: An N-stages distributed amplifier [2].

sections of the gate and drain lines, respectively. It is noted that the operating power gain in this topology is directly proportional to the square of the number of gain stages. In [47], a distributed amplifier was reported with a gain of 10.6 dB, NF of 3.4-5.4 dB across a bandwidth between 0.5 GHz and 14 GHz consuming 52 mW of power. Power consumption and chip area are the main shortcomings in this case. Other performance challenges arise in this topology due to several facts. The large bias current that flows through the load resistors gives rise to a trade-off between the achievable voltage gain and the allowable voltage headroom [39]. The additive gain nature of this topology leads to an increasing Miller multiplication effect on gate-drain capacitance as the output signal propagates from left to right. This effect lowers the characteristic impedance and the phase velocity of the gate ATL [39]. As a result, phase velocity mismatches occur between the gate and drain ATL's leading to gain ripples in the DA frequency response.

2.13 Multiplicative Gain Amplifier

A multiplicative gain amplifier topology was reported in GaAs MESFETs [40] and in CMOS [3]. In this topology, unlike the DA, gain cells are cascaded such that the output from one gain stage is the input to the next gain stage. Fig. 2.12 depicts the multiplicative architecture. The gain in this topology with N stages is given by [3, 40]

Figure 2.12: An N -stages cascaded distributed amplifier [3]

$$G_p = \frac{1}{4} g_{m0}^{2N} Z_{int}^{2(N-1)} Z_0^2, \quad (2.13.1)$$

where, Z_{int} is the interstage characteristic impedance and Z_0 is the system impedance. It is noted that the operating power gain grows exponentially with $2N$, a great advantage over the additive topology. Unlike the DA, the voltage head room is decoupled from the total bias current because each stage is biased independently. A gain of 21 ± 0.5 dB up to 5 GHz with a power consumption of 132 mW in a $0.35 \mu\text{m}$ process was reported in [3]. The main disadvantage is expected to be the noise figure because of the interstage resistive or passive elements' terminations. The noise generated by the resistive termination in stage i is expected to propagate through the subsequent $N - i$ stages degrading the overall noise performance of the amplifier. The power consumption is a concern in this topology.

2.14 Noise Cancelling Techniques

The destructive addition of noise voltage quantities has been exploited in the literature [4, 48]. In [4], and as is shown in Fig. 2.13, a negative feedback was used to obtain a wideband gain performance and a simultaneous noise and power matching [9]. Repositioning the

Figure 2.13: A feedback amplifier topology adopting a noise canceling technique [4]

optimum source impedance needed for noise matching such that it is closer to the necessary impedance for power matching, to a first order, is a benefit of adopting feedback topologies [6,9,49]. Part of the noise that was generated by the main amplifier and fed back to the input node was then amplified by an additional amplifier, “ A_2 ”, optimized for minimum noise performance. The amplified noise quantity has an opposite sign relative to that at the output of the main amplifier. The two noise quantities were made to add destructively such that noise is theoretically nullified. The required gain, A_v , such that “ A_2 ” should have to achieve noise cancelation at the output is given by:

$$A_v \approx 1 + \frac{R_{FB}}{R_s} + sC_{in}R_{FB}$$

where C_{in} is the effective input capacitance, R_{FB} and R_s are as shown in Fig. 2.13. The main limitation in this technique, however, is the degradation in noise canceling process

as frequency increases [4]. This made the technique effective at dc and low frequencies [4]. Another important limitation is that although the noise contribution of the second amplifier, “ A_2 ”, can be mitigated using a relatively high transconductance, this would still involve higher power dissipation and narrower bandwidth performance penalties due to the increased device size. If this technique is to be adopted for UWB amplifiers, the two amplifier stages (i.e. the main amplifier and the noise canceling amplifier) would have to be capable of achieving the UWB bandwidth requirement (3.1-10.6 GHz). More importantly, the noise canceling principle would have to still be effective over this wide range of frequencies.

2.15 Summary

In this Chapter, the UWB emission regulations were briefly discussed. The PSD of the fifth-order Gaussian monopulse was investigated for a single pulse, an unmodulated and a modulated train of pulses. It was shown that the polarity modulation kept the PSD of the train of impulses below the FCC emission mask while still achieving the same bit rates as in the unmodulated case for a constant PRF. It was also shown that for 110 Mbps correlator receiver architectures, a minimum theoretical signal power level of -70.6 dBm is required at the input of the BPF to achieve a probability of symbol error of 10^{-3} . Section 2.7 discussed different wide-band amplifier circuit topologies from the literature as possible candidates for a UWB LNA. The effect of non-linearity on correlation coefficient was investigated. It was shown that an ideal correlation coefficient output is more sensitive to IIP_3 than IIP_2 for IIP_3 levels below -10 dBm.

Chapter 3

Feedback Low-Noise Amplifiers

3.1 Introduction

The motivation toward the feedback amplifier topology stems from the advantages that it offers in terms of ultra-wideband flat gain, insensitivity to process variations which can be significant over such a wideband in the open-loop case and finally, the input and output impedances adjustment which makes the matching a simple task to achieve [34]. However, since the feedback topology introduces the idea of trading off the gain for bandwidth, it is often recommended for use with devices with high transconductance characteristics such as GaAs MESFETs. So, it comes as no surprise that most of the ultra-broadband feedback circuits reported to date deploy GaAs MESFETs as the amplifier raw device [41]. The CMOS process, however, offers quite acceptable transistor transconductance levels, although is not quite as high as GaAs MESFETs, but still good enough to make CMOS devices suitable candidates for such an amplifier topology.

The following advantages make the choice of feedback amplifiers attractive:

- The potential for broadband performance in a constant gain-bandwidth product (GBWP) system [38].

- The dependance on S-parameter variations of FET transistors is minimized
- The ability to modify the input and output impedances which not only aids wide-band power matching [50], but enables simultaneous noise and power matching [49].
- The sensitivity to Γ_{opt} is reduced which is a very crucial parameter for low-noise design
- Improved non-linearity performance [5] making the amplifier attractive for time-domain based correlation UWB systems.

3.2 Feedback Amplifiers

In Fig. 3.1 a dual feedback wideband gain stage is shown. Following the analysis outlined in [50], it is shown in Appendix A that the Z_S needed to achieve ideal Γ_{in} and Γ_{out} in the unilateral case can be approximated by:

$$Z_S|_{S_{11}, S_{22}=0} \approx \frac{Y_{FB}}{Y_0^2} - \frac{1}{g_m + Y_{DS}} \quad (3.2.1)$$

where, Y_{DS} is the transistor's drain-source admittance, g_m is the transistor intrinsic transconductance and $Y_0 = 1/Z_0$. In (3.2.1), g_m has a lower bound so that Z_S can

Figure 3.1: A shunt series feedback amplifier.

be realized. When solving for a g_m that achieves the minimum Z_S , we get:

$$g_m|_{S_{11}=S_{22}=0} = \frac{Y_0^2}{Y_{FB}} - Y_{DS} \approx \frac{Y_0^2}{Y_{FB}}. \quad (3.2.2)$$

This leads to the forward transmission coefficient given in terms of the minimum g_m by:

$$S_{21}|_{S_{11}=S_{22}=0} \approx 1 - \frac{g_m}{Y_0}. \quad (3.2.3)$$

Given a specific S_{21} , g_m can be obtained from (3.2.3). If the feedback network admittance, Y_{FB} , is chosen such that it is purely real, negative feedback is obtained where the open-loop gain can be traded for more closed-loop bandwidth or less delay. The resulting closed-loop transimpedance is given by:

$$\frac{v_{out}}{i_{in}} = -\frac{A_{OL}}{1 + A_{OL}Y_{FB}} \approx -\frac{1}{Y_{FB}} \Big|_{A_{OL}Y_{FB} \gg 1}, \quad (3.2.4)$$

where,

$$A_{OL} = \frac{G_m - Y_{FB}}{(Y_{ds} + Y_0)(sC_{gs} + Y_0)}. \quad (3.2.5)$$

and

$$G_m = g_m / (1 + g_m Z_s). \quad (3.2.6)$$

At the frequency where the transistor's parasitics become significant, the approximation made in (3.2.4) ceases to be valid and hence limits the achievable flat gain bandwidth for a purely real Y_{FB} network. If Y_{FB} is designed such that it compensates for the degradation in A_{OL} as frequency increases, a flat gain can be obtained over a wider frequency range as will be shown in section 4.2.

3.3 Noise Figure trade-offs

The equivalent impedance of the UWB antenna is expected to vary significantly along the entire band of interest. According to [51], however, in designing broadband low-noise amplifiers, the design process should focus on de-sensitizing the noise matching of the amplifier to variations of the source impedance. Therefore, the focus should be on the two-port noise equivalent parameters which are responsible for making the noise match insensitive to such antenna impedance variations. In Appendix B, it is shown that the intrinsic noise sources of a transistor can be represented by a two-port noiseless network preceded by a noise voltage source $\overline{e_n^2} = 4KTBR_n$, an uncorrelated noise current source $\overline{i_u^2} = 4KTBG_u$, and a correlation admittance $Y_{cor} = G_{cor} + jB_{cor}$ on its input side as shown in Fig. 3.2. R_n is the equivalent noise resistance, G_u is the uncorrelated equivalent noise conductance, G_{cor} and B_{cor} are the correlation conductance and susceptance, respectively. As discussed in Appendix B, these parameters are given by [38],

$$R_n = \frac{\overline{e_n^2}}{4KT\Delta f} = \frac{\gamma g_{d0}}{g_m^2}, \quad (3.3.1)$$

$$G_u = \frac{\omega^2 C_g^2}{5g_{d0}} \delta (1 - |c|^2), \quad (3.3.2)$$

and

$$Y_{cor} = j\omega C_g \left(1 + \frac{g_m}{g_{d0}} |c| \sqrt{\frac{\delta}{5\gamma}}\right). \quad (3.3.3)$$

where, $\alpha = g_m/g_{d0}$, $\delta \approx 1.3 - 4$, $\gamma \approx 0.67 - 2$, $|c| \approx 0.4$ and g_{d0} is the channel conductance at $V_{ds} = 0$ [38, 44, 52].

For a given signal source admittance of $Y_s = G_s + jB_s$, the general formula of the total noise factor, F , of a transistor when represented by its two-port equivalent network is

given by [6],

$$F = F_{min} + \frac{R_n}{G_s} [(G_s - G_{opt})^2 + (B_s - B_{opt})^2] \quad (3.3.4)$$

In (3.3.4), F_{min} is the minimum noise factor, G_{opt} is the optimum signal source conductance, B_{opt} is the optimum signal source susceptance. The equivalent two-port noise

Figure 3.2: Transistor equivalent two-port noise representation

resistance, R_n^T , of the transistor and that of the amplifier circuit, $\hat{R}_n$, is responsible for the sensitivity of the noise match. Constant noise factors can be represented as a group of circles on the Smith chart. The separation of those circles is a function of $\hat{R}_n$. When $\hat{R}_n$ is minimized, the least sensitive noise match to signal source impedance variations is obtained [51].

Despite the ultra-wide bandwidth capability that a feedback configuration can provide, there is a trade-off between the minimum noise figure that can be achieved and the bandwidth due to the losses introduced by the elements constituting the feedback network, Y_{FB} , that contribute to increasing the equivalent $\hat{R}_n$ of the closed-loop amplifier circuit. This directly adds to the sensitivity of the noise match of the amplifier to any monopulse source impedance variations. In choosing the optimum device size for the main amplifying device, the minimum noise figure, the optimum $\hat{R}_n$ and the wide bandwidth performance were the main determining factors. For the UWB case, choosing the optimum $\hat{R}_n$ was equally important to choosing NF_{min} [51]. Therefore, trade-offs were experienced from

the beginning while choosing the device size.

Figures 3.3, 3.4 and 3.5 show measured trends of two-port noise parameters for CMOS $0.18\ \mu\text{m}$ test structures with gate widths $64 \times 2.5\ \mu\text{m}$ and $128 \times 2.5\ \mu\text{m}$ above 1 GHz.

Figure 3.3: Equivalent normalized noise resistance for two transistor test structures at two-different bias conditions.

A trade-off exists between choosing the optimum device size needed to achieve enough gain-bandwidth product and choosing the optimum device size for achieving the minimum noise figure at a certain frequency and a certain current density. The equivalent two-port noise resistance, R_n , for a CMOS device as given by (3.3.1) leads to the conclusion that the sensitivity of the device noise figure to matching is inversely proportional to the transconductance of the device. This means that R_n is inversely proportional to the device gate-width. In short channel devices, measured R_n values in test structures for $0.18\ \mu\text{m}$ technology were observed to have become smaller than those obtained from devices with larger gate lengths [52].

Figure 3.4: Gain for two transistor test structures at two-different bias conditions.

Figure 3.5: Minimum Noise Figure, NF_{min} , for two transistor test structures at two-different bias conditions.

An UWB LNA must possess a flat gain over the entire UWB bandwidth with the lowest possible added noise. This implies that a compromise has to be made in choosing the amplifier device size from the beginning. Therefore, the optimum device for an UWB low noise amplification may not have the minimum possible NF_{min} and the minimum equivalent noise resistance if the required amplification bandwidth is to be attained. To quantify this further, by observing Figures 3.3 and 3.5, choosing the $128 \times 2.5 \mu\text{m}$ will give a lower R_n and NF_{min} however, a degradation in the gain is noticeable beyond 5.9 GHz as shown in Fig. 3.4. Choosing the device size that corresponds to a suitable maximum gain implies a trade off of 0.15 to 0.2 dB of extra NF_{min} . Larger device sizes with less NF_{min} and R_n may negatively impact the bandwidth.

The bandwidth limitation is a result of the gate-to-drain capacitance, C_{gd} . In choosing a large device to maintain enough gain and low noise figure, the size of C_{gd} will degrade the bandwidth performance [5]. One solution is to use a cascode configuration to overcome Miller's multiplication effect but this approach will lead to increased noise figure and power consumption. The overall noise figure of the cascode configuration, especially at high frequencies, was reported to degrade due to the added common-gate device [5, p. 232] [38, 45, 52].

3.4 Summary

In this chapter, the advantages of feedback amplifiers were highlighted. The resistive shunt and series feedback topology was discussed emphasizing the need for a frequency-controlled feedback technique to attain a UWB bandwidth. The transistor noise equivalent two-port network parameters were investigated. The trade-off between choosing the optimum transistor size that achieves a suitable gain-bandwidth product and choosing the optimum size that has the minimum $NF_{\min}$ and R_n was also highlighted.

Chapter 4

LNA Analysis and Design

This chapter discusses the LNA design procedure. It also explains a graphical design approach that was adopted to estimate the feedback network component values. A power and noise matching analysis using Miller's multiplication effect is also presented.

4.1 Design procedure and trade-offs

In designing the feedback low noise amplifier, two techniques were adopted. First, a low frequency model of the chosen topology was investigated to aid choosing the minimum transconductance needed. The gate size of the transistor was chosen to correspond to the required transconductance while possessing an acceptable NF_{min} and bandwidth performance. A two-port network analysis was then followed to obtain expressions describing the open- and closed-loop circuit quantities. A graphical technique for designing feedback microwave transistor amplifiers as outlined in [53] was applied in order to arrive at a first estimate of the feedback network component values. A sequence of s-parameters simulations and optimizations were performed while employing lumped component models that capture high frequency parasitic effects.

Figure 4.1: A small-signal equivalent circuit of the shunt-series feedback of the amplifier

With the conclusion drawn from section 3.2, a frequency-controlled feedback network is needed in order to achieve a flat gain across the UWB bandwidth. For this amplifier topology, the device transconductance and bias conditions were chosen based on an analysis done for a simple transistor model with the chosen feedback topology in Appendix A. The simple model and equivalent circuit was used to initially identify trends and gain design insights.

Fig. 4.1 shows a simple abstract model of the chosen feedback amplifier circuit topology. The abstract model depicts only the important MOSFET components needed to be taken into consideration to arrive at the important design conclusions and highlight trends. The relationship relating the required g_m to the forward transmission coefficient at perfect matching conditions, $S_{11} = S_{22} = 0$, was derived for this circuit in Appendix A to be,

$$S_{21}|_{S_{11}=S_{22}=0} \approx 1 - \frac{g_m}{Y_0}, \quad (4.1.1)$$

where, $Y_0 = 1/Z_0$. In a $50\ \Omega$ system, for an $|S_{21}|^2$ between 8-10 dB, g_m was found from

(4.1.1) to be between 70.2-83 mS. The length of the device is related to the unity current gain frequency, ω_T by [38],

$$\omega_T \approx \frac{3}{4} \frac{\mu_n E_{SAT}}{L}, \quad (4.1.2)$$

where E_{SAT} is the strength of the electric field at which the carrier velocity value drops by one half the extrapolated value from the that of the low-field case. Since the NF_{min} is inversely proportional to ω_T as it is given by [38],

$$F_{min} \approx 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma \delta (1 - |c|^2)}, \quad (4.1.3)$$

the device length, L , was chosen to be the minimum allowed by the technology (i.e. $0.18 \mu\text{m}$) such that it minimizes the noise figure. It is noted that although the relationship in (4.1.2) is independent of the gate overdrive, $V_{gs} - V_t$, this relationship was originally derived based on the assumption that the device is operating in the saturation region which is generally a bias dependent condition [38].

With the conclusions drawn from the discussion in section 3.3, a device width of $64 \times 2.5 \mu\text{m}$ with a minimum gate length of $0.18 \mu\text{m}$ was selected to provide the required transconductance. The $64 \times 2.5 \mu\text{m}$ transistor width was chosen to minimize the parasitic capacitances in order to achieve the bandwidth requirement imposed by the UWB specification. As the operating frequency increases, both the device parasitics and any feedback frequency dependent components come into play. These effects complicate the analysis further. A graphical design technique was used whereby more insight is obtained as will be explained in section 4.2. Since the noise simulation results from the available CMOS $0.18 \mu\text{m}$ models were not valid above 1 GHz, foundry provided fitted empirical

formulae for measured test structures were used instead. Using the following graphical method, a series of simulations were undertaken to achieve gain equalization across the ultra-wideband frequency range.

4.2 A Graphical Design Approach

In order to monitor the magnitude and phase relationships of the amplifier's S_{21} , the graphical design technique outlined in [53] was applied. In this technique, it is assumed that $Y'_{21} \ll Y_{21}^T$, $Y'_{22} \ll Y_{22}^T$ and $Y'_{11} \ll Y_{11}^T$. The transistor model and the feedback network are treated as two separate two-port networks connected in parallel. The S-parameters for the amplifier (i.e. the transistor combined with the shunt feedback network), was derived from the combined Y-parameters of the two networks and shown to be approximated by [53],

$$\frac{2}{S_{21}} \approx \frac{2}{S_{21}^T} + Y'_{12} \quad (4.2.1)$$

$$\frac{2S_{11}}{S_{21}} \approx \frac{2S_{11}^T}{S_{21}^T} - Y'_{12} \quad (4.2.2)$$

$$\frac{2S_{22}}{S_{21}} \approx \frac{2S_{22}^T}{S_{21}^T} - Y'_{12} \quad (4.2.3)$$

$$\frac{S_{12}}{S_{21}} \approx \frac{Y_{12}^T + Y'_{12}}{Y_{21}^T} \quad (4.2.4)$$

where, Y_{ij}^T and Y'_{ij} are the Y-parameters of the transistor and that of the feedback network, respectively. When looking at the S_{21} as a complex number we have:

$$S_{21} = |S_{21}|e^{j\angle S_{21}} \quad (4.2.5)$$

and

$$\frac{2}{S_{21}} = \frac{2}{|S_{21}|}e^{-j\angle S_{21}} \quad (4.2.6)$$

which leads to,

$$\frac{2}{S_{21}} = \frac{2}{|S_{21}|} \cos \angle S_{21} - j \frac{2}{|S_{21}|} \sin \angle S_{21} \quad (4.2.7)$$

When using a complex plane to plot $2/S_{21}$ as a complex number, the square of distance between any point on the complex plane and the origin, R^2 , is given by,

$$R^2 = \left(\frac{2}{|S_{21}|} \cos(\angle S_{21}) \right)^2 + \left(\frac{2}{|S_{21}|} \sin(\angle S_{21}) \right)^2 \quad (4.2.8)$$

and

$$R = \frac{2}{|S_{21}|} \sqrt{\cos^2(\angle S_{21}) + \sin^2(\angle S_{21})} = \frac{2}{|S_{21}|} \quad (4.2.9)$$

Therefore, the loci of $2/S_{21}$ in (4.2.1), when plotted on a complex plane, represents a group of constant $2/S_{21}$ circles centered at the origin with radii $2/|S_{21}|$. To obtain a flat gain, or constant S_{21} , the final $2/S_{21}$ has to align with one of the constant gain circles.

When plotting the left-hand-side of (4.2.1) on a complex plane, one would be plotting the $2/S_{21}^T$ curve with Y'_{12} added to it. The addition of Y'_{12} represents the effect of feedback network on $2/S_{21}^T$ curve. The reverse transmission of the feedback network, Y'_{12} , changes both the location and the shape of the $2/S_{21}^T$ curve on the complex plane. This change depends on what constitutes Y'_{12} . As a design exercise, one would be interested in repositioning $2/S_{21}$ such that it eventually aligns with a desired constant gain circle and hence equalizing the gain of the amplifier circuit across the band of interest.

Curve (a) in Fig. 4.2 corresponds to the transistor in its open loop configuration, $Y'_{12} = 0$. The curve crosses over the constant gain circles as expected due to the classical

Figure 4.2: Loci of $2/S_{21}$ in (4.2.1) for the transistor with and without different feedback network configurations

Figure 4.3: The transistor with an inductor in its drain and two different feedback network configurations. (a) is the transistor; (b) the transistor with an inductor connected in its drain, L_d ; (c) the transistor with a drain inductor, L_d , a feedback resistor, R_{FB} , and a DC blocking capacitor, C_{FB} ; (d) the same configuration as in (b) plus a series feedback inductor, L_{FB} , in the feedback network.

gain roll off of the transistor. In Fig. 4.3(b), an inductor, L_d , has been placed at the drain of the transistor. The resulting change in both magnitude and phase of the $2/S_{21}$ curve is more pronounced beyond 5 GHz as shown by curve (b) in Fig. 4.2. This change is due to the interaction between L_d and the complex intrinsic drain-source admittance of the transistor, Y_{ds} . The resulting $2/S_{21}$ curve (b) can be horizontally shifted to align with the -0.7 circle for most of the bandwidth up to approximately 6 GHz. From (4.2.1), we note that if Y'_{12} is real, curve $2/S_{21}$ is a horizontally shifted version of curve $2/S_{21}^T$ to the left by a purely real Y'_{12} . Therefore, the required horizontal shift for curve (b) can be achieved by a resistor, R_{FB} , shown in Fig. 4.3(c). The value of R_{FB} can be obtained from the horizontal distance between curve (b) and the -0.7 circle in Fig. 4.2. By inspection, this horizontal difference is $Y'_{12} \approx 0.228$ leading to $R_{FB} \approx Z_0/Y'_{12} \approx 219.3 \Omega$. A DC blocking capacitor, C_{FB} , is connected in series with R_{FB} to avoid self-biasing. The resulting curve (c) was finally brought to curve (d) through an inductor L_{FB} incorporated in series with R_{FB} as shown in Fig. 4.3(d). L_{FB} adds a frequency dependant nature to the amount of feedback provided from drain to gate and correspondingly to the Y_{FB} term in the denominator of (3.2.4). This frequency dependence is manifested in the curve pivoting at the higher end of the band shown by curve (d) in Fig. 4.2. L_{FB} can be estimated by using either the complete expressions in [53] or by inspection from the complex plot. By choosing one point on a desired $2/S_{21}$ curve beyond 10 GHz and denoting it as D , the estimated inductor value can be found by solving the equation:

$$Y'_{12} \approx D - \frac{2}{S_{21}^T|_{L_d}}, \quad (4.2.10)$$

where $(2/S_{21}^T|_{L_d})$ represents curve (b) in Fig. 4.2.

Knowing the real and imaginary components of $2/S_{21}$ eventually leads to a quadratic equation in terms of the inductance and when solved, a first estimate of the inductance can be obtained.

Since the feedback network has a direct influence on the input and output impedances, the estimated feedback inductor value should be optimized with that required for matching in order to simultaneously satisfy the two requirements. The effect of including an inductor in series with the feedback resistor and the final $2/S_{21}$ curve is shown in Fig. 4.2(d). The drain and the feedback inductors can be designed such that positive feedback deliberately occurs near the end of the band [9,53]. By adjusting the magnitude of the complex loop gain in (3.2.4) to be below unity at a suitable phase angle (> 110 degrees) such that the denominator in (3.2.4) becomes less than unity, a closed-loop transimpedance and gain that is higher than that of the open-loop case is obtained as will be further explained in section 4.8. In designing the feedback network components, careful modeling and layout design techniques were used to keep the loop gain below unity to avoid oscillations caused by variations in component values. At the schematic level, this was achieved by adopting schematic models that capture the non-ideal behaviour of lumped elements (e.g. resistors, inductors and capacitors). At the layout level, a 2.5 D electromagnetic solver was used as will be further discussed in Chapter 5.

4.3 Power and Noise matching

When designing the input matching network for an LNA, obtaining the optimum reflection coefficient at the input such that simultaneous power and noise matching is achieved across

an ultra-wide bandwidth is a primary challenge. In feedback amplifiers the input and the output impedances are affected by both the feedback network type and the feedback topology. In the chosen feedback technique, the feedback network simplifies the matching process and avoids the trade-off between optimum noise matching and optimum power matching [9,49]. The input impedance of the amplifier without the feedback configuration is capacitive due to the gate to source capacitance, C_{gs} , and the contribution of the gate to drain capacitance, C_{gd} , due to the Miller effect. At the higher end of the band, C_{gs} starts to short the gate to ground which severely degrades the input impedance [38]. Ideally, in order to match the input of the amplifier for maximum power transfer, the amplifier input stage should possess a constant and real input impedance as the signal source is expected to have the same impedance. For measurement purposes, this real input impedance should be matched to the measuring equipment signal source impedance which is standardized to 50 Ohms. For low noise amplifiers, matching for power and noise should be performed simultaneously for the amplifier to see the optimum source impedance. A noiseless real part of a transistor's input impedance is realized in narrow band circuits [45] by adding an inductor to the transistor's source terminal. The value of this real part is $\omega_T L_s$ as shown in (4.3.14). The input capacitive reactance of the same transistor is then cancelled out with an inductive reactance composed of L_s combined with another inductor connected in series, L_g , with the transistor gate giving one more degree of freedom. Since this technique relies on resonance at a single frequency before and after which the transistor input impedance will exhibit a non-zero imaginary part, it is mainly useful for narrow band circuits. For an UWB circuit matching network, its

required reactance can be visualized on the impedance Smith chart as a counterclockwise moving point with the frequency increasing. This behaviour does not conform with a purely inductive or capacitive reactance. In order to design the UWB matching network for the proposed amplifier, the equivalent input impedance, Z_{eq} , at the plane (1-1) in Fig. 4.4(b) was found using the transistor's small-signal model and Miller's theorem to incorporate the feedback network and C_{gd} into the analysis. Z_{eq} is given by,

$$Z_{eq}(s) \approx Z_{Miller} \parallel (Z_{Ls} + \omega_T L_S + \frac{1}{sC_{gs}}) \quad (4.3.1)$$

where,

$$Z_{Miller}(s) = \frac{1}{m_2 Y_{FB} + m_1 s C_{gd}} \quad (4.3.2)$$

$$= \frac{1}{\frac{1}{\frac{R_{FB}}{m_2}} + \frac{1}{\frac{sL_{FB}}{m_2}} + m_2 s C_{FB} + m_1 s C_{gd}}, \quad (4.3.3)$$

$$m_1 = 1 + |A_{v,OL,XY}(s)|, \quad (4.3.4)$$

$$m_2 = 1 + |A_{v,OL,XZ}(s)|. \quad (4.3.5)$$

In (4.3.2) and (4.3.3), we note that $Z_{Miller}(s)$ is a function of the open-loop voltage gain, $A_v(s)$. In order to quantify this relationship further, two expressions were derived for the open-loop gain from X to Y and from X to Z as shown in Fig. 4.5,

$$A_{v,OL}(s) |_{XY} = \frac{-g_m + sC_{gd} + \frac{(g_m + sC_{gs})(g_m + Y_{ds})}{g_m + sC_{gs} + Y_{ds} + \frac{1}{Z_s}}}{sC_{gd} + Y_{ds} \left(\frac{sC_{gs} + \frac{1}{Z_s}}{g_m + sC_{gs} + Y_{ds} + \frac{1}{Z_s}} \right) + \frac{1}{Z_L + Z_{Ld}}} \quad (4.3.6)$$

Figure 4.4: The equivalent input impedance, Z_{eq} , when looking from the reference plane (1-1). Z_{miller} contains the effect of the frequency-controlled feedback network, Y_{FB} , and the gate-to-drain capacitance on the closed-loop input impedance of the feedback amplifier.

$$A_{v,OL}(s) |_{XZ} = \frac{Z_L}{Z_L + Z_{Ld}} \left(\frac{-g_m + sC_{gd} + \frac{(g_m + sC_{gs})(g_m + Y_{ds})}{g_m + sC_{gs} + Y_{ds} + \frac{1}{Z_s}}}{sC_{gd} + Y_{ds} \left(\frac{sC_{gs} + \frac{1}{Z_s}}{g_m + sC_{gs} + Y_{ds} + \frac{1}{Z_s}} \right) + \frac{1}{Z_L + Z_{Ld}}} \right) \quad (4.3.7)$$

$$= \frac{Z_L}{Z_L + Z_{Ld}} A_{v,OL}(s) |_{XY} . \quad (4.3.8)$$

Figure 4.5: A small-signal model used for the open-loop gain calculations [5].

Expressions (4.3.6) and (4.3.7) were plotted versus frequency in Fig. 4.6 where the in-band gain roll-off is shown. The contribution of $Z_{Miller}(s)$ to Z_{eq} is expected to vary with frequency according to the Miller multiplication factors, m_1 and m_2 , as given in (4.3.4) and (4.3.5). Looking from the reference plane (1-1) in Fig. 4.4(b), the imaginary part of Z_{eq} is capacitive due to C_{gs} , $m_1 C_{gd}$ and $m_2 C_{FB}$. Since C_{FB} is a dc blocking capacitor (≥ 5 pF), its contribution to Y_{FB} is negligible within the frequency band of interest. The

Figure 4.6: Open-loop gains from points X to Y and from X to Z . These open-loop gain quantities were used in the Miller's multiplication factors' calculations.

series combination of L_{FB}/m_2 and R_{FB}/m_2 shunted by the parallel combination of $m_1 C_{gd}$ and $(Z_{Ls} + \omega_T L_S + \frac{1}{sC_{gs}})$, results in a stable and a smaller total capacitive reactance over a wide bandwidth compared to the open-loop case. The wideband nature of this resulting capacitive reactance is primarily due to the fact that Miller's multiplication factors, m_1 and m_2 vary with frequency, resulting in a decreasing effective inductive reactance of sL_{FB}/m_2 and a decreasing feedback resistance of R_{FB}/m_2 . With the aid of simulations, the term $(Z_{Miller} \parallel (Z_{Ls} + \omega_T L_S + 1/sC_{gs}))$ in (4.3.15) can be represented by an equivalent capacitance C_{II} shunted by a varying resistance R_{eq} (between 45-30 Ω) depending on $\omega_T L_s$. This parallel RC network has been combined with a series inductor, L_g , and an input shunt capacitance, C_I , to form a conceptual third-order ladder structure as shown

in Fig. 4.7. This ladder structure was designed to absorb the capacitive reactance from C_{II} over a wide bandwidth so that the amplifier is seen to have an approximate purely real input impedance. C_I was realized by the RF input pad capacitance. Higher order ladder structures might be used to allow a wider match however, the more the passive components were, the more losses were introduced which directly contribute to the noise figure. The real part of the Z_{eq} when looking from the reference plane (1-1) in Fig. 4.4(b) can be made close to 50Ω through the parallel combination of $\omega_T L_s$ and the components R_{FB}/m_2 and L_{FB}/m_2 . Given the average values of C_{II} and R_{eq} , the required values for L_g and C_I (or C_{pad}) were estimated using the following set of equations for a chosen 3 dB cut-off frequency of the input network, ω_c , [54]:

$$C_{II} = \frac{2 \sin \gamma_1}{R_{eq}(1 + \delta)\omega_c}, \quad (4.3.9)$$

$$L_g = \frac{4 \sin \gamma_3 \sin \gamma_5}{(1 - 2\delta \cos \gamma_4 + \delta^2)\omega_c^2 C_{II}}, \quad (4.3.10)$$

$$C_I = \frac{2 \sin \gamma_1}{R_s(1 - \delta)\omega_c}, \quad (4.3.11)$$

where,

$$\delta = \sqrt[3]{\frac{R_s - R_{eq}}{R_s + R_{eq}}}, \quad (4.3.12)$$

$$\gamma_m = \frac{m\pi}{6}. \quad (4.3.13)$$

Fig. 4.8 shows the S_{11} curves of the circuit in Fig. 4.9(b) depicting the effect of the frequency dependance of the Miller's multiplication factors, m_1 and m_2 . The arrow in Fig. 4.8 indicates the direction of decreasing m_1 and m_2 with frequency. As these factors vary with frequency, they modify the effective component values of the circuit elements constituting Z_{Miller} in Fig. 4.9(b) resulting in a better input match for frequencies beyond

Figure 4.7: An equivalent third order ladder structure using the C_{II} and R_{eq} of the closed-loop circuit as part of the structure to achieve the ultra-wideband matching.

8.5 GHz.

The amplifier's input impedance after incorporating L_g and C_{pad} can be approximated as shown in Fig. 4.9(b) by:

$$Z_{in}(s) \approx \frac{1}{sC_{pad}} \parallel \left[Z_{Lg} + \frac{Z_{Miller}(Z_{Ls} + \omega_T L_S + \frac{1}{sC_{gs}})}{Z_{Miller} + (Z_{Ls} + \omega_T L_S + \frac{1}{sC_{gs}})} \right] \quad (4.3.14)$$

$$\approx \frac{1}{sC_{pad}} \parallel \left[Z_{Lg} + Z_{Miller} \parallel (Z_{Ls} + \omega_T L_S + \frac{1}{sC_{gs}}) \right] \quad (4.3.15)$$

At this point, we successfully arrived at a first estimate of the lumped components values needed to achieve both gain equalization input and output matching through the entire bandwidth, 3.1-10.6 GHz. The S-parameters simulation results of the amplifier are shown in Fig. 4.10. Up to this point, all lumped components were assumed to be ideal components for simplicity. A series of simulations were carried out to optimize the amplifier components for flat gain, noise figure and VSWR at both input and output after incorporating non-ideal models for each of the lumped components used. The inductor models are examples of the real models which when included in simulations, the amplifier produced performance deviation compared to that based on ideal components for which

Figure 4.8: The effect of varying Miller's multiplication factors on S_{11} at the input of the ladder structure. As m_1 and m_2 vary with frequency, they result in a decreasing effective inductive reactance of sL_{FB}/m_2 and a decreasing feedback resistance of R_{FB}/m_2 with the frequency increasing. The resulting stable capacitive reactance in Z_{eq} can be absorbed in a third-order ladder structure at the input of the amplifier for which the S_{11} is shown.

Figure 4.9: The amplifier circuit and its small-signal approximation used for estimating the amplifier input impedance, Z_{in} .

some of the component values had to be optimized to compensate for such deviations as outlined in Chapter 5.

4.4 Noise Analysis and Simulations

When the intrinsic noise sources of a MOSEFT transistor are represented by a two-port noiseless network preceded by a noise voltage source $\overline{e_n^2} = 4KTBR_n^T$, an uncorrelated noise current source $\overline{i_u^2} = 4KTBG_u^T$, and a correlation admittance $Y_{cor}^T = G_{cor}^T + jB_{cor}^T$, on its input side, the noise factor is given by [6]:

$$F = F_{min} + \frac{R_n^T}{G_s} [(G_s - G_{opt}^T)^2 + (B_s - B_{opt}^T)^2], \quad (4.4.1)$$

where, R_n^T is the equivalent noise resistance, G_{opt}^T and B_{opt}^T are the optimum signal source conductance and susceptance respectively, G_s and B_s are the signal source conductance

Figure 4.10: S-parameters simulation results. S_{21} is at $8.0\text{ dB} \pm 0.2$. S_{11} has a minimum of -13 dB up to 9.5 GHz . S_{22} is below -15 dB for most of the ultra-wide bandwidth up to 9.5 GHz

and susceptance seen by the network respectively. From classical noise theory, the condition for noise matching and noise tuning for the signal source [6, 38], can be achieved

Figure 4.11: A transistor's equivalent two-port noise representation [6]. $T = 0$ represents the noiseless transistor two-port network when the equivalent noise resistance, R_n , the uncorrelated noise conductance, G_u and the correlation admittance, Y_{cor} , are used to represent the transistor noise sources at the input of the two-port network.

when,

$$B_s = B_{opt}^T = -B_{cor}^T = -\Im(Y_{cor}^T) \quad (4.4.2a)$$

$$\approx -\omega C_{gs} \left(1 + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right) \quad (4.4.2b)$$

and,

$$G_s = G_{opt} = \sqrt{\frac{G_u^T}{R_n^T} + |jB_s + Y_{cor}^T|^2} \quad (4.4.3a)$$

$$= G_{opt} |_{B_s = -B_{cor}^T} = \sqrt{\frac{G_u^T}{R_n^T} + (G_{cor}^T)^2}. \quad (4.4.3b)$$

Where, $\alpha = g_m/g_{d0}$, $\delta \approx 1.3 - 4$, $\gamma \approx 0.67 - 1.1$, $|c| \approx 0.4$ and g_{d0} is the channel conductance at $V_{ds} = 0$ [44]. From (4.4.2b), note that the optimum source susceptance is negative which is a characteristic of an inductive susceptance. However, it has a negative slope as frequency increases. This behaviour is opposite to that expected from an inductive susceptance. The susceptance shown as B_{opt}^T in Fig. 4.13 suggests that the ultra-wideband signal source noise tuning needed to get near optimum noise performance from an open-loop MOSFET device can not be satisfied by a pure inductive or capacitive susceptance.

In [6], it was pointed out that the noise tuning, noise matching and power match can be achieved simultaneously by introducing feedback techniques inside the noisy two-port network (i.e. the transistor). In the proposed amplifier topology, the feedback circuitry has altered the behaviour of the noise parameters of the circuit in general and B_{opt}^T in particular.

Figure 4.12: Equivalent two-port voltage and current noise sources at the input of a noiseless amplifier.

Based on the noise analysis provided in [9], the equivalent two-port noise parameters of the circuit shown in Fig. 4.12 have been derived in Appendix C and they are,

$$\hat{R}_n = R_{n,Lg} + R_{n1} |1 + Y_{cor1}a|^2 + G_{u1} |a|^2 \quad (4.4.4)$$

$$\hat{G}_u = |b|^2 \left[G_{u1} + R_{n1} |Y_{cor1}|^2 - \frac{|a^* (G_{u1} + R_{n1} |Y_{cor1}|^2) + R_{n1} Y_{cor1}|^2}{\hat{R}_n^*} \right] \quad (4.4.5)$$

$$\hat{Y}_{cor} = b \left[\frac{a^* (G_{u1} + R_{n1} |Y_{cor1}|^2) + R_{n1} Y_{cor1}}{G_{u1} |a|^2 + R_{n1} |1 + Y_{cor1}|^2 + R_{n,Lg}} \right]. \quad (4.4.6)$$

In (4.4.4), (4.4.5) and (4.4.6),

$$R_{n1} = \left| \frac{Y_{21}}{Y_{21} - Y_{FB}} \right|^2 \left(R_n^T + \left| \frac{Y_{FB}}{Y_{21}} \right|^2 R_{FB} \right) \quad (4.4.7a)$$

$$G_{u1} = G_u^T + |Y_{11} + Y_{21} - Y_{cor}^T|^2 \frac{\left| \frac{Y_{FB}}{Y_{21}} \right|^2 R_n^T R_{FB}}{R_n^T + R_{FB} \left| \frac{Y_{FB}}{Y_{21}} \right|^2} \quad (4.4.7b)$$

$$Y_{cor1} = Y_{cor}^T + (Y_{11} + Y_{21} - Y_{cor}^T) \frac{\frac{Y_{FB}}{Y_{21}} R_n^T + \left| \frac{Y_{FB}}{Y_{21}} \right|^2 R_n^T R_{FB}}{R_n^T + R_{FB} \left| \frac{Y_{FB}}{Y_{21}} \right|^2} \quad (4.4.7c)$$

$$a = \frac{(Z_{Lg} + Z_{11} + Z_S)Z_{21}}{Z_{21} + Z_S} - Z_{11} \quad (4.4.7d)$$

$$b = \frac{Z_{21}}{Z_{21} + Z_S}. \quad (4.4.7e)$$

Y_{11}, Y_{21} and Z_{11}, Z_{21} were obtained from the two-port admittance and impedance matrices of the feedback amplifier respectively. R_n^T , G_u^T and Y_{cor}^T represent the equivalent noise resistance, the uncorrelated noise conductance and the correlation admittance of the MOSFET transistor respectively. These parameters were derived for a simplified MOSFET model in [38] as explained in Appendix B.

In the proposed amplifier topology, the feedback circuitry has altered the behaviour of the noise parameters of the circuit in general and B_{opt} in particular. To understand this effect, equation (4.4.6) will be simplified by neglecting the effect of Z_S in the equations. In [55], it was pointed out that the effect of Z_S on the relative change of F_{min} is less than 0.15% for $L_S < 0.3$ nH up to 10.5 GHz. The noise contribution of L_g will also be ignored

seeking simplicity in the final expression. The simplified expression for (4.4.6) is given by,

$$\hat{Y}_{cor} \approx \frac{\Re(Y_{cor1}) + j \left[\Im(Y_{cor1}) - \omega L_g \left(\frac{G_{u1}}{R_{n1}} + |Y_{cor1}|^2 \right) \right]}{\omega^2 L_g^2 \left(\frac{G_{u1}}{R_{n1}} + |Y_{cor1}|^2 \right) - 2\omega L_g \Im(Y_{cor1}) + 1}. \quad (4.4.8)$$

and the optimum signal source susceptance is:

$$\begin{aligned} \hat{B}_{opt} &= -\Im(\hat{Y}_{cor}) \\ &= \Im \left[b \frac{a^* (G_{u1} + R_{n1}|Y_{cor1}|^2) + R_{n1}Y_{cor1}}{G_{u1}|a|^2 + R_{n1}|1 + Y_{cor1}|^2 + R_{n,Lg}} \right] \end{aligned} \quad (4.4.9)$$

$$\approx \frac{\omega L_g \left(\frac{G_{u1}}{R_{n1}} + |Y_{cor1}|^2 \right) + B_{opt1}}{\omega^2 L_g^2 \left(\frac{G_{u1}}{R_{n1}} + |Y_{cor1}|^2 \right) - 2\omega L_g \Im(Y_{cor1}) + 1}. \quad (4.4.10)$$

It was found numerically that $\omega^2 L_g^2 \left(\frac{G_{u1}}{R_{n1}} + |Y_{cor1}|^2 \right) - 2\omega L_g \Im(Y_{cor1}) \approx -0.2$ up to 9.5 GHz.

This allowed (4.4.10) to be further simplified as:

$$\begin{aligned} \hat{B}_{opt} &\approx \frac{10}{8} \left[\omega L_g \left(\frac{G_{u1}}{R_{n1}} + G_{cor1}^2 \right) + B_{opt1}(\omega L_g B_{opt1} + 1) \right] \\ &\approx \frac{10}{8} [\omega L_g G_{opt1}^2 + \omega L_g B_{opt1}^2 + B_{opt1}]. \end{aligned} \quad (4.4.11)$$

(4.4.11) was plotted against frequency in Fig. 4.13. $\hat{B}_{opt}$ has the nature of capacitive susceptance in its sign and its relation to frequency between 3 GHz and 10 GHz. Ultra-wideband noise tuning is thus achievable via a signal source susceptance of a capacitive nature which can be approximated by C_I in Fig. 4.7. C_I was realized by the RF input pad capacitance. This transformation in the nature of $\hat{B}_{opt}$ was achieved through the chosen feedback topology as well as the inclusion of the L_g in the amplifier circuit. Fig. 4.14 shows the noise figure of the amplifier which is higher than NF_{min} by less than 0.5 dB between 3-10 GHz. Fig. 4.15 shows a Smith chart plot of Γ_{opt} , Γ_{in}^* and VSWR circle = 2.

The proximity of optimum noise and power match conditions for the proposed amplifier topology is depicted between 3.1 GHz and 9.5 GHz.

Figure 4.13: Optimum signal source susceptances for the transistor by itself and for the complete feedback circuit with and without simplifications.

Since the noise simulations obtained from the available MOSFET models were only valid below 1 GHz, foundry provided empirical formulae for the R_n , NF_{min} , Γ_{opt} and G_{max} for a known device size under given bias conditions were used instead. Since these empirical formulae were obtained from the device in its open-loop configuration, they were substituted in a sequence of equivalent two-port network noise formulae given in [55, 56]. This way, the effect of the proposed feedback topology on the equivalent noise parameters; R_n , G_u and Y_{cor} of the amplifier could be monitored through both simulations

Figure 4.14: Amplifier noise figure based on a measured test structure from (1-6 GHz).

Figure 4.15: Amplifier's Γ_{opt} , Γ_{in}^* and VSWR circle = 2.

and calculations as shown in Appendix C. The generalized expressions for the equivalent two-port noise sources in [55, 56] treated feedback (i.e. series or parallel) and cascaded networks separately as shown in 4.16. As a result, multiple substitutions have been incrementally applied to arrive at the final expressions for the equivalent noise parameters of the complete amplifier circuit.

The transistor's Y-parameters were obtained in two different ways. First, by using the simulated Y-parameters of the existing, foundry provided, transistor models. Second, by using the CMOS RF Y-parameters from [57]:

$$Y_{11} = \omega^2 R_g C_{gg}^2 + j\omega C_{gg} \quad (4.4.12)$$

$$Y_{12} = -\omega^2 C_{gg} C_{gd} - j\omega C_{gd} \quad (4.4.13)$$

$$Y_{21} = g_m - \omega^2 R_g C_{gg} (C_m + C_{gd}) - j\omega (C_m + C_{gd}) \quad (4.4.14)$$

$$Y_{22} = g_{ds} + \omega^2 R_g C_{gg} (C_{bd} + C_{gd}) + j\omega (C_{bd} + C_{gd}) \quad (4.4.15)$$

where, $C_{gg} \equiv C_{gs} + C_{gd} + C_{gb}$, $C_m = 4/15 C_{ox} W L$.

Expressions, (4.4.4)-(4.4.6), (4.4.7) and (4.4.12)-(4.4.15) were built in the ADS schematic simulator where the noise figure was plotted as shown in Fig. 4.14. During simulations, the following trade-offs were observed:

- Based on the Feedback resistance, R_{FB} , there is a trade-off between the gain, gain flatness, VSWR and the total noise figure. As shown in Fig. 4.17, the higher the feedback resistance, the lower the total noise figure of the closed-loop amplifier. This can be explained as follows. If, for simplicity, we assume that Fig. 4.18 represents the amplifier noise performance at high frequencies and if we further assume that

Figure 4.16: Two-port network series and shunt connections showing the equivalent noise parameters associated with each network. Z^T represents the Z-parameters of the transistor network with its equivalent noise parameters (F_{min}^T, R_n^T and Y_{opt}^T) connected in a series feedback configuration with the Z_f network. The resulting $(Z^T + Z_f)$ network is then converted to its equivalent Y-parameters network with its new noise equivalent parameters (F_{min}^S, R_n^S and Y_{opt}^S). The shunt feedback network, Y_f , is then incorporated resulting in new set of total noise equivalent parameters.

Figure 4.17: The effect of different feedback resistance on noise figure.

the only change is in terms of the feedback resistance, then when calculating the noise contribution of this feedback resistance equivalent noise current to the total input equivalent noise generators, $\bar{v}_i^2$ and $\bar{i}_i^2$ for an amplifier in a shunt feedback configuration [7, 748-807]:

$$\bar{i}_i^2 = \bar{i}_{ia}^2 + \frac{\bar{v}_{ia}^2}{R_{FB}^2} + 4KT \frac{1}{R_{FB}} B \quad (4.4.16)$$

$$\bar{v}_i^2 = \bar{v}_{ia}^2 \quad (4.4.17)$$

Where, $\bar{i}_{ia}^2$ and $\bar{v}_{ia}^2$ are the statistical averages of the equivalent, partially correlated, 2-port noise current and voltage generators of the amplifier in its open loop configuration, respectively. $\bar{v}_i^2$ and $\bar{i}_i^2$ are the 2-port noise current and voltage generators for the amplifier in its closed loop configuration. In (4.4.16), the second term can

Figure 4.18: Shunt-shunt feedback circuit with internal and external noise sources [7, pp.748-807]

be neglected [pp. 748-807] [7]. As R_{FB} becomes larger, the total equivalent noise current becomes smaller. If the equivalent noise current generator of the feedback resistance contributes less noise current, the total noise current at the input becomes smaller and the closed-loop noise figure becomes smaller. The higher the feedback

resistance is, the closer the noise performance of the amplifier is to its open-loop case. The open-loop case has a better performance due to the absence of this extra noisy feedback resistor unless a pure reactive feedback is used [9]. On the other hand, as the feedback resistance gets smaller, the feedback loop contributes more noise current to the total input-referred equivalent noise current generator and hence higher total noise figure is obtained.

- The amplifier gain and noise figure act contrary to the input matching in general as shown in Figures 4.17 and 4.19. Higher feedback resistance forces the amplifier into its open-loop configuration and therefore higher gain can be obtained however, this comes at the expense of input matching. As a result, the noise figure and the gain were traded for an acceptable input matching level.

Figure 4.19: The effect of different Feedback Resistance on forward transmission coefficient

4.5 Stability

The stability of the amplifier was investigated. S-parameters simulations were performed to monitor stability factors through the operating frequency range (i.e. 3.1-10.6 GHz). The necessary and sufficient conditions for unconditional stability is that K , as given by (4.5.1), should be greater than 1 and B_1 , as given by (4.5.2), should be greater than zero [58].

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad (4.5.1)$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \quad (4.5.2)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

K and B_1 were plotted against frequency in Fig. 4.20. It is noted that $B_1 > 0$ and $K > 1$ over the entire frequency range. Therefore, the amplifier is unconditionally stable within the operating frequency range (i.e. 3.1-10.6 GHz).

4.6 Transient Response

A transient response simulation was performed using a fifth-order derivative Gaussian monopulse. The monopulse has a spectrum density as shown in Fig. 2.3 and discussed in Chapter 2. The input and the inverted output monopulses are shown in Fig. 4.21. It is noted that the input monopulse in Fig. 4.21 has been uniformly delayed by a 32.5 ps to allow for the comparison of the two monopulse pulse shapes. The correlation coefficient between the input and output monopulses is higher than 99%. In correlation-type receivers, as discussed in Chapter 2, the amplified monopulses at the output of the LNA

Figure 4.20: Simulated amplifier stability factors, K and B_1 . The amplifier is unconditionally stable between 3.1-10.6 GHz.

are correlated with locally generated templates. As a result, the harmonic distortion of the amplifier has a direct influence on the time domain correlation output. As a harmonic distortion measure, a periodic steady-state simulation was performed to identify the input referred second and third order intercept points (IIP_{2h} , IIP_{3h}) [32]. Fig. 4.22 shows a simulated IIP_{2h} and IIP_{3h} results using a fundamental frequency of 3.1 GHz. The resulting 2nd and 3rd order harmonics were at 6.2 GHz and 9.3 GHz, respectively. The LNA possesses IIP_2 , IIP_3 at 10.71 dBm and 20.76 dBm, respectively. A simulated input-referred 1 dB compression point at 5.4 GHz is also shown in Fig. 4.23. A summary of the LNA performance is shown in Table 6.1.

Figure 4.21: Amplifier simulated transient response using a fifth order Gaussian monopulse input.

4.7 Biasing Circuitry

The biasing circuitry was made through a drain-connected transistor biased from V_D through a $100\ \Omega$ resistor. A $5\ \text{k}\Omega$ RF blocking resistor was connected in series between the gate-drain of the diode connected transistor and the inductor L_g of the amplifier circuitry as is shown in Fig. 4.24. Since there is no current flowing through this RF

Table 4.1: Summary of the LNA simulations

Technology	0.18 μm CMOS
BW (GHz)	3.1-10.6
S_{11} (dB)	-13
S_{21} (dB)	8 ± 0.2
NF_{min} (dB)	3.5
NF_{av} (dB)	4.4
$1dB_{comp}$ (dBm)	-2.48
P_{diss}	10.3 mA/1.8V

Figure 4.22: Amplifier simulated second and third order harmonic intercepts using a fundamental frequency of 3.1 GHz, second harmonic of 6.2 GHz and third harmonic of 9.3 GHz.

blocking resistor, its contribution to noise is negligible to a first order. The biasing transistor width was chosen with a ratio of one to one with respect to the main amplifying transistor. A 5 pF MIM decoupling capacitor was connected between the gate-drain of the diode connected transistor and its source to decouple any AC quantities from the supply and hence stabilizing V_{gs} of the main amplifying transistor. More elaborate constant-gm biasing circuitries could have been adopted to stabilize gain over temperature and power supply variations however the focus was mainly on the ultra-wideband low noise amplifier prototype performance. The DC blocking capacitors were realized externally due to limited chip area.

Figure 4.23: A 1 dB compression point simulation at 5.4 GHz.

4.8 A Two-port network analysis

In order to arrive at expressions to facilitate describing the transfer function of the frequency-controlled feedback amplifier, a two-port network analysis was adopted to represent the circuit shown in Fig. 4.25 without the biasing circuitry. The main amplifier transistor is represented by its Y-parameters in [57]. The drain inductor, L_d , and the series feedback inductor, L_s , were then added to the transistor Y-parameters matrix. The lower dashed box in Fig. 4.26 shows the resulting Z_a matrix:

$$[Z]_a = Y_{transistor}^{-1} + \begin{bmatrix} Z_{L_s} & Z_{L_s} \\ Z_{L_s} & Z_{L_s} + Z_{L_d} \end{bmatrix}, \quad (4.8.1)$$

where, Z_{L_s} and Z_{L_d} are the impedances of the drain inductor and the source inductor,

Figure 4.25: The circuit used for calculating the transfer function and the closed-loop transimpedance.

To arrive at an expression for the closed-loop transimpedance and gain of the equivalent circuit shown in Fig. 4.26, a set of equations using direct nodal analysis can be written as follows;

$$-i_{in} + v_2(Y_s + Y_{11f}) + Y_{12f} + i_1 = 0, \quad (4.8.3)$$

$$v_{out}(Y_L + Y_{22f}) + Y_{21f}v_2 + i_2 = 0, \quad (4.8.4)$$

$$i_1 = \frac{v_2 - Z_{12f}i_2}{Z_{11a}}, \quad (4.8.5)$$

$$i_2 = \frac{v_{out} - Z_{21a}i_1}{Z_{22a}}. \quad (4.8.6)$$

Solving (4.8.3)-(4.8.6) gives

$$\frac{v_{out}}{i_{in}} = \frac{\left(-\frac{Y_{21f}Z_{11a} - \frac{Z_{21a}}{Z_{22a}} - \frac{Y_{21f}Z_{12a}Z_{21a}}{Z_{22a}}}{(Y_{22f} + Y_L + \frac{1}{Z_{22a}} + \frac{Y_{21f}Z_{12a}}{Z_{22a}})(1 + Y_{11f}Z_{11a} + Y_sZ_{11a} - \frac{(Y_{11f} + Y_s)Z_{12f}Z_{21a}}{Z_{22a}})} \right)}{1 + \left(-\frac{Y_{21f}Z_{11a} - \frac{Z_{21a}}{Z_{22a}} - \frac{Y_{21f}Z_{12a}Z_{21a}}{Z_{22a}}}{(Y_{22f} + Y_L + \frac{1}{Z_{22a}} + \frac{Y_{21f}Z_{12a}}{Z_{22a}})(1 + Y_{11f}Z_{11a} + Y_sZ_{11a} - \frac{(Y_{11f} + Y_s)Z_{12f}Z_{21a}}{Z_{22a}})} \right) (Y_{12f} + \frac{(Y_{11f} + Y_s)Z_{12f}}{Z_{22a}})} \quad (4.8.7)$$

Figure 4.26: The circuit used for calculating the transfer function and the closed-loop transimpedance.

The closed-loop transimpedance in (4.8.7) has the form of the standard closed-loop transfer function:

$$A(s) = \frac{a(s)}{1 + a(s)f(s)}. \quad (4.8.8)$$

Comparing (4.8.7) and (4.8.8) gives

$$a(s) = -\frac{Y_{21f}Z_{11a} - \frac{Z_{21a}}{Z_{22a}} - \frac{Y_{21f}Z_{12a}Z_{21a}}{Z_{22a}}}{(Y_{22f} + Y_L + \frac{1}{Z_{22a}} + \frac{Y_{21f}Z_{12a}}{Z_{22a}})(1 + Y_{11f}Z_{11a} + Y_sZ_{11a} - \frac{(Y_{11f} + Y_s)Z_{12f}Z_{21a}}{Z_{22a}})}, \quad (4.8.9)$$

$$f(s) = Y_{12f} + \frac{(Y_{11f} + Y_s)Z_{12f}}{Z_{22a}}. \quad (4.8.10)$$

Therefore, the closed-loop input and output impedances were found to be [7, pp.535-596]:

$$Z_{in|closed-loop} = \frac{Y_s^{-1} \| Z_{11a} \| Y_{11f}^{-1}}{1 + T} \quad (4.8.11)$$

and,

$$Z_{out|closed-loop} = \frac{Z_{22a} \| (Y_{22f} + Y_L)^{-1}}{1 + T} \quad (4.8.12)$$

where,

$$T = a(s)f(s). \quad (4.8.13)$$

The quantity $T = a(s)f(s)$ from (4.8.9) and (4.8.10) is the loop gain. $a(s)$ and $f(s)$ represent the open-loop transimpedance and the feedback factor, respectively. From (4.8.10), it is noted that the feedback factor has two components: the frequency-dependant feedback network and a combination of the degenerated transistor series feedback impedance with the loading effect. Therefore, the series inductor, L_g , also contributed to the loop gain and was used to adjust for the frequency point at which the positive feedback occurs. The phase of the loop gain, $T=a(s)f(s)$, was plotted in Fig. 4.27 showing the positive feedback effect near the end of the operating bandwidth [59]. the denominator in (4.8.7) becomes less than one resulting in a closed-loop gain that is higher than that of the open-loop as is shown in Fig. 4.28 [10]. The transducer power gain is given by [42],

$$G_T = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_{in}\Gamma_S|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \quad (4.8.14)$$

$$G_T|_{\Gamma_S=\Gamma_L=0} = |S_{21}|^2 \quad (4.8.15)$$

where, S_{21} is the forward transmission coefficient, Γ_S , Γ_{in} and Γ_L are the source, input

Figure 4.27: Phase angle of the complex loop gain based on (4.8.9) and (4.8.10).

and load reflection coefficients, respectively. In Figs. 4.25 and 4.26,

$$v_{in} = \frac{(i_{in}/Y_s)Z_{in}}{Z_{in} + Z_s}. \quad (4.8.16)$$

Since,

$$a_1 = \frac{v_{in}}{\sqrt{Z_0}} = \frac{(i_{in}/Y_s)Z_{in}}{(Z_{in} + Z_s)\sqrt{Z_0}} \quad (4.8.17)$$

and

$$b_2 = \frac{v_o}{\sqrt{Z_0}} \Big|_{a_2=0}, \quad (4.8.18)$$

it follows that,

$$S_{21} = \frac{b_2}{a_1} \Big|_{a_2=0} \quad (4.8.19)$$

$$\begin{aligned} &= \frac{v_o/\sqrt{Z_0}}{(i_{in}/Y_s)Z_{in}/(Z_{in} + Z_s)\sqrt{Z_0}} \\ &= Y_s \left(\frac{v_o}{i_{in}} \right) \left(\frac{Z_{in} + Z_s}{Z_{in}} \right) \\ &= 2 Y_s \frac{v_o}{i_{in}} \Big|_{Z_{in}=Z_s} \end{aligned} \quad (4.8.20)$$

Figure 4.28: Closed- and open-loop gain curves, it is shown that the closed-loop gain is higher than the open-loop gain beyond 9 GHz.

Expression (4.8.14) can be expressed in dB as

$$G_T(\text{dB}) = 20 \log |S_{21}| = 20 \log \left(2 Y_s \frac{v_o}{i_{in}} \right) \quad (4.8.21)$$

By substituting (4.8.7) in (4.8.21), G_T is plotted against frequency and compared to simulations in Fig. 4.29. It is noted that the difference between the calculated and the simulated curves for $20 \log(S_{21})$ follow a similar trend. However, the simulated curve is lower than the calculated curve because the later was based on a simplified small-signal transistor model compared to the more accurate model that was used in simulations.

Figure 4.29: Calculated versus simulated closed-loop transducer power gain. The difference between the two curves is due to the simplified small-signal model used in the calculations compared to the more accurate model used in simulations.

4.9 Summary

In this chapter, the design steps for a UWB frequency-controlled feedback LNA were outlined. A simple transistor model was used to arrive at simple design equations. A graphical design approach was then applied to estimate the feedback network component values. Miller's multiplication effect was investigated for this topology. A simultaneous power and noise matching technique utilizing Miller's multiplication effect and a third-order ladder structure at the input of the amplifier was discussed. Equivalent two-port network noise parameters of the amplifier were illustrated. It was shown that the proposed amplifier topology transformed the nature of the optimum signal-source susceptance needed to achieve UWB noise matching such that it can be approximated by a capacitive susceptance. Trade-offs between the amplifier gain, noise figure and matching were identified. The LNA was shown to be unconditionally stable between 0.1-12 GHz. The LNA

transient response to a fifth order Gaussian monopulse was simulated. The input-referred second- and third-order intercept points due to the second- and third-order harmonic distortion was also simulated. Finally, a two-port network analysis for the LNA was used to arrive at an expression for closed-loop transfer function. A comparison between the open- and closed-loop gains of the amplifier revealed that a positive feedback occurred beyond 9 GHz.

Chapter 5

Layout and Implementation

In this chapter, the LNA layout design details are discussed. Inductor modelling and parameters extraction from Momentum simulations are presented.

5.1 Implementation Technology

The technology used to implement the proposed UWB LNA in this work is a CMOS $0.18\mu\text{m}$ six metal, single poly, salicide CMOS process. The nominal supply voltage in this process is 1.8 V. The layout implementation commenced with the chosen device sizes, passive and reactive optimized component values.

5.2 Transistor Layout

When designing the layout of the $64\times 2.5\times 0.18\mu\text{m}$ transistor. the following factors were taken into consideration:

- Transistor gate-to-drain and gate-to-source capacitances were minimized by minimizing metal trace overlaps between the device terminals. This was accomplished by:

1. Breaking the device width into 4 equal sections $16 \times 2.5 \mu\text{m}$ width each. This gave flexibility in providing more routing areas and hence avoiding metal trace overlaps as shown in Fig. 5.1.
 2. Metal crossovers were also avoided when connecting to the sources and the drains of the transistor sections. This was accomplished by connecting to the source and drain terminals using metal 2 and metal 3. Via's were used to reach the source and drain terminals from the top. This eliminated the need to cross over the gate areas which resulted in less gate-to-source and gate-to-drain parasitic capacitances.
- The transistor gate resistance was minimized in order to reduce its negative impact on the noise figure and matching [5]. This was achieved by:
 1. Using the minimum gate width for each finger recommended by this technology ($2.5 \mu\text{m}$).
 2. Contacting the gate terminal from both sides. This technique was recommended by researchers [5, p.214] who investigated the impact of gate resistor on the MOSFET noise performance. The resultant gate resistance after using this approach was reduced by a factor of 1/4.
 3. Using metal 1 to route all the gate connections which saved a large amount of resistance compared to the case where all the gate routing is done completely in polysilicon. It is noted here that breaking the device width into multiple sections allowed for metal 1 routing to each and all the gates with minimum

Figure 5.1: A $64 \times 2.5 \times 0.18 \mu\text{m}$ device layout used as the main amplifying device

overlapping with other device terminal metal connections.

- Breaking the device into four sections also allowed more room for adding substrate contacts on both sides of each device section. Adding substrate contacts allows for minimizing the effective resistance between the transistor body and ground and hence lower the contribution of epi noise [38].
- Current handling capability of the drain and source metal lines was also considered. This determined the minimum width of the source and drain terminal metal lines which prevents electromigration. The current density specifications for both metal 3 and metal 4 are $1.0 \text{ mA}/\mu\text{m}$ at 110°C . With the DC current estimated to be 10 mA , the width of the metal traces of the drain and source was chosen to be $10 \mu\text{m}$.

Minimum metal line lengths were chosen such that parasitic capacitances were avoided [38], since the gain-bandwidth product is dependent on the input and output time-constants which may severely degrade as a result of these parasitic capacitances.

Since the gain, bandwidth, matching and noise figure performances of the implemented LNA were sensitive to any lumped or distributed reactive components, important metal line interconnects between the lumped inductors and other circuit components on the RF signal path were treated as transmission lines and were modeled using Momentum. The microwave mode was used with substrate and metallization properties configured as shown in Appendix D [60]. The line sections which were modeled in Momentum are:

- The metal5 trace between the RF input pad until the feed-point of the inductor L_g as shown in Fig. 5.2 was modeled. The amount of inductance introduced by

Figure 5.2: Line sections simulated in ADS Momentum enclosed in rectangles

this section will directly add to the inductance value of the gate inductor, L_g . The length of line was measured to be $139\text{ }\mu\text{m}$ in total with metal5 width of $20\text{ }\mu\text{m}$ was modeled. This line contributed an equivalent inductance of 0.17 nH .

- The metal 5 trace between the transistor drain connection point and the point feeding the drain inductor shown in the middle of the layout in Fig. 5.2. The length of this section is $42\text{ }\mu\text{m}$ horizontal and $208\text{ }\mu\text{m}$ vertical with a metal width of $15\text{ }\mu\text{m}$. The inductance contributed by this metal section was found to be 180 pH .
- The metal 5 trace between the "L" section connecting the drain inductor to the feedback inductor, L_{FB} , feeding point was modeled. This length of line has a horizontal distance of $104\text{ }\mu\text{m}$ with a line width of $20\text{ }\mu\text{m}$ and a $128\text{ }\mu\text{m}$ vertical distance at a metal width of $12\text{ }\mu\text{m}$ as shown in 5.2. The equivalent inductance was found to be 150 pH .

5.3 Inductors Layout and Performance Issues

All of the inductors except the source degeneration inductor were chosen from a library of inductors built in an Agilent® ADS Momentum Advanced Model Composer (AMC) which was initially investigated in [60]. In this library, different inductors were generated for various number of turns, radii, widths, and spacings. Initially, inductors geometry was designed to give the desired inductance required for the schematic simulations. The geometrical parameters, i.e. number of turns (N), metal width (W), spacing (s) and the average, inner and outer spiral diameters (d_{avg} , d_{out} , d_{in}), respectively, as shown in Fig. 5.3, were chosen based on a modified Wheeler expression proposed in [61]:

$$L_{mw} = K_1 \mu_0 \frac{N^2 d_{avg}}{1 + K_2 \rho}, \quad (5.3.1)$$

where, K_1 and K_2 are layout dependant coefficients. For octagonal spiral inductors, $K_1 = 2.25$ and $K_2 = 3.55$. $\mu_0 = 4\pi \times 10^{-7}$ is the permeability of free-space, ρ and d_{avg} are given by [61]

$$\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \quad (5.3.2)$$

$$d_{avg} = 0.5(d_{out} + d_{in}) \quad (5.3.3)$$

A list of the layout geometry for the inductors used in the LNA is shown in Table 5.1. Initially, the inductance values for each of the chosen inductors was based on the schematic simulations. Post layout simulations showed the effects of lengths of lines connecting the lumped inductors to each other or, to other circuit components in the layout. The drain and the feedback inductors, L_d and L_{FB} , respectively, were optimized to provide the rest

Figure 5.3: A spiral inductor geometry.

of the inductance needed after taking into consideration the existing distributed inductive effect of these length of lines. The choice of the inductors was based on an optimization script which was set up to simulate each inductor in the RF mode to evaluate three parameters [60]:

1. The inductance value over the desired UWB frequency range (i.e. 3.1 - 10.6 GHz).
2. The quality factor, Q , of the inductor within the same frequency range.
3. The self resonance frequency of the inductor (SRF).

The chosen inductors were then simulated using the microwave mode in Momentum to get a more accurate estimation of their inductance values, Q factors and SRF as shown in Figures 5.4-5.13.

Table 5.1: Summary of inductor geometry

Inductor	Number of Turns	Radius (μm)	Width (μm)	Spacing (μm)	$L(\text{nH})$ from (5.3.1)
L_g	2.5	100	16	6	1.24
L_{FB}	2.5	100	12	5	1.578
L_d	1.5	75	17	6	0.517
L_s	-	42	4	-	-
L_{load}	4.5	100	10	3	3.501

Figure 5.4: Source degeneration inductor geometry in Agilent ADS Momentum

Figure 5.5: Source degeneration inductor 2.5-D EM simulation results in Agilent ADS Momentum

Figure 5.6: Drain inductor geometry in Agilent ADS Momentum

Figure 5.7: Drain inductor 2.5-D EM simulation results in Agilent ADS Momentum

Figure 5.8: Gate inductor testbench in Agilent ADS Momentum

Figure 5.9: Gate inductor 2.5-D EM simulation results in Agilent ADS Momentum

Figure 5.10: Feedback inductor geometry in Agilent ADS Momentum

Figure 5.11: Feedback inductor 2.5-D EM simulation results in Agilent ADS Momentum

Figure 5.12: Load inductor geometry in Agilent ADS Momentum

Figure 5.13: Load inductor 2.5-D EM simulation results in Agilent ADS Momentum

The s-parameters were then fitted to the model shown in Fig. 5.14. In the model

Figure 5.14: A lumped model for integrated spiral inductors [8].

shown in Fig. 5.14, L_m corresponds to the series inductance. R_s approximates both the dc resistance of the inductor and the average ac resistance resulting from the skin effect. C_p models the overlap capacitance between the spiral planar structure and the underpass. C_p also models the cross talk between the input and output ports of the spiral inductor as well as the interwinding capacitance [8]. C_{ox} represents the parasitic capacitance between the spiral planar structure and the substrate. C_{sub} models the capacitive effects of the substrate at high frequencies. R_{sub} models the substrate resistivity.

The model parameters in Fig. 5.14 were extracted based on approximate expressions that incorporate two-port Y-parameters data obtained from Momentum s-parameters simulations [62, 63]:

$$L_m = \frac{1}{\omega \cdot \Im\{Y_{12}\}} \Big|_{low\ frequency} \quad (5.3.4)$$

$$R_s = -\Re\{Y_{12}\} \cdot \omega^2 L_s^2 \Big|_{low\ frequency} \quad (5.3.5)$$

$$C_{ox} = -\frac{1}{\omega \Im\left\{\frac{1}{Y_{11}+Y_{12}}\right\}} \quad (5.3.6)$$

$$R_{sub} = \Re\left\{\frac{1}{Y_{11}+Y_{12}}\right\} \Big|_{low\ frequency} \quad (5.3.7)$$

$$C_{sub} = \frac{1}{\omega} \sqrt{\frac{1}{R_{sub} \Re\left\{\frac{1}{Y_{11}+Y_{12}}\right\}}} \Big|_{high\ frequency} \quad (5.3.8)$$

Table 5.2 shows a list of the component values used to fit the inductor model to each of the inductors used. It is noted that the series resistance values, R_s , are somewhat higher than the those calculated. This was intentionally done to restrict the quality factor, Q , of the inductors to the 5-7 range as estimated by the foundry test structures.

The following guide lines were followed for inductors layout [8, 38, 61, 64]:

- Top metal (i.e. metal 6) was used for all the inductors to minimize the shunt parasitic

Table 5.2: Summary of the inductor model component values

Parameter	L_g	L_{FB}	L_d	L_m	L_{load}
L_s (nH)	1.056	1.372	0.408	0.153	2.88
R_s (Ω)	4.9	6	2.4	1.7	8.84
C_p (fF)	6.17	6.5	7.43	-	8.12
C_{ox1} (fF)	46.9	44	28	4.6	42.2
R_{sub1} (Ω)	490	442	550	1.5 K	340
C_{sub1} (fF)	32.3	38.5	20.24	11	40
C_{ox2} (fF)	46.9	49	22.4	4.6	47
R_{sub2} (Ω)	490	442	550	1.5 K	340
C_{sub2} (fF)	32.3	38.5	20.24	11	40

capacitance to the substrate because it allows the spiral planar structure to be the farthest from the silicon substrate.

- Metal6 in this technology is the thickest compared to lower-level metal layers. Thicker metal improves the quality factor of the inductor for a slight degradation in the parasitic capacitance and the inductance.
- The metal width was used as an optimization variable for choosing the location of the peak Q frequency whenever possible.
- 4-5 metal widths separation between the inductors and other components of the circuit was maintained whenever possible to avoid coupling and any disturbance from nearby inductors.
- Halo substrate contacts surrounded the inductors to improve the inductor Q performance. The halo substrate contact rings are broken in order not to form a closed loop and circulate induced current themselves which may impact the maximum Q by 15% [65].

The chip micrograph is shown in Fig. 5.15. It is noted that two bonding pads were added at the two sides of the L_g inductor. This was intended to investigate the effect of replacing L_g with a bondwire (0.5 nH/mm [66]) on the noise performance of the LNA after using laser cutting to isolate L_g from the circuit. The low ohmic loss and the high Q of the inductance realized from a low resistivity (i.e. gold) bondwire compared to aluminum on-chip lumped inductors is expected to improve the noise figure of the LNA [38]. The bonding pads were chosen to be on metal levels 4, 5 and 6 connected

Figure 5.15: A micrograph of the UWB LNA implemented in 0.18 μm CMOS process.

together and occupying an area of $70 \times 70 \mu\text{m}^2$. This gave rise to a capacitance close to 50 fF from each pad mandating the laser cutting before doing s-parameter measurements as this would greatly affect the input matching of the LNA. The effect of adding these pad capacitances on the S_{11} , S_{22} and S_{21} is shown in the post-layout simulation results in Figures 5.16, 5.17 and 5.18. Since the laser cutting was not available at the time of writing this manuscript, the results of this experiment were not provided here.

5.4 Summary

The transistor layout design guidelines in 0.18 μm CMOS technology were discussed. The geometry of the inductors were initially chosen based on the presented equations and calculations. The selected inductors were then simulated in ADS Momentum. A summary of the extracted Q and L for each inductor used in the LNA was provided. The adopted

Figure 5.16: Input reflection coefficient as per the post layout simulation for the tuned-feedback UWB LNA

Figure 5.17: Output reflection coefficient as per the post layout simulation for the tuned-feedback UWB LNA

inductor equivalent model parameters were extracted from Momentum S-parameters simulations. The final S-parameter simulations for the extracted LNA including the added bonding pads were presented.

Figure 5.18: Forward transmission coefficient as per the post layout simulation for the tuned-feedback UWB LNA

Chapter 6

Measurement Results

In this Chapter, DC and RF measurement results of the LNA are discussed. The results are compared with simulations from Chapter 3.

6.1 DC Measurements

DC measurements were performed on wafer to characterize the amplifier transistor performance and identify the DC operating point of the transistor amplifier.

Fig. 6.1 shows the measured drain current versus the gate-to-source voltage. The corresponding curves obtained from simulations are also plotted in the same figure. This comparison was performed to highlight the differences between the device expected and actual performance at DC. It is noted that the measured curves are below the slow models provided by the process foundry. The transconductance of the main transistor amplifier is given by,

$$g_m = \frac{\partial i_d}{\partial v_{gs}} \bigg|_{v_{ds}=\text{constant}} \quad (6.1.1)$$

This gave rise to the conclusion that the transconductance is less than its typical value obtained from simulations (0.0676 A/V). As a result, the gain of the amplifier is lower

than its typical value that was obtained from simulations.

Figure 6.1: Measured I_d versus V_{gs} . The measured curve shows that the transistor DC characteristics fell below the foundry provided slow models.

6.2 RF Measurements

6.2.1 S-Parameters Measurements

The LNA circuit performance was measured and characterized on-wafer using a Cascade Microtech ® G-S-G probes with $150\ \mu\text{m}$ pitch. The probes were first calibrated using a calibration substrate and the WinCal® calibration software. A short-open-load-thru (SOLT) calibration procedure was adopted to shift the measured S-parameters reference plane to the probe tips. An Agilent PNA-L network analyzer N5230A was used for S-parameters measurements. Figure 6.2 shows the measured results of S_{11} and S_{22} for different bias currents. The minimum value of S_{11} is -9.1 dB. The two bonding pads that

Figure 6.2: Measured S_{11} and S_{22} at different bias currents, I_d .

were added on each side of the inductor L_g resulted in an extracted capacitance equal to 50 fF from each pad. These capacitances degraded the input matching of the LNA which explains the reported S_{11} curve in Fig. 6.2 and why it is higher than that reported in Fig. 4.10 [59].

Figure 6.3 shows the measured results of S_{21} and $|S_{12}|$. $|S_{12}|$ has a minimum of -20.5 dB and a maximum of -17.7 dB between 3.1-10.6 GHz. $|S_{21}|$ is between 7.2 dB and 4 dB up to 3.3 GHz. $|S_{21}|$ rolls off beyond 5 GHz at a rate of 5.5 dB/octave. It is noted that the measured $|S_{21}|$ is lower than that obtained from simulations by 50 % beyond 3.26 GHz. The reasons for this noticeable power gain degradation will be explained in section 6.2.3.

Figure 6.3: Measured S_{21} and S_{12} at different bias currents, I_d .

6.2.2 Voltage Gain

For a fully integrated CMOS receiver, an on-chip correlator may be directly coupled to the LNA output. In this case, the voltage gain of the LNA becomes pertinent. The voltage gain was extracted from the measured s-parameters using:

$$A_v = -\frac{Y_{21}}{Y_{22}} \quad (6.2.1)$$

where,

$$\begin{aligned} Y_{21} &= Y_0 \frac{-2S_{21}}{(1+S_{11})(1+S_{22}) - S_{12}S_{21}} \\ Y_{22} &= Y_0 \frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{(1+S_{11})(1+S_{22}) - S_{12}S_{21}} \\ Y_0 &= \frac{1}{Z_0} \end{aligned}$$

Figure 6.4: Extracted voltage gain from measured S-parameters at different bias currents, I_d from 3.1-10.6 GHz.

Figure 6.4 shows the voltage gain of the LNA between 3.1-10.6 GHz for different bias currents. The LNA attains a voltage gain between 11 dB and 8 dB up to 6.95 GHz. The measured 3 dB bandwidth in Fig. 6.4 is 7.3 GHz. The low voltage gain beyond 7 GHz will be explained in section 6.2.3. The voltage gain of the LNA in the lower band (i.e. 3.1-5.15 GHz) [16] was plotted in Fig. 6.7. It is shown that the voltage gain attains a 9.53 ± 0.86 dB (maximum of 10.4 dB and a minimum of 8.67 dB) at 12 mA. The voltage gain and S_{11} of the LNA between 3.1-10.6 GHz were plotted for different bias currents in Figures 6.6 and 6.4, respectively.

Figure 6.5: Extracted voltage gain from measured S-parameters at different bias currents, I_d between 3.1-5.15 GHz.

6.2.3 Discussion

The low power and voltage gains and the bandwidth degradation were believed to be due to the performance of the two series-connected load inductors. The two inductors were used to provide the total load inductance of 7 nH. At design time, Momentum simulations of each inductor alone showed a nominal inductance of 3-3.5 nH with a quality factor above 5 for most of the operating frequency range as shown in figure 6.9.

The total series-connected inductors structure was not simulated in Momentum prior to tape-out. It was erroneously assumed that the total inductance would approximately double (i.e. 7 nH) with a slight degradation in the self resonance frequency (SRF) and the quality factor of the whole structure. After measurements, the structure shown in

Figure 6.6: Measured S_{11} at different bias currents, I_d from 3.1-10.6 GHz.

Fig. 6.10 was simulated in a microwave-mode simulation in Momentum. It was found, as shown in Fig. 6.11, that this structure suffered from an SRF beyond 9 GHz with a degradation exceeding 50 %. The simulation results also show that the total inductance value did not increase as expected and that the quality factor below 5 GHz has degraded by approximately 50 %. The degradation in both the SRF and the Q was believed to be related to the following:

- The increased area of the two inductors combined resulted in a doubled value of the shunt capacitance to the substrate. This shunt capacitance lowered the self resonance frequency. This is also explained by the direct proportionality between the C_{ox} in the inductor equivalent Π model and the total spiral area (i.e. $w \cdot l$) given by [8]:

$$C_{ox} = \frac{1}{2} \cdot w \cdot l \cdot \frac{\epsilon_{ox}}{t_{ox}}, \quad (6.2.2)$$

Figure 6.7: Measured S_{11} and extracted voltage gain from measured S-parameters in the lower band (3.1-5.15 GHz).

Figure 6.8: A geometry for one of the two series connected load inductors in Agilent ADS Momentum.

where factor of $1/2$ is used to divide the C_{ox} between the two ports of the Π model [8].

- The overlap capacitance between the underpass metal trace and each inductor structure resulted in 2 equivalent parasitic capacitances, C_s , shunting each inductor between its input and output ports. This overlap capacitance is given for each inductor by [8]:

$$C_p = N \cdot w^2 \cdot \frac{\epsilon_{ox}}{t_{ox, M_6-M_5}} \quad (6.2.3)$$

Figure 6.9: The 2.5-D EM simulation results for one of the two series connected load inductors in Agilent ADS Momentum.

- The decreased effective substrate resistivity besides the doubled shunt parasitic capacitance to substrate and the increased equivalent series capacitance between the input and the output ports of the total structure degraded the total Q of the two series-connected spirals [8].
- The transmission line connecting the two inductors in series was not taken into consideration while the extracted simulations were done. The direction of current flowing in this line opposes the direction of the current flowing in the inductor to the right. This opposite current flowing introduced flux lines in two opposite directions and reduced the resulting inductance.

The degradation in the DC characteristics of the transistor and the fact that the I_d - V_{gs} curve fell below the slow models resulted in a degradation in the F_T of the transistor which has degraded the transistor performance at high frequencies. Due to the low transconductance value extracted from the DC measurements, the reported power and voltage gains were obtained at higher biasing conditions (i.e. $I_d = 12$ mA) than those originally used at design time (i.e. $I_d = 10.3$ mA) and simulations). The load inductor performance and the measured DC characteristics of the transistor discussed above explained why the

Figure 6.10: The load inductor structure which consists of two series-connected identical inductors

Figure 6.11: Load inductor 2.5-D EM simulation results in Agilent ADS Momentum

amplifier has power gain at lower frequencies as shown in Fig. 6.3 where the inductor structure is below its SRF and the transistor is far from its degraded F_T . The power gain was degraded as the Q of load inductor and the inductance, L , decreased with frequency increasing toward the SRF (i.e. ≈ 9.5 GHz) as shown in Fig. 6.11.

6.2.4 Noise Figure Measurements

Noise figure measurements of the amplifier were carried out in a copper cage to prevent external interference from coupling into the test bench. The amplifier noise figure was measured using the noise figure analyzer (NFA) 8975A. The measured and calculated noise figures between 3-10.6 GHz are plotted in Fig. 6.12. The measured noise figure in the lower band (3-5.15 GHz) is shown in Fig. 6.13. The discrepancy in the measured noise figure compared to that initially simulated in [59] is believed to be due to the following

Figure 6.12: Measured and derived Noise figure between 3.1-10.6 GHz. The derived noise figure is based on foundary-provided measured test structures data.

Figure 6.13: Measured and derived Noise figure for the lower band (3.1-5.15 GHz). The derived noise figure is based on foundary-provided measured test structures data.

reasons:

- In the lower band, the poor load inductor performance that was discussed in section 6.2.3 resulted in a low power gain, degrading the noise performance. In the upper band (5.82-10.6 GHz), there is no power gain and as a result, there is a high uncertainty factor associated with the noise figure measurements in that band [67].
- In [52], it was reported that in short channel devices, measured two-port equivalent noise resistance, R_n , in test structures for 0.18 μm technology was observed to have become smaller than that obtained from larger gate lengths (e.g. 0.5, 0.8 and 1.5 μm). Furthermore, it was reported that as the gate voltage is increased, measured R_n values monotonically increased and they exceeded those values obtained for larger gate lengths at the same gate voltage level. Since DC measurements of the devices for the fabricated UWB LNA highlighted that the devices possess operating characteristics poorer than the foundry provided slow models, the gate voltage was increased to reach a higher transconductance. This resulted in an increased R_n value. The increased R_n resulted in an increase in the overall measured noise figure due to the increased sensitivity to the noise match (3.3.4).
- The degradation in the input reflection coefficient as reported in Section 6.2.1 resulted in a deviation from the noise matching by approximately 4 dB. The increased R_n discussed above combined with the increased mismatch is believed to have contributed to the noise figure degradation.
- The losses introduced by the passive elements in the circuit that was not accounted

Figure 6.14: Extrapolation of the measured amplifier IIP3 in a two-tone test of 5.39 GHz and 5.41 GHz.

for in calculations (e.g. L_d , L_{FB}).

- The differences between the transistor layout implemented in this work and the layout from which the foundry-provided noise data was obtained is believed to have contributed to the discrepancy between the derived and measured noise figure.

6.2.5 A Two-tone test and a Third-Order Intercept Extrapolation

A two-tone test was performed to measure the IIP_3 of the LNA. In this test, two signals (5.39 GHz and 5.41 GHz) were applied to the LNA. The output fundamental signal (5.39 GHz and 5.39 GHz) and the third-order intermodulation product (5.4 GHz) were measured using an Agilent PSA E4440A. The measurement results are shown in Fig. 6.14. The measured third-order intermodulation product and the fundamental outputs were extrapolated and found to be 10.67 dBm. A summary of the measured LNA performance is shown in Table 6.1. The amplifier voltage gain and noise figure reported may be used in an UWB receiver front-end targeted for the lower-band of the UWB allocated spectrum

Table 6.1: Summary of the measured LNA performance

Technology	0.18 μm CMOS
A_v (dB)	10 ± 1
Bandwidth $_{ 3\text{dB}}$ (GHz)	3.1-7.5
S_{11} (dB)	-9.1
NF $_{\text{min}}$ (dB)	6.41
IIP $_3$ (dBm)	10.67
I $_D$ /V $_{DD}$	12 mA/1.8 V

(i.e. 3.1-5.15 GHz) if an on-chip mixer or correlator is adopted.

6.3 Summary

In this Chapter, the DC and RF measurement results of the LNA were presented. The DC results showed that the amplifier transistor possess characteristics that are poorer than the foundry provided slow models. S-parameters measurements were reported and correlated with simulation results from Chapter 3. The voltage gain of the amplifier was extracted from the measured S-parameters. Noise figure measurements and two-tone test results were also reported. The amplifier demonstrated a voltage gain of 9.53 ± 0.86 dB with a 3 dB bandwidth of 7.3 GHz, a minimum $|S_{11}|$ of -9.1 dB, a minimum NF of 6.4 dB, an IIP $_3$ of 10.67 dBm while drawing a 12 mA of current from a 1.8 V supply.

Chapter 7

Conclusions and Future Work

In this Chapter, the thesis work is summarized and some directions for future work are presented.

7.1 Conclusions

In this thesis, the design and implementation of a UWB LNA in $0.18\ \mu\text{m}$ CMOS technology was investigated. The design criteria targetted a fully integrated LNA for the impulse radio (IRUWB) receivers. For this type of receivers, besides the low-power and near optimum noise and power matching performance, flat gain and constant group delay performance is important [21]. Several amplifier circuit topologies were critically reviewed. The frequency-controlled feedback topology was selected since it allowed for maintaining a flat gain across the UWB operating bandwidth. A graphical design approach [53] was applied to design the feedback network components. A theoretical analysis assisted by simulations showed the effect of Miller's multiplication effect on the feedback network components. The variation of Miller's multiplication factors with frequency resulted in a transistor closed-loop input impedance with a stable real and imaginary components.

This stable complex impedance could be absorbed in a third-order butterworth ladder structure comprised of a series inductor and the RF input pad capacitance.

Post layout simulations of the LNA showed an $|S_{21}|$ of 8 ± 0.2 dB across a 3.1-10.6 GHz bandwidth with a minimum spot noise figure of 3.5 dB at 5.73 GHz and an average noise figure of 4.4 dB. $|S_{11}|$ and $|S_{22}|$ were below -10 dB across the entire bandwidth with minimum values of -13 dB and -33 dB, respectively. Using a fundamental frequency of 3.1 GHz, the simulated IIP₂ and IIP₃ were at 10.71 dBm and at 20.76 dBm with 2nd and 3rd order harmonic tones at 6.2 GHz and 9.3 GHz, respectively. In simulations, the LNA required a 10.3 mA of current from a 1.8 V supply.

The measured results for the LNA showed a voltage gain of 9.53 ± 0.86 dB with a 3 dB bandwidth of 7.3 GHz, a minimum $|S_{11}|$ of -9.1 dB, a minimum NF of 6.4 dB, an IIP₃ of 10.67 dBm while drawing a 12 mA of current from a 1.8 V supply.

A 50 % degradation in the $|S_{21}|$ beyond 3.26 GHz was observed during measurements compared to that obtained from simulations. It is explained that the two series-connected load inductors used to provide the total load inductance were the main reason behind that degradation. The increased parasitics to the substrate due to the doubled inductor area and the increased shunt capacitance between the input and output of the total structure resulted in a degradation in the self resonance frequency and the Q of the inductor by more than 44 % and 80 %, respectively.

The reported LNA performance makes the amplifier suitable for use in UWB front-ends that operate in the lower-band with on-chip correlators.

7.2 Contributions

The main contributions of this thesis are as follows:

- The design of a single stage, frequency-controlled feedback LNA that spans the entire UWB spectrum.
- The analysis of Miller's multiplication factors, their variation with frequency and how they were used to facilitate the power and noise matching with minimum passive components at the input of the LNA.
- The development of the design technique that successfully applied a combination of the derived design equations, a graphical design approach adopted from the literature and the ladder structure approach that utilized the resulting closed-loop input impedance as one side of the structure.
- The final two-port noise parameters expressions that demonstrated how the optimum source susceptance has been modified due to the inclusion of the feedback network and the ladder structure at the input of the amplifier.

7.3 Future Work

Several topics deserve further study to address some the problems encountered during this work and to possibly improve upon the reported performance of the amplifier.

- Inductors test structures may be fabricated to facilitate characterizing on-chip inductor performance in this technology and to further identify the feasibility of obtaining

a 7 nH on-chip inductor with a SRF well beyond the UWB operating frequencies and $Q \geq 5$.

- Laser cutting can be used to isolate the inductor L_g and use a bondwire inductor instead. The high Q of the bondwire inductors is expected to improve the noise performance of the amplifier as discussed in Chapter 5.
- Transistor test structures with layout similar to that employed in the LNA should be fabricated to obtain measured noise parameters that can be used to accurately model the noise performance.
- Since the UWB antenna designers focus on obtaining impedance matched antennas over wider bandwidths, this specification can be relaxed by investigating antenna-LNA co-design. Instead of focusing on designing well matched antenna impedance separately from the LNA, the variable nature of Miller's multiplication effect analyzed in this thesis can be investigated such that it can be used to construct one side of the ladder structure to absorb antenna complex impedance variations across the operating bandwidth. This technique may relax the impedance matching specification on both the antenna and the LNA.
- Since the amplifier is cascadable without the need for interstage matching, multiple cascaded stages of this amplifier topology may be investigated to obtain higher gain.
- The amplifier transient response was simulated using a fifth-order Gaussian monopulse. It is important to investigate the measured transient response of the amplifier to a monopulse that has a frequency content comparable with the FCC spectrum mask.

- The amplifier reported in this thesis assumed a 100 fF load capacitance. If the amplifier is to drive a bank of correlators, the use of a buffer circuit at the output of the amplifier may be investigated such that the amplifier will be capable of driving a larger capacitive load.

Appendix A

A derivation for the Feedback Amplifier S_{21} and g_m Expressions

To arrive at the Y-parameters of the circuit shown in A.1, The MOSFET Y-parameters were found to be:

$$\begin{aligned} Y_{gg} &= \frac{jC_g}{1 + jC_g Z_g}, \\ Y_{gd} &= 0, \\ Y_{dg} &= \frac{jg_m}{1 + jC_g Z_g}, \\ Y_{dd} &= Y_{DS}, \end{aligned}$$

Adding the shunt feedback admittance Y_{FB} ;

$$Y_{Transistor+Y_{FB}} = \begin{pmatrix} \frac{j\omega C_g}{1+j\omega C_g Z_g} + Y_{FB} & -Y_{FB} \\ \frac{g_m}{1+j\omega C_g Z_g} - Y_{FB} & Y_{DS} + Y_{FB} \end{pmatrix} \quad (\text{A.0.1})$$

Adding the series feedback impedance;

$$Z_{Total} = \begin{pmatrix} Z_S & Z_S \\ Z_S & Z_S \end{pmatrix} + \begin{pmatrix} \frac{j\omega C_g}{1+j\omega C_g Z_g} + Y_{FB} & -Y_{FB} \\ \frac{g_m}{1+j\omega C_g Z_g} - Y_{FB} & Y_{DS} + Y_{FB} \end{pmatrix}^{-1} \quad (\text{A.0.2})$$

In [50], a minimum value of g_m is needed to guarantee that Z_S that achieves low-frequency power matching is kept non-negative. Converting the Z-parameters matrix of the total circuit to its corresponding S-parameters matrix and solving for the minimum

Figure A.1: A small-signal equivalent circuit of the shunt-series feedback of the amplifier

value of Z_S at perfect matching conditions, $S_{11} = S_{22} = 0$, one gets an expression for the minimum g_m to be:

$$g_m|_{S_{11}=S_{22}=0} \simeq \frac{Y_0^2}{Y_{FB}} - Y_{DS} - j\omega C_g \left(\frac{Y_{DS}}{Y_{FB}} + 1 \right) \quad (\text{A.0.3})$$

In (A.0.3), Z_g was ignored based on the assumption that the transistor width was split into multiple gate fingers and each gate finger was contacted from both sides in the layout. The operating power gain was found from S_{21} which is given by:

$$S_{21} = - \frac{2(g_m - Y_{FB})Z_0}{1 + j\omega C_g Z_0 + Y_{DS}Z_0 + 2Y_{FB}Z_0 + j\omega C_g Y_{DS}Z_0^2 + g_m Y_{FB}Z_0^2 + j\omega C_g Y_{FB}Z_0^2 + Y_{DS}Y_{FB}Z_0^2} \quad (\text{A.0.4})$$

If Y_{FB} that achieves the perfect power matching in (A.0.3) is used, the forward transmission becomes:

$$S_{21}|_{S_{11}=S_{22}=0} \simeq \frac{2j(gm^2 Z_0^2 - 1 + j\omega C_g g_m Z_0^2 + g_m Y_{DS} Z_0^2 + j\omega C_g Y_{DS} Z_0^2)}{-2j - 2jg_m Z_0 + 2\omega C_g Z_0 - 2jY_{DS} Z_0 + \omega C_g g_m Z_0^2 + j\omega^2 C_g^2 Z_0^2 - jg_m Y_{DS} Z_0^2 - jY_{DS}^2 Z_0^2} \quad (\text{A.0.5})$$

, which can be written in the form:

$$S_{21}|_{S_{11}=S_{22}=0} \simeq \frac{2j \left(1 + \frac{j\omega C_g}{g_m} + \frac{Y_{DS}}{g_m} + \frac{j\omega C_g Y_{DS}}{g_m^2} - \frac{1}{g_m^2 Z_0^2} \right)}{\left(\frac{\omega C_g}{g_m} + \frac{j\omega^2 C_g^2}{g_m^2} - \frac{jY_{DS}}{g_m} - \frac{jY_{DS}^2}{g_m^2} - \frac{2j}{g_m^2 Z_0^2} - \frac{2j}{g_m Z_0} + 2\frac{\omega C_g}{g_m^2 Z_0} - \frac{2jY_{DS}}{g_m^2 Z_0} \right)} \quad (\text{A.0.6})$$

Using the fact that $\frac{g_m}{C_g} = \omega_T$, (A.0.6) can be re-written as:

$$S_{21}|_{S_{11}=S_{22}=0} \simeq \frac{2j \left(1 + j\left(\frac{\omega}{\omega_T}\right) + \frac{Y_{DS}}{g_m} + \frac{jY_{DS}}{C_g} \left(\frac{\omega}{\omega_T}\right) - \frac{1}{g_m^2 Z_0^2} \right)}{\left(j\left(\frac{\omega}{\omega_T}\right)^2 + \left(\frac{\omega}{\omega_T}\right) - j\left(\frac{Y_{DS}}{g_m}\right) - j\left(\frac{Y_{DS}}{g_m}\right)^2 - \frac{2j}{g_m^2 Z_0^2} - \frac{2j}{g_m Z_0} + \frac{2}{C_g Z_0} \left(\frac{\omega}{\omega_T}\right) - \frac{2j}{Z_0 g_m} \left(\frac{Y_{DS}}{g_m}\right) \right)} \quad (\text{A.0.7})$$

Since the device is biased such that the term $\frac{\omega}{\omega_T} \ll 1$ and assuming that $\frac{Y_{DS}}{g_m} \ll 1$, it follows that

$$S_{21}|_{S_{11}=S_{22}=0} \approx 1 - \frac{g_m}{Y_0} \quad (\text{A.0.8})$$

Given a specific S_{21} , g_m can be obtained from (A.0.8).

Appendix B

Noise in MOSFETs at Microwave Frequencies

This chapter discusses the equivalent two-port network noise parameters used to represent the dominant noise sources in a MOSFET transistor at microwave frequencies. The noise parameters of the proposed LNA will be derived in Appendix C based on the two-port network parameters presented in this chapter.

B.1 Noise sources in MOSFETs

Noise in MOSFETs at microwave frequencies is dominated by thermal intrinsic and extrinsic noise sources. Random potential fluctuations in the channel result in two intrinsic noise sources: the drain noise current, $\overline{i_{nd}^2}$, and the induced gate noise current, $\overline{i_{ng}^2}$, resulting from the coupled random potential fluctuations in the channel to the gate terminal [68, p.88]. Other intrinsic thermal noise sources arise due to [44]:

- The effective contact resistance between the metal and the gate material (i.e. vias and silicide contacts)
- The effective resistances of the gate, source and drain electrodes.

B.2 MOSFET Two-port Noise Parameters

A two-port noiseless network preceded by a voltage and a current noise sources on its input, $\overline{e_n^2}$ and $\overline{i_n^2}$, is used to represent the intrinsic noise sources of a MOSFET transistor [6].

The MOSFET drain noise current, $\overline{i_{nd}^2}$, is commonly represented by two noise sources referred back to the input of the transistor noiseless two-port network as [38]:

$$\overline{e_n^2} = \frac{\overline{i_{nd}^2}}{g_m^2} = \frac{4KT\gamma g_{d0}\Delta f}{g_m^2}, \quad (\text{B.2.1})$$

and

$$\overline{i_{n1}^2} = \frac{\overline{i_{nd}^2}(j\omega C_g)^2}{g_m^2} = \overline{e_n^2}(j\omega C_g)^2. \quad (\text{B.2.2})$$

In (B.2.1) and (B.2.2), $\gamma \approx 0.67 - 1.1$ [44] and g_{d0} is the channel conductance at $V_{ds} = 0$.

In Fig. B.1, the equivalent noise voltage and current sources are represented by their equivalent resistance, conductance and correlation admittance. (B.2.1) leads to the equivalent noise resistance given by,

$$R_n = \overline{e_n^2}/4KT\Delta f = \gamma g_{d0}/g_m^2. \quad (\text{B.2.3})$$

The two equivalent noise sources $\overline{e_n^2}$ and $\overline{i_{n1}^2}$ give rise to the channel noise current when the input is short and open circuited respectively [38]. Since the two generators give rise to the total channel noise current, they are fully correlated by the correlation admittance Y_{cor1} given by:

$$Y_{cor1} = \frac{i_{n1}}{e_n} = j\omega C_g. \quad (\text{B.2.4})$$

At high frequencies the capacitive coupling to the transistor gate along with the distributed channel resistance can be represented by a distributed RC network [68, pp.88]. As a result, the gate admittance, Y_g , possesses a real part. This gate admittance was derived by Van der Zeil in [68, p.184] to be:

$$Y_g = j\omega C_g - g_g + \text{higher-order terms} \quad (\text{B.2.5})$$

where, $C_g = 2/3C_{ox} \cdot W \cdot L$ and $g_g = C_g^2\omega^2/5g_{d0}$. The gate noise current is attributed to this real component, g_g , through the relation [68]:

$$\frac{\overline{i_{ng}^2}}{\Delta f} = 4kT\delta g_g. \quad (\text{B.2.6})$$

Figure B.1: Transistor equivalent two-port noise representation

where $\delta \approx 1.3 - 3.3$ [44]. Since part of the induced gate noise current, i_{ng} , is because of the coupling with the channel varying potential [38], this current constitutes two components; i_{ngu} , i_{ngc} . The latter is fully correlated to the drain noise current and therefore it is correlated to its input referred noise voltage generator that precedes the two-port noiseless transistor network in 4.11. Thus, we have [38]:

$$Y_{cor2} = \frac{i_{ngc}}{e_n} = j\omega C_g \frac{g_m}{g_{d0}} |c| \sqrt{\frac{\delta}{5\gamma}} \quad (\text{B.2.7})$$

where g_m is the intrinsic transconductance and $|c|$ is the correlation coefficient between i_{ngc} and i_{nd} . From (B.2.4) and (B.2.7), the total correlation admittance between the two equivalent noise generators, $\overline{e_n^2}$ and $\overline{i_n^2}$, is given by [38]:

$$Y_{cor} = Y_{cor1} + Y_{cor2} = j\omega C_g \left(1 + \frac{g_m}{g_{d0}} \cdot |c| \sqrt{\frac{\delta}{5\gamma}}\right) \quad (\text{B.2.8})$$

The uncorrelated component of the gate noise current is given by [38]:

$$\overline{i_u^2} = 4KT\Delta f \delta g_g (1 - |c|^2) \quad (\text{B.2.9})$$

leading to the uncorrelated equivalent noise conductance in Fig. B.1 to be:

$$G_u = \frac{\omega^2 C_g^2}{5g_{d0}} \delta (1 - |c|^2) \quad (\text{B.2.10})$$

Knowing R_n , G_u and Y_{cor} in (B.2.3), (B.2.10) and (B.2.8) results in a complete description of the equivalent two-port network that represents the transistor noise characteristics [6, 68]. These expressions will be used to estimate the equivalent noise parameters of the proposed amplifier circuit and to arrive at the optimum signal source admittance for power and noise matching in Chapter 4 and Appendix C.

Appendix C

A Derivation for the Feedback Amplifier Equivalent Two-Port Noise Parameters

Following the noise analysis outlined in [9] to extract the noise parameters for the circuit shown in Fig. 4.12, the noise parameters were given by (4.4.7). In order to include the effect of both the gate inductor, L_g , and the series feedback inductor L_S in the overall noise parameters, the following equations can be written. From Fig. C.1,

$$\begin{aligned} V_1 &= I_1 Z_{L_g} + e_{n1} + \hat{V}_1 + \hat{V}, \\ &= e_{n1} + (Z_{L_g} + Z_{11} + Z_S)I_1 + (Z_{12} + Z_S)I_2 - Z_{11}i_{n1} + e_{n,L_g}, \end{aligned}$$

and,

$$V_2 = \hat{V}_2 + \hat{V}, \quad (\text{C.0.1})$$

$$= (Z_{21} + Z_S)I_1 + (Z_{22} + Z_S)I_2 - Z_{21}i_{n1}. \quad (\text{C.0.2})$$

Also, from Fig. C.2,

$$V_1 = \acute{e}_n + \hat{I}_1 Z_{L_g} + \hat{V}_1 + \hat{V}, \quad (\text{C.0.3})$$

$$= \acute{e}_n + (Z_{L_g} + Z_{11} + Z_S)I_1 + (Z_{12} + Z_S)I_2 - (Z_{L_g} + Z_{11} + Z_S)\acute{i}_n \quad (\text{C.0.4})$$

and,

$$V_2 = \hat{V}_2 + \hat{V}, \quad (\text{C.0.5})$$

$$= (Z_{21} + Z_S)I_1 + (Z_{22} + Z_S)I_2 - (Z_{21} + Z_S)\acute{i}_n. \quad (\text{C.0.6})$$

Figure C.1: An equivalent two-port noise representation of the feedback amplifier with the Z_{L_g} and Z_S and their noise sources located external to the two port network. e_{n1} and i_{n1} are the equivalent voltage and current noise sources of the feedback amplifier, respectively. e_{n,L_g} is the equivalent noise voltage source of the inductor L_g .

Figure C.2: $\hat{e}_n$ and $\hat{i}_n$ are the total equivalent two-port voltage and current noise sources of the complete amplifier including Z_S and Z_{L_g} . The equivalent noise voltage source of the L_g is part of the total two-port noise representation.

Comparing equations (C.0.1), (C.0.4) (C.0.2) and (C.0.6) we get:

$$\hat{e}_n = e_{n1} - Z_{11}i_{n1} + (Z_{L_g} + Z_{11} + Z_S)\hat{i}_n + e_{n,L_g} \quad (\text{C.0.7})$$

$$\hat{i}_n = \frac{Z_{21}}{Z_{21} + Z_S} i_{n1} \quad (\text{C.0.8})$$

which lead to:

$$\hat{e}_n = e_{n1} + \left[\frac{(Z_{L_g} + Z_{11} + Z_S)Z_{21}}{Z_{21} + Z_S} - Z_{11} \right] i_{n1} + e_{n,L_g}. \quad (\text{C.0.9})$$

Since

$$i_{n1} = i_{u1} + Y_{cor}e_{n1}, \quad (\text{C.0.10})$$

Therefore,

$$\hat{R}_n = R_{n1} |1 + Y_{cor1}a|^2 + G_{u1} |a|^2 + R_{n,L_g} \quad (\text{C.0.11})$$

and

$$\overline{\hat{e}_n^2} = \overline{e_{n1}^2} |1 + Y_{cor1}a|^2 + \overline{i_{u1}^2} |a|^2 + \overline{e_{n,L_g}^2}; \quad (\text{C.0.12})$$

where

$$a = \frac{(Z_{Lg} + Z_{11} + Z_S)Z_{21}}{Z_{21} + Z_S} - Z_{11}. \quad (\text{C.0.13})$$

The correlation admittance, $\hat{Y}_{cor}$, can also be found as follows;

$$\hat{Y}_{cor} = \frac{\overline{\hat{e}_n^* \hat{i}_n}}{\overline{\hat{e}_n^2}} \quad (\text{C.0.14})$$

$$= \frac{(e_{n1}^* |1 + Y_{cor1} a|^* + i_{u1}^* |a|^* + e_{n,Lg}^*)(\frac{Z_{21}}{Z_{21} + Z_S} i_{n1})}{4KT\Delta f \hat{R}_n} \quad (\text{C.0.15})$$

$$= \frac{(e_{n1}^* |1 + Y_{cor1} a|^* + i_{u1}^* |a|^* + e_{n,Lg}^*)(\frac{Z_{21}}{Z_{21} + Z_S} (i_{u1} + Y_{cor1} e_{n1}))}{4KT\Delta f \hat{R}_n} \quad (\text{C.0.16})$$

$$= b \left[\frac{a^* (G_{u1} + R_{n1} |Y_{cor1}|^2) + R_{n1} Y_{cor1}}{G_{u1} |a|^2 + R_{n1} |1 + Y_{cor1}|^2 + R_{n,Lg}} \right]. \quad (\text{C.0.17})$$

The uncorrelated noise current equivalent conductance is given by:

$$\hat{G}_u = \frac{\overline{\hat{i}_n^2}}{4KT\Delta f} - \hat{R}_n |\hat{Y}_{cor}|^2 \quad (\text{C.0.18})$$

$$= \frac{1}{4KT\Delta f} \overline{|b(i_{u1} + Y_{cor1} e_{n1})|^2} - (R_{n1} |1 + Y_{cor1} a|^2 + G_{u1} |a|^2 + R_{n,Lg}) |\hat{Y}_{cor}|^2 \quad (\text{C.0.19})$$

$$= |b|^2 \left[(G_{u1} + |Y_{cor1}|^2 R_{n1}) - \frac{|G_{u1} b^* + R_{n1} Y_{cor1} a^*|^2}{|G_{u1} |b|^2 + R_{n1} |a|^2 + R_{n,Lg}} \right], \quad (\text{C.0.20})$$

where

$$b = \frac{Z_{21}}{Z_{21} + Z_S}. \quad (\text{C.0.21})$$

Appendix D

Substrate configuration used for ADS Momentum simulations

Substrate layers information was included in the simulator from top to bottom as follows:

- OPEN boundary with a real permittivity and permeability of 1.
- Passivation layer with a $1.6\ \mu\text{m}$ thickness, a permittivity of 7.9 and a conductivity of $1\text{e-}5\ \text{S/m}$. A real permeability of 1.
- An Upper Oxide layer width of $1\ \mu\text{m}$. A permittivity was averaged based on the thicknesses of each layer and among all of the oxide layers to give a value 3.9. A conductivity of 1×10^{-5} and a permeability of 1 were used.
- A lower Oxide layer with a $6.9\ \mu\text{m}$ thickness.
- Silicon substrate layer with a thickness of $733\ \mu\text{m}$ with a permittivity of 11.7 and a conductivity of $10\ \text{S/m}$.
- A lower ground was chosen to be a closed boundary of a perfect conductance.

Metallization layers and their mapping were implemented in momentum as follows:

- Open boundary
- Passivation
- metal strip level 6
- via56
- metal strip level 5

- Oxide layer which represented the stacked oxide layers between metal 5 and the silicon substrate.
- Silicon substrate layer
- Ground plane

Appendix E

Publications

The following is a list of articles containing various aspects of the work presented in this thesis:

E.1 Conference Articles

Y. Soliman, L. MacEachern, and L. Roy, “A CMOS ultra-wideband LNA utilizing a frequency-controlled feedback technique,” in *Proceedings of IEEE International Conference on Ultra-Wideband*, 2005.

E.2 Submitted to Refereed Journals

Y. Soliman, L. MacEachern, and L. Roy, “A CMOS ultra-wideband LNA utilizing a frequency-controlled feedback technique,” submitted in August 2005 to the *Special Issue of the Transactions on Microwave Theory and Techniques on Ultra-Wideband*.

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