Electrostatic Discharge Protection for a 10 GHz Low Noise Amplifier

by

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Abstract

Electrostatic discharge (ESD) is one of the most important failure mechanisms of integrated circuits (ICs). ESD can damage ICs during manufacture, assembly of the component on the printed circuit boards and use in the field as part of a system. Therefore, an adequate ESD protection is required to improve yield and to reduce field return due to ESD damage, consequently, it is necessary that all ICs are protected against ESD.

However, ESD protection can adversely cause degradation of IC performance, particularly on radio frequency (RF) ICs. These types of ICs are the most affected by the introduction of ESD protection, which cause the degradation of RF parameters. As a result, reduction of the RF performance degradation is highly desired and was the focus of this study.

Two LNAs, one with ESD protection and another without ESD protection were designed and implemented in 0.13 μm RFCMOS technology. The operation frequency of the LNA was 10 GHz. The ESD protection used encompasses PI topology ESD protection, comprising the primary ESD protection diodes, LNA gate inductor, secondary ESD protection diodes, and power clamps. The desired level of ESD protection for the LNA was 2000 V for the Human Body Model (HBM).

The study was limited to the verification of the degradation of the S-parameters, noise figure, and ESD protection level at the LNA input.

Comparing the simulated results of the LNA without ESD protection with the LNA with ESD protection, the only significant RF parameter degradation was observed

in the noise figure (NF). The LNA without ESD protection exhibited NF=2.4 dB, while the LNA with ESD protection exhibited NF=3.4 dB. The LNA with ESD protection passed a 2000V ESD stress without showing leakage and degradation of the S-parameters and noise.

The main contribution of this work is to show that the degradation of RF parameters can be minimized by choosing the appropriate ESD protection and by taking it into account in early stages of the design process.

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First place, I would like to thank God for giving strength and perseverance to see this project to the end.

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1 Chapter: **Introduction**

1.1 Motivation

IC design enhancements have dramatically reduced the dimensions of the IC features such as gate oxide thickness, gate width, and diffusion depth. With each new technology node, new ESD protection solutions need to be designed, tested, and validated.

Among the different types of ICs, RF ICs are the ones that pose a greater challenge from an ESD protection design perspective, due to the continue increase of the operation frequency and degradation of the RF parameters caused by introduction of ESD protection circuits. Therefore, ESD protection is a subject that must be considered in early stages of the RF circuit design in order to minimize the degradation of the RF performance.

If, after the development of an IC, it fails the ESD tests or its performance does not meet the requirements due to the interference of the ESD protection, this could cause a delay in releasing a product to production by at least 6 months, which could incur a big loss for a company by losing the market window to launch the product; not considering the cost of redesign, new masks and requalification of the product.

By considering the interaction of the ESD protection with the RF circuit in early stages of the design phase, the degradation of the RF parameters can be minimized as well as a reasonable ESD protection can be achieved.

1.2 Thesis Objectives

The objective of this research project is to build an ESD protection for an LNA circuit operating at a frequency of 10 GHz, to provide a Human Body Model (HBM) protection of at least 2000 V, while minimizing the degradation of the RF circuit performance. Comparison between the LNA performance with and without the ESD protection will be studied.

1.3 Thesis Outline

This thesis is structured in five chapters. Chapter 1 is the introduction.

Chapter two provides a background on ESD protection, including ESD testing models, ESD protection schemes, and devices.

Chapter three describes the design and layout implementation of a common source cascode narrow band LNA for 10 GHz operation frequency. It also provides an overview of the ESD protection topology chosen for this study and the results of the post layout simulations are discussed.

Then in Chapter 4 the measurement results are presented. A comparison of the RF performance between the LNA with ESD protection and LNA without ESD protection is reviewed. The ESD HBM test plan and results of both LNA designs are presented and discussed.

Finally, Chapter 5 summarizes the thesis and provides recommendation for future research topics.

2 Chapter: **ESD Protection Background**

2.1 ESD Testing Models

The three main ESD testing models at the component level that IC manufactures and end users use to qualify ICs are: the HBM, machine model (MM), and charged device model (CDM). These models try to replicate the main ESD type of stress that a device will be subjected to during its manufacturing, and handling during assembly and testing of printed circuit boards (PCB).

These three models are destructive tests, if an IC is overstressed above its ESD protection voltage threshold. The only information they provide is whether an IC has passed or failed a certain ESD voltage level. In the following sub-sections, each of these models is discussed in more detail.

The Transmission Line Pulse (TLP) testing is the only nondestructive testing model. It has become more widely used since the first commercial test equipment was developed in 1997. The TLP testing is discussed in more detail in this chapter.

Other component level testing models such as cable discharge and system level testing models, (e.g. IEC 61000-4-2) are also used by the industry, but they are not discussed in this study.

2.1.1 Human Body Model (HBM)

The first ESD HBM test standard for component testing released was the Mil-Std 883, method 3015.7 [1], still in use today for military qualification. In 1993 the ESD Association (ESDA) released its own HBM standard [2], followed by JEDEC in 1996, both used for industry qualification purposes. In 2010 JEDEC and ESDA released a joint

standard, the ANSI/ESDA/JEDC JS-001 [3], which was intended to replace the existing HBM ESD standards. The ESD testing study was done based on this joint standard.

The HBM testing was developed to emulate the discharge of a human being charged with an electrostatic voltage touching the terminals of an electronic component with a finger. The HBM network consists of a 100 pF capacitor in series with a 1.5 KOhms resistor, as showed in Figure 2.1. A high voltage supply is used to charge the capacitor with the ESD voltage and then it is discharged between two pins of the device under test (DUT).

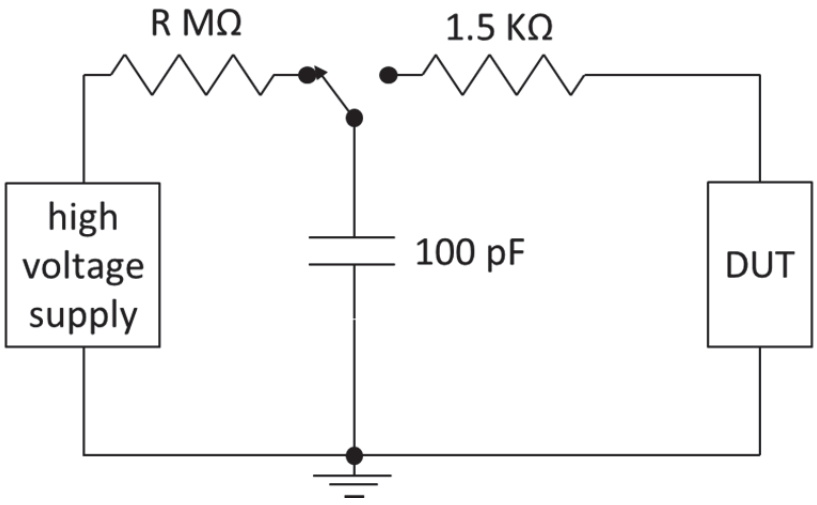


Figure 2.1 – Basic HBM Test Circuit

The basic HBM test circuit displayed in the figure above does not show the tester parasitics that are used for modeling HBM discharge, such as the stray capacitance in parallel with the 1.5 KOhms series resistance, the test board capacitance in parallel with the DUT, and the series inductance [4].

The voltage levels and classification according to ANSI/ESDA/JEDEC JS-001 [3] are shown in Table 2.1

Table 2.1 – HBM Voltage Classification Levels

Classification	Voltage Range (V)
0A	< 125
0B	125 to < 250
1A	250 to < 500
1B	500 to < 1000
1C	1000 to < 2000
2	2000 to < 4000
3A	4000 to < 8000
3B	≥ 8000

Table 2.2 based on JS-001 standard [3], provides the pin testing combination for the HBM ESD testing.

Table 2.2 – Pin Testing Combination

Configuration	Connected Individually to Terminal A (PUT)	Connected to Terminal B (Ground)	Floating Pins (Unconnected) (Must include no-connect pins)
1	All pins one at a time, except GND	GND	All pins except PUT and GND
2	All pins one at a time, except VDD1	VDD1	All pins except PUT and VDD1
3	All pins one at a time, except VDD2	VDD2	All pins except PUT and VDD2
n	All pins one at a time, except VDDn	VDDn	All pins except PUT and VDDn
n+1	All pins in IO group one at a time	All pins in IO group collectively except PUT	GND, VDD1, VDD2and VDDn

Pin Under Test (PUT)

A sample of three devices for each voltage level and pin combination shall be tested with one positive and one negative pulses.

The industry voltage protection requirement for HBM is 2000 V. This translates into a current peak range from 1.20 A to 1.48 A, a rise time from 2 ns to 10 ns, and a decay time from 130 ns to 170 ns using the short circuit method [3]. Before an HBM test is carried out, the waveform specifications of the testing equipment need to be verified.

In certain applications, such as RF circuits, in order to achieve circuit performance, lower protection voltage levels may be accepted.

There have been discussions within the industry to lower the voltage requirement for HBM to 1000 V, as based on billions of shipped devices, very few failures were attributed to HBM. This is because the manufacturing environment has improved a lot with personnel training and equipment such as air ionizers, ESD wrist straps, and ESD installations, reducing the chances of an HBM event with high voltage occurring.

2.1.2 Charged Device Model (CDM)

The first ESD CDM testing standard, JESD22-C101 [5], was released by JEDEC in 1995, followed by ESDA standard in 1997 [6].

The CDM testing was developed to emulate the discharge of an electronic component charged with an electrostatic voltage touching a grounded surface with one of the terminals. The equipment and means used for handling the devices during production can cause the ESD voltage in the device to build up, and when it touches a grounded metal surface with one of the terminals, the current discharges through the IC to ground. The CDM test circuit according to [5] is shown in Figure 2.2.

This method is also called field induced CDM because the charge is transferred to the DUT by means of a field-charging electrode, through a charging resistor (300

MOhms). Once the device is charged, a probe with 1 Ohm radial resistor touches the DUT pin discharging the voltage to ground.

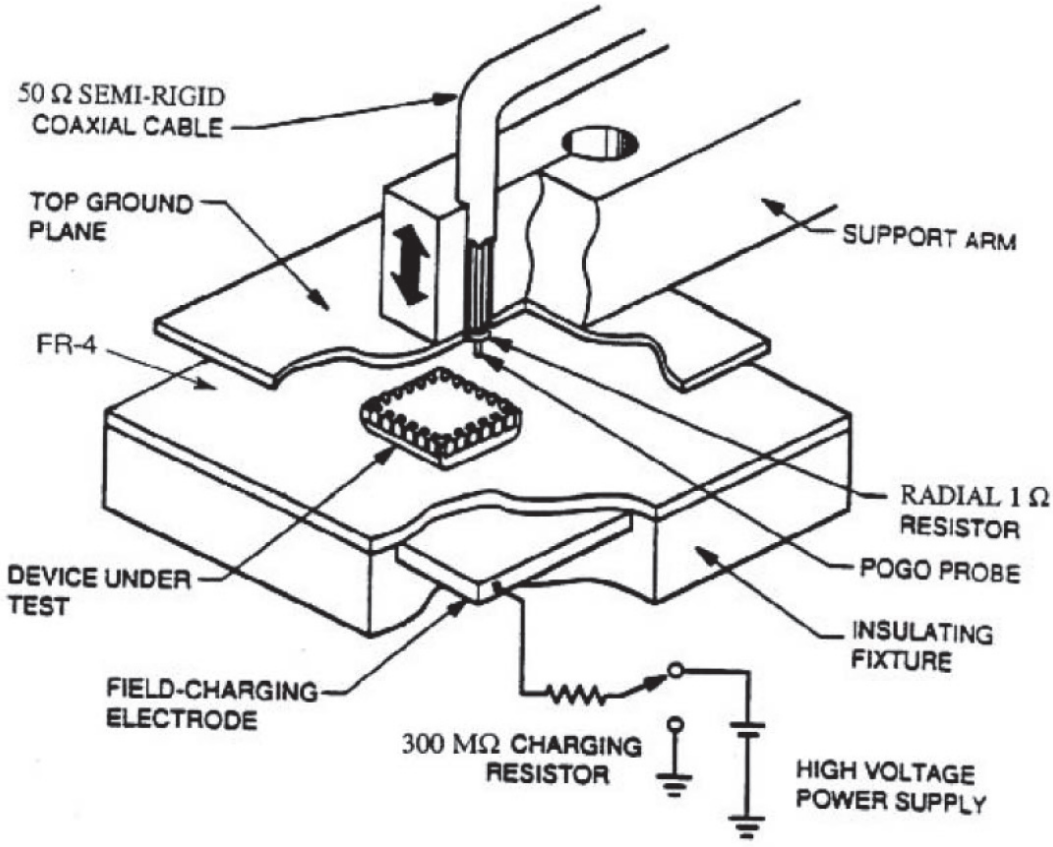


Figure 2.2 – CDM Test Circuit
(Excerpted from JESD22-C101E) [5]

A simplified CDM ESD test discharge circuit network is shown in Figure 2.3 [7].

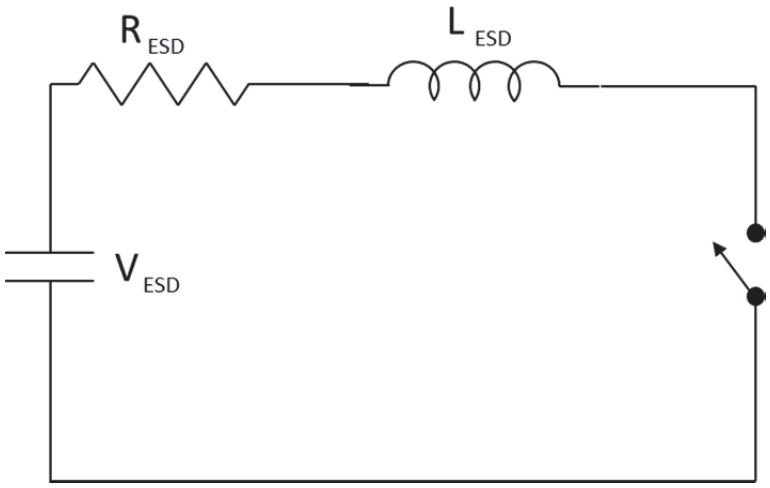


Figure 2.3 – Simplified CDM ESD Test Discharge Circuit Model

The voltage levels and classification according to JESE22-C101E [5], is shown in Table 2.3

Table 2.3 – CDM Voltage Classification Levels

Classification	Voltage Range (V)
Class I	< 200
Class II	200 to < 500
Class III	500 to < 1000
Class IV	>1000

A sample of three devices shall be tested at each voltage level. One positive and one negative ESD pulses shall be applied at each pin.

The industry voltage protection requirement for HBM is 500 V. However, the peak current associated with a certain CDM voltage, unlikely the HBM or MM, is dependent on the size of the package and of the die [8] because the bigger the package

and die sizes are, the more charge they are capable of storing. As an example, for a device with a package area of 1000 mm^2, the CDM peak current is about 10 A [8].

The CDM rise time is the fastest among the main ESD testing models and it is less than 400 ps, compared to 2 ns to 10 ns for HBM.

2.1.3 Machine Model (MM)

The ESD MM was originated in Japan [4]. The first ESD MM test standard for component testing released was the Mil-Std 883, method 3015.7 [1], still in use today for military qualification. In 1994, the ESD Association released its own HBM standard [9], the ANSI/ESD STM5.2 [10], followed by the JEDEC JESD22-A115 [11] in 1996, both to be used for industry qualification purposes.

The MM testing was developed to emulate the discharge of a piece of equipment charged with an electrostatic voltage touching the terminals of an electronic component. The MM network consists of a 200 pF capacitor in series with a 500 Ohms resistor as shown in Figure 2.4. The parasitics of the testing equipment are not shown in the basic MM test circuit.

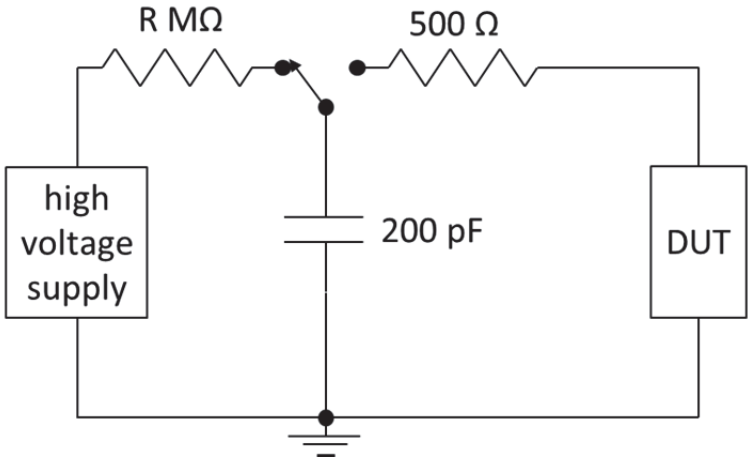


Figure 2.4 – Basic MM Test Circuit

The JESD22-115C [11] voltage levels for testing purposes are shown in Table 2.4

Table 2.4 – MM Voltage Levels

Voltage Range (V)
100
200
400

A sample of three devices for each voltage level and pin combination shall be tested with one positive and one negative pulses. The pin testing combination for MM ESD testing is the same as for HBM as shown in Table 2.2.

The industry voltage protection requirement for MM is 200 V, which translates into a current peak range from 2.8 A to 3.8 A, at a rise time of 100 ns [11].

2.1.4 Transmission Line Pulse (TLP)

The use of pulsed testing techniques to determine the ESD voltage threshold for electronic components has been studied for over 40 years. It started with Wunsch and R. R. Bell in 1968 [12], W. D. Brown in 1972 [13], and then T. Maloney and N. Khurana in 1985 [14] [9]. However, the first commercial test equipment only became available in 1997, and the first TLP testing standard, ESD SP 5.5 [15], was only released in 2004 by the ESD Association.

The TLP technique permits the study of the ESD protection behavior under short high current pulses, without damaging the device. The transmission line pulse generator

consists of a high voltage source and a transmission line cable. The transmission line cable is charged and then discharged through a resistor of at least 500 Ohms to generate the high current pulses that will be injected in the DUT. Then the IxV characteristic curve of the DUT ESD protection is measured using an oscilloscope. The pulse width can be changed by varying the transmission line length [4], which allows simulating different ESD events. A pulse of 100 ns is equivalent to a 0.66 A/1 KV HBM.

To study devices for CDM events, a very fast (VF) TLP tester is used. The pulse width is less than 5 ns [9] and the rise time in the order of hundreds of picoseconds.

2.2 ESD Protection Schemes

2.2.1 Whole Chip Unidirectional ESD Protection

In order to protect the chip against ESD discharge, all possible ESD current paths have to be accounted for. Figure 2.5 shows a generic schematic of a full chip ESD protection with all ESD modes, considering that unidirectional ESD protections are used. The arrows indicate the direction of the ESD current for each mode.

Where:

PD – Positive ESD pulse from IO to VDD

ND – Negative ESD pulse from IO to VDD

PS – Positive ESD pulse from IO to VSS

NS – Negative ESD pulse from IO to VSS

DS/SD – ESD pulse from VDD to VSS and from VSS to VDD

For each of the ESD modes listed above, it is necessary to have a defined ESD current path that will draw the current away from the main circuit, otherwise the chip will

likely be damaged.

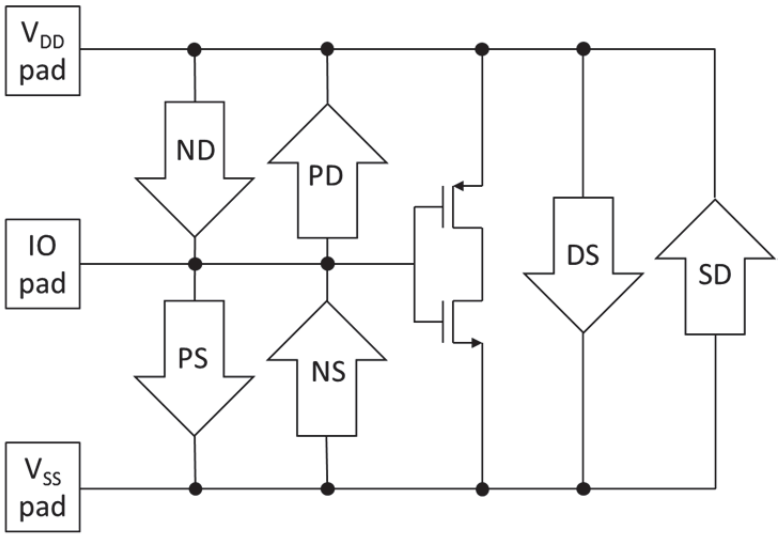


Figure 2.5 – Whole-Chip ESD Protection Scheme with Unidirectional ESD Devices

2.2.2 Whole Chip Mixed Direction ESD Protection

In practice, a full chip ESD solution usually encompasses both unidirectional and bidirectional ESD protection devices as shown in Figure 2.6. Similar to Figure 2.5, all ESD current paths are accounted for, but using less ESD protection devices, therefore, saving expensive chip area.

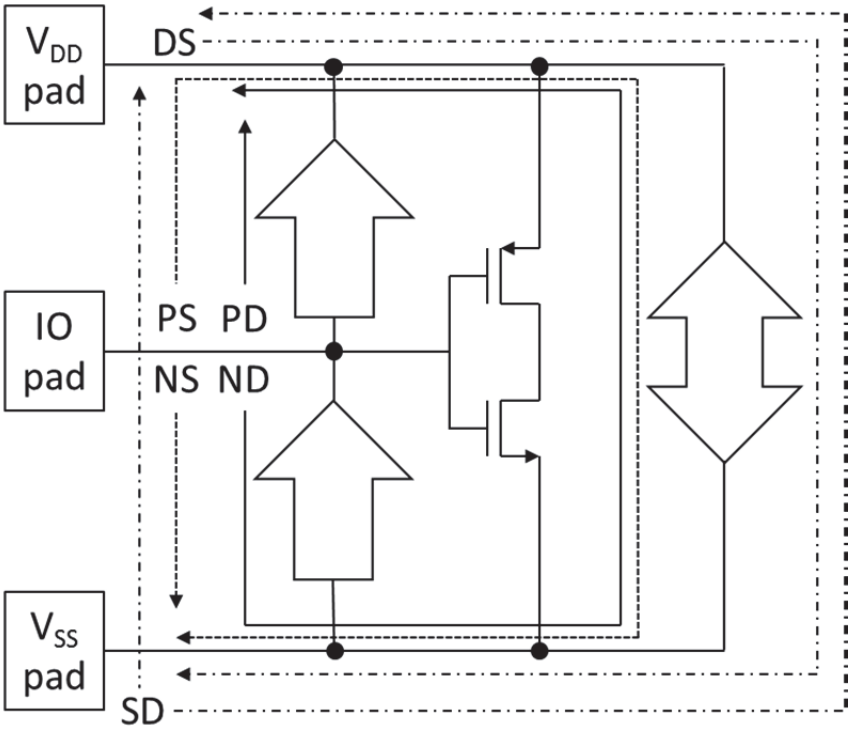


Figure 2.6 – Whole-Chip ESD Protection Scheme with Mixed Direction ESD Devices

2.2.3 Diode Based IO ESD Protection

Diodes are the most common ESD devices used for IO protection. One reverse diode is connected between the IO and V_{SS} pads and another between the V_{DD} and IO pads. This topology is commonly called double diodes, which together with the power clamp provides a good protection for HBM and MM ESD events. However, having only a primary ESD protection is not enough to protect a circuit against CDM event. In order to accomplish this, it is necessary to add a series resistor and a secondary ESD protection comprising smaller double diodes, as shown in Figure 2.7.

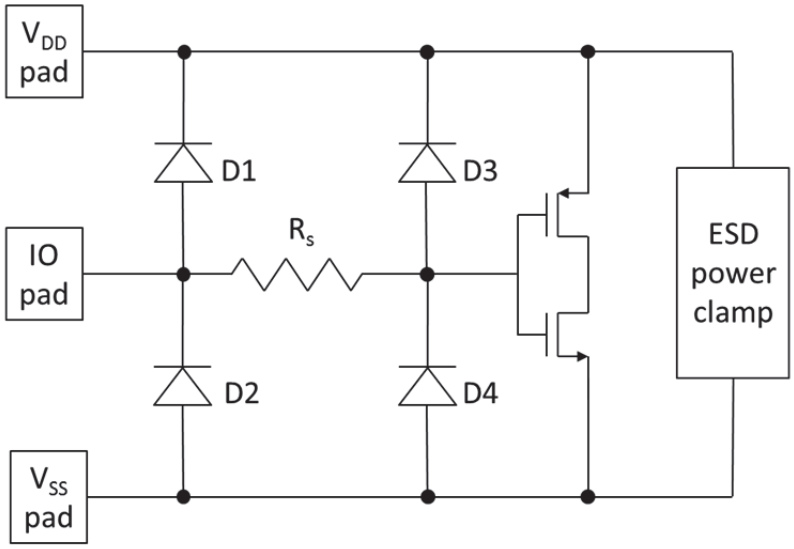


Figure 2.7 – ESD Protection Scheme for HBM and CDM ESD Events

Diodes D1 and D2 provide the primary protection for HBM/MM/CDM ESD events, and the series resistor R_S, and diodes D3 and D4 provide the secondary protection for a CDM ESD event.

The diodes D1and D2 of the primary ESD protection are the main ESD devices that will carry most of the HBM/MM current (~1.3A for 2000V HBM) and CDM current (~10A for 500V). These diodes have a large area and very small on-resistance (R_{ON}) in the order of 1 Ohm or less.

Diodes D3 and D4 of the secondary ESD protection and the series resistor R_S are used as a voltage divider between the IO pad and the input of the main circuit, in order to protect the transistor gate. Usually, the series resistor value is in the range of 50 Ohms to 200 Ohms, and as the diodes D3 and D4 don't need to carry a high current, they are small in area and consequently have a larger $R_{ON,}$ in the order of 3 Ohms to 4 Ohms.

During a CDM ESD event, without the secondary ESD protection, the current (~10 A), depending on the polarity of the voltage pulse, would follow through D1 or D2

(R_{ON}=1 Ohm), developing a voltage in the input gate of the main circuit of about 10 V, causing the gate oxide breakdown of the main circuit input MOS transistor.

However, with the secondary protection in place, the same current, considering R_S=100 Ohms and R_{ON}=3 Ohms, would develop a voltage of only approximately 0.3 V on the main circuit input MOS gate, thus protecting the gate.

2.2.4 ESD Power Clamp Placement

ESD power clamps are important elements in an ESD network. In order to work efficiently, the ESD power clamps have to be strategically placed, in order to keep low power bus resistance to any IO pin. The placement will depend on the power bus resistance and the distance of the IO pin. As the distance of an IO pin to the ESD power clamp increases, so does the path of the ESD current, as well as the voltage drop [9]. If the voltage drop is too high, it could damage the main circuit. The power bus resistance between an ESD power clamp and an IO pin should be less than 2 Ohms.

2.2.5 ESD Protection Between Different Power Domains

In order to provide an ESD current path between different power domains and lower the impedance [9], bi-directional diode strings are commonly used to allow the current to flow in both directions. Figure 2.8 shows a typical example of the ESD network. Both bi-directional diode strings between V_{DD} domains and V_{SS} domains are used. The number of diodes in the string depends, for example, on the voltage difference between the power domains, and the diodes may be sized in accordance with the desired impedance [9]. Referring to Figure 2.8, if there was an ESD power clamp between V_{DD2} and V_{SS2} of

circuit B, then the bi-directional diode string between the two V_{DD} domains could be optional.

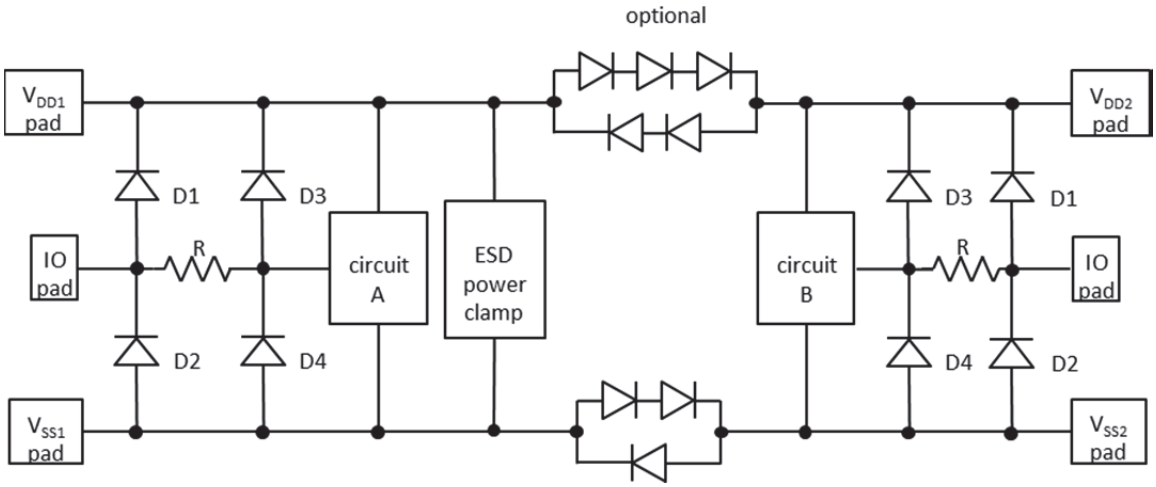


Figure 2.8 – ESD Network Between Different Power Domains

2.3 ESD Protection Devices

An ESD protection device needs to be able to withstand the high current and high voltage of an ESD event and protect the DUT at the same time. After the ESD event has occurred, the ESD protection device is required to continue functioning properly without exhibiting higher leakage current.

In this section, a brief description of the most commonly used ESD protection devices is provided, as well as the advantages and disadvantages of each one are highlighted.

2.3.1 IO Protection Devices

2.3.1.1 Diodes

The simplest ESD protection device is the pn junction diode. ESD diodes in forward bias condition have the capacity of carrying very high current density [4], and are used to protect the integrated circuit during the ESD event. The reverse-bias characteristic is used in normal operation of the integrated circuit. Figure 2.9 shows the IxV curve of a pn junction diode (not to scale). The anode is p-doped and the cathode is n-doped.

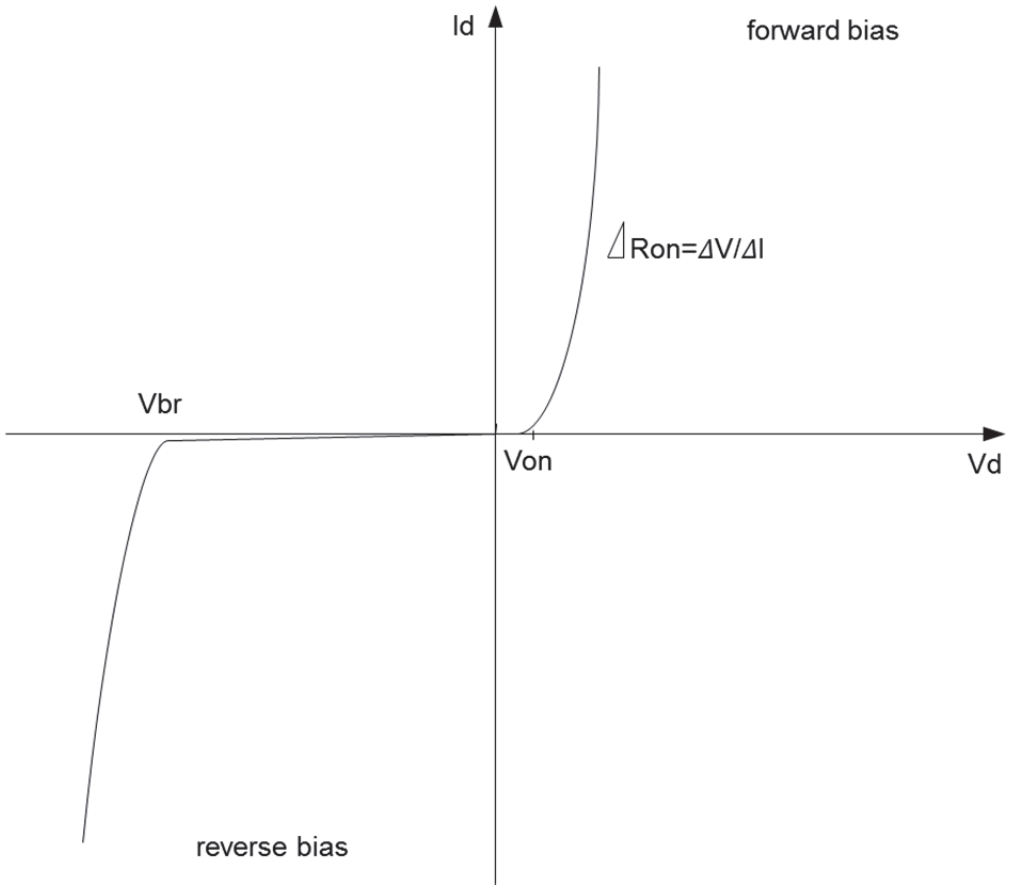


Figure 2.9 – PN Diode IxV Curve

The forward current equation for an ideal diode under low level injection [4] is expressed in (2.1):

$$\boldsymbol{I = I_0(T) \times \left[exp\left(\frac{qV}{kT}\right) - 1\right]} \tag{2.1}$$

Where: k is Boltzmann's constant ($1.38\text{x}10^{-23}\text{JK}^{-1}$), V is the voltage across the pn junction, T is the temperature in Kelvin, and I_0 is the diode saturation current expressed by (2.2).

$$\boldsymbol{I_0(T) = \frac{qAD(T)n_i^2(T)}{N_B L_d}} \tag{2.2}$$

Where: q is the electron charge, A is the area of the pn junction, $D(T)$ is the minority carrier diffusion coefficient, n_i is the intrinsic doping concentration, N_B is the minority carrier doping concentration, and L_d is the diffusion length.

During an ESD event there is a high level injection and the diode current changes, which is expressed in (2.3) [4]

$$I = I_0' exp\left(\frac{qV}{2kT}\right) \tag{2.3}$$

Where: I_0' is the saturation current at high level injection, given by (2.4):

$$\boldsymbol{I_0' = \left(\frac{2N_B}{n_i}\right) I_0 = \left(\frac{2qDn_i}{L_d}\right) I_0} \tag{2.4}$$

Now with reference to Figure 2.9, V_{on} is the voltage at which the diode starts to conduct a significant amount of current and it is generally in the range of 0.5 V to 0.7 V and is given by (2.5) [16].

$$V_{on} = \frac{kT}{q} ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{2.5}$$

Where: N_A is the acceptor impurity (Boron atoms) concentration and N_D is the donor impurity (Phosphorus or Arsenic atoms) concentration.

The diode dynamic on- resistance (R_{on}) is given by (2.6):

$$R_{on} = \frac{dV}{dI} = \frac{kT}{qI_0'} exp\left(\frac{-qV}{kT}\right), V > V_{on} \tag{2.6}$$

Equations (2.5) and (2.6) show that both V_{on} and R_{on} are process dependent, as they are functions of the doping levels and junction area. Because of its low V_{on} and R_{on} features, the diode is able to carry high forward current and dissipate high power while keeping a low internal temperature. The diode current in forward bias is in the range of 20 mA/μm to 50 mA/μm [16]. Hence, based on this current range, the size of an ESD diode necessary to withstand a 2000V HBM pulse (~ 1.3A) is in the range of 26 μm to 65 μm.

In reverse bias, the diode current is generated by avalanche breakdown and is given by (2.7) [4]:

$$I_R = \frac{qADN_CN_V}{L_dN_B} exp\left(\frac{-E_g}{kT}\right) + \frac{qW}{\tau_e}\sqrt{N_CN_V} exp\left(\frac{-E_g}{kT}\right) \tag{2.7}$$

Where: N_C is the density of states in the conduction band, N_V is the density of states in the valence band, W is the width of the depletion region, τ_e is the effective carrier lifetime, and E_g is the electrical field across the junction depletion region, which needs to be lower than the critical electrical field required for avalanche breakdown, approximately 10^5 Vcm^{-1}.

2.3.1.2 Grounded Gate NMOS (GGNMOS)

The NMOS transistor is another device used as ESD protection. It has a parasitic lateral npn bipolar transistor, where the drain is the collector, the p-sub is the base, and the source is the emitter. The NMOS transistor is used in a GGNMOS configuration, with the drain connected to the IO bond pad, and gate and source connected to the ground potential, capable of carrying high current during an ESD event. The GGNMOS configuration ensures that the transistor is turned off during the normal operation and will only turn on during an ESD event. Figure 2.10 and Figure 2.11 show a cross section (bulk substrate) and the high current IxV characteristic curve of the NMOS transistor in a grounded gate configuration, respectively.

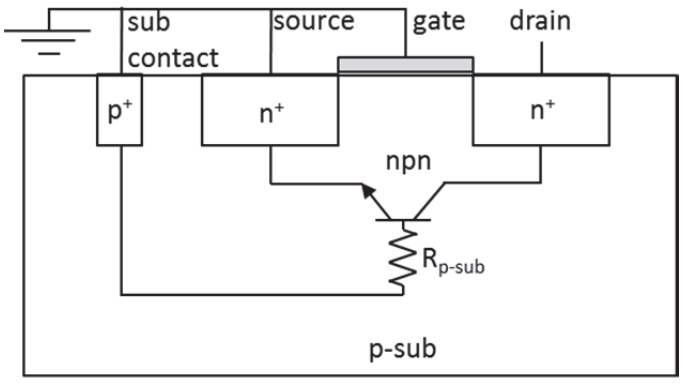


Figure 2.10 – GGNMOS Cross Section Showing Parasitic NPN Bipolar Transistor

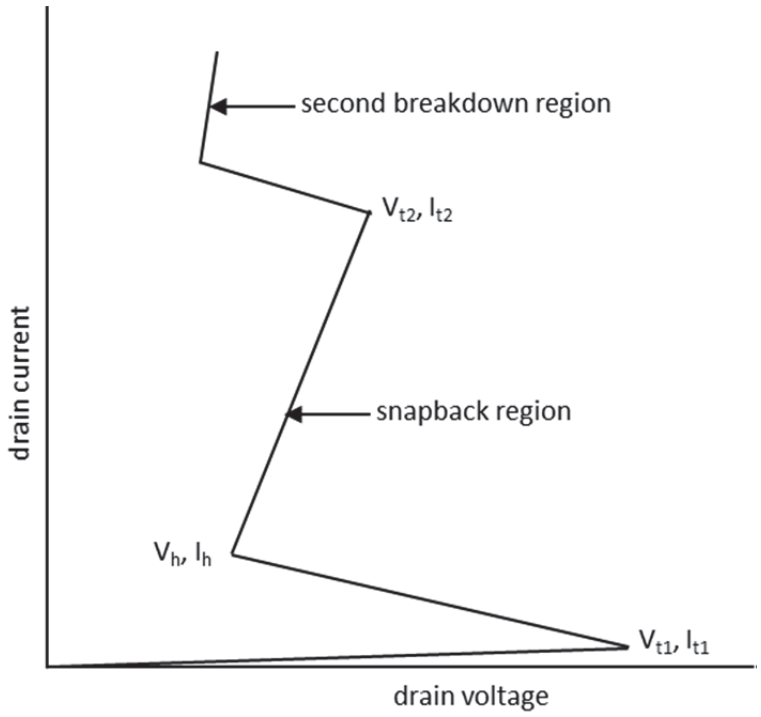


Figure 2.11 – GGNMOS High Current IxV Characteristic Curve

During an ESD event, as the voltage in the NMOS drain increases the collector to base junction of the parasitic npn bipolar transistor gets increasingly reverse biased and goes into avalanche breakdown. The positive current generated by the avalanche breakdown flows into the substrate and to ground, and the voltage drop built across $R_{p\text{-}sub}$ forward biases the base-emitter junction of the parasitic npn transistor turning it on (V_{t1}). When this happens, the voltage at the drain drops to V_h and the snapback action follows, allowing the npn transistor to carry a large amount of current, until it reaches $V_{t2,}$ where thermal breakdown occurs and the device enters the second breakdown, causing permanent damaged to the device.

The GGNMOS is implemented in a few hundred microns multi-finger configuration with silicide blocking between the poly gate and source and drain contacts,

to ensure that the fingers turn on at the same time, and a more uniform current distribution among the fingers is achieved.

In order to have an efficient ESD protection, the GGNMOS needs to meet the following requirements [16]:

- V_{t1} must be lower than the oxide breakdown
- V_{t2} must be higher than V_{t1} in order to trigger the multi-finger uniformly
- I_{t2} needs to be as high as possible, as it determines the capacity of the transistor to carry high current and not enter into thermal runaway
- V_h must be 10% to 20% higher than V_{DD} so that the NMOS is off during normal circuit operation conditions

Modified configurations of the GGNMOS and design optimizations are further described in [9], [4], [17].

2.3.1.3 Silicon Controlled Rectifier (SCR)

SCRs are another type of ESD protection that can be used either at the input or as power clamp. SCRs are intrinsic to the CMOS technology. The SCR is formed by parasitic vertical pnp and lateral npn bipolar transistors and respective n-well and p-sub, p-epi or p-well resistances depending on the process, generating a pnpn thyristor structure, as showed in Figure 2.12.

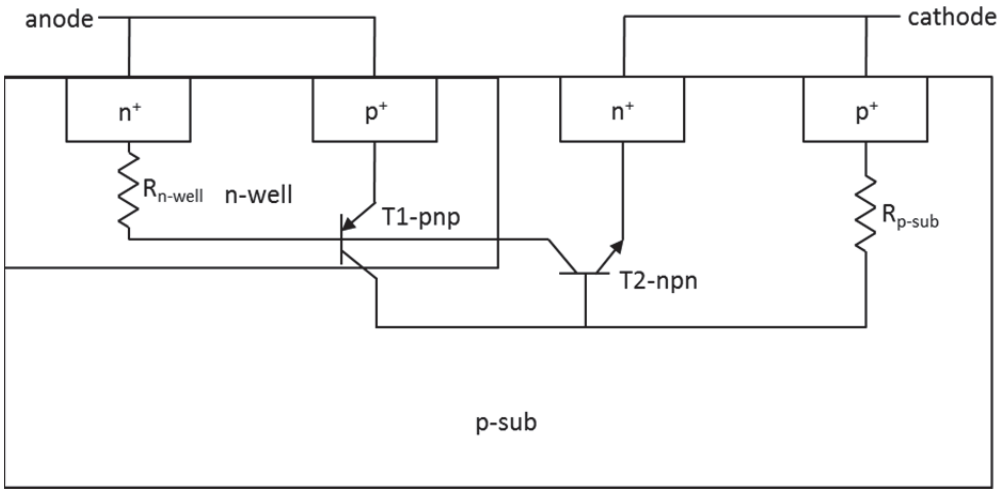


Figure 2.12 – SCR Cross Section for a Bulk Silicon Process

The following features of the SCR make it a very compelling ESD protection: fast switching from a high impedance state to a low impedance state, high current handling capability, low capacitance, and trigger voltage above the power supply voltage [9]. Their use and design have to be very carefully done, in order to properly control them and avoid false triggering during normal operation of the device.

As shown in Figure 2.12, the p^+ diffusion in the n-well and the n^+ diffusion in the p-sub form the SCR anode and cathode, respectively. The anode is connected to the IO bond pad, to which an IO signal is applied, and the cathode is connected to ground. Figure 2.13 shows an equivalent schematic circuit of the SCR.

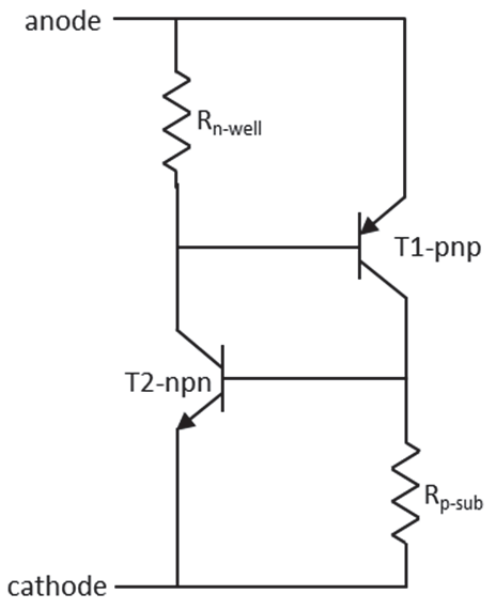


Figure 2.13 – SCR Equivalent Schematic Circuit

Figure 2.14 shows the SCR high current IxV characteristic curve. The trigger voltage (V_{t1}) and the holding voltage (V_h) on this curve are two very important parameters of the SCR. The trigger voltage is defined by the resistance of the substrate ($R_{p\text{-}sub}$), and the holding voltages by the overlap between the n-well and p^+ anode [4]. Typically, V_{t1} lies between 20 V and 25 V and V_h between 1 V and 2 V [16]. In order for the SCR to work effectively as an input ESD protection, V_{t1} has to be reduced below the oxide breakdown voltage, if no secondary protection is used, to protect input buffer transistors; for this purpose, low voltage trigger SCRs (LVTSCR) have been developed [18], [19].

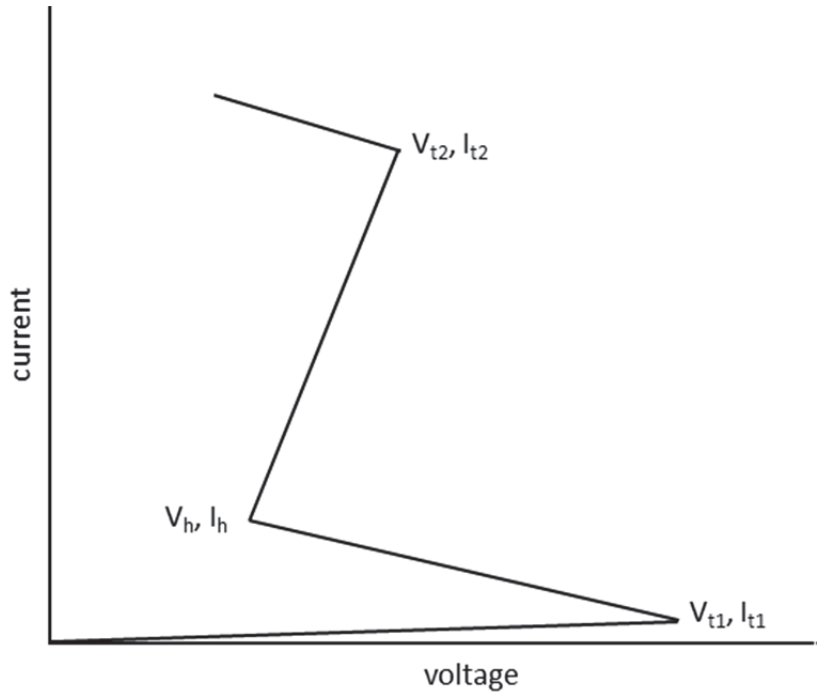


Figure 2.14 – SCR High Current I x V Characteristic Curve

2.3.2 ESD Power Clamps

An important component of the ESD protection network is the power clamp. In order to effectively protect an integrated circuit against positive, negative, pin to pin, and power to ground ESD events, it is necessary to have power clamps to conduct the ESD current between V_{DD} and V_{SS}. The power clamp needs to have a low clamping voltage in order to avoid triggering a current path through the main circuit [4].

There are two types of power clamps: static clamps, such as diode strings, MOSFETs, and SCRs that turn on when the voltage goes above a certain voltage threshold and turn off when the voltage falls below the voltage threshold; and transient-timed clamps, such as the RC clamps, which turn on when it detects a fast voltage transient of and ESD event, and turn off after a certain amount of time [16]. In the following sub-sections, the main ESD power clamps will be further discussed.

2.3.2.1 Diode String ESD Power Clamp

Diodes as ESD power clamp are often used as a forward bias string of series diodes configured as shown in Figure 2.15. The number of diodes in the string depends on the power supply voltage. This type of clamp is commonly used in mixed voltage applications [9]; the leakage, turn-on voltage and resistance are important parameters that have to be optimized during the design.

Figure 2.15 – Diode-String with Four Diodes

The diodes in the string are commonly realized by P^+/NW diodes as the emitter-base diode of a parasitic vertical pnp bipolar transistor as depicted in Figure 2.16. During operation, leakage current through the clamp can occur due to the Darlington multiplication effect [20].

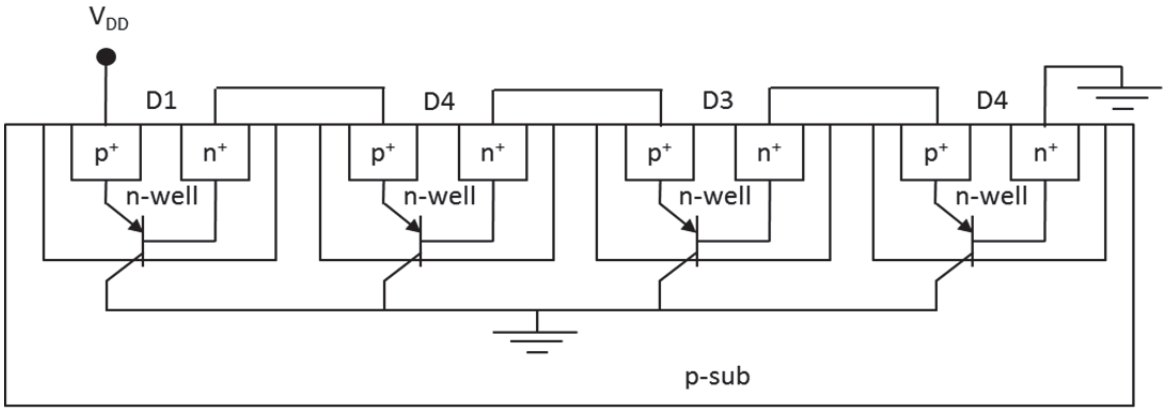


Figure 2.16 – Cross Section of P$^+$/NW Diode Showing Parasitic npn Bipolar Transistor

If the gain of the npn transistor is equal or greater than one, adding diodes to the string will not linearly increase the voltage of the diode string, rather it will cause more leakage current to flow into the substrate.

For ideal diodes, the diode string voltage increases linearly with the number of diodes in the string. However, in the case of the diode string, using the vertical parasitic pnp transistor, the voltage is given by (2.8) [21].

$$\boldsymbol{V_{trig}(I) = mV_D(I) - nV_T \times \left[\frac{m(m-1)}{2}\right] \times ln(\beta + 1)} \tag{2.8}$$

Where, $V_D(I)$ is the diode forward turn-on voltage, I is the current flowing into the diode string, V_T is the thermal voltage (KT/q), n is the ideality factor, m is the number of diodes in the string and β is the gain of the parasitic vertical pnp bipolar transistor.

From (2.8), if the gain of the pnp transistor is zero or close to zero, the voltage of the diode string increases linearly with the number of diodes, similar to an ideal diode. On the other hand, if the gain of the pnp transistor is equal to or greater than one, the diode string voltage is no longer linear, due to the leakage current flowing into the substrate, particularly at high temperatures, and a larger number of diodes would be

required to achieve a specific voltage. Alternatives to avoid the leakage current on a diode string were studied in detail in [22].

One of the ways to avoid the leakage current in the diode string during normal circuit operation, due to the Darlington action, is to decouple the diode string from the ground rail by using an RC-coupled p-channel MOSFET network, which is known as a cantilever diode string as shown in Figure 2.17 [9], [22].

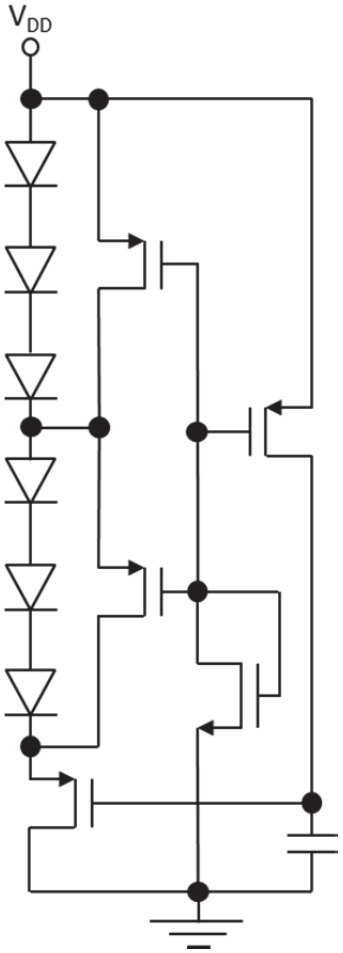


Figure 2.17 – ESD Diode String Power Clamp with Cladded Bias Network

2.3.2.2 MOSFET ESD Power Clamp

The simplest MOSFET power clamp is a GGNMOS connected between power and ground, as showed in Figure 2.18. The operation of this device was previously discussed in Section 0.

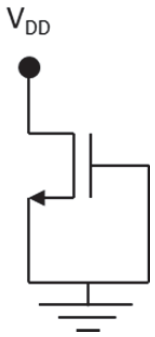


Figure 2.18 – GGNMOS ESD Power Clamp

The width of the NMOS transistor is large, typically 800 μm, in order to be able to quickly handle the ESD current [16]. Because the turn-on voltage of the parasitic npn transistor is typically about 8 V [4], it is desirable to reduce it to avoid the triggering of non-desired devices in the internal circuit; one method of doing this is to use a Zener diode connected to the gate of the NMOS, as showed in Figure 2.19 [16].

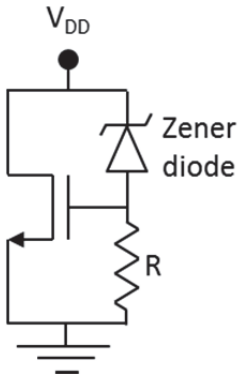


Figure 2.19 – Zener Diode Coupled NMOSFET

2.3.2.3 SCR ESD Power Clamp

The SCR functioning principles were discussed in Section 2.3.1.3. This device can also be used as an ESD power clamp. However, in order to effectively work as a power clamp, the SCR needs to have a low trigger voltage to protect the gate oxide, a holding voltage larger than the power supply voltage, and be immune to latch up and leakage due to noise pulses during normal operating conditions. Different SCR ESD networks have been proposed to satisfy the above SCR features as described in [9], [16], [23], [24], [18].

2.3.2.4 RC-Triggered MOSFET Power Clamp

The RC-triggered power clamp is a MOSFET-based ESD protection with an RC sensing circuit used to turn on the MOSFET during an ESD event. The RC network configuration circuit shown in Figure 2.20 is the most common one used because the three series inverters provide good immunity against power supply noise and latch-up during normal operation.

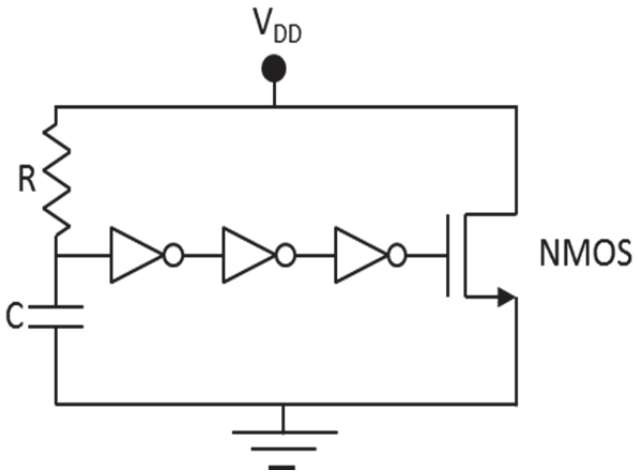


Figure 2.20 – RC-Triggered Power Clamp Circuit

As shown in Figure 2.20, the RC-triggered MOSFET power clamp comprises an RC frequency sensing circuit, an inverter drive circuit with three inverters in series, and a MOSFET output clamp [9].

The RC sensing circuit is used to keep MOSFET off during normal operation and to turn on during the transient pulse of the ESD event. Therefore, for it to work properly, it is important that the RC time constant chosen should be greater than the ESD event rise time (in the order of nanoseconds) and less than the system power-up rise time (in the order of milliseconds) [16]. The inverters are designed with increased size at each stage, in order to provide enough drive strength for the MOSFET gate [9], and to avoid false triggering of the RC-triggered sensing circuit. The MOSFET transistor must be wide enough (a few thousands of μm) to provide a low resistance shunt to ground (~0.5 Ohm) under ESD conditions to protect the gate of the MOS devices in the main circuit, and to withstand the ESD current.

One of the characteristics of the RC-triggered clamps is that they are frequency triggered instead of voltage triggered, which has the advantage of not being dependent on the turn-on voltage [9]. Other important characteristics of the RC-triggered MOSFET clamps are that they do not use parasitic elements and scale with the technology generation, which simplifies design migrations [9].

3 Chapter: **LNA Design and Analysis**

This chapter discusses the method used to design the LNA. A common source cascode LNA configuration, with a source follower output buffer, was chosen for this project. The cascode configuration is used to minimize the Miller effect of the common source transistor and to facilitate the input impedance matching. A simultaneous noise and power matching technique was used for the design.

In this chapter, it is also discussed the design of the ESD protection and how the components of the ESD protection were chosen.

3.1 LNA Design Procedure

3.1.1 Determination of Current Density for Minimum Noise

The first step is to determine the current density for minimum noise figure. This was done using the test bench circuit of Figure 3.1, where M1 and M2 are an arbitrary transistor size, e.g. a minimum length RF transistor (L=0.12 μm, finger width=4 μm, and number of fingers=40, total width=160 μm).

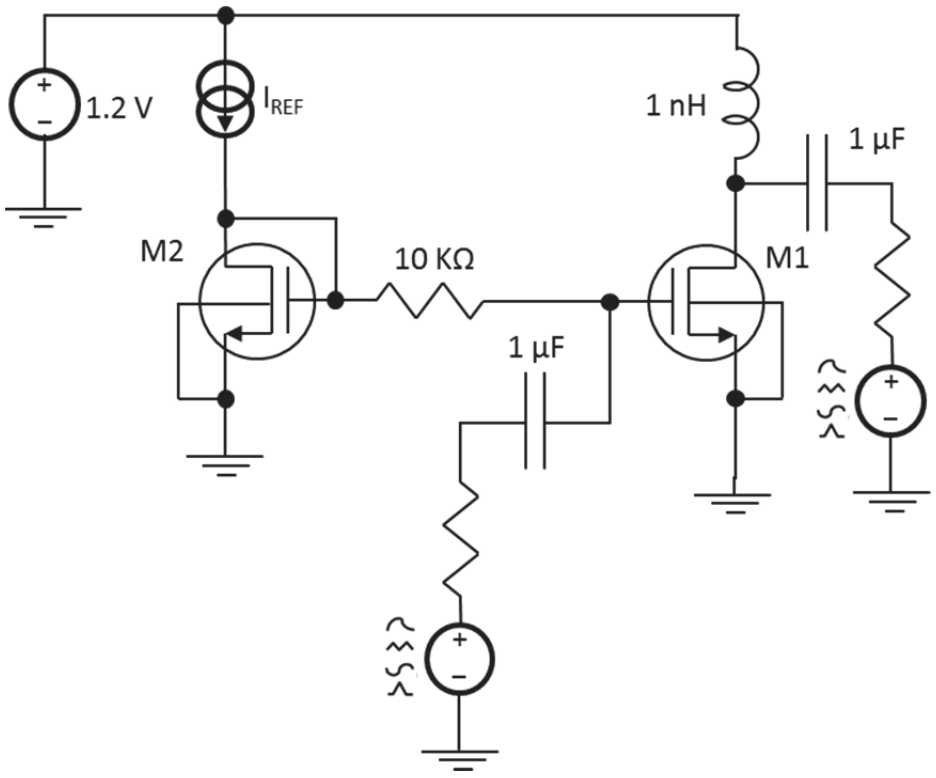


Figure 3.1 – Schematic to Simulate Current Density, f_T and G_{mim}

An S-parameter simulation was run while sweeping the current density (J), through the M1 transistor and plotting NF_{min} vs. J. The current density (J) is given by (**3**.**1**). The result of this simulation is shown in Figure 3.2, from which the following information was extracted: the minimum NF_{min} value is 591 mdB at J=29µA/µm. There is a very small change in NF_{min} for current density between 1 µA/µm and 1000 µA/µm, and NF_{min} starts increasing sharply after a current density of 1000 µA/µm.

$$\boldsymbol{J = \frac{I_{REF}}{total\ width}\ (\mu A/\mu m)} \tag{3.1}$$

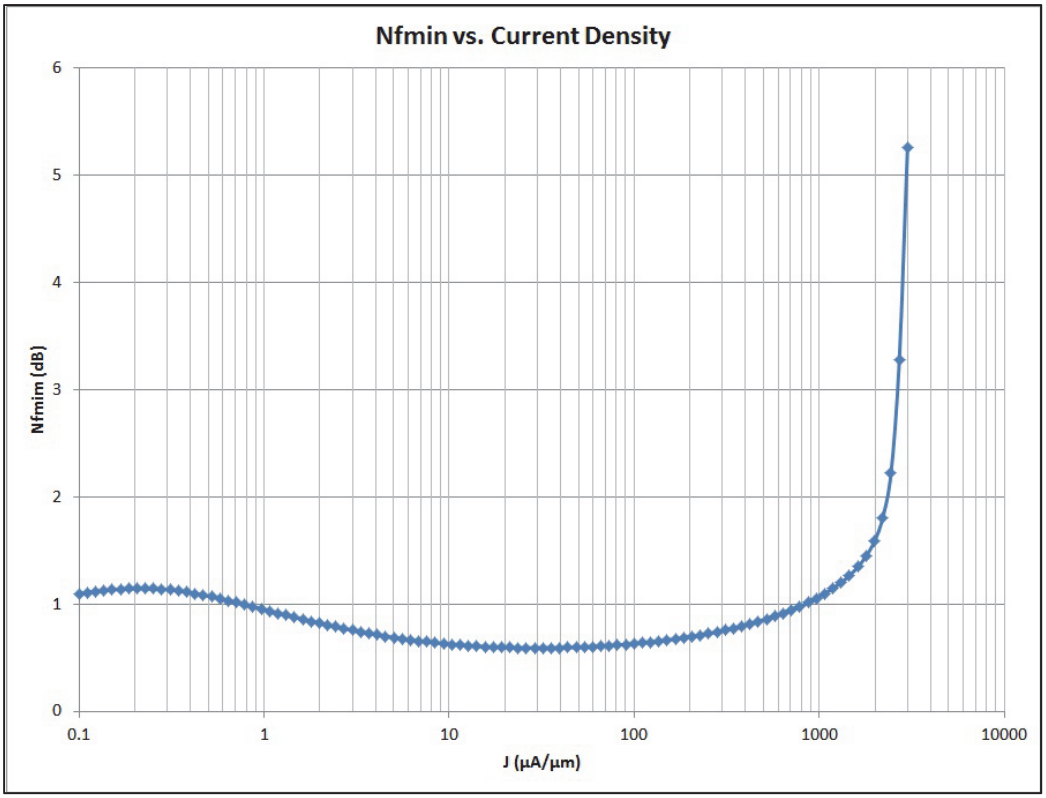


Figure 3.2- NF_{min} vs. Current Density

3.1.2 Determination of f_T

The transistor's switching frequency (f_T) is defined as the unity current gain frequency, or in other words, it is the frequency at which the current gain (H21) is equal to 1, or 0 dB, and is given by (3.2) [25]:

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{3.2}$$

f_T curve was obtained using the same test bench circuit shown in Figure 3.1. An S-parameter simulation was run while sweeping the frequency, and plotting H21 vs. frequency as shown in Figure 3.3. f_T is the frequency at which H21 is equal to 0 dB, which is 101 GHz.

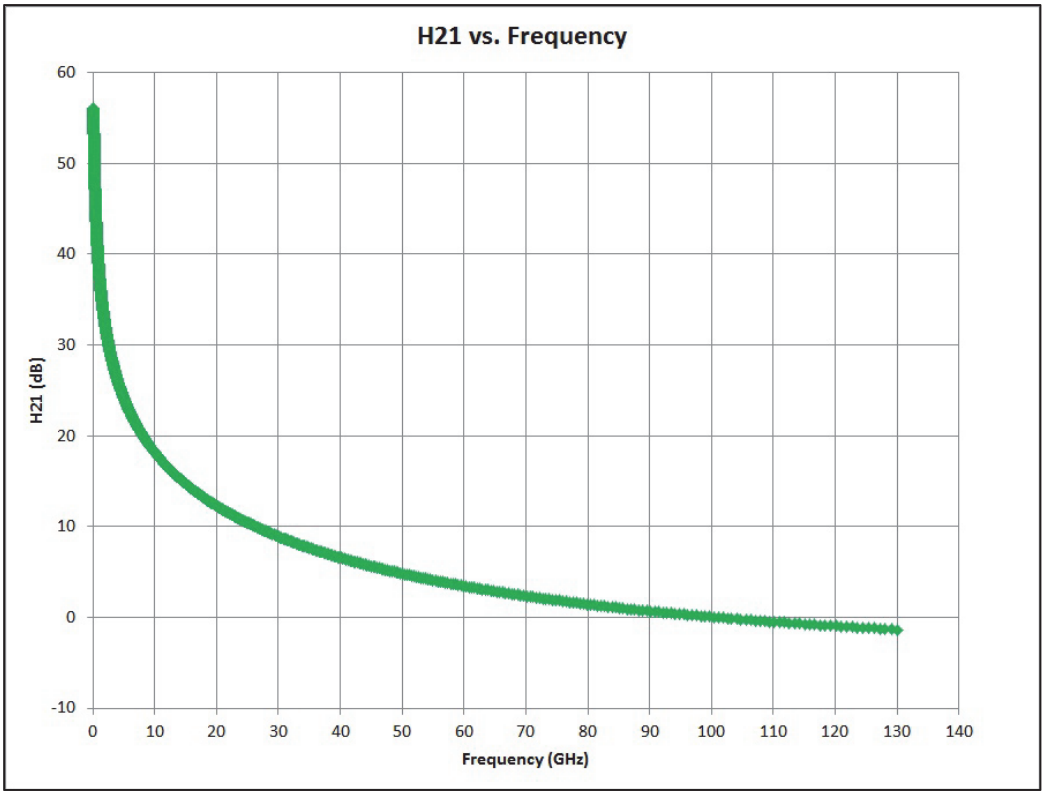


Figure 3.3 - H21 vs. frequency

It can be seen from (3.2) that f_T is a strong function of g_m, and thus depends on the current density. To understand f_T dependency of the current density, an S-parameter simulation and parametric analysis were run simultaneously while sweeping the frequency and current density, respectively, and plotting the unit gain frequency vs. the current density. The result of this simulation, as well the result of NF_{mim} vs. current density, is shown in Figure 3.4.

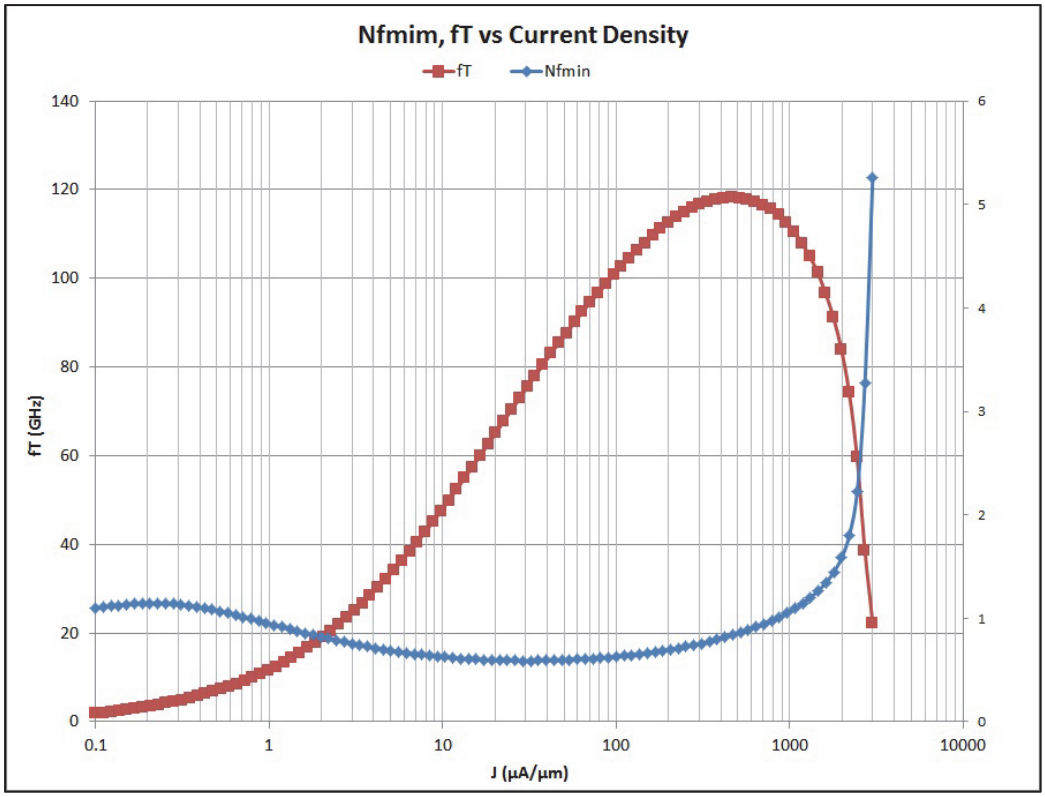


Figure 3.4 – Nf_{min}, f_T vs. Current Density

It can be seen that the maximum value of f_T is 118 GHz at J=460µA/µm, at this current density NF_{mim} is 834 mdB. On the other hand, the minimum NF_{mim} is 591 mdB at J=29µA/µm, at this current density f_T is 75 GHz. As the chosen frequency of operation is 10 GHz, there is a need to maximize f_T and therefore, a current density of 100µA/µm was chosen for this project; this will provide a higher f_T (101 GHz) in detriment of a slightly higher NF_{min} (631 mdB).

3.1.3 Determination of the Transistor Size for Optimum Source Impedance

The next step is to determine the optimum size of the LNA main input transistor. A rough estimation of the optimum transistor size can be calculated using (3.3) [26]:

$$W_{opt} = \frac{3}{2}\frac{1}{\omega L C_{ox} R_s Q_s} \tag{3.3}$$

Where ω is the frequency of operation, L is the transistor's length (0.12 μm), R_s is the signal source impedance (50 Ohms), Q_s is the quality factor of the input network (it may vary from 3.5 to 5.5), C_{ox} is oxide capacitance and is given by (3.4) [27]:

$$\boldsymbol{C_{ox}} = \frac{\boldsymbol{\varepsilon_r \varepsilon_0}}{\boldsymbol{t_{ox}}} \tag{3.4}$$

Where ε_r is the relative permittivity of SiO_2 (~3.9), ε_0 is the vacuum permittivity (~ 8.854×10^{-12} F/m), and t_{ox} is the gate oxide thickness, wherein the effective oxide thickness is 3.03 nm for the IBM cmrf8sf process. Applying these values into (3.4) results in C_{ox}=11.39 fF/μm^2.

Substituting C_{ox} value into (3.3), result in a W_{opt} between 77 μm^2 and 99 μm^2.

The optimum transistor size, considering a 50 Ohms source impedance, can also be obtained through simulation. In order to obtain maximum power transfer and minimum noise, the real part of the optimum source impedance of the transistor needs to be equal to 50 Ohms. An S-parameter simulation at the center frequency (10 GHz) was performed, by sweeping the number of fingers (nf) of the transistor (total width = nf*fw, where fw is the finger width, which was chosen to be 4 μm) while keeping the current density constant at 100 μA/um, and plotting G_{min} in the Smith chart. The width where G_{min} curve crosses the 50 Ohms circle in the Smith chart corresponds to W_{opt}. The simulation results (close-up image of the area of interest) is shown in Figure 3.5; for real part of G_{min} equal to one, the number of finger was rounded to 24, which corresponds to a W_{opt} of 96 μm.

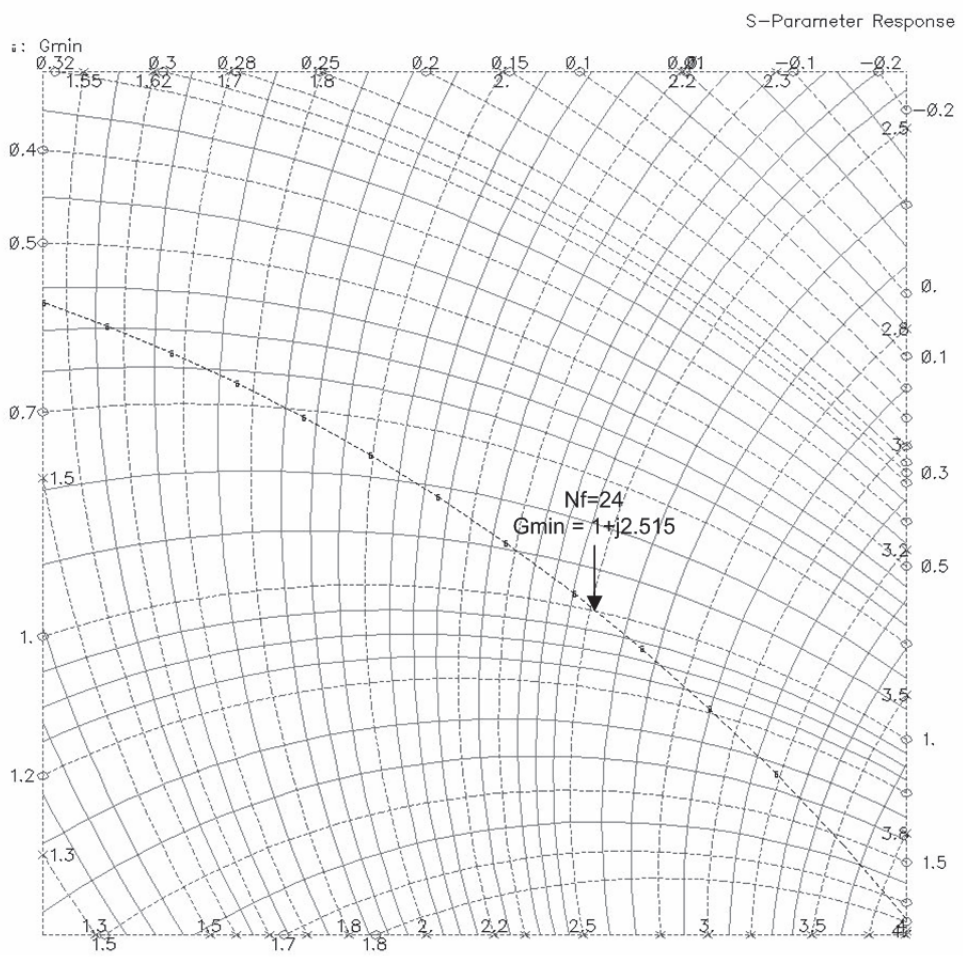


Figure 3.5 – Gmin vs. Number of Fingers

3.1.4 Determination of L_g and L_s for Input Impedance (S11) Match

L_g and L_s can be determined either using formulas, provided in the theory, to calculate the values, or using a simulation test bench.

3.1.4.1 Determination of L_g and L_s by Calculation

Next step was to determine L_g and L_s for input impedance match (minimum S11). When the input impedance is matched, S11 will be very small.

The input impedance is given by [25]:

$$\boldsymbol{Z_{in} = sL_g - \frac{1}{sC_{gs}} + sL_s + \frac{g_m}{C_{gs}}L_s \approx sL_g - \frac{1}{sC_{gs}} + sL_s + \omega_T L_s} \qquad (3.5)$$

Where, the product $\omega_T L_s$ represents the real part of the input impedance, which needs to match the 50 Ohms source impedance. In (3.5) $\omega_T = 2\pi f_T$, where f_T is the unit gain frequency of the cascode circuit shown in Figure 3.6.

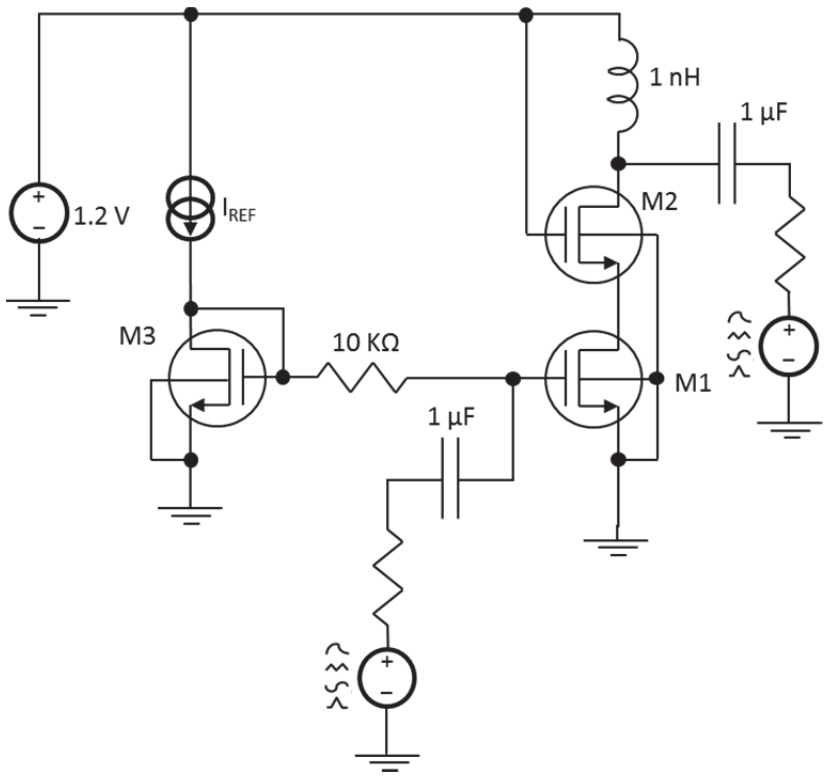


Figure 3.6 – Test Bench for Cascode f_T Characterization

The cascode f_T and NF_{min} were determined in the same way as was done for the f_T of the single transistor, but in this case using the 96 µm transistor and the current density of 100 µA/µm. The simulation results are shown in Figure 3.7. The values found for f_T and NF_{min} are 44.85 GHz and 1.40 dB, respectively.

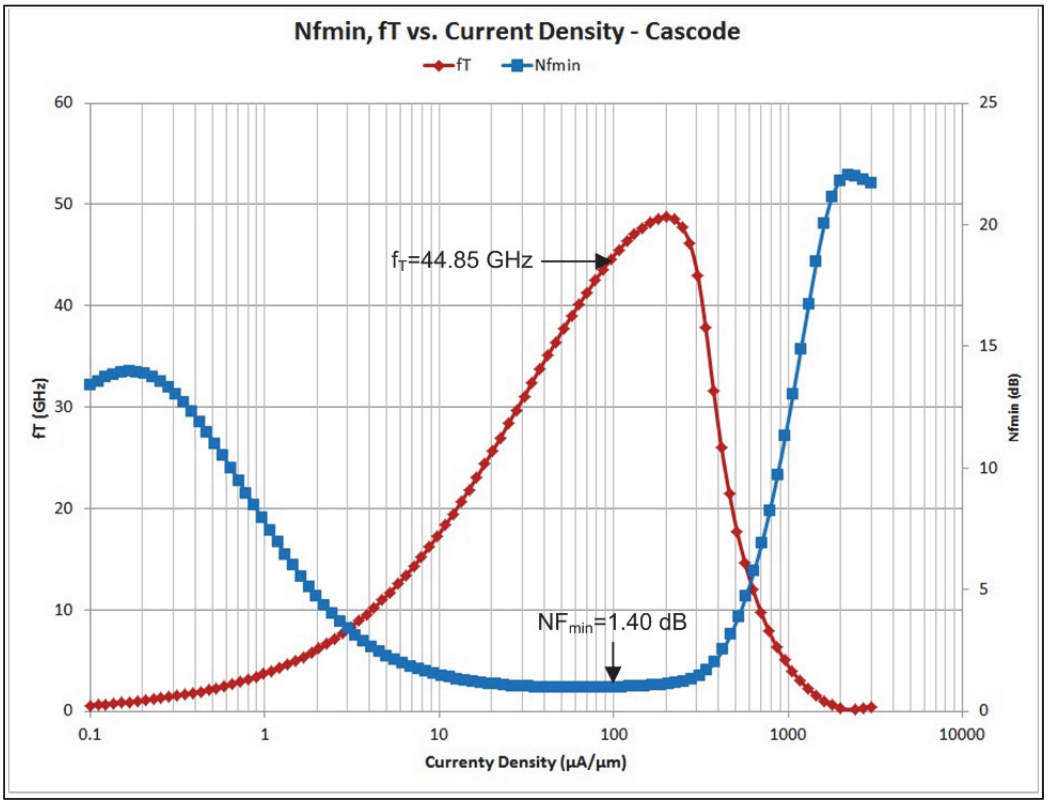


Figure 3.7 – NF_{min}, f_T vs. Current Density for the Cascode Configuration

Substituting f_T value into (3.6) results in an L_s of 177 pH.

$$\omega_T L_s = 50 \Rightarrow L_s = \frac{50}{\omega_T} = \frac{50}{2\pi f_T} \tag{3.6}$$

At the resonance, the imaginary part of Z_{in} is equal to zero. Substituting the value of L_s in (3.7) L_g can be determined, but first the value of C_{gs} needs to be found using (3.8) [25].

$$sL_g - \frac{1}{sC_{gs}} + sL_s = 0 \Rightarrow L_g = \frac{1}{s^2 C_{gs}} - L_s \tag{3.7}$$

$$C_{gs} = \gamma W L C_{ox} \tag{3.8}$$

In (3.8) γ is a parameter that depends on the technology and varies from 0.67 to 1.1, W is the transistor total width (96 µm), L is the transistor length (0.12 µm) and C_{ox} is the gate capacitance per unit area (11.39 fF/µm^2). Substituting these values in (3.8), it results a in C_{gs} in the range of 177 pF to 291 fF.

Substituting the C_{gs}, L_s and frequency values into (3.9) results an L_g range of 870 pH to 1.43 nH.

$$\boldsymbol{L_g = \frac{1}{(2\pi f_T)^2 C_{gs}} - L_s} \tag{3.9}$$

3.1.4.2 Determination of L_g and L_s by Simulation

As mentioned before, another way to determine L_g and L_s is by simulation, using the test bench circuit of Figure 3.8, and running an S-parameter simulation at the center frequency. The value of L_s can be determined by sweeping it during an S-parameter simulation and plotting S11 vs. L_s in a rectangular chart and reading the value of L_s for minimum S11 (refer to Figure 3.9). This leads to a value of L_s of 180 pH.

Similarly, the value of L_g can be determined by sweeping it during an S-parameter simulation and reading the value L_g that gives minimum S11, refer to Figure 3.10. This leads to an L_g of 1.77 nH.

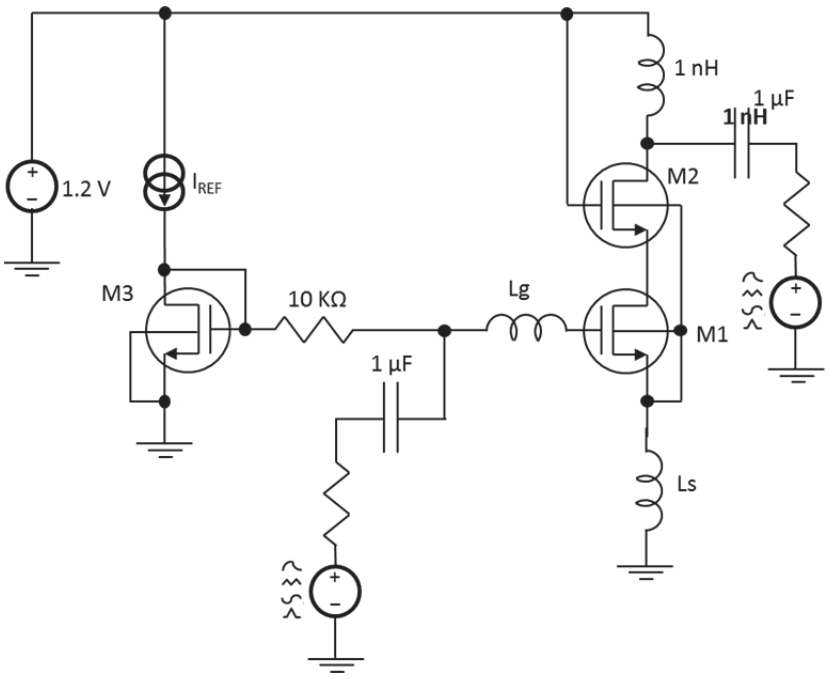


Figure 3.8 – Test Bench Circuit Used to Determine L_g and L_s

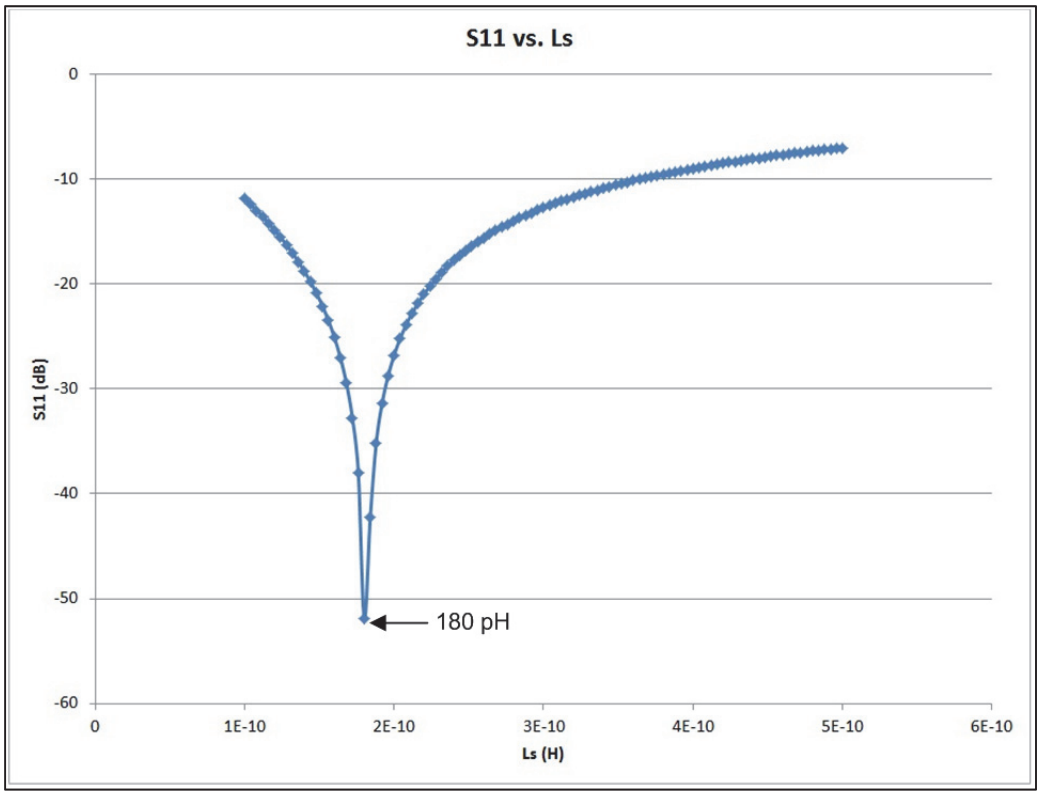


Figure 3.9 – L_s vs. S11

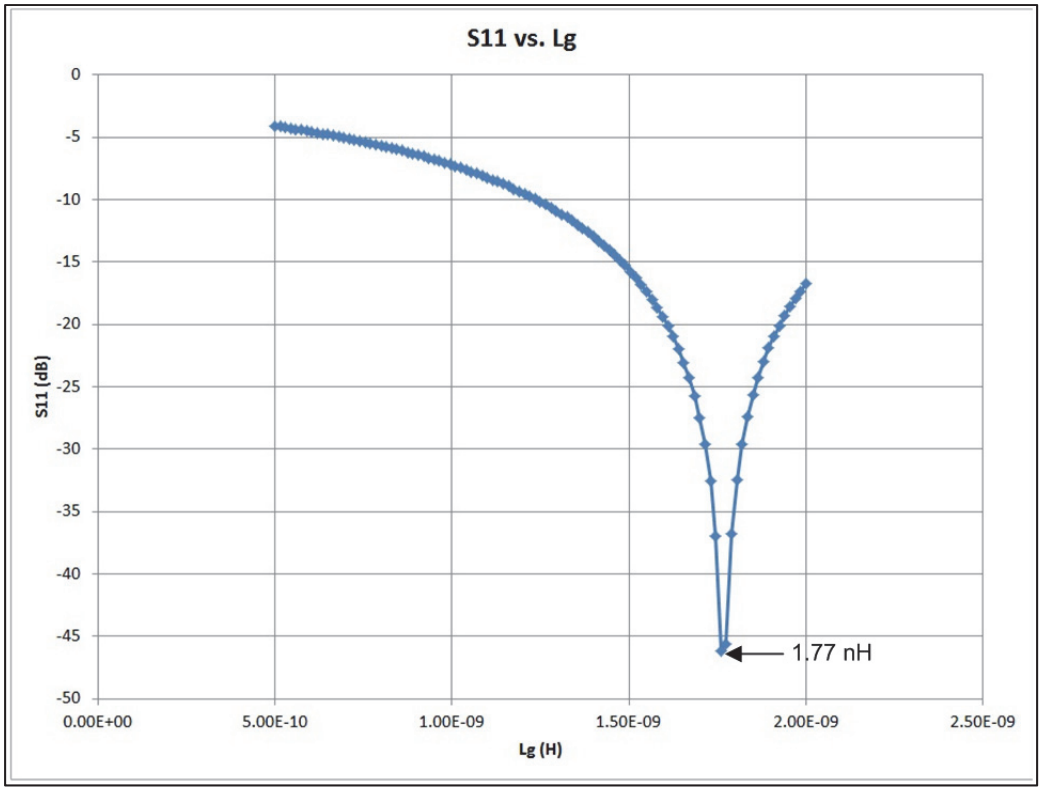


Figure 3.10 – S11 vs. Lg

3.1.5 Determination of the Tank Capacitor and Inductor

The tank capacitor and inductor must be sized, so that they are in resonance at the center frequency (10 GHz) and this is expressed in (3.10)

$$sL_t = \frac{1}{sC_t} \Rightarrow C_t = \frac{1}{s^2 L_t} = \frac{1}{4\pi^2 f^2 L_t} \tag{3.10}$$

Choosing L_t = 500 pH and substituting these values into (3.10), leads to a C_t of 506 fF.

The values obtained for L_s, L_g, L_t, and C_t are just initial values. Once they are replaced by real components, their values will have to be adjusted due to their parasitic resistance and capacitance. Moreover, parasitic capacitance and inductance of the metal interconnect introduced during the layout will lead to further adjustments of these

components. For the LNA with ESD protection, the introduction of the primary and secondary ESD protections will also require new tuning for L_s and L_g. The optimization of the values for these components will be done by performing the simulations on the final extracted circuit.

3.1.6 Design of Output Buffer Stage

The source follower output buffer stage was designed to drive an output load of 30 Ohms. As the current driven by the buffer in this case was not important, the same transistors sizes as the core LNA transistors were used.

Considering that the output impedance of the buffer is a function of $1/g_m$ of the output transistor, the buffer current had to be adjusted properly to provide an output impedance of about 30 Ohms.

3.1.7 Inductor Characterization

The test bench shown in Figure 3.11 was set up to characterize the inductors. The characterization was done only with the final values of L_s, L_g, and L_{tank}, for both LNAs, with and without ESD protection. For the L_{tank}, only one simulation was performed as both LNAs use the same inductance value. The following parameters were tweaked to obtain the highest Q as possible: inductor outer dimensions, metallization line width, and number of turns.

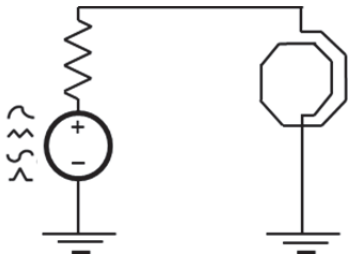


Figure 3.11 - Inductor Characterization Test Bench

An S-parameter simulation sweeping the frequency was performed and the values of L and Q were plotted against the frequency using (3.11) and (3.12), respectively. The results of these simulations are shown in Figure 3.12 to Figure 3.16, and a summary with all the final values is presented in Table 3.1.

$$L = \frac{imag(Z11)}{2\pi f} \tag{3.11}$$

$$Q = \frac{imag(Z11)}{real(Z11)} \tag{3.12}$$

The series resistance of the inductor can be calculated from (3.13).

$$Q = \frac{\omega L}{R} \tag{3.13}$$

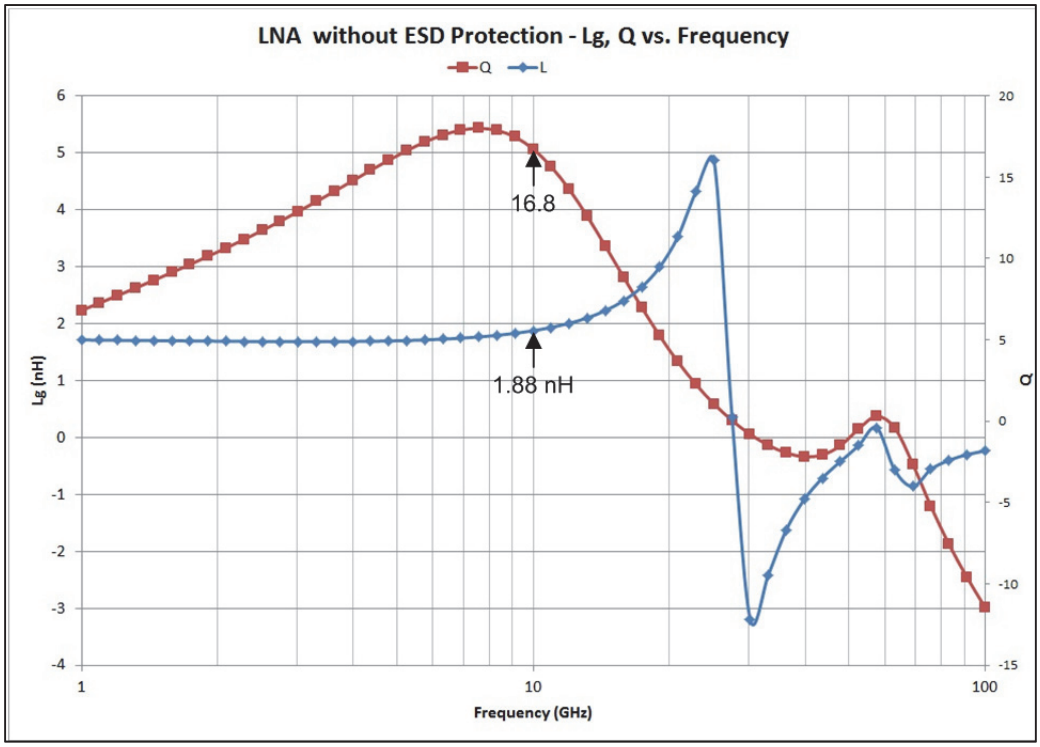


Figure 3.12 – L_g Characterization – LNA without ESD Protection

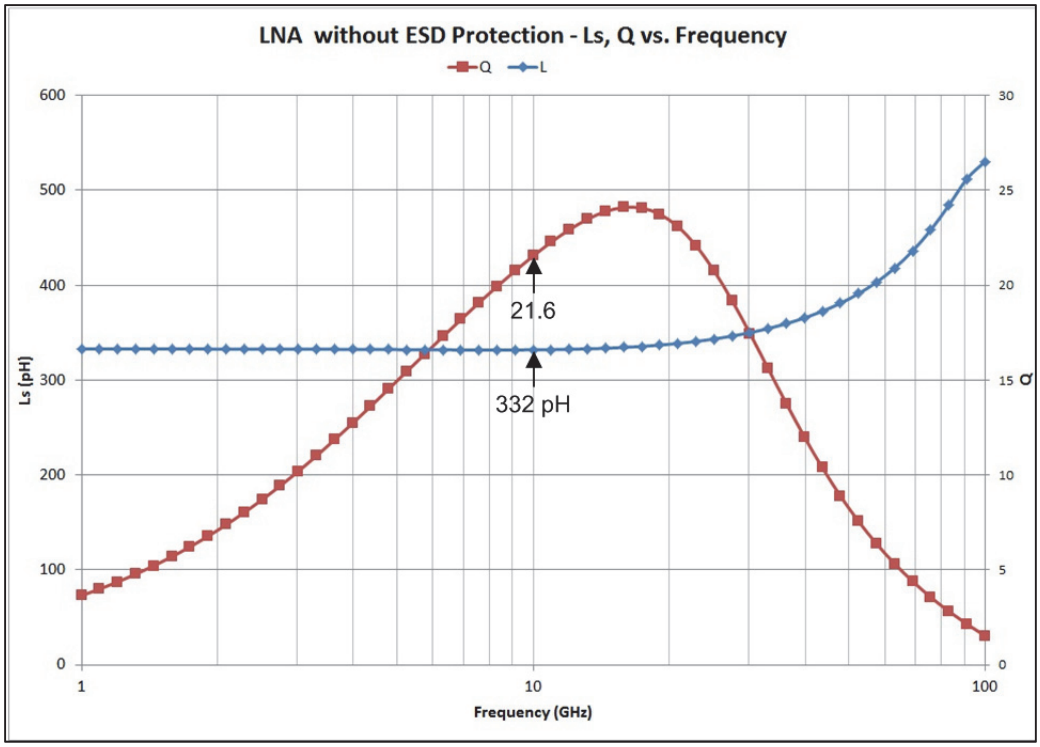


Figure 3.13 – Ls Characterization – LNA without ESD Protection

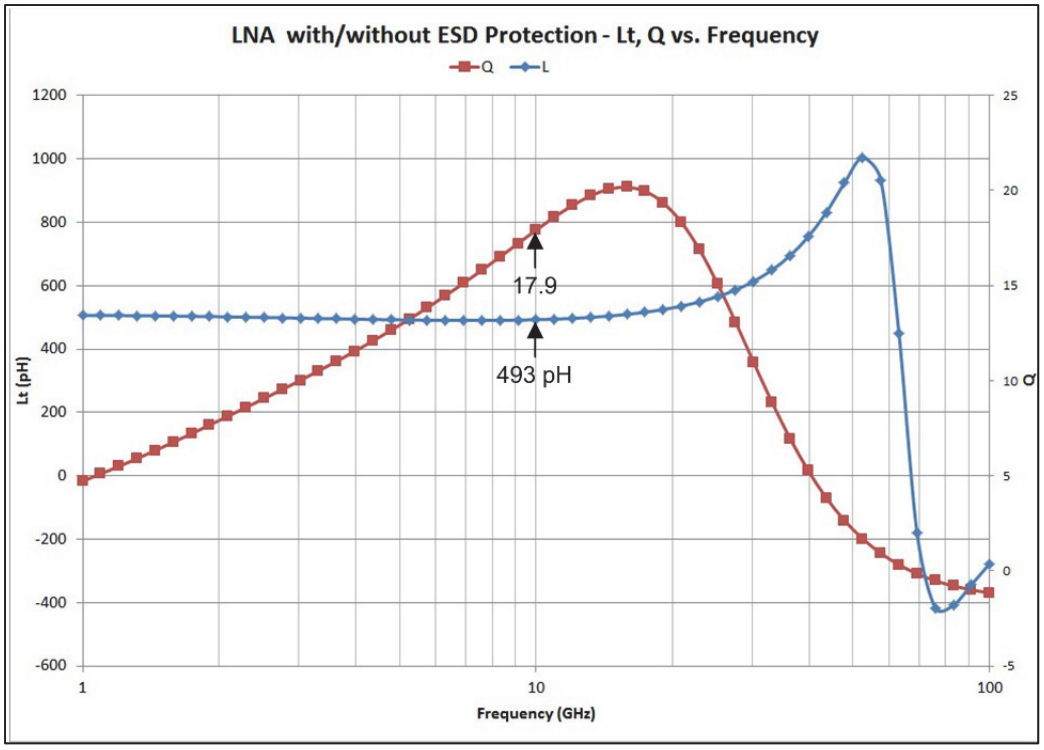


Figure 3.14 – Lt_{ank} Characterization – LNA with/without ESD Protection

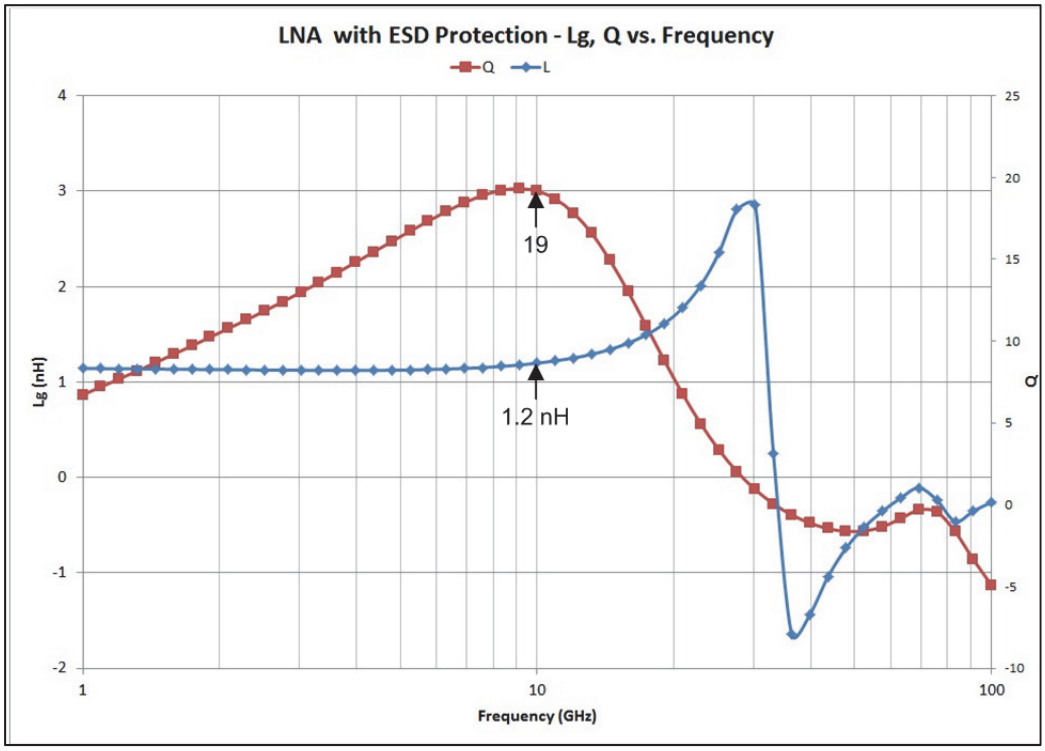


Figure 3.15 – L_g Characterization – LNA with ESD Protection

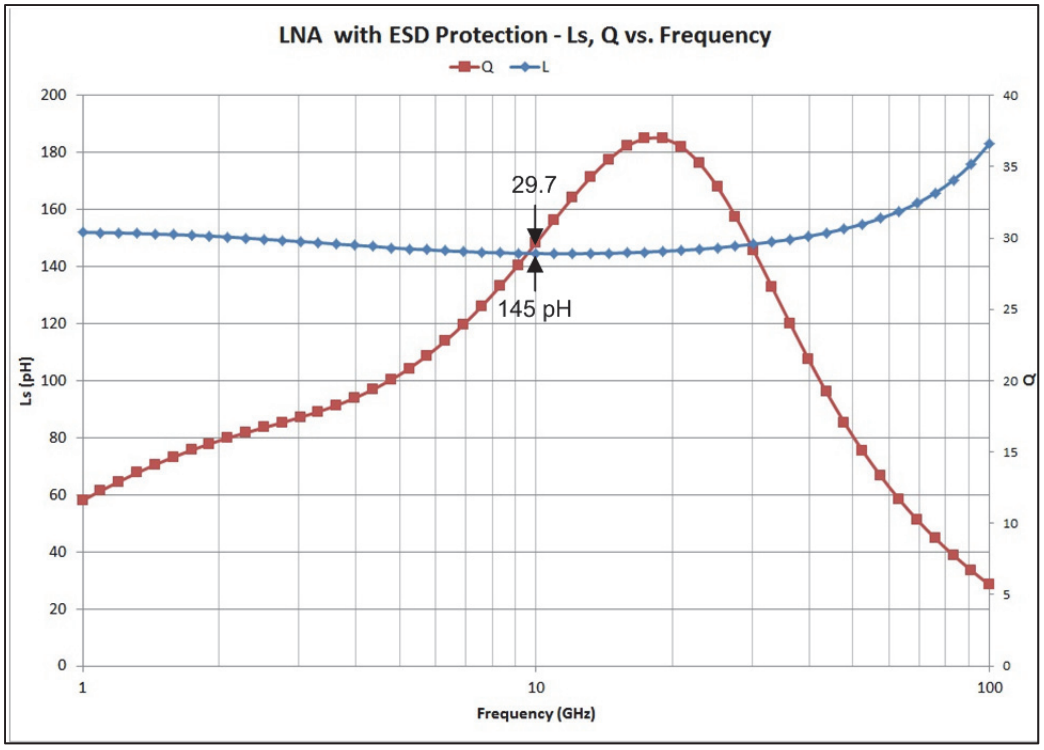


Figure 3.16 – L_s Characterization – LNA with ESD Protection

Table 3.1 – Final Inductors' Parameters

LNA	Inductor	Dimensions	Series Resistance	Inductance at 10 GHz	Q at 10 GHz
Without ESD	L_g	150 µm, 7 µm, 3.5	7 Ω	1.88 nH	16.8
	L_s	350 µm, 4 µm	1 Ω	332 pH	21.6
	L_{tank}	100 µm, 6.5 µm, 2	1.7 Ω	493 pH	17.9
With ESD	L_g	150 µm, 7.9 µm, 2.5	4 Ω	1.2 nH	19.0
	L_s	240 µm, 25 µm	0.3 Ω	145 pH	29.7
	L_{tank}	100 µm, 6.5 µm, 2	1.7 Ω	493 pH	17.9

In Table 3.1, the dimension of spiral inductors (L_g and L_{tank}) are outer dimensions, metal width and number of turns, respectively; while for the RF line inductor (L_s) dimensions are the length and width of the metal.

3.2 ESD Protection Design Procedure

3.2.1 Input ESD Protection Configuration

The parasitic input capacitance (C_p) at the input of the LNA as shown in Figure 3.17 encompasses all capacitances at the input of the LNA such as bonding pad, ESD protection network, gate-drain capacitance of M1, and wiring capacitance [28]. The use of an L-type network as shown is very restrictive and almost impossible to match the input if the parasitic capacitance is too large. As the frequency increases to GHz range, the L-type network doesn't work because the tolerated amount of parasitic capacitance decreases with the frequency [28], as showed in (3.14):

$$C_{p,max} = \frac{1}{2}\left(-C_{gs} + \sqrt{C_{gs}^2 + \frac{2C_{gs}}{R_s\omega_0}}\right) \tag{3.14}$$

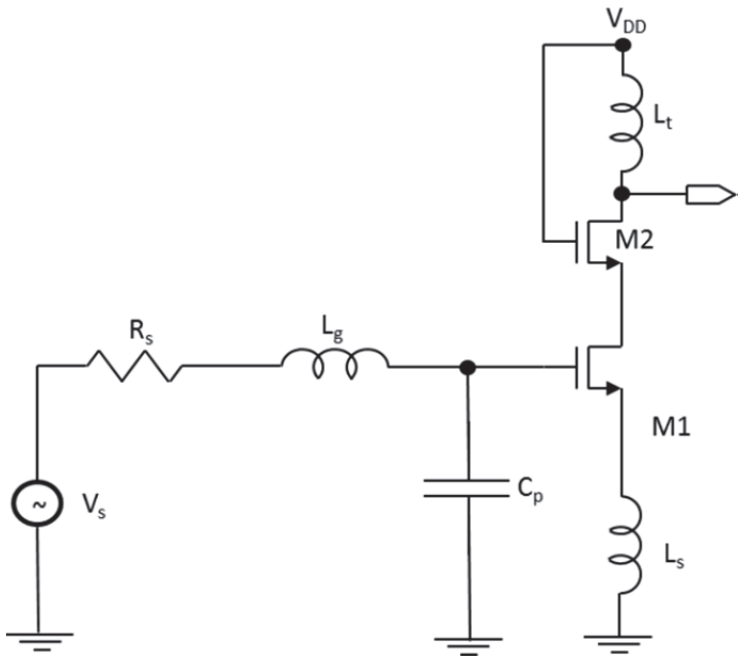


Figure 3.17 – Common Source LNA Schematic with L-Type ESD Protection

A PI-type network as depicted in Figure 3.18, offers an extra degree of freedom in comparison with the L-type network, as it has an additional component. The LNA ESD protection comprises the primary ESD protection device, the gate inductor (L_g) and the secondary ESD protection [28]. This network is very similar to the traditional ESD protection network with the current limiting resistance being replaced by an inductor.

Therefore, a PI network was chosen for this design because of the high operation frequency chosen for the LNA (10 GHz) and the additional degree of freedom that will facilitate matching the LNA input impedance.

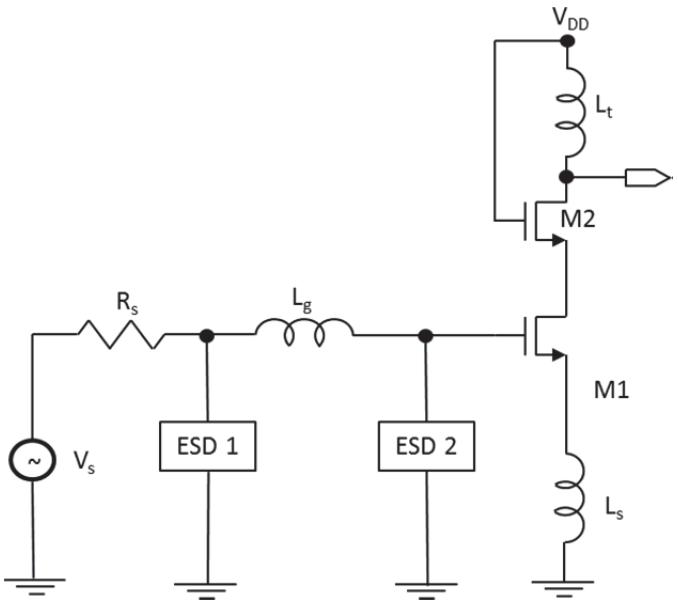


Figure 3.18 – Common Source LNA Schematic with PI ESD Protection Network

3.2.2 Input ESD Protection Devices

For the primary and secondary ESD protections, STI bounded diodes were used due to their low parasitic capacitance. The diodes were sized based on the 100 ns TLP data and other information contained in the 2007 IBM ESD Reference Guide [29]. However, presently there is a newer version of this document, the 2010 IBM Reference

Guide [30] that was not available at the time of the layout of the LNA, which would yield smaller ESD diodes based on more current TLP data. This will be further discussed in Section 5.3.

3.2.2.1 Primary ESD Protection Devices

The primary ESD protection comprises an N+/SX diode between the RF input and V_{SS} and a P+/NW 2-string diode between the input and V_{DD}. The diodes were sized to withstand an HBM ESD transient voltage greater than 2000 V.

The P+/NW 2-string diode was designed with four 55 µm long emitter fingers with a total perimeter of 440 µm; twice the size that would be required (220 µm, 2.5A) if we had only one diode. This was done to reduce in half the diode on-resistance, in order to keep the resistance of the path low, and help keep the voltage at the gate of the LNA transistor lower. The current handling capacity of the 440 µm 2-string diode is about 4 A. The capacitance of the diode was extracted through an S-parameter simulation by sweeping the frequency and plotting the capacitance value using (3.15). The result of this simulation yielded a capacitance of 127 fF at 10GHz as shown in Figure 3.19.

$$C = \frac{imag(Y11)}{2\pi f} \tag{3.15}$$

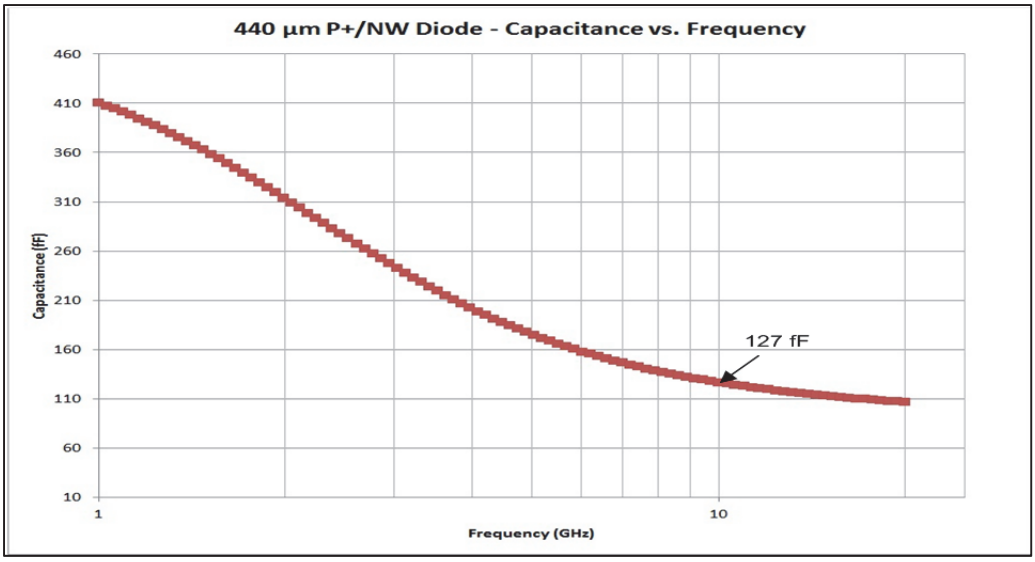


Figure 3.19 – 440 µm P+/NW Diode Capacitance vs. Frequency

The N+/SX diode was designed with three 55 µm long cathode fingers with a total perimeter of 330 µm. This translates to a maximum current carrying capacity of about 3 A during an ESD transient. A smaller diode, e.g. 220 µm with a current capacity of about 2 A, would satisfy a > 2000 V threshold voltage, but a bigger size was used instead, obtaining a current capacity closer to the 2-string diodes, in order to provide similar level of protection. The capacitance of the diode was extracted by performing an S-parameter simulation by sweeping the frequency and plotting the capacitance value using (3.15). The result of the simulation yields a capacitance of 73 fF at 10GHz as shown in Figure 3.20.

The summary of the primary diodes' design features and respective capacitance values obtained at 10 GHz are shown in Table 3.2.

Table 3.2 – Primary ESD Protection Diodes Characteristics

Diode Type	Dimensions	Capacitance (fF)
P+/NW	4 emitter fingers 55 µm finger length 440 µm perimeter	127
N+/SX	3 cathodes 55 µm finger length 330 µm perimeter	73

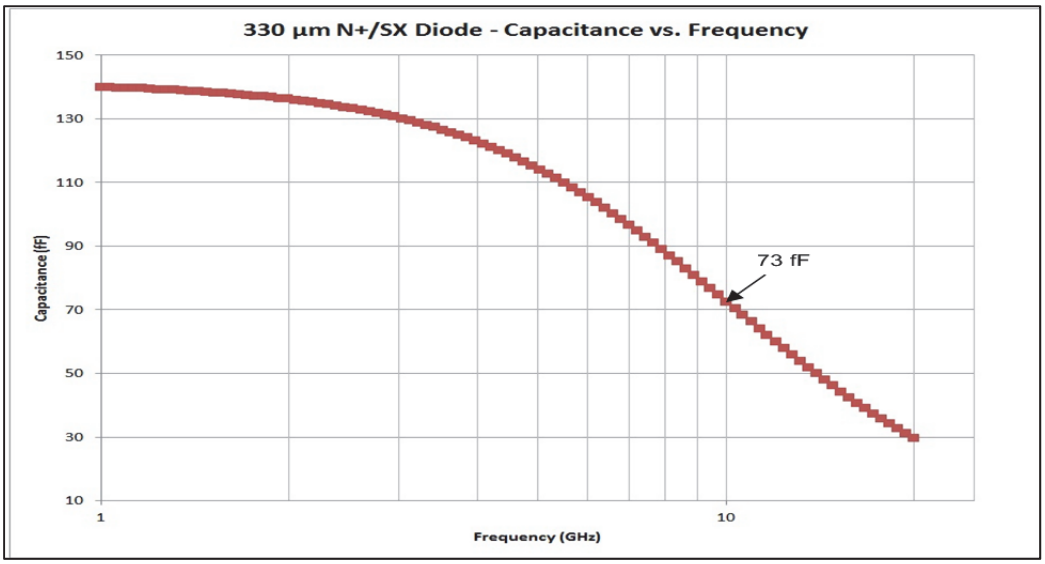


Figure 3.20 – 330 µm N+/SX Diode Capacitance vs. Frequency

A finger length of 55 µm was used for the N+/SX diode and the P+/NW 2-string diode in order to lower the anode and cathode metal interconnection resistance. Above this length value, the resistance does not decrease significantly [29]. Moreover, lower parasitic resistance will increase the diode current handling capability and also keep lower the voltage at the gate of the LNA input transistor.

3.2.2.2 Secondary ESD Protection Devices

Similar to the primary ESD protection, the secondary ESD protection also was designed with an N+/SX diode to ground and a P+/NW diode to V_{DD}. However, these diodes are smaller as most of the current flows through the primary diodes during an ESD event; most importantly, they are used to lower the voltage at the gate of the cascode LNA, mainly during an ESD CDM transient.

The fact that the gate inductor (L_g) has a series resistance (about 4 Ohms) significantly smaller than what would be recommended (50 Ohms - 100 Ohms), leads to a higher current flowing through the secondary diode during an ESD CDM transient. Consequently, the size of the secondary P+/NW and N+/SX protection diodes was designed with a perimeter of 100 µm to be able to handle a current greater than 1 A.

Table 3.3 summarizes the secondary diodes' design features and respective capacitance values, which were obtained the same way as was done for the primary ESD protection diodes. The plots of the capacitance vs. frequency for the P+/NW and N+/SX diodes are shown in Figure 3.21 and Figure 3.22, respectively.

Table 3.3 – Secondary ESD Protection Diodes Characteristics

Diode Type	Dimensions	Capacitance (fF)
P+/NW	2 emitter fingers 25 µm finger length 100 µm perimeter	87
N+/SX	2 cathodes 25 µm finger length 100 µm perimeter	38

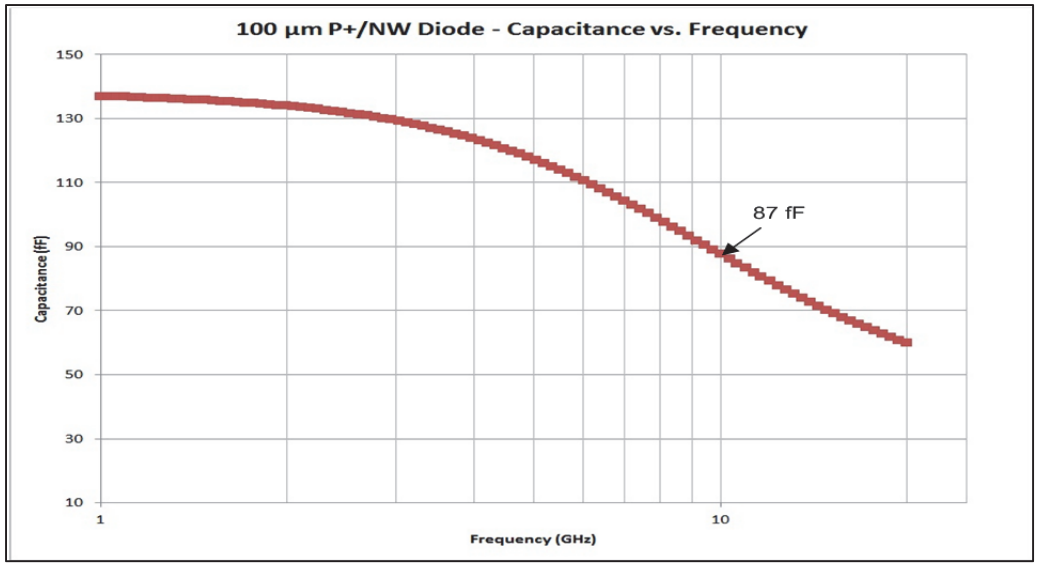


Figure 3.21 – 100 µm P+/NW Diode Capacitance vs. Frequency

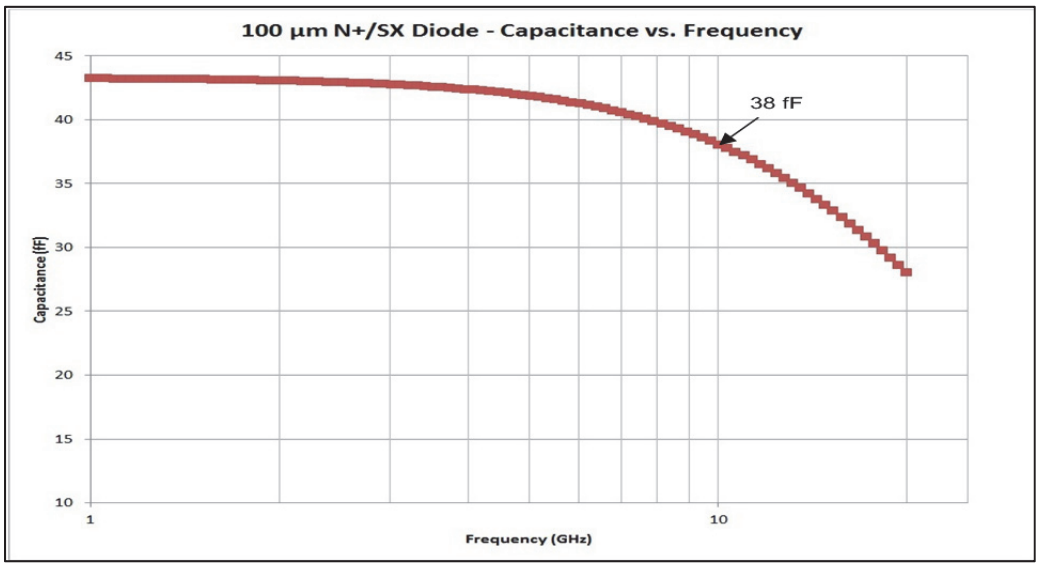


Figure 3.22 – 100 µm N+/SX Diode Capacitance vs. Frequency

3.2.3 Output ESD Protection Devices

An output ESD protection similar to the primary ESD protection was used in the output pin of the LNA. However, ESD testing will be performed only included the input pin, V_{DD}, and V_{SS}.

3.2.4 Power Rails ESD Protection

The power rails ESD protection is necessary to provide a current path between V_{DD} and V_{SS} during several ESD events. As discussed in Section 2.3.2, different options are available. The RC-triggered power clamp was chosen over the other options because it doesn't use parasitic devices, it is immune to latchup, and has very low on-resistance.

An RC-clamp with a low on-resistance is important to protect the LNA input transistor by keeping the gate voltage below the oxide breakdown voltage during an ESD event.

The RC-power clamp size was chosen based on the 100 ns TLP data [29]. A 4000 μm RC-clamp with current capacity greater than 5.5A and an on-resistance of 0.4 Ohms were used. As the RC-power clamp is placed between V_{DD} and V_{SS} it doesn't affect the RF parameters.

3.2.5 Thin Oxide FET Gates Connected to V_{DD}

A resistor was used to protect any thin oxide NFET gates that needed to be connected to V_{DD} in order to protect them against an ESD transient. As the resistance of the path to the NFET gate increases, the ESD current will find other least resistance path to flow through. This protection is specially needed during an ESD CDM event due to build up voltages higher than the oxide breakdown (~6.5 V for this technology) at the V_{DD} rail.

3.2.6 Final LNA Design Schematics

The design schematics for the LNA without ESD protection and LNA with ESD protection are provided in Figure 3.23 and Figure 3.24, respectively. The components sizes for both LNAs are listed in Table 3.4, with exception of the ESD components.

Table 3.4- LNA Components' Sizes

Component	LNA without ESD Protection	LNA with ESD Protection
LNA bias circuit resistor	732 Ω	732 Ω
LNA bias circuit NFET width	9 µm	9 µm
LNA bias circuit RF block resistor	10 KΩ	10 KΩ
Gate inductor (coil)	1.88 nH	1.2 nH
Source degeneration inductor (RF line)	348 pH	145 pH
LNA cascode NFETs width	96 µm	96 µm
Tank inductor	493 pH	493 pH
Tank capacitor	235 fF	235 fF
Tank resistor	918 Ω	918 Ω
Output buffer NFETs width	96 µm	96 µm
Output buffer bias circuit resistor	3.2 KΩ	3.2 KΩ
Output buffer bias circuit NFET width	9 µm	9 µm
All capacitors to ground	10 pF	10 pF

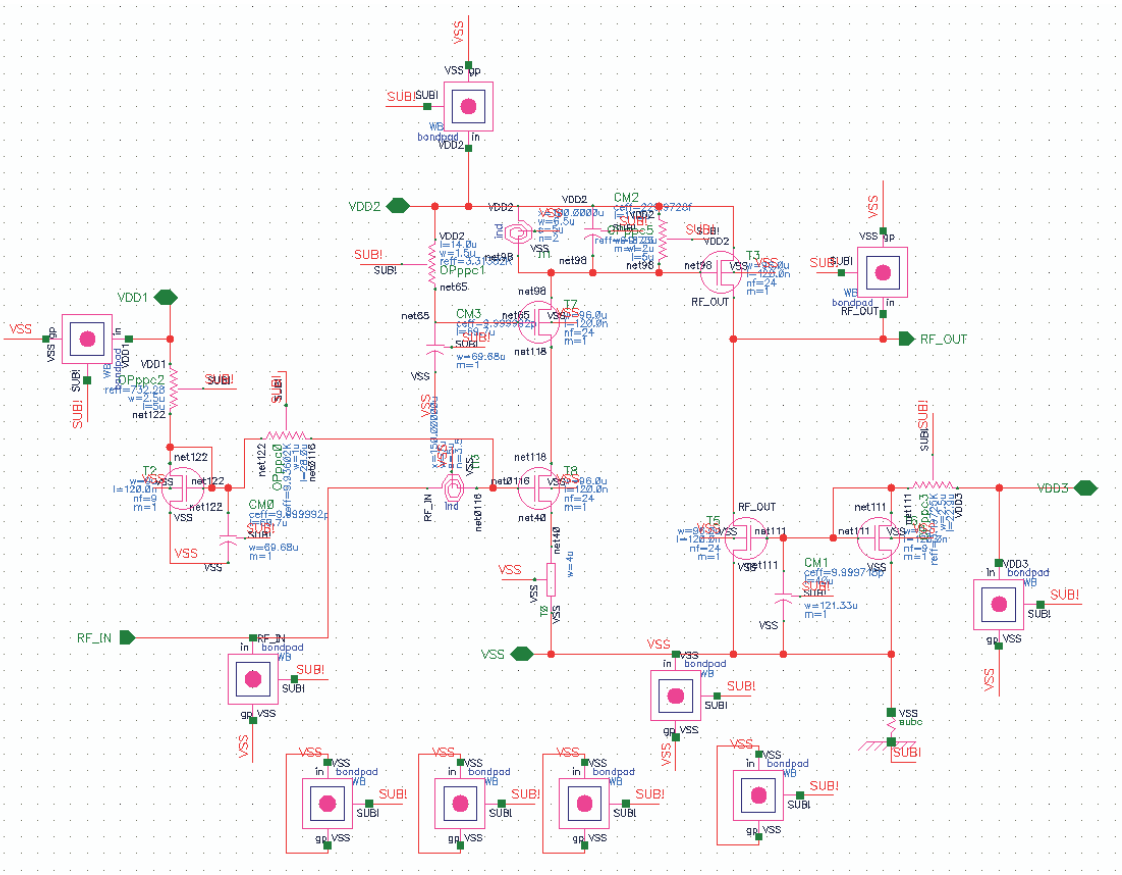


Figure 3.23 - Schematic for LNA without ESD Protection

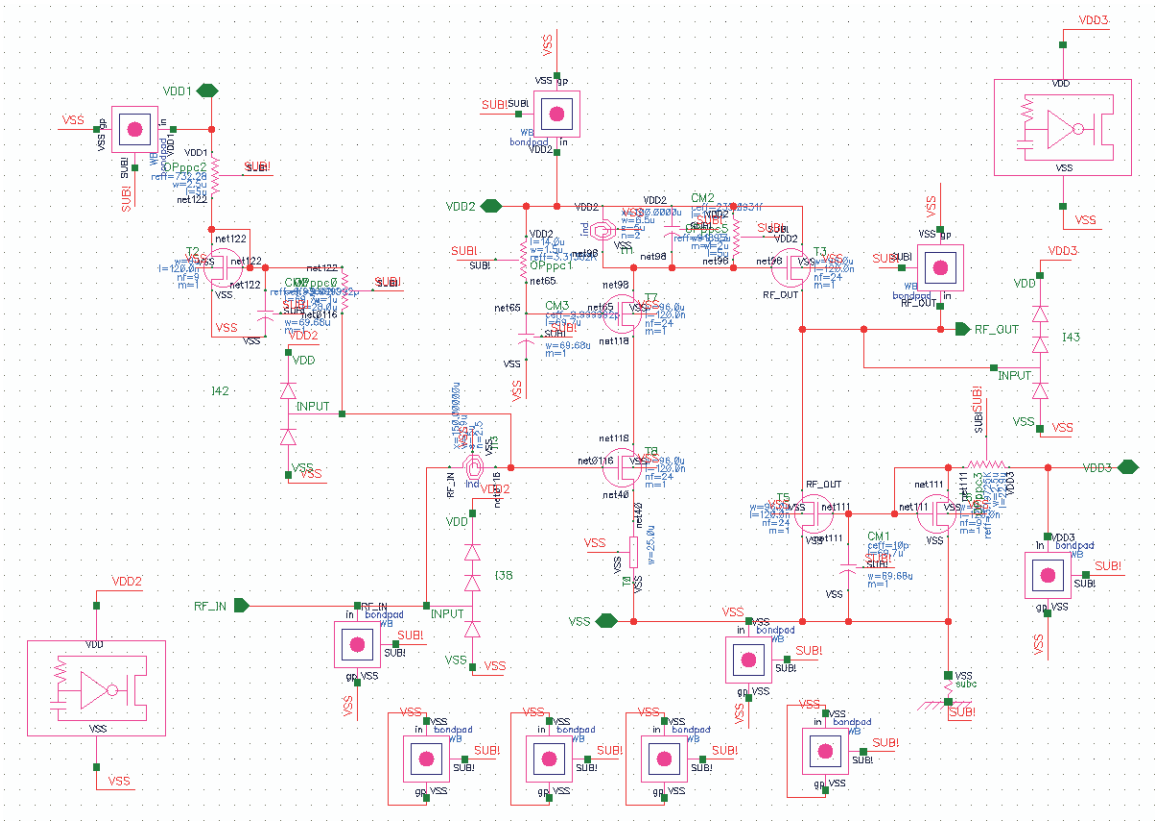


Figure 3.24- Schematic for LNA with ESD Protection

3.3 Layout and Implementation

In this section, the details of the implementation of the LNA layout are described. IBM CMOS8RF eight metal (seven Cu and one Al), single poly, tungsten contact, shallow trench isolation (STI), Co silicide 0.13 μm RF CMOS technology was used.

3.3.1 LNA without ESD Protection

First the layout for the LNA without ESD was designed. At the bottom side the 150 μm^2 RF input pads with ground/signal/ground (GSG) and at the opposite top side the RF output pads with GSG. Three power and one ground pad were used to provide DC bias to the circuit. One power pad was used for the LNA bias circuit, one for the LNA and buffer circuits, and the third power pad for the buffer bias circuit.

The inductors were the first components to be placed, due to their large sizes, followed by the 10 pF decoupling capacitors, and then the remaining components were placed around them and in a certain way to minimize parasitic inductance and resistance of the metal interconnect.

Certain areas were reserved for the ESD components, so that both LNA layouts would look basically the same and therefore have similar interconnect parasitics.

Multiple vias were used to connect different levels of metallization in order to reduce the resistance whenever was possible.

Although a lot of time could be spent in designing the LNA core transistors in order to minimize the gate resistance, this was not done, as both LNAs used the same transistors, and for comparison purposes this would not be necessary. Instead RF NFETs with multiple fingers were used and wider metallization lines were used to minimize

interconnect parasitics. Appendix A shows the LNA without ESD protection cadence layout and chip images, and Appendix D shows the whole chip image.

3.3.2 LNA with ESD Protection

The layout of the LNA with ESD protection is basically the same as the LNA without ESD protection, with the addition of the primary and secondary ESD protections, RC power clamp, and output ESD protection.

One problem that happened during the layout and required a significant amount of time trying to improve the S11 was the layout of tie downs. Tie downs are diodes connected in parallel with the NFET gate in order to protect them against plasma etch charging during the fabrication process. Depending on what is connected to the gate, the design rule checker (DRC) tool will request that additional tie downs are added in parallel with the gate. Most of the previous layouts that were used as examples used large tie downs matrix, e.g. 15 by 30, connected in parallel through a metal 1 (M1) plate. It is suspected, but not confirmed, that this is related with the frequency, as most of the previous examples were in the range of 5 GHz. Independent of the initial LNA input matching, after the tie downs were added, S11 was marginally around 10 dB. This problem was solved after discussing this issue with a PhD student, who suggested using 2x2 tie down blocks and connecting them with M1 lines. Once this was done, the number of tie downs reduced significantly, particularly for the LNA input NFET as shown in Figure 3.25 and Figure 3.26, and S11 improved at least 7 dB.

Appendix B shows the LNA with ESD protection cadence layout and chip images, and Appendix D shows the whole chip image.

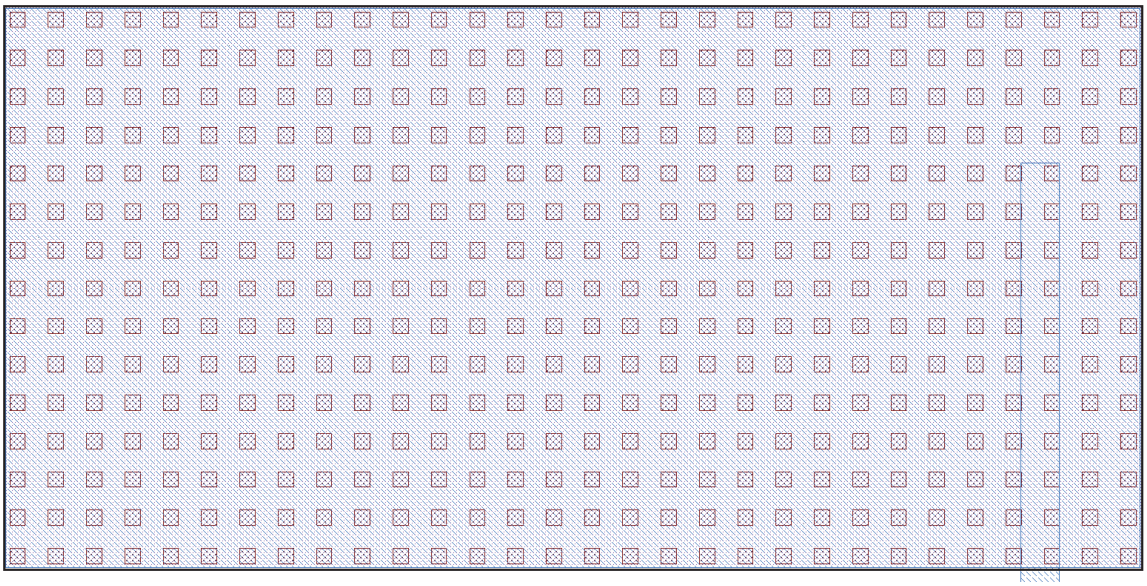


Figure 3.25 – LNA Input NFET Original Tie Down's Layout with Low S11

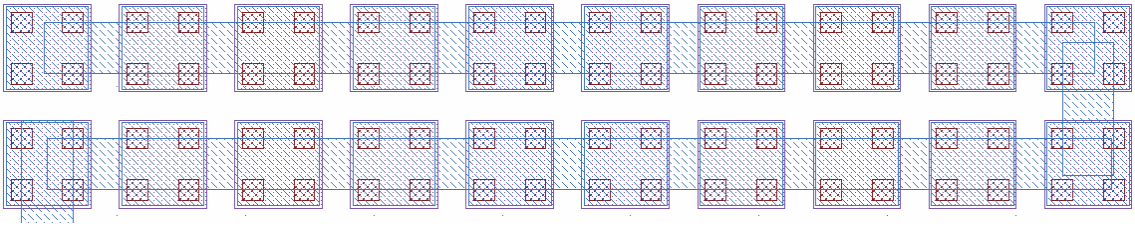


Figure 3.26 – LNA Input NFET Final Tie Down's Layout with High S11

3.3.3 De-Embedding Structures

De-embedding structures are used to subtract the influence of the parasitic inductance, capacitance, and resistance of bond pads and metal interconnect between the probe and circuit of interest; in order to measure the circuit parameters accurately.

De-embedding, open and short structures were added to the chip in case more accurate S-parameter measurements of the LNA circuits were necessary. However, as both circuits used the same bond pads, and the layout of the metal interconnect was

basically the same, therefore for the purpose of comparison between the two LNAs the de-embedding structures were not used.

The de-embedding structures were placed in the region between the two LNAs. Appendix C shows the de-embedding structures chip image and Appendix D shows the image of the whole chip.

3.3.4 Circuit Extraction

In order to perform the post layout simulation, it is necessary to first extract the circuit with the parasitics from the layout. There are four extraction options: R, RC, RLC, and RLCK. Theoretically, in order to account for all the parasitics, RLC extraction would be required. Although I was advised that the parasitic inductance of the QRC extraction tool would yield higher inductance than the circuit has in reality, due to time constraints, this was not taken into consideration.

Several iterations between layout, circuit extraction, and post-layout simulation were necessary in order to properly size the gate inductor, source degeneration inductor, tank inductor, tank capacitor to account for the interconnect parasitics. A parallel resistor needed to be added to the tank circuit in order to reduce the LNA gain and make it unconditional stable.

3.4 Post Layout Simulation Results

In this section the results of the post layout simulations of the LNA without ESD protection and LNA with ESD protection are compared. The test bench shown in Figure 3.27 was used to perform the S-parameters simulations.

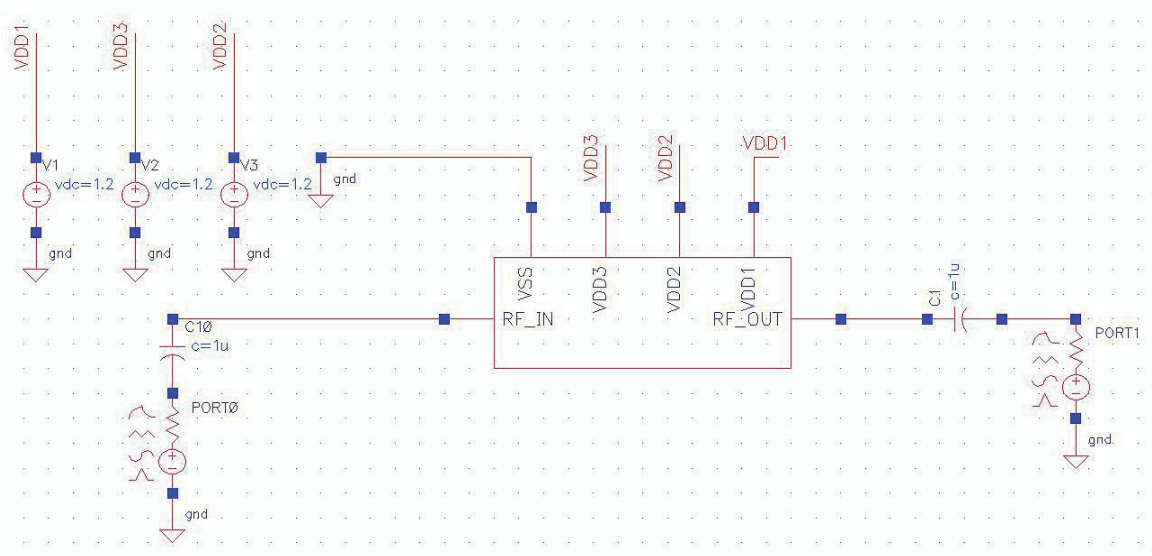


Figure 3.27 - LNA Simulation Test Bench

The circuits with parasitics of both LNAs were extracted and simulated. The gate inductor (L_g), the degeneration inductor (L_s), and the tank capacitor (C_{tank}) components were adjusted in order to have the S-parameters of the extracted circuit optimized at the center frequency.

During the comparison of measured and simulated results, it was noticed that the wrong extracted data set was used to tune both LNAs before tape-out; i.e. the RC instead of RLC extracted circuit was used to optimize the parameters at the center frequency. This will show as a downward frequency shift on the LNA parameters. Sections 3.4.1 and 3.4.2 show the comparison of RC vs. RLC extracted simulations for both LNAs.

3.4.1 LNA without ESD Protection RC vs. RLC Extracted

Figure 3.29 to Figure 3.33 show the RC vs. RLC extracted simulation results for the LNA without ESD protection. As mentioned before, a downward frequency shift of the curves can be observed.

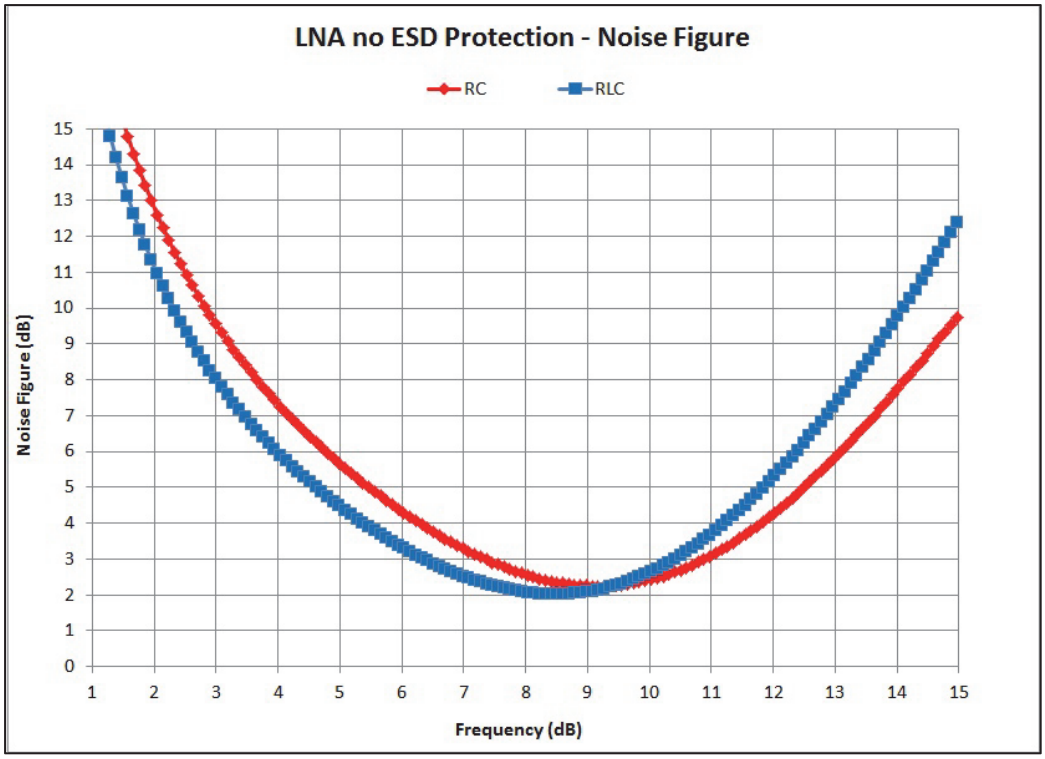


Figure 3.28 – LNA without ESD Protection RC vs RLC Simulation – Noise Figure

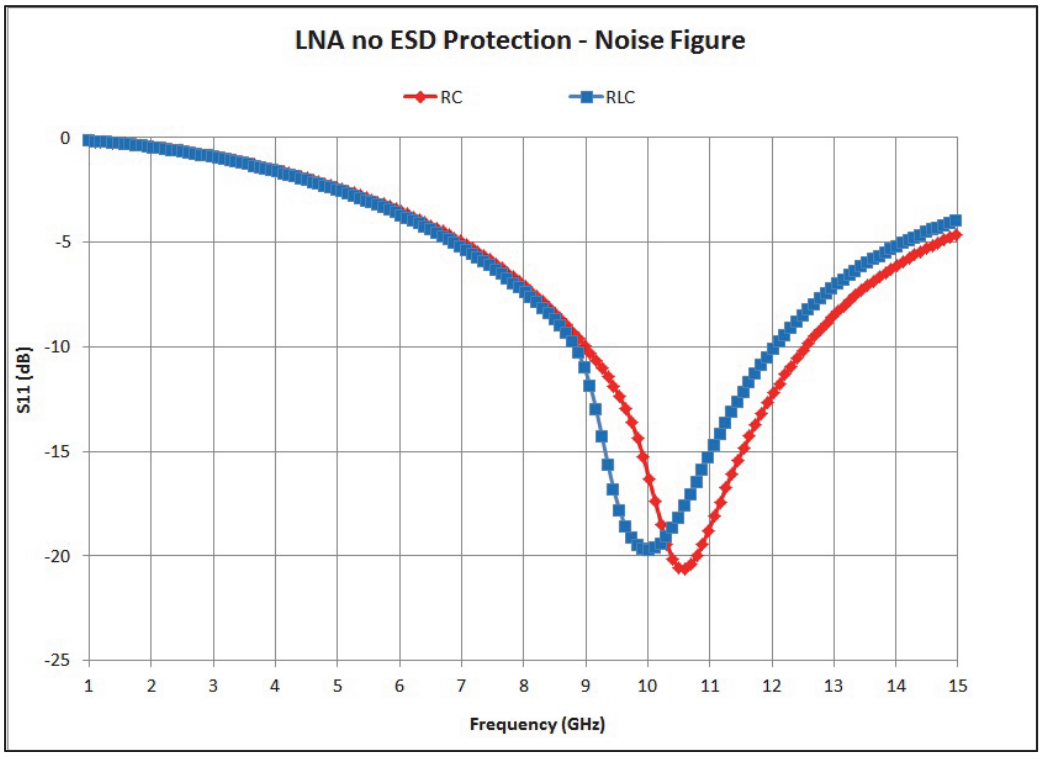


Figure 3.29 – LNA without ESD Protection RC vs RLC Simulation – S11

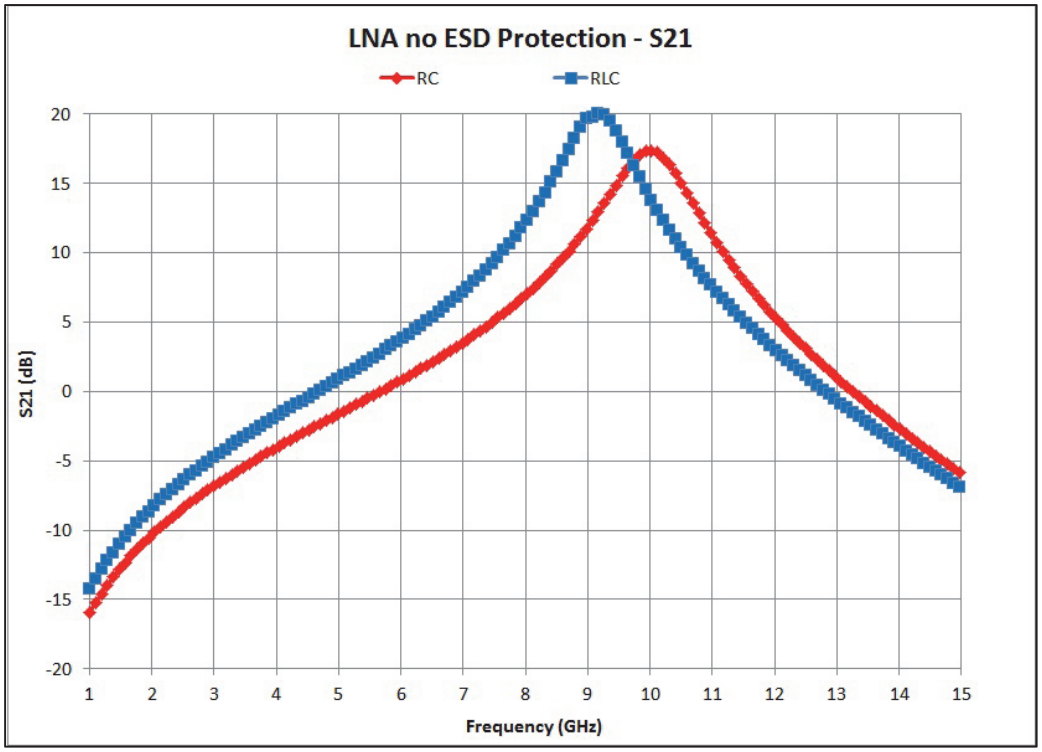


Figure 3.30 – LNA without ESD Protection RC vs RLC Simulation – S21

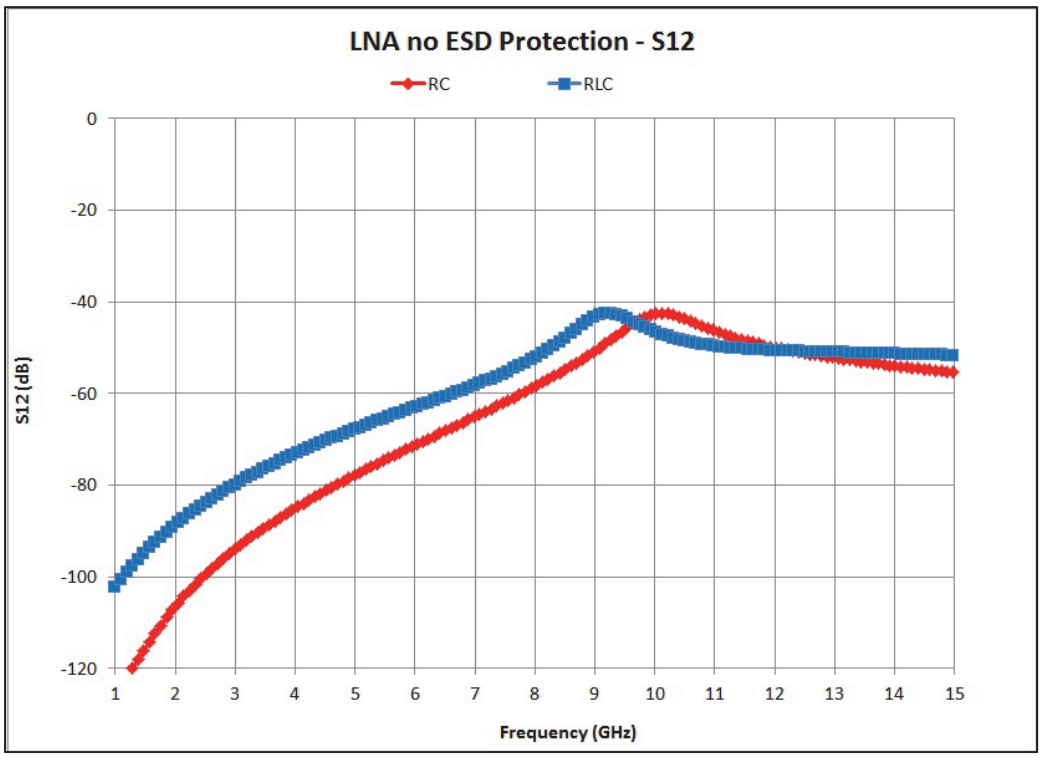


Figure 3.31 – LNA without ESD Protection RC vs RLC Simulation – S12

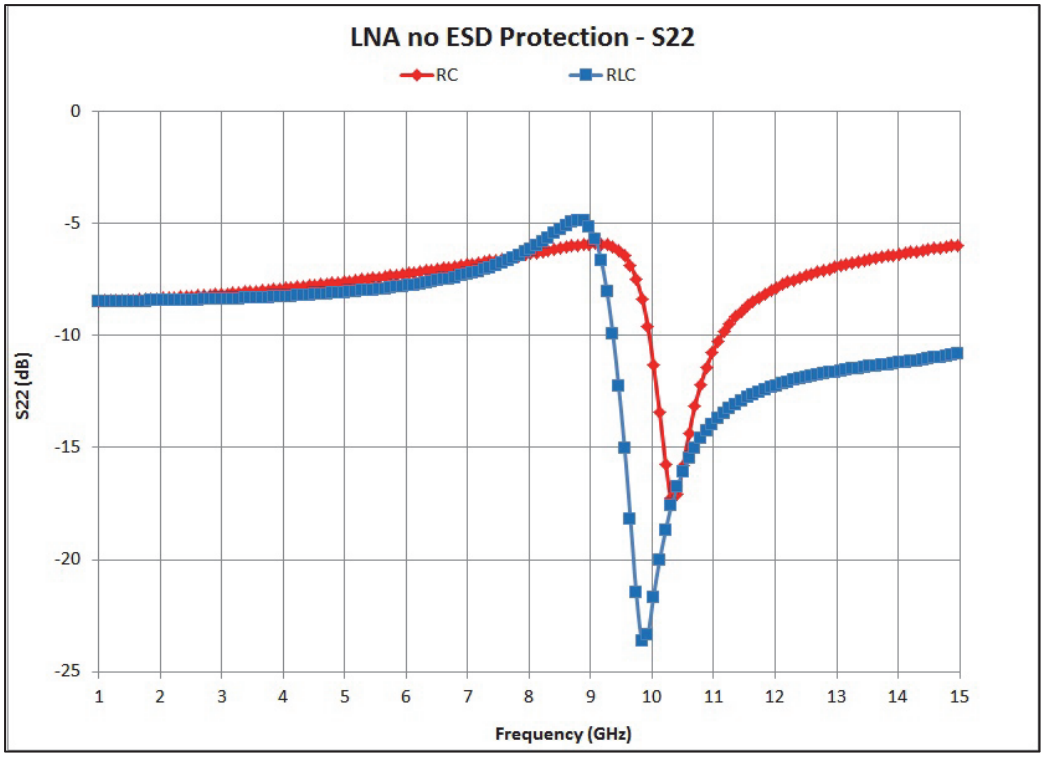


Figure 3.32 – LNA without ESD Protection RC vs RLC Simulation – S22

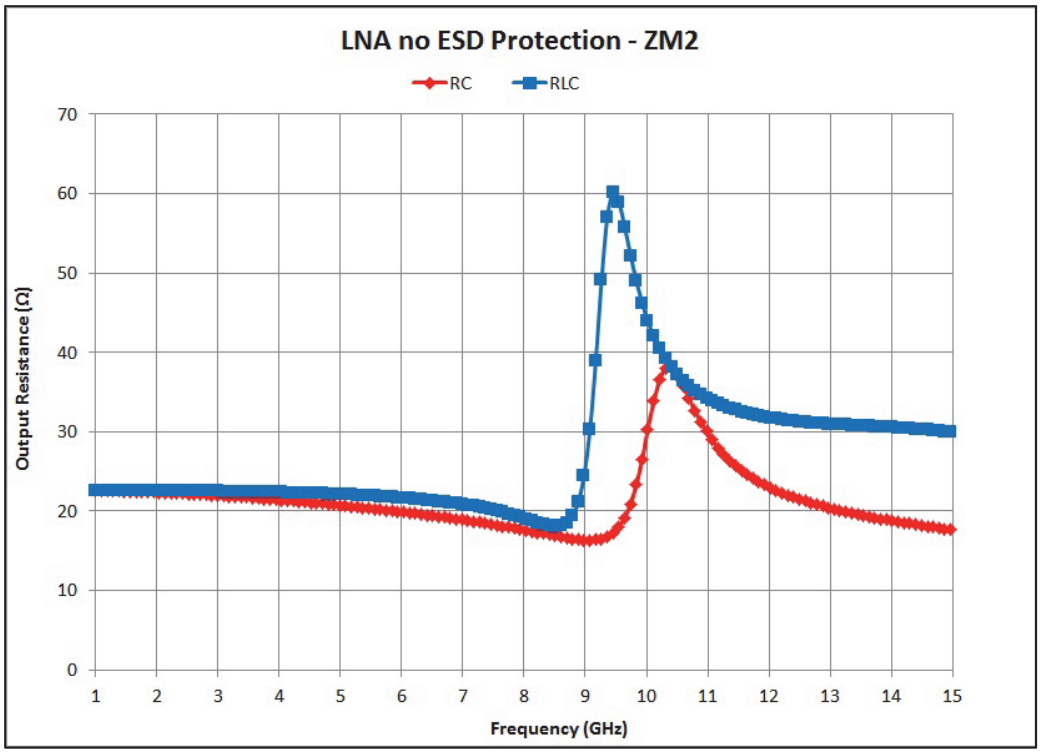


Figure 3.33 – LNA without ESD Protection RC vs RLC Simulation – Zout

3.4.2 LNA with ESD Protection RC vs. RLC Extracted Post Layout Simulation

Figure 3.34 to Figure 3.39 show the RC vs. RLC extracted simulation results for the LNA with ESD protection. As mentioned before, a downward frequency shift of the curves can be observed.

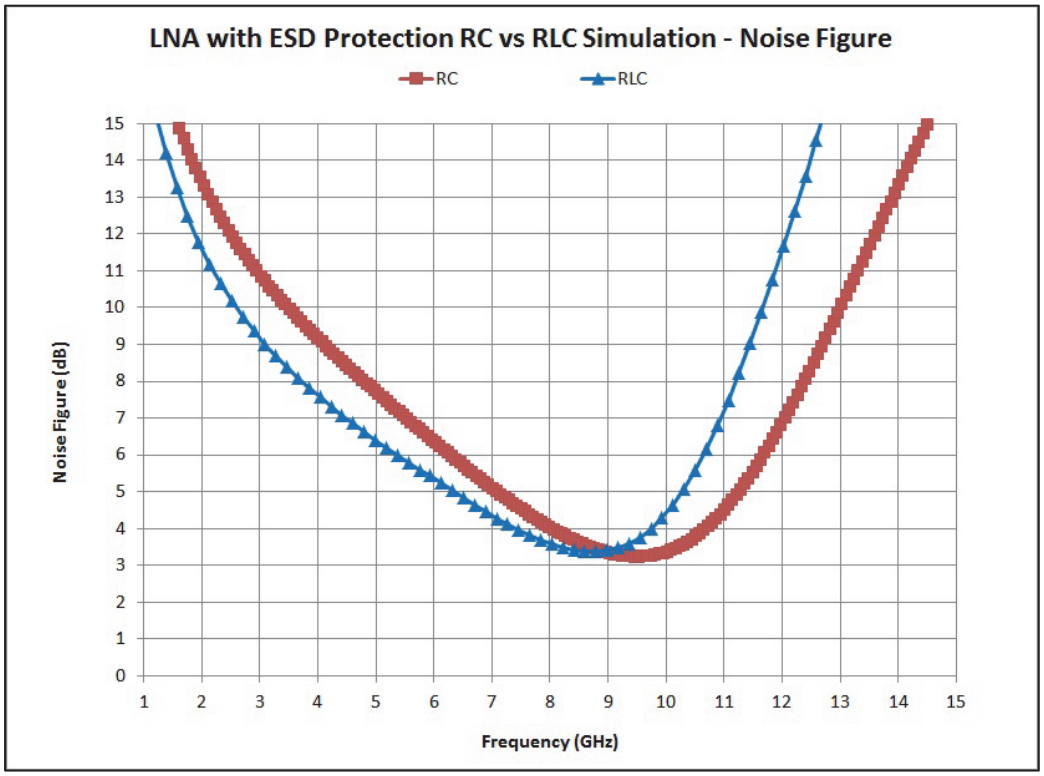


Figure 3.34 – LNA with ESD Protection RC vs RLC Simulation – Noise Figure

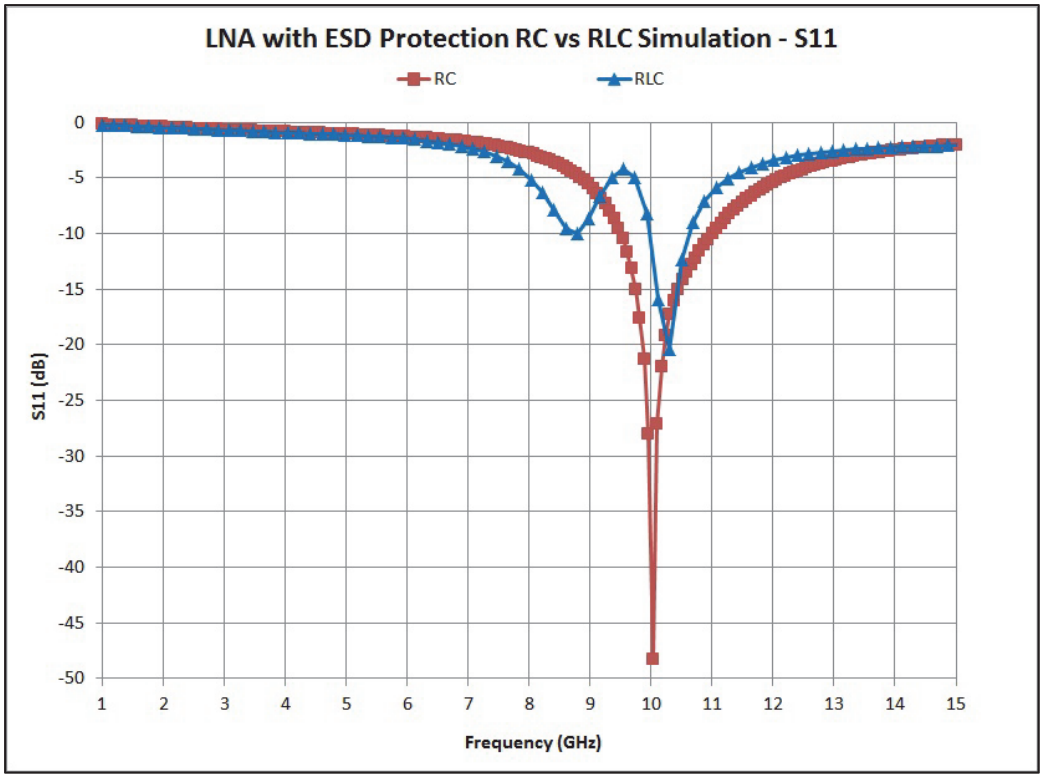


Figure 3.35 – LNA with ESD Protection RC vs RLC Simulation – S11

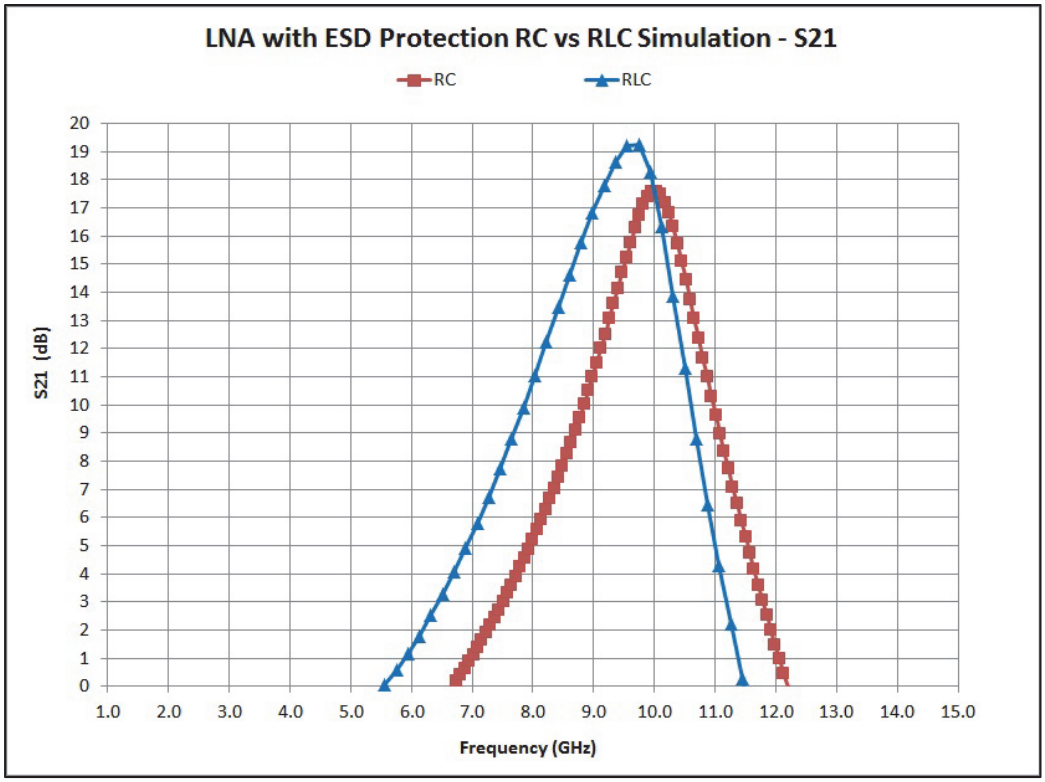


Figure 3.36 – LNA with ESD Protection RC vs RLC Simulation – S21

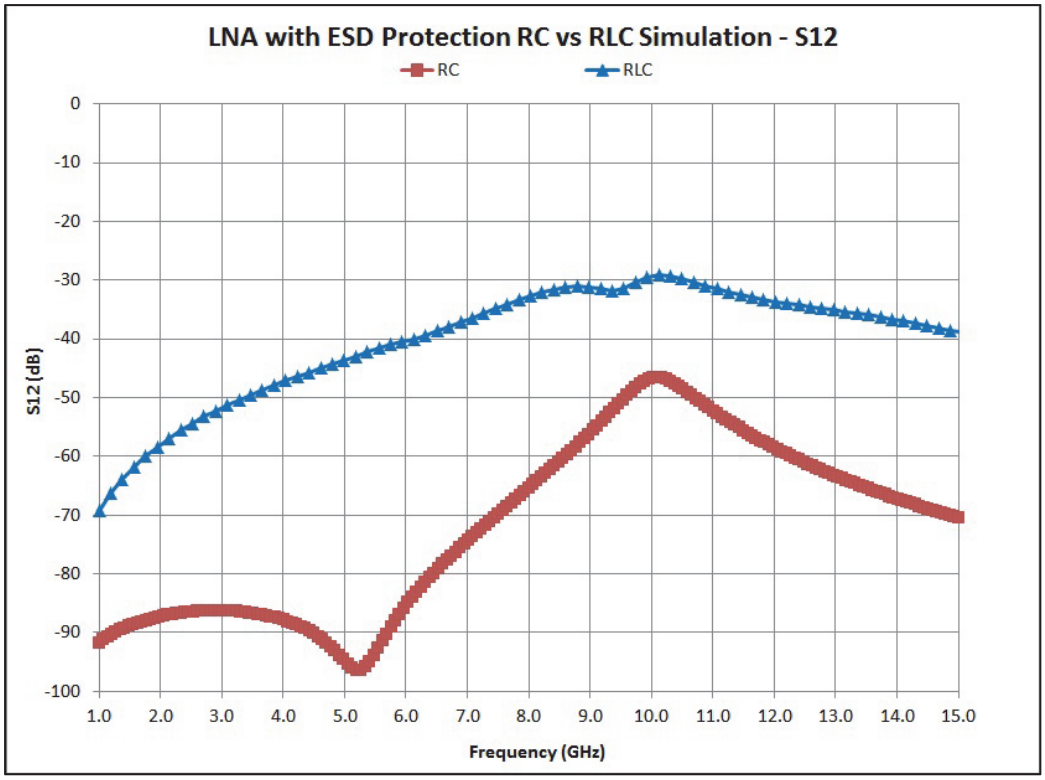


Figure 3.37 – LNA with ESD Protection RC vs RLC Simulation – S12

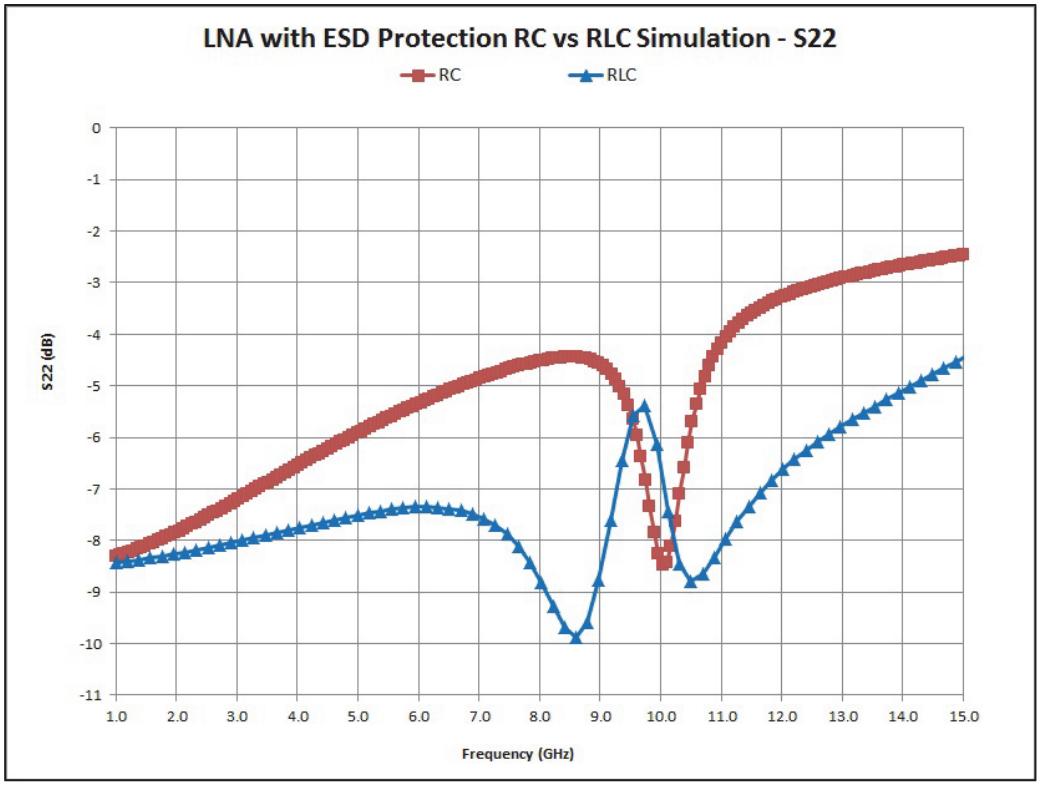


Figure 3.38 – LNA with ESD Protection RC vs RLC Simulation – S22

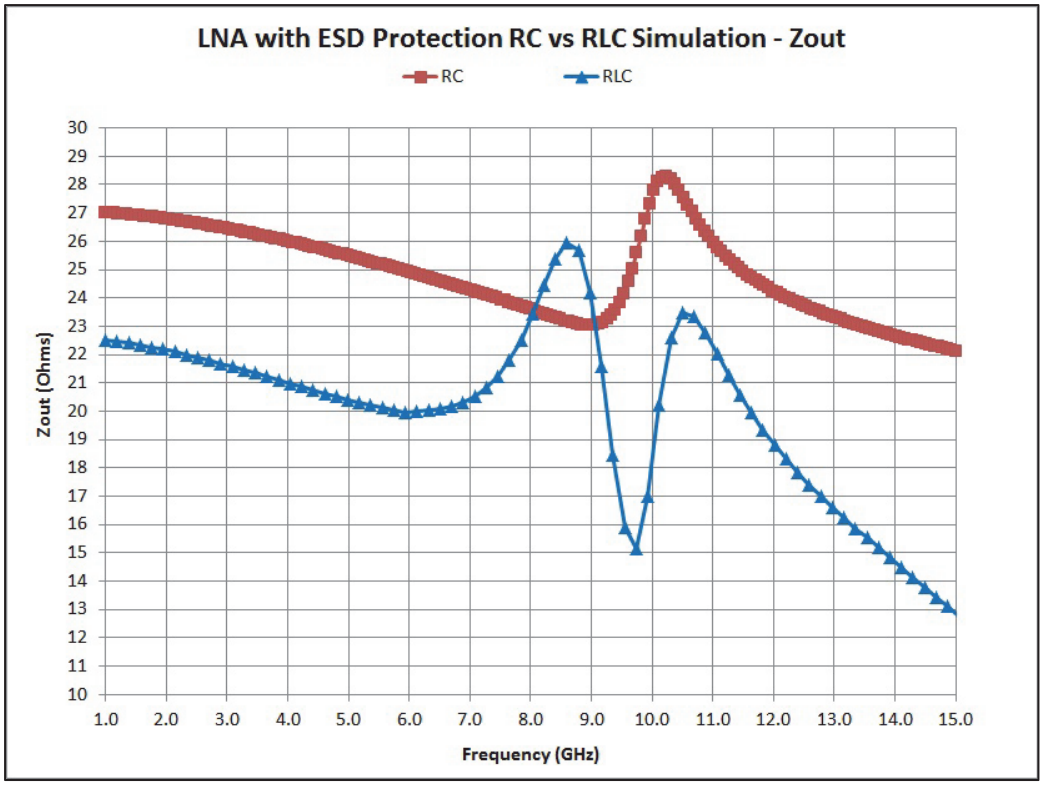


Figure 3.39 – LNA with ESD Protection RC vs RLC Simulation – Zout

3.4.3 LNA without ESD Protection vs. LNA with ESD Protection

Figure 3.40 to Figure 3.45 show the RC extracted simulation results comparison of the LNAs with and without ESD protection.

Table 3.5 shows the noise figure, S11, S21, S12, S22, and Z_{out} post layout simulation results for both LNAs, measured at center frequency (10 GHz).

Table 3.5 – Post Layout Simulation Comparison of LNA with ESD vs. LNA without ESD Protection

Parameter	LNA without ESD Protection	LNA with ESD Protection
Noise figure	2.4 dB	3.4 dB
S11	-16.2 dB	-48.2 dB
S21	17.4 dB	17.6 dB
S12	-46.7 dB	-42.5 dB
S22	-11.4 dB	-8.5 dB

From Table 3.5 and Figure 3.40 to Figure 3.45, the following can be observed:

- Noise figure: the ESD protection contributes with an increase of 1 dB, this is mainly due to the extra parasitic capacitance and resistance introduced by the ESD protection.
- S11: the LNA with ESD protection has a lower S11 than the LNA without ESD protection; since both are adequate, this is of little importance; however, as expected, S11 of the LNA with ESD protection has a smaller bandwidth due to the capacitance introduced by the ESD protection.
- S21: the gain for both LNAs is practically the same; this is because the CLC PI-network formed by the capacitance of the primary ESD protection, L_g, and the capacitance of the secondary ESD protection is a lossless CLC matching network.
- S12: this parameter is in the same order of magnitude for both LNAs.
- S22: the LNA with ESD has a 3 dB higher S22 and a smaller valley than the LNA without ESD protection. This was caused by additional the ESD protection capacitance at the output.

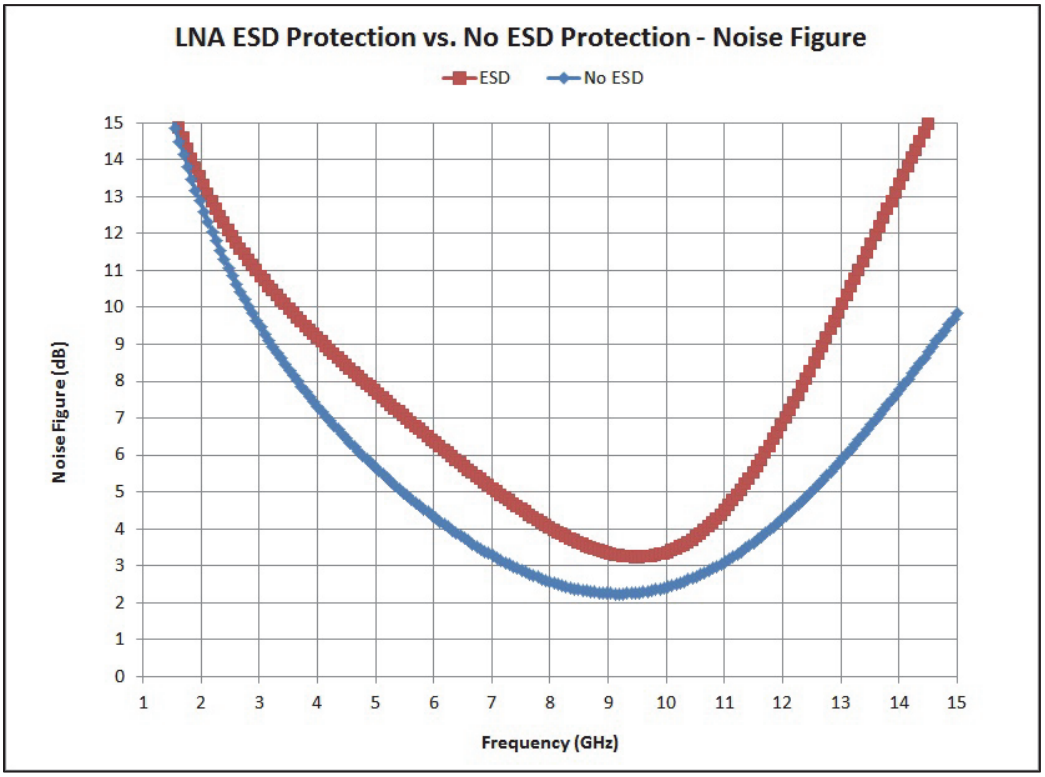


Figure 3.40 – LNA with ESD Protection vs. LNA without ESD Protection – Noise Figure

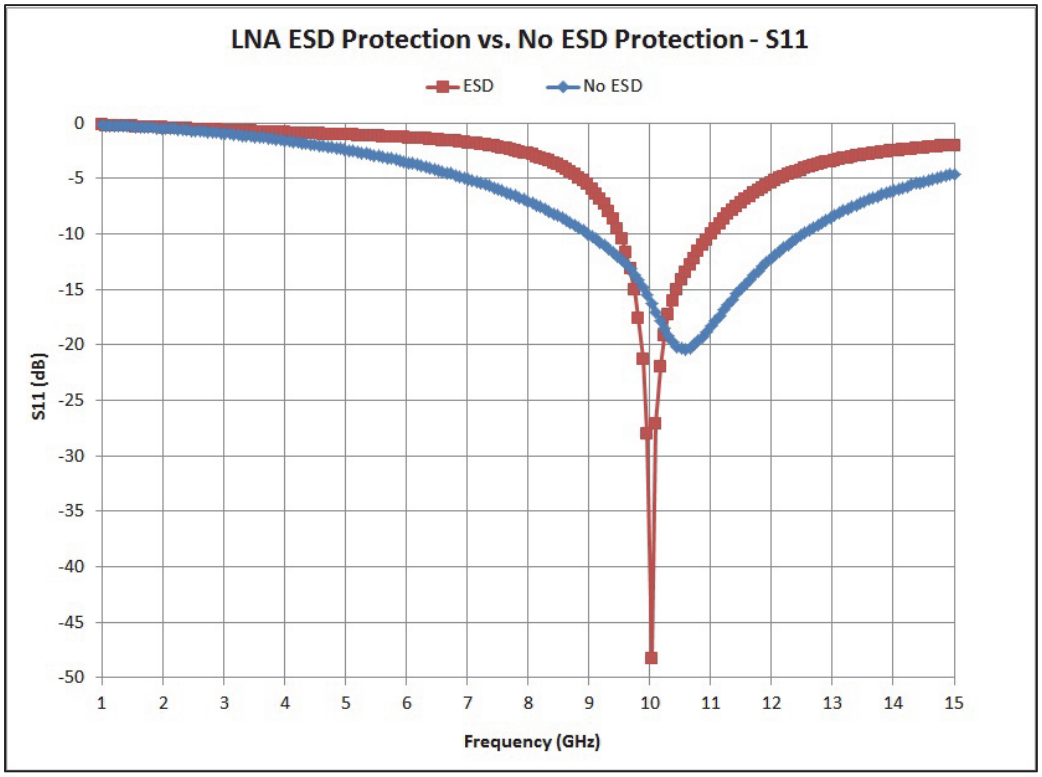


Figure 3.41 – LNA with ESD Protection vs. LNA without ESD Protection –S11

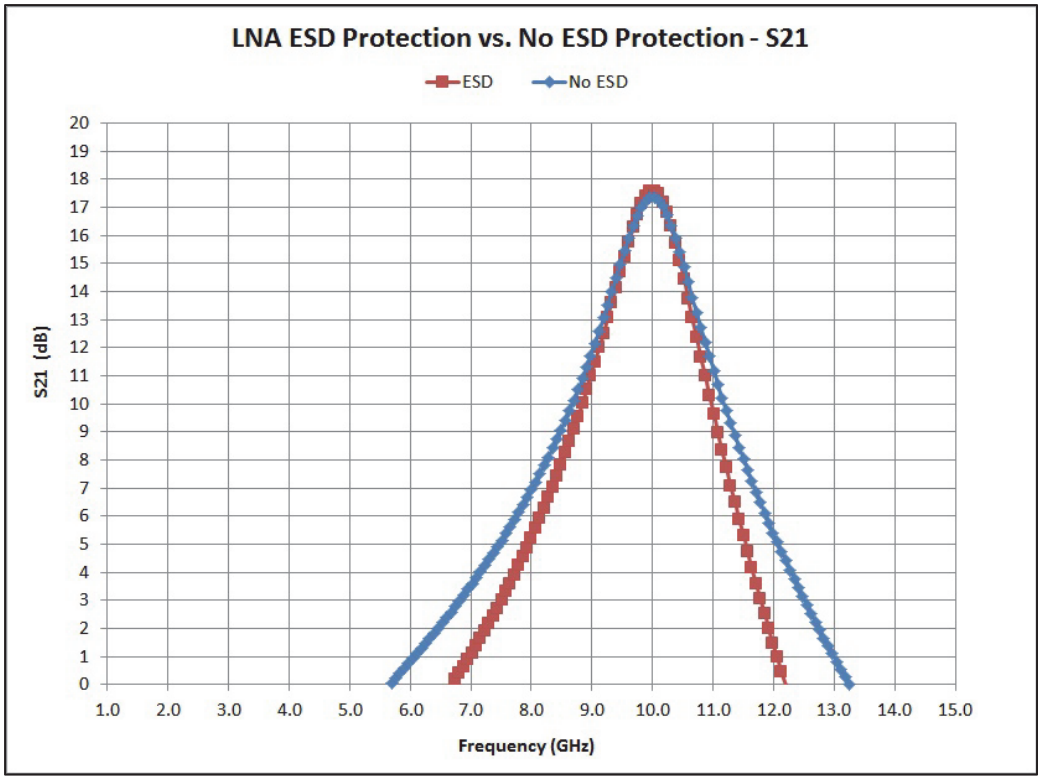


Figure 3.42 – LNA with ESD Protection vs. LNA without ESD Protection – S21

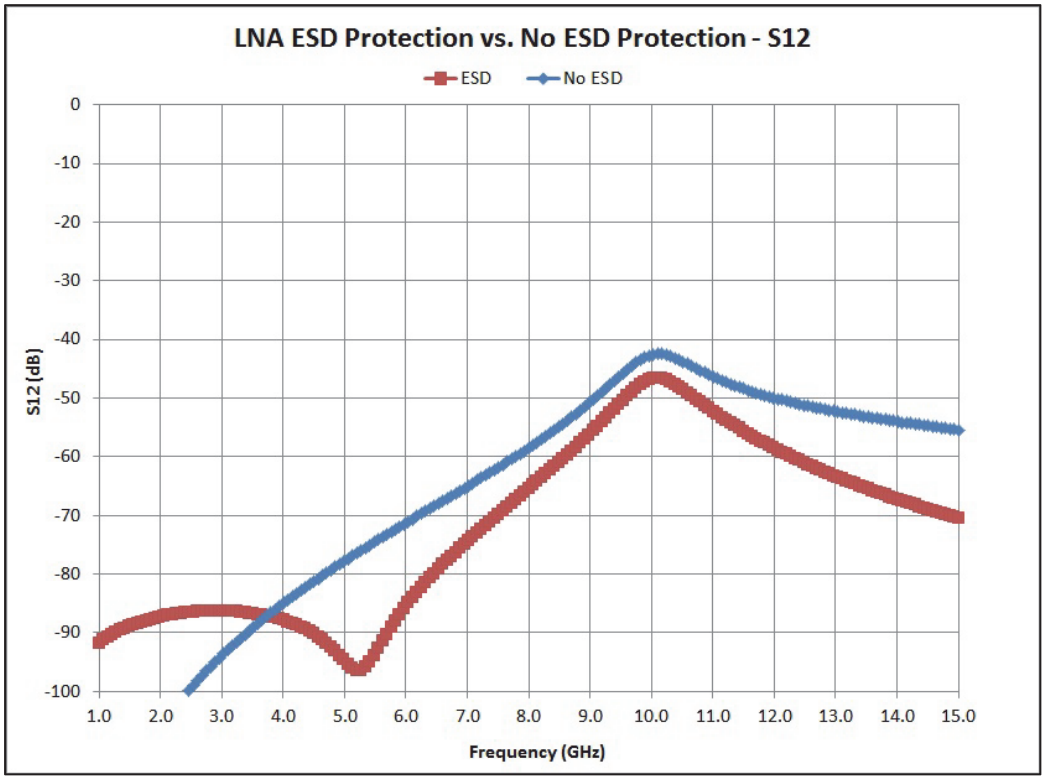


Figure 3.43 – LNA with ESD Protection vs. LNA without ESD Protection – S12

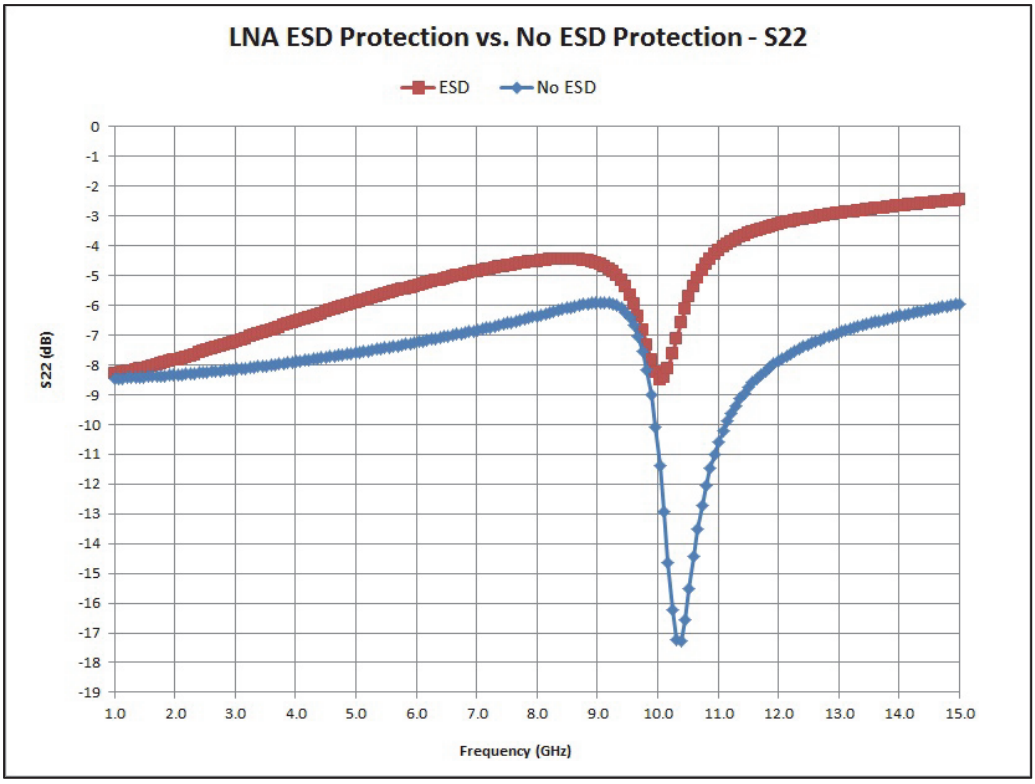


Figure 3.44 – LNA with ESD Protection vs. LNA without ESD Protection – S22

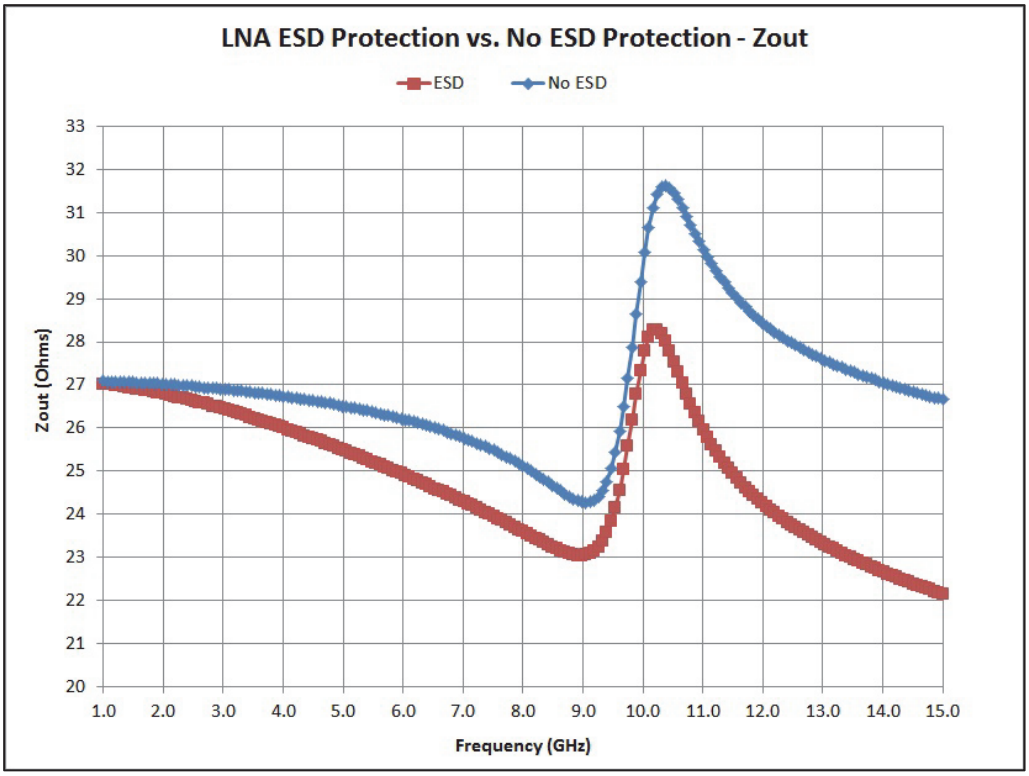


Figure 3.45 – LNA with ESD Protection vs. LNA without ESD Protection – Zout

3.5 Summary

As can be seen from the simulation results, the ESD protection has introduced degradation to some LNA parameters. However, the degradation has been minimized by having a PI matching network comprising the primary ESD protection capacitance, the gate inductor (L_g), and the secondary ESD protection capacitance. The main degradations observed were a 1 dB higher noise figure and a smaller S11 bandwidth.

4 Chapter: **Measurement Results**

In this chapter the LNA RF measurement results are compared with the LNA simulated results presented in Chapter 3. The measured S-parameters and noise figure pre and post ESD HBM testing are also compared and discussed.

4.1 Measured and Simulated Results Comparison

The LNA S-parameters and noise figure were measured in a Faraday cage in order to avoid any external interference on the measurements.

The measurements of the S-parameters were performed at chip level using an Agilent 8722ES S-Parameter Analyzer Network (50 MHz – 40GHz), 150 μm pitch SGS RF probes, 150 μm pitch 4-needle DC probe, GGB CS-5 calibration substrate, DC power supplies and multimeters. Each time, before S-parameters' measurements were carried out, the network analyzer was calibrated at the tip of the RF probes. The OSLT (open, short, load, through) calibration method was employed [31], [32], [33].

The noise figure measurements were performed at chip level using Agilent Noise Figure Analyzer (NFA) N8975A (10 MHz – 26.5GHz) and Agilent N4002A Noise Source (10 MHz – 26.5GHz). Prior to measurements, the NFA was calibrated at the tip of the RF probes [34].

In order to provide a better accuracy in the measurements, the parameters were measured in the frequency range of 8 GHz – 12GHz.

4.1.1 LNA with ESD Measured vs. Simulated DC Biasing

The extracted simulated circuit and the chip DC biasing are compared to show the transistors are operating in the saturation region ($V_{GS}>V_{TH}$ and $V_{DS}> V_{GS}-V_{TH}$). Figure 4.1 is the LNA with ESD Protection schematic identifying the transistors for which the DC biasing was measured.

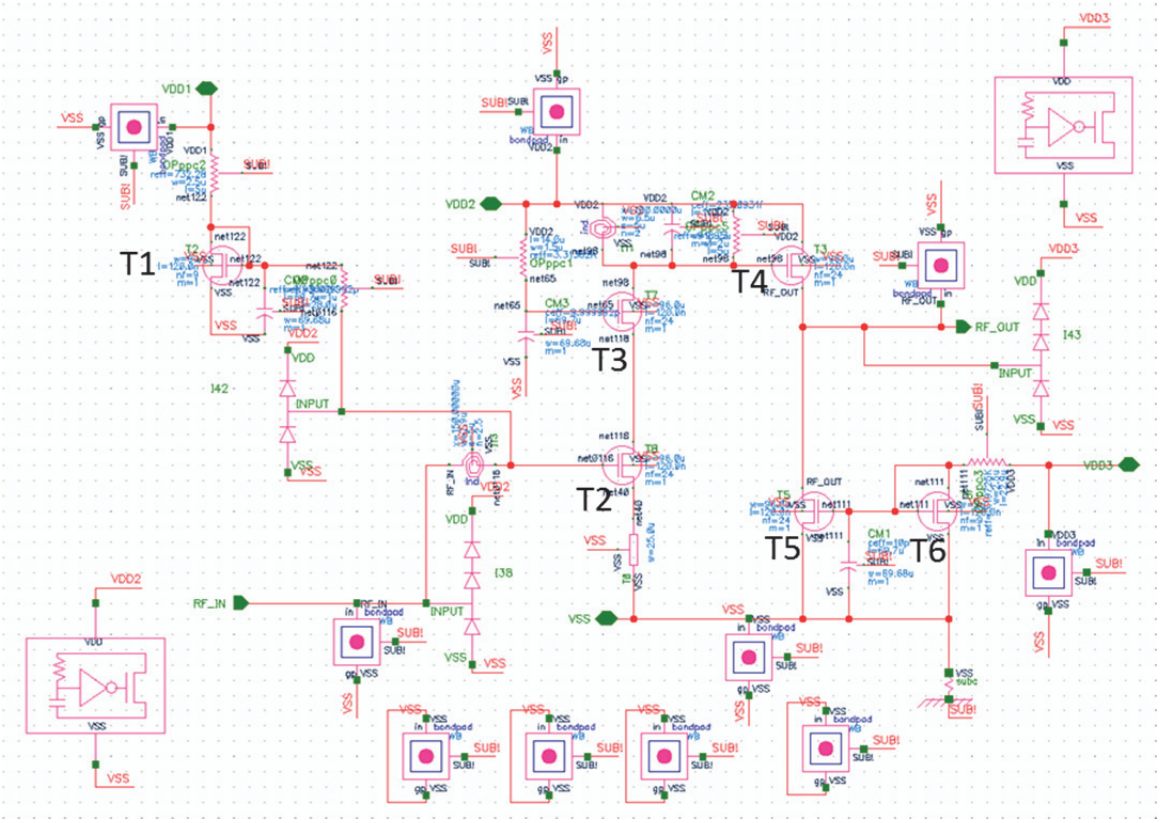


Figure 4.1 – LNA with ESD Protection Schematic Indicating Transistors for DC Biasing Measurements

Where T1 is the LNA current mirror transistor, T2 and T3 are the cascode LNA transistors, T4 and T5 are the buffer transistors, and T6 is the buffer current mirror transistor.

The V_{GS} of T2 was measure by DC biasing the LNA and measuring the voltage at RF_{in}, V_{GS}=629 mV. The current flowing through T2 and T3 was measured to be 8.4 mA.

The LNA current mirror I_{DS} was measured and is 682 µA. The V_{GS}=V_{DS}, and is given by (4.1):

$$V_{DS\,LNA\,CM} = V_{DD} - I_{DS} * R = 1.2 - 682 * 10^{-6} * 732 = 0.700\,V \quad (4.1)$$

The buffer current mirror I_{DS} was measured and is 218 µA. The V_{GS}=V_{DS}, and is given by (4.2):

$$V_{DS\,Buffer\,CM} = V_{DD} - I_{DS} * R = 1.2 - 218 * 10^{-6} * 3.3 * 10^{3} = 0.721\,V \quad (4.2)$$

The voltage at the drain of T3 and gate of T4 is given by (4.3):

$$V_{D\,T3} = V_{G\,T4} = V_{DD} - I_{DS} * R_{s\,ind} \quad (4.3)$$

Where the inductor series resistor is given by (4.4):

$$R_{s\,ind} = \frac{\omega L}{Q} = \frac{2\pi f L}{Q} = \frac{2\pi * (10 * 10^{9}) * (493 * 10^{-12})}{17.9} = 1.73\,Ohms \quad 4.4$$

Substituting the values in (4.3) gives:

$$V_{G\,T4} = 1.2 - 8.4 * 10^{-3} * 1.73 = 1.18\,V \quad (4.5)$$

V_{GS} of T4 is gate voltage minus the source voltage (measured at RF_OUT), which is 569 mV.

The DC biasing results obtained from simulation and measurements are summarized in Table 4.1.

Table 4.1 – LNA with ESD Protection Simulated and Measured DC Biasing

	T1		T2		T3		T4		T5		T6	
	ext	chip	ext	chip	ext	chip	ext	chip	ext	chip	ext	chip
V_{TH} (mV)	420		422		513		530		418		422	
V_{GS} (mV)	634	700	632	629	713		614	569	506	481	506	481
V_{DS} (mV)	634	700	484		702		623	616	575	584	506	481
I_{DS} (mA)	0.772	0.682	8.26	8.4	8.26	8.4	2.75	2.4	2.75	2.4	0.216	0.211

4.1.2 LNA with ESD Measured vs. Simulated Results

Figure 4.2 to Figure 4.6 show a comparison of the post tape-out RLC extracted simulation results with the measured results of the LNA with ESD protection. As mentioned in Section 3.4, RC extraction results were used to size L_g, L_s, and C_{tank}, and to optimize the LNA operation; therefore, the RLC extract and measured results don't show a good correlation.

- The noise figure shows a degradation of about 3 dB. As the input mismatch of the chip is higher than that of the simulated circuit, an increase in noise figure is observed, as can be explained based on the general noise figure equation (4.6) [26].

$$F = F_{min} + \frac{R_n}{G_s}\left[\left(G_s - G_{opt}\right)^2 + \left(B_s - B_{opt}\right)^2\right] \tag{4.6}$$

  As optimum conductance G_{opt} and susceptance B_{opt} at the input differ from the source conductance G_s and susceptance B_s, the noise figure increases.

- S11 curves have similar shapes. A slight upward frequency shift has been observed as the RLC extracted tool overestimated the parasitic inductance. The second resonance pole observed on both RLC extracted and measured curves at 10.3 GHz and 11.5 GHz, respectively, is caused by the resonance of the parasitic capacitance of the ESD protection with inductances at the input of the LNA.

- S21 of the measured and simulated results are quite different. The measured voltage gain degradation could be explained by the fact that there is no decoupling capacitor between power and ground for the return of the RF current. When the circuit is measured the inductance of the external connections to the power supply would cause a decrease in the gain.

Other reasons that could account for a degradation of the gain can be explained by using the simplified voltage gain expression given by [25]:

$$\left|\frac{v_{out}}{v_{in}}\right| = \frac{R_L \omega_T}{R_S \omega_0} \frac{50}{r_0+50} \tag{4.7}$$

Where, R_L is the tank parallel resistance, R_S is the source resistance, ω_T is the switching frequency and ω_0 the center frequency, and r_0 is the output buffer output impedance. The tank parallel resistance is determined by the equivalent parallel resistance of tank inductor parallel resistance (Rp_{ind}), with the tank resistance (R_{tank}) and tank capacitor parallel resistance (Rp_{cap}). The parallel resistance of the inductor and capacitor are given respectively by:

$$Rp_{ind} = Q * \omega_0 * L \tag{4.8}$$

$$Rp_{cap} = \frac{Q}{\omega_0 * C} \tag{4.9}$$

Based on (4.8) and (4.9), smaller Q of the real inductor and capacitor leads to smaller R_L and consequently to lower gain. The size of the inductors and capacitors used on the LNA design were not characterized by IBM in the Model Reference Guide [35]. EMC characterization of these components would be necessary to accurately predict their behavior at 10 GHz.

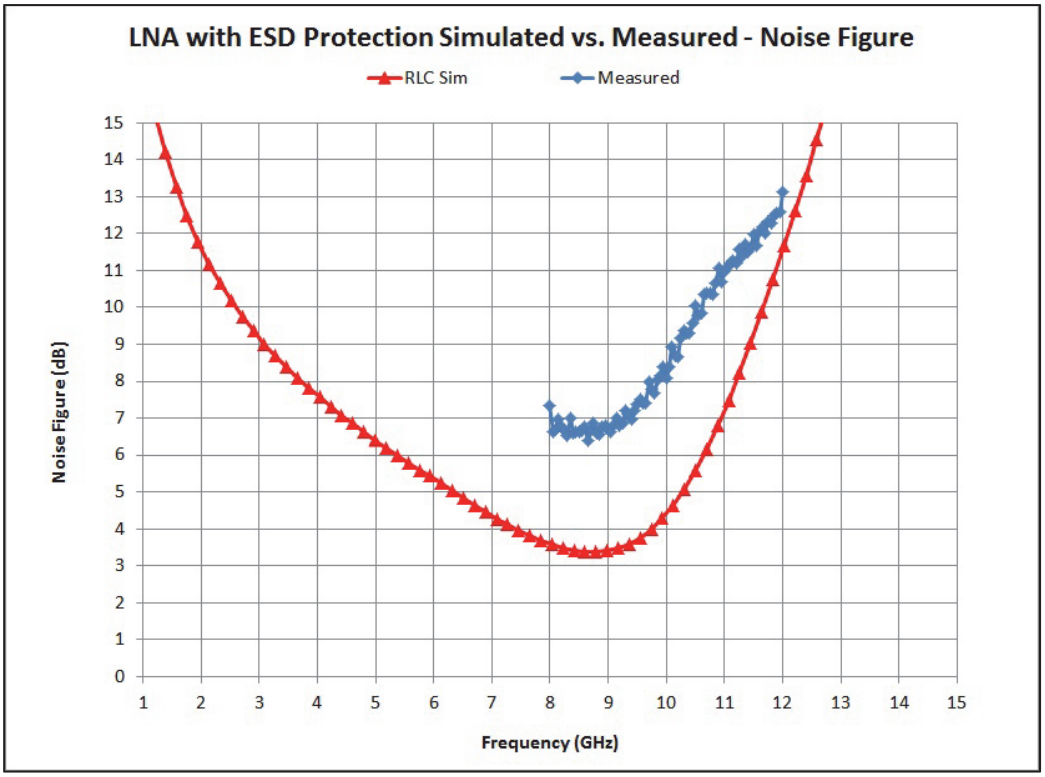


Figure 4.2 – LNA with ESD Protection Simulation vs. Measured – Noise Figure

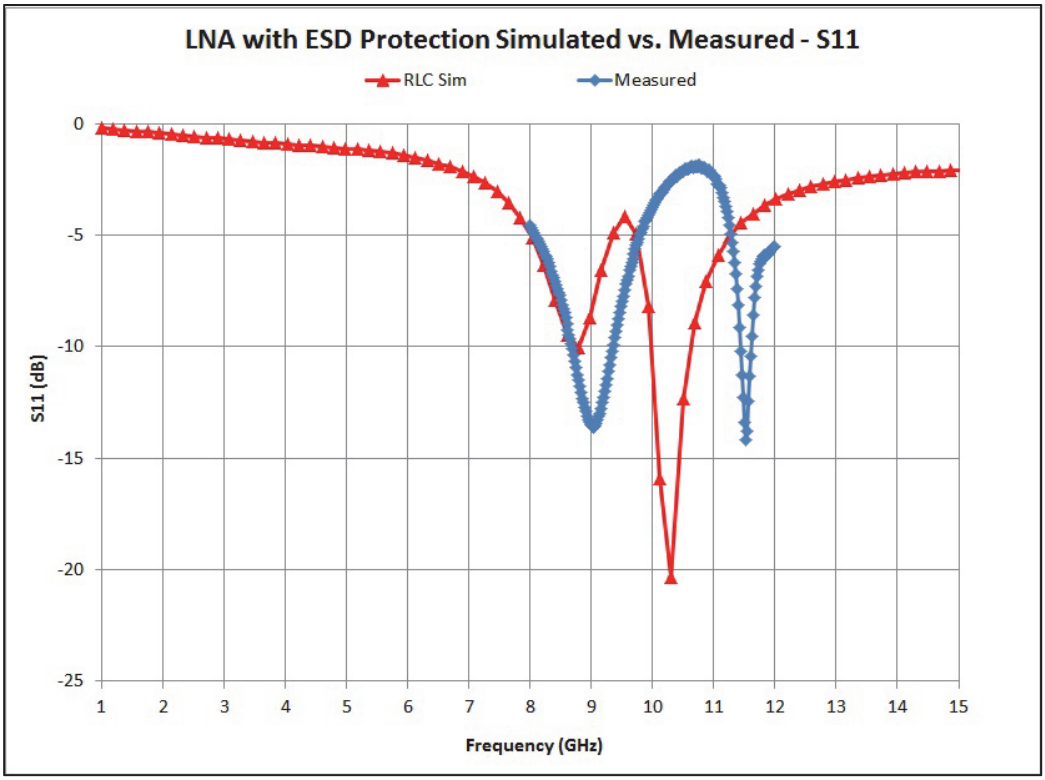


Figure 4.3 – LNA with ESD Protection Simulation vs. Measured – S11

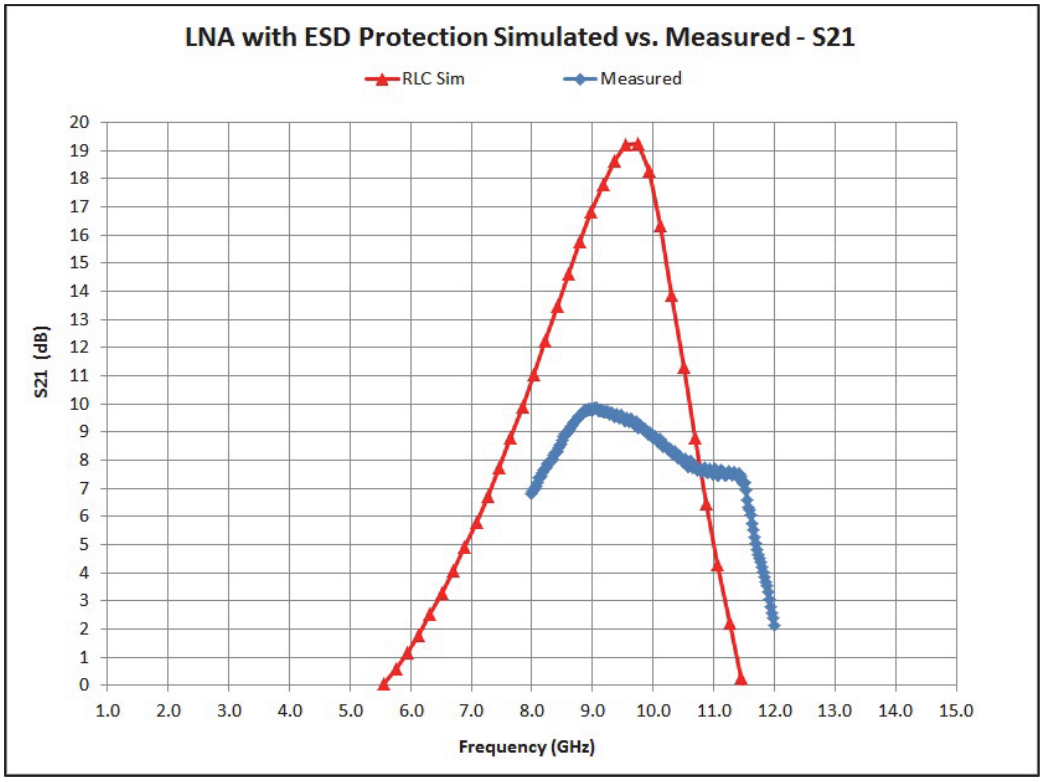


Figure 4.4 – LNA with ESD Protection Simulation vs. Measured – S21

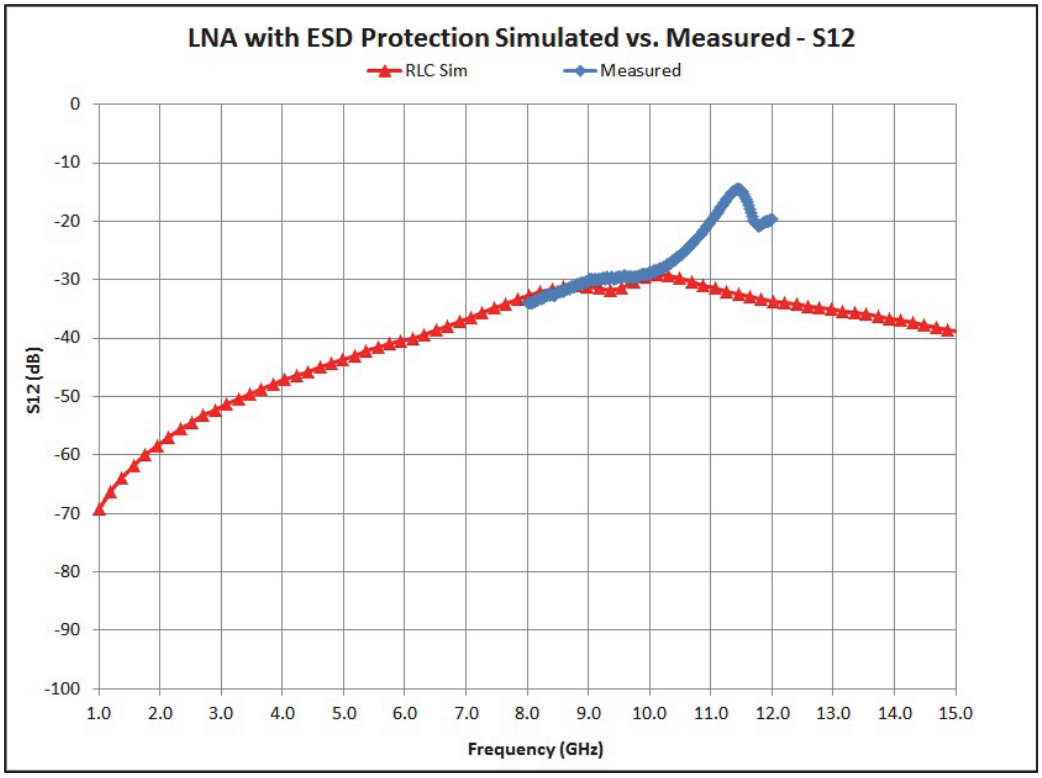


Figure 4.5 – LNA with ESD Protection Simulation vs. Measured – S12

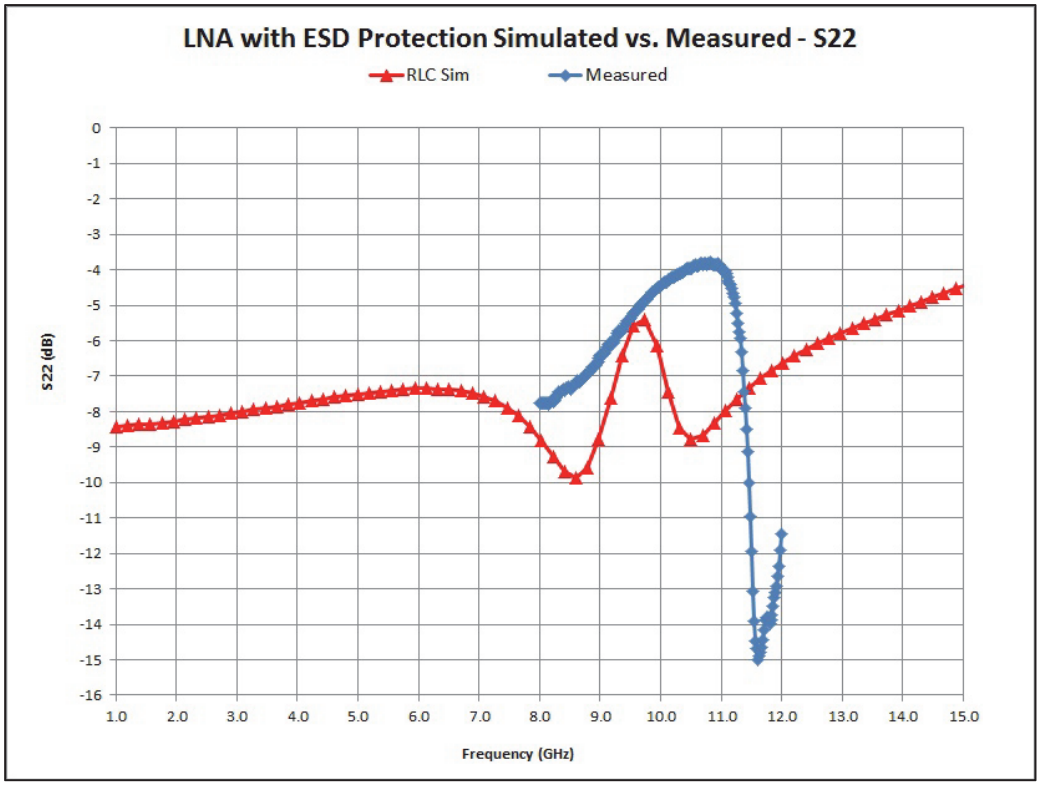


Figure 4.6 – LNA with ESD Protection Simulation vs. Measured – S22

4.1.3 LNA without ESD Measured vs. Simulated Results

Figure 4.7 to Figure 4.11 show a comparison of the post tape-out RLC extracted simulation with the measured results of the LNA without ESD protection. As mentioned in Section 3.4, RC extraction results were used to size L_g, L_s, and C_{tank}, and to optimize the LNA operation; therefore the RLC extract and measured results don't show a good correlation.

The same comments for the LNA with ESD protection is valid here, and therefore are not repeated.

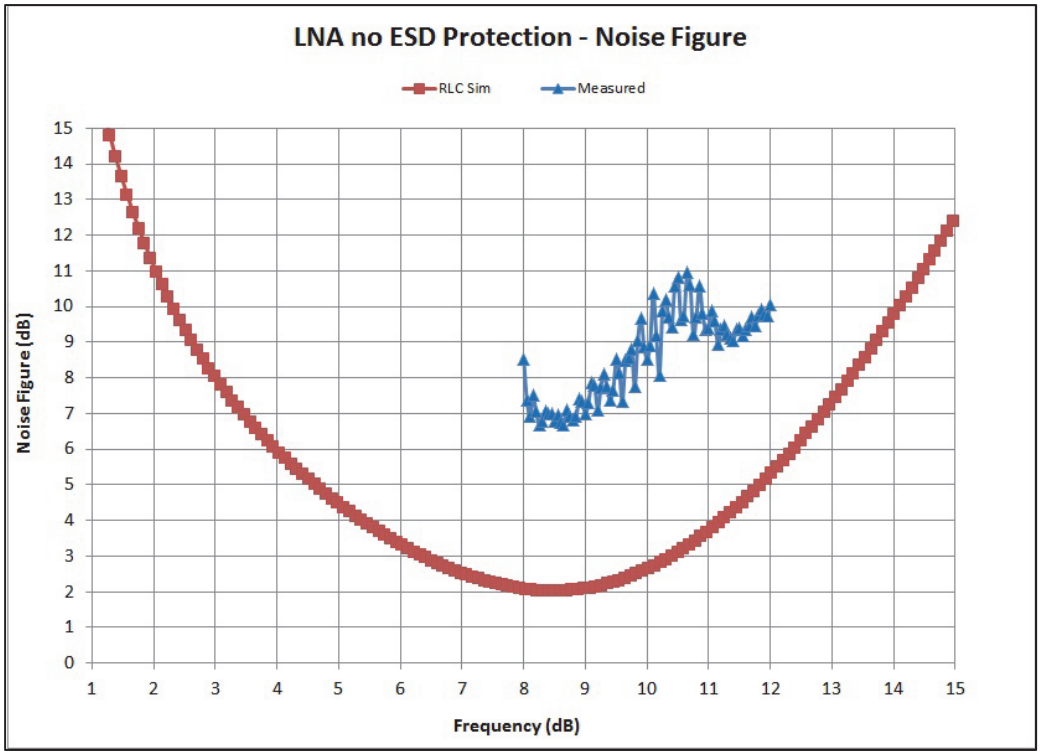


Figure 4.7 – LNA without ESD Protection Simulation vs. Measured – Noise Figure

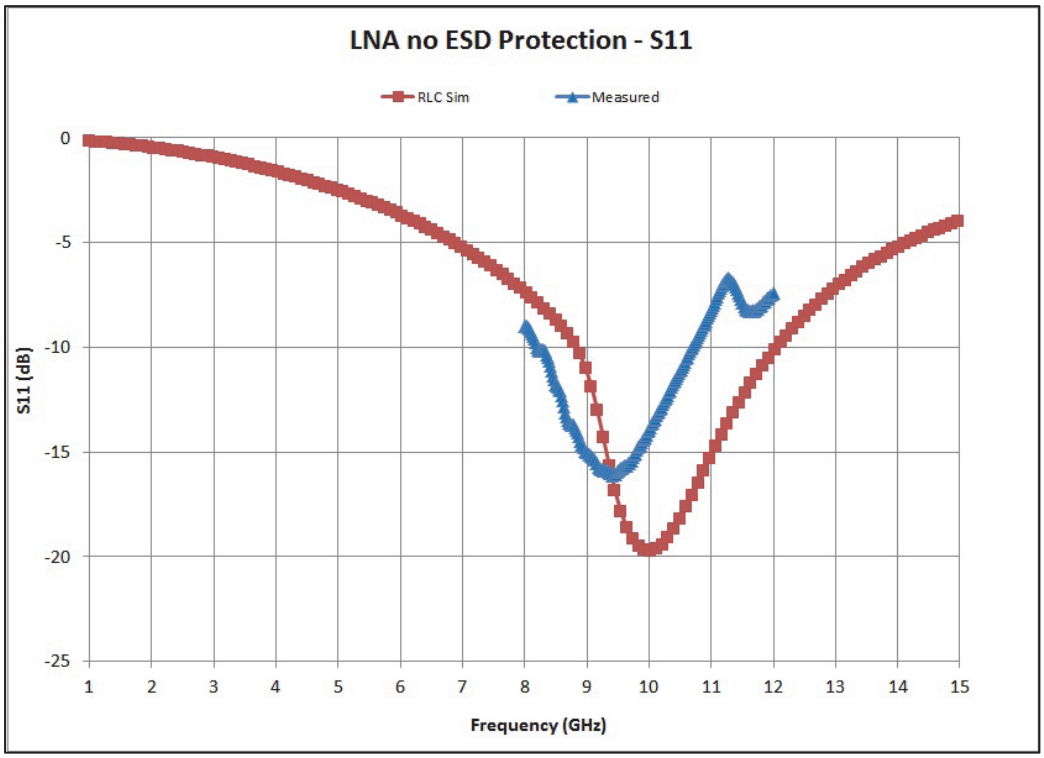


Figure 4.8 – LNA without ESD Protection Simulation vs. Measured – S11

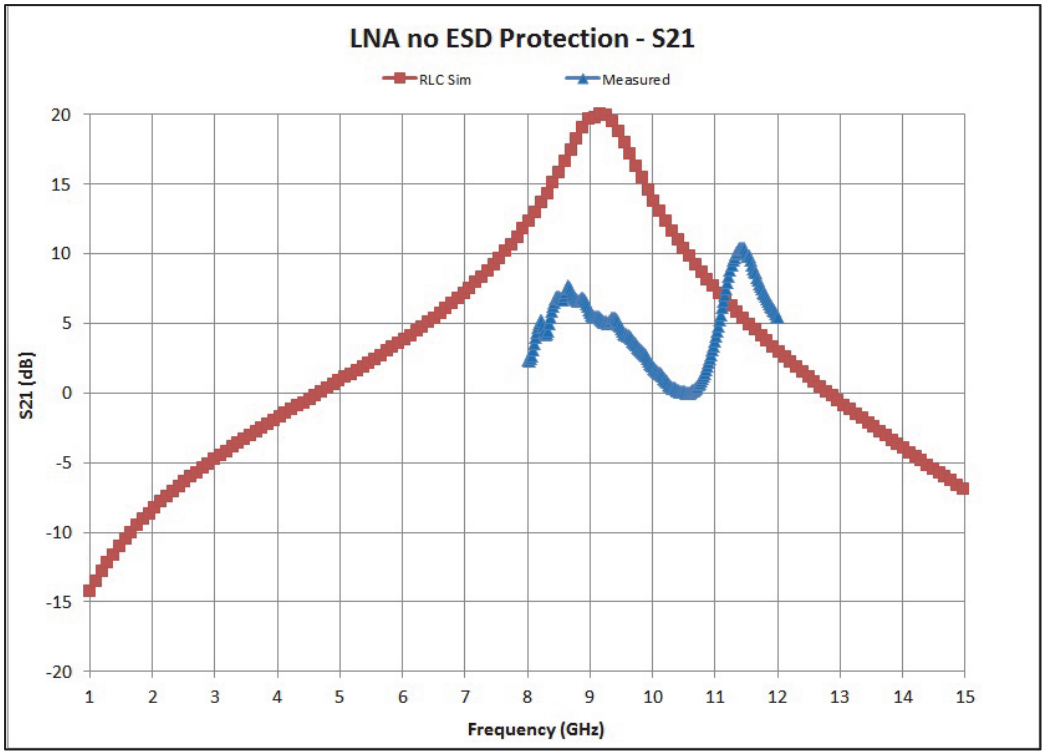


Figure 4.9 – LNA without ESD Protection Simulation vs. Measured – S21

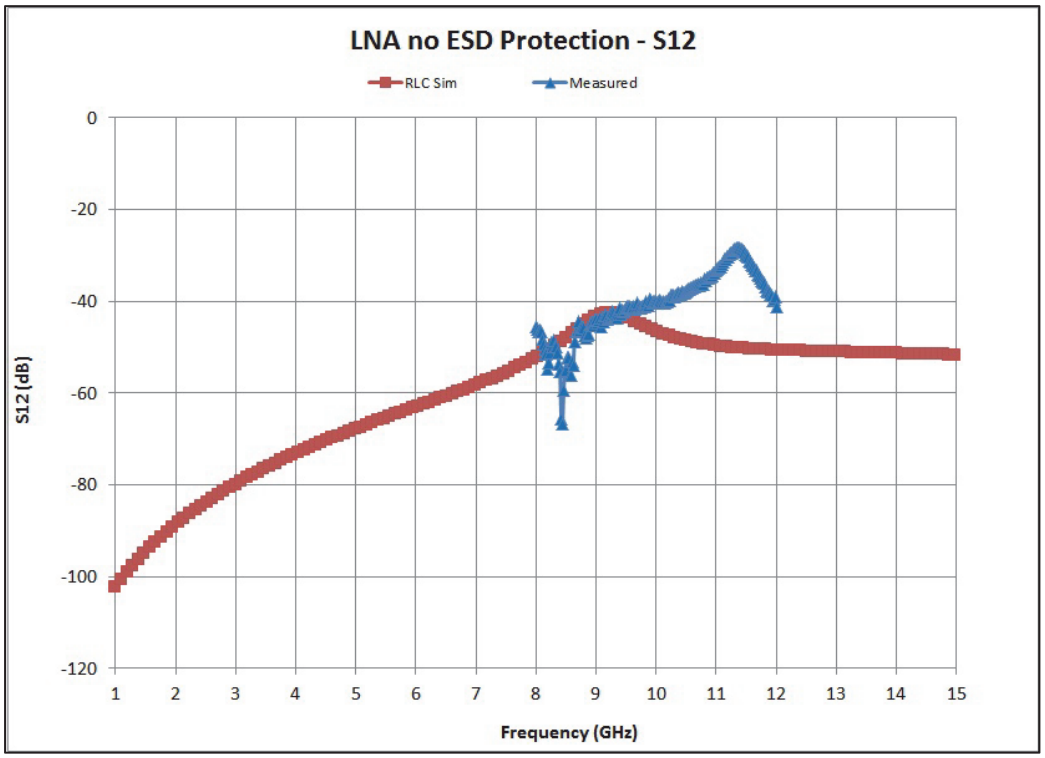


Figure 4.10 – LNA without ESD Protection Simulation vs. Measured – S12

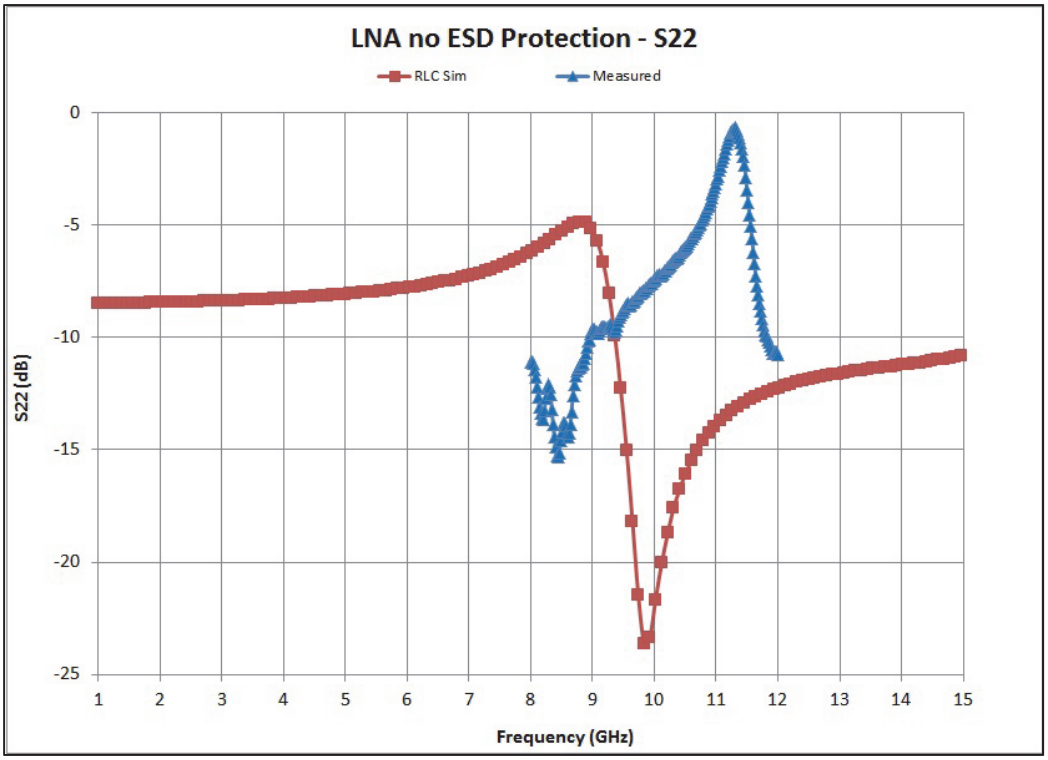


Figure 4.11 – LNA without ESD Protection Simulation vs. Measured – S22

4.1.4 LNA with ESD vs. LNA without ESD Measured Results

As RC circuit extraction data sets were used to tune the LNA without and the LNA with ESD protection, a frequency shift on the measured S-parameters was observed. This shift makes it difficult to compare the measured results, and therefore only the simulated results are compared.

4.2 Pre and Post ESD Stress Results Comparison

The ESD HBM testing was performed at the chip level using the Key Tech Zap Master ESD testing equipment and two probes. The lowest ESD HBM stress voltage allowed by the equipment is 50 V.

4.2.1 LNA without ESD Protection

The LNA without ESD protection, as expected, has failed the lowest ESD HBM stress voltage (50 V) for both RF_{in} vs. V_{SS} and RF_{in} vs. V_{DD2}. The pin combination V_{DD2} vs. V_{SS} failed at 500 V as there is no transistor gate directly connected to the power supply rail.

It was noticed, when measuring an LNA without ESD protection that was not ESD stressed that the noise figure has decreased on average by 1.7 dB. The same NFA calibration procedure was performed pre and post ESD test before measuring noise figure, and the source of this difference was not found. However, this difference was taken into account when analyzing the noise figure results post ESD testing.

Figure 4.12 to Figure 4.16 show a comparison of the LNA parameters pre and post ESD testing. The parameters most affected by the ESD zap were the noise figure, S21, and S11. Figure 4.17 shows the curve trace results performed pre (green line) and post (red line) 50 V ESD stress. The post stress curve shows a short circuit between the RF_{in} and V_{SS}.

The ESD test plan with complete summary of the ESD testing with results of the curve trace, and electrical test (S-parameters and noise figure) are shown in Table 4.2. The electrical test failure criteria used was 10% of the results of the pre-ESD zap. Once a failure was observed, ESD test for that pin combination at a higher voltage level was not performed.

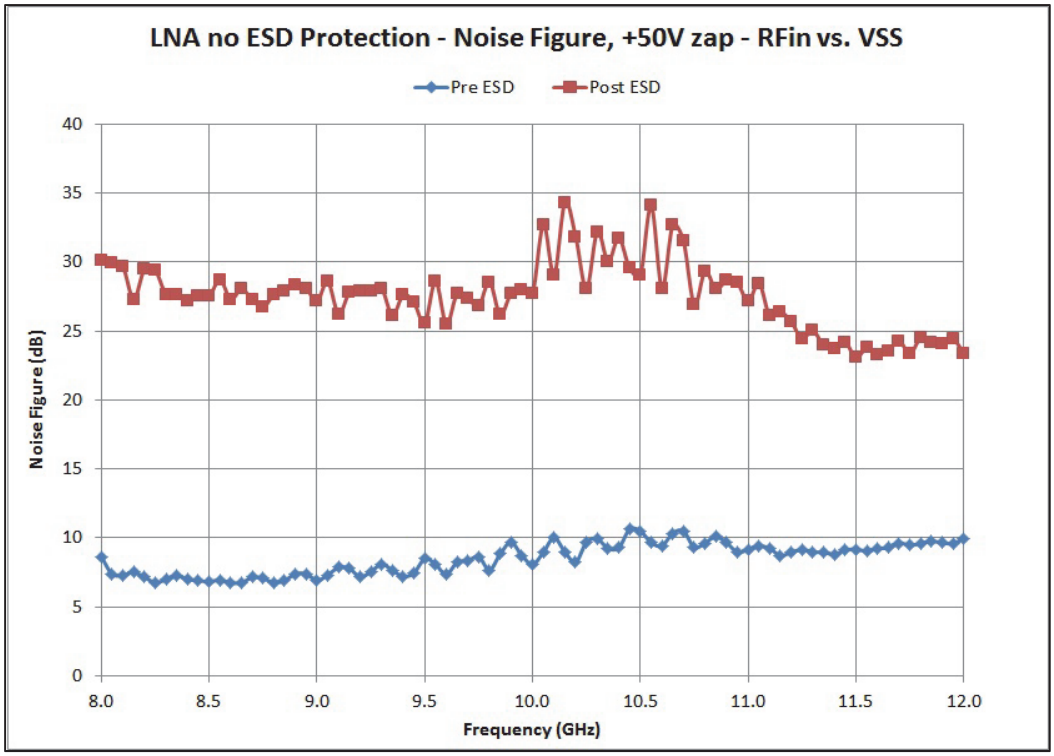


Figure 4.12 – LNA no ESD Protection, Noise Figure – +50 V RF_{in} vs. V_{SS}

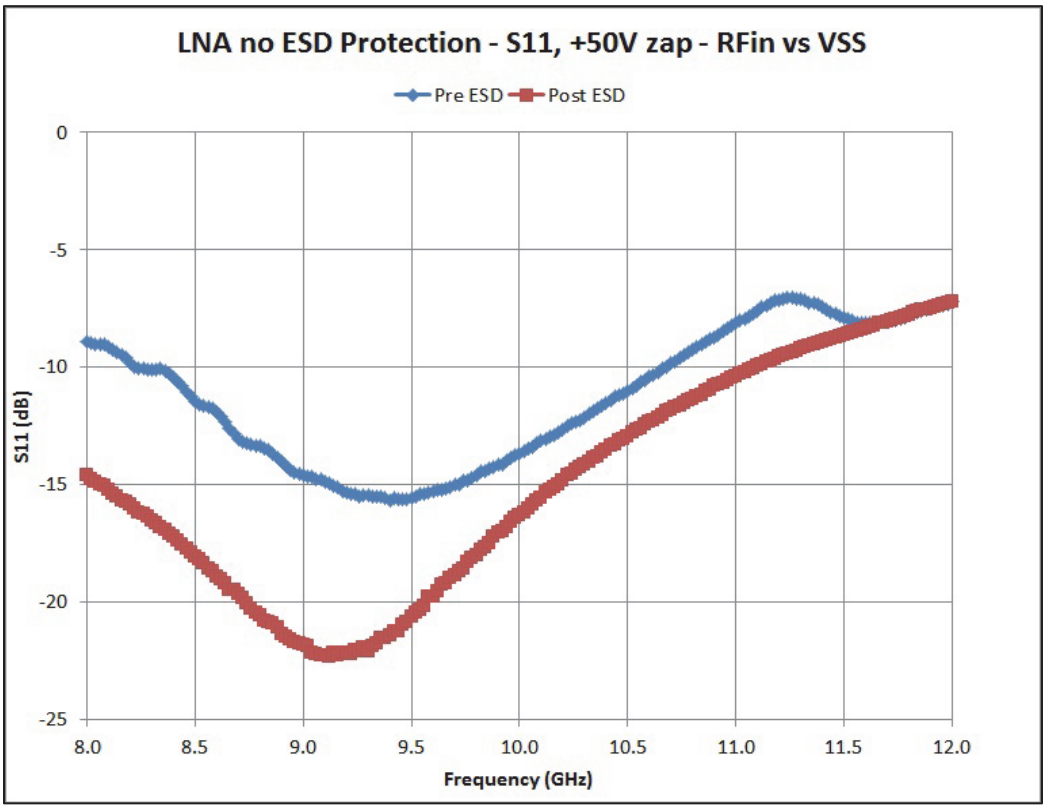


Figure 4.13 – LNA no ESD Protection, S11 – +50 V RF_{in} vs. V_{SS}

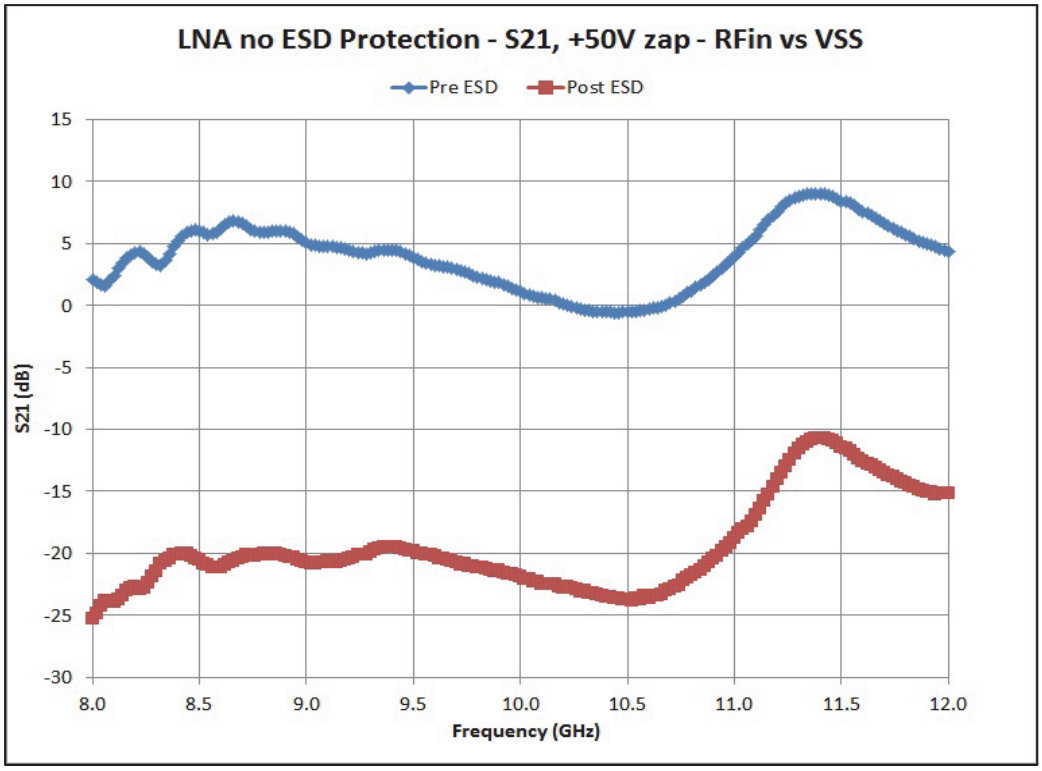


Figure 4.14 – LNA no ESD Protection, S21 – +50 V RF_{in} vs. V_{SS}

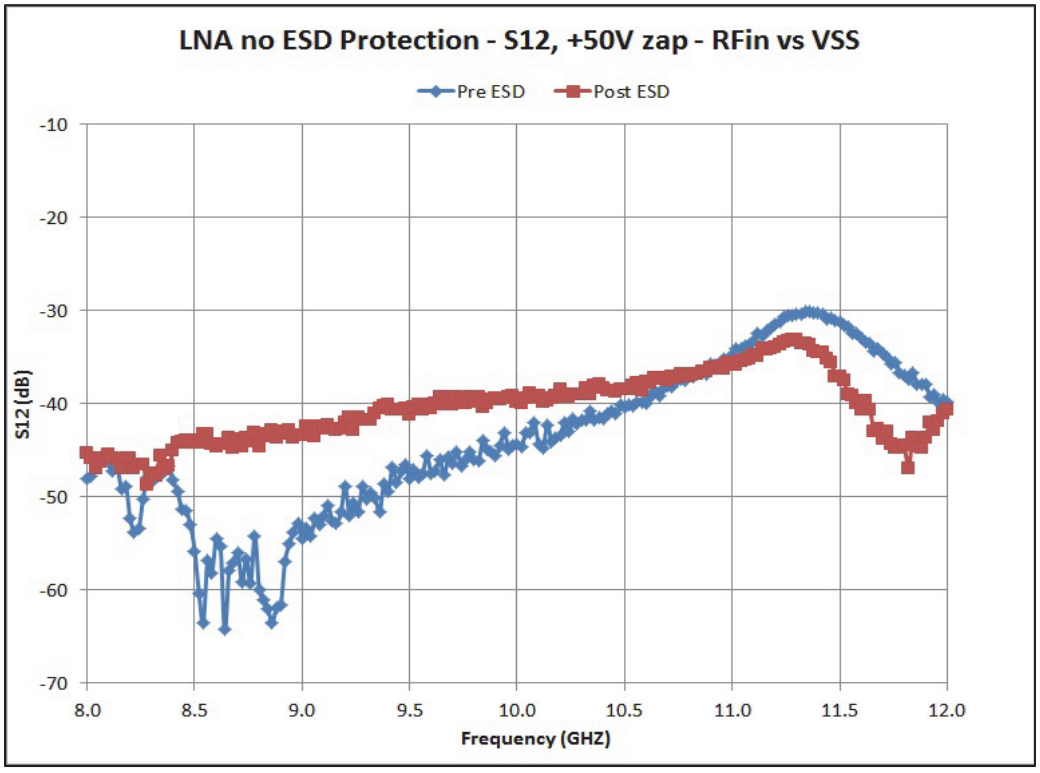


Figure 4.15 – LNA no ESD Protection, S12 – +50 V RF_{in} vs. V_{SS}

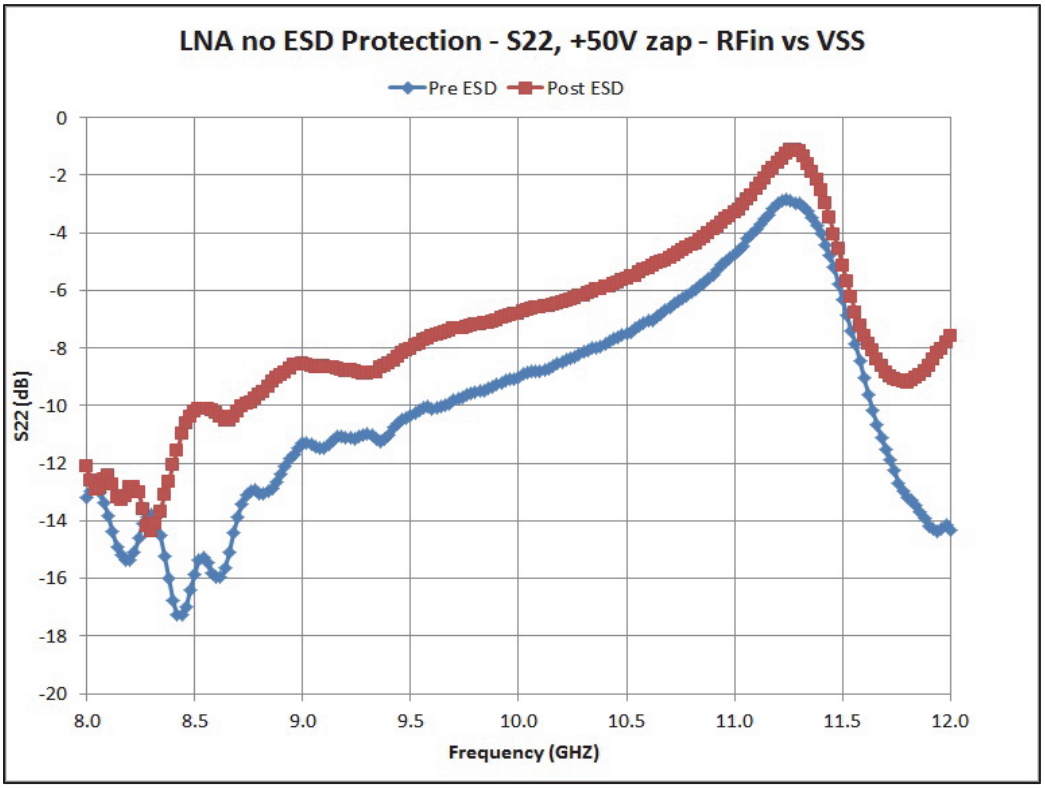


Figure 4.16 – LNA no ESD Protection, S22 – +50 V RF_{in} vs. V_{SS}

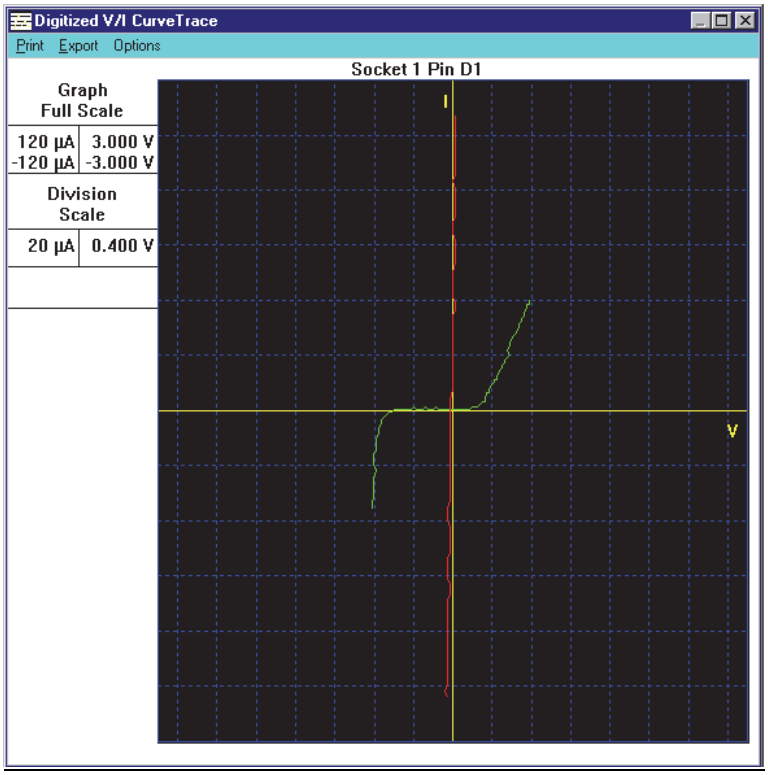


Figure 4.17 – LNA no ESD Protection, Curve Trace Pre and Post +50 V Zap, RF_{in} vs. V_{SS}

Table 4.2 – LNA no ESD Protection ESD HBM Test Plan and Results

Pin Group	Voltage	Chip #	Curve Trace	Electrical Test
RF_{in} vs. V_{SS}	+50	4	Short	Fail
	-50	5	Short	Fail
RF_{in} vs. V_{DD2}	±50	8	Leakage	Fail
V_{DD2}vs. V_{SS}	±50	9	Pass	Pass
	±100	10	Pass	Pass
	±250	11	Pass	Pass
	±500	12	Pass	Fail
	±1000	13	Short	Fail

4.2.2 LNA with ESD Protection

Sub-section 4.2.2.1 shows the measurement results of an LNA device that was not ESD stressed, sub-section 4.2.2.2 shows the results for the 2 KV HBM testing, sub-section 4.2.2.3 shows the curve trace test results for the 4 KV HBM testing, sub-section 4.2.2.4 shows the 8 KV HBM testing results, and sub-section 4.2.2.5 shows the ESD test plan with complete summary of the ESD testing including the results of curve trace, S-parameters and noise figure measurements.

The LNA with ESD protection has passed ESD HBM stress voltage up to 2 KV for all pin combinations RF_{in} vs. V_{SS}, RF_{in} vs. V_{DD2}, and V_{DD2} vs. V_{SS}.

In order to test above 2 KV, as not enough unstressed devices were left, one device (No. 15) was zapped at 4 KV for all pin combinations with no curve trace failure; then it was zapped at 8 KV and it failed curve trace for the RF_{in} vs. VDD_2 pin combination. For this device, the S-parameters and noise figure measurements post ESD

stress are only available for the last pin combination stress condition (-8 KV, RF_{in} vs. VDD_2).

4.2.2.1 LNA Device Not ESD Stressed

An LNA device not ESD stressed was used to correlate the measurements before and after ESD stress. This device showed a difference in the measurements done with the calibration before ESD stress and after ESD stress for both the network analyzer (S-parameters) and NFA (noise figure). The calibration for the two sets of measurements was performed using the same procedure.

It was observed that the amount of force applied to the probes may slightly change the results of the measurements. Therefore during the measurements attempts were made to apply the same force to the probes.

Two LNA devices with ESD protection that were not ESD stressed show similar differences, as do all devices stressed that were not damaged by the ESD stress (< 4KV). This shows that the difference is not related to the stress, but is related to the measurement equipment, calibration, or probes.

Figure 4.18 to Figure 4.22 show the S-parameters and noise figure measurements of a device not ESD stressed. For S11, it is observed that the second measurement has about +1 dB difference at the two valleys at about 9.1 GHz and 11.5 GHz. For S21 the second measurement shows a higher S21. For S12, both curves agree over almost the entire range, but between 11.5 GHz and 12 GHz, the second measurement shows a high value. S22 shows about a -1 dB improvement in almost the whole range, with a deeper

valley at 11.75 GHz. The noise figure shows on average -2 dB difference in the second measurement in the whole measurement range.

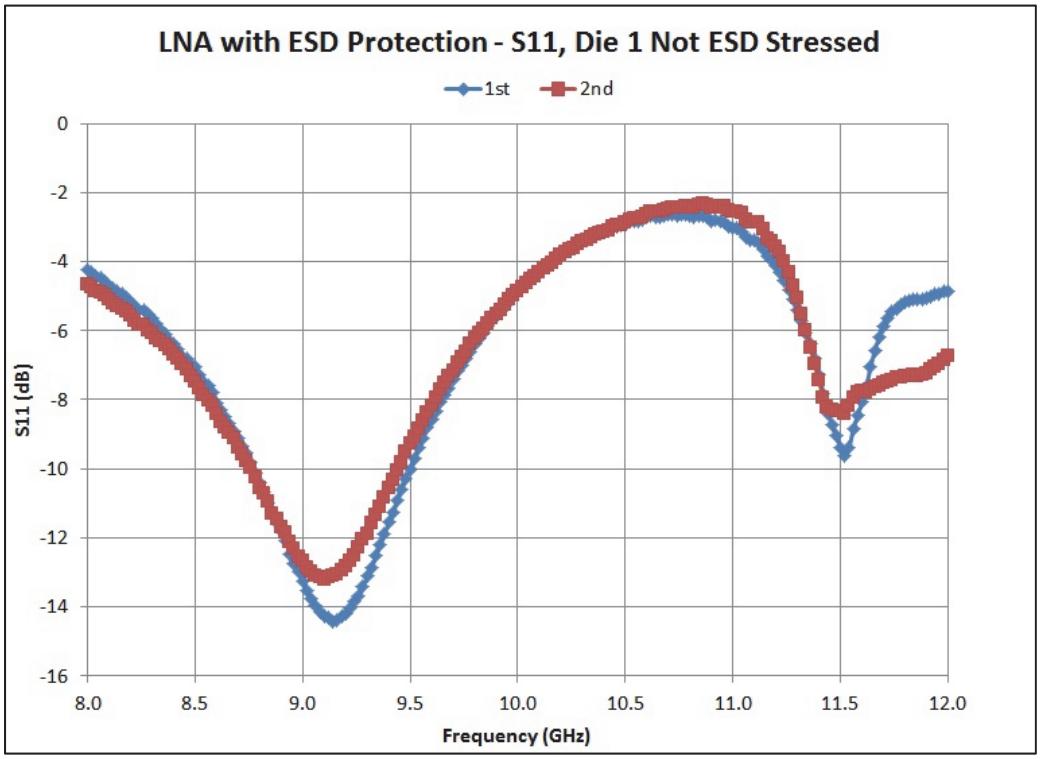


Figure 4.18 – LNA with ESD Protection, Correlation Device – S11

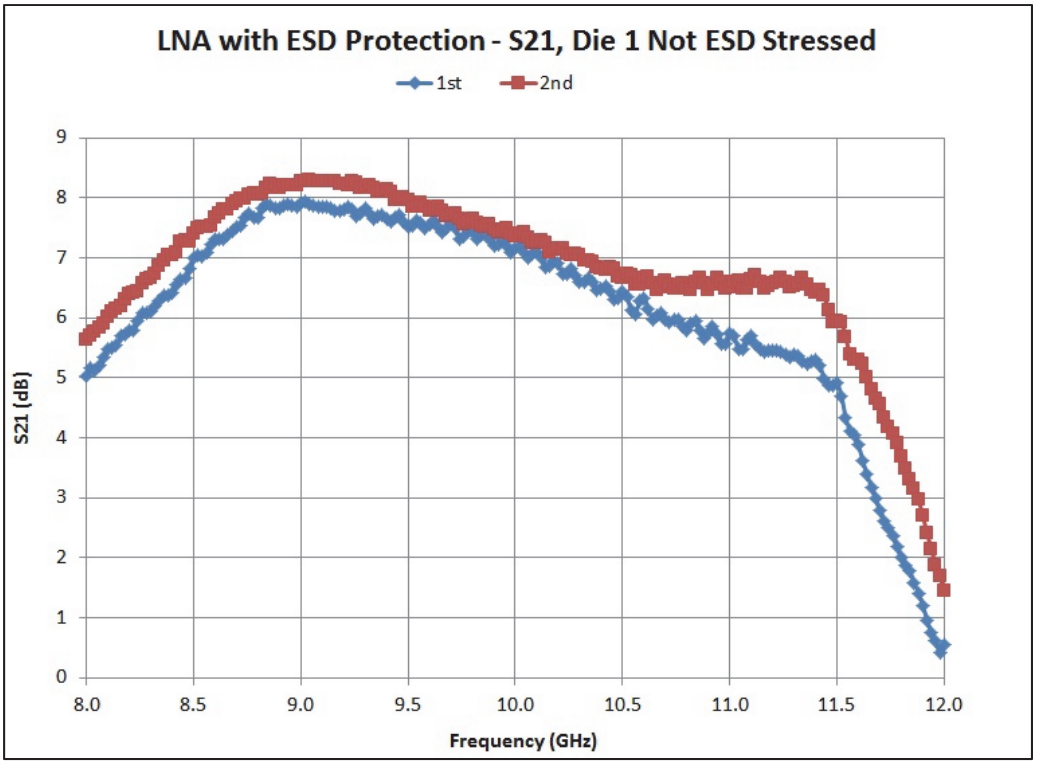
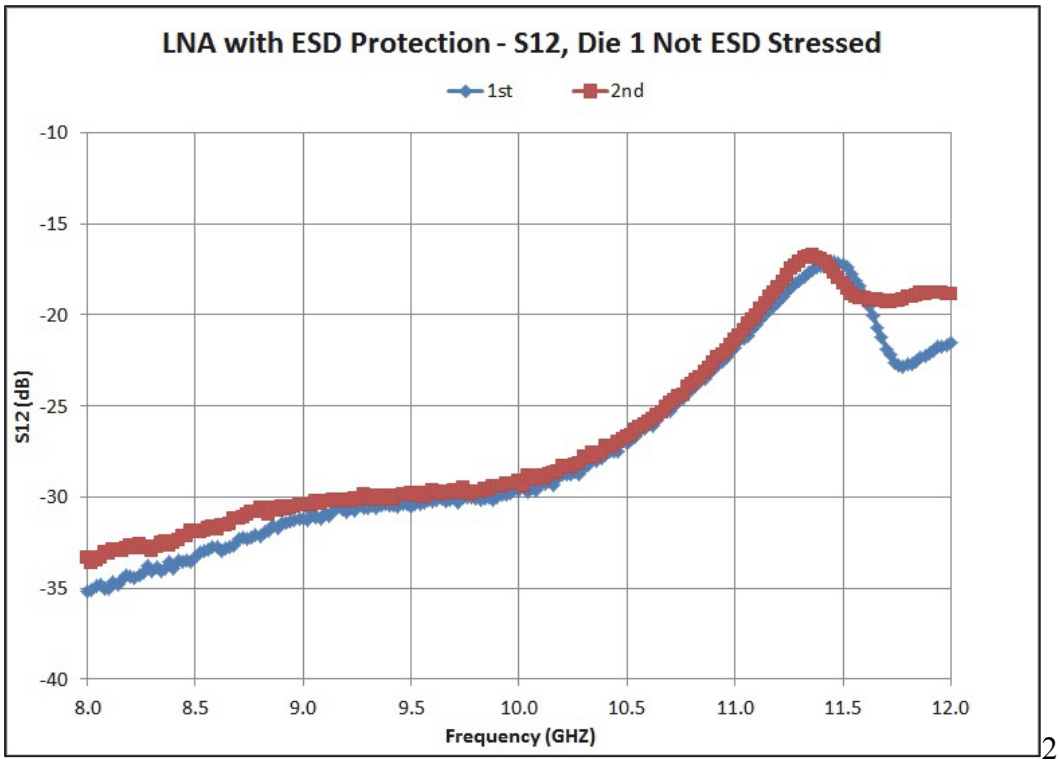


Figure 4.19 – LNA with ESD Protection, Correlation Device – S21



2

Figure 4.20 – LNA with ESD Protection, Correlation Device – S.12

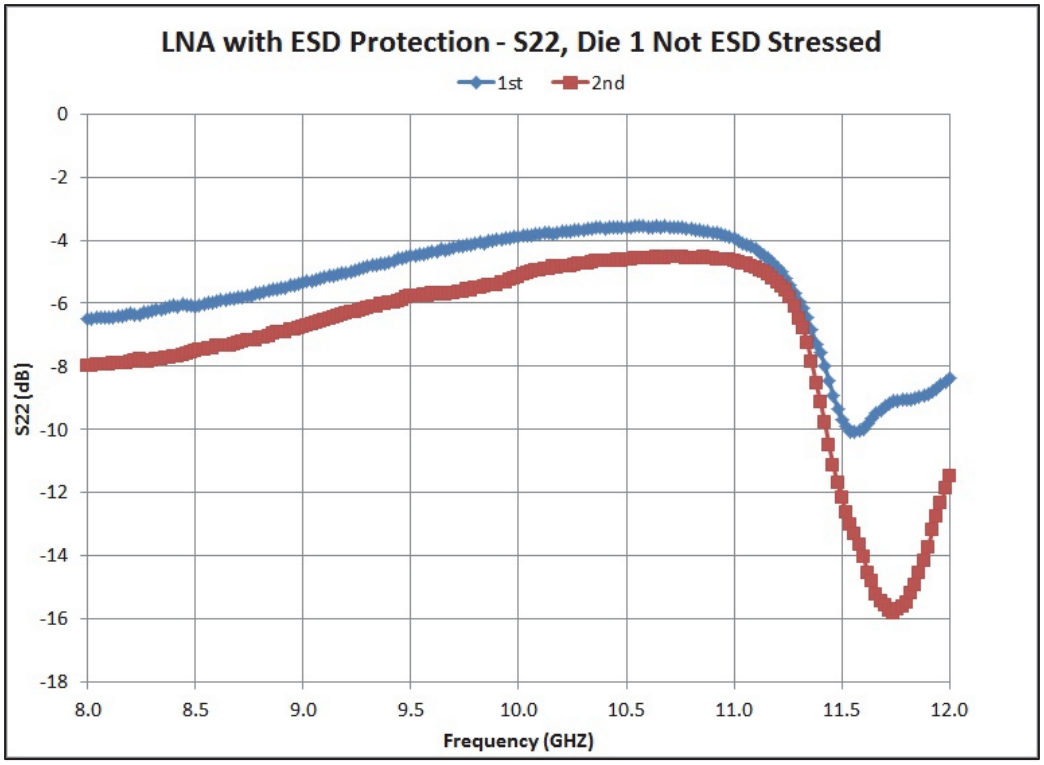


Figure 4.21 – LNA with ESD Protection, Correlation Device – S22

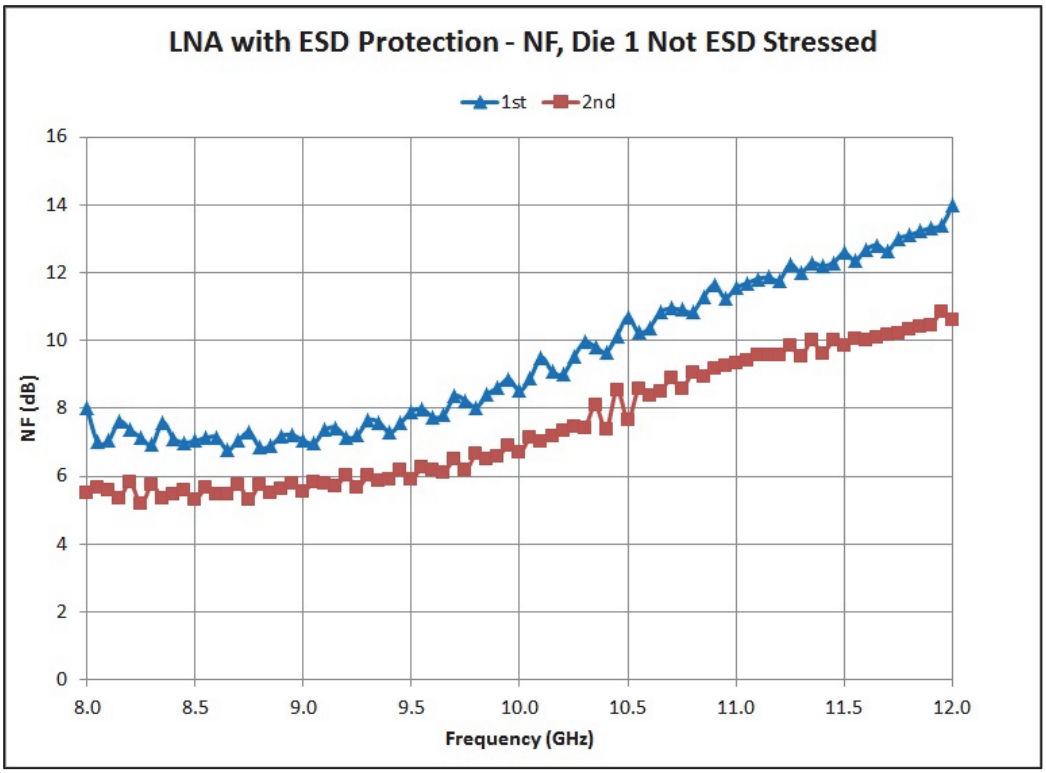


Figure 4.22 – LNA with ESD Protection, Correlation Device – Noise Figure

4.2.2.2 ESD HBM 2 KV Testing Results

Figure 4.23 to Figure 4.27 show the pre and post S-parameters and noise figure results for 2 KV ESD HBM stress for the RF_{in} vs. V_{SS} pin combination for device number 32. The curve trace results pre and post ESD stress are shown in Figure 4.28.

It was noticed in the LNA measurement results of the 2 KV zap that the differences in the S-parameter and noise figure were similar to the differences observed for the correlation device. Comparing the pre and post ESD zap measurement results and the measurement results of the correlation device, it was concluded that no significant change was observed in any of the S-parameters and noise figure.

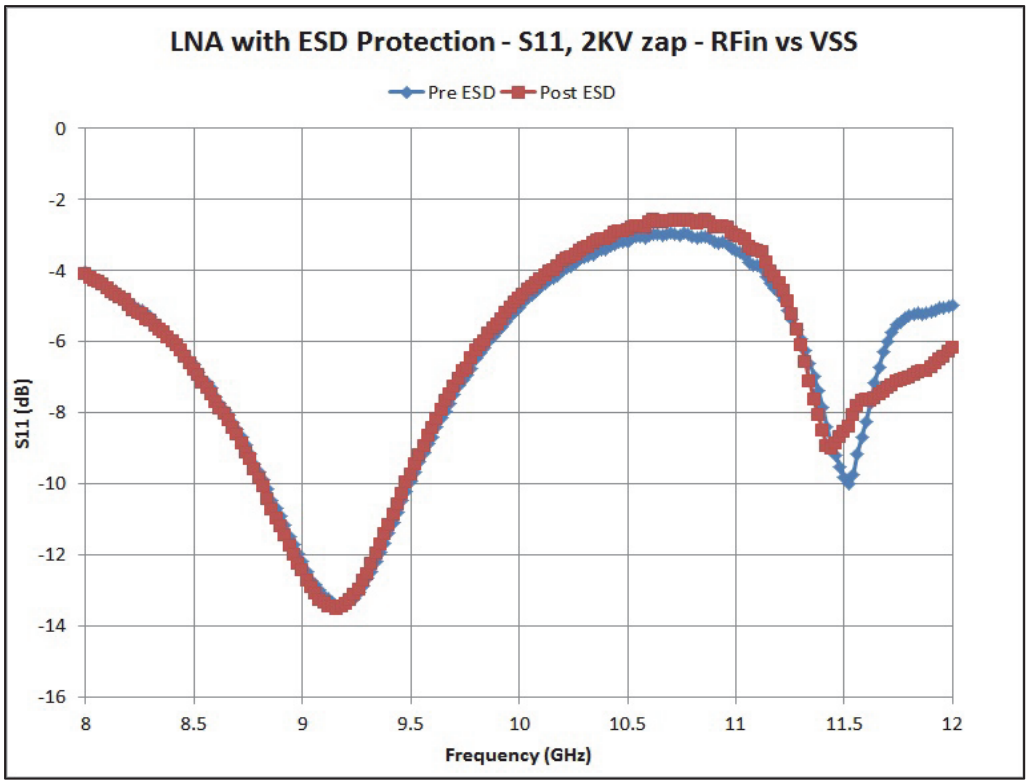


Figure 4.23 – LNA with ESD Protection – S11, 2 KV Zap – RF_{in} vs. V_{SS}

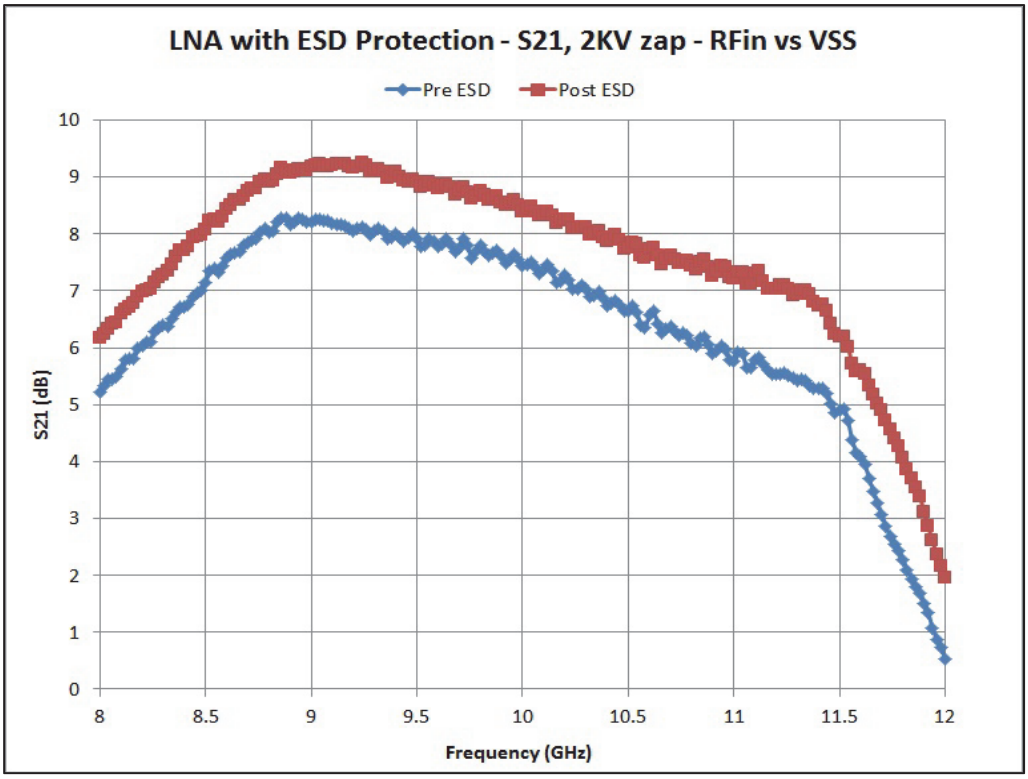


Figure 4.24 – LNA with ESD Protection – S21, 2 KV Zap – RF_{in} vs. V_{SS}

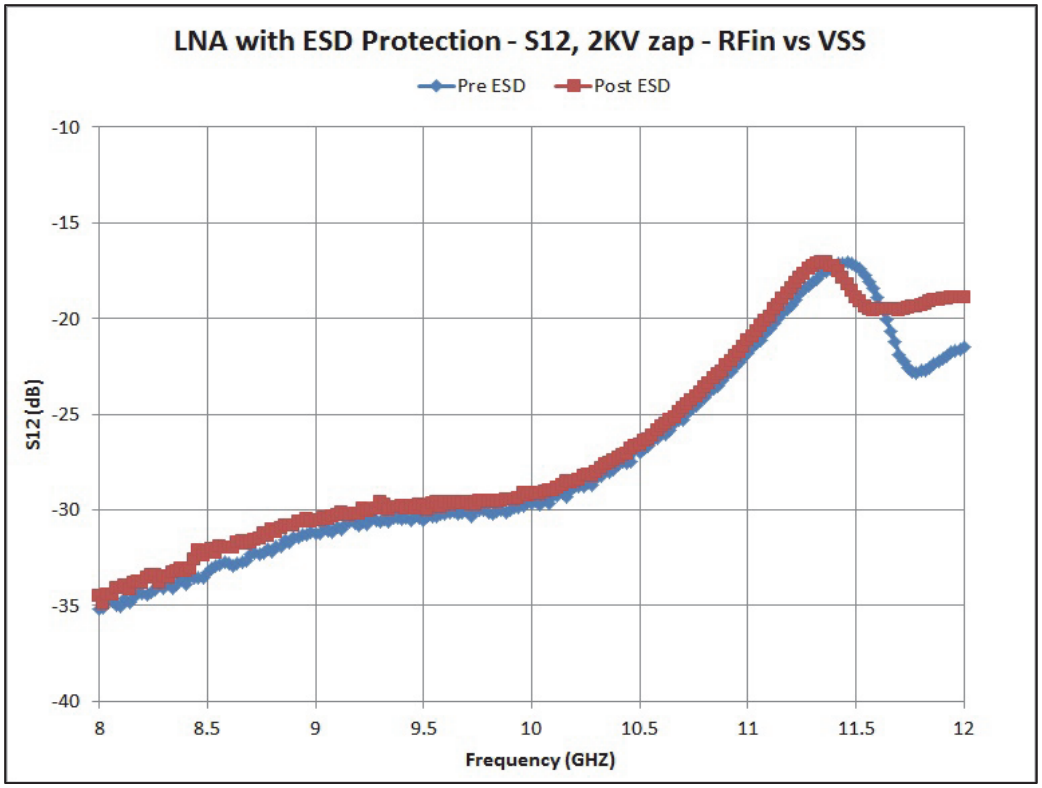


Figure 4.25 – LNA with ESD Protection – S12, 2KV Zap – RF_{in} vs. V_{SS}

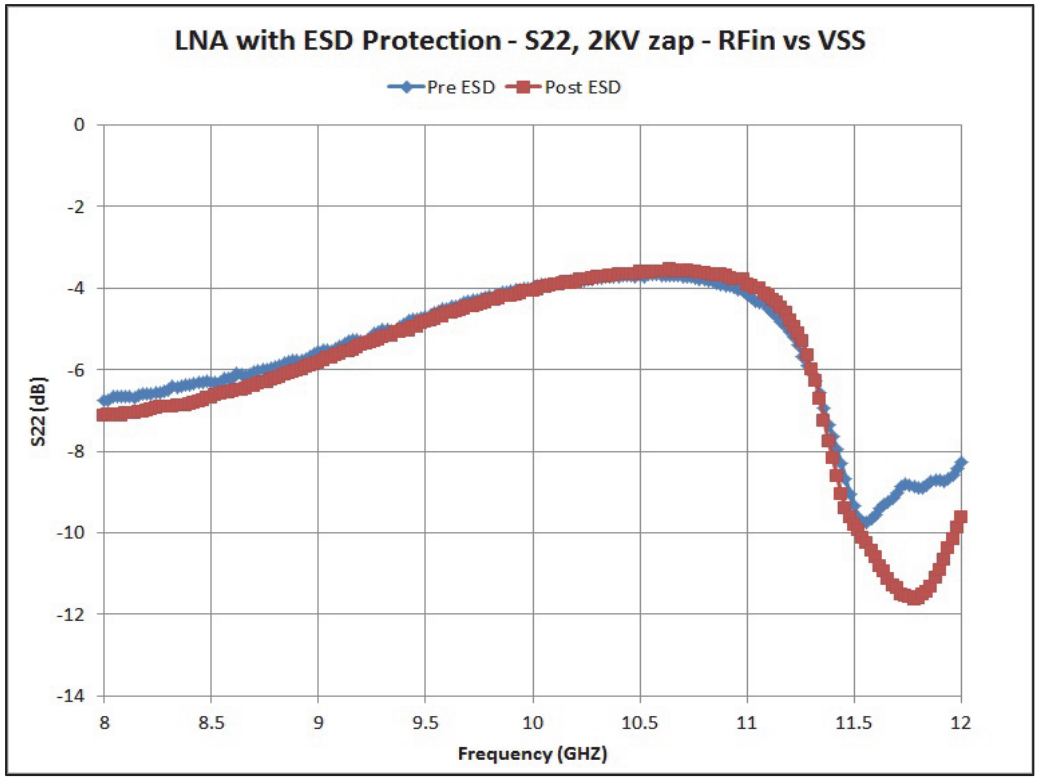


Figure 4.26 – LNA with ESD Protection – S22, 2 KV Zap – RF_{in} vs. V_{SS}

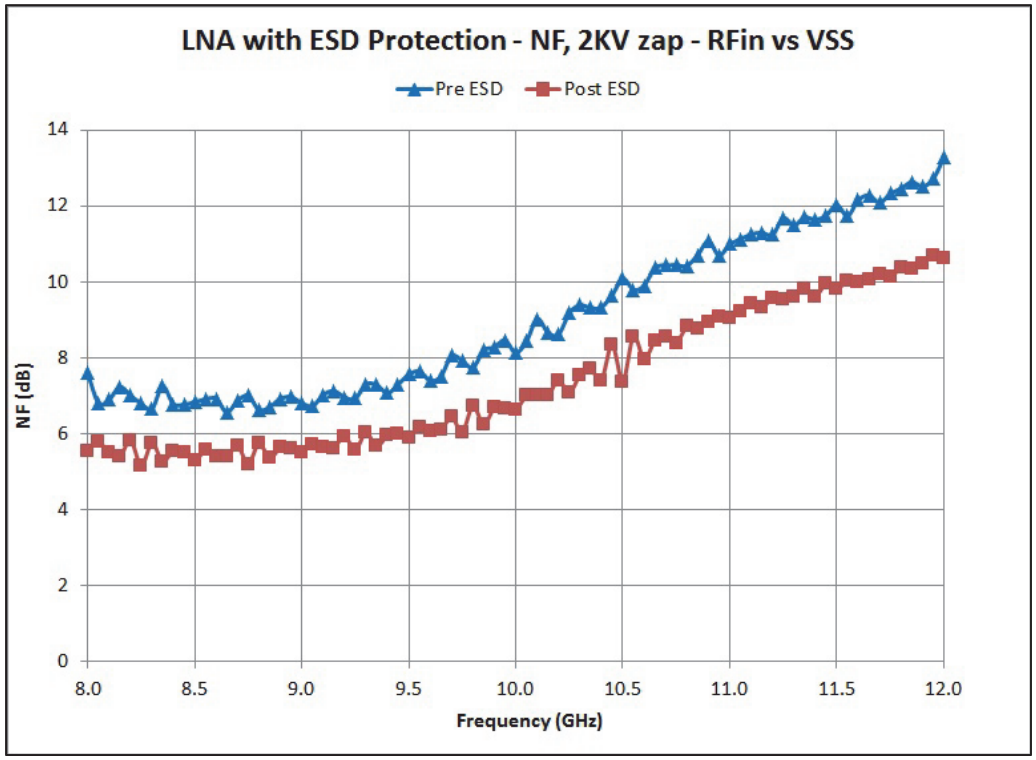


Figure 4.27 – LNA with ESD Protection – Noise Figure – 2 KV Zap – RF_{in} vs. V_{SS}

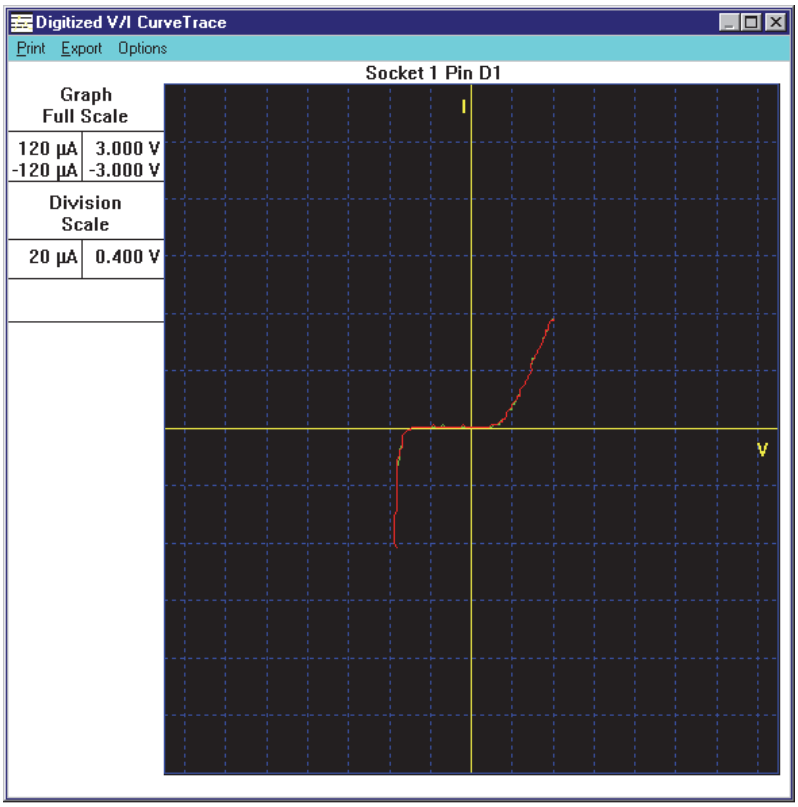


Figure 4.28 – LNA with ESD Protection – Curve Trace Pre and Post 2 KV Zap – RF_{in} vs. V_{SS}

Figure 4.29 to Figure 4.33 show the pre and post S-parameters and noise figure results for 2 KV ESD HBM stress for the RF_{in} vs. V_{DD2} pin combination for device number 35. The curve trace results pre and post ESD stress are shown in Figure 4.34.

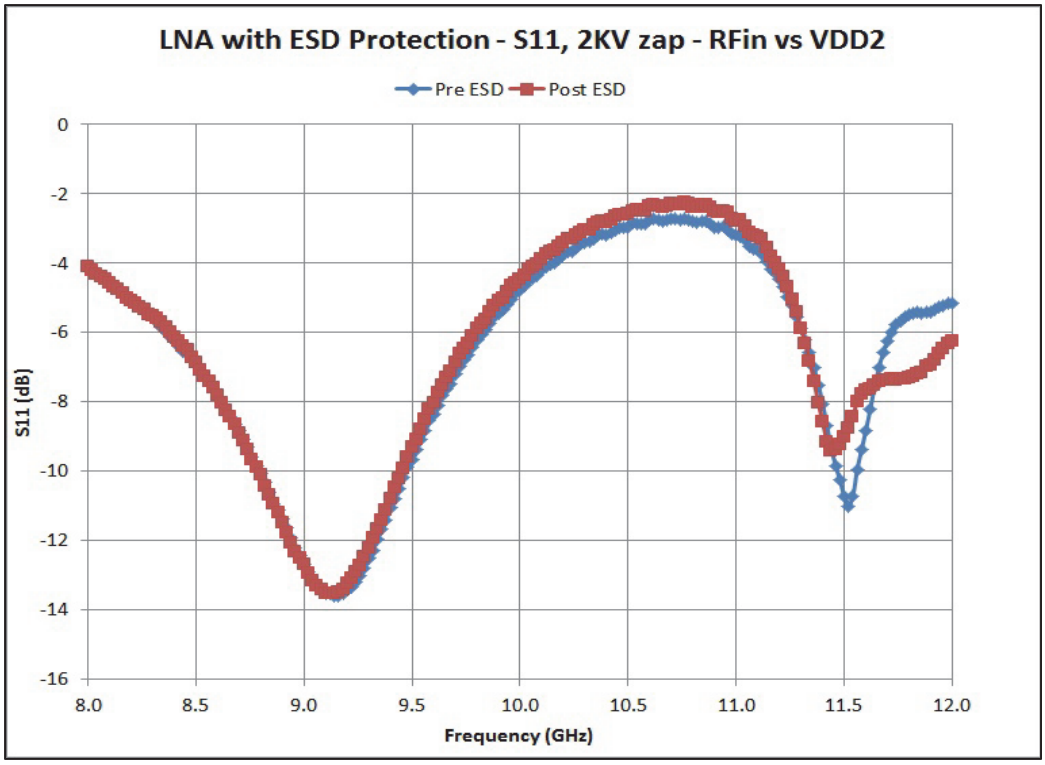


Figure 4.29 – LNA with ESD Protection – S11, 2 KV Zap – RF_{in} vs. V_{DD2}

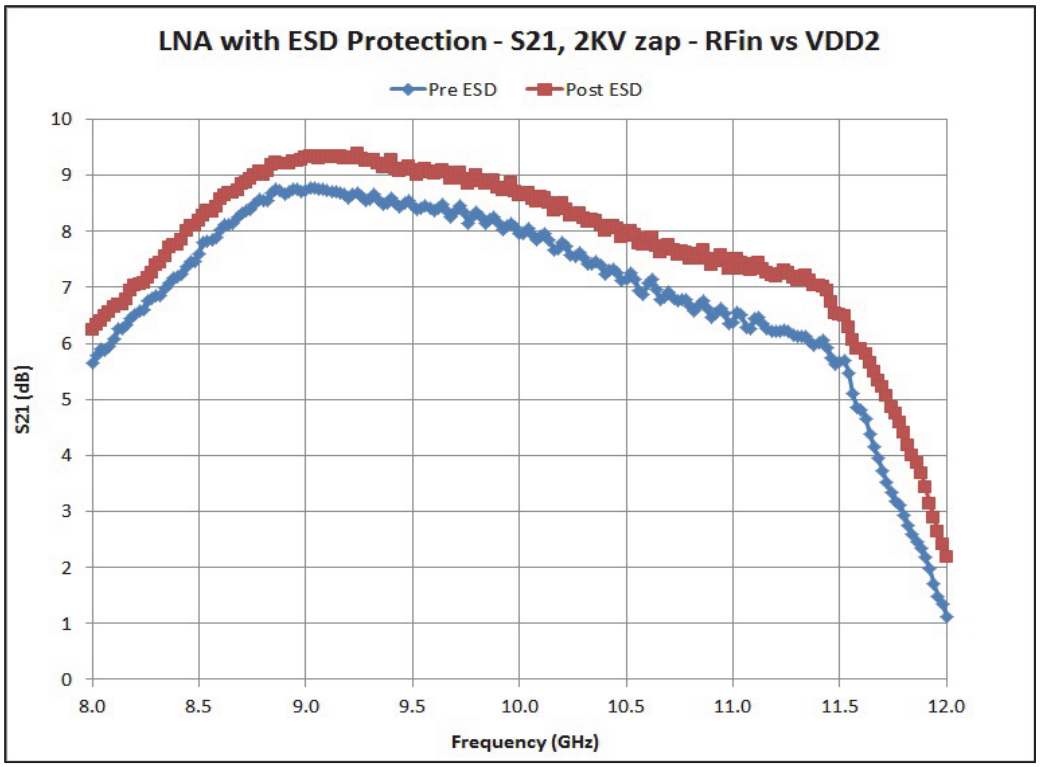


Figure 4.30 – LNA with ESD Protection – S21, 2 KV Zap – RF_{in} vs. V_{DD2}

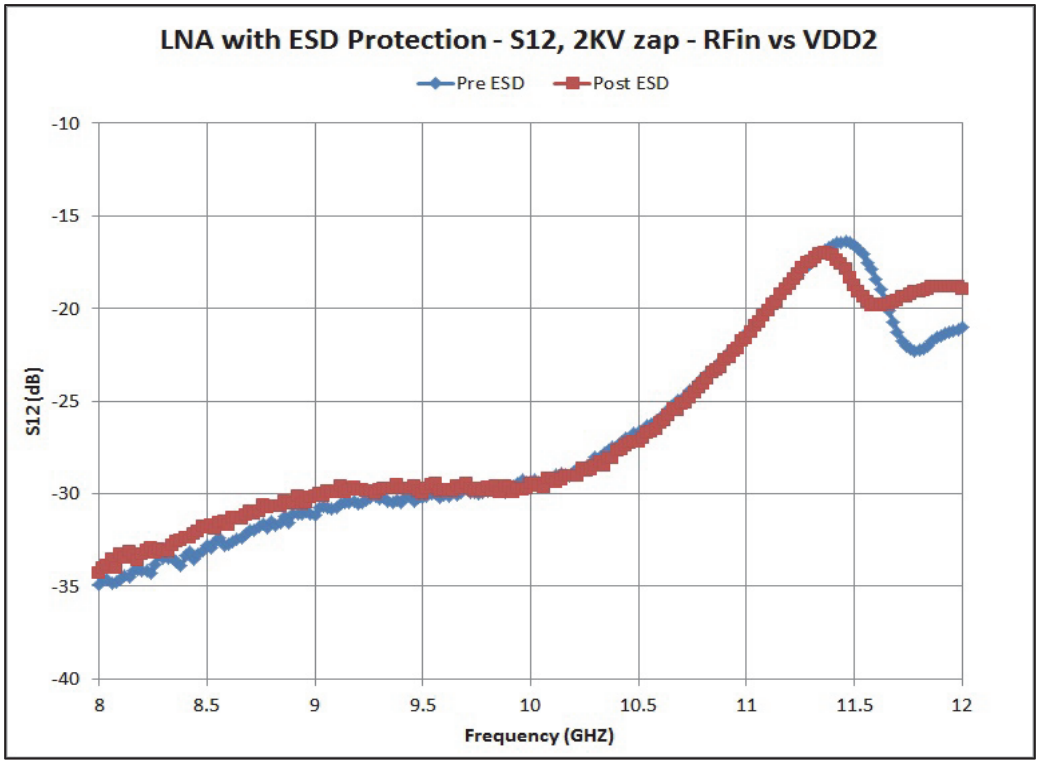


Figure 4.31 – LNA with ESD Protection – S12, 2 KV Zap – RF_{in} vs. V_{DD2}

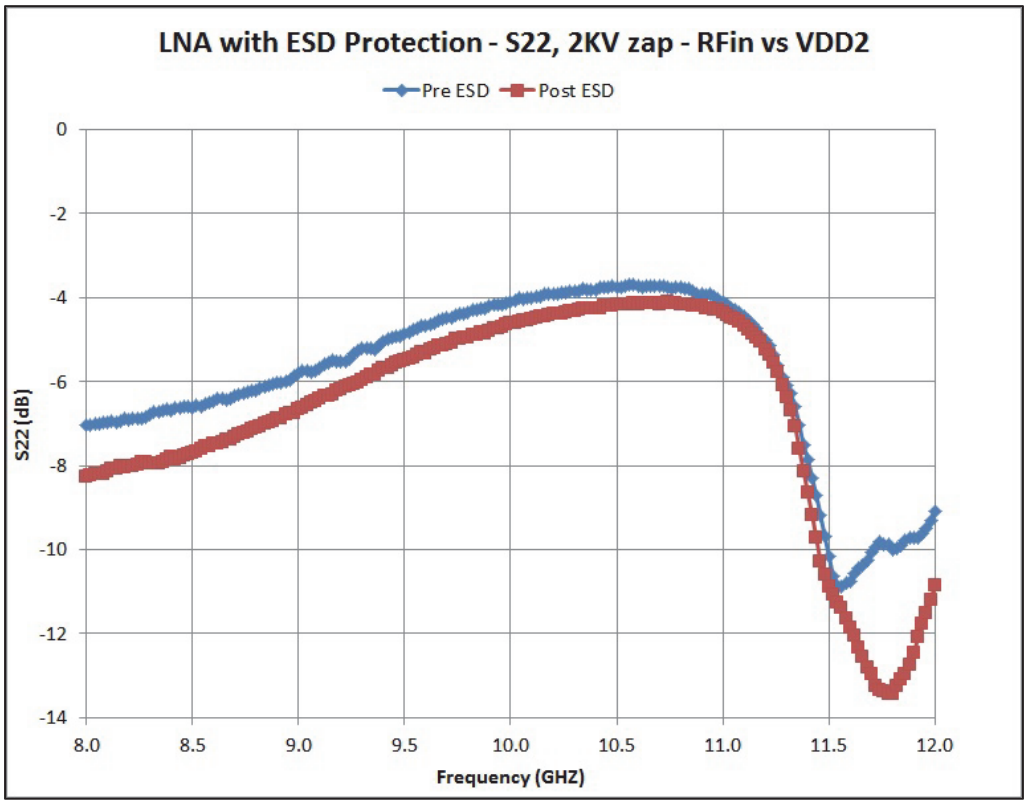


Figure 4.32 – LNA with ESD Protection – S22, 2 KV Zap – RF_{in} vs. V_{DD2}

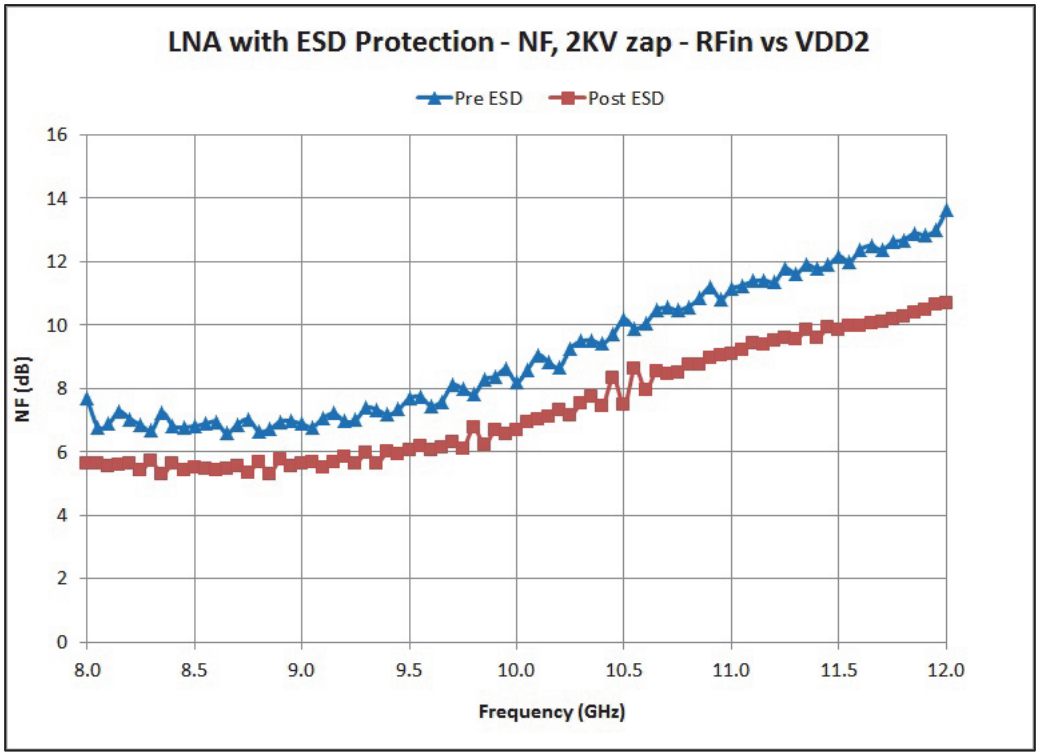


Figure 4.33 – LNA with ESD Protection – Noise Figure, 2 KV Zap – RF_{in} vs. V_{DD2}

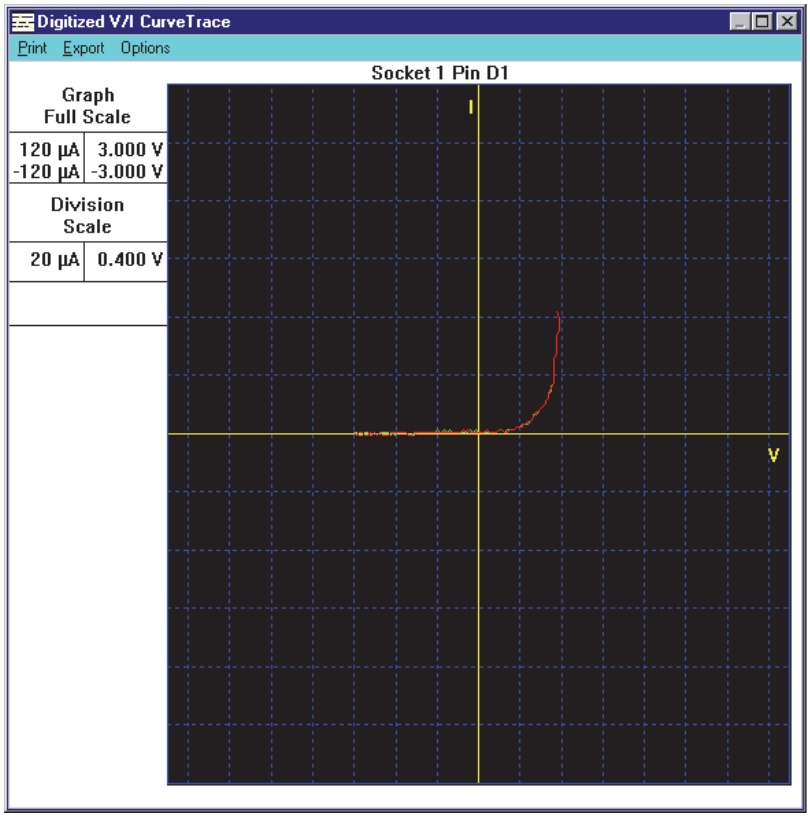


Figure 4.34 – LNA with ESD Protection – Curve Trace Pre and Post 2 KV Zap – RF_{in} vs. V_{DD2}

Figure 4.35 to Figure 4.39 show the pre and post ESD testing results for S-parameters and noise figure measurements for 2 KV ESD HBM stress for the V_{DD2} vs. V_{SS} pin combination for device number 38. The curve trace results pre and post ESD stress are shown in Figure 4.40.

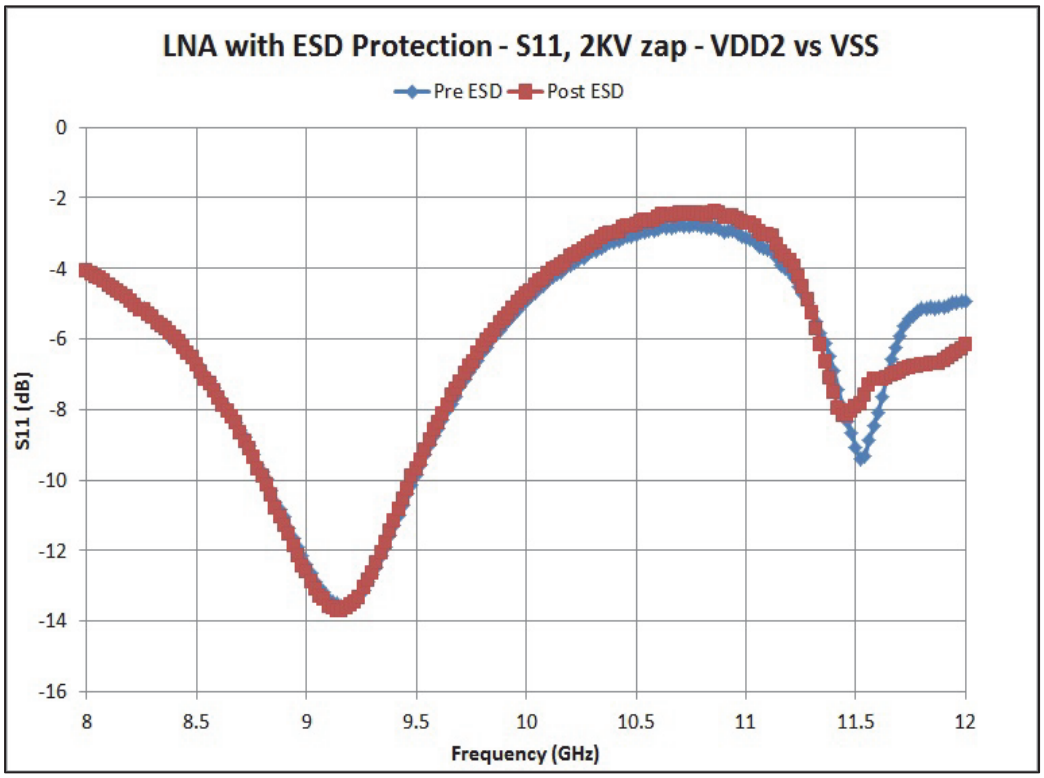


Figure 4.35 – LNA with ESD Protection – S11, 2 KV Zap – V_{DD2} vs. V_{SS}

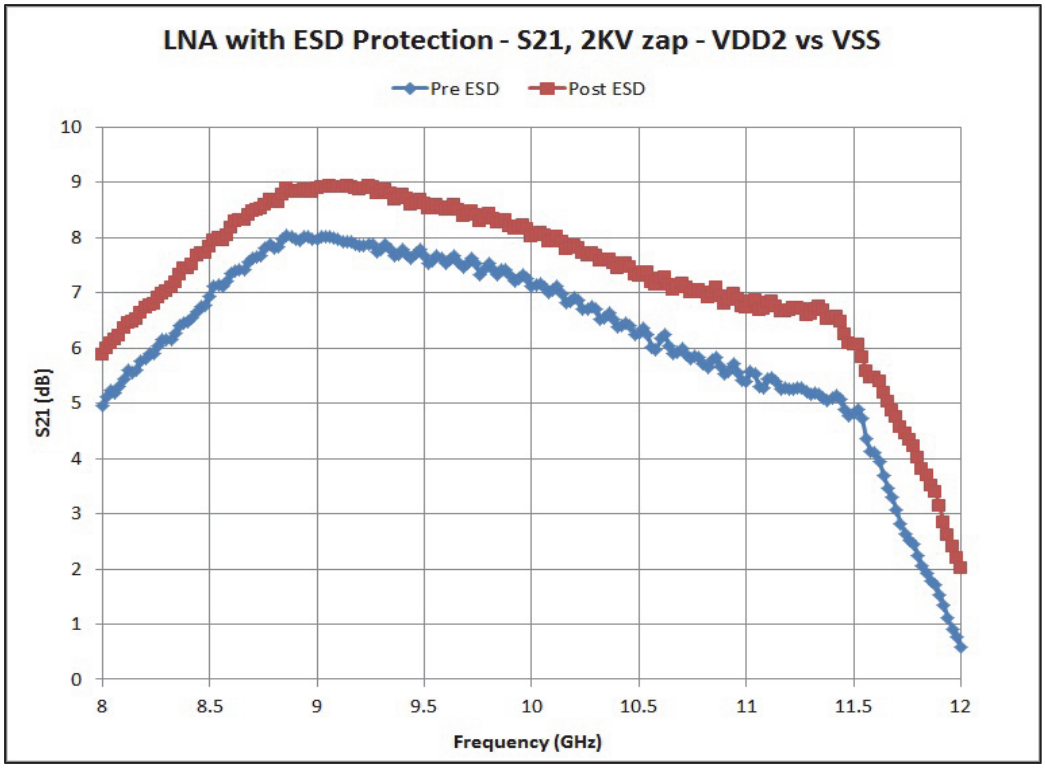


Figure 4.36 – LNA with ESD Protection – S21, 2 KV Zap – V_{DD2} vs. V_{SS}

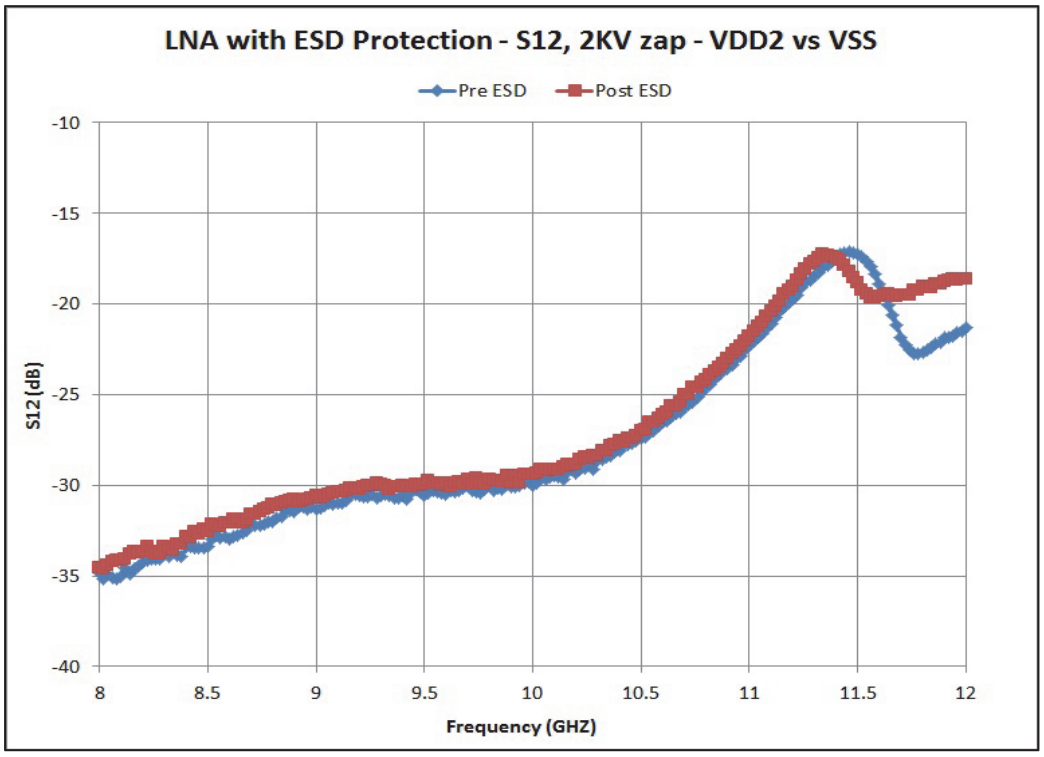


Figure 4.37 – LNA with ESD Protection – S12, 2 KV Zap – V_{DD2} vs. V_{SS}

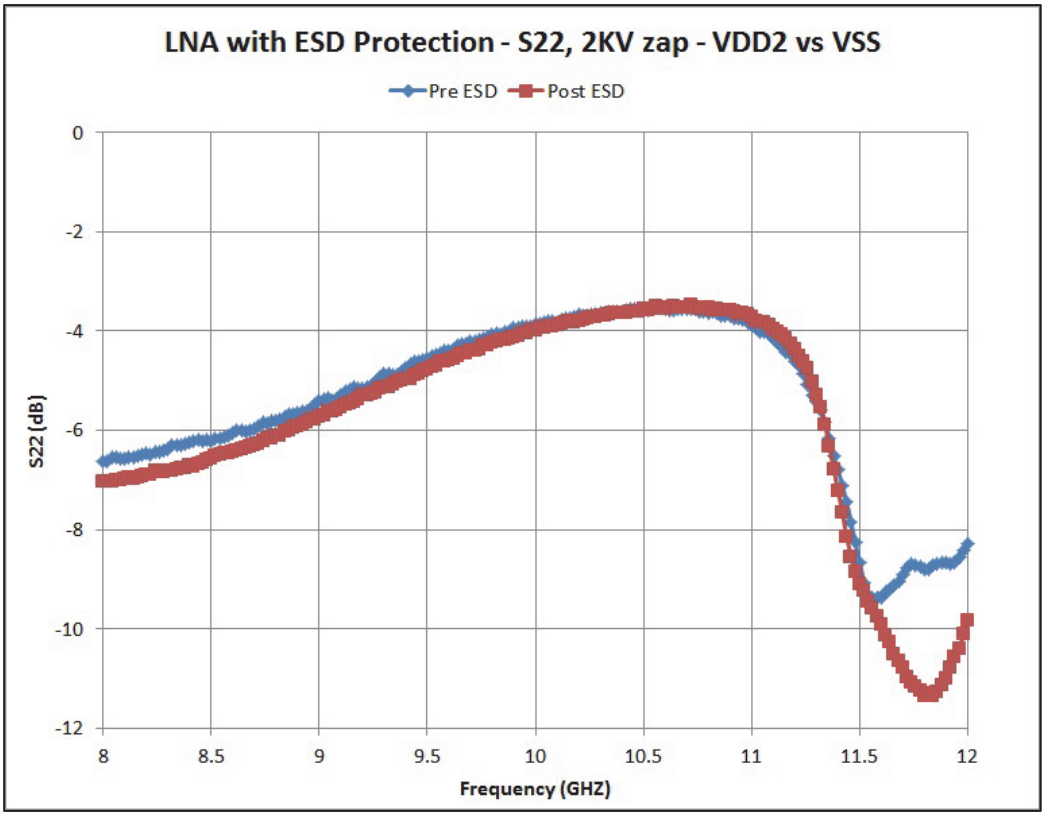


Figure 4.38 – LNA with ESD Protection – S22, 2 KV Zap – V_{DD2} vs. V_{SS}

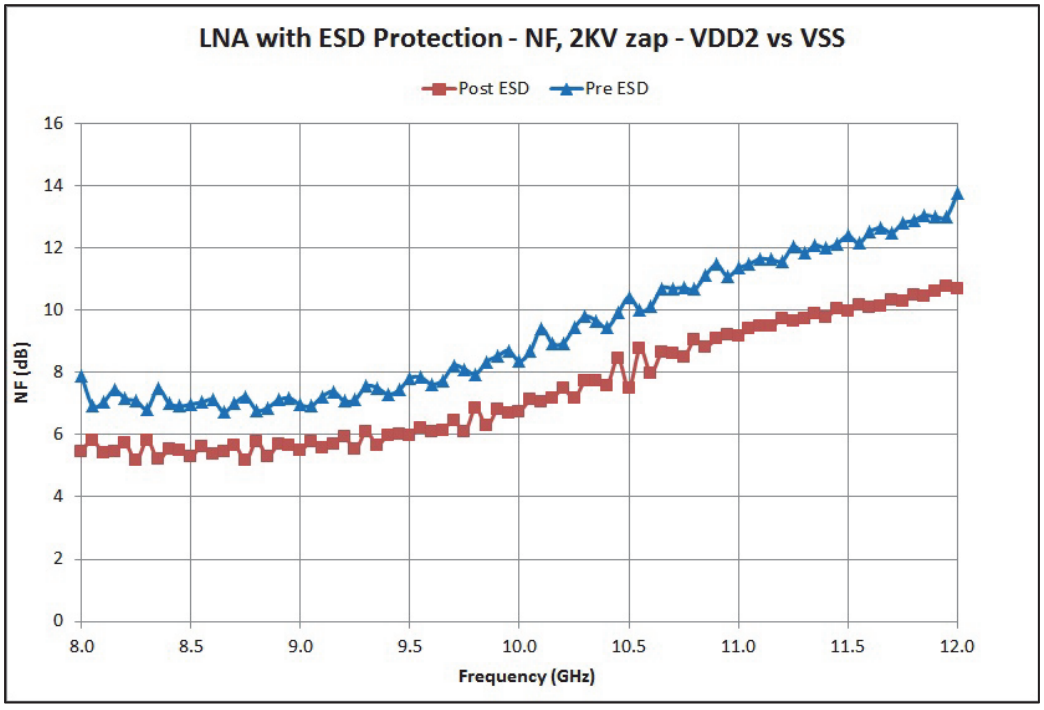


Figure 4.39 – LNA with ESD Protection – Noise Figure, 2 KV Zap – V_{DD2} vs. V_{SS}

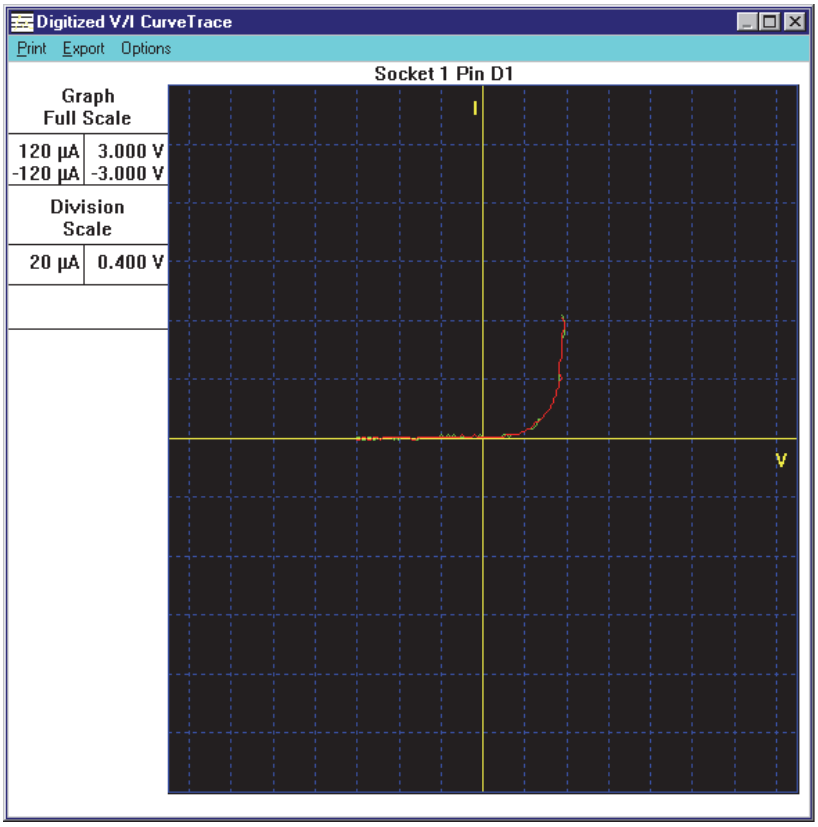


Figure 4.40 – LNA with ESD Protection – Curve Trace Pre and Post 2 KV Zap – V_{DD2} vs. V_{SS}

4.2.2.3 ESD HBM 4 KV Testing Curve Trace Results

Figure 4.41 to Figure 4.43 show the pre and post curve tracer for device 15 after the 4 KV zap. No leakage current was observed in the curve trace post ESD stress.

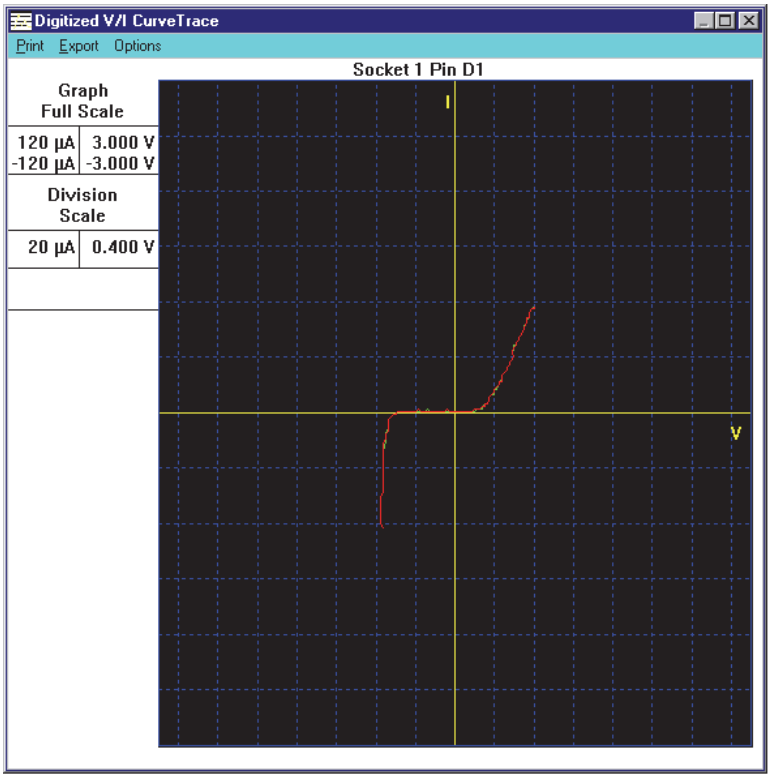


Figure 4.41 – LNA with ESD Protection – Curve Trace Pre and Post 4 KV Zap – RF_{in} vs. V_{SS}

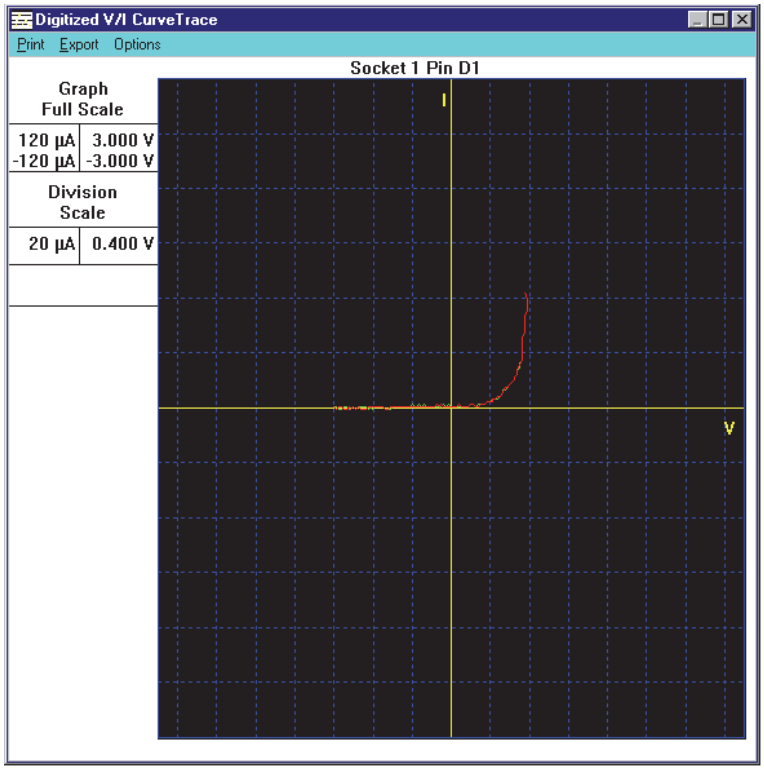


Figure 4.42 – LNA with ESD Protection – Curve Trace Pre and Post 4 KV Zap – RF_{in} vs. V_{DD2}

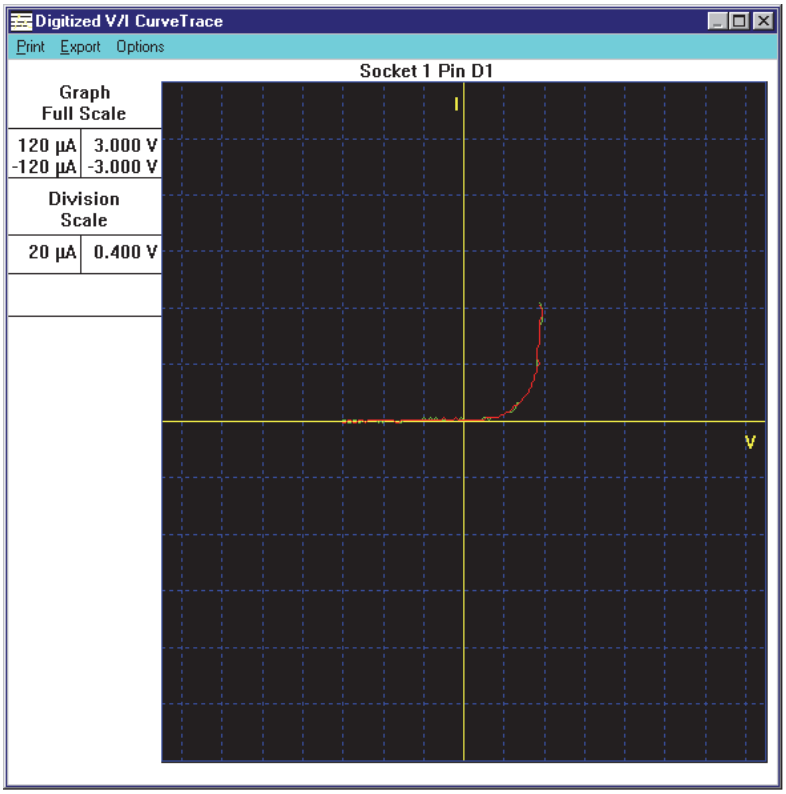


Figure 4.43 – LNA with ESD Protection – Curve Trace Pre and Post 4 KV Zap – V_{DD2} vs. V_{SS}

4.2.2.4 ESD HBM 8 KV Testing Results

Figure 4.44 to Figure 4.48 show the pre and post ESD stress S-parameters and noise figure measurement results for 8 KV ESD HBM stress for the RF_{in} vs. V_{DD2} pin combination for device number 15.

The curve trace results pre and post ESD stress are shown in Figure 4.49. A degradation of the ESD diodes between RF_{in} and V_{DD2} is observed, with the reduction of the on voltage from about 0.4 V to 0.1 V, which means that the diodes between them are damaged.

The post HBM testing results show a degradation of all S-parameters and noise figure measurements. It was also noticed that the current going through the LNA core

transistors has decreased from 10.68 mA to 3.1 mA, indicating that the bottom LNA cascode transistor has been damaged.

S11 shows a clear change in the input matching as the shape of the curve has changed, probably due to leakage of the upper diodes and damage on the bottom LNA cascode transistor. Another indication that the bottom LNA cascode transistor is damaged is the negative S21. S12 shows some degradation, but S22 and the noise figure similar to S21 shows a large degradation.

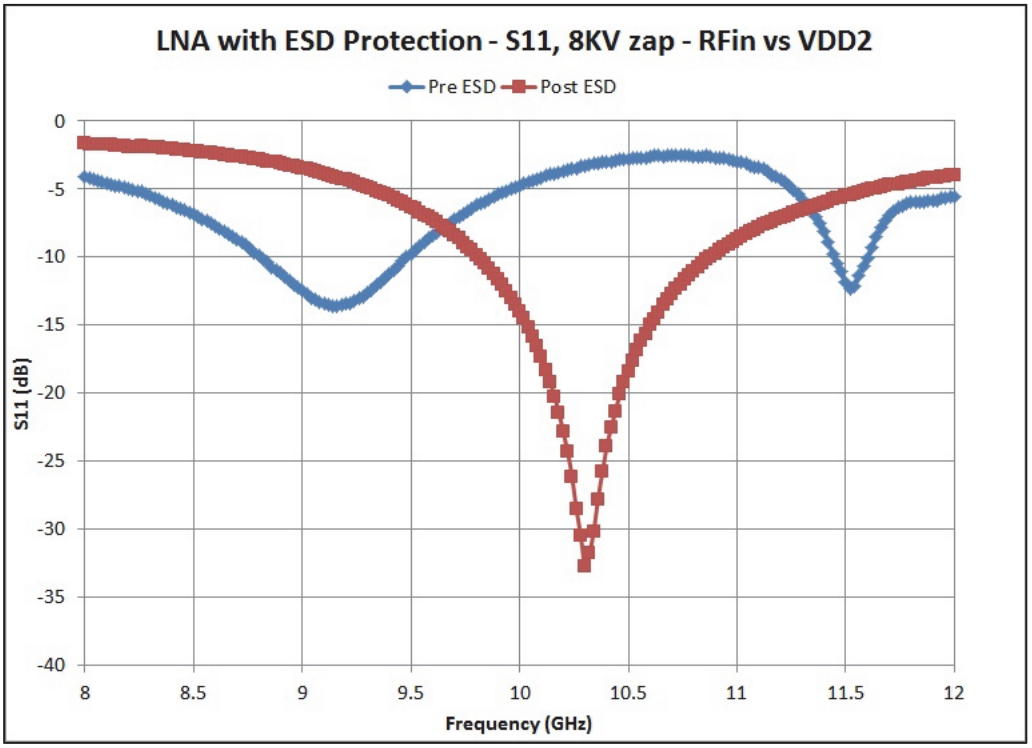


Figure 4.44 – LNA with ESD Protection – S11, 8 KV Zap – RF_{in} vs. V_{DD2}

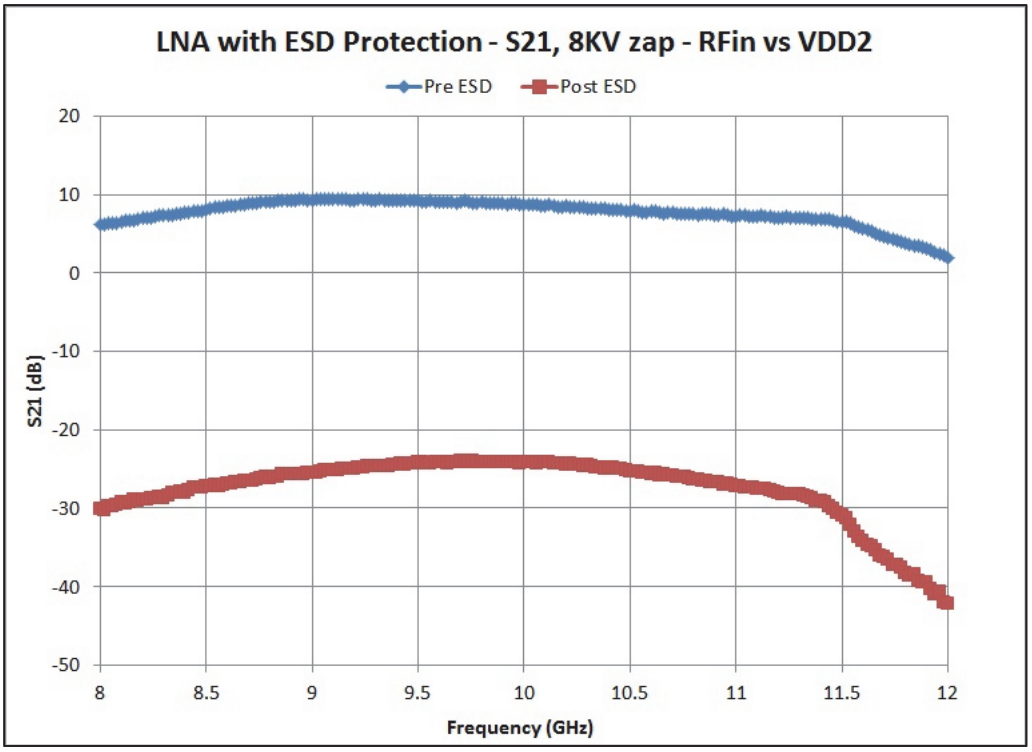


Figure 4.45 – LNA with ESD Protection – S21, 8 KV Zap – RF_{in} vs. V_{DD2}

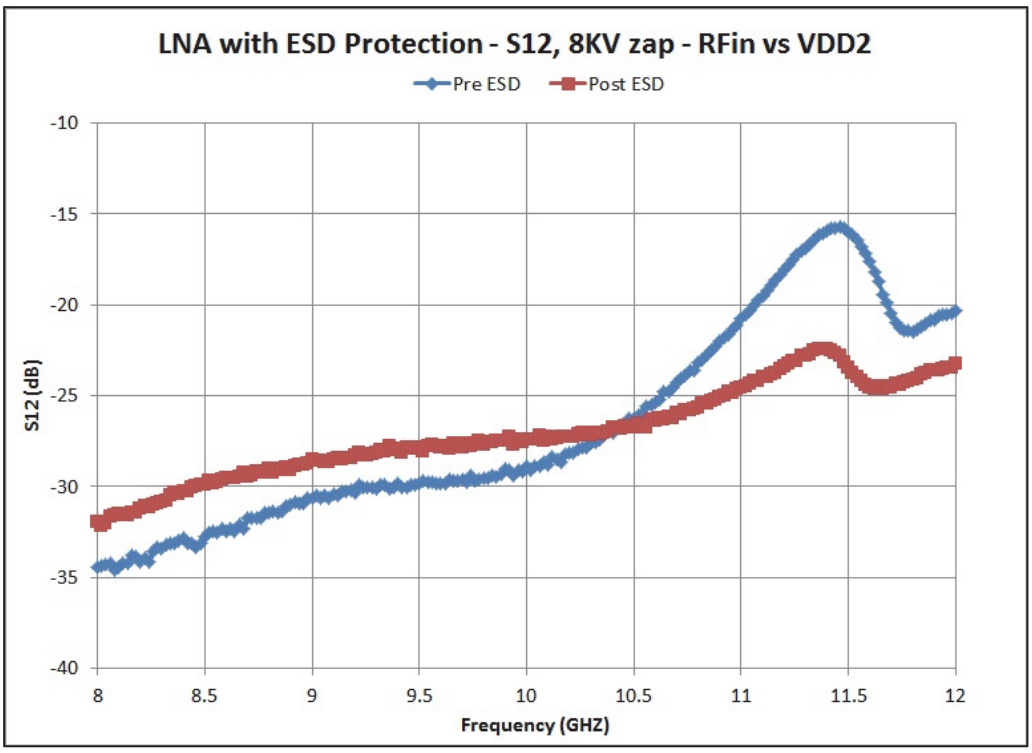


Figure 4.46 – LNA with ESD Protection – S12, 8 KV Zap – RF_{in} vs. V_{DD2}

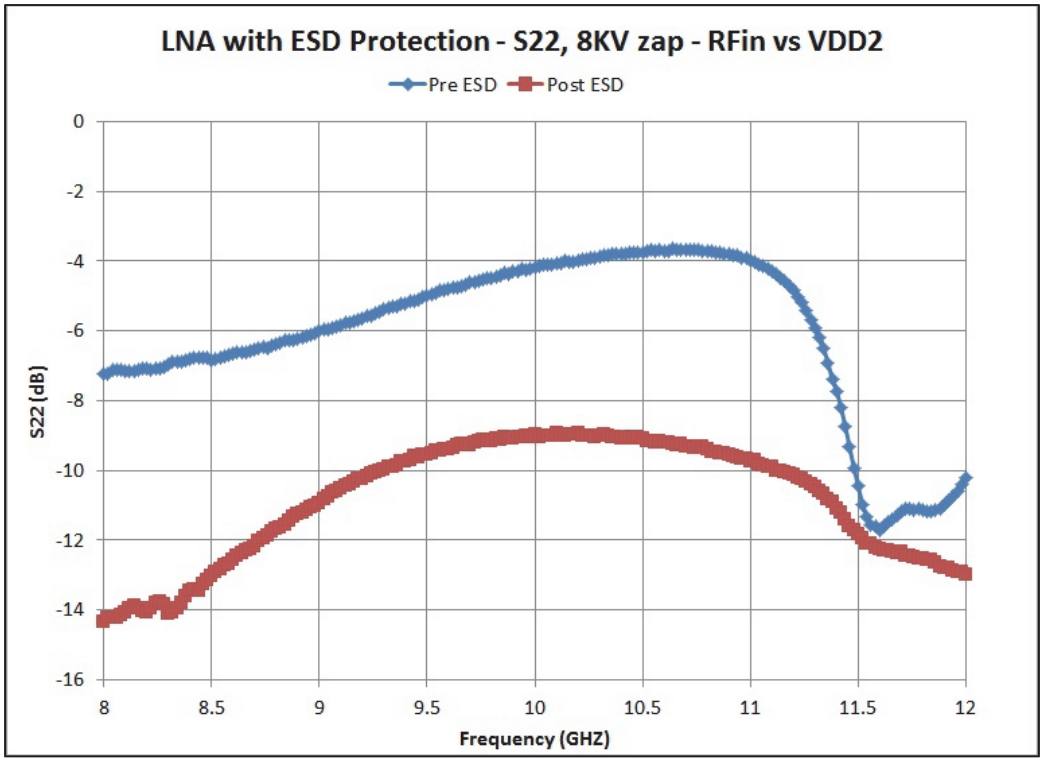


Figure 4.47 – LNA with ESD Protection – S22, 8 KV Zap – RF_{in} vs. V_{DD2}

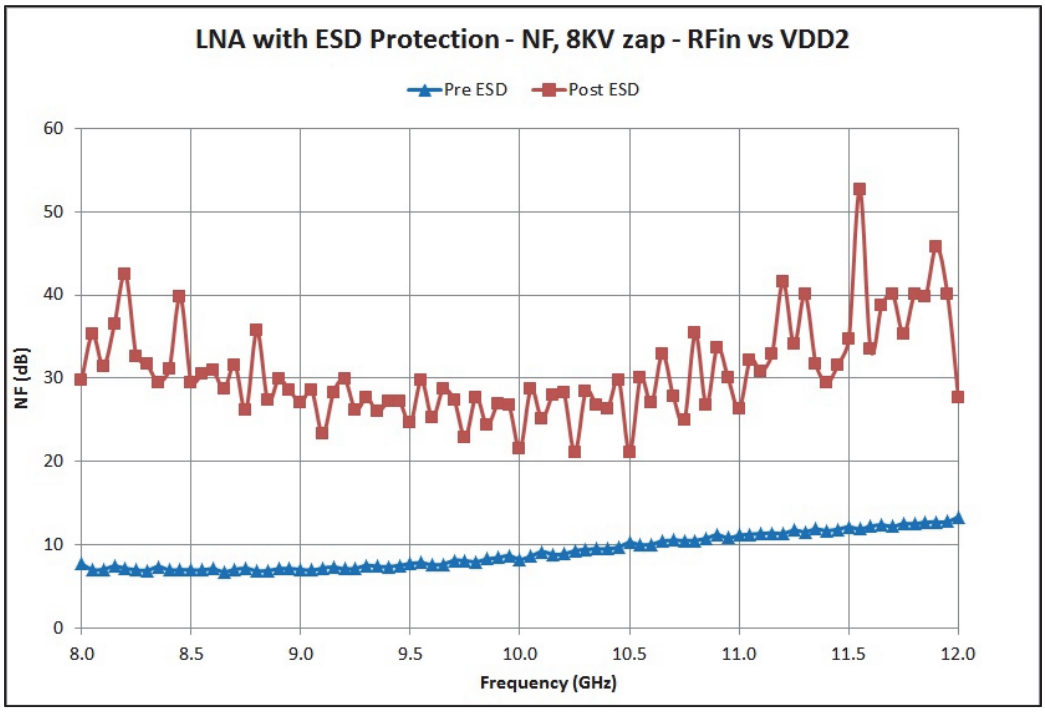


Figure 4.48 – LNA with ESD Protection – Noise Figure, 8KV Zap – RF_{in} vs. V_{DD2}

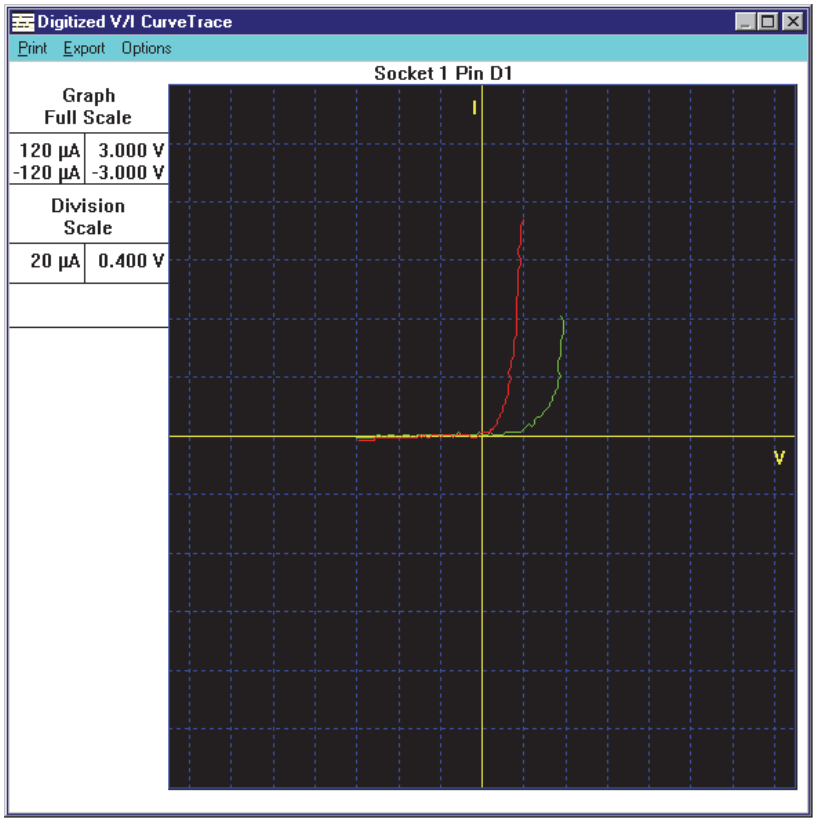


Figure 4.49 – LNA with ESD Protection – Curve Trace Pre and Post 8 KV Zap – RF_{in} vs. V_{DD2}

4.2.2.5 ESD HBM Test Plan and Results Summary

Table 4.3 and Table 4.4 show the ESD test plan and results for the LNA with ESD protection.

Table 4.3 – LNA with ESD Protection ESD HBM Test Plan and Results

Group	Voltage	Chip #	Curve Trace	Electrical Test
RF_{in} vs. V_{SS}	250	3	Pass	Pass
	250	4	Pass	Pass
	250	5	Pass	Pass
RF_{in} vs. V_{DD2}	250	6	Pass	Pass
	250	7	Pass	Pass
	250	8	Pass	Pass
V_{DD2} vs. V_{SS}	250	9	Pass	Pass
	250	10	Pass	Pass
	250	11	Pass	Pass
RF_{in} vs. V_{SS}	500	12	Pass	Pass
	500	13	Pass	Pass
	500	14	Pass	Pass
RF_{in} vs. V_{DD2}	500	16	Pass	Pass
	500	17	Pass	Pass
	500	18	Pass	Pass
V_{DD2} vs. V_{SS}	500	19	Pass	Pass
	500	20	Pass	Pass
	500	21	Pass	Pass
RF_{in} vs. V_{SS}	1000	22	Pass	Pass
	1000	23	Pass	Pass
	1000	24	Pass	Pass
RF_{in} vs. V_{DD2}	1000	25	Pass	Pass
	1000	26	Pass	Pass
	1000	27	Pass	Pass
V_{DD2} vs. V_{SS}	1000	28	Pass	Pass
	1000	29	Pass	Pass
	1000	30	Pass	Pass
RF_{in} vs. V_{SS}	2000	32	Pass	Pass
	2000	33	Pass	Pass
	2000	34	Pass	Pass
RF_{in} vs. V_{DD2}	2000	35	Pass	Pass
	2000	36	Pass	Pass
	2000	37	Pass	Pass
V_{DD2} vs. V_{SS}	2000	38	Pass	Pass
	2000	39	Pass	Pass
	2000	40	Pass	Pass

Table 4.4 – LNA with ESD Protection ESD HBM Test Plan and Results (Cont.)

Group	Voltage	Chip #	Curve Trace	Electrical Test
RF_{in} vs. V_{SS}	4000	15	pass	Not tested
RF_{in} vs. V_{DD2}	4000	15	Pass	Not tested
V_{DD2} vs. V_{SS}	4000	15	Pass	Not tested
RF_{in} vs. V_{DD2}	8000	15	Fail	Fail

4.3 Summary

In this section the pre and post ESD HBM stress measurement results of the LNAs with and without ESD protection were presented and discussed.

The LNA without ESD protection failed at 50 V, the lowest zapping voltage allowed by the testing equipment.

The LNA with ESD protection passed 2 KV based on both electrical and curve trace results, and passed 4 KV based only on curve trace results.

5 Chapter: **Conclusion and Future Work**

In this chapter the results of this study are summarized and a look into future work is provided.

5.1 Conclusion

The design and implementation of two narrow band LNA circuits operating at a center frequency of 10 GHz, one without ESD protection and another with ESD protection, have been completed. A comparison of the RF and ESD performance of both LNAs and the effect caused by the introduction of the ESD protection in the performance of the LNA has been studied.

An ESD HBM protection threshold of at least 2000 V was projected as the result of the ESD protection implementation, while minimizing the degradation of the LNA S-parameters and noise figure.

The simulation results show that the LNA with ESD protection has a similar performance to the LNA without the ESD protection. The most affected parameter is the noise figure with an increase of about 1 dB at the center frequency.

Unfortunately, the RF performance comparison of both LNAs measured results is not very straight forward due to several reasons. Firstly, the RC extracted data sets instead of the RLC were used to tune both LNAs, causing a downward frequency shift of the measured results. Secondly, the LNA with ESD protection RLC simulation results and the measured results show a second pole at a higher frequency, which was not observed in the RC simulated results; this is caused by of the resonance of the ESD

protection parasitic capacitance of the primary and secondary ESD protection, the gate inductor and parasitic inductance.

The ESD test results are very different for the two LNAs. The LNA without the ESD protection as expected has failed 50 V zap, the lowest ESD stress voltage of the ESD test equipment. The LNA with ESD protection has passed 2 KV based both on the electrical and curve trace results; however, based on the curve trace results of the device stressed at 4 KV, the LNA with ESD protection has an ESD threshold above 4 KV.

The results show that a properly tuned Pi ESD network is able to minimize the RF parameters degradation while providing an excellent ESD protection.

5.2 Contribution

In spite of the problems observed during the measured results, this thesis provides valuable contributions as follows:

- The PI ESD network is able to avoid S21 loss while adding a small noise figure degradation
- The PI ESD network provides very good ESD protection (>4 KV) to satisfy the industry standards
- At a frequency of 10 GHz and above, it is not enough to rely only upon the cadence simulations; electromagnetic simulation is a must to accurately determine the interconnect parasitics and the behavior of the circuit

5.3 Future Work

The PI network ESD protection has proven to provide an excellent ESD threshold voltage protection for the LNA. Further improvement of the ESD protection and reduction on the degradation of the RF parameters could be obtained with the following improvements.

Firstly, in order to overcome simulation problems encountered during the design and accurately predict the behavior of the manufactured LNA, it is highly recommended to use electromagnetic simulation to accurately determine the interconnect parasitics.

Secondly, based on more current TLP data from IBM [30], smaller ESD protection diodes could be chosen for the primary and secondary ESD protections, which would lead to smaller degradation of the RF parameters.

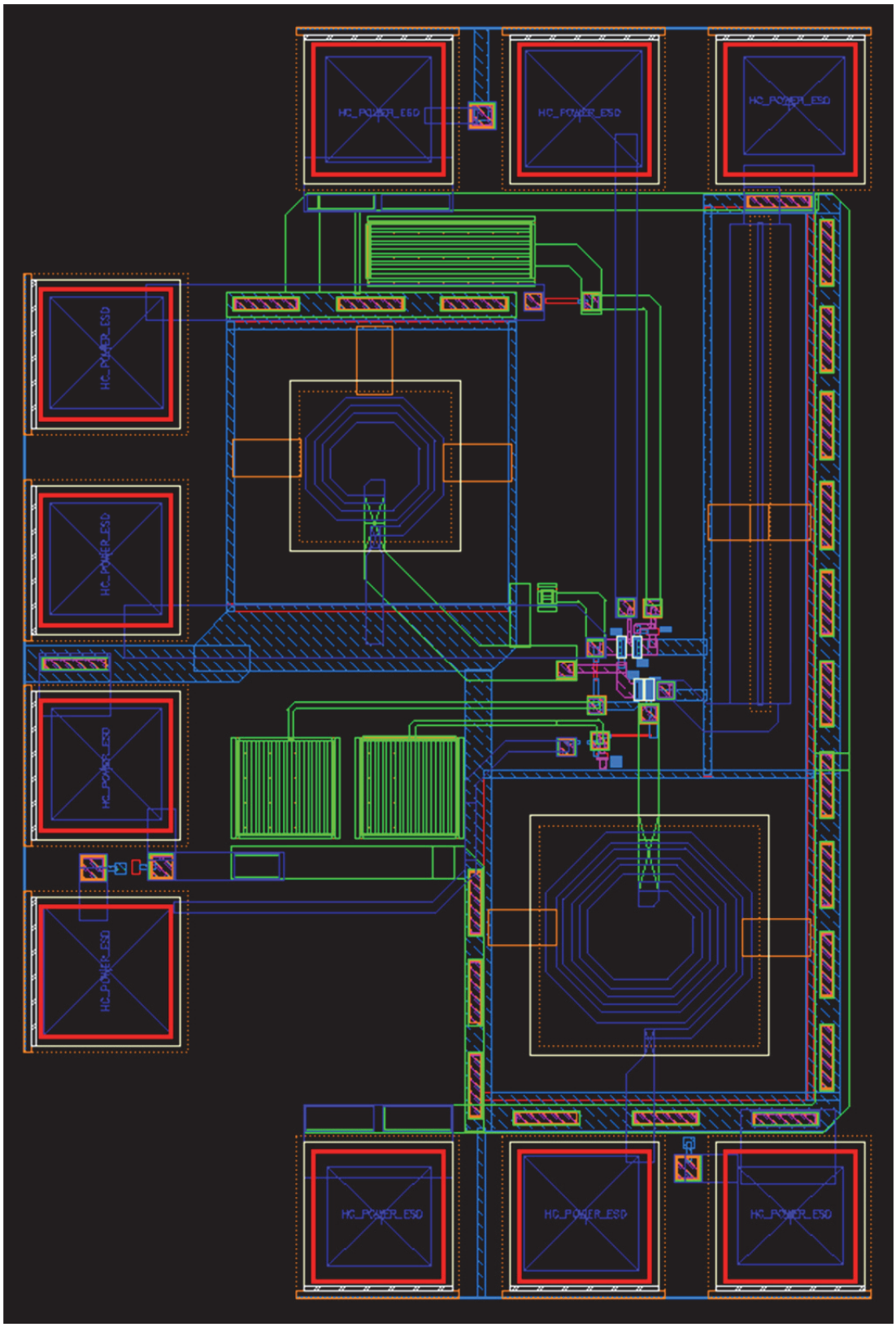
Thirdly, it is suggested to place the primary ESD protection closer to the input bond pad in order to reduce the interconnect parasitics

Appendices

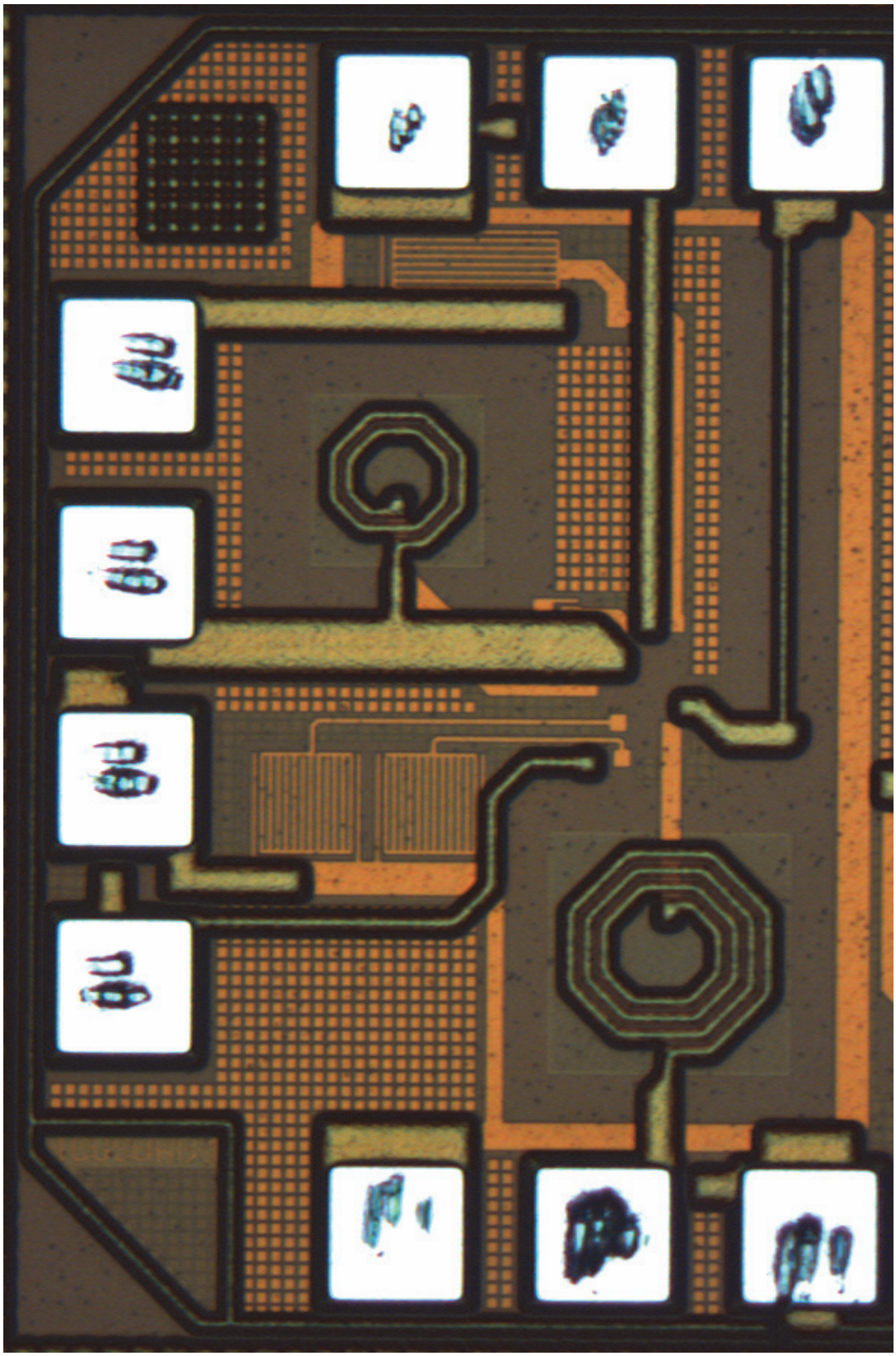
Appendix A – LNA Layout without ESD Protection

Images of the LNA layout are shown in this appendix. Sub-appendix A.1 shows the image of the LNA layout from cadence, and sub-appendix A.2 is an image of the actual LNA chip.

A.1 Sub-Appendix – LNA without ESD Protection Layout Image



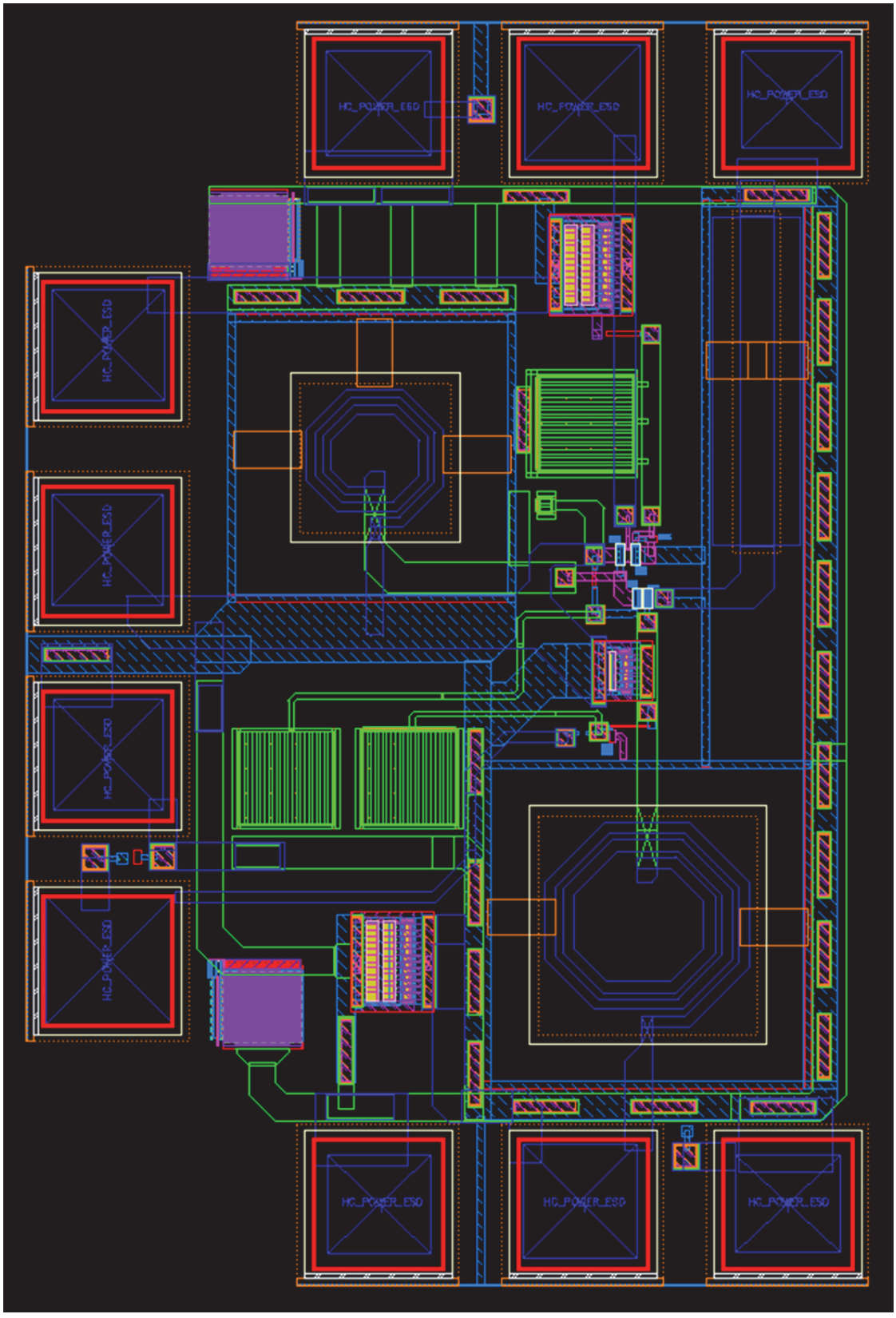
A.2 Sub-Appendix – LNA without ESD Protection Chip Image



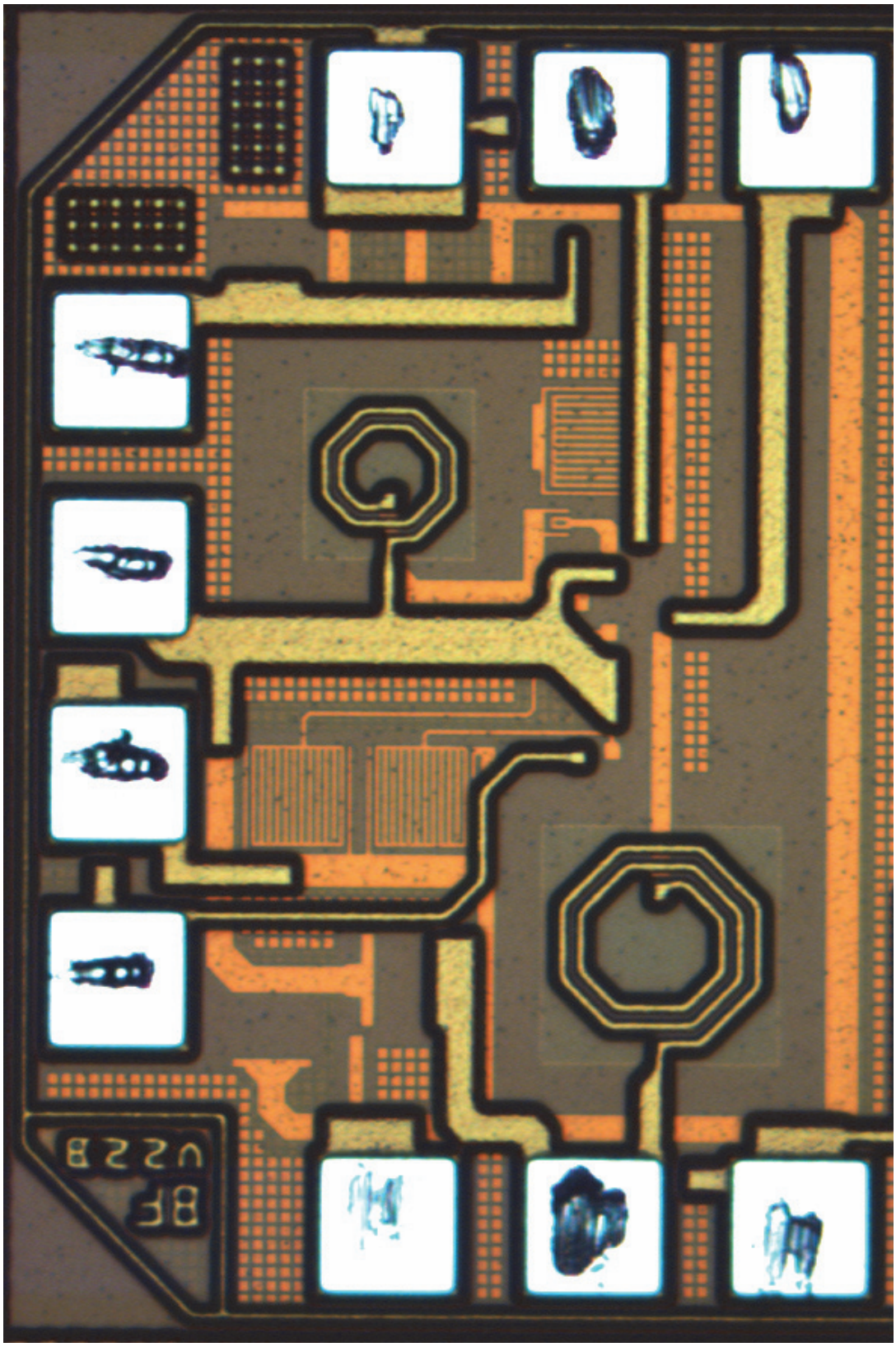
Appendix B – LNA Layout with ESD Protection

Images of the LNA layout with ESD protection are shown in this appendix. Sub-appendix B.1 shows the image of the LNA layout from cadence, and sub-appendix B.2 shows the image of the actual chip.

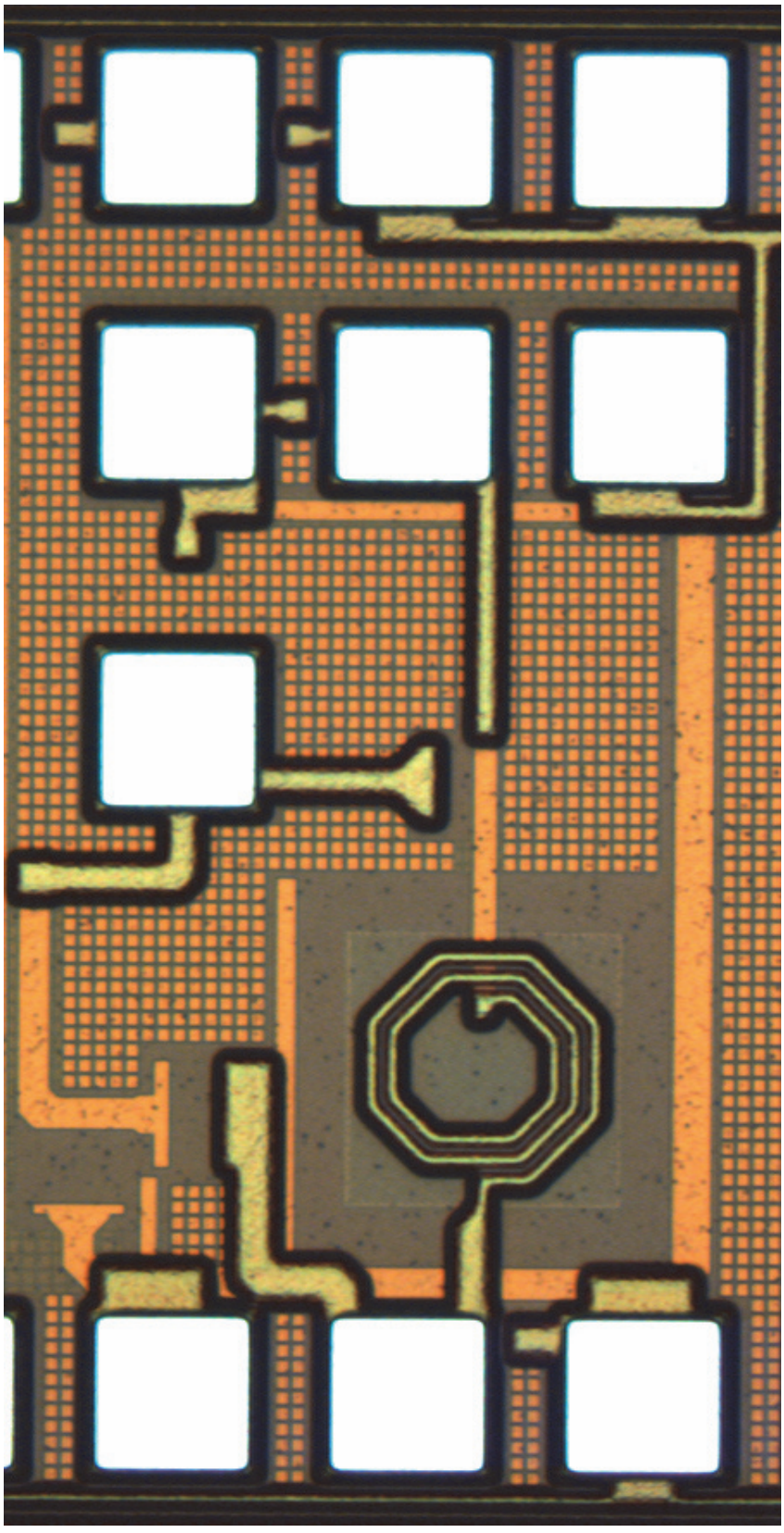
B.1 Sub-Appendix – LNA with ESD Protection Layout Image



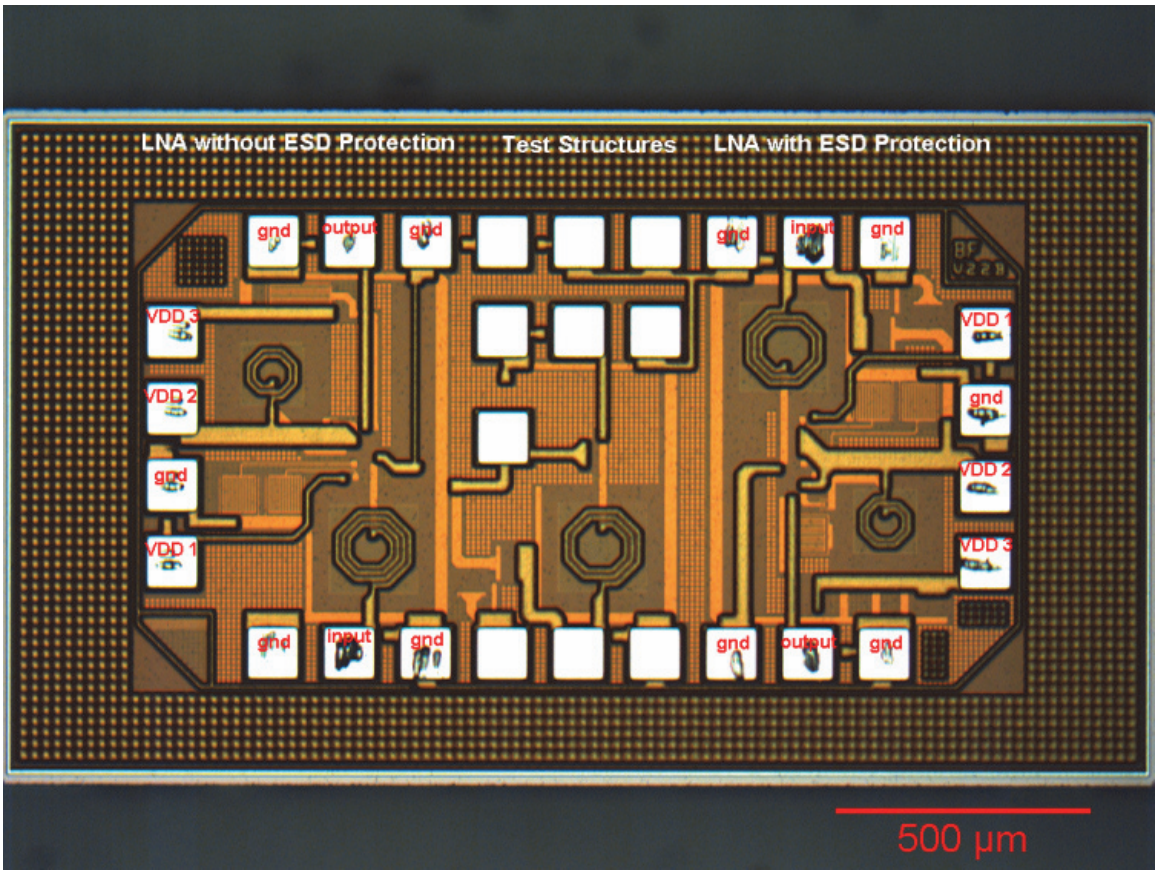
B.2 Sub-Appendix – LNA with ESD Protection Chip Image



Appendix C – De-Embedding Structures Chip Image



Appendix D – Whole Chip Image



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