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A MULTI-BAND VOLTAGE-CONTROLLED RING OSCILLATOR

By
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A thesis
presented to Carleton University
in fulfilment of the
thesis requirement for the degree of
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Abstract

This thesis presents the design of three-, five- and seven-stage voltage-controlled ring oscillators fabricated in 0.18- μm CMOS technology. The ring oscillators operate at 450MHz, 700MHz, 900MHz, 1800MHz, 1900MHz, and 2400MHz, have a narrow operating frequency range and exhibit near-constant amplitude of oscillation versus control voltage. A method for tuning curve linearization is proposed. A novel formula for calculating the frequency of oscillation based on the circuit parameters is derived. The VCO designs consume as low as $474\mu\text{W}$ from a 1.8V supply, while achieving a figure of merit (FOM) as low as -163.58dB.

This thesis presents a low-power three-stage multi-band voltage-controlled ring oscillator fabricated in a mixed-signal 0.18- μm CMOS technology as well. By using two-input voltage signals, featuring an abrupt and a fine control, six-band (450MHz, 700MHz, 900MHz, 1800MHz, 1900MHz, and 2400MHz) operation was realized in a single VCO. The VCO consumes from $275\mu\text{W}$ to $647\mu\text{W}$ from a 1-V supply. The VCO occupies $2461\mu\text{m}^2$ chip area.

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*to Simka,
my wonderful wife*

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List of Abbreviations

A/D	Analog to Digital
B	Bulk
CDR	Clock and Data Recovery
CLM	Channel Length Modulation
CMOS	Complementary Metal Oxide Semiconductor
C_j	Zero-bias junction capacitance
C_{BD}	Bulk to Drain Capacitance
C_{BS}	Bulk to Source Capacitance
C_{dep}	Depletion capacitance
C_{GBO}	Gate to Bulk Overlap Capacitor
C_{GB}	Gate to Bulk Capacitor
C_{GDO}	Gate to Drain Overlap Capacitor
C_{GD}	Gate to Drain Capacitor
C_{GSO}	Gate to Source Overlap Capacitor
C_{GS}	Gate to Source Capacitor
C_{jsw}	Zero-bias sidewall capacitance
C_{ox}	Oxide Capacitor
C_{var}	Varactor's capacitance
D/A	Digital to Analog
DIBL	Drain Induced Barrier Lowering
E_c	Critical electric field in the silicon

F_{osc}	Oscillation frequency
FC	Forward-bias non-ideal junction capacitance coefficient
FOM	Figure of Merit
FS	Frequency synthesis
G	Gate
Gbps	Giga-bits per second
G_m	Large signal transconductance
G_{ext}	Extension of the gate due to the design rules
K_{CGD}	Channel coefficient
K_{VCO}	VCO gain
ICO	Current-Controlled Oscillator
k	The Boltzmann's constant
kbps	Kilo-bits per second
L_{eff}	Effective Length
LD	Lateral Diffusion
m_j	Bulk junction grading coefficient
m_{jsw}	Bulk sidewall grading coefficient
MATS	Maury Automated Tuner System
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
N	Number of stages
N_D	Donor concentration
N_{SUB}	Substrate concentration
PCB	Printed Circuit Board
PLL	Phase-locked loop
pMOS	p-channel Metal Oxide Semiconductor
PN	Phase Noise

q	Electron charge
RFIC	Radio Frequency Integrated Circuit
rms	Root mean square
STI	Shallow Trench Isolation
t_{ox}	Gate Oxide Thickness
V_{BG}	Bulk to Gate voltage
V_{ctrl}	Control voltage
V_{DS}	Drain to Source Voltage
V_{FB}	Flatband voltage
V_{GS}	Gate to Source Voltage
V_{pp}	Peak to peak voltage
V_{TH}	Threshold Voltage
VCO	Voltage-Controlled Oscillator
VDD	Supply voltage
VNA	Vector Network Analyzer
W_{eff}	Effective Width
WLAN	Wireless Local Area Network
x_d	Depletion layer width
ϕ_j	Built-in junction potential
ϕ_{jsw}	Built-in sidewall junction potential
ϵ_{ox}	Dielectric Constant of the Silicon Dioxide
ϵ_{si}	Dielectric Constant of the Silicon

Chapter 1

Introduction

1.1 Thesis Objective

The phase-locked loop (PLL) is commonly found component in high-speed systems and can be used for frequency synthesis (FS), clock and data recovery (CDR), and synchronization. The voltage-controlled oscillator (VCO) directly provides the output to these applications and thus it is the most critical element of the PLL [1].

The spectral purity of the VCO output signal is the key factor in determining the VCO quality. Different applications require different VCO solutions. Some such as Wireless Local Area Network applications (WLAN) for ISM frequency band, 2.4-2.5GHz, have very stringent requirements for Radio Frequency Integrated Circuit (RFIC) VCOs. With their excellent phase noise performance, LC oscillators are the only choice for these applications. However, there are applications with specifications focused on low power consumption, low cost, low data rate (a few kbps), full integrability and small chip area. For example telemetry applications such as power control, alarm/security, and toys. Although LC oscillators achieve excellent performance (phase noise and frequency stability), ring oscillators benefit from transistor

scaling, achieving smaller layout areas as the feature size decreases. LC-based oscillators are largely limited in size by the inductors which do not scale dramatically with decreasing MOSFET feature size [2].

The objective of the research that is reported in this thesis is to design a fully integrated ring oscillator that occupies a small chip area and consumes a small amount of power. The intent was to implement ring oscillators that compare favorably with ring oscillators that are described in the literature.

1.2 Thesis Organization

Excluding the introduction, this thesis is organized into seven chapters.

Chapter 2 introduces the reader to the design specification of voltage-controlled oscillators and gives examples of a few research works in the field of ring oscillators.

Chapter 3 presents the proposed delay stage and discusses a model for the delay stage.

Chapter 4 provides a theoretical analysis of the proposed delay stage. Assuming purely differential signals, the transfer function of the delay stage is derived in the frequency domain.

Chapter 5 provides the theoretical analysis of a ring oscillator with N-stages. A novel formula for calculating the frequency of oscillation is derived based on the circuit parameters. The expression for the phase noise is derived as well. A technique for linearizing the frequency characteristic is proposed.

Chapter 6 discusses the simulated and measured results for the varactors used in this thesis and one randomly selected ring oscillator. The results for all other ring

oscillators including the layout and chip photos are given in Appendixes B to I.

Chapter 7 shows the design of a multi-band fully integrated ring oscillator. A single oscillator with a small chip area can cover frequencies in the range from 100MHz to 5GHz. Theoretical analysis regarding the frequency of oscillation and phase noise are provided.

Chapter 8 concludes the thesis and outlines some of the thesis contributions and future work.

Chapter 2

Background

2.1 Voltage Controlled Oscillator

Modulation and demodulation operations are often used to exploit better propagation characteristics of communication channels. An accurate frequency reference signal is normally needed for performing these operations.

An attractive technique for generating multiple carriers at RF frequencies is to use a less accurate RF oscillator whose frequency can be controlled and locked to an accurate low frequency reference. This frequency synthesis technique is based on a phase-locked-loop (PLL).

There are two prevalent types of controlled oscillators, called voltage-controlled oscillator (VCO) and current-controlled oscillator (ICO). The VCO uses a voltage signal to control the oscillator's frequency. Alternatively, the ICO uses the current signal to control the oscillator's frequency. In this thesis, the voltage-controlled oscillator is considered.

2.2 VCO Specifications

One of the most important characteristics of an oscillator is its spectral purity. It defines the degree to which the output spectrum of the oscillator is a pure tone. Noise sources such as thermal, flicker, shot, supply, and substrate noise affect the amplitude and frequency of oscillation and, as a result, the output spectrum of the oscillator is not a pure tone but has noise sidebands. In frequency domain the spectral purity is specified as phase noise, while in the time domain it is specified as jitter.

Center frequency, tuning range and tuning sensitivity are other characteristics of the VCO. The center frequency of the VCO is defined as the output frequency of the VCO when its control signal is at its center value. The tuning range is defined as the range of the output frequencies over the full range of the control signal. The tuning sensitivity is defined as a change in output frequency over the unit change in control voltage. It is also known as VCO gain (K_{VCO}).

Power consumption is also a very important characteristic. Both the DC power consumption and the dynamic power consumption of the VCO are of interest. Generally, it is desirable to reduce the power consumption to the extent possible while maintaining the required phase noise performance.

“Supply pulling” refers to the sensitivity of the output frequency to changes in the power supply voltage. Supply pulling is of concern in low voltage applications and in applications where the supply voltage can include transients, for example, during frequency lock-in.

The output power is defined as the power that the oscillator delivers to a specified

load.

2.3 VCO Classification

There are three prevalent types of voltage-controlled oscillators: tuned, relaxation, and ring oscillators. To set the frequency, tuned oscillators contain a passive resonator such as an LC tank. This type of oscillator is known as LC oscillator, and it has excellent frequency stability and spectral purity. Its phase noise performance primarily depends on the quality factor of the inductor. However, the size and the poor quality factor of the integrated passive inductor in standard CMOS technology makes the integration of the LC oscillators on chip harder compared with the integration for the other two VCO classification types [3]. Relaxation and ring oscillators can be easily integrated on a monolithic integrated circuit and occupy less chip area in comparison to LC oscillators. This improves both the manufacturing yield and cost [4]. These types of VCOs are more sensitive to changes in the supply voltage and have poorer spectral purity when compared with LC oscillators.

2.4 Ring Oscillator Publications

Figure 2.1 shows the figure of merit (FOM) of a LC oscillators (shown in [5], [6], [7], [8], [9], [10], [11], and [12]), and ring oscillators (RO) (shown in [13], [4], [14], [15], [16], and [3]). The FOM was determined using the equation [17],

$$FOM = PN(\omega_0, \Delta\omega) - 10 \log \left(\frac{[mW]}{P_{VCO}} \left(\frac{\omega_0}{\Delta\omega} \right)^2 \right) \quad (2.4.1)$$

where $PN(\omega_0, \Delta\omega)$ is the single-side-band noise at the offset frequency $\Delta\omega$ from the carrier frequency ω_0 . P_{VCO} denotes the power consumption of the VCO in mW.

Figure 2.1: FOM of LC and ring oscillators from the literature

Figures 2.2-2.7 show examples of ring oscillators found in the reviewed literature. Their selection is highlighted here because the ring oscillator's performances are explicitly shown. The cited work give an idea of the circuit topology that could be used for designing a ring oscillator.

Table 2.1 summarizes the performances of the cited works. Note that, N refers to the number of stages, VDD is the supply voltage, I_{tail} is the current consumption of one stage, P is the power dissipation, f refers to frequency, K_{vco} is the VCO gain, PN refers to the phase noise, offset refers to the frequency offset from the carrier, FOM is the figure of merit, area refers to the VCO core area, and R is the reference.

The reviewed literature [13] analyzes the effect of the number of stages, power dissipation, frequency of oscillation, and short channel effects on the jitter and phase noise of ring oscillators. It presents three different cell topologies. Figure 2.2(a) shows

Table 2.1: Performances of published Ring Oscillators

N	V_{DD} [V]	I_{tail} [mA]	P [mW]	f [MHz]	K_{vco} [$\frac{MHz}{V}$]	PN [$\frac{dBc}{Hz}$]	offset [MHz]	FOM [dB]	area [μm^2]	R
12	2.5	0.33	10.0	447	n/a	-109.5	1.0	-152.5	n/a	[13]
8	2.5	0.50	10.0	731	n/a	-106.2	1.0	-153.5	n/a	[13]
2	2.5	3.1	15.4	900	630	-105.5	0.6	-157.1	12750	[4]
3	2.0	3.1	19.0	913	487	-116.5	0.6	-167.4	6750	[14]
2	3.3	12.0	79.2	973	n/a	-117.0	1.0	-157.1	n/a	[15]
3	3.3	0.30	3.0	1250	145	-100.0	1.0	-157.2	n/a	[16]
4	3.0	2.50	30.0	900	300	-117.0	0.6	-165.8	99200	[3]

a CMOS inverter used for designing inverter-chain ring oscillators with no frequency tuning mechanism. Fabricated in a $0.25\mu m$ CMOS process, the ring oscillator with nineteen stages operates at 1.33GHz and consumes 10mA current from a 2.5V supply. The measured phase noise is -111.5dBc/Hz at 1MHz frequency offset. Figure 2.2(b) shows a delay cell structure for current-starved ring oscillators with no frequency tuning mechanism. The node V_{bias_N} is kept at VDD, while node V_{bias_P} is at 0V. The measured frequency of oscillation of the ring oscillator with three-stages fabricated in a $0.25\mu m$ CMOS process is 751MHz, measured current is 2.34mA from a 2.5V supply, and the measured phase noise is -114dBc/Hz at 1MHz frequency offset. Figure 2.2(c) shows the delay cell topology for differential ring oscillators with frequency tuning mechanism. Table 2.1 shows the measured results for two ring oscillators designed with this delay stage.

Figure 2.3 shows the circuit implementation of the delay cell and ring oscillator as shown in [4]. The reviewed literature presents a 900MHz two-stage voltage-controlled ring oscillator implemented in a $0.5\mu m$ CMOS technology. Table 2.1 shows the measured results.

Figure 2.4 shows the ring oscillator shown in [14]. The circuit is designed in a $0.18\mu\text{m}$ CMOS process and operates on a 2V supply. Table 2.1 shows the measured results.

Figure 2.5 shows the ring oscillator shown in [15]. The reviewed literature presents a two-stage 3.3V ring VCO in a $0.35\mu\text{m}$ CMOS technology with differential controll and quadrature outputs. Table 2.1 shows the measured results.

Figure 2.6 shows the delay stage topology and ring oscillator shown in [16]. The reviewed literature presents a four stage quadrature output differential ring oscillator implemented in a $0.5\mu\text{m}$ CMOS technology. Table 2.1 shows the measured results.

Figure 2.7 shows the delay cell and ring oscillator shown in [3]. The reviewed literature presents a low-noise, 900MHz ring VCO fabricated in a $0.6\mu\text{m}$ CMOS technology. Table 2.1 shows the measured results.

A study of phase noise in 2-GHz ring and 900-MHz relaxation CMOS oscillators is shown in [18]. The reviewed literature presents a method for deriving the phase noise in ring oscillators. This method was used in Section 5.2.4 of Chapter 5 when the ring oscillator with N-stages, proposed with this thesis, was analyzed regarding the phase noise.

Regarding the phase noise, [3] accomplished a phase noise of -117dBc/Hz at 600kHz frequency offset. The ring oscillators consumes 30mW power from a 3V supply and occupies $99200\mu\text{m}^2$ chip area. Regarding the figure of merit, [14] has the best performances compared with the other cited works in Table 2.1. The phase noise of this work is -116.5dBc/Hz at 600kHz frequency offset, which is almost the same as the cited work with -117dBc/Hz . However, the ring oscillator consumes 19mW power

Figure 2.2: Proposed delay stages for (a) inverter-chain, (b) current-starved inverter-chain and (c) differential ring oscillators [13]

Figure 2.3: Proposed (a) delay cell and (b) ring oscillator as shown in [4]

Figure 2.4: Proposed ring oscillator shown in [14]

Figure 2.5: Proposed ring oscillator shown in [15]

Figure 2.6: Proposed (a) delay stage, (b) ring oscillator shown in [16]

Figure 2.7: Proposed (a) delay stage, (b) ring oscillator shown in [3]

from a 2V supply and occupies $6750\mu\text{m}^2$ chip area.

2.5 Summary

This chapter discussed why voltage-controlled oscillators are important at RF frequencies, what the typical VCO specifications are and the type of VCOs most prevalent in literature. The FOM of the LC and ring oscillators from reviewed literature were shown. Six different topologies for ring oscillators were listed.

Chapter 3

MOSFET and Varactor Modeling

3.1 Proposed Delay Stage

Figure 3.1 shows the proposed delay stage that was used in this thesis work. The delay stage is a differential amplifier with two n-channel MOS transistors, one resistor placed at the source of the differential pair instead of a current source, and two drain resistors used as loads. Two varactors connected between the differential outputs are also included. Their design as well as their modeling and characteristics are discussed in Section 3.3 of this chapter. The modeling of the n-channel MOS transistors is discussed in Section 3.2 of this chapter as well. Theoretical differential mode analysis of one delay stage is given in Chapter 4.

3.2 Model for the MOS transistor

To analyze the delay stages presented in Figure 3.1, a model for the MOS transistors is needed. It should adequately describe the behavior of the MOSFET for the conditions expected during the operation of the circuit.

For the purpose of this thesis, emphasis is put on the simplest model that is appropriate for hand calculations. Figure 3.2 shows a model for an n-channel MOS

Figure 3.1: Proposed delay stages for configuring voltage-controlled ring oscillator. (a) The varactor has one finger, (b) the varactor has three fingers.

transistor [19]. Note that, the n-channel MOSFET transistor is denoted as M_{ideal} . Figure 3.3 shows the small signal model for this transistor. The model in Figure 3.2 includes pn junctions between the source and substrate, drain and substrate as well as source, and drain resistors, gate-to-drain, gate-to-source, gate-to-bulk, bulk-to-drain, and bulk-to-source capacitor. The diodes model the leakage currents, diode capacitances, and nonlinearities. The leakage currents are expressed as [19],

$$i_{BD} = I_S [\exp(\frac{v_{BD}}{kT/q}) - 1] \quad (3.2.1)$$

$$i_{BS} = I_S [\exp(\frac{v_{BS}}{kT/q}) - 1] \quad (3.2.2)$$

where

- I_S is the reverse saturation current of the pn junction,
- $q = 1.6 \times 10^{-19}$ [C] is the charge of an electron,

Figure 3.2: Model for the n-channel MOS transistor [19].

Figure 3.3: Small signal model for the n-channel transistor.

- $k = 1.38 \times 10^{-23} [\frac{J}{K}]$ is Boltzmann's constant, and
- T is temperature in Kelvin.

The resistors r_S , and r_D represent the ohmic resistance of the source, and drain, respectively. For a CMOS $0.18\mu\text{m}$ salicide process, these resistances can be ignored [19]. The gate, bulk, and drain-to-source resistance and drain-to-source capacitance are ignored as well assuming that their values are small and have no significant effect on the circuit performance for the application that is used in this thesis.

Figure 3.2 shows a model for the MOSFET transistor that account for the charge-storage effects in a MOS transistor. The charge-storage effects are represented by three non-linear capacitances C_{GB} , C_{GD} , and C_{GS} [20]. According to the operation region of the device, below are approximate expressions for these capacitances.

Cut-off region: $V_{GS} < V_{TH}$

$$C_{GB} = C_{ox}(W_{eff})(L_{eff}) + 2C_{GBO}L_{eff} \quad (3.2.3)$$

$$C_{GS} = C_{ox}(LD)(W_{eff}) = C_{GSO}(W_{eff}) \quad (3.2.4)$$

$$C_{GD} = C_{ox}(LD)(W_{eff}) = C_{GDO}(W_{eff}) \quad (3.2.5)$$

Saturation region: $V_{TH} \leq V_{GS} \leq V_{TH} + V_{DS}$

$$C_{GB} = 2C_{GBO}L_{eff} \quad (3.2.6)$$

$$C_{GS} = \frac{2}{3}C_{ox}(W_{eff})(L_{eff}) + C_{GSO}(W_{eff}) \quad (3.2.7)$$

$$C_{GD} = K_{C_{GD}} \cdot C_{ox}(W_{eff})(L_{eff}) + C_{GDO}(W_{eff}) \quad (3.2.8)$$

Linear region: $V_{GS} > V_{TH} + V_{DS}$

$$C_{GB} = 2C_{GBO}L_{eff} \quad (3.2.9)$$

$$C_{GS} = \frac{1}{2}C_{ox}(W_{eff})(L_{eff}) + C_{GSO}(W_{eff}) \quad (3.2.10)$$

$$C_{GD} = \frac{1}{2}C_{ox}(W_{eff})(L_{eff}) + C_{GDO}(W_{eff}) \quad (3.2.11)$$

where

- W_{eff} is the effective channel width,
- L is the channel length,

- LD is the amount that the gate overlaps the source and drain
- $L_{eff} = L - 2LD$ is the effective channel length,
- $C_{GDO} = C_{GSO} = LD C_{ox} [\frac{F}{m}]$ represent the overlap capacitances between the gate-source and gate-drain, respectively. For MOS transistors constructed with a lightly-doped-drain, these overlap capacitances can be highly bias dependent and therefore non-linear. In the case when the MOS transistors are constructed with a heavily-doped-drain, the overlap capacitances can be modeled as linear parallel-plate capacitors [20],
- $C_{GBO} = G_{ext} C_{ox} [\frac{F}{m}]$ represents the overlap capacitances between the gate-bulk. Capacitance due to rules that require the gate be extended (G_{ext}) beyond the channel by some amount. This capacitance is not bias dependent [21],
- $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} [\frac{F}{m^2}]$ is the thin-oxide field-capacitance per unit area under the gate region,
- $\epsilon_{ox} = 34.5306 \times 10^{-14} [\frac{F}{m}]$ is the dielectric constant of silicon dioxide ,
- t_{ox} is gate oxide thickness,
- K_{CGD} proposed constant, see explanation below.

Equations (3.2.3) - (3.2.11) show that the gate capacitances depend on the transistor's geometry. In (3.2.8) a new constant, noted as K_{CGD} , was proposed. This constant tells how much is the contribution from the channel to the gate-to-drain capacitance. For the transistors with a long channel, this constant is modeled to be equal to

zero [20]. However, when the derived curve for frequency of oscillation for the ring oscillators considered with this thesis work, discussed in Section 5.2.2, was compared to the simulated tuning curve then a better deviations between the two curves was accomplished if this constant was assumed not to be equal to zero. Considering ring oscillators designed with three-, five-, and seven-stages and center frequencies at 450MHz, 700MHz, 900MHz, 1800MHz, 1900MHz, and 2400MHz it was found that, when the MOSFET transistor was in saturation, the gate-to-drain capacitance can have values in the range from 4[fF] to 4.8[fF]. To simplify the hand calculations it was assumed that the gate-to-drain capacitance has an average value of 4.4[fF]. That means that the constant K_{CGD} noted in percentage will be 28.64%. With other words, the channel gives 28.64% contribution to the gate-to-drain capacitance.

Table 3.1 shows the values of the calculated gate capacitances depending of the operation region of an n-channel MOS transistor with a length = $0.18\mu\text{m}$, width = $2.5\mu\text{m}$, number of fingers = 4, $G_{ext} = 0.25\mu\text{m}$. These values are taken from the layout of the MOSFET transistors given in Appendix I. Fairly arbitrary, it was assumed that: $LD = 3.6\text{nm}$, $L_{eff} = 0.173\mu\text{m}$, $W_{eff} = 2.4\mu\text{m}$, and $t_{ox} = 4\text{nm}$.

Table 3.1: Gate Capacitance: n-channel MOSFET

Operation Region	$C_{GS}[F]$	$C_{GD}[F]$	$C_{GB}[F]$
Cut-off	298.34×10^{-18}	298.34×10^{-18}	17.30×10^{-15}
Saturation	9.85×10^{-15}	4.40×10^{-15}	2.98×10^{-15}
Linear	7.46×10^{-15}	7.46×10^{-15}	2.98×10^{-15}

The capacitance of the diffusion regions of the source and drain is shown in Figure 3.2 as well. This type of capacitance includes capacitors C_{BD} and C_{BS} which are a

Figure 3.4: Illustration of the bottom and sidewall components of the bulk junction capacitors [19].

function of the voltage across the pn junction. The total junction capacitance can be calculated from the sum of the bottom and sidewall capacitance. Figure 3.4 shows the bottom and sidewall components of the bulk junction capacitors. When $v_{BS}, v_{BD} \leq (FC)(\phi_j)$ the expressions for these capacitances are,

$$C_{BS} = \frac{C_j A_S}{(1 - \frac{v_{BS}}{\phi_j})^{m_j}} + \frac{C_{jsw} P_S}{(1 - \frac{v_{BS}}{\phi_{jsw}})^{m_{jsw}}} \quad (3.2.12)$$

$$C_{BD} = \frac{C_j A_D}{(1 - \frac{v_{BD}}{\phi_j})^{m_j}} + \frac{C_{jsw} P_D}{(1 - \frac{v_{BD}}{\phi_{jsw}})^{m_{jsw}}} \quad (3.2.13)$$

where

- FC is the forward-biased non-ideal junction-capacitance coefficient ($\cong 0.5$) [19], [21],
- A_S and A_D are the source and drain bottom areas, respectively,
- P_S and P_D are the source and drain sidewall areas (perimeters $\cdot x_j$), respectively,
- $C_j = \sqrt{\frac{q\epsilon_{si}N_{SUB}}{2\phi_j}} [\frac{F}{m^2}]$ is the zero-bias junction capacitance per unit area,

- $C_{jsw} = \sqrt{\frac{q\epsilon_{si}N_{SUB}}{2\phi_{jsw}}} \left[\frac{F}{m^2} \right]$ is the zero-bias, bulk-source/drain sidewall capacitance,
- $x_j[m]$ is metallurgical junction depth [21],
- $\epsilon_{si} = 103.5918 \times 10^{-14} \left[\frac{F}{cm} \right]$ is permittivity of silicon.
- N_{SUB} is the substrate doping concentration,
- m_j is the bulk-junction grading coefficient (0.5) [21],
- m_{jsw} is the bulk-source/drain sidewall grading coefficient (0.33) [21],
- ϕ_j and ϕ_{jsw} are the built-in junction potential and sidewall junction potentials, respectively ($\cong 0.9[V]$) [21].

The diffusion capacitances depend on the bulk-to-drain and bulk-to-source voltage. Figure 3.1 shows that the bulk of the n-channel MOSFET transistors are connected to ground. Assuming that the drain voltage varies between 300mV and 1.3V, and the source voltage varies between 100mV and 300mV, then Figure 3.5 shows the calculated values of the diffusion capacitances. The drain and source voltages are justified by simulating a 900MHz ring oscillator with three stages. Table D.1 in Appendix D gives the values for designing a ring oscillator with center frequency at 900MHz. Chapter 6 discusses the test-bench for simulating the ring oscillator. The layout of this ring oscillator is given in Chapter I.

For more accurate models, the parasitic capacitance and resistance need to be included as well. They are highly dependent on the layout design. Routing with a polysilicon layer would result in increased gate to bulk capacitance and resistance.

Figure 3.5: Calculated bulk-to-drain capacitance C_{BD} vs bulk-to-drain voltage.

Figure 3.6: Calculated bulk-to-source capacitance C_{BS} vs bulk-to-source voltage.

Routing with a metal layer would result in the appearance of overlap and fringing capacitance. Section 5.2.2 from Chapter 5 proposes a technique for including the parasitic capacitances into the theoretical analysis of the ring oscillator.

3.3 Model for the MOS Varactors

MOS varactors are variable, voltage-controlled capacitors based on the MOS structure [17]. Generally, two types of MOS varactors can be distinguished: Inversion MOS (I-MOS) and Accumulation MOS (A-MOS) varactors. In both cases, the MOS transistor realizes a MOS capacitor with a capacitance value dependent on the voltage between the bulk and gate, V_{BG} . In the case of a pMOS-capacitor, the MOS capacitor operates in the strong inversion region if $V_{BG} \gg |V_T|$, where $|V_T|$ is the threshold voltage of the transistor [22]. To configure this type of pMOS capacitor, the drain, source, and the bulk terminals of the pMOS transistor are connected together. These terminals will realize one varactor's terminal, while the other terminal is the gate of the pMOS transistor.

Another way to configure a pMOS-capacitor is accomplished by connecting the bulk to the highest dc-voltage available in the circuit (Vdd), connecting the drain and source as one terminal and using the gate as a third terminal.

Figure 3.7 shows the schematic of the varactor considered by this thesis. It was configured by designing the pMOS device to operate in the depletion and accumulation regions only.

This varactor has two terminals: one is the gate of the pMOS transistor while the bulk is the second terminal. The drain and source are connected together and unused

Figure 3.7: MOS Varactor used in this thesis work.

(i.e. no other signals are applied to them). Because the source and drain are not used, [23] proposed a varactor with removed drain and source (p^+ -doped) and replaced by bulk contacts (n^+ doped). On the one hand, this solution reduces the parasitic n-well resistance of the device. On the other hand, the overlap capacitances will be increased. To reduce these capacitances [17] suggests inserting STIs (Shallow Trench Isolations) in the place of the D-S diffusion regions. The negative aspect for this kind of device, with removed D-S diffusion regions, is the fact that it is not supported by all silicon vendors. Therefore, to avoid potential failure of the varactors, in this thesis the drain and source diffusions were included in the final layout of the varactors.

In the case when the applied gate voltage is greater than the flatband voltage, $V_G > V_{FB}$, the MOS capacitor will operate in the accumulation region. In the case when $V_{TH} < V_G < V_{FB}$, the MOS capacitor operates in the depletion region. V_{TH} is the threshold voltage of the pMOS device while V_{FB} is the flatband voltage. The flatband voltage is defined as the voltage that neutralizes the net charge between the two terminals of the MOS capacitor.

Figure 3.8: Simple Varactor model.

Figure 3.8 shows the simple varactor model. The varactor losses are modeled with a resistor connected in series with the varactor capacitance. The voltage drop between the two terminals noted as G and B determines the varactor capacitance. The control DC voltage is applied to the gate, noted as G, of the pMOS capacitor. When the gate voltage is greater than the flat-band voltage, the positive charge on the gate attracts electrons from the substrate to the oxide-semiconductor interface. The pMOS transistor is operating in accumulation region and the MOS capacitance is equal to the oxide capacitance [23],

$$C_{var} = C_{oxide}, V_G > V_{FB}. \quad (3.3.1)$$

When the applied gate voltage is between the threshold and flat-band voltages then the negative charge on the gate pushes the mobile electrons into the substrate, depleting the semiconductor of the mobile carriers. The pMOS transistor is operating in depletion region and the MOS capacitance is formed by two capacitors connected in series: one is the capacitance of the oxide and the second is the capacitance of the depletion layer:

$$C_{var} = \frac{C_{oxide}C_{dep}}{C_{oxide} + C_{dep}}, V_{TH} < V_G < V_{FB} \quad (3.3.2)$$

The depletion capacitance can be calculated from

$$C_{dep} = \frac{\epsilon_{si}}{x_d} \quad (3.3.3)$$

where x_d is the depletion layer width which can be calculated from [24]:

$$x_d = \sqrt{\frac{2\epsilon_{si}(\phi_i - V_{BG})}{qN_d}} \quad (3.3.4)$$

where ϕ_i is the built-in potential, V_{BG} is the bulk-to-gate voltage, ϵ_{si} is the silicon dielectric constant, q is the electron charge, and N_d is the dopant concentration.

Note that the equation (3.3.1) and (3.3.2) are approximate expressions for the varactor capacitance. According to these expressions, there is an abrupt change between the depletion and accumulation capacitance. The reason for this is the assumed simple model for the varactor. A more complicated accumulation and depletion model of the varactor is presented in [23]. An analytical model to quantitatively simulate capacitance - voltage (C-V) characteristics under accumulation conditions in metal-oxide-semiconductor structures is proposed in [25].

Following the reviewed literature, Figure 3.9 shows the expected capacitance - voltage characteristics for the varactor with one and three fingers. The pMOS transistor has $2.5\mu\text{m}$ width and $0.18\mu\text{m}$ length. The total capacitance in both depletion and accumulation region was calculated by multiplying C_{var} with the effective width and length of the used pMOS transistor.

Figure 3.9: Expected trend for the capacitance - voltage characteristics for the varactor with one and three fingers .

3.4 Summary

In this chapter, a delay stage topology for a single-band ring oscillator was proposed.

The delay stage consisted of two n-channel MOSFET transistors used in a differential pair configuration and MOS varactors to set the frequency of oscillation. A model for the varactor and n-channel MOS transistor was discussed and a new channel coefficient was proposed.

Chapter 4

Analysis of the Delay Stage

This Chapter is focused on the differential mode analysis of the proposed delay stage, shown in Figure 3.1, and deriving its transfer function. The model for the varactors was given in Section 3.3. The model for the n-channel MOSFET transistors was given in Section 3.2. The model for the n-channel MOSFET transistors included one ideal ideal transistor surrounded by gate and diffusion capacitances. Although it is known that the delay stage is used for designing a voltage-controlled oscillator and that large signals are expected, the ideal transistor is treated assuming small signals. To refer that the delay stage is in a large signal environment, the small signal transconductance g_m is replaced by the large signal transconductance G_m . By ignoring the large signal effects, such as mobility degradation, channel length modulation (CLM), and drain induced barrier lowering (DIBL), it is expected that the following analysis introduces errors during its derivations. However, the results are good for understanding the ring oscillators regarding their frequency of oscillation and phase noise.

4.1 Differential-mode Analysis without the Varactor and MOS parameters

In this section the differential gain of the delay stage is derived assuming frequencies where all capacitances in the circuit can be ignored. Figure 4.1 shows the implementation of the half-circuit technique that can be used for differential mode analysis of the delay stage. To simplify the hand calculations, it is assumed that the MOSFET transistors are in a small signal environment. In that case, for the pure differential signals the common source node represents a virtual ground [26], [27].

Figure 4.1: Implementation of the half-circuit technique for differential mode analysis of the proposed delay stage excluding all capacitances [26], [27].

In an ideal differential amplifier the output voltage depends only of the differences of the two input voltages:

$$(v_{out})_{diff} = A_{diff} \cdot v_{id} \quad (4.1.1)$$

where

$$v_{id} = v_{in} - \overline{v_{in}} \quad (4.1.2)$$

is called the differential input of the amplifier.

The output of the transistor $M1$ can be expressed as:

$$v_{d1} = -G_m R_D \frac{v_{id}}{2} \quad (4.1.3)$$

Similarly, the output of the transistor $M2$ would be:

$$v_{d2} = G_m R_D \frac{v_{id}}{2} \quad (4.1.4)$$

The differential output in this case would be:

$$(v_{out})_{diff} = v_{d1} - v_{d2} = -G_m R_D \cdot v_{id} \quad (4.1.5)$$

Hence, the differential gain

$$A_{diff} = \frac{(v_{out})_{diff}}{v_{id}} = -G_m R_D \quad (4.1.6)$$

4.2 Differential-mode Analysis: the Effect of the Varactor and MOS Parameters

The ring oscillators described in this thesis incorporate differential blocks. Signals are brought differentially to each block and taken out differentially as well. Therefore, the differential gain of one block is of special interest because it can be considered as a transfer function of one delay stage.

Figure 4.2 shows the implementation of the half-circuit technique for differential mode analysis of the proposed delay stage. It includes the MOSFET's and varactor's

Figure 4.2: Implementation of the half-circuit technique for differential-mode analysis of the proposed delay stage with included models for the MOSFET transistors and varactors.

models previously discussed in Chapter 3. Note that the parasitic capacitances due to the layout, such as the overlap metal capacitance and fringing capacitance are not included at this stage of the analysis, but their effects will be incorporated later.

Figure 4.2 shows the gate-to-drain capacitance between the input and output of the half-circuit. To simplify the circuit this capacitance can be replaced by one input and one output capacitance (Miller effect) [28].

Figure 4.3 illustrates the Miller Effect. The block in Figure 4.3 represents one half-circuit from Figure 4.2. The gain of the half-circuit at intermediate frequencies is $-\frac{1}{2}G_m R_D$ (expression 4.1.3 from Section 4.1).

The Miller theorem says that if there is a feedback impedance Z between the input and output of a voltage amplifier then that amplifier can be represented by one equal amplifier with the same voltage gain, however, the impedance Z that connects

Figure 4.3: The Miller Effect: (a) the impedance Z that exists between the input and output of the circuit can be replaced by (b) an input and output impedance, Z_1 and Z_2 respectively.

the input and the output is replaced by an input and output impedance, Z_1 and Z_2 respectively. The influence of the feedback impedance Z is such that through this impedance goes one current I_{z1} from the input and one current I_{z2} from the output. Figure 4.3(a) illustrates that the input current is divided into two parts. One part of the current I_1 enters the circuit, noted as I_{in1} and the second part I_{z1} goes through the impedance Z . If one impedance Z_1 is placed in parallel to the input of the circuit such that the current through that impedance is equal to I_{z1} then, regarding the input, there is the same situations as shown in Figure 4.3(a). Figure 4.3(a) illustrates that the output current is divided into two parts, as well. One part of the current I_2 enters the circuit, noted as I_{in2} and the second part I_{z2} goes through the impedance Z . If one impedance Z_2 is placed in parallel to the output of the circuit such that the current through that impedance is equal to I_{z2} then, regarding the output, there is the same situations as shown in Figure 4.3(a). Thus, the circuit in Figure 4.3(b) is equivalent to the circuit 4.3(a).

The following analysis will determine the impedances Z_1 and Z_2 .

From Figure 4.3(a) the input voltage is:

$$V_1 = I_1 Z + V_2. \quad (4.2.1)$$

Knowing that the gain of one half-circuit is $-\frac{1}{2}G_m R_D$, the output voltage is,

$$V_2 = -\frac{1}{2}G_m R_D V_1. \quad (4.2.2)$$

Substituting (4.2.2) into (4.2.1) and solving for V_1

$$V_1 = I_1 \frac{Z}{1 + \frac{1}{2}G_m R_D} \quad (4.2.3)$$

Thus, the input impedance is,

$$Z_1 = \frac{V_1}{I_1} = \frac{Z}{1 + \frac{1}{2}G_m R_D} \quad (4.2.4)$$

Substituting (4.2.3) into (4.2.2) and replacing $I_1 = -I_2$ then the output voltage has the expression

$$V_2 = I_2 \frac{\frac{1}{2}G_m R_D}{1 + \frac{1}{2}G_m R_D} Z \quad (4.2.5)$$

Hence, the output impedance is,

$$Z_2 = \frac{V_2}{I_2} = Z \frac{\frac{1}{2}G_m R_D}{1 + \frac{1}{2}G_m R_D}. \quad (4.2.6)$$

The impedance Z represents the gate-to-drain capacitance

$$Z = \frac{1}{j\omega C_{GD}} \quad (4.2.7)$$

Thus, the input is modified by including the capacitance C_1 at the input to the amplifier, where,

$$C_1 = C_{GD} \left(1 + \frac{1}{2}G_m R_D \right). \quad (4.2.8)$$

The output impedance is modified by including a capacitance C_2 at the output of the amplifier, where,

$$C_2 = C_{GD} \left(1 + \frac{2}{G_m R_D} \right). \quad (4.2.9)$$

Figure 4.4: Simplified delay stage for the differential-mode analysis by implementing the half-circuit technique.

Figure 4.4 shows the simplified half-circuits for differential-mode analysis. The drain impedance (Z_D) will see the drain capacitance in parallel with the load resistor and varactor's parameters,

$$Z_D = \left(\frac{1}{s(C_2 + C_{BD})} \right) \parallel (R_D) \parallel \left(R_{var} + \frac{1}{sC_{var}} \right). \quad (4.2.10)$$

The equation 4.2.10 can be rewritten as,

$$Z_D = \frac{R_D (1 + sR_{var}C_{var})}{1 + s[C_{var}R_{var} + R_D(C_{var} + C_2 + C_{BD})] + s^2[R_D R_{var} C_{var}(C_2 + C_{BD})]}. \quad (4.2.11)$$

The input impedance can be calculated from:

$$Z_{in} = \left(\frac{1}{sC_{GB}} \right) \parallel \left(\frac{1}{sC_1} \right) \parallel \left(\frac{1}{sC_{GS}} + (r_S) \parallel \left(\frac{1}{sC_{BS}} \right) \right). \quad (4.2.12)$$

From Table 3.1 (Section 3.2) $C_{GS} = 9.85[\text{fF}]$. At 400[MHz] the gate-to-source impedance is 40415 Ohms, while at 5[GHz] the gate-to-source impedance is 3233 Ohms. For the salicide process, the resistor $r_S \approx 0$ [19]. Thus,

$$\frac{1}{sC_{GS}} \gg \frac{r_S}{1 + sC_{BS}r_S}. \quad (4.2.13)$$

Hence, the input impedance is pure capacitive,

$$Z_{in} = \frac{1}{s(C_{GB} + C_1 + C_{GS})}. \quad (4.2.14)$$

The ring oscillators presented in this thesis employ a cascaded connection of an odd number of delay stages. This means that the input impedance of one delay stage will be a load to the previous stage. Therefore, the total load impedance of one delay stage would be:

$$Z_L = (Z_D) \parallel (Z_{in}). \quad (4.2.15)$$

By taking into consideration the equations (4.2.11) and (4.2.14), the expression for the load impedance is,

$$Z_L = \frac{R_D (1 + sR_{var}C_{var})}{1 + s[C_{var}R_{var} + R_D(C_{var} + C_{temp})] + s^2[R_D R_{var} C_{var} C_{temp}]} \quad (4.2.16)$$

where

$$C_{temp} = C_1 + C_2 + C_{BD} + C_{GB} + C_{GS}. \quad (4.2.17)$$

The source impedance will see the source resistance in parallel with the gate-to-source and bulk-to-source capacitance,

$$Z_S = (r_S) \parallel \left(\frac{1}{sC_{GS}} \right) \parallel \left(\frac{1}{sC_{BS}} \right) \quad (4.2.18)$$

The full expression of the source impedance is give by:

$$Z_S = \frac{r_S}{1 + s (C_{GS} + C_{BS}) r_S} . \quad (4.2.19)$$

The single-ended output of the half-circuit shown on the left side in Figure 4.4 is,

$$v_{d1} = -\frac{v_{id}}{2} G_m R_D \cdot f(R, C)_{diff} . \quad (4.2.20)$$

The single-ended output of the half-circuit shown on the right side is,

$$v_{d2} = +\frac{v_{id}}{2} G_m R_D \cdot f(R, C)_{diff} \quad (4.2.21)$$

where

$$f(R, C)_{diff} = \frac{1 + s [C_{var} R_{var} + (C_{GS} + C_{BS}) r_S] + s^2 (C_{GS} + C_{BS}) C_{var} R_{var} r_S}{1 + s [C_{var} R_{var} + R_D (C_{var} + C_{temp})] + s^2 [R_D R_{var} C_{var} C_{temp}]} . \quad (4.2.22)$$

The differential output in this case is,

$$(v_{out})_{diff} = v_{d1} - v_{d2} = -G_m R_D \cdot v_{id} \cdot f(R, C)_{diff} . \quad (4.2.23)$$

Thus, the differential gain is,

$$A_{diff} = -G_m R_D \cdot f(R, C)_{diff} . \quad (4.2.24)$$

The differential gain involves the factor $f(R, C)_{diff}$ when the MOSFET's and varactor's models are included. Let the transfer function in the s - domain of one block be noted as $H(s)$. According to the equation (4.2.24), the transfer function of one delay stage has the expression,

$$H(s) = -G_m R_D \cdot \frac{a_2 s^2 + a_1 s + 1}{b_2 s^2 + b_1 s + 1} \quad (4.2.25)$$

where

$$a_2 = (C_{GS} + C_{BS}) C_{var} R_{var} r_S \quad (4.2.26)$$

$$a_1 = C_{var} R_{var} + (C_{GS} + C_{BS}) r_S \quad (4.2.27)$$

$$b_2 = R_D R_{var} C_{var} C_{temp} \quad (4.2.28)$$

$$b_1 = C_{var} R_{var} + R_D (C_{var} + C_{temp}) . \quad (4.2.29)$$

The function $H(s)$ has two zeros:

$$z_1 = \frac{-a_1 + \sqrt{a_1^2 - 4a_2}}{2a_2} \quad (4.2.30)$$

$$z_1 = \frac{-a_1 - \sqrt{a_1^2 - 4a_2}}{2a_2} \quad (4.2.31)$$

and two poles:

$$p_1 = \frac{-b_1 + \sqrt{b_1^2 - 4b_2}}{2b_2} \quad (4.2.32)$$

$$p_2 = \frac{-b_1 - \sqrt{b_1^2 - 4b_2}}{2b_2} . \quad (4.2.33)$$

By replacing $s = j\omega$ the expression for the transfer function $H(s)$ can be rewritten as,

$$H(j\omega) = -G_m R_D \frac{(1 - a_2 \omega^2) + a_1 j\omega}{(1 - b_2 \omega^2) + b_1 j\omega} . \quad (4.2.34)$$

The equation 4.2.34 represents the transfer function of one delay stage in the frequency domain. The next chapter is dedicated for analysis of the ring oscillator and it starts by using this transfer function.

4.3 Summary

The focus of this chapter was the analysis of the proposed delay stage for a single-band ring oscillator. First, the differential-mode analysis, without the varactor and MOSFET parameters, was performed. Second, the effect of the varactor and MOSFET parameters was discussed. The Miller effect was discussed and the input, source and driving impedances of one delay stage were derived. The half-circuit technique was used to derive the transfer function of one delay stage in the frequency domain.

Chapter 5

Analysis of the Ring Oscillator

5.1 Feedback System

The ring oscillator is configured as a positive feedback system that generates harmonic waveforms.

Figure 5.1: Block diagram of a feedback system .

The feedback system consists of an amplifier stage and feedback connection. The concept of the feedback connection is returning part of the output signal to the input of the system. Figure 5.1 shows the block diagram of a linear feedback system. Denote the signal at the amplifier's input with X , the signal at the amplifier's output with X_0 , and the input signal to the amplifier together with the feedback connection with

X_i . The input signal to the feedback circuitry is X_0 , and the output of this circuit is X_r . The feedback circuitry is connected to the input such that

$$X = X_i + X_r. \quad (5.1.1)$$

Thus, the input signal to the amplifier is sum of the input signal to the system and the returned signal.

The transfer function of the amplifier is,

$$A = \frac{X_0}{X} \quad (5.1.2)$$

where with “X” is noted either a voltage or current signal. Therefore, the transfer function of the amplifier might be the ration of two voltages, two currents, a voltage and a current, or a current and a voltage.

The transfer function of the feedback circuitry is,

$$\beta = \frac{X_r}{X_0} \quad (5.1.3)$$

in which β is called the feedback coefficient. Depending of the signal type, it might be the ratio of two voltages, two currents, a voltage and a current, or a current and a voltage.

The transfer function of the feedback system is,

$$A_r = \frac{X_0}{X_i}. \quad (5.1.4)$$

Taking into consideration the previous three equations,

$$\frac{X_0}{X_i} = \frac{X_0}{X - X_r} = \frac{\frac{X_0}{X}}{1 - \frac{X_r}{X}} = \frac{\frac{X_0}{X}}{1 - \frac{X_r}{X_0} \frac{X_0}{X}}. \quad (5.1.5)$$

Hence, the transfer function of the feedback system is,

$$A_r = \frac{A}{1 - \beta A}. \quad (5.1.6)$$

The transfer function in the equation (5.1.6) is related to the product βA . This product is the loop gain. Depending from the loop gain value, three cases can be considered. When $0 < \beta A < 1$ then the denominator in the equation 5.1.6 is smaller than unity. That means that the amplification of the feedback system is greater than the amplification of the system without feedback. In that case, the returned signal has the same phase as the input signal and therefore, the amplifier's input signal is amplified. Thus, the output signal is amplified as well. The system where the product βA and returned signal are positive is called a positive feedback system. The maximum amplification that can be attained occurs when the loop gain is equivalent to unity i.e. $\beta A = 1$. In that case, the denominator in the equation 5.1.6 is equal to zero. Theoretically, the system provides infinite amplification. When $\beta A > 1$ then the denominator in the equation 5.1.6 is greater than unity. In that case, the amplification of the system with feedback is smaller than the amplification of the system without feedback. The system that incorporates this case is called a negative feedback system.

Of special interest for this thesis is the case when the loop gain is equal to unity*.

*That is the case when the feedback system is transformed into an oscillator. Nevertheless, the loop gain should not be exactly equal to unity. In that case the positive feedback will be critical and not sufficient for keeping the oscillation if some device parameters change. Thus, for stable oscillator, the loop gain should be greater than unity. However, the loop gain should not be greater than unity or not much greater than unity because in that case the output signal of the oscillator would be distorted. Instead of generating a fundamental harmonic only, the oscillator will generate higher harmonics as well.

5.2 Ring Oscillator with N-stages

5.2.1 Frequency of oscillation - Method A

To build a voltage controlled ring oscillator three differential blocks were enough, as shown in Figure 5.2. The non-inverted output of the first stage is fed to the inverted input of the second stage, while the inverted output of the first stage is fed to the non-inverted input of the second stage. The same procedure is performed between the second and the third stage. Finally, the inverted output of the third stage is fed back to the non-inverted input of the first stage, and the non-inverted output of the third stage is fed back to the inverted input of the first stage. Thus, a positive feedback system is designed and its frequency of oscillation can be programmed.

Figure 5.2: Three-stage ring oscillator .

The loop gain for this system is,

$$\beta A = H(j\omega) \cdot H(j\omega) \cdot H(j\omega) . \quad (5.2.1)$$

In order the oscillation to start, the returned signal should be in phase with the incoming signal. That means that the loop gain has a phase shift of zero or $2n\pi$

radians, where n is a positive integer:

$$\angle(\beta A) = 2n\pi \text{ radians.} \quad (5.2.2)$$

Each stage contributes a 180° phase shift due to the signal inversion of the stage. For a ring oscillator with three stages, it means 540° phase shift is required. Thus, each stage needs to contribute additional 60° phase shift* so the total phase shift to be 720° or 4π radians which will result in oscillation,

$$\angle(H(j\omega)) = \frac{\pi}{3} \text{ radians.} \quad (5.2.3)$$

Consider a ring oscillator designed with 5 stages. Since each stage contributes a 180° phase shift due to the negative transconductance, the total phase shift would be 900° . In order the feedback system to start to oscillate each stage should contribute additional 36° for total 1080° or 6π radians. Hence, for the ring oscillator with five-stages,

$$\angle(H(j\omega)) = \frac{\pi}{5} \text{ radians.} \quad (5.2.4)$$

Consider now a ring oscillator configured with 7 stages. With the same analogy as described for the three- and five-stages ring oscillator, each stage should contribute an additional $25^\circ 42'$ for a total phase shift of 8π radians. Thus, for the ring oscillator with seven-stages,

$$\angle(H(j\omega)) = \frac{\pi}{7} \text{ radians.} \quad (5.2.5)$$

Finally, the above discussion can be generalized for the ring oscillator configured with N -stages. For such a ring oscillator, each stage should contribute,

$$\angle(H(j\omega)) = \frac{\pi}{N} \text{ radians} \quad (5.2.6)$$

*On average.

phase shift in order for the feedback system to start to oscillate.

The transfer function of one stage is given by the equation (4.2.34),

$$H(j\omega) = -G_m R_D \cdot \frac{(1-a_2\omega^2)+a_1j\omega}{(1-b_2\omega^2)+b_1j\omega}$$

where

a_1 is given by the equation (4.2.27)

$$a_1 = C_{var}R_{var} + (C_{GS} + C_{BS})r_S$$

a_2 is given by the equation (4.2.26)

$$a_2 = (C_{GS} + C_{BS})C_{var}R_{var}r_S$$

b_1 is given by the equation (4.2.29)

$$b_1 = C_{var}R_{var} + R_D(C_{var} + C_1 + C_2 + C_{BD} + C_{GB} + C_{GS})$$

b_2 is given by the equation (4.2.28)

$$b_2 = R_DR_{var}C_{var}(C_1 + C_2 + C_{BD} + C_{GB} + C_{GS}).$$

For a CMOS $0.18\mu\text{m}$ salicide process $r_S \approx 0$ [19]. Thus, the simplified transfer function in frequency domain of one delay stage is,

$$H(j\omega) = -G_m R_D \cdot \frac{1 + j\omega C_{var}R_{var}}{(1 - b_2\omega^2) + b_1j\omega}. \quad (5.2.7)$$

Equations (5.2.6) and (7.1.1) together give,

$$\arctan(\omega C_{var}R_{var}) - \arctan\left(\frac{b_1\omega}{1 - b_2\omega^2}\right) = \frac{\pi}{N}. \quad (5.2.8)$$

If the function $\tan()$ is performed on both sides, and using the identity,

$$\tan(\alpha - \beta) = \frac{\tan(\alpha) - \tan(\beta)}{1 + \tan(\alpha)\tan(\beta)} \quad (5.2.9)$$

then,

$$\frac{\omega C_{var} R_{var} + \frac{b_1 \omega}{1 - b_2 \omega^2}}{1 + (\omega C_{var} R_{var}) \left(-\frac{b_1 \omega}{1 - b_2 \omega^2} \right)} = \tan \left(\frac{\pi}{N} \right). \quad (5.2.10)$$

The equation (5.2.10) can be simplified to,

$$-\tau_2 \cdot \omega^3 + (b_2 + \tau_1) \tan \left(\frac{\pi}{N} \right) \cdot \omega^2 + (b_1 + \tau_{var}) \cdot \omega - \tan \left(\frac{\pi}{N} \right) = 0 \quad (5.2.11)$$

where

$$\tau_{var} = C_{var} R_{var} \quad (5.2.12)$$

$$\tau_1 = b_1 \cdot \tau_{var} \quad (5.2.13)$$

$$\tau_2 = b_2 \cdot \tau_{var}. \quad (5.2.14)$$

The equation (7.2.3) has three roots: one real and two complex. The exact real solution is given in Appendix A. The approximate frequency of oscillation for the ring oscillator with N-stages can be calculated from,

$$f_{osc} = \frac{-b_1 - \tau_{var} + \sqrt{(b_1 + \tau_{var})^2 + 4(b_2 + \tau_1) \left(\tan \frac{\pi}{N} \right)^2}}{2\pi (b_2 + \tau_1) \tan \frac{\pi}{N}}. \quad (5.2.15)$$

Figure 5.3: Implemented buffer topology.

The equation (5.2.15) gives the frequency of oscillation for the feedback system with N-stages. In deriving this expression, the parasitic capacitances due to the layout, such as the overlap capacitances between the metal layers, fringing capacitances, and overlap capacitances between the metal layers and the substrate were ignored. Figure 5.3 shows the topology of the buffer stage used to isolate the ring oscillator output. The n-channel MOSFET is designed with $2.5\mu\text{m}$ width, $0.18\mu\text{m}$ length and five fingers. In an ideal situation, the buffer should not load the VCO output. However, in reality the buffer input impedance will load the VCO. It can be shown that the input impedance of the buffer shown in Figure 5.3 can be assumed as pure capacitive. To simplify the analysis, this capacitance is assumed as parasitic capacitance as well.

To simplify the analysis, the parasitic capacitances were assumed to be distributed throughout the circuit and appear in parallel to the capacitances used in analysis. That means that the value of the capacitors already incorporated during the analysis are increased by the value of the parasitic capacitances. Although each capacitor will see different parasitic capacitance due to the layout, for simplification it can be assumed that each capacitance see additional an average parasitic capacitance $C_{parasitics}$. Hence, if the value of the varactor capacitance C_{var} is replaced by $C_{var} + C_{parasitics}$, as well as the value of C_{temp} is replaced by $C_{temp} + 5 \cdot C_{parasitics}^*$ then the derived formula (5.2.15) is more accurate and closer to reality.

Figure 5.4 shows the calculated and simulated tuning characteristic of the 900MHz ring oscillator. From the simulated results was found that the average value of the

$$^*C_{temp} = C_1 + C_2 + C_{BD} + C_{GB} + C_{GS}$$

Figure 5.4: 900MHz ring oscillator with three stages - calculated and simulated frequency of oscillation.

parasitic capacitances is approximately $C_{parasitics} = 4.22[fF]$. After this value was taken into consideration, the maximum deviation between the simulated and calculated curve was 2.59%, and the average was 1.5%* for the entire range of the control signal (0 - 1.8[V]). Nevertheless, the analytical analysis provides an increased level of understanding of the functionality of the ring oscillator.

Figures 5.5-5.9 show the sensitivity of the derived formula (5.2.15) if some of the parameters such as C_{BD} , C_{GB} , C_{GD} , C_{GS} , and G_m change the value by $\pm 50\%$. The idea is to show that the $\pm 50\%$ does not result in abrupt changes of the estimated oscillation frequency. Note that the actual deviation is expected to be less than 50%. The 50% error was taken as an extreme.

Figure 5.5 shows that if the value of the bulk-to-drain capacitance C_{BD} is changed

*Other researchers' found that their analytical equation for the oscillation frequency has an average error of 8% [29].

Figure 5.5: Calculated variations of the frequency of oscillation when the value of the bulk-to-drain capacitance changes $\pm 50\%$.

Figure 5.6: Calculated variations of the frequency of oscillation when the value of the gate-to-bulk capacitance changes $\pm 50\%$.

Figure 5.7: Calculated variations of the frequency of oscillation when the value of the gate-to-drain capacitance changes $\pm 50\%$.

Figure 5.8: Calculated variations of the frequency of oscillation when the value of the gate-to-source capacitance changes $\pm 50\%$.

Figure 5.9: Calculated variations of the frequency of oscillation when the value of the G_m changes $\pm 50\%$.

by $\pm 50\%$ and all other parameters are kept constant then the frequency of oscillation is changed by $\pm 5\%$ compared with its nominal value ($V_{ctrl} = 0.9V$). Figure 5.6 shows that if the value of the gate-to-bulk capacitance C_{GB} is changed by $\pm 50\%$ and all other parameters are kept constant then the frequency of oscillation is changed by $\pm 2.3\%$ compared with its nominal value. Figure 5.7 shows that if the value of the gate-to-drain capacitance C_{GD} is changed by $\pm 50\%$ and all other parameters are kept constant then the frequency of oscillation is changed by $\pm 17.4\%$ compared with its nominal value. Figure 5.8 shows that if the value of the gate-to-source capacitance C_{GS} is changed by $\pm 50\%$ and all other parameters are kept constant then the frequency of oscillation is changed by $\pm 8\%$ compared with its nominal value. Finally, Figure 5.9 shows that if the value of the transconductance G_m is changed by $\pm 50\%$ and all other parameters are kept constant then the frequency of oscillation is changed by $\pm 5.2\%$

compared with its nominal value. According to the above discussions, the gate-to-drain C_{GD} capacitance is the most critical parameter in estimating the frequency of oscillation.

5.2.2 Frequency of oscillation - Method B

In [18] each stage is represented by the large-signal transconductance G_m of the active elements, while the load of each stage is represented by parallel combination of one resistor and capacitor. Figure 5.10 shows graphically this technique. Since it is an interesting approach, it is applied here for the ring oscillator in this thesis.

Recall that the load impedance of one delay stage, derived in Section 4.2, is given by the equation (4.2.16). Introducing two new variables,

$$\tau_{eq} = R_D C_{temp} \tau_{var} \quad (5.2.16)$$

$$\tau_D = R_D (C_{var} + C_{temp}) \quad (5.2.17)$$

the load impedance is of the form,

$$Z_L = \frac{R_D (1 + j\tau_{var}\omega)}{1 - \tau_{eq}\omega^2 + j(\tau_{var} + \tau_D)\omega} \quad (5.2.18)$$

If the expression for Z_L is represented using a real and imaginary part by multiplying the nominator and denominator with the conjugate of the denominator, then it can be expressed as,

$$Z_L = R_{ser} + \frac{1}{j\omega C_{ser}} \quad (5.2.19)$$

where

$$R_{ser} = R_D \frac{1 - \tau_{eq}\omega^2 + \tau_{var}(\tau_{var} + \tau_D)\omega^2}{(1 - \tau_{eq}\omega^2)^2 + (\tau_{var} + \tau_D)^2\omega^2} \quad (5.2.20)$$

Figure 5.10: Linearized model of three-stage ring oscillator [18].

$$C_{ser} = \frac{(1 - \tau_{eq}\omega^2)^2 + (\tau_{var} + \tau_D)^2 \omega^2}{R_D (\tau_D + \tau_{var}\tau_{eq}\omega^2) \omega^2}. \quad (5.2.21)$$

The expression (5.2.19) indicates that the load impedance is the series combination of a resistor and capacitor. Figure 5.10, considers the parallel connection of a resistor and capacitor. It is necessary to convert the series R-C into a parallel connection.

The values of the parallel resistor and capacitor can be calculated by,

$$R = R_{ser} (1 + Q_L^2) \quad (5.2.22)$$

$$C = C_{ser} \frac{Q_L^2}{1 + Q_L^2} \quad (5.2.23)$$

where Q_L is the quality factor of the load impedance defined as

$$Q_L = \frac{(\tau_D + \tau_{var}\tau_{eq}\omega^2) \omega}{1 - \tau_{eq}\omega^2 + \tau_{var} (\tau_{var} + \tau_D) \omega^2}. \quad (5.2.24)$$

Thus, the transfer function of one stage is,

$$H_i(j\omega) = -G_m \frac{R}{1 + jRC\omega} = -G_m R \frac{1}{1 + j \frac{\omega}{1/(RC)}}. \quad (5.2.25)$$

If a feedback system with N-stages is considered, then the open-loop transfer function (loop gain) would be,

$$H(j\omega) = \left(-\frac{G_m R}{1 + j \frac{\omega}{1/(RC)}} \right)^N. \quad (5.2.26)$$

This feedback system will start to oscillate if each stage contributes a $\frac{180^\circ}{N}$ phase shift.

Thus, the frequency of oscillation can be derived from,

$$\arctan\left(\frac{\omega_{osc}}{1/(RC)}\right) = \frac{180^\circ}{N} \quad (5.2.27)$$

and is given by,

$$f_{osc} = \frac{\tan\left(\frac{180^\circ}{N}\right)}{2\pi RC}. \quad (5.2.28)$$

Equation (5.2.28) gives the frequency of oscillation of a ring oscillator with N-stages. It tells that the frequency of oscillation is inversely proportional to the number of stages and the resistance and capacitance seen by the oscillator.

When the feedback system starts to oscillate, the magnitude of the loop-gain goes to unity,

$$\left(\frac{G_m R}{\sqrt{1 + \left(\frac{\omega}{1/(RC)}\right)^2}}\right)^N = 1. \quad (5.2.29)$$

Combining (5.2.28) and (5.2.29) one can calculate that at the frequency of oscillation,

$$G_m R = \sqrt{1 + \left(\tan\left(\frac{180^\circ}{N}\right)\right)^2}. \quad (5.2.30)$$

The equation (5.2.30) tells that the product $G_m R$ is a function of the number of delay stages. Table 5.1 gives the values of this product for three possible configurations of a ring oscillator.

Table 5.1: The values of $G_m R$ with respect to N

N	3	5	7
$G_m R$	2	1.236	1.11

By using the equation (5.2.30) and (5.2.28) the open-loop transfer function can be further simplified to,

$$H(j\omega) = \left(-\frac{\sqrt{1 + \left(\tan\left(\frac{180^\circ}{N}\right)\right)^2}}{1 + j \tan\left(\frac{180^\circ}{N}\right) \frac{\omega}{\omega_{osc}}} \right)^N. \quad (5.2.31)$$

To conclude, the advantages of the technique in [18] are simplified expressions for the frequency of oscillation and transfer function. Because of its simplicity, the simplified loop-gain (5.2.31) is a starting point for deriving the expression for the phase noise. However, calculating the values of the resistance R and capacitance C is not a straightforward process. As it can be seen from (5.2.20) and (5.2.21), an assumption for the frequency is necessary. When calculating the frequency of oscillation of the given ring oscillator, the values for R and C are important and to find their values, an assumption for the oscillation frequency is necessary. Therefore, the half-circuit technique is more straightforward for calculating the frequency of oscillation. It is based on the circuit parameters and updated with the parasitic capacitances introduced by the layout.

5.2.3 Method for Linearizing the Tuning Characteristic

Figure 5.4 shows that the tuning characteristic of the ring oscillator is non-linear curve. This section will discuss a method for making the tuning curve more linear.

Figure 5.4 shows the frequency versus the control voltage. An expression that will fit the plotted curve is required for linearization. Then a pre-distortion circuit is added with such performances that, when the controlled signal passed through it, the tuning characteristic is more linear.

A simplified way of modeling the tuning curve is to take points from the plotted curve

and then use a software tool to find the polynomial to fit the points. It was found that second (5.2.32) and third order polynomial (5.2.33) can represent the curve shown on Figure 5.4.

$$F_{osc} = a_2x^2 + a_1x + a_0 \quad (5.2.32)$$

$$F_{osc} = a_3x^3 + a_2x^2 + a_1x + a_0. \quad (5.2.33)$$

By fitting the curve with the polynomial expression, one introduces an error. For illustration, if the simulated curve from the Figure 5.4 is taken into consideration, then when it is represented by the second order polynomial, the correlation factor is $R^2 = 0.998114$, indicating a good fit to a second order polynomial. If the same curve is represented by the 3rd order polynomial then the correlation factor is $R^2 = 0.998347$, indicating a better fit. It is clear that both polynomials fit the plotted curve well. Furthermore, the deviation between the two correlation factors is considered to be insignificant. For that reason, the second-order polynomial is considered for the appropriate pre-distortion circuit.

To make the function (5.2.32) linear, the non-linear term, in this case the squared product, should be eliminated. If the variable x is replaced by,

$$x = c_1\sqrt{V_{ctrl}} + c_0 \quad (5.2.34)$$

then the expression for the function F_{osc} becomes,

$$F_{osc} = a_2 \left(c_1\sqrt{V_{ctrl}} + c_0 \right)^2 + a_1 \left(c_1\sqrt{V_{ctrl}} + c_0 \right) + a_0. \quad (5.2.35)$$

Once expanded, one can find that it would be a linear function if,

$$c_0 = -\frac{a_1}{2a_2}. \quad (5.2.36)$$

Figure 5.11: Simulated tuning characteristic with and without pre-distortion .

The expression for the function F_{osc} is then,

$$F_{osc} = a_2 c_1^2 V_{ctrl} - \frac{a_1^2}{4a_2} + a_0 . \quad (5.2.37)$$

The coefficient c_1 can have any value except zero. Hence, the generalized pre-distortion circuit for the 2nd-order polynomial is,

$$x = c_1 \sqrt{V_{ctrl}} - \frac{a_1}{2a_2} . \quad (5.2.38)$$

Example:

By using the above method it was found that the 2nd-order polynomial expression for the simulated tuning curve, given in Figure 5.4 is

$$F_{osc} = 910.35 + 32.1081 \cdot x - 43.3535 \cdot x^2 . \quad (5.2.39)$$

Note that the given numbers are normalized by dividing each of them by 10^6 .

For making this curve linear, the pre-distortion circuit is,

$$x = c_1 \sqrt{V_{ctrl}} + 0.37. \quad (5.2.40)$$

Figure 5.11 shows the effect of using the linearization circuit. Note that, this predistortion method was implemented using Analog Hardware Description Language code. Refer to the Section 5.2.5 for further comments on the linearization technique and its effect on the phase noise.

5.2.4 Phase Noise

A figure of merit of voltage-controlled oscillators is the phase noise. This section is dedicated to finding an expression that will predict the phase noise as closely as possible to the simulated/measured results. The analysis is performed in the frequency domain and a linearized model of the ring oscillator is assumed. The quality factor of the open-loop system is defined and determined. A unit bandwidth at an offset $\Delta\omega$ with respect to ω_{osc} is considered. With respect to this bandwidth, the output noise power is calculated and, dividing the result by the carrier power, the phase noise is quantified [18].

Figure 5.1 shows the block diagram of a feedback system. Denote $H(j\omega)$ as the open-loop transfer function of the ring oscillator with N-stages. All ring oscillators included in this thesis were designed with feedback system $\beta = 1$. Hence, the transfer function of the feedback system is,

$$\frac{X_o(j\omega)}{X_i(j\omega)} = \frac{H(j\omega)}{1 - H(j\omega)}. \quad (5.2.41)$$

This system oscillates at frequency $\omega = \omega_{osc}$ if the transfer function, given by 5.2.41,

goes to infinity i.e. if $H(j\omega_{osc}) = 1$.

For frequencies close to the carrier frequency, $\omega = \omega_{osc} + \Delta\omega$, the open-loop transfer function can be approximated by using the Taylor expression as,

$$H(j\omega) \approx H(j\omega_{osc}) + \Delta\omega \frac{dH}{d\omega}. \quad (5.2.42)$$

If 5.2.42 is substituted into 5.2.41 then the noise transfer function is,

$$\frac{X_o[j(\omega_{osc} + \Delta\omega)]}{X_i[j(\omega_{osc} + \Delta\omega)]} = \frac{H(j\omega_{osc}) + \Delta\omega \frac{dH}{d\omega}}{1 - H(j\omega_{osc}) - \Delta\omega \frac{dH}{d\omega}}. \quad (5.2.43)$$

When the feedback system starts to oscillate then $H(j\omega_{osc}) = 1$. Moreover, without introducing a considerable error, it can be assumed that $\Delta\omega \frac{dH}{d\omega} \ll 1$. Thus, the equation 5.2.43 could be further reduced to,

$$\frac{X_o[j(\omega_{osc} + \Delta\omega)]}{X_i[j(\omega_{osc} + \Delta\omega)]} \approx \frac{-1}{\Delta\omega \frac{dH}{d\omega}}. \quad (5.2.44)$$

The open-loop transfer function can be expressed in the form,

$$H(j\omega) = A(\omega) e^{j\Phi(\omega)} \quad (5.2.45)$$

where $A(\omega)$ and $\Phi(\omega)$ are the magnitude and phase, respectively.

Substituting (5.2.45) into (5.2.44) and performing the first derivative with respect to the angular frequency, the expression of the noise transfer function is,

$$\frac{X_o[j(\omega_{osc} + \Delta\omega)]}{X_i[j(\omega_{osc} + \Delta\omega)]} \approx \frac{-1}{\Delta\omega \left(\frac{dA}{d\omega} + jA \frac{d\Phi}{d\omega} \right) e^{j\Phi(\omega)}}. \quad (5.2.46)$$

Knowing that at the frequency of oscillation $A \approx 1$ and

$$|e^{j\Phi(\omega)}|^2 = \sqrt{(\cos\Phi(\omega))^2 + (\sin\Phi(\omega))^2} = 1 \quad (5.2.47)$$

then the noise power spectral density can be calculated from,

$$\left| \frac{X_o [j (\omega_{osc} + \Delta\omega)]}{X_i [j (\omega_{osc} + \Delta\omega)]} \right|^2 \approx \frac{1}{(\Delta\omega)^2 \left(\left(\frac{dA}{d\omega} \right)^2 + \left(\frac{d\Phi}{d\omega} \right)^2 \right)}. \quad (5.2.48)$$

If the open-loop quality factor, Q , of the system is defined as,

$$Q = \frac{\omega_{osc}}{2} \sqrt{\left(\frac{dA}{d\omega} \right)^2 + \left(\frac{d\Phi}{d\omega} \right)^2} \quad (5.2.49)$$

then the noise power spectral density is,

$$\left| \frac{X_o [j (\omega_{osc} + \Delta\omega)]}{X_i [j (\omega_{osc} + \Delta\omega)]} \right|^2 = \frac{1}{4Q^2} \left(\frac{\omega_{osc}}{\Delta\omega} \right)^2. \quad (5.2.50)$$

Equation (5.2.31) gives the simplified open-loop transfer function of ring oscillator with N delay stage in frequency domain. The magnitude and phase of this function are,

$$A(\omega) = \left(\frac{\sqrt{1 + \left(\tan \frac{180}{N} \right)^2}}{\sqrt{1 + \left(\frac{\omega}{\omega_{osc}} \tan \frac{180}{N} \right)^2}} \right)^N \quad (5.2.51)$$

$$\Phi(\omega) = -N \arctan \left(\frac{\omega}{\omega_{osc}} \tan \frac{180}{N} \right). \quad (5.2.52)$$

The first derivatives of the magnitude and phase in respect to the angular frequency at the point $\omega = \omega_{osc}$ are,

$$\frac{dA}{d\omega} \Big|_{\omega=\omega_{osc}} = -\frac{N}{\omega_{osc}} \cdot \frac{\left(\tan \frac{180}{N} \right)^2}{1 + \left(\tan \frac{180}{N} \right)^2} \quad (5.2.53)$$

$$\frac{d\Phi}{d\omega} \Big|_{\omega=\omega_{osc}} = -\frac{N}{\omega_{osc}} \cdot \frac{\tan \frac{180}{N}}{1 + \left(\tan \frac{180}{N} \right)^2}. \quad (5.2.54)$$

With substituting the equations 5.2.53 and 5.2.54 into 5.2.49 the Q of the open-loop system is,

$$Q = \frac{N}{2} \cdot \frac{\tan \frac{180}{N}}{\sqrt{1 + \left(\tan \frac{180}{N} \right)^2}}. \quad (5.2.55)$$

Table 5.2: The values of Q with respect to N

N	3	5	7
Q	1.299	1.469	1.519

The equation (5.2.55) tells that the quality factor of the open-loop system depends from the number of delay stages, however, it apparently does not depend on their topology. Note that this is due to the simplifications made during the analysis. Table 5.2 shows the values of the quality factor of the open-loop system for three possible configuration of ring oscillator.

The equation 5.2.50 gives the noise power spectral density in terms of voltage. To find the total output noise power, one should find what is the input noise and multiply that with this function, also known as noise transfer function. Generally, an input noise current i_n is considered as the noise source. Therefore, it can be assumed that one noise current is placed at each node of the feedback system. In that case, the input noise voltage can be calculated by multiplying this noise current with the load impedance at that node, i.e.

$$X_i = i_n \cdot \frac{R}{1 + j\omega RC} . \quad (5.2.56)$$

Hence, at the frequency of oscillation the input noise power is,

$$|X_i|^2 = \overline{i_n^2} \cdot \frac{R^2}{1 + \left(\tan \frac{180}{N}\right)^2} . \quad (5.2.57)$$

For the differential stage in Figure 5.12, the thermal noise current per unit bandwidth is,

$$\overline{i_n^2} = 4kT \left(\gamma \frac{I_{SS}}{E_C L_{eff}} + \frac{1}{R_D} + \frac{1}{R_{var}} \right) \quad (5.2.58)$$

Figure 5.12: Noise sources in the used differential delay stage .

where

- the coefficient γ is $2/3$ for long-channel devices in the saturation region and typically two to three times greater for short-channel devices [13]
- $E_C \approx 4 \times 10^6 \frac{V}{m}$ is the critical electric field in the silicon and is defined as the value of electric field resulting in half the carrier velocity expected from low field mobility [13]
- R_{var} is the parallel resistance of the varactor. Since the introduced varactor model included a series resistor, one should calculate the value of the parallel resistor by using (5.2.22). Since the serial resistance is small, the parallel resistor would have a comparatively large value and the contribution to the output noise current from the smaller resistor can be neglected.

For a differential ring oscillator with N stages, there is one such noise source at each

node. Therefore, the total output noise power due to 2N-noise currents is,

$$|X_o|^2 = \frac{2N \cdot \overline{i_n^2}}{1 + \left(\tan \frac{180}{N}\right)^2} \cdot \frac{R^2}{4Q^2} \left(\frac{\omega_{osc}}{\Delta\omega}\right)^2. \quad (5.2.59)$$

The phase noise of the oscillator is defined as ratio between the total output noise power and carrier power P_S ,

$$PN = \frac{|X_o|^2}{2P_S}. \quad (5.2.60)$$

Note that only one-half of the phase noise is considered. The other half is due to the amplitude noise.

The carrier power in term of the peak-to-peak voltage is given by the expression,

$$P_S = \frac{V_{pp}^2}{8}. \quad (5.2.61)$$

Finally, the expression for the phase noise is,

$$PN = \frac{8kTN}{V_{pp}^2 \left(1 + \left(\tan \frac{180}{N}\right)^2\right)} \left(\gamma \frac{I_{SS}}{E_C L_{eff}} + \frac{1}{R_D} + \frac{1}{R_{var}} \right) \cdot \frac{R^2}{Q^2} \left(\frac{\omega_{osc}}{\Delta\omega}\right)^2. \quad (5.2.62)$$

Table 5.3: Calculated phase noise at 1MHz frequency offset, $V_{ctrl}=1[V]$

Ring Oscillator	Stages	Varactor	γ	I_{SS} [μA]	V_{pp} [V]	PN [dBc/Hz]
450MHz	3	x 3	2	87.8	1.71	-108.9
700MHz	3	x 3	2	129	1.66	-103.4
900MHz	3	x 3	2	172	1.75	-103.1
1800MHz	3	x 3	2	331	1.57	-99.5
1800MHz	3	x 1	2	283	1.58	-97.8
1900MHz	3	x 3	2	344	1.54	-99.0
1900MHz	3	x 1	2	311	1.61	-98.0
2400MHz	3	x 3	2	413	1.35	-99.8
2400MHz	3	x 1	2	414	1.68	-97.0

Table 5.3 shows the calculated phase noise for all ring oscillators with three-stages included in this thesis work. The coefficient γ was arbitrary chosen to be 2 to account

for the worst case. The tail current and peak-to-peak voltage are simulated values and refer to the VCO core. The ambient temperature is 27°C. The calculated results are justified with the simulated and measured results presented in Chapter 6.

5.2.5 The Effect of the Varactor Nonlinearity on the Phase Noise

The linearization of the tuning curve was performed in Section 5.2.3 to examine the effect of varactor nonlinearity on the phase noise. Other researchers [30] found that the varactor nonlinearity has an effect on the phase noise of completely integrated VCOs. In Section 5.2.3 of this Chapter was demonstrated that the linearization technique improved the tuning curve by making it more linear. However, the simulated results show that the linearization of the tuning curve does not help for improving the phase noise. To illustrate this, the 900MHz ring oscillator with three stages was simulated. When $V_{ctrl} = 1[V]$ the simulated frequency was 903[MHz] and the phase noise at 1[MHz] frequency offset without linearization was -103.1[dBc/Hz]. When the predistortion was included, then the simulated frequency was 875[MHz] and the phase noise was -103.5[dBc/Hz]. It is clear that the phase noise was not improved. Therefore, it was concluded that the nonlinearities of the varactors used in this thesis did not affect the phase noise or their effect was insignificant.

5.3 Summary

In this chapter, a complete analysis of the ring oscillator with N stages, in terms of the frequency of oscillation and phase noise, was performed. Two methods for deriving the frequency of oscillation were considered. The transfer function of one delay stage (derived in Chapter 4) was used and a novel formula to estimate the oscillation frequency based on the circuit parameters was derived. The effect of the parasitic capacitances due to the layout was discussed. The sensitivity of the derived formula to $\pm 50\%$ deviation of the circuit parameters was investigated. A method for linearizing the tuning curve with a predistortion circuit was presented and its effect on the phase noise was investigated. An expression for estimating the phase noise of a ring oscillator with N stages was also derived.

Chapter 6

Simulated and Measured Results

The implemented ring oscillators were tested in two stages. First, verification of the varactors test structures was undertaken in order to ensure that the fabricated varactors' performances match the expected results. Second, the complete ring oscillator circuit was measured and the FOM was determined using equation (2.4.1) from Section 2.4.

6.1 Varactors

The varactors were tested on-wafer. Cascade Microtech 140-GSG-150 Microprobes were used to contact the test structures.

Figure 6.1: Block diagram of the Maury Automated Tuner System for varactor's s-parameters measurement .

Testing of the varactors was performed by using the Maury Automated Tuner System (MATS), shown in Figure 6.1, composed of,

- computer-controlled electro-mechanical tuners (MT986C Series),
- Agilent 8720ES Vector Network Analyzer (VNA),
- and auxiliary equipment (power sources, RF cables).

Figure 6.2: Measured capacitance versus the controlled voltage of the varactor with three fingers at different frequencies.

Due to lack of available chip area, the test structures of the varactors were not supported by equivalent test structures (Short-Open) for de-embedding. As a consequence, the measured varactor capacitance was affected by the measurement pad frame. For the purpose of this thesis work, verifying the order of the varactor's capacitance value (to a few femtofarads) and tuning characteristic of the varactor was sufficient.

Figure 6.3: Measured capacitance versus the controlled voltage of the varactor with one finger at different frequencies.

The MATS measured the varactor while sweeping the control voltage from 0 to 1.8[V] and the frequency of the VNA from 100MHz to 10GHz.

Figure 6.4: Illustration of the on-chip test structure for measuring the varactor with y-parameters.

The varactors are tested in a GSG (ground-signal-ground) test structure with a center-to-center spacing of $150\mu\text{m}$. Figure 6.4(a) represents the test structure as a two-port system. Assuming that there is no coupling between the input and output, the varactor capacitance can be calculated from the y_{21} (Figure 6.4(c)). The measured s-parameters were converted into y-parameters and the capacitance of the varactors was obtained by taking the imaginary part of y_{21} and dividing by the specified angular

frequency.

A formula to convert the s-parameters into y-parameters is [17],

$$y_{21} = \frac{1}{Z_0} \left[\frac{-2s_{21}}{(1 + s_{11})(1 + s_{22}) - s_{12}s_{21}} \right] \quad (6.1.1)$$

Figure 6.5: Extracted capacitances due to the varactor's layout.

Figures 6.2 and 6.3 show the C-V characteristic of the varactors used in this thesis. The varactor's capacitance is on the order of a few femtofarads and close to the expected values shown in Figure 3.9 Section 3.3 of Chapter 3. The varactor test structure is given in Appendix I. Figure 6.5 shows the extracted layout with parasitic capacitances of the GSG testing structure. Note that the antenna diodes are not extracted properly. However, for calculating the varactor's capacitance the antenna capacitance is assumed to be part of the padframe capacitance.

6.2 Ring Oscillators

The ring oscillators were tested by using the set-up shown in Figure 6.6. Figure I.17 in Appendix I shows a more detailed test structure.

Figure 6.6: Block diagram of the test structure used for measuring the ring oscillators .

The equipment comprised,

- Cascade Microtech ACP/10024 GSGSG-150 Microprobe,
- Cascade Microtech GSGSG-150 EYE-PASS Power Bypass Probe,
- Agilent E4440A PSA Series Spectrum Analyzer, 3 Hz - 26 GHz
- Agilent 54855A Infiniium DSO 6GHz Oscilloscope and InfiniMax 1134A probing system, (1134A probe amp plus the E2669A differential connectivity kit),
- and auxiliary equipment (power sources, RF cables) .

Twenty-two ring oscillators were fabricated in $0.18\mu\text{m}$ CMOS technology. This section presents the detailed results of one particular oscillator and the results of the other oscillators can be found in Appendixes B - G.

Figure 6.7 shows the test structure that was used for simulating the ring oscillators included with this thesis. The modeled input impedance of the Cascade Microtech ACP/10024 GSGSG-150 Microprobe was used for loading the ring oscillators.

Figure 6.7: Test structure used for simulating the ring oscillators.

The layout capacitances will tend to decrease the frequency of oscillation. For that reason, designing a reliable ring oscillator must always be based on the extracted layout rather than the schematic only*. This thesis proposes a formula that predicts the frequency of oscillation based on the device parameters and the approximated distributed parasitic capacitance due to the layout. Figure 6.8 shows the simulated and calculated tuning characteristics of the 2400MHz ring oscillator with three stages incorporating a varactor with one finger. The distributed capacitance due to the layout in this case is $C_{parasitics} = 2.75[\text{fF}]$. The value of each capacitor considered during the oscillator's analysis is increased by the value of this parasitic capacitor. The derived formula was tested for all oscillators included in this thesis and gave acceptable results.

The phase noise performance of the ring oscillator determines its potential application. The penalty for accomplishing a good phase noise is either power consumption

*Assuming the extraction routines actually work correctly. Refer to the conclusions of this thesis for further comments.

Figure 6.8: Calculated and simulated tuning characteristic for the 2400MHz ring oscillator with three-stages and varactor with one finger, $C_{parasitics} = 2.75[\text{fF}]$.

or chip area or package cost or their combination. There are many applications that are not critical regarding the phase noise. For example, telemetry applications such as power control, alarm/security, and toys. Table 6.1 shows the accomplished phase noise performance of the ring oscillators. The same table includes the calculated values for the cycle-to-cycle jitter assuming a white noise source in the oscillator [31],

$$\Delta T_{cc}^2 \approx \frac{4\pi}{\omega_o^3} S_\phi(\omega) (\omega - \omega_o)^2 \quad (6.2.1)$$

where $S_\phi(\omega)$ is the phase noise with the respect to the carrier, ω_o is the oscillation frequency, and $(\omega - \omega_o)$ is the offset frequency.

The cycle-to-cycle jitter represents the rms difference between two consecutive periods and it describes the short-term dynamics of the period [31],

$$\Delta T_{cc} = \lim_{N \rightarrow \infty} \sqrt{\frac{1}{N} \sum_{n=1}^N (\Delta T_{n+1} - \Delta T_n)^2} \quad (6.2.2)$$

Table 6.1 shows that for all ring oscillators, the cycle-to-cycle jitter has predicted

Table 6.1: Calculated cycle-to-cycle jitter based on the simulated results.

RO [MHz]	Stages	Varactor	Offset [MHz]	PN [dBc/Hz]	jitter [ps]
457	3	x 3	1	-106.0	1.81
453	5	x 3	1	-111.8	0.94
456	7	x 3	1	-114.6	0.68
703	3	x 3	1	-104.6	1.11
703	5	x 3	1	-109.7	0.63
703	7	x 3	1	-112.6	0.45
903	3	x 3	1	-103.1	0.91
903	5	x 3	1	-108.4	0.50
903	7	x 3	1	-111.3	0.36
1836	3	x 3	1	-96.3	0.69
1925	3	x 3	1	-95.9	0.67
2430	3	x 3	1	-94.1	0.58
1800	3	x 1	1	-96.8	0.67
1804	5	x 1	1	-101.2	0.40
1802	7	x 1	1	-105	0.26
1902	3	x 1	1	-97.3	0.58
1899	5	x 1	1	-101.3	0.37
1900	7	x 1	1	-104.7	0.25
2400	3	x 1	1	-96.1	0.47
2400	5	x 1	1	-100.4	0.29
2401	7	x 1	1	-103.0	0.21

values between 0.21 and 1.81 ps. This values for the cycle-to-cycle jitter make the ring oscillators attractive for timing applications*.

Figure 6.9 shows the measured phase noise for the 2400MHz ring oscillator with three fingers. The differences between the measured and simulated phase noise for this oscillator is 3 dBc/Hz. The ring oscillators are designed with differential output. The measurements of the phase noise were performed single-ended. Nevertheless, the measured phase noise of the ring oscillators is relatively close to the simulated values and demonstrate that these oscillators are good candidates for timing applications.

*For example, a cycle-to-cycle jitter of 73ps is good for recovering clock and data at rates of 2Gbps as shown in [32].

Figure 6.9: Measured phase noise for the 2400MHz ring oscillator with three-stages and MOS varactor with one finger .

It is important to note that calculated, simulated, and measured results show that, for the topology used with this thesis, improvements of the phase noise and cycle-to-cycle jitter can be accomplished by increasing the number of delay stages. Increasing the number of stages from three to five, or five to seven, or seven to nine, improved the phase noise by 4 dBc/Hz (as shown in Table 6.1). The penalty for this improvement is the power consumption. Justification for the phase noise improvement is that, with increasing the number of stages the voltage swing of the VCO output signal is increased, the delay of the stages is reduced and the switching speed is increased. These effects directly improve the phase noise of the ring oscillator [33]. Note, that the last statements are correct for the topology used in this thesis. Other researchers [13] found that for their ring oscillator topology the smaller number of stages results in improved phase noise.

Table 6.2 summarized the simulated and measured performances of the 2400MHz

Table 6.2: 2400MHz Ring Oscillator with Three-Stages - Performance Summary

	Simulated	Measured	Units	Comments
V_{DD}	1.8		V	
V_{ctrl}	0.4 - 1.8	0.8 - 1.8	V	
R_{DD}	4055.3	3544.3	Ω	tolerance: -12.6%
R_{SS}	99.2	86.7	Ω	tolerance: -12.6%
No. stages	3			
Varactors	2.5 x 0.18 x 1	2.5 x 0.18 x 1		$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$
I_{tail}	414	473	μA	
Power	2.234	2.557	mW	
V_{pp}	197.5	134.2	mV	buffer output
Frequency	2400	1508	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1		MHz	
Phase Noise	-96.1	-93.1	dBc/Hz	
FOM	-160.2	-152.6	dB	
Tuning Range	3.9	2.7	%	
K_{vco}	66.6	40	MHz/V	
VCO core area	4233.8		μm^2	

ring oscillator with three stages and a varactor with one finger.

The measured tail current is approximated by,

$$I_{tail(meas)} = I_{total(meas)} \cdot \frac{I_{tail(sim)}}{I_{total(sim)}} \quad (6.2.3)$$

where (sim) is for simulated, and $(meas)$ for measured.

Similarly, the measured values of the resistors are given by,

$$R_{(meas)} = R_{(sim)} \cdot \frac{I_{tail(sim)}}{I_{tail(meas)}} \quad (6.2.4)$$

where $R_{(sim)}$ is the extracted value of the R_{DD} or R_{SS} .

It is important to note that the expressions (6.2.3) and (6.2.4) do not always hold. Their approximation is made under assumption that the parameters of the extracted active devices match the parameters of the fabricated active devices (MOSFET transistors). This special case tells the maximum tolerance of the resistors (i.e. the worst

case). To justify the expression (6.2.4) the 2400MHz ring oscillator was simulated by changing the value of all resistors accordingly to the expression (6.2.4). The simulated and measured DC currents differed for about 1%. Again, this is under assumption that the device parameters are correctly extracted. This is important to note because the current through the stage is not only a function of the resistors R_{DD} and R_{SS} but also directly proportional to the gate oxide C_{ox} and ratio $\frac{W}{L}$ (MOSFET's width and length). Please see the next section for further details.

Table 6.2 shows that the tuning range of the 2400MHz ring oscillator is narrow. Typically, the ring oscillators are known to have a higher tuning range. This thesis demonstrates that a narrow band ring oscillator is attractive as well.

Table 6.2 shows that the simulated and measured frequency of oscillation are 2.4GHz and 1.5GHz, respectively. This discrepancy is explained in the next section.

6.2.1 Determination of Cause of Frequency Shift

Process variation of the resistor R_{DD} : Assuming that the approximated expressions (6.2.3) and (6.2.4) are not introducing a sizeable error, then Table 6.2 shows that the resistor R_{DD} , for the 2400MHz oscillator considered here, was reduced by 12.6% due to process variations*. This change of R_{DD} results in an increase in the simulated frequency of oscillation of the ring oscillator by 14.4%. Table 6.3 shows how the frequency of oscillation for all measured ring oscillators is affected due to process tolerance of the resistor R_{DD} .

However, the change of the resistor R_{DD} does not explain why the measured

*This is within the process tolerance.

Table 6.3: Affected frequency of oscillation due to the process variation of the R_{DD} .

Ring Oscillator	Stages	Varactor	R_{DD} [%]	$f_{osc}(R_{DD})$ [%]
1800MHz	3	x 3	-14.1	16.2
1900MHz	3	x 3	-14.1	16.2
2400MHz	3	x 3	-14.1	16.2
1800MHz	3	x 1	-24.4	32.2
1900MHz	3	x 1	-21.9	28.0
2400MHz	3	x 1	-12.6	14.4
1800MHz	5	x 1	+7.4	-6.9
1900MHz	5	x 1	+17.4	-14.8
2400MHz	5	x 1	+24.1	-19.4
1800MHz	7	x 1	+34.3	-25.5
1900MHz	7	x 1	+34.5	-25.6
2400MHz	7	x 1	+27.6	-21.5

frequency of oscillation is 900MHz down from the simulated one.

Sensitivity to the supply voltage: Figure 6.10 shows how the frequency of oscillation, of the ring oscillator considered here, is sensitive to the supply voltage. Figure 6.10 tells that if the supply voltage drop down to 1[V] then the simulated frequency of oscillation is 1.5GHz. However, it is not realistic to say that 0.8[V] drop of the supply voltage is possible during the measurements even if the contact between the probes and tested wafer is not very good. In addition, the ring oscillator was tested by adding one inductor between the supply voltage and ring oscillator. The simulated frequency of oscillation versus the “bond-wire” inductance was approximately constant. Therefore, the assumption that the frequency of oscillation drop due to drop of the power supply voltage is excluded.

Output buffer isolation: The ring oscillator was designed together with a source follower buffer for isolating the VCO output of the measuring equipment. To check if the ring oscillator has a good or poor isolation, (i.e. do the probes load the VCO)

Figure 6.10: Sensitivity of the frequency of oscillation due to changes of the supply voltages .

the output of the buffer was loaded with one capacitor and its values was swept up to few picofarads. The simulated frequency of oscillation versus the load capacitance was approximately constant. Thus, the probes do not load the ring oscillator, and this assumption (poor isolation) is therefore discounted.

Slow process: The ring oscillator was simulated with the slow model for the MOSFET transistors. The simulated frequency of oscillation was 200[MHz] down from the case when the typical model is used.

Parasitic resistance: The layout was extracted including the parasitic resistance only. The parasitic resistance affects the frequency of oscillation by 267[MHz].

Parasitic capacitances: The layout of the ring oscillator was extracted including the parasitic capacitance and the extracted view was analyzed. It was noticed that the simulator did not extract the capacitance of the antenna diodes. Figure 6.11 shows the layout of one antenna diode. This diode protects the transistor's gate from electron discharge. Following the expressions given in Section 3.2 of Chapter 3, the

Figure 6.11: Layout of the antenna diode.

capacitance of this antenna diode was calculated approximately to be $48.6[\text{fF}]$. Figure 6.12 shows that three antenna diodes were connected to the controlled line (i.e. the controlled signal of the varactors). This reasoning lead to conclusion that the tool (Cadence's "Diva") did not properly extracted all parasitic capacitance due to the lack of rules in the "divaExt.rul" file to account for the capacitance.

Figure 6.13 consider the scenario when extra capacitance appear inside the VCO loop. Each stage of the ring oscillator is loaded with an equal capacitance. Figure 6.13 shows that approximately $30[\text{fF}]$ extra load capacitance per stage results the frequency of oscillation to drop to $1.5[\text{GHz}]$.

The current through one MOSFET transistor is directly proportional to the oxide capacitance C_{ox} [19]. If it is assumed that all MOSFET parameters and resistors are

Figure 6.12: Location of the antenna diodes in actual layout .

Figure 6.13: Simulated scenario when the delay stages of the ring oscillator are loaded by an equal capacitance .

extracted correctly, then,

$$\frac{(I_{tail})_{meas}}{(I_{tail})_{sim}} = \frac{(C_{ox})_{meas}}{(C_{ox})_{sim}} \quad (6.2.5)$$

Table 6.2 shows that,

$$(C_{ox})_{meas} = 1.14 \cdot (C_{ox})_{sim} \quad (6.2.6)$$

Equation (6.2.6) tells that the measured oxide capacitance is 14% higher compared with the simulated oxide capacitance. More likely is that during the fabrication process all circuit parameters are affected. Nevertheless, this is just one more example to support the statement that the tool did not extract correctly the parasitic capacitances.

Figure 6.14: Simulated and measured tuning characteristic for the three-stage ring oscillators with center frequency 1.8, 1.9, and 2.4[GHz], and varactor with one finger.

Finally, Figure 6.14 shows the simulated and measured tuning characteristic of three-stage ring oscillators with center frequencies of 1.8, 1.9, and 2.4GHz and varactor with one finger. Note the differences between the simulated and measured tuning characteristic is 53.5%, 53.6%, and 59.2% for the 1800, 1900, and 2400[MHz] ring oscillator, respectively. That supports the notice that the simulator did not extracted properly the layout and therefore, the simulated results are more optimistic than real.

Theory of distributed capacitance: The previous discussions pointed that the tool did not extracted all parasitic capacitances properly. The effect of the parasitic capacitances on the frequency of oscillation is evident from the Table 6.2. Thus, the derived formula for the frequency of oscillation in Chapter 5 should be modified to account for the “fabricated” parasitic capacitances.

Table 6.4: Affected frequency of oscillation due to the existence of extra capacitance in the oscillators loop.

Ring Oscillator	Stages	Varactor	$f_{osc}(C_{extra})$ [%]	C_{extra} [fF]
1800MHz	3	x 3	-41.26	9.20
1900MHz	3	x 3	-41.82	9.50
2400MHz	3	x 3	-41.27	9.60
1800MHz	3	x 1	-50.83	8.42
1900MHz	3	x 1	-49.25	8.40
2400MHz	3	x 1	-45.27	7.72
1800MHz	5	x 1	-35.26	4.48
1900MHz	5	x 1	-29.90	3.60
2400MHz	5	x 1	-28.83	3.83
1800MHz	7	x 1	-18.88	2.34
1900MHz	7	x 1	-20.10	2.60
2400MHz	7	x 1	-20.10	2.02

The derived formula for frequency of oscillation consider six capacitances denoted as C_1 , C_2 , C_{BD} , C_{GB} , C_{GS} , and C_{var} . If the varactor’s resistance is ignored* then

*This introduces an error less than 1%.

all six capacitances appear in parallel. If extra parasitic capacitance appear on the VCO loop, then the value of these capacitances will be increased. For simplification, it can be assumed that the parasitic capacitance per stage that caused the frequency to drop to 1.5GHz can be equally distributed to all six capacitances. In that case, each capacitance will be increased by an average value of C_{extra} .

Table 6.4 shows the estimated values of C_{extra} and affection on the frequency of oscillation. Note that the effect of the extra capacitance can be minimized by increasing the number of stages. In one hand the increased number of stages will improve the phase noise. In other hand the increased number of stages will make the frequency of oscillation to be less sensitive to the extra capacitance in the circuit.

Figure 6.15: Calculated tuning characteristic with included effects from R_{DD} and C_{extra} for the 2400MHz ring oscillator with 3 stages and varactor with one finger .

Figure 6.15 shows what would be the measured frequency of oscillation due to the effects from the R_{DD} and C_{extra} for the 2400MHz ring oscillator with three stages and varactor with one finger. Not only the frequency of oscillation is turned down but

also the tuning range is narrower.

6.3 Summary

The simulated and measured results of the single-band ring oscillator and implemented varactors were discussed in this chapter. The varactors were tested using the Maury Automated Tuner System. The measured s-parameters were converted into y-parameters and the capacitance of the varactors was determined by taking the imaginary part of y_{21} and dividing it by the specified angular frequency. The test structure used for simulating and measuring the ring oscillators was discussed. A possible application for the ring oscillators was considered based on the simulated and measured results. An incomplete circuit extractions by the simulation tool (diva) was the reason for the discrepancy between the simulated and measured frequency of oscillation. The effect of the process variation on the frequency of oscillation was also discussed.

Chapter 7

Multi-Band Voltage-Controlled Ring Oscillator

Figure 7.1 shows the circuit schematic for the proposed adaptable delay cell. It includes a differential amplifier with two n-channel MOS transistors and one “common-source resistor”. Multi-band operation is achieved using p-channel MOS transistors acting as active loads along with p-channel MOS transistors acting as varactors. The varactors are $0.18\mu\text{m}$ in length and $3 \times 2.5\mu\text{m}$ in width and are connected between the differential outputs. The active loads and the n-channel MOS transistors are sized with $4 \times 2.5\mu\text{m}$ width and $0.18\mu\text{m}$ length.

Two voltage signals are available for controlling the delay stage. The first signal, denoted “ V_{freq_band} ” acts to adjust the active load impedance. This signal is for coarse control of the oscillator’s frequency of operation. For proper functionality of the oscillator, this signal is limited to a certain voltage values. For the implementation demonstrated in this thesis, if the power supply is set to 1[V] then V_{freq_band} can have values between 160 and 380 [mV], resulting in simulated frequencies of operation between 323[MHz] and 3140[MHz], respectively. However, if the supply voltage is set to 1.8[V] then V_{freq_band} can have values between 0.77 and 1.22[V] resulting in

Figure 7.1: Adaptable delay stage suitable for configuring a multi-band voltage-controlled ring oscillator.

simulated frequencies of operation as low as 22[MHz] and as high as 5.1[GHz].

The second control signal is named “ V_{ctrl} ”. It controls the varactor’s capacitance.

Figure 7.2 shows that once the frequency band is selected by the V_{freq_band} , then varying the V_{ctrl} from 0 to 1.8 [V]* enables the output signal to have fine tuning over a narrow frequency range of operation.

Figure 7.2: Multi-band operation with a single VCO. V_{fb} is a voltage control signal for a coarse tuning (in the text denoted as V_{freq_band}). V_{ctrl} is the second control signal used for a fine tuning. Δf is the tuning range.

*For the 0.18 μ m CMOS process used in this thesis.

simplified transfer function in the frequency domain for one delay stage is given by,

$$H(j\omega) = -G_m R_p \cdot \frac{1 + j\omega C_{var} R_{var}}{(1 - b_2 \omega^2) + b_1 j\omega} \quad (7.1.1)$$

where

$$b_1 = C_{var} R_{var} + R_p (C_{var} + C_{eqv}) \quad (7.1.2)$$

$$b_2 = R_p R_{var} C_{var} C_{eqv} \quad (7.1.3)$$

$$C_{eqv} = C_1 + C_2 + C_{BD} + C_{GB} + C_{GS} + C_{BDp} + C_{GDp} \quad (7.1.4)$$

$$C_1 = C_{GD} \left(1 + \frac{1}{2} G_m R_p \right) \quad (7.1.5)$$

$$C_2 = C_{GD} \left(1 + \frac{2}{G_m R_p} \right). \quad (7.1.6)$$

7.2 Analysis of the Multi-Band Ring Oscillator

Figure 7.4 shows an adaptable three-stage ring oscillator. Assuming* a linear model as in [18], the loop gain for this system is,

$$\beta A = H(j\omega) \cdot H(j\omega) \cdot H(j\omega). \quad (7.2.1)$$

As it was discussed in Section 5.2.2 of Chapter 5, each stage should contribute 60° phase shift in order for the oscillation to start,

$$\angle(H(j\omega)) = 60. \quad (7.2.2)$$

7.2.1 Frequency of Oscillation

Equations (7.1.1) and (7.2.2) together give

$$-\tau_2 \cdot \omega^3 + B_2 \sqrt{3} \cdot \omega^2 + B_1 \cdot \omega - \sqrt{3} = 0 \quad (7.2.3)$$

*This introduces some error, but is done to make the equations tractable.

Figure 7.4: Three-stage adaptable ring oscillator

where $\tau_{var} = C_{var}R_{var}$, $B_2 = b_2 + b_1 \cdot \tau_{var}$, $\tau_2 = b_2 \cdot \tau_{var}$, and $B_1 = b_1 + \tau_{var}$. The approximated frequency of oscillation for the ring oscillator with 3-stages can be calculated from

$$f_{osc} = \frac{-B_1 + \sqrt{B_1^2 + 12B_2}}{2\pi B_2 \sqrt{3}}. \quad (7.2.4)$$

The equation (7.2.4) gives the frequency of oscillation for the feedback system with 3-stages. In deriving this expression, the parasitic capacitances due to the layout, such as the overlap capacitances between the metal layers, fringing capacitances, overlap capacitances between the metal layers and the substrate as well as the input impedance of the buffer were ignored*.

In Section 5.2.2 of Chapter 5 the parasitic capacitances were assumed to be distributed and to appear in parallel to the capacitances used in the expression (7.2.4). Thus, including the parasitic capacitances, the expanded form of the equation (7.1.4) is,

$$\begin{aligned} C'_{eqv} = & (C_1 + C_{par1}) + (C_2 + C_{par2}) + (C_{BD} + C_{parBD}) + (C_{GB} + C_{parGB}) \\ & + (C_{GS} + C_{parGS}) + (C_{BD_p} + C_{parBD_p}) + (C_{GD_p} + C_{parGD_p}) \end{aligned} \quad (7.2.5)$$

*Again, this introduces error, but makes the equations tractable.

The expression (7.2.5) can be simplified to,

$$C'_{eqv} = C_{eqv} + C_{pc} \quad (7.2.6)$$

where C_{pc} is capacitor parasitics in addition to the desire capacitance, given by,

$$C_{pc} = C_{par1} + C_{par2} + C_{parBD} + C_{parGB} + C_{parGS} + C_{parBD_p} + C_{parGD_p}. \quad (7.2.7)$$

Equation (7.2.6) shows that the parasitic capacitances increase the equivalent capacitance C_{eqv} by the value of C_{pc} . The parasitic capacitances C_{par1} , C_{par2} , C_{parBD} , C_{parGB} , C_{parGS} , C_{parBD_p} , and C_{parGD_p} can be replaced with an equivalent average value denoted as $\overline{C_{pc}}$. Hence,

$$C_{pc} = 7 \cdot \overline{C_{pc}}. \quad (7.2.8)$$

In addition, the varactor capacitance will see a parallel parasitic capacitance denoted as C_{pv} . Equation 7.1.2 tells that if the varactor's resistance R_{var} is ignored* then it can be assumed that the C_{pv} and $\overline{C_{pc}}$ are in parallel. Thus, it can be assumed that a same parasitic capacitance due to the layout, denoted as C_{par} , appear in parallel to the capacitances already included in (7.2.4). Hence, if the value of the varactor capacitance C_{var} is replaced by $C_{var} + C_{par}$ as well as the value of C_{eqv} is replaced by $C_{eqv} + 7 \cdot C_{par}$ then (7.2.4) more closely accounts for layout parasitics.

Note that when the varactor's and parasitic capacitances are of the same order, as it is case in this thesis, then the parasitic capacitances “play” an important role for determining the frequency of oscillation. In that case, if the parasitic capacitances due to layout are not considered then the equation (7.2.4) is not accurate and the

*This introduces an error of 0.6% regarding the frequency of oscillation.

results are more optimistic than real. It is correct to say that without knowing the layout topology it is hard to know what is the value of the layout parasitics. However, statistical methods can be implemented to find what might be the typical values of the layout parasitic capacitances.

Figures 7.5 - 7.7 illustrate the implementation of the equation (7.2.4) and possible typical value for the parasitic capacitance C_{par} for three different cases implemented in $0.18\mu\text{m}$ CMOS technology. Note that in all three cases, if the parasitic capacitances are considered then the equation (7.2.4) is very accurate for the values of the control signal V_{ctrl} around 1[V]. That is a typical operation region of the voltage-controlled oscillator.

Figure 7.5 shows the calculated and simulated frequency of oscillation for one specific case when the supply voltage is set at 1[V], V_{freq_band} is fixed at 0.21V, $C_{par}=11.55[\text{fF}]$, and the second control signal is swept from 0 to 1.8V. The worst case error between the calculated and simulated curve is 1.2%.

Figure 7.6 shows the calculated and simulated frequency of oscillation for the case when the supply voltage is set at 1.8[V], V_{freq_band} is fixed at 0.86V, $C_{par}=19.86[\text{fF}]$, and the second control signal is swept from 0 to 1.8V. The worst case error between the calculated and simulated curve is 1.21%.

Figure 7.7 shows the calculated and simulated frequency of oscillation for the case when the supply voltage is set at 1.8[V], V_{freq_band} is fixed at 1V, $C_{par}=11.35[\text{fF}]$, and the second control signal is swept from 0 to 1.8V. The worst case error between the calculated and simulated curve is -0.67%.

Figure 7.5: Predicted and simulated frequency of oscillation, $V_{DD} = 1[V]$, $V_{freq_band} = 0.21[V]$, and $C_{par} = 11.55[fF]$.

Figure 7.6: Predicted and simulated frequency of oscillation, $V_{DD} = 1.8[V]$, $V_{freq_band} = 0.86[V]$ and $C_{par} = 19.86[fF]$.

Figure 7.7: Predicted and simulated frequency of oscillation, $V_{DD} = 1.8[V]$, $V_{freq_band} = 1[V]$ and $C_{par}=11.35[fF]$.

7.3 Test Results

Figure 7.8 shows the test structure for simulating the multi-band voltage-controlled ring oscillator. The ring oscillator was planned to be tested on chip by using a probe-station and Cascade Microtech probes. Figure 7.8 shows the test structure for simulating the multi-band VCO including the probe model and connection pint to the oscillator.

Table 7.1 shows the simulated performance summary of the multi-band ring oscillator illustrated in this thesis. By using two input voltage signals, featuring an abrupt and a fine control, six-band (450, 700, 900, 1800, 1900, and 2400)[MHz] operation was realized in a single VCO. The VCO consumes from $586\mu W$ to $3.675mW$ from a $1.8[V]$ supply. The VCO has simulated FOM values of -156dB, -157dB, -157dB, -156dB, and

Figure 7.8: Test structure for simulating the multi-band VCO.

-152dB for the bands specified above. The VCO occupies $2461\mu\text{m}^2$ chip area. The layout of this VCO is given in Appendix I.

Table 7.1: Multi-band Ring Oscillator - Simulated Performance Summary

	Band 1 450	Band 2 700	Band 3 900	Band 4 1800	Band 5 1900	Band 6 2400
V_{ctrl} [V]	1	1	1	1	1	1
V_{freq_band} [V]	1.152	1.081	1.030	0.858	0.845	0.802
Frequency [MHz]	454	703	903	1810	1918	2413
Offset [MHz]	1	1	1	1	1	1
PN [dBc/Hz]	-100.1	-100.2	-99.8	-95.9	-95.8	-89.5
Tuning Range [%]	9.0	8.1	7.0	4.0	3.8	2.6
K_{vco} [MHz/V]	27.1	40.4	48.5	80.0	80.0	90.0
V_{DD} [V]	1.8	1.8	1.8	1.8	1.8	1.8
I_{tail} [μA]	108.6	197.2	274.0	572.6	614.1	680.6
V_{pp} [mV] buffer	590	644	659	538	515	411
Number of Stages	3	3	3	3	3	3
Power [mW]	0.586	1.065	1.480	3.092	3.316	3.675
FOM [dB]	-156	-157	-157	-156	-156	-152

Table 7.2 shows the measured performance of the multi-band VCO. Due to process variations, the measured power dissipation is higher and varies from 2.245mW to 5.644mW. The reason for increased power consumption are the process variations which resulted the active load resistance to be lower than simulated one. On the one

hand, the lower resistance would result in higher current. On the other hand, the lower resistance should result in higher frequency as well. However, as it is discussed in Chapter 6, the simulated results are based on not properly extracted layout. The fabricated ring oscillator has more parasitic capacitances that the simulator can see. These capacitances tend to decrease the frequency of oscillation.

Table 7.2: Multi-band Ring Oscillator - Measured Performance Summary

	Band 1 450	Band 2 700	Band 3 900	Band 4 1800	Band 5 1900	Band 6 2400
V_{ctrl} [V]	1	1	1	1	1	1
V_{freq_band} [V]	1.120	1.040	0.990	0.875	0.870	0.840
Frequency [MHz]	455	706	910	1804	1905	2412
V_{DD} [V]	1.8	1.8	1.8	1.8	1.8	1.8
I_{tail} [μ A]	415.8	626.5	769.2	938.5	959.1	1045.1
V_{pp} [mV] buffer	242	211	311	249	238	182
Number of Stages	3	3	3	3	3	3
Power [mW]	2.245	3.383	4.154	5.068	5.179	5.644

7.4 Summary

In this chapter, a novel adaptable delay stage topology was proposed to design a multi-band ring oscillator. A formula for the frequency of oscillation was derived and compared to the simulated results. The effect of the parasitic capacitances due to the layout was discussed. The measured and simulated power consumption of the multi-band ring oscillator was compared and discussed.

Chapter 8

Conclusion

A delay stage with a fixed (resistive) load was used in three-, five-, and seven-stage narrow-band ring oscillators operating at 450, 700, 900, 1800, 1900, and 2400 [MHz]. The frequency tuning characteristic was achieved using a pMOS transistor designed to operate in the depletion and accumulation region. The MOS varactor capacitance was found to be less than the parasitic capacitances. The effect of the parasitic capacitances on the frequency of oscillation was investigated.

A formula for predicting the frequency of oscillation based on the circuit parameters was derived. If a reasonable value for the parasitic capacitances is assumed then this formula shows a good agreement with the simulated and measured results, typically with a frequency estimation error less than 2% within the operation region of the ring oscillator ($V_{ctrl} = 1[V]$).

The effect of the number of stages on the phase noise was investigated. The results show that the improvements of the phase noise can be accomplished by increasing the number of stages. This is explained in Section 6.2. The results point the way for new design techniques for ring oscillators.

A method for tuning curve linearization was proposed. The second order polynomial was used to represent the tuning curve.

The ring oscillators exhibited a low power dissipation and a FOM comparable with that of CMOS LC oscillators was accomplished in a small core layout area. Typically an entire ring oscillator VCO takes less area than a single integrated inductor.

A discrepancy between the simulated and measured frequency of oscillation was found. Methods to determine the cause of the discrepancy were presented. A possible mismatch between the simulated and fabricated resistors was noticed, but the dominant cause was that the tool (diva) did not properly extract the layout. The effect of the load resistor and additional parasitic capacitances was investigated.

A delay stage with active load was used for designing a three-stage ring oscillator. The single VCO supported operation in six frequency bands (450, 700, 900, 1800, 1900, and 2400[MHz]). The multi-band operation was accomplished by controlling the impedance of the active load and the capacitance of the varactors. By controlling the active load impedance, there is an abrupt selection of the frequency of operation. Changing the varactors capacitance resulted in a fine frequency change accompanied by a small VCO gain. The ring oscillator occupied $2461\mu\text{m}^2$ chip area.

8.1 Research Contribution

Three major contributions are coming out of this thesis.

The first contribution is the proposed ring oscillators. Two types of delay stages, novel in the field of ring oscillators are presented: one for single-band and one for multi-band ring oscillators. The single-band ring oscillator operates using a p-channel

MOSFET transistor as a varactor to set the operation frequency. The multi-band ring oscillator operates using two voltage signals to set the frequency of operation. Low dissipation power, small chip area, multi-band operation capability and good spectral purity make these oscillators attractive for timing and telemetry applications.

The second contribution is the formula based on the circuit parameters for predicting the frequency of oscillation. If reasonable parasitic capacitance is assumed, then this formula gives very accurate results especially around the operation region of the oscillator. Typically, the estimated frequency is within 1-2% of actual.

The third contribution was linearization of the tuning characteristic. To find if the non-linearities of the varactor affected the phase noise, a predistortion technique was examined. Although the tuning curve was linearized, the phase noise was not improved.

8.2 Future Work

To minimize the number of tape-outs and therefore the fabrication cost, this thesis recommends the following steps:

First, design and fabricate a varactor accompanied by the equivalent test structures (Short-Open) for de-embedding. Use the measured varactor's capacitance - voltage characteristic to determine an accurate varactor model.

Second, if a fixed resistive load is used then correspondence with the silicon vendor is necessary to design an accurate resistor (i.e. with minimum tolerance).

Third, an accurate model for MOSFET transistors is important for all possible configurations (i.e. width, length, and number of fingers). To do this, fabricate and

measure all possible configurations and create their models.

Forth, use a simulation tool with capabilities of simultaneous extraction of the parasitic resistance and capacitance of the layout. An accurate tool is recommended especially when the desired varactor capacitance is in the same order as the parasitic capacitances.

Finally, use a reliable simulator to minimize the discrepancy between the simulated and measured results.

The relationship between the number of stages included in the ring oscillator and the ring oscillator's phase noise requires further investigation. It may be possible to determine an optimum number of stages.

Techniques for rapidly estimating the required additional parasitic capacitance could be developed.

A full PLL using the ring oscillators described in this thesis could be implemented.

Appendix A

Frequency of oscillation - exact solution

$$-\tau_2 \cdot \omega^3 + (b_2 + \tau_1) \tan\left(\frac{\pi}{N}\right) \cdot \omega^2 + (b_1 + \tau_{var}) \cdot \omega - \tan\left(\frac{\pi}{N}\right) = 0$$

$$\omega = \frac{1}{6} \frac{C}{\tau_2} + \frac{2}{3} \frac{B}{A} + \frac{1}{3} \tan\left(\frac{\pi}{N}\right) (b_2 + \frac{\tau_1}{\tau_2})$$

$$\begin{aligned} \mathbf{A} = & \tau_2(36 \tan\left(\frac{\pi}{N}\right) \tau_2 b_1 b_2 + 36 \tan\left(\frac{\pi}{N}\right) \tau_2 b_1 \tau_1 + 36 \tan\left(\frac{\pi}{N}\right) \tau_2 \tau_{var} b_2 + 36 \tan\left(\frac{\pi}{N}\right) \tau_2 \tau_{var} \tau_1 - \\ & 108 \tan\left(\frac{\pi}{N}\right) \tau_2^2 + 8 \tan\left(\frac{\pi}{N}\right)^3 b_2^3 + 24 \tan\left(\frac{\pi}{N}\right)^3 b_2^2 \tau_1 + 24 \tan\left(\frac{\pi}{N}\right)^3 b_2 \tau_1^2 + 8 \tan\left(\frac{\pi}{N}\right)^3 \tau_1^3 + \\ & 12 \cdot 3^{\frac{1}{2}} (-12 \tau_2 b_1 \tau_{var}^2 - 4 \tan\left(\frac{\pi}{N}\right)^4 \tau_1^3 + 27 \tan\left(\frac{\pi}{N}\right)^2 \tau_2^2 - 12 \tau_2 b_1^2 \tau_{var} - \\ & b_1^2 \tan\left(\frac{\pi}{N}\right)^2 b_2^2 - b_1^2 \tan\left(\frac{\pi}{N}\right)^2 \tau_1^2 - \tau_{var}^2 \tan\left(\frac{\pi}{N}\right)^2 b_2^2 - \tau_{var}^2 \tan\left(\frac{\pi}{N}\right)^2 \tau_1^2 - 4 \tau_2 b_1^3 - 4 \tau_2 \tau_{var}^3 - \\ & 2 b_1 \tau_{var} \tan\left(\frac{\pi}{N}\right)^2 b_2^2 - 2 b_1 \tau_{var} \tan\left(\frac{\pi}{N}\right)^2 \tau_1^2 - 2 b_1^2 \tan\left(\frac{\pi}{N}\right)^2 b_2 \tau_1 - 4 b_1 \tau_{var} \tan\left(\frac{\pi}{N}\right)^2 b_2 \tau_1 - \\ & 2 \tau_{var}^2 \tan\left(\frac{\pi}{N}\right)^2 b_2 \tau_1 - 4 \tan\left(\frac{\pi}{N}\right)^4 b_2^3 - 18 \tan\left(\frac{\pi}{N}\right)^2 \tau_2 \tau_{var} b_2 - 18 \tan\left(\frac{\pi}{N}\right)^2 \tau_2 \tau_{var} \tau_1 - \\ & 18 \tan\left(\frac{\pi}{N}\right)^2 \tau_2 b_1 b_2 - 18 \tan\left(\frac{\pi}{N}\right)^2 \tau_2 b_1 \tau_1 - 12 \tan\left(\frac{\pi}{N}\right)^4 b_2^2 \tau_1 - 12 \tan\left(\frac{\pi}{N}\right)^4 b_2 \tau_1^2)^{\frac{1}{2}} \tau_2)^{\frac{1}{3}} \\ \mathbf{B} = & 3 \tau_2 b_1 + 3 \tau_2 \tau_{var} + \tan\left(\frac{\pi}{N}\right)^2 b_2^2 + 2 \tan\left(\frac{\pi}{N}\right)^2 b_2 \tau_1 + \tan\left(\frac{\pi}{N}\right)^2 \tau_1^2 \\ \mathbf{C} = & (36 \tan\left(\frac{\pi}{N}\right) \tau_2 b_1 b_2 + 36 \tan\left(\frac{\pi}{N}\right) \tau_2 b_1 \tau_1 + 36 \tan\left(\frac{\pi}{N}\right) \tau_2 \tau_{var} b_2 + 36 \tan\left(\frac{\pi}{N}\right) \tau_2 \tau_{var} \tau_1 - \\ & 108 \tan\left(\frac{\pi}{N}\right) \tau_2^2 + 8 \tan\left(\frac{\pi}{N}\right)^3 b_2^3 + 24 \tan\left(\frac{\pi}{N}\right)^3 b_2^2 \tau_1 + 24 \tan\left(\frac{\pi}{N}\right)^3 b_2 \tau_1^2 + 8 \tan\left(\frac{\pi}{N}\right)^3 \tau_1^3 + \\ & 12 \cdot 3^{\frac{1}{2}} (-12 \tau_2 b_1 \tau_{var}^2 - 4 \tan\left(\frac{\pi}{N}\right)^4 \tau_1^3 + 27 \tan\left(\frac{\pi}{N}\right)^2 \tau_2^2 - 12 \tau_2 b_1^2 \tau_{var} - b_1^2 \tan\left(\frac{\pi}{N}\right)^2 b_2^2 - \\ & b_1^2 \tan\left(\frac{\pi}{N}\right)^2 \tau_1^2 - \tau_{var}^2 \tan\left(\frac{\pi}{N}\right)^2 b_2^2 - \tau_{var}^2 \tan\left(\frac{\pi}{N}\right)^2 \tau_1^2 - 4 \tau_2 b_1^3 - 4 \tau_2 \tau_{var}^3 - 2 b_1 \tau_{var} \tan\left(\frac{\pi}{N}\right)^2 b_2^2 - \\ & 2 b_1 \tau_{var} \tan\left(\frac{\pi}{N}\right)^2 \tau_1^2 - 2 b_1^2 \tan\left(\frac{\pi}{N}\right)^2 b_2 \tau_1 - 4 b_1 \tau_{var} \tan\left(\frac{\pi}{N}\right)^2 b_2 \tau_1 - 2 \tau_{var}^2 \tan\left(\frac{\pi}{N}\right)^2 b_2 \tau_1 - \\ & 4 \tan\left(\frac{\pi}{N}\right)^4 b_2^3 - 18 \tan\left(\frac{\pi}{N}\right)^2 \tau_2 \tau_{var} b_2 - 18 \tan\left(\frac{\pi}{N}\right)^2 \tau_2 \tau_{var} \tau_1 - 18 \tan\left(\frac{\pi}{N}\right)^2 \tau_2 b_1 b_2 - \\ & 18 \tan\left(\frac{\pi}{N}\right)^2 \tau_2 b_1 \tau_1 - 12 \tan\left(\frac{\pi}{N}\right)^4 b_2^2 \tau_1 - 12 \tan\left(\frac{\pi}{N}\right)^4 b_2 \tau_1^2)^{\frac{1}{2}} \tau_2)^{\frac{1}{3}} \end{aligned}$$

Appendix B

450MHz Ring Oscillator

Table B.1: 450MHz Ring Oscillator with Three-Stages - Performance Summary

	Simulated	Units	Comments
V_{DD}	1.8	V	
V_{ctrl}	0.4 - 1.8	V	
R_{DD}	17494.6	Ω	
R_{SS}	2081.8	Ω	
No. stages	3		
Varactors	2.5 x 0.18 x 3	$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$	
I_{tail}	87.8	μA	
Power	0.474	mW	
V_{pp}	524	mV	buffer output
Frequency	456.5	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1	MHz	
Phase Noise	-106.3	dBc/Hz	
FOM	-162.5	dB	
Tuning Range	9.4	%	
K_{vco}	30.5	MHz/V	
VCO core area	3598.9	μm^2

Figure B.1: Calculated and simulated tuning characteristic for the 450MHz ring oscillator with three-stages, $C_{parasitics} = 3.83[\text{fF}]$.

Table B.2: 450MHz Ring Oscillator with Five-Stages - Performance Summary

	Simulated	Units	Comments
V_{DD}	1.8	V	
V_{ctrl}	0.5 - 1.8	V	
R_{DD}	11961.2	Ω	
R_{SS}	444.3	Ω	
No. stages	5		
Varactors	2.5 x 0.18 x 3	$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$	
I_{tail}	153	μA	
Power	1.38	mW	
V_{pp}	684	mV	buffer output
Frequency	453.3	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1	MHz	
Phase Noise	-111.9	dBc/Hz	
FOM	-163.6	dB	
Tuning Range	10.2	%	
K_{vco}	35.5	MHz/V	
VCO core area	5440.2	μm^2

Figure B.2: Calculated and simulated tuning characteristic for the 450MHz ring oscillator with five-stages, $C_{parasitics} = 166.7[\text{aF}]$.

Table B.3: 450MHz Ring Oscillator with Seven-Stages - Performance Summary

	Simulated	Units	Comments
V_{DD}	1.8	V	
V_{ctrl}	0.3 - 1.8	V	
R_{DD}	7251.8	Ω	
R_{SS}	444.3	Ω	
No. stages	7		
Varactors	2.5 x 0.18 x 3	$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$	
I_{tail}	244	μA	
Power	3.069	mW	
V_{pp}	964	mV	buffer output
Frequency	453.1	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1	MHz	
Phase Noise	-114.6	dBc/Hz	
FOM	-162.9	dB	
Tuning Range	10.1	%	
K_{vco}	30.4	MHz/V	
VCO core area	6621.0	μm^2

Figure B.3: Calculated and simulated tuning characteristic for the 450MHz ring oscillator with seven-stages, $C_{parasitics} = 700[\text{aF}]$.

Appendix C

700MHz Ring Oscillator

Table C.1: 700MHz Ring Oscillator with Three-Stages - Performance Summary

	Simulated	Units	Comments
V_{DD}	1.8	V	
V_{ctrl}	0.3 - 1.8	V	
R_{DD}	13183.8	Ω	
R_{SS}	592.4	Ω	
No. stages	3		
Varactors	2.5 x 0.18 x 3	$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$	
I_{tail}	129	μA	
Power	0.699	mW	
V_{pp}	346.4	mV	buffer output
Frequency	702.6	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1	MHz	
Phase Noise	-104.7	dBc/Hz	
FOM	-163.1	dB	
Tuning Range	10.4	%	
K_{vco}	48.5	MHz/V	
VCO core area	3143.9	μm^2

Figure C.1: Calculated and simulated tuning characteristic for the 700MHz ring oscillator with three-stages, $C_{parasitics} = 2.67[\text{fF}]$.

Table C.2: 700MHz Ring Oscillator with Five-Stages - Performance Summary

	Simulated	Units	Comments
V_{DD}	1.8	V	
V_{ctrl}	0.3 - 1.8	V	
R_{DD}	6604.3	Ω	
R_{SS}	444.3	Ω	
No. stages	5		
Varactors	2.5 x 0.18 x 3	$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$	
I_{tail}	258	μA	
Power	2.319	mW	
V_{pp}	656.3	mV	buffer output
Frequency	703.0	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1	MHz	
Phase Noise	-109.7	dBc/Hz	
FOM	-163.0	dB	
Tuning Range	10.2	%	
K_{vco}	48.0	MHz/V	
VCO core area	4716.6	μm^2

Figure C.2: Calculated and simulated tuning characteristic for the 700MHz ring oscillator with five-stages, $C_{parasitics} = 1.3[\text{fF}]$.

Table C.3: 700MHz Ring Oscillator with Seven-Stages - Performance Summary

	Simulated	Units	Comments
V_{DD}	1.8	V	
V_{ctrl}	0.4 - 1.8	V	
R_{DD}	4100.1	Ω	
R_{SS}	444.3	Ω	
No. stages	7		
Varactors	2.5 x 0.18 x 3	$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$	
I_{tail}	390	μA	
Power	4.914	mW	
V_{pp}	896.6	mV	buffer output
Frequency	702.9	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1	MHz	
Phase Noise	-112.6	dBc/Hz	
FOM	-162.3	dB	
Tuning Range	8.7	%	
K_{vco}	43.7	MHz/V	
VCO core area	5840.0	μm^2

Figure C.3: Calculated and simulated tuning characteristic for the 700MHz ring oscillator with seven-stages, $C_{parasitics} = 2[\text{fF}]$.

Appendix D

900MHz Ring Oscillator

Table D.1: 900MHz Ring Oscillator with Three-Stages - Performance Summary

	Simulated	Units	Comments
V_{DD}	1.8	V	
V_{ctrl}	0.4 - 1.8	V	
R_{DD}	8973.3	Ω	
R_{SS}	888.5	Ω	
No. stages	3		
Varactors	2.5 x 0.18 x 3	$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$	
I_{tail}	172	μA	
Power	0.931	mW	
V_{pp}	384.9	mV	buffer output
Frequency	902.9	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1	MHz	
Phase Noise	-103.1	dBc/Hz	
FOM	-162.5	dB	
Tuning Range	9.6	%	
K_{vco}	57.0	MHz/V	
VCO core area	2812.2	μm^2

Figure D.1: Calculated and simulated tuning characteristic for the 900MHz ring oscillator with three-stages, $C_{parasitics} = 4.22[\text{fF}]$.

Table D.2: 900MHz Ring Oscillator with Five-Stages - Performance Summary

	Simulated	Units	Comments
V_{DD}	1.8	V	
V_{ctrl}	0.3 - 1.8	V	
R_{DD}	4628.8	Ω	
R_{SS}	444.3	Ω	
No. stages	5		
Varactors	2.5 x 0.18 x 3	$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$	
I_{tail}	346	μA	
Power	3.112	mW	
V_{pp}	622.0	mV	buffer output
Frequency	902.7	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1	MHz	
Phase Noise	-108.4	dBc/Hz	
FOM	-162.6	dB	
Tuning Range	9.4	%	
K_{vco}	56.4	MHz/V	
VCO core area	4716.6	μm^2

Figure D.2: Calculated and simulated tuning characteristic for the 900MHz ring oscillator with five-stages, $C_{parasitics} = 2.3[\text{fF}]$.

Table D.3: 900MHz Ring Oscillator with Seven-Stages - Performance Summary

	Simulated	Units	Comments
V_{DD}	1.8	V	
V_{ctrl}	0.4 - 1.8	V	
R_{DD}	2881.9	Ω	
R_{SS}	444.3	Ω	
No. stages	7		
Varactors	2.5 x 0.18 x 3	$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$	
I_{tail}	510	μA	
Power	6.428	mW	
V_{pp}	831.1	mV	buffer output
Frequency	903.3	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1	MHz	
Phase Noise	-111.3	dBc/Hz	
FOM	-162.3	dB	
Tuning Range	7.9	%	
K_{vco}	51.2	MHz/V	
VCO core area	5840.0	μm^2

Figure D.3: Calculated and simulated tuning characteristic for the 900MHz ring oscillator with seven-stages, $C_{parasitics} = 2.97[\text{fF}]$.

Appendix E

1800MHz Ring Oscillator

Table E.1: 1800MHz Ring Oscillator with Three-Stages - Performance Summary

	Simulated	Measured	Units	Comments
V_{DD}	1.8		V	
V_{ctrl}	0.3 - 1.8	0.8 - 1.8	V	
R_{DD}	6220.6	4702.7	Ω	tolerance: -24.4%
R_{SS}	99.2	75.0	Ω	tolerance: -24.4%
No. stages	3			
Varactors	2.5 x 0.18 x 1	2.5 x 0.18 x 1		$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$
I_{tail}	283	374	μA	
Power	1.529	2.021	mW	
V_{pp}	188.3	104.4	mV	buffer output
Frequency	1800	1173	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1		MHz	
Phase Noise	-96.8	-95.2	dBc/Hz	meas: single-ended
FOM	-160.0	153.5	dB	
Tuning Range	4.2	3.0	%	
K_{vco}	50.8	35.5	MHz/V	
VCO core area	4233.8		μm^2

Figure E.1: Calculated and simulated tuning characteristic for the 1800MHz ring oscillator with three-stages, $C_{parasitics} = 1.45[\text{fF}]$.

Figure E.2: Calculated tuning characteristic with included effects from R_{DD} and C_{extra} for the 1800MHz ring oscillator with 3 stages and varactor with one finger .

Figure E.3: Measured phase noise for the 1800MHz ring oscillator with three-stages and MOS varactor with one finger .

Table E.2: 1800MHz Ring Oscillator with Three-Stages - Performance Summary

	Simulated	Measured	Units	Comments
V_{DD}	1.8		V	
V_{ctrl}	0.7 - 1.8	0.7 - 1.8	V	
R_{DD}	3743.3	3215.5	Ω	tolerance: -14.1%
R_{SS}	888.5	763.2	Ω	tolerance: -14.1%
No. stages	3			
Varactors	2.5 x 0.18 x 3	2.5 x 0.18 x 3		$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$
I_{tail}	331	385	μA	
Power	1.787	2.080	mW	
V_{pp}	327.6	n/a	mV	buffer output
Frequency	1836	1264	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1		MHz	
Phase Noise	-96.3	-95.1	dBc/Hz	
FOM	-159.1	-154.0	dB	
Tuning Range	6.9	n/a	%	
K_{vco}	113.7	n/a	MHz/V	
VCO core area	2480.4		μm^2

Figure E.4: Calculated and simulated tuning characteristic for the 1800MHz ring oscillator with three-stages and MOS varactor with three fingers, $C_{parasitics} = 6.3[\text{fF}]$.

Figure E.5: Calculated tuning characteristic with included effects from R_{DD} and C_{extra} for the 1800MHz ring oscillator with 3 stages and varactor with three fingers.

Figure E.6: Measured phase noise for the 1800MHz ring oscillator with three-stages and MOS varactor with three fingers.

Table E.3: 1800MHz Ring Oscillator with Five-Stages - Performance Summary

	Simulated	Measured	Units	Comments
V_{DD}	1.8		V	
V_{ctrl}	0.5 - 1.8	0.8 - 1.8	V	
R_{DD}	2576.0	2766.6	Ω	tolerance: +7.4
R_{SS}	99.2	106.5	Ω	tolerance: +7.4
No. stages	5			
Varactors	2.5 x 0.18 x 1	2.5 x 0.18 x 1		$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$
I_{tail}	697	649	μA	
Power	6.275	5.839	mW	
V_{pp}	434.8	204.7	mV	buffer output
Frequency	1804	1092	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1		MHz	
Phase Noise	-101.2	-99.0	dBc/Hz	
FOM	-158.4	-152.1	dB	
Tuning Range	3.4	3.0	%	
K_{vco}	47.6	33.1	MHz/V	
VCO core area	7123.1		μm^2

Figure E.7: Calculated and simulated tuning characteristic for the 1800MHz ring oscillator with five-stages, $C_{parasitics} = 1.75[\text{fF}]$.

Figure E.8: Calculated tuning characteristic with included effects from R_{DD} and C_{extra} for the 1800MHz ring oscillator with five stages and varactor with one finger .

Figure E.9: Measured phase noise for the 1800MHz ring oscillator with five-stages and MOS varactor with one finger .

Table E.4: 1800MHz Ring Oscillator with Seven-Stages - Performance Summary

	Simulated	Measured	Units	Comments
V_{DD}	1.8		V	
V_{ctrl}	0.6 - 1.8	0.8 - 1.8	V	
R_{DD}	1397.7	1877.1	Ω	tolerance: +34.3%
R_{SS}	99.2	133.2	Ω	tolerance: +34.3%
No. stages	7			
Varactors	2.5 x 0.18 x 1	2.5 x 0.18 x 1		$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$
I_{tail}	1.235	919	μA	
Power	15.567	11.585	mW	
V_{pp}	580.9	284.6	mV	buffer output
Frequency	1802	1092	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1		MHz	
Phase Noise	-105.0	-102.8	dBc/Hz	
FOM	-158.2	-152.9	dB	
Tuning Range	2.5	1.7	%	
K_{vco}	37.5	19	MHz/V	
VCO core area	9525.8		μm^2

Figure E.10: Calculated and simulated tuning characteristic for the 1800MHz ring oscillator with seven-stages, $C_{parasitics} = 3.75[\text{fF}]$.

Figure E.11: Calculated tuning characteristic with included effects from R_{DD} and C_{extra} for the 1800MHz ring oscillator with seven stages and varactor with one finger .

Figure E.12: Measured phase noise for the 1800MHz ring oscillator with seven-stages and MOS varactor with one finger .

Appendix F

1900MHz Ring Oscillator

Table F.1: 1900MHz Ring Oscillator with Three-Stages - Performance Summary

	Simulated	Measured	Units	Comments
V_{DD}	1.8		V	
V_{ctrl}	0.3 - 1.8	0.8 - 1.8	V	
R_{DD}	5537.6	4324.8	Ω	tolerance: -21.9%
R_{SS}	99.2	77.5	Ω	tolerance: -21.9%
No. stages	3			
Varactors	2.5 x 0.18 x 1	2.5 x 0.18 x 1		$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$
I_{tail}	311	398	μA	
Power	1.681	2.151	mW	
V_{pp}	195.1	105.8	mV	buffer output
Frequency	1902	1238	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1		MHz	
Phase Noise	-97.3	-93.6	dBc/Hz	
FOM	-160.6	-152.1	dB	
Tuning Range	4.2	2.4	%	
K_{vco}	53.4	30	MHz/V	
VCO core area	4233.8		μm^2

Figure F.1: Calculated and simulated tuning characteristic for the 1900MHz ring oscillator with three-stages and varactor with one finger, $C_{parasitics} = 1.97[\text{fF}]$.

Figure F.2: Calculated tuning characteristic with included effects from R_{DD} and C_{extra} for the 1900MHz ring oscillator with three stages and varactor with one finger .

Figure F.3: Measured phase noise for the 1900MHz ring oscillator with three-stages and MOS varactor with one finger .

Table F.2: 1900MHz Ring Oscillator with Three-Stages - Performance Summary

	Simulated	Measured	Units	Comments
V_{DD}	1.8		V	
V_{ctrl}	0.8 - 1.8	0.8 - 1.8	V	
R_{DD}	3533.2	3035.0	Ω	tolerance: -14.1
R_{SS}	888.5	763.2	Ω	tolerance: -14.1
No. stages	3			
Varactors	2.5 x 0.18 x 3	2.5 x 0.18 x 3		$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$
I_{tail}	344	400	μA	
Power	1.875	2.161	mW	
V_{pp}	320.7	n/a	mV	buffer output
Frequency	1925	1313	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1		MHz	
Phase Noise	-95.9	-92.6	dBc/Hz	
FOM	-158.9	-151.6	dB	
Tuning Range	6.6	n/a	%	
K_{vco}	124.5	n/a	MHz/V	
VCO core area	2480.4		μm^2

Figure F.4: Calculated and simulated tuning characteristic for the 1900MHz ring oscillator with three-stages and MOS varactor with three fingers, $C_{parasitics} = 6.5[\text{fF}]$.

Figure F.5: Calculated tuning characteristic with included effects from R_{DD} and C_{extra} for the 1900MHz ring oscillator with 3 stages and varactor with 3 fingers.

Figure F.6: Measured phase noise for the 1900MHz ring oscillator with three-stages and MOS varactor with three fingers.

Table F.3: 1900MHz Ring Oscillator with Five-Stages - Performance Summary

	Simulated	Measured	Units	Comments
V_{DD}	1.8		V	
V_{ctrl}	0.5 - 1.8	0.8 - 1.8	V	
R_{DD}	2387.0	2802.3	Ω	tolerance: +17.4%
R_{SS}	99.2	116.5	Ω	tolerance: +17.4%
No. stages	5			
Varactors	2.5 x 0.18 x 1	2.5 x 0.18 x 1		$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$
I_{tail}	762	649	μA	
Power	6.855	5.841	mW	
V_{pp}	434.2	227	mV	buffer output
Frequency	1899	1138	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1		MHz	
Phase Noise	-101.3	-96.4	dBc/Hz	
FOM	-158.5	-149.9	dB	
Tuning Range	3.3	2.5	%	
K_{vco}	49.0	28	MHz/V	
VCO core area	7123.1		μm^2

Figure F.7: Calculated and simulated tuning characteristic for the 1900MHz ring oscillator with five-stages, $C_{parasitics} = 2.05[\text{fF}]$.

Figure F.8: Calculated tuning characteristic with included effects from R_{DD} and C_{extra} for the 1900MHz ring oscillator with five stages and varactor with one finger.

Figure F.9: Measured phase noise for the 1900MHz ring oscillator with five-stages and MOS varactor with one finger.

Table F.4: 1900MHz Ring Oscillator with Seven-Stages - Performance Summary

	Simulated	Measured	Units	Comments
V_{DD}	1.8		V	
V_{ctrl}	0.6 - 1.8	0.8 - 1.8	V	
R_{DD}	1288.9	1733.5	Ω	tolerance: +34.5%
R_{SS}	99.2	133.4	Ω	tolerance: +34.5%
No. stages	7			
Varactors	2.5 x 0.18 x 1	2.5 x 0.18 x 1		$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$
I_{tail}	1.314	977	μA	
Power	16.562	12.306	mW	
V_{pp}	613.9	281	mV	buffer output
Frequency	1900	1132	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1		MHz	
Phase Noise	-104.7	-100.2	dBc/Hz	
FOM	-158.0	-150.4	dB	
Tuning Range	2.4	2.2	%	
K_{vco}	40.8	25	MHz/V	
VCO core area	9555.2		μm^2

Figure F.10: Calculated and simulated tuning characteristic for the 1900MHz ring oscillator with seven-stages, $C_{parasitics} = 4.05[\text{fF}]$.

Figure F.11: Calculated tuning characteristic with included effects from R_{DD} and C_{extra} for the 1900MHz ring oscillator with seven stages and varactor with one finger .

Figure F.12: Measured phase noise for the 1900MHz ring oscillator with seven-stages and MOS varactor with one finger .

Appendix G

2400MHz Ring Oscillator

Table G.1: 2400MHz Ring Oscillator with Three-Stages - Performance Summary

	Simulated	Measured	Units	Comments
V_{DD}	1.8		V	
V_{ctrl}	0.9 - 1.8	0.9 - 1.8	V	
R_{DD}	2684.5	2306.0	Ω	tolerance: -14.1%
R_{SS}	888.5	763.2	Ω	tolerance: -14.1%
No. stages	3			
Varactors	2.5 x 0.18 x 3	2.5 x 0.18 x 3		$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$
I_{tail}	413	481	μA	
Power	2.228	2.595	mW	
V_{pp}	279.1	n/a	mV	buffer output
Frequency	2430	1679	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1		MHz	
Phase Noise	-94.1	-91.6	dBc/Hz	
FOM	-158.3	-152	dB	
Tuning Range	4.8	n/a	%	
K_{vco}	129.2	n/a	MHz/V	
VCO core area	2480.4		μm^2

Figure G.1: Calculated and simulated tuning characteristic for the 2400MHz ring oscillator with three-stages and MOS varactor with three fingers, $C_{parasitics} = 6.6[\text{fF}]$.

Figure G.2: Calculated tuning characteristic with included effects from R_{DD} and C_{extra} for the 2400MHz ring oscillator with 3 stages and varactor with 3 fingers.

Figure G.3: Measured phase noise for the 2400MHz ring oscillator with three-stages and MOS varactor with three fingers.

Table G.2: 2400MHz Ring Oscillator with Five-Stages - Performance Summary

	Simulated	Measured	Units	Comments
V_{DD}	1.8		V	
V_{ctrl}	0.8 - 1.8	0.8 - 1.8	V	
R_{DD}	1680.9	2085.9	Ω	tolerance: +24.1%
R_{SS}	99.2	123.1	Ω	tolerance: +24.1%
No. stages	5			
Varactors	2.5 x 0.18 x 1	2.5 x 0.18 x 1		$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$
I_{tail}	1.049	845	μA	
Power	9.444	7.605	mW	
V_{pp}	423.3	252.3	mV	buffer output
Frequency	2400	1383	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1		MHz	
Phase Noise	-100.4	-99.9	dBc/Hz	
FOM	-158.2	-153.9	dB	
Tuning Range	2.9	2.5	%	
K_{vco}	64.3	34.5	MHz/V	
VCO core area	7123.1		μm^2

Figure G.4: Calculated and simulated tuning characteristic for the 2400MHz ring oscillator with five-stages, $C_{parasitics} = 3.1[\text{fF}]$.

Figure G.5: Calculated tuning characteristic with included effects from R_{DD} and C_{extra} for the 2400MHz ring oscillator with five stages and varactor with one finger .

Figure G.6: Measured phase noise for the 2400MHz ring oscillator with five-stages and MOS varactor with one finger .

Table G.3: 2400MHz Ring Oscillator with Seven-Stages - Performance Summary

	Simulated	Measured	Units	Comments
V_{DD}	1.8		V	
V_{ctrl}	0.8 - 1.8	0.8 - 1.8	V	
R_{DD}	899.2	1147.0	Ω	tolerance: +27.6%
R_{SS}	99.2	126.6	Ω	tolerance: +27.6%
No. stages	7			
Varactors	2.5 x 0.18 x 1	2.5 x 0.18 x 1		$\mu\text{m} \times \mu\text{m} \times \text{Fingers}$
I_{tail}	1.702	1.334	μA	
Power	21.443	16.809	mW	
V_{pp}	554.5	313.4	mV	buffer output
Frequency	2401	1608	MHz	$V_{ctrl} = 1[\text{V}]$
Offset	1		MHz	
Phase Noise	-103.0	-103.3	dBc/Hz	
FOM	-157.3	-155.2	dB	
Tuning Range	2.0	2.2	%	
K_{vco}	47.5	36	MHz/V	
VCO core area	9902.1		μm^2

Figure G.7: Calculated and simulated tuning characteristic for the 2400MHz ring oscillator with seven-stages, $C_{parasitics} = 5.45[\text{fF}]$.

Figure G.8: Calculated tuning characteristic with included effects from R_{DD} and C_{extra} for the 2400MHz ring oscillator with seven stages and varactor with one finger .

Figure G.9: Measured phase noise for the 2400MHz ring oscillator with seven-stages and MOS varactor with one finger .

Appendix H

Multi-Band Ring Oscillator

Figure H.1: Measured VCO output in time domain, $V_{DD}=1.8[V]$ $V_{ctrl}=1[V]$, and $V_{freq_band}=0.77[V]$.

Figure H.2: Measured VCO output in time domain, $V_{DD}=1.8[V]$ $V_{ctrl}=1[V]$, and $V_{freq_band}=0.84[V]$.

Figure H.3: Measured VCO output in time domain, $V_{DD}=1.8[V]$ $V_{ctrl}=1[V]$, and $V_{freq.band}=0.87[V]$.

Figure H.4: Measured VCO output in time domain, $V_{DD}=1.8[V]$ $V_{ctrl}=1[V]$, and $V_{freq.band}=0.875[V]$.

Figure H.5: Measured VCO output in time domain, $V_{DD}=1.8[V]$ $V_{ctrl}=1[V]$, and $V_{freq_band}=0.99[V]$.

Figure H.6: Measured VCO output in time domain, $V_{DD}=1.8[V]$ $V_{ctrl}=1[V]$, and $V_{freq_band}=1.04[V]$.

Figure H.7: Measured VCO output in time domain, $V_{DD}=1.8[V]$ $V_{ctrl}=1[V]$, and $V_{freq.band}=1.12[V]$.

Appendix I

Layout and Photographs

Figure I.1: Layout of the varactor with one finger .

Figure I.2: Die photograph of the test structure for varactor with one-stage .

Figure I.3: Layout of the varactor with three fingers.

Figure I.4: Die photograph of the test structure for varactor with three-stages.

Figure I.5: Die photograph of the three-stage ring oscillator .

Figure I.6: Layout of the three-stage ring oscillator designed with varactor with one finger .

Figure I.7: Layout of the three-stage ring oscillator designed with varactor with three fingers.

Figure I.8: Die photograph of the five-stage ring oscillator.

Figure I.9: Layout of the five-stage ring oscillator designed with varactor with one finger .

Figure I.10: Layout of the five-stage ring oscillator designed with varactor with three fingers .

Figure I.11: Die photograph of the seven-stage ring oscillator .

Figure I.12: Layout of the seven-stage ring oscillator designed with varactor with one finger .

Figure I.13: Layout of the seven-stage ring oscillator designed with varactor with three fingers.

Figure I.14: Die photograph of the three-stage ring oscillators that share same probe pads.

Figure I.15: Die photograph of the five-stage ring oscillators that share same probe pads.

Figure I.16: Die photograph of the three-stage multi-band VCO.

Figure I.17: Test structure used for measuring the ring oscillators.

Figure I.18: Testing in the copper cage at the Carleton University, Ottawa CANADA . Sinisa Milicevic is pressing the Agilent E4440A PSA serial spectrum analyzer to measure the phase noise of one fabricated ring oscillator .

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