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**GaAs Monolithic Microwave
Frequency Halver and Phase Detector for
use in a Phase Locked Oscillator**

by

SHAWN STAPLETON

A Thesis submitted to the Faculty of Graduate Studies and
Research in partial fulfillment of the requirements of the
degree of

DOCTOR OF PHILOSOPHY

Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada

June 1987

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**GaAs Monolithic Microwave
Frequency Halver and Phase Detector for
use in a Phase Locked Oscillator**

submitted by Shawn Stapleton, BSc. Eng., M.Eng., in partial
fulfillment of the requirements for the degree of Doctor of
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ABSTRACT

GaAs Monolithic Microwave Integrated Circuits (MMICs) are rapidly replacing existing technology due to their advantages in size, weight, cost and reliability. Many of the basic MMIC components (mixers, amplifiers, attenuators, etc.) are presently being used. However, MMIC oscillators are being rejected in many applications, primarily because of their inherently poor noise characteristics.

A technique for improving the noise characteristics of MMIC oscillators by use of phase locking is reported in this thesis. Four configurations for phase locking a noisy oscillator to a clean reference are introduced as viable solutions. These different phase locking configurations are comprised of mixers, oscillators, multipliers, frequency dividers, loop filters and phase detectors. Of these components, only the frequency divider and phase detector have no current realization in MMICs.

This thesis presents novel circuit configurations in MMIC form for a frequency halver and phase detector. Both of these circuits are theoretically analyzed in great detail and their operating criteria revealed.

An approximate algebraic method, based on the solution of a nonlinear differential equation, is used to obtain the steady state operation of the frequency halver. In the case of the phase detector, the analysis is based on the Ritz Method.

The novel circuits for the frequency halver and the phase detector are designed, fabricated and measured. Their performance is then evaluated and compared with their theoretical predictions.

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LIST OF SYMBOLS

<u>SYMBOL</u>	<u>FREQUENCY HALVER</u>
Q	Quality factor
R_s	Series resistance
R_L	Load resistance
v_p	Instantaneous pumping voltage
ω_0	Small-signal subharmonic resonance frequency
A	Junction area
e	Charge on an electron
ϵ	Permittivity of semiconductor material
ϕ_0	Thermal equilibrium built-in potential
v_r	Total reverse voltage across the junction
N_D	Donor concentration on n-side
ω	Angular frequency $2\pi F$
L	Inductance
C_F	FET feedback capacitance
$C_g(v_i)$	FET gate to source capacitance as a function of voltage v_i
g_b	FET drain to source conductance
g_m	FET transconductance
v_1, v_2	Instantaneous junction voltages on varactors 1 and 2
v_{01}, v_{02}	Instantaneous voltages at FET's output terminals
i_{fd}, i_{22}	Instantaneous current through the feedback capacitance
i_L	Instantaneous current through the load resistor
$d()/dt$	Derivative with respect to time t
v_Q, v_R	Instantaneous voltage at the fundamental frequency
v_s, v_o	Instantaneous voltage at half the fundamental frequency

V_{GS}	Gate to source d.c. voltage
V_{DS}	Drain to source d.c. voltage
V_{Tg}	$\phi_0 + V_{GS}$
$(^\circ)$	Derivative with respect to normalized time τ
$(^\circ\circ)$	Second derivative w.r.t. normalized time τ
$=$	Equals by definition
ω_p	$1/\sqrt{LC_g(V_{gs})}$
ω_R	$1/\sqrt{LC_F}$
Q_p	$1/\omega_p C_g(V_{gs}) R_s$
β	ω_p/ω_R
γ	$\omega C_F I_p$
χ	ω/ω_p
X	Normalized instantaneous pumping voltage
S, Y	Normalized instantaneous voltage at the subharmonic frequency
Q, R	Normalized instantaneous voltage at the fundamental frequency
τ	Normalized time = $\omega_p t$ [24]
α_1	$2g_L + g_0$
α_2	g_m
α_3	g_0
α	$\frac{1}{2}e^{j(\nu\tau + \Psi)}$ [24]
θ	Phase angle of $X(o)$
ϕ	Phase angle of $Q(o)$
ψ	Phase angle of $S(o)$
S	Siemens

SYMBOLPHASE DETECTOR

ϕ_o	Built in potential of junction capacitance
$C_{gs}(V_{gs})$	Gate to source varactor capacitance
V_{gs}	Total forward voltage between the gate and source
I_{ds}	Total drain to source current
V_{ds}	Total forward voltage between the drain and source
V_T	Threshold voltage
λ	Channel length modulation parameter
α	Hyperbolic tangent function parameter
C	Junction depletion capacitance at zero bias
β	Transconductance parameter
$v_{1,2,3}$	Instantaneous sinusoidal small signal voltages
$V_{1,2,3}$	Direct current signals
R_L	Load resistance
V_d	Drain DC voltage
v_{3s}, v_{3c}	Sine and Cosine voltage amplitude terms
X_o, Y_o, Z_o	Normalized direct current signals
X, Y	Normalized sinusoidal small signals
Z_s, Z_c	Normalized sine and cosine amplitude terms
D	Normalized drain D.C. voltage
K	Normalized threshold voltage
β_o	Normalized transconductance parameter
α_o	Normalized hyperbolic tangent function parameter
C_o	Normalized junction depletion capacitance at zero bias
g_L	Normalized output transconductance
$(^\circ)$	Derivative with respect to normalized time τ
X', Y', Z'	Total normalized voltages
λ_o	Normalized channel length modulation parameter
$\xi()$	Ritz equation
ω	Frequency of sinusoidal signal

$\int$	Integration symbol
A_o	$2B_o/\omega C_o$
B_o	$X_o - Z_o$
C'_o	$Y_o - K$
D_o	$D - Z_o$
J	$A_o^2(1 - B_o)(B_o - K)^2$
I_o	$1 + \lambda_o D_o + 2\lambda_o(B_o - K)$
ΔZ	Normalized D.C. variation as a function of phase difference
ϕ	Phase difference between the two input signals
$\sqrt{\quad}$	Square root function
$ $	Absolute value
$d(\quad)/dX_o$	Differential with respect to X_o

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CHAPTER 1

INTRODUCTION

1.1 General

The growth of high quality gallium arsenide (GaAs) in the early 1970's together with developments in computer aided design (CAD) has led to the realistic possibility of producing monolithic microwave integrated circuits. The birth of the analogue Monolithic Microwave Integrated Circuits (MMICs) industry was launched by the realization of the first successful GaAs MMIC in 1976 [1].

The term monolithic is used to identify an approach wherein all active and passive circuit elements or components and interconnections are formed into or on to the surface of a semi-insulating substrate. Deposition schemes such as epitaxy, ion implantation, sputtering, evaporation, diffusion, or a combination of these processes and others are used to fabricate MMICs.

Some promising attributes for designing and fabricating a microwave monolithic circuit include:

1. Low cost
2. Improved reliability and reproducibility
3. Small size and weight

4. Multioctave (broad-band) performance
5. Circuit design flexibility and multifunction performance on a chip.

The low cost attribute of MMICs is realized when systems applications based on a large number of identical components are considered. A current example is the design of space-borne phased-array radars planned for the near future, which require lightweight and reliable, low cost transmit-receive modules [2].

Improved reliability and reproducibility derives in part from the fact that wire bonding is eliminated in MMICs, at least within the chip itself, and is relegated to less critical and fewer locations at the periphery of the chip.

Small size and volume, and their corollary, light weight, are intrinsic properties of the monolithic approach. Small size allows batch processing of hundreds of circuits per wafer of substrate. Since the essence of batch processing is that the cost of fabrication is determined by the cost of processing the entire wafer, it follows that the processing cost per chip is proportional to the area of the chip.

The reduction of wire bonds eliminates many of the undesired parasitics which limit the broad-band performance of circuits employing packaged discrete devices.

The small circuit size intrinsic to the monolithic approach allows circuit integration on a chip level. These circuits range from the lowest degree of complexity such as an oscillator, mixer, or amplifier, to a higher "functional block" level, for example a receiver front end.

MMICs have been realized for frequencies in excess of 80 GHz [3], with bandwidths exceeding 30 GHz for circuit functions which would not have been possible using conventional hybrid technologies. The range of analogue circuits which have been designed and fabricated as GaAs integrated circuits includes both small-signal and power amplifiers, phase shifters, mixers, switches and multi-function circuits [4].

Many of these basic MMIC components are presently being used. However, MMIC oscillators are being avoided in many applications, primarily because of their inherently poor noise characteristics.

The noise characteristics of an oscillator are controlled by the resonant loop, which for MMICs, is generally a passive inductor-capacitor combination. The quality factor "Q" of a resonant loop is inversely proportional to the oscillator's phase noise [5]. Passive MMIC

components are very lossy because of the small cross sectional areas of the transmission lines used in their representation. The Q of an MMIC oscillator resonator is typically less than 20, and this is generally unacceptable for oscillator applications.

A technique for improving the noise characteristics of MMIC oscillators by means of phase locking is reviewed in this thesis. Four configurations for phase locking a noisy oscillator to a clean reference source are shown as viable noise reducing solutions. These different phase locking configurations are composed of mixers, oscillators, multipliers, frequency dividers, loop filters and phase detectors. Of these components, only the frequency divider and phase detector have not been thoroughly investigated in MMIC form.

This thesis presents novel MMIC configurations for a phase detector and a frequency halver. Both of these circuits are theoretically analyzed in great detail and their operating criteria revealed.

An approximate algebraic method, based on the solution of a nonlinear differential equation, is used to obtain the steady-state operation of the frequency halver. In the case of the phase detector, the analysis is based on the Ritz Method. These two theoretical techniques for analyzing nonlinear circuits are subsets of the more familiar Fourier analysis.

The novel circuits for the frequency halver and the phase detector are designed, fabricated and measured. Their performance is then evaluated and compared with theoretical predictions.

1.2 Thesis Objectives

The research reported in this thesis relates to the following investigations:

- a) A search for practical component implementations for a monolithic microwave phase locked oscillator (PLO).
- b) The development of the theoretical understanding of a frequency halver for a PLO.
- c) The development of a theoretical understanding of a phase detector for a PLO.
- d) The experimental design, development and evaluation of a monolithic microwave integrated frequency halver and phase detector.

1.3 Thesis Organization

Chapter 1 is an introductory chapter describing the advantages of the monolithic microwave medium together with a discussion of the dilemma of developing MMIC oscillators. The concept of phase locking is introduced as a possible practical solution, and the necessity for a phase detector and frequency halver is explained.

Chapter 2 describes the methods by which monolithic microwave integrated circuits are fabricated. A description is given for the implementation of the active and passive components used in a MMIC design. The design methodology employed is laid out in a systematic step-by-step procedure, and an underlying consideration of wafer yield is introduced.

In Chapter 3, some possible configurations of a phase locked oscillator are presented together with an identification of the required system components. The requirements of each individual building block of the different phase-locked oscillator scenarios are discussed at length. Also the least understood components, the phase detector and the frequency halver are singled out for further investigation.

In Chapter 4, the frequency halver is modelled and theoretically investigated. An analytical solution for the steady state response is described in detail.

In Chapter 5, the phase detector is modelled and theoretically investigated. An analytical solution based on the individual characteristics of the phase detector's FETs is presented. Optimization of the bias voltages to maximize the phase detector sensitivity is derived.

Chapter 6 describes the laboratory measurements carried out to confirm the theory developed for the frequency halver and the phase detector. The results of the measurements are compared with theory and conclusions are drawn regarding the accuracy of the models.

In Chapter 7, a summary of the achievements is presented and recommendations for further research are given.

CHAPTER 2

GaAs, MONOLITHIC MICROWAVE INTEGRATED CIRCUITS

2.1 Processing Techniques

Monolithic microwave integrated circuits (MMICs) are complete electrical circuits fabricated on a single chip. In addition to the active devices (FETs and diodes), these circuits generally include capacitors, inductors, and resistors. The ability to fabricate MMICs (and realize the advantage of size, ruggedness, reproducibility, and cost) requires that methods exist to fabricate required passive components. Economic considerations dictate that the MMIC chip size be minimized as much as possible in order to maximize the number of chips on a slice. The passive components, especially inductive elements, tend to utilize most of the chip area, whereas the area occupied by the active devices is relatively small. The next section deals with circuit fabrication on a GaAs substrate.

2.1.1 Integrated Circuit Technology

A cornerstone of the monolithic approach is the availability of a highly reproducible device technology.

This in turn is related, in part, to the control of the starting material, especially the active (semiconducting) layer.

Two general techniques are available for forming an active layer on GaAs substrates; namely, epitaxy and ion implantation [6,7].

In the epitaxy approach, a doped single crystal semiconducting layer is deposited on a semi-insulating GaAs substrate. Usually an intervening high-resistivity epitaxial "buffer" layer is used to screen out diffusion of impurities from the substrate during the active layer growth.

Using ion implantation, dopant atoms are implanted directly into the surface of a semi-insulating GaAs substrate. Ion implantation requires a higher crystal quality of the substrate. Epitaxy does not have the control or flexibility associated with implantation. With implantation, more uniform conducting layers are possible over a larger area; more uniform in doping level as well as in thickness. Furthermore, with implantation, selective doping is possible [8]. This is the formation of different doping profiles in different parts of the wafer. In addition a higher uniformity of device characteristics is achievable with implantation.

The processing technology used for FET fabrication is also applicable to the monolithic passive circuit elements. The high degree of dimensional definition associated with FET photolithography is more than adequate for the circuit elements.

Many laboratories developing GaAs ICs have already considerable experience in the fabrication of discrete FETs, thus there tends to be a marked resemblance between the two fabrication processes particularly where epitaxial layers are used. A brief discussion of the planar ion-implanted process technology will follow.

Figure 2.1 shows the process steps for one of the many possible techniques to fabricate a planar GaAs IC incorporating a FET, a level shifter and a switching Schottky diode. Fabrication of the GaAs IC wafer is initiated by the deposition of a Si_3N_4 (silicon nitride) layer on to the semi-insulating GaAs substrate. The first photoresist stage defines the device and circuit areas which require low dose implants, such as the channels of FETs. A shallow Se implant [Figure 2.1(a)] is then followed by a exposure of the photoresist and deeper n^+ implant [Figure 2.1(b)] for device contact areas, or Schottky barrier switching diodes. The implantation steps are followed by

Planar GaAs IC fabrication steps

Insulator deposition and masking for N- implant

N- Implant

Encapsulation and anneal

Ohmic contact metallisation

Schottky barrier and interconnect metallisation

Second layer metallisation

Cutaway view of a planar GaAs circuit fabrication with two localised implants.

Fig. 2.1. Planar GaAs Circuit Fabrication Process adopted by Rockwell. This uses Ion Implantation Directly into Qualified Semi-Insulating Substrate Material.[9]

encapsulation of the slice with Si_3N_4 and high temperature annealing. This annealing converts the shallow n-Se-implanted areas into the FET active channel layers [9]. Device ohmic contacts are defined next with a standard photoresist and lift-off technique [Figure 2.1(d)].

After alloying the ohmic contact areas, a photoresist operation is again performed to define the Schottky barrier metallization for the FETs and diodes. Rockwell uses Ti-Pt-Au for the Schottky barriers as well as for the first layer circuit interconnections [Fig. 2.1(e)]. A dielectric layer is then deposited on to the entire wafer, as insulation for the second layer interconnection and dielectric for circuit capacitors. Fig. 2.1(g) shows a cross-sectional view of the complete process where the interconnects can be clearly seen. The following section discusses the different FET fabrication techniques.

2.1.2 FET Fabrication Techniques

The two techniques used for GaAs MESFET (Metal Semiconductor Field Effect Transistor) fabrication which have gained the most popularity are the self-aligned and the etched-channel technologies [10,11]. Both techniques can exploit either optical or electron beam lithography to

define the gate stripe, depending on the transistor's gate length. Electron beam lithography is generally used for gate lengths of less than $.5 \mu\text{m}$. A discussion of the two different FET fabrication techniques is given below.

Self-Aligned Gate

Fig. 2.2 shows the basic processing steps of the self-aligned gate technology. In the first step, the isolation mesa is defined by etching away the active n-layer until the semi-insulating substrate is reached. The gate metal is then evaporated over the active area as shown in Fig. 2.2(a). Source and drain areas are defined in photoresist, and the exposed gate metal is removed by etching. Over-etching is used to undercut the resist as shown in Fig. 2.2(b), to allow the necessary space between gate to drain, and gate to source. Gold ohmic contact metal is then evaporated [Fig. 2.2(c)]. The resist which is protecting the gate strip is covered with this ohmic metal, but the metal is conveniently removed by dissolving away the resist and "floating off" the gold. Thus the remaining thin gate is left situated between source and drain contacts, as shown in Fig. 2.2(d).

Recessed Channel Technology

In this technology, the active channel thickness is defined by the height of the n-type epitaxial layer, a thicker layer is grown, and the channel region under the gate is defined by etching. This removes the higher tolerance in thickness required for the epitaxial layer, when the channel region is not etched. Source and drain contacts are deposited first, as shown in Fig. 2.3(a), and the gate is defined in photoresist. A channel is etched in the GaAs until a specific current is measured between the source and drain contacts. Gate metal is then evaporated and the excess metal [Fig. 2.3(c)] removed by using the "float-off" technique. This basic method works equally well with both photolithographic and electron beam resist exposure techniques. Gate lengths as short as $.25 \mu\text{m}$ can be produced.

The recessed channel technology can significantly improve the small signal performance GaAs FET [12]. Such a recess can decrease the source resistance of the device and thereby improve the noise figure and associated gain. The next section discusses the fabrication of the MMIC capacitors.

Fig. 2.2. Processing Steps of Self-Aligned Gate Technology. [4]

Fig. 2.3. Processing Steps of Etched-Channel Technology. [4]

2.1.3 Capacitor Technology

Capacitors fabricated as part of an MMIC are referred to as monolithic capacitors. They are used in MMICs for blocking, bypassing, or tuning purposes. There are four basic MMIC capacitor configurations. These are: a stub in a transmission line [Fig. 2.4(a)]; coupled lines, usually formed as an interdigital capacitor [Fig. 2.4(b)]; a metal-insulator-metal (MIM) capacitor [Fig. 2.4(c)] and a Schottky diode.

Schottky diodes on GaAs have a capacitance that is a function of diode area, GaAs doping profile, and applied voltage. The voltage dependence makes these structures unsuitable for use in most analog MMIC applications.

A stub in a microstrip transmission line can act as a capacitor or an inductor. An open stub, less than a quarter wavelength in length, is capacitive. A shorted stub, less than a quarter wavelength, is inductive. Such stubs are distributed elements and require substantial chip area at lower frequencies.

The more popular MMIC capacitors are the interdigital and the metal-insulator-metal types. These two types of MMIC capacitors will now be described in detail.

Interdigital Capacitors

The capacitance of interdigital capacitors arises from coupling between adjacent conductors, aided by the substrate dielectric. They are useful principally for capacitances of 1 pF or less. Larger values require significant chip area and involve distributed effects. They are not a pure, series capacitance, but have associated inductance, resistance, and shunt capacitance. Fig. 2.5 shows an equivalent circuit used for modelling interdigital structures [13,14].

The capacitance, C , is the interelectrode capacitance. The capacitance C can be calculated using [13]

$$C = (N_F - 1) C_g L \quad 2.1$$

where N_F is the number of fingers, L is the finger length and C_g is the static gap capacitance per unit length. The unloaded Q of these capacitors is typically in the range of 35 to 50, at 12-14 GHz. The losses associated with the current crowding near the conductor edges prevent obtaining significantly greater Q values. The major fabrication consideration, for interdigital capacitors, is to accurately achieve the design size and spacing of the conductors.

Fig. 2.4. Three implementations of capacitors on MMICs: (a) a stub in microstrip transmission line; (b) an interdigitated capacitor; (c) a metal-insulator-metal (MIM) capacitor.

Fig. 2.5. Equivalent circuit of an interdigitated series capacitor. The shunt capacitance is to the backside ground plane.

Metal-Insulator-Metal Capacitors

The most popular type of capacitor for MMICs is the MIM configuration shown in Fig. 2.4(c). This thin-film capacitor is composed of two metal plates separated by a dielectric material. The dielectric is typically 0.1 to 0.4 μm thick.

Because these MIM structures are parallel plate capacitors, their capacitance, to the first order, is given by the standard expression:

$$C_0 = \epsilon A/d \quad 2.2$$

where C_0 is the parallel plate capacitance, ϵ is the permittivity, A is the area of the top plate, and d is the distance between plates. For commonly used dielectrics and typical thicknesses, this capacitance is typically in the range of 50 pF/mm² to 600 pF/mm². However, these series capacitors, C , also have other parasitic components (resistive, R_p , G_p , inductive, L_p , and shunt capacitive, C_p), as illustrated in the equivalent circuit in Fig. 2.6. [14].

At 10 GHz, the Q of a large MIM capacitor (≈ 10 pF) can be 10 or even less, while the Q of a small MIM capacitor (≈ 1 pF) can exceed 100. The losses are either dielectric losses or conductive losses [14]. The most common choice for the capacitor's dielectric is silicon nitride or silicon dioxide. These are often used in the encapsulation process, so it is natural to use them for capacitor dielectrics also.

The yield of working capacitors on a slice is an important issue. Some MMICs make liberal use of capacitors, however one pinhole, which ruins one capacitor, also ruins the entire chip. Consider a complex MMIC which has ten reasonably large MIM capacitors, if the fabrication yield per capacitor is 95%, this would produce a chip yield of $.95^{10} = 60\%$, due to capacitors. Hence the capacitor yield must be very high.

Another important passive circuit component is the MMIC inductor, which is described in the next section.

Fig. 2.6. Equivalent circuit of a metal-insulator-metal (MIM) series capacitor [14].

2.1.4 Inductor Technology

Inductors are necessary elements in MMICs, where they function as part of tuned circuits. They are either lumped or distributed [15]. The distributed forms are treated as transmission lines. Inductor values, on GaAs MMICs are usually between 0.5 and 20 nH. Smaller inductors are achieved using short transmission lines.

Lumped Inductors

Fig. 2.7 illustrates several types of lumped inductors. These are lengths of metal lines that have mutual inductance between segments, because of electromagnetic interactions. These monolithic lumped inductors are described in several references [4,16,17]. Their small size makes modelling difficult, although some accurate equations have been developed [16]. Rectangular spiral inductors are treated in reference [16], and circular spiral inductors in reference [17]. Although these inductors are usually placed directly on the substrate, an air bridge spiral inductor has been used [18], in which most of the inductor length is elevated above the semi-insulating surface. The Q's of lumped inductors tend to be near 50 at 10 GHz, longer inductors having smaller Q's.

Fig. 2.7. Lumped inductor configurations.

Distributed Inductors

As noted above, lumped-element inductors are difficult to model accurately. It is generally preferable to form the inductors as transmission lines fabricated on the GaAs substrate. Although they function essentially as inductors, their treatment as transmission lines in computer aided design (CAD) modelling programs, does not accurately account for associated capacitance, mutual couplings, and discontinuities, where they join other metals.

For MMIC purposes, these transmission lines are almost always microstrip although coplanar transmission lines have been used [19,20]. Both are shown in Fig. 2.8. The transmission line impedance of the coplanar configuration depends on the dimensions of the centre strip, the spacing to the lateral ground planes, and the dielectric constant of the substrate material. Coplanar lines have two disadvantages. First, they occupy more space than microstrip lines because of the lateral ground planes. Second, a pure coplanar mode is difficult to obtain. Microstrip is the most popular choice for transmission lines. The impedance of the line is determined by the ratio of the conductor width to the substrate thickness, the dielectric constant of the substrate, and some secondary factors [21]. Losses in microwave transmission lines are dielectric, conductive, magnetic, and radiative losses. The transmission lines must

be sufficiently thick to carry the required current, without significant ohmic losses. This means that the metal should be at least two skin depths thick [21]. This, of course, applies for RF currents. If DC currents are present, then the cross section must be sufficient to support the current density. Another passive MMIC component is the resistor, which is discussed next.

Fig. 2.8. Two basic types of transmission lines used on MMICs: (a) coplanar; (b) microstrip.

2.1.5 Resistor Technology

Resistors are used in MMICs for several purposes, including feedback, isolation, self-biasing, terminations, and voltage dividers in bias networks [22]. Resistors on MMICs are divided here into two classes: those fabricated using the GaAs material, and thin-film resistors.

GaAs Resistors

The simplest way to fabricate a resistor on the GaAs slice is to use the resistivity of the GaAs itself. This approach requires no extra process steps, because the two

major steps, isolation and formation of ohmic contacts, must already be performed. Such a resistor is shown in Fig. 2.9. The resistance consists of both the resistance of the GaAs material, and the resistance of the two ohmic contacts. The resistance is given by [23]

$$R = R_s \frac{L}{W} + \frac{2R_c}{W} \quad 2.3$$

where R_s is the sheet resistance of the GaAs (ohms/square), L is the distance between the ohmic contacts, W is the width of the resistor, and R_c is the contact resistance for a unit length (ohm-mm). Typical values of sheet resistance are 300 to 450 ohms/square, and contact resistance is around .25 ohm-mm.

GaAs resistors have several potential problems; current saturation, Gunn domain formation, and temperature coefficient [24]. The temperature coefficient is the most serious disadvantage. The temperature coefficient is both large and positive, and thus can produce significant resistance changes over temperature [4].

Fig. 2.9. MMIC resistor composed of active GaAs material: (a) defined by mesa etching; (b) defined by implant isolation or selective implantation [4].

Thin-film Resistors

The use of GaAs material as resistance has several disadvantages. It is therefore useful to consider other thin-film materials to provide resistance. These must, of course, be compatible with GaAs processing. Materials that have been used for this purpose are listed in Table 2.1.

Resistors, other than GaAs resistors, generally require at least one additional masking level to define the pattern (GaAs resistors can be fabricated using the existing isolation and ohmic contact masks).

Having described all the MMIC components, the design methodology will now be explained.

TABLE 2.1

Material for Use as Thin Film Resistors [4]

<u>Material</u>	<u>Resistivity</u> ($\mu\text{ohm-cm}$)	<u>TCR</u> (ppm)
Cr	13 (bulk)	3000
Ti	55-135 (43 bulk)	2500
Ta	180-220 (13 bulk)	-100 to +500
TaN	280	-180 to -300
Ta ₂ N	300	-50 to -110
Ni	7 (bulk)	-
NiCr	60-600	200
GaAs	300-450 ohms/sq.	3000-3200
AuGeNi (alloyed)	2 ohms/sq.	-

NOTE: The exact value that is obtained is dependent on deposition parameters. In all cases, thin-film resistivity will be greater than bulk resistivity. Therefore this data should be used only as a guideline.

2.2 MMIC Design Methodology

The design of MMICs is a relatively new art and has not yet matured to the point where a designer may use well established methods to proceed from specifications to finished designs, which can be successfully fabricated to satisfy the requirements.

Every new art must have its foundations laid before specific designs are attempted. In monolithics these foundation blocks are the passive circuitry; the inductors, capacitors, resistors and interconnects. Until a circuit designer understands the CAD representations of these passive components, a design of an MMIC can take many iterations.

At present, a widely used design procedure involves the development of a microwave miniature active circuit (MMAC) as an intermediate stage, before a fully monolithic realization is attempted [22]. MMACs use most of the batch processing technology developed for MMICs to fabricate all circuit elements, except for the active devices, which are wirebonded in place on the substrate. This allows separate optimization of the passive circuit and active devices. It also allows for faster fabrication turnaround, because there are less critical and fewer fabrication process steps in MMAC processing. MMACs can serve as stepping stones in the development of MMICs.

For the MMIC design, the starting point is the design specification, from which a circuit approach or topology is evolved. The circuit topology and system requirements dictate the types of active elements to be used. The next step is the active device characterization. The active device will usually not be separately accessible, since it is fabricated at the same time as the rest of the circuit. Using a company's processing plant, the active devices normally have extensive data measured on them from previous MIC uses. This data is then used to obtain a model for the active device in a MMIC environment.

When an external processing plant is used to process MMICs, S-parameters or equivalent circuits are normally available for the active devices. After obtaining a circuit model for the active device, one can proceed to the computer aided design (CAD) phase.

In the CAD step the device data are incorporated into the circuit topology file to allow analysis, optimization, and tolerance studies to be performed on the circuit. The success of this step depends directly on the accuracy of the device and circuit models used in the computer programs.

After the circuit design is completed, the next step is the mask layout. Since much of the layout process is cut-and-try, or based on prior experience, it is convenient to use a computerized mask layout system. There must be a

capability for interaction between the layout process and the CAD step, and in general many iterations between the steps are necessary.

Once the circuit layout is complete, the numerical coordinate data describing the topologies of the various mask layers are recorded on magnetic tape. If a foundry (external fabrication service) is being used, the magnetic tape is then delivered. The following step is the conversion of this data to actual photomasks by automated pattern generators. The completed photomasks are sent to the technology laboratory where they are inspected, and if satisfactory, are used in the next step; namely, circuit fabrication.

The fabricated circuits are usually dc probed on the wafer. The wafer is diced into chips and the chips that have passed the dc probe test are mounted on carriers for RF measurements. The chips, with satisfactory RF performance, are packaged and delivered to the customer. In the case of the foundry, often only dc measurements are performed before delivery of a fraction of the wafer chips.

In practice, several design iterations are necessary before the desired circuit performance is obtained.

Once the design, fabrication, and testing processes are perfected, the incremental cost to produce additional wafers is quite small compared to the development cost. This contributes to a low cost per chip, provided that the

development cost can be spread over a sufficiently large number of units, and well-controlled automated techniques are used for fabrication and testing, resulting in high yield.

2.3 Yield Considerations

Yield-limiting factors in MMIC processing are generally classified as either catastrophic or parametric. The most significant yield-limiting factors are usually related to simple dc failure of MIM capacitors and GaAs FETs [25]. These failures are both processing-related and, particularly in the case of contact lithography, mask-alignment related.

The factors which limit MIM capacitor yield include control of the thickness and dielectric constant of the insulating layer, and the occurrence of short circuits between the first and second levels of metal [26,27,28]. Approaches to maximize MIM capacitor dc yield include minimization of overlap between the second-level and the first-level metal capacitor periphery, etching of the first-level metal to produce smooth edges that are less likely to produce shorts, and the use of air bridges to contact the top electrode of the capacitor.

Control of the thickness and dielectric constant of the deposited dielectric layer is necessary in order to achieve a high yield of MIM capacitors to a specified tolerance. The thickness of the deposited silicon nitride

layer can be accurately controlled using a deposition monitor, and the dielectric constant is controlled by maintaining consistent stoichiometry of the deposition gases.

The dc yield of GaAs FETs is related to the total gate length of the device on the chip. Typical dc failure modes for GaAs FETs are due to broken or shorted gates. In general, FET dc failures that occur during processing are a result of photoresist or masking defects. The incidence of such processing defects increases with total FET gate length and with reduced source-to-gate spacing [29,30].

The present (1986) yields are adequate for fabrication of integrated multi-component circuits, but must be improved for economically viable production of high-functionality circuits. A technique for measuring the wafer yields, RF and DC, is outlined in the next section.

2.4 GaAs MMIC Automatic Test Equipment System

The ability to perform a microwave assessment of GaAs integrated circuits on the wafer will significantly reduce the subsequent effort and costs incurred in conventional MMIC evaluation, prior to final assembly.

Development of an automatic measurement system has been previously reported by Eddison and Buck [31]. The system has been configured for measuring device DC characteristics, as well as RF quantities such as S-parameters, noise figure,

gain compression, etc. Fig. 2.10 shows a typical example of RF test equipment. The equipment switching is performed within the rack, and the probe channel-selection/RF-route reversal is implemented at the wafer probe station. A desktop computer controls all the test equipment, sets the RF signal routing, drives the wafer step movements, and manages the large quantity of data produced.

Prior to the wafer measurements, the system is automatically calibrated using an integrated calibration substrate. This substrate contains known co-planar components which have the same width as the devices to be tested, and are formed on an alumina substrate. This technique allows the measurement of error-corrected S-parameters to be made, with a reference plane at the probe tips.

Fig. 2.11 shows the S-parameter results of the first 50 cells on a GaAs MMIC wafer. It takes approximately 4 minutes to perform over 100 measurements on each cell. To measure an entire wafer would take approximately 9 hours.

Having described the design, fabrication and testing of MMICs in general, MMIC phased locked oscillator components, the central topic of this thesis, will be discussed in the next chapter.

Fig. 2.10. On-Wafer R.F. Measurement System Hardware [31]

Fig. 2.11. Measured FET S-Parameters of the First 50 I.C.s on a GaAs Wafer [31].

CHAPTER 3

PHASE LOCKED OSCILLATORS

In this chapter some possible configurations of a phase locked oscillator are presented together with an identification of the system components. The requirements of each individual building block of the different phase locked oscillator implementations are discussed at length. Also the least understood components, the phase detector and frequency divider, are isolated for further investigation.

3.1 System Configuration

There are two diametrically opposite varieties of oscillator stabilizers; narrowband and wideband [32]. In the first, a narrowband PLL is employed as a filter to improve the performance of another oscillator or signal that is accompanied by noise. In the second, a noisy oscillator is phase-locked to a clean reference to stabilize the locked oscillator.

The best performance for either type of stabilizer is obtained if two separate oscillators are used; a very low-level one for long-term stability and a second oscillator phaselocked to the first, for short-term stability. Bandwidth of the loop should be as narrow as possible, consistent with maintaining reliable lock, and the output taken from the locked oscillator.

An effective method of stabilization is to lock the microwave oscillator to a harmonic of a stable low-frequency source such as a crystal oscillator [33]. Here the loop tracks out the phase fluctuations of the locked oscillator so that the output has the stability of the frequency-multiplied reference source.

Another technique of stabilization is to divide the unstable oscillator frequency, and lock the reference oscillator to this signal. Four possible techniques for stabilizing an RF oscillator are shown in Figures 3.1a, b, c, d. Using any one of these techniques one can produce a microwave signal with excellent frequency accuracy, high spectral purity, low noise, and good frequency stability. The limitations of each individual configuration is in the realizability of the elements and also the performance of the elements.

The different system components which comprise a phase locked loop will be described in the next section.

Fig. 3.1. Phase Locked Oscillator Configurations [34].

3.2 System Components

7 Phase locked oscillators (PLOs) are derived by phase locking the fundamental output frequency of a microwave oscillator to a multiple or submultiple of the output frequency of a highly stable crystal oscillator. The crystal operates at a lower frequency than the microwave oscillator. The primary building blocks of a PLO are: a reference oscillator, a microwave oscillator, a frequency divider - balun combination, a multiplier, a low pass filter and a phase detector. One extra component which is present in the more sophisticated phased locked oscillators and synthesizers is the mixer. These components are discussed in the following sections.

3.2.1 Oscillators

Oscillators fall into one of two general categories: feedback or negative resistance types. A three-terminal FET with positive feedback also has negative resistance, so three-terminal devices may be placed in either category. To realize an oscillator some form of resonator is required in the feedback loop. This resonator may be in the form of a cavity or an inductor-capacitor circuit. If the oscillator is required to have some form of frequency tuning, a selection between mechanical or electrical tuning can be made. A mechanically tuned cavity may be as simple as an adjustable

screw in a cylinder. An electrically tuned circuit would probably consist of a voltage-variable-capacitance in a LC circuit.

Many different considerations must be taken into account before a decision is made on which oscillator topology will be used. Before selecting a FET oscillator design, consideration must be given to all the following points:

- Efficiency of DC to RF conversion
- Amplitude modulation and frequency modulation noise spectra
- Long term frequency stability
- Tuning bandwidth
- Temperature sensitivity
- Output power
- Frequency of operation
- Cost
- Size and weight
- Reliability.

Having selected an oscillator topology, improvement of its noise characteristics can be accomplished by either injection locking the oscillator, or by placing the oscillator in a phase-locked loop. Both of these techniques will be discussed in this chapter. However, first the most common microwave oscillators will be described.

Fixed Frequency Oscillators

Every FET oscillator has some form of tuning. From the very nature of the FET, the bias between the gate and source controls the depletion region characteristics. For a fixed-frequency oscillator, the feedback resonant loop generally consists of an inductor-capacitor (LC) circuit. The LC loop is the dominant element in determining the frequency of oscillation. By varying the FET's bias only minor changes in the oscillation frequency should be observed in a well-designed circuit. However, efficiency and output power may be substantially altered [35].

It is very important to have accurate information on the FET's S-parameters as well as the resonant loop. Any discrepancy between the predicted and actual S-parameters results in a difference in predicted oscillation frequency.

The advantage of fixed frequency oscillators is that they are very consistent from batch to batch, as well as being very simple to design. The primary disadvantage is that a few iterations will probably have to be made before the correct oscillation frequency is obtained. Generally, LC networks at microwave frequencies have low Q's [36], thus resulting in poor noise performance.

Voltage Controlled Oscillators

Many of today's electronic systems require the oscillating frequency of the microwave source to be variable. This frequency variation may be in discrete finite steps or it may be a smooth transition between two frequency states. Variation of the oscillator frequency with an applied dc signal opens up many possibilities for using the basic oscillator to perform more functions. The oscillator can be used in a phased locked loop for locking to a low-noise reference, thereby resulting in a low-noise oscillator. Oscillators are tuned using varactors or YIG devices. The latter device is controlled by a current while the former is controlled by a voltage. YIG devices can tune over multi-octave bandwidths but are slow in tuning [37]. The varactor's tuning range is limited by the capacitance change for the voltage range available [38]. The discussion to follow will concentrate on the Voltage Controlled Oscillator (VCO).

The important parameters which describe the performance of electronically tuned oscillators are:

a) Slew Rate: The rate at which the frequency of the oscillator can be changed from one end of the tuning range to the other, in response to a step change in the control parameter.

b) Settling Time: The maximum time taken by the oscillator to settle within some frequency band, centered on the predicted static frequency, after a step tuning signal is applied.

c) Post Tuning Drift: The largest value of frequency drift measured over a time interval large compared to the settling time, but not including the frequency drift settling time.

d) Tuning Linearity: The maximum frequency deviation of the experimental tuning curve from the best linear fit.

These parameters together with low A.M. and F.M. noise, and spurious-free response, define the broadband electronic tuning oscillator requirements.

Dielectric Resonator Oscillators

Microstrip circuits are generally limited to a Q value of 100 to 200 [39], and oscillators fabricated on this medium do not exhibit excellent low noise or high temperature stability. Dielectric resonators added to the microstrip circuit, on the other hand, add Q to the circuit and lock the frequency [40]. The high Q results in very low noise performance, and with proper temperature compensation can provide nearly constant frequency versus temperature characteristics.

A dielectric resonator, mounted near a microstrip line, is shown in figure 3.2. The resonator consists of a puck of high Q , high dielectric constant, and temperature compensated material ($ZrSnTiO_4$ or $BaTi_4O_9$).

Figure 3.2. Dielectric Resonator.

The equivalent circuit for a dielectric resonator is a parallel resonant RLC circuit in series with the micro-

strip line, with the reference plane at the center-line of the resonator [41]. The input impedance of the resonator with a matched load termination is [42]:

$$Z = Z_0 \left[1 + \frac{\beta}{1 + 2j Q_r \frac{\Delta F}{F_r}} \right] \quad 3.2$$

where

β = coupling factor

Q_r = resonator Q

ΔF = deviation from center resonator frequency

F_r = center resonator frequency.

3.2.2 Low Pass Filter

In the phase-locked oscillator implementation, a low-pass filter is set between the phase detector output and the VCO modulation input. The transfer function of the low-pass filter has considerable influence on the properties of the loop, and provides a means for modifying the loop's performance [43].

In a phase-locked oscillator there are two conflicting requirements. First, to minimize output phase jitter due to external noise, the loop bandwidth should be made as narrow as possible. Second, to minimize the transient error due to signal modulation, as well as minimize output jitter

due to internal oscillator noise, thereby obtaining improved tracking and acquisition properties, the loop bandwidth should be made as wide as possible. Improvement in one type of performance can only be achieved at the expense of degrading the other, consequently some compromise between the two is always necessary.

3.2.3 Mixer

Mixers are used in a number of different PLL configurations [44]. The use of a MESFET mixer presents significant advantages over its conventional diode counterpart [45]. Among these advantages is the possibility of obtaining conversion gains associated with low noise figures. A further advantage results from the fact that the local oscillator, RF signal and IF signal, are intrinsically separated at the three ports of the MESFET, because of the low inter-port coupling.

Four of the most widely used MESFET mixers are shown in Fig. 3.4. Each of these mixers exploits different aspects of the MESFET's nonlinearities.

The single MESFET mixer, Figure 3.4(1), introduces an RF signal into the gate, the gate is biased near pinch off, and the local oscillator is applied to the source. The difference-frequency is then extracted from the drain. The local oscillator frequency is superimposed on the dc voltage at the source and mixing is achieved using the MESFET's nonlinearities. This single MESFET mixer has the advantage of simplicity of construction, but its primary disadvantage

is the poor isolation between RF and LO ports as well as IF port [46].

The MESFET mixers can generally be categorized into the single MESFET mixers, Figure 3.4(i), the dual-gate MESFET mixers, Figure 3.4(ii) and the balanced MESFET mixers, Figure 3.4(iii). The dual-gate MESFET mixers have one major advantage, it has good LO/RF isolation. The main properties of a balanced MESFET mixer are, good LO isolation, spurious-response rejection, and noise rejection [46]. The balanced configurations require an IF hybrid as well as an input hybrid, this tends to complicate the circuit and may increase the size.

The next section discusses the multiplier; this component is used to transfer the crystal frequency up to the oscillator's frequency.

3.2.4 Multiplier

The MESFET multiplier has gained widespread attention in the microwave field. Its advantages include conversion gain instead of the usual conversion loss associated with conventional diode multipliers, low-noise figure, and high dynamic range [47]. The same nonlinearities that produce mixing in a FET, namely the $I_{GS}-V_{GS}$ and $I_{DS}-V_{GS}$ nonlinearities, are both used in the frequency multiplier application [48]. The first of these effects results from the Schottky barrier diodes. The second nonlinearity is created by the pinch-off effect. Dual-gate FETs are popular as multipliers, although they tend to have larger noise figures than single gate FETs, Figure 3.3, [49].

Figure 3.3. Dual-Gate MESFET Multiplier.

Figure 3.4. FET Mixer Configuration.

3.2.5 Frequency Divider

Another component which is commonly used in phase locked oscillators is the frequency divider.. Frequency division is necessary in a variety of microwave systems. Among the classic applications are frequency counting, and phase locked oscillation [50,51]. Additional applications lie in the area of electronic warfare, where the ability of divider circuits to compress bandwidths can be exploited in the processing of wideband signals [52].

There have been a number of different microwave frequency divider concepts described in the literature [53,54,55]. Each of these individual concepts may be viewed as belonging to one of three basic categories. The first category includes circuits that function in a manner similar to digital frequency counters, yielding instantaneous frequency division of a given signal on a cycle-by-cycle basis..

The second major category consists of the regenerative divider circuits, illustrated in Fig. 3.5, whose concept has been known since 1939, [56]. The necessary components include amplification, mixing, subharmonic feedback, and filtering..

In briefly reviewing the basic operation of the regenerative divider, it is assumed that a signal component at the subharmonic of the incident signal frequency is present initially, either due to noise or input signal transients. This signal is then mixed with the incident

signal to produce a lower sideband at the subharmonic, which subsequently is filtered out, amplified, and fed back to the mixer. This leads to the buildup of a subharmonic oscillation when the loop gain exceeds unity [57]. This yields a frequency-divided counterpart to the input signal. The turn-on threshold for the subharmonic oscillation is determined by the quiescent loop gain.

Fig. 3.5. General Concept of Regenerative Frequency Division.

The third frequency divider category commonly used is the parametric type. In this technique, frequency division occurs by the generation of an exact subharmonic of the input signal by a nonlinear capacitive circuit. This type of frequency divider is based on the general principles of the Harrison approach [58], whereby a pair of varactor diodes is used to simultaneously provide both (parametric)

amplification and mixing. However, the novel circuit described in this thesis and shown in Fig. 3.5 relies on MESFET characteristics to accomplish the parametric frequency division [50].

In Fig. 3.6, the input frequency F_{IN} is applied to the gate terminals of the FETs. The nonlinear gate-to-source capacitance initiates the generation of the subharmonic by the mixing process described previously. The inductors in the gate terminals are chosen so that a resonant loop is produced at $F_{IN}/2$ between the FET's gate to source capacitances. The resulting outputs at the FET's drain terminals are in-phase signals at F_{IN} and are out-of-phase at $F_{IN}/2$.

The balun, described in the next section, is then used to extract the $F_{IN}/2$ signal from the frequency divider.

Fig. 3.6. Frequency Divider.

3.2.6 Balun

A circuit which performs a transformation from a balanced transmission line to a unbalanced transmission line is called a balun. A twin-lead transmission line (two parallel-conductor line) is an example of a symmetrical balanced line, whereas a coaxial cable is inherently unbalanced [59]. The operation of a typical balun, shown in Fig. 3.7, can be outlined as follows. Starting at port A, the unbalanced transmission line has currents of equal magnitudes but opposite direction flowing on the center conductor and the outer conductor. At the end of transmission line A, the current on the outer conductor is choked by the quarter wavelength short circuited transmission line B. Similarly the center conductor current of transmission line A is choked by transmission line D. The result is that the transmission lines B and D are 180° out-of-phase, creating a balanced system.

Fig. 3.7. Transmission Line Balun.

Generally, monolithic circuits are fabricated on a GaAs substrate with gold backplating. This ground plane limits the possible selection of feasible baluns. The circuit diagram of a possible monolithic balun is shown in Fig. 3.8, [60]. The transmission line L_2 is a quarter wavelength long, so that between points B and O there is a -90° phase shift. The elements C_1 , C_2 and L_1 are chosen such that between point D and O there is a $+90^\circ$ phase shift. The resulting circuit has points B and D 180° out of phase to each other. This balun can be designed for a large bandwidth by optimizing the four elements over the frequency range of interest.

The next section describes the phase detector which is used in most phase locked loops.

Fig. 3.8. Monolithic Microwave Balun.

3.2.7 Phase Detector

Two broad categories of phase detectors can be distinguished: the multiplier and the sequential phase detector [61]. A sequential phase detector produces an output voltage that is a function of the time interval between the zero crossings of the two input signals. In comparison, multiplier phase detectors produce a dc output voltage which is the average product of the two input signals.

Sequential phase detectors are usually implemented with digital circuits (flip flops) and operate with binary (rectangular) input waveforms [62]. They trigger on waveform edges, consequently errors may result due to missing or extra crossings. Sequential phase detectors usually have poorer noise-handling capability than the multiplier phase detectors. Sequential phase detectors are currently limited to frequencies lower than the UHF band and thus are not considered in this thesis.

For an ideal multiplier, in which both inputs are sinusoidal, the useful dc output is proportional to both the product of the amplitude of the two inputs, and the cosine of the phase difference between them [32].

A popular multiplier phase detector circuit is shown in Fig. 3.9, [46]. This circuit can also be used as a double-balanced mixer. It has a wide bandwidth, is available over many frequency ranges, and has good performance [46].

Fig. 3.9. Multiplier Phase Detector (Diode-Ring)

Fig. 3.10. Multiplier Phase Detector (Diode Rectifier).

A phase detector which once was very common is shown in Fig. 3.10 [32]. Here the hybrid transformer produces the vector sum and difference of the two input signals, which are then converted to dc signals by the diode rectifiers. The useful output signal is the difference between the two rectified voltages. Since the output is the small difference between these two larger dc rectified voltages, balance is critical if dc offset is to be avoided. At low frequencies, the popularity of this circuit has declined with the advent of good integrated circuits and packaged rings.

A popular microwave phase-detector configuration is the single-balanced phase detector [46]. It is composed of a 3 dB hybrid coupler, two Schottky diodes, and two low-pass filters (Fig. 3.11).

Any phase detector configuration which requires the use of a transformer is very lossy and difficult to realize in a monolithic circuit. The single-balanced phase detector could form a feasible monolithic circuit, however its quadrature hybrid would occupy a large proportion of the chip area.

A novel phase detector which utilizes source-to-drain coupling between two FET's, is shown in Fig. 3.12. This phase detector operates according to the same principles as the single-balanced phase detector [46]. The gate voltages of the two FETs are modulated by their respective RF signals, so that the corresponding dc drain-to-source resistances are modulated. This novel phase detector offers

Fig. 3.11. Single-Balanced Phase Detector.

Fig. 3.12. Double-FET Phase Detector.

the advantages of small size and performance comparable to the single-balanced resistive diode mixer. A description of this novel phase detector is the major topic discussed in Chapter 5.

3.3 Discussion of MMIC Phase Locked Oscillator Components

Depending on the specific configuration of a phase locked oscillator, all or some of the components that have been discussed will be required. In general the reference oscillator will be at a lower frequency than the locking oscillator [63]. Under this situation the reference will either be multiplied to the locking oscillator frequency, or the locking oscillator will be divided to the reference, or a combination of the two.

Each of the phase locked oscillator configurations has its own advantages and disadvantages, the limitations are based on the components realizability. In addition, they all require frequency tuning capability to maintain lock with the reference, and hence require a voltage-controlled oscillator.

The design of MMIC VCOs is not unlike that of the hybrid integrated circuit VCOs which have been studied in great depth [64,65]. In addition, recently, some publications on MMIC VCO's are available [66,67].

Similarly, MMIC multiplier and mixer publications have appeared [68]. Again, multipliers and mixers have been

studied for a great number of years [66,68] and little more is required in the development of their MMIC counterparts.

The loop filter requirements are thoroughly discussed in a number of texts [32,33]. However in an MMIC design, problems arise due to the required large size of the passive components. At present, two approaches are available, either using passive components on the MMIC wafer or using integrated circuit chips off the wafer. These alternatives have to be examined in light of the specifications of a particular phase-locked-oscillator requirement.

In contrast with these components, there are very few publications on the MMIC frequency divider and phase detector [53,66]. As a result, this thesis concentrates on developing a greater understanding of the frequency divider and phase detector.

Chapter 4 describes the MMIC frequency divider and presents a detailed analysis of its performance.

Chapter 5 examines the MMIC phase detector and evaluates its performance.

CHAPTER 4

FREQUENCY HALVER

Some phased locked oscillator configurations require the use of frequency dividers. The frequency divider is a relatively unknown device in the communications field. This chapter introduces a novel frequency halver and performs a detailed theoretical analysis on it.

As discussed in Section 3.2.5, there are three general categories of frequency dividers: digital, regenerative and parametric. The digital frequency divider is generally limited to lower frequency bands. A few microwave digital frequency dividers have appeared in the literature [53,66], but their inherent noise along with the large required input power has limited their usefulness. The regenerative frequency divider has demonstrated unstable performance [54]. A regenerative monolithic frequency divider has demonstrated reasonable performance but its inherent stability problems limit this type of configuration [54]. The parametric frequency divider has shown a significant conversion loss and has required a large turn-on power.

The novel parametric frequency halver introduced in this chapter can provide a solution to the problems of large conversion loss and turn-on power.

Using the technique of a parametric divider, frequency division occurs by generating an exact subharmonic

of the input signal with a balanced nonlinear capacitive circuit. A realization of this technique has been demonstrated by using two varactor diodes to capacitively load a pair of transmission lines in a balanced bridge configuration [52]. The electrical lengths of the transmission lines are chosen to produce a resonance at half the input frequency, the output is coupled to a co-planar balun. The nonlinear varactor diodes provide the necessary parametric amplification and mixing. While the possible frequency response can be quite wideband (e.g. input frequencies covering 8-16 GHz), the conversion loss is typically 12 dB across the band. Furthermore, since the threshold signal required to initiate division is approximately 5-10 dBm, any subsequent stages used to achieve an overall division of four, eight, sixteen, etc., necessitate the use of intermediate amplification.

The frequency divider which is presented in this thesis utilizes GaAs FETs in place of varactor diodes together with a novel circuit approach. The big advantage of using FETs is the possibility of conversion gain, thereby eliminating the need of amplification if further division is desired. Also the "semi-unilateral" property of the FET provides excellent isolation between the resonant loop and the output. Using this circuit approach, such a divider is well suited for fabrication in a MMIC version.

4.1 Frequency Halver Model

The parametric frequency divider circuit considered here is shown in Fig. 4.1(a) and consists of two field effect transistors, a pumping source with instantaneous voltage $V_p(t)$, two input inductors, L , two lumped resistors R_g , and an output load R_L . Each resistance R_g represents the inductor loss plus the loss associated with the gate-to-source resistance of the FET. A FET can be represented by an equivalent model, which consists of a gate-to-source capacitor, a feedback capacitor, a drain conductance, and a drain-to-source current [67,69].

Referring to Fig. 4.1(b), the pump at frequency $2\omega_0$ is applied in phase to the gates of the FETs where the nonlinear capacitance of the Schottky barrier diodes, C_g , produces the desired subharmonics. The resonant loop, which largely consists of the two input inductors and the two gate-to-source capacitances in series, maintains the subharmonic out of phase across the two FETs. This subharmonic is amplified by the device transconductance, g_m , and appears at the output terminals of the two FETs.

At small input signal levels, the resonant loop has an approximate small-signal resonant frequency ω_0 , which in the case of Fig. 4.1(b), and with zero gate-to-source bias voltage is

$$\omega_0 = 1/\sqrt{L C_g(0)} \quad (4.1)$$

As will be shown, parametric subharmonic generation of an output frequency ω (and its odd-order harmonics) can

(a)

(b)

Figure 4.1. Field Effect Transistor Frequency Halver:
(a) Physical circuit layout; (b) Equivalent circuit layout.

be obtained in response to an input frequency 2ω lying in a band extending from considerably below to slightly above $2\omega_0$. The exact bandwidth of frequency division depends on the input power level. The minimum input power is required when the input frequency equals $2\omega_0$.

The next section will formulate the differential equations that describe the behaviour of the frequency halver shown in Fig. 4.1(b).

4.2 Formulation of the Differential Equation

The gate-to-source capacitance is the dominant nonlinear component for generating the subharmonic signal [69]. The gate-to-source capacitance of a FET is a metal/n-type Schottky barrier varactor with a depletion layer charge defined as [70]:

$$q(v) = -A \sqrt{2e\epsilon N_D(\phi_0 + v)} \quad (4.2)$$

where

A is the junction area

e is the charge on an electron

ϵ is the permittivity of semiconductor material

ϕ_0 is the thermal equilibrium built-in potential

v is the total reverse voltage across the junction

N_D is the donor concentration on n-side.

It is convenient to express the charge q in terms of conventional quantities. The junction capacitance is defined in terms of the varactor charge-voltage relationship as:

$$C_g(v) = \frac{\Delta}{-dq/dv} \quad (4.3)$$

Hence, from (4.2):

$$C_g(v) = \frac{1}{2} A \sqrt{2e\epsilon N_D} \cdot \frac{1}{\sqrt{\phi_0 + v}} \quad (4.4)$$

This relation is the starting-point for deriving the mathematical model for the frequency halver.

Figure 4.2 shows the frequency halver's equivalent network representation, the necessary voltage drops and identifies the nodal currents.

For the right-hand side of the network, voltage drop around the loop gives:

$$v_p = L \cdot d/dt(i_2) + R_s i_2 + v_2 \quad (4.5)$$

$$i_2 = C_g(v_2) \cdot d/dt(v_2) - i_{22} \quad (4.6)$$

$$i_{22} = C_F \cdot d/dt(v_{02} - v_2) \quad (4.7)$$

$$i_2 = C_g(v_2) \cdot d/dt(v_2) - C_F \cdot d/dt(v_{02} - v_2) \quad (4.8)$$

where

R_s is the resonant loop series resistance

C_F is the feedback capacitance

L is the resonant loop inductance

g_L is the load conductance

g_o is the FET drain to source conductance

g_m is the FET transconductance.

Combining (4.5) - (4.8) yields:

$$\begin{aligned} v_p = & L \cdot d/dt \{ C_g(v_2) \cdot d/dt v_2 - C_F \cdot d/dt (v_{02} - v_2) \} \\ & + R_s \cdot \{ C_g(v_2) \cdot d/dt (v_2) - C_F \cdot d/dt (v_{02} - v_2) \} \\ & + v_2 \end{aligned} \quad (4.9)$$

For the left-hand side of the network, voltage drop around the loop gives:

$$v_p = L \cdot d/dt \{ C_g(v_1) \cdot d/dt(v_1) - C_F \cdot d/dt(v_{01} - v_1) \} \quad (4.10)$$

$$+ R_S \{ C_g(v_1) \cdot d/dt(v_1) - C_F \cdot d/dt(v_{01} - v_1) \}$$

$$+ v_1$$

Focussing on the v_{02} node, the current at this node must sum to zero:

$$0 = g_L \cdot (v_{01} - v_{02}) - C_F \cdot d/dt(v_{02} - v_2) - g_m v_2 - g_0 v_{02} \quad (4.11)$$

Similarly at the v_{01} node, the current at this node must sum to zero:

$$0 = g_L \cdot (v_{01} - v_{02}) + g_0 v_{01} + g_m v_1 + C_F \cdot d/dt(v_{01} - v_1) \quad (4.12)$$

Equations (4.9), (4.10), (4.11) and (4.12) define the operation of the frequency halver. Solution of these equations is facilitated by assuming that a subharmonic signal exists, and by manipulation and normalization of the variables.

Figure 4.2. Field Effect Transistor Frequency Halver Nodal Voltage and Current Identification.

Assuming frequency division occurs, the voltage across the gate to source nonlinear capacitance has a fundamental frequency signal plus a signal at half this frequency. Ignoring higher order harmonics [55]:

$$\begin{aligned} v_2 &= v_Q + v_s + V_{GS} \\ v_{02} &= v_R + v_o + V_{DS} \\ v_1 &= v_Q - v_s + V_{GS} \\ v_{01} &= v_R - v_o + V_{DS} \end{aligned} \quad (4.13)$$

where v_Q, v_R are signals at the fundamental frequency
 v_s, v_o are signals at half the fundamental frequency
 V_{GS}, V_{DS} are dc bias conditions for the FET

From the definition of a resonant loop, the two gate-to-source voltages will be in anti-phase at the divided frequency. Thus, equations (4.9) and (4.10) become

$$\begin{aligned} v_p &= L \cdot d/dt \{ C_g (v_Q + v_s + V_{GS}) \cdot d/dt (v_Q + v_s) - C_F \cdot d/dt (v_R - v_Q + v_o - v_s) \} \\ &+ R_s \cdot \{ C_g (v_Q + v_s + V_{GS}) \cdot d/dt (v_Q + v_s) - C_F \cdot d/dt (v_R - v_Q + v_o - v_s) \} \quad (4.14) \\ &+ v_Q + v_s \end{aligned}$$

and,

$$\begin{aligned} v_p &= L \cdot d/dt \{ C_g (v_Q - v_s + V_{GS}) \cdot d/dt (v_Q - v_s) - C_F \cdot d/dt (v_R - v_Q - v_o + v_s) \} \\ &+ R_s \cdot \{ C_g (v_Q - v_s + V_{GS}) \cdot d/dt (v_Q - v_s) - C_F \cdot d/dt (v_R - v_Q - v_o + v_s) \} \\ &+ v_Q - v_s \quad (4.15) \end{aligned}$$

and equations (4.11) and (4.12) become

$$0 = g_L \cdot (-2v_o) - C_F \cdot d/dt(v_R - v_Q + v_o - v_s) - g_m \cdot (v_Q + v_s) - g_o \cdot (v_R + v_o) \quad (4.16)$$

$$0 = g_L \cdot (-2v_o) + C_F \cdot d/dt(v_R - v_Q - v_o + v_s) + g_m \cdot (v_Q - v_s) + g_o \cdot (v_R - v_o) \quad (4.17)$$

The nonlinear element in these equations is the gate-to-source capacitance, which is a function of the fundamental and subharmonic signals, as well as of the bias condition.

Given a pumping voltage v_p , equations (4.14)-(4.17) include all the conditions necessary for realizing a subharmonic signal.

To simplify the mathematics we will assume one equation as being dependent on the pumping voltage and another as being independent of the pumping voltage. This procedure will allow terms that are alike to be combined for further simplification.

Adding (4.14) and (4.15) gives:

$$\begin{aligned} 2v_p = & L \cdot d/dt \{ C_g(v_Q + v_s + V_{GS}) \cdot d/dt(v_Q + v_s) + C_g(v_Q - v_s + V_{GS}) \cdot d/dt(v_Q - v_s) \} \\ & - L \cdot d/dt \{ C_F \cdot d/dt(v_R - v_Q + v_o - v_s) + C_F \cdot d/dt(v_R - v_Q - v_o + v_s) \} \\ & + R_s \cdot \{ C_g(v_Q + v_s + V_{GS}) \cdot d/dt(v_Q + v_s) + C_g(v_Q - v_s + V_{GS}) \cdot d/dt(v_Q - v_s) \} \\ & - R_s \cdot \{ C_F \cdot d/dt(v_R - v_Q + v_o - v_s) + C_F \cdot d/dt(v_R - v_Q - v_o + v_s) \} \\ & + 2v_Q \end{aligned} \quad (4.18)$$

Subtracting (4.14) from (4.15) yields:

$$\begin{aligned}
 0 = & L \cdot d/dt \{ C_g (v_Q + v_s + v_{GS}) \cdot d/dt (v_Q + v_s) - C_g (v_Q - v_s + v_{GS}) \cdot d/dt (v_Q - v_s) \} \\
 & - L \cdot d/dt \{ C_F (v_R - v_Q + v_o - v_s) - C_F \cdot d/dt (v_R - v_Q - v_o + v_s) \} \\
 & + R_s \cdot \{ C_g (v_Q + v_s + v_{GS}) \cdot d/dt (v_Q + v_s) - C_g (v_Q - v_s + v_{GS}) \cdot d/dt (v_Q - v_s) \} \\
 & - R_s \cdot \{ C_F \cdot d/dt (v_R - v_Q + v_o - v_s) - C_F \cdot d/dt (v_R - v_Q - v_o + v_s) \} \\
 & + 2\dot{v}_s
 \end{aligned} \tag{4.19}$$

Adding (4.16) to (4.17) produces:

$$4g_L v_o + 2g_m v_s + 2g_o v_o = - \{ C_F \cdot d/dt (v_R - v_Q + v_o - v_s) - C_F \cdot d/dt (v_R - v_Q - v_o + v_s) \} \tag{4.20}$$

Subtracting (4.16) from (4.17) delivers:

$$2g_m v_Q + 2g_o v_R = - \{ C_F \cdot d/dt (v_R - v_Q + v_o - v_s) - C_F \cdot d/dt (v_R - v_Q - v_o - v_s) \} \tag{4.21}$$

In equations (4.18)-(4.21), the terms which include the gate-to-source capacitance have been combined; as well as terms including the feedback capacitance. In this form, the equations can be greatly simplified once the gate to source varactor capacitance given by equation (4.4) is included.

In order to separate the dc gate-to-source capacitance from the small signal nonlinear contribution to the overall capacitance we let:

$$V_{Tg} = \phi_o + v_{GS} \tag{4.22}$$

Hence

$$C_g(V_{GS} + v_o) = \frac{1}{2} A \sqrt{2e\epsilon N_D} \cdot [V_{Tg} + v_o]^{-\frac{1}{2}}$$

where v_o is a small signal voltage

Defining:

$$C_g(V_{GS} + v_o) = \frac{1}{2} A \sqrt{\frac{2e\epsilon N_D}{V_{Tg}}} \cdot [1 + v_o/V_{Tg}]^{-\frac{1}{2}} \quad (4.23)$$

$$C_g(V_{GS}) = \frac{1}{2} A \sqrt{\frac{2e\epsilon N_D}{V_{Tg}}} \quad (4.24)$$

we have:

$$C_g(V_{GS} + v_o) = C_g(V_{GS}) \cdot [1 + v_o/V_{Tg}]^{-\frac{1}{2}} \quad (4.25)$$

Equation (4.25) defines the total gate-to-source capacitance, where the first term is the dc capacitance and the second term is the small signal nonlinear contribution.

To simplify the calculations of the four differential equations the approximation given below is necessary.

$$[1 + v_o/V_{Tg}]^{-\frac{1}{2}} \approx [1 - v_o/2V_{Tg}] \quad \text{if } v_o \ll V_{Tg} \quad (4.26)$$

Using this approximation, we can modify the following terms as shown:

$$\begin{aligned} & C_g(v_Q + v_s + V_{GS}) \cdot d/dt(v_Q + v_s) - C_g(v_Q - v_s + V_{GS}) \cdot d/dt(v_Q - v_s) \\ &= -C_g(V_{GS}) \cdot \left\{ \frac{v_s}{V_{Tg}} \cdot d/dt(v_Q) - 2 \cdot d/dt(v_s) + \frac{v_Q}{V_{Tg}} \cdot d/dt(v_s) \right\} \quad (4.27) \end{aligned}$$

$$\begin{aligned} & C_g(v_Q + v_s + V_{GS}) \cdot d/dt(v_Q + v_s) + C_g(v_Q - v_s + V_{GS}) \cdot d/dt(v_Q - v_s) \\ &= C_g(V_{GS}) \cdot \left\{ 2 \cdot d/dt(v_Q) - \frac{v_Q}{V_{Tg}} \cdot d/dt(v_Q) - \frac{v_s}{V_{Tg}} \cdot d/dt(v_s) \right\} \quad (4.28) \end{aligned}$$

$$C_F \cdot d/dt(v_R - v_Q + v_O - v_S) - C_F \cdot d/dt(v_R - v_Q - v_O + v_S) = 2C_F \cdot d/dt\{v_O - v_S\} \quad (4.29)$$

$$C_F \cdot d/dt(v_R - v_Q + v_O - v_S) + C_F \cdot d/dt(v_R - v_Q - v_O + v_S) = 2C_F \cdot d/dt\{v_R - v_Q\} \quad (4.30)$$

These terms are common to the frequency halver defining equations (4.18)-(4.21). By substituting in these terms, and normalizing the equations with the following factors, we can obtain greatly simplified frequency halving equations.

We now introduce the following normalizations and definitions:

$$\omega_p = 1/\sqrt{LC_g(V_{GS})} \quad \omega_R = 1/\sqrt{LC_F} \quad Q_p = 1/(\omega_p C_g(V_{GS}) \cdot R_s)$$

$$\beta = \omega_p / \omega_R \quad Y = C_F \omega_p \quad v = \omega / \omega_p \quad (4.31)$$

$$X = v_p / V_{Tg} \quad Y = v_O / V_{Tg} \quad S = v_S / V_{Tg} \quad R = v_R / V_{Tg}$$

$$Q = v_Q / V_{Tg} \quad \tau = \omega_p t \quad \alpha_1 = 2g_L + g_O \quad \alpha_2 = g_m \quad \alpha_3 = g_O$$

In addition, differentiation with respect to τ will be represented using Newton's dot notation. Substituting (4.27) - (4.30) into equations (4.18) - (4.21) and normalizing, the resulting four nonlinear frequency halving equations are:

$$\begin{aligned} 2X = & 2\ddot{Q} - \dot{Q}^2 - Q\ddot{Q} - \dot{S}^2 - S\ddot{S} + (2L\alpha_2\omega_p)\dot{Q} + (2L\alpha_3\omega_p)\dot{R} \\ & + (2/Q_p)\dot{Q} - (1/Q_p)Q\dot{Q} - (1/Q_p)S\dot{S} + (2R_s\alpha_2)Q \\ & + (2R_s\alpha_3)R + 2Q \end{aligned} \quad (4.32)$$

$$0 = 2\ddot{S} - 2\ddot{S}\ddot{Q} - \ddot{S}\ddot{Q} - \ddot{Q}\ddot{S} + (2L\alpha_1\omega_p)\ddot{Y} + (2\alpha_2\omega_p L + 2/Q_p)\ddot{S} \\ - (1/Q_p)\ddot{S}\ddot{Q} - (1/Q_p)\ddot{S}\ddot{Q} + (2\alpha_1 R_s)Y + 2(1 + \alpha_2 R_s)S \quad (4.33)$$

$$0 = \alpha_1 \ddot{Y} + \alpha_2 S + \gamma \ddot{Y} - \gamma \ddot{S} \quad (4.34)$$

$$0 = \alpha_3 R + \alpha_2 Q + \gamma \ddot{R} - \gamma \ddot{Q} \quad (4.35)$$

where:

X is the normalized input forcing function of angular frequency $2v$.

Q is the normalized forcing function voltage developed across the varactor, of angular frequency $2v$.

R is the normalized output voltage, of angular frequency $2v$.

S is the normalized subharmonic voltage across the varactor, of angular frequency v .

Y is the normalized output subharmonic voltage, of angular frequency v .

Equation (4.32) contains the forcing function and will be used to evaluate the magnitude of the subharmonic as a function of the signal being pumped across the gate to source Schottky barrier diode. This equation will be called the driving equation. Equation (4.33) is the resonant loop equation, which describes the nonlinear transfer of the pumping voltage to its subharmonic. Equations (4.34) and (4.35) evaluate the field effect transistor's load driving characteristics for the fundamental and subharmonic frequencies. We will call equations (4.34) and (4.35) the fundamental output equation and the subharmonic output equation, respectively.

4.3 Analytical Solution

To analytically solve the frequency-halving differential equations, we first let the forcing function be defined as:

$$X = X(o)\sin(2v\tau - 2\theta) \quad \text{where } v = \omega/\omega_p \quad (4.36)$$

The differential equations can then be solved using an approach developed by Hayashi [71] where the approximate periodic solutions are substituted into the differential equations and the coefficients of the real and imaginary terms are equated separately to zero.

We will begin the derivation of the frequency-halving differential equations, by first solving the fundamental output equation. This equation is used to obtain the output voltage R as a function of the voltage across the varactor, Q , at the fundamental frequency.

Rewriting equation (4.35) gives:

$$\alpha_2 Q + \alpha_3 R = -\gamma[\dot{R} - \dot{Q}] \quad (4.37)$$

We will assume that R and Q are sinusoidal at the fundamental frequency with amplitudes $R(o)$ and $Q(o)$, respectively, and have a phase difference of ϕ between them. For simplicity, we will represent R and Q in their complex, rather than their sinusoidal form.

Using the fact that:

$$\sin(x) = \frac{e^{+jx} - e^{-jx}}{2j}$$

$$\text{Let: } R = -2jR(o)(\alpha^2 - \alpha^{*2}) \quad (4.38)$$

$$\text{where } \alpha = \frac{1}{2} e^{j(v\tau + \phi)}$$

* denotes the complex conjugate

Similarly:

$$Q = -2jQ(o)(\alpha^2 e^{-j2\phi} - \alpha^{*2} e^{j2\phi})$$

Substituting into (4.37)

$$\begin{aligned} 0 = & -2j\alpha_3 R(o)(\alpha^2 - \alpha^{*2}) \\ & -2j\alpha_2 Q(o)(\alpha^2 e^{-j2\phi} - \alpha^{*2} e^{j2\phi}) \\ & -2j\gamma \dot{R}(o)(\alpha^2 - \alpha^{*2}) \\ & +2\gamma R(o)(\alpha^2 + \alpha^{*2})(2v + \phi) \\ & +2j\gamma \dot{Q}(o)(\alpha^2 e^{-j2\phi} - \alpha^{*2} e^{j2\phi}) \\ & -4v\gamma Q(o)(\alpha^2 e^{-j2\phi} + \alpha^{*2} e^{j2\phi}) \end{aligned} \quad (4.39)$$

In this analysis we are only concerned with the steady state solution. The steady state solution requires $\dot{R}(o)=0$, $\dot{Q}(o)=0$, and $\phi = 0$, thereby eliminating the third and fifth terms in equation 4.39.

Now, since α^2 and α^{*2} are independent non-zero terms, their coefficients must equate to zero.

The coefficients of α^2 give:

$$0 = -j\alpha_3 R(o) - j\alpha_2 Q(o)e^{-j2\phi} + 2\gamma v R(o) - 2\gamma v Q(o)e^{-j2\phi} \quad (4.40)$$

The coefficients of α^{*2} give:

$$0 = j\alpha_3 R(o) + j\alpha_2 Q(o)e^{j2\phi} + 2\gamma v R(o) - 2\gamma v Q(o)e^{j2\phi} \quad (4.41)$$

Multiplying equation (4.40) by $e^{j2\phi}$ and solving yields:

$$e^{j2\phi} = \left\{ \frac{2\gamma v + j\alpha_2}{2\gamma v - j\alpha_3} \cdot \frac{Q(o)}{R(o)} \right\} \quad (4.42)$$

Rearranging equation (4.41) provides:

$$(2\gamma v + j\alpha_2)Q(o)e^{j2\phi} = (2\gamma v + j\alpha_3)R(o) \quad (4.43)$$

Using (4.42) and (4.43), we have:

$$\frac{R^2(o)}{Q^2(o)} = \frac{1 + [\alpha_2/2\gamma v]^2}{1 + [\alpha_3/2\gamma v]^2} \quad (4.44)$$

$$\text{and } 2\phi = \tan^{-1}[\alpha_2/2\gamma v] + \tan^{-1}[\alpha_3/2\gamma v] \quad (4.45)$$

Equations (4.44) and (4.45) are the solution of the fundamental output equation for the steady state value of $R(o)$ as a function of $Q(o)$. This solution shows a dependence on the normalized FET transconductance, α_3 ; the FET output conductance, α_2 ; the normalized FET feedback capacitance, γ ; and the normalized fundamental angular frequency, v .

The subharmonic output equation can similarly be solved to obtain the steady state value of $Y(o)$ as a function of $S(o)$. Here $Y(o)$ is the subharmonic output signal and $S(o)$ is the subharmonic signal across the varactor. The assumed phase difference between Y and S is represented by n . Solving equation (4.34) provides:

$$\frac{Y^2(o)}{S^2(o)} = \frac{1 + [\alpha_2/\gamma v]^2}{1 + [\alpha_2/nv]^2} \quad (4.46)$$

$$\text{with } n = \tan^{-1}[\alpha_2/\gamma v] + \tan^{-1}[\alpha_1/\gamma v]$$

where

$$Y = Y(o)(\alpha - \alpha^*), \text{ and } \alpha = \frac{1}{2}e^{j(vt+n)}$$

$$S = S(o)(\alpha e^{-jn} - \alpha^* e^{jn})$$

Thus far, the fundamental output equation and the subharmonic output equation have been solved and their solutions shown in equations (4.44) and (4.46), respectively.

In the derivations of the driving equation and the resonant loop equation, we will require the terms $R(o)e^{j2\phi}$ and $Y(\tau)e^{j\eta}$ in complex number notation, with real and imaginary terms. Rewriting equations (4.44), (4.42) gives:

$$R(o) = Q(o) \sqrt{\frac{1 + M^2}{1 + H^2}} \quad (4.47)$$

and

$$e^{j2\phi} = e^{j\tan^{-1}M} e^{j\tan^{-1}H} \quad (4.48)$$

where

$$M = \alpha_2 / (2\gamma v)$$

$$H = \alpha_3 / (2\gamma v)$$

Using the identity:

$$e^{j\tan^{-1}X} = \frac{1}{\sqrt{X^2+1}} + j \frac{1}{\sqrt{(\frac{1}{X})^2+1}}$$

we have:

$$\begin{aligned} e^{j2\phi} = & \frac{1}{\sqrt{(M^2+1)(H^2+1)}} + j \frac{MH}{\sqrt{(M^2+1)(H^2+1)}} \\ & + j \frac{M}{\sqrt{(M^2+1)(H^2+1)}} + \frac{0}{\sqrt{(M^2+1)(H^2+1)}} \end{aligned} \quad (4.49)$$

In equation (4.49), it is observed that $e^{j2\phi}$ is expanded into its real and imaginary terms. We can now proceed to express the quantity $R(o)e^{j2\phi}$ as shown:

$$R(o)e^{j2\phi} = Q(o) \left\{ \frac{1-MO}{1+O^2} \right\} + jQ(o) \left\{ \frac{M+O}{1+O^2} \right\} \quad (4.50)$$

Similarly for $Y(o)$ as a function of $S(o)$

$$Y(o)e^{jn} = S(o) \left\{ \frac{1-PL}{1+P^2} \right\} + jS(o) \left\{ \frac{L+P}{1+P^2} \right\} \quad (4.51)$$

where

$$P = \alpha_1 / \gamma v$$

$$L = \alpha_2 / \gamma v \quad (4.52)$$

Using the above expressions for $R(o)e^{j2\phi}$ and $Y(o)e^{jn}$, we will now proceed to solve the resonant loop equation (4.33). This equation will determine the nonlinear behaviour of the frequency-halver in the resonant loop. This loop consists of two varactors in series with two inductors.

Rewriting equation (4.33)

$$0 = 2\ddot{S} - 2\ddot{S}\ddot{Q} - \ddot{S}\ddot{Q} - \ddot{Q}\ddot{S} - (1/Q_p)\ddot{S}\ddot{Q} - (1/Q_p)\ddot{S}\ddot{Q} + 2(\alpha_2\omega_p L + 1/Q_p)\ddot{S} + 2(\alpha_1\omega_p L)\ddot{Y} \\ + 2(\alpha_1 R_s)\ddot{Y} + 2(1 + \alpha_2 R_s)\ddot{S} \quad (4.53)$$

Assuming subharmonic behaviour and using:

$$\alpha = \frac{1}{2} e^{j(\nu\tau + \psi)} \quad (4.54)$$

we can write:

$$S = -S(o)(\alpha - \alpha^*)$$

$$Y = -Y(o)(\alpha e^{jn} - \alpha^* e^{-jn})$$

$$Q = -2jQ(o)(\alpha^2 e^{-j2\psi} - \alpha^{*2} e^{j2\psi})$$

where,

S is the normalized subharmonic voltage across the varactor of angular frequency ν .

Y is the normalized output subharmonic voltage of angular frequency ν .

Q is the normalized forcing function voltage developed across the varactor of angular frequency 2ν .

Substituting in these approximate periodic solutions, and solving for the steady state solution, as demonstrated previously, we have:

$$\begin{aligned}
 0 = & 2j\nu^2 S(o)(\alpha - \alpha^*) \\
 & - 8\nu^2 S(o)Q(o)(\alpha + \alpha^*)(\alpha^2 e^{-2j\psi} + \alpha^{*2} e^{j2\psi}) \\
 & - 8\nu^2 S(o)Q(o)(\alpha - \alpha^*)(\alpha^2 e^{-j2\psi} - \alpha^{*2} e^{j2\psi}) \\
 & - 2\nu^2 S(o)Q(o)(\alpha - \alpha^*)(\alpha^2 e^{-j2\psi} - \alpha^{*2} e^{j2\psi}) \quad (4.55) \\
 & + 4j\nu/Q_p \cdot S(o)Q(o)(\alpha - \alpha^*)(\alpha^2 e^{-j2\psi} + \alpha^{*2} e^{j2\psi}) \\
 & + 2j\nu/Q_p \cdot S(o)Q(o)(\alpha + \alpha^*)(\alpha^2 e^{-j2\psi} - \alpha^{*2} e^{j2\psi}) \\
 & + 2\nu S(o)(\alpha_2 \omega_p L + 1/Q_p)(\alpha + \alpha^*) \\
 & + 2\nu(\alpha_1 \omega_p L)Y(o)(\alpha e^{j\eta} + \alpha^* e^{-j\eta}) \\
 & - 2j(\alpha_1 R_g)Y(o)(\alpha e^{j\eta} - \alpha^* e^{-j\eta}) \\
 & - 2j(1 + \alpha_2 R_g)S(o)(\alpha - \alpha^*)
 \end{aligned}$$

Since only coefficients of α and α^* are of interest, the higher order harmonics can be ignored. Solving for the coefficients of the α terms gives:

$$0 = \left[\frac{1}{2} v^2 - j \frac{1}{2} v / Q_p \right] S(o) Q(o) e^{-j 2 \psi} \\ + 2v(\alpha_2 \omega_p L + 1/Q_p) S(o) + 2j v^2 S(o) - 2j(1 + \alpha_2 R_g) S(o) \quad (4.56) \\ + 2v(\alpha_1 \omega_p L) Y(o) e^{j \eta} - 2j(\alpha_1 R_g) Y(o) e^{j \eta}$$

Using equation (4.51) we have:

$$Y(o) e^{j \eta} = S(o) \left[\frac{1-PL}{1+P^2} + j \frac{L+P}{1+P^2} \right] \quad (4.57)$$

Upon substituting this value for into equation (4.56) we obtain:

$$-Q(o) e^{j 2 \psi} \left[\frac{1}{2} v^2 - j \frac{1}{2} v / Q_p \right] = 2v(\alpha_2 \omega_p L + 1/Q_p) + 2v(\alpha_1 \omega_p L) \left[\frac{1-PL}{1+P^2} \right] \\ + 2\alpha_1 R_g \left[\frac{1+P}{1+P^2} \right] \quad (4.58) \\ + j \left[2v^2 - 2(1 + \alpha_2 R_g) + 2v(\alpha_1 \omega_p L) \left[\frac{1-PL}{1+P^2} \right] \right] \\ - j \left[2\alpha_1 R_g \left[\frac{1-PL}{1+P^2} \right] \right]$$

A similar expression results upon solving for the coefficients of the α^* terms. Combining these two expressions results in the following equation:

$$Q^2(o) \left[\left(\frac{1}{2} v^2 \right)^2 + \left(\frac{1}{2} v / Q_p \right)^2 \right] = K_o^2 + K_1^2 \quad (4.59)$$

where

$$K_0 = 2v(\alpha_2 \omega_p L + 1/Q_p) + 2v(\alpha_1 \omega_p L) \left[\frac{1-PL}{1+P^2} \right] + 2\alpha_1 R_s \left[\frac{L+P}{1+P^2} \right] \quad (4.60)$$

$$K_1 = 2v^2 - 2(\alpha_2 R_s + 1) + 2v(\alpha_1 \omega_p L) \left[\frac{L+P}{1+P^2} \right] - 2\alpha_1 R_s \left[\frac{1-PL}{1+P^2} \right]$$

and

$$-2\psi = \tan^{-1}[K_1/K_0] + \tan^{-1}[1/vQ_p] \quad (4.61)$$

Equations (4.59), (4.60) and (4.61) provide the solution to the resonant loop equation. In particular equations (4.59) and (4.60) show the relationship between the FET's parameters and the varactor's forcing function voltage, $Q(\omega)$. These equations demonstrate that the steady state voltage across the varactor, at an angular frequency of $2v$, is amplitude limited by the FET parameters, not by the load resistor. The load resistor does not absorb any power, since at an angular frequency of $2v$ the output voltages from the two FETs are in-phase.

The fourth and final equation, the driving equation, will determine the generated subharmonic voltage as a function of the input forcing voltage. We will solve this equation using the same approach as was applied to the resonant loop equation.

Rewriting equation (4.32):

$$\begin{aligned} 2X &= 2\ddot{Q} - \dot{Q}^2 - Q\ddot{Q} + 2(\alpha_2 L g_m \omega_p) \dot{Q} + 2(\alpha_3 L \omega_p) \ddot{R} + (2/Q_p) \dot{Q} \\ &- (1/Q_p) Q\dot{Q} + 2(\alpha_2 R_s) \dot{Q} + 2(\alpha_3 R_s) \ddot{R} + 2Q \\ &- \dot{S}^2 - S\ddot{S} - (1/Q_p) S\dot{S} \end{aligned} \quad (4.62)$$

Letting

$$\alpha = \frac{1}{2} e^{j(\nu\tau + \eta)} \quad (4.63)$$

$$X = -2jX(o)(\alpha^2 e^{-j2\psi} e^{j2\theta} - \alpha^{*2} e^{j2\psi} e^{-j2\theta})$$

$$S = -jS(o)(\alpha - \alpha^*)$$

$$Q = -2jQ(o)(\alpha^2 e^{-j2\psi} - \alpha^{*2} e^{j2\psi})$$

$$R = -2jR(o)(\alpha^2 e^{-j2\psi} e^{-j\phi} - \alpha^{*2} e^{j2\psi} e^{j\phi})$$

$$Y = -jY(o)(\alpha e^{-j\eta} - \alpha^* e^{j\eta})$$

X is the normalized input forcing function, of angular frequency 2ν .

Q is the normalized forcing function voltage developed across the varactor, of angular frequency 2ν .

R is the normalized output voltage, of angular frequency 2ν .

S is the normalized subharmonic voltage across the varactor, of angular frequency ν .

Y is the normalized output subharmonic voltage, of angular frequency ν .

Inserting these values into (4.62),

$$\begin{aligned}
 0 = & 4jX(o)(\alpha^2 e^{-j2\psi} e^{j2\theta} - \alpha^{*2} e^{j2\psi} e^{-j2\theta}) \\
 & + 16v^2 jQ(o)(\alpha^2 e^{-j2\psi} - \alpha^{*2} e^{j2\psi}) \\
 & - 16v^2 Q^2(o)(\alpha^2 e^{-j2\psi} + \alpha^{*2} e^{j2\psi})^2 \\
 & - 16v^2 Q^2(o)(\alpha^2 e^{-j2\psi} - \alpha^{*2} e^{j2\psi})^2 \\
 & + 8v(\alpha_2 L\omega_p + 1/Q_p)Q(o)(\alpha^2 e^{-j2\psi} + \alpha^{*2} e^{j2\psi}) \quad (4.64) \\
 & + 8v(\alpha_3 L\omega_p)R(o)(\alpha^2 e^{-j2\psi} e^{-j\phi} + \alpha^{*2} e^{j2\psi} e^{j\phi}) \\
 & + 8vj(1/Q_p)Q^2(o)(\alpha^2 e^{-j2\psi} - \alpha^{*2} e^{j2\psi})(\alpha^2 e^{-j2\psi} + \alpha^{*2} e^{j2\psi}) \\
 & - 4j(1 + \alpha_2 R_g)Q(o)(\alpha^2 e^{-j2\psi} - \alpha^{*2} e^{j2\psi}) \\
 & - 4j(\alpha_3 R_g)R(o)(\alpha^2 e^{-j2\psi} e^{-j\phi} - \alpha^{*2} e^{j2\psi} e^{j\phi}) \\
 & - v^2 S^2(o)(\alpha + \alpha^*)^2 \\
 & - v^2 S^2(o)(\alpha - \alpha^*)^2 \\
 & + j(v/Q_p)S^2(o)(\alpha - \alpha^*)(\alpha + \alpha^*)
 \end{aligned}$$

Again the effects due to higher order harmonics will be ignored, and the expanded driving equation solved by equating the coefficients of α^2 and α^{*2} to zero. The solutions to the resonant loop equation, the fundamental output equation and the subharmonic output equation, will be

inserted into equation (4.64) to reduce the number of unknowns. The result will produce $S(o)$ as a function of $X(o)$ and $Q(o)$, where $Q(o)$ has been previously found.

Rearranging equation (4.64) and solving for the coefficients of α^2 .

$$\begin{aligned}
 -4jX(o)e^{j2\theta} &= [8v(\alpha_2 L \omega_p + 1/Q_p) + 8v(\alpha_3 L \omega_p) \left[\frac{1-MH}{1+H^2} \right] + 4\alpha_3 R_s \left[\frac{M+H}{1+H^2} \right]] Q(o) \\
 &- \frac{2v^2 S^2(o) [1-K_1/(K_0 v Q_p)]}{\sqrt{1+(K_1/K_0)^2} \sqrt{1+(1/v Q_p)^2}} - \frac{(v/Q_p) S^2(o) [K_1/K_0 + 1/(v Q_p)]}{\sqrt{1+(K_1/K_0)^2} \sqrt{1+(1/v Q_p)^2}} \\
 &+ j \left[8v(\alpha_3 L \omega_p) \left[\frac{M+H}{1+H^2} \right] - 4(1+\alpha_2 R_s) - 4(\alpha_3 R_s) \left[\frac{1-MH}{1+H^2} \right] + 16v^2 \right] Q(o) \\
 &+ j \left[\frac{(v/Q_p) S^2(o) [1-K_1/(K_0 v Q_p)]}{\sqrt{1+(K_1/K_0)^2} \sqrt{1+(1/(v Q_p))^2}} - \frac{2v^2 S^2(o) [K_1/K_0 + 1/(v Q_p)]}{\sqrt{1+(K_1/K_0)^2} \sqrt{1+(1/(v Q_p))^2}} \right].
 \end{aligned}
 \tag{4.65}$$

Similarly one can derive the equation for the α^{*2} terms. This equation can be shown to be the conjugate of the above equation.

Combining equation (4.65) with its conjugate equation and rearranging the result gives:

$$16X^2(o) = [J_1 Q(o) - (I_1 + I_2) S^2(o)]^2 + [J_2 Q(o) + (I_3 - I_4) S^2(o)]^2
 \tag{4.66}$$

where the I 's and J 's are defined below (in equation (4.70) and (4.71)).

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Rearranging equation (4.66) gives:

$$[(I_3 - I_4)^2 + (I_1 + I_2)^2] S^4(\omega) + [2J_2 Q(\omega)(I_3 - I_4) - 2J_1 Q(\omega)(I_1 + I_2)] S^2(\omega) + (J_1 Q(\omega))^2 + (J_2 Q(\omega))^2 - 16X^2(\omega) = 0 \quad (4.67)$$

Solving this quadratic equation yields:

$$S^2(\omega) = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A} \quad (4.68)$$

where

$$\begin{aligned} A &= (I_3 - I_4)^2 + (I_1 + I_2)^2 \\ B &= 2J_2 Q(\tau)(I_3 - I_4) - 2J_1 Q(\tau)(I_1 + I_2) \\ C &= (J_1 Q(\tau))^2 + (J_2 Q(\tau))^2 - 16X^2(\tau) \end{aligned} \quad (4.69)$$

$$\begin{aligned} I_1 &= 2v^2 \cdot \{1 - K_1 / vK_o Q_p\} / J_3 \\ I_2 &= v \cdot \{K_1 / K_o + 1 / vQ_p\} / Q_p J_3 \end{aligned} \quad (4.70)$$

$$I_3 = v \cdot \{1 - K_1 / vK_o Q_p\} / Q_p J_3$$

$$I_4 = 2v^2 \cdot \{K_1 / K_o + 1 / vQ_p\} / J_3$$

$$\begin{aligned} J_1 &= 8v(\alpha_2 L \omega_p + 1 / Q_p) + 8v\alpha_3 L \omega_p F_1 + 4\alpha_3 R_s F_2 \\ J_2 &= 8v(\alpha_3 L \omega_p) F_2 - 4(\alpha_2 R_s + 1) - 4\alpha_3 R_s F_1 + 16v^2 \end{aligned} \quad (4.71)$$

$$J_3 = \sqrt{1 + (K_1 / K_o)^2} \cdot \sqrt{1 + (1 / vQ_p)^2}$$

$$K_o = 2v(\alpha_2 L \omega_p + 1 / Q_p) + 2v\alpha_1 \omega_p L F_3 + 2\alpha_1 R_s F_4 \quad (4.72)$$

$$K_1 = 2v^2 - 2(\alpha_2 R_s + 1) + 2v\alpha_1 \omega_p L F_4 - 2\alpha_1 R_s F_3$$

$$F_1 = (1 - MH) / (1 + H^2)$$

$$F_2 = (M + H) / (1 + H^2) \quad (4.73)$$

$$F_3 = (1 - PL) / (1 + P^2)$$

$$F_4 = (L + P) / (1 + P^2)$$

$$M = \alpha_2 / 2\gamma v$$

$$H = \alpha_3 / 2\gamma v$$

(4.74)

$$P = \alpha_1 / \gamma v$$

$$L = \alpha_2 / \gamma v$$

We have now solved the four frequency-halving nonlinear differential equations. In equation (4.68) the subharmonic signal, $S(o)$ has been evaluated as a function of the input pumping signal and the FET's characteristics.

In equation (4.46), the subharmonic output signal, $Y(o)$, has been derived in terms of the subharmonic signal, $S(o)$.

The next section will evaluate the amount of pumping voltage required to initiate subharmonic generation.

4.4 Analytical Solution to the Steady State Response

We will now evaluate the pumping voltage required to initiate frequency division. This pumping voltage will be plotted as a function of the normalized angular frequency v , and this plot will be called the (v, X) plane.

The boundary of the region of frequency halving on the (v, X) plane is found by setting $S(o) = 0$. Thus equation (4.68) becomes:

$$S^2(o) = 0 = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A}$$

Because: $A = 0$

then:

$$B = \sqrt{B^2 - 4AC}$$

or: $4AC = 0$

Now, since A is greater than zero, C must be equal to zero.

Therefore, from Equation (4.69) we have:

$$16 X^2(\omega) = \frac{4(J_1^2 + J_2^2)(K_0^2 + K_1^2)}{\omega^4 + (\omega/Q_p)^2} \quad (4.75)$$

Equation (4.75) defines the boundary where frequency division occurs. Given a normalized frequency, ω this equation gives the value of $X(\omega)$; below this value sub-harmonic generation will not occur. It can also be deduced from this equation that $X(\omega)$ follows a semi-parabolic shape in the (ω, X) plane.

A program has been written to calculate and plot the boundary region of unconditional frequency division. As observed in equation (4.75), using equations (4.71, 4.72), this boundary is very dependent on the parameters of the field effect transistor.

Figure 4.3 shows the effect on this boundary region as the field effect transistor's series resistance is altered. The table in the upper left-hand corner of the graph gives the FET characteristics which were used to simulate these curves.

In the (v, X) plane, the influence of the series resistance on the subharmonic threshold level is observed. As can be seen in this figure, the larger the series resistance, the greater input voltage required to initiate frequency-halving.

Figure 4.4 shows the influence of the gate to source voltage on the boundary region. Here the vertical coordinate is the pumping voltage (rather than the pumping voltage normalized to the gate-to-source bias voltage, X as used in most other figures). It can be readily observed that for a given input voltage, the bandwidth where subharmonic generation occurs is dependent on the bias voltage.

Although not apparent here, it should be noted that the gate-to-source bias voltage alters the point at which minimum threshold voltage will occur. This occurs because the normalizing frequency is bias dependent.

In Figure 4.5 the influence of the feedback capacitance can be observed. The FET's feedback capacitance has only a small effect on the subharmonic threshold curve.

A second program has been developed to calculate the frequency divider's voltage gain as a function of the input frequency, for a fixed driving voltage; using equations (4.68) and (4.46).

In Figure 4.6 the voltage gain as a function of the halving frequency is observed, with the load resistance as a parameter. This behaviour can be easily predicted since the smaller the load resistance the smaller will be the voltage gain.

In Figure 4.7 the influence of the gate-to source voltage on the voltage gain is observed. The gate-to-source voltage significantly alters the bandwidth where subharmonic generation occurs. Also the bias voltage increases the voltage gain at the expense of decreasing the frequency-halving bandwidth. This behaviour occurs because the larger the gate-to-source bias voltage, the smaller its capacitance. Hence the capacitor supports a greater fraction of the input voltage across it than the input inductor.

Finally the voltage gain as a function of the feedback capacitance is shown in Figure 4.8. The small influence of the feedback capacitance can be observed.

An approximate expression for the conversion from pumping voltage to input power (P_{IN}) is easily derived and is shown below.

$$P_{IN} = \frac{4 v_p^2 R_s}{[R_s^2 + 4(\omega_p \cdot v \cdot L)^2 (1 - 1/(2v)^2)^2]} \quad (4.76)$$

Figure 4.3. Boundary region of unconditional frequency halving as a function of the series resistance.

Figure 4.4. Boundary region of unconditional frequency halving as a function of the gate to source voltage.

Figure 4.5 Boundary region of unconditional frequency halving as a function of the feedback capacitance.

Figure 4.6. Voltage gain versus halving frequency as a function of the load resistance.

Figure 4.7. Voltage gain versus halving frequency as a function of the gate to source voltage.

Figure 4.8. Voltage gain versus halving frequency as a function of the feedback capacitance.

CHAPTER 5

PHASE DETECTOR

The requirements for realizing a phase detector and a frequency halver have been outlined in Chapter 3. The frequency halver was theoretically analyzed in the previous chapter, where a detailed understanding of its operation was revealed.

An analysis of the phase detector proposed in Chapter 3, will now be performed in this chapter.

All systems which require some form of locking to a reference or synthesizer must have a phase detecting capability. A phase detector is one form of a mixer, in which two signals are nonlinearly combined. As in a mixer, the phase detector will produce signals at frequencies which are sums and differences of the frequencies of the two input signals. However when the two signals differ only in phase, the phase detector will produce a dc signal which is dependent on the phase difference.

5.1 Phase Detector Model

The phase detector which is to be analyzed has been introduced in Chapter 3. This novel phase detector is shown in Fig. 5.1(a). It consists of two separate field effect transistors (FETs) which are connected by attaching the source

terminal of the upper FET to the drain terminal of the lower FET. The two input signals are presented separately to the gates of the FET's. This configuration isolates the two input signals from each other. When the phase detector is biased on, the common terminal of the two FETs is a D.C. floating point. Through the analysis presented, it will be shown that this terminal can be used as the phase detector output.

The phase detector equivalent circuit is shown in Fig. 5.1(b). The Curtice GaAs MESFET model [72] has been used to represent the nonlinearities. The principal nonlinear effects are: (a) the gate-to-source Schottky-barrier capacitance and, (b) the drain-to-source current.

The gate-to-source capacitance is modelled as:

$$C_{gs}(\bar{V}_{gs}) = C_{gs} (1 - \bar{V}_{gs} / \phi_0)^{-1/2} \quad (5.1)$$

and the drain-to-source current is modelled by [72]:

$$I_{ds}(\bar{V}_{gs}, \bar{V}_{ds}) = \beta (\bar{V}_{gs} - V_T)^2 (1 + \lambda \bar{V}_{ds}) \tanh(\alpha \bar{V}_{ds}) \quad (5.2)$$

where

ϕ_0 is the built in potential

C is the gate-to-source capacitance at zero bias

β is the transconductance parameter

V_T is the threshold voltage

λ is the channel length modulation parameter

α is the hyperbolic tangent function parameter

$\bar{V}_{gs}$ is the total forward voltage between the gate and source

$\bar{V}_{ds}$ is the total forward voltage between the drain and source

Figure 5.1. (a) Phase Detector; (b) Phase Detector's Equivalent Circuit.

5.2 Formulation of Differential Equation

To simplify the analysis of the phase detector, we will assume that the feedback capacitance C_F is negligible. This is generally the case except at high frequency, where C_F can be significant. We begin by using the nonlinear equations (5.1) and (5.2), in the phase detector circuit representation in Figure 5.1(b). Summing currents at the common node in Figure 5.1(b) yields

$$\begin{aligned}
 0 = & C(1 - \frac{v_1 + V_1 - v_3 - V_3}{\phi_0}) \cdot d/dt(v_1 + V_1 - v_3 - V_3) \\
 & + \beta(v_1 + V_1 - v_3 - V_3 - V_T)^2(1 + \lambda(V_{ds} - v_3 - V_3))\tanh(\alpha(V_{ds} - v_3 - V_3)) \\
 & - \beta(v_2 + V_2 - V_T)^2(1 + \lambda(v_3 + V_3))\tanh(\alpha(v_3 + V_3)) \\
 & - 1/R_L \cdot (v_3 + V_3)
 \end{aligned} \tag{5.3}$$

where

$v_{1,2,3}$ are the sinusoidal small signals

$V_{1,2,3}$ are the direct current signals.

The input signals will be represented as:

$$\begin{aligned}
 v_1 &= |v_1| \sin(\omega t) \\
 v_2 &= |v_2| \sin(\omega t + \phi)
 \end{aligned} \tag{5.4}$$

and ignoring higher order harmonics, the output signal will be assumed to be:

$$v_3 = |v_{3s}| \sin \omega t + |v_{3c}| \cos \omega t \tag{5.5}$$

To simplify the analysis of equation (5.3), we will normalize the voltage terms as well as the coefficients.

Normalizing provides:

$$\begin{aligned} X_0 &= V_1/\phi_0, X = |v_1|/\phi_0, Y_0 = V_2/\phi_0, Y = |v_2|/\phi_0 \\ Z_0 &= V_3/\phi_0, Z_s = |v_{3s}|/\phi_0, Z_c = |v_{3c}|/\phi_0, D = V_{ds}/\phi_0 \\ K &= V_T/\phi_0, \beta_0 = \beta\phi_0^2, \alpha_0 = \alpha\phi_0, C_0 = C\phi_0 \\ g_L &= \phi_0/R_L, \lambda_0 = \lambda\phi_0 \end{aligned} \quad (5.6)$$

Rewriting equation (5.3) gives:

$$\begin{aligned} &C_0(1-X'+Z')^{-1} \cdot d/dt(X'-Z') + \beta_0(X'-Z'-K)^2(1+\lambda_0[D-Z'] \cdot \tanh(\alpha_0[D-Z'])) \\ &- \beta_0(Y'-K)^2(1+\lambda_0 Z') \tanh(\alpha_0 Z') - g_L Z' = 0 \end{aligned} \quad (5.7)$$

where $X' = X_0 + X \sin(\omega t)$

$$Y' = Y_0 + Y \sin(\omega t + \phi) \quad (5.8)$$

$$Z' = Z_0 + Z_s \sin(\omega t) + Z_c \cos(\omega t)$$

The normalized equations (5.7) and (5.8) define the behaviour of the phase detector.

5.3 Analytical Solution

Having defined the nonlinear phase detector equation, we can now extract the solution for each term in the differential equation (5.7) for Z' .

The differential equation (5.7) is solved using the Ritz Method [73], whereby the coefficients of the Z' equation are obtained using the following relations:

$$\int_0^{2\pi} \xi(Z', X', Y') d(\omega t) = 0 \quad (5.9)$$

$$\int_0^{2\pi} \xi(Z', X', Y') \sin(\omega t) d(\omega t) = 0 \quad (5.10)$$

$$\int_0^{2\pi} \xi(Z', X', Y') \cos(\omega t) d(\omega t) = 0 \quad (5.11)$$

where $\xi(Z', X', Y')$ is equation (5.7)

In the above, Equation (5.9) separates the dc component from the sinusoidal signals, Equation (5.10) calculates the output coefficient of the odd function, and equation (5.11) calculates the output coefficient of the even function.

The dc output term called the dc Ritz equation, will be obtained first. Defining the left hand side of equation (5.7) as the Ritz function ξ , gives:

$$\begin{aligned} \xi(Z', X', Y') = & C_0 \cdot (1 - X' + Z')^{-1} \cdot d/dt(X' - Z') \\ & + \beta_0 (X' - Z' - K)^2 (1 + \lambda_0 [D - Z']) \cdot \tanh(\alpha_0 [D - Z']) \quad (5.12) \\ & - \beta_0 (Y' - K)^2 (1 + \lambda_0 Z') \cdot \tanh(\alpha_0 Z') - g_L Z' \end{aligned}$$

The integral for each of the four terms on the right-hand side of the Ritz function (5.12), will be independently solved. The first term of equation (5.12) can be expanded and integrated to give:

$$\text{1st term} = I_1^{Z_0} = \int_0^{2\pi} \frac{\omega C_0 [(X-Z_s)\cos\omega t + Z_c \sin\omega t] d(\omega t)}{[1-X_0+Z_0+(Z_s-X)\sin\omega t + Z_c \cos\omega t]^{\frac{1}{2}}} \quad (5.13)$$

To simplify this function we will use the first three terms of the binomial approximation,

$$(1+X)^{-\frac{1}{2}} = 1 - \frac{1}{2}X + \frac{3}{8}X^2 \quad (5.14)$$

Integrating out periodic terms we have:

$$I_1^{Z_0} = \frac{-\omega C_0}{\sqrt{1-X_0+Z_0}} \int_0^{2\pi} \left[\frac{(X-Z_s)Z_c}{4(1-X_0+Z_0)} + \frac{(Z_s-X)Z_c}{4(1-X_0+Z_0)} \right] d(\omega t) \quad (5.15)$$

Solving yields:

$$I_1^{Z_0} = 0 \quad (5.16)$$

Thus, the first term of dc Ritz equation equals zero. We will now solve the second term of the dc Ritz equation, which we define as:

$$\text{2nd Term} = I_2^{Z_0}$$

where:

$$I_2^{Z_0} = \int_0^{2\pi} B_0 (X_0 - Z_0 - K + (X-Z_s)\sin\omega t - Z_c \cos\omega t)^2 (1 + \lambda_0 D - \lambda_0 Z_0 - \lambda_0 Z_s \sin\omega t - \lambda_0 Z_c \cos\omega t) \cdot \tanh(\alpha_0 D - \alpha_0 Z_0 - \alpha_0 Z_s \sin\omega t - \alpha_0 Z_c \cos\omega t) d(\omega t) \quad (5.17)$$

For the tanh function we will assume:

$$D - Z_o \Rightarrow Z_s \sin \omega t + Z_c \cos \omega t \quad (5.18)$$

and use

$$\tanh X = \frac{1 - e^{-2X}}{1 + e^{-2X}}$$

Hence, expanding equation (5.17) we have,

$$I_2^{Z_o} = \frac{1 - e^{-2\alpha_o(D - Z_o)}}{1 + e^{-2\alpha_o(D - Z_o)}} \int_0^{2\pi} \left[\begin{aligned} &(1 + \lambda_o D - \lambda_o Z_o) \left[\beta_o (X_o - Z_o - K)^2 + \frac{1}{2} \beta_o (X - Z_s)^2 + \frac{1}{2} \beta_o Z_c^2 \right] \\ &- \lambda_o Z_s \left[\frac{1}{2} \beta_o (X_o - Z_o - K)(X - Z_s) + \frac{1}{2} \beta_o (X_o - Z_o - K)(X - Z_s) \right] \\ &- \lambda_o Z_c \left[-\frac{1}{2} \beta_o (X_o - Z_o - K)Z_c - \frac{1}{2} \beta_o (X_o - Z_o - K)Z_c \right] \end{aligned} \right] d(\omega t) \quad (5.19)$$

Integrating this equation gives:

$$I_2^{Z_o} = \frac{1 - e^{-2\alpha_o(D - Z_o)}}{1 + e^{-2\alpha_o(D - Z_o)}} \cdot 2\pi \cdot \left[\begin{aligned} &(1 + \lambda_o D - \lambda_o Z_o) \left[\beta_o (X_o - Z_o - K)^2 + \frac{1}{2} \beta_o (X - Z_s)^2 + \frac{1}{2} \beta_o Z_c^2 \right] \\ &- \lambda_o \beta_o Z_s (X_o - Z_o - K)(X - Z_s) + \lambda_o \beta_o Z_c^2 (X_o - Z_o - K) \end{aligned} \right] \quad (5.20)$$

This equation defines the second term of the dc Ritz equation.

We can now define the third term of the dc Ritz equation as:

$$3^{rd} \text{ term} = I_3^{Z_o}$$

where:

$$I_3^{Z_o} = \int_0^{2\pi} -\beta_o (Y_o + Y_s \sin(\omega t + \phi) - K)^2 (1 + \lambda_o Z_o + \lambda_o Z_s \sin \omega t + \lambda_o Z_c \cos \omega t) \cdot \tanh(\alpha_o [Z_o + Z_s \sin \omega t + Z_c \cos \omega t]) d(\omega t) \quad (5.21)$$

Using the previously mentioned approximation for the tanh function, we have:

$$I_3 Z_0 = \frac{1 - e^{-2\alpha_0 Z_0}}{1 + e^{-2\alpha_0 Z_0}} \cdot 2\pi \int_0^{2\pi} \left[\beta_0 [(1 + \lambda_0 Z_0) [(Y_0 - K) + \frac{1}{2} Y^2] + \lambda_0 Z_s [(Y_0 - K) Y \cos \phi] + \lambda_0 Z_c (Y_0 - K) Y \sin \phi] d(\omega t) \right] \quad (5.22)$$

Integrating,

$$I_3 Z_0 = - \frac{1 - e^{-2\alpha_0 Z_0}}{1 + e^{-2\alpha_0 Z_0}} \cdot 2\pi \beta_0 \left[(1 + \lambda_0 Z_0) [(Y_0 - K)^2 + \frac{1}{2} Y^2] + \lambda_0 Z_s (Y_0 - K) Y \cos \phi + \lambda_0 Z_c (Y_0 - K) Y \sin \phi \right] \quad (5.23)$$

This equation is the solution to the third term of the dc Ritz equation.

Finally, we define the fourth term of the dc Ritz equation as:

$$4^{th} \text{ Term} = I_4 Z_0$$

where:

$$I_4 Z_0 = \int_0^{2\pi} -g_L [Z_0 + Z_s \sin \omega t + Z_c \cos \omega t] d(\omega t) \quad (5.24)$$

Solving:

$$I_4 Z_0 = -2\pi g_L Z_0 \quad (5.25)$$

This provides solution of the fourth term of the dc Ritz equation.

We now have completed the integration of the four terms which comprise the dc Ritz equation. To complete the solution of the dc Ritz equation the four terms are summed and equated to zero,

$$I_1 Z_o + I_2 Z_o + I_3 Z_o + I_4 Z_o = 0 \quad (5.26)$$

This concludes the derivation of the dc Ritz equation. The odd-term defining equation (5.10) called the odd function Ritz equation, will now be solved.

Rewriting (5.10):

$$\int_0^{2\pi} \xi(Z', X', Y') \sin \omega t \, d(\omega t) = 0$$

Following a similar approach as for the dc Ritz equation, we define:

$$1^{st} \text{ Term} = I_1 Z_s$$

where:

$$I_1 Z_s = \int_0^{2\pi} \frac{C_o \sin \omega t [(X - Z_s) \omega \cos \omega t + Z_c \omega \sin \omega t]}{[(1 - X_o + Z_o) + (Z_s - X) \sin \omega t + Z_c \cos \omega t]^{\frac{1}{2}}} d(\omega t) \quad (5.27)$$

Using a binomial expansion, we can let: (as before, eq. 5.14)

$$(1+X)^{-\frac{1}{2}} \approx 1 - \frac{1}{2}X + \frac{3}{8}X^2$$

Integrating (5.27) we get:

$$I_1 Z_s = \frac{2\pi \omega C_o}{\sqrt{1 - X_o + Z_o}} \left[\frac{1}{2} Z_c + \frac{9}{64} \frac{Z_c (Z_s - X_o)^2}{(1 - X_o + Z_o)^2} + \frac{3}{64} \frac{Z_c^3}{(1 - X_o + Z_o)^2} - \frac{3}{32} \frac{(Z_s - X_o) Z_c}{(1 - X_o + Z_o)^2} \right] \quad (5.29)$$

We can define the second term as:

$$2^{nd} \text{ Term} = I_2 Z_s$$

where:

$$I_2 Z_s = \int_0^{2\pi} \left[\beta_o (X_o + X \sin \omega t - Z_o - Z_s \sin \omega t - Z_c \cos \omega t - K)^2 \cdot (1 + \lambda_o D - \lambda_o Z_o - \lambda_o Z_s \sin \omega t - \lambda_o Z_c \cos \omega t) \tanh \alpha_o [D - Z_o - Z_s \sin \omega t - Z_c \cos \omega t] \sin \omega t \, d(\omega t) \right] \quad (5.30)$$

Solving provides:

$$I_2^Z = \frac{1-e^{-2\alpha_0(D-Z_0)}}{1+e^{-2\alpha_0(D-Z_0)}} \cdot 2\pi\beta_0 \cdot \left[\begin{aligned} &(X_0-Z_0-K)(X-Z_s)(1+\lambda_0[D-Z_0]) \\ &-\frac{1}{2}\lambda_0 Z_s [(X_0-Z_0-K)^2 + \frac{1}{2}(X-Z_s)^2 + \frac{1}{2}Z_c^2] \\ &-\frac{1}{8}\lambda_0 Z_s (X-Z_s)^2 + \frac{1}{8}\lambda_0 Z_c^2 Z_s + \frac{1}{4}\lambda_0 Z_c^2 (X-Z_s) \end{aligned} \right] \quad (5.31)$$

We can now define the third term as:

$$3^{rd} \text{ Term} = I_3^{\Delta Z_s}$$

where:

$$I_3^Z = \int_0^{2\pi} -\beta_0 (Y'-K)^2 (1+\lambda_0 Z') \tanh \alpha_0 Z' \cdot \sin \omega t \, d(\omega t) \quad (5.32)$$

Solving this equation, similarly to the previous derivations yields:

$$I_3^Z = \frac{1-e^{-2\alpha_0 Z_0}}{1+e^{-2\alpha_0 Z_0}} (-2\pi\beta_0) \left[\begin{aligned} &Y(Y_0-K)(1+\lambda_0 Z_0) \cos \phi + \frac{1}{2}\lambda_0 Z_s (Y_0-K)^2 \\ &+\frac{1}{4}\lambda_0 Z_s Y^2 + \frac{1}{8}\lambda_0 Y^2 Z_s \cos 2\phi + \frac{1}{8}Y^2 \lambda_0 Z_c \sin 2\phi \end{aligned} \right] \quad (5.33)$$

We define the fourth term as:

$$4^{th} \text{ Term} = I_4^{\Delta Z_s}$$

where:

$$I_4^Z = \int_0^{2\pi} -g_L (Z_0 + Z_s \sin \omega t + Z_c \cos \omega t) \sin \omega t \, d(\omega t) \quad (5.34)$$

Solving gives:

$$I_4^Z = -g_L \cdot \pi \cdot Z_s \quad (5.35)$$

The values for the four terms of the odd function Ritz equation have now been derived. To complete this derivation we equate the summation of the four terms to zero:

$$I_1^{Z_s} + I_2^{Z_s} + I_3^{Z_s} + I_4^{Z_s} = 0 \quad (5.36)$$

We will now solve the third Ritz equation, which is called the even function Ritz equation. Again, we separate the Ritz function into four terms and integrate each term separately. These terms are then combined to produce the solution.

Following a similar approach to that for the odd function Ritz equation, we define the first term as:

$$1^{st} \text{ Term} = I_{10}^{Z_c}$$

where:

$$I_{10}^{Z_c} = \int_0^{2\pi} \frac{C_0 \cos \omega t [(X - Z_s) \omega \cos \omega t + Z_c \omega \sin \omega t]}{[(1 - X_0 + Z_0) + (Z_s - X) \sin \omega t + Z_c \cos \omega t]^{\frac{1}{2}}} d(\omega t) \quad (5.37)$$

Using the binomial expansion:

$$(1+X)^{-\frac{1}{2}} = 1 - \frac{1}{2}X + \frac{3}{8}X^2 \quad (5.38)$$

Yields the solution:

$$I_{10}^{Z_c} = \frac{2\pi \omega C_0}{\sqrt{1 - X_0 + Z_0}} \left[\frac{1}{2}(X - Z_s) + \frac{3}{64}(X - Z_s) \left(\frac{Z_s - X}{1 - X_0 + Z_0} \right)^2 + \frac{9}{64}(X - Z_s) \left(\frac{Z_c}{1 - X_0 + Z_0} \right)^2 \right. \\ \left. + \frac{6}{64} Z_c^2 \frac{(Z_s - X)}{(1 - X_0 + Z_0)^2} \right] \quad (5.39)$$

We have solved for the first term of the even function Ritz equation.

We can now proceed to solve the second term of the even function Ritz equation, which we define as:

$$2^{\text{nd}} \text{ Term} = I_2^{Z_c}$$

where:

$$I_2^{Z_c} = \int_0^{2\pi} \left[\beta_0 (X' - Z' - K)^2 (1 + \lambda_0 [D - Z']) \tanh \alpha_0 [D - Z'] \cdot \cos \omega t \right] d(\omega t) \quad (5.40)$$

Solving:

$$I_2^{Z_c} = \frac{1 - e^{-2\alpha_0(D-Z_0)}}{1 + e^{-2\alpha_0(D-Z_0)}} \cdot 2\pi\beta_0 \cdot \left[\begin{aligned} & -Z_c(X_0 - Z_0 - K)(1 + \lambda_0[D - Z_0]) + \frac{1}{8}\lambda_0 Z_8 Z_c(X - Z_8) \\ & - \frac{1}{8}\lambda_0 Z_c(X_0 - Z_0 - K)^2 - \frac{1}{8}\lambda_0 Z_c(X - Z_8)^2 - \frac{3}{8}\lambda_0 Z_c^3 \end{aligned} \right] \quad (5.41)$$

This is the solution for the second term of the even function Ritz equation.

We can now define the third term of the even function Ritz equation as:

$$3^{\text{rd}} \text{ Term} = I_3^{Z_c}$$

where:

$$I_3^{Z_c} = \int_0^{2\pi} \left[-\beta_0 (Y' - K)^2 (1 + \lambda_0 Z') \tanh(\alpha_0 Z') \cdot \cos \omega t \right] d(\omega t) \quad (5.42)$$

Solving 5.42 yields:

$$I_3^{Z_c} = -\frac{1 - e^{-2\alpha_0 Z_0}}{1 + e^{-2\alpha_0 Z_0}} \cdot 2\pi\beta_0 \cdot \left[\begin{aligned} & (Y_0 - K)Y(1 + \lambda_0 Z_0) \sin \phi + \frac{1}{8}\lambda_0 Z_8 Y^2 \sin 2\phi \\ & + \frac{1}{8}\lambda_0 Z_0 (Y_0 - K)^2 + \frac{1}{8}\lambda_0 Z_c Y^2 - \frac{1}{8}\lambda_0 Z_c Y^2 \cos 2\phi \end{aligned} \right] \quad (5.43)$$

The solution to the third term is given in (5.43). We now proceed to solve the fourth term of the even function Ritz equation, which we define as:

$$4^{\text{th}} \text{ Term} = I_4^{Z_c}$$

where:

$$I_4^{Z_c} = \int_0^{2\pi} -g_L (Z_0 + Z_g \sin \omega t + Z_c \cos \omega t) \cdot \cos \omega t \, d(\omega t) \quad (5.44)$$

This yields:

$$I_4^{Z_c} = -g_L \cdot \pi \cdot Z_c \quad (5.45)$$

Equation (5.45) shows the integrated fourth term of the even function Ritz equation. We can now combine the four integrated terms of the even function Ritz equation, and equate the summation to zero. Adding the four terms, we have

$$I_1^{Z_c} + I_2^{Z_c} + I_3^{Z_c} + I_4^{Z_c} = 0 \quad (5.46)$$

This completes the derivation using the Ritz method. We have reduced the three Ritz integrals to three algebraic equations in three unknowns. The three unknowns are Z_0 , Z_g and Z_c , which are the normalized dc output, the output's normalized odd function coefficient, and the output's normalized even function coefficient, respectively.

We now proceed to rewrite the three evaluated Ritz equations in their expanded form. Using equation (5.26) along with the four terms (5.16), (5.20), (5.23) and (5.25), we can rewrite this equation in its expanded form as:

$$\frac{1-e^{-2\alpha_0(D-Z_0)}}{1+e^{-2\alpha_0(D-Z_0)}} \left[2\pi \cdot \begin{aligned} & (1+\lambda_0 D - \lambda_0 Z_0) [\beta_0 (X_0 - Z_0 - K)^2 + \frac{1}{2} \beta_0 (X - Z_s)^2 + \frac{1}{2} \beta_0 Z_c^2] \\ & - \lambda_0 Z_s \beta_0 (X_0 - Z_0 - K)(X - Z_s) + \lambda_0 Z_c \beta_0 (X_0 - Z_0 - K) Z_c \end{aligned} \right]$$

$$- \frac{1-e^{-2\alpha_0 Z_0}}{1+e^{-2\alpha_0 Z_0}} \cdot 2\pi \beta_0 \cdot \left[\begin{aligned} & (1+\lambda_0 Z_0) [(Y_0 - K)^2 + \frac{1}{2} Y^2] + \lambda_0 Z_s (Y_0 - K) Y \cos \phi \\ & + \lambda_0 Z_c (Y_0 - K) Y \sin \phi \end{aligned} \right]$$

$$- 2\pi g_L Z_0 = 0 \quad (5.47)$$

Similarly using equation (5.36) along with its four terms (5.29), (5.31) and (5.35), we can rewrite the solution to this odd function Ritz equation as:

$$\frac{2\pi \omega C_0}{\sqrt{1-X_0+Z_0}} \left[\frac{Z_c}{2} + \frac{9}{64} \cdot \frac{(Z_s - X)^2}{(1-X_0+Z_0)^2} + \frac{3}{64} \frac{Z_c^3}{(1-X_0+Z_0)^2} - \frac{3}{32} \frac{(X-Z_s)^2 Z_c}{(1-X_0+Z_0)^2} \right]$$

$$+ \frac{1-e^{-2\alpha_0(D-Z_0)}}{1+e^{-2\alpha_0(D-Z_0)}} \cdot (2\pi \beta_0) \cdot \left[\begin{aligned} & (X_0 - Z_0 - K)(X - Z_s)(1+\lambda_0[D-Z_0]) - \frac{1}{2} \lambda_0 [(X_0 - Z_0 - K)^2 \\ & + \frac{1}{2} (X - Z_s)^2 + \frac{1}{2} Z_c^2] - \frac{1}{8} \lambda_0 Z_s (X - Z_s)^2 + \frac{1}{8} \lambda_0 Z_s Z_c^2 \\ & + \frac{1}{4} \lambda_0 Z_c^2 (X - Z_s) \end{aligned} \right]$$

$$+ \frac{1-e^{-2\alpha_0 Z_0}}{-2\alpha_0 Z} \cdot (2\pi \beta_0) \cdot \left[\begin{aligned} & (Y_0 - K) Y (1+\lambda_0 Z_0) \cos \phi + \frac{1}{2} \lambda_0 Z_s (Y_0 - K)^2 + \frac{1}{2} \lambda_0 Z_s Y^2 \\ & \frac{1}{8} Y \lambda_0 Z_s \cos 2\phi + \frac{1}{8} Y^2 \lambda_0 Z_0 \sin 2\phi \end{aligned} \right]$$

$$- g_L \pi Z_s = 0 \quad (5.48)$$

Similarly, we can expand the solution to the even function Ritz equation (5.46), using the terms (5.39), (5.41), (5.43) and (5.45).

$$\frac{2\pi\omega C_0}{\sqrt{1-X_0+Z_0}} \cdot \left[\frac{1}{2}(X-Z_s) + \frac{3}{64}(X-Z_s) \left(\frac{Z_s-X}{1-X_0+Z_0} \right)^2 + \frac{9}{64}(X-Z_s) \left(\frac{Z_c}{1-X_0+Z_0} \right)^2 \right] \\ + \frac{6}{64}Z_c \left(\frac{Z_s-X}{1-X_0+Z_0} \right) \left(\frac{Z_c}{1-X_0+Z_0} \right)$$

$$+ \frac{1-e^{-2\alpha_0(D-Z_0)}}{1+e^{-2\alpha_0(D-Z_0)}} \cdot 2\pi\beta_0 \cdot \left[-Z_c(X_0-Z_0-K)(1+\lambda_0[D-Z_0]) + \frac{1}{4}\lambda_0 Z_s Z_c (X-Z_s) \right. \\ \left. - \frac{1}{2}\lambda_0 Z_c (X_0-Z_0-K)^2 - \frac{1}{8}\lambda_0 Z_c (X-Z_s)^2 - \frac{3}{8}\lambda_0 Z_c^3 \right]$$

$$\frac{1-e^{-2\alpha_0 Z_0}}{1+e^{-2\alpha_0 Z_0}} \cdot 2\pi\beta_0 \cdot \left[(Y_0-K)Y(1+\lambda_0 Z_0)\sin\phi + \frac{1}{8}\lambda_0 Z_s Y^2 \sin 2\phi \right. \\ \left. + \frac{1}{2}\lambda_0 Z_c (Y_0-K)^2 + \frac{1}{4}\lambda_0 Z_c Y^2 - \frac{1}{4}\lambda_0 Z_c Y^2 \cos 2\phi \right]$$

$$-g_L \cdot \pi \cdot Z_c = 0$$

(5.49)

These last three equations are the expanded forms of the solution to the dc Ritz equation, the odd function Ritz equation and the even function Ritz equation. To simplify these equations let the hyperbolic tangent function, $\alpha_0 Z_0$ assumed to be large [72]. The dc Ritz equation (5.47) then reduces to:

$$\begin{aligned}
 & (1 + \lambda_o D - \lambda_o Z_o) [\beta_o (X_o - Z_o - K)^2 + \frac{1}{4} \beta_o (X - Z_s)^2 + \frac{1}{4} \beta_o Z_c^2] \\
 & - \lambda_o Z_s \beta_o (X_o - Z_o - K)(X - Z_s) + \lambda_o Z_c^2 \beta_o (X_o - Z_o - K) \\
 & - \beta_o (1 + \lambda Z_o) [(Y_o - K)^2 + \frac{1}{4} Y^2] - \beta_o \lambda_o Z_s (Y_o - K) Y \cos \phi \\
 & - \beta_o \lambda_o Z_c (Y_o - K) Y \sin \phi - \frac{g_L \cdot Z_o}{\tanh \alpha_o Z_o} = 0
 \end{aligned} \tag{5.50}$$

Similarly the odd function Ritz equation reduces to:

$$\begin{aligned}
 & [\omega C_o / \sqrt{1 - X_o + Z_o}] (Z_c / 2) + \beta_o (X_o - Z_o - K)(X - Z_s)(1 + \lambda_o [D - Z_o]) \\
 & - \beta_o \lambda_o (Z_s / 2) [(X_o - Z_o - K)^2 + \frac{1}{4} (X - Z_s)^2 + \frac{1}{4} Z_c^2] - \frac{1}{8} \beta_o \lambda_o Z_s (X - Z_s)^2 \\
 & + \frac{1}{8} \beta_o \lambda_o Z_s Z_c^2 + \frac{1}{4} \beta_o \lambda_o Z_c^2 (X - Z_s) - \beta_o (Y_o - K) Y (1 + \lambda_o Z_o) \cos \phi \\
 & - \frac{1}{4} \beta_o \lambda_o Z_s (Y_o - K)^2 - \frac{1}{4} \beta_o \lambda_o Z_s Y^2 - \frac{1}{8} \beta_o Y^2 \lambda_o Z_s \cos 2\phi \\
 & - \frac{1}{8} \beta_o Y^2 \lambda_o Z_c \sin 2\phi = 0
 \end{aligned} \tag{5.51}$$

Also, the even function Ritz equation reduces to:

$$\begin{aligned}
 & [\omega C_o / \sqrt{1 - X_o + Z_o}] [(X - Z_s) / 2] - \beta_o Z_c (X_o - Z_o - K)(1 + \lambda_o [D - Z_o]) \\
 & + \frac{1}{4} \beta_o \lambda_o Z_s Z_c (X - Z_s) - \frac{1}{4} \beta_o \lambda_o Z_c (X_o - Z_o - K)^2 - \frac{1}{8} \beta_o \lambda_o Z_c (X - Z_s)^2 \\
 & - \frac{3}{8} \beta_o \lambda_o Z_c^3 - \beta_o (Y_o - K) Y (1 + \lambda_o Z_o) \sin \phi - \frac{1}{8} \beta_o \lambda_o Z_s Y^2 \sin 2\phi \\
 & - \frac{1}{4} \beta_o \lambda_o Z_c (Y_o - K)^2 - \frac{1}{4} \beta_o \lambda_o Z_c Y^2 + \frac{1}{4} \beta_o \lambda_o Z_c Y^2 \cos 2\phi = 0
 \end{aligned} \tag{5.52}$$

To summarize the analytical solution of the phase detector, we began by assuming nonlinearities in the gate-to-source varactor and in the drain-to-source current. From the equations which described these nonlinearities, we formulated an equation which describes the phase detector behaviour. Two sinusoidal inputs which differed only in phase were applied, and with these inputs we assumed an output signal which contained a dc term plus a sinusoidal term and a cosinusoidal term. After normalizing the phase detector equation we then applied the Ritz Method. The Ritz Method required three weighted integral equations. Each of these equations were solved, and after some simplifications they were formulated in (5.50), (5.51) and (5.52).

The three equations obtained using the Ritz Method have three unknowns (Z_o, Z_s, Z_c) which are the coefficients of the normalized output signal. We now proceed to solve for the three unknowns.

Using equations (5.51) and (5.52) and neglecting second order terms such as Z_c^2 , Z_s^2 , Y^2 and X^2 , we can rearrange these equations and solve for Z_c and Z_s :

$$Z_c = (2B_o / \omega C_o) \sqrt{1 - X_o + Z_o} (Y_o - K) Y \cdot \left[\frac{\cos \phi - 2(B_o / \omega C_o) \sqrt{1 - X_o + Z_o} (X_o - Z_o - K) \sin \phi}{1 + (2B_o / \omega C_o)^2 (1 - X_o + Z_o) (X_o - Z_o - K)^2} \right] \quad (5.53)$$

$$(X - Z_s) = (2B_o / \omega C_o) \sqrt{1 - X_o + Z_o} [(Y_o - K) Y \sin \phi + Z_c (X_o - Z_o - K)] \quad (5.54)$$

From the evaluation of the Z_c and Z_s terms in equations (5.53) and (5.54), we can insert these values into equation (5.50) and solve for Z_o . After some mathematical manipulation we derive the equation:

$$0 = F(Z_o) - K(Z_o) \cos [\phi - \theta_o] \quad (5.55)$$

where:

$$F(Z_o) = (1 + \lambda_o D_o)(B_o - K)^2 - (1 + \lambda_o Z_o)(\frac{1}{2}Y^2 + C_o'^2) + \frac{1}{2}I_o A_o^2(1 - B_o)C_o'^2 Y^2 (J+1) \\ + \lambda_o A_o^2(1 - B_o)(B_o - K)/(1+J) - \frac{g_L \cdot Z_o}{\tanh \alpha_o Z_o}$$

$$K(Z_o) = - \lambda_o C_o' XY \frac{(1+2J)}{(1+J)} \sqrt{1 + J/(1+2J)^2} \quad (5.56)$$

$$\theta_o = \tan^{-1} (\sqrt{J}/(1+2J))$$

where:

$$A_o = 2\beta_o / \omega C_o$$

$$B_o = X_o - Z_o$$

$$C_o' = Y_o - K$$

$$D_o = D - Z_o$$

$$J = A_o^2(1 - B_o)(B_o - K)^2$$

$$I_o = 1 + \lambda_o D_o + 2\lambda_o B_o - 2\lambda_o K$$

Equation (5.55) can be solved iteratively to obtain the normalized dc output voltage Z_o as a function of ϕ .

Equation (5.55) describes the behaviour of the phase detector. This equation is the climax of all the previous derivations. The dc output voltage from the phase detector is calculated as a function of the phase difference between the two input signals. The next section derives the peak-to-peak dc output voltage change for a given phase variation.

Numerical Justification for Approximations

Typical parameters of the FETs used in the monolithic phase detector are:

$$\lambda = .084, K = -4.286, C_0 = 4.76E-13, \beta = .00414, \theta_2 = .001, \alpha_0 = 1.4$$

The externally applied signals are defined as:

$$X = 1.0, Y = 1.0, X_0 = -1.1, Y_0 = -2.0, D = 11.429$$

At $F = 5$ GHz, we can solve the equation for $|\Delta Z|$ and Z_0 .

$$|\Delta Z| = .104, Z_0 = 3.11$$

Given these variables we can now justify the approximations made in the phase detector derivation.

APPROXIMATION 1:

$$\left| \frac{(Z_s - X) \sin \omega t + Z_c \cos \omega t}{1 - X_0 + Z_0} \right| = X$$

where $(1+X)^{-\frac{1}{2}} \approx 1 - \frac{1}{2}X + \frac{3}{8}X^2$ equation (5.14)

Using the above parameters we can solve for $Z_c, (X - Z_s)$.

$$Z_c = 1.41 \cos \phi, (X - Z_s) = 1.41 \sin \phi$$

Therefore, $X = .27$

and

$$\text{exact } (1+x)^{-\frac{1}{2}} = .8873$$

$$\text{approx. } 1 - \frac{1}{2}X + \frac{3}{8}X^2 = .8922$$

This gives an error of 0.5%.

APPROXIMATION 2:

$$\left| \frac{Z_s \sin \omega t + Z_c \cos \omega t}{D - Z_o} \right| = X \ll 1$$

From the previous derivation,

$$Z_c = 1.41 \cos \phi$$

$$Z_s = 1 - 1.41 \sin \phi$$

$$D - Z_o = 3.319$$

$$X = \left| \frac{\sin \omega t - 1.41 \cos(\omega t - \phi)}{3.319} \right| < \left| \frac{2.82}{3.319} \right| = .34$$

This approximation is marginally valid, but the overall effect on the predicted value for Z_o and $|\Delta Z|$ is negligible, because this value is a factor in an exponential term.

APPROXIMATION 3:

$$\frac{1 - e^{-2\alpha_o Z_o}}{1 + e^{-2\alpha_o Z_o}} = 1$$

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Using the above parameter, $\alpha_o = 1.4$, $Z_o = 3.1$
therefore, $e^{2\alpha_o Z_o} = 2.2 \times 10^{-4}$

and
$$\frac{1 - e^{-2\alpha_o Z_o}}{1 + e^{-2\alpha_o Z_o}} = .9996$$

Error = 0.04%

5.4 Optimization of Phase Detector Sensitivity

Having reduced the phase detector's nonlinear equation to the form of equation (5.55), we can now use this equation to calculate the dc voltage deflection for a given phase difference. Preliminary investigations into this phase detector's behaviour and recalling the typical sinusoidal characteristics of multiplier phase detectors, one can assume the dc output voltage to be a sinusoidal function of the phase difference [32].

Differentiating (5.55) with respect to the phase ϕ gives:

$$dZ_o/d\phi = \frac{-\sin(\phi+\theta_o)}{dH(Z_o)/dZ_o} \quad (5.57)$$

where:

$$H(Z_o) = F(Z_o)/K(Z_o) \quad (5.58)$$

If it is assumed that the dc output voltage is sinusoidal with a peak deflection of ΔZ , and with an average value Z_o , then we can write:

$$Z_o = \tilde{Z}_o + \Delta Z \sin(\phi+\theta_1) \quad (5.59)$$

Therefore:

$$|\Delta Z| = |dZ_o/d\phi|_{MAX} = |dH(Z_o)/dZ_o|_{MAX}^{-1} \quad (5.60)$$

The peak-to-peak phase detector variation can be evaluated using equation (5.60). Taking the derivative of $H(Z_o)$ with respect to Z_o provides:

$$|dZ|^{-1} = dH(Z_o)/dZ_o = \frac{K \cdot dF/dZ_o - F \cdot dK/dZ_o}{K^2} \quad (5.61)$$

where:

$$\frac{dF}{dZ_o} = -2(1+\lambda_o D_o)(B_o - K) - \lambda_o (1+Y^2 + C_o'^2)$$

$$+ \frac{1}{2} C_0^2 A_0^2 Y_0^2 I_0 \cdot \left[1 + 2J \left\{ 1 - \frac{(1-B_0)}{(B_0-K)} \right\} - \frac{2\lambda_0}{I_0} (1-B_0)(1+J) \right] \quad (5.62)$$

$$+ \lambda_0 A_0^2 \cdot \left[\frac{2B_0 - K - 1 + J^2 (1-B_0)}{(1+J)^2} \right] - g_L / \tanh \alpha_0 Z_0$$

Since:

$$F(\tilde{Z}_0) = 0,$$

We have:

$$|\Delta Z| = \frac{K}{dF/dZ_0} \quad (5.63)$$

In order to obtain the maximum phase detector sensitivity, $|\Delta Z|$, equation (5.63) can be written directly as a function of bias voltages and FET characteristics. One can observe the influences that the bias voltages have on the phase detector's sensitivity in Figures 5.2 and 5.3. (Using the experimentally measured FET characteristics, $P_{IN} = 0$ dBm.)

Rewriting (5.6)

$X_0 = V_1/\phi_0$, DC voltage on the upper FET's gate

$Y_0 = V_2/\phi_0$, DC voltage on the lower FET's gate

$Z_0 = V_3/\phi_0$, DC voltage at the output terminal

ΔZ is the peak output voltage deflection for the phase varying output.

In the next chapter of the thesis, we will describe the design, development and fabrication of an MMIC phase detector and compare the experimental data with the theoretical predictions. Also in the next chapter we will investigate the performance of a MIC and MMIC frequency halver.

Figure 5.2. Phase Detector Output Voltages for Various Biasing Conditions.

Figure 5.3. Phase Detector Sensitivity to Bias Conditions.

CHAPTER 6

CIRCUIT DESIGN AND LABORATORY MEASUREMENTS

In Chapter 3, we outlined the requirements for a phase locked oscillator. It was mentioned that, of all the possible PLO components, the phase detector and frequency divider are the least understood. Novel MMIC configurations for each circuit were then devised. In Chapters 4 and 5, analyses were performed on the frequency divider and phase detector, respectively. These theoretical derivations revealed the requirements and constraints for frequency division and phase detection.

This chapter outlines the fabrication and experimental measurements of the frequency divider and the phase detector. The technology of MMICs is relatively new, and thus to fully understand the functioning of the novel frequency divider, the circuit is fabricated first on hybrid technology. However, due to dimensional restrictions, the novel phase detector can only be fabricated using MMIC technology.

In this chapter, the frequency halver will be examined first. Both the Hybrid circuit and the MMIC will be investigated, and the individual performances revealed. This is then followed by the phase detector study.

In the latter part of this chapter, we will draw conclusions, and discuss how the theoretical analysis compares with the measured performance of the circuits.

6.1 Frequency Halver

Two types of frequency dividers were designed, one using a soft substrate which we call a Hybrid circuit, the other fabricated on a single wafer which we call a Monolithic circuit. Both circuits were designed as parametric frequency halvers which utilize the nonlinearity of GaAs FETs to initiate frequency division. The big advantage of using FETs is the possibility of obtaining conversion gain thereby eliminating the need of amplification if further division is required. Also the "semi-unilateral" property of FET's provides excellent isolation between the resonant loop and the output. The following section explains the design strategies and performances of the Hybrid and MMIC frequency halvers.

6.1.1 Circuit Design

Three objectives should be sought in designing a parametric frequency halver. First, the resonant circuit should have a reasonably high quality factor (Q) at half the input frequency. Second, the resonant circuit should be designed for maximum isolation from the output; and third, the resonant circuit should be balanced with respect to the output frequency but unbalanced with respect to the input frequency.

Hybrid Microwave Frequency Halver

The above conditions are met by the frequency halver presented in Fig. 6.1. The FETs are connected in a common source configuration with the gates connected together by the inductors L . These inductors are realized with short lengths of high impedance line, and together with the gate to source capacitance of the FETs, form a series resonant circuit at half the input frequency.

The input signal is applied, in phase, to the gates of the FETs where the nonlinear capacitance of the Schottky barrier diodes, C_g , produces the desired subharmonic. The resonant loop maintains the subharmonic out of phase across the two FETs. This subharmonic is amplified by the device transconductance, g_m , and appears at the output terminals of the two FETs.

Since there is also feedthrough of the input frequency F_{IN} to the output terminals of the FET, a filter and balun combination is used to suppress this unwanted signal. The balun is designed to cancel the in-phase fundamental signals while combining the out-of-phase subharmonic signals. For less than octave operation, the filter provides increased suppression by attenuating F_{IN} while also matching $F_{IN}/2$ to the balun.

Figure 6.1. Frequency Divider Circuit Diagram.

Figure 6.2. Fabricated Frequency Halver.

The mechanism of parametric subharmonic generation is inherently nonlinear. Thus the pumped impedances $Z_{IN}(\omega)$, $Z_{IN}(2\omega)$ are quite different from the unpumped small-signal impedances. Harrison [74] has modified the "pumped" varactor impedance equations of Penfield and Rafuse [75] in order to obtain an approximation to the nonlinear impedances. These equations were used to obtain an approximate value for the input impedance as a function of frequency. The input signal was then matched to these impedances.

It is assumed here, from observations of the FET characteristics, that the output impedances are not significantly altered from their small-signal values, by the amplitude variation of the pumping signal [69]. The small signal output impedances of the FETs were then used for matching to the balun.

In Fig. 6.2, the fabricated frequency halver is displayed. The objective has been to design a frequency halver that would frequency divide a 10 GHz input signal over a 10% bandwidth. The FETs used were NEC710 with a 0.3 μm long, recessed gate.

Monolithic Microwave Frequency Halver

The monolithic frequency halver described here also utilizes the nonlinear gate-to-source capacitance C_g of two common-source FETs to produce subharmonic oscillations. FETs were used in order to take advantage of the gain and isolation between their input and output terminals. Lumped element, rather than distributed element matching minimized the area of gallium arsenide used for the circuit.

The basic circuit diagram can be seen in Fig. 6.3. The series resonator supporting oscillations at $f_0/2$ was realized using the C_g of both FETs and the two spiral inductors L_3 . Oscillations were confined to the loop by the high impedance presented by L_2 and C_1 . These components also acted as a matching circuit at the input frequency. Matching at the output was performed by L_4 and C_2 , with drain bias being applied through L_4 . The isolation provided by the FETs ensured that the output matching circuit did not load the resonant circuit. Capacitors C_3 were used to RF-ground one terminal of L_4 . Gate bias was applied through the resistor and choke combination R_1 and L_1 .

The basic design strategy followed similar lines as the Hybrid frequency divider. The fabricated monolithic frequency divider is shown in Fig. 6.4. Two $1 \times 400 \mu\text{m}$ FETs used in the circuit were fabricated on active layers formed using ion implantation into a $250 \mu\text{m}$ -thick GaAs substrate. The total chip size was approximately $500 \mu\text{m} \times 1500 \mu\text{m}$.

In the next section, the three most relevant measurements for characterizing the performance of the frequency halvers will be introduced.

6.1.2 Frequency Halver Measurements

The characteristic which most readily defines the operation of a microwave frequency halver is the measurement of the turn-on threshold power level versus frequency. This

curve defines the bandwidth where frequency division will occur given a minimum power input level; a possible mismatch at the input will be evident from this measurement.

A second measurement, that of conversion gain of a microwave frequency halver for varying input power levels, is useful as a demonstration of the advantage of using FETs.

The third measurement, of the swept response of the halver using a spectrum analyzer, provides the variation in output power level gain for a fixed input power, but varying frequency.

All of these measurements can be performed using the setup shown in Fig. 6.5

Figure 6.5 Frequency Divider Measurement Apparatus.

The next section compares the measured performance

of the frequency halvers with their theoretical predictions.

6.1.3 Comparison of Theoretical and Experimental Results

Hybrid Frequency Halver

The fabricated circuit successfully demonstrated division around the design frequency together with conversion gain. Figure 6.6 shows the region of frequency division. As mentioned previously, a minimum level of input power P_{IN} is required to initiate division, and this threshold signal level is dependent on the Q of the resonator. For this circuit, the minimum threshold signal input power was -11 dBm, and was centered about 5% higher than the design frequency. As seen in more conventional frequency halvers, the bandwidth of operation increases as the input power increases above this minimum level [58]. Using the theoretical analysis of the frequency halver from equations 4.75 and 4.76 and the equivalent FET's characteristics supplied by the manufacturer and shown in Figure 6.6, the minimum turn-on threshold point is predicted to be -10.6 dBm. The theoretical curve was adjusted in frequency so that a better comparison with the experimental curve can be observed.

Figure 6.7 illustrates the conversion gain of the divider as a function of P_{IN} at 10.5 GHz. A maximum conversion gain of 6 dB was achieved for low input powers. As P_{IN} was increased above 3.0 dBm, the gain gradually rolled off due to the onset of large signal effects.

Good suppression of the fundamental frequency was observed at the output of the divider. The filter and balun combination resulted in F_{IN} being nominally 36 dB below the desired output signal $F_{IN}/2$.

Figure. 6.6. Region of Frequency Division.

Figure 6.7. Frequency Divider's Conversion Gain at 10.5 GHz.

Figure 6.8. Swept Frequency Responses for $P_{TN} = 20.0$ dBm.

An example of the swept frequency response of the halver is shown in Figure 6.8. The spectrum represents the amplitude of $F_{IN}/2$ for an input signal of 2.0 dBm, as the input frequency is swept over a 400 MHz bandwidth.

Monolithic Frequency Halver

The fabricated monolithic halver demonstrated frequency division at 12 GHz and its frequency response characteristics are shown in Figures 6.9 and 6.10. The measured frequency where division occurs is approximately 20% higher than the predicted value. This offset can be attributed to the inaccuracies in the models of the spiral inductors, thin-film capacitors and FETs. Division occurred for input power levels greater than a threshold of 9.8 dBm. The theoretically predicted value is 8.0 dBm. The theoretical equations in chapter 4 show reasonable agreement with the experimental results; the frequency offset has been omitted. Mismatch losses as well as model inaccuracies can contribute to the discrepancy between experiment and theory.

The bandwidth of operation is dependent on the drive level, a bandwidth of 1.2 GHz being possible for an 18 dBm input level. For phase-locked-loop applications, lower power levels such as 14 dBm are sufficient where a bandwidth of typically 650 MHz is quite adequate. A relatively flat output frequency response for a swept input signal can be seen in Fig. 6.10.

The minimum conversion loss at 12 GHz was 9 dB, and occurred for input signals greater than 13 dBm. This conversion loss was attributed to the low Q of the input resonant loop. A better choice of input inductor and FET can improve the conversion loss to a value which is comparable to the hybrid configuration.

Figure 6.9. Threshold Power Required for Division Against Frequency.

Figure 6.10. Halver Output Spectrum for Swept 17 dBm Input Signal.

6.2 Phase Detector

This section describes the development of a simple, monolithic phase detector utilizing two FETs as shown in Fig. 6.11. Each input is presented to the gate of one of the FETs and the phase detector output is the common drain/source terminal.

6.2.1 Circuit Design

The monolithic phase detector described here utilizes the nonlinear gate-to-source capacitance, C_{gs} , of one FET and the nonlinear channel conductance, of the other FET, to produce the desired mixing. FETs have the advantages of gain, as well as isolation between their inputs. Lumped element matching, rather than distributed, minimizes the area of gallium arsenide used for the circuit.

A detailed equivalent circuit diagram can be seen in Figure 6.12. The input to FET1 is matched using a series L_1 -shunt C_1 , with gate bias applied through V_{g1} . Capacitor C_5 on FET1 is required for a dc block allowing biasing of the source. FET2 is matched using a series C_2 -shunt L_2 combination with gate bias V_{g2} through L_2 . Similarly, a capacitor C_4 is used on the drain of FET2 to provide a dc block for bias V_D while grounding the RF signal.

As is evident from Figure 6.12, the connecting terminal between the two FETs will become a dc floating output upon application of bias voltages V_d and V_s . A low-pass filter is required at this point to attenuate all the unwanted harmonics. The combination L_3 , C_6 , L_4 , and C_7 provides this low-pass filtering characteristics.

The input signal to the gate of FET1 will be amplified and appear at its drain. The signal input to the gate of FET2 will mix with the signal from FET1, across its non-linear gate-to-source capacitor. The resulting signal will include the intermodulation products of the two input signals. After low pass filtering, the phase detector's output voltage will appear at the terminal V_{OUT} .

The two $1 \times 400 \mu\text{m}$ FETs used in this circuit were fabricated on active layers formed using ion implantation into a $250 \mu\text{m}$ -thick GaAs substrate. The total chip size is $500 \mu \times 1500 \mu\text{m}$, as shown in Figure 6.13.

The selection of bias voltages V_D and V_S determine the dc reference value at the output of the phase detector. For simplicity of measurement, V_S was grounded.

Figure 6.11. Phase Detector Using FETs.

Figure 6.12. Equivalent Phase Detector Circuit.

Figure 6.13. Fabricated Monolithic Phase Detector.

6.2.2 Phase Detector Measurements

The characteristic which most readily defines a phase detector's performance is the phase difference versus dc voltage plot. Figure 6.14 illustrates the experimental set-up used to measure this characteristic. Here, an extension line phase shifter is used to control the phase difference between the RF and LO inputs, and the digital voltmeter records the corresponding change in phase detector voltage. The bias supply is used to optimize the phase detector output voltage sensitivity for a given phase change.

Figure 6.14. Phase Detector Measurement Apparatus.

6.2.3 Comparison of Theoretical and Experimental Results

Phase detection was measured over an 800 MHz bandwidth centered at 5.0 GHz. The isolation from the RF to LO terminals was found to be greater than 10 dB, while the isolation from the LO to RF terminals exceeded 16 dB. The measured return losses at the LO and RF terminals were better than 8 dB and 4 dB respectively.

The phase detector sensitivity was found to be very dependent on the bias condition and the input power levels. Figure 6.15 shows the variation in output voltage as a function of phase difference. Three traces with various input powers and bias conditions were measured. For an input power of 0 dBm, the maximum phase detector output voltage change was approximately 135 mV peak ($|\Delta Z| = 193$) into an open circuit.

The monolithic phase detector demonstrated good sensitivity to phase variations. However, in order to compare the experimentally measured values of $|\Delta Z|$ against their theoretical predictions, accurate parameters for the FET model are required. These can be determined, to differing accuracies, by using either a low frequency or a high frequency characterization method.

In the low frequency approach, the dc current versus voltage traces of a GaAs FET are measured on a transistor curve tracer. These measured curves are then used as an

optimization goal for circuit simulations. One such simulation, SPICE, provides a time-domain representation of a GaAs FET using parameters from the Curtice model [72]. Using SPICE, the various low frequency FET parameters, including λ , β , α and V_T can be deduced through a comparison of the measured and simulated curve traces.

Recently, it has been demonstrated that the current versus drain voltage curves are very dependent on the operating frequency [76]. The slope of these curves in the saturation region are particularly affected [77]. In simulation, this slope is primarily controlled by the channel modulation parameter (λ).

Measurements have indicated that this slope increases with increasing frequency, and consequently its inverse, R_{DS} decreases [77]. A measurement of R_{DS} at 1 MHz was observed to have dropped by approximately 10 percent from its value at 10 Hz. R_{DS} appears to be relatively constant for frequencies above 1 MHz.

Using the fact that λ is inversely proportional to R_{DS} , λ can be estimated to increase by a factor of approximately 10 as the frequency is increased from 10 Hz to 1 MHz. It is assumed then, for high frequencies, that λ is the primary GaAs FET parameter that alters the simulated curve traces.

The measured phase detector output voltage, V_{OUT} , is shown in Figure 6.15 as a function of port 1 gate bias voltage and port 2 gate bias voltage. Figure 5.3 illustrates the calculated phase detector sensitivity $|\Delta Z|$ as a function of gate bias voltages, X_0 and Y_0 . It is observed that, given appropriate bias conditions, $|\Delta Z|$ reaches a value comparable to the measured results.

In Figure 6.15, the theoretical prediction of the output voltage is observed, for a given phase difference at the input. The theoretical curves have been normalized to provide a more direct comparison of the phase detector's sensitivity. The predicted average output voltage is shown in Figure 6.15. Good agreement is observed at $P_{IN} = 0$ dBm, $V_1 = 1.5V$, $V_2 = -1.5V$, for the phase detector sensitivity, however the average output voltage shows considerable disagreement. The associated error can be predicted from observing Figure 5.3, as the FETs are biased closer to pinch-off the sensitivity to bias voltage becomes more apparent. The theoretically predicted values are very sensitive to an accurate value for the pinch-off voltage.

Figure 6.15. Measured Phase Detector Characteristics as a Function of Voltage and Power.

6.3 Conclusions

This section summarizes the experimental results for the frequency halvers and phase detector.

In the case of the hybrid frequency halver, the purpose of the measurements was to determine the region of frequency halving as well as to demonstrate subharmonic conversion gain using Field Effect Transistors. The small losses associated with the hybrid frequency halver contributed to the good agreement with the analytically predicted performance of the FET frequency halver.

One can show, by use of a simple calculation incorporating the equivalent FET's characteristics, that the frequency halver turn-on threshold point should be -10.6 dBm. This compares well with a measured value of -11.0 dBm. The agreement is particularly good considering the resonant loop's unmatched conditions at the fundamental and subharmonic frequencies. It can also be observed, by a comparison in Fig. 6.6, that the theoretical and experimental threshold boundary regions follow the same geometric shape. The hybrid frequency halver also demonstrated 6 dB subharmonic conversion gain, as was shown in Fig. 6.7.

The purpose of these laboratory measurements on the monolithic frequency halver was to determine its region of frequency halving. Because of the low Q of the subharmonic resonant loop the measured turn-on threshold point was +9.8 dBm. This is slightly higher than the predicted value of +8.0 dBm. The measured threshold boundary region was found to have the same general shape as that theoretically derived; any deviation being attributed to very large signal effects making the equation's assumptions invalid.

The predicted output power curve, Figure 4.6, shows a near step-function turn-on for $v < 1$, which gradually diminishes for larger v . This behaviour was also observed in the hybrid frequency halver (Fig. 6.8), however the input matching circuitry tended to mask this out.

For the phase detector, the principal purpose of the laboratory measurements was to demonstrate the phase detecting capability of the circuit. As predicted from the theoretical investigation, the sensitivity factor was found to be very dependent on the bias conditions as well as the power of the inputs. For both theoretical and experimental cases, increasing the input power to the phase detector resulted in an increase in its sensitivity factor. It was also observed that as the gate voltages approached their optimally predicted values, the sensitivity factor increased rapidly.

In summary, the frequency divider theoretical derivation provides insight into the operation of the parametric FET frequency halver and the analysis can be used to select the optimum FET as well as its biasing conditions. Also, the phase detector behaviour has been theoretically investigated in detail, with this analysis providing insight into the phase detector's operation.

CHAPTER 7

ACHIEVEMENT AND RECOMMENDATIONS FOR FURTHER RESEARCH

7.1 Achievement

The purpose of this thesis has been the investigation of key monolithic components of a phase locked loop. Following a preliminary investigation, it was determined that the monolithic components which were least understood and which required the most development are the frequency divider and the phase detector.

To verify the concept of FET frequency division, an initial experimental investigation of a hybrid form of the halver was undertaken. Furthermore, a mathematical derivation was developed. The principal characteristic behaviour of the divider (based on the FET's equivalent parameters) was observed, both experimentally and theoretically, in the relationship between the turn-on threshold with the sub-harmonic frequency.

Having laid the foundations for the FET frequency divider, a monolithic version was designed, fabricated, and tested.

Due to the necessity of close proximities, the novel phase detector could not be initially investigated in a hybrid form. Consequently, a mathematical derivation of the characteristics of this novel phase detector served as the initial design tool. Again, having laid the foundations for

this phase detector a monolithic version was designed, fabricated, and tested.

In summary, the design and implementation of both the frequency halver and the phase detector yielded to conceptual simplicity, with good agreement between measurement and expectation.

7.2 Recommendations for Further Research

The following could be considered for further research:

1. The development of a monolithic microwave frequency halver with reduced losses. This could be achieved by using monolithic amplifiers at the input and output of the frequency divider.
2. The integration of all the phase locked loop components into a system on gallium arsenide.
3. An investigation into producing high quality factor passive components on a monolithic wafer. Potentially, the introduction of a high dielectric constant material onto the wafer could greatly reduce the losses.
4. The development of a hybrid GaAs-Silicon wafer for the integration of silicon integrated circuit technology with the RF GaAs circuitry.
5. A graphical representation for the region of validity of the assumptions.

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