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The Reduction of Contact Resistance in AlGaN/GaN Heterostructure Field Effect Transistors

by

Rony Amaya, B. Eng.

A thesis

submitted to the

Faculty of Graduate Studies and Research

in partial fulfilment of the requirements

for the degree of

Master of Engineering

in

Electrical Engineering

Ottawa-Carleton Institute for Electrical Engineering

Department of Electronics

Faculty of Engineering

Carleton University

December 2001

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“The Reduction of Contact Resistance in AlGa_N/Ga_N Heterostructure Field Effect Transistors”

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ABSTRACT

In the growing market for the Internet, it is becoming more important to design high performance transistors to implement optical drivers for systems such as OC-768. The AlGaIn/GaN Heterostructure Field-Effect Transistor (HFET) promises to deliver the bandwidth, high voltage and power requirements, provided more reliable, reproducible methods are found for the fabrication of this epitaxially grown device. One major problem affecting the performance of AlGaIn/GaN HFETs is their high contact resistance values.

This thesis proposes two methods to optimize the performance of AlGaIn/GaN Heterostructure Field-Effect Transistors by reducing their contact resistance. Both methods rely on the formation of a matrix of 100 nm-scale pinholes in the resist mask using e-beam direct write lithography. In the first method, silicon ions are implanted through the mask to contact the conducting layer in the HFET. In the second method, sputter etching is used to remove AlGaIn in the pinhole matrix, allowing metal to come in direct contact with the conducting layer. Results for both experiments are presented here. Si implanted samples produced the lowest values of contact resistance measured for both experiments, as low as $R_c = (0.34 \pm 12\%) \Omega \text{ mm}$.

ACKNOWLEDGEMENTS

I would like to express my most sincere gratitude to my thesis supervisors, Prof. Garry Tarr and Prof. Calvin Plett, for their continuous support, guidance and involvement during this thesis work. Dr. Tarr, the support and expertise you provided me in the device fabrication area was invaluable, your optimism helped me through the times where nothing seemed to work.

To the supporting staff in the fabrication facilities at Carleton University, Carol Adams and Lyal Bernt, your help in fabricating these devices was much appreciated, thank you for making sure all the equipment was up and running and more important thank you for your friendship.

At NRC, I would like to thank Jim Webb and Jennifer Bardwell, for providing the material necessary to carry out this experiment. Also at Nortel Networks, thanks to Tom MacElwee, for supporting this project, both from the research point of view as well as financially, most of all, thank you for your patience, in waiting for the outcome of this project.

Financial Support was provided by Carleton University through a Research Assistantship, by The Government of Ontario and Conexant Systems in the form of a Ontario Graduate Scholarship in Science and Technology and by Nortel Networks in the form of a Research Grant.

Thanks to my parents Everildo and Rosa for being the light that has guided me through obscure times. This degree is the product of your investment in me. To my brothers for putting up with me all these years.

Finally I would like to thank my wife Dawn, for your understanding and patience of the sacrifice of being a graduate student, but most of all, for being there for me.

Table Of Contents

Chapter 1.0 - Introduction.....	1
1.1 Modern Optical Systems.....	1
1.2 Semiconductors for Electro-Optical Modulator Drivers.....	2
1.3 Ohmic Contacts to AlGaIn/GaN HFETs.....	3
1.4 Thesis Contributions	3
1.5 Thesis Organization	4
Chapter 2.0 - HFET Background.....	6
2.1 HFET History.....	6
2.2 AlGaIn/GaN Based HFET.....	7
2.3 Heterostructure Quality.....	9
2.4 Substrate Selection.....	10
2.5 Aluminum Mole Fraction	11
2.6 Piezoelectric Effects and Formation of the 2DEG Layer	13
2.7 HFET Operation.....	14
2.7.1 Charge Control in the HFET	14
2.7.2 Mobility.....	14
2.7.3 Carrier Velocity	15
2.8 Effect of series resistance in HFET performance	16
2.8.1 DC Analysis.....	16
2.8.2 AC Analysis.....	19
2.9 Some Recent Work in AlGaIn/GaN HFET Performance.....	20
Chapter 3.0 - Contact Resistance Background	23
3.1 Schottky vs. Ohmic Contacts.....	23
3.2 Practical AlGaIn/GaN Ohmic Contacts	25
3.3 Transmission Line Model (TLM)	26
3.4 The c-TLM Method [Reeves79].....	28
3.5 Effect of Metal Resistance	32
3.6 Some Recent Results on AlGaIn/GaN HFET Contact Resistance.....	35
Chapter 4.0 - Device Fabrication	38
4.1 Introduction.....	38
4.1.1 Pinhole Formation	38
4.1.2 Sputter Etch Pinhole Experiment	39
4.1.3 Silicon Implant Experiment in AlGaIn	40
4.2 Fabrication Techniques	42
4.2.1 E-Beam Lithography	43
4.2.2 Level to Level Alignment.....	44
4.2.3 Metal Deposition	46
4.2.4 Metal Lift-Off.....	47
4.2.5 AlGaIn Sputter Etching.....	49
4.3 Fabrication Process	50
4.3.1 Sample Preparation and Alignment Structure Formation.....	50
4.3.2 Pinhole Formation	51
4.3.3 Source/Drain Metallization	53
4.3.4 Gate Formation.....	54

Chapter 5.0 -Electrical Test Results	57
5.1 c-TLM Results	57
5.1.1 Effect of Metal Resistance Measurements	59
5.1.2 Si pinhole Implanted Experiment.....	60
5.1.3 Sputtered Pinhole Experiment.....	64
5.2 DC Circular HFET Results Using RF Nitro Ltd. Material	67
5.2.1 Schottky Gate Characteristics.....	67
5.2.2 Drain Characteristics	68
5.3 DC Circular HFET Results Using NRC Material.....	70
5.3.1 Schottky Gate Results.....	70
5.3.2 Drain Characteristics Using NRC Material.....	71
5.4 Summary of Results	72
Chapter 6.0 -Conclusions and Recommendations	73
Chapter 7.0 - List Of References	76
8.0 Appendices.....	82
8.1 Appendix A: Fabrication Run Sheet.....	82
8.1.1 Sample Cleaning.....	82
8.1.2 Level Zero Metal Deposition.....	82
8.1.3 Fine Alignment Marks.....	83
8.1.4 Pinhole Layer.....	83
8.1.5 Source/Drain Ohmic Deposition	84
8.1.6 Gate Formation.....	85
8.2 Appendix B: Writing Conditions using JEOL 840 SEM.....	86

List Of Figures

Fig. 1.	Terrabit Optical Fiber System.....	1
Fig. 2.	Schematic Cross-section of a Conventional AlGaIn/GaN-based HFET.	8
Fig. 3.	Band Diagram for an AlGaIn/GaN Heterostructure.....	9
Fig. 4.	Energy Gaps and Lattice Constants for a) GaAs materials b) Wide band gap materials[Size90].....	10
Fig. 5.	AlGaIn Band Gap Energy as a Function of the Al mole Fraction	12
Fig. 6.	Modulation Doped AlGaIn/GaN HEMT Structure and Polarization fields. ...	13
Fig. 7.	Effect of Contact Resistance on The Overall Series Resistance of FET...16	
Fig. 8.	Schematic of HFET Showing Extrinsic Resistances R_D and R_S	17
Fig. 9.	Effect of the Source/Drain Parasitic Resistances on The Normalized I_d , g_m and g_{ds}	18
Fig. 10.	HEMT AC Equivalent Circuit Including Parasitic Resistances	19
Fig. 11.	Dependence of f_t on the Source/Drain Parasitic Resistances.....	20
Fig. 12.	Electron Transport Mechanisms for a) Schottky and b) Ohmic Contacts	23
Fig. 13.	I-V Characteristic Curves for a) Schottky and b) Ohmic Contacts [Liu99] .	24
Fig. 14.	Typical Metal Ohmic Structure for an AlGaIn/GaN HFET	25
Fig. 15.	TLM Model for Contact Resistance	26
Fig. 16.	Plot of the Total Resistance as a Function of Length (l).....	27
Fig. 17.	Circular Contact Pattern for Circular TLM Contact.	28
Fig. 18.	Cross-section of Circular Transmission Line Contact Pattern.....	29
Fig. 19.	Distributed Model for Circular TLM Contact	29
Fig. 20.	Plot of Total Resistance at the Contact vs. Normalized Contact Radius ...	32
Fig. 21.	Probe Placement of $V_{measure}$ at an Angle θ from I_{source}	33
Fig. 22.	Dependence of the Measured Error on the Beta Parameter and Measuring Angle.....	34
Fig. 23.	Illustrating E-beam Scanning of NPGS System	38
Fig. 24.	SEM Picture of Pinholes into Resist Layer. Dimension Bar is 1 μm	39
Fig. 25.	Metal Contacting 2 DEG Through Pinhole after Sputter Etch	40
Fig. 26.	Comparison of Mass and Atomic Number for GaAs and GaN	41
Fig. 27.	Level to Level Alignment Windows Using the NPGS System.....	45
Fig. 28.	Double Stack Metal Liftoff process for deep submicron devices	48
Fig. 29.	Overheated AlGaIn Sample After Sputter Etching	50
Fig. 30.	RF Nitro Undoped AlGaIn/GaN HEMT Structure [RFNitro]	51
Fig. 31.	Layout of a c-TLM Structure Showing Pinhole Layer Near Source/Drain periphery.	52
Fig. 32.	c-TLM Metal Layer Layout.....	53

Fig. 33.	Gate length vs. E-beam Dose to Determine Minimum Achievable Geometries	54
Fig. 34.	Layout of Circular HFET Showing Gate Lines	55
Fig. 35.	Final Layout Used in this Experiment	56
Fig. 36.	V-I Characteristic Curves for Si implanted c-TLM Structures Annealed at 700 °C for Different Gap Separations (d).	58
Fig. 37.	Dependence of the Beta Parameter on the Measured Voltage Ratio for Probes Placed at 90° and 180° at Different Anneal Temperatures.....	59
Fig. 38.	Silicon Implanted Sample Annealed at 700 °C in N ₂ for 30 seconds.....	60
Fig. 39.	R _C vs. Anneal Temperature for Si implanted Sample	62
Fig. 40.	Sheet Resistance as a Function of RTA Temperature for Si Implant Experiment.....	62
Fig. 41.	Detailed Plot of Contact Resistance vs. Anneal Temperature for Si Implanted Sample... ..	63
Fig. 42.	Total Resistance vs. Normalized Length for a Sputtered Sample Annealed at 800 °C.	64
Fig. 43.	Contact Resistance vs. Annealing Temperature for Sputtered Pinhole Sample.....	65
Fig. 44.	Sheet Resistance vs. Annealing Temperature for Sputtered Pinhole Sample	65
Fig. 45.	Sputtered Etch Pinhole Experiment using NRC Material.....	66
Fig. 46.	Gate Current vs. Gate Voltage for DC Circular HFET	67
Fig. 47.	Drain Characteristics for HFET for V _g = 0V, -1V, -2V, -3V, -4V (The Characteristics Overlap).....	68
Fig. 48.	Schottky Characteristics for DC Circular HFET After Post Gate Metallization Anneal.....	69
Fig. 49.	Schottky Results for Circular HFET Fabricate on NRC Material	70
Fig. 50.	Drain Characteristics for HFET Fabricated on NRC Material	71

List of Abbreviations

2DEG	Two dimensional Electron Gas Layer
β	Metal Resistance Correction Parameter
AlGaN	Aluminum Gallium Nitride
CAD	Computer Aided Design
CIF	Caltech Intermediate Format
C _{gs}	Gate to Source Capacitance
C _{gd}	Gate to Drain Capacitance
C _{ds}	Drain to Source Capacitance
DEMUX	Demultiplexer
eV	Electron Volts
f_t	Transit frequency
$f_{\max}$	Maximum frequency for stability
GaN	Gallium Nitride
g_m	Transconductance
g_d	Output conductance
HEMT	High Electrom Mobility Transistor
HFET	Heterostructure Field Effect Transistor
LSS	Linhard, Scharff and Schiott theory to estimate implantation profile
L_T	Transfer Length
MODFET	Modulation Doped Field Effect Transistor

MOVBE	Molecular-Organic Vapor Beam Expitaxy
MOVCD	Molecular-Organic Vapor Chemical Deposition
MUX	Multiplexer
NPGS	Nanometer Pattern Generation System
OC-768	Optical Communication Standard
PMMA	Poly-Methyl Metal Acrylate E-beam Resist
R_C	Contact Resistance
R_{SH}	Sheet Resistance of Semiconductor
S_n	Nuclear Stopping Energy
SEM	Scanning Electron Microscope
TLM	Transmission Line Method
c-TLM	Circular Transmission Line Method
V_{GS}	Gate to Source voltage
V_{DS}	Drain to Source voltage
Wurtzite	Hexagonal crystal structure

Chapter 1.0 - Introduction

1.1 Modern Optical Systems

The development of the Internet has created a demand for telecommunications systems capable of providing extremely fast data transmission rates in excess of a terrabit per second. Fig. 1 represents a possible system architecture for a Terrabit optical fibre system

Fig. 1. Terrabit Optical Fiber System

Among the current problems requiring innovation for this optical system, are the implementation of lasers, drivers for their electro-optical modulators, ultra fast mux/demux electronics and photonic switches.

Lithium Niobate electro-optical modulators are currently being used in the design of optical systems, and will require amplifier drivers with breakdown voltages of 20 Volts and switching speeds of 40 GHz or more to meet OC-768 standards [OC768].

III-V Nitride electronic devices have emerged as one of the potential technologies that will be able to drive these electro-optic modulators, due to their ability to switch very high voltages at moderately high speed [Trew00].

1.2 Semiconductors for Electro-Optical Modulator Drivers

In order to meet the demands required to drive electro-optic modulators in the terrabit network, the ideal semiconductor will have to meet the following criteria [Trew00]:

- **Large energy gap:** It will provide the ability of the device to support high internal electric fields before breakdown occurs.
- **Low value of dielectric constant:** This is an indication of the capacitive loading of the device and affects the transistor's terminal impedance. Wide bandgap semiconductors have dielectric constants about 20 percent lower than conventional materials, thus allowing a wide bandgap device to be 20 percent larger in area for a given impedance. An increase in area permits larger RF currents and higher RF power to be generated.
- **High thermal conductivity:** Thermal conductance of the material is very important since this parameter indicates the ease with which dissipated power can be extracted from the device. Poor thermal conductivity, results in device operation at an elevated temperature degrading the performance of the device.
- **High critical electric fields for breakdown:** This parameter is an indicator of the strength of the electric fields that can be supported internally to the device before breakdown. This permits large terminal RF voltages to be supported, and thus is necessary for the generation of high RF power.

Of all possible structures, the AlGa_N/Ga_N-based Heterostructure Field Effect Transistor (HFET), has shown the most promise to meet the required characteristics for the ideal semiconductor to drive high voltage electro-optical modulators at high speed [Xu00].

The basic structure of an AlGa_N/Ga_N HFET is shown in Fig. 2 . The electrons are confined to the quantum well formed at the AlGa_N/Ga_N interface, creating a two-dimensional electron gas (2DEG). The device might also be viewed as an example of a High Electron Mobility Transistor (HEMT) or a Modulation Doped Field Effect Transistor (MODFET). Electrons can be supplied to the channel by doping the wide bandgap AlGa_N layer, but often the AlGa_N is left undoped, and the channel forms simply through piezo electric effects in the AlGa_N.

Table 1 , summarizes the properties of GaN compared to Silicon and Gallium Arsenide. Advantages of GaN include wider bandgap and higher breakdown fields among others. These advantages will become important when selecting devices to drive high voltage, high power, high bandwidth electro-optic modulators for OC-768 systems.

Table 1: Material Properties at 300 K (MacElwee99)

Property	Si	GaAs	GaN
Band Gap (eV)	1.12	1.43	3.45
Relative Permittivity	11.9	13.1	9
Breakdown Field (V/cm)	3×10^5	4×10^5	5×10^6
Electron Mobility (cm^2/Vs)	1350	8500	>1000
Maximum Velocity (cm/s)	1×10^7	1×10^7	3×10^7
Thermal Conductivity (W/cm-K)	1.5	0.5	1.3
Bulk Resistivity ($\Omega \text{ cm}$)	3×10^3	1×10^7	$> 1 \times 10^6$

1.3 Ohmic Contacts to AlGaIn/GaN HFETs

The realization of good ohmic contacts has been a major problem in the implementation of AlGaIn/GaN-based HFETs. Forming ohmic contacts to wide bandgap semiconductors invariably poses a technological challenge. The challenge is made even more severe in the AlGaIn/GaN HFET by the need to make a contact to the conducting channel of the HFET (2DEG), through the cap layer of AlGaIn, which is frequently undoped and typically more than 10 nm thick.

1.4 Thesis Contributions

Two techniques to reduce the source/drain contact resistance for AlGaIn/GaN HFETs are investigated here. Both use direct write e-beam lithography to open a matrix of 100 nm scale "pinholes" in a resist mask.

The first technique uses Si implantation to extend a doped/damaged spike from the surface into 2DEG. The second technique uses sputter etching to cut holes through the AlGaIn layer to the 2DEG, and then fill these pinholes with metal. The goal of the second technique is to create a large perimeter over which the 2DEG meets the contact metal. Both techniques are implemented using contact resistance test structures with cylindrical symmetry[Reeves79].

Following conventional practice, both techniques use Ti/Al ohmic metallization. Ti provides good adhesion to most materials and it has been shown that Ti based contact schemes reduce contact resistance by forming a AlTi₂N alloy with AlGaIn, creating an N deficiency in the AlGaIn, leaving the semiconductor heavily n-type doped beneath the AlTi₂N layer[Qiao00].

A series of HFETS intended for DC measurements were also fabricated to explore the ability of Carleton University inhouse fabrication facilities to implement sub-micron devices as well investigate the effect of contact resistance on the behaviour of AlGaIn/GaN HFETS.

1.5 Thesis Organization

A review of previous research on AlGaIn/GaN HFETs and an examination of the effect of contact resistance on the performance of these device will be presented in Chapter 2.

The problems associated with producing a good ohmic contact will be explored in Chapter 3, and methods to experimentally measure the contact resistance will also be described.

Chapter 4 will provide details of the experimental techniques developed to reduce contact resistance. Problems associated with the device fabrication will be described and a detailed experimental procedure provided.

The results of electrical measurements will be presented and analyzed in Chapter 5. The electrical characteristics of devices incorporating the two pinhole structures examined here and of control devices will be compared.

Finally a set of conclusions regarding this experiment will be given in Chapter 6, and recommendations for improvement and future work to be done in this topic will be presented.

Chapter 2.0 - HFET Background

The Field Effect Transistor (FET) has been the fundamental building block of the microwave industry; discrete devices are used in a number of low noise and power applications. However, dramatic progress has been made in recent years in the development of the Heterostructure Field Effect Transistor (HFET), and this transistor is replacing the FET in many applications, particularly where high power and low noise are the driving requirements [Smith89].

The HFET structure consists of epitaxially grown layers of compound semiconductors which have different bandgap energy, so the interface between them constitutes a heterojunction. Only the wider bandgap material is N-type doped to separate electrons from their donor ions, thus reducing impurity scattering and increasing electron mobility.

A number of names have been used to describe HFETs. All of them focus on a particular physical aspect of the device. The name HEMT (High Electron Mobility Transistor) emphasizes the improved electron mobility obtained, while the name Modulation-Doped Field-Effect Transistor (MODFET) focuses on the separation of dopant ions from the channel. Because modulation doping is sometimes referred to as selective doping, the term Selectively-Doped Heterostructure Transistor (SDHT) is also used. Finally, the name Two-Dimensional Gas Field-Effect Transistor (TEGFET) has been used to emphasize the reduced dimensionality of the electron momentum in the channel [Liu99].

2.1 HFET History

The concept of modulation doping was first proposed in 1969 by workers at IBM, but it was not until 1978 that it was demonstrated experimentally at Bell Laboratories. The first HEMT based on the AlGaAs/GaAs heterostructure was reported in 1981 at Bell Labs, and was intended for high speed digital applications. By 1983, the HEMT provided superior performance to conventional FETs, and the first commercial HEMT was reported in 1985

by Gould's Microwave Products Division [Smith89]. Since then, HEMTs have demonstrated very high f_t and f_{max} . Currently there are three well developed types of HEMTs:

- The conventional HEMT, based on an AlGaAs/GaAs heterojunction
- The pseudomorphic HEMT, based on the InGaAs/AlGaAs heterojunction
- InP based HEMT with an InAlAs/InGaAs heterojunction

2.2 AlGaN/GaN Based HFET

AlGaN/GaN devices are currently under investigation for high power and high voltage applications. A typical HFET structure is shown in Fig. 2 . These artificial crystalline structures are typically grown by molecular beam epitaxy (MBE) or molecular vapour chemical deposition (MOVCD), and consist of one or more pairs of alternating layers of aluminum gallium nitride (AlGaN) and gallium nitride (GaN), in which only the wide bandgap AlGaN is normally doped. The main objective is to create an excess population of free electrons in the AlGaN, which then diffuse across the heterojunction into the GaN. As a result, it is possible to create a high concentration of free electrons at the AlGaN/GaN interface, which are not located near dopant ions, and so are not subject to scattering by ionized impurities.

Hall measurements at 300 K of this structure, indicated a maximum two-dimensional electron gas (2DEG) density of $1.2 \times 10^{13} \text{ cm}^{-2}$ with a corresponding mobility of $1060 \text{ cm}^2/\text{Vs}$. Due to the strain of the AlGaN layers, the HEMT structure shows a considerable piezoelectric and spontaneous electric polarization increasing the 2DEG density of the AlGaN/GaN interface.

Fig. 2. Schematic Cross-section of a Conventional AlGaIn/GaN-based HFET.

At this point it is useful to review the basic physics of semiconductor heterojunctions. In conventional semiconductor devices, only one type of semiconductor is used throughout, and rectification of current flow is achieved by creating a pn junction within the structure. This type of structure is termed a homojunction. If two or more semiconductors of different bandgap are brought together a heterojunction results.

To form a heterojunction with useful electronic properties, the two materials must either have the same atomic spacing or be able to deform to adopt a common spacing. The latter possibility is known as lattice mismatch epitaxy or strained-layer epitaxy, and is said to give a pseudomorphic structure. Fig. 3 shows a representative band diagram for the AlGaIn/GaN heterostructure

Fig. 3. Band Diagram for an AlGaN/GaN Heterostructure

From Fig. 3 charge neutrality requires:

$$q \cdot n_s = Q_s + Q_{doping} - Q_{pol1} + Q_{pol1} - Q_{pol2} + Q_{pol2} \quad (1)$$

where $q \cdot n_s$ is the two dimensional electron gas (2DEG) charge density, Q_s is the surface charge, and Q_{doping} is the ionized impurity charge in the AlGaN barrier layer. Q_{pol1} and Q_{pol2} are the polarization charges of the AlGaN and GaN respectively. Fig. 3 also shows the conduction and valence edge discontinuities at the AlGaN/GaN interface.

2.3 Heterostructure Quality

In order to create a high quality heterostructure, the two components should have the same lattice constant or close to it (see Fig. 4). Growing layers that are lattice mismatched on top of each other, will usually lead to the formation of misfit dislocations at the heterointerface between the two materials, making it more difficult to implement good quality heterostructures. This undesired effect will minimize the carrier transport through such regions, leading to poor device characteristics [Liu99]. By adjusting the thickness of the

epitaxially grown layer to be less than the “critical thickness” (a figure of merit which describes the maximum thickness of material which can adopt the lattice constant of the substrate through strain rather than from the introduction of dislocations), one can reduce the misfit dislocations to close to zero [Kim96].

Fig. 4. Energy Gaps and Lattice Constants for a) GaAs materials b) Wide band gap materials[Sze90]

For GaN layers grown on sapphire, the critical thickness is approximately 3 nm. Fig. 4 shows the bandgap properties of GaAs materials and wide bandgap materials. Sapphire is out of the scale of Fig. 4 b, having a lattice constant of $4.74 \text{ \AA}$ and a bandgap energy level of 9.1 eV.

2.4 Substrate Selection

One of the major difficulties that GaN research has encountered, is the lack of suitable substrate material that is lattice matched and thermally compatible with GaN. Currently

many AlGa_N/Ga_N-based HEMTs are fabricated on sapphire substrates, despite its poor structural match with Ga_N and low thermal conductivity. This preference towards sapphire can be attributed to its wide availability, hexagonal symmetry, and its ease of handling and pre-growth cleaning. Sapphire is also stable at high temperatures. Due to the thermal and lattice mismatches between sapphire and Ga_N(13%), it is necessary to grow a thick Ga_N epilayer to obtain good quality material [Sze90].

Recently, the use of SiC substrates has been contemplated, yielding devices with better performance, due to a better lattice match between SiC and Ga_N (3%), and also the fact that SiC has a thermal conductivity of 4.0 W/°Kcm at 300 °K which is approximately 10 times higher than sapphire [Trew00]. However the current commercial cost for SiC is about five times larger than for sapphire.

2.5 Aluminum Mole Fraction

When referring to an AlGa_N heterostructure, we represent the AlGa_N composition in the following form: Al_xGa_{1-x}N, where the x correspond to the aluminum mole fraction. The HFET's behaviour depends on this aluminum mole fraction, since it affects the band discontinuities between the AlGa_N and Ga_N (see Fig. 3).

The ratios of the band edge discontinuities (ΔE_c and ΔE_v) to the total energy bandgap difference (ΔE_g) are among the most important parameters in determining the electrical properties of a heterojunction. Shan [Shan99], reported a study where the bandgap of the Al_xGa_{1-x}N was approximated as

$$E(x) = 3.43 + 1.44x + 1.33x^2 \text{ eV} \quad (2)$$

A plot of the Al mole fraction vs. band gap energy was also presented and is reproduced in Fig. 5

Fig. 5. AlGaIn Band Gap Energy as a Function of the Al mole Fraction

By increasing the aluminum mole fraction we increase the conduction band-edge-discontinuity between the AlGaIn and GaN. The significance of the conduction-band-edge discontinuity is that this parameter determines the extent of confinement of charge in the potential well at the heterointerface. This confinement is directly related to the ability to separate electrons from donor ion scattering centers. In addition, a larger bandgap discontinuity reduces the emission of hot electrons into the donor layer. Therefore parameters such as the saturation velocity and mobility are expected to depend on this Al mole fraction. For practical AlGaIn/GaN devices the Al mole fraction is limited to $x \leq 0.45$, due to trapping effects[Sze90]. Most reported AlGaIn/GaN HFETs have $0.15 \leq x \leq 0.3$.

2.6 Piezoelectric Effects and Formation of the 2DEG Layer

Strain induced piezoelectric polarization is a very important factor in the creation of the two dimensional electron gas (2DEG) at the strained AlGa_N/ relaxed GaN interface. This strain is a result of the lattice mismatch between Al_xGa_{1-x}N and GaN (x is typically between 0.15 and 0.3). To further enhance the sheet carrier concentration at the 2DEG, a Si doped AlGa_N layer may be grown that is typically separated from the channel by an undoped AlGa_N spacer layer. An additional $1 \times 10^{13} \text{ cm}^{-2}$ sheet density of carriers can be obtained by doping the AlGa_N at $0.5 - 5 \times 10^{19} \text{ cm}^{-3}$ with Si. This is about a factor of two increase over an undoped AlGa_N/GaN HEMT structure.

Fig. 6. Modulation Doped AlGa_N/GaN HEMT Structure and Polarization fields.

From Fig. 6, it can also be seen that there are two piezoelectric sources of polarization. The first one, P_{piezo} , corresponds to the previously described lattice mismatch between the AlGa_N and GaN. The second, P_{spont} , is due to the additional polarization which results from the AlGa_N:Si/AlGa_N interface, resulting in an additional contribution of electrons to the channel. The magnitude of this second polarization effect is proportional to the Si concentration in the AlGa_N:Si barrier layer, which causes a contraction in the wurtzite unit cell and becomes a source of strain [Piner00].

2.7 HFET Operation

2.7.1 Charge Control in the HFET

The sheet charge n_s to applied voltage V_g relationship is given by

$$n_s = \frac{\epsilon}{q(d_d + d_i + \Delta d)}(V_g - V_{th}) \quad (3)$$

where d_d is the AlGaIn donor layer thickness and d_i is the AlGaIn spacer-layer thickness (Refer to Fig. 2). The threshold voltage V_{th} is then given by

$$V_{th} = \phi_b - \Delta E_c - \frac{qN_d d_d^2}{2\epsilon} + \Delta E_{FO} \quad (4)$$

Δd and ΔE_{FO} are fitting parameters representing the variation of donor layer thickness and the variation in the zero bias Fermi energy level respectively [Sze90].

2.7.2 Mobility

One of the most important characteristics of HEMTs is the use of modulation doping to enhance mobility. The basis of this method is to have the donor energy levels in the wider-bandgap material lie above the conduction-band edge of the lower-bandgap material. Electrons from the ionized donors in the wide-bandgap semiconductor accumulate in the conduction band states with the larger electron affinity (or smaller gap in this case), because of the requirement that the Fermi level be constant throughout the structure. In other words, there is a separation of the conduction electrons in the AlGaIn from their parent donor ions, and these electrons reside in a narrow region on the GaN side of the AlGaIn/GaN interface. Since the GaN is usually undoped, the electrons in this region move with essentially no scattering by ionized impurities.

The electron mobility can be further increased by inserting an undoped AlGaIn spacer layer between the doped AlGaIn barrier and the undoped GaN where the 2DEG resides

(Refer to Fig. 2). This leads to a reduction in the electron density with a trade-off, where a larger spacer layer results in greater mobility but a lower sheet charge in the channel. The decreased gate to 2DEG spacing results in a higher device transconductance [Liu99].

2.7.3 Carrier Velocity

A figure of merit for HFETs is their effective carrier velocity. This is the average velocity of carriers in the FET structure. Since the field in the channel is not constant, this value is less than the peak velocity. We can express the transit time under the gate is as follows

$$\tau = (2\pi f_t)^{-1} = \frac{C_g}{g_m} = \frac{L_g}{v} \quad (5)$$

where C_g is the gate capacitance, g_m is the intrinsic transconductance, L_g is the gate length and v is the average electron velocity under the gate, and f_t represents the “transition frequency” or frequency for unity current gain. We could also express the transconductance of the HFET as a function of the average carrier velocity as follows

$$g_m = \frac{\epsilon v W}{d_d + \Delta d} \quad (6)$$

where W is the channel width, d_d is the doped AlGa_N barrier layer thickness, ϵ its permittivity, and Δd is the scaling distance for the 2DEG which represents the thickness of the confined region of electrons at the AlGa_N/Ga_N interface [Sze90].

2.8 Effect of series resistance in HFET performance

2.8.1 DC Analysis

The HFETs input series resistance R_S , including the source contact resistance $R_{contact}$ and the intrinsic FET resistance R_{SG} is

$$R_S = R_{contact} + R_{SG} \quad (7)$$

where R_{SG} correspond to the resistance between the source and the gate edge and $R_{contact}$ the associated source/drain ohmic contact parasitic resistance. To show the importance of $R_{contact}$ in the overall value for R_S , consider a FET with 100 μm gate width and intrinsic R_{SG} of 2 Ω , Fig. 7 shows how the value of contact resistance dominates the total series resistance for contact resistances higher than 0.1 Ωmm .

Fig. 7. Effect of Contact Resistance on the overall series Resistance of FET.

Fig. 8 can be used to analyze the effect of series resistance on the transistor's parameters. Gate resistance is not shown in this figure since its main effect is on $f_{\max}$ rather than f_t .

Fig. 8. Schematic of HFET Showing Extrinsic Resistances R_D and R_S

The extrinsic and the intrinsic bias voltages are related by:

$$V'_{GS} = V_{GS} - R_S I_D \quad (8)$$

$$V'_{DS} = V_{DS} - (R_S + R_D) I_D \quad (9)$$

By definition, current is as follows

$$\Delta I_D = \left. \frac{\partial I_D}{\partial V'_{GS}} \right|_{V'_{DS}} \Delta V'_{GS} + \left. \frac{\partial I_D}{\partial V'_{DS}} \right|_{V'_{GS}} \Delta V'_{DS} \quad (10)$$

$$\Delta I_D = g_{mi} \Delta V'_{GS} + g_{di} \Delta V'_{DS} \quad (11)$$

where g_{mi} and g_{di} represent the FET intrinsic transconductance and drain conductance respectively. The effective transconductance is then

$$g_m = \frac{g_{mi}}{1 + g_{mi} R_S + g_{di} (R_S + R_D)} \quad (12)$$

where g_{mi} represents the intrinsic transconductance of the HFET. Similarly

$$g_d = \frac{g_{di}}{1 + g_{mi} R_S + g_{di} (R_S + R_D)} \quad (13)$$

It can be seen from equations (12) and (13) , that the effective extrinsic transconductance and output conductance are reduced by a factor proportional to these parasitic resistances R_S and R_D , see Fig. 9 .

Fig. 9. Effect of the Source/Drain Parasitic Resistances on The Normalized I_d , g_m and g_{ds}

From Fig. 9 , to obtain less than a 10% degradation of these parameters a total R_S of 4Ω or less is required. Also, from Fig. 7 , the corresponding contact resistance values must be lower than $0.1\Omega mm$ to achieve this R_S (which is lower than most R_C values reported in literature) therefore showing the importance in reducing contact resistance in AlGaIn/GaN HFETs.

2.8.2 AC Analysis

Consider the equivalent AC lumped element circuit for an HFET, including the parasitic resistances shown in Fig. 10

Fig. 10. HEMT AC Equivalent Circuit Including Parasitic Resistances

A simple expression for the cutoff frequency represented in Fig. 10 is as follows

$$\frac{1}{2\pi f_t} = \frac{C_g}{g_m} + \frac{C_g}{g_m} (R_S + R_D) g_d + (R_S + R_D) C_{gd} \quad (14)$$

where C_g represents the total gate capacitance. Also, the maximum frequency of oscillation as a function of the source and drain parasitic resistances can be expressed as follows [Liu99]

$$f_{max} = \sqrt{\frac{f_t}{8\pi R_G C_{gd} \left[1 + \left(\frac{2\pi f_t}{C_{gd}} \right) \Psi \right]}} \quad (15)$$

where Ψ is

$$\Psi = (R_D + R_S) \frac{C_g g_d}{g_m^2} + (R_D + R_S) \frac{C_g C_{gd} g_d}{g_m} + \frac{C_g^2 g_d}{g_m^2} \quad (16)$$

The dependency of f_t on the parasitic resistances R_S is very dramatic and can be seen in Fig. 11 .

Fig. 11. Dependence of f_t on the Source/Drain Parasitic Resistances

2.9 Some Recent Work in AlGaIn/GaN HFET Performance

After the first HFET was presented experimentally in 1981, extensive research was done in AlGaAs/GaAs HFETs. The high electron mobility and superior noise performance that these devices provide prompted creation of well developed technologies in AlGaAs/GaAs.

GaN research began as early as 1960, where much effort was expended to characterize GaN, but there were problems in obtaining high quality material. With the technological advances in optical devices, there was a resurgence of interest in GaN in the 1990s, mainly for blue light emitters. By 1991 the advantages of using a AlGaIn/GaN cap layer in HFETs were known, and attributed to the presence of the 2DEG layer at the heterointerface [Strite92].

The first GaN HFETs give mobilities around $600 \text{ cm}^2/\text{Vs}$ [Nakamura91], but mobilities of $1600 \text{ cm}^2/\text{Vs}$ were observed when an AlGaIn cap layer was used, creating an HFET [Khan91]. Since then, AlGaIn/GaN has been subject to special interest as a microwave power technology. The power capabilities of these devices are far superior to any other microwave technology. Due to the relative low speed of these AlGaIn/GaN devices, much of their research is oriented towards increasing figures of merit such as f_t and f_{max} while preserving the interesting high power and current handling capabilities.

L. Eastman and J. Burm[Eastman96] have done research in $0.25 \mu\text{m}$ gate MODFETs in AlGaIn/GaN yielding f_t values of 21.4 GHz and f_{max} of 77.5 GHz . These devices were fabricated on sapphire substrates. In 1997, Eastman [Eastman97a], also reported AlGaIn/GaN based MODFET with gate lengths in the range $0.12\text{-}0.25 \mu\text{m}$ with f_t values of 50 GHz and f_{max} of 100 GHz . The average transit velocity for these devices was $1.25 \times 10^7 \text{ cm/s}$, and breakdown voltages higher than 100 Volts and power level in the order of 10 Watts/mm were observed when SiC substrates were used.

Nguyen [Nguyen97] reported a $\text{Al}_{0.14}\text{Ga}_{0.86}\text{N/GaN}$ MODFET on sapphire substrate with a f_{max} of 80 GHz and a gate-drain breakdown voltage of 100 V .

Khan [Khan96] reported on HFETs on sapphire with an f_{max} of 97.35 GHz . While Atkas[Atkas97] reported $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ HFET's on sapphire with transconductance of 270 mS/mm and 1.1 A/mm of saturated currents with an f_t of 6 GHz and f_{max} of 11 GHz , intended for high power operation.

High Power capabilities have also been studied in these devices and power densities of 1.1 W/mm [Wu96], $1.5\text{-}1.57 \text{ W/mm}$ [Akatas97] and 1.7 W/mm [Wu97] have been reported. Also Mishra[Mishra98] presented an AlGaIn/GaN based HFET with mobilities of over $1200 \text{ cm}^2/(\text{Vs})$ with current densities of over 1 A/mm , breakdown voltages of 280 Volts , f_t of 52 GHz and power densities greater than 3 W/mm at 18 GHz . This latter achievement was made possible through the use of higher Al contents (40%).

R. Li and J. M. Redwing[Redwing99] developed a HFET suitable for high voltage high power operation (over 200 Volts). The device is an $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}/\text{GaN}$ HFET on a SiC semi-insulating substrate with an $0.2\text{ }\mu\text{m}$ gate length. This HFET exhibited an f_t of 27 GHz, f_{max} of 107 GHz, a transconductance achieved was 260 mS/mm and a substrate current density of 1.2 A/mm which is suitable for power applications.

Bolognesi[Bolognesi00] reported AlGaN/GaN based HFETs with peak f_t of 43 GHz and f_{max} of 98 GHz. These devices had $0.2\text{ }\mu\text{m}$ length gates and achieved a maximum current density of 850 mA/mm. These devices were fabricated using wet etching mesa isolation.

As seen in this review, even though large current densities are obtained with AlGaN/GaN-based HFETs suitable for power applications, they still exhibit moderate speed compared with ultrafast bipolar technologies. The best f_t values recorded are around 50 GHz, and f_{max} around 107 GHz.

One of the factors affecting the speed of AlGaN/GaN devices, is the difficulty to create reliable, reproducible low resistance ohmic contacts[Burm97]. This problem is addressed in this thesis.

Chapter 3.0 - Contact Resistance Background

In this chapter we review the fundamental concept of an ohmic contact, some difficulties associated with the implementation of ohmic contacts in AlGaIn/GaN based HEMTs, and methods to measure contact resistance.

3.1 Schottky vs. Ohmic Contacts

Schottky-Mott theory explains the current voltage characteristics of metal-semiconductor contacts in terms of the existence of an energy barrier at the metal-semiconductor interface, as illustrated in Fig. 12 :

Fig. 12. Electron Transport Mechanisms for a) Schottky and b) Ohmic Contacts

The barrier height at zero bias is given by

$$\phi_{bo} = \phi_m - \chi_s \quad (17)$$

where ϕ_{bo} is the contact barrier height at zero applied bias, ϕ_m is the work function of the metal, χ_s is the electron affinity of the semiconductor and is further expressed by

$$\chi_s = \phi_s - (E_c - E_f) \quad (18)$$

where, ϕ_s is the work function of the semiconductor, E_c is the conduction band energy, and E_f is the Fermi energy level.

ϕ_{bo} is the barrier encountered by electrons in the metal attempting to enter the semiconductor, whereas the built in potential, V_{bi} , is the barrier encountered by electrons in the semiconductor attempting to enter the metal, and is given by:

$$V_{bi} = \phi_m - \phi_s = \phi_{bo} - (E_c - E_f) \quad (19)$$

If the semiconductor is lightly doped (Fig. 12 (a)), a rectifying Schottky diode contact forms with current voltage characteristics shown in Fig. 13 (a). If the semiconductor is very heavily doped (Fig. 12 (b)), electrons can tunnel freely through the narrow depletion region and the current voltage characteristic becomes ohmic, as suggested in Fig. 13 (b).

Fig. 13. I-V Characteristic Curves for a) Schottky and b) Ohmic Contacts [Liu99]

For the case in which the current mechanism is dominated primarily by quantum mechanical tunnelling (Fig. 12 (b)), this tunnelling current I_{tn} can be represented by:

$$I_{tn} = I_{tn0} \left(\exp \left(\left\{ \frac{qV_{app}}{E_0} \right\} - 1 \right) \right) \quad (20)$$

where,

I_{tn0} = tunneling saturation current and E_0 = tunnelling constant.

3.2 Practical AlGaN/GaN Ohmic Contacts

In most practical ohmic contacts to III-V material, the metal layers usually contain a suitable dopant species, either donor or acceptor atoms. A heat treatment is used to drive the dopant into the semiconductor to form a n^{++} or p^{++} layer, thus creating the tunnelling metal-semiconductor junction required to obtain ohmic behavior.

Other desirable properties of ohmic contacts include good adhesion to the semiconductor, smooth surface morphology (particularly where near micron device geometry is concerned), ability to bond gold wires to connect the device to external circuitry and, finally, contact reliability. With these in mind, practical ohmic contacts to III-V materials typically consist of a “wetting agent” to promote adhesion, followed by the dopant species and finally a thick layer of Au for bonding purposes. Where diffusion of the top Au poses potential reliability hazards, often a diffusion barrier is inserted between the gold and the dopant layer. The following represents a typical source/drain ohmic contact structure for AlGaN/GaN devices [Shur99]:

Fig. 14. Typical Metal Ohmic Structure for an AlGaN/GaN HFET

Alloyed ohmic contacts are the most typical type of contact for AlGaIn/GaN substrates. Typical metals used to contact AlGaIn/GaN HEMTs are titanium, aluminum and gold as shown in Fig. 14 .

Some concerns exist over this method, regarding the damage that is created to the device during contact annealing [Jang01a]. For this reason, non-alloyed ohmic contacts are gaining interest among researchers.

Non-alloyed ohmic contacts may become essential for high density integration, since they provide a more planar surface [Kuroda87]. The non-alloyed ohmic contact had been pre-scribed from actual use in a MODFET structure because of the high doping concentrations, in the range of 10^{19}cm^{-3} , needed to enable electron tunnelling. The addition of a heavily doped capping contact layer (see Fig. 2), is a possible solution to enable the use of non-alloyed ohmic contacts although pre-treatment of the surface prior to metallization has also been studied to lower the potential barrier [Jang01b]

3.3 Transmission Line Model (TLM)

One of the most widely accepted methods to measure the effective resistance of ohmic contacts is the Transmission Line Method, first proposed by H. Berger at IBM in 1974 [Berger74]. To aid our derivations of the basic equations outlining this method, consider Fig. 15 .

Fig. 15. TLM Model for Contact Resistance

Here L_1 and L_2 are the separation lengths between adjacent contact metal pads, and R_{SH} is the sheet resistance of the shallow doped layer in the semiconductor. The sheet resistance directly underneath the contact may differ from that between the contacts, and is denoted by R_{SK} . R_C represents the contact resistance contribution of the ohmic metal.

From Fig. 16, it can be shown that the total resistance between any two adjacent pads can be represented as:

$$R_T = 2R_C + R_{SH}l \quad (21)$$

where R_C represents the resistance due to the contact and R_{SH} defines the resistance due to the semiconductor material. The total resistance R_T between each two subsequent pads depends on the separation l as shown in Fig. 16 :

Fig. 16. Plot of the Total Resistance as a Function of Length (l)

L_T corresponds to the transfer length, a parameter representing the distance from the edge of the ohmic contact over which there is significant current flow.

For a very thin conducting layer, Berger [Berger74] showed that the contact resistivity ρ_c (also termed the specific contact resistance) is given by

$$\rho_c = R_{SH} \cdot L_T^2 \quad (22)$$

A relationship between L_T and L_X can be found

$$\frac{2R_{SK}L_T}{R_{SH}} = L_X \quad (23)$$

This equation allows the calculation of the transfer length L_T , from measured parameters in the semiconductor.

It can also be seen from Fig. 16, that the y intercept corresponds to twice the contact resistance, which is the quantity of interest for this study. Since our experimental technique used circular structures, more emphasis will be placed to the analysis of the contact and specific resistances for this variation.

3.4 The c-TLM Method [Reeves79]

A variation of the TLM method, known as the c-TLM or circular TLM, uses a central dot contact and two or more concentric ring contacts (Fig.). The theoretical model used to extract the contact resistance for the TLM method has to be modified to account for this circular geometry. A major advantage of this method lies in avoiding the need for mesa etching to define the boundaries of the conducting layer.

Fig. 17. Circular Contact Pattern for Circular TLM Contact.

The resistance between the center of the structure and any of the concentric rings can be determined using the model of Fig. 18

Fig. 18. Cross-section of Circular Transmission Line Contact Pattern

Fig. 19 shows the resistance of the contact using the equivalent transmission line circuit.

Fig. 19. Distributed Model for Circular TLM Contact

The basic transmission line equations are:

$$\frac{dV}{dx} = \frac{i(x) \cdot R_{SK}}{2\pi x}$$

$$\frac{di}{dx} = \frac{V(x) \cdot 2\pi x}{\rho_c} \quad (24)$$

where $i(x)$ and $V(x)$ represent the current flowing beneath the contact at x , and the voltage at x respectively. Eliminating $i(x)$ and substituting into (24), yields the following differential equation for voltage (Refer to Fig. 19)

$$\frac{\partial^2 V}{\partial x^2} + \left(\frac{1}{x}\right) \frac{dV}{dx} - \alpha^2 V = 0 \quad (25)$$

where

$$\alpha^2 = \frac{R_{SK}}{\rho_c} \quad (26)$$

The contact resistance of the inner most dot contact R_{c0} can be represented as follows,

$$R_{c0} = \frac{V(r_0)}{i(r_0)} = \frac{R_{SK}}{2\pi\alpha r_0} = Z_0 E(r_0) \quad (27)$$

where

$$Z_0 = \frac{R_{SK}}{2\pi\alpha r_0} \quad (28)$$

Similarly

$$R_{c1}' = \frac{V(r_1')}{i(r_1')} = \frac{R_{SK}}{2\pi\alpha r_1'} = Z_1' \frac{B(r_1', r_1)}{C(r_1', r_1)} \quad (29)$$

And E, B and C can be expressed as follows:

$$E(r_0) = \frac{I_0(\alpha r_0)}{I_1(\alpha r_0)} \quad (30)$$

$$B(r_1', r_1) = I_1(\alpha r_1) K_0(\alpha r_1') + I_0(\alpha r_1') K_1(\alpha r_1) \quad (31)$$

$$C(r_1', r_1) = I_1(\alpha r_1') K_1(\alpha r_1) - I_1(\alpha r_1) K_1(\alpha r_1') \quad (32)$$

where I and K are modified Bessel functions of the first and second kind respectively.

If we consider R_A and R_B to be the semiconductor resistance between the inner two contacts and the outer two contacts respectively (see Fig. 18), the resistance between the inner two contacts is

$$R_1 = R_A + (R_{c0} + R_{c1}') \quad (33)$$

and between the two outer contacts

$$R_2 = R_B + (R_{c1} + R_{c2}) \quad (34)$$

R_1 can be expressed as:

$$R_1 = \frac{R_{SH}}{2\pi} \left(\log \left(\frac{r_1'}{r_0} \right) + \frac{1}{\alpha} \left(\frac{E(r_0)}{r_0} + \frac{1}{r_1'} \frac{B(r_1', r_1')}{C(r_1', r_1')} \right) \right) \quad (35)$$

An analogous expression holds for R_2 . (35) accounts for the exact contribution of each one of the contacts based on its geometry. However an approximation is sometimes used, where the contribution of R_{c0} and R_{c1} are assumed to be nearly equal for small gap separations between the measured rings (see Fig. 20).

To apply (35), it is useful to plot the total resistance measured between the contacts versus the normalized radius (with respect to the radius r_0 of the inner ring), as shown in Fig. 20 .

To a good approximation the slope of the plot gives the sheet resistance of the region between the contacts, while the y-intercept gives $2R_C$.

Fig. 20. Plot of Total Resistance at the Contact vs. Normalized Contact Radius

From Fig. 20, the contribution of the sheet resistance R_{SH} , from the semiconductor to the overall resistance between two adjacent pads R_T is cancelled, by taking the y intercept of this linear plot. As the separation between two adjacent pads becomes zero, the total resistance R_T becomes equal to $2R_C$, where the factor of two accounts for the contribution of both of the contacts measured.

3.5 Effect of Metal Resistance

Reeves's [Reeves79] analysis assumes that the contact metal itself is a perfect conductor. For the thin metal layer defined by lift-off by ebeam lithography used here, this assumption is questionable. Recently Rechid [Rechid99] revised the work of Reeves to include the effect of metal resistance.

Rechid's results are expressed in the form of a parameter

$$\beta = \frac{R_a + R_b}{\pi^2 R_{tot}} \quad (36)$$

where R_a and R_b correspond to the metal resistances of the first and second contacts respectively, and R_{tot} is the total resistance between two adjacent contacts.

Measuring the voltage of a ring with the voltage probe positioned at different angles relative to the current source as suggested in Fig. 21, allows a correction for the effect of metal sheet resistance in the contact resistance measurement.

Fig. 21. Probe Placement of $V_{measure}$ at an Angle θ from I_{source}

Using the voltages at two angles (say 90 and 180 degrees for simplicity), it can be shown that the ratio of the two measured voltages is:

$$\frac{U_{\phi}(\pi/2)}{U_{\phi}(\pi)} = \frac{\sinh((\beta\pi)/2) + \sinh((\beta 3\pi)/2)}{2\sinh(\beta\pi)} \quad (37)$$

It is useful to define the relative error between the measured and true resistance, R_{tot} :

$$\Delta R_{rel} = \left| \frac{R_{measured} - R_{tot}}{R_{tot}} \right| \quad (38)$$

The term “true” is used to define a perfectly conductive metal. The relationship between ΔR_{rel} , the measuring angle ϕ and β is shown in Fig. 22 .

Fig. 22. Dependence of the Measured Error on the Beta Parameter and Measuring Angle.

This figure suggest that a measurement at an angle $\phi = 72^\circ$ yields the lowest possible error due to the effect of the metal resistance on the overall contact resistance measurement. However if β is small, Fig. 22 also suggest that a measurement with ϕ of 90° yields only about 10% error in the worst case, which is not a bad estimate considering the difficulty associated with accurately controlling the angle ϕ , (Fig. 21). Contact resistance measurements here were made with different values of ϕ to check for the effect of the metal resistance.

3.6 Some Recent Results on AlGaIn/GaN HFET Contact Resistance

Ja-Soon Jang [Jang98] used circular transmission line structures to examine Ni/Pt/Au contacts to pGaIn. The lowest value of specific contact resistance achieved was $2.1 \times 10^{-2} \Omega \text{ cm}^2$.

Burm and Eastman [Eastman96] reported a contact resistance of $0.097 \Omega \text{ mm}$ by using Si implantation on n-GaN wafers. Si implantation was shown to reduce contact resistance.

Y. L. Li and J. W. Graff [Li00] proposed two methods to achieve low-resistance ohmic contact to p-type GaIn using a metal electrode deposited on a highly doped p-type GaIn layer. The best contact resistance result was $0.9 \Omega \text{ mm}$.

J. Brown [Brown98] reported the use of Si implantation to reduce the specific contact resistance of p-GaIn grown on sapphire, yielding ρ_c values as low as $1.4 \times 10^{-5} \Omega \text{ cm}^2$, for a Ti/Al metal scheme, which was annealed at 800°C for 30 seconds in N_2 . Ring shaped contacts were used for these measurements.

R. Li and J. M. Redwing [Redwing99] achieved a contact resistance of $0.15 \Omega \text{ mm}$ for an undoped AlGaIn/GaN channel HFET with a f_{max} of 107 GHz. The ohmic contact was

formed by deposition of a Ti/Al layer approximately 100 nm thick, which was subsequently alloyed at 900 °C, where Ti replaces Al by diffusion.

Chu and Eastman [Eastman97b] reported a study of the contact resistance of AlGaIn/GaN for different metallization schemes. Results are summarized in Table 2 below

TABLE 2. Results for study of R_C vs. annealing temp and time for various metal schemes[Eastman97b]

Ohmic Metal Scheme($\text{\AA}^0$)	Anneal Temp ($^{\circ}\text{C}$)	Anneal Time (sec)	R_C (Ω -mm)
Ti/Al(200/1000)	800	60	0.6
Ti/Al/Ti/Au(200,1000, 450, 550)	800	60	0.6
Pd/Al/Ti/Au(200, 1000,450,550)	800	60	0.25 (Adhesion difficulties)

Ruden [Ruden99] presented a study of the contact resistance of AlGaIn/GaN devices versus annealing time. It was found that the lowest contact resistance achieved was 0.6 Ω mm, using 830 °C as the anneal temperature. Little improvement was observed for annealing time durations larger than 30 seconds in N_2 .

Bolognesi [Bolognesi00] fabricated AlGaIn/GaN devices with contact resistances as low as 0.7 Ω mm using a Ti/Al/Ti/Au metal scheme, with RTA at 850 °C for 30 s on N_2 . Bardwell [Bardwell99] used a Ti/Al metal scheme to achieve specific contact resistances of 1 Ω mm. For this last result, samples were annealed at 850 °C for 30 seconds on N_2 . Both experiments used AlGaIn/GaN samples grown using the same technique used by the National Research Council.

One of the most extensive studies found on contacts to AlGaIn was done by Qiao [Qiao00]. Alarming variation in contact resistance within the same sample was reported. R_C varied from 0.22 Ω mm to 15.25 Ω mm on one sample. This variation in R_C was attributed to differences in Al mole fractions and AlGaIn layer thickness. It was proposed that contact uniformity could be improved by using Si implantation to facilitate carrier tunneling across the contact.

Hilsenbeck [Hilsenbeck99] reported a new type of ohmic contact using a WSiN diffusion barrier on top of the Ti/Al/Ti/Au ohmic contact. The contact resistance achieved was $0.77 \Omega \text{ mm}$ for AlGaIn/GaN based HEMTs grown on sapphire with Al mole fractions of 20% and 25%.

Finally the contacts of the future may be non-annealed and Jeon[Jeon01] reported low resistance Ti/Al non-alloying contacts achieved with N_2 plasma pre-treatment of the AlGaIn/GaN surface. The specific contact resistance achieved was $1.02 \times 10^{-4} \Omega \text{ cm}^2$.

Chapter 4.0 - Device Fabrication

Two novel approaches are examined here to attempt to reduce the source/drain contact resistance of AlGaIn/GaN HFETs. The first technique involves the implantation of silicon (an n-type dopant in GaN) through a matrix of 100 nm-scale pinholes formed in resist. The intent here is to extend a matrix of dopant spikes through the AlGaIn cap layer to contact the 2DEG. The second technique uses sputter etching to remove the AlGaIn in the pin-hole matrix, allowing metal to directly penetrate to the 2DEG. The goal here is to provide direct contact between the metal and the 2DEG over an extended perimeter length.

4.1 Introduction

4.1.1 Pinhole Formation

The Nanometer Pattern Generation System (NPGS) electron beam lithography system used in Carleton's Microelectronic Fabrication Facility writes patterns as a series of discrete pixels. The electron beam scans rapidly between pixels, then is held in position for a time determined by the dose specified for that pixel, as suggested in Fig. 23

Fig. 23. Illustrating E-beam Scanning of NPGS System

The “center to center spacing” is the distance from the center of one pixel to the next. Once the electron beam has completed an entire sweep, it begins a new line. “Line spacing” is the distance between the center of two pixels from adjacent lines. Under normal writing conditions, “center to center spacing” and “line spacing” are made close enough so the action of the beam resembles a paintbrush covering the entire surface of the area in question.

It is possible to place this “center to center” and “line spacing” far enough apart, so that the area written is not exposed uniformly, but rather individual pixels are written. This creates a matrix of discrete pinholes with controlled physical dimensions. Fig. 24 shows an image taken with a JEOL 840 Scanning Electron Microscope of a series of pinholes created on the resist-coated surface of an AlGaIn/GaN sample. It was determined pinholes with diameters in the order of 200 - 300 nm could easily be implemented. Even smaller pinholes are in principle possible with careful adjustment of beam parameters [Nabity].

Fig. 24. SEM Picture of Pinholes into Resist Layer. Dimension Bar is 1 μm

4.1.2 Sputter etch pinhole experiment

Sputter etching techniques were used to contact the 2DEG through the wide bandgap AlGaIn layer. Using the pinhole resist mask, described above, sputter etching was applied to remove approximately 20 nm of AlGaIn material, sufficient to reach the 2DEG layer.

The final structure to be produced by this technique can be seen in Fig. 25 .

Fig. 25. Metal Contacting 2 DEG Through Pinhole after Sputter Etch

4.1.3 Silicon Implant experiment in AlGaN

The purpose of this experiment is to extend dopant spikes through the AlGaN cap layer to contact the 2DEG. Suitable implant energy and dose had to be predetermined to ensure a range of approximately 20 nm, equal to the thickness of the AlGaN cap layer (see Fig. 2). Table 3 shows projected ranges versus implantation energies and doses for GaN material [Burm96]

TABLE 3. Energy and Dose vs. Silicon Implant range in GaN

Energy (keV)	Dose(cm^{-2})	Simulated projection range (nm)
30	1×10^{15}	22.8
20	1×10^{15}	14.3
15	1×10^{15}	12.2
10	1×10^{15}	8.6
5	1×10^{15}	5.0

We could also use the available implantation tables for Si implants in GaAs, but a correction factor needs to be applied to account for the difference in stopping power of GaN and GaAs. LSS theory can be used to make the correction. Si is a very heavy ion, with critical energy levels of 150 keV. For ion energies much less than the critical energy, the dominant stopping mechanism during implantation is nuclear stopping [Ghandhi94]

Fig. 26. Comparison of Mass and Atomic Number for GaAs and GaN

It is possible to represent the nuclear stopping energy for a material as a ratio of the mass and atomic number of the incident and receptive atom,

$$S_n \cong 2.8e^{-15} \left(\frac{Z_1 Z_2}{Z^{\frac{1}{3}}} \right) \left(\frac{M_1}{M_1 + M_2} \right) \quad (39)$$

where

$$Z^{\frac{1}{3}} = \left(Z_1^{\frac{2}{3}} + Z_2^{\frac{2}{3}} \right)^{\frac{1}{2}} \quad (40)$$

Therefore, it is possible to express the ratio of nuclear stopping energies of GaN and GaAs using the values shown in Fig. 26 , to make use of the wide availability of implantation tables for GaAs materials

$$\frac{S_{GaN}}{S_{GaAs}} = \frac{3.5957(0.4076)}{3.9859(0.2855)} = 1.2879 \quad (41)$$

This shows that GaN materials have 1.3 times more stopping power than GaAs materials for Si implants, therefore an implantation energy 1.3 times larger is required to give the same projected range.

It should be noted that temperatures around 1120°C are required to achieve a 10% activation on the implants in GaN, which has melting temperatures much higher than 1700°C [Brown98]. There will be little activation of the implants used here at the anneal temperatures typically used for contact formation (800 - 900°C), and no values were found.

4.2 Fabrication Techniques

This section describes the common methods required to fabricate the required structures for this experiment. Problems associated with each technique are also discussed.

4.2.1 E-Beam Lithography

Electron beam lithography was used to pattern source/drain and gate metallization in this experiment, and to form the pinholes described earlier beneath the source/drain regions. E-beam lithography was carried out using a modified JEOL-840 scanning electron microscope with beam deflection controlled with an IBM PC using Nanometer Pattern Generation Systems (NPGS) software [Nabity]. This system is capable of defining very small features (200 nm pinholes were produced here, and considerably smaller features have been produced by other groups using comparable equipment), but is very slow. For example, writing a single 100 μm by 100 μm contact pad in PMMA required a write time of 5 minutes for a beam current of 200 pA, which translated to a time of 8 hours to pattern the source/drain metallization on four dice. Higher beam currents are not practical in the JEOL-840.

Input files for the NPGS system must be in Design CAD (an early commercial CAD program) format. However, translators are available to convert CIF and GDSII files to Design CAD, allowing layouts to be generated using CAD tools more suitable to microelectronics. Patterns for the present experiment were generated using Cadence, and then translated.

PMMA resist was used for all e-beam lithography here. PMMA is a positive e-beam resist, that can be thinned in chlorobenzene to form a layers of different thickness. The total thickness of PMMA that can be placed on a sample is about 250 nm due to accelerating voltage limitations of the SEM.

Since metal lines are to be patterned using lift-off techniques, PMMA was used for all layers. The higher the dose required to write one pixel, the longer the time it takes to write it. The dose is also dependant on the thickness of the PMMA layer. Since a double layer of PMMA with thickness of approximately 250 nm was used, the doses were around 150 nC/cm² - 300 nC/cm². The selected dose for each layer, was a trade-off between desired accuracy and writing time and can be seen in Appendix B.

Boxes and filled polygons were patterned using area doses in nC/cm^2 where both the line spacing and the center to center spacing is used. However when a line with very narrow width is desired, as is the case for the HFET gate lines, it is more appropriate to use a line dose in nC/cm where only the center to center spacing is used during writing. Typical line doses are in the order of 10 nC/cm to 20 nC/cm for PMMA.

4.2.2 Level to Level Alignment

Alignment or registration of successive mask levels is problematic in e-beam lithography, since the only means of seeing patterns already in place on a sample is to scan it with the electron beam, yet this scanning exposes the photoresist. The NPGS system solves this problem by incorporating a special scanning window in the Design CAD file, as shown in Fig. 27 . The scanning window sweeps the electron beam over a small area containing a special alignment pattern. When the NPGS system is operated in alignment mode, an image of the sample surface within the alignment window is formed from secondary electrons. Pattern recognition software within the system correlates structures visible in the secondary electron image with those present in the Design CAD layer structures (software overlays), and computes appropriate offsets to be applied when writing the next layer. Highly accurate alignment (ideally within 0.2 μm or better) of the gate to the source/drain metal, and of the pinhole matrix to the source/drain metal, is required here. To provide a starting grid for alignment, a "level zero" pattern was defined in a 1 μm thick e-beam evaporated aluminum layer using optical lithography and etching in H_3PO_4 solution. This coarse alignment pattern consisted of a box 1 mm on a side with 10 μm line width (see Fig. 27). Once the coarse alignment pattern had been defined, e-beam lift-off lithography was used with PMMA resist to form a fine alignment pattern of 10 μm by 10 μm boxes of aluminum centered around the area in which each device was to be fabricated. Limita-

tions on the maximum thickness of PMMA which could be exposed in the e-beam system restricted the height of the aluminum in the fine alignment pattern to $0.25\text{ }\mu\text{m}$.

Fig. 27. Level to Level Alignment Windows Using the NPGS System

The sapphire substrates on which AlGaIn/GaN HEMTs were fabricated here are effectively perfect insulators. When insulators are viewed in the SEM there is no mechanism to remove charge dumped on the sample surface by the electron beam. The surface appears to glow in the SEM display, making viewing and alignment almost impossible. Surface charging effects were a major obstacle in SEM lithography carried out here. Two attempts were made to alleviate the charging, but both failed.

A very thin (20 nm) layer of Al was sputter deposited on top of the photoresist, to increase the charge bleeding rate from the surface of the sample. This thin layer of metal did not affect the SEM's ability to expose the photoresist and was removed later during lift-off.

Unfortunately it was determined that the improvement in bleeding the excess charge was negligible compared to the amount of complexity added to the overall fabrication.

The second attempt to avoid charging effects involved reduction of the beam accelerating voltage to 7 keV during alignment. The voltage was set back to 35 keV for pattern writing. The result was a noticeable reduction in the charging effect. However it was found that changing the accelerating voltage altered the electron optics, leading to pattern shifts of up to 15 μm , which are utterly unacceptable when 0.5 μm alignment accuracy is required to align the gate to the source in a HEMT.

In the end, level to level alignment was accomplished by simply acquiring an image of the alignment patterns as quickly as possible before charging effects became a problem.

4.2.3 Metal Deposition

Most metal deposition required in this experiment was carried out using electron beam evaporation in a cryo-pumped Balzers BA510 System. The system was evacuated to a base pressure of 2×10^{-6} Torr or lower before evaporation. To facilitate lift-off, samples were placed a distance of 60 cm from the source, and were not rotated. The deposition rate was controlled using a quartz crystal monitor. Multiple layers (e.g. Ti/Al) were deposited without breaking vacuum.

The platinum layer forming the Schottky diode gate contact was deposited by RF diode sputtering in an MRC model 8620 system. Once again the chamber was evacuated to a pressure of 2×10^{-6} Torr or less prior to deposition. Sputtering was carried out in an argon plasma at 8 mTorr with an RF power of 100 W.

4.2.4 Metal Lift-Off

Source/Drain and gate metallization for the device structures reported here was defined by lift-off using e-beam lithography. The limited penetration depth of the electron beam, even at maximum available accelerating voltage of 35 keV, limits the maximum photoresist thickness which can be used to approximately 250 nm.

To facilitate the lift-off, a bilayer resist stack was used, as illustrated in Fig. 28 . The bottom layer consists of low molecular weight PMMA, and the top layer of high molecular weight PMMA. After exposure and development, more of the bottom layer than of the top layer is removed, giving an overhanging “lip” structure. This lip provides a clean break in the deposited metal layer, allowing removal of excess metal by dissolving the PMMA in acetone. Best results were obtained using overnight soaks in acetone, with a final brief burst of ultrasonic agitation using a Branson D-50. Excessive ultrasonic agitation caused metal delamination.

An oxygen plasma descum step was found essential to obtaining good metal adhesion in the lift-off process. Without the descum step, all the metal would frequently be removed during lift-off. The descum step removes resist residue left after development. Extreme care must be taken in establishing a descum process for e-beam lithography, due to the relatively thin resist layer required. The descum step was carried out in a Technics PE II-A Plasma etcher at a pressure of 0.3 Torr and RF power level of 50 W for 5 seconds. The erosion rate of PMMA under these conditions was found to be 5 nm/second, which will correspond to approximately 25 nm of removed PMMA in this interval.

Fig. 28. Double Stack Metal Liftoff process for deep submicron devices

4.2.5 AlGaN Sputter Etching

AlGaN and GaN can be etched in plasmas containing chlorine [Mynbaeva99]. Since the etch systems available here did not have chlorine-containing source gases, the only technique available for etching AlGaN/GaN was physical sputtering in an argon plasma. Initial experiments on sputter etching pinholes were carried out using the MRC model 8620 sputtering system operated in sputter etch mode. The chuck in this system is cooled with circulating refrigerant held at a temperature near 0°C. Etching was carried out in an atmosphere of 8 mTorr argon with an RF power of 100 W. 148 nm of AlGaN/GaN were removed from a test sample in 20 minutes, giving an etch rate of 7.4 nm/min.

This result indicates that an etch time of 3 min would be required to remove a 20 nm thick AlGaN cap. When a PMMA coated sample was etched for this length of time, it was found to be impossible to remove the resist either in acetone, various organic commercial photoresist strippers, or by prolonged exposure to an oxygen plasma. It appeared that the photoresist had become severely baked and hardened during the etch (Fig. 29). Subsequently sputter etching was carried out in a Plasma Therm SLR-772 ECR plasma etcher. This system uses liquid nitrogen to cool the chuck to cryogenic temperatures. Wafers are clamped to the chuck, and helium gas is passed over the wafer backside to maintain good thermal contact with the chuck. To use the system it was necessary to attach the small AlGaN/GaN samples to 100 mm diameter silicon carrier wafers using a small quantity of HPR504 photoresist as an adhesive. At 8 mTorr argon and 100 W RF power the sputter etch rate in this system was determined to be approximately 10 nm/minute. AlGaN/GaN samples coated with PMMA resist carrying the pinhole pattern were etched with the chuck temperature held at -100°C. To ensure the photoresist did not overheat, etching was carried out in 1 minute bursts with a period of 1 minute for cooling between each burst.

Even with this treatment, a strong smell resembling burnt rubber was noticed when the vacuum system was opened. Since it is unlikely that significant heating of the samples occurred during etching, it seems probable that ion bombardment was chemically modifying and possibly hardening the surface of the PMMA. Fortunately, it proved possible to

remove the PMMA by plasma etching for 30 minutes in the Technics Planar IIA etcher in a 0.5 Torr oxygen ambient with 500 W of RF power.

Fig. 29. Overheated AlGaIn Sample After Sputter Etching

4.3 Fabrication Process

4.3.1 Sample Preparation and Alignment Structure Formation

AlGaIn/GaN samples used in these experiments were obtained from two sources. The first group of samples was provided by J. Webb of Canada's National Research Council. This material was formed on 50 mm diameter sapphire substrates by magnetron sputtered epitaxy (MSE). An AlN nucleation layer and cap layer was grown on top and had an Al composition of 30 percent [Bardwell99]. The layer structure for this devices was shown in Figure 2 on page 8. Processing was carried out on wafer fragments, with sample dimensions typically in the 1 to 2 cm range. The second group of samples was purchased from

RF Nitro Communications Inc. and had an Al composition of 35 percent. The layer structure for these samples is shown in Fig. 30 .

Undoped AlGaIn/GaN HEMT Structure

Fig. 30. RF Nitro Undoped AlGaIn/GaN HEMT Structure [RFNitro]

Incoming samples were cleaned in a 1:1:1 solution of $\text{H}_2\text{SO}_4:\text{H}_3\text{NO}_4:\text{H}_2\text{O}$ at room temperature for 20 minutes. Coarse alignment patterns for SEM lithography were then formed by aluminum evaporation and wet etching, as described above. Once the coarse alignment structures were in place, fine alignment boxes were formed in aluminum by e-beam lift-off lithography as explained previously in Section 4.2.2 .

4.3.2 Pinhole Formation

Samples were next coated with 200 nm of PMMA, and the pinhole pattern was written using the NPGS lithography system with a beam current of 100 pA and dose of 250 nC/ cm^2 . To keep write times to reasonable values, the pinhole matrix was only formed near the periphery of the areas which would eventually be covered with the source and drain

contact metal, as shown in Fig. 31 . The samples were then divided into two groups as discussed earlier, with one group used for sputter etching of pinholes, and the other for silicon implantation through the pinholes.

Fig. 31. Layout of a c-TLM Structure Showing Pinhole Layer Near Source/ Drain periphery

Samples destined for the sputter etching experiment were etched in the Plasma therm ECR system for a total of 3 minutes in 1 minute bursts, as described above. After etching, the PMMA resist was stripped in an oxygen plasma.

Samples for the silicon implant experiment were attached to 100 mm diameter silicon backing wafers using HPR504 photoresist as glue, and shipped for $^{28}\text{Si}^+$ implantation at Core Systems of San Jose, California. The implant dose was 1×10^{15} ions/cm², and the energy 30 keV. It should be noted that the 200 nm photoresist layer provides a screening efficiency over 99.9% at this implant energy. On return from implant, the photoresist was stripped in oxygen plasma.

4.3.3 Source/Drain Metallization

The source/drain metallization consisted of a stack of 30 nm of Ti overlaid with 80 nm of Al. The stack was deposited by e-beam evaporation and patterned using e-beam lift-off lithography as described in Section 4.2 . A series of circular Transmission Line (c-TLM) structures with separations of 2.5 μm , 5 μm , 10 μm , 15 μm , 20 μm and 30 μm was fabricated as discussed in Chapter 3.

The inner ring had a 50 μm radius for all samples. The pattern written is shown in Fig. 32 .This figure also shows the location of the pinhole layer near the source/drain periphery of all c-TLM structures.

Fig. 32. c-TLM Metal Layer Layout

4.3.4 Gate Formation

For samples processed to form complete HFETs, a gate electrode stack consisting of 10 nm of platinum overlaid with 100 nm of gold was deposited. The platinum was deposited by RF sputtering, and the gold by e-beam evaporation. It was necessary to break vacuum between depositions. Since other groups have reported problems with platinum gate adhesion, the sample surface was sputter etched for 20 s at 100 W power prior to platinum deposition to remove contaminants. The gate stack was patterned by e-beam lift-off lithography.

Fig. 33 shows the result of an experiment in which an array of gates was written and metal subsequently lifted-off and measured using e-beam lithography.

Fig. 33. Gate length vs. E-beam Dose to Determine Minimum Achievable Geometries

Since a gate can best be represented as a line with zero width in the NPGS system, line doses were used instead of area doses as previously described. The HFET layout for the gates can be seen in Fig. 34 . For simplicity a circular HFET was fabricated to provide

drain isolation without mesa etching. The radius of the drain is $25\text{ }\mu\text{m}$ and the source-to-gate and drain-to-gate separations were both set at very conservative values of $2.5\text{ }\mu\text{m}$ for these initial experiments. Based on a dose of 12 nC/cm , a gate length of approximately $0.4\text{ }\mu\text{m}$ is expected.

Fig. 34. Layout of Circular HFET Showing Gate Lines

The complete layout showing all test structures and alignment marks used in this experiments is shown in Fig. 35 .

Fig. 35. Final Layout Used in this Experiment

Chapter 5.0 - Electrical Test Results

This chapter presents results of electrical testing on the contact resistance test structures and HFETs, whose fabrication was discussed in Chapter 4.

5.1 c-TLM Results

Current-voltage characteristics for a typical concentric-ring resistance test structure are shown in Fig. 36 . The particular structure whose characteristics are shown was given a silicon implant and subsequent anneal at 700 °C.

Characteristics were recorded using a four-point measurement technique with an HP4155 Semiconductor Parameter Analyzer. Current was provided through one pair of probes, while voltage was measured across a second pair of probes, as shown in Fig. 21 . In this way the resistance of probes and connectors is eliminated from the measurement. The characteristics shown are clearly ohmic.

Fig. 36. V-I Characteristic Curves for Si implanted c-TLM Structures Annealed at 700 °C for Different Gap Separations (d).

5.1.1 Effect of Metal Resistance Measurements

Recall that from (37), one can solve iteratively for the parameter β by measuring the voltage on the outer metal ring at 90° and 180° from the current source. Also, Fig. 22 shows the dependence on the parameter β of the relative error between measurements neglecting metal resistance effect and the actual resistance. Fig. 37 shows the ratio of the voltage measured for a 90° and 180° probe placement after different anneal temperatures for a silicon implanted sample, and the corresponding value of β .

Fig. 37. Dependence of the Beta Parameter on the Measured Voltage Ratio for Probes Placed at 90° and 180° at Different Anneal Temperatures

The highest measured value for β was 0.115, and as seen in Fig. 22 this correspond to relative resistance error of no more than 10 percent when both pairs of probes are located 90° apart. If the probes were placed 180° , a β of 0.115 would have corresponded to a resistance relative error of approximately 32 percent. All data reported below was taken with probes in the 90° position.

5.1.2 Si pinhole implanted experiment

Fig. 38 shows a plot of total resistance versus normalized radius for a sample with silicon pinhole implants annealed at 700°C . Similar plots were constructed for other anneal temperatures.

Fig. 38. Silicon Implanted Sample Annealed at 700°C in N_2 for 30 seconds

The y intercept from Fig. 38 corresponds to $R_{\text{tot}} = 14.0 \, \Omega$. Recall from (33) that this point represents twice the resistance of the contact only, since the contribution due to the sheet resistance of the semiconductor has been eliminated by extrapolating to zero separation between the contacts. We therefore have $R_C' = 7.0 \, \Omega$. Contact resistance is usually expressed as the product of the measured resistance and the contact length, so here we have

$$R_c = R_c' \cdot L_{\text{contact}} = 7.0\Omega \cdot 0.314\text{mm} = 2.2\Omega\text{mm} \quad (42)$$

Four different set of contacts were measured, averaged and shown in Fig. 39 . The best contact resistance measurement for the Si implanted experiment fabricated on NRC material corresponds to $(0.34 \pm 12 \%) \, \Omega \text{ mm}$ at an RTA temperature of $800 \, ^\circ\text{C}$, which compares to a value of $(0.63 \pm 7 \%) \, \Omega \text{ mm}$ for a non-implanted control sample. This value achieved by using Si implantation is considerably lower than the $0.7 \, \Omega \text{ mm}$ achieved by Bolognesi [Bolognesi00] with a double stack layer Ti/Al/Ti/Al and Eastman [Eastman97b] who achieved $0.6 \, \Omega \text{ mm}$ using a Ti/Al layer. Finally the sheet resistance of the 2DEG was monitored as a function of temperature and plotted in Fig. 40 . The relatively large variation in sheet resistance is puzzling, since one would expect R_{SH} to remain relatively constant until anneal temperatures became high enough to change the strain and polarization of the AlGaIn.

Fig. 39. R_C vs. Anneal Temperature for Si implanted Sample

Fig. 40. Sheet Resistance as a Function of RTA Temperature for Si Implant Experiment

Fig. 41. Detailed Plot of Contact Resistance vs. Anneal Temperature for Si Implanted Sample.

A detailed plot of Contact Resistance is also shown in Fig. 41 . Error bars as well as deviations are shown here. It can be seen that the lowest achieved value of Contact Resistance was $(0.34 \pm 0.04) \Omega \text{ mm}$ compared to $(0.63 \pm 0.044) \Omega \text{ mm}$ for a control sample, both annealed at an RTA of 800°C.

5.1.3 Sputtered pinhole experiment

A similar approach was taken to measure the contact resistance of samples produced in the sputtered pinhole experiment. Contact resistance was monitored as a function of the annealing temperature, and both sputtered as well as control samples on each piece were measured, for AlGaIn/GaN material purchased from RF Nitro Inc. [RFNitro_a].

Fig. 42. Total Resistance vs. Normalized Length for a Sputtered Sample Annealed at 800 °C

RF Nitro Inc. material was used initially, due to the lack of samples from NRC, although it is of interest to compare results for both sources of AlGaIn/GaN material. It can be seen from Fig. 42 that the total resistance at 800 °C is much higher than for the Si implant experiment. Following the same analysis as in (42) we extract a contact resistance of 7.48 Ω mm. Normalized contact resistance is shown as a function of annealing temperature in Fig. 43 .

Fig. 43. Contact Resistance vs. Annealing Temperature for Sputtered Pinhole Sample

Fig. 44. Sheet Resistance vs. Annealing Temperature for Sputtered Pinhole Sample

The results obtained from Fig. 43 , show very high values for sheet resistance at low anneal temperatures. This is not in agreement with the results from the NRC material plotted in Fig. 39 , suggesting differences in the properties of NRC and RF Nitro Inc. materials. At anneal temperatures higher than 800 °C, the sheet resistance reduces to about 700 Ω /square. After annealing the sample at 1050°C, no noticeable indication of sheet resistance degradation was seen, but due to equipment limitations of the Heat Pulse 210 RTA, no higher anneal temperatures were possible. The best contact resistance measured for both the sputter etch experiment as well as control samples was approximately $3.5 \pm 10\%$ Ω mm, which is much higher than the results obtained for the silicon implanted sample implemented on NRC material, and much higher than typical results for Ti/Al samples reported in the literature.

In view of the disappointing and puzzling results obtained in the sputtered pinhole experiment using RF Nitro Ltd. material, the experiment was repeated with NRC material. Due to the limited quality of samples provided by NRC, it was necessary to reuse wafer fragments employed earlier in the silicon implant experiment. Sputtered pinhole test structures were formed in regions not already used for the silicon implant experiment. Results are shown in Fig. 45

Fig. 45. Sputtered Etch Pinhole Experiment using NRC Material.

The lowest value of Contact Resistance achieved using NRC samples, was $(0.74 \pm 0.06) \Omega \text{ mm}$ at an RTA of 800°C compared to contact resistances of $(0.96 \pm 0.08) \Omega \text{ mm}$ for control samples and much lower than results obtained using RF Nitro Inc. material.

5.2 DC Circular HFET Results using RF Nitro Ltd. material

A circular HFET with length dimensions shown in Fig. 34 , was also fabricated using the RF Nitro Inc. substrates, as described in Chapter 4. The device had a drain radius r_o of $25 \mu\text{m}$ (see Fig. 34), the source-to-gate spacing L_{SG} and drain-to-gate spacing L_{DG} were both set to $2.5 \mu\text{m}$ and the gate length was $0.5 \mu\text{m}$. Source/Drain contacts were fabricated using a $30 \text{ nm Ti} / 80 \text{ nm Al}$ single stack layer, and annealed at 700°C . No silicon implant or pinhole sputter etching was done on this sample. Device characteristics were measured using the HP4155 Semiconductor Parameter Analyzer.

5.2.1 Schottky Gate Characteristics

First, the current-voltage characteristics of the Schottky junction formed between the gate and the channel were measured. Both the drain and source of the circular HFET were grounded, while the voltage applied to the gate was swept. Results are shown in Fig. 46 .

Fig. 46. Gate Current vs. Gate Voltage for DC Circular HFET

The reverse leakage becomes significant for gate voltages lower than -3 Volts. J. Redwing [Redwing98] found similar leakage currents for $V_{gs} < -4V$ on high performance HFETs formed on substrates with 25 % Al content.

5.2.2 Drain Characteristics

The drain characteristics of the HFET were also recorded and are shown in Fig. 47 . No measurable modulation of I_D in response to changes in V_G was observed.

Fig. 47. Drain Characteristics for HFET for $V_g = 0V, -1V, -2V, -3V, -4V$ (The Characteristics Overlap)

From Fig. 47 , we can see essentially ohmic behaviour in the I_d vs. V_{ds} characteristics. The device fabricated had approximately 0.15 mm of drain periphery. Bolognesi [Bolognesi00] obtained drain currents of 800 mA/mm for $V_g = 0 V$ using the NRC material. Fig. 47 show the RF Nitro Inc. material used for this experiment had drain currents of only 45 mA under similar bias. Fig. 43 showed a contact resistance of 20 Ω mm for control samples on the RF Nitro Ltd. material, this value correspond to a source/drain resistance of approximately 140 Ω . Assuming a transconductance of $g_m = 280$ mS/mm, a

typical number from literature [Bolognesi00] and a source resistance of $140\ \Omega$, by the use of (12), the calculated first order reduction in the effective transconductance is approximately 96%. Although this is a very large reduction, it does not explain the complete lack of modulation presented in Fig. 47.

To attempt to reduce the source/drain contact resistance, the sample was annealed at $850\ ^\circ\text{C}$ for 30 seconds and the DC characteristics remeasured for the HFET. No noticeable improvement in the drain characteristics was observed, and the Schottky gate leakage increased significantly as seen in Fig. 48

Fig. 48. Schottky Characteristics for DC Circular HFET After Post Gate Metallization Anneal.

The Schottky barrier height also appears to have been reduced. The increase of the leakage current in the reverse direction may be related to the decrease of the barrier height [Yu98]. Even though the barrier height is in principle determined by the difference in

electron affinities, modification to the metal-semiconductor interface to heating, after gate metallization, may have induced this lowering of the barrier height.

5.3 DC Circular HFET results using NRC material

Annealed NRC material from the silicon implant experiment was used to fabricate HFETs. Once again, devices were fabricated in regions not exposed to the silicon implant.

5.3.1 Schottky Gate Results

Fig. 49. Schottky Results for Circular HFET Fabricate on NRC Material

Fig. 49 shows the Schottky characteristics for the circular HFET fabricated on NRC material. Compared to Fig. 46, it shows less leakage current and also a lower potential barrier.

5.3.2 Drain Characteristics using NRC material

The drain characteristics obtained when using NRC material were much better than those obtained using RF Nitro Ltd. material. Gate modulation of drain current was observed and can be seen in Fig. 50

Fig. 50. Drain Characteristics for HFET Fabricated on NRC Material

The maximum achievable current density of 0.35 A/mm is still low compared with Bardwell [Bardwell99] maximum of 0.8 A/mm. The peak transconductance was approximately 96 mS/mm, which is about half the value obtained by Bardwell.

5.4 Summary of Results

Results from contact resistance and HFET experiments are summarized in Tables 4 and 5,

Table 4: Contact Resistance Results

Experiment	$R_C(\Omega mm)$	% devi. Control Sample	$R_{sheet}(\Omega/(sq))$	RTA($^{\circ}C$)	Source
Si Implant	0.34 +/-0.04	53	543 +/- 61	800	NRC
Sputtered	3.5 +/- 0.35	17	860 +/- 53	1050	RF Nitro Ltd.
Sputtered	0.74 +/- 0.06	25	670 +/- 84	800	NRC
Bardwell <i>et al</i>	0.9		496	850	NRC

Table 5: HFET Results ($L_G \sim 0.5 \mu m$)

Material Source	$I_{d,max}(A/(mm))$	$g_m(mS/(mm))$	$g_{ds}(mS/mm)$	Comments
RF Nitro Ltd.	N/A	N/A	N/A	no modulation
NRC	0.35	96.46	3.16	low values
Bardwell <i>et al</i>	0.8	200	7.5	similar material

Chapter 6.0 - Conclusions and Recommendations

This thesis began with a demonstration, both through a survey of existing literature and through SPICE simulation, of the importance of reducing source/drain contact resistance to obtain the best possible performance in AlGaIn/GaN HFETs. It was shown that contact resistance values in the range 0.5 - 1 Ω mm, typical of many devices reported recently, significantly degrade the performance of deep submicron devices. Two new contact structures with the potential to lower contact resistance were then introduced and evaluated experimentally.

The first new structure relies on silicon implantation through a matrix of 100 nm scale pinholes formed in resist to extend dopant “spikes” from the AlGaIn surface to the 2DEG gas at the AlGaIn/GaN interface. This structure was formed on AlGaIn/GaN samples grown by reactive MBE provided by NRC. The structure yielded contact resistance values as low as 0.34 Ω mm after rapid thermal annealing at 800 °C. Control samples also showed significant improvement for anneal temperatures higher or equal to 800°C. The best result for control samples was 0.63 Ω mm, recorded after an anneal at 800 °C. Results are summarized in Table 4 and Table 5.

The second new structure contacts the 2DEG by sputter etching through the AlGaIn in the pinhole matrix, and then filling the pinholes with metal. The intent of this structure is provide a large perimeter over which metal directly contacts the 2DEG. Examples of the second structure were fabricated on commercial AlGaIn/GaN samples purchased from RF Nitro Ltd. Contact resistance values obtained in this experiment were far higher than those obtained using NRC material, both for control samples and for those with the pinhole matrix. Contact resistance did drop for anneal temperatures above 800 °C, but remained an order of magnitude higher than for the first structure. The same experiment was later repeated using peripheral regions of NRC material, that had been used in the silicon implant experiment. Contact resistance values as low as (0.74 +/- 0.06) Ω mm were obtained compared to (0.96 +/- 0.08) Ω mm for control devices.

Clearly the RF Nitro material behaves very differently than that obtained from NRC. This difference became particularly apparent when both the contact resistance and sheet resistance of both materials was analyzed as a function of temperature. The samples purchased from RF Nitro did not show any degradation of sheet resistance even at temperatures as high as 1050 °C, which also suggests that higher temperature anneals are possible on this material, if suitable equipment were available.

Enclosed geometry HFETs were fabricated on RF Nitro Ltd. material. These devices exhibited Schottky gate current-voltage characteristics comparable to those reported by other researchers, but absolutely no modulation of drain current in response to gate bias was observed. Although these devices were known to suffer from very high source/drain contact resistances, analysis indicated that measurable transconductance should have been obtained. It is not clear why the devices were not able to function as transistors.

Following the failure to obtain working HFETs on RF Nitro Ltd. material, additional test HFETs were fabricated on NRC material. It was necessary to re-use material originally implanted with silicon. Devices were placed in regions not used in the earlier experiment. Reasonably good HFET performance was obtained, by peak current densities of 0.35 A/mm and transconductance of 96 mS/mm. The transconductance was about half the best value reported for NRC material [Bardwell99]

Finally, the ability to fabricate HFETs with gate lengths as short as 0.2 μm using the facilities at Carleton's Microfabrication Laboratory has been demonstrated. The development of these techniques should make possible the future fabrication of AlGaIn/GaN microwave integrated circuits. The techniques could also be applied to fabricate high performance HFETs in other material systems.

One recommendation for improvement in this experiment would be to increase the periphery that the pinhole implant layer cover in the source/drain regions. Ideally the entire source/drain are could be covered with the pinhole layer at the expense of longer lithography times. Also, as suggested by Qiao [Qiao00], the contact resistance of AlGaIn/GaN based HFETs seems to vary considerable along the same wafer, and it would have been

interesting to study its effect on both NRC and RF Nitro substrates if full wafers would had been available. The use of pinhole source/drain structures in an actual HFET could also have been implemented.

Chapter 7.0 - List Of References

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8.0 Appendices

8.1 Appendix A: Fabrication Run Sheet

8.1.1 Sample Cleaning

- Rinse 10 minutes in a 1:1:1 solution of H_2SO_4 : H_2NO_3 :DI
- Rinse in Acetone for 20 minutes

8.1.2 Level Zero Metal Deposition

- Evaporate 1um of Aluminum on sample using the Balzer Vacuum Evaporator with FDC-8000 Film deposition Controller.
- Spin photoresist adhesion promoter HMDS: 30 sec. at 4000 rpm using a Solitec photoresist spinner.
- Bake 1 min at 105°C
- Spin photoresist HPR504 30 sec. at 4000 rpm
- Bake 1 min at 105°C
- Expose Level Zero Optical Mask for 12 sec. using Karl Suss MA6 Mask Aligner and 330 Watts arc Lamp.
- Develop sample in 50:50 solution of MIF:DI for 1 minute
- Rinse sample for 3 minutes in DI
- Hard Bake sample for 3 minutes at 130°C.
- Apply a Photoresist Descum using Technics Planar Plasma etcher: 1 minute, 0.3 Torr, 100 Watts
- Strip exposed Aluminum using H_3PO_4 , heated at 60°C for approx. 2 minutes and 30 seconds
- Rinse in DI for 15 minutes
- Completely dry sample before going to next step

- Remove left HPR504 using Microstrip 2001 solution, heated to 90°C for 10 minutes
- Rinse in DI for 15 minutes
- Dry in oven at 250°C for 2 hours prior to next lithographic step

8.1.3 Fine Alignment Marks

- Apply PMMA 495K solution: 30 sec. at 4000 rpm
- bake 10 minutes at 180°C.
- Apply PMMA 950K solution: 30 sec. at 4000 rpm
- bake 10 minutes at 180°C.
- Load into JEOL 850 SEM
- Using Nanometer Pattern Generation System (NPGS) controller software/hardware, pattern Fine alignment boxes into sample
- Remove sample from JEOL 840 SEM
- Develop Sample in 1:3 solution of IPA:MIBK for 3 minutes
- Rinse sample for 5 minutes
- Apply a photoresist descum in Technics Planar Plasma Etcher: 5 sec at 0.3 Torr, 50 Watts
- Evaporate 2000 Å of Aluminum using Balzer evaporator
- Soak sample in acetone for at least 2 hours, prior to metal lift-off
- Load sample into Branson D-50 Ultrasonic for 10 - 20 seconds
- Rinse sample in DI for 2 minutes
- Dry in oven at 250°C for 2 hours prior to next lithographic step

8.1.4 Pinhole Layer

- Apply PMMA 495K solution: 30 sec. at 4000 rpm
- bake 10 minutes at 180°C.

- Apply PMMA 950K solution: 30 sec. at 4000 rpm
- bake 10 minutes at 180°C.
- Load into JEOL 850 SEM
- Using Nanometer Pattern Generation System(NPGS) controller software/hardware, pattern Pinhole Layer into sample using Coarse and Fine alignment Marks to guide process
- Remove sample from JEOL 840 SEM
- Develop Sample in 1:3 solution of IPA:MIBK for 3 minutes
- Rinse sample for 5 minutes
- Apply a photoresist descum in Technics PE II-A Planar Plasma Etcher: 5 sec at 0.3 Torr, 50 Watts
- Load into Balzer ECR system with plasma thermal process/sequence controller
- Cool substrate to -100 °C.
- Etch sample for 2 minutes: 100 Watts, 20 sccm Argon, 8 mTorr
- Load sample directly into Technics planar plasma etcher: 20 minutes, 0.5 Torr, 500 Watts
- Rinse sample in acetone for 10 minutes
- Dry in oven at 250°C for 2 hours prior to next lithographic step

8.1.5 Source/Drain Ohmic Deposition

- Apply PMMA 495K solution: 30 sec. at 4000 rpm
- bake 10 minutes at 180°C.
- Apply PMMA 950K solution: 30 sec. at 4000 rpm
- bake 10 minutes at 180°C.
- Load into JEOL 840 SEM

- Using Nanometer Pattern Generation System(NPGS) controller software/hardware, pattern Source/Drain Metal layer into sample using Fine and Coarse Alignment Marks to guide process
- Remove sample from JEOL 840 SEM
- Develop Sample in 1:3 solution of IPA:MIBK for 3 minutes
- Rinse sample for 5 minutes
- Apply a photoresist descum in Technics Planar Plasma Etcher: 5 sec at 0.3 Torr, 50 Watts
- Load sample into Balzer evaporator and deposit 300 Å of Titanium, 800 Å of Aluminum
- Soak sample in acetone for at least 2 hours, prior to metal lift-off
- Load sample into Branson D-50 Ultrasonic for 10 - 20 seconds
- Rinse sample in DI for 2 minutes
- Apply a Rapid Thermal Anneal at 850°C for 30 seconds using N₂
- Dry in oven at 250°C for 2 hours prior to next lithographic step

8.1.6 Gate Formation

- Apply PMMA 495K solution: 30 sec. at 4000 rpm
- bake 10 minutes at 180°C
- Apply PMMA 950K solution: 30 sec. at 4000 rpm
- bake 10 minutes at 180°C
- Load into JEOL 840 SEM
- Using Nanometer Pattern Generation System(NPGS) controller software/hardware, pattern Gate Metal layer into sample using Fine and Coarse Alignment Marks to guide process
- Remove sample from JEOL 840 SEM

- Develop Sample in 1:3 solution of IPA:MIBK for 3 minutes
- Rinse sample for 5 minutes
- Apply a photoresist descum in Technics Planar Plasma Etcher: 5 sec at 0.3 Torr, 50 Watts
- Using MRC Sputtering System, deposit $\sim 100 \text{ \AA}$ of Pt.:1 minute, 100 W, 60 sccm Ar, 8 mTorr
- Load sample into Balzer evaporator and deposit $300 \text{ \AA}$ of Platinum, $1000 \text{ \AA}$ of Gold
- Soak sample in acetone for at least 2 hours, prior to metal lift-off
- Load sample into Branson D-50 Ultrasonic for 10 - 20 seconds
- Rinse sample in DI for 2 minutes

8.2 Appendix B: Writing Conditions using JEOL 840 SEM

TABLE 6. SEM Writing conditions

Layer	Coarse Align	Fine Align	Current (pA)	Mag X	Dose (nC/cm^2)	Point Spacing	Line Spacing	Write Time
Fine AL Marks	yes	no	50	70	300	$400 \text{ \AA}^0$	$400 \text{ \AA}^0$	2 min
Pinhole	yes	yes	100	70	250	2000	2000	10 min
Ohmic Metal	yes	yes	200	70	150	400	400	35 min
Gate Metal	yes	yes	20	70	250	400	400	2 min