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◊A TRUE POLYSILICON EMITTER
TRANSISTOR

by

Michael Barry Rowlandson, B.Sc.

This thesis is submitted to the Faculty of Graduate
Studies and Research in partial fulfillment
of the requirements for the degree of

Master of Engineering

Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada

April 1988

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ISBN 0-315-40633-X

The undersigned hereby recommends to the Faculty of
Graduate Studies and Research acceptance
of the thesis,

A TRUE POLYSILICON EMITTER TRANSISTOR

submitted by Michael B. Rowlandson, in partial fulfilment
of the requirements for the degree of
Master of Engineering

Thesis Supervisor

Chairman,

Department of Electronics

Department of Electronics

Faculty of Engineering

April 1988

ABSTRACT

This thesis reports on the first polysilicon emitter transistors fabricated with the base emitter junction coincident with the polysilicon to single crystal silicon interface. This has been achieved by using in-situ phosphorus doped poly to form the emitter with no high temperature anneal step following the deposition.

The devices fabricated have some of the highest emitter Gummel numbers ever reported for bipolar transistors. Devices were found to be sensitive to interface preparation but not sensitive to emitter width, implying that the high emitter Gummel numbers result from the reflection of holes at or near the interface rather than from the minority carrier transport properties of the polysilicon. This device has potential applications in sophisticated VLSI processes where severe constraints on thermal budget place important restrictions on device design.

ACKNOWLEDGMENTS

I would like to thank Mr. L.Berndt, Mrs. J.McAinish and Mrs. C.Adams for their assistance in fabricating the devices studied in this thesis. I would also like to thank professor N.G.Tarr for originally suggesting this topic, for his help with the experiments and measurements, and finally for his patient guidance during the writing of this manuscript.

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CHAPTER 1.

INTRODUCTION

1.1 Motivation

Devices labelled as "polysilicon emitter" transistors have been reported in the literature for over a decade [1]. A cross-section through such a device is shown in Figure 1.1. Despite the name, in all polysilicon emitter transistors reported to date the polysilicon has simply served as a contact to a monocrystalline emitter region. In some devices the monocrystalline emitter has been formed by diffusion from a polysilicon doping source, while in others it has been formed in a more conventional fashion by ion implantation prior to polysilicon deposition. In all cases the structure has been subjected to an anneal following polysilicon deposition at a high enough temperature to ensure dopant diffusion into the substrate and, in all probability, major structural changes in the polycrystalline/monocrystalline interface.

FIGURE 1.1 A CROSS SECTION OF A CONVENTIONAL POLYSILICON
EMITTER TRANSISTOR

This thesis reports on what might be termed the first "true" polysilicon emitter transistor, in which the metallurgical base-emitter junction coincides with the polysilicon/substrate interface. This structure was formed by depositing in-situ phosphorus-doped polysilicon on a monocrystalline base region at a temperature too low for diffusion to occur, and avoiding any subsequent high temperature anneal.

Characteristics of devices produced with this technology are superior to conventional npn's in terms of current gain and, at least comparable to other polysilicon emitter transistors. The DC current gains reported for these transistors are the highest ever obtained for silicon bipolar devices. Examination of AC device characteristics was not attempted.

The use of as-deposited polysilicon to form the emitter offers some useful technological advantages. The absence of an emitter drive step in the fabrication sequence allows almost arbitrarily shallow base doping profiles to be used (ideal for superbeta transistors). In principle, there is no obvious reason why the usual gain- f_T tradeoff would not hold so these devices have potential for both high gain and high speed.

The low temperatures required for emitter formation allow additional flexibility in process design. Temperatures required for polysilicon deposition are compatible with some VLSI metallization schemes.

True polysilicon emitter transistors were found to be sensitive to the silicon substrate preparation prior to polysilicon deposition, but were not affected by the emitter thickness. The lack of dependence on emitter thickness, W_E (over the range of $15\text{nm} < W_E < 350\text{nm}$) suggests that the emitter characteristics are controlled purely by the interface and are not substantially affected by the bulk polysilicon properties. This result is different than some previously reported polysilicon emitter transistors and suggests that the mechanism responsible for gain improvement in these devices is different than conventional polysilicon emitter devices.

Potential applications of devices fabricated using this process are quite numerous. One important application is as a replacement for conventional high gain bipolar processes. These processes have quite low yields in general since conventional npn's require narrow, lightly doped base regions which are easily penetrated by emitter-

collector diffusion "pipes" [2]. Since this low temperature process has no possibility of an emitter collector diffusion pipe, the major yield loss mechanism for many bipolar processes has effectively been eliminated.

Because of the lack of any substantial thermal budget associated with emitter formation, this type of bipolar transistor should be easily integrated into a MOS process.

1.2 Thesis Outline

This thesis is organized into four main chapters. Chapter two reviews the published work related to polysilicon emitter transistors. The main theories of operation are discussed and related to measured electrical performance of devices reported to date.

Chapter three is a discussion of the experiments performed. The experiments are described in roughly chronological order. Important differences in device structure and fabrication procedure between the devices discussed here and those previously reported in the literature are highlighted in this chapter.

The fourth chapter relates the experimental results

reported in chapter three with the theories of polysilicon emitter operation discussed in chapter two. The devices reported in this work behave differently in a number of respects compared to previously reported polysilicon emitter transistors. It can therefore be inferred that the high temperature anneal step normally performed following polysilicon deposition produces changes in the structure of the polysilicon/silicon interface region that have a very significant effect on electrical performance.

Chapter five presents conclusions and some suggestions for applications and future work.

CHAPTER 2.

POLYSILICON EMITTER TRANSISTORS: A REVIEW

2.1 Introduction

In this chapter, a review of work to date on polysilicon emitter transistors is presented. Emphasis is placed on those papers which have suggested new physical models to explain the observed transistor characteristics rather than those which have emphasized obtaining precise "fits" between measured and calculated characteristics.

Much of the work to date on polysilicon emitter transistors has concentrated on the details of the emitter window surface preparation immediately prior to polysilicon deposition. Although numerous models have been proposed to explain the observed electrical characteristics, no model has been thoroughly verified by experiment. The theoretical development of the models themselves often relies on sweeping assumptions about the properties of the polysilicon or of the interface with little or no experimental justification.

2.2 Figures of Merit for Bipolar Transistors.

A brief discussion of some figures of merit for bipolar transistors is necessary to facilitate comparisons between devices.

The most widely quoted figure of merit is the common emitter current gain defined as:

$$h_{FE} = \frac{I_C}{I_B} \quad (2.1)$$

The common emitter gain represents a convolution of both base and emitter properties. To examine the emitter or base separately, we must use other figures of merit.

One important parameter is the emitter efficiency γ , defined as:

$$\gamma = \frac{\text{incremental electron current from the emitter}}{\text{incremental total emitter current}} \quad (2.2)$$

for npn transistors. Sze[3] shows how this reduces to:

$$\gamma = \left[1 + \frac{n_{po} D_p L_n \tanh(W_B/L_B)}{p_{no} D_n L_p} \right]^{-1} \quad (2.3)$$

for a uniformly-doped monocrystalline emitter with

n_{po} = equilibrium (minority) electron conc. in base

p_{no} = " " hole " in emitter

D_p = diffusion constant for holes in the emitter

D_n = " " " electrons in the base

L_p = minority carrier diffusion length in the emitter

This expression assumes no recombination in the emitter-base space charge region. The base transport factor is a measure of the minority carrier recombination losses in the base. From Sze[3]:

$$\alpha_T = \frac{\text{incremental electron current reaching collector}}{\text{incremental electron current from emitter}} \quad (2.4)$$

$$\alpha_T = \text{sech}(W_B/L_B) \sim 1 - \frac{(W_B)^2}{2(L_B)^2} \quad (2.5)$$

where

W_B = base width

L_B = minority carrier diffusion length in the base.

The usual case in modern bipolar transistors is that $W_B \gg L_B$ so $\alpha_T \sim 1$. Typical devices have $L_B > 10W_B$ so $\alpha_T > 0.995$. This usually means that the gain is determined purely by the emitter efficiency (unless the gain is extremely high).

A useful parameter in a transistor with a high base transport factor is the base Gummel number G_b , which is related to the number of impurities per unit area in the base by:

$$G_b = \int_0^{W_B} \frac{n_{i0}^2 N_A(x) dx}{n_{ib}^2(x) D_n(x)} \quad (2.6)$$

Here allowance has been made for the fact that the intrinsic carrier concentration n_{ib} in the base may be somewhat higher than the intrinsic carrier concentration n_{i0} in lightly doped material as a result of bandgap narrowing (equations (31) and (32) from chapter 3 of Sze[3]). In practice, n_{ib} and n_{i0} should be nearly equal in the base since the peak majority carrier concentration is usually not much greater than 10^{18} cm^{-3} . In the absence of recombination in the base, the collector saturation current density for forward active operation is given by:

$$J_{oc} = \frac{qn_i^2}{G_b} \quad (2.7)$$

The sheet resistance $R_{s, \text{base}}$ of the intrinsic base is

given by:

$$R_{s,base} = \left[\int_{base} q \mu_p(x) p(x) dx \right]^{-1} . \quad (2.8)$$

To the extent that the electron and hole mobilities are constant across the base, we therefore find that the base Gummel number is approximately proportional to the reciprocal of the base sheet resistance. If recombination in the neutral base is negligible, then at moderate to high values of V_{be} the base current will be dominated by the back injection of holes into the emitter. For a monocrystalline emitter, the base saturation current density is then given by:

$$J_{ob} = \frac{q n_{i0}^2}{G_e} , \quad (2.9)$$

where, by analogy to the base Gummel number, the emitter Gummel number G_e is given by:

$$G_e = \int_0^{W_E} \frac{n_{i0}^2 N_D(x) dx}{n_{ie}^2 D_p(x)} . \quad (2.10)$$

In transistors with non-conventional emitters, it is

still possible to write J_{ob} in the form given in (2.9), but G_e can no longer be given a simple interpretation in terms of the emitter doping profile as suggested in (2.10).

Assuming that the base current is dominated by back injection, then the current gain at moderate V_{be} is given by:

$$h_{FE} = \frac{J_{oc}}{J_{ob}} = \frac{G_e}{G_b} \quad (2.11)$$

(2.11) emphasizes that, for a given emitter structure, it is possible to obtain a high h_{FE} simply by minimizing the integrated doping in the base. This is not usually however, a practical approach to increasing h_{FE} , since reducing G_b lowers the current density at which high level injection effects such as base pushout are encountered, and results in an increase in the base resistance.

For this reason, G_b values for modern silicon transistors are typically in the 10^{10} to 10^{11} s cm⁻⁴ range. To obtain a high gain it is therefore necessary to minimize back injection or equivalently, maximize G_e .

In polysilicon emitter transistor, the back injection current is frequently suppressed to such an extent that there is no bias range over which the base current exhibits an ideal $J_b \propto e^{qV_{be}/kT}$ dependence on V_{be} . In devices with characteristics of this kind it seems reasonable that J_b is dominated by recombination in the base/emitter depletion region. G_e in this case can not be computed directly from (2.10). A lower bound on G_e can still be obtained, however, by noting that from (2.9) and (2.11)

$$G_e > \frac{h_{FE} q n_{i0}^2}{J_{oc}} \quad (2.12)$$

It is usually a straightforward matter to obtain J_{oc} , since the collector current normally follows an ideal $J_c \propto e^{qV_{be}/kT}$ law. The only assumption that must be made is what the exact value of n_{i0}^2 is (n_{i0} varies quite strongly with temperature).

2.3 Early Work

One of the earliest reports of polysilicon emitter transistors was made by Graul et al [1]. This early paper is particularly significant since it is one of the few reports to date on frequency response of polysilicon

emitter transistors.

The devices were fabricated on a 2.2 μm thick epitaxial layer with a heavily doped buried collector structure. A single step ion implantation was used to form the base. The total dose was varied from 5×10^{12} to $2 \times 10^{14} \text{ cm}^{-2}$ (either BF_2^+ or B^+ ions). A standard 30 minute anneal at 900°C was performed to remove implant damage.

After the emitter windows had been opened, a 300 nm thick layer of undoped polysilicon was deposited over the wafer surface using an LPCVD reactor. The poly was doped by a 100 keV arsenic implant. The implant energy was low enough to confine all of the implant damage to the polysilicon layer. The actual arsenic dose was varied, between 1×10^{15} and $5 \times 10^{16} \text{ cm}^{-2}$. After the arsenic implant, a high temperature furnace anneal (in the 900 to 1000°C temperature range) was carried out for an unspecified time (furnace anneals are typically a minimum of 30 minutes in duration).

It is significant that no explicit mention is made of any special treatment of the emitter window prior to polysilicon deposition. Later papers discuss details

of the surface preparation at some length.

In addition to the polysilicon emitters, conventional double implanted devices were fabricated for comparison purposes. These conventional devices were manufactured such that the dynamic parameters (eg. the unity gain frequency f_T and the emitter-collector transit time t_{EC}) were roughly equal to those measured for the polysilicon devices.

A comparison of device characteristics showed the polysilicon emitter to have a substantially higher G_e than the conventional device. The conventional transistors had a G_e of $1.5 \times 10^{13} \text{ s cm}^{-4}$ while the poly emitter devices were found to have G_e 's of approximately $1.9 \times 10^{14} \text{ s cm}^{-4}$. The measured f_T was 3.9 GHz for the poly emitter and 3.7 GHz for the conventional device. Both types of transistors had an identical t_{EC} of 30 picoseconds.

Graul et al attempted to explain these results in terms of a reduced bandgap narrowing in the polysilicon emitter (as compared with the bandgap narrowing in a single crystal emitter). The reduced bandgap leads to an increase in n_1 and a reduction in emitter efficiency (from (2.9) it can be

seen that the back injection current from the base is proportional to n_1^2). Since:

$$n_1^2 = N_C N_V e^{-E_g/kT} , \quad (2.13)$$

where N_C and N_V are equal to the density of states in the conduction and valence bands respectively, it follows that the emitter efficiency depends exponentially on the bandgap. Writing this in terms of gain and bandgap narrowing gives:

$$h_{FE} = h_{FE0} \exp[-\Delta E_g/kT] , \quad (2.14)$$

where h_{FE0} is the common emitter current gain which would be obtained in the absence of bandgap narrowing.

Graul et al made a plot of $\log h_{fe}$ versus $1/T$ for both polysilicon and conventional devices to obtain values for ΔE_g . Very good agreement to (2.14) was obtained. The slope gave a value of 44 meV for ΔE_g in the polysilicon device compared to a value of 70 meV for the conventional transistor.

Implicit in Graul's model is the assumption that conventional pn junction diode theory can be used to

predict the back injection current. The possible presence of a disordered region at the interface, or even of an ultra-thin interfacial oxide layer, casts doubt on the validity of such an assumption.

Graul et al did not suggest a physical reason why the bandgap narrowing might be less in polysilicon than in single crystal silicon. The bandgap narrowing model is also contrary to the generally accepted model for majority carrier conduction in polysilicon [4].

2.4 SIS Tunnel Emitter

Several years passed before another published report of polysilicon emitters appeared. de Graaf and de Groot [5] reported on a semiconductor-insulator-semiconductor (SIS) tunnel emitter structure that relied on an intentional interfacial oxide layer to provide an improvement in emitter efficiency.

The fabrication procedure as reported in [5] is unremarkable until the poly deposition step. After the emitter windows had been etched and immediately prior to polysilicon deposition, an oxide layer was deposited (using a plasma assisted deposition technique) or grown over the

emitter window opening. Both wet chemical treatment and plasma oxidation were used grow the thin layer of SiO_2 . The oxide thicknesses used in the experiments ranged between 2 and 6 nm (as measured by an ellipsometer). Immediately after the surface treatment (oxidation) 400 nm of polysilicon was deposited (undoped) using an LPCVD reactor. Polysilicon doping was accomplished by a two stage phosphorus diffusion at 900°C.

Subsequent analysis of the vertical doping profile revealed considerable uncertainty as to the exact state of the interface after polysilicon doping. Auger analysis showed a relatively broad oxygen peak at the interface corresponding to a peak concentration of 1.5 atomic percent oxygen (although this number is certainly distorted as the depth resolution of Auger analysis is not as fine as the oxide layer thickness).

SIMS analysis revealed a peak in both phosphorus and boron doping levels at the interface. This can be explained by the fact that dopant diffusion is much more rapid along a grain boundary (eg. the interface), hence it is quite reasonable to expect a pile-up of dopant to be observed since the interface is effectively a large grain boundary. However, both SIMS and Auger analysis (which

confirmed the phosphorus pile-up at the interface) measure only chemical concentration levels, and these do not translate directly into electrically active concentration levels. This lack of correspondence between chemical and electrical carrier concentration is especially true near the interface of the polysilicon - single crystal silicon where many carriers are captured in majority carrier traps causing a substantial difference between effective electrical carrier concentration and measured chemical dopant concentration.

Device electrical characteristics were strongly dependent on the method of oxide deposition/growth. Plasma oxidation at the interface produced superior devices in terms of emitter efficiency but with poor reliability and uniformity. Chemical oxidation of the surface produced devices with less dramatic improvements in emitter efficiency but with better reliability and uniformity. It is possible that some residual charge in the plasma oxide could be responsible for a favourable band bending (in order to induce a band bending favourable for npn gain improvement, the trapped charge would be positive and large.)

Before discussing further the results of measurements,

it is convenient to develop some theory behind the SIS tunnel emitter. A band diagram of the SIS tunnel emitter structure is shown in Figure 2.1.

The most important point to note concerning the operation of a tunnel junction emitter is that it is possible to suppress the hole back injection current into the emitter without interfering with the electron injection from the emitter into the base, even if the tunnelling probabilities for holes and electrons are similar[6]. Understanding this point requires identification of the bottlenecks for the flow of holes and electrons. The concentration of electrons on both sides of the interfacial oxide is large, resulting in large electron flows in both directions across the oxide. At moderate forward bias the rate at which electrons cross the base is, in comparison small, and in fact forms the bottleneck for electron motion from the emitter to the collector. A situation of quasi-equilibrium therefore exists between the electrons in the polysilicon and those at the surface of the monocrystalline substrate.

In terms of Figure 2.1, ΔV_n should be small in normal operation. In contrast, any hole injected into the polysilicon should recombine very quickly due to the high

Figure 2.1 The band diagram for a SIS tunnel emitter
From de Graaf and de Groot [5].

density of midgap energy levels in this disordered material. The bottleneck for hole flow is therefore the process of tunnelling across the oxide into the polysilicon, and so the hole flow is critically dependent on the height and width of the tunnelling barrier.

It seems at first that increasing the barrier thickness will increase the emitter Gummel number as the hole tunneling current will decrease. However, the voltage drop across the interfacial layer, ΔV_n increases as well. For devices with $\delta = 6$ nm, G_e was found to be 7.2×10^{14} s cm⁻⁴ at room temperature. It is clear from an examination of the Gummel plot of this device that G_e is a function of ΔV_n as the base current rises sharply above a junction voltage of ~ 800 mV.

de Graaf and de Groot explained these results by suggesting that the band bending term ψ_g was a decreasing function of V_n for large V_n . For the highest gain device, this implies an upwards band bending at the monocrystalline side of the interface.

A straightforward calculation of the emitter Gummel number (from 2.10) leads to a value for G_e of about 1×10^{13} s cm⁻⁴ if the device is treated as a simple npn

transistor. Clearly conventional npn theory cannot explain the results.

2.5 The Reduced Mobility Model

Although the tunnel model was quite successful at explaining de Graaf and de Groot's devices, it was incapable of explaining the results reported by workers who fabricated devices with no intentional oxide layer present at the interface.

About a year after de Graaf and de Groot's paper on the SIS tunnel emitter, a significant paper was published by Ning and Isaac[7]. In this paper, a comparison of various emitter contact technologies was presented. The three contact technologies examined were metal silicide (Pd_2Si), conventional $\text{Al}/1\% \text{Si}$ and polysilicon (with no intentional interfacial oxide layer between the polysilicon and the substrate). The central idea of their experiment was to form identical monocrystalline emitters that differed only in the type of emitter contact that was used (all devices saw identical thermal cycles). A comparison of the dc transistor characteristics was conducted and a simple model was proposed to explain the results for polysilicon contacted devices.

The devices under study here were all fabricated using a conventional double implantation process (arsenic was used for the n type dopant) up to the emitter contact step. On some wafers, polysilicon of two different thicknesses was deposited and then implanted with arsenic. All wafers (including those destined for Pd_2Si or Al contacts) underwent the same 30 minute 900°C anneal in nitrogen in order to ensure that the monocrystalline doping profiles were as close as possible to each other. No intentional interfacial oxide layer was grown prior to polysilicon deposition.

The results showed a reduced gain for the Pd_2Si contacted devices and an improved gain for the polysilicon contacted devices (with reference to the conventional Al contacted control devices). The reduction in gain for the Pd_2Si devices is easily explained as the width of the emitter is much less than the hole diffusion length thus leading the base current to depend inversely on emitter thickness. As about $1/4$ of the emitter was consumed in formation of the contact, it is quite reasonable to expect the gain to fall by a similar amount. For a thin emitter:

$$J_p = \frac{qD_p n_{ie}^2 \exp [qV_{be}/kT]}{N_D W_E} \quad (2.15)$$

when $W_E \ll L_p$.

The improvement in gain observed with the polycrystalline silicon contacted devices was explained using a two region mobility model which hypothesises that the minority carrier mobility is reduced in the polycrystalline part of the emitter. Figure 2.2 shows the hole distribution postulated by Ning and Isaac, with the hole mobility reduced in the polysilicon (as compared to the monocrystalline part of the emitter). A calculation of the emitter Gummel number can be done both for the case of no polysilicon layer (ie. the control devices) and the presence of a polysilicon layer. An important assumption in this calculation is that the hole diffusion length in the polysilicon is much larger than the width of the polysilicon layer. If this assumption is true, then the emitter Gummel number improvement can be calculated from (2.15) and Figure 2.2.

$$\frac{G_e(W_1)}{G_e(W_1=0)} = 1 + \frac{D_{p2}W_1}{D_{p1}W_2} = \frac{h_{FE}(\text{polysilicon})}{h_{FE}(\text{control})} \quad 2.16$$

It is clear that if the hole mobility is much smaller in the polysilicon the gain will be improved (as D_p

FIGURE 2.2: A plot of hole distribution in a polysilicon emitter as proposed by Ning and Isaac [6]. The solid line represents the hole distribution in a polysilicon emitter while the dashed line represents the hole distribution in a conventional single crystal emitter (from Ning and Isaac [6]).

varies inversely with mobility). Because of the problems with measuring the minority carrier mobility, Ning and Isaac assumed that the minority carrier mobility was identical to the majority carrier mobility of the same type of carrier in similarly doped material i.e., for holes in 10^{20} As doped polysilicon, they measured mobility for 10^{20} B doped polysilicon and assumed they were equivalent.

As well, the base current was observed to be a function of the emitter thickness. The thin emitter (30 nm of poly) had a base current about 1.7 times that of the thick emitter device (300 nm of poly).

An examination of the temperature dependence of the base current showed the thin poly emitter device to exhibit a stronger dependence on temperature than the thick poly emitter device. Ning and Isaac attributed this to an increase in hole diffusion length with temperature which would rapidly cause the thin poly device to be dominated by the ohmic contact, whereas this will be delayed in the thick poly device until the minority carrier diffusion length is quite large.

All of the data presented by Ning and Isaac seem to

support the claim of a two region mobility function. There are several points however that indicate some problems with their model.

The monocrystalline part of the emitter has been changed in the polycrystalline samples. Both the Pd_2Si and Al contacted devices had $r_{\text{base}} = 7.2 \pm 0.2$ kohms/square, but the polysilicon contacted devices had $r_{\text{base}} = 7.6 \pm 1.0$ kohms/square. It would seem that the monocrystalline device is not identical in all cases as Ning and Isaac had supposed. This is very probably due to different diffusion characteristics for boron and arsenic in the presence of a heavily damaged polysilicon layer at the surface.

No attempt is made to account for recombination in the polysilicon. In view of the highly disordered grain boundaries, with trap densities expected on the order of $10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$, the assumption of no recombination at the grain boundaries does not seem to be very reasonable.

Finally, no physical reason for the reduced minority carrier mobility in the poly is offered. It is generally believed that the reduction in the apparent mobility of majority carriers in polysilicon results from the formation

of potential energy barriers to majority carriers associated with the high density of midgap energy levels at the grain boundaries. Majority carriers must then pass over these energy barriers by a process of thermionic emission[4] . There is no reason however, to expect a potential barrier to majority carriers to interfere with minority carrier flow. Although it is plausible that both majority and minority carrier might undergo frequent scattering events in a disordered material such as polysilicon, it does not seem reasonable to conclude that the ratio of minority carrier mobility to majority carrier mobility should be the same in polycrystalline material as in monocrystalline material.

Despite the shortcomings of the two region mobility model, it has an important advantage over the tunnel model because it explains the gain improvement observed for devices with no intentional interfacial oxide layer present.

2.6 Intentional Oxide Treatments

Two years later, several papers appeared that discussed the influence of various surface treatments on the electrical characteristics of polysilicon emitter

transistors [8,9,10]. These papers were all aimed at an examination of the influence of oxide thickness (using chemical oxide growth techniques) on transistor characteristics.

A study of the effect of various interfacial oxide treatments was presented by Duffill[8] at the 1982 ESSDERC conference. Transistors subjected to various wet chemical growth techniques for the interfacial oxide layer were examined and compared to devices fabricated with only a dilute HF dip prior to polysilicon deposition. The effect of HCl as an in-furnace clean was examined and the effect on oxide thickness of a high temperature anneal was also considered. Three chemical surface treatments were used prior to poly deposition: Caro's acid, the second part of the RCA clean, and a solution of dilute HF at 30°C. Oxide thicknesses were measured using an Auger spectrometer with the sputtering rate calibrated to provide a thickness measurement.

As expected, the dilute HF treatment grew only about 0.3 nm of oxide at most on the samples studied. In some cases, no oxide layer at all was found. The Caro's acid clean showed about 0.5 to 1.0 nm of oxide on all samples and the RCA clean grew about 1.0 to 1.5 nm of oxide on all

samples.

HCl was used in an attempt to clean the wafers in the furnace. Experimental observations showed some small thickening in the oxide layer! This thickening was small enough (0.2 nm) to be masked by wafer to wafer variations hence it seems that the HCl clean has a negligible effect on the oxide thickness.

The effect on oxide thickness of high temperature furnace anneals at 900, 1000 and 1100°C was examined. Some evidence of an oxide layer was still detectable after a 15 minute anneal at 1100°C (although its thickness was reduced). The wafers showed an inverse relationship between anneal temperature and final oxide thickness (as expected).

Transistors fabricated with these chemically grown interfacial oxide layers showed improved gains. Furthermore, the gain improvement is due to base current suppression as all devices exhibited virtually identical collector currents.

Duffill acknowledged that with such small oxide thicknesses, it was unlikely that the interfacial layer was

pure SiO_2 (ie. stoichiometrically correct) or that it was necessarily continuous. A more realistic view of the layer (after high temperature anneal) might be oxygen doped silicon or discontinuous layers of SiO_x ($x < 2$). It is impossible to tell from Auger measurements what the nature of the interface is as it is sensitive to Si-Si or Si-O bonds and does not (directly) give any information about the stoichiometric makeup of the interfacial layer.

A similar paper by Soerowirdjo et al [9] compared both arsenic implanted and phosphorous diffused emitters as well as HF dip etch and RCA cleans of the interface prior to polysilicon deposition.

It was shown that the devices given a dip etch immediately prior to poly deposition have gains a factor of three better than the conventional control devices. Devices with an RCA clean had gains between 7 and 32 times greater than the control devices.

The emitter was formed by LPCVD of polysilicon at 600°C . Two methods of doping the emitter were used: ion implantation of arsenic, and phosphorous doping from a POCl_3 source. The phosphorus doped emitter was found to have lower series resistance than the arsenic doped

emitter, but no difference in G_e was observed between differently doped emitters [11].

The conclusion of the study was that devices exposed to an HF dip but no RCA clean (ie. no intentional oxide layer present) were best explained using the Ning and Isaac mobility model. Devices which were subjected to an RCA clean prior to polysilicon deposition were best explained by the de Graaf and de Groot tunnel model. Plots of current gain versus inverse temperature show clearly that two different temperature dependencies were present.

Device modelling efforts (analytic and numerical) attempted to unite both the tunnel model and the two region mobility model to form a comprehensive model capable of predicting device characteristics over a fairly complete range of temperatures and oxide thickness [12]. Both types of models had fair success in fitting the observed device characteristics, but neither was thoroughly tested against experimentally variable device parameters (eg. oxide thickness). Device modelling attempts were frustrated by a lack of any independent measurement of model parameters. No evidence of a reduced minority carrier mobility had been produced so models which assumed a reduction by a factor of three in D_p in the poly were really based on very little

experimental evidence.

2.7 Minority Carrier Transport at the Interface

Neugroschel et al [13] examined minority-carrier transport at the polysilicon-silicon interface with a series of experiments using pn diodes. The structures used in this experiment are shown in Figure 2.3. All of the diodes reported in this paper were n-epi on p substrates with various contacts to the n-epi material. Three different polysilicon layers were used to contact the n-epi material: 1) 150 nm of undoped poly, 2) 150 nm of in-situ arsenic doped poly and 3) a bilayer of 50 nm undoped poly followed by 100 nm of in-situ doped poly.

Comparison of these devices to control devices allowed a calculation of the maximum recombination velocity at the epi-polysilicon interface. It was found that undoped poly devices and bilayer structures with insufficient anneals to drive the arsenic to the interface had very high recombination velocities at the interface ($\sim 10^4 \text{ cm} \cdot \text{s}^{-1}$). In-situ doped devices and bilayer devices with substantial thermal anneals were observed to have recombination velocities of only $\sim 180 \text{ cm s}^{-1}$. Note that only the chemical concentrations of arsenic were found to

Figure 2.3: A cross-section of the device used by Neuroschel et al [13] to study minority carrier injection into the polysilicon. Devices were fabricated with and without the n+ contact ring (on each wafer). Control devices with no polysilicon film were also present.

be important, not the electronically active concentrations.

The reduction in diode saturation current was attributed to greatly reduced hole mobility in a thin interfacial layer extending up to 30 nm from the interface. The model also required that no recombination occurred while the holes were confined to this thin interfacial layer.

Although this model worked well to explain the experimental results, no disordered layer has been observed experimentally by any other workers. Bravman et al [14-16] have produced TEM photographs that show no evidence of any disordered region near the interface.

2.8. Summary

Numerous papers have appeared [17-19] on the subject of integrated circuit processes for bipolar transistors using polysilicon emitters. Despite its substantial advantages, both in terms of device characteristics and technologically, a lack of understanding of the exact mechanism responsible for the gain improvements has hindered the acceptance of the device structure as part of a manufacturable IC process.

Work to date on polysilicon emitters can be divided into those results which support the tunnel emitter theory and those which support the transport theory. Neither model is completely satisfactory and neither has been thoroughly verified by experiment. However, much of the work to date on polysilicon emitters has focussed on interface preparation technique and no effort has been made to examine the effect of high temperature anneals on device characteristics. Although a high temperature anneal serves to activate the majority carrier dopant, there is no experimental report on how this anneal affects the device characteristics (which depend strongly on minority carriers for bipolar devices). The exact composition of the interface (for the case of thin oxide layers) is unknown, although recent high resolution TEM photographs have provided some insight.

CHAPTER 3.

EXPERIMENT AND OBSERVATIONS

This chapter will outline some device design considerations, the design of the mask set used for all of the experiments and the details of the experiments performed. Observations made on the devices fabricated with these experiments will also be reported.

3.1 Device Design Considerations

Before discussing the experiment and the results, it is appropriate to examine some of the important points concerning device design, as it will outline which parts of the process are most important to the device characteristics and will explain some of the limitations on processing latitude. The design of a bipolar transistor can be broken down into three parts: design of the collector, of the base and of the emitter. Changing the design of any one part of the device will have some effect on all other parts, but for now, each will be treated independently.

3.1.1 Collector Design

Design of the collector is fairly straightforward if AC characteristics are not a concern. The prime concern of this work is the DC characteristics of the emitter-base junction hence collector design is greatly simplified. Isolation and buried collector structures are not required since collector resistance is not important and device isolation is only required for circuits. An epitaxial layer is required for the manufacture of discrete devices only if one wishes to minimize R_C while maintaining a high BV_{CEO} .

The only important concerns in the design of a collector, suitable for our devices is that 1) a good ohmic contact exist to the substrate and 2) the collector doping near the base should be low compared to the intrinsic base doping so as not to deplete a significant portion of the base at moderate collector-base reverse bias.

Substrates with a resistivity range of 1 to 10 ohm-cm. (phosphorus doped) were chosen. This provided a range of collector dopings from mid 10^{14} to mid 10^{15} cm^{-3} .

This doping range is satisfactory since it appears lightly)

doped with respect to the intrinsic base. Most of the intrinsic base will be doped in the mid 10^{16} cm^{-3} range and higher.

To ensure a good ohmic contact to the lightly doped substrate, a heavy phosphorous diffusion is done into the backside of the wafer. Ohmic contact to the collector is made through the backside of the wafer using a conventional aluminum metallization scheme. The heavy phosphorus diffusion also serves to getter heavy metals from the rest of the wafer where they will not affect device performance. Heavy metals will reduce the minority carrier lifetime in the base region (and thereby reduce the gain)

3.1.2 Base Design

Design of the base is much more complex than the design of the collector. The base must be narrow to allow high gain and high speed, but not too resistive since this will lead to non-uniform injection conditions across the base. The doping should not be too high since in the absence of recombination in the base, G_b determines the gain.

Given that we wish to examine the emitter injection efficiency, we wish to minimize the reduction in gain resulting from recombination in the base. This requires a minority carrier lifetime in the base that is large compared to the emitter collector transit time. Typical causes of reduced minority carrier lifetime are poor crystal quality, high levels of metallic contaminants or improperly annealed ion implantation damage. A very narrow base will reduce the total amount of recombination current (assuming a constant defect density throughout the base) and reduce the base transit time. This will allow the current gain to be controlled by the emitter injection efficiency.

A narrow base implies a high base spreading resistance and series resistance. Both of these effects will lead to "parasitic" voltage drops which are not desirable since the exact base-emitter junction voltage will not be known. Spreading resistance effects will lead to non-uniform injection conditions prevailing throughout the intrinsic base. It is possible for both high-level and low-level injection conditions to exist in different parts of the base due to the voltage drop caused by the base current being forced through a high resistance path in the intrinsic base.

The problem of base series resistance can be relieved by using a two part base design. This uses a highly doped extrinsic base region to contact a lightly doped (active) intrinsic base region. The edge of the extrinsic base extends as close to the emitter window opening as photolithographic tolerances will allow.

The problem of base spreading resistance is more difficult to solve. It requires the intrinsic base to have a lower sheet resistance. Unfortunately, there are several very good reasons why this solution is not possible. The reduction in sheet resistance cannot be obtained by making the intrinsic base thick (since this would increase the base recombination current). The other alternative is to keep the base shallow but increase the doping concentration. At first this solution might seem workable but there are some practical problems that limit this. The gain of the device is strongly affected by the base Gummel number (ie. the higher the doping, the lower the gain). There are also problems with annealing heavy implant damage (this may cause increased base recombination current). Finally, if the surface doping concentration gets too high then the junction may start to lose some of its rectifying characteristics due to the very high electric field.

All of the above factors combine to limit the practical range of intrinsic base doping to the range from 10^{16} cm^{-3} to 10^{18} cm^{-3} . The best way to reduce the spreading resistance to acceptable levels is to avoid device designs that have many "squares" of intrinsic base material. The best design is thus one with long thin stripes of intrinsic base material contacted by extrinsic material as close as possible to the emitter window regions.

3.1.3 Emitter Design

The design of the emitter is central to this work. The use of polysilicon to form the emitter is not new and it is known to provide some substantial advantages over emitter formation using conventional implantation or diffusion techniques. Emitter design using polysilicon is complicated due to the variety of interface treatments of the emitter window prior to polysilicon deposition and annealing procedures that have been used by previous authors.

Requirements for any emitter are that it must have low series resistance (due to the large current flowing) and should be heavily doped with respect to the intrinsic base so that forward current gain is maximized. Heavy doping effects combine to limit the effectiveness of increasing the emitter doping concentration at very high levels.

3.2 Mask Set

A mask set was designed for use in these experiments. Eight mask levels are used, although an abbreviated process sequence using only five levels is possible. Table 3.1 shows the mask levels with the essential levels noted with asterisks.

The mask set contains transistors of various areas (measured at the emitter window level) and geometries. There are also van der Pauw patterns to measure sheet resistance of various levels and contact resistance patterns. Finally, etch and resolution monitors for each level are provided to assure that the lithography and etching steps are well controlled.

Table 3.1: MASK LEVELS

LAYER NUMBER	IDENTIFICATION
01	Extrinsic (inactive) base
* 02	Intrinsic (active) base
* 03	Emitter window
* 04	Polysilicon emitter
* 05	First contact (to base)
* 06	First metal (to base)
07	Second contact (to emitter)
08	Second metal (to emitter)

* denotes essential masking levels.

The areas of the transistors studied must therefore be such that a large range of current densities can be generated by a single piece of test equipment. A large range of device areas must be designed with care taken to ensure that parasitic resistance effects are minimized for all designs.

There is another concern with transistor design that is related to the emitter metallization scheme. It is known [22] that an aluminum layer over unannealed LPCVD poly will rapidly diffuse through the poly during a metal sinter step leading to a very leaky emitter-base junction in our case. It is clear that if a simple Al metallization scheme is to be used, then a metal overlap of the active emitter base window prohibits the use of a metal sinter step after aluminum deposition. The alternative is to not allow the emitter contact metal to overlap the active emitter window area. This allows a sinter step to follow the emitter metal deposition step but it has the effect of increasing the emitter spreading resistance and complicating the analysis of the results since the emitter base junction voltage would not be uniform across the entire emitter window. Both types of device designs were included in the mask set.

A plot of the complete mask set is presented in Figure 3.1

3.3 Experiments

3.3.1 Introduction

The experimental work can be divided into three broad sections: 1) the establishment of a baseline process, 2) an examination of the effects of an oxidizing step prior to poly deposition and 3) a study of the effect of varying the emitter width on device characteristics.

The establishment of a baseline process was aimed at examining the basic electrical characteristics of the polysilicon - silicon junction with respect to minority carrier injection in particular. Devices fabricated using this process had relatively thick emitters and no intentional interfacial oxide present prior to polysilicon deposition.

An investigation of various oxidation techniques for introducing a thin interfacial oxide layer prior to polysilicon deposition was later conducted.

Figure 3.1 A plot of the mask set used for all experiments in this thesis.

A simple way to investigate the effect of bulk polysilicon parameters on device characteristics is to vary the thickness of the polysilicon used to form the emitter. Since the interface should be the same in the thin emitter devices as in the thick emitter devices, any change in device characteristics should be due to the properties of minority carrier transport in polysilicon.

The combination of these experimental results should allow the separation of device characteristics that are attributable to the bulk polysilicon and those that are attributable to the interface.

The first experiment attempted was designed to provide a very preliminary idea about the electrical characteristics of an unannealed polysilicon-silicon junction. In order to facilitate a rapid turnaround time for processing, an abbreviated mask set/process sequence was used. Naturally certain compromises in device performance were to be expected but, the basic junction electrical characteristics would not be affected (ie. only "parasitic" effects would change). The abbreviated process sequence is presented in appendix A.

The use of a single base diffusion step rather than a two step base (ie. both extrinsic and intrinsic bases) means that the base series resistance will be very high. This saves a mask and a diffusion step however and will not affect device characteristics provided that base currents are kept to the $A \cdot cm^{-2}$ range and below. Since the intrinsic base mask overlaps all of the extrinsic base regions, there is no problem in making ohmic contact to the base.

Another simplifying step is the omission of the emitter metal deposition. This saves the deposition step as well as two masking steps (levels 7 and 8). Probing the polysilicon directly will lead to a substantial contact resistance in series with the emitter, but should not be a problem if emitter currents are kept low.

Both of the preceding process modifications will lead to series resistance effects that will dominate device characteristics at high current levels, however at low current levels, the parasitic voltage drops are negligible and the transistor characteristics should be unaffected by the modification to the process.

The most critical step in the process is the interface preparation prior to polysilicon deposition. The wafers were given a 10 second dip etch in a 10:1 solution of DI water and HF immediately prior to being loaded into the furnace tube for poly deposition. After the dip etch, the wafers were quenched in running DI water for 5 minutes and then dried in dry N_2 . This etch step was done to ensure that any residual oxide that grew following the emitter window etch step was removed. Every reasonable effort was made to ensure that the time elapsed between etch and pumpdown in the furnace was minimized. In general, this time was kept to five minutes or less. During this five minute exposure to air, some oxide undoubtedly grew on the emitter window area but this is probably unavoidable from a practical viewpoint. It is certainly of minimal thickness in any event. TEM photographs from Stanford University suggest this is only a single atomic layer thick [16] and may not be continuous.

Polysilicon deposition was carried out in a LPCVD reactor at 627°C. from a mixture of SiH_4 and PH_3 diluted with silane to give an effective $SiH_4 : PH_3$ flow ratio of 300:1. This is approximately the flow ratio that produced optimal polysilicon-silicon diodes in earlier experiments by Liebllich and Bar-Lev [23]. These growth conditions produced a growth rate of about 3 nm s^{-1} .

Work done by Harbeke et al [24] suggests that the grain size should be only a few hundred angstroms in diameter, though this value was not measured for any of our samples.

Following the polysilicon deposition, the wafers were patterned and the polysilicon was etched in a plasma etcher using a freon/oxygen mixture. Metallization of the front and back of the wafer was done in an e-beam evaporator. 0.5 μm of aluminum was deposited. The wafer fronts were patterned to allow contact to the base regions and the aluminum was wet etched in a solution of hot phosphoric acid.

The final step of wafer processing was a metal sinter step to ensure a good ohmic contact to the base and collector. The sinter step was done at 450°C for 20 minutes in a H_2 ambient.

The first results of these experiments were very encouraging. Common emitter current gains of several hundred were routinely found, with some values of h_{FE} in excess of 1000. A plot of typical common emitter characteristics is shown in Figure 3.2.

Figure 3.2 Common emitter characteristics for a typical transistor from wafer GTE-2. No metal contact to emitter. Base current is scanned from 0 to 60 nAmps. The transistor area is $1.75 \times 10^{-5} \text{ cm}^2$.

Although there were several problems with these first devices, such as a fall-off in gain at high collector current, the most important point observed is that the unannealed polysilicon-silicon junction is able to act as a very efficient emitter. These first results encouraged more detailed investigation with wafers following a process flow similar (but not identical to) the one used in the first run.

3.3.2 Development of a Baseline Process

A second experiment was conducted that followed closely on the process used in the first experiment. A more complete mask set was used to provide a metal contact to the emitter as well as a two step base formation. An overview of the process flow presented in appendix B,

The extrinsic base was formed by diffusion. The intrinsic base was formed by implantation of B^+ ions at 50 keV energy. Dose was varied between 10^{12} and 10^{13} ions/cm² and annealing was done at either 950°C or 1000°C for 30 minutes. SUPREM3 simulation of the various device doping profiles are presented in Figure 3.3.

Figure 3.3 (a): SUPREM simulations of the net doping profile in the base collector region. Implant conditions were Boron at 50 keV and $1\text{E}12\text{ cm}^{-2}$ dose with a 950 C. half hour anneal.

Figure 3.3 (b): SUPREM simulations of the net doping profile in the base collector region. Implant conditions were Boron at 50 keV and $1E13 \text{ cm}^{-2}$ dose with a 1000 C. half hour anneal.

Metallization of the emitter was done using thermal evaporation of aluminum by resistive heating of a tungsten filament. Although base and collector metallization was done using e-beam evaporation of aluminum, the radiation damage (X-rays due to Bremstrahlung) caused by this processing step would require a sinter in H_2 at approximately $400^\circ C$ following the evaporation to remove this damage. Unfortunately no sinter step is possible with aluminum overlying the emitter windows since aluminum is known to penetrate the grain boundaries very rapidly. The presence of a high concentration of aluminum at the interface will lead to very leaky junctions with very high generation current in forward bias. A thermal evaporation eliminates the damage due to X-rays although the deposited metal is not as pure as the e-beam evaporated metal. There is some danger of sodium contamination of the aluminum as sodium is incorporated as an impurity in tungsten and tungsten is soluble in aluminum. The collector base junction is somewhat leaky, suggesting a problem with mobile ion contamination.

The devices produced by this experiment gave startling results. Transistor gains of several thousand were found on many devices and gains of about 20,000 were found on a few devices. Wafer number GTE-4 produced the most

exceptional gains, although the processing of the wafer was in no way intentionally different than the other wafers in this batch.

The problem of comparing our devices to previously reported devices is now apparent. Although common emitter current gain is a commonly noted figure of merit, it actually compares both the base and emitter properties. In order to compare emitter properties only, which are the prime concern of this work, it is necessary to find a figure of merit which depends on the emitter properties only. One such commonly used figure of merit for emitters only is the emitter Gummel number, introduced in chapter two.

Table 3.2 presents data on the experimentally determined emitter Gummel numbers for wafers in this batch. G_e values as high as $5 \cdot 10^{15} \text{ s} \cdot \text{cm}^{-4}$ were obtained. By way of comparison, emitter Gummel numbers in the low to mid $10^{13} \text{ s} \cdot \text{cm}^{-4}$ are typical for good conventional BJT's while values in the mid 10^{13} to mid $10^{14} \text{ s} \cdot \text{cm}^{-4}$ range have been reported in the literature for polysilicon emitter transistors. The devices fabricated in run number two compare quite favourably with previously reported polysilicon emitter

Wafer number	Ge,max	Ge,avg
GTE-4	5.0E14	2.1E14
GTE-12	1.4E14	4.5E13
GTE-13	3.8E14	4.3E13
GTE-19	2.7E13	1.5E13

Table 3.2 Emitter Gummel numbers for run number 2.

transistors. A selection of common emitter characteristics is presented in Figure 3.4 and a selection of Gummel plots is presented in Figure 3.5. A plot of current gain versus current density can be seen in Figure 3.6.

There are several points worthy of note for devices fabricated in run number two. The current gain versus current density plots show that all devices experience a very rapid falloff in gain as the collector current exceeds about $1000 \text{ A}\cdot\text{cm}^{-2}$. The initial falloff in gain occurs somewhat before this and is more gradual (roughly one decade of gain per decade of current). The rapid falloff occurs for currents in excess of about $1000 \text{ A}\cdot\text{cm}^{-2}$ and is at a rate of about four decades per decade.

The second point to note is the very low Early voltage on the devices with highest gains. Early voltages of roughly 3.5 V are typically found on wafer GTE-4, the wafer with the highest current gain. This is unacceptably low for many practical purposes where 5 volt operation is essential, but it does compare very favourably to previously reported super beta transistors [25].

Figure 3.4(a) Common emitter characteristics for a typical transistor from wafer GTE-12. No metal contact to emitter. Base current is scanned from zero to four nAmps.

Figure 3.4(b) Common emitter characteristics for a typical transistor from wafer GTE-4. Metal contact to emitter. Base current is scanned from zero to four μAmps .

Figure 3.4(c) Common emitter characteristics for a typical transistor from wafer GTE-4. Metal contact to emitter. Base current is scanned from zero to four microamps.

Figure 3.5 (a) Gummel plot of a typical transistor from wafer GTE-2. This wafer is from the first batch produced and there is no metal contact to the emitter.

Figure 3.5 (b) Gummel plot of a typical transistor from wafer GTE-12. Implanted base (dose= $1E13$ cm⁻²) with a 1000 C. 30 minute anneal.

Figure 3.5 (c) Gummel plot of a typical transistor from wafer GTE-4. Implanted base (dose= $1E12cm^{-2}$) with a 950 C. 30 minute anneal.

Figure 3.6 (a) A log-log plot of current gain versus current density for GTE-19. Note the abrupt drop in gain above 200 Amps/cm².

Figure 3.6 (b) A log-log plot of current gain versus current density for GTE-4. Note the abrupt drop in gain above 1000 Amps/cm².

An increase in the collector-base voltage increases the gain in all cases. The base Gummel number is reduced as the collector-base space charge region extends into the metallurgical base region (recall that transistor gain is inversely proportional to base Gummel number as in (2.11)).

It can be seen that the best estimate of the emitter Gummel number is obtained for the largest collector base voltage possible without base punchthrough or avalanche effects contributing significantly to the measured current. If we assume that recombination centres due to unannealed implant damage are distributed more or less uniformly throughout the base, then the less undepleted base present, the less will be the recombination current component of the measured base current. This in turn means that one of the approximations made in the calculation of the emitter Gummel number becomes more accurate (ie. the approximation that the entire measured base current is due to the hole injection into the emitter).

Typical curves showing variation in current handling with collector-base voltage are shown in Figure 3.7. Increasing collector-base voltages allows higher collector currents to be observed before a sharp falloff in gain occurs. Note also in Figure 3.8 that I_b is reduced by

Figure 3.7 The effect of collector base voltage on the current gain falloff point. The bottom curve represents $V_{ec}=1.0$ Volts and the top curve represents $V_{ec}=8$ Volts. Results are from wafer GTE-19.

Figure 3.8 The effect of collector base voltage on base current. The top curve shows base current for $V_{bc}=0$ volts and the bottom curve shows the base current for $V_{bc}=6$ volts.

increasing V_{bc} indicating a reduction in the base recombination current. It is clear that the transistors fabricated in this experiment are at least comparable with previously reported polysilicon emitters, in terms of emitter Gummel numbers.

Good devices have been obtained with a simple very low temperature process. Of particular interest is an investigation of how the emitter Gummel number is affected by different surface preparation techniques prior to polysilicon deposition

3.3.3 Oxide Interfacial Layers

Two wafers with diffused bases were selected for an experiment designed to grow a thin thermal oxide over the emitter window immediately prior to polysilicon deposition. Process specifications for this experiment are given in appendix C. A thin thermal oxide was grown at 500°C in a dry O_2 ambient for 20 minutes. Polysilicon deposition followed immediately after the oxidation cycle.

A typical Gummel plot for a finished device is shown in Figure 3.9. Clearly the device characteristics have been severely degraded by the presence of such a thick oxide layer. Previous reports lead us to believe that this oxide layer is only a few tens of angstroms thick, however this thickness seems enough to produce severe tunnel resistance effects.

Subsequent attempts to grow oxide on the interface prior to polysilicon deposition did not yield any better devices. It seems that there is no advantage to growing an oxide at the interface prior to polysilicon deposition for true polysilicon emitter devices.

3.3.4 Polysilicon Thickness

Next, the effect varying the polysilicon film thickness on device characteristics was investigated. Until this point, all wafer runs had the same polysilicon thickness (about 350 nm).

Polysilicon deposition times were varied from 3 minutes to 30 minutes, with all other aspects of the processing kept standard (two part diffused bases, HF dip-etched prior to polysilicon deposition in the usual way). It was felt

Figure 3.9 Gummel plot for a transistor with a thermal oxidation prior to poly deposition. Wafer MR-14. RCA clean followed by 500°C oxidation.

that examining the wide variation in polysilicon thicknesses would reveal any effect that poly thickness has on device characteristics (the anticipated range of thickness was 15-350 nm).

Typical device Gummel plots from each wafer are presented in Figure 3.10. These plots show essentially no difference between all three wafers. Average Gummel numbers are presented in Table 3.3. Common emitter characteristics are presented in Figure 3.11.

This result is of critical importance. Although W_E has been varied by more than one order of magnitude, no variation in emitter Gummel number is observed. This result is not consistent with minority carrier mobility models but strongly suggests an interface controlled device.

3.5 Summary

A review of all of the experiments has been presented. Initial experiments produced devices with high values for G_e .

Experiments were conducted to investigate the effects of growing (thermally and chemically) a thin interfacial

Figure 3.10(a) A Gummel plot for a transistor with a thick poly emitter (350 nm nominal thickness). Wafer MR-16.

Figure 3.10(b) A Gummel plot for a transistor with a thin poly emitter (15 nm nominal thickness). Wafer MR-1.

Wafer number	Poly thickness	Ge,max	Ge,avg
MR-1	350 nm	1.7E14	8.7E13
MR-2	50 nm	1.6E14	3.2E13
MR-5	50 nm	6.2E13	4.3E13
MR-6	15 nm	6.8E13	4.9E13
MR-16	15 nm	3.4E14	7.1E13

Table 3.3 Emitter Gummel Numbers for Wafers with Different Poly Thickness.

Figure 3.11(a) Typical common emitter characteristic for thin poly emitter transistor. Wafer MR-1. Base current stepped from zero to four microamps.

Figure 3.11(b) Typical common emitter characteristic for thick poly emitter transistor. Wafer MR-16. Base current stepped from 0 - 0.4 μ Amps.

oxide layer. The results were not encouraging and the devices exhibited extremely high emitter series resistance.

An investigation of the effect of varying the emitter thickness showed no sensitivity of device characteristics to emitter width.

CHAPTER 4.

DISCUSSION OF RESULTS

4.1 Introduction

In this chapter, the experimental results reported in chapter three for the true polysilicon emitter structure are compared with results reported for "conventional" polysilicon emitters, and with existing theories of polysilicon emitter operation. True polysilicon emitter transistors are found to behave differently than devices subjected to a high temperature anneal after polysilicon deposition. The evidence suggests that the very high emitter Gummel numbers obtained with the true polysilicon emitter result from a quantum reflection effect at the interface.

Performance limitations in the true polysilicon emitter structure are also discussed.

4.2 Comparison with Previous Results and Models

The most important result of the previous chapter is that the true polysilicon emitter transistor has a very high emitter Gummel number, superior to conventional npn's and comparable to "conventional" polysilicon emitter transistors. The absence of an intentional oxidation prior to the emitter deposition suggests that a continuous thin interfacial oxide layer may not be essential to improved operation for our devices.

It is interesting to note that work by Soerwirdjo et al [10] on annealed devices suggests that the interfacial oxide layer is important to device operation. Soerwirdjo's experiments examined conventional npn's, dip-etched polysilicon emitters (the same interface treatment used for our devices) and devices prepared with an RCA clean prior to polysilicon deposition. The dip etched devices were inferior to the RCA clean devices, which are thought to have ~1.5 nm of thermal oxide present prior to polysilicon deposition.

It is clear that our devices have some oxide present in the emitter windows prior to polysilicon deposition. How much oxide is present, whether it is continuous or even if

it is important to device operation cannot be said for certain. High resolution cross-sectional TEM photographs of the interface [14-16] suggest that the oxide layer is not continuous, and that the amount of oxide present is a function of the exact cleaning and loading procedure used. Ashburn et al have found that a thin interfacial oxide layer is important to their devices as it acts to improve G_e .

The experiments reported in chapter three related to oxide growth at the interface prior to polysilicon deposition are not thorough enough to be conclusive, however no encouraging results were obtained with any experiment and it seems unlikely that any substantial improvement is possible in our structure with a deliberately introduced oxide layer unless a high temperature anneal is done.

None of our attempts at oxidation (either chemical or thermal) produced devices with improved G_e 's. Figure 4.1 shows a Gummel plot from a typical transistor with a thin thermally grown interfacial oxide layer. These devices in every case appear to have a very high emitter series resistance. While it is possible that our oxide was simply too thick, no further work on oxidation was attempted.

Figure 4.1 Gummel plot for a transistor with thermal oxidation prior to poly deposition. Wafer MR-4, RCA clean followed by 500 deg. C. oxidation.

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Note that the chemical oxidation procedure used here was the same as reported by Ashburn [26].

Theories based on minority carrier mobility reduction in the polysilicon all predict some variation in gain with emitter thickness. Experiments reported in chapter three show that transistors fabricated with 15 nm thick emitters gave G_e 's comparable to the best devices fabricated with 350 nm emitters.

It is important to note that the 15 nm poly emitter is certainly only a single crystallite high (ie. a horizontal packing of vertical columns). What this means is that in the one dimensional view of the device cross-section, the only grain boundary that matters is the one between the single crystal substrate and the polysilicon. The current injection properties of the junction are controlled by this single interface and do not appear to be affected by the bulk properties at all. It would appear that theories related to current flow transverse to grain boundaries are in error.

Ashburn reports an improvement of a factor of three in device gain (with respect to conventional npn devices) using HF dip etched devices. No direct comparison of true

polysilicon emitter transistors with conventional npn's was attempted here, but values of G_e were calculated for the true polysilicon emitter devices and these can be compared to values for conventional npn's. This comparison is a more useful one than Ashburn's since the base properties are not a factor in G_e calculation but they will effect any gain calculation.

Typical values of G_e for the true polysilicon emitter range from mid 10^{14} to low 10^{15} s cm⁻⁴. This compares with a few times 10^{13} s cm⁻⁴ for conventional npn's. It is clear that the emitter Gummel number is increased by much more than the factor of three reported for Ashburn's HF dipped polysilicon emitters.

Previous experimental work with conventional polysilicon emitters has not dealt in detail with polysilicon properties. Models based on minority carrier transport in the polysilicon [7] will, of course, predict a variation in gain with the emitter width. Conventional npn theory shows us that the base current injected into the emitter is given by:

$$J_p(\text{emitter}) = \frac{p n_{e-b} j_n - p n_{\text{emitter contact}}}{\int_0^{W_E} \frac{n(x)}{D_p(x)} dx} \quad (4.1)$$

Ignoring variations in the intrinsic carrier concentration across the base, the difference in the pn product between the metallurgical junction and the emitter contact is proportional to $n_i^2 \coth(W_E/L_p)$. If $W_E \gg L_p$ then the pn product at the emitter contact is n_i^2 as expected. The denominator of the above expression (4.1) accounts for the doping profile and variations in minority carrier mobility in the emitter.

Conventional npn transistors are designed with this limitation in mind. Unfortunately, it is not practical to have $W_E \gg L_p$ since this is incompatible with other device design considerations as well as technologically troublesome. If the emitter is deep then in any controllable process the base must inevitably be wide. Charge storage in the deep emitter may also dominate the switching time of the device [27].

The minority carrier mobility models [7] simply attempt to extend this model to the polysilicon emitter by suggesting that an unusually low value for the function $D_p(x)$ causes the hole current into the emitter to be suppressed.

The true polysilicon emitter transistor exhibits no dependence of G_e on emitter width. This implies the minority carrier diffusion length in the polysilicon must be less than the smallest emitter width (15 nm) for the mobility model to be valid. Recall that:

$$L_p^2 = D_p t_p . \quad (4,2)$$

If we assume the mobility reduction theory is correct then $L_p < 3$ nm (for $W_E \gg l_p$) and the $D_p t_p$ product is $\sim 10^{-15} \text{cm}^2$ which forces very small values for D_p and t_p . Ning and Isaac suggest a value of D_p that is only smaller by a factor of three (with respect to the single crystal values).

Comparison with previous models shows that our device does not fit easily into either the mobility model or the tunnel emitter model. The improvement in G_e is much larger than expected by models such as Ashburn's which rely on a tunnel oxide to explain the gain. The Ning and Isaac model is not necessarily inconsistent with the values observed in chapter three, but it does require that L_p , D_p and t_p assume some extreme values which seem intuitively unlikely.

4.3 Performance Limitations

Some of the experiments in chapter three produced devices with important but solvable problems. The single step base process, for example gives devices with high base series resistance. This problem was later addressed by the use of a two step base process. This improved the current handling capability of later devices. Figure 4.2 and 4.3 show Gummel plots of both types of devices.

The emitter in the early devices had no metallization at all. Not suprisingly, this produced devices with high emitter series and spreading resistance. This problem was later partially addressed by the use of an unsintered, thermally evaporated pure aluminum contact. The use of thermally evaporated aluminum did not solve the problem completely since the aluminum cannot be sintered without affecting the junction [22]. A more sophisticated metallization scheme perhaps making use of a sputtered silicide layer and a barrier layer followed by the interconnect layer (pure aluminum) would be required to produce an optimal, reliable interconnect scheme.

One of the most important observations of device characteristics is the behaviour of the device at high

Figure 4.2 Gummel plot for a two step base device.
Wafer MR-15.

Figure 4.3 Gummel plot for a one step base device.
Wafer GTE-3.

current levels. Examination of a plot of $\log h_{FE}$ versus $\log J_C$ reveals a very rapid falloff in gain when $J_C > 10^3 \text{ A cm}^{-2}$. This falloff in gain occurs at the rate of approximately four decades per decade.

The Kirk effect [25] is one high level effect that may be active here. This effect is due to mobile charge in transit and causes a modulation in the depletion layer width. This has an effect on the position of the neutral base region boundaries and is sometimes called "the base push-out effect".

The base push-out effect starts to occur when the mobile charge is roughly the same order as the base doping at the edge of the collector base depletion layer. If we assume $N_A \sim 5 \times 10^{16} \text{ cm}^{-3}$ at this edge then for $W = 0.20$ microns (neutral base width) the onset of the high level base push-out effect occurs for a current:

$$J_n \sim \frac{n'(\text{emitter boundary}) D_n q}{W_B} \sim 2000 \text{ A cm}^{-2}, \quad (4.3)$$

which is in reasonable agreement with our observations.

Note that this level can be changed if the collector base voltage is changed. Some experimental evidence for this is

shown in Figure 3.7. The mobile charge in transit through the collector can be calculated as:

$$n = \frac{J_n}{qv_{\text{drift}}} \sim 10^{15} \text{ cm}^{-3} \quad (4.4)$$

(assuming $v_{\text{drift}} = 10^7 \text{ cm s}^{-1}$) or roughly the same order as the collector doping.

Another high level effect that may be active here is a reduction of the emitter base junction voltage due to a non-zero "Webster voltage" [26]. The Webster voltage is non-zero when the mobile hole concentration in the base of our npn begins to deviate from the low level equilibrium value. The expression for V_{be} as applied to the base emitter terminals is:

$$V_{be} = V_W + V_{\text{ohmic}} + V_{je} \quad (4.5)$$

where: V_W refers to the Webster voltage and

V_{ohmic} refers to the majority carrier ohmic drop

V_{je} refers to the actual base emitter voltage at the junction.

Recall:

shown in Figure 3.7. The mobile charge in transit through the collector can be calculated as:

$$n = \frac{J_n}{qv_{\text{drift}}} \sim 10^{15} \text{ cm}^{-3}, \quad (4.4)$$

(assuming $v_{\text{drift}} = 10^7 \text{ cm s}^{-1}$) or roughly the same order as the collector doping.

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$$V_{be} = V_W + V_{\text{ohmic}} + V_{je}, \quad (4.5)$$

where: V_W refers to the Webster voltage and

V_{ohmic} refers to the majority carrier ohmic drop

V_{je} refers to the actual base emitter voltage at the junction.

Recall: ~

$$V_W = \frac{kT}{q} \ln \left(\frac{P_{be}}{P_c} \right) - \ln \frac{P_{0,be}}{P_{0,c}} \quad (4.6)$$

where 'c' refers to the base contact and 'be' refers to the base emitter junction.

Our devices have a heavily doped extrinsic base, hence we assume low level conditions at the base contact and find:

$$V_W \sim \frac{kT}{q} \ln \left(\frac{P_{be}}{P_{0,be}} \right) \quad (4.7)$$

Evaluating the term $(P_{be})/(P_{0,be})$ gives:

$$\frac{P_{be}}{P_{0,be}} = \frac{1}{P_{0,be}} (P_{0,be} + P_{be}') = \frac{P_{0,be} + n_{be}'}{P_{0,be}} \quad (4.8)$$

where n_{be}' is due to the emitter disturbance and:

$$P_{be}' = n_{be}' \quad (4.9)$$

due to charge neutrality considering the base is operating under high level injection conditions.

The disturbance can be written as:

$$n_{be}' = \frac{n_{0,be}(p_{be} - p_{0,be})}{p_{0,be}} \quad (4.10)$$

The electron current injected into the base is (remembering that the emitter is still in low level):

$$n_{be}' = \frac{n_i^2 (e^{qV_j/kT} - 1)}{p_{0,be}} \quad (4.11)$$

where V_j is the actual voltage across the base-emitter junction, not the voltage across the terminals. Here, we consider the junction voltage to be the difference between the terminal voltage and the "Webster voltage."

From (4.10) and (4.11) we can write a quadratic equation in $(p_{be})/(p_{0,be})$. If we consider the case of high level injection we find:

$$p_{be} = n_{be}' = n_i e^{(qV/2kT)} \quad (4.12)$$

where V is the voltage across the base-emitter terminals.

Thus, we see that the effect of the "Webster voltage"

is to force the injected carrier density to follow a $e^{qV/2kT}$ law instead of the usual $e^{qV/kT}$ law. One-half of the applied voltage appears as the "Webster voltage" and the other half appears as a junction voltage (neglecting for the moment any ohmic losses).

An examination of the doping profile shows that this effect might be expected to occur for roughly the same J_c (2000 A cm^{-2}) that leads to the Kirk effect.

The rapid falloff in gain appears to be due to base push-out. The modulation of the current gain "falloff" point by collector-base voltage indicates that this is not related to any unusual property of the emitter-base junction, but related solely to the collector-base junction.

Experiments to date have produced devices in which current handling capability is limited by factors other than the base-emitter junction. A more elaborate experiment would be required to examine properties of the junction.

4.6 Summary

A baseline process flow has been established which

produces transistors with emitter Gummel numbers comparable to "conventional" polysilicon emitters and superior to conventional ion-implanted emitters. The performance of the devices at high current levels has been shown to be limited by high level injection effects in the base or base-collector depletion region.

The range of high transconductance is fairly limited owing to large series resistance contributions from the collector and from the emitter as well. The primitive metallization scheme used to contact the emitter may make an important contribution to this series resistance.

Attempts to fabricate devices with an intentional interfacial oxide layer present prior to polysilicon deposition produced devices with extremely low gains and very high series resistance.

Experiments have shown no variation of G_e with emitter width. This strongly suggests that models based on reduced minority carrier mobility in the poly emitter are inapplicable to our device. The true polysilicon emitter transistor is different than previously reported polysilicon emitter transistors.

CHAPTER 5.

SUMMARY AND CONCLUSIONS5.1 A Review of Work Reported in This Thesis

A series of experiments has been conducted to investigate what might be referred to as a "true polysilicon emitter transistor" where, for the first time, the emitter-base junction corresponds to the polysilicon-substrate interface [28,29,30].

Initial experiments were aimed at establishing a baseline process. This allowed subsequent experiments to proceed from a well established set of repeatable process steps thus ensuring a high degree of confidence in experimental results.

A summary of the experimental work done is presented in Table 5.1. Table 5.2 presents a summary of G_e values observed.

The true polysilicon emitter transistor gives a very

Run no.	Poly Dep.	Wafers	Base formation	Oxidation
1	A	GTE-1,2,3, 7,8,9	5 min. predep at 800 C 1100 C drive-in	none
2	B	GTE- 4,6,12, 19	Implanted at UBC	none
	G	GTE-5,11,20	Implanted at UBC	none
	F	GTE-13	Implanted at UBC	none
3	B	GTE-15,16	5 min. predep at 780 1050 C drive-in	none
	C	GTE-17,18	5 min. predep at 780 1050 C drive-in	500 C thermal
4	D	MR-1,3,4, 13,14	5 min. predep at 780 1050 C drive-in	500 C thermal for MR 4,14
	E	MR-8,9,10	5 min. predep at 780 1050 C drive-in	MR-8 HCl/H ₂ O ₂ MR-9 RCA
	F	MR-18	5 min. predep at 780 1050 C drive-in	none
	G	MR-7	5 min. predep at 780 1050 C drive-in	none
	H	MR-2,5	5 min. predep at 780 1050 C drive-in	none
	I	MR-6,16	5 min. predep at 780 1050 C drive-in	none

Table 5.1 Summary of the Experimental Work

Wafer	Base Doping	Oxide	Gain	Ge	Comments	Run #
GTE-1	diffused	- -				1A
GTE-2	diffused	- -	$>10^3$		no emitter metal	1A
GTE-3	diffused	- -	$\sim 10^3$		has emitter metal poor C-B leakage	1A
GTE-4	10^{12} cm^{-2} 950 C. anneal	- -	$>10^4$	5E14		2B
GTE-5	$5 \times 10^{12} \text{ cm}^{-2}$ 950 C. anneal	- -			poly severely over- etched, not useable	2G
GTE-6	diffused	- -	~ 100	5E13		3B
GTE-7	diffused	- -	no data			1A
GTE-8	diffused	- -	no data			1A
GTE-9	diffused	- -	no data			1A
GTE-10	MIS emitter	- -				
GTE-11	10^{12} cm^{-2} 950 C. anneal	- -			broken	2G
GTE-12	10^{13} cm^{-2} 1000 C. anneal	- -	~ 100	1E14	generally low gain	2B
GTE-13	10^{12} cm^{-2} 1000 C. anneal	- -	~ 100	4E14		2F
GTE-14					lost at UBC	
GTE-15	diffused	- -	$>10^3$	3E13	high Early voltage high punchthrough	2B
GTE-16	diffused, 5min. 780	- -	>100			3B

Table 5.2 A Summary of the Ge Values Observed

Wafer	Base Doping	Oxide	Gain	Ge	Comments	Run #
GTE-17	diffused, 780 C. predep		<10		Very high series resistance	3C
GTE-18	diffused, 780 C. predep	500 C 30 min	<10		Very high series resistance	3C
GTE-19	10^{12} cm^{-2} 1000 C. anneal	- -	$>10^3$	3E13		2B
GTE-20	$3 \times 10^{12} \text{ cm}^{-2}$	- -			thin poly	2G
MR-1	all MR series wafers received diffused base, 5 min. 780 C. predep.	- -	$\sim 10^3$	2E14	high Early voltage	4D
MR-2		- -		2E14	thin poly, 10 min. deposition time	4H
MR-3		- -			similar to MR-1	4D
MR-4		500 C. 30 min.	<10		very high series resistance	4D
MR-5		- -			thin poly, 10 min. deposition time.	4H
MR-6		- -		7E13	very thin poly, 3 min. dep time.	4I
MR-7			2000	9E13		4G
MR-8		HCl + H ₂ O ₂			run aborted; thin poly.	4E

Wafer	Base Doping	Oxide	Gain	Ge	Comments	Run #
MR-9		full RCA			run aborted, thin poly	4E
MR-10						4E
MR-11					to UBC	
MR-12					to UBC	
MR-13						4D
MR-14		500 C. 30 min.	<100	low	high resistance	4D
MR-15			~100	1E13		
MR-16			1000	3E14	very thin poly, 3 min. dep time. Evidence for high Ge with thin poly emitter. Excellent Early voltage.	4I
MR-17						
MR-18						4F
MR-19						
MR-20						

high emitter Gummel number despite the lack of any intentionally grown oxide. However, it should be noted that recent results from Stanford University [16] suggests that a thin oxide layer may be present even for devices given an HF dip etch immediately prior to polysilicon deposition.

The experiments with varying poly thickness show no variation of G_e with W_E . This clearly shows the high G_e to be due to an interface effect rather than due to bulk properties of the polysilicon (such as a low minority carrier diffusion coefficient or simply increased W_E).

Deliberate oxidation of the interface prior to poly deposition by both chemical and thermal means produced transistors with low gains and very high series resistance. This contrasts sharply with results reported by other researchers for devices subjected to a high temperature anneal after polysilicon deposition.

The true polysilicon emitter device is attractive for those applications requiring high current gain. Conventional superbeta bipolar IC processes require a low dose base implant just slightly deeper than the emitter implant. Problems with process control inevitably lead to

low yields in this type of process. Yields for the true polysilicon emitter are expected to be much higher than a conventional bipolar transistor process since the main yield limiting step (the emitter drive which produces emitter collector piping) has been eliminated.

Of critical importance to controllability of device manufacture is control of the interface quality. Recent advances in semiconductor equipment technology such as vertical furnaces with low pressure capability and anhydrous HF vapour phase etchers will certainly help to keep the interface uniformly clean prior to deposition.

5.2. Future Work

There remain several important questions regarding the mechanism responsible for enhanced current gain in the devices fabricated to date. The cleaning procedure prior to polysilicon deposition is not ideal. After etching back the emitter window areas and prior to poly deposition, the wafers are quenched in DI water where some oxide is grown. The wafers are dried in dry nitrogen and loaded into the boat. When the boat is loaded into the tube (at 627°C.) some back-streaming of the room air into the furnace occurs. Naturally, steps are taken to minimize back-

streaming (such as increasing the nitrogen purge flow rate) but some amount of backstreaming is unavoidable in all "elephant" type or "cantilever" type loading systems. Oxide can grow on the wafers during the time from when the boat is loaded until the tube is sealed and pumped down to a vacuum. The oxide grown will probably not be uniform nor reproducible. This problem is a serious concern for all devices since it may ultimately determine the uniformity of transistor gain across a wafer and across a batch.

The recent appearance of vertical furnaces offers some considerable potential for minimizing this "backstreaming" problem and possibly improving uniformity of device gain across a wafer. In a vertical furnace system, the wafers are loaded onto a platform inside a bell jar and then the bell jar is pumped down to a vacuum. Only then are the heater elements lowered around the bell jar and the boat is ramped from room temperature to the process temperature (either in a vacuum or with a nitrogen or argon purge). These systems offer considerable potential for controllability and reproducibility of interface properties prior to polysilicon deposition that is not possible in conventional horizontal furnaces.

Molecular beam epitaxy machines also offer a solution

to the problem of backstreaming in much the same way as the vertical furnace (evacuation of the process chamber prior to substrate heating) and offer the additional advantage of an in-situ sputter preclean to ensure a good quality uniform interface.

To form a more complete understanding of polysilicon emitter transistors, a complete study of emitter Gummel number versus anneal time and anneal temperature for dip-etched and intentionally oxidized interface should be performed.

5.3 Concluding Remarks

A complete explanation of the improvement in G_e cannot be offered based on the experimental results obtained here. There are at least three explanations that are consistent with the results reported here. Briefly, the plausible explanations for improved G_e are:

- a) there is a non-zero quantum reflection-coefficient for holes attempting to enter the emitter from the base. This causes the back-injected hole current to be suppressed.
- b) a thin disordered layer of < 20 nm. greatly reduces hole mobility in the emitter without providing

recombination sites.

c) a thin oxide layer, perhaps no more than a monolayer thick acts to block hole injection into the emitter, thereby suppressing the base current.

The quantum reflection at the poly-mono interface is based on the fact that charge carriers will certainly see some disorder as they approach the interface (the substrate is $\langle 100 \rangle$ and the poly is possibly $\langle 111 \rangle$, $\langle 311 \rangle$ or $\langle 511 \rangle$ [21]). The exact nature of the poly-mono interface is not well understood and a calculation of the reflection coefficient at the interface is not possible without much more detailed knowledge of the interface. It should be possible to construct a theoretical model that with appropriate fitting coefficients could model the interface.

The Neugroschel model of the poly-mono interface suggests a disordered region of $\sim 15\text{-}20$ nm where it is proposed the minority carrier mobility is greatly reduced without providing any recombination sites. Recent high resolution cross-sectional TEM photographs [15] have not shown such a region to exist on samples that did demonstrate high G_e 's. If such a layer is present as Neugroschel suggests it does not seem to be necessary for improved G_e 's.

Recent work related to annealing/regrowth of the poly-mono interface suggests that a thin layer of SiO_x is present even on samples given an HF etch prior to depositions [16]. The conclusion is based on the epitaxial regrowth behaviour that is exhibited with these samples after sufficiently long or high temperature anneals. The conclusions are that any anneal sufficient to cause appreciable epitaxial regrowth to occur reduces the base current suppression of the poly-mono interface.

The true polysilicon emitter is different than previously reported "conventional" polysilicon emitters. Unlike all previously reported polysilicon emitters, no high temperature anneal step is necessary to produce high emitter Gummel numbers. We observed no significant variation of G_e with polysilicon thickness, unlike Ning and Isaac [7]. No improvement of G_e was observed when a thin thermal or chemical oxidation was performed just prior to polysilicon deposition (unlike results by Soerwirdjo et al [9] and de Graaf and de Groot [5]). For our devices, introduction of any deliberate oxide severely degraded device performance.

The true polysilicon emitter transistor offers some

technological advantages compared with a conventional polysilicon emitter. The true polysilicon emitter completely solves the problem of emitter - collector diffusion "pipes" since the emitter is formed at a temperature too low for any appreciable diffusion to occur. The thermal budget associated with forming the true polysilicon emitter is negligible after base formation. This is an important advantage in VLSI compatible device designs.

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APPENDIX ARunsheets for the Abbreviated Process Sequence

Starting Material: n type <100>

1-2 ohm-cm. GTE-1 thru GTE-6

3-5 ohm-cm. GTE-7 thru GTE-20

1. MASK OXIDE GROWTH FOR BASE DIFFUSION

RCA clean

Oxidation: 1100°C

- 5 min. preheat
- 2 min. push
- 5 min. dry O₂
- 10 min. wet O₂
- 5 min. dry O₂ + 2% HCl
- 5 min. dry O₂
- 20 min. N₂ anneal
- 2 min. pull
- 10 min. cool

2. OPEN WINDOWS FOR BASE DIFFUSION

Mask CU-063-02 negative photoresist

3. BASE BORON DIFFUSION

RCA clean

Predep: 800°C   5 min. preheat
                     2 min. push
                     5 min. dry O₂ + N₂
                     2 min. dopant
                     10 min. dry O₂ + N₂
                     2 min. pull
                     10 min. cool

Boron deglaze: 20 sec. in 10:1 DI:HF

Drive-in: 1100°C   5 min. preheat
                     2 min. push
                     2 min. dry O₂
                     30 min. wet O₂
                     5 min. dry O₂
                     5 min. dry O₂ + 2% HCl
                     5 min. dry O₂
                     20 min. N₂ anneal
                     2 min. pull
                     10 min. cool

4. STRIP OXIDE FROM WAFER BACK

5. PHOSPHORUS DIFFUSION INTO BACK

(Getter and back contact formation)

RCA clean

Predep: 1000°C   5 min. preheat
                  2 min. push
                  5 min. dry O₂ + N₂
                  10 min. dopant
                  5 min. dry O₂ + N₂ purge
                  2 min. pull
                  10 min. cool

Phosphorus deglaze: 10 seconds in 10:1 DI:HF

Drive-in: 1000°C   5 min. preheat
                  2 min. push
                  20 min. N₂
                  2 min. pull
                  10 min. cool

6. OPEN EMITTER WINDOWS

Mask CU-063-03 negative photoresist

7. DEPOSIT AND PATTERN EMITTER POLYSILICON

Dip wafers in 10:1 DI:HF immediately prior to deposition

Deposition: LPCVD 625°C SiH_4 25% PH_3 15%

Mask: CU-063-05 negative photoresist

Plasma etch

8. OPEN BASE CONTACT WINDOWS

Mask CU-063-05 negative photoresist

9. DEPOSIT AND PATTERN BASE CONTACT METAL

Deposition: 0.5 microns Aluminum by e-beam evaporation

Deposit metal on both sides

Mask CU-063-06 positive photoresist

10. BASE CONTACT ANNEAL

450°C H_2 20 min.

APPENDIX BRunsheets for the Baseline Process Sequence

Starting Material: n type <100>

1-2 ohm-cm. GTE-4, GTE-5

3-5 ohm-cm. GTE-10 thru GTE-14, GTE-19, GTE-20

All wafers have 250 nm. of thermal oxide on them

1. OPEN WINDOWS FOR EXTRINSIC BASE DIFFUSION

Mask CU-063-01 negative photoresist, protect backs

2. EXTRINSIC BASE BORON DIFFUSION

RCA clean

Predep: 1000°C   5 min. preheat
                     5 min. push
                     5 min. dry O₂ + N₂
                     10 min. dopant
                     10 min. dry O₂ + N₂
                     5 min. pull
                     10 min. cool

Boron deglaze: 30 sec. in 10:1 DI:HF

Drive-in: 1100°C

5 min. preheat
5 min. push
10 min. dry O₂
15 min. wet O₂
5 min. dry O₂ + 2% HCl
5 min. dry O₂
5 min. pull
10 min. cool

3. PHOSPHORUS BACKSIDE GETTER

Strip oxide from wafer backs

RCA clean

Predep: 1000°C

5 min. preheat
5 min. push
5 min. dry O₂ + N₂
10 min. dopant
5 min. dry O₂ + N₂ purge
5 min. pull
10 min. cool

Phosphorus deglaze: 10 seconds in 10:1 DI:HF

Drive-in: 950°C   5 min. preheat
5 min. push
20 min. wet O₂
5 min. dry O₂
5 min. pull
10 min. cool

4. OPEN WINDOWS FOR INTRINSIC BASE IMPLANT

Mask CU-063-02 negative photoresist, protect backs

5. IMPLANT MASK OXIDE GROWTH

RCA clean

Oxidation: 1000°C   5 min. preheat
5 min. push
30 min. dry O₂ + 2.5% HCl
5 min. dry O₂
10 min. N₂
5 min. pull
10 min. cool

6. INTRINSIC BASE BORON IMPLANT

Implant dose: 10^{12} cm⁻²

Implant energy: 50 keV

7. INTRINSIC BASE ANNEAL

Drive-in: 950°C   5 min. preheat
                         5 min. push
                         30 min. anneal in N₂
                         5 min. pull
                         10 min. cool

8. OPEN EMITTER WINDOWS

Mask CU-063-03 negative photoresist

9. DEPOSIT AND PATTERN EMITTER POLYSILICON

Dip wafers in 10:1 DI:HF immediately prior to
deposition

Deposition: LPCVD 625°C SiH₄ 25% PH₃ 15%

Mask: CU-063-05 negative photoresist

Plasma etch

10. OPEN BASE CONTACT WINDOWS

Mask CU-063-05 negative photoresist

11. DEPOSIT AND PATTERN BASE CONTACT METAL

Deposition: 0.5 microns Aluminum by e-beam evaporation

Deposit metal on both sides

Mask CU-063-06 positive photoresist

12. BASE CONTACT ANNEAL

450°C H₂ 20 min.

13. DEPOSIT AND PATTERN EMITTER CONTACT METAL

Deposition: 0.5 microns Aluminum by e-beam evaporation

Deposit metal on backs as well.

Mask CU-063-07 positive photoresist

Etch metal in hot H₃PO₄

APPENDIX CRunsheets for Intentional Oxidation prior to Poly Deposition

Follow the same runsheet as appendix B with the exception of step 9, the polysilicon deposition step. For an intentional oxide growth, step 8 should read as follows.

9. DEPOSIT AND PATTERN EMITTER POLYSILICON

RCA clean

Dip wafers in 10:1 DI:HF immediately prior to loading into the furnace.

Oxidation:	500°C	2 min. preheat
		2 min. push
		20 min. dry O ₂
		5 min. N ₂
		2 min. pull
		5 min. cool

Polysilicon deposition: LPCVD 625°C SiH₄ 25%
PH₃ 15%

Mask: CU-063-05 negative photoresist

Plasma etch

APPENDIX D

Page 127 to 129
The text of a paper entitled
"A True Polysilicon Emitter
Transistor" Published in
Electron Device Letters,
vol. EDL, no. 6, pp.
288-290, 1985.

A TRUE POLYSILICON EMITTER
TRANSISTOR

Manuscript received
January 22, 1985; revised
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are with the department of
Electronics. Carleton University
Ottawa, Ontario. Canada K1S 5B6

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APPENDIX D

Page 127 à 129
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APPENDIX E

The extended abstract of a presentation made to
the 43rd annual Device Research Conference, 1985.

SUPER-GAIN POLYSILICON EMITTER TRANSISTORS

by

M.B. Rowlandson and N.G. Tarr

Department of Electronics, Carleton University
Ottawa, Ontario, Canada K1S 5R6

Polysilicon emitter transistors have been fabricated in which the emitter-base metallurgical junction coincides with the polysilicon-substrate interface. This structure was realized by depositing in-situ phosphorus-doped polysilicon in an LPCVD reactor at a temperature low enough to prevent dopant diffusion into the substrate. In contrast, in all previously reported polysilicon emitter transistors, the polysilicon has served only as a contact to a monocrystalline emitter region formed either by diffusion from the polysilicon, or by conventional ion implantation techniques.

By depositing the polysilicon emitter at very low temperatures, and avoiding subsequent high-temperature annealing steps, it is possible to use very light base implant doses without concern for "emitter pipe" effects. In consequence, extremely high gains are possible. Common emitter current gains of several thousand have been routinely obtained using both diffused and implanted bases. On one wafer with a base implant dose of 10^{12}cm^{-2} , h_{FE} values in excess of 20,000 were obtained, which are comparable to the highest gains ever reported for silicon bipolar transistors [1]. The corresponding emitter Gummel number is in excess of 10^{14}acm^{-4} . The Early voltage for these devices was approximately 3.5V, with base punch-through setting in at $V_{CB} = 15\text{V}$. The gain peaked at collector current densities of roughly 10^3Acn^{-2} and appeared to be limited by base push-out effects at higher current densities.

In an attempt to determine the mechanism responsible for the very high gains reported above, additional fabrication runs were undertaken in which the thickness of the polysilicon emitter was progressively reduced to values as low as 10nm. No variation of h_{FE} with polysilicon thickness was found. This result strongly suggests that the high gain results from suppression of the hole back-injection current by quantum reflection effects [2], rather than from a low minority carrier mobility in the polysilicon [3]. If this explanation is correct, then the devices described here are in fact quite similar to the MIS tunnel junction emitter transistors reported in [1]. Quantum reflection of holes at the polysilicon-substrate interface could occur even in the absence of an interfacial oxide layer, but would no doubt be greatly enhanced by the growth of such a layer during the brief interval between the final cleaning of the substrates in dilute hydrofluoric acid and their insertion into the LPCVD reactor.

In summary, the deposition of in-situ doped polysilicon at low temperatures using an LPCVD reactor has been shown to provide a means for fabricating bipolar transistors with very high gains, and potentially high process yields.

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APPENDIX F

The text of a paper presented at the Canadian
Conference on VLSI, 1985.

SUPER-GAIN POLYSILICON EMITTER TRANSISTORS FABRICATED IN A LOW-TEMPERATURE PROCESS

M.B. Rowlandson, E.P. Keyes and N.G. Tarr
Department of Electronics, Carleton University
Ottawa, Ontario K1S 5B6

ABSTRACT

It is shown that polysilicon contacts deposited at a temperature of 627°C and subjected to no additional high-temperature processing can function as very efficient minority carrier injectors, giving emitter Gummel numbers in excess of 10^{14} cm^{-4} . Polysilicon emitters formed in this way have been combined with lightly-doped ion-implanted base regions to produce transistors with common emitter current gains in excess of 10,000.

1. INTRODUCTION

In modern silicon bipolar transistors, the base is usually so narrow that minority carriers can traverse it with little chance of recombining. The gain of such a transistor is therefore controlled by two factors: the integrated base doping and the injection efficiency of the emitter. The former quantity is commonly described by the base Gummel number G_B , defined as

$$G_B = \int_{\text{base}} (N_A(x)/D_n) dx \quad (1)$$

When recombination in the base is negligible, the collector current density can be expressed in terms of G_B as

$$J_C = (qn_1^2/G_B) \exp(qV_{BE}/kT) \quad (2)$$

The emitter injection efficiency can also be conveniently described by an emitter Gummel number G_E . If the base current is dominated by back injection into the emitter, then G_E is related to J_B by

$$J_B = (qn_1^2/G_E) \exp(qV_{BE}/kT) \quad (3)$$

From (2) and (3), it is clear that the common emitter current gain h_{FE} is given by

$$h_{FE} = G_E/G_B \quad (4)$$

(4) reveals that a high gain can be obtained by simply lowering the base doping to reduce G_B . However, fabrication technology places a lower bound on G_B . In a conventional npn transistor with a phosphorus-doped emitter diffused into a boron-doped base, the "emitter push" effect limits the minimum attainable base width and G_B value. Narrower bases and smaller, better-controlled base Gummel numbers can be obtained using ion implanted processes with arsenic as the emitter dopant, but even in this case the formation of emitter-collector pipes reduces yield if G_B is made too small. In view of the problems associated with reducing G_B , attention has turned to schemes for raising G_E in order to improve gain.

Over the past decade, a number of groups have shown that the injection

efficiency can be significantly improved if the emitter is contacted with heavily-doped polysilicon rather than a conventional metal ohmic contact [1]. Devices of this kind have come to be known as "polysilicon emitter" transistors. The use of polysilicon contacts has been found to raise G_E by roughly an order of magnitude. This increase in G_E can be exploited either to increase h_{FE} if G_B is kept fixed, or to maintain a fixed h_{FE} while raising G_B . (Increasing G_B results in a reduction in the parasitic base spreading resistance, which helps improve high-frequency performance.).

In the majority of polysilicon emitter transistors reported to date, the polysilicon has itself been used as a source for the emitter diffusion. Even in those cases in which the emitter has been formed by ion implantation, devices have been annealed after polysilicon deposition at temperatures high enough to cause dopant diffusion into the substrate. This paper describes a somewhat different class of polysilicon emitter structure, in which the emitter is deposited by low pressure chemical vapor deposition (LPCVD) techniques at a temperature too low for appreciable diffusion to occur. This structure might well be referred to as a "true" polysilicon emitter, since the metallurgical base/emitter junction coincides with the polysilicon/silicon interface. With a true polysilicon emitter, the base doping profile can be established without concern for anomalous diffusion effects. It is therefore possible to tailor the base width and G_B to almost any desired values, limited only by the minimum allowable collector-base punchthrough voltage and the maximum allowable base sheet resistance.

II. EXPERIMENT

The basic transistor structure examined here is shown in Fig. 1. The lightly-doped intrinsic base was formed by the implantation of $11B^+$ at 50keV through a 50nm oxide. Implant doses ranging from 10^{12} to $10^{13}cm^{-2}$ were used with an implant anneal at 950°C, giving a base width of approximately 0.4 μm and an extrinsic base sheet resistance of several kilohms per square. The wafers were briefly dipped in 10% hydrofluoric acid immediately prior to polysilicon deposition to minimize the thickness of any native oxide layer which might be present at the polysilicon/silicon interface. The polysilicon emitter was deposited from a 300:1 silane/phosphine mixture at 627°C.

The J_C and J_B characteristics for a representative transistor are shown in Fig. 2, while the common emitter characteristics for the same device are presented in Fig. 3. From Fig. 3 it can be seen that h_{FE} for this device is approximately 2,500 at moderate current densities, and that the device can operate at a collector-emitter bias of 20V. The high gain is due in part to the light base doping, but also results in large measure from the high injection efficiency of the polysilicon emitter. Taking values for h_{FE} and I_C at $V_{BE} = 600mV$, and assuming $n_i = 1.45 \times 10^{10}cm^{-3}$ at room temperature, it is found from (2) and (4) that $G_E \approx 10^{14}scm^{-4}$ for this device. If anything, this is an underestimate of G_E , since J_B undoubtedly contains contributions from recombination in the base-emitter depletion region and in the neutral base which are not accounted for in (3). By way of comparison, the emitter Gummel number for a transistor formed by conventional techniques is typically close to $10^{13}scm^{-4}$, while the best polysilicon emitters reported to date have G_E values of approximately $5 \times 10^{14}scm^{-4}$. For devices with lighter base implant doses, we have obtained current gains of up to 20,000, at the expense of reducing the Early voltage to only a few volts.

III. DISCUSSION

The mechanism responsible for the high minority carrier injection ratio associated with the polysilicon emitter contact is still the subject of debate. Some authors have suggested that a reduced diffusion coefficient for minority carrier holes traversing the polysilicon is the critical factor in providing high G_E values [2], while others have postulated that the holes undergo quantum reflection at the polysilicon/silicon interface [1,3]. Quantum reflection of holes is certain to occur if an ultra-thin oxide layer separates the polysilicon from the substrate, but might also take place even in the absence of an oxide layer if the hole wavefunction is scattered by the disordered region present at the grain boundary which forms the interface. To obtain some indication of which model most accurately describes the devices reported here, transistors were fabricated with polysilicon thicknesses ranging down to 10nm. Even with emitters this thin, G_E values in excess of 10^{14} cm^{-2} were recorded for some devices. This strongly suggests that reflection of holes at the polysilicon/silicon interface, rather than hole transport in the polysilicon, is responsible for controlling G_E .

Despite the high gains and G_E values reported above, considerable work remains to be done in optimizing the true polysilicon emitter structure. In particular, in their present form the transistors have a rather high effective emitter series resistance. This resistance must be reduced by approximately an order of magnitude to make the current handling capability comparable to that of conventional commercial BJTs. It is as yet not clear whether the resistance is an inherent feature of the polysilicon/silicon interface, or whether it is a parasitic effect which can be eliminated.

The polysilicon emitter structure reported here appears very attractive from the viewpoint of merging bipolar transistors into an n-well CMOS process. Using the n-well as a collector, it should be possible to form the lightly doped implanted intrinsic base and the polysilicon emitter with minimal disruption of other processing steps.

IV. CONCLUSION

It has been shown that in-situ phosphorus doped LPCVD polysilicon layers deposited at low temperature can function as very efficient minority carrier injectors. Polysilicon contacts of this kind have been combined with lightly doped ion-implanted bases to produce super-beta transistors in a process that should be immune to emitter-collector pipes.

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Fig. 1 Structure of the true polysilicon emitter transistor.

Fig. 2 J_C and J_B characteristics for a transistor with a base implant dose of $2 \times 10^{12} \text{ cm}^{-2}$. The area of the base-emitter junction is $1.75 \times 10^{-5} \text{ cm}^2$. $V_{CB} = 1.0 \text{ V}$.

Fig. 3 Common-emitter characteristics for the device of Fig. 2. The base current step is 100 nA.

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FIN