Efficient Inductor layout geometries for Radio Frequency Integrated Circuits

by

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A thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfillment of the requirements
for the degree of

Master of Applied Science

in

Electrical Engineering

Ottawa-Carleton Institute for Electrical and Computer Engineering

Department of Electronics

Faculty of Engineering

Carleton University

Ottawa, Canada

September, 2008

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ISBN: 978-0-494-44045-2

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ISBN: 978-0-494-44045-2

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Abstract

Demand for low cost compact circuits is ever increasing for consumer products as well as medical and sensor applications. Consequently this has lead to the use of silicon processes with high integration of components. Inductors implemented on silicon substrates have higher losses due to the more conductive silicon substrate, relative to GaAs which has a resistivity that is orders of magnitude higher. A further understanding of the losses directly affected by this can lead to reducing the design restrictions surrounding the layout of inductors and allow much more compact circuits.

Compact models are examined for the inductor and their accuracy studied. For narrow bandwidth circuit designs even the simple traditional models appear accurate enough to use during circuit design, saving time during circuit modelling.

In this thesis the loss mechanisms of inductors on silicon substrates are examined with the goal of recovering some of the area lost to the interior of the planar inductors. If components and even entire circuits can be placed inside the inductor there exists the possibility of large area, and thus cost savings for RF circuits. Once the loss mechanisms are understood the effects of placing material inside the inductor are studied using two electromagnetic simulators, HFSS and Sonnet. A worst case scenario is examined where a highly conductive sheet is placed inside the inductor and performance is seen to drop in proportion to the area of the sheet. According to simulation if the conductive sheet is broken up into smaller pieces representing the same area the lost performance can start to be recovered and in one case according to Sonnet there is virtually no difference between the inductor alone and with material representing a $100\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$ capacitor placed inside while HFSS predicts only a 3% performance drop.

A Voltage Controlled Oscillator is presented as a test circuit to verify the simulations done using the phase noise as a figure of merit. With the VCO circuitry placed inside the inductor the area can be reduced by approximately 20%. With further optimizations this could possibly be reduced even more. Other test circuits designed include the use of a digital divider circuit implemented inside the inductor as well inductors that use a patterned ground shield to improve performance. A simple resonator circuit is used to verify the effects of adding the Metal-Insulator-Metal (MIM) capacitors inside the inductor in various configurations and sizes.

Acknowledgements

I would like to thank Dr. Rony Amaya for his time and effort to help me with any and all aspects of my research, from helping with Matlab code to setting up the EM simulations in HFSS and Sonnet to planning and reviewing this thesis and doing so on top of his busy work and personal life. Professor Tom Smy provided much appreciated administrative assistance with obtaining required software licences for Sonnet that was previously unavailable to the department as well as providing the funding for the fabrication of the test chip.

Professor Calvin Plett helped with the VCO design that is the circuit used to verify the ideas proposed here and was always available to answer a quick question or three. Victor Karam let me use one of his previous digital circuits to use in my testing and this saved me a great deal of time.

Finally I'd like to thank Professor David Walkey, who originally accepted me as a graduate student and whose enthusiasm and energy was inspirational and contagious. His loss was and will be felt by his friends and colleagues for a very long time. I am lucky to have had the chance to study and work with him.

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1. Introduction

The demand for smaller and cheaper devices has driven the development and production of more advanced and integrated processes. One of the most prevalent technologies is based on the use of a silicon substrate as a semiconductor, unfortunately the required use of important passive components in radio frequency (RF) circuits such as the inductor lead to losses that affect the quality factor of the circuits. A good deal of modeling has been done in an effort to understand the interactions between the passive components and the surrounding structures but circuit designers still use the models as a “black box” when designing circuitry.

A study of the loss mechanisms of an inductor and silicon may allow more compact circuits to be made. Silicon technologies are preferred as they support System-On-Chip (SOC) solutions, resulting in an overall reduction in power, layout area and cost of fabrication. The principle difference between a silicon substrate and a Gallium Arsenide (GaAs) process previously used for high performance RFICs is the lower resistivity of the silicon substrate which increases the losses due to eddy currents as well as poor isolation from thin silicon dioxide (SiO_2) dielectric layers. This thesis will start by looking at compact models that attempt to model the various loss mechanisms and comparing these circuits to the models used in a commercial computer aided design (CAD) circuit design software. A closer look at each loss mechanism will be provided using electromagnetic simulators.

A large number of compact models have been developed in increasing complexity and methods for parameter extraction to obtain model values for the structures in question have been studied. Once the essential losses were understood different methods of design and fabrication have been investigated to reduce the parasitic elements involved. Design methods include the use of patterned ground shields to prevent the creation of eddy currents in the substrate by patterning the metal in such a way as to increase the resistance of the induced substrate current (Yue, 1998). The effects of these ground shields have been studied and can be added to the compact physical models (Yim, 2002). Typically these shields are done in lower metal layers and since this increases the parasitic capacitance with the spiral another method of shielding using polysilicon (Chen, 2004) or reverse biased pn junctions instead of a lower metal layer to form the shield (Steinmair, 2005).

Specialized fabrication techniques are now being used to minimize the losses of the inductors by modifying the physical surroundings on the wafer. One study found that the magnetic field is maximum at the centre of the inductor and since the field strength is inversely proportional to the distance an addition of a dielectric layer is added under the inner turns of the inductor to increase the distance from the substrate and reduce the magnetic field that induces eddy currents (Tang, 2006). Other efforts to reduce the substrate effects include using micromachining techniques to etch cavities in the silicon below the inductor spiral (Lin, 2005). Lastly, the use of different materials has been investigated in order to improve the performance of integrated inductors, such as porous silicon to greatly increase the substrate resistance (Li, 2005). Even the use of the very new carbon nano-tubes bundles has been examined to be used as the conductor of on-chip inductors due to their reduced resistivity (Nieuwoudt, 2008). These exotic solutions that require additional specialized processing steps and materials increase the cost of production.

1.1 Motivation

Once the technology that will be used to fabricate a device is chosen, the principle factor that will determine the cost of the chip is the area required to realise the design. The cost is directly related to the area required to fabricate it and since inductors, if needed, require a large amount of area, a better understanding of losses may lead to more compact circuits. For example if 4 inductors that measure 300 microns per side are used on a chip that is 1 square millimetre, over a third of the chip area is required only for the inductors. Results from the literature show multi-level metal stack to achieve high inductor values in small area but at the cost of reduced quality factor (Tai & Liao, 2007). In an effort to retain high Q planar inductors while reducing the layout area lost to the designer, this thesis will look at the effects of putting circuitry on the interior of a hollow planar inductor. Simulations will be done using Sonnet (Sonnet), a "2.5D" electromagnetic (EM) simulator as well as HFSS (Ansoft) a full 3D EM simulator. In many RFIC designs decoupling capacitors are used to reduce noise in the circuit, generally these can be fairly large and so to reduce the space required the effects of putting the capacitors in the interior of the inductors will be studied. A test chip will be designed and manufactured to study the effects of using the dead space of the inductor for decoupling capacitors of varying size as well as the presence of digital circuitry. An RF design will also be tested by using a Voltage Controlled Oscillator (VCO) with the circuitry placed in a normal fashion outside of the inductor as well as the design of a self

contained VCO where all circuitry is placed on the interior of the inductor, thus the only area required will be that of the inductor. If the performance of the VCO does not suffer in this arrangement this could allow for smaller and cheaper chips to be made. An example shown below demonstrates the area required for inductors and the amount of space that could potentially be recovered (Plett).

Figure 1 - Example space needed for inductors

1.2 Thesis Organization

This thesis will begin by examining the development and limitations of compact models used to simulate physical device performance, principally the inductor, and the loss mechanisms present in general that affect the quality factor as well as ones that are specific to silicon processes. Compact models use a small number of discrete circuit elements to represent the losses to minimize computation time in

simulators. More elements in the equivalent circuit mean higher accuracy but longer computation time and a balance between the two determines how complex the model is. This will be investigated in Chapter 2.

By understanding the principle loss mechanisms involved in inductors it may be possible to regain some of the area lost inside spiral inductors leading to more compact circuits. For example placing an RF circuit inside its inductor to save space or including digital circuitry inside the inductor of an RF circuit. This will be investigated using electromagnetic simulations and a test chip will be designed to examine how the performance of a Voltage Controlled Oscillator is affected.

In Chapter 3 the inductor losses will be studied using two electromagnetic simulators, one a “2.5 D” simulator Sonnet and the fully 3D field simulator HFSS. The contribution of individual loss mechanisms will be simulated by eliminating other losses through the use of perfect materials in the simulator. The ability of the compact models to fit data exported from these simulations will also be examined. Once the origin of the principle losses are understood the effects of introducing structures into the interior of the inductor will be investigated by using sheets of metal to represent capacitors.

To verify these ideas, a Voltage Controlled Oscillator (VCO) will be used and its theory of operation presented in Chapter 4. In this chapter the VCO will be designed to be operated in the 5GHz range with a tuneable frequency of a few hundred megahertz. Phase noise will be estimated as well as other operating figures such as output voltage swing and power dissipation.

Chapter 5 presents the test chip with various structures to be analyzed as well as the de-embedding techniques needed to accurately measure performance.

Chapter 6 summarizes the work done and what potential further work can be done as well as publications that may arise from the studies done in this thesis.

2. Background

2.1 Loss Mechanisms

The main issue with using on-chip inductors with silicon is the additional losses associated with the low resistivity substrate and the eddy currents generated by the magnetic fields of the inductor. As the magnetic fields penetrate the substrate currents are induced leading to a loss of power and reduced quality factor. These eddy currents increase in frequency and so when designing at higher frequencies, the associated losses cause the quality factor to continue to degrade (Christensen, 1998).

The second loss mechanism is the dielectric stack between the metal forming the inductor and the substrate which creates parasitic capacitances. These capacitances, and others that arise due to the capacitances between the metal traces themselves, affect the self-resonant frequency of the inductor as well as the quality factor. A diagram of these capacitances can be seen in Figure 3.

Thirdly the ohmic losses of the metal used to form the inductor introduce a resistance which lowers the quality factor. For the thin metal traces used for inductors however the skin depth of the metal must also be taken into account, since as the frequency of operation increases the current is restricted to smaller areas close the edges of the conductor. An example of this is shown below using Sonnet to calculate current density through a 10 μm wide metal trace from nearly dc up to a frequency of 30 GHz. At low frequency the current is uniformly distributed through the conductor but as the frequency increases current is more confined to the outer edges.

$$Q = \frac{\text{Im}\{Z\}}{\text{Re}\{Z\}} \quad (1)$$

Figure 2 - Current distribution at varying frequencies; a) 0.1GHZ, b) 6 GHZ, c) 12 GHZ, d) 18 GHZ, e) 24 GHZ, f) 30 GHZ

From these losses certain steps can be made to maximize the quality factor of on-chip inductors and have been studied before and have been outlined above. For example it is now clear why copper has been studied as a replacement for aluminum as the conductor since it has a higher conductivity, mitigating some of the conductor losses. Also more modern processes have a greater number of metal layers and so if the top metals are used the inductor is moved further away from the substrate which reduces not only the capacitance between the metal and the substrate but also the strength of the magnetic field that penetrates it and induces eddy currents. These top metal layers are included expressly for this purpose and are known as “Thick Analog Metal Layers”.

Figure 3 - Parasitic capacitances of inductors

2.2 Compact Physical Models

A variety of equivalent circuits have been developed in an attempt to model the various losses and parasitic elements of an inductor with increasing complexity as more losses are understood and higher accuracy is needed. The idea is to prevent long simulation times associated with electromagnetic simulators while still modelling the physical parasitic losses of a passive in a circuit. Based on the physical parameters of the passive, in this case an inductor, it can be replaced in the circuit by its own equivalent circuit. Below are examples of inductor models that have been used.

Figure 4 - Compact physical models, referred to as Model 1 (top left); Model 2 (top right); Model 3 (bottom left) and Model 4 (bottom right)

In the first two models R_s is the series resistance associated with the metal spiral with L_s being the ideal inductor. The feed-forward and interwinding capacitance is modelled by C_s . In the first (upper left) model the substrate effects are modelled via the capacitors C_{ox} and C_{si} which represent the oxide capacitance and substrate capacitance respectively. The substrate resistance is included via R_{si} . The second (upper right) model shows a simplification to the first and makes calculation of the quality factor easier. Most of these components can be estimated mathematically and are done so in (Stojanovic & Zivanov, 2006), as well both models 1 and 2 are defined.

The third model, shown in Figure 4c, (Gaiewski, Dunleavy, & Geis, 1994) is used here because it has the same number of elements as the first model but in a different configuration and so should have about the same accuracy as the first model (Gaiewski, Dunleavy, & Geis, 1994). The last model is much more complicated and so should have a longer solution time but much more accurate fit to the data. This model was used to provide more accurate modelling by including the current induced to flow in the

substrate as well as skin and proximity effects (Lai & Fujishima, 2006) through the added components R_{sk} and L_{sk} .

It should be noted that these models are 2-port models initially with the second port grounded. An example of the full PI-model is shown below in Figure 5.

Figure 5 - 2-Port inductor PI model

2.3 Nodal Analysis

Modelling of the compact physical models can be done using MATLAB (MATLAB) and Modified Nodal Analysis (MNA) techniques. This is done by forming a matrix that represents the circuit, in this case a 1-port circuit of a basic inductor model. If a unit current source is placed at the input the impedance of the circuit can easily be seen to be the voltage at the top node. This impedance can then be used to find the inductance (L) and the quality factor (Q) at a given frequency. The impedance is found by solving

$$Ax = b \quad (2)$$

where x is the node voltages being solved, b is the current sources and A is the matrix representation of the circuit, traditionally formed by

$$A = G + sC \quad (3)$$

where G represents the real components, the resistances, and C the imaginary components, the capacitors and inductors. The example below contains L_s , the ideal inductor with the series resistance of the metal trace represented by R_s . The feed-

forward and inter-winding capacitances are represented by C_S with C_{OX} modelling the capacitance formed between the inductor metal and the substrate with an oxide dielectric. Substrate effects are modelled with R_{SI} and C_{SI} which represent the substrate resistance and capacitance.

Other software is available that can fit an arbitrary lumped element model to S-parameters, HPSICE for example, but in this case MATLAB is used as a preliminary tool to give better control and the option to explore other nuances of fitting the data, such as examining the model's sensitivity to a given parameter.

In order to fit the components to data generated from Cadence models or from electromagnetic simulators such as Sonnet or HFSS, MATLAB (MATLAB) must be able to fit all components to both L and Q simultaneously. Using the *nlinfit* function allows a vector of data to be input and fitted parameters are output, the details of this function can be found in the Appendix. There were many difficulties with this function due to the large differences in scale of the numbers being used. For example, most capacitances are of the order of tens of femto-Farads while some resistors are in the kilo-Ohm range resulting in a difference of up to 18 orders of magnitude. When fitting the parameters if each component is adjusted by the same amount, say 10^{-15} the capacitors can be seen to have some effect on the fit since their values are being changed by a few percent, but the resistor values are being adjusted by miniscule amounts and so the fitting procedure concludes that the resistors have no effect on the fit and proceeds to ignore them. To fix this the resistor values need to first be scaled down to about the same order of magnitude as the capacitors and then the fit will proceed as expected. A similar adjustment must be made to the data as well since the *nlinfit* function can only take a one dimensional vector as the input the L and Q values must be concatenated. Again however if the L and Q values are of different orders of magnitude, typically 10^{-9} for inductor values and 10-20 for quality factor the fitting procedure will preferentially fit the L values and ignore the Q. By scaling the inductor values by a factor of 10^9 this issue is again avoided. This also would allow the user to set a scale if it is determined that one measurement needs to be more tightly fit than the other, if for example the inductance fit needs to be more accurate the L values could be scaled by an order of magnitude lower than 10^9 .

Figure 6 - Compact Model 1

$$G = \begin{bmatrix} 1/R_S & 0 & -1/R_S & 0 \\ 0 & 1/R_{Si} & 0 & 0 \\ -1/R_S & 0 & 1/R_S & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix} \quad C = \begin{bmatrix} C_{OX} + C_S & -C_{OX} & 0 & 0 \\ -C_{OX} & C_{OX} + C_{SI} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -L \end{bmatrix}$$

$$b = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad x = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ I_1 \end{bmatrix}$$

Solving for x and taking $Z=x(1)$ the quality factor can be found from equation (1) above and the inductance by (4)

$$L = \frac{\text{Im}\{Z\}}{2\pi f} \quad (4)$$

Other models used can be found with their matrix representation in the Appendix.

An example of a fit with the compact model to data simulated from the Cadence library is seen below. The inductor metal width is $5 \mu m$ with 6.5 turns and a $5 \mu m$

spacing between turns with an outer radius of $300\text{ }\mu\text{m}$. Again an example of the code to generate these fits is shown in the Appendix.

Figure 7 - Compact model fit to Spectre data

The model parameters that the fitted curve represents are as follows, with Model 1 being used for the fit

C_{OX}	45.3 fF
C_{SI}	46.6 fF
C_S	0.02 fF
R_S	5.1 Ohms
R_{SI}	193.8 Ohms
L_S	3.96 nH

To represent a more realistic measurement some noise was added to the signal. This was done by adding an uncertainty that followed a normal distribution with sigma equal to 5% of the signal and then 1000 iterations were fit. Histograms of the fitted parameters can be seen below and the code in the MATLAB m-file in the Appendix.

Figure 8 - Parameters fit with 5% noise on signal

The fit in Figure 7 may not appear to be very useful but when designing using a known frequency it can be seen that these compact models can be much more accurate. For example using the compact model to fit the Cadence library data for frequencies between 4 GHz and 6 GHz the curve fit is much better at the design frequency of 5 GHz. This fit is shown Figure 9 below and it shows an excellent fit to the library data used in the simulation design kit.

Figure 9 - Compact model narrow bandwidth fit

Figure 10 - Wideband model fit

If a larger bandwidth is needed a slightly more complicated model can be used (Guo & Tan, 2006). Figure 10 shows the resulting fit of the model shown below in Figure 11. With the inclusion of only one additional element, in this case a resistor, it can be seen that the fit improves over the entire range of frequencies fit.

Figure 11 - Wideband compact inductor model

In the early phases of research these models were to be investigated as a potential replacement for the more complex models and look-up tables currently used by commercial simulators such as Spectre, the argument being that the fabrication process has more uncertainty than the precision of the models used by Spectre. A Monte Carlo simulation was done to investigate the effects of small fabrication perturbations on the inductor. Below are the results with the blue line being the original data, the green solid line represents the highest deviation at the 5GHz and the red solid line represents the lowest (most negative) deviation at 5GHz. The black dotted line represents the fit to the original data and it can be seen that at the frequency of interest, say between 4 and 6 GHz the line lies between the two extremes. The Monte Carlo simulations are the result of 50 iterations with each parameter having no more than σ deviation. This shows that the accuracy of the compact models may be good enough and results of a fabricated device are limited by the fabrication tolerances and not by the accuracy of the models used.

Figure 12 - Monte Carlo simulation of inductor; inductance (top) and quality factor (bottom)

The following table summarizes the compact model simulation times and accuracy for the four models examined. Accuracy is defined in terms of the sum of the square of the difference between the data and the fitted line.

Table 1 - Compact model speed and accuracy summary

Model	Solution Time	L residual	Q residual	# of components
Model 1	0.92 sec	3.52	38.2	6
Model 3	8.22 sec	2.82	39.1	6
Broadband	6.69 sec	0.0814	4.67	7
Model 4	9.52 sec	0.381	0.693	8

2.4 Parameter Sensitivity

The fitted line to the provided data fits all parameters in the model but some are obviously more crucial to the fit. Below is a plot showing the sensitivity of the fit in terms of residual over ± 2 decades. The residual is defined as being the sum of the squares of the difference between the original data and the fitted data

$$R = \sum_f \left[\frac{(L - L_{fitted})}{L_{average}} \right]^2 \quad (6)$$

We would expect that the parasitic capacitances would have a large impact on the inductance curve since they affect the self-resonant frequency and indeed the first plot below shows that a small deviation in the capacitances C_{OX} or C_S , the oxide capacitance and the interwinding capacitance respectively, cause a large increase in residual, whereas a change in series resistance R_S we would expect only has an effect on the real part of the model's impedance and so would have a much lower sensitivity on the inductance residual. However since the real impedance has a large bearing on the quality factor of the model we would expect a large sensitivity to this parameter in the Q residual study and in fact the lower plot shows that R_S is the most crucial parameter in the quality factor fit. The use of compact models with a smaller amount of elements relative to large models that can be extracted using other software are used to have small, robust models that are less sensitive to arbitrary changes and yet still be accurate enough to use to design circuits.

Figure 13 - Parameter sensitivity; inductance (top) and quality factor (bottom)

A note on Figure 13 above, the independent axis is a ratio of parameter plotted compared to its value as determined by the fit, for example R_s is swept from $0.01R_s$ to $100R_s$.

2.5 Improvements

There are two principle limitations to this method, first as shown above the current distribution in the conductors is not frequency independent due to the skin depth and so a better model would include frequency dependent components. An electromagnetic simulation from Sonnet, Figure 14, shows that a fairly simple polynomial could be used to model the resistance as a frequency dependant component. The simulation comprised a metal trace equivalent to the top metal used to create the inductor. This data was also used to verify that the electrical properties of the simulator matched those listed in the Cadence design manuals since Sonnet will be used to verify the Cadence models as well as to further study the losses of the inductor.

Secondly these models are only 1-port devices to make modeling in MATLAB simpler. A 2-port model would need to calculate scattering parameters (S parameters) and while these models are fairly simple we will see that they still are able to adequately fit the Cadence models and Sonnet results using only a single port.

Figure 14 - Frequency dependent resistance in top metal

2.6 Introduction to Fabrication Process

As the performance and design of chips evolve so too must the technology. Generally as a fabrication process is improved upon the scale of physical dimensions will decrease, with transistors shrinking in both the vertical and horizontal direction. Metal traces will also scale down but as seen above a thinner metal will have a higher resistance, which will adversely affect the quality factor of inductors. So as demand increased for integrated designs that included inductors, such as Voltage Controlled Oscillators and Low Noise Amplifiers, commercial foundries have adopted the use of thicker top-metal layers to accommodate integrated inductors such as IBM (Process) and Jazz Semiconductors (Semiconductors). The dielectric layers for these new metals were also made thicker than those of lower layers to further remove the inductor from the substrate to reduce the parasitic capacitances. An example of the metallization options used by IBM in their commercial BiCMOS processes is shown below with the right side being a $2\ \mu\text{m}$ thick aluminum top metal, the middle a $4\ \mu\text{m}$ thick aluminium top metal and the left side a $4\ \mu\text{m}$ thick aluminium top metal and a second thick metal layer in $3\ \mu\text{m}$ thick copper. The latter is similar to the process used in this thesis with the top two metal layers connected in series, as seen in the SEM image below (Dunn, 2003), to implement the inductors.

Figure 15 - Process cross section (Dunn, 2003)

3. 3D Simulation of Losses

To examine the loss mechanisms of inductors in more detail electromagnetic simulators are used. The purpose of these simulators is to find numerical solutions to Maxwell's equations for problems specified by a given geometry and material properties. In this case two simulators will be used and the geometry will be an inductor similar to that found in the 0.13 μm IBM technology. Some material properties will not exactly match but the relative performance of the structures should be consistent.

3.1 Simulation Solution Methods

Two electromagnetic simulators were used to investigate the losses involved in the inductor through the field interactions between the metal conductors, substrate and dielectrics. The first program is Sonnet, a method of moments "2.5D" simulator. It is called a "two-and-a-half dimensional" simulator because the problem is defined in layers from a planar point of view. The simulator focuses on the metal conductors on each plane and the dielectric stack is defined by thicknesses and electromagnetic properties. Generally "2.5D" simulators have fields that have three dimensions but the sources, currents, of these fields are confined to a two dimensional plane (Swanson & Hoefer, 2003).

The second program is HFSS, a fully 3D simulator based on the Finite Element Method (FEM). Simulators that are fully three dimensional have much more freedom to define the problem in space and are not restricted only to two dimensional planes. This is an advantage for some problems where metal thicknesses are different from one level to another, and in this case in particular where the top metal layer is a few microns thick, simulators that are not fully 3D have difficulty modelling this accurately.

3.2 Method of Moments

A method of moments (MOM) simulator forms a solution by finding the field contribution of the current of each segment of conductor and integrating of the surface of the conductors to find the total field. Since the surfaces of the conductors are limited

to planes the integrals only need to be done in two dimensions. The field contribution of each segment of conductor is found using an expansion of known basis functions and unknown coefficients, similar to Fourier expansions where sine and cosine functions are combined to approximate a function. Other examples are power series expansions and Bessel functions, depending on the coordinate system. Due to the arbitrary shapes of the structures a higher flexibility is achieved using subsectional expansion functions and the structure is then broken up into subdomains. This is the first step in solving the fields, to create a “mesh” that will divide the structure into enough elements as to give an accurate solution. Obviously the higher the resolution of the mesh the more accurate, but also the more computationally intensive the solution will be. In an effort to reduce computation time and memory yet still have an accurate solution as possible, not all divisions need to be the same size. In a more homogeneous area of the structure the divisions can be larger and where large non-uniformities are present a denser mesh can be applied. This process is known as graded or irregular meshing. Generally this meshing procedure is done prior to any solution solving is started, but one further option to increase accuracy is to use adaptive meshing where the mesh divisions are modified based on feedback from the solution generated by the solver.

Once the meshing is completed the solution itself must be found. Without going into too much mathematical detail the unknown coefficients of the known basis functions must be determined (Swanson & Hoefer, 2003). To do this testing functions are used and the inner products between the testing functions and the basis functions must be found. Inner products give projections onto the basis vectors and this is what fills the matrices to be solved. The size of the matrix will determine computation time since the time taken to invert a matrix is proportional to N^3 and to find the unknown coefficient vector α_n the matrix of inner products $[I_{m,n}]$ must be inverted.

$$[I_{m,n}][\alpha_n] = [f_m] \quad (7)$$

In a “2.5D” simulator the structures are either defined to be laterally open or enclosed in perfectly conducting planes. In an open solution the dielectrics are assumed to extend infinitely where a closed solution has a periodicity created by the perfect sidewalls. Each approach has its strengths and weaknesses. An example of an open boundary simulator is Agilent Momentum (Agilent).

Table 2 - Summary of open planar simulators

Laterally open planar simulators	
Advantages	Disadvantages
<ul style="list-style-type: none">- No fixed grid so no limit of resolution- Possible to approximate smooth curves- Well suited for antennas	<ul style="list-style-type: none">- Numerical integration needed for Green's function (slower)- Difficult to take advantage of symmetry of problem- No ground reference- De-embedding more difficult than closed box solution

Table 3 - Summary of closed planar simulators

Laterally closed planar simulators	
Advantages	Disadvantages
<ul style="list-style-type: none">- Fixed grid yields analytic solution to Green's function (faster than numerical)- Easy to take advantage of symmetry- Bounding box serves as obvious ground plane	<ul style="list-style-type: none">- Limited resolution due to fixed grid, higher resolution increases memory requirement- Only 45 degree elements- Open solutions must be approximated

In general Method of Moments simulators have large, dense matrices to manipulate and although the matrices are smaller than the equivalent Finite Element Method (FEM) matrices, the FEM generate more sparsely populated matrices which are faster to invert. Also the MOM simulators use vias to connect different planes, but the current flow through the vias is limited only to the vertical direction. Conductors are treated as infinitely thin strips and so thick conductors can pose a problem to planar simulators. Some do offer a way to approximate thick conductors using a "Thick Metal" option where a finite number of conducting sheets are used to approximate a thicker conductor but this will take more memory and solution time will increase.

3.3 Finite Element Method

Fully three dimensional simulators need to discretize the volume of the problem, not just surfaces as in the 2.5D simulators. The volume is divided into discrete, continuous elements, generally tetrahedral in nature and can be used to divide up arbitrary shapes. This is the Finite Element Method's greatest strength; it can be used to solve almost any shape or structure and can focus on small geometries in a larger space, unlike the MOM

that has a fixed grid resolution regardless of whether the area has features or not. However this ability to solve an entire volume comes at the cost of computational complexity and time since the solution is now to be solved in three dimensions rather than only two. To help reduce the computation time FEM solvers have automatic mesh refinement to reduce the subsections in more constant regions of the problem using different sized tetrahedrons. Regardless of the refinement though a FEM solution will have a larger matrix to invert than a MOM one, but the benefit for the FEM case is the matrix is much more sparse than the dense MOM matrix and so sparse matrix techniques can be applied to the solution when inverting.

To generate the solution the field or potential values are found in the subdomains as linear combinations of expansion functions. Each point of a tetrahedron is a node and for those nodes that do not coincide with a known potential a coefficient must be solved. The fact that HFSS can solve the problem in three dimensions will likely give more accurate results over Sonnet in the cases studied here since two of the major loss mechanisms, both dealing with substrate coupling from the inductor above, are vertical in nature so a planar simulator like Sonnet may give less accurate results.

3.4 Sonnet Simulations of Loss Mechanisms

Using a 3D simulator the three main loss mechanisms were studied by building an octagonal inductor in Sonnet similar to that in the IBM 0.13 micron technology. Initially the inductor is simulated with all losses present and then the effect of replacing the lossy materials with an ideal structure is compared to the original.

The effects on the self-resonant frequency of the inductor can be seen by the shifting of the zero-crossing of the inductance plot versus frequency. As the frequency increases, the parasitic capacitances begin to become important and start to cancel out the imaginary impedance of the inductor. When these impedances are matched the inductor self-resonates and its reactance falls to zero. By understanding the main loss mechanisms it would seem likely that any change that introduces parasitic capacitances would have the most detrimental effect on the self-resonant frequency. For example without changing the physical dimensions of the inductor spiral the largest parasitic capacitance would likely be the capacitance formed between the spiral and the substrate and the dielectric oxide in between. Figure 14 shows the shift in self-resonant frequency when this dielectric is changed to an ideal dielectric of permittivity equal to 1. Since the capacitance is directly proportional to the electrical permittivity a large shift in self-resonant frequency is observed. This capacitance also has an adverse effect on the

quality factor since there is energy stored in this capacitance and another definition of quality factor is the proportional to the ratio of maximal energy stored in the inductor divided by its average dissipated power (Aguilera & Berenguer, 2003).

As mentioned one of the key differences in using on chip inductors with a silicon technology is the lower resistivity of the substrate which allows eddy currents to form from the magnetic field of the spiral. This leads to a large loss in power and as Figure 16 shows, is a large source of the limitations of the quality factor at higher frequencies due to the power lost to these currents.

At lower frequencies (e.g. 2.4 GHz) however and where many typical devices are used the limit on quality factor is the resistance of the metal traces. This can be understood from the definition of quality factor since the real part of the resistance appears in the denominator of the ratio and if this value approaches zero the Q value will become very large. Figure 16 shows this as a large spike in the quality factor when the conductors are treated as ideal.

Figure 16 - Sonnet loss effects on quality factor; Inductance (top) and quality factor (bottom)

The figures below show the breakdown of losses as they are removed from the simulation. The solid blue line is the standard inductor with all losses present, the red line is the same inductor with an ideal dielectric and the green line additionally has the substrate as ideal leaving only metal losses.

Figure 17 - Dissection of losses simulated in Sonnet; inductance (top) and quality factor (bottom)

3.5 HFSS Simulation of losses

A similar exercise was done using HFSS, a fully 3D electromagnetic simulator, using the layout extracted from Cadence and the thicknesses of the dielectrics and metals from the technology's manual and can be seen below in Figure 18. Again the effects on self resonant frequency are easily observed with the dielectric having the

largest effect on inductance. The main difference between the two structures used is that in Sonnet since you can only define shapes on a single plane at a time to connect metal layers the built in vias needed to be used. This put a limitation on the size of the vias since in the actual layout many vias are used in parallel to reduce the parasitic resistance. The problem with multiple vias and using a closed boundary method of moments simulator is the fixed grid size needed to be kept as large as possible to keep the memory usage of the simulator manageable. Due to the fact that the vias used are smaller than the grid size selected the resistances of the vias were included by estimating the resistance using the values in the process manual and tailoring the conductivity of the vias' metal in Sonnet. The goal of this simulation was to study the effects of each of the three main loss mechanisms and so an exact replica of the Cadence layout was not needed.

Figure 18 - HFSS loss sources; inductance (top) and quality factor (bottom)

To confirm that the compact models used above are based on physical parameters HFSS was used to compare the performance of two inductors, one with the standard dielectric thickness between the inductor metal and the substrate and a second with half the thickness. Compact model fitting for the two different oxide dielectric thicknesses is shown below. Figure 19 shows the HFSS simulation with a noticeably lower Q for the thinner dielectric and the results of the fit are shown in Table 4. The inductor with the thicker oxide shows much less capacitance in the fitted parameters. The first plot shows how the self resonant frequency is affected by the

thinner dielectric due to the increased capacitance. The compact model fit also reflects this with the oxide capacitance C_{OX} being much larger as well as C_{S1} and R_{S1} which model the losses due to the substrate. With the inductor being 2 times closer these parameters are about 2 times worse with the capacitance doubles and the resistance halved. See Figure 20 for the layout of the inductor used for these simulations.

Figure 19 – Effects on L and Q when dielectric is halved; inductance (top) and quality factor (bottom)

Table 4 - Model 1 fit parameters for different dielectric thicknesses

Parameter	Standard Thickness	Half thickness dielectric
Rs	2.443 Ω	2.484 Ω
Rsi	6.010 k Ω	3.542 k Ω
Csi	20.7 fF	39.1 fF
Cox	183 fF	284 fF
Cs	23.5 fF	28.5 fF
Ls	3.027 nH	2.839 fF

Figure 20 - 2 port inductor used for HFSS simulations

From the simulations above it appears that HFSS may more accurately represent the losses studied here due to the fact that it solves all fields in 3 dimensions where Sonnet is essentially a planar simulator with limited functionality for thick conductors.

3.6 Magnetic field of inductor

With the inductor metal being moved further from the substrate not only is the capacitance reduced but also the strength of the magnetic field that penetrates it is also reduced along with the power loss due to eddy currents. Niknejad solves the magnetic vector potential for a filament source from Maxwell's equations. The mathematical derivation can be found in (Niknejad & Meyer, 2001) but an outline of the procedure is as follows; once the magnetic vector is solved the eddy currents can be derived using the Poynting vector to find the power crossing into the substrate and the final solution is a sum of first- and second-order Bessel functions and a hypergeometric function. Since both types of Bessel functions decrease with distance from the current source we would expect the field to drop off away from the inductor and a plot of the maximum magnitude (90° phase) shows, in Figure 21, that indeed the field drops in strength a short distance away from the metal traces.

Figure 21 - Magnetic Field Distribution @ 5 GHz

3.7 MIM Capacitor simulations

By studying the fields on the interior of the spiral inductors we can determine how structures added to this space can affect the losses and thus performance of the inductor. If the metal added to the interior is in an area with high field the induced currents will be larger and losses higher. The results of these simulations will be used to replace the Spectre inductor model to analyze the effects of a MIM-cap placed inside the inductor on VCO performance. These simulations were done using HFSS and the differential inductor layout that will be used in the VCO design; see Figure 31 for the layout of this inductor. The capacitors will be represented by a grounded piece of metal 7 which is the top metal layer used to fabricate MIM-caps and while there are other metal layers present the small dimensions of the vias used would drastically increase simulation time and memory requirements. Firstly by looking at the magnetic field distributions inside the inductor in Figure 21 the field around a structure placed inside the inductor approximately $60\ \mu m$ away from the spiral will be in a relatively low field. With the dimensions of the inductor used here that leaves about a 100 square micron area in the centre and so for this inductor a capacitor with dimensions less than $100\ \mu m$ on a side should have minimal effect on the inductor's performance due to the eddy currents induced on the surface. There will be however a higher interwinding capacitance with the addition of metal to the interior and so performance may be limited by this factor as well. Figure 22 below shows the magnetic field magnitude with a $50\ \mu m \times 50\ \mu m$ grounded metal block and there appears to be little effect on the surrounding magnetic field. With a $150\ \mu m \times 150\ \mu m$ piece the metal is now present inside regions of high field and so higher eddy currents would lead to more losses and reduced quality factor.

Figure 22 - Magnetic Field Distribution @ 5 GHz with 50µm x 50µm MIM

Figure 23 - Magnetic Field Distribution @ 5 GHz with 150µm x 150µm MIM cap

Figure 24 - Performance effects of various sized MIM caps; inductance (top) and quality factor (bottom)

Figure 24 shows the effects on inductor performance predicted by HFSS and in terms of Q we see there is almost no difference between the inductor alone and the addition of the $50\ \mu\text{m} \times 50\ \mu\text{m}$ metal piece. With the $100\ \mu\text{m} \times 100\ \mu\text{m}$ capacitor

there does appear to be a slight degradation in Q from 28 to 26, but once the largest capacitor is added, $150\ \mu\text{m}$ per side, the quality factor drops sharply, indicating there is a limit to the amount of material that can be placed inside the inductor. If these losses are in fact due to eddy currents induced on the capacitor an array of capacitors representing the same area but broken up into smaller pieces should reduce the losses by restricting the amount of current induced per piece, in a similar fashion to a patterned ground shield. This was examined again using HFSS and replacing the $100\ \mu\text{m} \times 100\ \mu\text{m}$ sheet of metal with four $50\ \mu\text{m} \times 50\ \mu\text{m}$ sheets and one hundred $10\ \mu\text{m} \times 10\ \mu\text{m}$ sheets. Figure 25 shows that the inductance at typical working frequencies below 8 GHz or so is not affected much by the different capacitor layouts, but the quality factor is lowered for a single piece $100\ \mu\text{m}$ per side. By breaking this piece into smaller pieces and restricting the induced current the quality factor improves. For example, by placing a $100\ \mu\text{m} \times 100\ \mu\text{m}$ sheet inside the inductor the quality factor falls by close to 7%. If this sheet is replaced by one hundred $10\ \mu\text{m} \times 10\ \mu\text{m}$ sheets, representing the same area, the quality factor only falls by 3% compared to the standard inductor alone. A more involved study on optimizing the patterning of interior capacitors with larger pieces in areas with lower field (centre) and smaller pieces closer to inductor traces in high field regions may lead to even better improvements. A similar study looking at varying the metal trace width of each turn of an inductor can be found in the literature (Lopez-Villegas & Samitier, 2000). This study essentially decreases the trace width on the interior turns where magnetic fields are high and eddy currents are induced in the metal of the inductor.

Table 5 - Inductance and Q of various MIM capacitors inside inductor spiral

Capacitor	L@5GHz	Q@5GHz	Capacitor	L@5GHz	Q@5GHz
None	4.65	26.0	$(100\mu\text{m})^2$	4.44	24.2
$(50\mu\text{m})^2$	4.60	26.2	$4 \times (50\mu\text{m})^2$	4.42	24.1
$(150\mu\text{m})^2$	3.89	20.7	$100 \times (10\mu\text{m})^2$	4.52	25.2

Figure 25 - L and Q for various 100umx100um capacitor layouts; inductance (top) and quality factor (bottom)

These simulations support the idea that if placed with some thought components on the interior of planar spiral inductors can have negligible effect on the performance of the inductor. For most components in a typical RF circuit (VCO, mixer, LNA) the layers used are closer to the substrate than those of the MIM-cap and so induced eddy

currents would be comparatively smaller due to reduced fields further from the inductor. The dimensions of the transistors and metal interconnects used are much smaller and we have seen that the effects of small conductors inside the inductor are also reduced relative to larger ones. In order to examine these effects in a real circuit a VCO will be designed and modified to study the consequences of including RF as well as digital circuitry and passive components where this has traditionally not been permitted.

A similar exercise was done in Sonnet using a standard inductor with only the top metal used as the inductor trace with the second as the underpass. This inductor had the same outer diameter but with only one metal layer instead of two in parallel the resistance will be higher, decreasing the quality factor. The relative performance however is similar; with a $50\ \mu\text{m} \times 50\ \mu\text{m}$ metal sheet there is little performance lost, only 0.7% drop in Q while with a $100\ \mu\text{m} \times 100\ \mu\text{m}$ sheet the quality factor drops 12.1%; see Figure 26.

Figure 26 - Sonnet quality factor for different MIM sizes

The $100\ \mu\text{m} \times 100\ \mu\text{m}$ capacitor was then again replaced by a grid of capacitors representing the same area, broken up into 4 pieces and then 100. The first case, a grid of 4 $50\ \mu\text{m} \times 50\ \mu\text{m}$ showed a slight improvement but still a 9.9% drop in peak quality factor. Once the capacitor was broken up into one hundred $10\ \mu\text{m} \times 10\ \mu\text{m}$ the drop in quality factor was negligible compared to the standard inductor alone; only a drop of 0.01%, these plots can be seen below in Figure 27.

Figure 27 - Sonnet simulations of capacitor grids

The next step to being able to use the interior of the inductor would be to develop a compact model that reflects the changes in performance. For example allow a circuit designer to place whatever elements he wants but in an area restricted to the centre of the inductor where losses are lower and the magnetic field is minimal. Other models may also be affected by including devices in a magnetic field and so transistor models should be simulated to verify any performance changes due to the presence of the inductor's field. Another effect that needs to be addressed as well include increased coupling from having to route signals into the inductor.

4 Voltage Controlled Oscillator

The purpose of a voltage controlled oscillator (VCO) is to provide a stable periodic reference signal, and can be a clock for digital logic or a frequency for transmitters, receivers or mixers. At the core of the oscillator is the LC resonator and this is the reason tuneable capacitors and an inductor with a high quality factor is needed. These passive components have a series resistance and for an oscillator to be made positive feedback must be added, for this circuit a negative gm ($-G_M$) structure will be used to provide the compensation for the losses, in the inductor and capacitors. Also a differential design will be used for common mode noise rejection. A basic topology for this VCO is seen below in Figure 28.

Figure 28 - Negative Gm oscillator (differential)

4.1 Phase Noise

Ideally a VCO oscillates at the desired frequency with no power in nearby frequencies, an impulse function in the frequency domain. However due to noise that causes phase variations in the signal a real oscillator has a waveform as seen below

$$V_{osc} = A \cos [\omega_o t + \phi_n(t)] \quad (8)$$

with $\phi_n(t)$ being the phase noise of the oscillator.

Figure 29- Feedback model of oscillator

With $H(s) = H_1(s) + H_2(s)$

$$\frac{N_{in}(s)}{N_{out}(s)} = \frac{H_1(s)}{1-H(s)} \quad (9)$$

If $H(s)$ is approximated with a Taylor series $H(j\omega) = H(j\omega_o) + \Delta\omega \frac{dH}{d\omega}$ and assuming stable oscillation, $H(j\omega) = 1$ then

$$\frac{N_{in}(s)}{N_{out}(s)} = \frac{H_1}{-\Delta\omega \frac{dH}{d\omega}} \quad \text{or as noise power: } \left| \frac{N_{in}(s)}{N_{out}(s)} \right|^2 = \frac{|H_1|^2}{(\Delta\omega)^2 \left| \frac{dH}{d\omega} \right|^2}$$

Using $H(j\omega) = |H|e^{j\phi}$ and $\frac{dH}{d\omega} = \frac{d|H|}{d\omega}e^{j\phi} + |H|je^{j\phi} \frac{d\phi}{d\omega}$ and since the two right hand terms are orthogonal,

$$\left| \frac{dH}{d\omega} \right|^2 = \left| \frac{d|H|}{d\omega} \right|^2 + |H|^2 \left| \frac{d\phi}{d\omega} \right|^2 \quad (10)$$

At oscillator resonance the variation of the phase is much greater than that of the amplitude and $|H|$ is approximately unity and so the second term is dominant

resulting in $\left| \frac{dH}{d\omega} \right|^2 = \left| \frac{d\phi}{d\omega} \right|^2$ and substituting this result back in to the noise power equation we get

$$\left| \frac{N_{in}(s)}{N_{out}(s)} \right|^2 = \frac{|H_1|^2}{(\Delta\omega)^2 \left| \frac{d\phi}{d\omega} \right|^2} \quad (11)$$

Since we have a definition of quality factor as

$$Q = \frac{\omega_o}{2} \left| \frac{d\phi}{d\omega} \right| \quad (12)$$

At resonance $|H|=1$ and thus the noise power equation becomes

$$\left| \frac{N_{in}(s)}{N_{out}(s)} \right|^2 = \frac{\omega^2}{4Q^2(\Delta\omega)^2} \quad (13)$$

If P_S is the input power of the carrier and the phase noise is half the noise present, along with amplitude noise, and we take the ratio of absolute output noise over half the carrier power to get the usual expression for phase noise

$$PN = \left(\frac{\omega}{2Q\Delta\omega} \right)^2 \left(\frac{|N_{in}(s)|^2}{2P_S} \right) \quad (14)$$

The source of the resonator losses are due to its resistance and so the input noise power is kT and the noise from the biasing network transistors can be found from the noise figure F , giving the final expression for phase noise as (Leeson, 1966)

$$PN = \left(\frac{\omega}{2Q\Delta\omega} \right)^2 \left(\frac{FkT}{2P_S} \right) \quad (15)$$

4.2 Overall Circuit Design

In order to be able to measure the performance of the Voltage Controlled Oscillator (VCO) the circuit must have an output buffer to provide a high resistance output, an LC tank that provides the desired oscillating frequency and a feedback or amplification stage to overcome the losses present in the passives of the tank. To begin the current density for the transistors must be set to give the best noise figure to ensure a lower phase noise. Below shows a plot of the noise figure with respect to biasing current for a $5 \mu m$ transistor. We can see that the optimum bias current occurs at $0.15 mA$, which corresponds to $30 \mu A/\mu m$. Realistically the current can be slightly reduced from this to conserve power dissipation without hurting the noise

factor too much. This information will be used to size the transistors once the needed bias current is found.

Figure 30 - Minimum noise figure vs. bias current (5 μ m transistor)

4.3 LC Resonator Design

To keep the inductors studied in the 3D and compact model simulations consistent the inductor will be of the same dimensions and design as previously used. This means a 3 turn differential inductor with a metal width of 10 μ m spaced 5 μ m apart. The differential inductor is used to have an increased Q over the standard inductor. The standard inductor has the metal that forms the inductor implemented in the top metal layer, with the second metal layer providing an underpass. In the case of the differential inductor there is no need for an underpass and so the top two metal layers can be connected in parallel, reducing the resistance of the inductor. It should be noted that this inductor is not optimized for the frequency range being studied, and if the desire was to design a VCO with the best phase noise possible, further optimizations would

need to be run. The purpose of this study is to measure the relative effects on performance due to the inductors interactions with nearby structures.

Figure 31a - Standard octagonal inductor; b – Differential octagonal inductor

The target frequency range of the VCO is around 5 GHz. The purpose of the VCO will be to show how the quality factor of the inductor affects figures of merit such as the phase noise as well as any frequency shift so we will set the frequency of the resonator using minimum size capacitors and varactors that give a decent amount of tuning.

Figure 32 - Inductor characterization

Characterizing the inductor in the circuit simulator gives the inductance at close to 5 GHz and from this the necessary total capacitance can be calculated.

$$\omega = \frac{1}{\sqrt{LC_{TOT}}}$$

$$C_{TOT} = \frac{1}{(2\pi \cdot 5GHz)^2 4.8nH}$$

$$C_{TOT} = 211fF$$

To make the frequency tuneable a varactor needs to be able to provide a range of capacitances. Two varactors will be used to allow a centre node where the bias voltage will be applied. The two varactors in series will halve the capacitances so each individually must have twice the desired tuning range. To ensure the correct tuning range the varactor must be able to provide a total capacitance swing of about 75fF which means each individually must be able to provide a range of 150fF. A 5um by 5um ncap varactor (Division, 2007) is characterized below showing the capacitance range and

its Q value. To ensure a good parallel resistance for the varactors they should be kept to a minimum size that still gives the necessary tuning range. In this case a total of 211 fF is required and from the graph below it can be seen that the capacitance will be less than this value for the varactors since at the high end of the bias range it is still only 75 fF . The rest of the capacitance in the circuit will be provided by the parasitic capacitances of the transistors that load the inductor or fixed capacitances if needed.

$$C_{TOT} = 2C_{VAR} + 2C_{buff} + C_{fixed}$$

Where C_{buff} is the parasitic loading capacitance added by the output buffer and C_{fixed} is any additional capacitance needed to give the desired resonance frequency. In this case the output of the resonator will load a 120 nm by 100 μm transistor and from the model parameters given by the simulator the parasitic capacitance of this size transistor is about 33 fF .

We can now see that the total capacitance added by the varactors and fixed capacitors needs to be about 178 fF . By placing two varactors with an AC ground between them they are effectively connected in parallel to allow a biasing voltage to be applied their total capacitance will be twice that of each one individually. The figure below shows the capacitance versus frequency plot for the varactor described above. At a moderate bias voltage of 1V the capacitance of each varactor is close to 75fF, a higher bias voltage is used to give a better Q value for the varactors. With an AC ground between them this gives another 150 fF leaving slightly less than 30 fF which will be provided by the output buffer if transistors of a similar size are used and making it unnecessary to include a fixed capacitor. There are likely more parasitic capacitances and so the simulated circuit may oscillate slightly below the targeted 5 GHz but again the purpose of this design is not a fully optimized, ultra low-noise VCO but more to study the inductor's effects on the design.

Figure 33 - Varactor capacitance characterization

Figure 34 - Varactor quality factor characterization

From the capacitance values we can now estimate the oscillator frequency.

$$\omega = \frac{1}{\sqrt{L(2 \cdot C_{VAR} + 2 \cdot C_{buff})}}$$

$$f = \frac{1}{2\pi \sqrt{L(2 \cdot C_{VAR} + 2 \cdot C_{buff})}}$$

$$f = \frac{1}{2\pi \sqrt{4.8nH(2 \cdot 75fF + 2 \cdot 33fF)}}$$

$$f = 4.94 \text{ GHz}$$

4.4 Negative Gm design

The passive elements that make up the LC tank however have a resistance associated with them and so it is not a purely LC circuit but RLC instead and any oscillation would then decay proportional to $e^{-t/RC}$. The amplifier stage of the VCO must compensate for the resistance of the passive components to ensure oscillation.

In this case the inductor has a value of 4.8 nH and a Q of 11.2 at 5 GHz.

$$R_{P,L} = \omega L Q$$

$$R_{P,L} = 2\pi \cdot 5\text{GHz} \cdot 4.8\text{nH} \cdot 11.2$$

$$R_{P,L} = 1.69 \text{ k}\Omega$$

The varactors, assuming a bias potential of 1V, have a value of 75 fF and a Q of 9.8 which results in the following parallel resistance.

$$R_{P,Cvar} = \frac{Q}{\omega C}$$

$$R_{P,Cvar} = \frac{9.8}{2\pi \cdot 5\text{GHz} \cdot 75\text{fF}}$$

$$R_{P,Cvar} = 4.16 \text{ k}\Omega$$

These resistances in parallel thus give a total resistance of $1.20 \text{ k}\Omega$. To ensure oscillation the g_m of the transistors used must be larger than $2/R_p$ which is 1.6 mA/V , a very small g_m and so a transistor with any moderate amount of current should be enough to ensure oscillation. The lengths of the transistors were kept to minimum size

and the width set at $100 \mu m$ to ensure adequate current flow. Simulation showed that the g_m of these transistors is $13.9 mA/V$ well above what is needed to balance the losses in the passive components. A current mirror was used to bias the circuit and this transistor was also made to be $100 \mu m$ but the length was increased to $3 \mu m$ instead of the minimum $120 nm$ to reduce $1/f$ noise since a noise analysis showed that the biasing transistor of the current mirror was a main source of noise and $1/f$ noise is proportional to the area of the gate of the transistor.

Once the condition for oscillation has been satisfied, the oscillations will grow until the gain limit is reached, set by non-linearities in the transistors. To get a desired output voltage swing the bias current must be determined since

$$V_{Tank} = \frac{2}{\pi} R_p I_{bias} \quad (16)$$

If we assume a peak amplitude of $400 mA$, or $800 mA$ peak-to-peak the bias current needed can be found

$$\begin{aligned} I_{bias} &= \frac{\pi V_{Tank}}{2 R_p} \\ I_{bias} &= \frac{\pi 800 mA}{2 \cdot 1.2 k\Omega} \\ I_{bias} &= 1.05 mA \end{aligned} \quad (17)$$

With this we can now size the transistors in the $-G_m$ stage of the circuit. Above we found that the best current density for minimum noise figure was $30 \mu A/\mu m$, but to conserve power consumption this can be reduced to $10 \mu A/\mu m$ while not raising the noise factor too much. Thus with slightly over $1000 \mu A$ needed a $100 \mu m$ transistor will adequately bias the oscillator. The addition of these transistors adds parasitic capacitances that appear in parallel with the varactors adding to the total capacitance and lowering the frequency of oscillation. The simulator shows that the parasitic overlay capacitances total close to $33 fF$. With the inductor centre-tapped the equivalent circuit with the parasitic capacitances are shown below each branch has a varactor at $75 fF$ and the capacitance of the buffer transistor. In total there are two branches in parallel each with $108 fF$ of capacitance giving a total of $216 fF$ close to the desired amount giving an expected $4.94 GHz$ oscillation frequency. There are additional capacitances from the amplifier stage but they are minimal because they are not connected to an AC ground directly but instead are in series with the capacitance of the current mirror transistor as well as the decoupling capacitor which drastically reduces the capacitance. These calculations are also just a starting point of the design and depending on the biasing current required or capacitances supplied by the

transistors some parameters may need to be modified. The values reported here were decided upon after an iterative process.

Figure 35 - Parasitic capacitance

From the parallel resistance of the passive components the quality factor of the VCO can be determined.

$$Q_{osc} = R_P \sqrt{\frac{C_{TOT}}{L}} \quad (18)$$

$$Q_{osc} = 1.2 \, k\Omega \sqrt{\frac{211 \, fF}{4.8 \, nH}}$$

$$Q_{osc} = 8.0$$

Using the quality factor of the tank and the calculated output response the phase noise can be estimated using the equation as seen earlier

$$PN = \left(\frac{\omega}{2Q\Delta\omega} \right)^2 \left(\frac{FkT}{2P_S} \right)$$

Assuming the noise from the rest of the circuit is minimal F will be close to 1 and so with P_S calculated as

$$P_S = \frac{v_{tank}^2}{2R_P} \quad (19)$$

$$P_S = \frac{(800 \text{ mV})^2}{2 \cdot 1.20 \text{ k}\Omega}$$

$$P_S = 0.267 \text{ mW}$$

This gives an estimate of the phase noise at 1 MHz as

$$PN = \left(\frac{2\pi \cdot 5 \text{ GHz}}{2 \cdot 8 \cdot (2\pi \cdot 1 \text{ MHz})} \right)^2 \left(\frac{kT}{2 \cdot 0.267 \text{ mW}} \right)$$

$$PN = 2.99 \times 10^{-11}$$

$$PN = -105.2 \text{ dBc/Hz}$$

4.5 VCO simulation results

To verify that the VCO performs as expected from the design Spectre was used to find the phase noise, tuning range and output voltage swing. As seen in Figure 36, the phase noise is close to the expected -105 dBc/Hz for the three bias conditions shown. Figure 37 shows that the tuning range for biasing of $0 - 1.5 \text{ V}$ is approximately 4.9 GHz to 5.12 GHz . The third graph, Figure 38, shows that at the design point of bias voltage of 1 V , the frequency of oscillation is 4.98 GHz with a voltage swing of slightly over 300 mV .

Figure 36 - Phase Noise of VCO

Figure 37 - VCO Oscillation Frequency vs. Bias Voltage

Figure 38 - VCO Transient Response

5 Test Chip

In RF circuits the quality of the circuit will be dependant on the quality factor of the passive components. In this section we will look at the Voltage Controlled Oscillator (VCO) as a test circuit and how adding circuitry to the interior of the inductor affects the performance of the VCO by examining the phase noise and oscillation frequency. Also an inductor will be more directly studied in a resonator to examine the effects of the addition of various arrangements of decoupling capacitors to the interior space. De-embedding techniques will be needed to extract the scattering parameters of the structures as well as to characterize the other passive components used to make the VCO, namely the varactors. Design layout was done using the Virtuoso Schematic Editor in the Cadence tool kit (Virtuoso) and circuit simulations with the Spectre Circuit Simulator (Spectre). The total chip area is 2mm x 2mm with the inductors approximately 300 μm on a side.

Figure 39 - Layout of Test Chip

5.1 Resonator

Before examining the VCO a simpler circuit will be built and analyzed. A basic LC resonator with a single inductor and a capacitance to give a resonant frequency near 5GHz is used. In order to be able to measure the performance of the circuit the capacitance is broken up in to 3 series capacitors to allow the measurement probes to be connected without additionally loading the inductor, Figure 40 shows the circuit.

Figure 40 - Resonator circuit

In order to avoid loading the inductor with the capacitances of the measurement probes the inductor is placed in a resonator and the S parameters used to analyze the inductors characteristics. This is done to avoid unnecessarily loading the inductor with a mismatched impedance that would introduce loss not related to the inductor performance since as we saw in the compact model fitting the series resistance of the inductors is less than $3\ \Omega$. Two test structures are designed using the inductor studied above along with the necessary de-embedding structures. Using the 3 turn differential inductor introduced earlier and a frequency of 5 GHz the necessary capacitance can be trivially calculated.

$$\omega = \frac{1}{\sqrt{LC}} \quad (20)$$

$$C = \frac{1}{(2\pi f)^2 L}$$

$$C = \frac{1}{(2\pi \cdot 5GHz)^2 4.8nH}$$

$$C = 211 fF$$

To avoid applying the measurement probes across the inductor the capacitance is broken into three series capacitors each with 3 times the capacitance calculated above.

Figure 41 below shows the expected reflection coefficient of the resonator from the circuit simulator in Cadence. The circuit was then exported to HFSS to verify the results from a purely electromagnetic simulator, the results are seen below in Figure 42. It shows that as expected with a $100\mu m \times 100\mu m$ capacitor on the interior the inductance is slightly affected, and in fact slightly lowered which will correspond to a slight increase in resonant frequency. As seen in Table 5 the inductance shifts from about $4.65 nH$ to $4.44 nH$. Using these values the expected resonant frequencies should be $5.08 GHz$ and $5.20 GHz$ respectively. We see that the Spectre models predict that the resonant frequency should be $5.09 GHz$ for the resonator and HFSS about $4.95 GHz$. This difference is likely due to the dielectric thickness used in HFSS since no value for this is given in the design manual for the process and had to be estimated. However with the MIM capacitor in place in the HFSS simulation we do see the expected $200 MHz$ shift in resonant frequency.

Figure 41 - Spectre S11 of resonator

Figure 42 - HFSS simulation of resonator

In the diagram of the test chip seen above in Figure 39 there are 5 different versions of the resonator to test the performance impact of different inductor configurations.

- Standard resonator – Baseline measurement to which other circuits will be compared (Labelled A in diagram)
- Resonator with $50\ \mu\text{m} \times 50\ \mu\text{m}$ MIM inside inductor (Labelled B in diagram)
- Resonator with $100\ \mu\text{m} \times 100\ \mu\text{m}$ MIM inside inductor (Labelled C in diagram)
- Resonator with grid of $10\ \mu\text{m} \times 10\ \mu\text{m}$ MIMs inside inductor (Labelled D in diagram)
- Resonator with patterned ground shield inductor (Labelled E in diagram)
- De-embedding structures for resonator measurements (Labelled F in diagram)

Other ideas that could be investigated to reduce coupling and loss would be to include a guard ring inside the inductor and to use a parallel ground plane to isolate signals that are being brought into the inductor.

Figure 43 - Divider schematic

Figure 44 - Divider Layout

5.2 Resonator De-embedding

In order to measure the performance of the inductor alone the parasitic elements introduced by the pads and surrounding circuitry must be accounted for. For the inductor alone a resonator is built to measure the performance and the S11 reflection coefficient is used to determine inductance value and quality factor. In order to isolate the parameters of the inductor alone the parasitics of the rest of the devices and metal interconnects must be accounted for and removed from the measurements.

Traditionally only the parallel parasitics are taken into account by measuring the complete structure as a reference, in the following discussion referred to as S_{DUT} , followed by removing the device of interest, in this case an LC tank circuit and measuring the rest of the structure, giving another set of S-parameters S_{open} . This S_{open} measurement takes into account the parasitic capacitances of the probe pads and interconnects. From these two measurements the S-parameters of the tank alone can be calculated

$$Y_{resonator} = Y_{DUT} - Y_{open} \quad (21)$$

An improved technique also takes into consideration the S-parameters of a short circuit of the probe pad and interconnects to compensate for their associated parasitic resistances (Koolen, Geelen, & Versleijen, 1991). The admittance parameters can be found from

$$Y_{resonator,OS} = \left((Y_{measured} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1} \right)^{-1} \quad (22)$$

These admittance parameters can then be transformed into S parameters or any other form needed. A second method to de-embed is to use a slightly different equation; the method above is referred to as “open-short” de-embedding while the following is a “short-open” method.

$$Y_{resonator,SO} = (Y_{measured}^{-1} - Y_{short}^{-1})^{-1} - (Y_{open}^{-1} - Y_{short}^{-1})^{-1} \quad (23)$$

According to the research the open-short equation can give negative resistance values for inductors and for passive devices this is not realistic and so the short-open technique is preferred (Tiemeijer & Havens, 2003).

5.3 VCO designs

Above in Section 4.1 the phase noise of the VCO is shown and repeated here for convenience. The phase noise is seen to be inversely proportional to the quality factor of the passive components and so if the quality factor of the inductor is not adversely affected by placing circuit elements inside the phase noise should not suffer.

$$PN = \left(\frac{\omega}{2Q\Delta\omega} \right)^2 \left(\frac{FkT}{2P_S} \right)$$

To test this variations of the VCO designed above will be fabricated. The first is just a standard VCO with current design rules followed, i.e. no structures placed inside the metal spiral of the inductor. The second is the same VCO design but with the VCO core circuitry placed inside the spiral of the inductor, or a so-called Self Contained VCO. The third test geometry will test the performance of the VCO with slower digital circuitry placed inside the inductor. The digital circuit in this case is a frequency divider circuit

designed by Carleton graduate student Victor Karam (Karam, 2008) and should just take the waveform output by the VCO and divide the frequency in two. Other circuits to be tested include a VCO with a patterned ground shield (PGS) under the inductor as well as with a single MIM capacitor.

- Standard VCO (Labelled G in diagram)
- Self-Contained VCO (Labelled H in diagram)
- VCO with divider (Labelled I in diagram)
- VCO with PGS (Labelled J in diagram)

By placing the divider circuit inside the VCO's inductor we can compare the difference in performance of the RF circuit when the circuit's own circuitry is placed inside the inductor versus when an unrelated digital circuit is used. In the case of the Self-Contained VCO there is a greater likelihood of increased coupling because the signal on the inductor directly affects the VCO circuitry.

Below is the schematic for the VCO design in Figure 45.

Figure 45 - VCO schematic

5.4 Varactor Characterization and De-embedding

The final structures needed are those to characterize the performance of the varactors used in the VCO. These include a two-port measurement of the varactor and the necessary de-embedding formations. Two ground-signal-ground (GSG) pad configurations are used and can be seen at the bottom of the chip in Figure 39 above. According to (Tiemeijer & Havens, 2003) again a short-open de-embedding technique

will be used but this time the full complement of S-parameters can be measured; S_{11} , S_{21} , S_{12} , and S_{22} .

6 Conclusions

6.1 Summary of Work

The goal of this thesis is to further understand the compact models and losses present in planar spiral silicon on-chip inductors and determine if using the space inside the inductor can lead to reduced layout footprint without sacrificing performance. Compact models were implemented in Matlab and electromagnetic simulators used to model the losses present as well as more complex structures.

Results from the simulated inductors from HFSS and Sonnet suggest that using the area inside the inductor should not decrease performance, or quality factor, due to eddy currents as long as the layout is done with an understanding of the losses involved. Large sheets of metal placed near the metal traces of the inductor will have large eddy currents due to the magnetic field of the spiral, but if this metal is broken up the eddy currents will be much smaller and losses negligible. An application studied here is the use of Metal-Insulator-Metal (MIM) capacitors used for decoupling capacitors since they are typically fairly large. If the equivalent amount of capacitance is implemented as many smaller capacitors in parallel instead of one large capacitor losses can be reduced from 7 percent to less than 3 percent. If the capacitor is small enough that its edges are far from the inductor metal then the affects are minimal. Further work in this area can lead to more formal design rule changes to govern the use of interior spaces of inductors.

A Voltage Controlled Oscillator (VCO) was designed to study the effects of different elements placed inside the inductor. A standard VCO is designed first as a baseline for other measurements. Modelling suggests that the figures of merit of the VCO should not be affected and a test chip was designed to verify the simulations.

6.2 Thesis Contributions

The contributions of this thesis to the RFIC design and modelling are summarized as follows

- Understanding the compact model parameters and how they model physical losses
- Using electromagnetic simulations to isolate and investigate losses in inductors due to metal resistivity, parasitic capacitances and induced eddy current losses in the silicon substrate
- Investigating the effects of including circuitry inside spiral inductors, from simple capacitors to digital and analog circuits
- Design of a typical Voltage Controlled Oscillator as a test circuit to examine the effects on phase noise when circuitry is added inside the inductor
- The design and implementation of various test circuits to verify simulations and proposal that some of the lost area in the interior of a spiral inductor can be recovered, including a simple LC resonator and an analog circuit whose figure of merit largely depends on the performance of the inductor

6.3 Future Work

Unfortunately the test chip will not be fabricated in time for measurement results to be included here and so once the chip comes back measurements of the VCO and resonator will be done to verify the simulations and the results possibly published at that time.

An extension to this work could include a more thorough and mathematical analysis of the magnetic fields and determination of a minimum induced current acceptable for a given size of structure inside the inductor to allow design rules to be written to allow chip designers to use the space inside an inductor. From here a compact model could be developed to represent the effects of adding circuitry into the inductor.

Other compact circuits that depend on inductors can also be investigated, such as mixers, low noise amplifiers or even RFID tags. The electromagnetic simulation and circuit level simulation can also be brought closer together by using the data from the EM simulators (S-parameters or L and Q values) and importing them into Cadence to study the relative effects on phase noise that the additional components inside the

inductor has on the circuit as a whole. This can also be done using the compact models to study whether or not they are accurate enough to use and thereby increase simulation speed.

7 Appendix

Model 2

Figure 46 - Compact Model 2

$$G = \begin{bmatrix} 1/R_P + 1/R_S & -1/R_S & 0 \\ -1/R_P & 1/R_S & 1 \\ 0 & 1 & 0 \end{bmatrix}$$

$$C = \begin{bmatrix} C_P + C_S & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -L \end{bmatrix}$$

$$b = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \quad x = \begin{bmatrix} V_1 \\ V_2 \\ I_1 \end{bmatrix}$$

Model 3

Figure 47 - Compact Model 3

$$G = \begin{bmatrix} 1/R_1 & -1/R_1 & 0 & 0 & 0 \\ -1/R_1 & 1/R_1 + 1/R_3 & 0 & -1/R_S & 0 \\ 0 & 0 & 1/R_3 & 0 & 1 \\ 0 & -1/R_S & 0 & 1/R_S & 1 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix}$$

$$C = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & C_1 + C_2 & -C_2 & 0 & 0 \\ 0 & -C_2 & C_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -L \end{bmatrix}$$

$$b = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad x = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ I_1 \end{bmatrix}$$

Broadband Model

Figure 48 – Broadband inductor model

$$G = \begin{bmatrix} 1/R_1 + 1/R_P & -1/R_1 & 0 & 0 & 0 \\ -1/R_1 & 1/R_1 + 1/R_3 & 0 & -1/R_S & 0 \\ 0 & 0 & 1/R_3 & 0 & 1 \\ 0 & -1/R_S & 0 & 1/R_S & 1 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix}$$

$$C = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & C_1 + C_2 & -C_2 & 0 & 0 \\ 0 & -C_2 & C_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -L \end{bmatrix}$$

$$b = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad x = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ I_1 \end{bmatrix}$$

Matlab function "addnoise"

```
function y = addnoise(x,percent)
% takes data vector x and adds noise to it

n=(2*rand(max(size(x)),1)-1)*percent/100;

lengthn=size(n);
lengthx=size(x);

if lengthn(1)~=lengthx(1)
    n=n';
end

noise = n.*x;

y=x+noise;
```

Matlab function "noise1" – used to generate histograms of fitted parameters with noise added to signal

```
% open datafile
file='../data\spectre.txt';

iterations = 1000;
Cs_fit(iterations)=0;
Cox_fit(iterations)=0;
```

```

Csi_fit(iterations)=0;
Rs_fit(iterations)=0;
Rsi_fit(iterations)=0;
Ls_fit(iterations)=0;

for n=1:1:iterations

    [Cs_fit(n) Cox_fit(n) Csi_fit(n) Rs_fit(n) Rsi_fit(n) Ls_fit(n) L Q
freq] = fit1(file);

end

subplot(2,3,1)
hist(Cs_fit)
title('Cs')
subplot(2,3,2)
hist(Csi_fit)
title('Csi')
subplot(2,3,3)
hist(Cox_fit)
title('Cox')
subplot(2,3,4)
hist(Rs_fit,10)
title('Rs')
subplot(2,3,5)
hist(Rsi_fit)
title('Rsi')
subplot(2,3,6)
hist(Ls_fit)
title('Ls')

```

Matlab function “fit1” – used to return Model 1 fitted parameters of a given file

```

function [Cs_fit,Cox_fit,Csi_fit,Rs_fit,Rsi_fit,Ls_fit,L,Q,freq] =
fit1(file)

% % open datafile
file = fopen(file,'r');

[data,count]=fscanf(file,'%g %g %g',[3 inf]);
data=data';
count=count/3;

freq=data(:,1);
L=data(:,2);
Q=data(:,3);

L=addnoise(L,5);
Q=addnoise(Q,5);

% Generated Data Initial Conditions
beta0(1)=20e-15;
beta0(2)=100e-15;

```

```

beta0(3)=20e-15;
beta0(4)=3;
beta0(5)=500;
beta0(6)=6e-9;

scaleL=1;

if mean(L)<0.01
    scaleL=1e9;
end

if beta0(4)>1e-5 && beta0(5) > 1e-5
    scaleR=1e15;
end

beta0(4)=beta0(4)/scaleR;
beta0(5)=beta0(5)/scaleR;
L=L*scaleL;

fitdata=cat(1,L,Q);
beta0=beta0';

% options=statset('Robust','on','TolFun',1e-
12,'MaxIter',1000,'TolX',1e-16)
options=statset('Robust','off','TolX',1e-17,'MaxIter',1000,'TolFun',1e-
20);

[beta,r,J]=nlinfit(freq,fitdata,@modell,beta0,options);

Cs_fit=abs(beta(1));
Cox_fit=abs(beta(2));
Csi_fit=abs(beta(3));
Rs_fit=abs(beta(4))*scaleR;
Rsi_fit=abs(beta(5))*scaleR;
Ls_fit=abs(beta(6));

```


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