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An FM Receiver Architecture For Dual-Mode/Multi-Mode Mobile Receivers

by

Brian Robar

A thesis submitted to the Faculty of Graduate Studies and Research in
partial fulfillment of the requirements for the degree Masters of Engineering

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the Faculty of Graduate Studies and Research
acceptance of this thesis

“ An FM Receiver Architecture For
Dual-Mode/Multi-Mode Mobile Receivers”

submitted by Brian David Robar, B. Eng.

in partial fulfilment of the requirements
for the degree of Master of Engineering

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Abstract

The purpose of this thesis is to investigate a possible dual mode radio receiver suitable for backward compatibility with older first generation cellular systems. With the number of conflicting digital standards emerging in North America, and internationally, multi-mode radios will become important. This backward compatibility not only provides easier deployment of newer technologies, but also provides an extended coverage range for the user.

The architecture explored in this thesis uses a bandpass sigma-delta modulator to perform an analog to digital conversion at an intermediate frequency in the receiver. This architecture takes advantage of recent advances in very large scale integration ($\sqrt{\text{VSLI}}$), by allowing as much signal processing to be performed digitally as possible. This permits the possibility of a high level of integration resulting smaller size and lower costs. This receiver is a good candidate for use in digital demodulation, and can also be used for FM demodulation required by AMPS, by closing the loop on the circuit to form a phase-locked loop (PLL). This eliminates the need for much of the extra digital circuitry. Simulations are performed on the closed loop PLL receiver, and are verified with bench measurements. A design is presented for using the architecture in an AMPS radio.

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List of Symbols and Abbreviations

B	modulation index of a frequency modulated signal
$\Sigma-\Delta$	sigma delta
BW	bandwidth of information signal
H(s)	closed loop transfer function of a phase-locked loop
PLL	phase-locked loop
FM	frequency modulation
BP- $\Sigma\Delta$	bandpass sigma-delta
IF	intermediate frequency
DSP	digital signal processing
LNA	low noise amplifier
VCO	voltage controlled oscillator
LO	local oscillator
RF	radio frequency
A/D	analog to digital conversion
NTF	noise transfer function

MASH	multi-stage sigma-delta
$F(s)$	phase-locked loop loop filter transfer function
Q	filter quality factor
AGC	automatic gain control
FPGA	field programable gate array
ACI	adjacent channel interference

1.1 Introduction

Today's markets for wireless products continues to grow at a substantial pace. In 1996, market surveys showed that over 20,000 users were joining the cellular market every day [Raz96]. Competitive market pressures continue to demand handsets with lower power consumption (for longer battery life), small size, better quality, and at lower cost. To meet these demands, research has focused on new components and architectures that reduce power consumption, improve the system level performance, and have a higher level of integration [Law98],[Abi95].

Early cellular systems provided voice service to users using FM transmission. In North America, a unified standard called the Advanced Mobile Phone Standard (AMPS) was used, while other countries used different standards. Most notably, there were several different, and incompatible, systems deployed in Europe [Goo91]. The needs for improved system capacity, and implementation of new (digital) services helped to motivate the creation of second generation digital standards. In Europe, the unified standard of GSM was created to ensure compatibility for users from country to country. However, in North America, several different incompatible digital schemes emerged, which fragmented the market. This has created the need for handsets which are capable of supporting multiple standards. This thesis exams a possible architecture which provides a backward compatibility with the older standards based on current work in new architectures.

One architecture introduced for a wireless receiver uses a bandpass sigma-delta modulator

which performs an analog-to-digital conversion of the signal at an IF frequency, and offers several advantages [NST97]. Digital circuits have better noise immunity, and do not suffer the same adverse affects to component mismatch, as compared to analog circuits, and as such have a strong advantage for use in VLSI circuit implementations. The final downconversion from the IF to baseband can be performed with no I/Q mismatch, and filtering done with DSP can have better stopband attenuation and better controlled phase performance, which is important for intersymbol interference. Since the backend DSP can be programmed to demodulate many different modulation standards, this architecture would be ideal for a multi-mode digital radio receiver.

Even with the improved capacity and new services offered by digital radio, there still exists a need for backward compatibility with the older FM standards, especially in North America. The backwards compatibility ensures that the user will have voice service in areas where digital service is not available. Even as the digital service matures, it will not likely have the same coverage as the older analog service, due to the cost of the infrastructure. The newer digital services are economically feasible in urban centres, where there are enough users to pay for the service. In outlying areas, it will take longer (if ever) to get digital service. Figure 1.1 is representative the digital service coverage for part of Canada (copyright Bell Canada, 1999), and shows that the digital coverage is concentrated around urban centres, while most of the outlying areas are serviced by the older analog system. The backwards compatibility in digital phones is provided by additional software and added computational complexity, or more frequently simply the addition of a separate hardware FM demodulator, both of which add time and cost to the development of the dual mode phone.

Figure 1.1 Cellular Coverage Map South Ontario/Quebec

In this thesis, an alternate architecture for demodulation of an FM signal, based on the bandpass sigma-delta digital radio is explored. For digital demodulation, the radio operates like a single-IF receiver performing the A/D conversion at the IF. For FM demodulation, rather than using separate hardware or DSP, the output is fed back to the frequency synthesizer, and the receiver is operated as a PLL. Rather than having a second path for the analog FM receiver as is typically done [KHG93], this architecture reuses the same parts. This can help to reduce parts count (not needing a separate FM demodulator), and reduce power consumption (can turn off the DSP part of the receiver). This receiver is both modeled, and tested on the bench using previously designed components at Carleton, including the fre-

quency synthesizer [FIL97] and the bandpass sigma-delta modulator [SWA96].

1.2 Thesis Outline

Chapter 2 provides some relevant background information. Performance considerations for radio receiver in a mobile environment background are discussed, and background information on phase-locked loops, sigma-delta modulators, and FM modulation is also presented. Chapter 3 introduces the architecture, describes the operation and presents models for simulation, and discusses implementation considerations. Chapter 4 has simulation results and laboratory measurements. Focus of the observations is on the static performance of the loop including hold range, sinusoidal and frequency step response, and on the effects of adjacent channel interference.

CHAPTER 2 Receivers for Mobile Communications

In this chapter, some background information relevant to this thesis will be presented. The discussion will begin with some communications fundamentals for wireless mobile communications systems, followed by communications standards with emphasis on techniques to overcoming some of the problems in a mobile wireless environment. The next section introduces receiver architectures for wireless mobile applications. This is followed by an overview of oversampled data converters, which are used throughout the thesis. In the final section phase-locked loops (PLL's) are presented, which are the basis of the proposed architecture in this thesis.

2.1 Communication Fundamentals

The purpose of any communication system is to transfer some type of information (such as voice, video, data, etc.) from a source to a destination (which may also be referred to as a sink). The fundamental limits as to how much information can be transmitted are determined by the available bandwidth, and the relative noise and signal powers in the system, as summarized by Shannon's information theorem [Sha49]. Wireless mobile applications have many unique problems beyond noise that further impair performance of the communication system. This section discusses communication fundamentals for wireless mobile communication systems, with a focus on these problems.

2.1.1 Noise

Noise is an unavoidable impairment to system performance in any communication system, and is caused by sources in the channel and in the electronics of the receiver. The effect of noise is to decrease the intelligibility of voice in analog systems, or cause receivers to make errors detecting bits in digital systems. Noise can be modeled by a random process, $n(t)$, and the noise power in the communication system is given by its power spectral density (PSD). In general, for a signal $s(t)$, the PSD is defined as:

$$P(\omega) = \int_{-\infty}^{\infty} R(\tau) e^{-j\omega\tau} d\tau \quad (2.1)$$

where $R(\tau)$ is the autocorrelation function of the signal $s(t)$, given by:

$$R(\tau) = \int_{-\infty}^{\infty} s(t)s(t+\tau)dt \quad (2.2)$$

Although generally the PSD of noise can be frequency dependent, noise found in the channel is usually modeled as a uniform PSD up to very high frequencies (and is referred to as “white”). The thermal noise floor of the receiver is -174 dBm/Hz for a 50 Ω system, which sets a limit on the performance of communications systems. Since the PSD gives the power per unit bandwidth, the total noise power in a channel bandwidth is simply given by:

$$P_n = \int_{f1}^{f2} N_o df = N_o \cdot BW. \quad (2.3)$$

The signal to noise ratio (SNR) is a measure of the ratio of the power of the desired signal to the noise power in the band of interest. The minimum acceptable SNR depends on the application. For transmission of speech, the minimum acceptable SNR for intelligibility is about 12 dB [SS95b].

2.1.2 Cellular Systems and Interference

The cellular concept was introduced to provide high capacity for using limited spectrum by frequency reuse over a (relatively) large area. This allows service providers to provide access to the wireless network for an arbitrary number of users over a given coverage area. The principle of cellular systems involves splitting up the number of available channels into groups, such that the channels in each group are separated as far apart (spectrally) as possible. Each group of frequencies is assigned to a geographical cellular coverage area, called a cell, to provide access for the user. The cells are assigned (arranged) such that two identical frequency groups are never placed adjacent to one another. Figure 2.1 shows a cluster of 7 cells (a), and the arrangement of clusters, so that cells with the same frequency set are separated by distance D (b).

Figure 2.1 Cellular Arrangement and Distance Between Cells

There exists a design trade-off in the selection of D , because as decreasing D increases the system capacity (effectively giving more channels/km²), the decrease in D also increases the co-channel interference which exists due to frequency reuse in the nearby cell with the same channel allocation [Ham97]. There is no way of removing or filtering this source of interference, and must be dealt with at the system design level to ensure adequate signal

quality.

As in all wireless systems, the cellular receiver must contend with adjacent channel interference (ACI), which originates from both users in the same cell, and from users in adjacent cells. The worst case ACI occurs when the receiver is near the edge of the cell, and there is another user transmitting in another cell using an adjacent channel. This gives rise to a problem known as near-far effect, when the receiver is trying to receive a weak signal (due to distance) in the presence of a strong ACI. The ACI can cause overload and distortion in the radio receiver in the IF and baseband stage, and degrade the desired signal. The adjacent-channel interferer can be removed by filtering, but it is quite difficult to build the narrow bandwidth filters required at higher frequencies. This must be addressed with the receiver architecture, to ensure that the worst case ACI has been adequately dealt with.

2.1.3 Line of Sight Issues

Yet another problem arises because line of sight transmission (LOS) is not possible. Surrounding obstacles cause the received signal to be the summation of several reflections and diffractions of the transmitted signal, arriving at the antenna with different phases and amplitudes. The summation of these received signals causes a random variation of the strength of the received signal that is dependent on the location of the receiver. This is referred to as slow fading or large scale fading, and can cause variations of up to 40 dB in the received signal [Rap96]. Receivers must budget for this fading in their design.

Mobile receivers also experience fading due to their own motion. This phenomenon is referred to as fast fading or small-scale fading, and not only does it cause variations in the signal strength, but these variations happen quite fast. For transmit frequencies in the typical range of cellular systems (around 1 GHz), and typical cruise speeds of an automobile, the signal strength would change several hundreds of times per second. The net effect of

fast fading is that the rapidly changing amplitude and phase of the signal paths tends to cause increased intersymbol interference (ISI) in the channel, causing errors in the received signal [Rap96].

2.2 Receiver Architectures

The purpose of the receiver is to recover the transmitted information over the channel impairments discussed in the previous section. In this section, different architectures will be discussed, and some strengths and weaknesses pointed out. There are many specifications which a mobile wireless receiver must meet in order to be successful.

Generally, a receiver consists of a low noise amplifier (LNA) at the front end and at least one downconversion stage. The LNA is required to increase the signal level while adding as little additional noise as possible. Noise added by successive stages is diminished by gains in previous stages. A measure of the noise added by a stage is the noise figure, defined for a 50 Ω source input, as:

$$NF = 10 \log \left(\frac{SNR_{in}}{SNR_{out}} \right) \quad (2.4)$$

Another important figure of merit for a receiver is the sensitivity, which is a measure of the minimum strength signal detectable by the receiver. The maximum signal strength (amplitude) receivable is limited by the linearity of the receiver. The dynamic range is defined as the difference between the minimum detectable signal and the maximum signal before overload and distortion. This specification is very important in determining how large an adjacent channel interference can be tolerated by the receiver before degradation of signal quality.

For mobile receivers, performance in a hostile channel is just one of the performance re-

quirements which must be met. Low power improves battery life for the receiver, and indirectly affects weight. Cost of the receiver is very important in a consumer market. Thus, it is preferred to have as simple a receiver as possible, and to reduce the number of expensive off-chip components (and to minimize the cost of the chips themselves). In the following sections, receiver architectures will be presented and strengths and weaknesses will be discussed.

2.2.1 Direct Conversion

The simplest receiver would mix the RF signal directly down to baseband. As there are no intermediate frequencies in the downconversion, this is referred to as a zero-IF receiver.

Figure 2.2 Direct Conversion Receiver Architecture

Although this is the simplest receiver architecture in terms of number of parts, it does have some problems. Due to the limited gain of the LNA and mixer, the signal coming out at baseband is rather small. This signal is sensitive to noise in the electronics, especially $1/f$ noise. Simply adding gain will not help, as adjacent channel interferers will saturate the back end, destroying the signal. The adjacent channel interferer must be filtered out, but at the RF this requires filters with very high Q values, which are not practical.

DC offsets are yet another problem, caused by self mixing in the mixer. Self mixing occurs when the strong LO signal feeds into the RF path through parasitics in the mixer. This LO is then reflected back to the mixer, and mixes with itself down to DC. This DC offset corrupts the received signal, and may change the biasing or saturate further circuit stages.

Even with these problems, direct conversion is the simplest architecture, requiring only one external filter before the LNA. This architecture is already used in low-cost receivers such as pagers, and with the promise of high integration, research is being done in direct conversion architecture towards a completely integrated cellular radio.[Abi95] The future popularity and use of this architecture remains unclear.

2.2.2 Heterodyne Receiver

A possible alternative to a zero IF architecture is to have intermediate stages, where adjacent channel interferers can be filtered out with lower Q filters, while the signal is amplified without distortion. The heterodyne receiver consists of several mix-down stages. The advantage of such an architecture is the specifications on the filters are relaxed, at the cost of more hardware (mixers, local oscillators and IF filters). A typical architecture might have

the following form:

Figure 2.3 Heterodyne Receiver Architecture

This receiver mixes the RF down through two IF frequencies before the information is brought down to baseband, where it can be demodulated. Unlike the zero IF architecture, there is no DC offset problem from self-mixing. The overall gain to baseband can be much larger, reducing the problem with $1/f$ noise. This is also better at receiving a small desired signal in the presence of interferers.

Heterodyne receivers do have disadvantages. There are several more parts, increasing power consumption and cost. The heterodyne receiver must also contend with image frequencies, which become another interferer to the system. Where a low IF makes suppression of adjacent channel interferers easier, it becomes more difficult to filter out the image. Because of this trade-off, it is common to have several IF stages to relax the filter requirements for both adjacent channel interference filtering and image filtering.

Some alternatives have been presented to minimize the image problem. For example, an image reject mixer can be used to perform image rejection. This method makes use of the

properties of the in-phase and quadrature components of the signal (I and Q), and is sensitive to mismatches. If the I and Q LO signal are not perfectly orthogonal (i.e. I and Q not at 90 degree phase difference), unwanted feedthrough of the image signal will occur. Mismatch cannot be avoided in high frequency designs, and image rejection over 30 dB is hard to achieve. Another alternative involves using an image reject notch filter, rather than relying only on the bandpass filter for the image rejection [MC98].

2.2.3 Direct Digital Conversion

One proposed alternative is to directly digitize the RF signal, and perform all functions (including channel selection, filtering, mixing, etc.) in DSP [Too97]. As DSP can overcome problems inherent to analog circuits like circuit mismatch and nonlinearities, can provide noise immunity, and provide better filtering, it is desirable to perform the A/D conversion as close to the antenna as possible to minimize the negative effects of analog processing. However, there are several problems with the design of the converter. To sample a cellular signal at the RF carrier frequency, the sampling rate needed is in the Gbit/sec range. The required dynamic range must include not only the dynamic range of the required signal, but also include fading effects and overhead for adjacent channel interference, which can approach a required dynamic range of up to 120 dB, or 20 bits of converter resolution.

A possible compromise is to do the conversion at the IF stage. One proposed architecture is to perform the A/D conversion at the IF using a bandpass sigma-delta (Σ - Δ) modulator [JSF93], [Vie95], [SS95a]. Bandpass Σ - Δ modulators effectively oversample the baseband information on the IF carrier to provide a high resolution A/D converter. More detail is given on the operation of Σ - Δ modulators in a later section. A receiver block diagram is

shown below:

Figure 2.4 Single-IF Bandpass Sigma-Delta Receiver Architecture

The single IF stage makes the filtering requirements more difficult than a multi-stage heterodyne architecture. However, the required Q of the IF filter can be relaxed, if the bandpass $\Sigma\text{-}\Delta$ modulator has enough dynamic range to handle adjacent channel interference. The IF bandpass filter is also required to act as the anti-alias filter for the bandpass $\Sigma\text{-}\Delta$ modulator.

The choice of sampling frequency is important in optimizing the architecture. If the sampling rate is chosen at four times the IF frequency, this helps to simplify the second down-conversion stage to baseband. The downconversion is accomplished by multiplying the digital IF bitstream by an LO at the IF frequency. If the data rate is at $1/4$ the clock frequency, then the LO has a convenient digital form. A sine or cosine wave, sampled 4 times per period, can be represented by a zero crossing, its maximum, the next zero crossing, and finally the second zero crossing. Thus, a cosine wave can be represented by the digital sequence 1, 0, -1, 0, and the sine wave can be represented by 0, 1, 0, -1. For an I/Q downcon-

version, this provides two perfectly separated quadrature signals and a mixer with just a minimum of digital logic. The multiplication can then be performed by an XOR gate, which greatly simplifies the mixer implementation.

2.3 Modulations Methods

Modulation is the process of changing the properties of a carrier signal to represent the content of an information signal. In RF modulation, the transmitted signal is no longer at base-band (centred around DC), but at higher frequencies, with its spectrum centred around a carrier frequency. A modulated signal can be expressed as:

$$S(t) = A(t)\cos(\omega_c t + \theta(t)) = \text{Re}\{A(t)e^{j(\omega_c t + \theta(t))}\} \quad (2.5)$$

There are really only two degrees of freedom in the carrier for the modulating signal to change: the amplitude and the phase. The amplitude and phase can be represented by two orthogonal vectors known as the in-phase and quadrature components, or I and Q components, respectively. Thus, the previous equation can be rewritten as:

$$S(t) = x(t)\cos(\omega_c t) + y(t)\sin(\omega_c t) \quad (2.6)$$

where $x(t) = A(t)\cos\theta(t)$ and $y(t) = A(t)\sin\theta(t)$ give the in-phase and quadrature components.

Modulation has several important properties in mobile communications. By using different carrier frequencies, several users can share the transmission channel. Modulation at high frequencies also reduces the antennas to a reasonable size for hand held radios.

Information signals can be categorized into two broad types: analog, where the information

is represented by bandwidth limited, continuous time functions; and digital, consisting of series of sampled, quantized symbols that represent the information. Older communication systems used analog communications systems due to their relative simplicity. Most recent communication systems are based on digital transmission, which has inherent advantages in noise immunity, and in transmission bandwidth when using data compression techniques. Since FM modulation is of importance to this thesis, it will be covered in some detail in the next section.

2.3.1 Frequency Modulation

In frequency modulated systems, the amplitude of the carrier is kept constant while the frequency is changed as a function of the amplitude of the information signal. Thus, the amplitude of the modulating signal is carried by the instantaneous frequency of the modulated carrier, while the frequency is carried in the rate of change of the instantaneous frequency.

The instantaneous frequency has the form:

$$f_{inst} = f_c + k_f m(t) \quad (2.7)$$

The modulated signal has the form:

$$S_{FM}(t) = A_m \cos \left(2\pi f_c t + 2\pi k_f \int_{-\infty}^t m(u) du \right) \quad (2.8)$$

Although the instantaneous frequency is a linear function of the modulating signal, the modulated carrier is a nonlinear function of $m(t)$. More specifically, the time varying phase of the carrier is the integral of the modulating signal. Thus, a general formula for the bandwidth of an FM modulated signal cannot be obtained. Typically, the bandwidth for an FM signal depends on the frequency deviation of the carrier. Carson's Rule [Rap96] can be

used to approximate the total transmitted bandwidth, and states that the bandwidth containing 98% of the signal power is given by:

$$BW = 2(\beta_f + 1)f_m \quad (2.9)$$

where β_f is the modulation index, which defines the relationship between the information signal amplitude and the bandwidth of the transmitted signal:

$$\beta_f = \frac{k_f A_m}{BW} = \frac{\Delta f}{BW} \quad (2.10)$$

If the modulation index is small ($\beta_f < 0.5$), the modulation is said to be narrow band, and the bandwidth approximately the same as AM. If the modulation index is larger, then the modulation is called wideband. Since FM is a nonlinear modulation scheme, an exact expression of the spectrum for a random source is not obtainable. For a single tone modulating signal of frequency ω_m , the spectrum is given by a summation of tones spaced at integer multiples of ω_m , with magnitude given by the n-th order Bessel function [KBR80]:

$$\begin{aligned} F_\beta(t) = & A_m \{ J_0(\beta) \cos \omega_c t \\ & + J_1(\beta) [\cos(\omega_c + \omega_m)t - \cos(\omega_c - \omega_m)t] \\ & + J_2(\beta) [\cos(\omega_c + 2\omega_m)t - \cos(\omega_c - 2\omega_m)t] \\ & + J_3(\beta) [\cos(\omega_c + 3\omega_m)t - \cos(\omega_c - 3\omega_m)t] \\ & + J_4(\beta) [\cos(\omega_c + 4\omega_m)t - \cos(\omega_c - 4\omega_m)t] \\ & + \dots \} \end{aligned} \quad (2.11)$$

The first seven Bessel functions for a modulation index of up to 10 in shown in Figure 2.5 :

Figure 2.5 Bessel Functions of Order One Through Seven

Increasing the modulation index (and hence bandwidth) actually improves the SNR performance of the FM signal, as long as the input SNR is above a certain threshold. Assuming the noise is small compared to the signal, only the quadrature component of the noise impairs the SNR (recall that FM is a constant envelope modulation scheme, with ideally no variation of the amplitude). For a demodulator to recover the information signal, it must take the derivative of the incoming signal (and noise). For white noise, the noise seen after the demodulator is then the derivative of the incoming noise, as shown in Figure 2.7. For the signal sufficiently larger than the noise floor, it can be shown that the improvement in SNR over amplitude modulation is $3\beta^2$ [Ham97].

Figure 2.6 Noise Power Spectral Density in FM Demodulation

FM demodulation can be implemented in a number of ways. One method is by using a frequency dependent circuit (such as a tuned circuit), which can convert changes in frequency to changes in voltage. Another method is by using a zero-crossing detector to demodulate the output. Another popular method is by using a phase-locked loop (PLL). PLL's are covered more in Section 2.4.

2.3.2 Mobile Radio Standards: AMPS/IS-54

This section discusses the Advanced Mobile Phone Standard (AMPS), the first widespread North American cellular standard. The standard uses wideband FM for voice, and FSK for transmission of control information (i.e., call setup, etc.). A nominal 1kHz reference input tone of nominal volume should generate a 2.9 kHz peak frequency deviation. Furthermore, the specification states that modulation products outside 20 kHz from the carrier shall not exceed 26 dB below the unmodulated carrier, and products greater than 45 kHz from the carrier shall not exceed 45 dB below the unmodulated carrier. This is to help minimize the adjacent channel interference between users.

Multiple access is provided through frequency division multiple access (FDMA), where the

spectrum is broken down into 832 channels, each channel 30 kHz wide, allocated as shown in Figure 2.7 . AMPS uses frequency division duplexing (FDD) using a forward and reverse channel for two way communications, with the forward and reverse channels fixed at a 45 MHz offset. There are 42 control channels in each the forward and reverse channel, used to send control messages.

Figure 2.7 Allocation of Forward and Reverse Channels in AMPS

Baseband processing is used to help improve the quality of the transmitted signal. A block diagram of this is shown below in Figure 2.9.

Figure 2.8 AMPS Baseband Processing

The compander compresses the amplitude of the input signal 2:1, to give a wider dynamic range and produce a quieting effect during a speech burst. The received signal must then be expanded to remove this distortion. Next, a pre-emphasis filter is used to help improve the

perceived quality of the transmitted speech signal. Pre-emphasis increases the power in the higher frequency content of speech, which may be lost in the noise since the noise power of speech decreases with frequency [SS95b], and in FM, the noise PSD increases with frequency as shown in Figure 2.7. For AMPS, this filter should have a highpass response of 6 dB/octave between 300 Hz and 3 kHz. Again, the receiver must use a de-emphasis filter to undo the pre-emphasis in the transmitter.

To prevent transmitted energy outside the user's channel, a deviation limiter is used to limit the maximum deviation to 12 kHz. The postdeviation limiter filter is also used to help limit emissions outside the channel bandwidth, and is involved with handshaking signals used to setup and maintain calls with AMPS.

2.4 Phase Locked Loops

As described before, a phase locked loop (PLL) is a negative feedback loop that follows the phase of an input signal. A block diagram of a PLL is shown below.

Figure 2.9 Block Diagram of Phase Locked Loop

When the loop is locked, the loop can be linearly modeled to predict the behavior of the

loop. This requires a linear model of each component. The first element to be considered is the phase detector. There are several phase detectors available for analog and digital loops, but each provide an output (error) voltage that is proportional to the phase difference of the inputs. Assuming a linear phase detector, the transfer characteristic for the phase detector is then just $k_d\theta_e(s)$, where k_d is in volts/rad. The loop filter transfer function will depend on the type of filter required, and will be given by $F(s)$. The VCO gives an output frequency proportional to the input voltage applied. Since the phase is the integral of the frequency, the transfer function of the VCO is given by k_v/s , where k_v is in rads/volt.

The general linearized transfer function of a PLL is defined as:

$$H(s) = \frac{\theta_v}{\theta_i} = \frac{k_d k_v F(s)}{s + k_d k_v F(s)} \quad (2.12)$$

The error function is defined as:

$$1 - H(s) = \frac{\theta_e}{\theta_i} = \frac{s}{s + k_d k_v F(s)} \quad (2.13)$$

It can be seen that the loop filter determines the characteristics of the PLL. Usually, the loop filter is a first-order low-pass filter (LPF). Since the order of the loop is one order higher than the order of the filter, a first-order LPF will result in a second-order PLL. For a passive LPF with a single pole $F(s) = 1/(1 + s\tau)$, the general transfer function is given by:

$$H(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (2.14)$$

where $\omega_n^2 = k/\tau$, k is referred to as the open loop gain, and $2\xi\omega_n = 1/\tau$. This notation is taken from control systems engineering, and is convenient in investigating the transient behavior of second order systems. Of interest is the transient response to a frequency step at the input of the loop. This final steady-state condition of the loop, as well as the settling time, can be

determined from the PLL transfer function by applying a frequency step input to the transfer function. Since the transfer function is in terms of phase, a frequency step $\Delta\omega$ at time zero appears as an input of $\theta_i = \Delta\omega/s^2$ in the Laplace domain. For a single pole LPF, the LPF output becomes:

$$u = \frac{\Delta\omega \cdot k_d}{s(\tau s^2 + s + k_d k_v)} \quad (2.15)$$

The final value theorem can be used to find the steady state final values. Of interest is the phase error, because, if the phase error exceeds the range of the phase detector, the PLL will lose lock (to be discussed later). Also, the transient settling time can be determined with this equation.

Another important behaviour of the PLL is its response to an FM signal, when the PLL is being used for FM demodulation. Using notation from Section 2.3.1, an FM input to the loop has the form:

$$\theta_i = 2\pi \frac{k_f}{k_m} \sin \omega_m t \quad (2.16)$$

For a PLL in lock, the output from the LPF is used to modulate the VCO, and thus represents the modulating signal. The PLL response to FM modulation is:

$$u = \frac{\Delta\omega \cdot k_d}{s(\tau s^2 + s + k_d k_v)} \quad (2.17)$$

Linear models are also useful for determining stability of the closed loop. The PLL must obey Barkhausen's criterion, which states that for negative feedback systems, the open loop gain must be lower than 1 at 180 degrees (or π radians) of phase shift, or else it will oscillate. Stability analysis can be easily done by examining a bode plot of the open loop transfer function. The design of higher order loops is difficult, as each pole causes $\pi/2$ radians

of phase shift. Phase lead correction can be used for improving the stability

Normal operation for the loop is when it is in lock. However, it is very unlikely that the loop will start up in lock. The process of acquiring lock is called acquisition, and requires a non-linear analysis of the loop. Depending on the difference between the PLL initial frequency ω_o and the input frequency $\Delta\omega$, there are three different ranges of operation, as shown in Figure 2.10.

Figure 2.10 Relationship Between Hold, Pull-in, and Lock Range

When the PLL is not in lock, there is a frequency difference between the input and the VCO signal. This sum and difference frequencies appear after the mixer/phase detector, and the LPF filters out the sum frequency, leaving only the difference. This difference frequency is applied to the VCO, which FM modulates the VCO. This FM modulated signal is mixed with the input to provide the signal required to obtain lock.

The lock range is the range in which the PLL can achieve lock within one cycle (i.e. without cycle slipping). This is illustrated in Figure 2.11. If the instantaneous frequency of the VCO matches the input frequency, the loop generates the DC value required to achieve lock. The lock range is given by $\Delta\omega_L = k_d k_v |F(j\Delta\omega_L)|$ [Bes97]. If the initial offset is greater than the lock range, then the loop must go through a pull in process, as shown in (a). If the initial

frequency offset is less than the lock range, the PLL acquires phase lock within a cycle, as shown in (b).

Figure 2.11 Lock and Pull-in Range of PLL

The pull-in process is much slower than the lock-in process, and is described in [Bes97]. If the difference frequency is larger than the frequency deviation of the VCO, the mixer output will cycle slip, causing the VCO control voltage to oscillate. These oscillations are non-linear, and have a DC value which forces the VCO to move closer to the input frequency. It can take several cycles for the loop to lock in this case. The time required depends of the transfer function of the loop.

The hold range is a measure of the maximum tuning range of the loop, given that the loop is initially locked. If the input signal is outside of the hold range, the loop is unable to produce the required control voltage to the VCO to follow the input. This is caused by the phase detector not being able to maintain phase tracking between the input and VCO frequencies. In theory, the hold range is determined by the overall loop gain. Practically, the hold range is limited by the VCO tuning range.

2.5 Sigma-Delta Modulators

A $\Sigma\text{-}\Delta$ modulator is a feedback loop consisting of a filter (which can be continuous or discrete time), an A/D converter (modeled as a converter gain G , and quantization noise source Q_{in}), and a D/A converter which feeds the output back to the input. An intuitive way of understanding the operation of a $\Sigma\text{-}\Delta$ modulator can be obtained by looking at the negative feedback action. Negative feedback loops try to suppress any change at its input by supplying feedback back to the input. As it is the output of the loop that provides this feedback, this output must change, trying to cancel the input. Thus, a changing input to the modulator will cause the modulator's output to follow the input, hence the input signal can be thought of modulating the output bit stream, and the output signal Y_{out} appears as a digital representation of the input signal X_{in} . A block diagram for a typical $\Sigma\text{-}\Delta$ modulator is shown below in Figure 2.13.

Figure 2.12 Block Diagram of a Sigma-Delta Modulator

Sigma-delta modulators often use single bit quantizers (comparators) as the A/D converter. Since the overall linearity is determined by the linearity of the A/D and D/A converter, using a single bit converter provides the possibility of having ideal linearity. Nonlinearity in converters occurs when the converter step size is not uniform, but changes between the quantization levels. The converter can be modeled as a straight line, with a gain propor-

tional to the slope of the straight line. Nonuniform quantization levels force this line to deviate from straight, causing the nonlinearity. Since the single bit converter has only two levels, the slope between those two levels must form a straight line (hence no nonlinearity). The output of this converter can be written as:

$$Y_{out} = \frac{X_{in}H(s)}{1 + H(s)} + \frac{Q_{in}}{1 + H(s)} \quad (2.18)$$

High converter resolution is gained through two mechanisms: sampling at frequencies much higher than the Nyquist rate (oversampling), and by noise shaping. For a “busy”¹ input to the converter, the quantization error can be assumed to be uncorrelated to the signal, and approximated as a white noise source with its energy distributed from DC to half the sampling rate. The total noise power in the signal bandwidth is then just the fraction of the signal bandwidth to half the sampling bandwidth, or the inverse of the oversampling ratio $f_s/2f_{in}$. Hence, doubling the oversampling ratio provides a 3 dB improvement in the signal to quantization noise ratio, or about 0.5 bit of resolution.

From Equation 2.18, it can be seen that the signal transfer function and noise transfer function are different for a given selection of $H(s)$. The signal to quantization noise ratio (SQNR) can be improved even further by selecting a filter which will pass the signal information, but change the noise PSD from uniformly flat to having a notch in the signal bandwidth, hence pushing the noise power away from the signal bandwidth. For example, a pole in the filter at DC (an integrator) will be transformed to a zero in the noise transfer function at DC, reducing the quantization noise in band for a baseband signal. It can be shown for a filter of order L with L poles at DC, the noise in the signal bandwidth is approximately [NST97]:

1. “busy” is defined as a signal where the modulator does not fall into limit cycles, as in the case of a DC input to a first-order $\Sigma\text{-}\Delta$ modulator.

$$n_o = q_{rms} \frac{\pi^L}{\sqrt{2L+1}} \left(\frac{2f_{in}}{f_s} \right)^{L+0.5} \quad (2.19)$$

where q_{rms} is the rms quantization noise error, $\Delta/(\sqrt{12})$, where Δ is the distance between quantization levels. Note that the noise shaping transfer function does not need to place all zeros at DC, but can spread them out to improve the SQNR over a wider input signal bandwidth [NST97]. Also, the signal need not be at baseband, but can be at an IF frequency, and the noiseshaping zeros can be placed to shape the noise away from a narrow bandwidth at that IF also, as in the case of the bandpass Σ - Δ converter [SS95a].

Although the use of a one bit quantizer makes for a very linear converter, the quantizer has a gain dependent on its input, and becomes a nonlinear element in the loop, making stability analysis very difficult (and generally not analytically possible) for high-order loops (above order 2). An alternative architecture, the cascaded (or MASH) Σ - Δ modulator uses a series of cascaded, lower-order (1st or second-order) modulators, and combines their outputs using the appropriate noiseshaping function, high-order noiseshaping can be obtained while guaranteeing stability. The only problems with the architecture are that the single-bit outputs must be summed to give a multi-bit output word (which may or may not be a problem), and that the architecture is sensitive to coefficient mismatches in the first stage converter of the cascade. By using an all digital architecture, there are no component mismatches, and the noise shaping is ideal. A block diagram for cascaded first order modulators is

shown in Figure 2.13.

Figure 2.13 Block Diagram of a MASH Sigma-Delta Modulator

2.6 Conclusions

This chapter began with a discussion of issues in radio receivers, and discussed both different architectures for those receivers and various standards for communications (specifically FM) they need to implement. The second part of Chapter 2 presented some important building blocks for the proposed receiver architecture, which will be presented in Chapter 3.

3.1 Introduction

The proposed architecture is shown in Figure 3.1. The analog/demodulation switch is open for digital demodulation, and the receiver uses the bandpass $\Sigma\text{-}\Delta$ to perform the A/D conversion at the IF, and quadrature downconversion is performed in the digital domain. This I and Q signal are then sent to DSP for demodulation of the signal. When demodulation of an FM signal is desired, the switch is closed, and the phase information is used as a feedback signal back to the frequency synthesizer to operate the receiver as a heterodyne PLL.

Figure 3.1 Block Diagram of Proposed Receiver Architecture

This chapter discusses the operation of the loop, and presents models for both the understanding, and for use in simulation of the receiver. The first section discusses the operation of the heterodyne (or long) PLL. The following two sections provide an overview and describe the operation of the frequency synthesizer and bandpass Σ - Δ , respectively. The final section describes the overall operation, and highlight important properties of the architecture.

3.2 Heterodyne PLL

When a conventional PLL is locked, the mixer produces a sum and difference frequency at its output, where the difference is mixed down directly to baseband. The sum frequency is removed by filtering, and the DC component provides a tuning voltage for the VCO to keep the loop locked.

The heterodyne PLL operates in a similar way, but rather than mixing down to baseband, the first mixer mixes down to an IF frequency. For a PLL input of $A \cos(\omega_{rf} + \theta)$, and a VCO output of $B \cos(\omega_v + \phi)$, the output from the initial mixer can be written as:

$$A \cos(\omega_{rf} + \theta) B \cos(\omega_v + \phi) = \frac{AB}{2} [\cos(\omega_{rf} + \omega_v + \theta + \phi) + \cos(\omega_{rf} - \omega_v + \theta - \phi)] \quad (3.1)$$

This signal is passed through the bandpass filter, with its passband centred around the IF frequency. This filter will remove the sum frequency component, leaving only the difference frequency. This component is then mixed down to baseband by the digital mixer. For a digital mixer LO input of $\cos(\omega_{lo} + \varphi)$, the resulting signal after mixing to baseband is:

$$\begin{aligned}
& \cos(\omega_{lo} + \varphi) \frac{AB}{2} \cos(\omega_{rf} - \omega_v + \theta - \phi) = \\
& \frac{AB}{4} [\cos(\omega_{rf} - \omega_v + \omega_{lo} + \theta - \phi + \varphi) + \\
& \cos(\omega_{rf} - \omega_v - \omega_{lo} + \theta - \phi - \varphi)]
\end{aligned} \tag{3.2}$$

Again, if the high frequency components are filtered out, the result is simply the difference frequency, with the total phase difference around the loop. If the resultant frequency offset after the first mixer, $\omega_{rf} - \omega_v$, is the same as the LO frequency, then the signal after the second mixer is a DC term proportional to the phase difference between the input RF signal and the phase of the reference LO and VCO. Assuming the LO and VCO phases are derived from the same source (and stay locked relative to each other), the LO phase is just an offset, and the two mixers combined appear as a phase detector. Where in a normal PLL, the RF and VCO must be at the same frequency to be phase locked, in the heterodyne PLL the RF and VCO must be offset by the LO frequency to be locked. Since multiplication in the time domain is convolution in the frequency domain, the two FM inputs to the first mixer (the RF FM signal, and the VCO, which is FM modulated by the demodulated signal) mix together to produce the information signal AM modulated at an IF carrier frequency. As the heterodyne PLL tracks a drifting input, the overall phase changes so that the VCO may track the RF input, but the first IF stage must remain at a fixed frequency.

From the above discussion, it can be seen that the tuning voltage is represented by the magnitude of the carrier at the IF frequency, which is mixed down to the required DC value by the IF mixer. Although this helps with an understanding of the static (DC) operation, the IF stage presents a problem in understanding the small signal operation of the loop, which is important in determining loop response and stability. Since the mixer is a nonlinear element, it is difficult to write a Laplace transform for use in the small signal model. However, since the mixer does a frequency translation, it is possible to reduce the model to

an equivalent baseband model, thus replacing the IF stage with an baseband equivalent model [Ste97]. A bandpass filter can be derived from a lowpass prototype, such that the bandpass filter has a transfer function similar to the low pass filter, but symmetrical around the chosen centre frequency, as shown in Figure 3.2

Figure 3.2 Lowpass and Bandpass Filter Transfer Functions

Given the lowpass prototype transfer function, $F(s)$, the bandpass transfer function can be obtained by substituting for the lowpass complex frequency variable [Hue93]:

$$s = \frac{p^2 + 1}{p} \quad (3.3)$$

where s is the lowpass complex frequency variable, and p is the bandpass variable, normalized to a centre frequency of 1 radian/sec. This transformation shifts the poles and zeros from centred around DC to another centre frequency (while also creating the necessary complex conjugates). The envelope of the time domain response of the new bandpass filter resembles the time domain response of the lowpass prototype, as shown in Figure 3.3. The mixer and bandpass filter can be replaced with the lowpass filter equivalent for the small signal model of the heterodyne PLL, and will have the same response as the bandpass filter and mixer. Then the PLL small signal model becomes the same as for the regular PLL in Chapter 2. It should be noted that the small signal model does not take the nominal VCO frequency into account, which could conceptually be replaced with a VCO running at f_v .

$c_0 + f_{IF}$, so that the first mixer would mix down to DC.

Figure 3.3 Comparison of Lowpass Filter Response and Bandpass Response Envelope

3.3 Bandpass Sigma-Delta Modulator

As mentioned in Chapter 2, the Bandpass Σ - Δ modulator performs an A/D conversion directly to a narrowband signal centred around an IF frequency. After mixing down to base-band, the signal is a digital representation of the information at the IF, which, in the heterodyne PLL, happens to be an AM representation of the information signal. Assuming appropriate filtering for the image, the bandpass Σ - Δ modulator and digital mixer are simply an A/D converter, and can be modeled by a quantization noise source with a PSD appropriate for the noise transfer function. Note that since a bandpass filter is required, the noise transfer function has half the order of the bandpass equivalent. For example, the NTF of a fourth-order bandpass Σ - Δ , using two resonators in the loop filter to get zeros in the

NTF, will have a second-order slope (40 dB/decade), the same as a baseband second-order Σ - Δ modulator.

3.4 Frequency Synthesizer

In general, frequency synthesizers supply the required tunable frequencies within the radio architecture for up and downconversion. One emerging architecture for the frequency synthesizers is the fractional-n PLL, which has several attractive features, including good phase noise performance, fast acquisition time, high frequency resolution, and the potential for a high level of integration [RCK93], [PTS97].

Figure 3.4 Fractional-N Frequency Synthesizer with Dual Modulus Divider

The divider, which scales down the output frequency to match the reference frequency, acts as an attenuator for the VCO output phase (or a decimator in a digital PLL). As a starting point, consider the case where the divider is fixed so that it divides by a fixed integer N . The transfer function for the loop (with a first order LPF) becomes

$$\frac{\theta_v}{\theta_i} = \frac{N \cdot \omega_n^2}{N \cdot s^2 + 2N\xi\omega_n s + \omega_n^2} \quad (3.4)$$

In steady state (as s tends to zero), the VCO phase increases N times faster than the reference phase, providing an output frequency N times larger than the reference frequency. The divider can be viewed as an attenuation of the VCO phase in a continuous time sense, or a decimation in discrete time. The divider does affect the transient behavior of the loop, and also the stability.

For a fractional- n synthesizer, the frequency output is controlled by changing the divide ratio with a control bit stream, b_i . If the synthesizer is being used for channel select, the divider value is $N=n+p$, where n is the lowest (or when $p=0$) value of the divider, and p is the average (DC) of the channel select bit stream controlling the divider. For example, for a dual modulus divider 80/81, the divide ratio would be $80+p$, where p is the bitstream average (between 0 and 1). However, this ignores any possible noise contribution from the controlling bit stream, and doesn't take into account any ac component to the input bit stream (modulation or changing channel select, for instance), and a model in terms of input/output phases is required. Such models have already been developed, and two different derivations for a dynamic divider model can be found in [Don92] and [Bax95]. Although both arrived at the same model, the derivation presented here is similar to the derivation found in [Bax95]

To help understand the model, consider the typical divider waveforms are shown in

Figure 3.5.

Figure 3.5 Input and Output Waveforms for a Dual Modulus Divider

The first waveform f_{vco} represents the ideal phase output of the VCO with period T_v , where the j th rising edge of the VCO would occur at a time jT_v . The actual VCO would have a phase close to the ideal reference, but with an offset (or error) Δt_v . The time of the j th VCO cycle, $t_{v,j}$, in terms of the reference is then:

$$t_{v,j} = jT_v + \Delta t_{v,j} \quad (3.5)$$

The VCO phase can then be represented by:

$$\theta_{v,j} = \frac{2\pi}{T_v}(jT_v - t_{v,j}) = \frac{2\pi}{T_v}(-\Delta t_{v,j}) \quad (3.6)$$

Note that by this definition, a lagging VCO results in a negative phase error, which is what a PLL requires to generate a feedback signal [Bax95]. The time to the k th divider output, $t_{d,k}$, depends on the value of the divider, and is given by the VCO resampled (decimated) at the divided down rate, $t_{d,k} = t_{v,j}$, where $j = \sum_k (n + b_i)$ b_i is the control waveform value, and n is the lower divider modulus. The time to the k th divider output in terms of

the VCO input is then:

$$t_{d,k} = \sum_{i=1}^k (n + b_i) T_v + \Delta t_{v,k} \quad (3.7)$$

The phase at the divider output can then be written as:

$$\theta_{d,k} = \frac{2\pi}{T_v} (kT_d - t_{d,k}) = \frac{2\pi}{T_d} \left(kT_d - \sum_{i=1}^k (n + b_i) - \Delta t_{v,k} \right) \quad (3.8)$$

where T_d is the divider period. The value of the control bitstream b_i is changed much faster than the loop bandwidth of the PLL, hence the PLL will only track the average value of the control bitstream. When the loop is locked, the average divider value can be written as $N = n + p1$ where $p1$ is the average value of the bitstream and n is the lower divider modulus. Since $T_d = NT_v$, the equation for the divider output phase can be written as:

$$\theta_{d,k} = \frac{2\pi}{N} \left(kN - \sum_{i=1}^k (n + b_i) - \frac{\Delta t_{v,k}}{T_v} \right) \quad (3.9)$$

For proper PLL operation, the bitstream b_i must carry both the modulating information signal, Δ , and a DC error voltage $p1$ to lock the loop, or $b = p1 + \Delta$. Substituting this into the equation for the divider phase, we have:

$$\theta_{d,k} = \frac{2\pi}{N} \left(\theta_{v,k} - \sum_{i=1}^k \Delta_i \right) \quad (3.10)$$

The block diagram for the divider is shown in Figure 3.6 .

Figure 3.6 Block Diagram of a Multi-Modulus Divider

To gain an understanding of how the model works, consider Δ is simply a DC value on the input to the divider. The constant value will accumulate in the integrator, adding to the VCO phase $\theta_{v,k}$. For the loop to remain in lock, the VCO output phase must also increase, to keep the loop in lock. By using the average divider ratio N , the DC content of the controlling bit stream is included in the selection of the divider value, and a more accurate representation of the loop dynamics can be obtained. If the DC content of the bit stream is not known, then the divider must be replaced with the lower modulus n , and the divider input Δ must be replaced with b to include the DC information.

Since the summation appears as an integration in the discrete time domain, a block diagram

for the divider appears as follows:

Figure 3.7 Frequency Synthesizer Model

where p_i is the information signal, and q_i is again the quantization noise. The PLL reference ref can be considered an analog ground (as the reference point for the ideal VCO signal). If the frequency synthesizer is to be used as a numerically controlled oscillator in the loop, the transfer function from the input p to the VCO output would be very useful. It is given as:

$$H_{FS}(s, z) = \frac{2\pi z^{-1}}{1 - z^{-1}} \cdot \frac{k_d k_v F(s)}{Ns + k_d k_v F(s)} \quad (3.11)$$

For frequencies below the sampling rate, or $f \ll f_s/6$, the discrete integrator can be replaced in the Laplace domain by an integrator $(\pi f_{ref})/3 \cdot 1/s$ [Bax95]. This is conceptually important in our application where the frequency synthesizer will be operated as a voltage controlled oscillator, with transfer function k_{vco}/s , multiplied by a transfer function $V(s)$

representing the lowpass filtering action of the PLL. The phase output of the PLL is then the desired output for an FM modulated signal, consisting of the carrier term and integral of the information signal, attenuated by the loop gain of the PLL.

Although the analysis in [Don92] comes to the same model for the divider as [Bax94], the [Don92] analysis depends on an approximation from a Taylor's series to linearize the divider. This approximation depends on the AC (modulating) component of the divider controller to be much smaller than the average divider value, N . This assumption is valid in the case here, where the effective divider value is a divide by 80/82. No more consideration to the linearity of the frequency synthesizer as a VCO is given in this thesis, although this may be an area for future research.

The final topic to discuss is the generation of the control bitstream, b_i . Since the changing of divider moduli also appears as an equivalent step in the reference frequency, the spectral properties of the bitstream are very important in the noise performance of the loop. The use of a sigma-delta modulator allows a control bitstream to be generated which sufficiently randomizes the bits to reduce tonal behavior (for higher order modulators), and moves most of the quantization noise to outside the loop bandwidth, where it can be filtered out, reducing the jitter which appears in the output phase. Single-bit sigma-delta modulators have a dynamic range limited by the saturation of their internal integrators, which puts a limit on the minimum/maximum density of zeros or ones out of the converter. Intuitively, if one desires a DC value of the bit stream to be 0.99 of full value, 99 out of 100 of the bits need to be one, which leaves no room for noise shaping. This puts a limit on the total tuning range of the synthesizer, depending on the dynamic range of the modulator. One possible solution that has been proposed is to use a modulus extension circuit (MEC) [Ken94] to extend the division factor; in [Ken94] from $n/n+1$ to $n/n+5$ as an example. This allows the single bit bitstream to control a larger divider range, so that only a fraction of the bit stream

dynamic range is required to control the desired divider ratio. Another alternative, used in this thesis, is to use a multibit (MASH) sigma-delta modulator, which produces a multi-bit output word to control the divider (rather than the single bit control bitstream). Since there was no restriction placed on the control bitstream content (other than positive integer), the model for the divider can be easily extended from the dual-modulus divider case to include multi-modulus dividers.

3.5 Complete FM Demodulator Model

All of the models can now be combined to produce the small-signal model of the overall PLL:

Figure 3.8 Model of FM Demodulator

There are several parameters which can be adjusted to vary the performance in terms of noise, bandwidth, etc. This section attempts to put some of these trade-offs into perspective. The open loop transfer function for the entire PLL is given by:

$$H_{OL}(s) = k'_d k'_v F'(s) \frac{\pi f_{ref}}{3s} \frac{kF(s)}{Ns + kF(s)} \quad (3.12)$$

where $k = k_d k_v$, the gain of the synthesizer. The value k'_d represents the forward loop gain, and combines the mixer, IF amplifier, and bandpass sigma-delta gain. It also includes a scaling factor for the A/D conversion of the bandpass Σ - Δ , as its output is a digital representation of the input, and hence a reference voltage must be included. The feedback gain k'_v represents a scaling factor at the MASH Σ - Δ input. The MASH Σ - Δ is used to control the divider in the synthesizer. The input to the MASH is a 16 bit word, but the output from the bandpass Σ - Δ is a single bit bitstream, and it is this single bit that is connected to only one of the input bits on the MASH Σ - Δ . When using the synthesizer as a VCO, the maximum frequency deviation is set by the input into the MASH Σ - Δ . If the full 16 bit word was used, the full scale deviation would be 20 MHz. The single bit output can only toggle one of the bits, so the full scale deviation is just a fraction of the 20 MHz, or $2^k / (2^{16} - 1)$, where the bitstream controls the k th bit. Note that the remaining unused bits on the MASH Σ - Δ are used for channel select, which will be covered in more detail in Chapter 4.

The delay caused by the digital circuits in the MASH, and the delay from the bandpass Σ - Δ modulator is very important to the open loop transfer function, as it can affect stability. A short time delay can be approximated as a parasitic pole [Cra94]:

$$e^{-s\tau} \approx \frac{1}{1 + s\tau} \quad (3.13)$$

This parasitic pole can be included into the overall loop filter, $F'(s)$. The open loop transfer function can be used to determine the stability of the system. The Bode plot for the receiver

is shown in Figure 3.9 .

Figure 3.9 Bode Plot for Open Loop Transfer Function for Overall PLL Receiver

The closed loop transfer function is given as:

$$H = \frac{k'_d F'(s)}{s + k'_d k'_v F'(s) V(s)} \quad (3.14)$$

where $V(s)$ is the transfer function of the frequency synthesizer.

The closed loop Bode plot is shown in

Figure 3.10 Bode Plot for Closed Loop Transfer Function for Overall PLL Receiver

For low loop gain, the system behaves as a first order PLL, with loop gain $kk'_dk'_v$. The closed loop gain is set by the VCO gain, $1/(k'_v)$. Since the maximum deviation is set by the feedback to the VCO input, this gain can be used to adjust the loop to accept either high or low deviation FM inputs. However, because of the trade-off of bandwidth to frequency deviation, the receiver will work only as a narrowband small deviation receiver, or wide-band large deviation receiver.

3.6 Frequency Planning and System Issues

The models presented are useful for determining the performance of the system. This section discusses some of the system design issues in integrating it within the communication system.

3.6.1 Frequency Planning

The first step of any receiver design is frequency planning. At minimum, this requires deciding the requirements for all filters in the system. For heterodyne receivers, this also requires deciding what intermediate frequencies should be used. The choice of IF frequency not only determines the filters required, but the frequency of the local oscillators/frequency synthesizers required for the system.

As mentioned earlier, the IF stage was introduced as a means to help improve the filtering of any adjacent channel interference. Since the filter Q is defined as the ratio of the centre frequency to the bandwidth, it appears to be desirable to have as low an IF as possible to relax the filter requirements while still providing the required adjacent channel interference filtering. However, selection of the IF frequency is not an independent design variable, but sets the location of the image at the front end of the receiver. Since the AMPS standard uses several narrowband channels, the receiver must be capable of using any channel which it is assigned. From Chapter 2, the total spectrum occupied by the reverse channels is 25 MHz.

The lower the IF is, the closer the image is to the desired band of interest. This makes it more difficult for the front end filters to remove the image, as they need a sharper roll-off. The IF must be at least larger than the bandwidth of the incoming bandwidth, for AMPS this is 25 MHz. As shown in Figure 3.10, the image frequency is two times the IF frequency

away from the desired frequency (as mixing produces sum and difference components). To ensure that all channels within the reverse link can be received, the bandwidth of the front end filter must be larger than 25 MHz. The difference between the LO and RF signal must then be greater than half that bandwidth, or 12.5 MHz. To ensure that the image lies outside of the reverse channel, the IF must be greater than 12.5 MHz. Of course, the higher the IF, the more relaxed the image reject filter requirements are.

Figure 3.11 Filter Requirements for Receiver

Although the IF filter is important in helping to determine the digital radio ACI performance, it will be shown in Chapter 4 that relying on dynamic range in the bandpass sigma-delta (followed by DSP to postfilter) is not applicable for this architecture, as the PLL will lock onto a strong ACI, which cannot be corrected for later on. As far as filter selection for the digital radio, the bandwidth required will depend on the standard, as the IF bandwidth must be as wide as the channel. The IF filtering could be performed with a SAW filter, but this would require more off-chip components, and the associated extra circuits and power for off-chip interfacing. There has been much work done with on-chip filters, but they are not capable of performing as well, mostly due to limited dynamic range, higher noise, and lower Q than achievable with a SAW [Tsi94],[FSW98]. At an IF of 50 MHz, AMPS would require a Q of nearly 1000, where on-chip continuous time filters are only capable of around 200. However, they may provide a useful solution in the future, especially with wideband digital standards.

Selection of the IF filter has a significant effect on the behavior of the loop. The first problem the IF filter may cause is instability. For a high Q , the filter will use many poles and/or zeros, which have the potential of causing a very large phase shift. Although this phase shift may appear at higher frequency, this tends to reduce the phase margin of the loop. Care must be taken in order to ensure that the corner frequency is sufficiently above the open loop unity gain bandwidth of the PLL receiver. A second problem which may occur is the possibility of false lock when using a high order IF filter [Far79],[Ste97]. When a PLL undergoes pull-in, the beat note that is created is both attenuated and phase-shifted while passing through the loop. Recall that for the PLL to demodulate FM, the two FM inputs (one from the source, the other from the VCO) must mix down to the baseband modulating signal.

For this radio, there are other considerations in determining the IF frequency. The sampling rate of the bandpass sigma-delta modulator will be determined by the IF. As the sampling rate is 4 times the IF frequency, it is undesirable to have too high an IF. For sampling rates above 100 MHz, the performance of the modulator (specifically the SQNR) diminishes due to the limitations of the switched capacitor filter [NST97]. For example, the complex bandpass modulator used in testing could clock over 60 MHz, but had better performance when clocked at lower frequencies [Swa97]. For a 60 MHz clock, the IF would be at 15 MHz, which is acceptable for AMPS, although such a choice makes the image reject filter selection difficult. Modulators capable of higher IF frequencies have been published with switched capacitor filters [OW97] and continuous time filters [Gao97].

The initial bandpass $\Sigma\text{--}\Delta$ chosen for experimental use was the part described in [SS95a], which had a maximum clocking frequency of around 42 MHz, or an IF of 10.7 MHz. Initial considerations of the IF selection problem led to the possible solution of using a 40 MHz clock, but using an IF frequency of $5f_s/4$, or 50 MHz, rather than 10 MHz. As an aside,

initial testing showed that there was negligible decrease in the performance of the modulator at $5f_s/4$ compared to $f_s/4$, which means that the IF could be subsampled, maintaining the oversampling properties of the modulator. Unfortunately, this only remaining engineering sample failed before formal testing was performed and measurements taken, hence no results are given here. Testing was also done at $9f_s/4$ (90 MHz IF), but at this higher frequency, the noiseshaping notch appeared much more filled in, and shifted. No explanation was found for this. There were no measurements done with the complex bandpass Σ - Δ modulator. This topic is certainly an area for further research.

One last consideration used here in setting the system IF was in the reference frequencies available. Having a clock for the sigma-delta modulator that is a multiple of the system reference frequency is also convenient. The synthesizer requires a 20 MHz reference to generate the LO frequencies (the 20 MHz is divided down on board to provide the PLL reference), and uses this 20 MHz reference to generate a clock for the digital logic implementing the fourth order MASH and the digital mixer. Selection of the system reference is important, since the PLL is sensitive to phase noise in the reference. Of course, care must be taken in selecting the clock frequencies on board to minimize noise and spurious signals.

The front end image reject filter must pass the entire AMPS band from 868 MHz to 894 MHz, while providing sufficient image rejection, about 80 dB. Because of the high frequency, this filter will most likely be a SAW filter. Most SAW filters only provide about 40-50 dB of rejection, so two filters would be required, typically one placed before the LNA and the other after. It is important that the insertion loss of these filters be as low as possible, as they add directly to the noise figure of the receiver. Typical insertion losses are 3 dB. Rather than using two filters, a combination of one filter and an image reject scheme could be used, where typical mismatch at RF frequencies can still give over 30 dB of rejection. Both solutions have been presented in the literature [Rud97].

3.6.2 Automatic Gain Control

Due to the fading properties of the wireless channel, some kind of automatic or programmable gain control (AGC) is required for proper receiver performance. To achieve the required resolution from the bandpass Σ - Δ converter, the input signal must be sufficiently large. If there is not enough gain, the signal to noise ratio due to the bandpass Σ - Δ noise contribution will be too small for acceptable performance. If the gain is too high, components in the receiver will saturate, and many components (such as the bandpass Σ - Δ) cannot function properly under such conditions, causing equally unacceptable performance. The overall input dynamic range required may typically be as high as 140 dB for a given standard [LHH94], requiring many orders of magnitude of AGC. As an example, assume an LNA gain of 16 dB, a mixer gain of 8 dB, and 6 dB of attenuation from the SAW filters, the total gain of the front end is 18 dB. Take the bandpass Σ - Δ dynamic range as 8 bits, or 48 dB. The required AGC is then 76 dB for the receiver to operate at 8 bit resolution, which is significant.

There are two possible places to place the AGC in this receiver architecture: before the first mixer (at the RF), or after the mixer (at the IF). Placing the AGC at the IF has some obvious advantages, most notably designing the AGC at the RF would be much more challenging, especially in terms of power consumption. However, placing the AGC after the mixer has certain problems to take into consideration. This receiver is a feedback control system, and changing the gain changes the dynamics of the loop. As the received signal strength fluctuates, the gain will also fluctuate, which may affect the performance of the loop. The bandwidth of the AGC loop must be wide enough to keep up with the fluctuations in received signal strength. If the PLL bandwidth is close to the bandwidth of the AGC control loop, stability may become a concern [Gar79].

There are two places to obtain the error voltage (representing the received signal strength)

in the receiver: noncoherently at the IF stage, or coherently in the in-phase (I) signal after the I/Q digital mixdown after the bandpass Σ - Δ modulator. Using the coherent signal offers the advantage of having reduced sensitivity to noise [Gar79], but the DC value representing the received signal strength only exists when the loop is locked. To lock the loop, either the noncoherent IF signal strength must be used, or some software controlled algorithm must be used to help set the AGC to lock the loop.

3.6.3 Noise Analysis

Since the PLL is a nonlinear system, detailed noise analysis is quite involved, and not presented in this thesis. However, this architecture does have an interesting advantage over the conventional PLL for FM demodulation. Consider two of the noise sources which can lead to poor noise performance in FM demodulation for the PLL: noise at the input (i.e. channel noise) and phase noise from the VCO in the loop. Since the PLL will filter out noise components appearing at the input of the loop above the natural loop frequency of the PLL, it is desirable to minimize this natural frequency of the loop. However, the phase noise contribution of the VCO is suppressed within the loop bandwidth, due to the feedback action of the PLL. Hence, it is desirable to have a narrow loop bandwidth to suppress PLL input noise, while at the same time have a wide loop bandwidth, to suppress VCO noise contributions to the demodulated output signal.

In the architecture, there are two loops: the outer heterodyne loop, while the VCO is found in the inner frequency synthesizer loop. This inner loop provides another degree of freedom for the designer, in that the loop bandwidth of the synthesizer can be chosen wide, to suppress the VCO noise, while the loop bandwidth of the heterodyne loop can be made narrow to filter out input noise. Because of this nested loop architecture, the noise contributions of both sources can be minimized.

CHAPTER 4 Simulation and Measurement Results

4.1 Introduction

In this chapter, the results of measurements obtained will be presented, and compared to simulations done with Matlab. The first section describes the test setup, and following sections provide measurements and simulations of tuning range, frequency step response, and adjacent channel interference, as well as the demonstration of the loop performing FM demodulation. The order of the measurement section does not represent the order the measurements were done; initial tests were done replacing the bandpass sigma-delta modulator and IF path with a baseband A/D, to verify operation before the heterodyne loop was used. However, like measurements are grouped together for convenience. The measurement setup is described in later sections.

Matlab was chosen for the simulations because of the discrete time components required, namely the divider and the sigma-delta modulators. Complex envelop simulators and harmonic balance methods cannot handle these discrete time components, and circuit level simulations (such as Spice) are simply too computationally (and time) intensive for such a large system. Although the models presented in Chapter 3 are suitable for stability and noise analysis, and to gain insight into the frequency response of the PLL, it is not possible to examine the transient behaviour unless a discrete time analysis is used. Also, the PLL is by nature a nonlinear device. Simulations with a linear model could not predict problems with acquisition, signal tracking, and stability. By performing simulation using more ac-

curate models, more information can be obtained, and a higher degree of confidence in the operation of the device.

The MATLAB model was obtained by transforming the various elements to their z-domain equivalent. This is quite easy for components such as mixers and VCO's, and filters were transformed using the bilinear transform. Although frequency warping is a problem with the bilinear transform (as opposed to the impulse invariant transform), if the sampling frequency is quite large, then there is effectively no difference at lower frequencies.[Lyo97] If a complex envelope notation had been used up to the IF stage, then the impulse invariant transform would have been required to transform the IF stage filter. The IF bandpass filter was a simple second order, as used in the measurements. The loop filter within the synthesizer was an integrator with phase lead correction with an additional pole at higher frequency, to more accurately model the circuit on the bench. Also, the phase/frequency detector within the synthesizer was replaced with a sinusoidal phase detector, for simplicity. Since startup and acquisition was never (intentionally) simulated, this was not a problem. The bandpass sigma-delta used in simulation was second order, as was initially used in testing. Also, the 4th order MASH was replaced with a second order $\Sigma\text{--}\Delta$. Second order $\Sigma\text{--}\Delta$ modulators still have good tonal behaviour, but not as good noise performance. These simpler models help with simulation time, and other than noise performance, do not affect the PLL performance. Other models could be substituted in their place.

There were three possible models for the divider. The simplest was to use a linear model for the divider. For a static divider where the modulus was known, this provided the fastest simulation time. However, if the fractional part was required, simply changing the linear divider value causes discontinuities in the divided phase, and produces large tones in the output dependant on the properties of the controlling bitstream. The next two approaches, which are more suitable to dynamic dividers, were tried with good results. The first was to

use the small-signal model for the divider, subtracting phase from the VCO to obtain the correct VCO phase. The final approach was to use an a state machine, modelled in MATLAB, to divide down the VCO phase by counting VCO edges. This is the approach used in the final model, as this most closely represents the actual circuit. Further work could be put into the second divider model, as it might be possible to use it if it becomes necessary to perform simulations using complex envelope representation.

4.2 Measurement Setup

The PLL Receiver was measured using various available components used in, or built as, previous research work at Carleton. Notably, the frequency synthesizer was a lab prototype built with discrete parts based on [Fil97]. The initial bandpass Σ - Δ modulator used was a second-order switched capacitor [SS95a], which later had to be replaced with for a newer complex 6th-order switched capacitor bandpass Σ - Δ modulator [Swa97] due to a component failure. All measurements presented here are with the newer version of the bandpass Σ - Δ modulator. Most other components were discrete components, and will be discussed in the appropriate section.

A block diagram of the test setup is shown in Figure 4.1.

Figure 4.1 Block Diagram of Test Setup

4.2.1 Complex Bandpass Sigma-Delta Modulator

As discussed previously, the bandpass $\Sigma\Delta$ modulator performs an A/D conversion on the information signal at the IF frequency, rather than at baseband. Initial measurements were done with a second-order bandpass $\Sigma\Delta$ modulator designed by [SS95a], which was replaced with a 4th order complex bandpass $\Sigma\Delta$ modulator by [Swa97]. The primary difference between a regular and complex bandpass $\Sigma\Delta$ modulator is that the complex bandpass $\Sigma\Delta$ modulator uses a complex filter to give different transfer functions to the signal at $f_s/4$ (desired signal) and the image at $3f_s/4$ (an image that will alias to baseband after mixing down). To suppress this image, a normal bandpass $\Sigma\Delta$ would need to rely on the IF filter proceeding the modulator. The complex bandpass $\Sigma\Delta$ performs uses the I and Q channel to perform the image rejection, similar to an image reject mixer. Within the overall modulator, there are actually two bandpass $\Sigma\Delta$ modulators, each with its own filter (resonator) section. However, stages of the resonator structure between modulators are cross

coupled, to provide the complex (nonsymmetrical) transfer function, which allows a different transfer function for the signal at $f_s/4$ and $3f_s/4$. Selection of the filter coefficients allows selection of the noise and signal transfer functions for the Σ - Δ modulator. The design of this modulator was such that the signal transfer function had a gain of 6 dB, while the image transfer function (at $3f_s/4$) had a gain of -2dB. Also, the 4th order complex filter was selected to provide 3 noiseshaping zeros in the noise transfer function, and only one zero in the image transfer function. This provides noiseshaping as if the modulator was 6th order.

Just as the input to the modulator requires a complex representation of the input signal, in terms of the in phase and quadrature (I and Q) components, the output of the modulator is also in terms of the complex representation of the signal. Downconversion of the output to the usable I and Q baseband output can be achieved through the circuit in [Swa97]. This digital circuit was implemented using a programmable gate array logic (GAL) chip. The downconversion frequency signals (cosine represented by 1,0,-1,0 and sine represented by 0,1,0,-1) were generated from the 20 MHz clock reference, and the mixing was performed using XOR gates. The second stage addition was performed by a simple 2:1 mux, con-

trolled by the clock signals.

Figure 4.2 Complex Mixer

With the theoretical improvement in performance by the complex filter, this second-order complex sigma-delta modulator should give the same resolution as a third-order lowpass sigma-delta modulator. The modulator was tested using a 10 MHz clock and a 2.5 MHz input tone. For a 30 KHz bandwidth, the ideal SQNR would be 20 bits, or 120 dB. The mea-

sured SNR was 27 dB [Swa97]. The measured output spectrum is shown in Figure 4.3 .

Figure 4.3 Measured Output Spectrum of Bandpass Sigma-Delta Modulator

A major reason for the significant inband noise is due to circuit noise within the modulator [Swa97]. This noise dominates the noise observed in the measured results.

4.2.2 Frequency Synthesizer

As mentioned, the frequency synthesizer used here was a prototype build using discrete components based on a design done at Carleton [Fil97], and a block diagram of this syn-

thesizer is shown in Figure 4.4 .

Figure 4.4 Block Diagram of Frequency Synthesizer Prototype Board

The synthesizer provides an output frequency between 800 and 820 MHz, with a minimum resolution of approximately 300 Hz. A fourth order MASH is used to control a multi-modulus divider to provide the frequency tuning. The input to the MASH is a 16 bit word, with the least significant bit corresponding to a 300 Hz frequency resolution. Normally, this 16 bit input is used for channel selection, but here is also used as the input for the feedback path to close the loop on the PLL. The MASH and offset summing block are both implemented in a Xilinx XC3195APC84 field programmable gate array (FPGA). Due to speed limitations within the FPGA, the long delay within the accumulators in the MASH limited

the maximum clock speed to 5 MHz. This was corrected by pipelining the 16 bit adders, so that there was a total delay of 4 clock cycles through the MASH, and another 4 through the offset summation, giving the FPGA a maximum clock speed over 20 MHz. The delay in the signal path of 8 clock cycles is equal to a time delay of 0.4 μ s with the 20 MHz clock.

Since the output of the 4th order MASH is a 4 bit word, an 8 bit programmable divider is used to control the divide ratio of the synthesizer. The MC10EO16 is an 8 bit synchronous programmable up/down counter capable of clocking up to 700 MHz [Mot96]. A line driver is used as a buffer between the VCO and divider to ensure correct ECL voltage levels. Since the VCO output is over 800 MHz, a divide by 2 is placed before the so that its maximum clock speed is only 410 MHz. To provide an average divide ratio of 40/41, the 8 control bits (which set the divide ratio) are set by the MASH output and a fixed offset, which is set to 33. The 4 least significant bits of the divider are controlled by the MASH, which provide for an average divide ratio of $33+(7/8)$, or 40/41. Since the 20 MHz reference is divided by two before being used as the reference for the loop, the overall divide ratio achieved by this synthesizer is 80/82, giving a frequency range of 800 to 820 MHz.

The AD9901 was used to provide the phase/frequency detector, which uses an XOR gate for phase detection, and a state machine for frequency detection, to provide the correct steering voltage for locking [AD9901]. The VCO is a Z-Comm part, V700ME03, with a tuning range of 770-830 MHz, and a typical tuning sensitivity of 31 MHz/V [Zcom].

The loop filter used is shown in Figure 4.5 . The loop transfer function is given as:

$$F(s) = -\frac{1}{s\tau_2} \left[\frac{1 + s\tau_3}{1 + s\tau_1} \right] \left[\frac{1}{1 + s\tau_4} \right] \quad (4.1)$$

where $\tau_1 = \frac{R_1 R_2 C_1}{R_1 + R_2}$; $\tau_2 = C_2(R_1 + R_2)$, $\tau_3 = R_3 C_2$, and $\tau_4 = R_4 C_3$.

Figure 4.5 Frequency Synthesizer Loop Filter

The channel centre frequency will be determined by the average value of the input word. Since the bandpass sigma-delta requires one bit for the feedback, the other unused 15 bits can be used to perform a channel select, accurate to 305 Hz. The centre frequency of a channel is given by:

$$F_{centre} = 820 \cdot 10^6 - 305 \cdot w_{in} - b_{DC} \cdot F_{in} \quad (4.2)$$

where F_{centre} is the centre frequency in Hertz, w_{in} is the value of the 15 bit channel select input, b_{DC} is the DC value of the bit stream from the sigma-delta, and F_{in} is the frequency for the input bit used for the feedback. The bit chosen for the feedback determines the maximum frequency deviation of the frequency synthesizer when used as an NCO. It also effectively sets the gain of the NCO in the PLL analysis, in terms of KHz/volt. Note that the bit used for feedback cannot be used in the channel select word. For an FM input, the av-

erage bit value going into the feedback bit will be 0.5, which must be taken into account in the channel select word. This is important to take into account in the recalculation of the channel offset if the NCO gain is changed by changing the feedback bit.

4.2.3 Other Loop Components

This section discusses the remaining loop components, namely the RF front end mixer, IF bandpass filter and IF amplifier. The mixer was a diode ring mixer, MiniCircuits part number ZEM-4300. Since the mixer LO port is driven with a large signal from the synthesizer VCO, the mixer output can be written as [KBR80]:

$$V_o(t) = V_{RF} \cos \omega_{RF} t \left(\frac{1}{2} + \sum_1^{\infty} \frac{\sin n\pi/2}{n\pi/2} \cos n\omega_{LO} t \right) \quad (4.3)$$

Assuming an ideal IF filter, the voltage at the IF is then $(V_{RF}/\pi) \cdot \cos(\omega_{LO} - \omega_{RF})$, and the gain for the mixer is $1/\pi$.

The IF amplifier was required to boost the mixer output for the bandpass sigma-delta, and an HP8447E was available. The HP8447E was a wideband amplifier (0.1-1300 MHz) supplying 22dB of gain over that bandwidth with a specified maximum ripple of 1.5dB over the bandwidth. The IF bandpass filter is required to filter out the sum frequency component (and higher harmonics) from the mixer output. The filter used here in the loop was a simple tank circuit, to provide the bandpass filtering, with a detuning resistor used to set the Q of the filter. An infinite Q filter would have made the loop unstable, so a wide bandwidth was selected for the filter, making the PLL basically first order. For a centre frequency of 2.5 MHz, the selected inductor and capacitor were $L=120\text{nH}$ and $C=0.033\mu\text{F}$. Since the output impedance of the mixer wasn't known, a $5\ \Omega$ resistor was added, to ensure that the bandwidth wasn't too wide. The measured insertion loss of the final filter was about 8 dB, with

a 3 dB bandwidth of 60 KHz with 50 Ω source and load. The circuit is shown in Figure 4.6

Figure 4.6 IF Filter

4.3 Tuning Range

After demonstrating that the loop would be stable with the frequency synthesizer used as an NCO, the Harris A/D converter was replaced with the bandpass sigma-delta modulator, and second LO/mixer to downconvert the IF to baseband. The loop was demonstrated to work for any of the feedback bits shown in Table 4.1. The loop tuning range was measured for those different feedback gains, and those results are also shown below in Table 4.1

Bit	Centre Frequency (MHz)	Ideal Deviation (KHz)	Measured High (MHz)	Measured Low (MHz)	Measured Deviation (KHz)	Measured/Ideal
7	809.9904	19.2	809.99065	809.98916	1.49	0.0776
9	809.9616	76.8	809.96732	809.95823	9.09	0.1184
11	809.8464	307.2	809.89050	809.87160	18.9	0.0615
13	809.3856	1228.8	809.588500	809.428500	160	0.1302

Table 4.1: Measured Tuning Range of PLL with Bandpass Σ - Δ Modulator

The measured tuning range is about 10% of the theoretical frequency range. The theoretical bandwidth is based on the full range frequency deviation of the synthesizer, which is achieved by setting the input bit to either a zero or a one. Although the bits coming out of the sigma-delta modulator do toggle the input of the synthesizer over full scale, the average measured value of the bits only ranges from 0.45 to 0.55 of full scale. Thus, the achievable tuning range will only be about 10% of full scale. Since AMPS has a maximum deviation of 12 KHz, ideally the input bit used should be bit 7, giving an ideal deviation of 19.2 KHz. To get the required deviation, bit 10 was used as the input to the synthesizer.

Identical to the problem with sigma-delta modulators controlling dual-modulus dividers, the full dynamic range of bit densities (all zeros to all ones) is not available from the output of the bandpass Σ - Δ modulator. Measurements taken show that the maximum range of the bit density goes from about 0.44 to 0.56 (normalized density can range from 0 to 1). This result isn't completely surprising, considering the maximum useful range of the sigma-delta bit density to be between 0.25 and 0.75. After passing through the digital mixer, half the

signal power is lost, reducing the useful range now to between 0.375 and 0.625.

Figure 4.7 Range of Bit Stream Density for Bandpass Σ - Δ Modulator

4.4 Frequency Step Response

The initial frequency step response tests were done with an 8 bit A/D converter (Harris HI 1175) on a prototype board [AN9331] in place of the bandpass Σ - Δ converter. This allowed testing of the frequency synthesizer as a voltage controlled oscillator in the loop, without having the troubleshooting difficulties of the heterodyne PLL. The output from the A/D converter was connected to the 8 LSB's of the frequency synthesizer input, giving a maximum deviation of 75 KHz for a full scale input, peak to peak.

The loop was first tested open loop, to demonstrate the frequency synthesizer used as an VCO. Figure 4.8 shows an FM spectrum with $\beta=2$.

Figure 4.8 Measured Spectrum for Frequency Synthesizer as an FM Modulator

Figure 4.12 shows the simulated spectrum.

Figure 4.9 Simulated Spectrum of Frequency Synthesizer as FM Modulator

In closed loop, the tuning range measured was 21.6 KHz. A 10 KHz frequency step was applied to the loop, and the loop was demonstrated to have a dominant pole of about 11 KHz, which corresponds to the dominant pole in the closed loop. To see the transient, the bits from the A/D converter were captured, and Figure 4.10 shows these captured bits from the HP 16005A. The sample rate was 4 MHz, and the total simulation time displayed is 1500 points. The time constant was measured as 0.063 msec., which is expected as the loop

gain was set higher in this loop than in the heterodyne loop to follow.

Figure 4.10 Frequency Step Measured with Short Loop, 8 Bit A/D Converter

The measured step response for the heterodyne loop is shown in Figure 4.11 . Although noisy, the response can be seen to be underdamped, and takes about 0.15 ms to complete. Again, the dominant noise source appearing in Figure 4.11 is due to the poor noise performance of the bandpass sigma-delta modulator used, as discussed previously in Section

4.2.1.

Figure 4.11 Measured Response for Heterodyne Loop

The simulated response to a frequency step is shown in Figure 4.12. The noise floor is dominated in simulation by the noise floor of the 2nd order bandpass sigma-delta modulator, where the measured noise floor seems to have more discrete spikes. Simulations with a higher order bandpass sigma-delta modulator should improve the noise floor.

Figure 4.12 Simulated Response to Frequency Step

4.5 Sinusoidal Response

Since this PLL is intended for demodulation of FM, demonstration of this is very important. Again, initial testing was performed with the Harris A/D converter, but no results are presented here. Figure 4.13 shows the experimental measured result to an FM input signal.

Figure 4.13 Measured Sinusoidal Response to FM Input

Note that the dynamic range is larger than measured for the frequency step. The first reason for this is that a sigma-delta modulator has a larger dynamic range for a sinusoidal input than a DC input, thus allowing a larger output swing. The second reason was that the PLL was driven harder with a larger deviation input. For the frequency step, had the output exceeded the maximum deviation of the PLL, the loop would have lost lock. For the sinusoidal input, it was easier to determine where the loop was losing lock (by listening to the audible clicks caused by the phase jumps). The simulated response is shown in Figure 4.14.

Figure 4.14 Simulated Sinusoidal Response to FM Input

4.6 Adjacent Channel Interference

Perhaps the most important requirement for the receiver is its performance with adjacent channel interference. With the digital radio, the IF filter is only partly responsible for filtering the ACI. Sufficient dynamic range is used in the A/D converter so that the desired signal and ACI are passed to the DSP without distortion, where any remaining ACI is filtered out. Similarly in the PLL, the closed loop bandwidth can be used to filter out some of the ACI. However, where a large adjacent channel interferer will cause saturation in a typical receiver, in the PLL, this large interferer can cause the loop to lock onto it, rather than the desired signal, and no amount of dynamic range will help. Furthermore, there is a

limit to the amount of filtering which can be performed due to stability concerns within the loop

The adjacent channel interference (ACI) response was measured with the loop, and is shown in terms of the ability of the ACI rejection in Figure 4.15 . The response was measured using two RF frequency sources capable of generating a narrowband FM signal. Each source was FM modulated with a slightly different modulating signal (200 Hz and 220 Hz). The output of the loop was filtered with an analog LPF, and sent to an amplified speaker. Each source could be identified by which tone was demodulated by the PLL. The two sources were combined using a splitter/combiner, and both fed into the RF front end mixer, with one source set to a constant -30 dBm input power. The second source was varied in power at different frequencies, and the point at which the loop locked onto the second source was noted. The source the PLL had locked on to was evident from the demodulated frequency heard at the output. As can be seen from Figure 4.15 , the ACI rejection at 60

KHz was found to be about 14 dB, where the specification required 65 dB of rejection.

Figure 4.15 Measured Adjacent Channel Response of Heterodyne PLL Receiver

No information regarding PLL response to ACI was found in the literature, hence some simulations were performed using MATLAB to attempt to gain an understanding. To help understand, it is helpful to compare this to the pull-in process for a PLL. When the PLL acquires lock, the input frequency and VCO free running frequency mix to produce a beat frequency. This beat frequency FM modulates the VCO, producing sidebands around the VCO free running (carrier) frequency, at a distance equal to the beat frequency away from the VCO carrier. This causes one of the sidebands to mix with the input frequency to pro-

duce a DC component, which tends to pull the VCO toward the desired VCO tuning voltage for lock. As the VCO frequency moves closer to the input frequency, the beat frequency decreases, until no more cycle slips occur, and the PLL achieves phase lock.

Now consider a locked PLL, and an adjacent channel interference is added to the input. The mixer output again has a beat frequency, equal to the frequency difference between the interferer signal and the locked VCO frequency. Normally, this would cause the PLL to lock onto the signal; the signal that the PLL is locked onto will tend to pull the PLL back into lock such that the average of the VCO tuning signal is the DC required to remain locked to the initial input. Figure 4.16 shows the error voltage fed to the VCO to provide tuning. At timestep 20000, an interferer signal is applied to the loop of equal amplitude to the initial

input and 100 KHz offset, which causes the beat frequency to appear.

Figure 4.16 Beat Frequency in PLL Error Voltage Due to Interferer

For the PLL to lock onto the interferer, it must pull harder than the initial signal, and this depends on the strength of the signal modulating the VCO. Figure 4.17 shows at timestep 100000 the error voltage step as the PLL locks onto a interferer signal 10 times stronger (in amplitude) than the initial signal, at a frequency difference of 10 KHz. The PLL goes from being locked at the initial frequency (where the average VCO tuning voltage is a little above zero), to the new frequency (where the average VCO tuning voltage is a little above one). The strength of the interferer required for the PLL to lock onto it depends on both its

amplitude and frequency difference between it and the locked VCO.

Figure 4.17 PLL Error Voltage Locking on to Strong Interferer

4.7 Conclusions

In this chapter, simulations and a prototype design with measurements of the proposed architecture are presented. The transient measurements verify the modeled and simulated transient response, with a single dominant pole at around 11 KHz. Sinusoidal response is also presented. The bandpass sigma-delta modulator was the dominant noise source, which limits the performance in terms of voice quality. This architecture fails to meet the AMPS adjacent channel interference specification, with only 14 dB of ACI available (where 60 dB was required).

In this thesis, an alternative architecture for a first generation analog FM cellular receiver is presented, including models for design, time domain simulations and measurements of a prototype to verify the models and simulations. This architecture features the reuse of the same components required for a digital receiver, which gives a dual mode radio the savings of any extra components in the analog receive chain. This helps to reduce the overall cost of the radio, since the components of the multi-mode radio were all designed to provide a high degree of integration. Although the architecture presented did not achieve the final goal of meeting the required standards for AMPS, specifically the adjacent channel interference specification, the models and design methods presented are generally applicable to future designs incorporating complex PLL architectures.

This architecture was successful at demodulation of both small deviation and large deviation FM signals, given the gain adjustment inherent to the MASH input of the synthesizer. Because of the poor noise behavior of the bandpass sigma-delta modulator, there were no quantitative noise measurements made. However, with better noise performance from the bandpass sigma-delta modulator, the receiver could have provided suitable performance for acceptable voice transmission. During one demonstration of the receiver, music from a CD player was used as the modulating signal; it was demodulated, filtered, and sent to a speaker. The deviation was adjusted so that the music and voice could be heard over the noise, but since the deviation was adjusted to near maximum for a nominal amplitude input, the receiver lost lock (heard by audible clicks) for large amplitude deviations. This problem would have been corrected by a better SNR in the bandpass sigma-delta modulator.

As shown from the measurements, the shortcoming of this architecture is in dealing with adjacent channel interference. Measurements taken show that the receiver can handle about 14 dB of adjacent channel rejection, as opposed to the 60 dB that is required. Clearly, PLL's have a problem dealing with ACI, which would explain why they are not popular used on their own for FM demodulation. Used in an environment where the ACI is expected (such as an urban setting), this receiver will suffer from dropped calls. In the future, there may be applications where adjacent channel interference is not significant, and this architecture may be feasible.

5.1 Future Research

There are a number of issues that remain to be examined in this receiver. A quantitative analysis of the noise performance of the receiver could be performed to compare to the performance of other receivers. Also, the natural acquisition behavior of the loop could be examined. Obviously, improved ACI performance would be desired, and this could be an area of additional research. Another problem with the current architecture was the limitation of the dynamic range of the single-bit output from the bandpass sigma-delta modulator. The use of a bandpass sigma-delta with a multi-bit output would be of use, not only in improving the dynamic range, but may also help future higher-order bandpass sigma-delta designs in terms of stability.

MATLAB was selected to perform the discrete time simulations of the receiver. To take into account the nonlinear nature of the components within the sigma-delta modulators and the divider, only discrete time simulations were applicable. There are very few tools for the simulation of nonlinear time domain components, such as dividers and comparators, and even the available choices lead to long simulations. MATLAB was selected over SIMULINK to take advantage of the opportunity to optimize code for simulation time. Some

improvement might be achieved by using complex envelope notation, allowing the sampling rate to be based on the IF frequency, and not the RF frequency, thus reducing the number of samples (hence the sampling time) for the simulation. There is also a problem with memory limitations for large simulations. For a simulation of a system with 30 state variables, using double precision floating point representation (8 bytes) and 1 million data points, the memory requirements are over 228 MBytes. For very large simulations, the computer will need to begin to use virtual memory, which will slow the simulation down considerably. Rather than storing every state variable in an array, only the required state variables (ideally, only the output) are stored, and all other state variables only store as many samples as required for calculation (for example, an FIR filter requires a memory location for each tap, etc.). This requires more calculation for maintaining the contents of the state variables, but will save time for long simulations in not accessing virtual memory. The need for simulators capable of handling such systems is quickly becoming quite important, and is perhaps one of the most important future research topics in this field.

There are certainly variations of this architecture which should be investigated in the future. Although the bandpass filter within the loop needs to have a wide bandwidth for use with wideband digital standards, there exists an opportunity to investigate the addition of a narrowband digital loop after the baseband downconversion, which would make the architecture appear more similar to [Bax95].

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