Applications of Waveform Relaxation for EMI and Power Integrity Analysis in High-Speed Designs

by

Arvind Sridhar

A thesis submitted to the Faculty of Graduate Studies and Research in partial
fulfillment of the requirements for the degree of Master of Applied Sciences

Ottawa-Carleton Institute for Electrical and Computer Engineering

Department of Electronics

Faculty of Engineering

Carleton University

Ottawa, Ontario, Canada

March 2009

© Arvind Sridhar 2009

Library and
Archives Canada

Published Heritage
Branch

395 Wellington Street
Ottawa ON K1A 0N4
Canada

Bibliothèque et
Archives Canada

Direction du
Patrimoine de l'édition

395, rue Wellington
Ottawa ON K1A 0N4
Canada

Your file Votre référence
ISBN: 978-0-494-52031-4
Our file Notre référence
ISBN: 978-0-494-52031-4

NOTICE:

The author has granted a non-exclusive license allowing Library and Archives Canada to reproduce, publish, archive, preserve, conserve, communicate to the public by telecommunication or on the Internet, loan, distribute and sell theses worldwide, for commercial or non-commercial purposes, in microform, paper, electronic and/or any other formats.

The author retains copyright ownership and moral rights in this thesis. Neither the thesis nor substantial extracts from it may be printed or otherwise reproduced without the author's permission.

AVIS:

L'auteur a accordé une licence non exclusive permettant à la Bibliothèque et Archives Canada de reproduire, publier, archiver, sauvegarder, conserver, transmettre au public par télécommunication ou par l'Internet, prêter, distribuer et vendre des thèses partout dans le monde, à des fins commerciales ou autres, sur support microforme, papier, électronique et/ou autres formats.

L'auteur conserve la propriété du droit d'auteur et des droits moraux qui protègent cette thèse. Ni la thèse ni des extraits substantiels de celle-ci ne doivent être imprimés ou autrement reproduits sans son autorisation.

In compliance with the Canadian Privacy Act some supporting forms may have been removed from this thesis.

Conformément à la loi canadienne sur la protection de la vie privée, quelques formulaires secondaires ont été enlevés de cette thèse.

While these forms may be included in the document page count, their removal does not represent any loss of content from the thesis.

Bien que ces formulaires aient inclus dans la pagination, il n'y aura aucun contenu manquant.

Canada

Abstract

Traditional methods of circuit simulation are proving to be inadequate in handling the issues due to higher operating frequencies, higher densities and increasing complexity of circuits. This is especially true in the case of electromagnetic interference (EMI) and power integrity analysis in high-speed designs. High frequency effects have to be taken into account in the early stages of a design in order to reduce the cost of manufacturing and to increase yield.

Recently, waveform relaxation (WR) techniques were proposed for efficient simulation of large coupled high-speed interconnects. In this thesis, the WR method has been further advanced to handle two important applications in high-speed designs. First, a new algorithm for fast EMI analysis of large coupled interconnects is presented. For this purpose, the recently developed transverse partitioning technique is exploited to decouple the large coupled interconnects. Also, methods to efficiently compute equivalent sources representing the effect of incident fields on the interconnects are developed.

Next, an efficient technique for the transient analysis of on-chip power distribution networks (PDNs) in VLSI systems is proposed. For this purpose, smart partitioning schemes and convergence accelerating mechanisms are developed for CPU efficient performance. Numerical examples are presented to demonstrate the validity and efficiency of the proposed methods.

Acknowledgements

I would like to thank my supervisors, Professors Ram Achar and Michel Nakhla, who provided the initial inspiration for this work and gave critical guidance throughout the process. Their solid understanding of the subject and mentorship helped me grow and mature as a serious graduate researcher and made this thesis an enjoyable experience.

I thank Professor Emad Gad, Dr. Albert Ruehli of IBM, Koko Mihan of Javelin Systems, Dr. Eli Chiprout of Intel and Dr. Ihsan Eridin of Nortel Networks for their valuable comments and ideas, which were indispensable in producing this thesis.

I would like to acknowledge and thank my colleagues, D. Saraswat, B. Nouri, A. Bhullar, P. Triverio, A. Charest, N. Nakhla, A. Narayanan, M. Adel, A. Jerome, V. Ambalavanar, M. Siddique, Y. Hong, D. Trifkovic and L. Filipovic for the friendly, often philosophical, discussions which made me laugh and kept me engaged. I would also like to express my gratitude to the professors, staff and students at the department of electronics for making my work an enjoyable experience.

I leave a special note of thanks to my friend and colleague Harjot Dhindsa, and his parents. Without their affection and encouragement, working on this thesis would have been very hard.

I am grateful to my friend and colleague Douglas Paul who was patient enough to answer all my questions and helped me navigate smoothly through the course of my research.

Finally, I thank my parents Sridhar and Savithri, and my brother, Arun, for their years of patience. They inculcated in me, the dedication and discipline to do whatever I undertake well. I am grateful to you for loving me even when I was mischievous, defiant and stubborn.

Dedicated to my parents
for their unconditional love

Contents

1	Introduction	1
1.1	Background and motivation	1
1.2	Contributions	5
1.3	Organization of the thesis	6
2	EMI, Power Integrity- Modeling and Simulation	8
2.1	High-speed interconnects exposed to EMI	9
2.1.1	Inhomogenous Telegrapher's equations	11
2.2	Power Integrity	19
2.2.1	Transistor and power delivery switching	20
2.2.2	Significance of power distribution in VLSI circuits	25
2.2.3	Components of a power distribution network	26
2.2.4	On-chip power distribution networks	29
2.2.5	Modeling of on-chip PDN	32

2.2.6	Conventional methods of analyzing power grid networks . . .	34
2.2.7	Direct vs. Iterative methods	40
3	Review of waveform relaxation techniques	42
3.1	Traditional simulation methods	43
3.1.1	Conventional iterative techniques	44
3.2	Waveform relaxation	44
3.2.1	Mathematical formulation of the WR method for a general dynamical system	45
3.2.2	The WR method for a MNA based system of circuits	48
3.3	Convergence of the WR algorithm	50
3.4	Summary	52
4	Fast EMI analysis via transverse partitioning	53
4.1	Transverse partitioning for transmission lines	54
4.2	Proposed algorithm for fast EMI analysis in the presence of large number of coupled interconnects	60
4.2.1	Computation of equivalent sources compatible with waveform relaxation	60
4.2.2	Formulation of the proposed macromodel	65
4.3	Computational and implementation considerations	69

4.4	Numerical examples	71
4.5	Summary	85
5	Fast analysis of power distribution networks via Waveform Relaxation	87
5.1	Problem formulation: power grid circuits	88
5.2	Proposed transient analysis of power grid networks via waveform relaxation	92
5.2.1	Proposed partitioning of power grids, suitable for application of waveform relaxation	93
5.2.2	Computation of the initial-guess waveforms	98
5.2.3	Proposed GS-WR algorithm for transient analysis	105
5.3	Numerical results	108
5.4	Summary	117
6	Conclusions and Future Work	119
6.1	Summary	119
6.2	Future Work	121
A	Weighting factors for WR algorithm in transmission lines	124

List of Figures

1.1	High-speed interconnect effects	2
1.2	CPU cost of EMI analysis (lumped macromodel + HSPICE) for vary- ing number of coupled interconnects.	3
2.1	Interconnect hierarchy in high-speed VLSI systems.	9
2.2	Various types of interconnect structures in packages and circuit boards.	10
2.3	Description of parameters for formulation of EMI coupling.	11
2.4	Incident field coupling for the k^{th} line.	13
2.5	CPU cost of EMI analysis (lumped macromodel + HSPICE) for vary- ing number of coupled interconnects.	18
2.6	Inverter circuit (driver and receiver).	20
2.7	Input capacitance of receiver being (a)charged and (b)discharged, as the driver circuit switches states.	22
2.8	Current drawn by a CMOS inverter, with an input square wave. . . .	23

2.9	Switching noise due to voltage fluctuations in the PDN.	24
2.10	Components of a power distribution network.	26
2.11	Schematic of a power distribution network.	27
2.12	Power grid components.	29
2.13	Wire bond package.	30
2.14	Flip chip package.	31
2.15	An example transient current source waveform for representing active power drains in the PDN.	34
2.16	Reduction of power grid in the Multigrid method.	35
2.17	Partitioning of power grid in the Hierarchical analysis.	37
3.1	Test circuit for waveform relaxation	48
3.2	Partitioned subcircuits with Relaxation sources	49
3.3	Modified WR implementation	51
4.1	Distributed interconnect structure with n coupled lines.	55
4.2	Implementation of waveform relaxation in unexcited lines.	58
4.3	Equivalent sources due to external field for a short lossless line. . . .	63
4.4	EMI sources for the m^{th} segment of the k^{th} line in an MTL structure.	65
4.5	Proposed equivalent EMI (EE) sources for the m^{th} segment of an MTL structure.	66

4.6	Proposed time-domain macromodel for MTLs exposed to EMI.	68
4.7	Test MTL circuit for Example 1.	73
4.8	Temporal envelope of the incident electric field $E_0(t)$ (Example 1). . .	74
4.9	Comparison of transient waveforms for the far-end voltage of (a) line-1 and (b) line-2 (Example 1).	75
4.10	CPU cost for the computation of EMI sources for varying number of lines (Example 1).	76
4.11	Nonlinear circuit with 3-line MTL (Example 2).	77
4.12	Transient waveforms at (a) direct-line output, V_{OUT1} , and (b) victim- line output, V_{OUT2} , illustrating the impact of external incident fields with a peak amplitude of 1 V/m (Example 2). Note that there is no difference in the transient waveforms with and without EMI, due to the low peak amplitude of the incident field.	78
4.13	Transient waveforms at (a) direct-line output, V_{OUT1} , and (b) victim- line output, V_{OUT2} , illustrating the impact of external incident fields with a peak amplitude of 5 kV/m (Example 2). Note that there is significant difference in the transient waveforms with and without EMI, due to the large peak amplitude of the incident field.	80
4.14	Comparative study of convergence of waveform relaxation iterations for output transient waveforms at V_{OUT1} (Example 2).	81

4.15	Percentage error between WR results and CCLS results for successive iterations (Example 2).	82
4.16	Transient response at the far-end of line 15, showing the convergence of WR-TP iterations for the case, n=30 (Example 3).	83
4.17	Transient response at the near-end of line 6, showing the convergence of WR-TP iterations for the case, n=30 (Example 3).	84
4.18	CPU cost for varying number of lines: Conventional EMI analysis vs proposed (Example 3).	85
5.1	Mesh type circuit structure of a flip chip power grid.	89
5.2	3x3 Power grid example	90
5.3	Structure of the MNA matrices for the power grid circuit in Fig. 5.2.	91
5.4	Proposed BRP scheme for power grid	94
5.5	Subcircuit description for the i^{th} block in the BRP scheme	95
5.6	Voltage contours on a sample 50x50 grid without transient sources(for <i>Illustrative Example 2</i>).	96
5.7	Voltage contours on a sample 50x50 grid with a strong transient source at the center(for <i>Illustrative Example 2</i>).	97
5.8	Ramped waveform representing DC sources	99
5.9	Ramped waveform representing the initial-guess for the boundary nodes of the partitioned blocks, while computing WR sources.	101

5.10	A small area of the power grid shown with the highlighted source-region enclosed by its grid-shell.	102
5.11	Comparative study of convergence of waveform relaxation using the proposed BRP and SRP schemes for voltage transient waveforms at a sample node in <i>Ckt-1</i> (Example 1).	110
5.12	Illustration of the impact on transient voltage waveforms while using WR algorithm: with and without appropriate DC-level estimation (Example 2).	111
5.13	CPU cost comparison of power grid analysis using different methods (Example 3).	114
5.14	Convergence waveforms at a sample node in <i>Ckt-3</i> while using the proposed GS-WR method (Example 3).	115
5.15	Convergence waveforms at a sample node in circuit <i>PG</i>₁ (Example 4).	116

List of Tables

1.1	CPU cost comparison of power grid analysis using a conventional iterative technique	4
4.1	CPU cost comparison of EMI analysis for varying number of lines (Example 3)	85
5.1	CPU cost comparison of power grid analysis using different methods (Example 3)	113
5.2	CPU cost comparison for simulating industrial power grid circuits (Example 4)	117

List of Symbols

α	Order of computational complexity of a sparse matrix technique, while solving a system of linear equations
β	Order of complexity of a conventional macromodel of a system of MTLs
c_i	Capacitance connected at node i
g_{ij}	Value of the conductance between node i and node j
h	Step-size used in the backward Euler method
i	Time-domain current waveform
$\kappa_x, \kappa_y, \kappa_z$	Direction cosines of the incident electric field in a system of MTLs
n	Number of coupled lines in a system of MTLs
r	The number of the current iteration in the waveform relaxation process
s	Frequency in the laplace domain

t	Time
v	Time-domain voltage waveform
ω	Frequency
z	Distance measured along a system of multiconductor transmission lines from the near end
$\mathbf{A}$	MNA matrix
$\mathbf{A}_x, \mathbf{A}_y, \mathbf{A}_z$	Components of the incident electric field
$\mathbf{b}$	Selection matrix for the input sources in a MNA system
$\vec{\mathbf{B}}^i$	Vector of the incident magnetic field in a system of MTLs
$\mathbf{C}$	Frequency-dependent part of the MNA matrix
$\mathbf{d}$	Decoupling vector in the waveform relaxation algorithm
$\vec{\mathbf{E}}_t^i$	Vector of the transverse component of the incident electric field in a system of MTLs
E_0	Envelope (frequency/time-domain) of the incident electric field in a system of MTLs
$\mathbf{F}$	System of equations representing the time-domain behavior of a general dynamical system

F_{max}	Maximum frequency of operation of a microprocessor
$\mathbf{G}$	Frequency-independent part of the MNA matrix
Gnd	Ground terminal in an integrated circuit
$\mathbf{I}$	Vector of currents in a system of MTLs
I_{WR}	Waveform relaxation current source
$\mathbf{J}$	Convolution integral representing the effect of incident fields in a system of MTLs
N	Number of nodes in a power grid circuit
$\mathbf{u}$	Input vector in a MNA system
$\mathbf{V}$	Vector of voltages in a system of MTLs
$\mathbf{X}$	Vector of unknown variables in a MNA system
$\mathbf{y}$	Vector of unknown variables in a general dynamical system

Abbreviations

BRP	Block row partitioning scheme – a partitioning technique for simulating power grid circuits proposed in this thesis
C4	Controlled collapse chip connection – a method to make wire connections to an integrated circuit from a flip chip package
CAD	Computer-aided design
CCLS	Conventional coupled lumped segmentation – a macromodeling technique for multiconductor transmission lines
CGS	Conventional Gauss-Seidel method – an iterative technique to solve for a system of linear equations
CMOS	Complementary metal oxide semiconductor – a class of integrated circuits
CPU	Central processing unit

DEPACT	Delay extraction-based passive compact transmission line macromodel – a macromodeling technique for multiconductor transmission lines
EE	Equivalent EMI sources – equivalent sources representing the effect of incident field coupling in a system of high-speed interconnects proposed in this thesis
EEW	Equivalent EMI combined with waveform relaxation sources – sources representing the combined effect of incident fields and coupling from neighboring lines in a system of multiconductor transmission lines proposed in this thesis
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
GJ	Gauss-Jacobi method – an iterative technique to solve for a system of linear equations
GS	Gauss-Seidel method – an iterative technique to solve for a system of linear equations
IC	Integrated circuit
IFFT	Inverse fast fourier transform
KCL	Kirchhoff's current law

MEMS	Micro electro-mechanical systems
MNA	Modified nodal analysis
MoC	Method of characteristics – a macromodeling technique for multiconductor transmission lines
MRA	Matrix rational approximation – a macromodeling technique for multiconductor transmission lines
MTL	Multiconductor transmission lines
NMOS	n-channel metal oxide semiconductor transistor
PCB	Printed circuit board
PDN	Power distribution network
PEEC	Partial element equivalent circuit – a modeling technique for the representation of multiconductor transmission lines
PMOS	p-channel metal oxide semiconductor transistor
RLGC	resistance-inductance-conductance-capacitance – in reference to multiconductor transmission lines
SOR	Successive over-relaxation method – an iterative technique to solve for a system of linear equations

SRP	Single row partitioning scheme – a partitioning technique for simulating power grid circuits proposed in this thesis
SSN	Simultaneous switching noise – noise induced in the integrated circuits from the fluctuations in the power supply
TEM	Transverse electromagnetic wave
TP	Transverse partitioning scheme – a partitioning technique for simulating multiconductor transmission lines
VLSI	Very large scale integration
VRM	Voltage regulator module
WR	Waveform relaxation

Chapter 1

Introduction

1.1 Background and motivation

The ever increasing design constraints of submicron VLSI chips are placing enormous demands on computer-aided design (CAD) tools to perform accurate analysis of high-speed effects and circuit parasitics. Trends such as increasing operating frequency, denser layouts and integration of analog circuits and digital blocks have led to phenomenon such as crosstalk, signal distortion, and false switching. Also, the trends of decreasing operating voltages, increasing chip functionalities and performance have highlighted effects such as signal attenuation, reduced noise margin and timing failures.

The bulk of the effects of high-speed operation and circuit parasitics come from

Figure 1.1: High-speed interconnect effects

the high-speed interconnects that exist at different levels of system hierarchy, such as chips, packages and the PCBs. At high frequencies, these high-speed interconnects exhibit effects such as attenuation, reflections, crosstalk, ringing, signal delay, electromagnetic radiation and susceptibility, and consequently, cause signal degradation and faulty system performance (Fig. 1.1). If not predicted accurately at the early stages of design, these effects can severely degrade the system performance and, in many cases, even damage the devices. Therefore, it is important to model and simulate high-speed interconnects at various hierarchical levels in time-domain as accurately and as efficiently as possible.

In the recent years, several CAD techniques and methodologies have been pro-

Figure 1.2: CPU cost of EMI analysis (lumped macromodel + HSPICE) for varying number of coupled interconnects.

posed to handle high-speed modules in an efficient and accurate manner within the framework of conventional circuit simulators [1–5]. Most of these methods, which are based on macromodeling, prove to be inadequate in handling densely coupled systems (large coupled interconnects) and very large systems (power distribution networks). For example, for the simulation of high-speed interconnects exposed to external electromagnetic interference (EMI) using conventional techniques, the CPU cost of simulation grows as a cubic or fourth power of the number of lines (n^β , where $3 < \beta < 4$), as shown in Fig. 1.2.

In the case of power distribution networks (PDNs), where the circuits encountered

Table 1.1: CPU cost comparison of power grid analysis using a conventional iterative technique

Circuit	Circuit size (# of nodes)	CGS method (CPU time, in seconds)
<i>Ckt-1</i>	491,401	358.01
<i>Ckt-2</i>	641,601	537.41
<i>Ckt-3</i>	811,801	590.50
<i>Ckt-4</i>	1,002,001	755.60
<i>Ckt-5</i>	1,212,201	957.28
<i>Ckt-6</i>	1,442,401	1203.04

typically contain millions of nodes and circuit elements, the simulation times using conventional techniques can be excessive. For the purpose of illustration, Table 1.1 provides the CPU performance of the conventional gauss-seidel iterative solver (CGS method) for circuit sizes (of PDNs) varying from 500k to 1.5 million nodes.

Recently, waveform relaxation (WR) based techniques have emerged as viable solution methodologies for analysis of large coupled interconnects. The early application of waveform relaxation techniques for circuit simulation (proposed in the 1980s) was limited in its scope and success [6–10]. However, the recently developed transverse partitioning (TP), in conjunction with waveform relaxation for simulation of high-

speed interconnects, has renewed the interest in this method [11–13]. The transverse partitioning scheme divides a large coupled line system into subcircuits consisting of individual lines, exploiting the weak coupling between the lines. The convergence of the WR iterations in this case was shown to be quick, resulting in large savings in computational cost.

In this thesis, the scope of waveform relaxation techniques has been further advanced, by successfully applying it for two important problems in high-speed designs: 1) electromagnetic compatibility analysis of high-speed interconnects and 2) transient simulation of on-chip power distribution networks. Using effective partitioning techniques and optimizing existing macromodels for compatibility, the effectiveness and versatility of the waveform relaxation techniques in the broad area of signal and power integrity analysis is demonstrated.

1.2 Contributions

The subject of this thesis is to advance the scope of waveform relaxation techniques for EMI and power integrity analyses. The algorithms proposed in this work provide accurate and efficient solutions for high-speed effects which can be incorporated in SPICE like simulators. The main contributions of the thesis are:

1. **EMC analysis:** New methodologies based on transverse partitioning and

waveform relaxation are developed for the electromagnetic interference (EMI) analysis of large coupled high-speed interconnects. In addition, efficient computation of equivalent sources, representing the effect of incident fields on the interconnects are developed [14–16].

2. **Power integrity analysis:** Novel waveform relaxation based algorithms are developed for fast transient analysis of large power grid networks. New partitioning schemes exploiting the localized voltage distribution behavior of power grid circuits are developed. In addition, improved initial-guess computing techniques are developed for quick convergence of WR iterations [17–19].

1.3 Organization of the thesis

The thesis is organized as follows. Chapter 2 provides a background and literature survey of EMI and power integrity analysis. Various existing techniques addressing these problems are also examined. Chapter 3 reviews the theory behind waveform relaxation techniques and provides literature survey for the same. Chapter 4 proposes a waveform relaxation based algorithm for efficient EMI analysis and demonstrates the effectiveness of the algorithm using some numerical examples. Chapter 5 proposes a waveform relaxation based algorithm for efficient power grid analysis. Finally,

Chapter 6 gives a brief summary of the thesis and provides some ideas for future research.

Chapter 2

EMI, Power Integrity- Modeling and Simulation

Electromagnetic interference (EMI) and power integrity analysis in VLSI circuits are two very important areas of high-speed designs. In this chapter, the EMI and power integrity problems, and the related analysis challenges are discussed.

In Section 2.1, the formulation and conventional analysis techniques of high-speed interconnects in the presence of incident fields are presented. In Section 2.2, the power integrity problem is introduced. In addition, the power distribution network in a modern VLSI design is described and the conventional analysis techniques for on-chip power grids are examined.

2.1 High-speed interconnects exposed to EMI

With the rapid rise in operating frequencies and layout density, analysis of high-speed interconnects is becoming critically important. One of the major concerns emerging from these trends is the issue of increased susceptibility of electrical systems to electromagnetic interference (EMI). High-speed interconnects typically exist at various hierarchical levels such as on-chip, package, PCB etc. (as shown in Fig. 2.1). These interconnects may serve as efficient antennas at high frequencies leading to strong coupling of EMI, thereby altering the signal propagation behaviour in high-speed designs. This can seriously deteriorate the signal integrity of the design and lead to false switching of waveforms. Hence, fast and accurate analysis of high-speed interconnects in the presence of incident fields becomes necessary in modern circuit designs.

General interconnect structures, such as the ones shown in Fig. 2.2, are typically modeled as uniform multiconductor transmission lines (MTLs), under the assumption

Figure 2.1: Interconnect hierarchy in high-speed VLSI systems.

of a quasi-TEM mode of propagation. Although this is inaccurate for structures comprising of inhomogeneous dielectric medium, this approach is still used because of its relative ease and low CPU cost as compared to full-wave techniques. In addition, the quasi-TEM approximation allows modeling of signal propagation in interconnects, in terms of usual circuit voltages and currents instead of electric and magnetic fields. The governing equations characterizing the quasi-TEM behaviour are in the form of homogenous partial differential equations, known as Telegrapher's equations. The effects of EMI on these quasi-TEM structures can be modeled by introducing inhomogeneity to the Telegrapher's equations depending upon the nature and geometry of the waveforms and solving the resulting equations [20]. In the following subsection, formulation of transmission line equations in the presence of incident fields is described.

Figure 2.2: Various types of interconnect structures in packages and circuit boards.

Figure 2.3: Description of parameters for formulation of EMI coupling.

2.1.1 Inhomogenous Telegrapher's equations

Consider the geometry of n coupled lines, backed by a reference plane, with an incident transverse electromagnetic wave (Fig. 2.3). The quasi-TEM scenario of such a structure can be represented in the frequency-domain, by the following standard inhomogenous Telegrapher's equations [20–22]:

$$\frac{\partial}{\partial z} \begin{bmatrix} \mathbf{V}(z, s) \\ \mathbf{I}(z, s) \end{bmatrix} = \mathbf{Q}(s) \begin{bmatrix} \mathbf{V}(z, s) \\ \mathbf{I}(z, s) \end{bmatrix} + \begin{bmatrix} \mathbf{V}_F(z, s) \\ \mathbf{I}_F(z, s) \end{bmatrix}, \quad (2.1)$$

where

$$\mathbf{Q}(s) = \begin{bmatrix} 0 & -(\mathbf{R} + s\mathbf{L}) \\ -(\mathbf{G} + s\mathbf{C}) & 0 \end{bmatrix}, \quad (2.2)$$

$$\mathbf{V}_{\mathbf{F}}(z, s) = s \begin{bmatrix} \vdots \\ \int_a^{\dot{a}} \vec{\mathbf{B}}^i \odot \vec{a}_n dl \\ \vdots \end{bmatrix} \quad (2.3)$$

and

$$\mathbf{I}_{\mathbf{F}}(z, s) = -(\mathbf{G} + s\mathbf{C}) \begin{bmatrix} \vdots \\ \int_a^{\dot{a}} \vec{\mathbf{E}}_t^i \odot d\vec{l} \\ \vdots \end{bmatrix}. \quad (2.4)$$

Here, $\mathbf{V}$ and $\mathbf{I}$ represent the voltage and current vectors along the lines as a function of distance (z) and frequency (s). $\mathbf{R} \in \Re^{n \times n}$, $\mathbf{L} \in \Re^{n \times n}$, $\mathbf{G} \in \Re^{n \times n}$ and $\mathbf{C} \in \Re^{n \times n}$ are the per unit length (p.u.l.) parameter matrices of the MTL. The p.u.l. voltage and current vectors, $\mathbf{V}_{\mathbf{F}}$ and $\mathbf{I}_{\mathbf{F}}$, represent the effect of the EMI on the lines. $\vec{\mathbf{B}}^i$ and $\vec{\mathbf{E}}_t^i$ are the incident magnetic and transverse electric field vectors, respectively and $\odot$ denotes dot product. The integrals of the fields are evaluated from the position of the reference conductor to the k^{th} conductor in the transverse direction as shown in Fig. 2.4 (here, a single reference strip is assumed - expressions for a ground plane are similar and would be discussed later). Premultiplying both sides of (2.1) by $e^{-\mathbf{Q}(s)z}$ and regrouping, we get,

$$e^{-\mathbf{Q}(s)z} \frac{\partial}{\partial z} \begin{bmatrix} \mathbf{V}(z, s) \\ \mathbf{I}(z, s) \end{bmatrix} - e^{-\mathbf{Q}(s)z} \mathbf{Q}(s) \begin{bmatrix} \mathbf{V}(z, s) \\ \mathbf{I}(z, s) \end{bmatrix} = e^{-\mathbf{Q}(s)z} \begin{bmatrix} \mathbf{V}_{\mathbf{F}}(z, s) \\ \mathbf{I}_{\mathbf{F}}(z, s) \end{bmatrix}. \quad (2.5)$$

Figure 2.4: Incident field coupling for the k^{th} line.

The above equation can be rewritten as,

$$\frac{\partial}{\partial z} \left\{ e^{-\mathbf{Q}(s)z} \begin{bmatrix} \mathbf{V}(z, s) \\ \mathbf{I}(z, s) \end{bmatrix} \right\} = e^{-\mathbf{Q}(s)z} \begin{bmatrix} \mathbf{V}_F(z, s) \\ \mathbf{I}_F(z, s) \end{bmatrix}. \quad (2.6)$$

Integrating (2.6) on both sides with respect to the distance, from 0 to d , we get,

$$e^{-\mathbf{Q}(s)d} \begin{bmatrix} \mathbf{V}(d, s) \\ \mathbf{I}(d, s) \end{bmatrix} - \begin{bmatrix} \mathbf{V}(0, s) \\ \mathbf{I}(0, s) \end{bmatrix} = \int_0^d e^{-\mathbf{Q}(s)z} \begin{bmatrix} \mathbf{V}_F(z, s) \\ \mathbf{I}_F(z, s) \end{bmatrix} dz. \quad (2.7)$$

Hence,

$$\begin{bmatrix} \mathbf{V}(d, s) \\ \mathbf{I}(d, s) \end{bmatrix} = e^{\mathbf{Q}(s)d} \begin{bmatrix} \mathbf{V}(0, s) \\ \mathbf{I}(0, s) \end{bmatrix} + \mathbf{J}(s), \quad (2.8)$$

where d is the length of the lines and $\mathbf{J}(s)$ is the convolution integral given by [20]

$$\mathbf{J}(s) = \int_0^d e^{\mathbf{Q}(s)(d-z)} \begin{bmatrix} \mathbf{V}_F(z, s) \\ \mathbf{I}_F(z, s) \end{bmatrix} dz. \quad (2.9)$$

In (2.8), the first term on the right-hand side, $e^{\mathbf{Q}(s)d}$, corresponds to the solution of the homogeneous part of the equation in (2.1), representing the behaviour of the unexcited MTL (the term *unexcited* is used to refer to MTLs which are not exposed to external EMI in this thesis). The convolution integral $\mathbf{J}(s)$ represents the effect of the incident fields on the line. Note that both these terms do not have a direct time-domain representation. However, nonlinear devices, which are connected to these high-speed interconnects in a VLSI circuit, are best represented in the time-domain. This gives rise to the problem of mixed frequency/time while performing EMI analysis using nonlinear circuit simulators [1–5, 20, 23].

In order to address this issue, several modeling and simulation techniques have been proposed in the literature [24–27]. Below is a brief summary of these algorithms.

1. **Lumped segmentation:** The conventional lumped segmentation model is a straightforward solution to the mixed frequency/time problem [28]. Here, the lines are divided into small segments. Each segment contains a lumped resistance, inductance, capacitance and conductance calculated from the p.u.l. parameters of the MTL and the length of the segment. The effects of EMI are represented using lumped voltage and current sources derived from

the corresponding discretization of the p.u.l. voltage and current terms on the right-hand side of (2.1).

2. **Method of characteristics:** The method of characteristics (MoC) [20] is a popular technique for modeling interconnects in the time-domain . In this method, the time-domain characteristics of interconnects in the presence of EMI are numerically computed including frequency-dependent losses. The interconnect characteristics are then modeled using rational functions and ideal delay modules. Method of characteristics provides an analytical closed form representation for lossless lines. When applied to lossy lines, the interconnect characteristics and the equivalent sources due to EMI do not have an analytical form in time-domain. Hence, they must be evaluated numerically using appropriate curve fitting techniques in time-domain or frequency-domain. However, these approaches may suffer from non-convergence and non-passivity. It is to be noted that preserving the passivity of the interconnect macromodels is a very important in circuit simulation. This is because stable but non-passive models when terminated with other passive models can lead to unstable global transient simulation.
3. **Matrix rational approximation:** The matrix rational approximation (MRA) method [26] was suggested to overcome the above discussed passivity

related difficulties in the modeling of lossy coupled transmission lines,. In this method, the interconnect response is approximated using closed form expressions, computed as a function of per unit length parameters of the interconnects. Passivity is guaranteed by construction in the MRA macromodel. The MRA technique is shown to be more efficient than either MoC or the lumped segmentation technique. However, this technique becomes inefficient for long low loss lines, which are more likely to be exposed to EMI. This is because these lines, which have huge delays, require higher orders of approximation resulting in a higher complexity of the corresponding time-domain macromodels. In addition, since this method requires intermediate steps consisting of numerical inversion of matrices, this approach is not fully analytical.

4. **Delay extraction based passive macromodels:** Recently, a new technique for the EMI analysis of high-speed interconnects based on DEPACT (delay extraction and passive compact transmission-line) macromodeling algorithm was proposed [22,27]. Using this approach, the MTL structure is divided into cells consisting of individual lossless and lossy segments. The DEPACT macromodel was shown to capture the characteristics accurately, even for interconnects with long delays, while keeping the order of the macromodel low. For representing the effects of EMI, semi-analytical models,

consisting of near and far-end sources, as well as fully analytical models, consisting of distributed sources, have been developed [22]. These models were appropriately incorporated for analysis while using the DEPACT macromodel [22, 27].

All the macromodels discussed above consist of 3 steps:

- 1) computing an appropriate macromodel representing the unexcited MTLs,
- 2) finding an equivalent circuit representation for the convolution integral in (2.9) (representing the effect of incident fields on the lines),
- 3) combining the equivalent circuits of the unexcited interconnect macromodel and the sources due to EMI during transient analysis.

In the conventional methods, the computation of sources representing the effect of EMI (step 2) becomes inefficient. This is especially so, when we consider the practical cases of interconnect structures with a large number of coupled lines. For example, consider the calculation of near and far-end equivalent sources of an MTL structure subjected to EMI [27]. Employing an IFFT-based approach for this purpose requires $O(n^3 N_f)$ computations for evaluating frequency-domain sources, followed by $O(n N_f \log N_f)$ computations for conversion into the time-domain, where n is the number of lines and N_f is the number of frequency points taken into consideration.

Figure 2.5: CPU cost of EMI analysis (lumped macromodel + HSPICE) for varying number of coupled interconnects.

For a recursive convolution based approach given in [27], the above cost amounts to $O(n^2 N_t)$, where N_t is the number of time points considered.

Another common feature of all the above methods is that the average cost of simulating an n -coupled line structure is n^β , where $3 < \beta < 4$, a prohibitively time-consuming task, especially for the case of large coupled interconnects. This is because, the complexity of conventional interconnect macromodels grows approximately at a rate of n^2 , while the CPU expense of simulating a circuit of size P is proportional to P^α , with $1.5 < \alpha < 2$ depending upon the sparsity of the macromodel. This is demonstrated in Fig. 2.5, which shows the CPU time for EMI analysis of a uniform MTL

structure with varying number of coupled conductors using conventional techniques.

From the above discussion, it is evident that the computational complexity of the EMI analysis increases drastically with the increase in the number of lines and poses a significant challenge to existing circuit simulators. In order to address this difficulty, a new algorithm for EMI analysis based on waveform relaxation techniques is presented in Chapter 4.

In the next section, power integrity issues, and the associated modeling/analysis challenges are discussed.

2.2 Power Integrity

Preserving power integrity has become one of the challenging tasks facing the designers of modern multifunction and miniature electronic products. These products warrant mixed-domain integration of heterogeneous circuit components such as digital, analog, RF, optical and micro-electro-mechanical (MEMS) devices and consequently, require diverse power management strategies. In addition, as devices scale and more transistors are integrated into a single integrated circuit, the power and current levels are expected to increase with a corresponding decrease in voltage. With gigabit signals being propagated through the package and board, the ability to supply clean power to the transistor circuits becomes very critical. These issues make the design of robust and reliable power distribution networks (PDNs) consisting of chip, package

Figure 2.6: Inverter circuit (driver and receiver).

and printed circuit boards, essential to the success of the high-speed products.

In this section, the power distribution network and the power integrity issues in a modern VLSI design are described. Also, a literature survey of modeling and analysis techniques is provided.

2.2.1 Transistor and power delivery switching

The role of power delivery in the operation of active devices must be examined in order to understand the significance of PDNs in VLSI designs. Modern VLSI circuits are

built using complementary metal oxide semiconductor (CMOS) field effect transistors (MOSFETs), which are connected in various configurations between power supply and ground. These transistors operate as multi-terminal switches, which direct current from the power supply to ground based upon the control signal given to them as input. There are two kinds of MOSFETs: NMOS (n-channel) transistor and PMOS (p-channel) transistor. For NMOS, a negative gate voltage has to be applied to turn it OFF. For PMOS, on the other hand, a positive gate voltage has to be applied to turn it OFF. These two transistors can be combined to form an inverter, which is one of the basic building blocks of any IC, as shown in Fig. 2.6.

Here, the circuit is made up of two CMOS inverters, a driver and a receiver, connected via an interconnect. The inverter circuit is connected to a power supply (shown as V_{DD} and Gnd terminals).

Since the gate of a receiver transistor has some capacitance (formed between the gate and the substrate), when the output of the driver is on, it charges the input capacitance of the receiver [29]. This is illustrated by considering a logic level low input to the driver in Fig. 2.7(a). The PMOS transistor here is now ON and the NMOS is OFF. Hence, there is a direct path between the V_{DD} and the input capacitance of the receiver through the interconnect. Current flows through this path and the input capacitance of the receiver is charged to logic level high. Similarly, when the input to the driver changes to logic level high, the PMOS is turned OFF and the NMOS

Figure 2.7: Input capacitance of receiver being (a) charged and (b) discharged, as the driver circuit switches states.

is turned ON. This creates a direct path between the input capacitance of receiver (C_R) and the Gnd terminal, through which it discharges until reaching a voltage level corresponding to logic level low (as shown in Fig. 2.7(b)). The speed at which the circuit operates is determined by how quickly the capacitor can be charged or discharged through the switches.

The power supply (which is the source of voltage and current) is typically bulky and cannot be connected directly to the V_{DD} and Gnd terminals of the active circuits in the IC. Therefore, wires (interconnects) are used to establish this connection.

Figure 2.8: Current drawn by a CMOS inverter, with an input square wave.

However, these interconnects have parasitics (resistance, inductance, capacitance etc.) associated with them. This interconnection framework, called the power distribution network (PDN), supplies the transistors with sufficient voltage and current for them to switch states. Fig. 2.8 shows the switching current drawn from the V_{DD} terminal by a CMOS inverter (built around a 180nm process technology with an ideal 1.8V power supply) when excited with an input square wave. When this current flows through a non-ideal PDN with parasitics, voltage drops and fluctuations are encountered. The

Figure 2.9: Switching noise due to voltage fluctuations in the PDN.

voltage fluctuation across the V_{DD} and Gnd terminals of the transistors can cause the following problems with the transistor operations [30]:

1. Voltage drop across the power supply terminals of the IC slows down the transistor operation, or some times even prevents transistors from switching states.
2. Voltage fluctuation caused by an active transistor circuit leaking into a quiet

transistor (as shown in Fig. 2.9) can cause incorrect switching of the quite transistor circuit at the far end of a communication path along with crosstalk from neighboring signal lines. This voltage fluctuation across the power supply of the IC is called simultaneous switching noise (SSN), since it occurs only during the switching of transistors.

3. Can lead to timing margin errors due to the degraded waveforms at the output of the drivers.

2.2.2 Significance of power distribution in VLSI circuits

Modern digital VLSI circuits (for example microprocessors) contain millions of CMOS transistors interconnected through wires in a very complex manner. The operating speed of a microprocessor is limited by both gate (or transistor) delays and interconnect delays. There is a strong relationship between the operating voltage and the gate delays. The inverse of switching delay of a logic circuit (which influences the maximum frequency of operation, F_{max}) is proportional to the gate voltage. This is because the strength of the gate-source voltage determines the conductivity of the channel formed in a MOSFET, which in turn determines how fast the logic levels of the gates can be switched.

This relationship is described for a microprocessor in [31]. Near the nominal operating voltage, a linear relationship is observed between the maximum frequency

Figure 2.10: Components of a power distribution network.

of a microprocessor and the voltage. Around the nominal operating voltage, there is a window of fluctuation specified by the designer, for the acceptable operation of the microprocessor. The power distribution network must be designed properly to ensure that the fluctuations in the operating voltage of the chip remains within these acceptable limits provided by the designer.

2.2.3 Components of a power distribution network

A PDN consists of a power supply, DC-DC converters (also called voltage regulator modules, or VRMs), decoupling capacitors, and interconnections that provide the

Figure 2.11: Schematic of a power distribution network.

path for the supply and removal of charge to and from the switching circuits [30]. A typical power distribution network for a VLSI circuit on a PCB is shown in Fig. 2.10. The power supply module provides high voltage and high current to the PCB. This voltage is appropriately reduced in the DC-DC converter and supplied through the power/ground planes and interconnects on the PCB, to the IC. The decoupling capacitors are distributed across the PCB and act as reservoirs of charge. They provide the switching circuits with charge as needed. The interconnects from the board and the package are then connected to the on-chip power distribution networks. These on-chip PDNs are constructed as multilayer grids of metal. A schematic of the PDN is shown in Fig. 2.11. The input voltage V_{IN} here comes from the power supply mod-

ule. The voltage regulator module (VRM) typically consists of a pass element, a low pass filter to remove high frequency noise, and a comparator in the feedback. The power is then fed through the decoupling capacitors and power planes, to the on-chip metallization layers via the package interconnects.

Design of on-chip power distribution networks is highly challenging because of the continual scaling of CMOS devices, increase in switching speeds and circuit densities. In addition, increasing density of on-chip interconnects has led to a reduction in their widths. This results in increase in the resistances of the on-chip interconnects adding to the resistance of the PDN.

Hence, analysis of voltage drops and currents becomes crucial in the early stages of the design of on-chip power distribution networks. Also, due to the reduced timing and power margins, the concurrent analysis of signal and power integrity aspects becomes important. In many cases, these analyses require not just a simple estimation of statistical average power consumption of the chip using DC simulations, but also a detailed study of the effects of voltage and current transients generated by the sporadic and sudden switching of specific functional blocks [32]. This mandates the development of an efficient method for time-domain simulation of on-chip PDNs.

Figure 2.12: Power grid components.

2.2.4 On-chip power distribution networks

Typically, power distribution in an integrated circuit is done hierarchically, starting from the top-level metal layer, which is connected to the package, down through interlayer vias, and finally to the active devices. Adjacent layers have metal lines laid out at right angles to each other. The power is fed to the top layers from the package through interconnects contacts, called V_{DD} (or Gnd). The functional blocks such as logic gates, memory units, latches, etc., in the active layers act as power drains, drawing current from the PDN at the bottommost layer. A 3-D visualization of a simple 2-layer PDN is shown in Fig. 2.12.

The behavior of on-chip PDNs is largely governed by the type of package interconnection made between the IC and the PCB. The two most commonly used packages

Figure 2.13: Wire bond package.

are of types, wire bond and flip chip [33]. In wire bond packages, the connection between the IC and PCB is made using wires soldered to pads patterned at the edges of the IC as shown in Fig. 2.13. In flip chip packages (also known as Controlled Collapse Chip Connection, C4), the ICs are connected to the external circuitry with solder bumps that have been deposited onto the chip pads on the top side of the wafer during the final wafer processing step. In order to mount the chip to the PCB, it is flipped over so that its top side faces down, and aligned so that its pads align with matching pads on the external circuit, and then the solder is flowed to complete the interconnect as shown in Fig. 2.14.

Figure 2.14: Flip chip package.

2.2.4.1 Wirebond vs Flipchip

Both wire bond and flip chip packages have their merits and disadvantages. Wire bonding is highly cost effective and flexible when compared to flip chip packages. The flip chip packages are not suitable for easy replacement or manual installation. They also require very flat surfaces to mount to, which is not always easy to arrange, or sometimes difficult to maintain as the boards heat and cool. Also, the short C4 connections are very stiff, so the thermal expansion of the chip must be matched to the supporting board to prevent the connections from cracking.

However, performance wise flip chip packages are far superior to the wire bond

packages. This is because, as seen from Fig. 2.13, the V_{DD} or Gnd contacts from the board in wire bond packages are limited to the edges of the on-chip PDN. This implies that active devices in the core of the IC are farther away from the power supply contacts than those along the edges, and hence are connected to power supply through more resistive paths. This results in the core of the chip being *voltage starved*, adding additional design constraints for the designer in terms of cell placement and layout. In flip chip packages, the V_{DD} and Gnd are made at regular intervals across the face of the IC, making the power distribution much more uniform. In addition, the flip chip assembly is much smaller than the wire bond package, both in area and height. The chip sits directly on the PCB and the resulting short wires greatly reduce interconnect parasitics from the package such as inductance, allowing relatively higher-speed signals, and also improve heat conduction. Because of these advantages, flip chip packages have become much more popular among many low power, small size VLSI applications in the recent years, compared to wire bond packages. The focus of this thesis is the analysis of a flip chip based on-chip PDN.

2.2.5 Modeling of on-chip PDN

The type of models to be used to describe power grid depends on the purpose, accuracy and efficiency desired by the designer. A full-wave electromagnetic model for the metallization layers (used in conjunction with sophisticated nonlinear circuits

representing the active devices), although very accurate, is highly CPU expensive and hence may not be desirable in the context of large-scale simulation and design. Hence, approximations are made at various hierarchical levels to obtain a trade-off between accuracy and run time.

Since the on-chip metal interconnects are predominantly resistive and capacitive in nature, RC models are employed to describe the power grid in the analyses in this thesis [34]. Metal segments between vias are modeled as lumped resistors. The via resistances are typically ignored. Capacitances are connected between each node in the grid and the ground to account for the capacitive effects in the PDN. As a result, a mesh type structure of resistances is obtained. Hence, on-chip PDNs are referred to as power grid networks or simply power grids.

V_{DD} contacts from the package, which are placed on top metal layer at uniform intervals in a flip chip package, are modeled as ideal voltage sources. The nonlinear switching devices (i.e active power drains shown in Fig. 2.12) are replaced by time-varying current sources consisting of the static and dynamic switching currents drawn by these devices (as shown in Fig. 2.8). A typical switching current waveform used for such time-varying current sources is shown in Fig. 2.15. For a modern integrated circuit such as a microprocessor, such a network can easily include millions of nodes and elements.

Figure 2.15: An example transient current source waveform for representing active power drains in the PDN.

2.2.6 Conventional methods of analyzing power grid networks

The behavior of the power grid network can be expressed using modified nodal analysis (MNA) as follows:

$$\mathbf{G}\mathbf{X}(t) + \mathbf{C}\dot{\mathbf{X}}(t) = \mathbf{b}\mathbf{u}(t), \quad (2.10)$$

where $\mathbf{X}(t)$ represents the vector of voltages on the nodes of the circuit, $\mathbf{G}$ and $\mathbf{C}$ are the conductance and capacitance matrices of the circuit, $\mathbf{u}(t)$ is the vector of inputs to the circuit and $\mathbf{b}$ is a selection matrix. The power grid network for integrated circuits can consist of millions of nodes and circuit elements. This results in very large MNA matrices, leading to computationally expensive and time consuming transient simulations. Several simulation techniques have been proposed in the literature to

Figure 2.16: Reduction of power grid in the Multigrid method.

address these issues [34–42]. Some of these techniques are examined in the following subsections.

2.2.6.1 Multigrid method

A multigrid-like technique for power grid analysis was proposed in [34]. In this method, the power grid is reduced by removing the nodes via coarsening, as shown in Fig. 2.16. Next, the resulting smaller grid is simulated at each time-point in the time-interval of interest. Finally, the results of the reduced grid is interpolated back on to the original grid through algebraic multigrid (AMG) interpolation.

For the purpose of illustration, consider the following system of linear equations representing the power grid problem to be solved,

$$\mathbf{A}\mathbf{X} = \mathbf{b}, \quad (2.11)$$

where $\mathbf{X} \in \mathbb{R}^N$, $\mathbf{b} \in \mathbb{R}^N$ and $\mathbf{A} \in \mathbb{R}^{N \times N}$. The above equation is first reduced using reduction operator $\Omega_h \in \mathbb{R}^{N \times N_h}$ as follows,

$$(\Omega_h^T \mathbf{A} \Omega_h) \mathbf{X}_h = (\Omega_h^T \mathbf{b}), \quad (2.12)$$

or

$$\mathbf{A}_h \mathbf{X}_h = \mathbf{b}_h, \quad (2.13)$$

where $\mathbf{X}_h \in \mathbb{R}^{N_h}$, $\mathbf{b}_h \in \mathbb{R}^{N_h}$ and $\mathbf{A}_h = \Omega_h^T \mathbf{A} \Omega_h \in \mathbb{R}^{N_h \times N_h}$, with $N_h < N$. This reduced problem is solved and the results are mapped back onto the original grid using the interpolation operator,

$$\mathbf{X} = \Omega_h \mathbf{X}_h. \quad (2.14)$$

Depending upon the accuracy and efficiency desired, many levels of reduction can be applied to the grid, resulting in a much smaller problem to be solved. Since size of the problem being actually solved (N_h) is smaller than the original problem size, the computation time is considerably reduced. However, the interpolation of the results from the coarse grid onto the fine grid creates unpredictable errors. There is no direct relationship between the level of coarsening applied and the maximum error obtained in the solution. Hence, the power grid circuit is solved only approximately.

Figure 2.17: Partitioning of power grid in the Hierarchical analysis.

2.2.6.2 Hierarchical analysis

In [36], a hierarchical analysis technique is proposed. Here, the power grid is divided into a global partition and multiple local partitions as shown in Fig. 2.17. Each local partition is simulated separately and their behavior is captured using low-order macromodels. These macromodels are then input as multi-port circuit elements at the corresponding interface nodes in the global partition, and the resulting reduced grid is simulated. Approximations are made during the macromodeling of the local partitions in order to maintain sparsity and efficiency. Hence, this method sacrifices a certain degree of accuracy towards achieving lower time and memory requirements.

2.2.6.3 Random walks method

A simulation technique based on the classical random walks method in statistics is proposed in [38,39]. In this technique, the travelling salesman algorithm is applied to find the voltage at each individual node. For a brief illustration, consider the following experiment. The node being solved is taken as the starting point for the salesman. The salesman travels to one of the neighboring nodes randomly. The probability that the salesman travels from node A to neighboring node B is proportional to the conductivity between these two nodes. At the neighboring node, if there is a current load present (also called *motel*), he loses money (according to the Kirchoff's current law requirement at that node) and resumes the journey to another neighboring node. If there is a DC voltage source (V_{DD} or Gnd contact, also called *home*) at that node, the salesman gains money and the journey ends. Several such experiments are performed for the given node, and the average money (voltage) obtained for all the experiments is calculated to be the voltage at that node.

Here again, the number of experiments needed to be run in each case for obtaining accurate results is difficult to determine, and the resulting node voltages are prone to unpredictable errors.

2.2.6.4 Successive over-relaxation method

In this method, the classical successive over-relaxation (SOR) iterative technique is applied to solve for the node voltages of the power grid [41,42]. The power grid is first divided into subcircuits consisting of individual nodes (or rows). The node voltages of the grid are initialized using an appropriate initial-guess. In a given iteration, each node (or row) is simulated independently assuming that the voltages of the other nodes (or rows) are already known. The solution set of the current iteration is updated as soon as a node (or row) has been simulated. The above process is repeated for every time point in the simulation.

For faster convergence, the successive over-relaxation method uses the information from the previous iteration to correct the results for the current iteration. For example, if $\bar{V}_i^r$ is the voltage of the i^{th} node obtained from simulation in the r^{th} iteration at a given time point, then this voltage is corrected using the following equation:

$$V_i^r = \omega \bar{V}_i^r + (1 - \omega)V_i^{r-1}, \quad (2.15)$$

where ω is a weighting factor. It is to be noted that the rate of convergence of the SOR method is highly sensitive to this weighting factor. Hence, the optimum value for the weighting factor for the given problem (ω_{opt}), which results in the fastest convergence of the iterations, has to be determined accurately. For a regular power grid circuit with equal resistances everywhere, the value of ω_{opt} can be analytically

computed as follows. Let $\mathbf{A}$ is the matrix defining the linear system of equations as given in (2.11), and $\mathbf{B} = \mathbf{I} - \mathbf{D}^{-1}\mathbf{A}$, where $\mathbf{I}$ is an $N \times N$ identity matrix. Then, the value of ω_{opt} is given by,

$$\omega_{opt} = \frac{2}{1 + \sqrt{1 - S(\mathbf{B})^2}}, \quad (2.16)$$

where $S(\mathbf{B})$ is the spectral radius (magnitude of the eigenvalue with the largest absolute value) of the matrix $\mathbf{B}$. The value of ω_{opt} can be either found by trial and error or by using the above formula, both of which result in excessive CPU cost. Moreover, typical power grid circuits are made up of multiple layers of metallizations in a chip and so are nonuniform in nature, with different resistances at different points on the grid. Hence, the analytical definition of ω_{opt} described above does not hold true in such scenarios.

2.2.7 Direct vs. Iterative methods

In general, the techniques discussed above can be categorized into direct-solver methods (multigrid method, hierarchical analysis) and iterative methods (random walks method, SOR method). In [34], it was shown that direct solvers offer better speed-ups over iterative solvers for the analysis of power grids, where smooth spatial variations in potential are observed. However, direct solver based methods suffer from high memory consumption and are not suitable for implementation on the emerging parallel computing platforms. Iterative solvers, on the other hand, converge very slowly

but are memory efficient and can easily be parallelized.

In Chapter 5, a new algorithm for transient analysis of power grids is presented. This method is based on the waveform relaxation techniques and combines the merits of both direct and iterative solvers.

Chapter 3

Review of waveform relaxation techniques

As discussed in the previous chapter, conventional circuit simulation techniques face difficulties while handling large, dense systems, that are encountered in EMI and power integrity analysis. In order to address these difficulties, in this thesis, waveform relaxation based techniques are advanced to handle EMI and power integrity analysis of high-speed modules. In this chapter, a brief review of waveform relaxation is presented as relevant to this thesis. In Section 3.1, the conventional circuit simulation techniques are examined. In Section 3.2, the mathematical formulation behind the waveform relaxation techniques are presented. In Section 3.3, the convergence of the WR algorithm is discussed.

3.1 Traditional simulation methods

Conventional circuit simulators like SPICE used for VLSI design are based on the following standard techniques for transient simulation:

1. Convert the circuit description into a matrix-based system of algebraic-differential equations using modified nodal analysis (MNA).
2. Convert the algebraic-differential equations into a system of algebraic equations describing the behaviour of the circuit in the time interval of interest, using stiffly stable implicit methods like the backward Euler formula.
3. Linearize the system of nonlinear algebraic equations at each time-step, using Newton-Raphson iterations .
4. Solve the system of linear algebraic equations, using sparse matrix techniques based methods like LU decomposition and Gaussian elimination.

In the context of VLSI circuits, the requirement is to solve very large system of equations at each time point. Consequently, the circuit simulators end up taking excessive memory and CPU time for analysis of large-scale circuits.

3.1.1 Conventional iterative techniques

In order to increase the speed of simulation, alternate approaches were suggested for some of the above mentioned standard features of circuit simulation. For example, for large circuits the linearized system at each time point was simulated using iterative techniques instead of using exact solution methods. Although this resulted in some reduction of CPU time and memory resources, convergence of the system solution at each time step became sensitive to the choice of the step-size. As a result, in some cases, the size of the time step had to be chosen to be very small in order to avoid instability of the Newton-Raphson iterations.

3.2 Waveform relaxation

In order to address the above discussed difficulties, the waveform relaxation (WR) technique for circuit simulation was introduced in the early 1980s for the simulation of VLSI circuits [6–10]. The basic idea is to apply relaxation directly to the system of equations describing the circuit. As a result, the system is divided into decoupled subsystems of algebraic-differential equations, representing decoupled subcircuits. Each decoupled subcircuit is simulated for the entire time-interval of interest using the standard simulation techniques (this is the major difference between waveform relaxation and conventional iterative techniques like the SOR method described

in Section 2.2.6.4). This provided two main advantages. First, since each subcircuit is simulated using conventional techniques as if it were a separate circuit, accuracy of the simulation results within a given iteration is improved with little investment in memory. Second, different integration methods and different step-sizes may be used for the numerical integration of different subcircuits depending on the local error requirements, thereby removing the dependence of convergence on the integration techniques and step-sizes.

3.2.1 Mathematical formulation of the WR method for a general dynamical system

Consider a dynamical system described by a system of implicit algebraic-differential equations of the form,

$$\mathbf{F}(\dot{\mathbf{y}}, \mathbf{y}, \mathbf{u}) = \mathbf{0}, \quad (3.1)$$

where $\mathbf{u}(t) \in \mathbb{R}^p$ is the vector of input variables at time t , and $\mathbf{F} \in \mathbb{R}^n$ is a continuous function describing the dynamic behaviour of the system. $\mathbf{y}(t) \in \mathbb{R}^n$ is the vector of unknown variables at time t and $\dot{\mathbf{y}}(t) \in \mathbb{R}^n$ is the time derivative of $\mathbf{y}(t)$ with known initial conditions,

$$\mathbf{y}(0) = \mathbf{y}_0, \dot{\mathbf{y}}(0) = \mathbf{0}. \quad (3.2)$$

In circuit simulation, the above initial conditions are obtained from the DC solution of the system.

The general structure of a WR algorithm for analyzing (3.1) for a given time interval of $[0, T]$ consists of two major steps, namely, the *partitioning* and the *relaxation process*. In the partitioning process, the system is divided into m decomposed subsystems and correspondingly m equations are written, which are derived from (3.1) as follows:

$$\begin{bmatrix} \mathbf{F}_1(\dot{\mathbf{y}}_1, \mathbf{y}_1, \mathbf{d}_1, \mathbf{u}) \\ \mathbf{F}_2(\dot{\mathbf{y}}_2, \mathbf{y}_2, \mathbf{d}_2, \mathbf{u}) \\ \vdots \\ \mathbf{F}_m(\dot{\mathbf{y}}_m, \mathbf{y}_m, \mathbf{d}_m, \mathbf{u}) \end{bmatrix} = \mathbf{0}, \quad (3.3)$$

where for $i = 1, 2, \dots, m$, $\mathbf{y}_i \in \mathbb{R}^{n_i}$ is the subvector of unknown variables assigned to the i^{th} partitioned subsystem, $n_1 + n_2 + \dots + n_m = n$, $\mathbf{F}_i \in \mathbb{R}^{n_i}$ and $\mathbf{d}_i = \text{col}(\mathbf{y}_1, \dots, \mathbf{y}_{i-1}, \mathbf{y}_{i+1}, \dots, \mathbf{y}_m, \dot{\mathbf{y}}_1, \dots, \dot{\mathbf{y}}_{i-1}, \dot{\mathbf{y}}_{i+1}, \dots, \dot{\mathbf{y}}_m)$, with

$$\text{col}(a, b) \equiv \begin{bmatrix} a \\ b \end{bmatrix}. \quad (3.4)$$

It is clear that the vectors $\mathbf{d}_i$ are treated as inputs and convey the information from one subsystem to another. Hence, they are called the *decoupling* vectors of the subsystems.

The relaxation process is an iterative process. The relaxation process starts with an initial-guess of the solution waveforms of the original dynamical equations (3.1) in order to initialize the approximate waveforms for the decoupling vectors. During

each iteration, each decomposed subsystems is solved for its assigned variables in the given time interval $[0, T]$ by using the approximate waveform of its decoupling vector. Two most commonly used types of relaxation, namely, *Gauss-Jacobi* (GJ) and *Gauss-Seidel* (GS) relaxation, are discussed below. For the GJ relaxation, all waveforms of the decoupling vectors are updated, based on the results obtained in a given iteration, at the beginning of the next iteration. For the GS relaxation, the waveforms solution obtained by solving one decomposed subsystem is immediately used to update the approximate waveforms of the decoupling vectors of the other subsystems, within a given iteration. The relaxation process is carried out repeatedly until satisfactory convergence is achieved.

The general structure of a WR algorithm can be formally described as follows.

Let the superscript r denote the iteration count.

Step 1: Partition the system in (3.1) into m subsystems as given by (3.3).

Step 2: Set $r = 1$ and initialize the waveforms for the unknown vectors ($\mathbf{y}^0(t); t \in [0, T]$) such that $\mathbf{y}^0(0) = \mathbf{y}_0$.

Step 3: For each $i = 1, 2, \dots, m$, set

$$\mathbf{d}_i^r = \text{col}(\mathbf{y}_1^{r-1}, \dots, \mathbf{y}_{i-1}^{r-1}, \mathbf{y}_{i+1}^{r-1}, \dots, \mathbf{y}_m^{r-1}, \dot{\mathbf{y}}_1^{r-1}, \dots, \dot{\mathbf{y}}_{i-1}^{r-1}, \dot{\mathbf{y}}_{i+1}^{r-1}, \dots, \dot{\mathbf{y}}_m^{r-1}) \quad (3.5)$$

for GJ relaxation, or

$$\mathbf{d}_i^r = \text{col}(\mathbf{y}_1^r, \dots, \mathbf{y}_{i-1}^r, \mathbf{y}_{i+1}^{r-1}, \dots, \mathbf{y}_m^{r-1}, \dot{\mathbf{y}}_1^r, \dots, \dot{\mathbf{y}}_{i-1}^r, \dot{\mathbf{y}}_{i+1}^{r-1}, \dots, \dot{\mathbf{y}}_m^{r-1}) \quad (3.6)$$

Figure 3.1: Test circuit for waveform relaxation

for GS relaxation. Solve for $(\mathbf{y}_i^r(t); t \in [0, T])$ using

$$\mathbf{F}_i(\dot{\mathbf{y}}_i^r, \mathbf{y}_i^r, \mathbf{d}_i^r, \mathbf{u}) = \mathbf{0}. \quad (3.7)$$

Step 4: $r = r + 1$ and go to Step 3.

3.2.2 The WR method for a MNA based system of circuits

In this section, a simple circuit is used to illustrate the WR process as applied to the MNA formulation. Consider a simple 2 node circuit as shown in Fig. 3.1.

The MNA formulation of this circuit using Kirchhoff's current law (KCL) gives rise to the following equations:

$$\begin{bmatrix} G_1 + G_3 & -G_3 \\ -G_3 & G_2 + G_3 \end{bmatrix} \begin{bmatrix} v_1(t) \\ v_2(t) \end{bmatrix} + \begin{bmatrix} C_1 & 0 \\ 0 & C_2 \end{bmatrix} \begin{bmatrix} \dot{v}_1(t) \\ \dot{v}_2(t) \end{bmatrix} = \begin{bmatrix} I_s(t) \\ 0 \end{bmatrix}, \quad (3.8)$$

where $G_1 = 1/R_1$, $G_2 = 1/R_2$ and $G_3 = 1/R_3$. $v_1(t)$ and $v_2(t)$ are the time-domain voltage waveforms at the nodes 1 and 2, with initial conditions, $v_1(0) = v_{1,0}$ and

Figure 3.2: Partitioned subcircuits with Relaxation sources

$v_2(0) = v_{2,0}$, respectively. Next, the circuit is partitioned into 2 parts- one containing node 1 and the other node 2. Physically, the resistor R_3 is the coupling element between these two subcircuits and hence, the coupling functions to be incorporated must constitute the current flowing through this resistor from node 1 to 2, written as a function of the their voltages. Hence, modifying (3.8), the following equations are obtained.

$$G_1 v_1(t) + C_1 \dot{v}_1(t) = I_s(t) - G_3 (v_1(t) - v_2(t)), \quad (3.9)$$

$$G_2 v_2(t) + C_2 \dot{v}_2(t) = -G_3 (v_2(t) - v_1(t)), \quad (3.10)$$

or

$$G_1 v_1(t) + C_1 \dot{v}_1(t) = I_s(t) - I_{WR1}(t), \quad (3.11)$$

$$G_2 v_2(t) + C_2 \dot{v}_2(t) = -I_{WR2}(t), \quad (3.12)$$

where I_{WR1} and I_{WR2} are called waveform relaxation (WR) sources. These sources implement the functions corresponding to the decoupling vectors in (3.3). Considering

r^{th} iteration of a GJ based relaxation process, these WR sources can be written as

$$I_{WR1}^r(t) = G_3 \left(v_1^{r-1}(t) - v_2^{r-1}(t) \right), \quad (3.13)$$

$$I_{WR2}^r(t) = G_3 \left(v_2^{r-1}(t) - v_1^{r-1}(t) \right). \quad (3.14)$$

The WR algorithm is started by initializing these WR sources using the initial-guess waveforms, $v_1^0(t)$ and $v_2^0(t)$ and then updating them at the end of each iteration using the new voltage waveforms. The above formulation corresponds to the partitioned subcircuits shown in Fig. 3.2.

3.3 Convergence of the WR algorithm

In [6,8,43], it was shown that the algorithm presented in the previous section converges to the solution of the given system if the following conditions hold:

1. the model in (3.3) is consistent with the original function in (3.1),
2. the canonical form of the WR algorithm is globally Lipschitz continuous [6] with respect to the vector of the unknowns $\mathbf{y}(t)$,
3. the input waveforms $\mathbf{u}(t)$ are continuous functions of time and the canonical form of the WR algorithm are continuous functions with respect to these inputs.

Figure 3.3: Modified WR implementation

The first condition holds for the formulation in (3.11),(3.12), since the solution of (3.8) also satisfies the equations (3.11) and (3.12). The third condition holds for all realistic circuit problems. The second condition is shown to hold true for circuits if the equations were diagonally dominant [6]. Intutively, this translates to the idea that the subcircuits are at least as strongly coupled to themselves as are coupled to each other. In the implementation shown in Fig. 3.2, this would hold if, when written in Laplace domain,

$$|G_1 + sC_1| \geq G_3, \quad (3.15)$$

$$|G_2 + sC_2| \geq G_3, \quad (3.16)$$

for $0 \leq \omega \leq \infty$, where $s = j\omega$ and ω is the angular frequency. This can be ensured by adding ground resistances at the points of decoupling (as shown in Fig. 3.3, with newly added grounded resitances R_3).

The new implementation can be formulated for GJ based relaxation as,

$$(G_1 + G_3) v_1^r(t) + C_1 \dot{v}_1^r(t) = I_s(t) - I_{WR1}^{mod,r}(t), \quad (3.17)$$

$$(G_2 + G_3) v_2^r(t) + C_2 \dot{v}_2^r(t) = -I_{WR2}^{mod,r}(t), \quad (3.18)$$

where

$$I_{WR1}^{mod,r}(t) = -G_3 v_2^{r-1}(t), \quad (3.19)$$

$$I_{WR2}^{mod,r}(t) = -G_3 v_1^{r-1}(t). \quad (3.20)$$

In any case, the actual rate of convergence of a given circuit depends strongly on the method used for partitioning, relaxation process and the physical behaviour of the circuit itself. Much of the effort in the implementation of the WR algorithm is directed at efficient partitioning such that the partitioned subcircuits are loosely coupled to each other.

3.4 Summary

In this chapter a brief description of the theory behind the waveform relaxation was discussed and its implementation in circuit analysis based on MNA formulation was described. Also, the convergence properties of the WR algorithm for the general dynamic system and its implications on the corresponding circuit analysis techniques were presented.

In Chapter 4, the WR algorithm described here will be used to develop a fast algorithm for EMI analysis of high-speed interconnects. In Chapter 5, a WR-based algorithm for fast transient analysis of power grid circuits will be developed.

Chapter 4

Fast EMI analysis via transverse partitioning

As discussed in Section 2.1, the computational complexity of the EMI analysis using conventional techniques increases drastically with the increase in the number of coupled lines. In order to address the above computational difficulty, a new algorithm based on recently developed transverse partitioning and waveform relaxation is presented in this chapter. The major advantages of the proposed EMI analysis algorithm are as follows:

1. It can handle large number of coupled interconnects. A linear growth in the computational complexity, with the increase in the number of coupled lines subjected to EMI, is achieved [14–16].

2. The same waveform relaxation sources that are computed for MTL analysis are also employed for EMI analysis, leading to a further reduction in CPU time.
3. The new method is highly parallelizable, which can lead to a large reduction in the CPU time.

The next section reviews the transverse partitioning technique for MTL simulation as relevant to the proposed EMI analysis algorithm presented in this chapter.

4.1 Transverse partitioning for transmission lines

Transverse partitioning (TP), which was recently introduced for the simulation of unexcited MTLs (the phrase *unexcited MTLs* is used in this thesis, to mean specifically those MTLs not exposed to *external* field excitation), takes advantage of the weak coupling between individual lines in a realistic MTL structure [11]. Accordingly, the partitioning of the circuit into subcircuits is done in the transverse direction rather than the conventional longitudinal direction [10]. The idea here is to simulate single lines as subcircuits, with the coupling to other lines represented by lumped sources.

For the purpose of illustration, consider an MTL structure consisting of n lossy coupled lines, with constant **RLGC** parameters, as shown in Fig. 4.1. The volt-

Figure 4.1: Distributed interconnect structure with n coupled lines.

ages and currents on these lines can be described using homogeneous Telegrapher's equations in the time-domain as follows:

$$\frac{\partial}{\partial z} \begin{bmatrix} \mathbf{v} \\ \mathbf{i} \end{bmatrix} = \begin{bmatrix} \mathbf{0} & -\mathbf{R} \\ -\mathbf{G} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{v} \\ \mathbf{i} \end{bmatrix} + \begin{bmatrix} \mathbf{0} & -\mathbf{L} \\ -\mathbf{C} & \mathbf{0} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \mathbf{v} \\ \mathbf{i} \end{bmatrix}. \quad (4.1)$$

Here, $\mathbf{v}$ and $\mathbf{i}$ represent the voltage and current vectors along the lines as a function of distance (z) and time (t). $\mathbf{R} \in \mathbb{R}^{n \times n}$, $\mathbf{L} \in \mathbb{R}^{n \times n}$, $\mathbf{G} \in \mathbb{R}^{n \times n}$ and $\mathbf{C} \in \mathbb{R}^{n \times n}$ are the p.u.l.) parameter matrices of the MTL. Next, the equations for the k^{th} line can be written in terms of subcircuits as [11],

$$\frac{\partial v_k}{\partial z} = -r_{kk}i_k - l_{kk}\frac{\partial i_k}{\partial t} - \sum_{j=1, j \neq k}^n [r_{kj}i_j + l_{kj}\frac{\partial i_j}{\partial t}], \quad (4.2)$$

$$\frac{\partial i_k}{\partial z} = -\hat{g}_{kk}v_k - \hat{c}_{kk}\frac{\partial v_k}{\partial t} - \sum_{j=1, j \neq k}^n [g_{kj}v_{kj} + c_{kj}\frac{\partial v_{kj}}{\partial t}], \quad (4.3)$$

where

$$\hat{c}_{kk} = c_{kk} - \sum_{j=1, j \neq k}^n c_{kj}, \quad (4.4)$$

$$\hat{g}_{kk} = g_{kk} - \sum_{j=1, j \neq k}^n g_{kj}, \quad (4.5)$$

and $v_{kj} = v_k - v_j$. Note that all the voltages and currents indicated above are functions of distance from the near-end z , and time t . The summation terms in (4.2) and (4.3) represent the coupling voltages and currents on the line k due to the neighbouring lines. Rewriting (4.2) and (4.3),

$$\frac{\partial}{\partial z} v_k(z, t) = -r_{kk} i_k(z, t) - l_{kk} \frac{\partial}{\partial t} i_k(z, t) - e_k(z, t), \quad (4.6)$$

$$\frac{\partial}{\partial z} i_k(z, t) = -\hat{g}_{kk} v_k(z, t) - \hat{c}_{kk} \frac{\partial}{\partial t} v_k(z, t) - f_k(z, t), \quad (4.7)$$

where the sources are represented by

$$e_k = \sum_{j=1, j \neq k}^n [r_{kj} i_j(z, t) + l_{kj} \frac{\partial}{\partial t} i_j(z, t)], \quad (4.8)$$

$$f_k = \sum_{j=1, j \neq k}^n [g_{kj} v_{kj}(z, t) + c_{kj} \frac{\partial}{\partial t} v_{kj}(z, t)]. \quad (4.9)$$

Illustrative Example 1: For the purpose of illustration, consider a 3-line structure described by the following p.u.l. parameters:

$$\mathbf{R} = \begin{bmatrix} r_{11} & r_{12} & r_{13} \\ r_{21} & r_{22} & r_{23} \\ r_{31} & r_{32} & r_{33} \end{bmatrix}, \quad \mathbf{G} = \begin{bmatrix} \hat{g}_{11} + g_{12} + g_{13} & -g_{12} & -g_{13} \\ -g_{21} & \hat{g}_{22} + g_{21} + g_{23} & -g_{23} \\ -g_{31} & -g_{32} & \hat{g}_{33} + g_{31} + g_{32} \end{bmatrix}$$

$$\mathbf{L} = \begin{bmatrix} l_{11} & l_{12} & l_{13} \\ l_{21} & l_{22} & l_{23} \\ l_{31} & l_{32} & l_{33} \end{bmatrix}, \mathbf{C} = \begin{bmatrix} \hat{c}_{11} + c_{12} + c_{13} & -c_{12} & -c_{13} \\ -c_{21} & \hat{c}_{22} + c_{21} + c_{23} & -c_{23} \\ -c_{31} & -c_{32} & \hat{c}_{33} + c_{31} + c_{32} \end{bmatrix}.$$

Then, the decoupled line equations for line-1 can be written as,

$$\frac{\partial}{\partial z} v_1(z, t) = -r_{11} i_1(z, t) - l_{11} \frac{\partial}{\partial t} i_1(z, t) - e_1(z, t), \quad (4.10)$$

$$\frac{\partial}{\partial z} i_1(z, t) = -\hat{g}_{11} v_1(z, t) - \hat{c}_{11} \frac{\partial}{\partial t} v_1(z, t) - f_1(z, t), \quad (4.11)$$

where the sources are represented by

$$e_1 = \{r_{12} i_2(z, t) + r_{13} i_3(z, t)\} + \left\{ l_{12} \frac{\partial}{\partial t} i_2(z, t) + l_{13} \frac{\partial}{\partial t} i_3(z, t) \right\}, \quad (4.12)$$

$$f_1 = \{g_{12} v_{12}(z, t) + g_{13} v_{13}(z, t)\} + \left\{ c_{12} \frac{\partial}{\partial t} v_{12}(z, t) + c_{13} \frac{\partial}{\partial t} v_{13}(z, t) \right\}. \quad (4.13)$$

Using the above coupling relationships, WR with TP can be implemented by adopting a distributed approach [11], by dividing each line into small segments. At the terminals of each segment, lumped current and voltage sources are connected (derived from the above expressions), representing the coupling from the corresponding segments of all other lines. These sources could be incorporated in a suitable way, depending upon the specific transmission line macromodel being used. For example, for an n -line MTL, consider the lumped macromodel with M segments. The equation for the m^{th} segment of the k^{th} line (of length Δz_m) can be written using lumped sources derived by assigning a suitable weighting factor, w_m , to the expressions in

Figure 4.2: Implementation of waveform relaxation in unexcited lines.

(4.6) and (4.7) as follows,

$$v_k(z_m, t) = v_k(z_{m-1}, t) - r_{kk}\Delta z_m i_k(z_{m-1}, t) - l_{kk}\Delta z_m \frac{\partial}{\partial t} i_k(z_{m-1}, t) - w_m \Delta z_m e_k(z_m, t), \quad (4.14)$$

$$i_k(z_m, t) = i_k(z_{m-1}, t) - \hat{g}_{kk}\Delta z_m v_k(z_{m-1}, t) - \hat{c}_{kk}\Delta z_m \frac{\partial}{\partial t} v_k(z_{m-1}, t) - w_m \Delta z_m f_k(z_m, t). \quad (4.15)$$

The resulting time-domain macromodel for the unexcited MTL structure is shown in Fig. 4.2. Here, the lumped voltage and current sources are defined by,

$$\tilde{e}_k(z_m, t) = w_m \Delta z_m e_k(z_m, t), \quad (4.16)$$

$$\tilde{f}_k(z_m, t) = w_m \Delta z_m f_k(z_m, t), \quad (4.17)$$

respectively, with $1 \leq k \leq n$, $1 \leq m \leq M$. The significance of the weighting factor, w_m , is described in Appendix A.

Thus, using the above method, the problem of simulating an n -line structure can be reduced to that of simulating n - single lines. As a result, the computational cost of analyzing an unexcited MTL now grows only *linearly* with the number of lines. Exploiting this feature, we propose a new algorithm in this chapter for the analysis of EMI in MTLs, leading to a large reduction in computation time.

4.2 Proposed algorithm for fast EMI analysis in the presence of large number of coupled interconnects

In this section, the proposed algorithm for fast EMI analysis in the presence of large number of coupled lines is given. The algorithm exploits the waveform relaxation (WR) and transverse partitioning (TP) technique for this purpose. This section is organized as follows. In Section 4.2.1, an efficient way of computing the EMI sources (the effect of EMI, as discussed in Section 2.1) is given and in Section 4.2.2, a new methodology to include these sources with the waveform relaxation macromodel is given.

4.2.1 Computation of equivalent sources compatible with waveform relaxation

In this section, development of equivalent sources compatible with WR algorithm is described. First, the basic incident field coupling formulation, that is necessary for the derivation of the proposed algorithm is described. For the purpose of illustration, consider the structure described in Fig. 2.3, with an incident TEM plane wave having

the electric field vector of the form [20, 22],

$$\vec{E}^i(x, y, z, s) = E_0(s)(A_x \hat{a}_x + A_y \hat{a}_y + A_z \hat{a}_z) e^{-s(\kappa_x x + \kappa_y y + \kappa_z z)}. \quad (4.18)$$

Here the directional cosines and the propagation vector are computed using the geometrical parameters of the incident wave, shown in Fig. 2.3, as follows:

$$A_x = \sin \vartheta_E \sin \vartheta, \quad (4.19)$$

$$A_y = -\sin \vartheta_E \cos \vartheta \cos \varphi - \cos \vartheta_E \sin \varphi, \quad (4.20)$$

$$A_z = -\sin \vartheta_E \cos \vartheta \sin \varphi + \cos \vartheta_E \cos \varphi, \quad (4.21)$$

$$\kappa_x = -\frac{\cos \vartheta}{v}, \quad (4.22)$$

$$\kappa_y = -\frac{\sin \vartheta \cos \varphi}{v}, \quad (4.23)$$

$$\kappa_z = -\frac{\sin \vartheta \sin \varphi}{v}, \quad (4.24)$$

where ϑ_E is the polarization angle of the electric field, ϑ and φ describe the angle of incidence at the origin, and v is the speed of wave propagation in the medium.

Next, consider the case of a short single lossless line subjected to an incident field. Let the length of the line (d) be significantly less than the smallest wavelength of interest (λ_{min}), i.e.,

$$d \ll \lambda_{min}; \quad \lambda_{min} = \frac{v}{f_{max}}, \quad (4.25)$$

where v is the velocity of the wave in the medium and f_{max} is the maximum frequency of interest. In such a case, efficient expressions for equivalent sources due to an external field can be computed at any convenient point on the line, by imposing a first order approximation [20] on the spatial integrals in the transverse direction ((2.3) and (2.4)), as follows. For a single line in the xz plane and at a height h above an infinite ground plane (as described in Fig. 2.3 and Fig. 2.4), the sources can be defined as,

$$\hat{V}_F(d, s) = V_F(d, s)d, \quad (4.26)$$

$$\hat{I}_F(d, s) = I_F(d, s)d. \quad (4.27)$$

Noting that in (2.3) and (2.4), for the region between the single line and the reference plane, we have, $\vec{a}_n = \hat{a}_y$, and $\vec{E}_t^i = \vec{E}_x^i$, respectively. Using this, we can write (4.26) and (4.27), by expressing the incident magnetic field in terms of the electric field, as

$$\begin{aligned} \hat{V}_F(d, s) &= sd \left[\int_0^h \vec{B}_y^i(x, z) dx \right]_{z=d} \\ &= d \left\{ \left[\vec{E}_z^i(h, z) - \vec{E}_z^i(0, z) \right] - \frac{d}{dz} \left[\int_0^h \vec{E}_x^i(x, z) dx \right] \right\}_{z=d}, \end{aligned} \quad (4.28)$$

$$\hat{I}_F(d, s) = -scd \left[\int_0^h \vec{E}_x^i(x, z) dx \right]_{z=d}. \quad (4.29)$$

It is to be noted that the total electric field incident on the transmission line is the sum of the incident and the reflected electric field at the ground plane. Using the definition of the incident electric field in (4.18), the reflected electric field at the

Figure 4.3: Equivalent sources due to external field for a short lossless line.

infinite ground plane (yz) can be written as [20],

$$\vec{E}^r(x, y, z, s) = E_0(s)(A_x \hat{a}_x - A_y \hat{a}_y - A_z \hat{a}_z) e^{-s(-\kappa_x x + \kappa_y y + \kappa_z z)}. \quad (4.30)$$

Hence, the components of the total electric field incident on the transmission line are as follows,

$$\vec{E}_x^{total} = \vec{E}_x^i + \vec{E}_x^r = 2E_0(s)A_x \cos(\omega \kappa_x x) e^{-s(\kappa_y y + \kappa_z z)}, \quad (4.31)$$

$$\vec{E}_y^{total} = \vec{E}_y^i + \vec{E}_y^r = -2jE_0(s)A_y \sin(\omega \kappa_x x) e^{-s(\kappa_y y + \kappa_z z)}, \quad (4.32)$$

$$\vec{E}_z^{total} = \vec{E}_z^i + \vec{E}_z^r = -2jE_0(s)A_z \sin(\omega \kappa_x x) e^{-s(\kappa_y y + \kappa_z z)}, \quad (4.33)$$

where ω is the angular frequency. Substituting (4.31), (4.33) in (4.28), (4.29), and recognizing that $y = 0$ for the xz plane, the expressions for the EMI sources can be simplified as follows,

$$\hat{V}_F(d, s) = s\Gamma E_0(s) \left[\frac{\sin(\omega \kappa_x h)}{\omega \kappa_x h} \right] e^{-s\kappa_z d} (\kappa_z A_x - \kappa_x A_z), \quad (4.34)$$

$$\hat{I}_F(d, s) = -sc\Gamma \left[\frac{\sin(\omega \kappa_x h)}{\omega \kappa_x h} \right] e^{-s\kappa_z d} A_x, \quad (4.35)$$

where $\Gamma = 2hd$. For an electrically short line of small cross sectional dimensions, $\omega\kappa_x h = \frac{2\pi h}{\lambda_x}$ and $\omega\kappa_z d = \frac{2\pi d}{\lambda_z}$ will be small. Hence, the sources in (4.34) and (4.35) can be approximated as,

$$\hat{V}_F(d, s) \approx s\Gamma(A_x\kappa_z - A_z\kappa_x)E_0(s), \quad (4.36)$$

$$\hat{I}_F(d, s) \approx -s\Gamma A_x E_0(s). \quad (4.37)$$

These sources can be connected at the end of an unexcited line, as shown in Fig. 4.3.

In the case of a long lossy MTL, the above equivalent sources can be adopted by dividing the line into M short segments. Correspondingly, (4.36) and (4.37) can be modified for the m^{th} segment of the long lossy MTL (which is at a distance of z_m from the near-end), in the frequency-domain as follows:

$$\hat{\mathbf{V}}_{\mathbf{F}}(z_m, s) = sE_0(s) \begin{bmatrix} \vdots \\ \Gamma_k(A_x\kappa_z - A_z\kappa_x)e^{-s\kappa_y y_k} \\ \vdots \end{bmatrix} e^{-s\kappa_z z_m}, \quad (4.38)$$

$$\hat{\mathbf{I}}_{\mathbf{F}}(z_m, s) = -(\mathbf{G} + s\mathbf{C})E_0(s) \begin{bmatrix} \vdots \\ \Gamma_k A_x e^{-s\kappa_y y_k} \\ \vdots \end{bmatrix} e^{-s\kappa_z z_m}, \quad (4.39)$$

where $\Gamma_k = 2x_k\Delta z_m$.

These sources can be connected at the end of each segment of each line in the MTL structure to simulate the effects of EMI (Fig. 4.4 shows the equivalent subcircuit for

Figure 4.4: EMI sources for the m^{th} segment of the k^{th} line in an MTL structure.

the m^{th} segment of the k^{th} line). The expressions for the sources above provide the equivalent representation compatible with the proposed EMC analysis. Details of incorporating them in the proposed macromodel are given in the next subsection.

4.2.2 Formulation of the proposed macromodel

In this subsection, the compatibility of the sources defined above with the waveform relaxation macromodel is demonstrated and the proposed macromodel is described. For this purpose, sources in (4.38) and (4.39) are written in time-domain as follows:

$$\hat{\mathbf{v}}_{\mathbf{F}}(z_m, t) = \begin{bmatrix} \vdots \\ \Gamma_k(A_x \kappa_z - A_z \kappa_x) \frac{\partial}{\partial t} \hat{E}_{k,z_m} \\ \vdots \end{bmatrix}, \quad (4.40)$$

Figure 4.5: Proposed equivalent EMI (EE) sources for the m^{th} segment of an MTL structure.

$$\hat{\mathbf{i}}_{\mathbf{F}}(z_m, t) = -\mathbf{G} \begin{bmatrix} \vdots \\ \Gamma_k A_x \hat{E}_{k,z_m} \\ \vdots \end{bmatrix} - \mathbf{C} \begin{bmatrix} \vdots \\ \Gamma_k A_x \frac{\partial}{\partial t} \hat{E}_{k,z_m} \\ \vdots \end{bmatrix}, \quad (4.41)$$

where,

$$\hat{E}_{k,z_m} = E_0(t - \kappa_y y_k - \kappa_z z_m). \quad (4.42)$$

For the purpose of simplicity of presentation, these time-domain sources are referred to as *equivalent EMI* (EE) sources in the rest of this paper.

$$\hat{\mathbf{v}}_{\mathbf{F}}(z_m, t) \Rightarrow \begin{bmatrix} \vdots \\ v_{EE,k}(z_m, t) \\ \vdots \end{bmatrix}, \quad (4.43)$$

$$\hat{\mathbf{i}}_{\mathbf{F}}(z_m, t) \Rightarrow \begin{bmatrix} \vdots \\ i_{EE,k}(z_m, t) \\ \vdots \end{bmatrix}. \quad (4.44)$$

The equivalent EMI sources for the m^{th} segment of the k^{th} line is shown in Fig. 4.5.

Writing the inhomogeneous MTL equations due to incident fields, (2.1), in the time-domain for the MTL, we have,

$$\frac{\partial}{\partial z} \mathbf{v}(z, t) = -\mathbf{R}\mathbf{i}(z, t) - \mathbf{L} \frac{\partial}{\partial t} \mathbf{i}(z, t) + \hat{\mathbf{v}}_{\mathbf{F}}(z, t), \quad (4.45)$$

$$\frac{\partial}{\partial z} \mathbf{i}(z, t) = -\mathbf{G}\mathbf{v}(z, t) - \mathbf{C} \frac{\partial}{\partial t} \mathbf{v}(z, t) + \hat{\mathbf{i}}_{\mathbf{F}}(z, t). \quad (4.46)$$

An important merit to be noted here is that, the form of (4.45), (4.46) is similar to that of (4.6), (4.7). Hence, the sources in (4.43), (4.44) (that are computed to account for EMI using (4.40), (4.41)), can be incorporated in a way similar to the relaxation sources in the WR model in Fig. 4.2. In other words, the sources due to EMI and those due to WR can be combined to obtain a compact time-domain macromodel.

Figure 4.6: Proposed time-domain macromodel for MTLs exposed to EMI.

Consequently, the waveform relaxation sources in (4.16), (4.17) are added to the EE sources given in (4.43), (4.44) to obtain the combined sources $v_{EEW,k}$ and $i_{EEW,k}$ (EEW stands for *equivalent EMI combined with waveform relaxation sources*) for connecting at the end of each segment as,

$$v_{EEW,k}(z_m, t) = v_{EE,k}(z_m, t) - w_m \Delta z_m e_k(z_m, t), \quad (4.47)$$

$$i_{EEW,k}(z_m, t) = i_{EE,k}(z_m, t) - w_m \Delta z_m f_k(z_m, t). \quad (4.48)$$

The new time-domain macromodel represented by (4.47) and (4.48) is shown in Fig. 4.6 [14]. Importantly, any specific macromodel available in the literature can be used for representing the individual unexcited segments.

4.3 Computational and implementation considerations

In this section, several observations regarding the efficient implementation of the proposed macromodel for fast EMI analysis and related discussions are presented.

1. Note that the EE sources described in (4.40)-(4.44) only need to be computed once, for the first set of segments in each line, independent of the number of time points considered. This is possible because, in (4.40) and (4.41), $\hat{E}_{k,z_m}$ is the only term that is dependant on the position of the lines and

their segments. As can be seen from (4.42), $\hat{E}_{k,z_m}$ can be computed as a time-shifted version of $E_0(t)$ for successive segments. Consequently, it is sufficient to compute only the first set of EE sources in (4.40) and (4.41) (i.e. $m = 1$). EE sources for the rest of the segments can be simply obtained as a time-shifted version of the first.

2. The total cost of the proposed EMI analysis grows only linearly with the number of lines. This is because, at the beginning of each iteration, the above pre-computed sources (as described in *item-1*) are appropriately combined with the relaxation sources of the corresponding segments and the resulting subcircuits are simulated. Hence, the computational cost involved in the analysis of a given MTL structure exposed to EMI is the sum of a) the cost for computing the EMI sources (as described in *item-1*, which is done only once) and, b) the cost of waveform relaxation iterations applied to the resulting compact time-domain macromodel. The number of WR iterations needed for convergence may vary with the given problem. Based on numerous experimental runs, for most high-speed interconnect structures, typically 2-4 iterations are required for SPICE-level accuracy. As noted in Section 3, computational cost of the WR iterations with transverse partitioning grows only linearly with the increase in the number of coupled lines.

3. The proposed WR method can be implemented based on either the Gauss-Seidel (GS) or Gauss-Jacobi (GJ) relaxation techniques. The WR process typically converges within 3-4 iterations for most industrial high-speed interconnect structures. Detailed reading of the convergence properties of WR as applied to dense coupled interconnects can be found in [7, 8, 14, 44].
4. The equations presented in the previous section pertain to a lumped segment (lossy, constant parameters) macromodel for the unexcited MTL. However, the computed EMI sources and the waveform relaxation algorithm can be used in conjunction with any other macromodel.
5. An important advantage of the proposed algorithm is that, it is highly parallelizable as each line can be independently simulated on a different processor.

A brief summary of the steps associated with the proposed EMI analysis is given in Pseudocode 4.1 [14].

4.4 Numerical examples

Three case studies are presented here. The first experiment assesses the accuracy of the proposed equivalent EMI sources (described in (4.43) and (4.44)) that are compatible with the waveform relaxation macromodel, using a 3-line example [27]. The second experiment uses a similar structure to demonstrate the speed of convergence

Step 1: Divide the MTL into required number of segments (M), using the criterion in (4.25).

Step 2: Compute the equivalent EMI (EE) sources, v_{EE} and i_{EE} for the first segment of each line using (4.40) and (4.41) for the given $E_0(t)$ and $\frac{d}{dt}E_0(t)$ waveforms, the polarization data and the relative cross sectional positions of the lines.

Step 3: Shift the waveforms obtained above through appropriate time-delays to obtain the rest of the EE sources for the other segments.

Step 4: Define ϵ as the tolerance error for the convergence of waveform relaxation iterations.

Step 5: Set $r = 1$. Generate an initial guess for the WR sources $\tilde{e}_k^{(r)}(z_m, t)$ and $\tilde{f}_k^{(r)}(z_m, t)$ in (4.16) and (4.17), for $1 \leq k \leq n$, $1 \leq m \leq M$. The superscript (r) denotes the r^{th} waveform relaxation iteration. Combine these sources with the EE sources from **Steps 2, 3** to obtain the EEW sources, $v_{EEW,k}^{(r)}(z_m, t)$ and $i_{EEW,k}^{(r)}(z_m, t)$, as described in Fig. 4.6.

Step 6: Simulate the individual subcircuits to obtain the line voltages/currents, $v_k^{(r)}(z_m, t)$ and $i_k^{(r)}(z_m, t)$.

Step 7: Based on the results obtained in **Step 6**, update the WR sources to $\tilde{e}_k^{(r+1)}(z_m, t)$ and $\tilde{f}_k^{(r+1)}(z_m, t)$ using (4.16) and (4.17). Combine them with the EE sources from **Steps 2, 3** to obtain the new EEW sources, $v_{EEW,k}^{(r+1)}(z_m, t)$ and $i_{EEW,k}^{(r+1)}(z_m, t)$.
Compute error=norm(the difference between the waveforms of the present and previous iterations).

Step 8:
 if (error $\leq \epsilon$) **exit**;
 else $r = r + 1$, go to **Step 6**;
 end

Pseudocode 4.1: Summary of computational steps for the proposed EMI analysis of high-speed interconnects

and accuracy of the proposed macromodel. The third example considers several MTL structures with different numbers of lines to determine the relationship between the CPU time and the number of lines, and compares the performance of conventional techniques with that of the proposed algorithm. For examples 2 and 3, since the transmission lines considered are uniform in nature and were divided into segments of identical length, (A-9) is evaluated using piece-wise constant approximation, with the weighting factors ω_m set to the value of 1. All the experiments were executed using an INTEL P4-2GHz based CPU.

Example 1: This example demonstrates the accuracy of the proposed EE sources

Figure 4.7: Test MTL circuit for Example 1.

Figure 4.8: Temporal envelope of the incident electric field $E_0(t)$ (Example 1).

developed in Section 4.2. For this purpose, an MTL structure (a 3-line structure, with line parameters shown in Fig. 4.7) is simulated using the conventional coupled lumped segment macromodel (CCLS) with the proposed EE sources. The results are compared with the simulation of the same CCLS macromodel using exact EMI sources generated via IFFT [27].

The MTL structure is terminated by passive capacitive loads at the far-end and 50Ω resistive loads at the near end. The cross sectional geometry of the lines and the incident field parameters are shown in Fig. 4.7. It is to be noted that, in this experiment no direct sources were used to excite the lines (in order to highlight the effects of EMI). The curve "No EMI" in Fig. 4.9 corresponds to the zero voltage input response at the far-end nodes of the circuit.

Figure 4.9: Comparison of transient waveforms for the far-end voltage of (a) line-1 and (b) line-2 (Example 1).

Next, the structure was subjected to a plane wave, with the electric field having a time-shifted Gaussian temporal envelope [45–49] with a peak value of 1 V/m at 10 ns and a temporal standard deviation of 100 ps as shown in Fig. (4.8). A conventional coupled lumped segment (CCLS) macromodel with 30 segments was used to represent the MTL (the number of segments was chosen so that each segment is small compared to the smallest wavelength of interest, which in turn corresponds to the 90% bandwidth of the signal used for excitation) and was simulated using the proposed EE sources (described in (4.43) and (4.44)). The corresponding transient waveforms are shown by dashed lines in Fig. 4.9. Next, the accuracy of these waveforms are verified by simulating the same macromodel using near/far-end voltage/current sources

Figure 4.10: CPU cost for the computation of EMI sources for varying number of lines (Example 1).

computed by taking the IFFT of the corresponding frequency-domain sources due to EMI [27] (henceforth, these sources are referred to as *IFFT sources*). Corresponding transient waveforms are shown by solid line in Fig. 4.9. We see that there is a good match between the sources computed using the proposed and the IFFT based approaches.

Computation of sources due to EMI using the IFFT based approach required (considering 1000 frequency points) 2.625 seconds, while the computation of proposed EE sources took less than $1 \mu\text{s}$. This computational difference becomes even more pronounced when considering a large number of coupled lines. In order to demonstrate this, several MTL structures with varying numbers of coupled lines were considered

Figure 4.11: Nonlinear circuit with 3-line MTL (Example 2).

and the time to compute the sources using both the above approaches were recorded. The results are shown in Fig. 4.10. As seen, the acceleration achieved using the proposed approach increases significantly, with the increase in the number of coupled conductors.

Example 2: In this experiment, a non-linear circuit given in Fig. 4.11 was considered to demonstrate the convergence of the proposed macromodel for EMI analysis, as well as the impact of the EMI on transient results. The lines 1 and 2 are terminated with nonlinear receivers (CMOS based inverters, constructed using HSPICE level-1 transistor models [50]). The circuit is driven by an input voltage source of amplitude = 3 V, rise/fall time = 1 ns, and pulse width = 4 ns. The MTL used has the same cross-sectional dimensions as the 3-line structure given in Fig. 4.7, with the length decreased to 5 cm. Conventional coupled lumped segment (CCLS) macromodel with 15

Figure 4.12: Transient waveforms at (a) direct-line output, V_{OUT1} , and (b) victim-line output, V_{OUT2} , illustrating the impact of external incident fields with a peak amplitude of 1 V/m (Example 2). Note that there is no difference in the transient waveforms with and without EMI, due to the low peak amplitude of the incident field.

segments was used to represent the unexcited structure. Transient simulation results using this macromodel and SPICE (with *no EMI*) for nodes V_{OUT1} and V_{OUT2} , the outputs of the inverter-receivers, are given by dashed lines in Figs. 4.12(a)- 4.12(b).

In the second part of this experiment, the effect of external incident fields was investigated. For this purpose, the structure was subjected to different types of EMI excitations:

1. First, the structure was subjected to a plane wave, with the electric field having the form of a Gaussian pulse with a peak amplitude of 1V/m (same as

in Example 1, representing a weak EMI excitation). The same macromodel (the CCLS macromodel as described in the first part of this experiment) is now simulated directly in HSPICE along with the proposed EE sources (obtained using (4.43) and (4.44)). Henceforth, this analysis is referred to as the conventional EMI analysis. Corresponding transient results are shown by solid lines in Figs. 4.12(a)- 4.12(b). As seen, the low amplitude EMI did not impact the output waveform significantly.

2. Next, to demonstrate the ability of the proposed algorithm to handle high amplitude EMI disturbances, the experiment was repeated with a Gaussian pulse of 5kV/m and the corresponding results are given Figs. 4.13(a)- 4.13(b) (representing a large EMI excitation). As seen, in this case the output waveform was significantly impacted due to EMI.

In the third part of this experiment, efficiency and convergence properties of the proposed macromodel are investigated. For this purpose, the results obtained in the second part of this experiment (with the EMI excitation of 5kV/m) are compared with the successive waveform relaxation iterations using the EEW sources of (4.47) and (4.48). A comparative study of convergence of the WR iterations is given in terms of graphs in Fig. 4.14, by considering the output waveform at node V_{OUT1} . In Figs. 4.14(a)- 4.14(b), the solid line indicates the V_{OUT1} response obtained in the second part of this experiment (using conventional EMI analysis). The dotted lines

Figure 4.13: Transient waveforms at (a) direct-line output, V_{OUT1} , and (b) victim-line output, V_{OUT2} , illustrating the impact of external incident fields with a peak amplitude of 5 kV/m (Example 2). Note that there is significant difference in the transient waveforms with and without EMI, due to the large peak amplitude of the incident field.

indicate the V_{OUT1} response at the end of first three WR iterations. As seen, the WR results quickly converge to that of the conventional EMI analysis results, within three iterations. This is also demonstrated in Fig. 4.15, by plotting the percentage-error versus the number of iterations. For convergence, this experiment uses a conventional voltage norm of the form $\|v^{(r+1)} - v^{(r)}\| < \epsilon$, which is highly conservative.

Example 3: In this experiment, the computational efficiency of the proposed EMI analysis is demonstrated using several experiments with a varying number of coupled

(a) Iteration 1

(b) Iteration 3

Figure 4.14: Comparative study of convergence of waveform relaxation iterations for output transient waveforms at V_{OUT1} (Example 2).

Figure 4.15: Percentage error between WR results and CCLS results for successive iterations (Example 2).

conductors. In each experiment, the following analyses are performed. The line parameters are chosen to be close to those in the previous examples. All the lines are terminated with a resistance of $50\ \Omega$ and a capacitance of $1\ \text{pF}$ at the near-end and far-end respectively. The structure is exposed to an external field with a saturated ramp of $1\ \text{V/m}$ and rise time $1\ \text{ns}$ [20] at arbitrary positions on the xy plane.

In each of the experiments, first, the conventional EMI analysis is performed using the conventional coupled lumped segment (CCLS) macromodel of the unexcited line and the equivalent EMI sources as described in Fig. 4.5. Next, the performance metrics of this analysis are compared with the proposed WR and TP algorithm, using the new EEW sources described in Fig. 4.6. The above experiment is repeated

Figure 4.16: Transient response at the far-end of line 15, showing the convergence of WR-TP iterations for the case, $n=30$ (Example 3).

for numerous interconnect structures with the number of coupled lines varying from 5 to 60.

Sample results for the case of a coupled interconnect system of 30-lines are shown in Fig. 4.16- 4.17. Note that the results from proposed macromodel with 2 iterations and the conventional EMI analysis are indistinguishable.

In all the experiments in this example, only 2 iterations were found to be sufficient for convergence. The CPU time required for each case was noted and are plotted against the number of coupled lines in Fig. 4.18. The results for a few of the exper-

Figure 4.17: Transient response at the near-end of line 6, showing the convergence of WR-TP iterations for the case, $n=30$ (Example 3).

iments have also been tabulated in Table. 4.1. As can be seen, the CPU cost using conventional EMI analysis increases more than cubically with the number of lines. In comparison, the computational cost for the proposed algorithm increases only linearly. Thus, the new algorithm yields a significant acceleration with the increase in the number of coupled lines.

Figure 4.18: CPU cost for varying number of lines: Conventional EMI analysis vs proposed (Example 3).

Table 4.1: CPU cost comparison of EMI analysis for varying number of lines (Example 3)

Number of coupled lines (N)	Conventional EMI Analysis (sec)	Proposed macromodel (sec)	Speed-up
15	7.53	3.96	1.9
30	50.69	7.92	6.4
60	591.24	15.84	37.3

4.5 Summary

In this chapter a new time-domain macromodel for MTL structures exposed to external EMI was presented. The method uses transverse partitioning for waveform

relaxation including equivalent EMI sources. The same waveform relaxation sources that are computed for MTL analysis are also employed for EMI analysis. This method is efficient both in the construction of the macromodel as well as the transient simulation. Importantly, the computational cost of the proposed algorithm increases only linearly with the number of lines. In addition, the new method lends itself to parallel implementation leading to further reduction in computational cost.

Chapter 5

Fast analysis of power distribution networks via Waveform Relaxation

As discussed in Section 2.2, the significance of on-chip power integrity analysis and the related challenges are becoming increasingly important in high-speed designs. Conventional techniques which are based on either direct solver methods or iterative methods have their relative merits and disadvantages and do not adequately address the emerging power integrity challenges. To address this difficulty, a new algorithm based on waveform relaxation techniques for the transient analysis of on-chip power grid circuits is developed in this chapter. The new algorithm is hybrid in nature and exploits the advantages of both classes of methods (i.e. direct solvers and iterative solvers). Novel partitioning schemes and convergence accelerator mechanisms are de-

veloped for fast convergence of the waveform relaxation iterations [17–19]. Numerical examples are presented to demonstrate the accuracy and efficiency of the proposed method.

The rest of the chapter is organized as follows. Section 5.1 defines the power grid problem to be solved. Section 5.2 develops the proposed waveform relaxation based algorithm. Sections 5.3 and 5.4 present the numerical results and summary, respectively.

5.1 Problem formulation: power grid circuits

The models used to represent the on-chip power distribution networks was described in Section 2.2.5. A typical RC mesh structure resulting from this kind of modeling is shown in Fig. 5.1. The behavior of such a mesh structure can be expressed using modified nodal analysis (MNA) as follows:

$$\mathbf{G}\mathbf{X}(t) + \mathbf{C}\dot{\mathbf{X}}(t) = \mathbf{b}\mathbf{u}(t), \quad (5.1)$$

where $\mathbf{X}(t)$ represents the vector of voltages on the nodes of the circuit, $\mathbf{G}$ and $\mathbf{C}$ are the conductance and capacitance matrices of the circuit, respectively, $\mathbf{u}(t)$ is the vector of inputs to the circuit and $\mathbf{b}$ is a selection matrix. Integration methods such as the backward Euler (BE) can be used for solving (5.1). Applying BE to (5.1) with

Figure 5.1: Mesh type circuit structure of a flip chip power grid.

a step size (h) leads to

$$\mathbf{G}\mathbf{X}(t) + \mathbf{C} \left(\frac{\mathbf{X}(t) - \mathbf{X}(t-h)}{h} \right) = \mathbf{b}\mathbf{u}(t). \quad (5.2)$$

$$\Rightarrow \left(\mathbf{G} + \frac{\mathbf{C}}{h} \right) \mathbf{X}(t) = \mathbf{b}\mathbf{u}(t) + \left(\frac{\mathbf{C}}{h} \right) \mathbf{X}(t-h). \quad (5.3)$$

The equation (5.3) can be further simplified to

$$\mathbf{A}\mathbf{X}(t) = \mathbf{B}, \quad (5.4)$$

where $\mathbf{A} = (\mathbf{G} + \mathbf{C}/h)$ and $\mathbf{B} = \mathbf{b}\mathbf{u}(t) + (\mathbf{C}/h)\mathbf{X}(t-h)$.

Figure 5.2: 3x3 Power grid example

Solving the above set of equations at every time point involves finding the LU factors of matrix $\mathbf{A}$. Since this process can be very costly for large circuits, the step size h is held constant and the inversion process is executed only once at the beginning of the simulation for all circuits/subcircuits in our analyses. The time step should be kept small enough to ensure the accuracy of simulation. For the purpose of illustration, the formulation given by (5.1)-(5.3) is described through an example below.

Illustrative Example 1: To better explain the formulation of MNA matrices for the power grid networks, consider a simple example of 3x3 power grid with 2 current sources (representing active power drains) and 1 voltage source (V_{DD} contact) as shown in the Fig. 5.2.

For the test grid network shown in Fig. 5.2, there are 9 nodes. The size of matrix

$$\underbrace{\begin{bmatrix} g_1 & -g_{12} & & -g_{14} & & & & & & \\ -g_{12} & g_2 & -g_{23} & & -g_{25} & & & & & \\ & -g_{23} & g_3 & & & -g_{36} & & & & \\ -g_{14} & & & g_4 & -g_{45} & & -g_{47} & & & \\ & -g_{25} & & -g_{45} & g_5 & -g_{56} & & -g_{58} & & \\ & & -g_{36} & & -g_{56} & g_6 & & & -g_{69} & \\ & & & -g_{47} & & & g_7 & -g_{78} & & \\ & & & & -g_{58} & & -g_{78} & g_8 & -g_{89} & \\ & & & & & -g_{69} & & -g_{89} & g_9 & \\ & & & & & & & & & 1 \end{bmatrix}}_{\mathbf{A}} \underbrace{\begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \\ x_8 \\ x_9 \\ I_{VDD} \end{bmatrix}}_{\mathbf{X}(t)} = \underbrace{\begin{bmatrix} 0 \\ -I_2 \\ 0 \\ 0 \\ 0 \\ 0 \\ -I_7 \\ 0 \\ 0 \\ V_{DD} \end{bmatrix}}_{\mathbf{B}} + \frac{\mathbf{C}}{h} \mathbf{X}(t-h) \quad (5.5)$$

Figure 5.3: Structure of the MNA matrices for the power grid circuit in Fig. 5.2.

($\mathbf{A}$) is 10x10; the source vector ($\mathbf{B}$) and voltage vector ($\mathbf{X}(t)$) are 10x1. The first 9 equations are KCL equations on the 9 nodes of the power grid and the last equation is the KVL equation for the voltage source at node 5. The current sources at nodes 2 and 7 appear on the right-hand side in source vector $\mathbf{B}$. The resulting MNA matrix is given in Fig. 5.3. Here, the diagonal entries of the $\mathbf{A}$ matrix on the left-hand side of equation (5.4) are defined as

$$g_i = \sum_{j \in n_i} g_{ij} + c_i/h, \quad (5.6)$$

where c_i represents the capacitance to ground plane at node i , n_i is the set of the neighboring nodes of node i , and h is the constant step size. The off diagonal conductance terms g_{ij} define the conductance between the adjacent nodes i and j . As

can be seen in Fig. 5.3, matrix $\mathbf{A}$ has a block triangular structure [34].

5.2 Proposed transient analysis of power grid networks via waveform relaxation

In this section, the proposed transient analysis algorithm for power grids is presented. The new algorithm adopts the waveform relaxation techniques [6,11,12,51,52] for the power-grid problem described by (5.1), by appropriately partitioning the power grid circuit into smaller subcircuits.

In the proposed algorithm, the coupling between the partitioned subcircuits is represented by relaxation sources, appended at the boundaries of each subcircuit. Since in the partitioned power grid subcircuits, the coupling is mainly through resistors (which serve as current paths between neighbouring subcircuits), coupling effects are represented by current sources. At the beginning of the execution of the algorithm, all relaxation sources are calculated using an initial guess of voltage waveforms at the boundary nodes of the subcircuits. Next, each of the small subcircuits are simulated for a suitable time interval of interest. In this step, the merits of the state-of-the-art fast direct solvers can be exploited. Subsequently, all relaxation sources are updated reflecting the new values of voltages and currents in the subcircuits. The subcircuits are simulated again. This iterative process is repeated until convergence is achieved.

For the proposed algorithm to be practically viable, the relaxation process must converge within a few iterations. To achieve this, the following contributions are proposed in this chapter:

1. Efficient partitioning scheme for the power grid network suitable for waveform relaxation.
2. Fast convergence mechanisms for WR iterations, in power grid circuits. For this purpose, improved techniques for computing initial guess waveforms are developed.

Details are given in the following subsections.

5.2.1 Proposed partitioning of power grids, suitable for application of waveform relaxation

One important issue to be addressed in the WR algorithm for power grids is that of partitioning. In the specific case of multiconductor transmission line type interconnects, transverse partitioning [11] was suggested to identify parts of the circuit that are weakly coupled to each other (this happens to be partitioning the MTL structure as individual lines, as described in Section 4.1). This resulted in the quick convergence of waveforms, leading to large savings in CPU time. However, in power grid circuits, this becomes a challenging task, since there is a strong coupling between the

Figure 5.4: Proposed BRP scheme for power grid

neighboring nodes in all directions. Hence, partitioning a power grid circuit in an arbitrary fashion can lead to very slow convergence.

To address the above issue, a novel partitioning method, referred to as block row partitioning (BRP) scheme is developed. In the proposed method, the given power grid is partitioned into subcircuits consisting of blocks of rows enclosed by V_{DD} contacts as shown in Fig. 5.4. A more detailed description is given in Fig. 5.5, which shows the i^{th} BRP subcircuit with relaxation sources attached. The i^{th} BRP subcircuit shown here contains L rows. It is to be noted that, the V_{DD} contacts (represented by $\otimes$ in Fig. 5.5) are present only on the top and the bottom edges of the subcircuit, and the active power drains (represented by $\odot$) are present at

Figure 5.5: Subcircuit description for the i^{th} block in the BRP scheme

various locations. Here, a power grid with M columns is considered such that there are M resistors coupling the i^{th} BRP subcircuit to its neighbors, on each of the top and the bottom sides. In addition, assuming that there are F ideal voltage sources representing V_{DD} contacts on each of the top and the bottom sides of a particular partition, we have a total of $(2M - 2F)$ WR current sources on the top and bottom edges of the subcircuit as shown in Fig. 5.5, with

$$I_{WR,j}(t) = \hat{g}_j * v_{neigh,j}(t), \quad \forall 1 \leq j \leq (2M - 2F). \quad (5.7)$$

Figure 5.6: Voltage contours on a sample 50x50 grid without transient sources(for *Illustrative Example 2*).

Here, $\hat{g}_j$ is the coupling conductance term at a particular boundary node of this subcircuit and $v_{neigh,j}$ is the voltage at its (corresponding boundary node) neighboring node, in the adjoining BRP block.

It is to be noted that the proposed BRP scheme exploits the localized voltage transients in the power grids and identifies subcircuits based on it and hence leads to faster convergence. For the purpose of illustrating the connection between the BRP scheme and the localized voltage transients, the following example is considered.

Illustrative Example 2: In this example, localized behavior of voltage transients in a power grid is studied. For this purpose, a sample 50×50 power grid is considered.

First, the power grid is simulated in the absence of any transient current drains

Figure 5.7: Voltage contours on a sample 50x50 grid with a strong transient source at the center(for *Illustrative Example 2*).

(the only input sources in the circuit being the V_{DD} sources and the DC current drains). The corresponding voltages were measured at nodes of the grid for the entire duration of the simulation. The voltage contours in the grid are shown in Fig. 5.6. The white spots represent the V_{DD} contacts. As seen, the voltage distribution is quite uniform through out the grid.

Next, a single strong transient current source (a triangular pulse as shown in Fig. 2.15, with amplitude=100 mA, representing an active power drain) is added to the grid in the center to estimate the worst-case scenario, and the resulting circuit is simulated. Voltage was measured at all nodes of the grid for the entire time of simulation and the corresponding contours for the peak voltage drop are shown in Fig. 5.7. The darkest spot represents the worst voltage starved spots, which corresponds to

the position of the transient current source. It can be observed that even for such a strong current source, the voltage drops taper off to within 1 mV of the DC solution when we move away 10 nodes in any direction. Note that this strong locality in the transient behavior is an artifact of the regularity of V_{DD} contacts in the circuit [53]. In other words, the current requirement of power drains is met by the nearest voltage sources (V_{DD} contacts) rather than by the ones that are far away.

Since the proposed BRP scheme exploits the above phenomenon by dividing the power grid into subcircuits consisting of blocks of rows enclosed by V_{DD} contacts as shown in Fig. 5.4, it leads to faster convergence for both Gauss-Jacobi (GJ) and Gauss-Seidel (GS) based relaxation. This is because most of the current requirements of such a subcircuit are satisfied by the V_{DD} contacts that are within it (subcircuit). This is further verified by comparing it with other possible partitioning schemes, such as single row partitioning (SRP), which does not take into account the above discussed localized behavior and the corresponding details are given in Example 1 of Section 5.3 (Numerical Examples).

5.2.2 Computation of the initial-guess waveforms

In this section, fast convergence mechanisms, based on improved initial-guess waveform computations, are presented. The waveform relaxation algorithm described in Section 3.2 requires that the value of the voltages at all the nodes in the circuit must

Figure 5.8: Ramped waveform representing DC sources

be known exactly at time $t = 0$, as given in (3.2). This can be found by solving the DC version of (5.1),

$$\mathbf{G}\mathbf{X}(0) = \mathbf{b}_{DC}, \quad (5.8)$$

where $\mathbf{b}_{DC}$ represents the DC source vector. However, solving this equation using either direct or iterative solvers can be computationally expensive, and can severely undermine the efficiency of the solution process.

In order to overcome this difficulty, in the proposed algorithm, the problem of computing the DC solution is combined with the WR formulation for transient analysis (in other words, in the proposed algorithm, the DC solution comes naturally as a result of converged WR iterations). For this purpose, various types of sources in the given power grid circuit are treated as follows:

- 1) *DC sources in the partitioned blocks*

The DC voltage and current sources in the partitioned blocks (represented by $\otimes$ and $\odot$ respectively, in Fig. 5.5) are replaced with ramped sources, with the waveform as shown in Fig. 5.8. For example, to represent a DC source corresponding to a V_{DD} contact, the amplitude A_{DC} is set equal to V_{DD} . A suitable t_{DC} is chosen such that the steady-state of the circuit is reached before the actual transient sources in the circuit are switched on.

2) *Waveform relaxation sources at the boundary nodes of the partitioned blocks*

It is to be noted that, the proposed algorithm also requires waveform relaxation sources to be connected at the boundary nodes of the partitioned blocks (as shown in Fig. 5.5), representing the resistive coupling between the adjacent partitioned blocks (on both sides). Note that these relaxation sources are evaluated using (5.7), where $v_{neigh,j}(t)$ is the voltage at the corresponding neighboring node in the adjacent block. Accordingly, the initial-guess voltage waveforms for these boundary nodes of the partitioned blocks can also be represented by ramp type waveforms, as shown in Fig. 5.9. One of the obvious choices for the amplitudes (A_{WR}) of these waveforms is V_{DD} . However, this may not be accurate enough, and hence can lead to slow convergence of WR iterations [54]. To address this problem, a more accurate estimation of A_{WR} is required (i.e., the estimated values of A_{WR} used for the initial-guess voltage waveforms of the boundary nodes must be close to the final DC solution of these nodes). It is to be noted that, the final DC solution of the nodes in the power grid circuit

Figure 5.9: Ramped waveform representing the initial-guess for the boundary nodes of the partitioned blocks, while computing WR sources.

depend only upon the DC sources in the circuit (i.e, the V_{DD} sources and the DC current drains).

To accomplish the above (i.e, to obtain a good estimation for A_{WR}), the method described in [53] is appropriately adopted exploiting the fact that the effects of DC current sources in power grids are highly localized because of the regularity of the V_{DD} contacts. DC current sources, which draw current from the power distribution network obtain most of their currents from the closer V_{DD} sources than those which are farther away through more resistive paths. Exploiting this principle, the power grid is partitioned into tiles, consisting of non-overlapping *source-regions* between any four neighboring V_{DD} contacts, and overlapping *grid-shell* partitions enclosing each of these source-regions (as illustrated in Fig. 5.10). To obtain the DC voltages

Figure 5.10: A small area of the power grid shown with the highlighted source-region enclosed by its grid-shell.

for the nodes in each source-region, the corresponding grid-shell is simulated as an independent circuit, neglecting the effects of sources in other regions. For example, to obtain the node voltages of the source-region 14 (highlighted in Fig. 5.10), the corresponding grid-shell (which includes the regions 7, 8, 9, 13, 14, 15, 19, 20 and 21) is simulated and the corresponding boundary node voltages are recorded. Similarly, to obtain the boundary node voltages for the source-region 15, the grid-shell consisting of the regions 8, 9, 10, 14, 15, 16, 20, 21 and 22 is simulated. The voltages so obtained represent a good estimate for the amplitudes (A_{WR}) for the boundary node voltages

of a BRP partitioned block in that region.

It is to be noted that, power grids have a regular structure and leakage current profiles are uniform in a VLSI circuit. As a result, the above discussed DC source-regions differ only slightly from each other in a chip. Hence, in the proposed algorithm, a single representative source-region (or, if necessary, a set of representative source-regions) is defined for a power grid and the A_{WR} amplitudes estimated for these regions are replicated for the rest of the circuit, making the process very efficient. Since the individual grid-shells are quite small, the corresponding DC simulations can be completed in a very short time. In addition, since the simulation of these grid-shells are independent of each other, they can be executed in parallel giving rise to further savings in CPU time.

It is to be noted that for starting WR iterations, we only need a good estimate of A_{WR} and not its exact value. The DC levels in the waveform relaxation algorithm with this *fast* estimation of A_{WR} levels showed significant improvement in the accuracy of the final transient analysis results. This is demonstrated in Example 2 in Section 5.3. The computational steps for generating the initial-guess waveforms of the power grid node voltages are summarized in Pseudocode 5.1.

- Step 1:** Divide the entire power grid into non-overlapping source-regions and overlapping grid-shells as shown in Fig. 5.10.
- Step 2:** Identify a representative grid-shell partition or a set of representative grid-shell partitions for the entire grid.
- Step 3:** Compute the DC solution of the representative grid-shell partition by simulating it using the given independent DC sources.
- Step 4:** Map the solution of the representative source-region onto the relevant portion of the power grid and generate an approximate DC estimation for the boundary node voltages of the BRP partitioned blocks in that region. Let B be the set of boundary nodes in that region obtained as a result of BRP scheme and let $v_{DC,b}$ represent the estimate of the DC voltage obtained at a boundary node $b \in \{B\}$.
- Step 5:** Initialize the voltages of all the boundary nodes of the BRP partitioned blocks in the region, in the form of a ramped waveform shown in Fig. 5.9, with amplitude $A_{WR,b}$. Assign the amplitudes as follows:
 $A_{WR,b} = v_{DC,b} \quad \forall b \in \{B\}$.
- Step 6:** Repeat **Step 3-Step 5** for the various representative source-regions in the power grid.
- Step 7:** Replace the DC voltage sources corresponding to the V_{DD} contacts in the power grid circuit with ramped waveforms shown in Fig. 5.8, with amplitude $A_{DC} = V_{DD}$.
- Step 8:** Replace the DC current sources corresponding to the DC power drains in the power grid circuit with ramped waveforms shown in Fig. 5.8, with amplitude $A_{DC} = I_{DC}$.

Pseudocode 5.1: Computational steps for generating initial-guess waveforms for the proposed GS-WR algorithm.

5.2.3 Proposed GS-WR algorithm for transient analysis

For the application of waveform relaxation for a given power grid problem, the subcircuits are generated using the BRP partitioning scheme described in Section 5.2.1. The initial-guess waveforms for the relevant boundary nodes in these subcircuits are then generated using the technique presented in Section 5.2.2. Next, the Gauss-Seidel waveform relaxation process described in Section 3.2.2 is applied to the resulting subcircuits. Several observations regarding the implementation of the proposed algorithm are discussed below.

- 1) Since the RC models are used for the power grid circuits, the technique described in Section 3.3 (Fig. 3.3) for the implementation of the WR algorithm can be used to ensure the diagonal dominance of the subcircuits. Hence, in the proposed algorithm, while using both Gauss-Jacobi (GJ) as well as Gauss-Seidel (GS) waveform relaxation processes, convergence is guaranteed.
- 2) It is to be noted that, the GS-WR has many merits, such as better convergence, over the GJ-WR. In addition, GS-WR requires less memory consumption than GJ-WR. This is because, in GS-WR, the relaxation sources are computed as the solution is updated and hence, only one copy of the solution needs to be stored at any time. In contrast, in GJ-WR, the so-

Step 1: Generate the initial-guess waveforms for the node voltages in the power grid using the method described in Section 5.1.

Step 2: Partition the power grid network into subcircuit blocks numbered 1, 2, 3 ... as shown in Fig. 5.4.

Step 3: Define ϵ as the tolerance error for the convergence of waveform relaxation iterations.

Step 4: Set the number of iterations, $r = 1$.

Step 5: For each of the subcircuits 1, 2, 3... , do the following:

1. Calculate the WR sources $I_{WR}(t)$ for the current subcircuit as described in (5.7), using the voltages of the boundary nodes of the neighbouring subcircuits.
2. Simulate the current subcircuit for the entire time-interval of interest.
3. Update the voltages on the boundary nodes of the current subcircuit.

Step 6: Compute error=norm(*the difference between the waveform at the output node from the present and previous iterations*).

Step 7:

```

if (error  $\leq$   $\epsilon$ ) exit;
else  $r = r + 1$ , go to Step 5;
end

```

Pseudocode 5.2: Computational steps for the transient analysis of power grids via the proposed GS-WR algorithm.

lution from the previous iteration is used to calculate the WR sources in the current iteration and so, two sets of the solution need to be stored at any time. In power grid circuits, where the circuit sizes are typically of the order of millions of nodes, memory consumption is one of the major concerns. Hence in this thesis, GS-WR is employed for a fast, memory efficient transient analysis of power grid networks.

- 3) Since the step-size for the transient simulation of power grid circuits (using the backward Euler integration method) has been fixed based on the given rise-times of the switching circuits (as discussed in Section 5.1), the LU factors for each subcircuit need to be computed only once at the beginning of the first iteration of the proposed GS-WR algorithm. These LU factors can be reused for the subsequent iterations. This considerably reduces the CPU cost of the proposed algorithm.

The computational steps involved in the proposed GS-WR algorithm [17] are summarized in Pseudocode 5.2. In the next section, the performance of the proposed algorithm is demonstrated using various case studies.

5.3 Numerical results

In this section, four case studies are presented. The first experiment uses a test power grid circuit, to demonstrate the effectiveness of the proposed block row partitioning (BRP) scheme (Section 5.2.1) by comparing it with another partitioning scheme, which does not take into account the localized behavior of voltage transients in a power grid. The second experiment uses the same test circuit to illustrate the improvement in the accuracy of the DC-level in the final solution when the waveform relaxation algorithm is used in conjunction with the proposed initial-guess algorithm (Section 5.2.2). The third experiment considers several test power grid circuits of different sizes, and compares the performance of the proposed GS-WR algorithm with a direct solver method and a purely iterative technique. For the examples in case studies 1-3, all the simulations were run on a 1.60GHz Intel Xeon dual quad-core machine with 8 GB of RAM running Gentoo Linux. In the fourth experiment, the proposed GS-WR algorithm is applied to two large power distribution networks (PDNs) and the corresponding performance metrics are investigated.

In all the above experiments, while using the proposed waveform relaxation algorithm, all the partitioned subcircuits were solved using state-of-the-art direct solver [55] techniques in each iteration. The proposed algorithm was implemented on a C++ based linear circuit simulator (internal) with OpenMP multithreading extensions. This circuit simulator uses the backward Euler integration method for time-domain

analysis. The KLU package (direct solver) [55] is used to solve the resulting system of linear equations.

Example 1:

In this experiment, the performance of the proposed block row partitioning (BRP) scheme, which takes into account the localized behavior of voltage transients in a power grid (as described in Section 5.2.1), is investigated. For this purpose, its performance is compared with another partitioning scheme where single rows in the grid are treated as individual subcircuits (which does not take into account the localized behavior of voltage transients). This scheme is referred to as the single row partitioning (SRP) scheme (here, many of the subcircuits may not have V_{DD} sources and hence, may depend heavily on their neighbouring subcircuits for their current requirements). This implies that, in the SRP scheme, the information of the voltages and currents from the active nodes of a subcircuit needs to be transferred through many other subcircuits for obtaining convergence.

The superiority of the BRP scheme over SRP is illustrated using transient simulations performed on a test power grid circuit (referred to as *Ckt-1*), which contains 491,401 nodes. The circuit corresponds to a 2-metal layer on-chip power distribution network. Transient current sources with ramped waveforms as shown in Fig. 2.15 were used at various nodes on the grid, to represent the power drains in the PDN. The test circuit was simulated for a time period of 2 ns using the Gauss-Seidel waveform

Figure 5.11: Comparative study of convergence of waveform relaxation using the proposed BRP and SRP schemes for voltage transient waveforms at a sample node in *Ckt-1* (Example 1).

relaxation algorithm, first by employing the proposed BRP scheme and then using the SRP scheme. The resulting voltage waveforms at a sample node in the circuit are shown in Fig. 5.11. Here, the dashed line represents the solution obtained using the BRP scheme and the dotted line represents the solution obtained using the SRP scheme. For the purpose of further comparison, the exact solution was obtained by solving the circuit directly using LU decomposition and forward-backward substitutions for the entire grid. The corresponding result (exact solution) is shown by the solid line in Fig. 5.11. As seen, the proposed BRP scheme with just 5 iterations is significantly more accurate than 30 iterations of the SRP scheme.

Figure 5.12: Illustration of the impact on transient voltage waveforms while using WR algorithm: with and without appropriate DC-level estimation (Example 2).

Example 2:

In this example, the effectiveness of the proposed estimation of initial-guess waveforms and A_{WR} amplitudes (described in Section 5.2.2) is demonstrated. For this purpose, the same test power grid circuit *Ckt-1* described in the previous example, is used. Ramped current sources (with a waveform as shown in Fig. 5.8) were connected at various nodes on the grid as shown in Fig. 2.12, to represent the static power drains in the PDN.

For the execution of the proposed WR algorithm, initial-guess waveforms of the type in Fig. 5.8 (ramped sources) are used. The required A_{WR} amplitudes for the initial-guess voltage waveforms were calculated using the proposed method described

in Section 5.2.2, and the circuit was simulated via the proposed BRP scheme and GS-WR algorithm. The resulting voltage waveforms at a sample node after five iterations are shown in Fig. 5.12 using dashed lines. The above results are compared against the case of selecting initial-guess A_{WR} amplitudes simply equal to V_{DD} . Corresponding results (also using the same BRP scheme) are also plotted in Fig. 5.12 (using dotted lines).

The results from both the above simulations are also compared with the exact solution (shown in Fig. 5.12 using solid line). As seen from these plots, the proposed estimation of the A_{WR} amplitudes of the initial-guess waveforms shows significant improvement in the accuracy of the DC-level in the final transient analysis.

Example 3:

In this experiment, the computational efficiency of the proposed algorithm is compared with both a purely iterative technique and a direct-solver method using several test power grid circuits of varying sizes. In each experiment, the following analyses were performed.

- a) First, the test power grid circuits were simulated using a purely iterative solver. For this purpose, conventional Gauss-Seidel relaxation (referred to as *CGS* method in this thesis), was applied on the Kirchhoff's current law (KCL) based equations at individual nodes in the power grid circuit at each time point.

Table 5.1: CPU cost comparison of power grid analysis using different methods (Example 3)

Circuit	Circuit size (# of nodes)	CPU time (sec)		
		CGS method	Direct-LU solver	Proposed GS-WR method
<i>Ckt-1</i>	<i>491,401</i>	358.01	80.15	21.62
<i>Ckt-2</i>	<i>641,601</i>	537.41	116.15	29.22
<i>Ckt-3</i>	<i>811,801</i>	590.50	162.18	37.52
<i>Ckt-4</i>	<i>1,002,001</i>	755.60	230.64	47.14
<i>Ckt-5</i>	<i>1,212,201</i>	957.28	303.89	57.96
<i>Ckt-6</i>	<i>1,442,401</i>	1203.04	361.77	70.71

- b) In the next set of simulations, the given circuits were simulated using a conventional direct-solver technique. The direct-solver used in our experiments to solve the system of equations represented by (5.3) is the conventional LU decomposition based solver (KLU package [55]). This is referred to as the *direct-LU solver* method in this thesis.
- c) Finally, the same circuits were simulated using the proposed Gauss-Seidel waveform relaxation (GS-WR) algorithm, which combines the merits of *di-*

Figure 5.13: CPU cost comparison of power grid analysis using different methods (Example 3).

rect and *iterative* techniques, and the performance metrics are compared with the above analyses.

The above experiment was conducted for 6 different power grid circuits (*Ckt-1* to *Ckt-6*) of sizes varying from about 500,000 nodes to about 1.5 million nodes. In all these experiments, it was found that about 4-5 iterations were sufficient for achieving convergence using the proposed GS-WR algorithm. The convergence waveforms at a sample node in *Ckt-3* while using the proposed GS-WR method is shown in Fig. 5.14. For each of these simulations, the CPU cost comparison of all the above three methods are given in Table 5.1. The CPU times are also plotted against the increasing circuit size in Fig. 5.13. As seen from the table, the proposed GS-WR algorithm,

Figure 5.14: Convergence waveforms at a sample node in *Ckt-3* while using the proposed GS-WR method (Example 3).

which combines the merits of both the CGS and the direct-solvers, yields significant speed-ups compared to both the purely iterative or purely direct-solver based methods.

Example 4:

In this experiment, the proposed GS-WR algorithm is applied to two large industrial power grid examples, PG_1 and PG_2 , and the performance metrics are investigated. PG_1 is a power grid structure generated from a 4-metal layer PDN and PG_2 is generated from a 5-metal layer PDN. Both belong to a flip-chip package based micro-processor of dimensions $10\text{mm} \times 10\text{mm}$, built around a 65nm process [56]. The V_{DD} contacts are made at about every $300\mu\text{m}$ on the face of the chip, at the top metalliza-

tion layer. The resulting circuit PG_1 contained 2.5 million nodes and circuit PG_2 contained 7.5 million nodes.

All simulations in this experiment were run on the high performance computing virtual laboratory's (HPCVL) [57] SunFire machine. The SunFire is a symmetric multiprocessor (SMP) system based on the UltraSPARC line of processors and Solaris 10. The machine used for simulations in this experiment contained 72X dual-core UltraSPARC-IV+ 1.5 GHz processors with 576 GB of RAM.

These circuits were simulated for 100 time points using both the proposed GS-WR algorithm, and the direct-LU solver (KLU package [55]) technique. It was found that the proposed GS-WR algorithm converges to within 0.5mV of the exact solution of these circuits, in five iterations. This is illustrated in Fig. 5.15, via the transient

Figure 5.15: Convergence waveforms at a sample node in circuit PG_1 (Example 4).

Table 5.2: CPU cost comparison for simulating industrial power grid circuits (Example 4)

Circuit	Size (# of nodes)	Direct-LU method (hr:min:sec)	Proposed GS-WR method (hr:min:sec)	Speed Up
PG_1	2.5 million	1:03:05	00:42:00	1.51
PG_2	7.5 million	8:14:07	03:31:10	2.34

voltage plot at a sample node in PG_1 .

The above experiment was repeated for PG_2 . The resulting CPU simulation times, and the corresponding speed-ups compared to the direct-LU solver are tabulated in Table 5.2. As seen, while using the proposed GS-WR algorithm, the required simulation times are reduced considerably.

5.4 Summary

In this chapter, a novel algorithm for transient analysis of power distribution networks has been presented. The proposed method is based on Gauss-Seidel waveform relaxation techniques, and is hybrid in nature exploiting the advantages of both of direct and iterative solver methods. Efficient partitioning schemes and improved initial-guess estimation techniques were developed to achieve fast convergence. The

proposed algorithm gives significant speed-ups compared to both direct as well as conventional iterative solvers.

Chapter 6

Conclusions and Future Work

6.1 Summary

In this thesis, the waveform relaxation (WR) techniques were advanced for two important applications in high-speed VLSI design:

1. **EMI analysis of high-speed interconnects:** Using the tranverse partitioning (TP) technique [11], a system of high-speed interconnects represented by multiconductor transmission lines (MTLs) was divided into subcircuits consisting of individual lines. Sources representing the effect of EMI on these lines were formulated to be compatible with this WR-TP macromodel and a combined robust time-domain macromodel for fast EMI analysis was generated. The CPU cost of the simulations using this macromodel

was shown to increase only *linearly* with the number of lines in the MTL structure, as compared to the more than cubic increase exhibited by conventional EMI analyses.

2. **Fast transient analysis of Power Distribution Networks:** A new waveform relaxation based algorithm for the transient analysis of massive on-chip power distribution networks (PDNs) was proposed. Novel partitioning schemes, exploiting the localized voltage distribution behavior of the power grids and improved initial-guess generation mechanisms for faster convergence were developed. Test power grid structures and industrial standard power grid circuits were simulated, to demonstrate the efficiency of the proposed method.

The proposed algorithms are highly generic in nature and can be used in conjunction with any existing macromodel/circuit-solving technique, to obtain desirable results. For instance, in the case of EMI analysis, any MTL macromodel, such as matrix rational approximation (MRA) or delay extraction-based passive compact transmission line macromodel (DEPACT), can be used to describe the individual segments in the WR-TP algorithm to improve computational efficiency and accuracy. In the case of power grid analysis using the proposed WR algorithm, individual partitions can be simulated using any direct-solver technique for circuit simulation, such as QR-decomposition of matrices used with trapezoidal-rule for numerical integration of the

circuit equations, depending upon the given error criterion and matrix structures.

6.2 Future Work

Through the work in this thesis, many possibilities for future research have become apparent. They are summarized below.

1. **Parallel implementation of the proposed algorithms:** There is a tremendous potential to parallelize the proposed WR algorithms for EMI and power grid analysis on fast emerging parallel computing platforms, which could result in huge savings in CPU time. The general WR-TP algorithm for multiconductor transmission lines has already been parallelized [52]. The effects of EMI could be included in this algorithm, resulting in a parallel EMI analysis of high-speed interconnects.

In the case of power grids, research towards a parallel implementation of the proposed GS-WR algorithm for simulation in multi-core processor environments is already underway, in collaboration with other members of the CAD group [17]. The initial results in this direction are very encouraging.

2. **Extension of EMI analysis to include other macromodels:** EMI analyses of high-speed interconnects using DEPACT-based analytical closed-form macromodels have been shown to be superior to the lumped-segment

macromodel in terms of both accuracy and computational efficiency [22].

One area of future research would be to extend the proposed EMI analysis algorithm to include this closed-form macromodel, with further savings in CPU cost.

3. **Second order effects in power grid:** A resistive-capacitive model for the power distribution network was used for the implementation of the proposed algorithm. With the increasing operating frequencies of VLSI circuits, it is predicted that second order effects such as inductive coupling, distributed effects, package-power grid interaction, and electromagnetic interference would gain prominence in the operation of power grids in the near future. The inclusion of these effects in the early simulations of power grid would then be imperative. Hence, future research in power grid analysis would be to investigate the influence of these effects on circuit simulation and the feasibility of waveform relaxation techniques under these circumstances.
4. **Sensitivity analysis:** The behavior of high-speed interconnects and power distribution networks depends strongly on the design parameters such as metal width, spacing etc. In these cases, sensitivity analyses provide valuable insight into the upper and lower bounds of the performance metrics of the

circuits and their sensitivities to the process variations. In the presence of very large number of such design parameters, sensitivity analyses could become a time-consuming task, often taking days to complete. One area of future research would be to extend the principles of the proposed waveform relaxation-based techniques to large-scale sensitivity analysis and use parallel computing to make this analysis computationally efficient.

Appendix A

Weighting factors for WR algorithm in transmission lines

This appendix provides a discussion on selecting an appropriate weighing factor, w_m , in (4.16) and (4.17) [11,44]. Starting from (4.6) and (4.7), if we apply waveform relaxation techniques, we obtain a recursive set of decoupled differential equations of the form,

$$\frac{\partial}{\partial z} v_k^{(r+1)} = -r_{kk} i_k^{(r+1)}(z, t) - l_{kk} \frac{\partial}{\partial t} i_k^{(r+1)}(z, t) - e_k^{(r)}(z, t), \quad (\text{A-1})$$

$$\frac{\partial}{\partial z} i_k^{(r+1)} = -\hat{g}_{kk} v_k^{(r+1)}(z, t) - \hat{c}_{kk} \frac{\partial}{\partial t} v_k^{(r+1)}(z, t) - f_k^{(r)}(z, t), \quad (\text{A-2})$$

where, r represents the r^{th} iteration. Expressing (A-1) and (A-2) in frequency-domain, we obtain,

$$\frac{\partial}{\partial z} \mathbf{\Phi}_k^{(r+1)} = \mathbf{F}_k(s) \mathbf{\Phi}_k^{(r+1)}(z, s) + \mathbf{\Psi}_k^{(r)}(z, s), \quad (\text{A-3})$$

where

$$\Phi_k(z, s) = \begin{bmatrix} V_k(z, s) \\ I_k(z, s) \end{bmatrix}, \quad (\text{A-4})$$

$$\mathbf{F}_k(s) = \begin{bmatrix} 0 & -r_{kk} - sl_{kk} \\ -g_{kk} - sc_{kk} & 0 \end{bmatrix}, \quad (\text{A-5})$$

and

$$\Psi_k(z, s) = \begin{bmatrix} E_k(z, s) \\ F_k(z, s) \end{bmatrix}. \quad (\text{A-6})$$

The solution to (A-3) can be obtained in frequency-domain as,

$$\Phi_k^{(r+1)}(d, s) = e^{\mathbf{F}_k(s)d} \Phi_k^{(r+1)}(0, s) + \delta_k^{(r)}(d, s), \quad (\text{A-7})$$

where

$$\delta_k^{(r)}(d, s) = \int_0^d e^{\mathbf{F}_k(s)(d-z)} \Psi_k^{(r)}(z, s) dz. \quad (\text{A-8})$$

In the distributed approach of implementing the WR-TP method, the above integral can discretized into a weighted sum, using w_m as follows.

$$\delta_k^{(r)}(d, s) \approx \sum_{m=1}^M w_m e^{\mathbf{F}_k(s)(d-z_m)} \Psi_k^{(r)}(z_m, s) \Delta z_m. \quad (\text{A-9})$$

In [11], it is shown that (A-9) and the realization in Fig. 3 are equivalent. Hence, the weighting factors w_m can be derived based on the specific summation technique used to approximate the convolution integral in (A-8). For example, for piecewise constant approximation, the weighting factors can be conveniently chosen to be 1, with z_m

selected appropriately corresponding to Right Riemann, Left Riemann, or midpoint approximation [58]. Alternatively, Simpson's Rule or more advanced techniques can be used [58].

References

- [1] R. Achar and M. Nakhla, “Simulation of high-speed interconnects,” vol. 89, no. 5, pp. 693–728, May 2001.
- [2] A. Dounavis, R. Achar, and M. Nakhla, “A general class of passive macro-models for lossy multiconductor transmission lines,” *IEEE Trans. Microwave Theory Tech.*, vol. 49, no. 10, pp. 1686–1696, October 2001.
- [3] K. Branch, J. Morsey, A. Cangellaris, and A. Ruehli, “Physically consistent transmission line models for high-speed interconnects in lossy dielectrics,” *IEEE Trans. Adv. Packag.*, vol. 25, no. 2, pp. 129–135, May 2002.
- [4] A. Dounavis, N. Nakhla, and R. Achar, “Delay extraction and passive macromodeling of lossy coupled transmission lines,” *Symposium on Electrical Performance of Electronic Packaging*, October 2003.
- [5] N. Orhanovid, N. Tripathi, and P. Wang, “Generalized method of characteristics for the time domain simulation of multiconductor lossy transmis-

sion lines,” *IEEE International Symposium on Circuits and Systems*, May 1990.

- [6] E. Lelarasmee, A. Ruehli, and A. Sangiovanni-Vincentelli, “The waveform relaxation method for time-domain analysis of large scale intergrated circuits,” *IEEE Trans. Computer-Aided Design*, vol. CAD-I, pp. 131–145, August 1982.
- [7] G. Antonini, J. Ekman, and A. E. Ruehli, “Waveform relaxation for the parallel solution of large PEEC model problems,” *IEEE Trans. Electro-magn. Compat.*, pp. 1–6, July 2007.
- [8] G. Gristede, A. E. Ruehli, and C. Zukowski, “Convergence properties of waveform relaxation circuit simulation methods,” *IEEE Trans. Circuits Syst.*, vol. 45, no. 7, pp. 726–738, July 1998.
- [9] F. Y. Chang, “The generalized method of characteristics for waveform relaxation analysis of lossy coupled tranmission lines,” *IEEE Trans. Microwave Theory Tech.*, vol. 37, no. 12, pp. 2028–2038, December 1989.
- [10] F. Y. Chang, “Waveform relaxation analysis of RLCG transmission lines,” *IEEE Trans. Circuits Syst.*, vol. 37, no. 11, pp. 1394–1415, November 1990.

- [11] N. Nakhla, A. Ruehli, M. Nakhla, and R. Achar, "Simulation of coupled interconnects using waveform relaxation and transverse partitioning," *IEEE Trans. Adv. Packag.*, vol. 29, no. 1, February 2006.
- [12] N. Nakhla, A. Ruehli, M. Nakhla, R. Achar, and C. Chen, "Waveform relaxation techniques for simulation of coupled interconnects with frequency-dependent parameters," *IEEE Trans. Adv. Packag.*, vol. 30, no. 2, May 2007.
- [13] D. Paul, N. Nakhla, R. Achar, and M. Nakhla, "Parallel simulation of massively coupled interconnect networks," *IEEE Trans. Adv. Packag.*, 2008 (accepted).
- [14] A. Sridhar, N. Nakhla, R. Achar, M. Nakhla, and A. Ruehli, "Fast EMI analysis of high-speed interconnects via waveform relaxation and transverse partitioning," *IEEE Trans. Electromagn. Compat.*, (accepted for publication).
- [15] A. Sridhar, N. Nakhla, R. Achar, and M. Nakhla, "Fast EMC analysis of high-speed interconnects via WR and TP," in *Proc. IEEE Conference on Electrical Performance of Electronic Packaging*, Atlanta, USA, October 2007, pp. 329–332.

- [16] R. Achar, A. Sridhar, N. Nakhla, and M. Nakhla, "Parallel EMI analysis of large coupled interconnects via transverse partitioning and waveform relaxation," in *Proc. Asia-Pacific Symposium on Electromagnetic Compatibility*, May 2008, pp. 490–493.
- [17] R. Achar, M. Nakhla, H. Dhindsa, A. Sridhar, and D. Paul, "Parallel transient simulation of power grid networks via waveform relaxation," *IEEE Trans. Very Large Scale Integration Syst.*, (submitted).
- [18] R. Achar, M. Nakhla, A. Sridhar, H. Dhindsa, and D. Paul, "Fast analysis of power distribution networks using waveform relaxation," in *IEEE workshop on Signal Propagation on Interconnects*, May 2009, p. (submitted).
- [19] H. Dhindsa, A. Sridhar, R. Achar, M. Nakhla, and D. Paul, "Transient analysis of power grid networks via waveform relaxation techniques," in *Proc. IEEE MMT-S International workshop series on Signal Integrity and High-Speed Interconnects (IMWS)*, Guadalajara, Mexico, February 2009, pp. 91–94.
- [20] C. R. Paul, *Analysis of Multiconductor Transmission Lines*. New York: John Wiley & Sons, 1994.

- [21] A. Agarwal, H. Price, and S. Gurbaxani, "Transient response of multiconductor transmission lines excited by a nonuniform electromagnetic field," *IEEE Trans. Electromagn. Compat.*, no. 2, pp. 119–129, May 1990.
- [22] G. S. Shinh, "Closed-form macromodels for analysis of high-speed interconnects in the presence of electromagnetic fields," M. A. Sc. thesis, Carleton University, Ottawa, Canada, 2005.
- [23] F. Chang, "Transient analysis of lossless coupled transmission lines in an nonhomogeneous dielectric medium," *IEEE Trans. Microwave Theory Tech.*, no. 9, pp. 616–626, September 1970.
- [24] R. Khazaka and M. Nakhla, "Analysis of high-speed interconnects in the presence of EMI," *IEEE Trans. Microwave Theory Tech.*, vol. 46, no. 7, pp. 940–947, July 1998.
- [25] I. Maio and F. Canavero, "Analysis of crosstalk and field coupling to lossy MTLs in a SPICE environment," *IEEE Trans. Electromagn. Compat.*, vol. 38, no. 3, August 1996.
- [26] I. Erdin, A. Dounavis, R. Achar, and M. Nakhla, "A SPICE model for incident field coupling to lossy multiconductor transmission lines," *IEEE Trans. Electromagn. Compat.*, vol. 43, no. 4, pp. 485–494, November 2001.

- [27] G. Singh, N. Nakhla, R. Achar, and M. Nakhla, "Fast transient analysis of incident field coupling to multiconductor transmission lines," *IEEE Trans. Electromagn. Compat.*, vol. 48, no. 1, February 2006.
- [28] T. Chane and D. Zutter, "Selection of lumped element models for coupled lossy transmission lines," *IEEE Trans. Computer-Aided Design*, vol. 11, pp. 957–967, July 1991.
- [29] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital integrated circuits: a design perspective*. Pearson Education, 2003.
- [30] M. Swaminathan and A. Engin, *Power Integrity Modeling and Design for Semiconductors and Systems*. Upper Saddle River, NJ: Prentice Hall, 2007.
- [31] A. Waizman, O. Vikinski, and G. Sizikov, "CPU power delivery impedance profile resonances impact on FMAX," in *IEEE Conference on Electrical Performance of Electronic Packaging*, October 2006, pp. 119–122.
- [32] F. Najm, "A survey of power estimation techniques in VLSI circuits," *IEEE Trans. Very Large Scale Integration Syst.*, vol. 2, no. 4, pp. 446–455, December 1994.

- [33] J. Lau and S. Lee, *Chip scale package (CSP): design, materials, processes, reliability, and applications*. McGraw-Hill Professional, 1999.
- [34] J. Kozhaya, S. Nassif, and F. Najm, "A multigrid-like technique for power grid analysis," *IEEE Trans. Computer-Aided Design*, vol. 21, no. 10, pp. 1148–1160, October 2002.
- [35] C. Zhuo, J. Hu, M. Zhao, and K. Chen, "Power grid analysis and optimization using algebraic multigrid," *IEEE Trans. Computer-Aided Design*, vol. 27, no. 4, pp. 738–751, April 2008.
- [36] M. Zhao, R. Panda, S. Sapatnekar, and D. Blaauw, "Hierarchical analysis of power distribution networks," *IEEE Trans. Computer-Aided Design*, vol. 21, no. 2, pp. 159–168, February 2002.
- [37] H. Yu, Y. Shi, and L. He, "Fast analysis of structured power grid by triangularization based structure preserving model order reduction," in *Design Automation Conference ('06)*, San Francisco, USA, July 2006, pp. 205–210.
- [38] H. Qian, S. Nassif, and S. Sapatnekar, "Random walks in a supply network," in *Design Automation Conference ('03)*, Anaheim, USA, June 2003, pp. 93–98.

- [39] H. Qian, S. Nassif, and S. Sapatnekar, "Power grid analysis using random walks," *IEEE Trans. Computer-Aided Design*, vol. 24, no. 8, pp. 1204–1224, August 2005.
- [40] T. Chen and C. Chen, "Efficient large-scale power grid analysis based on preconditioned krylov-subspace iterative methods," in *Design Automation Conference ('01)*, Las Vegas, USA, June 2001, pp. 559–562.
- [41] Y. Zhong and M. Wong, "Fast algorithms for IR drop analysis in large power grid," in *IEEE/ACM International Conference on Computer-Aided Design ('05)*, San Jose, USA, November 2005, pp. 351–357.
- [42] Y. Zhong and M. Wong, "Efficient second-order iterative methods for IR drop analysis in power grid," in *IEEE/ACM International Conference on Computer-Aided Design ('07)*, San Jose, November 2007, pp. 768–773.
- [43] R. Bagnara, "A unified proof for the convergence of Jacobi and Gauss-Seidel methods," *Society for Industrial and Applied Mathematics Review*, vol. 37, no. 1, pp. 93–97, March 1995.
- [44] N. M. Nakhla, "Waveform relaxation and transverse partitioning algorithms for simulation of massively coupled interconnects," Ph.D. dissertation, Carleton University, Ottawa, Canada, 2008.

- [45] S. Christian and W. Fichtner, "Parasitic modes on printed circuit boards and their effects on EMC and signal integrity," *IEEE Trans. Electromagn. Compat.*, vol. 43, no. 4, November 2001.
- [46] G. Caccavo, G. Cerri, V. M. Primiani, L. Pierantoni, and P. Russo, "ESD field penetration into a populated metallic enclosure: a hybrid time-domain approach," *IEEE Trans. Electromagn. Compat.*, vol. 44, no. 1, February 2002.
- [47] M. G. M. Hussain, "Antenna patterns of nonsinusoidal waves with the time variation of a Gaussian pulse- Part I," *IEEE Trans. Electromagn. Compat.*, vol. 30, no. 4, November 1988.
- [48] G. Cerri, R. D. Leo, V. M. Primiani, and S. Pennesi, "Modeling of electromagnetic interference induced by electrostatic discharge (ESD) inside resonant structures," *IEEE Trans. Electromagn. Compat.*, vol. 44, no. 1, February 2002.
- [49] M. G. M. Hussain, "Antenna patterns of nonsinusoidal waves with the time variation of a Gaussian pulse- Part II," *IEEE Trans. Electromagn. Compat.*, vol. 30, no. 4, November 1988.
- [50] *HSPICE Simulation and Analysis User Guide*. Release U-2003.03-PA, Synopsys Inc., March 2003.

- [51] A. Sridhar, N. Natalie, R. Achar, and M. Nakhla, "Fast EMC analysis of high-speed interconnects via waveform relaxation and transverse partitioning," in *IEEE Conference on Electrical Performance of Electronic Packaging*, Atlanta, USA, October 2007, pp. 329–332.
- [52] N. Nakhla, M. Nakhla, R. Achar, and A. Ruehli, "Parallel simulation of high-speed interconnects using delay extraction and transverse partitioning," in *IEEE Conference on Electrical Performance of Electronic Packaging*, Atlanta, USA, October 2007, pp. 237–240.
- [53] E. Chiprout, "Fast flip-chip power grid analysis via locality and grid shells," in *IEEE Intl. Conference on Computer Aided Design*, San Jose, USA, November 2004, pp. 485–488.
- [54] M. Gander and A. Ruehli, "Optimized waveform relaxation methods for RC type circuits," *IEEE Trans. Circuits Syst.*, vol. 51, pp. 755–768, April 2004.
- [55] T. A. Davis, *Direct methods for sparse linear systems*. Philadelphia, USA: SIAM, September 2006.
- [56] Private communication: K. Mihan, Javelin Design Automation, Ottawa, Canada.

- [57] High Performance Computing Virtual Laboratory, <http://www.hpcvl.org/>.
- [58] P. J. Davis and P. Rabinowitz, *Methods of Numerical Integration*, 2nd ed.
New York: Academic, 1984.