1

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS
STANDARD REFERENCE MATERIAL 1010a
(ANSI and ISO TEST CHART No. 2)

National Library
of Canada

Acquisitions and
Bibliographic Services Branch

395 Wellington Street
Ottawa, Ontario
K1A 0N4

Bibliothèque nationale
du Canada

Direction des acquisitions et
des services bibliographiques

395, rue Wellington
Ottawa (Ontario)
K1A 0N4

Your file Votre référence

Our file Notre référence

NOTICE

The quality of this microform is heavily dependent upon the quality of the original thesis submitted for microfilming. Every effort has been made to ensure the highest quality of reproduction possible.

If pages are missing, contact the university which granted the degree.

Some pages may have indistinct print especially if the original pages were typed with a poor typewriter ribbon or if the university sent us an inferior photocopy.

Reproduction in full or in part of this microform is governed by the Canadian Copyright Act, R.S.C. 1970, c. C-30, and subsequent amendments.

AVIS

La qualité de cette microforme dépend grandement de la qualité de la thèse soumise au microfilmage. Nous avons tout fait pour assurer une qualité supérieure de reproduction.

S'il manque des pages, veuillez communiquer avec l'université qui a conféré le grade.

La qualité d'impression de certaines pages peut laisser à désirer, surtout si les pages originales ont été dactylographiées à l'aide d'un ruban usé ou si l'université nous a fait parvenir une photocopie de qualité inférieure.

La reproduction, même partielle, de cette microforme est soumise à la Loi canadienne sur le droit d'auteur, SRC 1970, c. C-30, et ses amendements subséquents.

Canada

A Technique for On-Chip Analog VLSI Circuit Testing

by

Kenny W. L. Tung, B. Eng.

**A thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfilment of the requirements
for the degree of
Master of Engineering**

**Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Faculty of Engineering
Carleton University
September, 1993**

© K.W.L. Tung 1993

National Library
of Canada

Acquisitions and
Bibliographic Services Branch

395 Wellington Street
Ottawa, Ontario
K1A 0N4

Bibliothèque nationale
du Canada

Direction des acquisitions et
des services bibliographiques

395, rue Wellington
Ottawa (Ontario)
K1A 0N4

Your file Votre référence

Our file Notre référence

The author has granted an irrevocable non-exclusive licence allowing the National Library of Canada to reproduce, loan, distribute or sell copies of his/her thesis by any means and in any form or format, making this thesis available to interested persons.

L'auteur a accordé une licence irrévocable et non exclusive permettant à la Bibliothèque nationale du Canada de reproduire, prêter, distribuer ou vendre des copies de sa thèse de quelque manière et sous quelque forme que ce soit pour mettre des exemplaires de cette thèse à la disposition des personnes intéressées.

The author retains ownership of the copyright in his/her thesis. Neither the thesis nor substantial extracts from it may be printed or otherwise reproduced without his/her permission.

L'auteur conserve la propriété du droit d'auteur qui protège sa thèse. Ni la thèse ni des extraits substantiels de celle-ci ne doivent être imprimés ou autrement reproduits sans son autorisation.

ISBN 0-315-89909-3

Canada

Name Kenny W.L. Tung

Dissertation Abstracts International is arranged by broad, general subject categories. Please select the one subject which most nearly describes the content of your dissertation. Enter the corresponding four-digit code in the spaces provided.

Electronics

SUBJECT TERM

0544

SUBJECT CODE

U·M·I

Subject Categories

THE HUMANITIES AND SOCIAL SCIENCES

COMMUNICATIONS AND THE ARTS

Architecture 0729
Art History 0377
Cinema 0900
Dance 0378
Fine Arts 0357
Information Science 0723
Journalism 0391
Library Science 0399
Mass Communications 0708
Music 0413
Speech Communication 0459
Theater 0465

EDUCATION

General 0515
Administration 0514
Adult and Continuing 0516
Agricultural 0517
Art 0273
Bilingual and Multicultural 0282
Business 0688
Community College 0275
Curriculum and Instruction 0727
Early Childhood 0518
Elementary 0524
Finance 0277
Guidance and Counseling 0519
Health 0680
Higher 0745
History of 0520
Home Economics 0278
Industrial 0521
Language and Literature 0279
Mathematics 0280
Music 0522
Philosophy of 0998
Physical 0523

Psychology 0525
Reading 0535
Religious 0527
Sciences 0714
Secondary 0533
Social Sciences 0534
Sociology of 0340
Special 0529
Teacher Training 0530
Technology 0710
Tests and Measurements 0288
Vocational 0747

LANGUAGE, LITERATURE AND LINGUISTICS

Language 0679
General 0289
Ancient 0290
Linguistics 0291
Modern
Literature 0401
General 0294
Classical 0295
Comparative 0297
Medieval 0298
Modern 0316
African 0591
American 0305
Asian 0352
Canadian (English) 0355
Canadian (French) 0593
English 0311
Germanic 0312
Latin American 0315
Middle Eastern 0313
Romance 0314
Slavic and East European

PHILOSOPHY, RELIGION AND THEOLOGY

Philosophy 0422
Religion
General 0318
Biblical Studies 0321
Clergy 0319
History of 0320
Philosophy of 0322
Theology 0469

SOCIAL SCIENCES

American Studies 0323
Anthropology
Archaeology 0324
Cultural 0326
Physical 0327
Business Administration
General 0310
Accounting 0272
Banking 0770
Management 0454
Marketing 0338
Canadian Studies 0385
Economics
General 0501
Agricultural 0503
Commerce-Business 0505
Finance 0508
History 0509
Labor 0510
Theory 0511
Folklore 0358
Geography 0366
Gerontology 0351
History
General 0578

Ancient 0579
Medieval 0581
Modern 0582
Black 0328
African 0331
Asia, Australia and Oceania 0332
Canadian 0334
European 0335
Latin American 0336
Middle Eastern 0333
United States 0337
History of Science 0585
Law 0398
Political Science
General 0615
International Law and Relations 0616
Public Administration 0617
Recreation 0814
Social Work 0452
Sociology
General 0626
Criminology and Penology 0627
Demography 0938
Ethnic and Racial Studies 0631
Individual and Family Studies 0628
Industrial and Labor Relations 0629
Public and Social Welfare 0630
Social Structure and Development 0700
Theory and Methods 0340
Transportation 0709
Urban and Regional Planning 0999
Women's Studies 0453

THE SCIENCES AND ENGINEERING

BIOLOGICAL SCIENCES

Agriculture
General 0473
Agronomy 0285
Animal Culture and Nutrition 0475
Animal Pathology 0476
Food Science and Technology 0359
Forestry and Wildlife 0478
Plant Culture 0479
Plant Pathology 0480
Plant Physiology 0817
Range Management 0777
Wood Technology 0746
Biology
General 0306
Anatomy 0287
Biostatistics 0308
Botany 0309
Cell 0379
Ecology 0329
Entomology 0353
Genetics 0369
Limnology 0793
Microbiology 0410
Molecular 0307
Neuroscience 0317
Oceanography 0416
Physiology 0433
Radiation 0821
Veterinary Science 0778
Zoology 0472
Biophysics
General 0786
Medical 0760

EARTH SCIENCES

Biogeochemistry 0425
Geochemistry 0996

Geodesy 0370
Geology 0372
Geophysics 0373
Hydrology 0388
Mineralogy 0411
Paleobotany 0345
Paleoecology 0426
Paleontology 0418
Paleozoology 0985
Palynology 0427
Physical Geography 0368
Physical Oceanography 0415

HEALTH AND ENVIRONMENTAL SCIENCES

Environmental Sciences 0768
Health Sciences
General 0566
Audiology 0300
Chemotherapy 0992
Dentistry 0567
Education 0350
Hospital Management 0769
Human Development 0758
Immunology 0982
Medicine and Surgery 0564
Mental Health 0347
Nursing 0559
Nutrition 0570
Obstetrics and Gynecology 0380
Occupational Health and Therapy 0354
Ophthalmology 0381
Pathology 0571
Pharmacology 0419
Pharmacy 0572
Physical Therapy 0382
Public Health 0573
Radiology 0574
Recreation 0575

Speech Pathology 0460
Toxicology 0383
Home Economics 0386

PHYSICAL SCIENCES

Pure Sciences
Chemistry
General 0485
Agricultural 0749
Analytical 0486
Biochemistry 0487
Inorganic 0488
Nuclear 0738
Organic 0490
Pharmaceutical 0491
Physical 0494
Polymer 0495
Radiation 0754
Mathematics 0405
Physics
General 0605
Acoustics 0986
Astronomy and Astrophysics 0606
Atmospheric Science 0608
Atomic 0748
Electronics and Electricity 0607
Elementary Particles and High Energy 0798
Fluid and Plasma 0759
Molecular 0609
Nuclear 0610
Optics 0752
Radiation 0756
Solid State 0611
Statistics 0463
Applied Sciences
Applied Mechanics 0346
Computer Science 0984

Engineering
General 0537
Aerospace 0538
Agricultural 0539
Automotive 0540
Biomedical 0541
Chemical 0542
Civil 0543
Electronics and Electrical 0544
Heat and Thermodynamics 0348
Hydraulic 0545
Industrial 0546
Marine 0547
Materials Science 0794
Mechanical 0548
Metallurgy 0743
Mining 0551
Nuclear 0552
Packaging 0549
Petroleum 0765
Sanitary and Municipal System Science 0790
Geotechnology 0428
Operations Research 0796
Plastics Technology 0795
Textile Technology 0994

PSYCHOLOGY

General 0621
Behavioral 0384
Clinical 0622
Developmental 0620
Experimental 0623
Industrial 0624
Personality 0625
Physiological 0989
Psychobiology 0349
Psychometrics 0632
Social 0451

**The undersigned recommend to the Faculty of Graduate Studies
and Research acceptance of the thesis**

"A Technique for On-Chip VLSI Circuit Testing"

**submitted by Kenny W. L. Tung, B. Eng.
in partial fulfillment of the requirements for
the degree of Master of Engineering**

Thesis Supervisor

Chair, Department of Electronics

**Carleton University
September, 1993**

Abstract

The objective of this thesis is to investigate the possibility of implementing the $\Sigma\Delta$ modulator on-chip for analog-circuit testing. The investigation concentrates on using the $\Sigma\Delta$ modulator to measure the AC characteristics of an Op-Amp. Simulation results using a Two-Stage-Third-Order (T2S3) $\Sigma\Delta$ modulator to measure the slew rate and bandwidth are presented. It is shown that a $\Sigma\Delta$ modulator can be used for measuring slew rate and bandwidth using a moderate oversampling factor. The limitations imposed on using the technique by the $\Sigma\Delta$ moderator are discussed and analyzed. Finally, in an attempt to remove random error added by $\Sigma\Delta$ modulator, the use of the auto-correlation technique, and of multi-level and adaptative quantizers to improve its measuring capability is investigated.

Acknowledgments

I would like to express my gratitude to my thesis supervisor, Prof. T. A. Kwasniewski for his support and guidance during the course of this project. His assistance in developing and refining many ideas explored in this thesis was invaluable.

I would also like to thank my mother and my sister, Alice, for their support and encouragement. To whom I dedicate this thesis.

Table of Contents

Chapter 1	Introduction	1
1.1	Thesis Motivation and Objective.....	1
1.2	Thesis Organization.....	2
Chapter 2	Overview of Analog Circuit Testing Techniques	3
2.1	Consistency Checking Method	4
2.2	Analog Built-In Self-Test (ABIST) Structure	6
2.3	Fault Diagnosis based on Sensitivity Computation and Functional Testing.....	7
2.4	D.C. Fault Dictionary	8
2.5	Digital Modelling	9
2.6	Conclusion	10
Chapter 3	Analog Circuit Testing Using DSP Techniques	12
3.1	Proposed Technique	13
3.2	Theory of Oversampling A/D Converters	15
3.2.1	First-Order Sigma-Delta ($\Sigma\Delta$) Modulators	16
3.3	Testing of Op-Amp using the Proposed Technique	19
3.3.1	Experimental Setup	20
3.4	Slew Rate	22
3.4.1	Slew Rate measurement	25
3.4.2	Unity Gain Bandwidth (GBW).....	27
3.5	Conclusion	31
Chapter 4	Architecture Alternatives and Characteristics for Sigma-Delta Modulators	32
4.1	Characterization Technique	34
4.2	Double-Integration $\Sigma\Delta$ (DI $\Sigma\Delta$) Modulators	39
4.2.1	Triple-Integration $\Sigma\Delta$ (TISD) Modulator	43
4.2.2	Two-Stage Third-Order $\Sigma\Delta$ (T2S3) Modulator	47
4.2.3	Three-Stage Third-Order $\Sigma\Delta$ (T3S3) Modulator	51

4.3	Effect of Circuit Nonidealities	53
4.4	Conclusions	55
Chapter 5	Verification of the Proposed Technique Using Simulation	58
5.1	$\Sigma\Delta$ Modulator Measuring Capability	59
5.1.1	Demodulation Process	59
5.1.2	Slew Rate Measurement	61
5.1.3	Unity Gain Bandwidth (GBW) Measurement	67
5.1.4	Simulation Results	72
5.2	Measurement of Damped Second-Order Operational Amplifier Circuits	76
5.3	Techniques to Improve the Measuring Capability of $\Sigma\Delta$ Modulator	80
5.3.1	Noise Reduction Using Auto-Correlation on Periodic Square Wave	81
5.3.2	Multi-level Quantizer	86
5.3.3	Adaptive Quantizer	92
5.4	Conclusion	96
Chapter 6	Conclusions and Recommendation for Further Work	98
6.1	Summary and Conclusions	98
6.2	Recommendations for Future Work	100
Appendix A	Blackman-Harris Window	106

List of Figures

Figure 2.1.	Example circuit for consistent method checking technique.	5
Figure 2.2.	An ABIST structure.	6
Figure 3.1.	Block diagram of the proposed testing technique.	13
Figure 3.2.	Topology of a $\Sigma\Delta$ modulator.	16
Figure 3.3.	Block diagram in Z-Transform.	17
Figure 3.4.	Frequency response of the noise shaping term for a first order $\Sigma\Delta$ modulator.	18
Figure 3.5.	Block diagram of second-order $\Sigma\Delta$ modulator.	21
Figure 3.6.	Coefficients (impulse response) and frequency response of the low-pass filter	22
Figure 3.7.	Voltage follower using generalized Op-Amp model.	23
Figure 3.8.	Non-linear Transfer characteristics of the input stage.	23
Figure 3.9.	Effect of slew rate on the output of a voltage follower.	25
Figure 3.10.	Test circuit configuration.	26
Figure 3.11.	The effect of sampling rate on the recovered waveform for slew rate (a) 0.3V/us and (b) 2.0V/us.	27
Figure 3.12.	Effect of slew rate on the power spectrum.	28
Figure 3.13.	Improved power spectrum using proposed technique.	29
Figure 3.14.	Power spectrums for sampling rate (a) 20.48MHz and (b) 40.96MHz.	30
Figure 4.1.	The simulation environment for the characterization of the $\Sigma\Delta$ modulators.	34
Figure 4.2.	z-domain block diagram for (a) Double-Integration $\Sigma\Delta$ modulator (b) Triple-Integration $\Sigma\Delta$ modulator.	36
Figure 4.3.	z-domain block diagram for Three-Stage Third-Order $\Sigma\Delta$ modulator.	37
Figure 4.4.	z-domain block diagram for Two-Stage Third-Order $\Sigma\Delta$ modulator.	38
Figure 4.5.	SNR plot for a Double-Integration Sigma-Delta modulator.	40
Figure 4.6.	Output Vs. DC input plot for DISD.	41
Figure 4.7.	Idle channel noise against DC input for DISD.	41
Figure 4.8.	DC error plot for DISD.	42
Figure 4.9.	Inband quantization noise for Input=0.255.	42
Figure 4.10.	SNR plot for Triple-Integration $\Sigma\Delta$ modulator.	44

Figure 4.11.	Output vs. Input plot for Triple-Integration $\Sigma\Delta$ modulator.	45
Figure 4.12.	Idle channel noise plot for Triple-Integration $\Sigma\Delta$ modulator.	46
Figure 4.13.	DC Error plot for Triple-Integration $\Sigma\Delta$ modulator.	46
Figure 4.14.	SNR calculation for Two-Stage Third-Order $\Sigma\Delta$ modulator.	48
Figure 4.15.	Idle channel noise plot for Two-Stage Third-Order $\Sigma\Delta$ modulator.	49
Figure 4.16.	DC error plot for Two-Stage Third-Order $\Sigma\Delta$ modulator.	49
Figure 4.17.	SNR plot for Three-Stage Third-Order $\Sigma\Delta$ modulator.	51
Figure 4.18.	Idle channel noise for Three-Stage Third-Order $\Sigma\Delta$ modulator.	52
Figure 4.19.	DC error for Three-Stage Third-Order $\Sigma\Delta$ modulator.	52
Figure 4.20.	SNR for T2S3 when $a_2 = 0.225$	54
Figure 4.21.	DC Error for T2S3 when $a_2 = 0.225$	54
Figure 5.1.	Demodulation process of $\Sigma\Delta$ modulator.	60
Figure 5.2.	Magnitude plot for filter ($f_{cutoff} = 0.06 * f_s$) and quantization noise transfer functions.	63
Figure 5.3.	Recovered output waveform ($f_{cutoff} = 0.06 * f_s$).	64
Figure 5.4.	Recovered Output Waveform ($f_{cutoff} = 0.04 * f_s$).	65
Figure 5.5.	Recovered Output Waveform ($f_{cutoff} = 0.002 * f_s$).	65
Figure 5.6.	3-D Surface Plot for Measured Slew Rate Using T2S3.	66
Figure 5.7.	Contour for the 3-D Surface of Measured Slew Rate.	66
Figure 5.8.	Bode Plot illustrating the relationship of closed-loop bandwidth of the test circuit and open-loop bandwidth of the Op-Amp.	67
Figure 5.9.	Power spectrum for Op-Amp with GBW of 0.003MHz.	69
Figure 5.10.	Power spectrum for Op-Amp with GBW of 0.03MHz.	69
Figure 5.11.	Power spectrum for Op-Amp with GBW of 0.1MHz.	70
Figure 5.12.	Power spectrum for Op-Amp with GBW of 0.3MHz.	70
Figure 5.13.	Figure showing the power spectrum distorted by slew rate vs. one recovered using the curve shifting technique discussed.	71
Figure 5.14.	3-D Surface plot showing the measured GBW by T2S3.	73
Figure 5.15.	Contour plot showing the accuracy of the measured GBW by T2S3.	73
Figure 5.16.	Power spectrum of a critically damped operational circuit ($f_t = 0.1\text{MHz}$).	77

Figure 5.17.	Power spectrum of a underdamped operational circuit ($f_t=f_p=0.1\text{MHz}$).	78
Figure 5.18.	Power spectrum of a underdamped operational circuit ($f_t=0.1\text{MHz}$, $f_p=0.0125\text{MHz}$).	80
Figure 5.19.	Power spectrum of DUT ($f_t = 0.3\text{MHz}$) using input square wave with frequency $f_i = 10\text{KHz}$	84
Figure 5.20.	Windowed auto-correlation of the differentiated waveform.	84
Figure 5.21.	Power spectrum of the DUT by performing FFT on the auto- correlation function shown in Fig. 5.19.	85
Figure 5.22.	Power spectrum of the DUT with $f_t=0.6\text{MHz}$ (Solid line in the figure represents the approximation).	85
Figure 5.23.	SNR for T2S3 $\Sigma\Delta$ modulator using multi-level quantizer.	86
Figure 5.24.	Idle channel noise calculation for T2S3 using 16-level quantizer.	88
Figure 5.25.	DC error calculation for T2S3 using 16-level quantizer.	88
Figure 5.26.	Power spectrum using multi-level quantizer ($f_t=0.4\text{MHz}$).	89
Figure 5.27.	Power spectrum using multi-level quantizer ($f_t=0.6\text{MHz}$).	89
Figure 5.28.	Estimation of 3-dB point using the curve fitting method for DUT with $f_t= 0.4\text{MHz}$	90
Figure 5.29.	Estimation of 3-dB point using the curve fitting method for DUT with $f_t= 0.6\text{MHz}$	90
Figure 5.30.	Structure of a first-order $\Sigma\Delta$ modulator using feedfor- ward adaptative quantizer.	93
Figure 5.31.	SNR calculation for a T2S3 $\Sigma\Delta$ modulator using an adaptive quantizer.	94
Figure 5.32.	Gain measurement of the T2S3 $\Sigma\Delta$ modulator using an adaptive quantizer.	95
Figure 5.33.	Power spectrum using the T2S3 $\Sigma\Delta$ modulator with adaptive quantizer.	95
Figure A.1.	Magnitude plot for four-term Blackman-Harris window.	107
Figure A.2.	Log-Magnitude plot of transform of four-term Blackman-Harris window.	107

List of Tables

TABLE 4.1.	Coefficients for Double-Integration $\Sigma\Delta$ modulator	39
TABLE 4.2.	Coefficients for Triple-Integration $\Sigma\Delta$ modulator	44
TABLE 4.3.	Coefficients for Two-Stage Third-Order $\Sigma\Delta$ modulator	50
TABLE 4.4.	Coefficients for Three-Stage Third-Order $\Sigma\Delta$ modulator	53
TABLE 4.5.	Summary of analysis results	56
TABLE 5.1.	Table showing how the number of samples can affect the accuracy of slew rate measurements for a DUT with $f_t =$ 0.1 MHz.	63
TABLE 5.2.	Measured results for slew rate and GBW.	75
TABLE 5.3.	Results of GBW measurements vs. input square wave frequency.	83
TABLE 5.4.	The required oversampling ratio for GBW measurements for each noise reduction technique.	97

List of Symbols

ABIST	Analog-Built-In-Self-Test
AIWN	Additive Independent White Noise
ADC	Analog-to-Digital Converter
A/D	Analog-to-Digital
BIST	Built-In-Self-Test
Δ	The distance between quantization level.
dB	decibel
D/A	Digital-to-Analog
DISD	Double-Integration $\Sigma\Delta$ modulator
DSP	Digital Signal Processing
DUT	Device-Under-Test
$\Sigma\Delta$	Sigma-Delta
f_s	Sampling Frequency of the $\Sigma\Delta$ modulator
f_t	Unity Gain Bandwidth of the DUT
FFT	Fast Fourier Transform
FIR	Finite Impulse Response filter
GBW	Unity Gain Bandwidth
Op-Amp	Operational Amplifier

RMS	Root Mean Square
SNR	Signal-to-Noise Ratio
T2S3	Two-Stage Third-Order $\Sigma\Delta$ modulator
T3S3	Three-Stage Third-Order $\Sigma\Delta$ modulator
TISD	Triple-Integration $\Sigma\Delta$ modulator

CHAPTER 1

Introduction

Advances in Integrated Circuits (IC) process technology have enabled the design of complex analog and mixed-signal devices to the extent that devices with over fifty Operational-Amplifiers (Op-Amp) are not uncommon. Because of their size, manual testing of these types of devices has become impractical. Traditional on-chip testing methods for analog circuits are limited to open/short fault detection, which is generally not adequate for high performance analog circuitry. Devices that are free of catastrophic faults do not guarantee that they will meet all parametric specification constraints and be functional in the target systems. Normally, these devices have to be re-tested using expensive and complex testers to ensure they meet tight design specifications.

1.1 Thesis Motivation and Objective

The primary research goal of this thesis is to address the testability issue by implementing an on-chip oversampling A/D Converter for analog circuit testing. The use of an on-chip A/D converter allows fault detection and parametric measurements to be conducted simultaneously and eliminates the requirement for expensive testing hardware. The conversion of test data to digital form provides added benefits in that digital data has higher noise immunity and can be transmitted to remote test equipment without using expensive shielded cable. Although conventional A/D converters can be used for this purpose, they are expensive and usually require post-fabrication trim-

ming. Oversampled A/D converters, on the other hand, have high tolerance for circuit imperfections and require a minimal number of analog components. In addition, the output of an oversampling A/D is usually no more than a few bits wide, and therefore does not increase the pin overhead. However, the requirements of an extremely high sampling rate for this type of converter, normally a hundred times above the Nyquist frequency of the sampled signal, may impose limitations for its usage in this area. The aim of this thesis is to study whether accurate measurements can be made without meeting the normally required oversampling ratio for $\Sigma\Delta$ modulator.

1.2 Thesis Organization

This thesis comprises six chapters. Chapter 2 studies some of the proposed analog circuit testing techniques that have attempted to address the testability issues facing this type of circuit; the chapter concludes with a summary of drawbacks that plagued these techniques. An overview of the oversampling A/D converter and the technique of using a second-order oversampling converter for slew rate measurements are presented in Chapter 3. Chapter 4 studies the architectures of different oversampling A/D converters, followed by a complete characterization to analyze whether oversampling A/D converters are suitable for precision measurement application. This is due to fact that the quantization noise for oversampling A/D converters are highly DC-bias dependent and the work is required to ensure that it will not affect the measuring accuracy of the proposed technique. Chapter 5 provides a detailed analysis of the use of a fully characterized oversampling A/D converter for circuit measurement. Simulation results are presented and analyzed; techniques to further improve the measuring capability of an oversampling A/D converter are discussed at the end of the chapter. Finally, Chapter 6 summarizes the findings of the thesis and conclusions are drawn.

CHAPTER 2

Overview of Analog Circuit Testing Techniques

The testing of analog circuits is generally more difficult and costly than that of digital circuits because of their complex dynamic behavior. Although efforts have been devoted to develop efficient test methodologies for digital circuits, very little has been accomplished on the analog front. The advent of integrated circuit technology, which allows designers to pack increasingly more circuitry on silicon and implement mixed-signal circuits, has further complicated the testability issues for analog integrated circuits.

The main difficulties in testing analog integrated circuits can be summarized as follows:

- Analog circuits have complicated input-to-output characteristics that vary from one type of circuit to another; different test setup and input stimuli are required for different types of circuitry.
- They are susceptible to noise and electromagnetic interference and require stable ambient conditions.
- They have limited accessibility to internal critical nodes which limits the observability of the device under normal and faulty conditions.

- Technological disparity exists between newly designed circuits and testing equipment.

In recent years, many analog circuit fault detection and diagnostic techniques have been developed to address some of these issues. Most of the techniques developed so far are simulation based and require extensive computation. This chapter will provide an overview on some of the recently published ones.

2.1 Consistency Checking Method [MW89]

This technique is used for detecting and locating faults in analog circuits by checking that the measurements are consistent with the circuit function. Fault detection is conducted as follows: stimuli are applied to the input nodes and measurements are taken at the output nodes of the Device-Under-Test (DUT) and compared with the expected values. The circuit is assumed to be faulty if any one of the measured values differ from the expected value by more than the allowed tolerance. Otherwise, the circuit is fault-free.

To locate the fault(s) in the circuit, computer simulation is used. The circuit is first partitioned into blocks with each block represented by a model. Unlike models for a circuit simulator, the models used in this technique are a set of rules that describe the mode(s) of behavior of the block. For example, a resistor has only one mode of behavior which states that the sum of currents at the two connections must be zero.

At the start of the simulation, all external (input and output) nodes are forced with values that were used in or obtained from the real measurements; all internal nodes are set to extremes of possible values (e.g. power rail voltage). The simulator is not allowed to change the external values but is allowed to propagate the values at its input into the circuit based on the rules of the models. The new values will thus overwrite the preset values. For a fault-free circuit, all values between the input and output of models

Figure 2.1. Example circuit for consistent method checking technique.

should be consistent with the rule used in the model. However, for circuits with faults, inconsistency occurs between the input and output of one or more models. The location of the faulty block can thus be deduced as follows: if consistency is restored by removing the consistency constraint of the model, the block represented by the model is at fault.

The technique is illustrated by application on the example circuit in Fig. 2.1, assuming the gains of X, Y, and Z are 1, 2 and 3 respectively. If the input at A is 1, then, for a fault-free circuit, the measured values at C and D will be 2 and 3 respectively. However, if the measured value at C is 0.1 instead, a fault is assumed to occur. Using the consistency checking technique discussed above, simulation will show that an inconsistency occurs at node B due the fact that a conflicting value at B will be required to keep the values at C and D to the measured values. By suspending the consistency constraint on Block Y (i.e. the gain constraint at Block Y is suspended), the consistency of the circuit is restored. It can therefore be deduced that Block Y is faulty.

2.2 Analog Built-In Self-Test (ABIST) Structure [Wey90]

The ABIST structure proposed by Wey is modelled after the BIST structure [McC85] using a scan-path for digital circuits. The idea behind using BIST structure is to allow access to the internal nodes without increasing pin overhead; because of the increased number of test points available, fault diagnosis can be significantly simplified. The structure of an ABIST is shown in Fig. 2.2. The shift registers used for a digital BIST structure are replaced by a series of analog shift registers (ASR), which are basically Sample-and-Hold (S/H) circuits.

The ABIST structure has two modes of operation: normal operation mode and test mode. In normal operation mode, all switches are open and no test data are sampled. When the device enters test mode, all "sw" are closed and test data are loaded into the

Figure 2.2. An ABIST structure [Wey90].

corresponding S/H circuit. After all test data are loaded, they will be shifted out of the device serially. As shown in Fig. 2.2, sp3 will be closed first and test data held at S3 will be shifted out of the device. At the completion of this operation, sp2 will be closed (sp3 will remain closed) and test data held at S2 will be available at the output SO. The subsequent test data are processed in the same manner until they are all shifted out of the device. SI is an input where signal is applied to test the ABIST structure.

2.3 Fault Diagnosis based on Sensitivity Computation and Functional Testing [SK92]

This technique is similar to the Consistency Rule Checking technique discussed in Section 1.0. Instead of using a rule-based model, test measurements from a faulty device are used to solve a set of sensitivity equations to compute the deviation of the internal components. The components with the largest deviation from their nominal values are deemed as the culprits that cause the device to behave faultily.

The relative deviation of the output parameter ($\frac{\Delta T}{T}$) is defined as:

$$\frac{\Delta T}{T} = \frac{\sum_{i=1}^k S_{x_i}^T \frac{\Delta x_i}{x_i}}{1 + \sum_{i=1}^k S_{x_i}^D \frac{\Delta x_i}{x_i}} \quad (\text{EQ 2.1})$$

where

T is the nominal value of the output parameter and is defined as:

$$T(w, x) = \frac{N(w, x)}{D(w, x)} \quad (\text{EQ 2.2})$$

$$\Delta T = T(\text{measured}) - T(\text{nominal}) \quad (\text{EQ 2.3})$$

$s_{x_i}^T$ and $s_{x_i}^D$ are the differential sensitivity of output parameter T and denominator D respectively for the i^{th} component. These two parameters can be computed by using a circuit simulator (SPICE) and are defined as:

$$s_{x_i}^T = \frac{x_i}{T} \frac{\partial T}{\partial x_i} \quad (\text{EQ 2.4})$$

$$s_{x_i}^D = \frac{x_i}{D} \frac{\partial D}{\partial x_i} \quad (\text{EQ 2.5})$$

x_i is the i^{th} component of the circuit.

To locate the fault, EQ 2.1 has to be solved to determine which component, x , has the largest deviation. Assuming the equation has k unknowns, k independent equations are required. In order to meet this requirement, k different test points are needed to construct this set of equations and T is defined as a column matrix with k values. For a large circuit, the choice of test points is critical since new unknowns cannot be introduced to the new equations.

2.4 D.C. Fault Dictionary [AS90]

This technique is primary used for detecting open/short catastrophic faults. The technique is basically a two-stage process:

- a pre-test stage to compile the fault dictionary by simulating the DUT under

nominal and preselected catastrophic faulty conditions. The voltage at the test nodes is calculated and forms the dictionary.

- the post-test stage to compare the voltages measured at the test nodes with the nominal values stored at the fault dictionary. The circuit is assumed to be faulty if the two values at a node deviate by more than the allowed tolerance. To determine what type of fault is present in the DUT, the measured value is compared against the calculated faulty voltages of that node stored in the fault dictionary.

The advantage of this approach is that it uses only DC test signals at the inputs of the DUT and is, therefore, relatively inexpensive. Because the output signals are DC in nature, they can be detected by digital test equipment. The technique is very appealing for mixed-signal devices since only one type of test equipment is required to test both analog and digital circuits.

2.5 Digital Modelling [AS90]

Like the DC fault dictionary technique discussed in the previous section, digital modelling is primarily used for open/short catastrophic fault detection. All catastrophic faults are thought of as stuck-at faults as in a digital circuit. The technique requires that all analog circuit blocks are first reduced conceptually to a combination of digital blocks. DC inputs are then applied to each block, guaranteeing digital switching at the output. The results are then compared with those obtained from a model to determine if a fault is present.

2.6 Conclusion

Analog circuit testing is generally more difficult than digital circuit testing because of the complex nature of analog circuits. As chip densities continue to increase, the testability issues facing analog circuits have become even more severe. This chapter presents five analog circuit testing techniques which represent some of the latest attempts to address the testability issues of analog circuits. However, none of techniques proposed so far offers a complete solution to address these issues. The following outline some of the drawbacks commonly found in these techniques:

- They are restricted to detection of open/short catastrophic faults. This may help reduce production costs by sorting out all the faulty circuits early on in the production cycle, but does not provide the ability for fault diagnosis for devices that fail parametrically.
- They require expensive and precision hardware to implement the technique. For example, the ABIST structure discussed in Section 2 requires a S/H circuit for each internal node that needs to be accessed. Although the technique increases accessibility to internal nodes and simplifies fault diagnosis to certain extent, it is achieved at the expense of increased overall device complexity and would be extremely expensive to implement in a large circuit.
- They require massive computer simulation up front to predict all possible faults that may occur in the circuit to form a fault dictionary. While techniques using such an approach may be useful for detecting DC faults in a small circuit, they may not be feasible for a large circuit, particularly in terms of detecting soft faults.
- They rely on the use of models - circuit models, behavior models or rule-based

models - to predict the location and cause of the fault. Several techniques discussed in this chapter are based on this approach. However, the development of these models is very costly since they have to account for the faulty operation of the circuit. They may also require constant refinements when more fault conditions are discovered. Unless they can be reused in a constantly based way, like ASIC cell libraries, it may be difficult to justify their development cost.

CHAPTER 3

Analog Circuit Testing Using DSP Techniques

The previous chapter has shown various fault detection and diagnosis techniques for analog circuits that are currently being proposed. The basic requirement for analog circuit testing is to allow for direct testing of the device's sub-section, which will provide greater observability when the device is in its normal mode of operation, and to simplify fault diagnosis when the device does not function properly.

With the advances in Integrated Circuit (IC) process and the ability to place increasingly more circuits on silicon, the limited capability offered by techniques discussed in the previous chapter does not look very appealing, since a significant amount of testing effort still has to be devoted to determine whether the DUT meets the parametric specifications. Although simulation can be used for this purpose, the fault models required are very expensive to develop and maintain.

Unlike their digital counterparts, analog circuits have far more complicated input-to-output characteristics that may require special input stimulus to reveal their inherent characteristics at the circuit's outputs. To complicate matters even further, the limited access to internal critical nodes can also hamper the effectiveness of the testing process. In light of these issues, the demand for an efficient and feasible test strategy for complex analog devices has heightened to a new level.

3.1 Proposed Technique

The block diagram of the proposed technique is illustrated in Fig. 3.1. The fundamental idea behind the concept is to drive the DUT with an appropriate input stimulus that will reveal the DUT's inherent characteristics; data is sampled at the output with an on-chip A/D converter and the results are fed to an external Digital Signal Processing unit to extract the desired information from these sampled data. Blocks within the DUT can be tested individually or collectively by using switches to scope the test boundary.

Figure 3.1 Block diagram of the proposed testing technique.

The advantages of digitizing the output signals on-chip are:

- Output signal degradation over long transmission cables will no longer be an issue.

- An inexpensive tester can be utilized, since its primary function will be to provide input stimulus and receive digital signals from the DUT.
- No separate tester will be required for testing digital and analog circuits since a single digital tester can be used.

However, the feasibility of the proposed technique lies in the design of the A/D converter. In order to obtain accurate and precise measurements, the A/D must be of high-speed and resolution type. Conventional A/D converters that use successive approximation or flash techniques are too expensive to implement. Moreover, this type of converter is extremely sensitive to process parameters and post fabrication trimming is normally required to achieve the desired results [TTK⁺84].

In light of all these problems with conventional A/D converters, it is proposed that an Oversampling A/D converter be used for this work. The advantages of oversampling A/D over conventional A/D converters can be summarized as follows [CHE90]:

- They occupy a very small area as compared to conventional A/D converters.
- They are insensitive to component tolerances.
- Their resolution, as measured by comparing its signal-to-noise ratio, is quite high in comparison to conventional A/Ds.

The fundamental concern in using this technique is that since both the DUT and the Oversampling A/D will be built on same technology and the Oversampling A/D requires that the input be sampled at a rate significantly higher than the Nyquist rate, the technique may not be able to measure circuit performances at the upper boundary. However, the proposed technique is meant for testing circuits whose desired performance and performance variations are known before hand. Such prior knowledge of the device characteristics allows comparison of measured results with those from a device model, leading to a precise determination of device parameters. For example, a go/no-go decision can be made for the frequency response of the DUT by comparing

the measured results against the results obtained from the model of the DUT. Direct measurements are still possible for low performance DUT's.

In subsequent sections, the theory of Oversampling A/D converters will be introduced and the proposed concept will be demonstrated by using computer simulation to determine various AC/DC parameters for an Operational-Amplifier (Op-Amp). The purpose is to demonstrate the feasibility of the technique.

3.2 Theory of Oversampling A/D Converters

The Sampling Theorem dictates that a signal must be sampled at the Nyquist rate in order for it to be recovered perfectly. This requirement puts significant constraints, particularly for high speed applications, on the design of an anti-aliasing (AA) filter to band-limit the signal to half of the Nyquist rate. As well, conventional A/D converters, such as those that use successive approximation or flash technique, require a precise Sample/Hold circuit. Furthermore, these types of converters are highly sensitive to component tolerances and, for high precision applications, post fabrication trimming is normally required [MUI⁺87].

As their name implies, Oversampling A/D converters sample the input signal at a rate significantly higher than the required Nyquist rate. Oversampling A/D converters have attracted considerable attention in recent years particularly in the fields of high precision audio and telecommunications. Their relaxed requirement for AA filtering, the fact that no S/H circuit is required, and their insensitivity to IC fabrication process variations, make them particularly appealing for many types of applications.

The operating principle of an Oversampling A/D converter is very straightforward. Input signal is combined with a feedback signal from the output indicating the equivalent digital value of the previous sample; the combined data is then filtered by an integrator and quantized to generate a new sample. The quantizer of an Oversampling A/D

is often coarse, usually no more than a few bits wide. The coarse digital results are then low-passed and decimated to regenerate a sequence of high resolution digital data at Nyquist rate. To explain its underlying theory, an Oversampling A/D converter with one-bit quantizer, referred to as a sigma-delta ($\Sigma\Delta$) modulator, will be examined in detail.

3.2.1 First-Order Sigma-Delta ($\Sigma\Delta$) Modulators

The topology of a first-order $\Sigma\Delta$ modulator is shown in Fig. 3.2. Its basic building blocks include an integrator and a one-bit quantizer. The frequency of the quantizer determines the oversampling frequency. The most commonly used analytical model for $\Sigma\Delta$ modulators is the Additive Independent White Noise (AIWN) approach, which replace the one-quantizer by a noise source with a white spectrum.

where $i = \text{integer}$
 $T = \text{sampling period}$

Figure 3.2. Topology of a $\Sigma\Delta$ modulator.

The AIWN is based on the assumption that the quantization noise is signal independent and is white in nature [Hau91][AS83]. The input signal to the $\Sigma\Delta$ also has to be active and at a fairly high level in order for the approximation to hold [Gra90]. The AIWN model linearizes the non-linear elements, the quantizer, within the structure and allows a much simpler analysis. Fig. 3.3 shows the block diagram of the $\Sigma\Delta$ modulator in Z-domain with the quantizer replaced by a white noise source $Q(z)$.

Figure 3.3. Block diagram in Z-Transform.

The Z-domain expression for the $\Sigma\Delta$ modulator is

$$Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}Q(z) \quad (\text{EQ 3.1})$$

where

$$H(z) = \frac{z^{-1}}{1-z^{-1}} \quad (\text{EQ 3.2})$$

is a digital, delaying integrator transfer function.

Substituting, EQ. 3.2 into EQ. 3.1,

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})Q(z) \quad (\text{EQ 3.3})$$

The equation shows that the output at the $\Sigma\Delta$ modulator composes a delayed version of the input signal plus an added noise term. The noise term is commonly referred to as a noise-shaping transfer function. The frequency response for the noise-shaping term is shown in Fig. 3.4. The graph shows that the noise spectrum is shaped in such a way that its spectral density inside the base band is minimal. Hence, it is obvious that by filtering out the noise outside the baseband, the input signal waveform can be restored. Normally, Finite Impulse Response (FIR) is used to avoid multibit multiplications.

Figure 3.4. Frequency response of the noise shaping term for a first order $\Sigma\Delta$ modulator.

The resolution of a $\Sigma\Delta$ modulator is determined by its Signal-to-Noise Ratio (SNR) and by comparing it with the conventional A/D converter [Hau91]. The SNR of a first order $\Sigma\Delta$ is

$$SNR_{max} (dB) = 6.02(N + 1.5L) - 3.41 \quad (\text{EQ 3.4})$$

where

L = oversampling factor¹

From EQ 4, it is clear that the SNR or the resolution of a first order $\Sigma\Delta$ modulator can be enhanced by increasing the oversampling factor. The enhancement factor is expressed as

$$SNR(\text{enhancement}) = 9.03L - 5.17 \quad (\text{EQ 3.5})$$

3.3 Testing of Op-Amp using the Proposed Technique

The feasibility of the new technique will be demonstrated by using it to measure various circuit parameters of an Op-Amp. An Op-Amp is selected because it is the most basic building block in analog integrated circuits. Therefore, it can be safely assumed that the AC performance of the Op-Amp, such as bandwidth or slew rate, represent the upper limits that the overall circuit can achieve. DC performance, on the other hand, can be improved by using feedback or circuit compensations. However, this should pose no threat to the proposed testing techniques as the ability to measure DC parameters is largely dependent on the dynamic range and SNR of the Oversampling A/D converter. Since the circuit requirements are known beforehand, the Oversampling A/D converter can be designed to accommodate all input ranges. The circuit parameters that will be measured are unity-gain-bandwidth (GBW) and slew rate. These parameters are deemed essential for determining the performance of the overall circuit performance. DC parameters such as offset voltage will not be considered here. According to the theory of oversampling A/D converters, the time average of the sampled data should be equal to DC input value. However, the quantization noise for $\Sigma\Delta$ modulators is highly DC-bias dependent [CNL⁺90], and the effects of DC input to $\Sigma\Delta$ modulators will be analyzed in Chapter 4.

1. Oversampling factor is defined as the ratio between the initial sampling frequency and the baseband frequency..

3.3.1 Experimental Setup

Computer simulation has fast become the method of choice for analyzing and studying complex systems due to the availability of Computer-Aided-Design (CAD) tools and decreasing costs of computational resources. CAD is considered by far the most cost effective and efficient means of analyzing complex systems. Tasks that were previously done using traditional methods, such as prototyping or emulation, are now often replaced by computer simulation. Moreover, computer simulation has the advantage of allowing the complexity of the analysis to grow gradually without sacrificing its integrity, enabling designers to gain a more thorough understanding of the impact of each parameter on the overall system.

The simulations will be performed using MATLAB, which runs on a 486-PC. MATLAB is a mathematical tool designed to solve scientific and engineering numerical calculations. It incorporates many build-in mathematical functions and essential DSP features that will facilitate building up the simulation environment for this project. Users can create unique functions by using the interpretive language of MATLAB [MAT91]. The models for both the Op-Amp and Oversampling A/D converters will be captured in this manner.

The Oversampling A/D converter that will be used in the demonstration is an ideal second-order type with a one-bit quantizer at the output. The block diagram of this converter is shown in Fig. 3.5. Circuit nonidealities will not be dealt with in this initial idea presentation stage. However, the effects of quantization noise will be discussed later in the chapter. A second-order coder is used since it offers higher resolution than the first-order type. Higher order structures for Oversampling A/D could also be considered, but at the price of increasing complexity and susceptibility to oscillation [Can85].

Figure 3.5. Block diagram of second-order $\Sigma\Delta$ modulator.

To reconstruct the sampled waveform, the sampled data is passed through a low-pass FIR filter to eliminate the high frequency noise [PM88]. The cutoff frequency of the FIR filter should be above the GBW of the Op-Amp. For this particular demonstration, a seventy-five taps FIR filter with relative cutoff frequency of 0.06 is used. Fig. 3.6 shows the frequency response of the low-pass filter used for the demonstration. The Op-Amp used is assumed to have a single-pole roll-off. The slew rate and the GBW of the Op-Amp are programmable.

Figure 3.6. Coefficients (impulse response) and frequency response of the low-pass filter.

3.4 Slew Rate

Slew rate is a non-linear behavior of an Op-Amp. It occurs when the input stage of the Op-Amp is driven by a large differential signal which causes it to saturate and enter the non-linear operation region [GM84] [DOS81]. The cause can be illustrated by using a generalized Op-Amp model configured as a voltage follower as shown in Fig. 3.7. The model consists of two stages: a differential input stage and an output stage at which the dominant pole of the Op-Amp is assumed to be located.

Figure 3.7. Voltage follower using generalized Op-Amp model.

The input stage has a small-signal transconductance, gmI , and a large-signal maximum current of Ixm . The non-linear transfer characteristic of the input stage can be approximated by three linearized regions as shown in Fig.8.

Figure 3.8. Non-linear Transfer characteristics of the input stage.

As mentioned before, the dominant pole of the Op-Amp is normally located at the output stage and creates a single-pole roll-off well below the frequency of GBW. As seen in Fig. 3.7, the transfer characteristics of the output stage are approximated by the nor-

malized gain equation so that total open-loop gain is identical in the linear region:

$$A_o = -\frac{1}{g_{ml}} \frac{\omega_t}{s} \quad (\text{EQ 3.6})$$

When a large differential signal, a step, is applied to the Op-Amp, the feedback loop is not closed immediately. This, in turn, drives the input stage into saturation. The output current of the input stage is at its maximum, I_{xm} . The output voltage seen at the output is approximated by a straight line:

$$V_o(t) = \frac{\omega_t I_{xm}}{g_{ml}} t = S t \quad \text{where} \quad S = \frac{\omega_t I_{xm}}{g_{ml}} \quad (\text{EQ 3.7})$$

However, at time t_x , the voltage fed back from the output forces the differential voltage back to the boundary of the linear region, and the output current of the input stage falls below I_{xm} . From that point on, the Op-Amp enters its linear operation region and settles into its steady value.

$$t_x = \frac{V_s}{S} - \frac{I_{xm}}{g_{ml} S} = \frac{V_s}{S} - \tau_t \quad \text{where} \quad \tau_t = \frac{I_{xm}}{g_{ml} S} \quad (\text{EQ 3.8})$$

and the output voltage is approximated by:

$$V_o(t) = V_s - S \tau_t e^{-\frac{(t-t_x)}{\tau_t}} \quad (\text{EQ 3.9})$$

Fig. 3.9 shows the effect of slew rate on the output of a voltage follower.

Figure 3.9. Effect of slew rate on the output of a voltage follower.

3.4.1 Slew Rate measurement

The test circuit configuration for measuring the slew rate of an Op-Amp is shown in Fig. 3.10. The DUT is configured as a voltage follower. A voltage step of 1V is applied to the input; output of the DUT is sampled by a second-order $\Sigma\Delta$ modulator and the 1-bit digital output will be fed to the DSP unit. The clock rate for the $\Sigma\Delta$ modulator is set at 10.24MHz and a total of 2,048 samples will be collected at the DUT's output. The DUT is assumed to have a GBW of 0.5MHz and a slew rate range from 0.3 to 2.0V/us.

Fig. 3.11 (a) and (b) show the original output waveform from the DUT and the recovered waveform based on the proposed technique for slew rates of 0.3 and 2.0 V/us respectively. Please note that the delay on the recovered waveforms caused by the digital FIR filter is ignored in order to facilitate a comparison between the recovered

waveform and the original waveform. At low slew rate, the recovered waveform form is almost identical to the original waveform, whereas at high slew rate the recovered waveform is totally uncorrelated to the original waveform. The reason for the discrepancy is that the input to the $\Sigma\Delta$ modulator is rising at a rate much higher than the rate that it is able to track. The remedy to this problem is to increase the sampling frequency.

Figure 3.10. Test circuit configuration.

The algorithm used to find the slew rate is quite straightforward: it merely searches for the break point at which the exponential part of the waveform begins. The algorithm has also made provision to account for extreme cases when the slew rate is extremely high and the output is totally dominated by an exponential.

Figure 3.11. The effect of sampling rate on the recovered waveform for slew rate (a) 0.3V/us and (b) 2.0V/us.

3.4.2 Unity Gain Bandwidth (GBW)

The same test circuit configuration for measuring slew rate can be used for measuring GBW. The GBW can be determined by performing a Fast Fourier Transform (FFT) on the sampled data; the 3-dB point of the power spectrum is the GBW of the DUT. However, with slew rate, the resulting power spectrum is distorted by this non-linear effect. Fig. 3.12 shows the power spectrum for an output with slew rate against one with a pure exponential.

Figure 3.12. Effect of slew rate on the power spectrum.

The problem can be circumvented by determining the point at which the exponential begins by using the algorithm presented in the last section and simply performing the FFT on the remaining portion of the waveform. Fig. 3.13 shows some of the results obtained using this technique. Since this technique represents a shifting of the waveform in time, it does not change the time constant of the original exponential. Provision has also been made on the algorithm to account for extreme cases when the output is totally dominated by the slew rate. However, it has been found that when the break point occurs after 80% of the output and not enough points are sampled, the technique will fail.

Figure 3.13. Improved power spectrum using proposed technique.

Although the power spectrum of the Op-Amp resembles more of an ideal one using the proposed technique, many spikes occur in the vicinity of the 3-dB point. These spikes are caused by high frequency noise aliasing back to the baseband of the Op-Amp. By increasing the sampling rate of the $\Sigma\Delta$ modulator, which in effect increases the Nyquist region, the results are significantly improved. Fig. 3.14 (a) and (b) shows the improvement in the determination of the GBW of the DUT by increasing the sampling to 20.48MHz and 40.96MHz respectively.

Figure 3.14. Power spectrums for sampling rate (a) 20.48MHz and (b) 40.96MHz.

3.5 Conclusion

This chapter proposes the idea of using an on-chip A/D converter for analog circuit testing purposes. The principles of the oversampling A/D converter were discussed. A second-order oversampling A/D converter was used to measure the slew rate and GBW of an Op-Amp to demonstrate the feasibility of the proposal. Simulation results and problems confronting the techniques were discussed at the end of the chapter.

CHAPTER 4

Architecture Alternatives and Characteristics for Sigma-Delta Modulators

In the previous chapter, the concept of using a Sigma-Delta Modulator for analog circuit testing has been demonstrated by using a Double-Integration Sigma-Delta (DISD) Modulator. The accuracy of the measurements, as previously discussed, can be enhanced by using higher order coders, primarily due to their improved Signal-to-Noise Ratio (SNR). However, the drawbacks of using higher order (greater than two) $\Sigma\Delta$ modulators are their stability problem and added complexity [Can85].

The main objective of this chapter is to provide a unified comparison of different architectures of Oversampling A/D converters with the aim of selecting one which exhibits the following characteristics for further analysis:

- High resolution to ensure that it can be used for precision measurement.
- High SNR at low sampling rates to ensure that the selected system can be adopted by various fabrication processes.
- Low idle channel noise within its baseband to ensure that DC bias will not affect performance.

Basically, all $\Sigma\Delta$ modulators have two types of architectures: serial or multi-stage. Both types can be used to realize high order $\Sigma\Delta$ modulators. Serial architecture has high tolerance to circuit nonidealities but does not lend itself easily to higher order implementations because of the AC stability problem [Can85]. Multi-stage architecture, on the other hand, has been specifically developed recently to counteract the stability problem. However, this type of architecture does not match the high tolerance to circuit nonidealities of its serial counterpart because of its reliance on cancellation of quantization noise generated from each stage [LON88][Hau91].

This chapter will concentrate on the analysis of four $\Sigma\Delta$ modulators with emphasis on their performance with DC input since $\Sigma\Delta$ modulators are generally not used for such applications. The $\Sigma\Delta$ modulators to be evaluated are limited to second and third order. It is deemed impractical at this time to use any modulators higher than third order due to their complexities. Each modulator will be evaluated based on its output vs. input characteristics, SNR, idle channel noise and DC error. The performance of the four $\Sigma\Delta$ modulators with DC inputs is particularly important since the majority of analog testing involves the measurement of DC signals, such as offset voltage, output voltage swings, etc.

For serial architecture, the Double-Integration (DISD) and Triple-Integration (TISD) $\Sigma\Delta$ Modulators will be discussed. For multi-stage architecture, the Two-Stage Third-Order (T2S3) and the Three-Stage Third-Order (T3S3) $\Sigma\Delta$ Modulators will be discussed. These four $\Sigma\Delta$ modulators have been studied and implemented on silicon for other applications and the effects of circuit non-idealities on their performance have also been documented [LON88] [RIL89]. The selection of these four $\Sigma\Delta$ modulators will enhance the analysis of using oversampling A/D for measurement applications.

Figure 4.1. The simulation environment for the characterization of the $\Sigma\Delta$ modulators.

4.1 Characterization Technique

The common technique for analyzing $\Sigma\Delta$ modulators is to perform time domain analysis on the overall system using computer simulation. This can be done by first capturing the z-domain analytical model of the $\Sigma\Delta$ modulators using a high-level programming language, such as C, and then performing discrete time analysis on the model within a simulator. The simulation results can then be analyzed using other techniques such as FFT to predict the performance of the system. This approach eliminates the need to perform complicated mathematical analysis which may or may not be soluble [CHE90].

Moreover, it is well known that the performance of $\Sigma\Delta$ modulators is dependent on certain circuit defects and component specifications. Time domain simulation allows

these types of nonidealities to be factored into the analysis, and the effects of these nonidealities on the overall system performance can be easily determined. Another advantage of using time domain simulation is that it can be done independent of the sampling rate and allows the performance of the modulators to be analyzed based on the oversampling factor. Fig. 4.1. shows the simulation environment and the steps taken to perform the characterization.

The characterization of the four $\Sigma\Delta$ modulators follows very much the descriptions above. The simulator used is again MATLAB. All models for the four $\Sigma\Delta$ modulators are captured in C. The programs use special routines supplied by MATLAB to facilitate the transfers of data between the simulator and the C programs. Using external C programs instead of MATLAB interpretive language for the models reduces the simulation time by at least two orders of magnitude.

All analysis is based on 65,536 time steps simulation. This ensures that all measurements are accurate to 16-bit of resolution. Although more points can be used to enhance the accuracy of the measurements, unfortunately, the computation time is proportional to $N \cdot \log(N)$ [Lon88] and 65,536 points are selected as compromise. The SNR and idle channel noise are determined by transforming the digital output from time domain to frequency domain using Fast Fourier Transform (FFT). Because of the non-periodic nature of $\Sigma\Delta$ modulator output and the finite number of samples used for FFT, spectral leakage occurs and causes the spectrum to smear out. The problems are due to the lack of continuity at the end point of the observation window and the fact that FFT assumes the observation window is periodic in nature [HAR78]. To overcome this problem, a four-term Blackman-Harris window [see Appendix A] is used to compensate for this error. The window removes the non-symmetry at the boundaries by smoothly bringing the data to zero.

The oversampling factors used for the second-order and third-order $\Sigma\Delta$ modulators are 192 and 64 respectively. The oversampling factors are chosen to ensure that both

Figure 4.2. z-domain block diagram for (a) Double-Integration $\Sigma\Delta$ modulator (b) Triple-Integration $\Sigma\Delta$ modulator.

Figure 4.3. z-domain block diagram for Three-Stage Third-Order $\Sigma\Delta$ modulator.

Figure 4.4. z-domain block diagram for Two-Stage Third-Order $\Sigma\Delta$ modulator.

second-order and third-order $\Sigma\Delta$ modulators exhibit the same peak SNR to facilitate the comparison. The signal used for SNR measurements is a sine with frequency set at 0.0012•fs for second-order and 0.004•fs for third-order $\Sigma\Delta$ modulators. This is to ensure that second to fourth harmonic terms will be inband.

4.2 Double-Integration $\Sigma\Delta$ (DISD) Modulators

Fig. 4.2a shows the z-domain block diagram of a double-integration $\Sigma\Delta$ modulator. Basically, the system consists of two first-order $\Sigma\Delta$ modulators cascaded in series. Two non-delaying integrators are also used in the system. The output at the second integrator is digitized by a two-level quantizer to form the digital output of the $\Sigma\Delta$ modulator and this digital output is fed back to the inputs of the integrators via two feedback loops. The gain coefficients for the structure are listed in Table 4.1.

Coeff.	a1	a2	b1	b2
Value	0.5	1.0	0.5	1.0

TABLE 4.1. Coefficients for Double-Integration $\Sigma\Delta$ modulator

By using the AIWN approach and replacing the quantizer by a noise source with white spectrum, the output signal can be expressed as follows:

$$V_o(z) = \left(\frac{0.5}{(1 - 0.5z^{-1})} \right) X(z) + \frac{(1 - z^{-1})^2}{(1 - 0.5z^{-1})} Q(z) \quad (\text{EQ 4.1})$$

EQ. 4.1 shows that the quantization noise, $Q(z)$, is being filtered by a second-order high-pass function. This will have the effect of reducing the inband quantization noise and consequently improving the SNR of the $\Sigma\Delta$ modulator. However, this is achieved

Figure 4.5. SNR plot for a Double-Integration Sigma-Delta modulator.

at the expense of noise gain at high frequency.

The SNR plot for the DISD is shown in Fig. 4.5. The SNR is calculated based on an oversampling factor of 192 for a sine input with frequency of $0.0012 \cdot f_s$. The structure shows a peak SNR of 84dB which represents 14 bits resolution. The straight line represents the ideal SNR of the DISD, which is expressed as follows [LON88]:

$$SNR = 50 \cdot \text{Log} \left(\frac{f_s}{f_o} \right) + 20 \cdot \text{Log} \left(\frac{V_p}{\Delta} \right) - 20.17 \text{ (db)} \quad (\text{EQ 4.2})$$

where

$\left(\frac{f_s}{f_o} \right)$ is the oversampling factor.

V_p is the peak input level.

Δ is the distance between quantization levels.

The plot shows that the SNR peaks as the input approaches -6dB. Beyond that point,

Figure 4.6. Output Vs. DC input plot for DISD.

Figure 4.7. Idle channel noise against DC input for DISD.

Figure 4.8. DC error plot for DISD.

Figure 4.9. Inband quantization noise for Input=0.255.

the SNR of the structure begins to roll off. The drop in SNR is due to the saturation of the $\Sigma\Delta$ modulator [CHE90]. When the quantizer is saturated, it loses its noise tracking capability at high frequency and causes quantization noise to spread out the entire spectrum, including the baseband. The rise of quantization noise in the baseband is the main culprit for the decline in SNR. It corrupts the in-band signals and causes them to be indistinguishable from the quantization noise.

The output vs. input plot of the DISD is shown in Fig. 4.6. The output is determined by averaging the 65,536 points from the DISD output for each DC input level. The plot demonstrates that the structure has a good linear tracking capability for DC signals.

Fig. 4.7 shows the idle channel noise of the DISD. The idle channel noise is a measure of the RMS value of the quantization noise at the baseband against the DC input signal. The figure shows that the noise is gathered into a series of peaks [CB81]. The peaks indicate that, at certain DC input levels, low frequency quantization noise is generated and corrupts the baseband. These peaks can affect the accuracy of the measurements when the signal being measured is biased to that level. As well, the idle channel noise gradually increases as the input level increases, indicating the quantizer is beginning to saturate.

The DC error plot in Fig. 4.8 shows its high correlation with the idle channel noise plot. The peaks at the DC error plot coincide with those at the idle channel noise plot. If the quantization noise is white, the averaging of the output will cause the noise value to go to zero. The peaks indicate that the quantization noise is highly correlated. Fig. 4.9 shows the frequency components of the components in the baseband of the DISD when input is 0.255.

Figure 4.10. SNR plot for Triple-Integration $\Sigma\Delta$ modulator.

4.2.1 Triple-Integration $\Sigma\Delta$ (TISD) Modulator

Fig. 4.3 shows the z-domain block diagram for a TISD. Similar to a DISD, the structure basically consists of three first order $\Sigma\Delta$ modulators cascaded in series. The digital output of the modulator is obtained by quantizing the output of the third integrator by using a two-level quantizer. The coefficients used for the structure are listed in Table 4.2.

Coeff.	a1	a2	a3	b1	b2	b3
Value	0.10	0.40	0.80	0.625	0.60	1.75

TABLE 4.2. Coefficients for Triple-Integration $\Sigma\Delta$ modulator

Figure 4.11. Output vs. Input plot for Triple-Integration $\Sigma\Delta$ modulator.

This set of coefficients has been optimized by using repetitive search type simulations in the time domain [RIL89] to ensure the stability of the structure. To prevent overloading from occurring at the output of the integrators, each of them is preceded by a gain stage of less than one. The input signal is reduced to one-tenth of its original value before it is fed to the modulator, which significantly reduces the dynamic range of the modulator. The z-domain expression of the output is as follows:

$$V_o(z) = \frac{0.032z^{-3}}{H(z)}X(z) + \frac{(1-z^{-1})^3}{H(z)}Q(z) \quad (\text{EQ 4.3})$$

where

$$H(z) = 1 - 1.25z^{-1} - 0.02z^{-2} + 0.47z^{-3} \quad (\text{EQ 4.4})$$

Figure 4.12. Idle channel noise plot for Triple-Integration $\Sigma\Delta$ modulator.

Figure 4.13. DC Error plot for Triple-Integration $\Sigma\Delta$ modulator.

EQ 4.3 shows that the quantization noise is filtered by a third-order high pass function. This third order function provides a better reduction of quantization noise in the base-band than the DISD and theoretically should improve the SNR of the structure. However, because of the attenuation of the input signal, the overall SNR of the structure is below the ideal SNR expected for a third order $\Sigma\Delta$ modulator as shown in Fig. 4.10. The ideal SNR expression for a third-order $\Sigma\Delta$ modulator is as follows:

$$SNR = 70 \cdot \text{Log} \left(\frac{f_s}{f_o} \right) + 20 \cdot \text{Log} \left(\frac{V_p}{\Delta} \right) + 34.67 \text{ (db)} \quad (\text{EQ 4.5})$$

The output vs. input plot for the structure is shown in Fig. 4.11. The gain of the modulator can be determined by finding the slope of the curve, which is approximately equal to the expected value of 0.16 as expressed by the first term of EQ 4.3. The idle channel noise plot of Fig. 4.12 shows there are several extremely high peaks: the first occurs when input is 0.792.

The peaks are caused by the use of ideal integrators which allow the output to swing to an unrealistic level. At those input points where the peaks occur, the output of the third integrator starts overloading and the modulator begins to lose its tracking capability. This problem is removed when clipping is used to limit the swings at the output of the integrators. The DC error curve is shown in Fig. 4.12. Even though the TISD is a third order modular, it does not show a marked improvement on its capability on DC signal measurement over the DISD.

4.2.2 Two-Stage Third-Order $\Sigma\Delta$ (T2S3) Modulator

The Two-Stage Third-Order $\Sigma\Delta$ modulator belongs to a new class of multi-stage oversampled A/D [LON88]. This type of architecture allows high order modulators to

Figure 4.14. SNR calculation for Two-Stage Third-Order $\Sigma\Delta$ modulator.

be built without encountering the instability problems that occur in conventional serial type $\Sigma\Delta$ modulators. The basic concept of this approach is to place several low order, first to second order, $\Sigma\Delta$ modulators in parallel to obtain the desired transfer characteristics present in high order serial $\Sigma\Delta$ modulators.

The T2S3 depicted in Fig. 4.4 consists of a second-order modulator and a first-order modulator cascaded in parallel. The error term of the second-order modulator, which is the quantization noise, is fed to the input of the first-order modulator. The output of the first order modulator is essentially the digital estimate of the input error signal plus the associated quantization noise. This output is then spectrally shaped to match the noise-shaping function of the previous stage, so that at the last summing point, it will cancel out the quantization noise generated from the previous stage. The final modulator output is a multi-bit value that consists of the input signal and the quantization noise from the second stage shaped by a third order high-pass function. Because of the added

Figure 4.15. Idle channel noise plot for Two-Stage Third-Order $\Sigma\Delta$ modulator.

Figure 4.16. DC error plot for Two-Stage Third-Order $\Sigma\Delta$ modulator.

delay for the error signal to traverse the first order modulator, delay is added at the output of the second order modulator to ensure that the overall delay between the two stages match.

One of the disadvantages of using a multi-stage $\Sigma\Delta$ modulator is that any decimation filters used with this type of modulator are required to handle multi-bit inputs [HAU91], which will increase the complexity of the design. Another drawback associated with multi-stage $\Sigma\Delta$ modulators is their sensitivity to circuit nonidealities. This is due to the stringent requirement for the transfer function from both stages to match in order for the quantization noise to cancel out.

The mathematical expression for this multi-stage $\Sigma\Delta$ modulator is as follows:

$$V_o = z^{-1} \cdot X(z) + (1 - z^{-1})^3 \cdot Q(z) \quad (\text{EQ 4.6})$$

This expression is obtained by assuming that $H_1 = \frac{1}{(a_1 \cdot a_2)}$ and $F_1 = 1$, which causes the second-order effects from two separate stages to cancel out. The coefficients used for the modulator are listed in Table 4.3 [LON88].

Coeff.	a1	a2	a3	H1	F1
Value	1.0	0.25	0.25	4.0	1.0

TABLE 4.3. Coefficients for Two-Stage Third-Order $\Sigma\Delta$ modulator.

The calculation of the SNR for T2S3 is shown in Fig. 4.14. The simulation is based on an oversampling factor of 64 and a sine input with a frequency of 0.0012•fs. The figures show that when input approaches -10dB, saturation begins to set in and causes the SNR to drop. As indicated by EQ 4.6, the overall gain for the input signal is one. Therefore, the output vs. input characteristic for this modulator is identical to that for DISD, shown in Fig. 4.11. The idle channel noise calculation and the DC error for the

Figure 4.17. SNR plot for Three-Stage Third-Order $\Sigma\Delta$ modulator.

modulator are shown in Fig. 4.15 and Fig. 4.16 respectively. These figures show that the T2S3 has better idle channel noise and DC error performance than the two serial modulators discussed in previous sections. This indicates that quantization noise in a third order $\Sigma\Delta$ modulator is less signal dependent [CML⁺90].

4.2.3 Three-Stage Third-Order $\Sigma\Delta$ (T3S3) Modulator

Fig. 4.4 is the z-domain block diagram for a T3S3 modulator. This oversampled A/D converter is formed by cascading three first-order modulators in parallel. The principle of the operation is similar to that of the T2S3. The quantization noise of the first stage is then input to the second stage, whose quantization noise is the input to the third stage. The outputs of the second and third stages are then spectrally compensated to

Figure 4.18. Idle channel noise for Three-Stage Third-Order $\Sigma\Delta$ modulator.

Figure 4.19. DC error for Three-Stage Third-Order $\Sigma\Delta$ modulator.

match the noise transfer function of the previous stages so that they will cancel out the quantization noise of the previous stages at the summing node. The final output of the modulator is again a multi-bit value consisting of a delayed input signal plus the quantization noise shaped by a third order high-pass function.

Assuming that $H_1 = \frac{1}{a_1}$, $F_1 = 1$, $H_2 = \frac{1}{a_2}$ and $F_2 = 1$, the mathematical expression for the output of T3S3 is as follows

$$V_o = z^{-2} \cdot X(z) + (1 - z^{-1})^3 \cdot Q_3(z) \quad (\text{EQ 4.7})$$

As in the case of T2S3, these assumptions are made to ensure that the quantization noise from the first two stages will be cancelled out. The coefficients for the structure are listed in Table 4.4 [LON88].

Coeff.	a1	a2	a3	H1	H2	F1	F2
Value	0.25	0.25	0.25	4.0	4.0	1.0	1.0

TABLE 4.4. Coefficients for Three-Stage Third-Order $\Sigma\Delta$ modulator

Fig. 4.17 shows the SNR calculation for a T3S3 structure. Unlike the two-stage structure, this one does not suffer from overloading when the amplitude of the input increases. This is primarily due to the fact that the input signal is only subject to a single integrator gain. The idle channel noise and DC error calculations are shown in Fig. 4.18 and Fig. 4.19 respectively. The results are comparable to those obtained for the other third order modulators discussed in previous sections.

4.3 Effect of Circuit Nonidealities

The analysis of circuit nonidealities on the performance of $\Sigma\Delta$ modulators is dependent on the circuit configuration of the structure and the characteristics of the compo-

Figure 4.20. SNR for T2S3 when $a_2 = 0.225$.

Figure 4.21. DC Error for T2S3 when $a_2 = 0.225$.

nents used to realize the system. Often, after the system is realized, timing-domain simulation using a circuit simulator such as SPICE is used to analyze the effects of these circuit imperfections on the performance of the structures [Ril89].

For $\Sigma\Delta$ modulators, switch-capacitor technique is often used for the realization of the systems [MB86][DPO⁺92]. Constraints that need to be considered for switch-capacitor circuits include limited Op-Amp gain, Op-Amp settling time and swing and capacitor mismatches. However, since the discussion of the implementation of the various $\Sigma\Delta$ modulators is beyond the scope of this project, a detailed analysis of system degradation caused by these circuit imperfections will not be provided. This section, instead, discusses how deviations of the system coefficients caused by circuit imperfection, such as capacitor mismatches, will impact on the overall system performance.

Fig. 4.20 and Fig. 4.21 show how the SNR and DC errors of T2S3 are affected when the coefficient a_2 is decreased by ten percent (10%). The SNR is deviated from the ideal SNR by almost 5dB and the DC error is increased by about 5dB. The decrease in a_2 may be due to capacitor mismatches. The drop in SNR and the increase in DC error is due to the increase of in-band quantization noise. Since multi-stage $\Sigma\Delta$ modulators require the exact cancellation of quantization noise from each individual stage to achieve high resolution, a deviation of coefficient values from the expected would have significant effect on the overall performance of the system.

4.4 Conclusions

An analysis of four different $\Sigma\Delta$ modulators is presented in this chapter. The results of the analysis are tabulated in Table 4.5. Simulation results show that the DISD has better idle channel noise and DC error performance than the other three high order $\Sigma\Delta$ modulators, but that this is achieved at a high oversampling factor. The required high sampling rate may prohibit its use as a measuring device for high performance DUT's.

Because of the AC stability problem, the gain stages for the TISD are heavily attenuated to prevent saturation of the structure. The result is that the overall SNR is well below the ideal value and the dynamic range of the modulator is significantly reduced. Therefore this modulator is not particularly suitable for precision measurement applications.

With the exception of the saturation point, which set in earlier in T2S3 than T3S3, both multi-stage $\Sigma\Delta$ modulators have similar performance. Their SNR's hover around the ideal value and their DC errors are below -70dB. However, as indicated previously, multi-stage $\Sigma\Delta$ modulators are extremely sensitive to integrator nonidealities, such as capacitor mismatch, finite amplifier gain and linear settling errors. An analysis of the sensitivities of the two multi-stage $\Sigma\Delta$ modulators to these circuit nonidealities is presented in [LON88]. Of the two multi-stage modulators, it has been demonstrated that T2S3 is much less sensitive to these impairments.

	DISD	TISD	T2S3	T3S3
SNR _{max} (dB)	86.2	76.47	79.16	91.88
DR ₆₅ (dB)	29.5	10.0	21.00	20.98
ICN _{avg1} (dB)	-45.05	-41.47	-35.75	-36.21
ICN _{avg2} (dB)	-48.54	N/A	-39.77	N/A
ICN _{max} (dB)	-34.65	19.8	-27.96	-25.13
DCA _{avg1} (dB)	-93.77	-92.73	-85.72	-84.45
DCA _{avg2} (dB)	-97.33	N/A	-88.49	N/A
DCA _{max} (dB)	-82.73	-64.93	-76.12	-73.28

TABLE 4.5. Summary of analysis results

where

- SNR_{max} is the peak signal-to-noise ratio before saturation occurs.
- DR_{65} is the range of relative input signal levels that produce an SNR greater than 65dB.
- ICN_{avg1} is the average idle channel noise for the whole input range.
- ICN_{avg2} is the average idle channel noise before saturation occurs.
- ICN_{max} is the peak idle channel noise before saturation occurs.
- DCA_{avg1} is the average DC Error for the entire input range.
- DCA_{avg2} is the average DC Error before saturation occurs.
- DCA_{max} is the maximum DC Error before saturation occurs.

CHAPTER 5

Verification of the Proposed Technique Using Simulation

The measuring capability of the $\Sigma\Delta$ modulator is dictated by the order of the modulator and the oversampling factor used. The relationship between these two was discussed in the previous chapter. Basically, a low-order $\Sigma\Delta$ modulator must use a high oversampling factor to achieve the same SNR as a high-order modulator. However, stability becomes an issue when high order modulators are used. They are more complex and, thus, more prone to process imperfection. Therefore, the choice of the modulator is largely a compromise between the available technology and the required performance of $\Sigma\Delta$ modulator.

This chapter concentrates on analyzing the use of $\Sigma\Delta$ modulator to perform AC parameter measurements, particularly on the slew rate and bandwidth of an Op-Amp. The $\Sigma\Delta$ modulator used will be the Two-Stage Third-Order (T2S3) $\Sigma\Delta$ modulator discussed previously. The chapter begins with the analysis of the maximum slew rate and bandwidth that the $\Sigma\Delta$ modulator is able to measure. This is followed by an analysis of the factors that limit the measuring capability of $\Sigma\Delta$ modulators. Finally, three different quantization techniques to improve the measuring capability of the $\Sigma\Delta$ modulator are analyzed and the results presented.

5.1 $\Sigma\Delta$ Modulator Measuring Capability

This section will discuss the capability of a T2S3 $\Sigma\Delta$ modulator to measure the GBW and slew rate of an Op-Amp. The Op-Amp is configured as a unity-gain buffer to facilitate measurement. This test circuit configuration is chosen for its simplicity and because it does not require additional circuit components. The modulator will be used to sample data at the output of the DUT. The test signal used to stimulate the DUT is a step with a normalized amplitude of -6dB. The step input is chosen because it allows both slew and GBW to be obtained with a single test. The slew rate and the GBW of the Op-Amp will be determined by analyzing the sampled data of the $\Sigma\Delta$ modulator at the output of the DUT. The effectiveness of using a $\Sigma\Delta$ modulator to measure the GBW and slew rate of an Op-Amp is studied by means of computer simulation.

5.1.1 Demodulation Process

To determine the slew rate of the DUT, the output waveform must first be recovered from the digital bit stream of the $\Sigma\Delta$ modulator. The demodulation, or recovering, process is illustrated in Fig. 5.1. The process starts by first integrating the bit stream output from the $\Sigma\Delta$ modulator. The results are then differentiated and subsequently filtered by a sharp cut-off low-pass filter to eliminate the effect of quantization noise. Since the integrator and differentiator blocks are complementary to each other, the process can be simplified by eliminating the two blocks. The resulting demodulation process thus contains only a sharp cut-off low-pass filter.

The requirements of the digital filter to recover the output waveform for slew rate measurements are as follows:

- It must have a sharp cut-off to limit the quantization noise being aliased back to the baseband.

Figure 5.1. Demodulation process of $\Sigma\Delta$ modulator.

- The passband of the filter must be wide enough for the maximum allowable GBW to pass through.
- The magnitude of the passband must be flat to avoid distorting the output waveform.

The theory and concept of digital filter design is covered in many texts and will not be repeated here [PM88]. A 137-pole low-pass FIR filter using a Hamming window is selected for use to recover the output waveform in this analysis [PM88]. The cutoff frequency of the filter is set at six percent of the sampling frequency ($0.06 * f_s$). This cutoff frequency determines the maximum allowable GBW that can be measured. If the cut-off frequency is set too low, the recovered waveform will be distorted and thus render the measurement inaccurate. The magnitude plots for the transfer functions of the low-pass filter and the quantization noise of the $\Sigma\Delta$ modulator are depicted in Fig. 5.2. The figure shows a small region of overlap between the two transfer functions

indicating the recovered waveform will have a certain amount of quantization noise superimposed on it.

5.1.2 Slew Rate Measurement

Fig. 5.3 shows an example of an output waveform from a DUT recovered from the digital bit-stream using the low-pass filter discussed above. The DUT has a GBW of 0.1MHz and a slew rate of 0.2V/us. The delay between the input and output waveform is caused by the low-pass filter. The recovered waveform clearly resembles that of the input waveform to the $\Sigma\Delta$ modulator. However, the figure also indicates the effect of the quantization noise on the recovered waveform, making the determination of the slew rate extremely difficult. As mentioned before, the effect of quantization noise can be minimized by reducing the cut-off frequency of the low-pass filter. Fig. 5.4 shows the recovered waveform of the same DUT using a low-pass filter with a cutoff frequency set at four percent of the sampling rate ($0.04 * f_s$) and the result is a much cleaner waveform. But this is achieved at the expense of lowering the maximum allowable GBW that can be measured. Fig. 5.5 shows the effect of using a low-pass filter with an extremely low cut-off frequency for demodulation. The restored output waveform is heavily distorted.

The measurement of slew rate is further complicated by the fact that not all outputs from the DUTs are dominated by slew rate. As discussed in Chapter 3, output from a DUT may first rise at the slew rate and then settle with an exponential before it reaches the steady-state. The point at which it switches over is a function of the slew rate and the GBW of the Op-Amp. Thus, any algorithms used for slew rate measurement have to first determine where this break point occurs and account only for the slope up to the break point.

However, problems occurs for DUTs with a high or moderately high slew rate whose

break points occur at the very early stage of the step response. Because of the effect of quantization noise and the fact that the recovered waveform is slightly distorted when it first comes out of the low-pass filter, large errors may result in the slew rate measurements if the slope is taken in that region. In these circumstances, the measurements are deemed inaccurate and must be discarded. A worst case estimate of the slew rate can be derived once the GBW of the DUT is determined and with the assumption that the break point occurs at the point where the distortion stops.

The other factor that determines the accuracy of the measurements is the number of points that the $\Sigma\Delta$ modulator is able to sample during slewing. For DUTs with a high GBW and slew rate, the number of samples that the modulator can sample is limited and, because of the drawbacks discussed above, the accuracy of the measurements will suffer severely. By using EQ 3.8 in Chapter 3 and the fact that:

$$t_x > \frac{N}{f_s} \quad (\text{EQ 5.1})$$

where N is the number of samples that must be taken.

f_s is the sampling rate.

t_x is the time at which slewing stops and exponential begins.

the maximum slew rate that can be determined is expressed as:

$$\text{Slew}_{(max)} \leq \frac{f_s \cdot \omega_t}{N \cdot \omega_t + f_s} \quad (\text{EQ 5.2})$$

where ω_t is the GBW of the DUT in rad/s

Table 5.1 shows how the accuracy of the measurements is affected by the number of samples taken. The results, which are the measurements of the slew rate for a DUT with GBW of 0.1MHz, indicate that at least 15 samples are required in order to obtain

Figure 5.2. Magnitude plot for filter ($f_{\text{cutoff}} = 0.06 \cdot f_s$) and quantization noise transfer functions.

accurate measurements. This constraint limits the maximum slew rate that can be measured for each GBW. The measurements are re-taken by assuming random jitter (max-

N of points on rising edge	Max. Slew Rate (V/us) (expected slew rate)	Measured Slew Rate (V/us)	% of Error	Avg. ten Measured Slew Rate (V/us)	% of Error
10	0.3984	0.7306	87.6	0.5935	48.9
15	0.3272	0.2703	-17.4	0.2714	-17.1
20	0.2821	0.2939	4.2	0.2764	-2.0
25	0.2480	0.2310	-6.8	0.2194	-11.54
30	0.2212	0.2111	-4.6	0.2057	-6.9

TABLE 5.1. Table showing how the number of samples can affect the accuracy of slew rate measurements for a DUT with $f_t = 0.1$ MHz.

Figure 5.3. Recovered output waveform ($f_{\text{cutoff}} = 0.06 \cdot f_s$).

imum of five percent of the sampling period) occurs on the sampling clocks. The measured results (for an average of ten samples) and the calculated percentage of error are shown in the last two columns of Table 5.1. For small values of N , the errors reduce due to the average of ten measured results. However, for large values of N , the errors increase because of the noise introduced by the jitter on the output waveform. The added noise obscures the detection of the breaking point and causes errors in the measurements of the slew rate.

Fig. 5.6 is a 3-D surface plot showing the measured slew rate for DUTs with various characteristics. The X-axis represents the specified slew rate of the Op-Amp and the Y-axis represents the specified GBW of the Op-Amp, and the measured slew rate is represented by the vertical axis. The sampling rate used by the T2S3 $\Sigma\Delta$ modulator is 10.24MHz. Fig. 5.7 is the contour plot for the surface plot of Fig. 5.6. The contour plot provides information on how accurately the $\Sigma\Delta$ modulator can measure the slew rates

Figure 5.4. Recovered Output Waveform ($f_{\text{cutoff}} = 0.04 \cdot f_s$).

Figure 5.5. Recovered Output Waveform ($f_{\text{cutoff}} = 0.002 \cdot f_s$).

Figure 5.6. 3-D Surface Plot for Measured Slew Rate Using T2S3.

Figure 5.7. Contour for the 3-D Surface of Measured Slew Rate.

Figure 5.8. Bode Plot illustrating the relationship of closed-loop bandwidth of the test circuit and open-loop bandwidth of the Op-Amp.

of the DUTs. The expected 3-D surface should be a flat surface tilted at a 45 degree angle with the X-axis; the expected contour plot should be composed of only vertical straight lines which should line up with the grid values on the X-axis. The deviation of the measured from the expected results is primarily due to the reasons stated previously.

5.1.3 Unity Gain Bandwidth (GBW) Measurement

The GBW of an Op-Amp is defined as the frequency of the Op-Amp at which the open-loop gain is unity. The test circuit configuration for the Op-Amp is a unity gain buffer; therefore, the closed-loop bandwidth of the test circuit will be identical to the GBW of the Op-Amp. Fig. 5.8 is the Bode Plot showing the relationship between the

closed-loop bandwidth and the open-loop bandwidth of the Op-Amp. As mentioned in Chapter 3, the GBW can be measured by performing a Fast Fourier Transform on the sampled bit-stream. The measured 3-dB point on the power spectrum will be equal to the GBW of the Op-Amp.

The GBW of an Op-Amp can also be interpreted by using the 3-dB points at two different closed-loop gain levels [Jun86]. This method may ease the requirements on the performance of the $\Sigma\Delta$ modulator in terms of sampling rate, since the 3-dB points will occur at a much lower frequency. However, because of the gain of the test circuitry, the $\Sigma\Delta$ modulator may not be able to handle the large voltage swings of the DUT and may require extra circuitry to attenuate the input signal before applying it to the $\Sigma\Delta$ modulator. The required extra circuitry for voltage attenuation and gain setting may significantly increase the complexity and overhead of the device. Nonetheless, the method could be used to measure the bandwidth of a high performance Op-Amp.

Fig. 5.9 to Fig. 5.12 show the power spectrums for some of the DUTs. The plots are based on a 16,384-point FFT using a rectangular window. The sampling rate used for the $\Sigma\Delta$ modulator is 10.24 MHz. The slew rates for the DUTs are assumed to be high and thus the rise times of the outputs are dominated by the exponential (the effect of slew rate on the measuring of GBW will be addressed later in this section). For 3-dB point falls between FFT bins, linear extrapolation is used to estimate the points. Accuracy can be improved by using more sampled data points.

As shown in the figures, the measured 3-dB points, as marked by circles on the plots, match the corresponding DUT's GBW very closely. For DUT's with low GBW, the measurements are quite accurate with incurred error of no more than half the bin width in either direction. However, as the DUT's GBW reaches three percent of the sampling frequency ($0.03 * f_s$), quantization noise starts to take effect and becomes dominant at frequencies beyond four percent of the sampling rate ($0.04 * f_s$). This frequency repre-

Figure 5.9. Power spectrum for Op-Amp with GBW of 0.003MHz.

Figure 5.10. Power spectrum for Op-Amp with GBW of 0.03MHz.

Figure 5.11. Power spectrum for Op-Amp with GBW of 0.1MHz.

Figure 5.12. Power spectrum for Op-Amp with GBW of 0.3MHz.

Figure 5.13. Figure showing the power spectrum distorted by slew rate vs. one recovered using the curve shifting technique discussed.

sents the maximum allowable GBW that can be measured. GBW that falls beyond this point will be buried by quantization noise and would be impossible to recover. For GBW falls between two to four percent of the sampling rate, the curve starts to roll-off at around one percent of the sampling rate ($0.01 \cdot f_s$). The 3-dB points can still be estimated by using the curve fitting method even though the curve is contaminated by noise. Similarly to the limitation imposed on the slew rate measurements, the bandwidth limitation is again due to the fact that not enough samples are taken to resolve the time-constant of the exponential, causing large errors to be incurred. The problem can be circumvented by using a higher sampling rate for the $\Sigma\Delta$ modulator as discussed in Chapter 3, but this may not always be possible to achieve due to hardware constraints.

For output signals that are dominated by slew rate, the power spectrum will be distorted. Fig. 5.13 shows the power spectrum of a DUT which is dominated by slew rate;

the 3-dB break point of the DUT is distorted by the slew rate which renders its measurement inaccurate. The problem can be alleviated by first estimating the break point at which the slew rate ends and the exponential begins, then shifting the sampled data by the same number of points and performing a FFT on it. The result of this operation on the output signal depicted in Fig. 5.13 is superimposed on the same figure to indicate the 3-dB points that can be restored in this manner. By shifting the sampled data, the effective amplitude of the output signal is reduced. This has the effect of reducing the signal energy level in the power spectrum as shown in the figure. Therefore, the method is effective for output signals that are only partly dominated by the slew rate. The estimation of the slew-to-exponential break point can be coupled with the algorithm used to estimate the slew rate.

The capability of the T2S3 $\Sigma\Delta$ modulator to measure the GBW of the DUT is illustrated in Fig. 5.14 and Fig. 5.15. Fig. 5.14 is a 3-D surface plot showing the measured GBW against the DUT's slew rate and the GBW; Fig. 5.15 is the contour plot of the 3-D surface plot, which shows the accuracy of the measurements. The sampling rate used for the $\Sigma\Delta$ modulator is 10.24MHz. Again, the measurement of the GBW of the DUT is based on a 16,384-point FFT with a rectangular window.

The expected 3-D surface should be a flat surface tilted at a 45 degree angle with the Y-axis; the expected contour plot should be a set of horizontal lines which line up with the grid points on the Y-axis. As shown in the two figures, the measured results deviated from the results at the regions when the GBW of the DUT is high. This problem is attributed to quantization noise as mentioned previously.

5.1.4 Simulation Results

The simulation results for slew rate and GBW measurements using T2S3 are presented in the following table. The test is conducted by using the $\Sigma\Delta$ modulator to sample an

Figure 5.14. 3-D Surface plot showing the measured GBW by T2S3.

Figure 5.15. Contour plot showing the accuracy of the measured GBW by T2S3.

Op-Amp output waveform. An algorithm is then used to determine the breaking point between the slew and the exponential. The average slope of the first part of the curve is the slew rate. A FFT is performed on the portion of the waveform which not affected by the slew rate and the 3-dB point is determined from the resulting frequency spectrum.

The algorithm to determine the break point works as follows: after the output waveform is restored from the sampled data, the rising edge of the waveform is divided into ten equal steps. The average slope for the edge to rise from zero to each step is calculated. When the exponential starts to dominate, the average slope will start to fall. The break point will be assumed to occur at the time where the average slope begins to drop. However, because of the noise factor discussed in the previous section, large fluctuations occur when calculating the average slope. To ensure that the algorithm works properly, the incremental slope for each step is calculated and used as a conditional check to ensure that the transition takes place. When the exponential begins to dominate, both the incremental and average slopes should decrease consistently.

Table 5.2 lists some of the results obtained by using the technique. Three different frequency points with three different slew rates are used for the measurements. The slew rates are chosen such that the break-point will occur at one of the following three regions of the rising edge: 0-20%, 20-80 and 80-100%. The results show that the slew rate measurements are highly accurate when the break points occur at the 80-100% region. This is due to the fact that the rise time is totally dominated by the slew rate and enough sampling points are collected to determine the slew rate. However, the errors for the GBW measurements are large when break points occur in this region because of the lack of sampling points to resolve the GBW. When break points occur in the 0-20% region of the rise time, the reverse is true. The GBW measurements are highly accurate but the slew rate is not, because the rising edge is totally dominated by the exponential. Only when the break points occur in the center region of the rising edge is the accuracy of the measurements acceptable for both measurements.

Op-Amp Characteristic		Slew Rate (V/us)		GBW (MHz)	
Slew (V/us)	GBW (MHz)	Measured	% of Error	Measured	% of Error
0.01	0.05	0.0100	0.3	0.014	-37.5
0.10	0.05	0.096	4.0	0.05	0.0
0.30	0.05	0.240	-20.0	0.05	0.0
0.05	0.1	0.051	1.2	0.05	-50.0
0.20	0.1	0.158	-21.0	0.092	-8.0
0.50	0.1	0.317	-36.6	0.098	-1.9
0.10	0.2	0.098	-2.2	0.129	-35.5
0.50	0.2	0.465	-7.1	0.181	-9.5
0.90	0.2	1.05	16.5	0.186	-7.0

TABLE 5.2. Measured results for slew rate and GBW.

The measured results in Table 5.2 are based on an ideal $\Sigma\Delta$ modulator and did not take circuit imperfection into consideration. The effect of circuit nonidealities on the performance of the $\Sigma\Delta$ modulator has been discussed briefly in Section 4.3. As stated before, switch-capacitor technique is often used for realization of $\Sigma\Delta$ modulators. The fundamental constraints of switch-capacitor circuits for the realization of $\Sigma\Delta$ modulator are as follows [DPO⁺92][HB86]:

- Thermal noise generated by the switches and the Op-Amps used to construct the $\Sigma\Delta$ modulator.
- Settling errors due to the finite values of GBW and the slew rate of the Op-Amps used to construct the $\Sigma\Delta$ modulator.

These circuit constraints cause the in-band noise-floor of the overall system to rise,

which, in turn, causes the SNR of the overall system to suffer. [DPO⁺92] shows that as the oversampling factor rises for the $\Sigma\Delta$ modulator, the settling errors start to take effect and the resolution of the system begins to decrease. Therefore, it can be concluded that circuit nonidealities will impair the measuring capability of the $\Sigma\Delta$ modulator.

5.2 Measurement of Damped Second-Order Operational Amplifier Circuits

If an additional pole to the open-loop transfer function of the operational amplifier circuit is introduced, this will have a detrimental effect on the measurement of the GBW of the test circuit. Such an additional pole may arise from an uncompensated Op-Amp or heavy capacitive loading at the output of the test circuit. Depending on the location of the new pole, the power spectrum of the DUT will be affected. If the new pole is placed near f_1 , large ringing or oscillations may occur and the DUT will be deemed unstable. This section will investigate the capability of the $\Sigma\Delta$ modulator to handle a damped second-order output.

The step response of an operational circuit is given as:

$$y = 1 + K_1 e^{-[\omega_n (\delta - \sqrt{\delta^2 - 1})]t} + K_2 e^{-[\omega_n (\delta + \sqrt{\delta^2 - 1})]t} \quad (\text{EQ 5.3})$$

where

$$K_1 = -\frac{1}{2(\sqrt{\delta^2 - 1})(\delta - \sqrt{\delta^2 - 1})}$$

Figure 5.16. Power spectrum of a critically damped operational circuit ($f_t=0.1\text{MHz}$).

$$K_2 = \frac{1}{2(\sqrt{\delta^2 - 1})(\delta + \sqrt{\delta^2 - 1})}$$

$$\delta = \frac{1}{2} \sqrt{\frac{\omega_p}{\omega_t}} = \text{damping ratio.}$$

$$\omega_n = \sqrt{\omega_t \omega_p} = \text{undamped natural frequency.}$$

ω_p is frequency in rad/s for the new pole.

When $f_p \gg f_t$, the damping ratio is large and K_2 is small. The step response of the test circuit is approximately equal to:

Figure 5.17. Power spectrum of a underdamped operational circuit ($f_t=f_p=0.1\text{MHz}$).

$$y \approx K_1 e^{-\gamma_1 t} \quad (\text{EQ 5.4})$$

The 3-dB frequency of the test circuit is equal to f_t . Provided that f_t is below the maximum allowable GBW that the $\Sigma\Delta$ modulator can handle, the 3-dB point of the DUT can be determined.

However, when $f_p = 4f_t$, the damping ratio is equal to one and the circuit is critically damped. The step response of the of the test circuit is equal to:

$$y = 1 - (1 + t\omega_n) e^{-\omega_n t} \quad (\text{EQ 5.5})$$

The 3-dB frequency is approximately equal to f_n . Fig. 5.16 shows the power spectrum of a DUT with f_t of 0.1MHz. The measured 3-dB point is 0.1531MHz. The error is due to the additional pole introduced to the open-loop transfer function of the test circuit. This new pole causes slight gain peaking around f_t which drives the 3-dB point to a

higher frequency location. Since the expected DUT is known beforehand, the higher than expected GBW indicates that an additional pole is located in the vicinity of the expected GBW.

When the new pole is placed below the $4*f_t$, the damping ratio will become less than one. This results in ringing or oscillation on the output of the operational circuit. The step response of the test circuit is equal to:

$$y = 1 - \frac{e^{-\delta\omega_n t}}{\sqrt{1-\delta^2}} \sin \left[(\omega_n \sqrt{1-\delta^2}) t + \arccos(\delta) \right] \quad (\text{EQ 5.6})$$

EQ 5.6 shows that the output of the test circuit is a damped sine waves with a frequency:

$$\omega_d = \omega_n \sqrt{1-\delta^2} \quad (\text{EQ 5.7})$$

Fig. 5.17 shows the power spectrum of the a test circuit with $f_t=f_p=0.1\text{MHz}$. The peak in the figures, referred to as resonant gain peaking, indicates a large sinusoidal is present at the output of the operational amplifier circuit. The measured 3-dB point is 0.1568MHz. As in the case of a critically damped circuit, the gain peaking near f_t drives the 3-dB points beyond f_t , making the determination of f_t very difficult. However, since the expected f_t is known beforehand, f_t can be determined by using the magnitude of the resonant gain peaking and the frequency at which the peak occurs [DOS81]. When the new pole is placed well below f_t , a large peak occurs at ω_d . But since the peak occurs well below f_t , its influence on f_t is not as significant. Fig. 5.18 shows the power spectrum of a test circuit with $f_t=0.1\text{MHz}$ and $f_p=0.0125\text{MHz}$., the measured 3-dB point is 0.1181MHz.

Figure 5.18. Power spectrum of a underdamped operational circuit ($f_t=0.1\text{MHz}$, $f_p=0.0125\text{MHz}$).

5.3 Techniques to Improve the Measuring Capability of $\Sigma\Delta$ Modulator

Although $\Sigma\Delta$ modulators can be used to measure the frequency response of analog circuitry, the maximum allowable GBW that can be measured by using $\Sigma\Delta$ modulators is limited by the requirement of a high sampling rate to avoid the effect of quantization noise. For T2S3, as shown in previous sections, quantization noise starts to dominate at around three percent of the sampling rate ($0.03 * f_s$) and becomes totally dominant around four percent of the sampling rate ($0.04 * f_s$), making any DUTs with bandwidth beyond that point not measurable. To make the technique feasible and appealing for implementation on chip, the maximum allowable bandwidth that can be measured should be improved.

In order to improve the bandwidth measurement of $\Sigma\Delta$ modulators, the quantization

noise must be reduced at high frequency. Increasing the order of the $\Sigma\Delta$ modulator alone cannot achieve this result since noise gain is of a high-pass nature, which attenuates quantization noise at baseband but amplifies it at high frequency [AS83]. In other words, quantization noise increases at high frequency as the order of the $\Sigma\Delta$ modulator increases. One approach to resolving the problem is to alter the transfer function of the $\Sigma\Delta$ modulator to reduce the high noise gain at high frequency, but this may not be achievable without destroying the primary function performed by the modulator. This section will investigate three different techniques in an attempt to improve the measuring capability of the $\Sigma\Delta$ modulators.

5.3.1 Noise Reduction Using Auto-Correlation on Periodic Square Wave

As mentioned before, quantization noise begins to dominate around three percent ($0.03 \cdot f_s$) of the sampling rate. This is attributed to the fact that the input signal is rising at a very high rate and very few samples are collected by the $\Sigma\Delta$ modulator to resolve the time constant of the input exponential. Since $\Sigma\Delta$ modulators use very coarse quantizers and require a large collection of samples to resolve the magnitude of the input signal, this lack of input samples causes the noise to rise in that region.

One way to resolve the problem is to apply spectral averaging. This technique requires the GBW test to be repeated a number of times and the corresponding power spectrums to be averaged. This technique should provide even better results in practice due to the randomness of noise such as clock jitter and thermal noise. However, the additional testing time and computational requirement may prohibit its use.

The other technique is to use a periodic square wave as test signal and then perform auto-correlation on the output bit-stream of the $\Sigma\Delta$ modulator. This technique effectively increases the number of input samples and, consequently, the maximum allow-

able GBWs that can be measured should also be improved. However, the improvement is achieved at the expense of a more complicated test signal.

The Fourier series expansion of a square wave is an odd function containing an infinite number of sine terms [Pap80]:

$$x = \sum_{n=0}^{\infty} \frac{1}{2n+1} \sin((2n+1)\omega_o t) \quad (\text{EQ 5.8})$$

The Fourier Transform of a periodic square wave thus contains a series of peaks located at all the odd harmonics of the square wave, and the magnitude of the peaks is rolling off at 20dB/decade. The output from the test circuit is then the convolution of EQ 5.8 and the transfer function of the test circuit. Fig. 5.19 shows the resulting power spectrum of a DUT with $f_1=0.3$ MHz; slew rate of the DUT is assumed to be high. The frequency of the input square wave, f_i , is 10KHz.

To determine the 3-dB of the DUT, the output bit-stream from the $\Sigma\Delta$ modulator is first differentiated to remove the power of the input square wave in the power spectrum. Auto-correlation is then performed on the differentiated output waveform and window (Blackman-Harris) is applied to the resulting auto-correlation function. Finally, FFT is performed on the windowed auto-correlation function to determine the f_1 of the DUT.

Fig. 5.20 and Fig. 5.21 shows the windowed auto-correlation function and its FFT. Since the auto-correlation will result a 40dB roll-off in the frequency domain, the f_1 of the DUT is measured at the 3-dB point of the power spectrum. The measured f_1 is 0.3481MHz and the measurement error is 16.03%. By increasing the frequency of the input square wave to 20KHz, the measured f_1 becomes 0.3256 and the measurement error is reduced to 8.5%.

As shown in Fig. 5.21, the quantization noise begins to rise around 0.5MHz and f_1 that falls in beyond 0.5MHz is totally obscured. However, for DUTs with GBW between

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS
STANDARD REFERENCE MATERIAL 1010a
(ANSI and ISO TEST CHART No. 2)

0.4-0.7MHz, the curve begins to roll-off at 40dB/decade before quantization noise becomes dominant. By extending the curve in this manner, f_1 of the DUT can be approximated. Fig. 5.22 shows the power spectrum of a DUT with f_1 of 0.6MHz; the frequency of the input square wave is 10KHz. The measured f_1 is 0.625MHz and the error is 4.2%. Table 5.3 shows the results of the measurements of DUTs with GBWs vary from 0.4 to 0.7MHz. The measurements are conducted for different frequencies of input square wave.

GBW (MHz)	Input Period Square Wave Frequency					
	5KHz		10KHz		20KHz	
	Measured f_1	% of Error	Measured f_1	% of Error	Measured f_1	% of Error
0.4	0.435	8.75	0.4181	4.53	0.4225	5.63
0.5	0.5563	11.3	0.5431	8.63	0.5056	1.13
0.6	0.645	7.5	0.6369	6.15	0.6262	4.38
0.7	0.7612	8.75	0.7576	8.13	0.741	6.0

TABLE 5.3. Results of GBW measurements vs. input square wave frequency.

The frequency of the input square wave plays a significant role in the measurement accuracy of the technique. By increasing the frequency of the input square wave, the technique provides better approximation of f_1 . However, the pulse width of the square wave should be wide enough to allow the exponential to settle; otherwise, large error will occur. Since the expected f_1 is known beforehand, the selection of the frequency of the input square wave should not pose any difficulty.

The results in Table 5.3 show that by using periodic input square wave and auto-correlation function techniques to extract the GBW of the DUT, a T2S3 $\Sigma\Delta$ modulator can achieve an adequate measuring capability with an oversampling factor of fifteen. However, the benefit is achieved at the expense of additional computational time and a more complicated test signals.

Figure 5.19. Power spectrum of DUT ($f_t = 0.3\text{MHz}$) using input square wave with frequency $f_i = 10\text{KHz}$.

Figure 5.20. Windowed auto-correlation of the differentiated waveform.

Figure 5.21. Power spectrum of the DUT by performing FFT on the auto-correlation function shown in Fig. 5.19.

Figure 5.22. Power spectrum of the DUT with $f_t=0.6\text{MHz}$ (Solid line in the figure represents the approximation).

5.3.2 Multi-level Quantizer

The Multi-level quantizer was originally developed for solving the stability problem of the high-order $\Sigma\Delta$ modulators using a two-level quantizer, which is the result of quantizer overload [Can85]. The quantization noise power, P_n , is equal to the quantization step size, Δ [PM88]:

$$P_n = \frac{\Delta^2}{12} \quad (\text{EQ 5.9})$$

The step size is in turn proportional to the number of bits, b , used in the quantizer:

$$\Delta \propto \frac{1}{2^b} \quad (\text{EQ 5.10})$$

Therefore, each additional level used in the quantizer will reduce the noise level by 6dB. [CT92].

Figure 5.23. SNR for T2S3 $\Sigma\Delta$ modulator using multi-level quantizer.

The design of a multi-level quantizer is relatively straight forward: it should provide sufficient levels to code both the worst case noise at its input as well as the input signal range without overload [Car89]. Assuming overloading does not occur, the quantization error is bounded between $\pm 1/2$ LSB. If the noise gain is $|W(Z)|$, then the number of bits required to represent the noise in a worst-case scenario will be $\pm 1/2 \text{ LSB} * |W(Z)|$. If the input signal also occupied $\pm N$ LSB, then the total number of bits required to represent the signal at the input of the quantizer will be equal to:

$$N + \left(\frac{1}{2}|W(Z)|\right) \quad (\text{EQ 5.11})$$

Since the gain of the quantizer, which is 1 LSB/digital level, is known, the number of levels required to prevent overloading is also equal to the number of bits required to represent the signal at the input of the quantizer.

However, the drawback of using a multi-level quantizer is the requirement for a high accuracy digital-to-analog (D/A) converter in the feedback loop. Any error introduced by the D/A converter will usually have a large baseband energy content that will degrade the performance of the overall structure [CT92]. Nevertheless, the gain in the measuring capability of the $\Sigma\Delta$ modulator may justify the decision. Several techniques have been developed to simplify the development of the D/A converter [CT92], [PBS⁺87] [LS90]. This section will investigate the performance of the T2S3 equipped with a multilevel quantizer at both of its stages, mainly to determine how its capability to measure bandwidth can be improved. A sixteen level quantizer will be used to investigate the trade-off between bandwidth and complexity of the quantizer.

Fig. 5.23 shows the SNR for T2S3 using a multi-level quantizer, with the SNR improving as the number of levels of the quantizer increase. This is attributed to the reduction of quantization noise in the baseband. The figure shows that overloading still occurs at high levels of input signals, due to the fact that the input signal has totally occupied the bit range of the quantizer. Fig. 5.24 and Fig. 5.25 shows the idle channel

Figure 5.24. Idle channel noise calculation for T2S3 using 16-level quantizer.

Figure 5.25. DC error calculation for T2S3 using 16-level quantizer.

Figure 5.26. Power spectrum using multi-level quantizer ($f_t=0.4\text{MHz}$).

Figure 5.27. Power spectrum using multi-level quantizer ($f_t=0.6\text{MHz}$).

Figure 5.28. Estimation of 3-dB point using the curve fitting method for DUT with $f_t = 0.4$ MHz.

Figure 5.29. Estimation of 3-dB point using the curve fitting method for DUT with $f_t = 0.6$ MHz.

noise and the DC error measurement of T2S3 using a sixteen level quantizer. As expected, the average idle channel noise level has improved by almost 20dB and the average DC error has also been reduced by at least 20dB. Comparing the figures to those using the two-level quantizer, the peaks that are shown in the figures using the two-level quantizer have also been smoothed out, indicating that the multi-level quantizer has decorrelated the noise.

The results of using a T2S3 with a 16-level quantizer to measure the bandwidth of two DUTs with different bandwidth are shown in Fig. 5.26 and Fig. 5.27. The DUT used in Fig. 5.26 has a GBW of 0.4 MHz, while the one in Fig. 5.27 has a GBW of 0.6 MHz. The slew rates for both DUTs are assumed to be high to eliminate the distortion on the power spectrum that may result. As shown in both figures, the magnitude of quantization noise has been reduced by at least 25dB at high frequency and the effect of quantization noise does not become dominant until 0.7 MHz. This effectively doubles the bandwidth measuring capability of the $\Sigma\Delta$ modulator. The measured 3-dB points for both DUTs obtained by direct measurement from the power spectrum are 0.32 MHz and 0.42MHz.

The discrepancy is due to the effect of quantization noise as shown in the figures. However, by smoothing out the noise effect using the curve fitting techniques, the estimated results become 0.3769MHz and 0.63MHz, representing a maximum error of less than five percent. Fig. 5.28 and Fig. 5.29 show the estimates of the 3-dB points of Fig. 5.26 and Fig. 5.27 using the curve fitting technique. The results indicate that signal improvement on the $\Sigma\Delta$ modulator's capability of measuring the GBW of an Op-Amp. For a T2S3 using a 16-level quantizer, the required oversampling factor to achieve adequate measuring capability is reduced to seventeen.

5.3.3 Adaptive Quantizer

This section will investigate the possibility of using an adaptive quantizer in an attempt to improve the frequency measurement capability of the $\Sigma\Delta$ modulator. The technique was first proposed by Yu et al [YSH92]. The goal in using adaptive quantization is again to minimize the quantization noise by choosing a quantization step just large enough to match the varying amplitude of the input signal. Although the feasibility of the technique has been demonstrated by using computer simulation [YSH92], it has yet to be implemented in silicon and the hardware requirements are still an unknown factor.

The design of the adaptive quantizer is quite straight forward. Two methods can be used: feed-forward and feedback adaptation [RS78]. Feed-forward adaptation is based on unquantized samples, $U(n)$, at the input of the $\Sigma\Delta$ modulator; while feedback adaptation is based on the quantized samples, $Y(n)$, at the output $\Sigma\Delta$ modulator. The structure of a first-order $\Sigma\Delta$ modulator using a feed-forward adaptive quantizer is shown in Fig. 5.30. Both methods involve the estimation of the variance of the signal (quantized or unquantized) by assuming it is proportional to the short-time energy [RS78]. The short-time energy is defined as the output low-pass filter with input, $x^2(n)$:

$$\sigma^2 = \sum_{m=-\infty}^{\infty} x^2(m) h(n-m) \quad (\text{EQ 5.12})$$

where $h(n)$ is the impulse response of the low-pass filter.

The quantization step is then defined as:

$$q_n = c\sigma_x^2(n) \quad (\text{EQ 5.13})$$

Figure 5.30. Structure of a first-order $\Sigma\Delta$ modulator using feedforward adaptive quantizer.

where σ_x^2 is the variance for either $U(n)$, feed-forward adaptation, or $Y(n)$, feedback adaptation.

c is a scaling factor.

However, a large number of calculations are required to obtain the short-term energy for the signal. The technique is simplified by using the local values of peak magnitude to determine the quantization level. The quantization step is thus equal to:

$$q_n = c|u|_{max} \quad (\text{EQ 5.14})$$

where $|u|_{max}$ is the peak of a data block that contains K samples. It can be defined as:

$$|u|_{max} = \max \{ |u(n-k)| \} \quad (\text{EQ 5.15})$$

where $k = 1, 2, \dots, N$. N depends on the stationery property of the

Figure 5.31. SNR calculation for a T2S3 $\Sigma\Delta$ modulator using an adaptive quantizer.

input signal.

The SNR ratio for a $\Sigma\Delta$ modulator using adaptive quantizer is given as [YSH92]:

$$SNR = \left(\frac{3}{2c^2}\right) SNR_{enhancement} \quad (EQ 5.16)$$

The SNR calculation for the T2S3 using the adaptive quantizer is shown in Fig. 5.31. The SNR is a horizontal line across the input range, indicating that the dynamic range of the system is improved by the presence of an adaptive quantizer. The test signal is 10KHz sinusoidal and the scale constants are 1.5 and 1.0 for the adaptive quantizer at first stage and second stage respectively. The scaling factors are chosen in such a way that the quantization level plus the maximum input signal will not overload the integrators. The number of sample points used to detect the peak value is 500 for both stages. The lower than expected SNR is due to the high in-band quantization noise which may be caused by the interaction of two quantizers, resulting in the quantization

Figure 5.32. Gain measurement of the T2S3 $\Sigma\Delta$ modulator using an adaptive quantizer.

Figure 5.33. Power spectrum using the T2S3 $\Sigma\Delta$ modulator with adaptive quantizer.

noise from the two stages not cancelling each other.

The constant SNR indicates that the adaptive quantizer introduces non-linear gain to the system. The gain of the modulator is depicted in Fig. 5.32 which shows the gain is inversely proportional to the magnitude of the input signal. Hence, the input to output relationship of the system is no longer linear, making it not suitable for measurement purposes, particularly for DC signals. Fig. 5.33 shows the GBW measurement for a device using the T2S3 with an adaptive quantizer. The result indicates heavy distortion on the power spectrum.

5.4 Conclusion

This chapter provided detailed verification of the proposed technique of using $\Sigma\Delta$ modulator for slew rate and bandwidth measurement for an Op-Amp. The Two-Stage-Third-Order (T2S3) $\Sigma\Delta$ modulator discussed in previous chapter was chosen to analyze the merits and problems of using a $\Sigma\Delta$ modulator for analog circuit testing purposes. For slew rate measurements, the accuracy is dependent on the number of samples the $\Sigma\Delta$ modulator able to sample on the rising edge of the output signal. The results are summarized in Table 5.1. With the adequate number of sampling points, the accuracy of the measurements lies within ten percent. For GBW measurements, simulation results show that the technique requires an oversampling factor of only 25 for the T2S3 $\Sigma\Delta$ modulator using a two-level quantizer in order to produce accurate measurements.

Other techniques of improving the GBW measurement capability of the $\Sigma\Delta$ modulator have also been investigated. The use of periodic square wave inputs as a test signal and auto-correlation techniques to reduce quantization noise reduce the requirement of oversampling factor for GBW measurements to 15. By using a 16-level multi-level quantizer on the T2S3, it was found that the quantization noise at high frequency can

be significantly reduced and can reduce the requirement for the oversampling factor to 17 for accurate GBW measurements. The results are summarized in Table 5.4. However, the drawback of using the multi-level quantizer is that it will increase the bit-width of the output data and the requirement for a precision A/D quantizer in the feedback path of the $\Sigma\Delta$ modulator.

Noise Reduction Technique	Required Oversampling Factor
Direct Oversampling	25
Autocorrelation	15
16-level Quantizer	17
Adaptive Quantizer	N/A

TABLE 5.4. The required oversampling ratio for GBW measurements for each noise reduction technique.

The chapter also investigated the possibility of using an adaptive quantizer on the T2S3 to reduce the quantization effect. Because of the non-linear gain introduced by the overall structure, the adaptive quantizer is deemed impractical for measurement purposes.

CHAPTER 6

Conclusions and Recommendation for Further Work

6.1 Summary and Conclusions

Current analog testing techniques cannot address the testability issues that have been brought on by increasingly complex analog and mixed-analog circuits. New techniques [MW89][Wey90][AS90][MW89] have been proposed to address these issues, but they suffer a series of drawbacks that restrict their broad usage. By placing an A/D converter on-chip, test data can be taken and encoded within the device before it is shifted out. The encoding of test data on-chip offers an added advantage in that, since digital data is more immune to noise and other types of interference, less expensive test equipment is required. Although conventional A/D converters can also be used for this purpose, oversampled A/D converters are more cost effective because of their insensitivity to process variations and the output data is usually only few bits wide which will not increase pin overhead.

The motivation for this research project was to investigate the possibility of using an on-chip oversampling A/D converter for testing purposes. To achieve the objectives set out for the thesis, the following work was conducted. After an introduction to the

thesis in Chapter 1, an overview of the currently proposed analog circuit testing techniques was provided in Chapter 2. The five selected techniques provided a general feel for how testability issues are currently being addressed. To circumvent the problem of inaccessibility to internal nodes, most techniques resort to using models or other circuit analysis approaches which require extensive computer simulation to predict fault locations and causes. Other techniques discussed can either only be used for open/short detection or require expensive hardware to implement.

In Chapter 3, the idea of using on-chip A/D for analog circuit testing was proposed, and the reasons for choosing an oversampling A/D converter over conventional A/D converters were detailed. The chapter then proceeded with a presentation of the operating principle of oversampling A/D converters. Simulation results using a second order oversampling A/D converter to measure the slew rate and GBW were presented and discussed. The results indicated that the technique is technically feasible for analog circuit testing purpose.

Chapter 4 examined the use of high order oversampling A/D converters to improve the measurement accuracy. Four different oversampling A/D converters belonging to two classes of architectures were analyzed and characterized. The oversampling A/D converters selected for analysis were limited to second- and third-order types; converters of higher than third order were deemed impractical at present due to their complexity and were therefore excluded from the analysis. The characterization of the four oversampling A/D converters was based on their SNR, idle channel noise, linearity and DC error. The characterization of oversampling A/D converters was deemed important due to the fact that their idle channel noise is highly DC-bias dependent [CNL⁺90]. The results indicated that a Two-Stage Third-Order (T2S3) oversampling A/D converter has the best overall performance among the four.

Using a Two-stage Third-Order (T2S3) oversampling A/D converter, a detailed analysis of slew rate and GBW measurements was provided in Chapter 5. The chapter stud-

ied the effect on quantization noise on the accuracy of the measurement. Simulation results indicated that accurate measurements can be obtained with an oversampling factor of twenty-five. The chapter then proceeded with the analysis of the use of the auto-correlation technique and of multi-level and adaptive quantizers to improve the measuring capability of the oversampling A/D converter. It is found that the auto-correlation technique can reduce the requirement of oversampling factor to fifteen. By using a sixteen-level multi-level quantizer, accurate measurements can be obtained with an oversampling factor of seventeen. An adaptive quantizer was deemed inadequate for this precision measurement due to its non-linear gain characteristic.

This thesis report demonstrates that the use of an $\Sigma\Delta$ modulator for on-chip analog circuit testing is technically possible. The advantages of using an on-chip A/D converter for analog circuit testing have been discussed in Chapter 3. The use of an on-chip $\Sigma\Delta$ modulator eliminated some the problems that plagued the current analog circuit testing techniques discussed in Chapter 2. This technique does not require the use of circuit models which are expensive to develop and maintain. Since all analog signals are digitized on-chip, a single digital tester can be used for testing the devices. Moreover, the technique allows parametric measurements to be performed on-chip, thus providing better screening of faulty devices before reaching the final-test stage.

Naturally, the requirement of the extra hardware is a price to pay for the use of this technique. For a large device, the extra circuitry required to route output signals to the $\Sigma\Delta$ modulator may increase the complexity and overhead of the devices. Yet it is believed that the ability to eliminate the need of external analog test equipment and the fact that the analog signal is 'probed' on chip offers the advantages to be considered while deciding on the testing strategy to be implemented. The high frequency clock required to operate the $\Sigma\Delta$ modulator may also have an adverse effect on the overall performance of the DUT.

6.2 Recommendations for Future Work

Although this thesis has demonstrated that oversampling A/D converters can be applied to analog circuit testing through the use of simulation, it is recommended that the work be duplicated by using actual hardware to assess what would be required to implement the technique on silicon. A strategy as to how the technique could be used in testing a large complex analog circuit is worth pursuing, due to the large number of test points that may be required for observation. An efficient way to capture data at all test point will definitely reduce testing time.

Other recommended areas for future work in using the oversampling A/D converter for analog circuit testing include:

- A study as to whether the oversampling A/D converter can be used to measure non-linear characteristics of the device-under-test.
- An investigation of an efficient way to handle current measurements since this will require the breaking of the circuit.
- A study of ways to apply the technique to measure low amplitude signals (signals in μV range).
- An investigation of pattern matching techniques to determine the frequency response or impulse response of the DUT.

Bibliography

- [AS83] B. Agrawal and Kishan Shenoi, "*Design Methodology for $\Sigma\Delta M$,*" IEEE Trans. Communications, vol. com-31, pp. 360-370, Mar. 1983.
- [AS90] M. A. Al-Qutayri and P. R. Shepherd, "*On the testing of mixed-mode integrated circuits,*" Journal of Semicustom ICs, vol. 7, pp. 32-39, 1990.
- [Can85] J. C. Candy, "*A Use of Double Integration in Sigma Delta Modulation,*" IEEE Trans. Communications, vol. COM-33, pp. 249-258, Mar. 1985.
- [Car89] L. R. Carley, "*A Noise-Shaping Coder Topology for 15+ Bit Converters,*" IEEE Jour. Solid-State Circuits, vol. 24, pp. 267-273, Apr. 1989.
- [CB81] J. C. Candy and O. J. Benjamin, "*The structure of Quantization Noise from Sigma-Delta Modulation,*" IEEE Trans. Communication, vol. COM-29, pp. 1316-1323, Sept. 1981.
- [Che90] A. Chee, *Oversampled analog-to-digital converter and subscriber line channel modelling for digital subscriber loop transmission*, Master's thesis, Carleton University, 1990.
- [CNL⁺90] K. Chao, S. Nadeem, W. Lee and C. Sodini, "*A Higher Order Topology for Interpolative modulators for Oversampling A/D Converters,*" IEEE Trans. Circuits and Systems, vol. 37, pp. 309-318, 1990.

- [CT92] J. C. Candy and G. C. Temes, *Oversampling Delta-Sigma Data Converters*, IEEE Press, 1992.
- [DOS81] J. Dostal, *Operational Amplifiers*, Elsevier Scientific Publishing Company, 1981.
- [DPO⁺92] V. F. Dias, G. Palmisano, P. O'Leary and F. Maloberti, "Fundamental limitations of switched-capacitor sigma-delta modulators," IEE Proc.-G, vol. 139, pp. 27-32, Feb. 1992.
- [EK91] P. M. Rmbree and B. Kimble, *C Language Algorithms for Digital Signal Processing*, Prentice Hall, 1991.
- [Gra90] R. M. Gray, "Quantization Noise Spectra," IEEE Trans. on Information theory, vol. 36, pp. 1220-1244, Nov. 1990.
- [GM84] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons, 1984.
- [Har78] F. J. Harris, "On the use of Windows for Harmonic Analysis with the Discrete Fourier Transform," Proc. of the IEEE, vol. 66, pp. 51-83, Jan. 1978.
- [Hau91] M. W. Hauser, "Principles of Oversampling A/D Conversion," Jour. Audio Eng. Soc., vol. 39, pp. 3-26, Jan. 1991.
- [Jun86] W. G. Jung, *IC op-amp cookbook*, Howard W. Sams & Co, 1986.
- [Ken88] J. G. Kenney, *Design Methodology for N-th order Noise-Shaping Coders*, Master's Thesis, Carnegie Mellon University, 1988.
- [Lon88] L. L. Longo, *Multi-Stage Sigma-Delta Modulators*, Master's thesis, Carleton University, 1988.
- [LS90] T. C. Lesile and B. Singh, "An improved sigma-delta Modulator Architecture," IEEE Proc. ISCAS, pp. 372-375, 1990.

- [MAT91] The MathWorks, Inc., *MATLAB User's Guide*, Oct. 1990.
- [MB86] M. W. Hauser and R. W. Brodersen, "Circuit and technology considerations for MOS Delta-Sigma A/D converters," Proc. ICASSP, pp. 1310-1315, Apr. 1986.
- [McC85] E. J. McCluskey, "Built-in self-test technique," IEEE Design & Test of Computers, vol. 2, pp. 21-28, Apr. 1985.
- [MUI⁺87] Y. Matsuya, K. Uchimura, A. Iwata, T. Kobayashi, M. Ishikawa, and T. Kobayashi, "A 16-bit Oversampling A-to-D Conversion Technology Using Triple-Integration Noise Shaping," IEEE Jour. Solid-State Circuits, vol. sc-22, pp. 921-929, Dec. 1987.
- [MW89] A. McKeon, and A. Wakeling, "Fault Diagnosis in Analogue Circuits Using AI Techniques," Proc. International Test Conference, IEEE CS Press, pp. 118-123, 1989.
- [Pap80] A. Papoulis, *Circuits and Systems*, Holt, Rinehart and Winston, Inc., 1980.
- [PBS⁺87] J. J. Paulos, G. T. Brauns, M. B. Steer and S. H. Ardalan, "Improved signal-to-noise ration using tri-level delta-sigma modulation," IEEE proc. ISCAS, pp. 463-466, 1987.
- [PM88] J. G. Proakis and D. G. Manolakis, *Introduction to Digital Signal Processing*, Macmillian Publishing Company, 1988.
- [Ril89] T. A. D. Riley, *A comparison of implementation aspects in over-sampled analog to digital converters for use in ISDN subscriber loops*, Master's thesis, Carleton University, 1989.
- [RS78] L. R. Rabiner and R. W. Schafer, *Digital Processing of Speech Signals*, Prentice-Hall, Inc., 1978.

- [SK92] M. Slamani and B. Kaminska, "*Analog Circuit Fault Diagnosis based on Sensitivity Computation and Functional Testing*," IEEE Design & Test of Computers, pp. 30-39, Mar. 1992.
- [TTK⁺84] T. Tsukada, K. Takagi, Y. Kita and M. Nagata, "*An Automatic Error Cancellation Technique for Higher Accuracy A/D Converters*," IEEE Jour. Solid-State Circuits, vol. sc-19, pp. 266-268, Apr. 1984.
- [Wey90] C. L. Wey, "*Build-In Self-Test (BIST) Structure for Analog Circuit Fault Diagnosis*," IEEE Tran. Instrumentation and Measurement, Vol. 39, pp. 517-521, June 1990.
- [YSH92] J. Yu, M. B. Sandler and R. E. Hawken, "*Adaptive quantization for one-bit sigma-delta modulation*," IEE Proc. G vol. 139, Feb. 1992.

Appendix A

Blackman-Harris Window (4 term)

DFT considers the observed data sequence to be periodic in nature. For signals with a natural period not commensurate with the observation intervals, spectral leakages occur. This is due to the fact that only signals with frequencies that coincide with one of the frequency bins on the frequency axis will be projected onto a single frequency bin; all other frequencies will exhibit non-zero projections on all frequency bins. Windowing is applied to data to reduce the spectral leakage associated with finite observation intervals. The approach used by windows is to force both the beginning and end of the data sequence to zero, and to give emphasis to data in the middle of the sequence to compensate for the loss of power at the two ends of the observation window.

The four-term Blackman-Harris window used in this project is given as [EK91]:

$$w(n) = a_0 + a_1 \cos\left(\frac{2\pi}{N}n\right) + a_2 \cos\left(\frac{2\pi}{N}2n\right) - a_3 \cos\left(\frac{2\pi}{N}3n\right)$$

where $n = 0, 1, 2, \dots, N-1$.

$$a_0 = 0.35875$$

$$a_1 = 0.48829$$

$$a_2 = 0.14128$$

$$a_3 = 0.01168$$

The four-term Blackman-Harris window provides a -92dB sidelobe reduction and an equivalent noise bandwidth of 2 bins. The magnitude and log-magnitude plots are given in the following figures.

Figure A.1. Magnitude plot for four-term Blackman-Harris window.

Figure A.2. Log-Magnitude plot of transform of four-term Blackman-Harris window.

END

2 1-0 7-9 4

FIN