Slow Wave Transmission Lines used as Integrated Inductors with Improved Performance

by

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Abstract

Slow wave transmission lines (SWTLs) are analyzed in literature as an interconnections having the ability to slow down the propagating wave and consequently saving area, shielding substrate and lowering losses. In this thesis, on the other hand, possible ways are investigated to exploit these improvements to enhance, optimize and tune the inductive parameters of SWTLs; effective inductance (L_{eff}), quality factor (Q), self-resonance frequency (f_{srf}) and area efficiency.

Integrated in low-cost silicon substrate, on-chip inductors are facing crucial challenges, like design flexibility, area efficiency, conductive and substrate losses. Early studies have identified many techniques to overcome these challenges, such as post processing, magnetic core filling, ground plane modification, and others, however each technique has its drawbacks at RF frequencies which are reflected on either performance or cost.

The principle of operation of SWTLs is analyzed mathematically as a periodic structure by cascading multiple capacitive-loaded transmission line unit cells. L_{eff} and Q are extracted from the ABCD parameters. It has been proved that the distributed nature of SWTLs provides an enhanced inductive performance.

A parametric study on a coplanar stripline is introduced to explore and quantify the relation between eight spacial design variables related to the TL structure, and five inductive parameters. A parametric table, considered as a guideline to build SWTLs as inductors, have been created.

To validate the idea practically, various configurations of slow-wave coplanar striplines are designed, fabricated and measured on CMOS 130nm process (silicon substrate).

Optimized SWTLs are applied as inductors in a generic injection locked oscillator (ILO). Using SWTLs as inductors have provided additional degrees of freedom to lay out and tune L_{eff} , Q and f_{srf} efficiently. The differential balanced structure of the designed SWTLs have provided an equal single-ended inductance to both sides of the circuit without using lengthy interconnections leading to 50% enhanced Q compared to conventional transmission lines. SWTLs as inductors have shown a 75% and 60% enhanced Q compared to a single and double conventional spiral inductors. Additionally, an enhanced noise performance have been demonstrated in ILO using SWTLs as inductors compared to the conventional inductors.

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List of Abbreviations and Symbols

5G	Fifth generation
α	Attenuation constant
ADC	Analog to Digital Converter
AMC	Artificial Magnetic Conductor
β	Phase constant
BEOL	Back End of Line
BPF	Bandpass Filter
C	Capacitor
CMOS	Complementary Metal Oxide Semiconductor
D2D	Device to Device
DAC	Digital to Analog Converter
DUT	Device Under Test
ϵ	Permittivity
EM	Electromagnetic
FOM	Figure of Merit
γ	Propagation Constant
GHz	Giga Hertz (Frequency measuring unit)
GSG	Ground Signal Ground
θ	Electrical length
IC	Integrated Circuit
ILO	Injection Locked Oscillator
IoT	Internet of Things
λ	Wavelength
L	Inductance
LNA	Low Noise Amplifier

LNTA	Low Noise Transconductance Amplifier
μ	Permeability
MEMS	Micro-electro-mechanical System
MIM	Metal Insulator Metal
MIMO	Multiple-Input Multiple-Output
mmWave	Milli-metric Wave
nH	Nano Henry (Inductance measuring unit)
NPF	N-Path Filter
PBG	Periodic Band Gap
PCB	Printed Circuit Board
PLL	Phase Locked Loop
PN	Phase Noise
Q	Quality Factor
RF	Radio Frequency
SAW	Surface Acoustic Wave
SDR	Software Defined Radio
SOLT	Short, Open, Load, and Through
SRF	Self Resonance Frequency
SW	Slow Wave
SWF	Slow Wave Factor
SWTL	Slow Wave Transmission Line
V_p	Phase velocity
VCO	Voltage Control Oscillator
W	Watt
Ω	Ohm
Z_0	Characteristic impedance

Chapter 1

Introduction

1.1 Thesis Motivation

Fast emerging new wireless communication standards and the drastic growth in the ways and means by which people (and devices) need to communicate, have led to the fifth generation (5G) communication network architecture. Now, 5G is incorporating a variety of communication systems like multiple-input multiple output (MIMO), mmWave, device to device communication (D2D), internet of things (IoT) and software-defined radio (SDR) as shown in Figure 1.1. Specifically, SDR attempts to modify radio devices efficiently and cost-effectively using multi-standard RF reconfigurable transceivers which process signals following various specifications of these distinct standards.

A closer look at the RF front end in transceivers to the circuit level, reveals the main challenges facing their design. One challenge is that the benefits gathered from CMOS downscaling by digital circuits are not proportional to that gathered by analog circuits. This is because passive components are not scalable with the technology.

The advantages provided by passive components necessitates their existence in nearly all RF front-end modules. Reactive components have the desirable properties of almost zero noise contribution, low power, high linearity over the most extensive

Figure 1.1: A general 5G cellular network architecture [1].

possible dynamic range compared to active components [2]. In VCOs, for example, the stringent phase noise requirements make inductors unavoidable. To the contrary, inductor-less ring oscillators cannot achieve the same spectral purity, even with higher DC power [3]. On-chip inductors consumes most of the chip area in the RF front end circuits. That requires spending considerable effort to optimize the performance of on-chip inductors from many points of views; that is, effective inductance, quality factor, self resonance frequency and size efficiency.

At RF frequencies, a transmission line (TL) is a useful component used in transporting energy from one point to another. Various microwave components are based on TL theory and successfully realized. This is because transmission lines are well understood and highly matured in linking electromagnetic design to circuit analysis. The most important aspect of transmission lines operating at microwave frequencies and beyond is the fact that such lines can replace lumped elements, such as capacitors and inductors, in planar circuits, thus avoiding higher cost and circuit complexity [4]

During the last decade, potential enhancement in transmission-line based microwave devices using various techniques like Slow Wave [5, 6], electromagnetic bandgap [7, 8] and metamaterials [9, 10] have attracted research focus. Specifically Slow wave techniques have demonstrated high effective dielectric constant, high quality factor and size reduction in transmission lines.

These advantages, beside the challenges facing integrated inductors, have motivated the conduction of this research. That is to study how to enhance the performance of on-chip inductors by applying the Slow Wave techniques at least at the operating frequency and/or range of frequencies. Performance enhancement refer to the value of inductance, quality factor, size manipulation, self-resonance frequency, etc.

1.2 Thesis Objectives

This thesis aims at investigating the benefits of using slow wave transmission lines as on-chip inductors rather than using conventional spiral inductors. This is useful to efficiently use the assigned silicon area for low cost IC design. It is required to study in-depth the proportionality between the design parameters, like effective inductance (L_{eff}), peak quality factor (Q_{peak}), slow wave factor (SWF), self resonance frequency (f_{srf}), versus the physical dimensions of the slow wave transmission line (SWTL). Such a study can be leveraged to tune and optimize the properties of the inductance to meet specific requirements. In addition, the study is evaluating the use of SWTLs as inductors in injection-locked oscillators (ILO) as an example of a widely used circuit in reconfigurable RF front end. These objectives can be summarized as follows:

1. Understand the effect of SW techniques on the design parameters of integrated inductors.
2. Develop a scalable approach to optimize any arbitrary inductors for a desired frequency by changing its slow-wave periodic loading via the floating metal beneath.
3. Apply the developed method to experimentally validate integrated inductors on silicon substrate and the frequency scalability of the proposed approach.
4. Make use of the proposed technique to integrate SWTL inductors on injection-locked oscillators to demonstrate how the improved performance can translate to lower phase noise.

1.3 Thesis Contributions

Literature have shown possibility of using slow wave transmission lines as inductors, however this is lacking a scientific study to tune and optimize them as inductors on silicon substrate at specific frequencies. The contributions presented in this thesis are believed to be the first attempt at:

1. A thorough study to generate a parametric table to design SW structures as inductors which is useful to design on-chip inductors based on SWTLs with the ability to tune the effective inductance, peak quality factor to the desired frequency.
2. Based on the generated design table, two SWTLs as inductors are designed with 45% and 75% reduced length compared to conventional transmission lines (Publication in MWSCAS-2018 Eldahshan2018).
3. To demonstrate Q enhancement using SWTLs as inductors, two SWTLs are designed, based on the generated design table, with 75% and 60% enhanced Q compared to conventional single and double spiral inductors.
4. A novel technique to evaluate the performance of on-chip inductors by calculating their noise contribution to the circuit output. This technique do not require circuits enclosing the inductors to be fully optimized from the noise point of view.

1.4 Thesis Organization

After this introduction, Chapter 2 provides a thorough survey of on-chip inductors and slow-wave transmission lines either on-chip or on PCB. Various techniques are compared, leading to selecting the slow-wave technique applied in microwave components. In the same chapter, mathematical analysis of SWTLs as a periodic structures is introduced. Parametric analysis of SWTLs is introduced in Chapter 3. Additionally, primitive designed slow-wave structures are designed, fabricated and measured leading to validating the design. Chapter 4 introduces the design, simulation and measurement of injection-locked oscillator including conventional and optimized slow-wave transmission line inductors. Finally, the study is concluded in Chapter 5 along with a discussion of the results and future work.

Chapter 2

Background and Survey

2.1 Introduction

Lossy silicon substrate imposes constraints on inductors to perform efficiently. This requires more research to design on-chip inductors with custom requirements that optimize RF circuits at least at the operating frequency and/or range of frequencies.

In this chapter, various techniques reported to enhance on-chip inductors are surveyed. Slow wave transmission line (SWTL) is one candidate selected to be tested. Without changing its physical outline, SWTL provides the ability to tune its transmission-line parameters. This can be exploited to tune its inductive parameters (effective inductance (L_{eff}), peak quality factor (Q_{peak}) and self-resonance frequency (f_{srf})) to provide customized optimum design.

The inductive parameters for capacitive loaded SWTLs are derived theoretically based on classical and periodic-structure mathematical analysis. The effect of varying the capacitive loading on these design parameters is verified. Moreover, distributed capacitive loading is compared to lumped element loading.

Injection-locked oscillator (ILO) is a circuit level application selected to test the designed SWTLs as inductors. That requires illustrating the design steps for a generic ILO for completion.

2.1.1 Inductors in Modern Reconfigurable RF front-end

In modern reconfigurable RF front end circuits, inductors are playing an important role in improving the overall performance. In RF filters, inductors are the key components that facilitates the removal of the unwanted blockers within the operating bandwidth. Reconfigurability and flexibility are essential features required in modern communication standards. N-Path filter (NPF) is a good candidate for these requirements. The switching property of this filter provides a baseband filtering after down converting the RF signal then up-converting the filtered signal to the original band using the same set of switches resulting in a higher order bandpass filter [11,12].

Direct tunability with the Local Oscillator frequency, high quality factor, high linearity and scaling with the process are attractive features of N-path filters. This leads to extensive research during the last decade in enhancing, modeling and analyzing the performance of N-path filters [12] [13].

Inductors that are included in N-path filters have many benefits like reducing unwanted signal folding due to switching, improving the insertion loss and the out-of-band rejection [11] [13]. The inevitable shunt parasitic capacitance (due to transistor non-ideality) at the filter input can be absorbed by series inductors leading to lower in-band insertion loss [14] as shown in Figure 2.1. Additionally, the quality factor of inductors affects the level of filter's Noise Figure as shown in Figure 2.2. One approach is to design NPF without inductors; however, designers have to overcome the challenges discussed above.

Figure 2.1: Out-of-band rejection of an N-path filter without (dashed) and with (solid) series inductors at different resonance frequencies.

Inset: Chip micrograph [14].

Figure 2.2: NF variation with Q of the series inductors in N-Path filter [14].

Another useful RF component used in the RF front-end is the low-noise amplifier (LNA). Receiving the signals with the lowest possible Noise Figure is the main function of LNA. For example, in [15], a common gate LNA is loaded by LC tank circuit to improve common-mode rejection capability. The quality factor of inductors is useful for the receiver to switch between low band, mid band and high band operation with optimized noise performance. Tuning the L_{eff} and Q_{peak} without manipulating the inductor shape, while maintaining or enhance the overall performance can save more chip area.

Injection-Locked Oscillator (ILO) is another useful component in RF front-end used in modern communication transceivers. Its outstanding low phase noise performance, compared to free running oscillators, leads to its wide usage in modern transceivers [16–19]. ILO is a test circuit for this thesis as it performs a similar function to that of a synthesizer based on a phase-locked loop, but without the conventional components such as the dividers, phase detector and charge pump. Thus, potentially it realizes saving in dissipated power and integrated-circuit layout area. The ability to reduce the losses in the inductors (high Q) will be reflected on total phase noise enhancement.

The usefulness of inductors in the reconfigurable RF front end necessitates researching enhancement techniques for on-chip inductors.

2.2 On-Chip Inductor Enhancement Techniques

Techniques in literature to enhance on-chip inductors can be classified into various categories as shown in Figure 2.3.

Figure 2.3: Classification of inductors enhancement techniques.

Magnetic core inductors are filled with magnetic materials of high permeability which increases the inductance at DC and low frequencies. However, the challenge is to extend this inductance to higher frequencies (in the GHz range) while keeping the quality factor as high as possible. In [20], a comparison between several magnetic-core inductors (L_m) to their air-core equivalent (L_a) is introduced as shown in Figure 2.4. At low frequencies, magnetic core inductors enhanced the inductance by more than ten times compared to the air core inductors. This inductance enhancement comes at the expense of more losses. At relatively higher frequencies, the inductance of magnetic core inductors starts to decrease and the losses tend to be higher. Many inductor configurations are compared including spiral, racetrack, solenoid, and meander and they roughly follow the same trend. Therefore, a trade-off between peak quality factor, inductance enhancement, and the operating frequency exists for the magnetic core inductors.

Figure 2.4: Peak Q and Inductance (magnetic/air core) vs frequency for magnetic core inductors [20].

More studies have been conducted in this area [21] [22] [23]. In [21], an inductor was built with integrated vertical nano-particles forming a magnetic core on a 180 nm CMOS process. The inductor was realized in a VCO having $L=3$ nH, $Q=7$ at 1.7 GHz occupying an area of $280 \mu\text{m} \times 280 \mu\text{m}$. The on-wafer cross-section of the fabricated inductor is shown in Figure 2.5. Three inductors are compared in Figure 2.6. The first one (L_1 , red) is a traditional inductor without magnetic core having a size of $325 \mu\text{m} \times 325 \mu\text{m}$ to achieve $L=3$ nH and $Q=7.45$ at 1.7 GHz. The second inductor (L_2 , blue) is a smaller sized magnetic core inductor having a size of $280 \mu\text{m} \times 280 \mu\text{m}$. The last one (L_3 , black) is having the same layout as L_2 but without the ferrite. This study has shown that magnetic core inductors have a better performance at relatively lower frequencies. In [23] where a phase shifter is designed utilizing patterned magnetic core inductors and MIM caps. A common issues in the illustrated magnetic core examples is that the peak Q values exist at low operating frequencies. This is because of low self-resonance frequency of ferrites and low resistive (lossy) magnetic cores in addition

to the complexity of the ferrite preparation process.

Figure 2.5: The cross section of the implemented ferrite core inductor [21].

Figure 2.6: Inductance (a), and quality factor (b), of the magnetic core inductor.

Many post-processing techniques are applied to enhance the performance of on-chip inductors. For example, in [24], a wafer-level packaging technique is used where another metal layer is deposited on top of the passivation layer of the CMOS process. In this way, substrate effects and parasitic capacitances to ground are reduced resulting in implementing an inductor of 1.8 nH having a quality factor in the range of 40. Another example introduced in [25] where a post-processed inductor was tested after removing the substrate under it resulting in a suspended rectangular copper spiral inductor with an air-bridge as shown in Figure 2.7a. The inductor performance is enhanced as seen by the difference between the Q for both of the inductors with and without post-processing as shown in Figure 2.7b.

Either by removing the substrate under the inductor (suspended) or by depositing

Figure 2.7: Post processed inductor in [25], (a) Top and side views.
(b) Inductor performance.

another metal layers on top of the passivation layer, mechanical instability issues start to arise in addition to the high cost of the post-processing technique.

Modifying the ground plane of the inductors is another technique used to enhance the inductor performance. One method is to replace the ground plane with a periodic band gap (PBG) structure. In [26] and [27], a spiral inductor was implemented over a spiral-shaped PBG structure as shown in Figure 2.8a. Despite the slight enhancement in the quality factor, there was no increase in inductance and quality factor as seen in Figure 2.8 (b,c).

Another technique is introduced in [28] where a one-turn inductor is implemented over an artificial magnetic conductor (AMC) as shown in Figure 2.9a. The study has shown an enhanced inductance and quality factor on the PCB, however, on-wafer

Figure 2.8: Modified ground plane on-wafer inductor in [26] (a) Physical layout, (b) Inductance, (c) Quality factor.

performance degraded due to the generation of eddy currents on the AMC, as shown in Figure 2.9 (b,c).

In [29], helical inductors demonstrated lower area occupation. However, lower interconnect metal layers, and the highly resistive vias degraded the quality factor.

Table 2.1 summarizes the techniques used to increase inductance density, applications, technologies, and frequency ranges.

Ongoing research is being conducted to modify fabrication processes and enhance the conductivity of metal layers to reduce the loss resistance of the inductor as in [30].

One of the widely used techniques in enhancing transmission-line (TL) components

Figure 2.9: Artificial magnetic conductor plane for on-wafer inductor in [28]
(a) Physical layout, (b) Inductance, (c) Quality factor.

rely on the Slow Wave phenomenon. This technique is well matured analytically and has attracted much attention for their potential in building low loss transmission line based microwave components like filters, hybrid couplers and integrated waveguides. Therefore it is studied in the next section in an attempt to apply it to inductors.

Table 2.1: Enhancement techniques for on-chip Inductors.

No.	Technique	L (nH)	F (GHz)	Q_{peak}	Area or D_{out}^*	CMOS Tech.	Ref.
1	Magnetic core	3	1.36 - 1.86	16	$280 \times 280 \mu\text{m}^2$	180 nm	[21]
		14.5	2.2	<5	890 μm	custom	[22]
2	Helical Inductors	1.9	1 - 18	<10	$90 \times 90 \mu\text{m}^2$	180 nm	[29]
3	Post processing/ (MEMS)	1.8, 5	1 - 4	>25	220 μm	180 nm	[31]
	Post processing/ (Ferromagnetic core)	0 - 150	<1	<17	$50 \times 50 \mu\text{m}^2$		[32]
		1.8	2.8 - 18	>30	390 μm	90 nm	[24]
		0.038	<10	11	$4 \times 4 \mu\text{m}^2$		[33]
	Post processing/ (Suspension)	5	<10	<60	300 μm	CMOS compatible	[25]

* D_{out} is the outer diameter.

2.3 Slow Wave Transmission Lines

Slow Wave (SW) is a phenomenon defined as an electromagnetic wave propagating with a phase velocity lower than the speed of light [4]. This phenomenon is leveraged to implement low-loss transmission-line-based components like resonators, filters, dividers, couplers and antennas [34–36].

The idea behind the SW phenomenon is to store the electric and/or magnetic energies as much as possible in the guided wave media leading to slowing down the phase

velocity (V_p) [37]. For a plane wave propagating in a medium, a reduction in phase velocity results in a corresponding reduction in the guided wavelength (λ_g) which means a higher electrical length (βl) as follows [38]:

$$V_p = f \cdot \lambda_g = \frac{c_0}{\sqrt{\mu_r \cdot \epsilon_r}} \quad (2.1)$$

$$\beta l = 2\pi \frac{l}{\lambda_g} \quad (2.2)$$

where l is the physical length, c_0 is the velocity of the light in free space, ϵ_r and μ_r are the effective relative permittivity and permeability respectively. Slow wave factor (SWF) determines the ratio between the phase velocity of the wave in free space to that in the material and expressed as follows:

$$\text{SWF} = \frac{\beta}{k_0} = \frac{\lambda_0}{\lambda_g} \quad (2.3)$$

where, k_0 is the free space phase constant, and β is the material phase constant.

To further understand the SW phenomenon, introducing series L and/or shunt C sections (having a length much lower than λ_g) to a lossless transmission line results in a characteristic impedance and electrical length defined as follows:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \simeq \sqrt{\frac{L}{C}} \quad (2.4)$$

$$\theta = \beta l = \omega l \sqrt{LC} \quad (2.5)$$

$$V_p = \frac{\omega}{\beta} = \frac{\omega \lambda_g}{2\pi} \quad (2.6)$$

As a result, by introducing L and/or C sections (presuming that they are much shorter in length than the guided wavelength, λ_g) to the transmission line (of length l), it

acquires a higher electrical length (θ) and a fixed characteristic impedance (if L and C sections are added by the same ratio).

Many applications based on the Slow wave effect, fabricated on PCB and on wafer, are studied and summarized in Table 2.2 and Table 2.4 respectively.

Table 2.2: SW applications fabricated on PCB.

No.	Application	Frequency	References
1	Band Pass Filter	1-1.8 GHz	[6] [39]
		5-7 GHz	[40]
2	Hybrid Coupler	<3 GHz	[41] [37]
3	Substrate Integrated Waveguides	4-17 GHz	[36] [42]

Table 2.3: SW applications fabricated on wafer.

No.	Application	Technology	Frequency	References
1	Interconnect	CMOS 0.13 μm	20 - 70 GHz	[43]
		CMOS 0.25 μm	0 - 40 GHz	[44]
		BiCMOS 0.35 μm	>12 GHz	[45]
2	BPF	CMOS 65 nm	50 - 60 GHz	[46]
3	Resonator	CMOS 90 nm	60 GHz	[47]

It can be observed that the most widely used approach in building on-wafer Slow Wave Transmission Lines (SWTLs) is by using metallic rods under coplanar transmission lines. This configuration acts as a capacitive coupling of the signal terminal to the ground terminal of a transmission line as shown basically in Figure 2.10.

Figure 2.10: Equivalent circuit for capacitive loaded (C_{ls}) lossless transmission line.

Other than maximizing the Slow Wave Factor (SWF), the floating metallic rods are providing shielding for the line which minimizes the electric field linkage from the line to the lossy substrate [2].

Floating rods are more favorable than grounded ones for the following reasons. First, they do not need an explicit $0V$ ground reference [2]. Second, floating rods are not connected to each other, so isolation is improved between them. Finally, they cause less reduction in the self resonance frequency than that of the grounded rod. The rods are oriented orthogonal to the current flow to minimize the induced eddy currents. These design guidelines are considered in the following testing and implementation phases of SWTLs.

In the following section, SWTLs are analyzed using both classical microwave analysis and periodic structure analysis. It is required to find how the distributed implementation of SWTLs is providing advantages over lumped configuration.

2.4 Analysis of SW Transmission lines and Parameters Extraction

In this section, classical and periodic structure analysis are applied to study and understand the SW technique theoretically. Additionally, transmission line parameters (characteristic impedance, electrical length) are extracted from the simulated and/or measured S-parameters. From which, the effective inductance (L_{eff}), quality factor (Q) and self-resonance frequency (SRF) are determined.

2.4.1 Classical Analysis of SWTLs

A transmission line of length l , loaded by L and/or C sections (provided that they are much shorter in length than the guided wave length, λ_g), acquires a higher electrical length, θ , a slower phase speed, V_p , and a fixed characteristics impedance, Z_0 (if required). For TEM or quasi-TEM wave propagation in planar TLs, [4],

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \simeq \sqrt{\frac{L}{C}} \quad (2.7)$$

$$\theta = \beta l = \omega l \sqrt{LC} \quad (2.8)$$

$$V_p = \frac{\omega}{\beta} = \frac{\omega \lambda_g}{2\pi} \quad (2.9)$$

$$SWF(f) = \frac{\beta}{k_0} = \frac{\omega c}{V_p \omega} = \sqrt{\frac{\mu \epsilon}{\mu_0 \epsilon_0}} = \sqrt{\epsilon_r} \quad (2.10)$$

The proportionality between the signal speed and the guided wavelength (λ_g) is exploited to make compact transmission lines by slowing down the phase velocity and consequently maximizing the electrical length. Capacitive loaded transmission line is the technique used in this thesis and it is modeled as previously shown in Figure 2.10.

For a single conductor interconnect, the Telegrapher's equation is solved and the propagation constant and the characteristic impedance are determined as a function of transmission parameters from the ABCD matrix (S-parameters) of the interconnect as follows [48]:

$$A = D = \cosh(\gamma l) \quad (2.11)$$

$$B = Z_0 \sinh(\gamma l) \quad (2.12)$$

$$C = (Z_0)^{-1} \sinh(\gamma l) \quad (2.13)$$

from which [49], [50],

$$\gamma = \frac{\cosh^{-1} \frac{A+D}{2}}{l} = \alpha + j\beta \quad (2.14)$$

$$Z_0 = \sqrt{\frac{B}{C}} \quad (2.15)$$

where, γ is the propagation constant, l is the transmission line length, Z_0 is the characteristic impedance, α is the attenuation constant and β is the phase constant.

The input impedance of a shunt series two-port network terminated with a short circuit is determined as follows (Appendix C):

$$Z_{\text{in}} = \frac{1}{Y_{11}} = \frac{B}{D} \quad (2.16)$$

Consequently the transmission line effective inductance (L), quality factor (Q) and slow-wave factor (SWF) can be determined as follows [51].

$$L = \frac{Im(Z_{in})}{\omega} \quad (2.17)$$

$$Q = \frac{Im(Z_{in})}{Re(Z_{in})} \quad (2.18)$$

$$SWF = \frac{\beta}{k_0} = \frac{\beta c}{\omega} \quad (2.19)$$

For one-port transmission lines, L, Q are determined from S-parameters as follows [38]:

$$Z_{in} = Z_0 \frac{1 + S_{11}}{1 - S_{11}} \quad (2.20)$$

Then L and Q are determined using (2.17) and (2.18) respectively.

2.4.2 Periodic Structure Analysis of SWTLs

One way to form slow wave transmission lines is by periodically loading the conventional TL (host) with reactive elements (capacitive or inductive). In this study, capacitive loading is used to implement SWTLs. A uniformly shaped TL loaded with a uniformly distributed floating metallic rods can be represented by cascading infinite number of electrically small lumped-element unit cells [4, 38]. From the unit cell, four design parameters can be extracted; effective inductance (L), peak quality factor (Q_{peak}), self-resonance frequency (f_{srf}) and slow wave factor (SWF).

The lumped element unit cell of a general lossy transmission line is shown in Figure 2.11. R', G' are representing the per unit length series and shunt losses while L', C' are representing the per unit length series self inductance and the capacitance shunting the line, respectively.

Figure 2.11: Lumped-element unit cell of length (Δz) for a general unloaded transmission line.

The propagation constant (γ) and the characteristic impedance (Z_0) of this transmission line can be derived from the ABCD parameters (transmission parameters) of the unit cell as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{One unit cell}} = \begin{bmatrix} 1 & 0 \\ G + j\omega C & 1 \end{bmatrix} \cdot \begin{bmatrix} 1 & R + j\omega L \\ 0 & 1 \end{bmatrix} \quad (2.21)$$

$$= \begin{bmatrix} 1 & R + j\omega L \\ G + j\omega C & 1 + (R + j\omega L)(G + j\omega C) \end{bmatrix} \quad (2.22)$$

Where, $R = R'\Delta z$, $L = L'\Delta z$, $G = G'\Delta z$, $C = C'\Delta z$.

For N unit cells, the total transmission parameters are:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{tot.}} = \prod_{i=1}^N \begin{bmatrix} A_i & B_i \\ C_i & D_i \end{bmatrix} = \begin{bmatrix} A_i & B_i \\ C_i & D_i \end{bmatrix}^N \quad (2.23)$$

The propagation constant (γ) and the Bloch impedance (Z_B) can be determined as follows: [38]:

$$\gamma = \alpha + j\beta = \ln\left(\frac{A + D \pm \sqrt{(A + D)^2 - 4(AD - BC)}}{2}\right) * \frac{1}{\Delta z} \quad (2.24)$$

$$Z_B = \frac{-2B}{(A - D) - \sqrt{(A + D)^2 - 4}} \quad (2.25)$$

The effective inductance (L_{eff}) and quality factor (Q) for this line are determined by grounding port 2 (short circuit) as in (2.17), (2.18) while considering Z_{in} as follows:

$$Z_{in} = \frac{B}{D} \quad (2.26)$$

Where ABCD are the total transmission parameters of the cascaded N unit cells determined from (2.23) and Z_{in} is the input impedance looking from port 1 while port 2 is shorted to ground.

To show the benefits of representing the TL as inductor using distributed multiple unit cells instead of a single unit cell, a numerical example is considered. Refer to the TL model illustrated in Figure 2.11. Assume a TL of $L = 1$ nH is required to be implemented on CMOS 130 nm process. In this process, the top layer is having a sheet resistance ($R_{\square}$) around $0.007 \Omega/\square$. A line of length 1 mm, and a width of $10 \mu\text{m}$ has a total series resistance of about 1Ω ($R = R_{\square} \times \frac{L}{W}$). The total shunt capacitance to the substrate is assumed to be $C = 1$ pF. For simplicity, it is assumed that the shunt conductance $G = 0$. The line inductance, L, and quality factor, Q, are determined for 1, 5 and 100 unit cells representing the same TL as shown in Figure 2.12 and Figure 2.13 respectively. Compared to a single capacitive loading, distributed loading provides an enhanced inductor performance of higher Q and f_{srf} .

Table 2.4: Components values of TL model represented by 1, 5, and 100 unit cells, assumed $G=0$. (refer to Figure 2.11).

No. of unit cells	Δz (mm)	R/cell (Ω) ($R=R' \times \Delta z$)	L/cell (nH) ($L=L' \times \Delta z$)	C/cell (pF) ($C=C' \times \Delta z$)
1	1	1	1	1
5	0.2	0.2	0.2	0.2
100	0.01	0.01	0.01	0.01

Figure 2.12: Effective inductance of TL represented by one versus multiple unit cells.

Figure 2.13: Quality factor of TL represented by one versus multiple unit cells.

Capacitive loaded TL can be analyzed by splitting the unit cell of a conventional TL into two portions each of length $\Delta z/2$ and inserting the per-unit-cell shunt capacitive loading in the middle as shown in Figure 2.14 [38].

Figure 2.14: Lumped element unit cell for capacitive loaded transmission line.

The equivalent transmission matrix (ABCD parameters) defining the unit cell of the SWTL is determined by cascading half TL section, shunt loading section and the other half TL section as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{SWTL}} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{section 1}} \begin{bmatrix} 1 & 0 \\ j\omega C_{\text{load}} & 1 \end{bmatrix} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{section 2}} \quad (2.27)$$

$$= \begin{bmatrix} A^2 + j\omega C_{\text{load}} AB + BC & AB + j\omega C_{\text{load}} B^2 + BD \\ AC + j\omega C_{\text{load}} AD + CD & BC + j\omega C_{\text{load}} BD + D^2 \end{bmatrix} \quad (2.28)$$

Where the transmission parameters of each TL section,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{section 1/2}} = \begin{bmatrix} 1 & \frac{R+j\omega L}{2} \\ \frac{G+j\omega C}{2} & 1 + \frac{(R+j\omega L)(G+j\omega C)}{4} \end{bmatrix} \quad (2.29)$$

The SWTL unit cell is still reciprocal network ($AD-BC=1$). In this case, γ and Z_B are determined from (2.24) and (2.25) respectively. Similarly, L and Q for this SWTL are function of the loading capacitance C_{load} and can be determined from (2.17), (2.18) respectively while considering Z_{in} as in (2.26).

To investigate the effect of varying the capacitive loading (C_{load}) of SWTL on its effective inductance, quality factor, self-resonance frequency, the case study of the on-chip transmission line discussed before is considered. In this case, the number of cells are kept constant (5 unit cells) while testing two loading capacitance (500 fF and 1000 fF).

Substituting in (2.27) - (2.29), while varying C_{load} over the frequency range 1-20 GHz, L_{eff} , Q and f_{srf} are shown in Figure 2.15. Varying C_{load} can potentially tune the effective inductance of the SWTL. The price payed for this tuning is lower Q (Figure 2.16) which can be recovered by distributing the capacitive loading over the TL to provide better Q and higher f_{srf} as discussed in Figure 2.13.

Figure 2.15: Effective inductance of SWTL as inductor with two different capacitive loading distributed on 5 unit cells. Lower f_{srf} is observed by increasing C_{load} .

Figure 2.16: Quality factor of SWTL as inductor with two different capacitive loading distributed on 5 unit cells. Lower f_{srf} is observed by increasing C_{load} .

This verifies that the SWTLs' nature facilitates distributed capacitive loading; a preferable feature required by on-chip inductors to achieve tunability without sacrificing much losses compared to lumped element loading. This is provided without changing the TL footprint which leads to saving more area.

2.5 Injection Locked Oscillator design

The injection locked oscillator (ILO) is a widely used RF circuit in modern reconfigurable transceivers. It is included in many applications, for example, phase shifters [52], signal modulation conversion [53], frequency dividers [54] [55], PLL [56] and frequency synthesizers [57]. This circuit is selected to test the SW transmission line inductors. This section illustrates the design steps for ILO used in this thesis.

Detailed design and analysis for this kind of oscillators and other topologies can be found in [58].

Injection locking is a technique forcing the oscillator phase/frequency, ω_0 , to follow a reference frequency, ω_{inj} , and this leads to attenuating phase-noise effects [59] as long as ω_{inj} is within the locking range, ω_L .

The ILO consists of two main parts; the oscillator core and the injection amplifiers. A differential topology is selected for the core due to its immunity to common mode noise. The oscillator core consists of the tank circuit and the negative resistance formed from two NMOS cross-coupled transistors ($-g_m$ transistors). The circuit diagram for the tank circuit is shown in Figure 2.17. The second part is the differential amplifier in which the injected signal is applied having a specific frequency and amplitude to achieve the required locking range. The ILO schematic without biasing is shown in Figure 2.18.

Figure 2.17: Oscillator tank circuit.

The condition to start oscillation is defined as follows:

$$g_m > \frac{2}{R_{Tank}} \quad (2.30)$$

Figure 2.18: Oscillator circuit diagram without the biasing. T_1, T_2 are the $-g_m$ transistors, T_3, T_4 are the injection transistors and T_5, T_6 are the buffer transistors.

where g_m is the transconductance of the cross coupled transistors, R_{Tank} represents the losses in the tank circuit due to finite quality factor (Q_{Tank}) of L_{Tank} and C_{Tank} shown in Figure 2.17.

Since the tank circuit is in parallel configuration R_{Tank} can be calculated as follows:

$$\frac{1}{R_{Tank}} = \frac{1}{R_L} + \frac{1}{R_C} \quad (2.31)$$

$$\therefore \frac{1}{R_{Tank}} = \frac{1}{Q_L \omega_0 L} + \frac{\omega_0 C}{Q_C} \quad (2.32)$$

$$\therefore R_{Tank} = \frac{1}{\frac{1}{Q_L \omega_0 L} + \frac{\omega_0 C}{Q_C}} \quad (2.33)$$

where, R_L and R_C are the equivalent shunt resistive losses for the tank inductor

(L_{Tank}) and capacitor (C_{Tank}) respectively.

Given the total inductance (L_{Tank}) and the operating frequency ω_0 , the total capacitance can be determined as follows:

$$C_{Tank} = \frac{1}{\omega_0^2 \times L_{Tank}} \quad (2.34)$$

As shown in Figure 2.18, the buffer, having a high resistance, is adding minimal resistive loading to the core oscillator. Therefore the total resonator resistance $R_{tot} \approx R_{Tank}$.

The peak voltage swing over the tank circuit, V_{tank} , can be determined as follows:

$$V_{Tank} = \frac{2}{\pi} \cdot I_{bias} \cdot R_{Tank} \quad (2.35)$$

where I_{bias} is the total bias current of the $-g_m$ transistors plus current through the injection transistors.

The lock range, ω_L , is the range of frequencies allowed for the injected signal, ω_{inj} , to change with respect to the oscillator frequency, ω_0 , while keeping the locking condition. It can be shown that the ILO locks if ω_{inj} is in the range $(\omega_0 \pm \omega_L)$ [59]

$$\omega_L = \omega_0 - \omega_{inj} = \frac{\omega_0}{2Q_{Tank}} \cdot \frac{I_{inj}}{I_{osc}} \cdot \frac{1}{\sqrt{1 - \frac{I_{inj}^2}{I_{osc}^2}}} \quad (2.36)$$

$$\therefore 2 \cdot \frac{Q_{Tank} \cdot \omega_L}{\omega_0} = \frac{I_{inj}}{I_{osc}} \cdot \frac{1}{\sqrt{1 - \frac{I_{inj}^2}{I_{osc}^2}}} \quad (2.37)$$

where $I_{osc} = I_{inj} + I_{tank}$.

Substituting $\alpha = \frac{I_{inj}}{I_{osc}}$ and $\beta = \frac{Q_{Tank}\omega_L}{\omega_0}$ in (2.37), α can be determined as follows

$$2 \cdot \beta = \alpha \cdot \frac{1}{\sqrt{1 - \alpha^2}} \quad (2.38)$$

from which the ILO lock range can be determined from (2.36).

Finally, the Phase Noise of the free running oscillator can be estimated as follows [58]:

$$PN = \left(\frac{\sqrt{2} \times \omega_0}{2Q_{Tank} \Delta \omega} \right)^2 \cdot \left(\frac{FkT}{2P_s} \right) \quad (2.39)$$

where $\Delta\omega$ is the frequency offset from the carrier frequency, F is the active devices noise figure, k is Boltzmann constant, T is the temperature in Kelvin, and P_s is the carrier power determined as follows:

$$P_s = \frac{(V_{Tank})_{peak}^2}{2 \cdot R_{Tank}} \quad (2.40)$$

2.6 Conclusion

The usefulness of on-chip inductors in modern RF reconfigurable applications like N-path filters, Low-Noise Amplifiers and Injection Locked Oscillators have been introduced. Reconfigurability and design flexibility are major requirements in these applications. Implemented on lossy silicon substrates, inductors need more research to enhance their performance and achieve tunability to be compatible with modern RF applications.

Several enhancement techniques for integrated inductors were surveyed and classified. Magnetic core inductors have the advantage of high inductance density; however, this is not suitable for applications operating at high RF frequencies due to the low self-resonance frequency of ferrites. The post-processing techniques enhance the inductor performance, but this came at the expense of high cost and mechanical instability issues. Modifying the ground plane of the inductor has the drawback of induced eddy currents which degrade its performance. Helical inductors have shown lower area occupation, but the high resistance of the lower metal layers maximizes the resistive losses.

One widely used technique in transmission-line based microwave components is Slow Wave (SW). SW technique has shown the ability to build compact sized integrated passive components, and this was demonstrated in literature within different applications like interconnects, bandpass filters and resonators. Slow wave transmission lines (SWTLs) are used as inductors in some reported applications. However, literature is lacking a comprehensive study to exploit more advantages of these TLs as inductors in RF applications. In this chapter, SW technique has been surveyed and thoroughly studied to be verified in transmission line on-chip inductors.

Classical and periodic structure analysis for two-port SWTLs are introduced to study and understand the SW technique theoretically. The transmission line parameters (characteristic impedance (Z_0), electrical length (θ)) are extracted from the simulated and/or measured transmission (ABCD) parameters. The input impedance (looking from port-1 and shunting port-2) is determined, from which the effective inductance (L_{eff}), quality factor (Q), self-resonance frequency (f_{srf}) were derived. Periodic structure analysis have proved that distributed nature of SWTLs have provided the tunability feature to on-chip inductors without sacrificing much Q and f_{srf} compared to lumped capacitive loading to conventional transmission lines. These results are verified in two case studies considering practical on-chip values.

One technique to implement SWTLs is by applying metallic rods under the transmission line which couples the signal terminal to the ground terminal. In the next chapter, various coplanar SWTL configurations implemented on different metal layers on CMOS 130nm technology are tested. Variation of the effective inductance and quality factor of SWTLs with the physical dimensions needs to be studied as well.

As a test circuit, injection locked oscillator (ILO) is selected to test the SWTL inductors. For completion, the detailed design equations for a generic ILO were introduced.

Chapter 3

Testing and Verification of Slow Wave Inductors

3.1 Introduction

Studying the approaches in literature that enhanced the performance of on-chip inductors, paved the way to tackle the gaps that require more research and analysis. This chapter studies how to steer the advantages provided by slow wave transmission lines (SWTLs) to overcome these gaps.

Capacitive loaded coplanar microstrip TL using floating metallic rods is the SW configuration selected to be applied. Eight design variables, related to the physical shape of the SWTL, are analyzed to monitor the inductor performance. The eight design variables are classified into two classes; four variables related to the TL terminal and four variables related to the floating metallic rods. This parametric analysis aims at determining the factors that enhance slow wave transmission lines (SWTLs) when used as inductors. Three case studies are designed and compared to examine the design flexibility provided by SWTL inductors.

To validate the idea practically, eight different shapes of TLs are fabricated and measured on CMOS 130nm technology to determine the most suitable design achieving optimized inductors considering the allowed design rules dictated by the process.

3.2 Parametric Analysis of SW Transmission Lines

Capacitive loading is the selected technique to form SWTLs in this study. A typical capacitive loaded SWTL consists of the transmission line underlined by a floating metallic rods which couples the signal terminal to the ground terminal [2] [43]- [45]. A coplanar microstrip transmission line (signal-ground terminals) is selected instead of coplanar line (ground-signal-ground terminals) due to its smaller footprint on the substrate [60]. The cross section and side views of the transmission line over the back-end-of-line (BEOL) in CMOS 130nm node are shown in Figure 3.1. The transmission line terminals are occupying the uppermost metal layer while the floating rods are occupying the second metal layer from the top.

In this section, parametric analysis is applied on this SWTL configuration for eight design variables (refer to Figure 3.1); four related to the TL terminal (width, w_B , length, l_B , thickness, h_B , and terminal-terminal separation, s_B), and four related to the metallic rods underneath the line (length, l_R , thickness, h_R , rod-rod separation, s_R , and rod-terminal separation, s_{BR}).

Figure 3.1: On-wafer coplanar microstrip TL with metallic rods underneath on Si substrate including the eight design variables, (a) Cross section, (b) Side view.

s_R , and rod-terminal separation, s_{BR}). This parametric analysis completes the reported studies which are dedicated for two design variables (s_B , w_B) vs two design parameters (L_{eff} , Q) [61, 62].

The dependence of the TL parameters (effective inductance (L_{eff}), quality factor (Q), electrical length (βl), characteristic impedance (Z_0), and self-resonance frequency (f_{srf})) on the spatial dimensions of the SWTL (design variables) are explored systematically. TL parameters are extracted from the two port ABCD parameters based on the analysis introduced previously in Section 2.4 (Eqns. 2.14 - 2.18).

A design space is generated for each design variable ranging between arbitrary maximum and minimum limits (considering the fabrication constraints of the technology used in the consequent design phases) while keeping the other design variables at their nominal values and observe how this is affecting the TL parameters. For example, when changing the line terminal width, w_B , between 5-40 μm , the other variables are kept at their nominal values. The objective of this methodology is to determine how changing each variable is affecting the TL parameters L_{eff} , Q_{peak} , βl , Z_0 and f_{srf} of the SWTL.

Nominal dimensions are selected for each design variable to be convenient with the process design rules. The coplanar microstrip line length, l_B , is arbitrarily selected to be 755 μm which is equivalent to the perimeter of the one-turn kit inductor used in the fabrication process. The layer thickness in the process dictated each of the thickness of the terminal (h_B), the thickness of the rods (h_R), terminal-rods separation (s_{BR}), the length and rod-rod separation. The characteristic impedance is not restricted to 50 Ω , therefore, w_B and s_B are selected arbitrarily.

The transmission-line parameters (γ , Z_0) are calculated from the two-port S-parameters of the simulated SWTL using a 3D Finite Difference Time Domain numerical simulation tool (HFSS [63]) over a frequency range from 1-50 GHz at the dimensions referred in Table 3.1. It is assumed that the line is inserted in a SiO_2 dielectric layer having a thickness of 25 μm grown over silicon substrate thick layer (300 μm), refer to Figure 3.1. The transmission lines and the rods are made from copper ($\sigma = 2.5 \times 10^7$ [S/m]), while the material of the dielectric separating the lines is silicon dioxide (SiO_2) having a thickness of 25 μm grown over silicon substrate ($\rho_{Si} = 1.5$ [Ω - cm]). The design space for each design variable is summarized in Table 3.1.

Table 3.1: Design space of the SWTL variables (all in μm). Refer to Figure 3.1.

Variable	w_B	l_B	s_B	h_B	s_{BR}	h_R	l_R	s_R
Min.	5	188	2.5	1	1	0.75	0.3	0.5
Nom.	20	755	10	4	4	3	1.5	2
Max.	40	1510	40	10	10	8	6	8

One simulation phase of the SWTL having all-nominal values is shown in Figure 3.2. Except for $Q_{peak_{nom}}$ and SRF_{nom} , the values of the transmission line parameters at 10 GHz are of interest (L_{nom} , βl_{nom} , and $Z_{0_{nom}}$). This case is considered as the reference case and all the TL parameters are normalized to it. For example, the normalized effective inductance, $L' = L/L_{nom}$.

Figure 3.2: TL parameters at the nominal TL dimensions.

Sweeping the terminal width, w_B , the TL parameters are determined without (case(a)) and with the rods (case (b)) as shown in Figure 3.3. In general, the effective inductance in case (b) is higher by 10% compared to case (a). The proportionality of w_B with the TL parameters is the same in both cases except for Q_{peak} and βl . In the presence of the rods, varying w_B causes a minor effect on Q_{peak} . On the other hand, βl is sensitive to the variation of w_B in the presence of the rods due to the higher coupling capacitance between the line and the rods.

The next variable to be investigated is the line length, l_B . The two cases of the TL without and with the rods are compared in Figure 3.4. In both cases, the effective inductance and the electrical length are proportional to l_B . Minimizing l_B is more beneficial from the Q_{peak} point of view. As expected, changing the line length have a minor effect on Z_0 in both cases.

Figure 3.3: Normalized TL parameters variation with the line terminal width, w_B , (a) Without the rods, (b) With the rods.

Figure 3.4: Normalized TL parameters variation with the line length, l_B , (a) Without the rods, (b) With the rods.

The third variable to be investigated, shown in Figure 3.5, is the lateral separation between the line terminals, s_B . In case (a), the proportionality between s_B and Z_0 while βl and SRF are not sensitive, gave the advantage of increasing L and Q_{peak} . In case (b), adding the rods causes βl to be proportional to s_B variation and this leads to higher effective inductance but lower Q_{peak} .

Figure 3.5: Normalized TL parameters variation with the line terminals separation, s_B , (a) Without the rods, (b) With the rods.

The fourth variable to be investigated is the thickness of the TL, h_B , is illustrated in Figure 3.6. In case (a), there is an optimum value for h_B at which Q_{peak} is maximum. This is because increasing the thickness provides a higher capacitive coupling between the line terminals leading to lower Q_{peak} . Increasing the thickness of the TL in case (b) provides higher electrical length compared to case (a). This is translated to a higher effective inductance. Case (b) is showing proportionality between Q_{peak} and the thickness, but the effective inductance is not.

Figure 3.6: Normalized TL parameters variation with the line thickness, h_B , (a) Without the rods, (b) With the rods.

To summarize, comparing the two cases of the transmission lines, without and with the rods, have shown that inserting the floating metallic rods under the TL have provided a tunability to the effective inductance at 10 GHz. According to βl and Z_0 steepness (whichever is dominant), the effective inductance will be affected proportionally. This came at the expense of lower quality factor and self resonance frequency.

The next step is to study the other four design parameters related to the rods on the TL parameters. Referring to Figure 3.1, the four design variables to be discussed are the vertical spacing between the line and the rods, s_{BR} , the thickness of the rods, h_R , the longitudinal length of the rods, l_R , and the longitudinal spacing between the rods, s_R . Figure 3.7 shows the effect of the four variables on the TL parameters normalized

to the nominal values.

Figure 3.7: Effect of varying rods dimensions on TL parameters, (a) s_{BR} , vertical spacing between the line and the rods, (b) h_R , thickness of the rods, (c) l_R , longitudinal length of the rods, (d) s_R , longitudinal spacing between the rods.

In general the design variables related to the rods have minimal effect on the line effective inductance to a certain extent. In contrast, the quality factor is sensitive to that variation.

Figure 3.7a is showing that a reduction in line-to-rod separation, s_{BR} , tends to maximize the electrical length and the effective inductance of the TL. This is associated with lower Q , Z_0 and f_{srf} .

Using thinner floating rods (low h_R), Q can be recovered back without affecting the

other parameters as shown in Figure 3.7b. This is because thin floating rods tends to resist the generated eddy currents. However, this is not practical due to the dedicated layer thickness of the technology.

The same Q enhancement can be achieved by increasing rod-to-rod separation (s_R), without the effective inductance being changed as shown in Figure 3.7d. It is worth mentioning that, in this parametric study, decreasing s_R and/or l_R is associated with increasing the number of rods below the line leading to higher coupling capacitance between the line terminals. This explains the Q degradation with a lower s_R and/or l_R . Varying the longitudinal length of the rods, l_R , has shown that there is an optimal length at which peak Q is the highest as shown in Figure 3.7c.

To summarize, the previous parametric analysis has shown how the effective inductance and quality factor are proportional to the design variables of a SWTL without and with the floating metallic rods. The effect of varying the rod-rod (horizontal), and the line-rod (vertical) separation on the TL parameters are presented. These results are summarized in Table 3.2 indicating the relation between the design variables and the TL parameters. This analysis potentially clarifies which design variable is more effective than the other on the inductor performance and provides a parametric design-table that links TL parameters to the spacial dimensions of SWTL.

Table 3.2: Parametric design table linking TL parameters to the spacial dimensions of TL and rods. ($\propto$) = Increases with, and ($1/\propto$) = Decreases with).
Case (a)= Without rods, Case (b)= With rods.

Variable	w_B		l_B		s_B		h_B		s_{BR}	h_R	l_R	s_R
Case	(a)	(b)	(a)	(b)	(a)	(b)	(a)	(b)	(b)	(b)	(b)	(b)
L	$\frac{1}{\propto}$	$\frac{1}{\propto}$	$\propto$	$\propto$	$\propto$	$\propto$	opt*	$\frac{1}{\propto}$	$\frac{1}{\propto}$	–	$\frac{1}{\propto}$	–
Q_{peak}	$\propto$	–	$\frac{1}{\propto}$	$\frac{1}{\propto}$	$\propto$	$\propto$	opt*	$\propto$	$\propto$	$\frac{1}{\propto}$	opt*	$\propto$
βl	–	$\propto$	$\propto$	$\propto$	–	$\propto$	$\propto$	–	$\frac{1}{\propto}$	–	–	$\frac{1}{\propto}$
Z_0	$\frac{1}{\propto}$	$\frac{1}{\propto}$	–	–	$\propto$	$\propto$	opt*	$\frac{1}{\propto}$	$\propto$	–	–	$\propto$
f_{srf}	$\frac{1}{\propto}$	$\frac{1}{\propto}$	$\frac{1}{\propto}$	$\frac{1}{\propto}$	–	$\frac{1}{\propto}$	$\frac{1}{\propto}$	–	$\propto$	–	$\propto$	$\propto$

– Minor change

*Optimum at some point

3.3 Case Studies

In this section, three case-studies are introduced to demonstrate the advantages of using SWTL as inductors. The three transmission lines are designed based on the parametric table introduced in the previous section as a design guide tool. The effective inductance (L_{eff}), characteristic impedance (Z_0) and electrical length (βl) of the three lines are kept constant while the physical shape of each inductor is being modified. This is crucial in saving chip area (consequently the cost) for the circuits using on-chip inductors.

The three lines are common in the terminal width (w_B), thickness (h_B) and rods thickness (h_R). The dimensions are selected to be compatible with the fabrication design rules dictated by the foundry. Consequently, optimum performance discussed in Section 3.2 can not be achieved. Nevertheless, this will not affect the ultimate goal of comparison. The lines are simulated using a 3D Finite Difference Time Domain numerical simulator (HFSS). Figure 3.8 depicts the three designed TL configurations with their cross section at the figure inset. Table 3.3 summarizes the final dimensions and the design procedure is discussed throughout this section.

Figure 3.8: Length comparison of the three TL configurations having constant L , Z_0 and θ . (a) Conventional line of length 755 μm , (b) SW transmission line of length 340 μm , (c) SW transmission line of length 200 μm .

Inset: Cross section of the SW transmission lines

Table 3.3: Design variables used in SW transmission lines optimization (all in μm).

Parameter	Case	w_B	l_B	s_B	h_B	s_{BR}	h_R	l_R	s_R
Value	(a)	20	755	10	4	—	—	—	—
	(b)	20	340	40	4	2	3	1	2
	(c)	20	200	160	4	1	3	0.75	2.25

The first case is a coplanar microstrip TL without rods and it is considered as a reference case to be compared with the other two SWTLs. The length of TL is selected to be 755 μm which is equivalent to the perimeter of the one-turn design kit inductor. The separation between the line terminals and terminal width (s_B , w_B) are arbitrarily selected to achieve an effective inductance per unit length (L') of 0.45 [pH/ μm] ($L=340$ pH, Z_0 of 65 Ω and θ of 18° at 10 GHz).

The addition of the rods under the line leads to reduction of the characteristic impedance (Z_0) and maximization of the electrical length (βl) simultaneously, as expected in Section 3.2. To equalize Z_0 back, three options are available; decreasing w_B , decreasing h_B , or increasing s_B (refer to Table 3.2). Maximizing s_B option is selected because it leads to an enhanced Q with a slight decrease in the SRF. To equalize βl back, either w_B or l_B can be reduced. Reducing l_B option is selected because it does not affect the previously adjusted Z_0 with an increased Q and SRF (Figure 3.4). However, reducing w_B will further increase Z_0 requiring a system re-adjustment (Figure 3.3). The resultant line configuration is line (b) in Figure 3.8. As shown, a length reduction of 45% is achieved. Moreover, the total line area is reduced by 28%. This length reduction with the same effective inductance leads to an increase in the effective inductance per unit length (L') to 1 [pH/ μm].

Further manipulation can be achieved to reduce the physical length (if required) while keeping L , βl and Z_0 the same. s_{BR} can be minimized (Figure 3.7a) following the same procedure applied on line (b) to equalize the TL parameters. This resulted in line (c) configuration shown in Figure 3.8. A 73% reduction in the line length is achieved in this case with a slight increase in the line area by 6%. The effective inductance per unit length (L') in this case has reached 1.7 [pH/ μm].

Based on the calculations in Section 2.4 the SWF for the three cases are determined

from their S-parameters and compared in Figure 3.9a. As shown, the SWF is increased by two times for case (b) and by four times for case (c). From the effective inductance density and loss point of view, an enhancement is achieved for the SW transmission lines as shown in Figure 3.9b due to the achieved length reduction as expected in Figure 3.4b.

In summary, the three introduced transmission lines are having different configurations and achieving the same L , Z_0 and θ . The three case studies are showing the design flexibility provided by using SWTL as inductors where the effective inductance per unit length can be increased up to three times its original value. Based on the chip area and the arrangement of the electronic components, the optimum inductor shape can be selected.

Figure 3.9: Regular coplanar line and the SW transmission lines comparison
 (a) Slow wave factor (b) Effective inductance/ μm and Quality factor.
 (Cases defined in Figure 3.8).

3.4 Fabrication and Measurement of SWTL

Inductors

After investigating the SW transmission lines as inductors theoretically, it is of paramount importance to complete the design cycle through fabrication and measurements. The constraints imposed by the process might hinder achieving the optimum performance, but it is sufficient for the proof-of-concept.

In this section, eight transmission lines are fabricated in CMOS 130nm process. The cross section of the back-end-of-line (BEOL) is shown in Figure 3.10. This node is a commercial eight layer process divided into three portions according to the metal thickness. Mostly inductors are implemented on the top portion (Top, M8, and M7 layers) because it contains the thickest metal layers (4 μm) and consequently the lowest resistive losses. The middle portion (M6 and M5) includes two layers having a thickness of about one eighth that of the top metal layer. They have the advantage of a small vertical separation which is exploited to implement closely separated rods to the TL terminals. The last portion (M1-M3 in Figure 3.10) includes the low metal layers used for transistors connections and no inductors are implemented on these layers due to their relative tiny thickness and their closeness to the substrate (low Q).

The implemented TLs can be categorized into two groups; two-port and one-port configuration. The detailed design, simulation, and measurement for each transmission line inductor is introduced. Four de-embedding structures are included as well on the same chip. The twelve structures (eight transmission lines and four de-embedding structures) are confined on a wafer area of $2.25 \times 1 \text{ mm}^2$. A screen capture of the final layout of the designed chip is shown in Figure 3.11.

Figure 3.10: BEOL cross section for 130nm CMOS process.

Each number shown in Figure 3.11 is used throughout the chapter to refer to a TL configuration. The shapes numbered (1, 4, 5 and 8) are the one-port transmission lines, the shapes numbered (2, 3, 6 and 7) are the two-port transmission lines, and the shapes numbered (9, 10, 11 and 12) are the de-embedding structures. A photograph of the fabricated chip is shown in Figure 3.12.

Figure 3.11: Screen capture of the chip layout. (Area= $2.25 \times 1 \text{ mm}^2$).

Figure 3.12: Fabricated chip micrograph. (Area= $2.25 \times 1 \text{ mm}^2$).

The selected dimensions for fabrication are decided so that more test shapes can be enclosed within the dedicated chip area. For this reason, all the fabricated transmission lines in this chip have a common configuration with a length of $755 \text{ }\mu\text{m}$ and a total width of $50 \text{ }\mu\text{m}$.

The transmission lines are simulated using the electromagnetic simulator EMX; a numerical solver compatible with Cadence based on Method of Moment [64].

Considering the fabrication features associated with the CMOS process, the material properties introduced in Table 3.4 are accounted for in the simulation.

Measurements are applied using a vector network analyzer (Agilent 8720ES) over the frequency range from 0.5 to 20 GHz. It was calibrated using Short, Open, Load, and Through (SOLT) calibration method to the Ground Signal Ground (GSG) probe tips ($150 \text{ }\mu\text{m}$ pitch) utilizing a ceramic Impedance Standard Substrate (GGB CS-5), Figure 3.13. Therefore, the need for de-embedding structures arises to remove the parasitic effects of the probe pads and their interconnects from the measurement results achieving calibration to the structures input/output ports.

Table 3.4: Material properties used in EMX simulation tool.

Index	Parameter	Symbol	Value	Range
1	Silicon substrate resistivity	$\rho_{Si} [\Omega - cm]$	1.5	1 - 2
2	Silicon dioxide tangential loss	$\tan\delta_{SiO_2}$	0.001	0.00-0.001
3	Sheet Resistance for Upper metal*	$R_{\square Up} [\Omega/\square]$	0.01	0.007 ± 0.0014
	Upper metal Conductivity***	$\sigma_{Up} [S/m]$	2.5×10^7	
4	Sheet Resistance for Lower metal**	$R_{\square Lo} [\Omega/\square]$	0.0649	0.0339 ± 0.0068
	Lower metal Conductivity***	$\sigma_{Lo} [S/m]$	2.8×10^7	

*Thickness(T)=4 $[\mu m]$

**Thickness(T)=0.55 $[\mu m]$

*** $\sigma = 1/\rho [S/m]$, $\rho = R_{\square} \times T [\Omega.m]$

(a)

(b)

Figure 3.13: Measurement setup for selected shapes (a) Shape #5, (b) Shape #7.

3.4.1 De-embedding Structures

The de-embedding structures (numbered 9, 10, 11 and 12 in Figure 3.11) are one-port networks which are suitable for de-embedding one-port transmission lines. Due to the

symmetry of the two port transmission lines, two port de-embedding is derived from the one port as detailed in Appendix B.

According to the de-embedding method used (SOLT), the de-embedding structures built are Open and Short configurations. One of the designed shapes on the chip (Shape #1 in Figure 3.11) has a different layout for its input terminals compared to the remaining shapes. An extension is needed in the de-embedding structure to fit this input port. Therefore, its own de-embedding structures are built as shown in Figure 3.14. The remaining shapes are de-embedded using the structures shown in Figure 3.15. The ground pad is shared throughout the structures.

Figure 3.14: Deembedding structures for Shape #1, (a) Open (Shape #9), (b) Short (Shape #10).

Figure 3.15: Deembedding structures for the rest of the shapes, (a) Open (Shape #11), (b) Short (Shape #12).

To test how the simulated S-parameters of the de-embedding structures are matched to that measured, they are compared in Figure 3.16 and Figure 3.17. As shown, the simulated and measured S-parameters are matched within 10% up to 20 GHz.

(a)

(b)

Figure 3.16: Simulated vs measured S-parameters for the Shapes (a) #9 and (b) #10.

(a)

(b)

Figure 3.17: Simulated vs measured S-parameters for Shapes (a) #11 and (b) #12.

3.4.2 Shape #1 (Kit Inductor)

The chip includes one of the kit inductors to be compared with the designed SWTL inductors. This is a one turn inductor, shown in Figure 3.18, with an estimated

inductance of 465 pH. It is a parallel inductor implemented on the last two metal layers (Top, M8 layers in Figure 3.10) having an outer diameter of 200 μm with metal width of 5 μm .

Figure 3.18: Shape #1 detailed.

This inductor has a ground plane option on M1 layer that helps to lower the substrate losses by blocking the p-well implant under the inductor. However, this option is not applied on the remaining transmission lines on the chip. One terminal of the inductor is grounded, and the signal is injected through the other terminal. As indicated before, the parasitic effects of the probe pads and the interconnects are de-embedded from the results up to the inductor input terminals using the on-chip de-embedding structures (Shape #9, Shape #10). The effective inductance and the quality factor are calculated from the simulated and measured S-parameters then compared in Figure 3.19. The results are matched to within 10% with a slight shift in the peak Q.

Figure 3.19: Simulated vs measured results for Shape #1, (a) Effective inductance, (b) Quality factor.

3.4.3 Shapes #2, #3 (M5 and M6 metal layers two-port inductors)

These are two port coplanar transmission lines implemented in the middle metal layers (M5, M6 in Figure 3.10). These layers gave the ability to test the closely separated metallic rods from each other and from the transmission line (s_{BR} , s_R , refer to Section 3.2).

Shape #2 is testing the line properties without the rods then compared to the same line underlined with rods represented by Shape #3. Q is expected to be low due to the thin metal thickness in the middle layers, refer to Figure 3.6a. The line width and the signal-ground separation are temporarily selected to be 20 μm and 10 μm , respectively. This achieves around 50 Ohm characteristic impedance for the line without the rods over the measurement frequency range.

In the middle layers, the technology permits a minimum rod width of 1 μm , and

minimum separation of $0.5\text{ }\mu\text{m}$. A screen capture of the detailed structure for Shape #2 and Shape #3 are shown in Figure 3.20 and Figure 3.21 respectively.

Figure 3.20: Shape #2 detailed.

Figure 3.21: Shape #3 detailed.

The simulated and measured effective inductance per unit length and quality factor for the two shapes are compared in Figure 3.22. As expected, the self-resonance frequency has decreased drastically after inserting the metallic rods due to the increased line capacitance. This leads to a reduction of the line Z_0 and an increase of its electrical length βl as shown in Figure 3.23.

Figure 3.22: Simulated vs measured for Shapes #2, #3 (a) Effective inductance per unit length, and (b) Quality factor.

Figure 3.23: Simulated vs measured (a) Characteristic impedance, and (b) Electrical length for Shape #2, #3.

Based on the study introduced in Section 3.2, the reduced Z_0 and the raised βl of Shape #3 can be recovered back to be equivalent to that of Shape #2. Consequently, a length reduction of 30% can be achieved as shown in Figure 3.24 and the effective inductance per unit length can be increased by 25% and the quality factor by 80% as shown in Figure 3.25 and Figure 3.26.

Figure 3.24: (a) Length reduction in Shape #3 after Z_0 and βl adjustment, (b) Shape #2.

Figure 3.25: Effective inductance per unit length for adjusted Shape #3 compared to shapes #2, #3.

Figure 3.26: Quality Factor for adjusted Shape #3 compared to shapes #2, #3.

Making use of the allowed small spacing provided by the fabrication process, the rods can be inserted in the order shown in Figure 3.27 without affecting the overall performance. This result may contradict with that introduced in Figure 3.7d where Q is expected to decrease. In Figure 3.7d with reduced spacing the number of rods is increased and total capacitance is higher and hence Q decreased. However, here, although spacing has decreased, the total number of rods has remained the same, hence capacitance and Q remains the same.

Figure 3.27: Shape #3 with closely separated rods.

These results demonstrate the flexibility provided by using SWTLs in applications

requiring length reduction of inductors like circuits arranged in cascaded order.

3.4.4 Shape #4, #5 (M5 and M6 metal layers one-port inductors)

The implemented one-port transmission lines on the middle metal layers, are introduced in this subsection. In order to test the effect of the metallic rods on one-port transmission lines, Shapes #4, #5 are added to the chip.

Shape #4 is a one-port flipped version of Shape #3, shorted at one end as shown in Figure 3.28. This shape has a perimeter equivalent to the length of Shape #3.

Figure 3.28: Shape #4 detailed

The effective inductance per unit length of Shape #4 without and with the rods, Figure 3.29, are compared in Figure 3.30. As expected, the resonance frequency is reduced by introducing the rods and the effective simulated effective inductance at 10

GHz is higher. The quality factor is reduced due to the capacitive effect of the rods. Measurements and simulations are roughly matched although there is some deviation in the numerical values.

Figure 3.29: Shape #4 (a) Without, and (b) With rods.

Figure 3.30: Simulated vs measured results for Shape #4, (a) Effective inductance, (b) Quality factor.

Differential network calculations are used to determine the electrical length and the characteristic impedance of the one-port line. The unfolded versions of Shape #4 without and with the rods are shown in Figure 3.31. The characteristic impedance

and the electrical length are compared in Figure 3.32. In contrast to the two-port case, at the targeted frequency, the characteristic impedance doesn't change much and neither does the electrical length by adding the rods. Therefore, the rods have a minor effect on Z_0 and βl of the one-port line.

Figure 3.31: Shape #4 unfolded line, (a) Without rods, (b) With rods.

Figure 3.32: Simulated vs measured results for Shape #4, (a) Characteristic impedance, and (b) Electrical length.

To make use of the allowed small dimensions on this metal layer, the metal rods can be inserted closer to each other while leaving different areas of the line not having rods. This gives an opportunity to provide a wider separation between the line terminals to form Shape #5 as shown in Figure 3.33. The measured and simulated results

are compared in Figure 3.34. As illustrated previously, the rods are not effective in increasing the electrical length of this one-port configuration.

Figure 3.33: Shape #5 detailed.

(a)

(b)

Figure 3.34: Simulated vs measured (a) Effective inductance per unit length, and (b) Quality factor for Shape #5 with and without rods.

3.4.5 Shape #6, #7 and #8 (Top and M8 metal layers two-port inductors)

These transmission lines are built on the top metal layer stack which has a relatively thick metal. Therefore, the series resistive losses are expected to be low (refer to Q in Figure 3.6). Three TLs are implemented on this layer, two of them are two-port, and the third is one-port. Compared to the lower metal layers, this layer does not allow for closely spaced rods. The separation between the top metal and layer M8 is $3\text{ }\mu\text{m}$ therefore the separation between the rods and the line (s_BR) is dictated by this separation.

Shape #6 is a two-port line without rods as shown in Figure 3.35. The characteristic impedance of Shape #6 is around $60\text{ }\Omega$.

Figure 3.35: Shape #6 detailed.

In Shape #7, shown in Figure 3.36, the SW technique is applied in a different way; that is by applying a periodic inductive and capacitive loading on the transmission line. The inductive loading is applied by decreasing the line width (as illustrated in Figure 3.3) while the capacitive loading is applied by the metallic rods. Compared to Shape #6, the results are shown in Figure 3.37. As shown, the effective inductance per unit length is enhanced while the quality factor is not lowered very much. Better measurement conditions may be required for the quality factor.

These lines require more analysis steps as held in Shapes #2 and #3 by equating their characteristic impedance and electrical length to find the effect of simultaneous inductive and capacitive loading on the line effective inductance.

Figure 3.36: Shape #7 detailed.

Figure 3.37: Simulated vs measured (a) Effective inductance per unit length, and (b) Quality factor for Shapes #6 and #7.

In Shape #8 (one-port), periodic inductive and capacitive loadings are applied as well. Inductive loading is achieved by reducing the line width, as Shape #7, while capacitive loading is achieved by reducing the separation between the line terminals periodically as shown in Figure 3.38a. Compared with the unfolded version, shown in Figure 3.38b, the effective inductance and quality factor do not change as shown

in Figure 3.39. This TL demonstrates the layout flexibility of implementing SWTLs as inductors.

Figure 3.38: Shape #8 detailed (a) folded and, (b) unfolded.

Figure 3.39: Simulated vs measured results for Shape #8 including unfolded case, (a) Effective inductance, (b) Quality factor.

3.5 Conclusion

In this chapter, slow wave transmission lines (SWTLs) are designed, fabricated and measured to verify and highlight the advantages of using SWTLs as on-chip inductors.

Coplanar microstrip transmission line underlined with metallic rods is one way to form SWTLs in microwave applications. In the previous chapter, it has been shown that periodic capacitive loading manipulates the TL parameters and consequently its effective inductance, quality factor and self-resonance frequency. This feature have been exploited in this chapter to enhance and optimize on-chip inductors.

Coplanar configuration is selected due to its smaller footprint on-chip. The designed transmission lines, simulated using Ansoft HFSS electromagnetic simulator, are implemented on SiO_2 dielectric over silicon substrate to emulate the fabrication conditions.

Parametric analysis for eight design variables, related to the SWTL structure, potentially clarifies which design variable is more effective on the inductor performance. Five design variables related to the inductor are investigated; L_{eff} , Q_{peak} , βl , Z_0 and f_{srf} . As predicted, L_{eff} is function of βl and Z_0 , whichever is dominant, affects the inductance proportionally.

Inserting distributed metallic rods (instead of single lumped capacitor) under coplanar TL have the advantage of tuning the effective inductance, Q_{peak} and f_{srf} of the transmission line. Moreover, the distributed nature of metallic rods is exploited to provide enhanced Q and higher f_{srf} . In general, capacitive loading results in lower Q due to the coupling effect. However, parametric analysis have shown that this can be recovered back either by increasing the separation between the TL terminals (higher Z_0), and/or decreasing the TL length (l_B), and/or increasing the thickness of the TL

terminals (w_B). Thinner metallic rods is preferable from Q point of view.

A parametric table summarizing the relations between the five TL parameters to the eight spacial parameters of SWTL have been created. This table is considered as a design guideline to be applied in the next design phases.

To demonstrate the usefulness of the parametric table, three transmission lines, having different configurations and achieving the same L_{eff} , Z_0 and βl , are introduced. Comparing these three cases have shown the ability to reduce the physical length of the TLs by 45% compared to conventional line in one case and by 73% in the other case. This length reduction, while preserving effective inductance, increased the inductance per unit length and reduced the associated series resistance resulting in higher quality factor. Based on the chip area and the arrangement of the electronic components, the optimum inductor shape can be selected. This feature have demonstrated a flexibility provided by SWTLs as inductors that is useful in cascaded designs.

To close the design cycle, eight transmission lines are designed using the created parametric table, fabricated then measured. The two port configurations had shown a considerable increase in the effective inductance per unit length with an enhanced Q. The one-port configurations did not provide much variation in the electrical length, however, the capacitive loading have provided tunability for L_{eff} and f_{srf} . One port structures, should have been measured differentially to clarify the SW effect but this facility was not available during the time of conducting measurements. The close-separation capability provided by the middle metal layers are tested on four configurations. This layers gave the advantage of saving more area occupied by the rods. Transmission lines built on the top metal layers have shown better quality factor due to the higher thickness provided. After de-embedding the probe pads and

their interconnects, the measurements and simulations are matched to a great extent.

The measurements conducted in this chapter are useful in verifying the SWTL design and calibrating the electromagnetic simulator to perform in more realistic fashion. This adjustment is useful for the next simulations to be reliable. Parameters like dielectric loss tangent ($\text{Tan}\delta_{\text{SiO}_2}$), silicon resistivity (ρ_{Si}) and metal conductivity (σ) are adjusted based on the technology tolerance.

The next step is to test these inductors in a circuit. Injection-Locked Oscillators are a good candidate for that. This step is illustrated in the next chapter.

Chapter 4

SW Transmission Lines as Inductors in Injection Locked Oscillator

4.1 Introduction

In this chapter, one design phase of slow wave transmission line (SWTL) inductors is selected and included in an Injection Locked Oscillator (ILO) as a test circuit.

Based on proposed specifications for ILOs applied in software-defined radio (SDR) applications, the design steps of a differential ILO are introduced. The characterization of the electronic components used in CMOS 130nm PDK kit like transistors, varactors, coupling and decoupling capacitors are detailed throughout the chapter.

Four different inductors are tested within four ILO circuits of the same schematic. One of the four inductors is a conventional spiral inductor, inserted for reference. The other three inductors are transmission lines. The performance of the four circuits are compared from different point of views like frequency tunability, output peak voltage, injection locking range and phase noise.

Matched measurements and simulations have pushed towards designing an optimized SWTL inductor. The five proposed ILOs including SWTLs as inductors on silicon substrate are compared to the state-of-the art ILOs.

Figure 4.1: ILO circuit diagram including bias circuits.

4.2 ILO Overview and Specifications

In this section, a generic injection locked oscillator (ILO) is introduced (Figure 4.1). The core oscillator consists of the resonator and the negative resistance represented by a cross-coupled transistors M_1 and M_2 . They are biased with a current mirror represented by M_5 and M_6 . The current is injected through transistors M_3 and M_4 with their own biasing current mirror represented by M_7 and M_8 .

The differential output from the core oscillator is applied to a high input-impedance voltage buffer. The buffer circuit isolates the tank circuit from the consequent stages. For single-ended (SE) measurements, the buffer circuit is designed in a clever way to convert the differential to SE output with minimal signal loss.

Differential to SE conversion is achieved by feeding the differential output from the core oscillator to the gates of the common-drain transistors M_{10} and M_{11} . The +ve output of the buffer circuit is ac-coupled (through C_c) to the output pin of the oscillator ($+V_{out}$), while the -ve output is ac-coupled and folded back to the gate of M_9 . This achieves an in-phase addition of the -ve and +ve output of the oscillator. M_9 provides two functions; delivering the output from M_{11} and biasing M_{10} . To minimize the signal loss, two resistors R_b are added to block the unwanted paths of the output signal.

The transistors M_9 , M_{12} and M_{13} are the biasing current mirror for the buffer circuit. The two input terminals of the injected signal are connected as follows; V_{inj+} to the signal pad and V_{inj-} to the ground pad. Two varactors (C_1, C_2) are added to the circuit to fine tune the operating frequency of the oscillator in case of the predicted process variations.

The frequency of operation for the ILO is chosen to be within the band of operation for SDR applications. The synthesized frequency in nearly all the existing wireless standards requires a frequency range from 47 MHz to 12.4 GHz [18] [65–69]. The locking range is arbitrarily selected to be 500 MHz and this is applied in various applications [70,71]. The operating power supply voltage is dictated by the fabrication process to be 1.2V. System specifications are outlined and summarized in Table 4.1.

The following subsections are introducing the characterization and design of the oscillator core, transistors, varactors, coupling and decoupling capacitors used in the ILO.

Table 4.1: ILO proposed specifications.

Index	Parameter	Value
1	Operating frequency (f_0)	10 GHz
2	Lock Range (ω_L)	500 MHz ($\pm 5\%$)
3	Phase Noise (PN)	Min*
4	DC voltage (Vdd)	1.2 V
5	Power consumption	Min*
6	Load	50 Ω
7	Resonator Inductance ($L_{Tank} = 2L_1$)	534 pH

*The goal is to examine the oscillator functionality using SW lines as inductors.

4.2.1 Oscillator Core design

A one-turn kit inductor having a value of 267 pH is considered as the given inductance per branch (L_1) in the differential oscillator circuit, shown in Figure 4.2, achieving a total inductance of 534 pH (L_{Tank}).

Figure 4.2: Oscillator tank circuit.

The following numerical calculations are based on the analysis of the ILO introduced in Section 2.5. Referring to Figure 4.2, given the total inductance, L_{Tank} , of 534 pH and an operating frequency f_0 of 10 GHz, the total capacitance of the tank circuit

and the capacitance per branch can be determined from (2.34) as follows:

$$\begin{aligned}
 \therefore C_{Tank} &= \frac{1}{\omega_0^2 \cdot L_{Tank}} \\
 &= \frac{1}{(2\pi \times 10G)^2 \times 534p} \\
 \therefore C_{Tank} &= 474fF \\
 \Rightarrow C_1 &= C_2 = 948fF
 \end{aligned}$$

As a somewhat arbitrary starting assumption, let $Q_L = 10$ and $Q_C = 25$ (will later be verified or adjusted based on their characterization), we can calculate the branch losses, R_1 , and the total R_{Tank} numerically from (2.33) and substitute in (2.30) to get g_m as follows:

$$\begin{aligned}
 \therefore R_1 &= \frac{1}{\frac{1}{Q_L \omega_0 L_1} + \frac{\omega_0 C_1}{Q_C}} \\
 \therefore R_1 &= \frac{1}{\frac{1}{10 \times 2\pi \times 10G \times 267p} + \frac{2\pi \times 10G \times 948f}{25}} = \frac{1}{\frac{1}{168} + \frac{1}{420}} \\
 &\approx 120\Omega \\
 \Rightarrow R_{Tank} &\approx 240\Omega
 \end{aligned}$$

The condition to start oscillation:

$$\begin{aligned}
 g_m &> \frac{2}{R_{Tank}} \\
 &> \frac{2}{240} \\
 \Rightarrow g_m &> 8.5 \text{ mA/V}
 \end{aligned}$$

V_{tank} can be determined from (2.35) as follows:

$$V_{Tank} = \frac{2}{\pi} \cdot I_{bias} \cdot R_{Tank} \quad (4.1)$$

If V_{Tank} is required to be 600 mV, I_{bias} of 4 mA is required. Additionally, I_{bias} have to achieve the minimum g_m condition to start oscillation. This step requires deciding the channel size of the transistors as discussed in the following subsection.

4.2.2 Transistors design

All the transistors in this circuit use the RF model with minimum gate length of 120 nm. Regarding the $-g_m$ transistors, a transistor width of 25 μm with V_{gs} of 0.6 V and I_{bias} of 2 mA fulfills the required minimum g_m with some margin (8.5 mA/V). Consequently, the transistor bias current can be determined as shown in Figure 4.3b. For this transistor, the bias current required to meet the condition to start oscillation is about 2 mA.

To simplify the design, the same parameters are used to design injection transistors.

Figure 4.3: Transistors characterization (a) Circuit diagram, (b) Bias current, I_d , and Transconductance, g_m , vs V_{gs} .

Therefore, the current mirror for either the cross coupled or the injection transistors should be designed to handle a minimum current of 4 mA. Buffer transistors are assumed to handle double the current of the cross-coupled transistors, therefore they are designed with a transistor width of 50 μm .

The ratio between I_{inj} and I_{osc} , α , can be determined from (2.38) as follows:

$$\alpha = \frac{I_{inj}}{I_{osc}} = \frac{2 \cdot \beta}{\sqrt{1 + 4\beta^2}}$$

$$\text{but } \beta = \frac{Q_{Tank} \cdot \omega_L}{\omega_0}$$

$$\text{we have } Q_{Tank} = R_{Tank} \sqrt{\frac{C_{Tank}}{L_{Tank}}} \simeq 240 \sqrt{\frac{474f}{534p}} \simeq 7.1.$$

Given $\omega_L = 0.5 \text{ GHz}$

$$\therefore \beta = \frac{7.1 \times 0.5G}{10G} = 0.35$$

$$\text{and } \alpha = \frac{2 \cdot \beta}{\sqrt{1 + 4\beta^2}} = \frac{2 \times 0.37}{\sqrt{1 + 4 \times 0.37^2}} \simeq 0.58$$

Finally, referring to (2.39), the Phase Noise can be determined as follows:

$$PN = \left(\frac{\sqrt{2} \times \omega_0}{2 Q_{Tank} \Delta \omega} \right)^2 \cdot \left(\frac{FkT}{2P_s} \right)$$

$$\text{where } P_s = \frac{(V_{Tank})_{peak}^2}{2 \cdot R_{Tank}} = \frac{(700m)^2}{2 \times 240} = 1mW$$

The noise figure, F, of the active devices can be estimated from the noise summary of the simulated circuit (detailed later) then comparing the result to the calculation and measurements. For a well designed low PN circuit, F can take the value of 3. Substituting to get the PN:

$$\therefore PN = \left(\frac{\sqrt{2} \times 10G}{2 \times 7.15 \times (1M)} \right)^2 \cdot \left(\frac{3 \times (1.38 \times 10^{-23}) \times 298}{2 \times 1m} \right)$$

$$\Rightarrow PN = -112.2 \text{ dBc/Hz}$$

4.2.3 Varactor design

The selected gate dimensions for the varactors are $4.7 \mu\text{m} \times 0.24 \mu\text{m}$ having 6 gates, repeated by 12 times. The voltage drop across the varactor is defined as $V_{DC} - V_{Tune}$, as shown in Figure 4.4a. Keeping $V_{dc}=1.2 \text{ V}$ and sweeping V_{Tune} from -0.5 to 1.5 V (this is the maximum voltage sweep allowed by the kit), the kit varactor

characterization circuit and diagram (capacitance and quality factor vs frequency) is shown in Figure 4.4b. According to the calculations in Section 4.2, the required branch capacitance is about 900 fF. Therefore, the provided varactor tuning range can tune the oscillator frequency roughly from 9 GHz to 15 GHz.

Figure 4.4: Varactor characterization (a) Circuit diagram, (b) C and Q versus tuning voltage.

4.2.4 Coupling and Decoupling capacitors design

The coupling capacitors are designed to pass the input and output signals with the minimum possible attenuation and at the same time to keep the transistors biasing unchanged. A Metal Insulator Metal capacitor (mimcap) is selected to fulfill this function. A capacitor with $C=5$ pF at 10 GHz was designed to be sufficiently large to have minimal attenuation (-0.38 dB) having the size of $15 \mu\text{m} \times 45 \mu\text{m}$ (with a

multiplicity of 3). The characterization details are shown in Figure 4.5b.

The decoupling capacitors provide the reference AC ground, while also preventing undesirable ac perturbations from DC supplies. The bigger their value, the better, but this comes at the expense of an increase in layout area and cost. Dual mimcaps capacitors available in this technology are selected with dimensions of $10\text{ }\mu\text{m} \times 30\text{ }\mu\text{m}$ (with a multiplicity of 4) for the V_{dc} supply and $60\text{ }\mu\text{m} \times 20\text{ }\mu\text{m}$ (with a multiplicity of 2) for the current mirrors ($I_{\text{bias_buffer}}$, $I_{\text{bias_osc}}$, $I_{\text{bias_inj}}$). Therefore, optimized values are selected achieving the relatively high capacitance with convenient on-chip area to be 9 pF and 13 pF respectively. The characterization details are shown in Figure 4.5c and Figure 4.5d.

(a)

(b)

(c)

(d)

Figure 4.5: Coupling and Decoupling capacitors characterization (a) Characterization circuit diagram, (b) Coupling cap. char. ($15 \times 45 \mu\text{m}^2$), (c) Decoupling cap. char. for V_{dc} ($60 \times 20 \mu\text{m}^2$), (d) Decoupling cap. char. for current mirrors ($10 \times 30 \mu\text{m}^2$).

4.3 ILO Circuit Simulation

In this section, four ILO circuits (Circuit #1, #2, #3, #4) having the same circuit schematic but including four different inductors, are simulated. The associated inductors have the specified values illustrated before ($L_1 = L_2 = 267$ pH) while the performance of the ILO is monitored.

The detailed layout of the four inductors are shown in Figure 4.6. A kit inductor, Figure 4.6a, included in Circuit #1, is considered as the reference circuit to compare its performance with the others. Circuit #2 demonstrates ILO including conventional RF transmission line from the design kit. This RF transmission line, shown in Figure 4.6c, is implemented on the top metal layer having the dimensions of $4\text{ }\mu\text{m} \times 280\text{ }\mu\text{m}$ and it is underlined by a relatively high resistive layer.

Circuit #3 and Circuit #4 represent ILOs including SWTL inductors developed from the studied transmission lines in the previous chapter. The first SWTL inductor, Figure 4.6b, is periodically loaded by series inductive and shunt capacitive loading. Inductive loading is represented by the narrow widths and the capacitive loading is represented by the thick widths of the transmission line. The flexibility of TL design is exploited to flip the line to fit in the circuit layout. This TL is implemented on the top metal layer.

In Circuit #4, a second SWTL inductor (Figure 4.6d) is tested. A periodic capacitive loading using metallic rods are applied under a coplanar transmission line. The small thickness permitted by the low metal layers is exploited to build thin metallic rods under the line to enhance the quality factor as concluded from Chapter 3 (Figure 3.7d). The rods in the bottom layer is connected vertically to the nearest layer under the TL using vias as shown in the inset of Figure 4.6d.

Figure 4.6: Inductors used in the ILO design (a) Kit inductor (L_1) in Circuit #1, (b) SW line 1 (L_3) in Circuit #3, (c) Kit RF line (L_2) in Circuit #2, (d) SW line 2 (L_4) in Circuit #4 with its cross section.

All the transmission lines are modeled and characterized using the EM simulator, EMX, by extracting their inductance from their two-port S-parameters as discussed in Chapter 3.

For each of the four designed oscillators, various aspects are to be discussed and compared to the theory. The first aspect is the inductor characterization which is

performed by sweeping the inductance and the quality factor of the transmission line with the frequency to determine its L , Q_{peak} at the operating frequency and its self-resonance frequency (SRF). The characterization circuit is the same as that shown in Figure 4.5a with the capacitor replaced by the inductor. The inductance and quality factor of the four inductors are compared in Figure 4.7a and Figure 4.7b, respectively. The designed inductance is given by 267 pH for each branch of the differential circuit and the small tolerance from this value can be adjusted by the varactors to oscillate at 10 GHz. This design phase of the SW lines have a lower Q compared to the reference circuit. This is because, at this design phase, these transmission lines are not optimized to provide Q_{peak} at the required frequency. However, this is enough for the proof-of-concept.

Figure 4.7: (a) Inductance (b) Quality factor of the four inductors in each ILO. Subscripts indicate the circuit number.

The second aspect is to compare the amplitude of input signal for the oscillator to lock (locking range = 500 MHz). To find that, a signal at 10.5 GHz is injected and its amplitude is swept between 0V and 1.2V. As shown in Figure 4.8, a locking voltage of approximately $120 mV_{peak}$ is required for the four circuits to lock.

Figure 4.8: Oscillating Frequency vs $(V_{inj})_{Peak}$ of the four free running ILO (schematic simulation). Subscripts indicate the circuit number.

The next aspect is to compare the output peak voltage of the oscillator, V_{peak} , to the injected peak voltage V_{inj} . This is useful to find how the output is affected by the injected signal. The comparison of the four circuits, Figure 4.9, shows that the output peak voltage is about the same with an average of 0.32V.

The final aspect is the phase noise (PN) which is an interesting feature in assessing the oscillator performance. The PN of the four circuits (free running without injection) are compared in Figure 4.10. Although the PN of the reference circuit (Circuit #1) is not showing a competitive performance, preliminary analysis for this circuit has shown considerable room for improvement to PN. All the designed inductors are tested on the same test circuit therefore, a relative comparison is considered to be valid.

Figure 4.9: $(V_{out})_{Peak}$ vs $(V_{inj})_{Peak}$ of the four free running ILO (schematic simulation). Subscripts indicate the circuit number.

Figure 4.10: Phase Noise of the four free running ILO (schematic simulation). Subscripts indicate the circuit number.

The circuits including the SWTL inductors are showing a degraded performance, which is expected, due to the lower Q of the inductors. This requires optimizing the

design of the used SW transmission lines and test the circuit performance which is introduced in the next section.

The DC power consumption of the four designed injection-locked oscillators is discussed for completion. The designed oscillators are not competing for minimum power, however they demonstrates the feasibility of using slow-wave lines as inductors optimized for Q_{peak} in oscillators using CMOS 130nm technology. The DC power consumption without and with injection can be summarized in Table 4.2.

Table 4.2: DC power consumption for the four designed oscillators at 1.2 V.
(Refer to Figure 4.1).

Index	Mode	Current (mA)			
		Core	Injection	Buffer	Total
		Transistors M_1, M_2	Transistors M_3, M_4	Transistors $M_9 - M_{12}$	
1	Free running	4	0	8	12
2	Injection	4	4	8	16

4.4 ILO Measurements

In this section, the ILO including SW transmission lines as inductors are measured. Four oscillators of the same schematic comprising four different transmission lines are tested. The chip is implemented on 130nm CMOS process. The layout and dimensions of the four implemented circuits are shown in Figure 4.11. As shown, the circuits are having the same layout except for the inductors and their connections.

Circuit #1, including the kit inductors, is considered as a reference circuit. Circuit #2 is including a conventional RF line used as inductor. Circuit #3 and #4 include the SW inductors. The flexibility of SWTLs have provided less area occupied by the inductors. The SW line used in Circuit #4 is saving area by 25% compared to the reference circuit.

Figure 4.11: Layout of the four designed oscillators. (a) Cir. #1, inductor area= $144 \times 144 \mu\text{m}^2$, (b) Cir. #2, inductor area= $290 \times 14 \mu\text{m}^2$, (c) Cir. #3, inductor area= $255 \times 50 \mu\text{m}^2$, (d) Cir. #4, inductor area= $230 \times 40 \mu\text{m}^2$.

Figure 4.12 shows the total dimensions and a micrograph of the implemented chip. The measurement setup for one of the circuits with the RF (GSG) and DC probes landed on the pads is shown in Figure 4.13. A spectrum analyzer, HP 8564E, is used to measure the output signal and the phase noise (PN). A signal generator,

Agilent E8257C, is used to inject the input signal to test the injection locking of the oscillators. The measurement setup is shown in Figure 4.14.

Figure 4.12: The chip physical layout including the four designed injection locked oscillators. (a) Dimensions (b) Chip micrograph.

Figure 4.13: RF (right and left) and DC (top and bottom) probes landed.

Figure 4.14: Measurement setup.

Initially, the circuits were designed to oscillate at a nominal frequency of 10 GHz; however, due to some limitations (not considered in the initial simulations), the circuits oscillate at lower frequencies. One limitation is the parasitic inductance resulting from interconnections between the inductors and the circuit. Design rules for the circuit layout force the kit inductors to be placed 80 μm away from any metals. Parasitic gate-to-channel capacitance in CMOS transistors and the coupling capacitance between the tracks and substrate results in more limitations. These limitations are the main reasons for the reduction of the oscillating frequency in the four circuits.

Considering the previous limitations, an electromagnetic simulator (EMX [64]) is a useful step to verify the practical results for this design phase and the consequent phases. Figure 4.15 shows the interconnection for each inductor resulting in parasitic inductance which lowers the oscillating frequency (refer to Figure 4.6). The inductance and quality factor for each inductor are re-determined as shown in Figures 4.16 to 4.19. As shown, interconnection lengths differ from circuit to circuit, leading to

different inductance (and resonance) in each design. In Circuit #1, for example, the total inductance has increased from 470 pH to 876 pH, and this has reduced the operating frequency to 7.2 GHz.

Figure 4.15: Physical layout of the fabricated inductors with their extra connections used in (a) Circuit #1, (b) Circuit #2, (c) Circuit #3, (d) Circuit #4.

(a)

(b)

Figure 4.16: L_1 (Kit inductor) characterization with and without interconnections, (a) Inductance, (b) Quality factor.

(a)

(b)

Figure 4.17: L_2 (RF line) characterization with and without interconnections, (a) Inductance, (b) Quality factor.

Figure 4.18: L_3 (SWTL #1) characterization with and without interconnections, (a) Inductance, (b) Quality factor.

Figure 4.19: L_4 (SWTL #2) characterization with and without interconnections, (a) Inductance, (b) Quality factor.

Measured and simulated output signals from the four oscillators are compared in Figure 4.20. Matched simulated and measured results are sufficient to have the confidence that the subsequent simulations are reliable.

The injection-locking feature is tested in the four oscillators as shown in Figure 4.21.

Figure 4.20: Measured and extracted output signal for the four oscillators (a) Circuit #1, (b) Circuit #2, (c) Circuit #3, (d) Circuit #4.

The injected signal has a peak value of 150 mV (-6.5 dBm) at the operating frequency of each oscillator. As expected, the injection has enhanced the phase noise by about 30 dB at 1 MHz offset.

Figure 4.21: Measured output signal without injection (blue) and with injection (black) for the four oscillators (a) Circuit #1, (b) Circuit #2, (c) Circuit #3, (d) Circuit #4.

The simulated and measured PN of the four circuits are compared in Figure 4.22. As shown, the simulations are following the same trend as the measurements in the four circuits. With the injection signal applied, the simulated PN is shown to be lower than that measured. This is because, at injection locking state, the measured noise is no-longer dominated by the transistors' flicker noise. Instead, the measured noise is dominated by noise floor of the spectrum analyzer (≈ -133 dBm @ 1MHz [72] indicated in red dashed line in Figure 4.22).

Figure 4.22: Measured and extracted phase noise without and with injection for the four oscillators with the noise floor of the spectrum analyzer represented by the red dashed lines (a) Circuit #1, (b) Circuit #2, (c) Circuit #3, (d) Circuit #4.

Circuits comprising lower Q inductors are expected to have low PN, however, this is not observed. This means that other factors (other than Q_{tank}) are contributing for lower PN. To study the reasons for that, the noise contributions of each component in each circuit are determined using the Noise Analysis feature in Cadence SpectreRF and they are summarized in Table 4.3. For reference, the schematic of ILO including bias circuits is re-introduced in Figure 4.23.

Table 4.3: Dominant noise contributions at the output of the four oscillators
(acquired from Cadence SpectreRF Noise Summary).

Component / Noise type	Circuit #1		Circuit #2		Circuit #3		Circuit #4	
	V^2/Hz ($\times 10^{-14}$)	%	V^2/Hz ($\times 10^{-14}$)	%	V^2/Hz ($\times 10^{-14}$)	%	V^2/Hz ($\times 10^{-14}$)	%
M_1, M_2 Thermal noise	5.4	2.7	7.9	27.4	7.9	28.2	10	26.1
M_1, M_2 Flicker noise	4.5	2.2	0.42	1.4	0.41	1.4	1.01	2.6
M_5, M_6 Thermal noise	5.1	2.5	3.6	12.6	3.6	12.7	2.6	6.7
M_5, M_6 Flicker noise	175	86.5	4.5	15.7	3.6	13.3	10.9	28.2
L_{Tank}^* Thermal noise	3.9	1.9	5.5	19.3	5.55	19.9	7.1	18.5
C_{Tank} Thermal noise	0.93	0.48	1.34	4.6	1.35	4.8	1.72	4.5
Total	195/202	96.2	23.3/29	81	22.4/28.2	80.3	33.3/38	86.6

* L_{Tank} includes the interconnection lines.

Figure 4.23: ILO circuit diagram including bias circuits.

Although the four circuits have the same schematic and layout except for the inductors, noise contribution from the transistors differs from circuit to circuit. Therefore, the noise contribution from the inductors in each circuit is to be addressed at this stage. As shown in Table 4.3, the low-Q inductors in Circuits #2,#3, #4 are contributing much noise to the total output noise compared to Circuit #1. Although Circuit #1 is showing the highest total noise, noise sources, other than those from inductors, are the reason for total noise contribution. This requires optimization for the design of current source transistors M_5, M_6 which are the dominant noise sources in the circuit.

4.5 ILO with an Optimized SWTL as Inductor

At this stage, the designed oscillators are verified with measurements and further reliable simulations can be done on optimized SWTLs. An optimized SWTL inductor compatible with CMOS 130nm technology is designed specifically for this ILO. Compared to the double-kit-inductor configuration, the physical shape of the optimized SWTL inductor, including interconnections to the oscillator core, is providing efficient chip area as shown in Figure 4.24a,b. The SWTL inductor is providing 25% less area compared to the spiral kit inductors. The separation between the two kit inductors is imposed by the kit design rules to a minimum spacing of $80\ \mu\text{m}$ between the kit inductor and the nearest metal to prevent any coupling and consequently losses. The floating metallic rods in the SWTL inductor are providing tuning Q_{peak} to the required operating frequency, besides shielding the electric field from penetrating the substrate leading to lower losses. For completion, a single-kit-inductor configuration is compared to another SWTL (Figure 4.24c) of the same inductance.

Figure 4.24: Optimized SWTL inductor demonstrated 25% lower area compared to double kit inductors, (a) Physical shape of SWTL having $L_{\text{diff}} = 470\ \text{pH}$ (without interconnections), (b) Physical shape of the double-kit inductor configuration having the same L_{diff} (without interconnection), (c) Physical shape of SWTL having $L_{\text{diff}} = 240\ \text{pH}$ ($= L_{\text{diff}}$ of a single kit inductor).

Since the optimized SWTL inductor is connected differentially within the oscillator core, differential characterization is required. Differential inductance (L_{diff}) and quality factor of the SWTL is compared to the kit inductor (assuming ideal interconnections) as shown in Figures 4.25 and 4.26. In both cases, the optimized SWTL is achieving the same inductance as the kit inductor with the advantage of higher Q. In the first case (double kit inductor), the SWTL is providing 60% Q-enhancement at 10 GHz. In the second case (single kit inductor), although Q_{peak} is not fully tuned to 10 GHz, the SWTL is providing 75% Q-enhancement. The resonance frequency is safely above the operating frequency by at least two decades.

(c)

Figure 4.25: Performance comparison of SWTL vs two-kit inductor configuration.
 Connection setup for (a) the kit inductor, (b) the $375\mu\text{m}$ SWTL, (c)
 Differential inductance and quality factor.

Figure 4.26: Performance comparison of SWTL vs one-kit inductor configuration. Connection setup for (a) the kit inductor, (b) the 200 μm SWTL, (c) Differential inductance and quality factor.

Compared to the kit inductor, the SW line achieved the required inductance with a higher quality factor. Therefore, when applying the SWTL in the oscillator, it is expected that the noise contribution from the tank circuit to be lower. The oscillator performance with the optimized SW line as inductor is tested without and with injection as shown in Figure 4.27.

An ideal inductor having the specified inductance is applied to the same oscillator to be compared to that including the optimized SWTL inductor. The output signal and PN for both circuits are shown in Figure 4.28. Noise contribution at the output of each circuit are compared in Table 4.4.

Figure 4.27: Oscillator performance using the optimized SWTL without and with injection, (a) Output signal, (b) PN.

Figure 4.28: Oscillator output signal (a), and PN (b), using the ideal inductor and the optimized SWTL.

Compared to the low-Q inductors introduced previously, the noise contribution of the optimized SWTL inductor is meager. It is observed that the dominant noise source is the flicker noise of current sources (M_5, M_6). This requires more optimized design for the transistors to reduce their flicker and thermal noise by adjusting their current density and number of fingers. The circuit diagram and the final layout of the oscillator including the slow wave transmission line are shown in Figure 4.29 and Figure 4.30 respectively.

Table 4.4: Dominant noise contributions at the output for the oscillators comprising Ideal inductor and SWTL shown in Figure 4.24a (acquired from Cadence SpectreRF Noise Summary).

Component / Noise type	Ideal L ($2 \times 234\text{pH}$)		SW L (484 pH)	
	V^2/Hz ($\times 10^{-14}$)	%	V^2/Hz ($\times 10^{-14}$)	%
M_1, M_2 Thermal noise	2.8	2.3	4.54	1.8
M_1, M_2 Flicker noise	16.2	13.7	4.68	1.8
M_5, M_6 Thermal noise	3.4	2.8	4.1	1.6
M_5, M_6 Flicker noise	77	65.6	219	87
M_3, M_4 Flicker noise	5.1	4.3	—	—
L_{Tank}^* Thermal noise	—	—	2.4	0.98
C_{Tank} Thermal noise	1.05	0.9	1.45	0.6
Total	105.5/118	89.5	197/206.8	95.3

* L_{Tank} without interconnections.

Figure 4.29: ILO circuit diagram including SW line as inductor.

Figure 4.30: ILO layout including SW line as inductor.

The performance of the four implemented circuits and the one including the optimized inductor are summarized and compared to the state-of-the-art oscillators in Table 4.5. The circuits implemented by using SWTLs have demonstrated the flexibility provided to make use of the dedicated chip area. It should be noted that the main objective of this comparison is to highlight the advantage of the SWTL inductor-based VCO as compared to its counterpart designed with lumped LC tank.

Table 4.5: Performance summary of ILO using SWTLs and prior art.

References	This Work					[73]	[74]	[75]	
	Cir.	Cir.	Cir.	Cir.	Cir.				
	#1	#2	#3	#4	Opt.				
Technology [nm]	130					40	180	180	
Frequency [GHz]	7	7.8	7.9	8.5	9.5	4.6	11.2	2.5-4.9	
V_{DC} [V]	1.2					1.1	1.8	1.8	
I_{DC} [mA]	4					12.8	3.8	3.5	
Tuning Range [MHz]	500					200	300	2500	
Phase Noise @ 1MHz [dBc/Hz]	-103	-109	-110	-106	-105	-103	-109	-121	
Total Area [μm^2]	L	413	320	440	310	380	~519	530	410
	W	520	520	520	520	600	~519	625	640

4.6 Conclusion

This chapter has investigated the performance of slow wave transmission lines (SWTLs) as inductors in injection locked oscillator (ILO) circuit implemented on lossy silicon substrate using CMOS 130nm technology. ILO, as a widely used circuit in RFIC, is the vehicle in which SWTLs as inductors are tested and compared with the state-of-the-art oscillators at RF frequencies.

Design steps of the ILO are introduced with detailed calculations to meet an assumed generic specifications based on reported applications in software-defined radio transceivers. Transistors, varactors, coupling and decoupling capacitors are designed to fit the requirements, while the characterization of each component has been illustrated.

The investigation methodology is to design and implement four ILO circuits of the same schematic and layout using different inductors. The first ILO circuit (Circuit #1) incorporated a kit inductor (conventional spiral inductor) and considered as a reference circuit. The second circuit (Circuit #2), incorporated an RF transmission line (from the kit) used as inductor to test the performance of regular RF lines in ILOs. The other two circuits (Circuit#3, #4) test two versions of a developed SWTLs as inductors.

The four circuits are compared from different points of views; tunability, amplitude of the output signal, injection locking, phase noise and chip area. The two circuits incorporating the SW lines have shown the design flexibility in saving chip area. Circuit #3 have provided layout flexibility for the designer to efficiently use the chip area and add more components, if required. Circuit #4 occupies 75% the area occupied by the reference circuit (Circuit#1). Since the two SW lines are not fully

optimized at this design phase, lower quality factor relative to the kit inductor and degraded phase noise (PN) are resulted.

Parasitic inductance from interconnects (not considered in the initial design phases) is the main reason of shifting the measured operating frequency of the four circuits to lower values. Considering this in the subsequent simulations, results have shown to be consistent with measurements to a great extent. Circuits comprising higher-Q inductors did not show a better PN. Nevertheless, further circuit investigation indicated that Q_{tank} is not the dominant contributor to the total output noise. Applying noise analysis using Cadence SpectreRF have shown that thermal noise from cross-coupled transistors and flicker noise from current mirrors are the main noise contributors. This can be addressed by adjusting the transistors' current density and number of fingers.

To assess the performance of the inductors in the ILO, a novel technique is proposed. Noise contribution from the tank circuit is quantified and compared to the other noise sources. As expected, low-Q inductors have contributed more to the output noise.

At this stage, the main goal was to validate a matched results between the design and measurements to perform a reliable consequent simulations on an optimized SWTLs used as inductors in RF circuits.

Since the inductors are connected differentially in the tank circuit, an optimized differential SWTL have been designed (length = 375 μm) and compared to a differential conventional double-kit-inductor. The differential SWTL inductor have demonstrated a 60% Q-enhancement at the operating frequency compared to the kit inductor. For completion, another SWTL (length = 200 μm) was designed and compared to a single kit inductor of the same inductance. The former have shown 75% Q-enhancement.

This is mainly due to the low series resistance provided by SWTLs, shorter interconnections to and from SWTL inductors, the ability to store more energy, and the shielding provided by the floating metallic rods under the line.

The optimized SWTL inductor is applied to the ILO and compared to an ideal inductor. A PN of -105 dBc/Hz have been achieved despite a room for more enhancement in the transistors design. The noise contribution from the SWTL to the output of the oscillator is minimal. Therefore, applying SWTL as inductors did not inhibit injection locked oscillators from operating normally, provided its layout flexibility, efficient chip area occupation, better quality factor compared to conventional spiral inductors. Compared to the prior art, using SWTLs as inductors in ILOs highlighted the extra degrees of freedom of using the SWTLs as inductors in RF applications.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

This thesis has introduced a comprehensive study to explore the feasibility of replacing conventional on-chip spiral inductors by the Slow Wave (SW) based transmission lines to be used as on-chip inductors in RF applications. Reported approaches aiming at enhancing on-chip inductors is limited by the technology constraints.

Several enhancement techniques for integrated inductors were surveyed and classified. The drawbacks are summarized as a very low f_{srf} (below 3 GHz) and mechanical instability of the magnetic core inductors, extra cost of the post processing techniques, induced eddy currents of the modified ground plane structures and high resistive losses of the helical inductors.

Classical and periodic structure analysis for two-port SW transmission lines are introduced to study and understand the SW technique theoretically. The distributed feature provided by SWTLs have proven to be advantageous for on-chip inductors instead of lumped inductors. Distributed capacitive loading (instead of one lumped capacitor), have the advantage of tuning L_{eff} , Q_{peak} , and f_{srf} . Moreover, the distributed nature can be exploited to provide an enhanced Q.

Applying metallic rods under the transmission line which couples the signal terminal

to the ground terminal is the selected structure to build and further study SWTLs. For completion, the detailed design equations for a generic injection locked oscillator (ILO), as a vehicle to test SWTL inductors, were detailed.

Parametric analysis for eight design variables, related to the SWTL structure, potentially clarifies which design variable is more effective on the inductor performance. Five design variables related to the inductor are investigated; L_{eff} , Q_{peak} , βl , Z_0 and f_{srf} , versus eight spacial variables related to coplanar stripline physical structure; w_B , l_B , s_B , h_B , s_{BR} , h_R , l_R , and s_R . As predicted, L_{eff} is a function of βl and Z_0 , whichever is dominant, affects the inductance proportionally. In general, capacitive loading results in lower Q due to the coupling effect. This can be recovered back either by increasing the separation between the TL terminals (higher Z_0), and/or decreasing the TL length (l_B), and/or increasing the thickness of the TL terminals (w_B). Thinner metallic rods is preferable from Q point of view.

The parametric analysis held in this thesis have provided a parametric table which is considered as a design guideline to tune and optimize the inductive parameters (L_{eff} , Q_{peak} and f_{srf}) of SWTL to the desired frequency of operation.

Based on the design table provided by the parametric analysis, three case studies are conducted. Three transmission lines, having the same L_{eff} , Z_0 and βl , are compared and have shown the physical design flexibility provided by SWTLs as inductors. Referring to conventional coplanar TL, one case have shown 45% reduction in length and the other case have shown 73% reduction. This gives the designer the flexibility to fill the dedicated chip area efficiently especially in cascaded circuits.

Fabrication and measurements of eight SWTLs have ensured the theory and simulations (Chip #1). This is useful as well in calibrating the simulator to provide trustable

consequent simulation phases. This design phase have examined transmission lines on different metal layers in CMOS 130nm process. TLs implemented in lower metal layers got benefits of allowable close separation to verify the rod-rod separation factor on L_{eff} and Q. As expected, these layers provided lower Q due to higher resistive losses. Different irregular shapes of SWTLs are tested on this chip and the SWTL inductors are verified to be tested in injection locked oscillators (ILOs).

ILO is the vehicle in which SWTLs as inductors are tested and compared with the state-of-the-art oscillators at RF frequencies (Chip #2). Specifications for a generic ILO applied in reported software-defined radio transceivers are assumed. Using the same PDK kit, electronic components like transistors, varactors, capacitors are characterized to fit the requirements.

Four different inductors are inserted in four circuits having the same schematic and physical layout. (Circuit #1) incorporated a kit inductor (conventional spiral inductor) and considered as a reference circuit. The second circuit (Circuit #2), incorporated an RF transmission line (from the kit) used as inductor to test the performance of regular RF lines in ILOs. The other two circuits (Circuit#3, #4) test two versions of a developed SWTLs as inductors.

Comparing the four circuits, have revealed the potential of SWTL inductors to save more area on-chip. Circuit #3 have provided layout flexibility for the designer to efficiently use the chip area and add more components, if required. Circuit #4 occupies 75% compared to the reference circuit (Circuit#1). In the circuits including the kit inductors and RF lines, the lengthy interconnections introduced more inductance which resulted in lower oscillation frequency (7 GHz for Circuit #1 and 7.8 GHz for Circuit #2) rather than the required (10 GHz). Shorter interconnections of the SWTL inductors provided lower parasitic inductance resulted in closer oscillation

frequencies to that required (8 GHz for Circuit #3, 8.5 GHz for Circuit #4).

The designed SWTLs in this phase required more development due to their lower Q, especially that this is not reflected in lower phase noise (PN). The PN is function of other parameters other than Q_{tank} like the transistor's number of fingers and the current density. To address this problem, and evaluate the performance of inductors, a novel technique is introduced. The noise contribution of each component in the circuit is quantified and compared using Cadence SpectreRF. As expected, low Q inductors have contributed more noise to the circuit output.

An optimized differential SWTL have been designed (length = $375\ \mu\text{m}$) and compared to a differential conventional double-kit-inductor. The differential SWTL inductor have demonstrated a 60% Q-enhancement at the operating frequency compared to the kit inductor. For completion, another SWTL (length = $200\ \mu\text{m}$) is designed and compared to a single kit inductor of the same inductance. The former have shown 75% Q-enhancement. This is mainly due to the low series resistance provided by SWTLs, shorter interconnections to and from SWTL inductors, the ability to store more energy, and the shielding provided by the floating metallic rods under the line.

The optimized SWTL inductor is applied to the ILO and compared to an ideal inductor. A PN of -105 dBc/Hz have been achieved despite a room for more enhancement in the transistors design. The noise contribution from the SWTL to the output of the oscillator is minimal compared to the conventional kit inductor. Therefore, applying SWTL as inductors did not inhibit injection locked oscillators to operate normally, provided its layout flexibility, efficient chip area occupation and better quality factor. Compared to the prior art, using SWTLs as inductors highlighted the extra degrees of freedom of the SWTLs as inductors.

This thesis have highlighted the advantages of using SWTLs as on-chip inductors and this is summarized as follows:

- The ability to tune its transmission-line parameters and consequently L_{eff} , Q and f_{srf} without changing its physical outline.
- Compared to lumped element loaded transmission line, SWTLs provides an enhanced Q_{peak} and f_{srf} due to the distributed loading provided.
- Higher inductance per unit length (useful in cascaded circuits).
- Shorter interconnections reduces the parasitic inductance and resistive losses compared to spiral conventional inductors.
- Differentially connected SWTLs as inductors have saved a huge area on-chip instead of using double spiral inductors.
- Balanced feature is useful in differential networks without the need for balun circuits.

5.2 Thesis Contributions

This study has resulted in the following contributions:

1. A thorough study to generate a parametric table linking eight spatial variables, related to the SWTL structure, to five design variables related to the inductor. This is a useful design guideline for SW structures as inductors with the ability to tune its effective inductance, peak quality factor to the desired frequency.
2. To demonstrate size manipulation, two SWTLs as inductors are designed using the parametric table with 45% and 75% reduced lengths compared to conventional transmission lines. This (Publication in MWSCAS-2018).
3. To demonstrate Q enhancement, two SWTLs are designed based on the generated parametric table with 75% and 60% enhanced Q, compared to conventional single and double spiral inductors.
4. A novel technique to evaluate the performance of on-chip inductors within RF circuits by calculating their noise contribution to the circuit output.

5.3 Future work

In this study, the floating metallic rods under the transmission line are distributed uniformly. Non uniform distribution can be studied to find their effect on the performance of SWTLs as inductors.

Slow wave is one technique used to maximize the electrical length of transmission lines in microwave applications. Other techniques might be useful to be tested in RF

circuits like composite right left-handed transmission lines (metamaterials). At this stage, losses must be checked due to series resistive and shunt conductive lossy nature of transmission lines. The low-frequency inductance should be checked as well due to the series capacitance of these composite right-left handed transmission lines.

Further improvement could be made to the modeling of SW transmission lines to help in minimizing the design time to facilitate the optimization of SWTLs as inductors for the best performance.

This study can be extended to electrically tune on-chip inductors which is one useful topic in software defined radio transceivers. This might be provided by controlling the coupling capacitance between the transmission line terminals.

One useful application in which the length reduction feature could be exploited is in the field of printed electronics. This application is suffering from resistive (lossy) transmission lines so SW lines with reduced lengths may prove to be useful in the implementation of transmission lines and/or inductors.

Recently there has been significant research interest on electromagnetic applications of engineered materials, where the material characteristics can be tailored. Controlling the electromagnetic properties of materials (the permeability) is going beyond the limit that is attainable with naturally existing substances, and this has become a reality with the advent of meta-materials [76, 77].

Artificial magnetism is another approach that could be applied for improving the material permeability μ_r . This can be realized by suitably tailoring set of currents arranged in space resulting in an effective permeability of a material which might be useful for inductance density enhancement [78, 79].

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Appendix A

Inductance of two-wire transmission line

In this appendix, for completion, the inductance per unit length is determined for a basic two wire transmission line shown in Figure A.1 [80]. In this case, it is assumed that the two-wire lines are having a cylindrical cross section, and the wire diameter ($2a$) is much lower than the spacing between the centers of the wires (d).

Figure A.1: Two-wire transmission line. (a) Two parallel conductors each carrying a current I , in opposite directions with radii a and separation d , (b) Horizontal cross-section, (c) Vertical cross-section.

In this case the steady currents in each conductor is uniformly distributed along the wire cross section. Hence, the magnetic flux density (B) in the region of the $y=0$ plane that extends from $x = -d/2 + a$ to $x = d/2 - a$ is given by:

$$B_y = -\frac{\mu_0 I}{2\pi} \left(\frac{1}{x + (d/2)} - \frac{1}{x - (d/2)} \right)$$

The total flux linkage through the area on the $y=0$ plane between the conductors each of length l can be found from:

$$\begin{aligned} \Psi &= \int_S B \cdot ds = \frac{\mu_0 I l}{2\pi} \int_{-(d/2)+a}^{(d/2)-a} \left[\frac{1}{x + (d/2)} - \frac{1}{x - (d/2)} \right] dx \\ &= \frac{\mu_0 I l}{2\pi} [\ln(x + (d/2)) - \ln(x - (d/2))]_{-(d/2)+a}^{(d/2)-a} \\ &= \frac{\mu_0 I l}{\pi} \ln\left(\frac{d-a}{a}\right) \end{aligned}$$

Since $d \gg a$, it can be written as follows:

$$\Psi = \frac{\mu_0 I l}{\pi} \ln\left(\frac{d}{a}\right)$$

Therefore, the inductance per unit length of two-wire line is:

$$L = \frac{L}{l} = \frac{\Psi}{I l} = \frac{\mu_0}{\pi} \ln\left(\frac{d}{a}\right) = 0.4 \ln\left(\frac{d}{a}\right) [\mu H \cdot m^{-1}]$$

A more accurate analysis for the general case can be written as follows:

$$\begin{aligned} L &= \frac{\mu_0}{\pi} \ln\left[\frac{d}{a} + \sqrt{\left(\frac{d}{2a}\right)^2 - 1}\right] H \cdot m^{-1} \\ &= 0.4 \ln\left[\frac{d}{a} + \sqrt{\left(\frac{d}{2a}\right)^2 - 1}\right] H \cdot m^{-1} \end{aligned}$$

Appendix B

Deembedding Probe Pads and Interconnects

To measure on-wafer devices, an interface must be established between device ports and the probe tips. This is done by constructing a fixture for mounting the DUT.

Calibration is one crucial step which removes the measurements. On-wafer calibration can be done by the use of ceramic Impedance-Standard-Substrate (ISS) containing high precision calibration standards. However, this establishes the reference plane at the probe tips ignoring the effects of the fixture mounting the DUT.

The problem with the interface between device ports and probe tips, while doing the measurement, is that some parasitic features arise which could drastically affect the actual performance of the DUT. These unwanted features arise from low substrate resistivity and low conductance of metal traces. Deembedding is a mathematical way which removes these adverse effects from the actual measurements of the DUT.

Hence, the reference plane is established close to the intrinsic boundary of the device as desired.

The basic approach for de-embedding is to assume a model topology for the fixture including the DUT, pads and interconnects [81]. The assumed model for the parasitic components associated with the DUT is shown in Figure B.1.

Figure B.1: Model of the DUT with the parasitics.

In the model, G_{1a} represents the pads parasitic capacitance with the substrate. Z_{1b} is the impedance of the interconnect from the pads to the DUT. G_3 represents the coupling between the two ports (can be assumed to be zero in our case due to the long distance between the two ports). Open-Short de-embedding technique is used to extract the parasitic components and subtract them from the measurements. In the Open case, the model looks as shown in Figure B.2. The equivalent Y-parameters for this pi network is as follows:

$$Y_{Open} = \begin{bmatrix} G_{1a} + G'_3 & -G'_3 \\ -G'_3 & G_{2a} + G'_3 \end{bmatrix}$$

Where

$$G'_3 = \frac{1}{Z_{1b} + (1/G_3) + Z_{2b}}$$

From which G_{1a} and G_{2a} can be extracted as follows:

$$G_{1a} = (Y_{Open})_{11} + (Y_{Open})_{12} \quad (B.1)$$

$$G_{2a} = (Y_{Open})_{21} + (Y_{Open})_{22} \quad (B.2)$$

Figure B.2: Model with the DUT replaced by open circuit.

In the Short case, the model looks as shown in Figure B.3. Here,

$$G_{ab1} = G_{1a} + \frac{1}{2 * Z_{1b}}$$

$$G_{ab2} = G_{2a} + \frac{1}{2 * Z_{2b}}$$

The equivalent Y-parameters for this pi network is as follows:

$$Y_{Short} = \begin{bmatrix} G_{ab1} + G_3 & -G_3 \\ -G_3 & G_{ab2} + G_3 \end{bmatrix}$$

From which $Z1b$ and $Z2b$ can be extracted as follows:

$$Z1b = \frac{1}{2 * ((Y_{Short})_{11} + (Y_{Short})_{12} - G1a)} \quad (B.3)$$

$$Z2b = \frac{1}{2 * ((Y_{Short})_{21} + (Y_{Short})_{22} - G2a)} \quad (B.4)$$

$$G3 = -(Y_{Short})_{21} \quad (B.5)$$

The on-chip short circuit is not an ideal short, it has some series impedance. Therefore, the denominator in Equation B.3 and Equation B.4 may need to be multiplied by a factor of 1.5 in our case.

Figure B.3: Model with the DUT replaced by short circuit.

The equivalent ABCD parameters of the DUT+parasitics (measured data) can be evaluated from the cascaded networks A_{ab1} , A_{ab2} , and A_{3DUT} as shown in Figure B.4.

Figure B.4: Model with the DUT + parasitics.

Therefore:

$$A_{ab1} = \begin{bmatrix} 1 & 0 \\ G1a & 1 \end{bmatrix} * \begin{bmatrix} 1 & (2 * Z1b) \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} 1 & 2 * Z1b \\ G1a & (2 * G1a * Z1b) + 1 \end{bmatrix}$$

and

$$A_{ab2} = \begin{bmatrix} 1 & 0 \\ G2a & 1 \end{bmatrix} * \begin{bmatrix} 1 & (2 * Z2b) \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} 1 & 2 * Zb2 \\ G1a & (2 * G2a * Z2b) + 1 \end{bmatrix}$$

Referring to Figure B.4, the measured ABCD parameters is equivalent to:

$$A_{meas} = \begin{bmatrix} A_{ab1} \end{bmatrix} * \begin{bmatrix} A_{3DUT} \end{bmatrix} * \begin{bmatrix} A_{ab2} \end{bmatrix}$$

Therefore,

$$A_{3DUT} = \begin{bmatrix} A_{ab1} \end{bmatrix}^{-1} * \begin{bmatrix} A_{meas} \end{bmatrix} * \begin{bmatrix} A_{ab2} \end{bmatrix}^{-1}$$

A_{3DUT} can be converted to Y_{3DUT} . The final step is to determine the equivalent Y-parameters for the parallel two-port networks Y_{DUT} and $G3$, as follows:

$$Y_{3DUT} = \begin{bmatrix} G3 & -G3 \\ -G3 & G3 \end{bmatrix} + \begin{bmatrix} Y_{DUT} \end{bmatrix}$$

From which the deembedded DUT can be determined as follows:

$$Y_{DUT} = \begin{bmatrix} Y_{3DUT} \end{bmatrix} - \begin{bmatrix} G3 & -G3 \\ -G3 & G3 \end{bmatrix}$$

Appendix C

Input Impedance of short-circuit and open-circuit terminated networks from ABCD parameters

In this appendix, the input impedance for two port networks open/short circuit terminated is determined from its ABCD parameters. Two configurations are considered; shunt series and series shunt L networks shown in Figure C.1.

Figure C.1: Two L-network configurations, (a) Shunt-series, (b) Series-shunt.

Starting with shunt-series LC network terminated by a short circuit, the input

impedance can be determined as:

$$Y_{in} = Y_L + Y_C \quad (C.1)$$

$$Y_L = \frac{1}{j\omega L} \quad (C.2)$$

$$Y_C = j\omega C \quad (C.3)$$

$$\therefore Y_{in} = j\omega C + \frac{1}{j\omega L} \quad (C.4)$$

$$\therefore Z_{in} = \frac{j\omega L}{1 - \omega^2 LC} \quad (C.5)$$

The ABCD parameters for this two-port network can be determined as follows [38]:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix} \cdot \begin{bmatrix} 1 & j\omega L \\ 0 & 1 \end{bmatrix} \quad (C.6)$$

$$= \begin{bmatrix} 1 & j\omega L \\ j\omega C & 1 - \omega^2 LC \end{bmatrix} \quad (C.7)$$

Comparing Equation C.7 with Equation C.5,

$$\therefore Z_{in} = \frac{B}{D}$$

For the series-shunt LC network terminated by an **open circuit**, the input

impedance can be determined as:

$$Z_{in} = Z_C + Z_L \quad (C.8)$$

$$Z_L = j\omega L \quad (C.9)$$

$$Z_C = \frac{1}{j\omega C} \quad (C.10)$$

$$\therefore Z_{in} = j\omega L + \frac{1}{\omega C} = \frac{1 - \omega^2 LC}{j\omega C} \quad (C.11)$$

The ABCD parameters for this two-port network can be determined as follows [38]:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & j\omega L \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix} \quad (C.12)$$

$$= \begin{bmatrix} 1 - \omega^2 LC & j\omega L \\ j\omega C & 1 \end{bmatrix} \quad (C.13)$$

Comparing Equation C.13 with Equation C.11,

$$\therefore Z_{in} = \frac{A}{C}$$