# An Efficient RF Rectifier for Energy Harvesting Systems with Applications to Wireless Dosimetry

by

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# Abstract

In the medical industry, there exists a great need for donated blood, which must first be sterilized before being used in transfusions. A growing number of facilities have begun to use X-ray irradiation for blood sterilization, along with a tag employing a radiation-sensitive chemical to measure the applied dose. Such an approach is prone to measurement error and inaccuracy, leading to the wastage of blood, time, and expense. A wireless RFID sensor tag has been proposed by researchers at Carleton University. This work presents both a system-level overview of the X-ray dosimeter tag and a design of the energy harvesting module.

The wireless X-ray dosimeter tag is estimated to consume 263.1 $\mu$W of power and is designed to operate at a distance of one metre away from a 2.45 GHz intentional RF power source. This source is harnessed by the energy harvesting module, which consists of a: dipole antenna, matching network, Dynamic $V_{th}$ Cancellation (DVC) rectifier, Smart Voltage Regulator (SVR), and off-chip ceramic capacitor.

As part of the energy harvesting module, an RF rectifier employing DVC was designed and implemented in a commercial 0.13 $\mu$m CMOS process. Experimental measurements demonstrate that the design achieves a peak power conversion efficiency (PCE) of 49.7% at a power level of -12.0 dBm, an operational frequency of 2.45 GHz, and an output loading of 25 k$\Omega$.

This thesis is dedicated to my parents, for whose love and support has made this journey possible, and to the enduring memory of my grandparents.

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# Table of Contents

# List of Tables

# List of Figures

# Nomenclature

| | |
|---|---|
| ALC | Automatic Levelling Control |
| AM | Amplitude Modulation |
| ASK | Amplitude-Shift Keying |
| BAN | Body Area Network |
| CMOS | Complementary Metal-Oxide Semiconductor |
| CMRR | Common-Mode Rejection Ratio |
| CW | Continuous Wave |
| dBi | Decibel isotropic |
| DC | Direct Current |
| DCP | Dickson Charge Pump |
| DCT | Diode-Connected Transistor |
| DFN | Dual-Flat No-Leads |
| DRAM | Dynamic Random-Access Memory |
| DUT | Device Under Test |
| DVC | Dynamic $V_{th}$ Cancellation |
| EDLC | Electrochemical Double Layer Capacitor |
| eFuse | Electronic Fuse |
| EH | Energy Harvesting |
| EIRP | Effective Isotropically Radiated Power |
| EM | Electromagnetic |
| ESD | Electrostatic Discharge |
| ESR | Equivalent Series Resistance |
| EVC | External $V_{th}$ Cancellation |
| FDA | Food and Drug Administration |
| FSK | Frequency-Shift Keying |

| | |
|---|---|
| FFP | Fresh Frozen Plasma |
| FG | Floating-Gate |
| FWBR | Full-Wave Bridge Rectifier |
| Gy | Gray |
| HF | High Frequency |
| HIV | Human Immunodeficiency Virus |
| HWR | Half-Wave Rectifier |
| IBM | International Business Machines Corporation |
| IC | Integrated Circuit |
| ISM | Industrial, Scientific, & Medical |
| ITU | International Telecommunication Union |
| IVC | Internal $V_{th}$ Cancellation |
| IEEE | Institute of Electrical and Electronics Engineers |
| kbps | Kilobits-per-second |
| LDO | Low-Dropout, a type of voltage regulator |
| LF | Low Frequency |
| LTCC | Low Temperature Co-Fired Ceramic |
| MIM | Metal-Insulator-Metal |
| MOSFET | Metal-Oxide Semiconductor Field Effect Transistor |
| NMOS | n-Type Metal-Oxide Semiconductor |
| NRZ | Non-Return to Zero |
| NVM | Non-Volatile Memory |
| OOK | On-Off Keying |
| PIE | Pulse-Interval Encoding |
| PCB | Printed Circuit Board |
| PCE | Power Conversion Efficiency |
| PR-ASK | Phase-Reversal Amplitude-Shift Keying |
| PSK | Phase-Shift Keying |
| PSRR | Power Supply Rejection Ratio |
| PSS | Periodic Steady-State |
| PVT | Process, Voltage, Temperature |
| PWM | Pulse-Width Modulation |
| Q Factor | Quality Factor |
| QAM | Quadrature Amplitude Modulation |

| | |
|---|---|
| QPSK | Quadrature Phase-Shift Keying |
| RBCs | Red Blood Cells |
| RF | Radio Frequency |
| RFID | Radio Frequency Identification |
| SEE | Single-Event Effect |
| SEL | Single-Event Latchup |
| SET | Single-Event Transient |
| SEU | Single-Event Upset |
| SMA | SubMiniature version A |
| SMT | Surface Mount Technology |
| SiP | System-in-Package |
| SoC | System-on-Chip |
| SPE | Signal Processing Electronics |
| SRAM | Static Random-Access Memory |
| SSB-ASK | Single-Sideband Amplitude-Shift Keying |
| Sv | Sievert |
| SVC | Self-$V_{th}$ Cancellation |
| SVR | Smart Voltage Regulator |
| TA-GvHD | Transfusion-Associated Graft-versus-Host Disease |
| TID | Total Ionizing Dose |
| UHF | Ultra High Frequency |
| UWB | Ultra-Wide Band |
| VCR | Voltage Conversion Ratio |
| VM | Voltage Multiplier |
| VNA | Vector Network Analyzer |
| VNCAP | Vertical Natural Capacitor |
| $V_t$ | Transistor threshold voltage |
| $V_{th}$ | Alternative abbreviation to $V_t$ |
| WBCs | White Blood Cells |

# Chapter 1

# Introduction

## 1.1 Motivation

### 1.1.1 The Proliferation of Biomedical Sensors

The global market for medical sensors has experienced significant growth in recent years and is expected to continue growing at an accelerated rate. In fact, the global market demand for medical sensors is expected to increase more than 50% by the year 2016 compared to 2006 [1]. This trend can be attributed to both constant innovation in sensor system design and the proliferation of novel applications for sensors, including X-ray imaging and radiation dosimetry [2]. The latter category refers to sensors which measure X-ray and gamma radiation, also known as ionizing radiation [3]. These sensors are used in a variety of critical procedures, including radiotherapy for cancer treatment. In an effort to minimize costs, the medical industry has expressed growing interest over the use of inexpensive, silicon-based radiation dosimeters [4].

In addition to imaging and radiation sensors, there are many other kinds of medical sensors. For instance, biosensors are a rapidly growing subset of medical sensors

which include "analytical devices incorporating a biological material and either associated with, or integrated within, a physiochemical transducer or transducing microsystem" [5]. Sample applications of biosensors include: water quality control [6], cancer therapy [7], glucose monitoring [8], and *E. coli* detection [9]. Many biosensors are also examples of implantable sensors, which are inserted into the body of a human or animal subject. Consequently, the widespread adoption of medical sensors and biosensors has prompted the Institute of Electrical and Electronics Engineers (IEEE) to commence drafting a standard for the communication of sensors that operate within or near the human body. Named the "Body Area Network" (BAN) protocol, or IEEE 802.15.6, this standard is currently under development by the IEEE Standards Association [10].

All of the previously mentioned sensor systems include some degree of electronic circuitry powered by electricity. Therefore, an energy source is required. In the past, sensors predominantly used an electrochemical battery as a primary energy source. Contemporary sensors, however, are highly miniaturized and are required to operate for long periods of time without replacement. They may also measure and process multiple signals. Computational speed and wireless data rates are also increasing rapidly over time. Modern battery technology, meanwhile, has failed to maintain such a pace [11]. Lithium-ion batteries, for example, are ubiquitous among mobile commercial devices. However, despite dedicated research efforts, major improvements in energy density have proven elusive, and are predicted to remain so [12]. In lieu of the widening disparity between required and achievable energy storage in mobile devices, sensor designers are looking toward alternative sources of energy. This, in turn, has led to the rise of energy harvesting (EH).

Energy harvesting, otherwise known as power harvesting or energy scavenging, involves the harnessing of energy from an external source. The source may originate from the environment, such as wind, solar, thermal, and vibrational energy, or it may stem from a person or person's actions [11]. For example, an energy harvester was embedded within a shoe sole in [13]. During walking, the wearer's gravitational potential energy is converted into electrical energy via the piezoelectric effect. Alternatively, energy harvesters can be placed *in vivo*, as in [14], where an EH device was inserted into a knee replacement implant. Once again, the patient's knee movements were converted into electrical energy through the piezoelectric effect.

Beyond the aforementioned sources of energy exist synthetic sources. A burgeoning class of energy harvesters generates electricity by capturing electromagnetic (EM) energy from synthetic, human-made sources [15–17]. In large metropolitan areas, the vast majority of electromagnetic energy emanates from cellular and television broadcast stations. Since most of this energy lies in the radio frequency (RF) portion of the frequency spectrum, devices that harness this type of energy are known as RF energy harvesters [18].

RF energy harvesters are further classified according to the nature of the energy source being harnessed. The RF energy harvesters mentioned previously capture energy from communications signals propagating throughout the environment. These signals are destined for other devices and are not intended to be scavenged. Hence, the energy source is referred to as non-intentional, non-deliberate, or ambient. Conversely, if a dedicated transmitter specifically designed to deliver power wirelessly to an energy harvester is employed, then the energy source is considered to be intentional or deliberate [11]. Therefore RF harvesters are dichotomized as being either ambient or intentional energy harvesters.

Regardless of the origin or nature of the energy source, virtually all energy harvesters possess a common goal: optimal power conversion efficiency, or PCE. Non-ideal effects invariably exist during the energy conversion process. Energy harvesters, then, are never completely efficient. Thus, maximizing the conversion efficiency is of paramount importance in mobile and sensor applications.

In summary, energy harvesters represent a pervasive trend in sensors and mobile computing, where traditional sources of energy such as batteries are either replaced or supplemented by alternative energy obtained from environmental, biological, or synthetic sources. This is especially useful in mobile sensor applications, where longevity and remoteness from a power source are highly valued. In particular, medical dosimeters, which are used to measure ionizing radiation, are ideally suited for integration with an energy harvesting unit.

### 1.1.2 The X-Ray Dosimeter Project: A Brief History

The origins of wireless dosimetry research at Carleton University can be traced back to the mid-1980s, when Ian Thomson (of Thomson and Nielson Electronics Ltd.) approached the Department of Electronics seeking collaboration on novel floating-gate (FG) metal-oxide semiconductor field effect transistor (MOSFET) dosimeters. In the ensuing decades, the project advanced significantly, due to contributions by numerous graduate students and professors.

Early work on FG-MOSFET dosimeters began in the 1990s under Professor N. Garry Tarr and several collaborators. In 1996, the group of Ottawa researchers published their first paper on dosimeters. The paper demonstrated a novel FG-MOSFET, which was used for measuring gamma radiation. High sensitivity was

achieved through the use of a polysilicon gate extension over the field oxide, providing a sizable area for capturing the electric charge created by the impinging gamma rays. The first device was fabricated at Carleton University using a 5 $\mu$m n-type metal-oxide semiconductor (NMOS) process [19]. A second device was later fabricated using a 1.5 $\mu$m conventional complementary metal-oxide semiconductor (CMOS) process and published in 1998. This newer design was capable of achieving up to four times more sensitivity than the first prototype [20]. In the following years, further enhancements were made to the dosimeter, including the integration of the sensing and reference transistors. In addition, temperature compensation was added to ensure accurate measurements over a range of operating environments [21].

The next stage of research began during the 2000s, spearheaded by Ph.D. students Atif Shamim and Muhammad Arsalan, under the guidance of professors Langis Roy, Maitham Shams, and N. Garry Tarr. Building upon the successful demonstration of the radiation sensor, Shamim and Arsalan set out to explore the various architectural and packaging considerations of the wireless sensor. During their tenure at Carleton University, the pair of researchers developed novel System-on-Chip (SoC) and System-in-Package (SiP) transmitters and receivers specifically designed for MOSFET dosimeters. Their contributions include [22–25]:

1. A 5.2 GHz SoC transmitter with on-chip antenna, fabricated using the IBM (International Business Machines Corporation) 0.13 $\mu$m CMOS process.

2. A 5 GHz SoC receiver with on-chip antenna, fabricated using the IBM 0.13 $\mu$m CMOS process.

3. A SiP transmitter with in-package antenna, fabricated using a low temperature co-fired ceramic (LTCC) package.

4. A SoC MOSFET dosimeter with integrated signal processing electronics, fabricated using the DALSA 0.8 $\mu$m CMOS process.

This research marked a significant step forward for the wireless dosimeter project. In fact, in 2008, the research team at Carleton University formed a collaborative relationship with Best Medical Canada (which acquired Thomson and Nielson Electronics Ltd. in 2007). Best Medical, a prominent manufacturer of radiation measurement devices with a global reach, was interested in commercializing a wireless medical X-ray dosimeter for radiotherapy and blood sterilization applications.

Each year, countless medical operations involving blood transfusions are performed. To avoid patient infection and excessive immune response, the blood is often sterilized through X-ray irradiation. Modern blood sterilization systems are comprised of a blood irradiator unit and a radiation tag. A radiation tag placed on each blood bag changes in colour according to the amount of irradiation applied. After irradiation, a human operator assesses the tag to determine whether the blood is sufficiently sterile. This technique is prone to subjective measurement error and lacks certainty of the exact X-ray dose received. Furthermore, this method suffers from inherent operational and cost inefficiency, which frequently leads to the wastage of precious blood [26].

Recognizing these shortcomings, the Carleton University team, in collaboration with Best Medical Canada, initiated the third stage of dosimetry research in 2009. The ultimate goal involves the development of a completely integrated SoC wireless medical X-ray dosimeter for blood sterilization. An early, simplified system-level model of the dosimeter is depicted in Figure 1.1; the system features transmit and receive antennas, an energy harvesting unit for self-powered operation, an FG-MOSFET

which senses the received radiation dosage, a transmitter or modulator, and signal processing electronics. These modules are integrated on to a single integrated circuit (IC) which will be fabricated by IBM in a commercial 0.13 $\mu$m CMOS process.

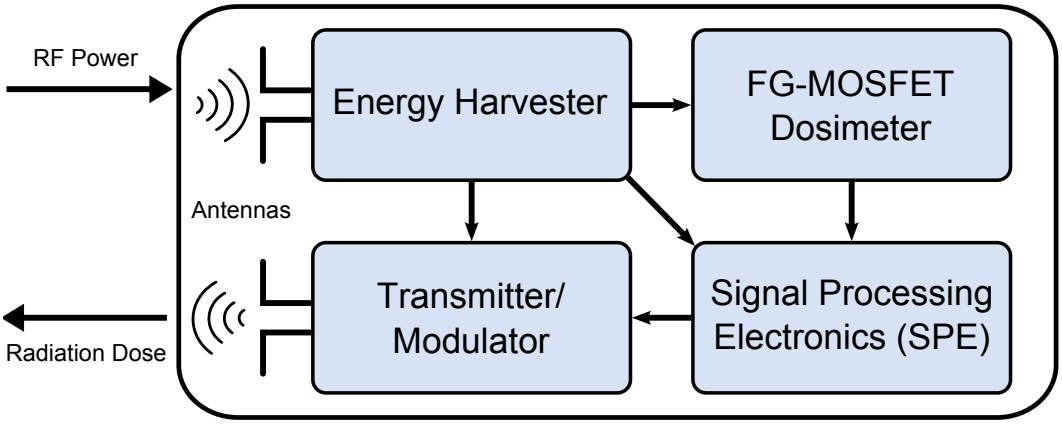


**Figure 1.1:** Simplified system diagram of the X-ray medical dosimeter project. This early model includes: transmit and receive antennas, an energy harvesting unit, the FG-MOSFET radiation sensor, signal processing electronics (SPE), and a transmitter or modulator. A detailed model is presented in Chapter 2.

To date, considerable progress has been made on the third stage of the project. An improved FG-MOSFET fabricated using IBM's 0.13 $\mu$m CMOS technology was demonstrated in 2012 by Behzad Yadegari as part of his Master's thesis [27]. In addition, using the same IBM technology, an RF energy harvester was designed, manufactured, and tested. The results of that work are presented in this thesis. Presently, Master's student Mohammadjavad Sheikhzadeh Nadjar is designing the signal processing electronics (SPE) necessary to interface the FG-MOSFET dosimeter with the transmitter sub-block. Behzad Yadegari, currently pursuing Ph.D. studies, is investigating the system-level integration of the entire sensor, including: SoC packaging, transmitter and receiver design, and in-depth analysis of a highly sensitive novel FG-MOSFET. The team at Carleton University is on target to deliver a working prototype, developed in a commercial CMOS process, by 2017.

## 1.2 Thesis Objectives

The X-ray dosimeter project owes its present state to the immense efforts of numerous researchers affiliated with Carleton University. Its scope is comprised of a multitude of electrical engineering research fields encompassing a vast breadth of knowledge. The work presented here focuses on the energy harvesting portion of the X-ray dosimeter project. The research objectives include:

1. A system-level analysis of wireless dosimetry.
2. The design of an energy harvesting module for the X-ray dosimeter project.
3. The implementation and optimization of a Dynamic $V_{th}$ Cancellation rectifier designed for:
   (a) A commercial 0.13 $\mu$m CMOS process.
   (b) High frequency operation (2.45 GHz).
4. A complete characterization of the Dynamic $V_{th}$ Cancellation rectifier.

## 1.3 Thesis Organization

The remaining sections of this thesis are organized as follows. Chapter 2 provides an overview of system-level concepts related to wireless dosimetry, with an emphasis on energy harvesting. Power and link budget analyses of the X-ray dosimeter project are also presented. Chapter 3 examines common energy harvesting techniques described in contemporary literature. With the relevant background knowledge sufficiently elaborated, an in-depth analysis of the Dynamic $V_{th}$ Cancellation rectifier is described in Chapter 4, including design, simulation, and optimization. Design considerations for the remaining portions of the energy harvesting module are also discussed. Chapter 5

presents the experimental results of the Dynamic $V_{th}$ Cancellation rectifier, followed by a discussion of the outcome. Finally, Chapter 6 provides a summary of the work presented, as well as a list of noted contributions. Suggestions for future work are also given. Appendix A provides additional mathematical analysis of backscatter modulation techniques.

# Chapter 2

# Wireless Dosimetry: System Considerations

Broadly speaking, this chapter serves two purposes. First, it provides an overview of relevant concepts related to wireless dosimetry. Secondly, this chapter presents a system-level overview of the wireless X-ray dosimeter project. The chapter concludes with an examination of energy-related design issues, including: energy source selection, power consumption, link budget allocation, and energy storage devices.

## 2.1 Medical Concepts

### 2.1.1 Properties of Blood

Blood is an essential bodily fluid which is responsible for a variety of functions. It serves as the medium in which nutrients (including oxygen) are transported throughout the human body. Conversely, it also transfers waste products to the liver and kidneys. Furthermore, blood is used to regulate body temperature and fight infection from foreign antibodies. Its clotting ability promotes coagulation and mitigates blood loss in cases of injury involving open wounds [28].

In total, the average human possesses five litres of blood [29]. This includes blood circulating throughout the veins, arteries, and capillaries [28]. Its pH level is strictly controlled to a range of 7.35 – 7.45. Since blood is composed mostly of water, its density is similar, at 1.06 kg/L [29]. Generally speaking, blood contains four basic components: red blood cells (RBCs), white blood cells (WBCs), platelets, and plasma. When all four components are present, it is referred to as "whole blood" [28].

RBCs, also known as erythrocytes, give blood its characteristic colour and are responsible for delivering oxygen throughout the body from the lungs, while also transporting carbon dioxide in the opposite direction. WBCs, or leukocytes, are a group of cells which fight infection; in essence, they contribute to an individual's immune response. Platelets, also known as thrombocytes, are responsible for the coagulation of blood. Finally, plasma serves as a transport mechanism for nutrients, waste products, and several other components. It consists mostly of water, fat, and sugar, and is yellow in colour [28]. These four components – RBCs, WBCs, platelets, and plasma – exist in proportion to one another as illustrated in Figure 2.1.

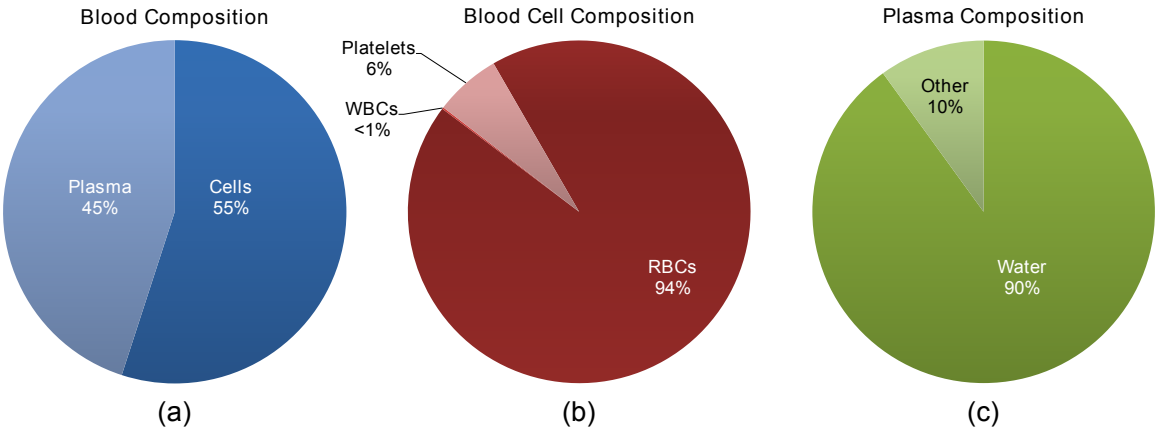


**Figure 2.1:** The composition of blood. (a) Blood is composed 45% of plasma and 55% of blood cells (*i.e.* RBCs, WBCs, and platelets). (b) The majority of blood cells are RBCs. (c) Plasma primarily consists of water. [30]

### 2.1.2 Blood Storage

In the healthcare industry, the transfusion of blood into a patient is required for numerous kinds of medical operations. Blood cannot be manufactured and therefore must be obtained through a network of generous volunteer donors. In the United States, 41,000 donations are required every day. Thus, a system of storage and management is essential to maintaining an adequate supply of blood [31]. Recently this system has experienced increased pressure, as the costs associated with blood transfusions rise and the base of available donors shrinks [32].

Blood may be stored as whole blood, although it is more commonly separated into its constituent components prior to storage. For example, RBCs, if stored separately under refrigeration, have a usable shelf life of several weeks (depending on the governing country's laws and the additives used). Blood is typically not stored at room temperature due to the fact that WBCs expire within 24 hours. When plasma is stored at freezing temperatures, it is referred to as "fresh frozen plasma" (FFP) [33]. Table 2.1 provides a summary of the common storage procedures used for a variety of blood products.

**Table 2.1:** Overview of blood storage procedures, describing the typical storage temperature and maximum duration for a variety of blood components [33–35].

| Blood Product | Storage Temperature Range | Maximum Storage Time |
|---|---|---|
| Whole Blood | Room temperature | 6–8 hours |
| RBCs | Refrigeration ($\sim 6\,^{\circ}\mathrm{C}$) | 35–49 days |
| | Frozen | 10 years |
| Platelets | Room temperature | 5 days |
| | Frozen | 1 year |
| Plasma | Refrigeration | 24 hours |
| | Frozen ($\leq -25\,^{\circ}\mathrm{C}$) | 2 years |

### 2.1.3 Blood Sterilization

The use of blood transfusions carries inherent risk, due to the plethora of fatal blood-borne diseases that exist. Therefore proper donor screening and sterilization are critical steps in the blood donation process. The most common types of diseases targeted for sterilization include: hepatitis B & C, syphilis, and various forms of the Human Immunodeficiency Virus (HIV) [36]. Numerous methods of sterilization exist. However, irradiation, in particular, is most commonly used for its efficacy against transfusion-associated graft-versus-host disease (TA-GvHD) [37].

As its name suggests, TA-GvHD originates from complications during blood transfusion. Although uncommon, the overwhelming majority of patients who acquire TA-GvHD will die. Therefore the sterilization of blood through irradiation is absolutely necessary. Blood irradiation involves the application of X-ray or gamma radiation to donated blood for the purposes of sterilization. If the appropriate amount of radiation is applied, the blood can be considered safe to use for transfusion [37].

Gamma radiation has historically been the dominant method of irradiation. However, medical facilities have recently begun to use X-ray irradiation units instead. This trend is primarily motivated by cost: X-ray-based irradiators, unlike those that rely on gamma rays, do not require any radioactive source material. Furthermore, on account of this, they do not require re-calibration as the source material decays [37].

Radiation can be quantified in many different ways. Today, less commonly used units include the roentgen (R) and rem. Most literature uses the sievert (Sv), the gray (Gy), or the rad (rad). For X-ray and gamma rays, the following relationship holds [38]:

$$1\ Sv = 1\ Gy = 100\ rad \tag{2.1}$$

In the United Kingdom, health guidelines specify the minimum dose of ionizing radiation to be 25 Gy within the volume of blood, while the maximum dose is set at 50 Gy (Canada and other countries adhere to similar guidelines) [37]. As noted in Chapter 1, blood is placed into a bag, and a 'tag' is attached to the bag. The tag, which is sensitive to ionizing radiation, changes in colour according to the amount of radiation received. A popular brand of tags include Ashland's Rad-Sure™ blood irradiation indicators, depicted in Figure 2.2. In contrast, the wireless X-ray dosimeter project does not depend on the judgement of a human operator to assess the dose, thereby improving radiation dose accuracy.

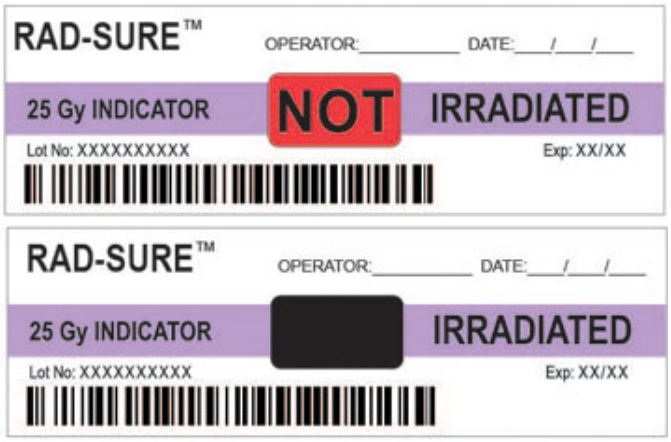


**Figure 2.2:** Ashland Rad-Sure$^{TM}$ blood irradiation indicator. If the minimum dose of radiation is received (*i.e.* 25 Gy), the tag will change colour, indicating that the blood bag is sufficiently irradiated [39].

Best Theratronics, which is located in Ottawa, Ontario, manufactures several blood irradiators for both research and commercial applications. Best Theratronics is part of Team Best, a consortium of companies which also includes Best Medical, the industry collaborator for the X-ray dosimeter project. Best Theratronics is a major competitor in the global blood irradiator industry. Its two commercial product lines, the Gammacell and Raycell brands, sterilize blood via gamma radiation and X-ray radiation, respectively [40, 41].

The Raycell Mk2, shown in Figure 2.3, features two X-ray tubes which emit radiation. Blood is transferred into blood bags and placed into either a 2.0 L or 3.5 L canister inside the machine. Either 300 mL or 600 mL of blood is contained in each bag. The Raycell Mk2 is capable of sterilizing between two and eight bags at a time, depending on which size of blood bags and canister are selected. X-ray radiation must be applied for at least 3.8 or 5.7 minutes to achieve the required 25 Gy of radiation, depending on which canister is chosen. Dose uniformity varies between 1.8:1 and

1.5:1. This is noticeably less than the Gammacell units, and a particular downside for hospitals looking to switch to X-ray irradiators to save cost. However, if wireless X-ray dosimeters are employed, then dosage uniformity may be monitored accurately and in real-time throughout the procedure [40, 41].

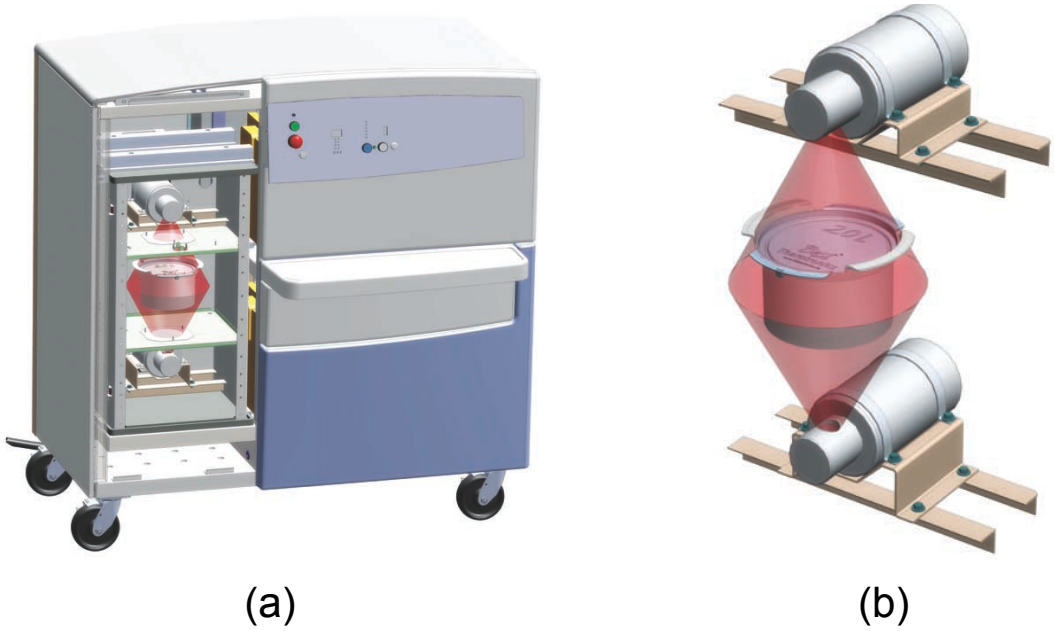


**Figure 2.3:** (a) Best Theratronics Raycell Mk2 blood irradiator unit. (b) The Raycell Mk2 uses opposing X-ray tubes which apply radiation to the blood bags contained within the inner canister [41].

### 2.1.4 Biological Effects of RF Radiation

The potential effects of RF and microwave radiation on biological systems has been studied for over six decades. As the number of wireless consumer devices continues to grow, so does the quantity of RF and microwave radiation permeating the atmosphere. This has caused concern among the general public, who are worried that exposure to RF/microwave radiation is harmful. This section seeks to clarify the relationship between electromagnetic radiation and biological systems.

First, it is important to distinguish between two main categories of electromagnetic radiation. Radiation which contains enough energy to ionize an atom – that is, to liberate an electron from an atom – is classified as "ionizing radiation." X-rays and gamma rays are both examples of ionizing radiation. Due to their ability to alter the chemical structure of molecules, X-rays and gamma rays are dangerous to biological systems. Ionizing radiation can lead to cell mutation, and consequently, cancer [42].

Radiation which lacks the required energy to induce ionization is referred to as "non-ionizing radiation." RF and microwave radiation falls under this category. Due to its lower energy, this type of radiation has a comparatively limited effect on matter. In the presence of non-ionizing radiation, matter undergoes thermal heating as atoms experience increased vibrational energy. The degree of heating experienced depends on the intensity of the electromagnetic field [42].

Biological systems, however, are composed of complex molecules and governed by intricate processes. Hence, there is a greater risk that exposure to RF/microwave radiation will result in negative effects. For decades, researchers have sought to determine whether such effects exist. Unfortunately, consensus remains elusive. As noted in [42], an exhaustive review of hundreds of studies yielded contradictory or inconclusive results. The authors of the review cite a high degree of variability among experiments as the likely cause of discrepancy. Across the experiments, a variety of signals were used, each with different modulation schemes, frequencies, and power levels. Environmental conditions also varied considerably. Furthermore, some studies used animals such as rats as test subjects. However, the effects of RF radiation do not scale well from rats to humans [42].

Studies examining the effects of RF radiation on blood are also mixed. Some researchers have found that an organism's WBC count tends to decrease from prolonged exposure to RF/microwave radiation [43, 44]. However, the researchers note that these results remain "consistent with normal physiological responses to systemic temperature fluctuation" [44]. There exists evidence that RBCs may also be susceptible to RF/microwave radiation. In [45], researchers found that exposure to low-power RF/microwave radiation led to an increase in hemolysis, or the destruction of RBCs. Conversely, a comprehensive analysis from fundamental principles was conducted in [46]; the author claims to have shown that RF/microwave radiation cannot, by the principles of physics and biology, affect biological systems if the intensity of electromagnetic radiation remains below 10 $mW/cm^2$ [46].

More recently, the United States Food and Drug Administration (FDA) granted approval for the use of radio frequency technology to track blood products in medical facilities. Researchers at the University of Wisconsin-Madison spent six years testing their design prior to gaining approval. During this time, the researchers claimed to have witnessed no negative effects from RF radiation on blood [47].

In conclusion, there exists conflicting evidence that exposure of blood to RF/microwave radiation produces negative effects. Studies which support such claims show only minor effects which are neither harmful or concerning. Therefore the X-ray dosimeter project, which uses RF electromagnetic waves, poses no threat to the blood which it measures.

## 2.2 RFID Principles

### 2.2.1 Introduction to RFID

Radio frequency identification, or RFID, refers to a ubiquitous class of wireless devices used in a variety of industries for managing, tracking, and identifying objects. For example, RFID technology is employed in electronic toll collection for highways, as well as restricted parking areas. It is also used by retailers to prevent store theft and track the distribution of merchandise from warehouses to stores [48].

All RFID systems are composed of two elements: a "reader" and a "tag." The tag, or transponder, is attached to an object that is required to be tracked. Real-world applications involve multiple objects, each with its own tag. Every tag features a unique identity which is used to distinguish one tag (or object) from another. A reader is used to interrogate or assess a tag based on its identity (ID). Upon interrogation, a tag may convey its identity, a sensed value, or some other type of information [48].

RFID tags are further divided into three classes: passive, semi-passive, and active. Passive tags do not have an internal energy source; in other words, they are "batteryless." Instead, energy is captured from an RF signal sent by the reader. Backscatter modulation (discussed below) is commonly employed to transmit information back to the reader. Due to their batteryless nature, passive tags contain relatively simple circuitry and often lack power-consuming RF components such as power amplifiers and transmitters. The primary advantages of a passive tag include a long operating life and low production cost. However, passive tags suffer from poor operating range, low data rates, and poor reliability [48].

Active tags, on the other hand, are self-powered devices capable of operating over much longer distances and at higher data rates. They are more characteristic of typical RF transceivers than passive tags, usually featuring amplifiers, frequency mixers, oscillators, and transmitters. This additional circuitry comes at the price of higher production cost and a comparatively short operating life. Tags which combine properties of active and passive devices are called "semi-passive" tags; these tags often feature a battery, but may also use backscatter modulation to reduce energy requirements. A typical RFID system is shown in Figure 2.4. First, the reader transmits a signal to provide information and (in some cases) power to the tag. This is referred to as the downlink or forward link. Next, the tag is powered on and transmits some information back to the reader. This is referred to as the uplink or reverse link; when backscatter modulation is employed, it is also called the backscatter link [48].

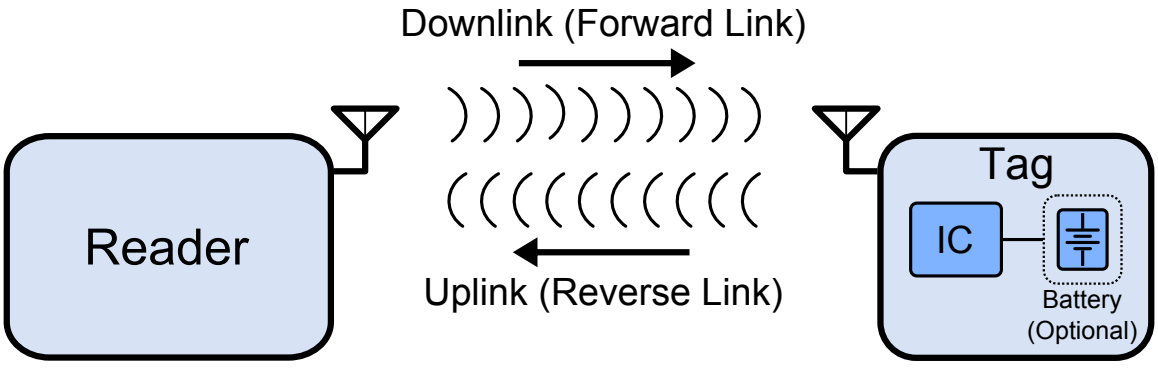


**Figure 2.4:** A typical RFID system. The tag is composed of an IC and (optionally) a battery. The circuitry contained within the IC depends on the classification of the tag. Passive tags require relatively simple circuitry, while active tags resemble classical RF transceiver architectures [48].

RFID readers, meanwhile, are classified according to their antenna configuration. If a single antenna is used to both transmit and receive data, the reader is referred to as monostatic. However, if separate antennas are employed, then the reader is classified as bistatic. Monostatic readers, though less expensive, suffer from comparatively

low receiver sensitivity. This is especially true in systems employing backscatter modulation. To understand why, consider a situation where a reader communicates with a passive tag. The reader must operate in full-duplex mode, simultaneously listening for the tag's response while supplying power to the tag. Using backscatter modulation, the tag transmits its data using the same frequency as the downlink signal (for more detail, see Section 2.2.4). Therefore, the reader may not use a duplexer to provide suitable isolation between its transmitter and receiver (however, most monostatic systems employ circulators, which offer a small amount of isolation). The preclusion of a duplexer results in significant power leakage from the transmitter into the receiver, effectively limiting the reader's sensitivity to weak signals. On account of this, many designers prefer to use a bistatic design which affords the reader an inherent degree of isolation between its transmitter and receiver [48].

### 2.2.2 Coupling Mechanisms

There exists two distinct mechanisms for wirelessly transferring electromagnetic energy from one device to another. In RFID systems, the mechanism employed depends on the operating range and size of the antenna relative to the wavelength of the signal. Recall that the wavelength of an electromagnetic wave is related to its frequency by [49]:

$$\lambda = \frac{c}{\sqrt{\epsilon_r}\, f} \tag{2.2}$$

Here, $\lambda$ represents the wavelength, $f$ corresponds to the frequency of oscillation, $c$ represents the speed of light (approximately $2.998 \times 10^8$ m/s in a vacuum), and $\epsilon_r$ denotes the relative dielectric permittivity of the medium in which the electromagnetic wave propagates [49]. If the wavelength of the transmitted signal from the reader is

very large compared to the tag's antenna, then the RFID system likely uses inductive coupling. In this case, the reader and tag are operating within each other's near-field region, a radiation area dominated by complex EM field patterns. The energy in this zone is mostly concentrated near the antenna and rapidly diminishes with increasing distance from the source (by a factor of the cube of distance). Information exchange is nearly instantaneous, though the energy absorbed by the tag directly affects the reader (and vice versa). Furthermore, inductively-coupled RFID systems have a very limited range. However, they are considered comparatively reliable; either the tag is visible and transmits successfully, or it is out of range and does not transmit at all. A typical inductively-coupled RFID system is shown in Figure 2.5 [48].

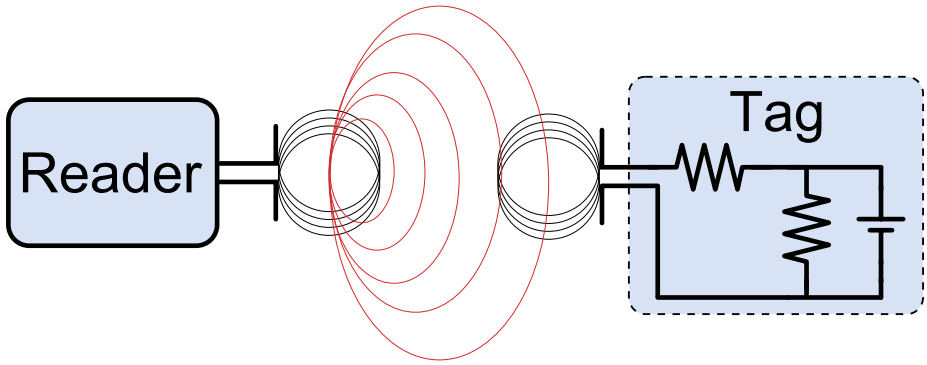


**Figure 2.5:** A sample RFID system which uses inductive coupling to transfer information from the reader to the tag. The tag is represented by its equivalent circuit [48].

Conversely, if the wavelength is comparable to the size of the antenna, then the RFID system likely uses radiative coupling. When radiative coupling is employed, an electromagnetic field is propagated from the reader uniformly outwards through space. The reader and tag are operating in the far-field region. This region is characterized by a uniform electromagnetic field whose power fades by the square of the distance from the source. Therefore, radiative-coupled RFID systems can operate over much longer distances than inductively-coupled systems. Furthermore, the amount of radiation

absorbed by the tag does not affect the reader. However, as the EM field propagates radially outward from the antenna, the environment and nearby objects create many undesirable effects, including: attenuation, reflection, refraction, and absorption. Due to this behaviour, these systems are considered less reliable than those which are inductively-coupled. Figure 2.6 illustrates an example of a radiative-coupled RFID system [48].

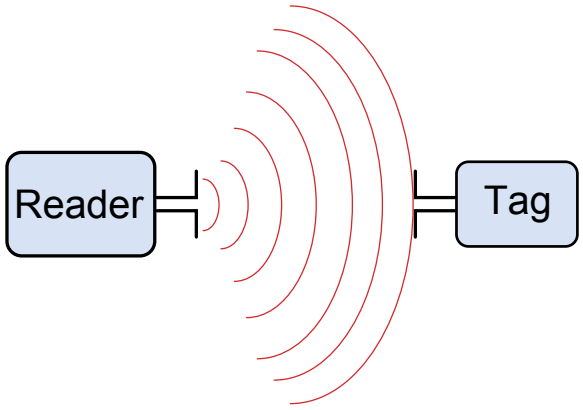


**Figure 2.6:** An example RFID system which uses radiative coupling to transfer information from the reader to the tag. Shown in red is the electromagnetic wave emitted by the reader. The EM wave propagates radially outwards and is often distorted by the environment and nearby objects [48].

### 2.2.3 Downlink Communication: Reader to Tag

In most passive and semi-passive RFID systems, downlink communication is comprised of two stages. During the first stage, the reader transmits a signal containing information to the tag. This information may consist of commands or data for the tag and is usually transmitted using amplitude modulation (AM), or some variant thereof. Compared to other, more complex modulation schemes, AM is relatively simple to demodulate. This enables RFID tags to receive information using minimal circuitry and consequently very little power [48].

The most commonly used form of AM is amplitude-shift keying (ASK), a digital modulation technique. ASK-modulated information is represented by one of two binary symbols, each consisting of a sequence of one or more pulses of the carrier signal. Two distinct amplitude levels are used to distinguish between a binary '0' and a '1.' A special case known as on-off keying (OOK) arises when a binary 0 is represented by the absence of pulses. OOK modulation is not suitable for passive RFID systems, since a sequence of zeroes will result in the tag receiving zero power and thus powering off. However, this issue may be mitigated through data coding. Pulse-interval encoding (PIE), for example, is commonly employed to improve the consistency of power delivered to the tag. In PIE, all symbols are encoded using a combination of both low and high amplitude states. To distinguish between states, the width of the high-amplitude portion is adjusted. Other ASK derivatives, such as single-sideband ASK (SSB-ASK) and phase-reversal ASK (PR-ASK), are used to improve spectral efficiency [48].

Some RFID systems, however, do not employ any downlink modulation. When no information is required by the tag, the first stage of downlink communication is omitted. During the second stage, the reader transmits an unmodulated continuous wave (CW) to the tag. In systems that use backscatter modulation, this waveform is received by the tag, modulated, and reflected back to the reader. If backscatter modulation is not used, then the second downlink stage may be omitted [48].

### 2.2.4 Uplink Communication: Tag to Reader

Unlike downlink communication, uplink communication always involves the transfer of data from the tag to the reader, and therefore requires modulation. The type of modulation employed depends on the classification of the tag. Active tags, which

contain RF transceiver circuitry, often take advantage of more efficient, though complicated, modulation schemes such as quadrature amplitude modulation (QAM) or quadrature phase-shift keying (QPSK). Non-active tags, on the other hand, usually employ a special technique known as backscatter modulation [48].

### Backscatter Modulation

Backscatter modulation is a technique used in passive and semi-passive RFID tags, which usually lack a transmitter and battery. As mentioned earlier, an RFID reader transmits a CW tone, which is received by the tag's antenna. However, if the impedance of the antenna is not well matched to that of the tag's circuitry, a portion of the captured RF energy will be reflected back into the medium. By varying the load impedance that is presented to the antenna, it is possible to modulate the amplitude and/or phase of the reflected signal. This is illustrated in Figure 2.7(a), where a switch is employed to vary the impedance seen by the antenna between the two values $Z_1$ and $Z_2$ [48, 50].

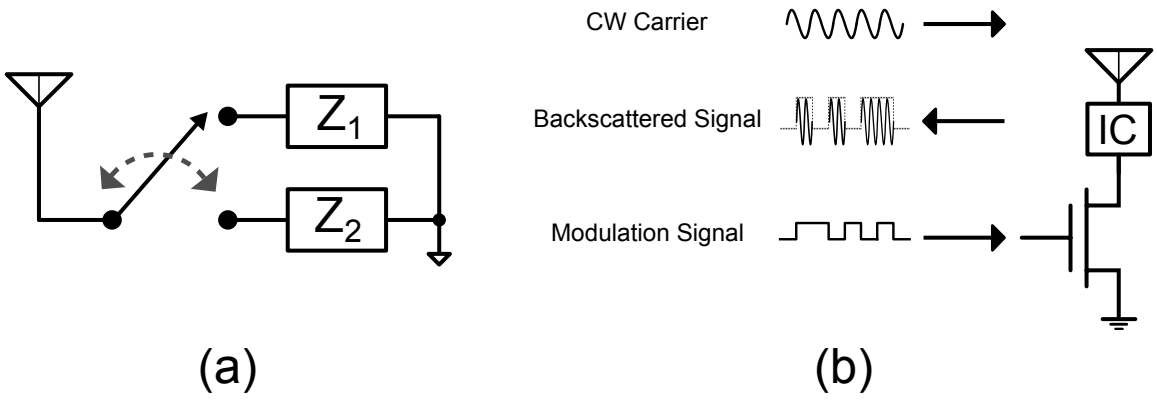


**Figure 2.7:** A simplified depiction of backscatter modulation. (a) A switch is used to vary the impedance seen by the antenna between two values, effectively modulating the carrier [50]. (b) The switch may be implemented using a single MOSFET transistor. The tag's IC receives power only when the switch is closed.

The simplest way to implement the impedance switching action involves the use of a transistor operating as a switch, as shown in Figure 2.7(b). By modulating the gate voltage, the transistor's operation toggles between a short circuit and an open circuit (ignoring non-ideal effects for now, such as leakage and on-resistance). In the open-circuit state, no current flows and therefore the tag's IC receives no power. Furthermore, since no current circulates through the antenna, no EM field will be generated, and hence no backscattered signal is produced (in reality, the antenna may reflect a negligible amount of RF energy incident upon it [51]). In the short-circuit state, the tag's IC will receive power and a backscattered signal will be generated. In this simple example, toggling between these two states produces an ASK-modulated signal on to the CW carrier, which is then reflected back towards the reader [48].

Backscatter modulation is advantageous for several reasons. Most importantly, the tag's circuitry does not need to operate at high frequency: the tag simply modulates information on to the CW carrier provided by the reader. In many RFID systems, information bandwidth is quite low, on the order of hundreds of kilohertz. Thus, transistors with slower performance may be used, thereby minimizing production cost [48].

### Backscattering Methods

In addition to Figure 2.7(b), there exist several other methods which are used to produce a modulated backscattered signal. In Figure 2.7(b), it is assumed that the antenna is conjugately matched to the IC to provide optimum power transfer. Therefore the impedance as seen by the antenna alternates between an open circuit and a matched load. A second method involves placing the switch in parallel with the IC, so that the antenna is presented with either a short circuit or a matched

load. Further still, in some cases the IC is placed in series with a load, consisting of a switch in parallel with a "modulation" resistor. This method, known as resistive ASK, ensures that some amount of power is always supplied to the IC. Using this technique, the amplitude of the backscattered signal is modulated via the switch and modulation resistor [48].

Thus far, all of the backscattering methods discussed involve varying the amplitude of the reflected signal by changing the resistance seen by the antenna. In reality, however, backscatter modulation is achieved by varying the reflection coefficient of the load presented to the antenna. Since the load impedance is a complex quantity, it is also possible to vary the load reactance, thereby phase-modulating the backscattered signal. In contrast to resistive modulation, varying the reactive component of the load does not significantly change the power delivered to the IC between states. This approach is referred to as phase-shift keying (PSK) [48].

### Backscatter Power Availability

One of the most important issues to consider when designing passive RFID tags is the apportioning of available power between the tag's IC and the amount to be backscattered. Table 2.2 presents a summary of achievable IC and backscatter power for the four methods discussed. It is assumed that each binary state occurs with equal repetition, and no additional data coding is used. As can be seen, resistive ASK results in a modest increase in IC power compared to the other ASK methods; however, substantially less backscattered power is obtained. PSK, meanwhile, is shown to be a highly efficient backscattering method. It is also possible to achieve constant IC power using PSK modulation. A detailed mathematical analysis of each technique is provided in Appendix A.

**Table 2.2:** Summary of achievable backscatter and IC power for each backscattering method. All powers are expressed with respect to $P_{Rx}$, the available power at the tag's antenna when no modulation is used, and when the tag's IC and antenna are conjugately matched. It is assumed that both binary states occur with equal repetition. For derivations of these expressions, see Appendix A [48].

| **Backscatter Method** | **Backscattered Power** | **IC Power** |
|---|---|---|
| Open-Matched Load ASK | 0.5 $P_{Rx}$ | 0.25 $P_{Rx}$ |
| Short-Matched Load ASK | 0.5 $P_{Rx}$ | 0.25 $P_{Rx}$ |
| Resistive ASK | 0.22 $P_{Rx}$ | 0.28 $P_{Rx}$ |
| PSK | 0.32 $P_{Rx}$ | 0.4 $P_{Rx}$ |

### Subcarrier Modulation

As explained earlier, backscatter modulation is accomplished through amplitude or phase modulation. However, amplitude modulation (of the uplink channel) is usually avoided due to poor immunity to noise. In a passive RFID system, the reader generates a CW carrier while simultaneously receiving information from the tag. This CW tone will result in significant reflections from nearby objects and other tags. Furthermore, the CW tone and backscattered signal share the same frequency. Therefore, uplink communication (from reader to tag) must occur in the presence of substantial noise. The signal received by the reader's antenna is comprised of the vector sum of this noise in addition to the backscattered signal. If ASK is employed, the amplitude of the backscattered signal may become sufficiently distorted by the time it is received by the reader, resulting in bit errors [48].

Consequently, most RFID tags implement an additional layer of modulation known as frequency-shift keying (FSK). This digital modulation technique represents each binary state using a different frequency. Unlike amplitude and phase, the frequency

of a transmitted signal remains unaffected by non-ideal propagation effects such as fading and reflection. Thus, coding the number of state changes (*i.e.* the frequency), as opposed to the magnitude of state changes (*i.e.* the amplitude and phase), provides for improved communication reliability. During uplink communication, FSK and ASK are often used in combination: FSK is used to reliably transmit information, while ASK is used for data encoding (*e.g.* Non-Return to Zero (NRZ), Manchester encoding) [50].

The combination of FSK and ASK modulation is sometimes referred to as subcarrier modulation. To understand why, consider Figure 2.7(b). By varying the switching frequency of the transistor, the amplitude-modulated carrier signal is further frequency-modulated, resulting in the following subcarrier signals [50]:

$$F_{Sub,1} = F_c \pm F_{0,1} \tag{2.3}$$

$$F_{Sub,2} = F_c \pm F_{0,2} \tag{2.4}$$

In Equations 2.3 & 2.4, each subcarrier, $F_{Sub}$, consists of the sum and difference of the CW carrier frequency, $F_c$, and the switching frequency, $F_0$. This example illustrates FSK modulation, since two distinct switching frequencies are used. Subcarrier or FSK modulation of backscattered signals requires relatively simple circuitry to implement. However, compared to dedicated ASK, data rates are considerably slower [52].

### 2.2.5 Frequency Considerations

The majority of RFID systems operate within unlicensed/unallocated frequency bands officially known as Industrial, Scientific, & Medical (ISM) bands. ISM bands are governed by the International Telecommunication Union (ITU) and are recognized internationally. A summary of commonly used bands is provided in Table 2.3. This includes bands within the Low Frequency (LF), High Frequency (HF), and Ultra High Frequency (UHF) ranges. With the exception of 125–134 kHz, all of the listed frequencies are ISM bands. To differentiate between the two UHF bands, RFID systems operating in the 2.4–2.5 GHz band are sometimes referred to as microwave readers. The frequency band that an RFID system operates within has a significant influence on the design of the system, especially the antenna. For example, higher frequencies allow for smaller antennas. However, due to the skin effect, signals at higher frequencies do not penetrate as far through materials or objects; this is especially important in situations where a direct line-of-sight does not exist between the reader and tag. These considerations are discussed in further detail in the following section regarding the X-ray dosimeter system [48, 53, 54].

**Table 2.3:** Frequency bands commonly used by RFID systems [48, 53, 54].

| **Frequency Band** | **Frequency Range** | **ISM Band** |
|---|---|---|
| LF | 125 – 134 kHz | No |
| HF | 13.553 – 13.567 MHz | Yes |
| UHF | 902 – 928 MHz | Yes |
| UHF (Microwave) | 2.4 – 2.5 GHz | Yes |

### 2.2.6 RFID in Blood Bag Management

Over the past several years, a number of countries have begun testing RFID-based blood management systems. These systems are targeted toward different points along the blood supply chain, from donor extraction to patient transfusion. They are primarily intended to replace the existing barcode-based systems currently used today. In most cases, passive tags operating in the HF or UHF frequency range are used. Some facilities process up to 60,000 units of blood annually. Through the use of RFID-based solutions, hospitals are able to ease the tracking of blood products, minimize costs, and avoid mismanagement due to human error. Table 2.4 summarizes a number of RFID integration experiments around the world [55–61]. In fact, RFID-based blood management solutions are becoming so popular in hospitals that Vox Sanguinis, the International Journal of Blood Transfusion Medicine, published a draft document which sets forth a series of guidelines for the use of RFID technology in blood management systems. The document suggests a standard based on passive HF 13.56 MHz RFID tags [62].

**Table 2.4:** A summary of several RFID-based blood management trials around the world.

| Year | Country of Origin | Blood Product | Tag Frequency | Reference |
|---|---|---|---|---|
| 2004 | United States | Various | 13.56 MHz | [55] |
| 2006 | United Kingdom | WBCs | Not Specified | [56] |
| 2006 | Germany | Whole Blood | 13.56 MHz | [57] |
| 2007 | Italy | Whole Blood | 860–960 MHz | [58] |
| 2007 | France | RBCs | 13.56 MHz | [59] |
| 2010 | Balearic Islands | FFP (Plasma) | 860–960 MHz | [60] |
| 2010 | United States | Blood Cooler Boxes | Not Specified | [61] |

## 2.3 The X-Ray Dosimeter Project: System Development Overview

The X-ray dosimeter project was introduced in Chapter 1, followed by a cursory review of the project's history. In this section, the current development status of the X-ray dosimeter is presented in further detail. First, the dosimeter's system concept and operating environment are discussed. Second, the dosimeter tag is examined, including its operating conditions, specifications, and various sub-blocks. Lastly, a preliminary discussion of the dosimeter reader is presented.

### 2.3.1 Dosimeter System & Operating Environment

The X-ray dosimeter project is a collaboration between Carleton University researchers and Best Medical Canada. The primary goal is to design a wireless dosimeter tag for blood bags. This tag is intended to be part of a larger RFID-based solution for blood bag management. Instead of a barcode label, each blood bag will be attached with an RFID tag featuring an integrated X-ray dosimeter. This dosimeter measures the amount of ionizing radiation received during blood sterilization procedures. Presently, it is being targeted for use inside the Best Theratronics Raycell Mk2 blood irradiator unit, shown previously in Figure 2.3.

#### Dosimeter System

The dosimeter system, illustrated in Figure 2.8, is comprised of a portable reader and up to eight tags, depending on the size of the blood bags and the model of canister selected. The reader is placed inside the Raycell Mk2, near the irradiation chamber. A small opening in the side of the chamber would enable the reader to communicate with the tags from a distance of up to one metre away through radiative coupling.

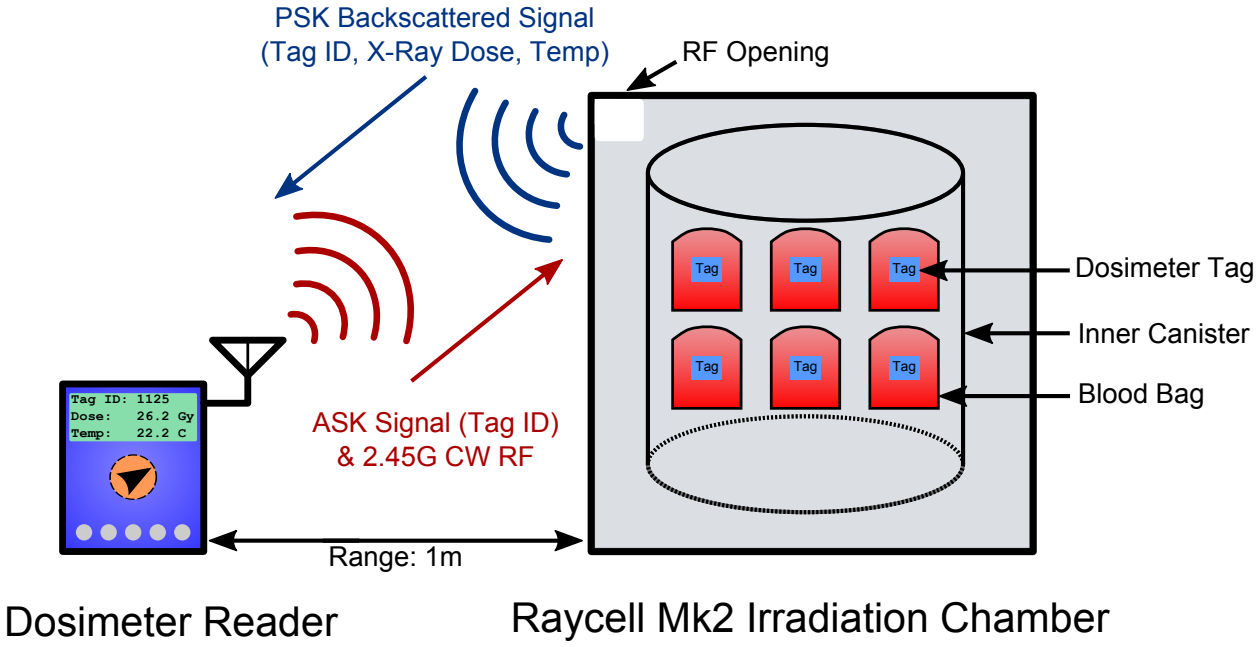


**Figure 2.8:** Proposed system-level overview of the X-ray dosimeter project. Blood bags are affixed with RFID dosimeter tags and placed in the irradiation chamber. A reader, placed inside the Raycell Mk2, measures the dosage of the RFID tags through a small opening in the side of the chamber.

Every dosimeter tag is uniquely identified by an ID value which is hard-coded into the tag's IC. To communicate with a specific tag, the reader transmits a UHF 2.45 GHz ASK-modulated signal containing the ID value of the tag it wishes to interrogate. Consequently, each tag inside the Raycell Mk2 demodulates this RF signal and compares the received ID value to its own ID. If the ID values match, the tag transmits its ID, sensed X-ray dose, and measured temperature to the reader using backscatter modulation. The reader establishes a backscatter link by broadcasting a 2.45 GHz CW carrier tone. During uplink communication, the specified tag modulates its data on to this CW carrier using PSK modulation, and reflects the signal back to the reader.

The remaining tags, which do not transmit data (because their IDs do not match the ID value transmitted by the reader), enter a special energy harvesting (EH) mode. In this mode of operation, tags collect energy from the reader's CW signal using their integrated energy harvesting circuitry; the harnessed energy is then stored in the tag's energy storage device. Thus, the dosimeter tags are categorized as RF energy harvesting devices whose energy source is an intentional microwave UHF signal.

### Operating Environment

Since blood bags are used in a variety of medical environments (including hospitals, storage refrigerators, and blood irradiation rooms), the X-ray dosimeter system must be highly adaptable to its environment. To achieve this level of versatility, the dosimeter reader would require two distinct modes of operation. In one mode, the dosimeter reader would be placed inside the Raycell Mk2 (but external to the irradiation chamber), as shown in Figure 2.8. This would allow for real-time monitoring of received X-ray dosage levels during the sterilization process. In the second mode, the reader would operate outside of the Raycell Mk2. This would enable the interrogation of tags while blood bags are transported to, or stored in, various medical facilities. In either mode, the operating range of the tags is desired to be (up to) one metre.

### Propagation Environment

When used inside the Raycell Mk2, the X-ray dosimeter system is subjected to a unique operating environment, as shown in Figure 2.9. It is clear from this figure that the reader may not possess a line-of-sight path with the tags. In addition, the Raycell Mk2 features a metallic enclosure, while blood is largely comprised of water (which is highly effective at absorbing RF radiation). Furthermore, polarization mismatches inevitably exist between the incident RF signal and the physical orientation of the

tag antennas. In combination, these factors will severely limit the operating range if the reader is placed external to the blood irradiator unit [48]. Therefore, if possible, the reader should be placed inside the machine.

**Figure 2.9:** Best Medical Raycell Mk2 blood bag canister. Blood is stored in 300 mL or 600 mL bags. Up to eight bags may fit into the canister, depending on the configuration [41].

### Tag Operating Range

Ultimately, the operating range of the tags will be limited by federal regulations governing maximum transmit power. In Canada, digitally modulated transmitters operating in the 2.4–2.5 GHz UHF ISM band are limited to 1.0 W of peak transmit power or 4.0 W of effective isotropically radiated power (EIRP) [63]. However, this regulation may be bypassed if the reader is confined to operate within the Raycell Mk2, which is presumably highly shielded. Nonetheless, if the reader is to be versatile and used in various medical environments such as blood storage freezers and refrigerators, then the aforementioned regulations must be followed.

**Ionizing Radiation Effects on CMOS Electronics**

During the irradiation process, dosimeter tags placed inside the Raycell Mk2 will receive similar amounts of ionizing X-ray radiation compared to the blood bags (relative to their respective sizes). CMOS electronics may exhibit negative effects when exposed to high-energy radiation, such as X-rays. Fortunately, these effects are well-studied. The science of mitigating these effects is known as radiation hardening [64].

High-energy radiation effects in integrated circuits are divided into two categories. Prolonged exposure to high-energy radiation is measured by the total ionizing dose (TID) received. When exposed to a high lifetime TID, ICs are subjected to permanent damage [64]. In CMOS processes, high-energy radiation results in an accumulation of charge in the oxide layer. This consequently affects the manner which MOSFETs operate in a number of ways, including changes to the threshold voltage and channel mobility. TID-related damage occurs gradually over time [65]. However, this damage may be minimized through the use of significant radiation shielding [64].

Single-event effects (SEEs) are a second category of high-energy radiation effects which include the following errors: single-event upset (SEU), single-event latchup (SEL), and single-event transient (SET). SEEs are classified as "soft" errors and usually result in the changing of a logic state in digital circuits (including sequential and combinational circuitry). Unlike high TID, SEEs do not lead to permanent damage, and may often be resolved by simply resetting the circuit [64]. A variety of radiation-hardening techniques exist at the system, circuit, and device levels, and are discussed in [66].

In conclusion, the X-ray dosimeter project may exhibit susceptibility to TID-related damage. However, no adverse effects were discovered by other team members during

testing of the FG-MOSFET sensor and read-out circuitry. Nonetheless, extensive radiation testing of the entire dosimeter tag is required.

### 2.3.2 Dosimeter Tag Overview

The X-ray dosimeter tag is a low-cost, low-power RFID-based sensor. In order to minimize production cost, a SoC design using IBM's commercial 0.13 $\mu$m CMOS process was chosen. The tag is a semi-passive design, employing backscatter modulation and RF energy harvesting to ensure minimal power consumption. A system-level diagram of the tag is shown in Figure 2.10, followed by a discussion of each sub-block.

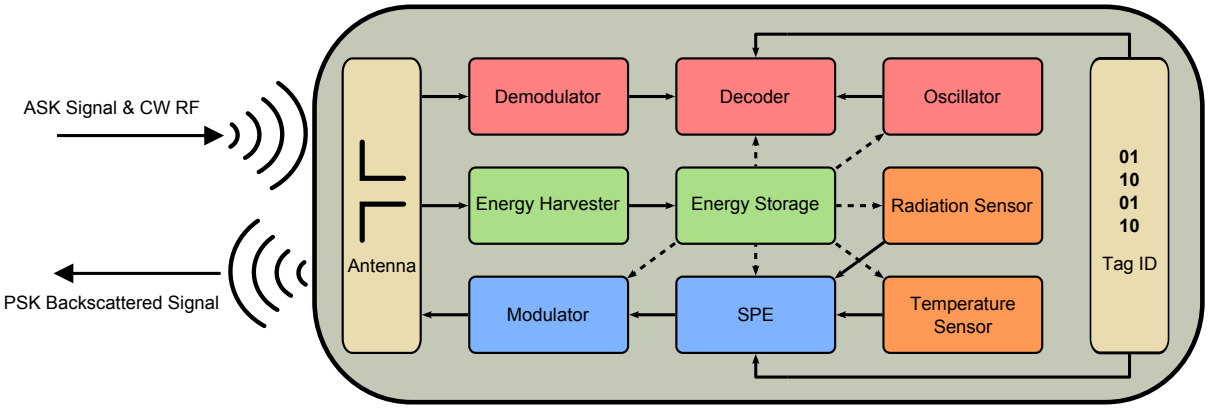


**Figure 2.10:** System-level diagram of the X-ray dosimeter tag. The sub-blocks are colour-coded to emphasize their shared functionality: red corresponds to demodulation circuitry, green represents energy harvesting and storage components, orange corresponds to sensors, and blue signifies modulation circuitry. The antenna and tag ID are used by multiple sub-blocks.

#### Radiation Sensor

The dosimeter tag features an on-chip X-ray dosimeter implemented using FG-MOSFET technology. A pair of FG-MOSFET transistors sense the received X-ray radiation dosage, and, using integrated read-out circuitry, convert the sensed dose to a voltage. This circuit does not require power in order to sense the received dose; power

is consumed only when the dosage is read by the tag. To achieve high sensitivity, a sizable voltage range of ± 0.9 V is used. In its current implementation, the FG-MOSFET dosimeter and its read-out circuitry consumes approximately 135 $\mu$A of current and 243 $\mu$W of power. This sub-block was designed by Behzad Yadegari as part of his Master's thesis [27]. Presently, further attempts are being made to both minimize power consumption and improve sensitivity.

**Temperature Sensor**

Blood bags are routinely moved into and out of low-temperature storage. To avoid expiry, the temperature of each bag must be monitored. Therefore, the dosimeter tag will feature an integrated temperature sensor. Numerous low-power temperature sensor designs have been published, such as [67], which achieves sub-$\mu$W power consumption in a standard 0.18 $\mu$m CMOS process. In 0.13 $\mu$m CMOS, a ring oscillator-based temperature sensor which consumes only 95 nW of power was reported by [68]. In addition, an RFID-based temperature sensor was designed in [69] using a standard 0.13 $\mu$m CMOS process; the entire design, which uses RF energy harvesting similar to the dosimeter tag, consumes 8.5 $\mu$W during operation. Therefore, it is presumed that the dosimeter tag's temperature sensor will consume less than 10 $\mu$W of power.

**Energy Harvester & Energy Storage**

The dosimeter tag employs a dual power source configuration, consisting of an RF energy harvester and an energy storage device. Similar to passive RFID systems, the tag harnesses energy from a CW RF tone transmitted by the reader at 2.45 GHz (*i.e.* directly in the centre of a UHF ISM band). The incident RF wave is rectified to a direct current (DC) voltage, which is used to charge the energy storage device. When sufficiently charged, the storage device supplies power to each of the tag's sub-blocks.

The following chapters of this thesis are devoted to discussion of the energy harvesting module.

### Demodulator, Decoder, & Oscillator

Every dosimeter tag must compare the ASK-modulated signal transmitted by the reader to its own ID. This requires the use of a demodulator, decoder, and oscillator. Amplitude-modulated signals are relatively simple to demodulate, requiring a single diode operating as an envelope detector. The decoder may be implemented using combinational digital logic and a serial-to-parallel converter consisting of a series of flip-flops. Lastly, the oscillator, which is required to supply a clock signal to the digital circuitry, may be implemented using any one of numerous designs. It is conservatively estimated that these sub-blocks will not consume more than 10 $\mu$W of power [48].

### Tag ID Storage

The ID value of the tag may be stored on-chip in a variety of ways. Only some techniques, however, are suitable for the dosimeter tag. For example, since the ID value must not change when the energy storage is depleted, volatile storage techniques such as static random-access memory (SRAM) and dynamic random-access memory (DRAM) cannot be used. Furthermore, the tag is implemented using IBM's standard 0.13 $\mu$m CMOS process. Hence, storage solutions such as flash memory, which use special CMOS processes and floating gate transistors, are not available in IBM's conventional 0.13 $\mu$m process.

Consequently, researchers challenged by these limitations have developed non-volatile memory (NVM) solutions aimed at low-power RFID tags fabricated using

conventional CMOS processes [70, 71]. However, flash-based technologies in conventional CMOS exhibit poor resilience to ionizing radiation; TID values as little as 500 Gy may cause memory errors [72]. During the irradiation process, the Raycell Mk2 produces a maximum 41 Gy of X-ray radiation in some blood bags [41]. Thus, the re-use of dosimeter tags would be limited to approximately one dozen irradiation procedures.

In view of these shortcomings, the dosimeter tag will instead employ an alternative storage technique. Using the electronic fuse or "eFuse" component available in the IBM 0.13 $\mu$m CMOS process, the tag ID may be permanently stored in each IC with negligible power dissipation. A separate programming device is needed to apply a 3.3 V electric field across a portion of an array of eFuses, where each fuse represents a single storage bit [73]. This allows for the hard-coding of the tag ID into each IC. However, the disadvantage of this approach lies in the lack of reprogrammability of the stored value.

### Signal Processing Electronics

The design of the signal processing electronics (SPE) represents the thesis objective of Master's student Mohammadjavad Sheikhzadeh Nadjar. Using a modified Schmitt trigger topology, the SPE circuitry interfaces the radiation and temperature sensors with the modulator. The voltage levels representing the sensed measurements are translated into a series of pulses, where the sensed values are encoded within the frequency of the pulses. These frequencies are on the order of hundreds of kilohertz. Next, the pulses are digitized and fed into the modulator. The SPE circuitry employs ultra low-power sub-threshold design techniques to achieve extremely low power requirements; power dissipation is estimated to be 100 nW.

### Modulator & Antenna

To transmit information back to the reader, the dosimeter tag employs PSK-based backscatter modulation using the RF CW tone broadcast by the reader. This is accomplished through the use of a simple transistor which serves as a RF switch. The switch is controlled by the pulse sequence generated by the SPE circuitry, and is used to vary the impedance as seen by the tag antenna between two reactances of different values. Compared to techniques which vary the resistance seen by the antenna, reactive-based modulation techniques allow for constant power to be delivered to the IC (for further discussion on backscattering techniques, refer to Appendix A).

Based on the lower performance of on-chip antennas obtained by previous members of the dosimeter project, an off-chip solution will be employed [24]. The current dosimeter tag design is based on a half-wavelength ($\lambda/2$) dipole antenna. Using a dipole antenna ensures a large effective area, differential operation (to satisfy the EH circuitry requirements), and a compact design. To operate at 2.45 GHz, the antenna size must be approximately six centimetres. The antenna will be manufactured on a compact flexible inlay, which also contains the IC. The inlay, comprising the entire dosimeter tag, will be attached to a blood bag using an adhesive material [48].

### Additional Tag Circuitry

Development of the X-ray dosimeter project remains active. Hence, design specifications are subject to change according to future results. Additional functionality of the dosimeter tag not shown in the system diagram concept may be implemented in a later revision.

For instance, the radiation sensor currently operates using a differential power supply of ± 0.9 V. The energy harvester, however, produces a positive DC voltage with respect to ground. Therefore, DC level-shifting circuitry is required to interface the energy harvester with the radiation sensor. Alternatively, a dual energy harvester design could be explored, where one rectifier is responsible for the +0.9 V power rail, and the second rectifier is responsible for the -0.9 V power rail. Similarly, DC-DC voltage converters may be required depending on the chosen energy storage device (many rechargeable batteries, for example, require a large DC charging voltage). In addition, to limit the maximum voltage applied to the tag's input and its sub-blocks, a voltage limiter circuit (for instance, series diodes) is required at both the RF and DC interfaces of the EH sub-block.

### 2.3.3 Dosimeter Reader Overview

Thus far, work on the dosimeter project has concentrated primarily on the tag and its radiation sensing capabilities. There remains much work to be done on the RFID-based reader. Currently, the reader is being envisaged as a portable hand-held device. Since the reader would be significantly larger than the dosimeter tags, a larger antenna and discrete battery may be employed. To ensure a maximum operating range of up to one metre, the reader should operate at the maximum 1 W of allowed transmit power. The increased production cost of the reader will be offset by the fact that, for a given number of tags, relatively few readers are required.

To maximize the operating range, the reader should employ full RF transmitter and receiver architectures. During transmission, the reader must first generate an ASK-modulated 2.45 GHz RF signal, followed by an RF CW tone at the same frequency to facilitate backscatter modulation. Similarly, during reception, the reader must

demodulate a PSK-modulated backscatter signal. This signal will be very weak when it arrives at the reader's antenna; therefore the receiver must have high sensitivity. This may be achieved through the use of a bistatic antenna configuration [48].

In addition, the integration of the reader with Best Theratronics' existing blood bag management system should also be explored. The Best Theratronics Irradiated Products Database Management software currently supports only barcode-based blood bag labels [41]. Therefore, an investigation would be required to assess the feasibility of expanding the software to support RFID-based tags as well.

## 2.4 The X-Ray Dosimeter Project: Power Considerations

This section examines several energy-related aspects of the X-ray dosimeter project. First, a survey of available energy sources is presented. Next, a set of power and link budgets for the dosimeter tag are formulated. Finally, this section concludes with a survey of potential energy storage devices.

### 2.4.1 Energy Harvesting Source Selection

#### Survey of Potential Energy Sources

After decades of research, the field of energy harvesting has grown to include countless devices and a vast breadth of energy sources. One of the most commonly harvested forms of energy originates from sources of kinetic or vibrational motion. Examples of kinetic energy sources include: a person walking, a rotating vehicle tire, and wind pressure. Devices which harvest this form of energy are classified according

to the mechanism that is used to generate electricity. Broadly speaking, these mechanisms involve a change in either a physical displacement or a material property, due to kinetic or vibrational motion [74].

Mechanisms which rely on a change in physical displacement include EM induction and electrostatics. For example, EM induction may involve moving a metallic coil through a magnetic field to generate an electric current [75]. Meanwhile, an electrostatic energy harvester may harness vibrational energy to modulate the separation distance between two capacitive plates, thereby inducing a change in capacitance between the plates [74].

Mechanisms which rely on a change in some material property include piezoelectricity, and, much less commonly, electrostriction and magnetostriction. In piezoelectric devices, when a mechanical stress is exerted on the device due to an applied force, a voltage difference across the piezoelectric material is created (the converse is also true) [74]. For example, the piezoelectric effect may be used to generate electricity from acoustic pressure waves (*i.e.* sound waves) [76]. Similarly, electrostriction and magnetostriction are phenomena involving the change in shape of some material when an electric or magnetic field is applied, respectively. Unlike the piezeoelectric effect, these mechanisms are not reversible, and result in much smaller mechanical strains. Only ferromagnetic materials exhibit magnetostriction [77].

Other popular sources of energy include solar energy and thermal gradients. Solar energy harvesters exploit the photovoltaic effect to generate electricity from light, or more specifically, photons. The light may originate from the sun, indoor lighting, or an intentional light source. In contrast to the sun, indoor lighting provides a limited

amount of energy. Thus, most photovoltaic EH devices rely on solar energy. Thermal energy harvesting, meanwhile, utilizes the Seebeck effect to generate electricity. When a temperature differential exists between two junctions connected by a pair of conductors of different materials, a voltage is produced. This configuration is referred to as a thermocouple, while a series of thermocouples is known as a thermopile. These structures are employed by thermal energy harvesters to generate electricity [78].

Electricity may also be generated from electromagnetic radiation. TV and cellular base stations emit large quantities of RF and microwave radiation. This energy may be collected by RF energy harvesters through the use of an antenna. However, RF/microwave radiation provides relatively small amounts of power compared to the other forms of energy previously mentioned. For example, researchers in [79] were only able to collect energy at a maximum power density of 4 nW/cm$^2$. In [80], researchers obtained a much higher power density over the same frequency band. These measurements were taken at street-level, outside of London Underground metro stations. The average power density of GSM-1800 radiation was measured to be 84 nW/cm$^2$, while peak power density reached 6.39 $\mu$W/cm$^2$. However, available RF energy varies widely based on several factors, including: the communications traffic load, the time of day, and the distance from the base station. This variance is illustrated by the fact that researchers were able to harvest an impressive 1.73 W of power using a directional antenna at a distance of 100 metres from the venerable Tokyo (communications) Tower, Japan's second tallest structure [16].

In summary, energy harvesters employ a variety of mechanisms to generate electricity from ambient or intentionally placed sources of energy. Each source and technique possesses its own advantages and limitations. Therefore, EH designers must wisely select an energy source and conversion mechanism suitable to their needs. Table 2.5

presents a summary of selected energy sources and the power obtained through EH.

**Table 2.5:** A summary of energy sources and the typical power densities which may be obtained through energy harvesting. Power densities are calculated by dividing the achievable harvested power of a typical device by the area of the sensing device. Energy sources which originate from an individual's body or movements are further classified as "human" sources. These power densities are estimates and should be used primarily for comparative purposes [78].

| Energy Source | Environment | Typical Harvested Power |
|---|---|---|
| Optical | Indoor (Lighting) | 10 $\mu$W/cm$^2$ |
| | Outdoor (Solar) | 10 mW/cm$^2$ |
| Kinetic/Vibrational | Human | 4 $\mu$W/cm$^2$ |
| | Industrial | 100 $\mu$W/cm$^2$ |
| Thermal | Human | 30 $\mu$W/cm$^2$ |
| | Industrial | 1–10 mW/cm$^2$ |
| RF | Outdoor | 0.1 $\mu$W/cm$^2$ |

### Selecting an Energy Source

Due to its unique operating environment, the X-ray dosimeter tag is unable to harvest energy from many of the aforementioned sources. The tags will be used throughout a variety of medical environments, including inside the Raycell Mk2 irradiation machine. While inside this machine, the tags are not directly visible. Therefore, optical and acoustic sources, whether ambient or intentional, are not useful approaches for generating electricity. Similarly, the tags are not subjected to significant kinetic or vibrational motion. Further still, temperature gradients across the tags and blood bags will also be negligible. Thus, RF energy harvesting would seem to be the most suitable way to collect energy. However, the Raycell Mk2 blood irradiation machine is presumably well-shielded, which implies that a relatively low amount of ambient RF radiation will be present.

Therefore, as noted in Section 2.3, an intentional RF source was ultimately chosen. This approach is ideal for RFID-based tags such as the X-ray dosimeter tag. The dosimeter reader, which serves as the RF source, is capable of transmitting a large amount of power (up to 1 W) to the tags [63]. The choice of a 2.45 GHz source was made for two primary reasons. First, this frequency lies in the centre of an ISM band, which does not require a license to use. Secondly, it enables the use of compact tag antennas which easily fit on to the blood bags. However, this relatively high frequency poses a unique challenge to the design of a high-efficiency voltage rectifier.

### 2.4.2 Power & Link Budget Assessment

Now that a suitable energy source has been selected, the next design aspects to consider include the power and link budgets of the dosimeter tag. Although certain portions of the tag remain under development, it is still possible to obtain an estimate of the tag's power requirements by making a series of reasonable design assumptions.

#### Tag IC Power Consumption

A summary of the power requirements of the dosimeter tag's various sub-blocks is presented in Table 2.6. This table is based on the values for power consumption given in Section 2.3, which describes the dosimeter tag in detail. Some of these numbers are based on experimental data, while others are estimates based on design assumptions and published research. Recall that the tag ID is implemented using IBM's eFuse device, and thus does not consume any power [73]. In addition, it is assumed that the modulator, which is comprised of an RF switch, consumes a negligible amount of power. However, modulation efficiency and EH conversion efficiency are taken into account during the assessment of the power and link budget.

**Table 2.6:** Power budget summary for the dosimeter tag IC.

| **Dosimeter Tag Sub-Block** | **Estimated Power Consumption ($\mu$W)** |
|---|---|
| Radiation Sensor | 243 |
| Temperature Sensor | 10 |
| Signal Processing Electronics (SPE) | 0.1 |
| Demodulator, Decoder, & Oscillator | 10 |
| Tag ID Storage (eFuses) | 0 |
| Modulator (RF Switch) | 0 |
| **Total** | **263.1** |

### Energy Harvesting Efficiency

The purpose of the energy harvesting sub-block is to convert a fluctuating RF signal into a stable DC voltage. This process is inherently inefficient. The most significant sources of inefficiency include the voltage rectifier and voltage regulator stages. A detailed discussion of these critical stages is presented in Chapter 3. For now, an assumption of power efficiency will be made. The rectifier is conservatively assumed to have an efficiency of 50%, which is somewhat less than the maximum achievable efficiency of the chosen topology [81]. Similarly, the voltage regulator is assumed to have an efficiency of 75%; this is a reasonable level of efficiency to expect from a low-dropout (LDO) linear voltage regulator when the (unregulated) input and (regulated) output voltages are close in value to one another [82]. Hence, the efficiency of the rectifier, $\eta_{Rect}$, and voltage regulator, $\eta_{Reg}$, are assumed to be 0.5 and 0.75, respectively. Therefore, the overall efficiency, $\eta_{EH}$, of the energy harvesting circuitry is:

$$\eta_{\mathrm{EH}} \;=\; \eta_{\mathrm{Rect}} \times \eta_{\mathrm{Reg}} \;\doteq\; 0.38 \tag{2.5}$$

**Minimum Required Tag Power**

To calculate the minimum power required by the tag's IC, $P_{IC}$, the results of Equation 2.5 and Table 2.6 are used. Note that $P_{PB}$ corresponds to the tag's power budget (*i.e.* 263.1 $\mu$W). Thus, the minimum required power is:

$$\mathrm{P_{IC}} \;=\; \frac{\mathrm{P_{PB}}}{\eta_{\mathrm{EH}}} \;\doteq\; 702\ \mu\mathrm{W} \tag{2.6}$$

**Antenna Modulation Efficiency**

The dosimeter tag utilizes backscatter modulation in lieu of a transmitter. Therefore, the power received by the tag's antenna, $P_{Rx}$, must be shared between the tag's IC and the backscatter signal. The allocation of the received power depends on which backscatter technique is employed. As explained earlier, the dosimeter tag will use PSK-based backscatter modulation. This provides constant power to the tag's IC. From Table 2.2, the received power is apportioned between the power allocated to the backscatter signal, $P_{BSC}$, and the tag's IC, $P_{IC}$, as follows [48]:

$$\mathrm{P_{BSC}} \;=\; 0.32 \times \mathrm{P_{Rx}} \tag{2.7}$$

$$\mathrm{P_{IC}} \;=\; 0.4 \times \mathrm{P_{Rx}} \tag{2.8}$$

Therefore, by rearranging Equation 2.8, the minimum required power to be received by the tag's antenna, $P_{Tag,\,Min}$ (*i.e.* $P_{Rx}$), may be determined:

$$\mathrm{P_{Tag,\,Min}} \;=\; \frac{\mathrm{P_{IC}}}{0.4} \doteq 1.75\ \mathrm{mW} \tag{2.9}$$

### Power Budget Summary

The preceding mathematical analysis of the dosimeter tag's power budget may be summarized visually, as shown in Figures 2.11 & 2.12. In Figure 2.11, the power efficiency of each module and the remaining available power after each module is presented. In Figure 2.12, the power consumption of each module is represented by its relative size.

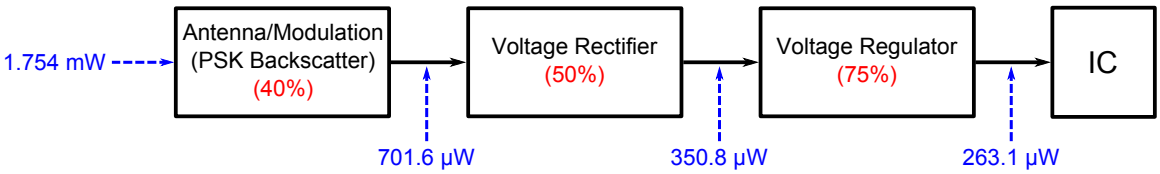


**Figure 2.11:** A summary of the power efficiency of each dosimeter tag module (shown in red) and the remaining power after each module (shown in blue).

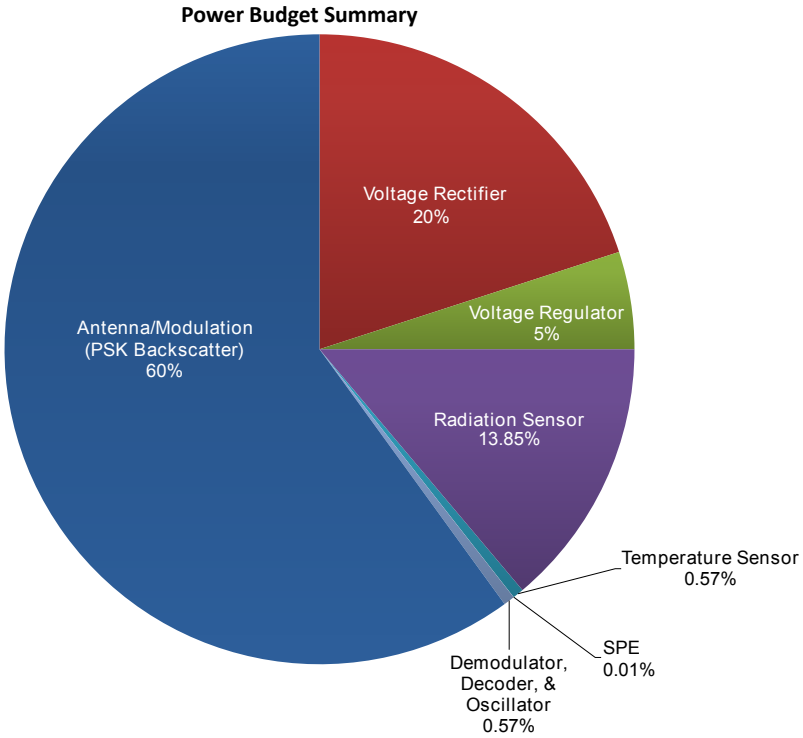


**Figure 2.12:** Graphical illustration of the dosimeter tag's power budget. Each module's power consumption is represented by its relative size in the chart.

**Reader & Tag Antenna Properties**

As explained in Section 2.3, the dosimeter tag employs a $\lambda/2$ dipole antenna. This type of antenna has a directivity, $D$, of approximately 1.6. It is assumed that antenna inefficiency is minimal, so that the directivity and power gain are roughly equal. Thus, the $\lambda/2$ dipole antenna has a gain of approximately 2.2 dBi. Also, note that at 2.45 GHz, the wavelength is approximately 12 centimetres. Therefore, the tag antenna's effective area (*i.e.* antenna aperture), $A_e$, may be calculated as follows [83]:

$$\mathrm{A_e} \;=\; \frac{\lambda^2}{4\pi}\,\mathrm{D} \;\doteq 19.6\ \ \mathrm{cm}^2 \tag{2.10}$$

For the dosimeter reader antenna, it is assumed that a microstrip rectangular patch design will be employed. Although the directivity of 'patch' antennas varies greatly according to implementation, it is possible to obtain high directivity. Therefore, it will be assumed that the power gain of the reader's patch antenna is 7 dBi (or approximately 5.0 on a linear scale) [83].

**Maximum Transmit Power**

As noted earlier, federal regulations limit the maximum transmitted EIRP to 4.0 W. Therefore, let $P_{EIRP}$ refer to the maximum allowed EIRP, and $G_{Reader}$ denote the reader antenna's gain. The maximum power which may be transmitted by the reader, $P_{Tx,\,Reader}$, is determined by rearranging Equation 2.11 as follows [84]:

$$\mathrm{P_{EIRP}} \;=\; \mathrm{G_{Reader}} \times \mathrm{P_{Tx,\,Reader}} \tag{2.11}$$

$$\rightarrow \mathrm{P_{Tx,\,Reader}} \;=\; \frac{\mathrm{P_{EIRP}}}{\mathrm{G_{Reader}}} \;\doteq\; 0.8\ \ \mathrm{W}$$

(Note: The maximum transmit power of the dosimeter tag need not be determined, as the tag's antenna gain and transmit power is much less than that of the reader.)

### Link Budget Assessment

The system link budgets between the reader and tag will now be derived. Two separate link budgets will be formulated: one for the downlink and one for the uplink communication channels.

### Link Budget: Downlink Channel

The link budget of the downlink channel may be estimated using the Friis transmission equation. This formula implicitly assumes that the transmitter and receiver are operating within the far-field region and an ideal environment, free of any physical objects. Consequently, non-ideal effects such as signal reflection and scattering, or antenna polarization mismatch, are not taken into account. However, in practice, the reader and tags operate in a non-ideal environment similar to Figure 2.8. Therefore, the following estimate for received power should be considered to be an optimistic, best-case scenario [48].

The Friis transmission formula is shown in Equation 2.12. $P_{Rx,\,Tag}$ represents the power received by the tag; $P_{Tx,\,Reader}$ corresponds to the maximum transmit power of the reader (0.8 W); $G_{Reader}$ and $G_{Tag}$ refers to the power gain of the reader and tag antennas, respectively (5.0 & 1.6); $\lambda$ corresponds to the wavelength of the transmitted signal (0.12 m); finally, $r$ denotes the distance between the reader and tag (1 m). The power received by the tag is [48]:

$$\mathrm{P_{Rx,\,Tag}} \;=\; \mathrm{P_{Tx,\,Reader}} \times \mathrm{G_{Reader}} \times \mathrm{G_{Tag}} \times \left(\frac{\lambda}{4\pi \mathrm{r}}\right)^{2} \;\doteq\; 0.6 \;\; \mathrm{mW} \tag{2.12}$$

However, from Equation 2.9, it was determined that the tag requires at least 1.75 mW of power to operate. Therefore, an energy storage device is required to supply additional power. The power which must be supplied by this device, $P_{Storage}$, may be determined as follows:

$$\mathrm{P_{Storage}} \;=\; \Delta\mathrm{P} \;=\; \mathrm{P_{Tag,\,Min}} - \mathrm{P_{Rx,\,Tag}} \;\doteq\; 1.1 \;\; \mathrm{mW} \tag{2.13}$$

**Link Budget: Uplink Channel**

During uplink communication, the dosimeter tag transmits a signal back to the reader using PSK-based backscatter modulation. Of the 0.6 mW of power received by the tag antenna ($P_{Rx,\,Tag}$), the amount which is allocated for the backscatter signal, $P_{Tx,\,Tag}$, may be determined by rearranging Equation 2.7 as follows [48]:

$$\mathrm{P_{Tx,\,Tag}} \;=\; 0.32 \times \mathrm{P_{Rx,\,Tag}} \;\doteq\; 0.2 \;\; \mathrm{mW} \tag{2.14}$$

Next, the Friis transmission equation may be employed once more to determine the power received by the reader antenna, $P_{Rx,\,Reader}$, in an ideal environment. Using Equations 2.12 and 2.14, the received reader power may be referred back to the original transmitted power, $P_{Tx,\,Reader}$, as follows [48]:

$$\mathrm{P_{Rx,\,Reader}} \;=\; \mathrm{P_{Tx,\,Tag}}\;\mathrm{G_{Reader}}\;\mathrm{G_{Tag}}\;\left(\frac{\lambda}{4\pi\mathrm{r}}\right)^{2} \tag{2.15}$$

$$\mathrm{P_{Rx,\,Reader}} \;=\; (0.32 \cdot \mathrm{P_{Rx,\,Tag}})\;\mathrm{G_{Reader}}\;\mathrm{G_{Tag}}\;\left(\frac{\lambda}{4\pi\mathrm{r}}\right)^{2} \tag{2.16}$$

$$\mathrm{P_{Rx,\,Reader}} \;=\; 0.32 \cdot \mathrm{P_{Tx,\,Reader}}\;{\mathrm{G_{Reader}}}^{2}\;{\mathrm{G_{Tag}}}^{2}\;\left(\frac{\lambda}{4\pi\mathrm{r}}\right)^{4} \tag{2.17}$$

The same values used previously in Equation 2.12 may be employed once again to determine the power received by the reader. At a distance of one metre, the received power is [48]:

$$P_{\text{Rx, Reader}} \doteq 0.2\ \mu\text{W} \equiv -37\ \text{dBm} \tag{2.18}$$

In contrast to typical RFID systems, the power received by the reader's antenna is relatively large. Therefore, achieving the necessary level of receiver sensitivity is possible without great difficulty [48].

### Link Budget Summary

A summary of the preceding link budget analysis is provided in Table 2.7. The link budget calculations are repeated for operating distances of 0.25 m, 0.5 m, and 0.75 m.

**Table 2.7:** Link budget summary for the dosimeter tag. The columns correspond to the: operating distance, received tag power ($P_{\text{Rx, Tag}}$, eq. 2.12), power which must be supplied by the energy storage device ($P_{\text{Storage}}$, eq. 2.13), tag transmit power ($P_{\text{Tx, Tag}}$, eq. 2.14), and received reader power ($P_{\text{Rx, Reader}}$, eq. 2.17). Note that for an operating distance of 0.6 m or less, no storage device is required.

| **Distance (m)** | $\mathbf{P_{Rx,\,Tag}}$ **(mW)** | $\mathbf{P_{Storage}}$ **(mW)** | $\mathbf{P_{Tx,\,Tag}}$ **(mW)** | $\mathbf{P_{Rx,\,Reader}}$ **($\mu$W)** |
|---|---|---|---|---|
| 0.25 | 10.0 | — | 3.2 | 40 |
| 0.5 | 2.5 | — | 0.8 | 2.5 |
| 0.75 | 1.1 | 0.6 | 0.4 | 0.5 |
| 1 | 0.6 | 1.1 | 0.2 | 0.2 |

The forward and reverse link budgets are also presented visually, in Figure 2.13. Each link budget is plotted as a function of the distance from the reader.

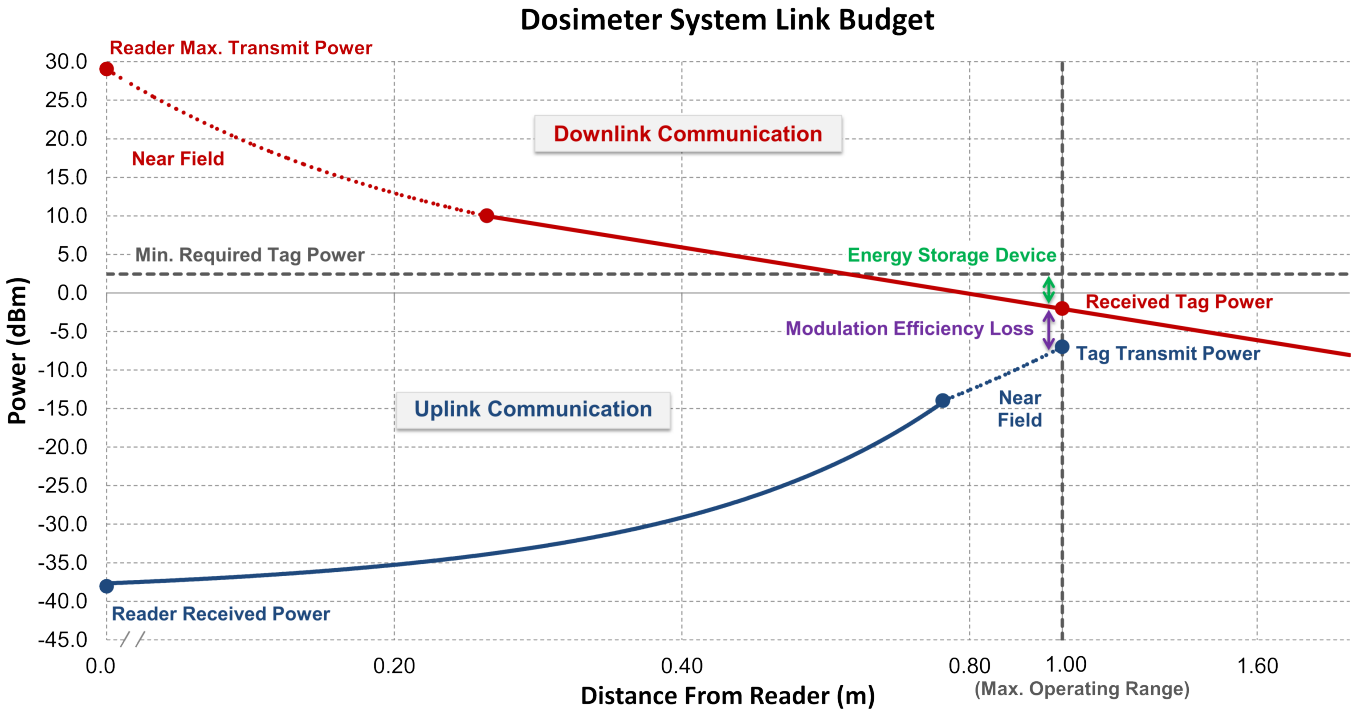


**Figure 2.13:** A summary of the dosimeter system link budgets. Downlink communication is shown in red, while uplink communication is shown in blue [48].

During downlink communication, the reader transmits a signal at a power level of 0.8 W (29 dBm). This signal's power subsequently decreases at a rate of 20 dB/decade as a function of distance (*i.e.* $1/r^2$). At an operating distance of one metre, the reader's signal is received by the tag at a power level of 0.6 mW (-2.2 dBm). Since the received power is considerably less than the power required by the tag (1.75 mW or 2.4 dBm), an energy storage device is required to supply an additional 1.1 mW of power. Using PSK backscatter modulation, the tag's modulation efficiency is 32%, or -4.9 dB. Thus, the tag transmits its information back to the reader with an initial power of 0.2 mW (-7.0 dBm). This signal's power subsequently decreases at a rate of 40 dB/decade as a function of distance (*i.e.* $1/r^4$). At last, the backscattered signal is received by the reader at a power level of 0.2 $\mu$W (-37 dBm) [48].

### 2.4.3 Energy Storage Requirements & Selection

Following a complete power and link budget analysis, the next and final energy-related design consideration to examine involves the selection of a suitable energy storage device. Before choosing a storage device, however, it is first necessary to determine the amount of energy storage which is required.

#### Energy Storage Requirements

The amount of energy which must be stored by the dosimeter tag ultimately depends on two factors: the amount of additional power which must be supplied by the energy storage device, and the tag's duty cycle. The first factor, $P_{Storage}$, was determined in the previous section to be 1.1 mW. For simplicity, it will be assumed that the tag's power consumption remains constant during operation. In practice, however, the tag's power consumption is a function of the number of sub-blocks which are simultaneously active at any given time. For example, during demodulation, the modulator and SPE sub-blocks should be disabled to conserve power. In addition, the quantity of RF power harvested by the tag is also assumed to be constant (again, this is not necessarily the case in reality: RF power may fluctuate over time).

The second factor, the tag's duty cycle, will now be examined. The duty cycle is defined as the portion of time that the tag spends in an active mode of operation, as opposed to a low-energy 'sleep' mode [48]. The dosimeter tag is therefore considered to be in an active mode during downlink and uplink communication. It will be assumed that downlink and uplink communication occurs consecutively, and that no time elapses between intervals. Thus, the time that the tag spends in active mode, $t_{ON}$, may be expressed mathematically as the sum of the time spent on downlink communication, $t_{Downlink}$, and the time spent on uplink communication, $t_{Uplink}$, as

follows:

$$\mathrm{t_{ON}} \;=\; \mathrm{t_{Downlink}} + \mathrm{t_{Uplink}} \tag{2.19}$$

The time spent transmitting data in either direction is governed by the bit rate (or data rate). During uplink communication, the tag's SPE circuitry modulates the carrier signal at a frequency, $F_{Mod}$, of approximately 100 kHz. Therefore, the time required to transmit a single bit, $T_b$, is given by:

$$\mathrm{T_b} \;=\; \frac{1}{\mathrm{F_{Mod}}} \;=\; 10 \;\; \mu\mathrm{s} \tag{2.20}$$

If a single bit is transmitted during each modulation period, then the bit rate is equal to the modulation frequency. For simplicity, it will be assumed that the bit rate of the downlink and uplink channels are equal. Therefore, the bit rate, $R_b$, of both channels is:

$$\mathrm{R_b} \;=\; \frac{1}{\mathrm{T_b}} \;=\; 100 \;\; \mathrm{kbps} \tag{2.21}$$

Hence, the bit rate is 100 kilobits-per-second (kbps). During downlink communication, the reader transmits the ID of a tag it wishes to interrogate. The ID is assumed to be represented by a 16-bit value, which allows for up to 65,536 unique IDs. The time required by the tag to demodulate, decode, and compare the received ID to its own ID value is defined as $t_{Downlink}$. The time required for downlink communication is a function of the bit rate, $R_b$, and the number of bits to be transmitted, $N_{b,\,Downlink}$ (*i.e.* 16 bits), and may be determined as follows:

$$\mathrm{t_{Downlink}} \;=\; \frac{\mathrm{N_{b,\,Downlink}}}{\mathrm{R_b}} \;=\; 160 \;\; \mu\mathrm{s} \tag{2.22}$$

The time required for uplink communication, $t_{Uplink}$, may be analyzed in a similar manner. During uplink communication, the tag transmits its ID, sensed radiation dose, and measured temperature back to the reader. It will be assumed that the radiation and temperature values are also represented by 16-bit values. Therefore, the tag must transmit a total of 48 bits. Note that, in practice, additional parity or error correction bits are also required (this is referred to as channel coding). However, this consideration will be omitted for the purposes of estimating the required energy to be stored. Hence, $t_{Uplink}$ may be calculated as follows:

$$\mathrm{t_{Uplink}} = \frac{\mathrm{N_{b,\,Uplink}}}{\mathrm{R_b}} = 480 \ \mu\mathrm{s} \tag{2.23}$$

Therefore the total time in which the tag is powered on, $t_{ON}$, may be determined:

$$\mathrm{t_{ON}} = \mathrm{t_{Downlink}} + \mathrm{t_{Uplink}} = 640 \ \mu\mathrm{s} \tag{2.24}$$

A summary of the preceding analysis is presented in Figure 2.14, which illustrates one complete cycle of operation of the dosimeter tag. By contrast, the Raycell Mk2 requires 2.8–4.9 minutes to perform a single cycle of blood irradiation (depending on the number of blood bags and canister selected) [41]. If it is assumed that an operator wishes to assess each tag every 20 seconds, then the dosimeter tag's duty cycle will be very low.

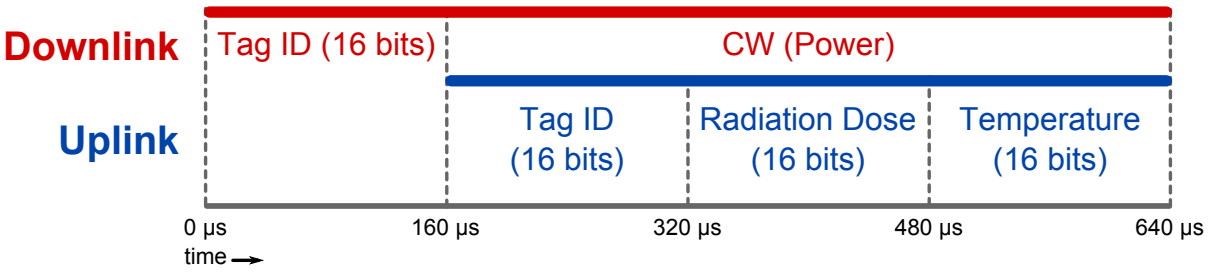


**Figure 2.14:** One cycle of active operation of the dosimeter tag.

However, depending on which energy storage device is employed, the communication cycle depicted in Figure 2.14 may require modification. If the chosen storage device requires charging prior to tag operation, then the downlink communication sequence must be prefixed with an additional interval. This interval would involve charging the tag's storage device via a CW carrier tone, similar to what is used during backscatter modulation. The duration of this charging interval depends on the choice of energy storage element.

Next, assuming constant power consumption during operation, the total energy required by the tag for one complete communication cycle, $E_{Storage}$, may be determined as follows [85]:

$$\mathrm{E_{Storage}} = \int_{\mathrm{t_1}}^{\mathrm{t_2}} \mathrm{P_{Storage}}\,\mathrm{d}t = (1.1\ \mathrm{mW}) \cdot t \Big|_{0\,\mathrm{s}}^{640\,\mu\mathrm{s}} \doteq 0.72\ \ \mu\mathrm{J} \tag{2.25}$$

If a capacitor-based energy storage device is employed, then the required capacitance, $C_{Storage}$, may be determined by rearranging Equation 2.26. The voltage applied across the capacitor will be taken to be the nominal operating voltage of the IBM 0.13 $\mu$m CMOS process (*i.e.* $V_{DD} = 1.2$ V) [73].

$$\mathrm{E} = \frac{1}{2}\,\mathrm{C}\,\mathrm{V}^2 \rightarrow \mathrm{C_{Storage}} = \frac{2\,\mathrm{E_{Storage}}}{\mathrm{V_{DD}}^2} \doteq 1.0\ \ \mu\mathrm{F} \tag{2.26}$$

**Survey of Potential Energy Storage Devices**

Having analyzed the tag's energy storage requirements, it is now possible to conduct a survey of potential energy storage solutions. Four solutions will be examined:

1. On-chip capacitor.

2. Off-chip conventional capacitor.

3. Off-chip supercapacitor.

4. Thin film rechargeable battery.

**1. On-Chip Capacitor:** The IBM 0.13 $\mu$m CMOS design kit includes an assortment of capacitors, including: MOS, single- and dual-layer metal-insulator-metal (MIM), and vertical natural capacitors (VNCAPs). Of these, the MOS capacitor offers the highest per unit area capacitance. However, due to their characteristically high temperature coefficients, MOS capacitors are also highly sensitive to variations in temperature. This is of special concern to the X-ray dosimeter tag, which must operate over a wide temperature range. Consequently, a dual-layer MIM capacitor should be used instead, on account of its smaller temperature coefficient. Although details of IBM's design kit are protected by a non-disclosure agreement, it is widely known that typical on-chip per unit area capacitances are on the order of 1–10 fF/$\mu$m$^2$ [86]. If the per unit area capacitance is taken to be 10 fF/$\mu$m$^2$, then a capacitance of 1.0 $\mu$F would require a chip area of approximately 100 mm$^2$. Clearly then, an on-chip energy storage device is not a feasible solution.

**2. Off-Chip Conventional Capacitor:** Compared to on-chip capacitors, discrete capacitors offer much larger capacitance, and hence, energy storage. Conventional capacitors are typically classified by their dielectric material. Broadly speaking, capacitors may be classified as either electrostatic (*e.g.* ceramic, paper, polymer, film) or electrolytic (*e.g.* aluminum, tantalum) [87]. Each type of capacitor offers a unique set of advantages and disadvantages. When selecting a capacitor, many attributes must be considered, including, but not limited to: capacitance, component cost, physical size, leakage current, and equivalent series resistance (ESR). A summary of discrete capacitors and their typical capacitance ranges is presented in Table 2.8 [88], while a

detailed comparison of conventional capacitors is provided in [89].

**Table 2.8:** Capacitance ranges for several classes of discrete capacitor [88].

| Capacitor Type | Typical Capacitance Range |
|---|---|
| Electrostatic | 50 fF – 3 mF |
| Electrolytic | 22 nF – 2.2 F |
| Supercapacitor | 6.8 mF – 5,000 F |

**3. Off-Chip Supercapacitor:** Supercapacitors, also known as ultracapacitors, are a special class of capacitor featuring extremely large capacitance. This remarkable level of capacitance is obtained through one of two special manufacturing techniques (or, in some cases, a hybrid of the two). The majority of supercapacitors are classified as electrochemical double layer capacitors (EDLCs). EDLCs are composed of an electrolyte and several carbon-based electrodes. Charge separation occurs between the electrode and electrolyte at a distance of less than one nanometre, resulting in tremendous capacitance. Alternatively, supercapacitors may also exploit the principle of pseudocapacitance. These so-called pseudocapacitors store electric charge using reversible redox reactions occurring at or near the surface of suitable electrodes [90]. However, in respect to the X-ray dosimeter tag's requirements, supercapacitors provide an excessive amount of energy storage. As illustrated in Table 2.8, even the smallest supercapacitors provide thousands of times more energy storage than is required by the tag. Furthermore, in contrast to conventional capacitors, supercapacitors are typically expensive and bulky. Therefore, in the case of the dosimeter tag, a discrete supercapacitor is not an ideal choice of energy storage.

**4. Thin Film Rechargeable Battery:** There is a great demand among active and semi-active RFID tags for an inexpensive rechargeable battery. Rechargeable (or

secondary) batteries possess very high energy densities that surpass even supercapacitors. The recent development of solid-state thin film batteries has proven very useful for battery-assisted EH devices [91]. For example, consider Cymbet Corporation's EnerChip CBC012, shown in Figure 2.15. The CBC012 is a highly compact thin film battery featuring a capacity of 12 $\mu$Ah [92].

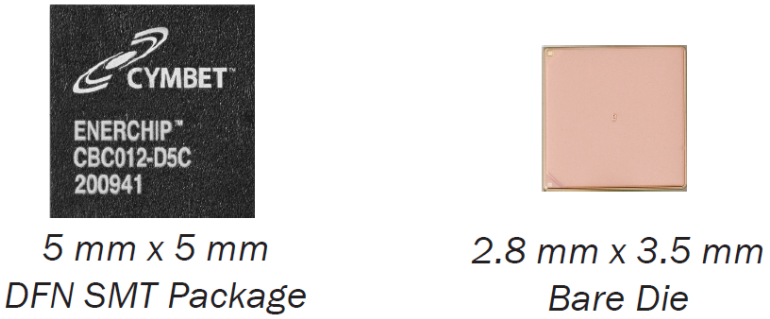


**Figure 2.15:** The Cymbet EnerChip CBC012 solid-state thin film battery. On the left, the CBC012 is shown in a surface mount technology (SMT) dual-flat no-leads (DFN) package. At right, the CBC012 is shown as a bare die [92].

The nominal open-circuit voltage of this battery, $V_{Batt,\,nom}$, is 3.8 V. However, due to the battery's internal cell resistance, $R_{Cell}$, the voltage which is delivered to the load (*i.e.* the IC), $V_{Load}$, will be less than $V_{Batt,\,nom}$. The load voltage depends on the DC current, $I_{DC}$, and cell resistance of the battery, and is expressed mathematically as follows:

$$\mathrm{V_{Batt,\,nom}} \;=\; \mathrm{V_{Cell}} + \mathrm{V_{Load}} \;=\; \mathrm{I_{DC}} \cdot \mathrm{R_{Cell}} \;+\; \mathrm{V_{Load}} \tag{2.27}$$

To determine how much current the CBC012 is capable of delivering, Equation 2.27 may be rearranged as shown below. $V_{Load}$ will be taken to be 1.2 V, the nominal operating voltage of the 0.13 $\mu$m IBM CMOS process. According to the datasheet, the typical cell resistance of a new CBC012 battery is 2.8 k$\Omega$ [92]. Therefore, the

current which may be obtained from the battery is:

$$\mathrm{I_{DC}} \;=\; \frac{\mathrm{V_{Batt,\,nom}} - \mathrm{V_{Load}}}{\mathrm{R_{Cell}}} \;\doteq\; 0.9 \;\; \mathrm{mA} \tag{2.28}$$

Thus, at an output voltage of 1.2 V and a current of 0.9 mA, the power delivered by the battery is approximately 1.1 mW. Conveniently, this happens to be the additional power required by the dosimeter tag from an energy storage device during operation. The total discharge time of the battery may be calculated from the battery's stored electrical charge (*i.e.* its capacity), $Q$, as follows:

$$\mathrm{I_{DC}} \;=\; \frac{\Delta \mathrm{Q}}{\Delta \mathrm{t}} \;\rightarrow\; \Delta \mathrm{t} \;=\; \frac{\Delta \mathrm{Q}}{\mathrm{I_{DC}}} \;=\frac{12\,\mu\mathrm{Ah} \times 3600\,\mathrm{sec/h}}{0.9\,\mathrm{mA}} \;\doteq\; 47 \;\; \mathrm{sec} \tag{2.29}$$

Therefore, if a Cymbet CBC012 battery is employed, the X-ray dosimeter tag would be capable of several dozen communication cycles from a single charge. In addition, Cymbet's EnerChip batteries were found to be tolerant to irradiation: samples placed inside an irradiation chamber did not exhibit any apparent degradation in performance. Furthermore, these batteries are priced competitively to supercapacitors. However, if the CBC012 is employed, then additional tag circuitry is required to: (A) recharge the battery at 4.1 V, and (B) disconnect the battery when the open-circuit voltage falls below 3.0 V [92]. This would consequently result in increased power dissipation.

**Selecting an Energy Storage Device**

In view of the preceding investigation, it is evident that a conventional off-chip capacitor would be the ideal energy storage device for the X-ray dosimeter tag. Following an exhaustive review of commercial capacitors, it was determined that a ceramic

capacitor would best serve the unique requirements of the tag. Ceramic capacitors are inexpensive, highly miniature, exhibit minimal DC leakage (due to low ESR), and are exceptionally robust to over-voltage conditions [89]. A capacitor such as the Kemet ceramic capacitor shown in Figure 2.16 provides a sufficient amount of capacitance (2.2 $\mu$F) and satisfies all other requirements [93].

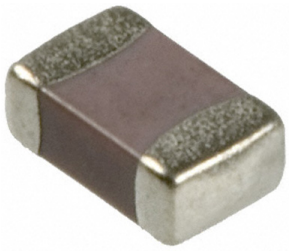

**Figure 2.16:** The Kemet C0805C225K8RACTU ceramic capacitor represents the ideal energy storage device for the X-ray dosimeter tag. This capacitor employs a standard-size 0805 SMT package [93].

At an operating voltage of 1.2 V, the energy which may be stored by this capacitor, $E_{Storage}$, is found from Equation 2.26 to be 1.6 $\mu$J. As established earlier, at a distance of one metre from the reader, the dosimeter tag is capable of harvesting 0.6 mW of power ($P_{Rx,Tag}$). Hence, the approximate time required to charge the capacitor, $t_{Req}$, may be calculated as follows [85]:

$$\mathrm{t_{Req}} = \frac{\mathrm{E_{Storage}}}{\mathrm{P_{Rx,\,Tag}}} \doteq 2.5 \ \mathrm{ms} \tag{2.30}$$

Therefore the dosimeter tag must remain in its energy harvesting mode for approximately 2.5 ms. During this time, the reader must transmit an RF CW tone. Once fully charged, the capacitor is capable of providing enough energy for two complete downlink/uplink communication cycles. It should also be noted that, for Equation 2.30 to be accurate, the time constant of the capacitor and EH circuitry must be sufficiently small. In addition, depending on the voltage regulator topology that is

chosen, the applied voltage across the capacitor may be different than 1.2 V. However, for the purpose of system development, Equation 2.30 provides a reasonable estimate.

## 2.5 Summary

In this chapter, a comprehensive overview of system considerations pertaining to wireless dosimetry was presented. First, an introduction to relevant medical concepts, including blood storage and sterilization procedures, was provided. It was noted that X-ray irradiation is a common method of sterilization, despite its inherent weaknesses, such as dose uniformity, which the X-ray dosimeter tag intends to eliminate. Second, an outline of RFID principles, including backscatter modulation, was given. After reviewing several popular backscattering techniques, it was determined that PSK-based modulation provides the best combination of backscatter and IC power. Third, the development of the X-ray dosimeter system was presented in detail. As explained earlier, this project is an RFID-based system used to monitor ionizing radiation levels in blood bags during (and after) medical blood irradiation procedures. Semi-active RFID tags placed on blood bags are used to wirelessly transmit data back to a hand-held reader when interrogated. Lastly, power considerations relating to the X-ray dosimeter system were examined. This included a power and link budget analysis, as well as energy harvesting source and storage selection. It was concluded that the X-ray dosimeter system should employ an intentional RF source and off-chip ceramic capacitor.

# Chapter 3

# Energy Harvesting Techniques

The main objective of this chapter is to provide a thorough examination of energy harvesting (EH) systems. Whereas Chapter 2 included a discussion of energy harvesting considerations as they pertained to the X-ray dosimeter project, this chapter focuses exclusively on energy harvesting systems. First, a high-level overview of RF EH systems is provided, including a discussion of each sub-block. Next, a literature review of voltage rectifiers is presented; both conventional rectifier topologies and techniques for high efficiency rectification are explored. Lastly, a preliminary investigation of voltage regulators is presented.

## 3.1 RF Energy Harvesting Systems

### 3.1.1 System Overview

A typical RF energy harvesting system is shown in Figure 3.1. RF energy harvesters are commonly implemented as RF front-end interfaces in passive and semi-passive RFID tags, which require an external energy source for operation. In this application, the energy harvester's basic role is to provide electrical power to the RFID tag's electronics. This is accomplished through the conversion of RF electromagnetic

energy into an electric current.

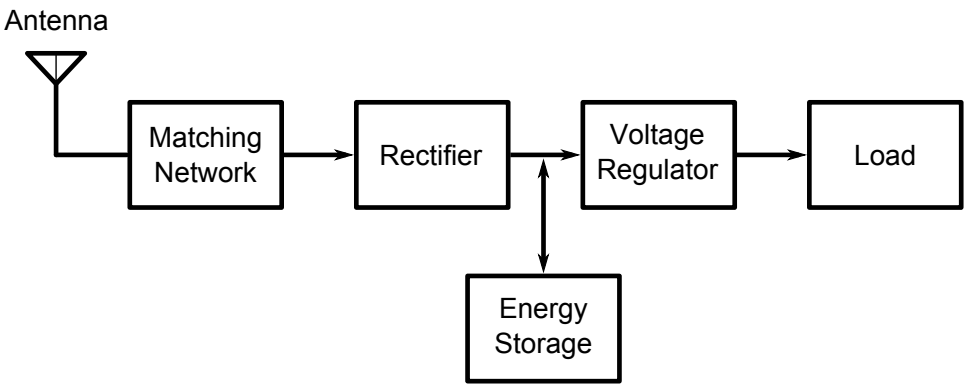


**Figure 3.1:** System-level overview of a typical RF energy harvesting system.

### 3.1.2 Subsystem Overview

Next, the various sub-blocks of RF energy harvesting systems will be examined.

#### Antenna

Antennas are passive structures which convert electromagnetic energy to electrical energy and *vice versa* [48]. The study of antennas is immense, and comprises an entire research area on its own. Consequently, myriad types of antennas exist, consisting of various shapes and physical properties. As noted in Chapter 2, RFID tags employ a variety of different antennas; common configurations include: loop, dipole, and patch. However, complex antenna configurations are also employed. For instance, polarization-independent antennas are highly beneficial to ensuring that the tag antenna is able to operate efficiently regardless of its physical orientation [94, 95].

Some energy harvesters employ a special antenna known as a "rectenna," or rectifying antenna. From a cursory glance, the distinction between rectennas and RF energy harvesters may appear blurred. However, the term "rectenna" generally applies to

systems which feature an antenna and transmission line-based matching network fabricated on a printed circuit board (PCB), in addition to the use of discrete diodes (typically Schottky type). Numerous examples of rectenna-based EH systems are found in literature [94–96]. These systems are capable of achieving high power conversion efficiency (PCE). However, the need for discrete electronic components results in a higher per-unit cost.

Ultimately, the choice of antenna configuration depends on the specific needs of the RFID tag under design. As noted in Section 2.3.2, an off-chip half-wavelength dipole antenna was chosen for the wireless X-ray dosimeter, due to its ability to provide a differential voltage to the rectifier.

### Matching Network

A matching network is placed between the antenna and voltage rectifier sub-blocks to ensure maximum power transfer, and hence, maximum PCE. Although numerous matching techniques exist, conjugate matching is used pervasively among RFID systems. This technique involves the use of 'L-sections,' consisting of carefully sized capacitors and inductors, to conjugately match the impedance of the antenna to that of the rectifier. Since rectifiers are typically capacitive, inductors are employed to perform the necessary impedance conversion. Using conjugate matching, it is also possible to boost the voltage amplitude of the input waveform received from the antenna. This is especially important in EH systems, where the received waveform's amplitude may be insufficient to overcome the turn-on voltage of the rectifier's diodes or transistors without voltage boosting [48].

Despite these advantages, conjugate matching also involves several limitations. For instance, conjugate matching is only capable of providing an optimal match over a narrow frequency band [48]. (Note: Multi-stage matching networks offer improved bandwidth; however, this comes at the expense of additional resistive loss from non-ideal components [97]). Impedance matching in energy harvesters is further complicated due to the inherent non-linear nature of rectifiers, which are typically constructed using diodes or diode-connected transistors. As a result, the condition for maximum power transfer also exhibits a dependence on the output load impedance and received input power of the energy harvester. Despite this caveat, many designers still rely on conjugate matching techniques. A small contingent of researchers, however, have elected to use the more precise source-pull technique for optimum impedance matching [98].

**Rectifier**

Voltage rectifiers perform the necessary RF-to-DC electrical conversion between the antenna's AC input waveform and the regulator's DC input voltage. A rectifier's output voltage is comprised of two components: the desired DC voltage, and a smaller AC ripple voltage superimposed on to the DC component. Rectifiers are characterized by several performance metrics, including: operating frequency, output loading, output voltage, PCE, voltage conversion ratio (VCR), and sensitivity. In RF EH systems, however, PCE is typically the most important parameter to maximize, as this results in the lowest required power consumption. The PCE of a rectifier is defined by Equation 3.1 [81]. A complete study of rectifiers is presented in Section 3.2.

$$\text{PCE} = \frac{\text{P}_{\text{out}}}{\text{P}_{\text{in}}} \tag{3.1}$$

**Energy Storage**

Energy storage devices were examined in detail in Section 2.4.3, where it was determined that the ideal storage solution for the wireless X-ray dosimeter tag is an off-chip ceramic capacitor.

**Voltage Regulation**

Due to ripple in the output voltage of the rectifier, a voltage regulator is required to provide a stable DC voltage supply to the EH system's circuitry. It is also used to regulate the voltage delivered by the energy storage device. In the case of capacitor-based storage, a regulator may be used to provide a stable voltage in spite of the capacitor's exponential discharge characteristic. Regulators are described by several performance metrics, including: drop-out voltage, power and voltage efficiency, power supply rejection ratio (PSRR), and line regulation. An overview of voltage regulators is presented in Section 3.3.

## 3.2 Rectifier Topologies

This section presents an overview of voltage rectifiers for energy harvesting applications, with specific emphasis given to RF EH systems (*i.e.* passive and semi-passive RFID tags, such as the wireless X-ray dosimeter project). Beginning with well-known rectifier topologies, this section examines the notable improvements made to rectifiers over time which are cited in literature.

### 3.2.1 Elemental Rectifier Topologies

Before examining contemporary rectifier architectures, it is highly instructive to first review what may be considered the two foremost elemental rectifier topologies,

since most modern designs operate in a similar manner. The full-wave bridge rectifier (FWBR), depicted in Figure 3.2(a), accepts a differential-ended AC input signal and produces a DC output voltage. The term "full-wave" refers to the fact that negative half-cycles of the FWBR's input are rectified to positive crests. For intuitive analysis, ideal diodes, which are modeled only by a forward voltage drop, may be assumed [99].

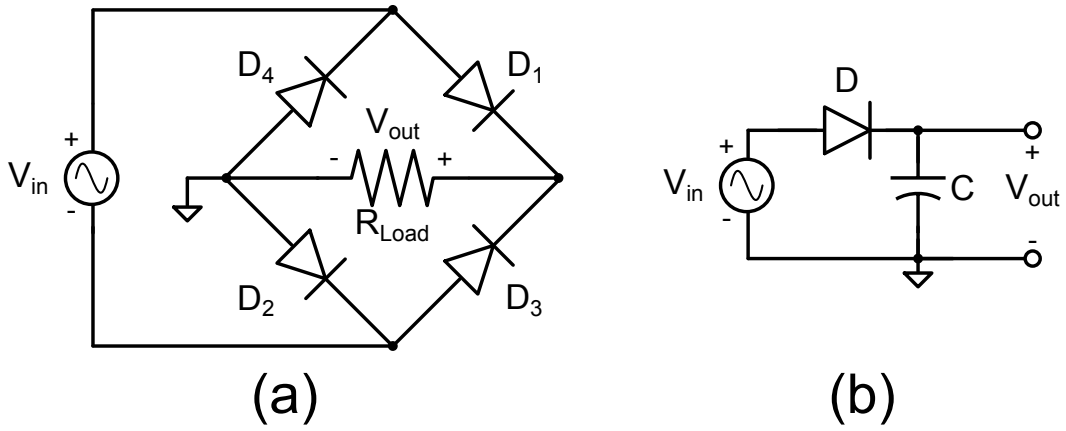


**Figure 3.2:** Elemental rectifier topologies. (a) The full-wave bridge rectifier (FWBR) topology. (b) The half-wave rectifier (HWR) topology [99].

During positive half-cycles of the input signal, diodes $D_1$ and $D_2$ are forward-biased (*i.e.* on), while $D_3$ and $D_4$ are reverse-biased (*i.e.* off) (it is assumed that the input amplitude is sufficiently large to overcome the forward voltage drops of the diodes). During negative half-cycles of the input signal, the operation of the diodes is reversed. Therefore, the output voltage, $V_{out}$, may be expressed in terms of the input voltage, $V_{in}$, and the forward voltage drop of the diodes, $V_D$, as [99]:

$$\mathrm{V_{out}} \;=\; \mathrm{V_{in}} \;-\; 2 \cdot \mathrm{V_D} \tag{3.2}$$

From Equation 3.2, it is evident that the primary disadvantage of FWBRs involves the significant voltage drop incurred from the two forward-bias diodes in the current path. This behaviour does not pose a problem for high-power rectifier designs.

However, in IC designs, where power supplies are relatively small (and continually shrinking), this voltage drop may prove prohibitively large. IC FWBRs are discussed in further detail later in this section [99].

The second elemental topology, the half-wave rectifier (HWR), is shown in Figure 3.2(b). The HWR is sometimes referred to as a "peak rectifier" or "peak detector." As its name suggests, the HWR is capable of rectifying only one-half of the AC input cycle. Hence, in the case of Figure 3.2(b), only the positive half-cycle of the input is rectified. A capacitor, $C$, must be placed at the output terminal and be sufficiently large in order to provide the necessary energy to the output load during the input half-cycles which are not rectified. Although omitted for clarity, the FWBR depicted in Figure 3.2(a) requires a similar capacitor at its output terminal [99].

### 3.2.2 Diode Implementations

The majority of rectifier designs consist of some combination of capacitors and diodes. Diodes are non-linear electronic devices which are used by rectifiers to direct current in only one direction. At a basic modeling level, diodes are characterized by an on-resistance during forward-bias operation, and a reverse leakage current during reverse-bias operation. There are numerous distinct implementations of diodes. In this section, implementations that are applicable to microelectronics are examined.

**PN Diodes:** Conventional PN diodes are formed by abutting two heavily and oppositely doped regions (p+ and n+) together within a monolithic piece of crystalline silicon. The formation of a PN junction results in a "built-in potential," $\phi_o$, which is modeled by a voltage drop during forward-bias operation. For silicon PN diodes, $\phi_o$ is typically taken to be 0.7 V, though in reality this parameter depends on the

dopant concentrations and the thermal voltage, $V_T$ [99]. PN diodes implemented in silicon-based IC processes suffer from comparably large forward voltage drops and depletion capacitance; these diodes are also generally not designed for forward-bias operation [100]. As a result, PN diodes are primarily employed as discrete components in low-cost, PCB-based rectifiers.

**Schottky Diodes:** When metal (such as an aluminum IC interconnect) directly contacts a lightly doped region of silicon, the large work-function difference between the materials creates a depletion region, and hence, a Schottky diode. The Schottky diode's unique construction results in many advantages over conventional PN junctions [101]. Most importantly, the effective voltage drop across the diode is much smaller: on the order of 200–300 mV. However, semiconductor foundries that offer Schottky diodes require additional mask layers and processing steps, consequently resulting in increased fabrication costs [81]. Therefore, like PN diodes, Schottky diodes are typically relegated to PCB-based rectifiers, such as [102].

**Diode-Connected Transistors:** Due to the aforementioned design limitations of PN and Schottky diodes, the majority of IC rectifiers cited in literature utilize diode-connected transistors (DCTs), which are shown in Figure 3.3. Diode-like behaviour is achieved by connecting the gate and drain terminals of an NMOS or PMOS transistor together [103].

Consider the NMOS DCT depicted in Figure 3.3(a). When $V_{GS}$ (which is equal to $V_{DS}$) is less than the transistor's effective turn-on or threshold voltage, $V_{th}$, the transistor will operate in the subthreshold region and very little current will flow through the device. When $V_{GS} \geq V_{th}$, a channel is formed and current flows from the

drain to source terminal. During this condition, the transistor operates in the saturation region, never entering the triode region [103]. During forward-bias operation, the DCT's energy loss is characterized by its on-resistance, while during reverse-bias operation, loss is primarily due to reverse leakage current. Designers typically adjust the size of the DCT (*i.e.* the width-to-length ratio, W/L) to provide an appropriate trade-off between low on-resistance (large W/L) and minimal reverse leakage current (small W/L) [81].

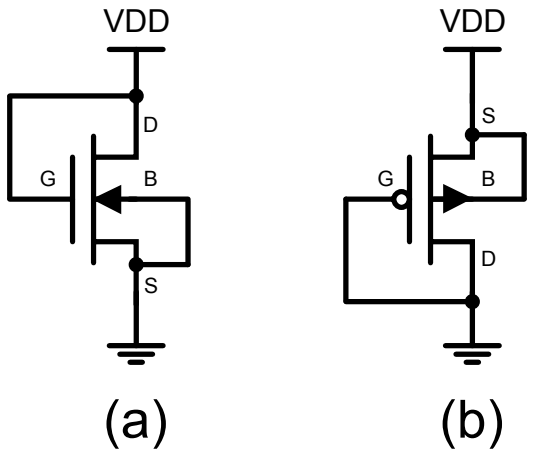


**Figure 3.3:** Diode-connected transistor (DCT) variants. (a) Diode-connected NMOS transistor. (b) Diode-connected PMOS transistor [103].

MOSFET-based DCTs are well-suited for use in IC rectifiers for several reasons. First, their characteristics are highly adjustable through W/L sizing, affording designers the necessary tuning ability to obtain maximum PCE from their designs. Second, the DCT's effective turn-on voltage is less than that of a PN diode (although typically larger than a Schottky diode). Finally, MOSFETs are ubiquitous among IC foundries, easy to manufacture, and well-characterized [81].

Some IC technologies such as IBM's 0.13 $\mu$m CMOS process offer a variety of different MOSFETs featuring a range of threshold voltages. Low-$V_t$ devices, for instance,

use thinner gate oxide thicknesses to achieve lower threshold voltages compared to standard MOSFETs [73]. However, low-$V_t$ devices also exhibit significantly larger reverse leakage currents, which effectively counteracts any advantage gained from a lower $V_{th}$ value. Consequently, this increased leakage current results in reliability issues and increased power consumption. Designers therefore typically employ standard MOSFETs when designing rectifiers [104].

### 3.2.3 Common IC Rectifier Topologies

This section describes the rectifier topologies most commonly employed in IC energy harvesting systems. Since many contemporary rectifiers are considered to be derivatives of these topologies, it is first necessary to examine their operation and understand their respective strengths and limitations before proceeding.

#### CMOS FWBR

The diode-based FWBR presented in Figure 3.2(a) may be modified for use in IC designs as shown in Figure 3.4(a). This variation, first introduced in [105], employs diode-connected PMOS transistors for improved PCE. Transistors MP2 and MP4 are diode-connected, while MP1 and MP3 are cross-connected to the opposite terminal of the input source [105]. The voltage, $V_{in}$, represents the input voltage from a transducer, such as an antenna (*e.g.* RF harvesting) or electrostatic capacitor (*e.g.* piezoelectric harvesting).

During positive half-cycles of the input voltage, current flows through MP1, MP4, and the output load (not shown), while transistors MP2 and MP3 are in cutoff mode. The situation is reversed for negative half-cycles of the input voltage. In either case, the cross-coupled PMOS transistor (*i.e.* MP1 or MP3) behaves as a MOS switch,

exhibiting only a minimal voltage drop due to its on-resistance. As a result, there exists only one diode voltage drop in the conduction path (due to MP2 or MP4), since the second voltage drop is replaced by the on-resistance of a MOS switch. Therefore, the PMOS FWBR offers superior PCE compared to the diode-based FWBR, which exhibits two forward voltage drops [104].

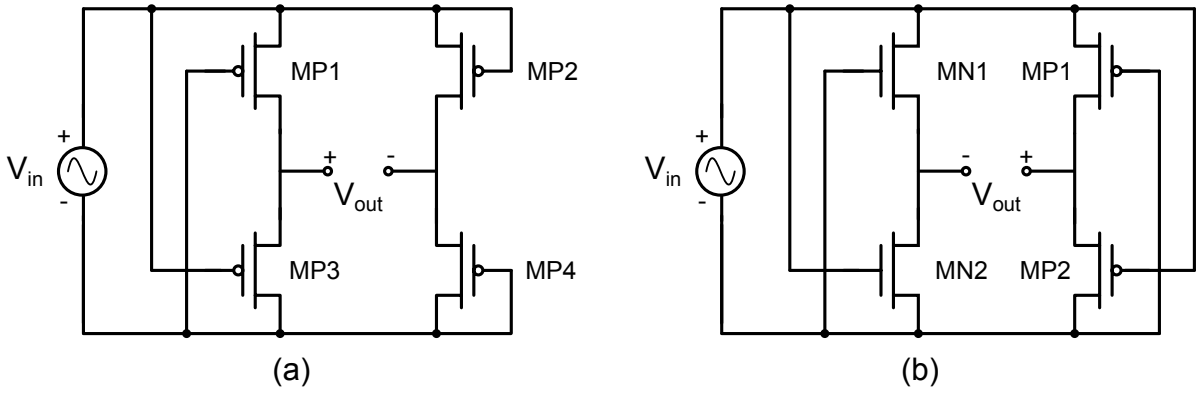


**Figure 3.4:** MOS FWBRs employing diode-connected transistors. (a) Partially cross-coupled PMOS FWBR [105]. (b) Fully cross-coupled CMOS FWBR [104].

It may seem sensible to modify the PMOS FWBR design in Figure 3.4(a) by cross-connecting all of the transistors. This would effectively replace both forward voltage drops with smaller drops arising from the on-resistance of a MOS switch. An example of this enhancement, which employs both NMOS and PMOS transistors, is shown in Figure 3.4(b). During positive half-cycles of the input voltage, current flows through MP1, MN2, and the output load (not shown), while transistors MN1 and MP2 are in cutoff mode. The situation is again reversed for negative half-cycles of the input voltage. The connection of the NMOS and PMOS bulk terminals, which are not shown for simplicity, are connected to $V_{out\,(-)}$ and $V_{out\,(+)}$, respectively; this is necessary to minimize substrate leakage and avoid latch-up [100]. In theory, this topology should offer improved PCE over the partially cross-coupled FWBR. However, it has been

shown that this variation suffers from significant reverse current flow from the output capacitor (not shown) to the input source [104].

CMOS FWBRs and their derivatives are typically targeted toward low-frequency systems (13.56 MHz and below) [100, 104, 105], and applications which include vibrational, magnetic, and implantable biomedical energy harvesting [106].

### Voltage Multiplier (Charge Pump)

Voltage multipliers, also known as charge pumps, are among the most widely used rectifier topologies in IC EH systems, especially in RFID tags which operate at the UHF and microwave frequency bands. One of the first IC voltage multipliers was presented in 1976 by John Dickson, and is eponymously known as the Dickson Charge Pump (DCP) [107]. The DCP is a minor variation of a much earlier configuration known as the Cockcroft-Walton multiplier, or sometimes as the Greinacher multiplier. This configuration, in turn, is similar to the Villard circuit. Although there exist minor differences among these configurations, the terms are often used interchangeably in EH literature. In this thesis, the terms "voltage multiplier" and "charge pump" will be used.

A generic, diode-based voltage multiplier (VM) is depicted in Figure 3.5. During negative half-cycles of the input waveform, current flows through $C_1$ and $D_1$, while diode $D_2$ is off. The capacitor $C_1$ is charged to $V_{in,\,pk} - V_D$ with the polarity shown in the figure; the voltage $V_D$ represents the forward voltage drop of the diode (it is assumed that $V_{D1} = V_{D2}$). During the following positive half-cycle of the input waveform, $D_1$ turns off while $D_2$ is turned on. Assuming that the capacitor is fully charged (and neglecting parasitic effects), the peak voltage at node X will be [48]:

$$\mathrm{V_X} \;=\; \mathrm{V_{in,\,pk}} \;+\; \mathrm{V_{C1}} \;=\; 2 \cdot \mathrm{V_{in,\,pk}} - \mathrm{V_D} \tag{3.3}$$

Meanwhile, the DC output voltage which is stored across $C_2$ is given by [48]:

$$\mathrm{V_{out}} \;=\; \mathrm{V_{C2}} \;=\; \mathrm{V_X} - \mathrm{V_D} \;= 2 \cdot (\mathrm{V_{in,\,pk}} - \mathrm{V_D}) \tag{3.4}$$

If $V_D$ is small compared to the input voltage, then the output voltage will be roughly double that of the peak input voltage. Thus, this circuit is sometimes referred to as a voltage doubler [48].

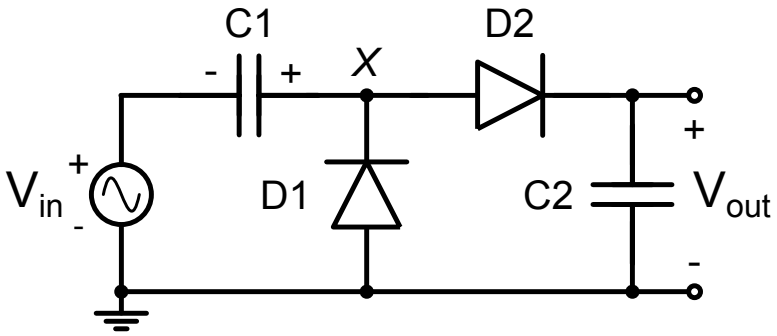


**Figure 3.5:** Diode-based voltage multiplier, or charge pump [48].

One of the most significant advantages of the voltage multiplier topology is its inherent scalability. That is, larger output voltages may be obtained by cascading unit stages of the circuit depicted in Figure 3.5. For example, a two-stage MOSFET-based charge pump is shown in Figure 3.6. For an arbitrary N-stage voltage multiplier, the steady-state output voltage when no current is drawn by the output load is given by [48]:

$$\mathrm{V_{out}} \;=\; 2 \cdot \mathrm{N}\,(\mathrm{V_{in,\,pk}} - \mathrm{V_{th}}) \tag{3.5}$$

Note that $V_D$ has been replaced by $V_{th}$, the threshold voltage of the transistors ($V_{th}$ is roughly equivalent to the effective forward voltage drop of a DCT). The analysis of an N-stage charge pump is similar to that of a single-stage voltage multiplier. In each unit stage, the intermediate nodes (*e.g.* node B in Figure 3.6) serve as reference nodes by which the unit-stage output voltage is referred to. Thus, charges are 'pumped' along through the unit stages until arriving at the output node. As a result, voltages are gradually scaled higher along the chain of unit stages. When implementing charge pumps in IC technology, care must be taken to avoid exceeding the maximum operating voltage of the capacitors and MOSFETs. This is especially important in the later unit-stages of the charge pump, where voltages are relatively large [48].

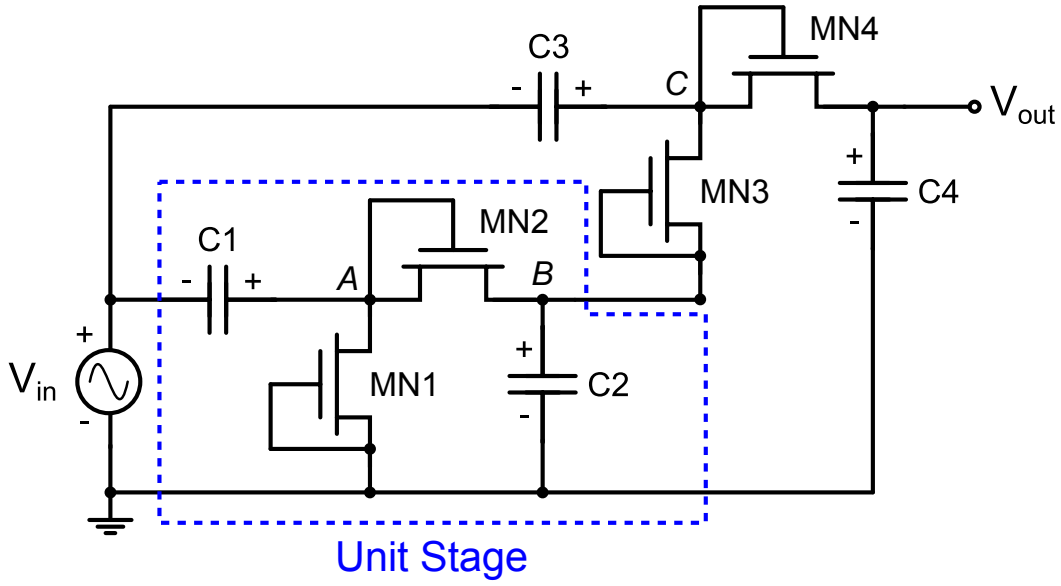


**Figure 3.6:** A two-stage MOSFET-based charge pump [108].

The mathematical analysis presented in this section is primarily intended to serve as an aid in understanding charge pumps and their design trade-offs. In reality, numerous factors affect the output voltage and PCE of a charge pump, including: the output

current drawn by the load, leakage current through the reverse-bias DCTs, and unit-stage parasitic capacitance. Equations relating these parameters to the output voltage are described in detail in [109, 110], while a rigorous analysis is provided in [111]. In practice, however, many researchers prefer to use simple mathematical models as a guide for their design, while employing circuit simulation tools to optimize the design. Design equations for the rectifier topology employed in the wireless X-ray dosimeter front-end of this thesis are discussed in Chapter 4.

As explained earlier, charge pump-based rectifiers are commonly employed in UHF and microwave EH systems due to the attractive levels of PCE which may be achieved. For example, in [112], a UHF charge pump implemented in 0.18 $\mu$m CMOS is presented. In [113], a 2.4 GHz charge pump implemented in 65 nm CMOS which achieved a PCE of over 40% is demonstrated. Finally, in [109], a 5.8 GHz charge pump was demonstrated using 0.13 $\mu$m CMOS technology. Numerous other examples of charge pumps may be found in literature.

### Dickson Charge Pump

The original Dickson Charge Pump, or DCP, is a variation of the voltage multiplier shown in Figure 3.5, and is implemented using two anti-phase clocks connected in an interleaving manner to the unit-stage capacitors. These clocks are used to pump electric charges from the input to the output node [107]. In modern EH systems, however, high-voltage clocks are not typically available. Hence, EH charge pumps are usually implemented as shown previously in Figure 3.6. Nonetheless, many designers refer to charge pumps such as Figure 3.5 as DCPs.

### 3.2.4 Design Techniques for High Efficiency Rectification

This section examines the evolution of modern design techniques which have been developed to achieve high PCE in rectifiers that are employed in EH systems. With the exception of the first technique, all of the techniques described in this section are based on the voltage multiplier topology shown in Figure 3.6.

#### Active Rectification

In practice, the CMOS FWBR described in the previous section (and shown in Figure 3.4(b)) may operate with a lower-than-expected PCE. One of the reasons this can occur stems from a design characteristic common to fully cross-coupled FWBRs: During operation, a reverse current may flow from the fully charged output storage capacitor back toward the input voltage source. Unlike diodes which are able to restrict the direction that current may flow, transistors, which effectively function as MOS switches in the CMOS FWBR, do not possess such a mechanism. Fortunately, this limitation can be overcome by the addition of an active rectification stage [106].

An example of a CMOS FWBR with additional active circuitry is presented in Figure 3.7. To control the direction of current flow, two components are added to the design: a PMOS pass transistor and a comparator. This extra circuitry is sometimes referred to as an active diode [100]. When the input voltage (from the output of the FWBR) is larger than the output voltage (*i.e.* the voltage stored across the energy storage device), the comparator generates a logic low signal (*e.g.* 0 V), causing the pass transistor to turn on. When the output voltage is larger than the input voltage, the comparator generates a logic high signal which causes the pass transistor to turn off, thus preventing current from flowing back towards the input. By espousing active circuitry with a CMOS FWBR, a highly efficient rectifier is obtained [106]. Note that,

although not shown in the figure, sampling circuitry is required at both inputs of the comparator [104]. The comparator may be implemented using a differential transistor pair, a latch, and inverter stage, as in [106].

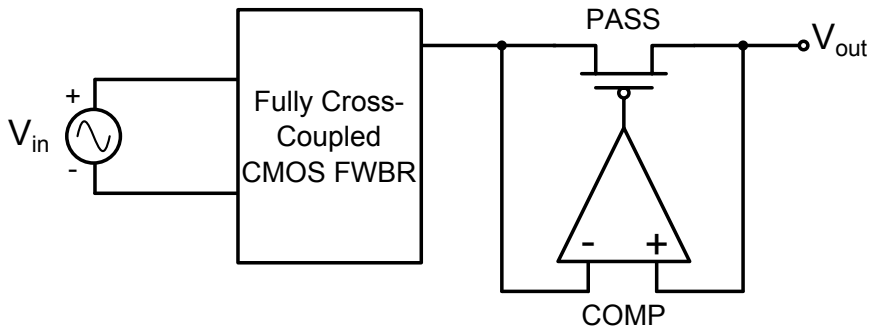


**Figure 3.7:** CMOS FWBR with active rectification stage [104].

There are, however, some notable drawbacks to this approach. Most importantly, the addition of active circuitry requires a stable power source from which to power the comparator. This fact proves especially troubling for passive RFID systems, which lack a regulated voltage supply prior to the rectifier stage. Furthermore, to achieve maximum PCE, the pass transistor is typically sized to be very large, so that its forward voltage drop is minimized. The size of the pass transistor, in turn, results in large parasitic capacitance that limits the maximum frequency the circuit may operate at [104]. This trade-off is highly prevalent in EH literature, where active rectifiers are typically employed in low-frequency applications (*i.e.* Hz to kHz range). Nonetheless, active rectifiers are able to achieve a high PCE, typically around 60–90% [100, 106]. In one unique example, researchers were able to achieve a PCE of nearly 82% at a comparably high frequency of 13.56 MHz using an additional speed-up comparator [114].

### Threshold Voltage Cancellation

The following high-efficiency design techniques belong to a pervasive trend among MOSFET-based rectifiers, particularly charge pumps. As noted earlier, commercial CMOS rectifiers are typically comprised of diode-connected MOSFETs, and the threshold voltage of these devices plays a significant role in determining the overall PCE of an EH system. However, there inevitably exists a trade-off between large and small transistors, *i.e.* between low on-resistance and minimal reverse leakage current. The following techniques employ various biasing schemes to vary the transistors' effective threshold voltages in ways which maximize PCE.

### External Threshold Cancellation

External $V_{th}$ Cancellation, or EVC, is one of the earliest cancellation techniques that was developed. A simplified EVC rectifier is depicted in Figure 3.8. Recall that the achievable output voltage of a conventional single-stage voltage doubler is given by [108]:

$$\mathrm{V_{out}} \;=\; 2 \cdot \;(\mathrm{V_{in,\,pk}} - \mathrm{V_{th}}) \tag{3.6}$$

To maximize PCE, it is necessary to minimize the input voltage that is required to generate the desired output voltage. From Equation 3.6, it is evident that this can be achieved by reducing $V_{th}$. However, utilizing low-$V_t$ transistors is not a viable solution, due to significant reverse leakage current. Alternatively, the gate-source voltages may be compensated by an external DC bias voltage, $V_{bth}$, as shown in Figure 3.8. If it is assumed that $V_{bth} \cong V_{th}$, then the equation for the output voltage becomes [108]:

$$\mathrm{V_{out}} \;=\; 2 \cdot (\mathrm{V_{in,\,pk}} - \mathrm{V_{th}} + \mathrm{V_{bth}}) \;\cong\; 2 \cdot \mathrm{V_{in,\,pk}} \tag{3.7}$$

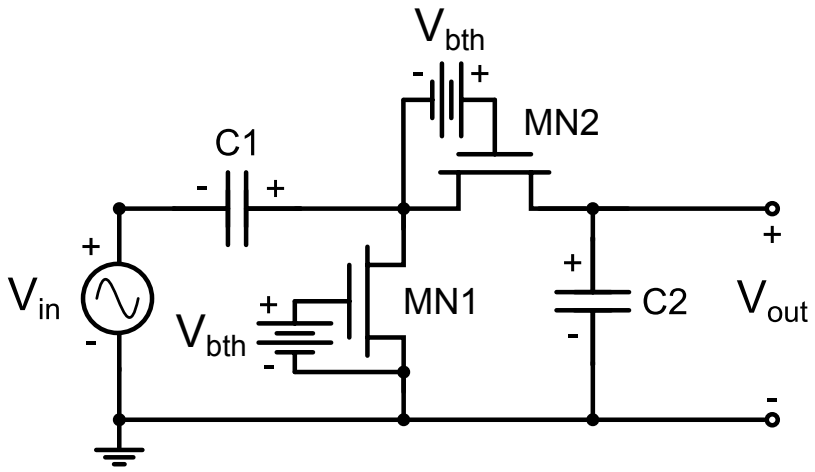


**Figure 3.8:** External $V_{th}$ Cancellation (EVC) rectifier [108].

The first EVC rectifier, demonstrated in [108], achieved a peak PCE of 11% at an operating frequency of 953 MHz. Although the EVC rectifier was shown to be more than twice as efficient as a conventional charge pump rectifier designed in the same technology, the overall PCE is considered to be very low by modern standards. In [108], capacitors were used to generate the necessary threshold cancellation. However, in multi-stage charge pumps, the rectified voltage is gradually scaled to higher voltages along the unit-stage chain. Therefore, each stage requires a different bias voltage. To accomplish this, a "$V_{bth}$ distribution network" is required, consisting of an elaborate array of pass transistors, charging capacitors, and a pulsed input signal (which are not shown in the figure). This circuitry presents additional overhead to the system power budget, which in turn limits the maximum achievable PCE. Furthermore, if the external bias voltage is not dynamically compensated, the transistors in a unit stage may both turn on, causing an undesirable reverse current to flow [108].

### Internal Threshold Cancellation

Internal $V_{th}$ Cancellation (IVC) is another form of threshold cancellation which uses additional circuitry (*i.e.* transistors, resistors, and capacitors) to generate a gate bias voltage from internal nodes within the rectifier. In contrast to the EVC technique, IVC requires relatively little extra circuitry. IVC was first demonstrated in a passive RFID tag using 0.35 $\mu$m CMOS/Ferroelectric-RAM technology. The design achieved a peak PCE of roughly 37% at a frequency of 953 MHz, representing a three-fold improvement over the EVC rectifier [115].

### Self-Threshold Cancellation

The IVC technique may be further refined by discarding the additional bias circuitry and directly connecting the transistor gates to nodes within the rectifier. This is referred to as Self-$V_{th}$ Cancellation (SVC). The first demonstrated SVC rectifier is shown in Figure 3.9 [116]. A CMOS implementation was chosen for its ability to minimize parasitic capacitance. The gate of the PMOS transistor is connected to the circuit ground, while the NMOS transistor's gate is connected to the output node. These gate connections effectively boost the gate-source voltage of the transistors, thereby lowering their threshold voltage. This results in dramatic improvements to PCE: at 953 MHz, the SVC rectifier achieved a PCE of 29%. This efficiency was obtained at a lower input power than the IVC rectifier in [115]; at the same power level, the IVC rectifier achieves a PCE of less than 20% [116].

Care must be taken, however, not to over-boost the gate-source bias voltages. Although the SVC rectifier performs well at low input power (making it ideal for use in passive RFID tags), performance at higher input powers is significantly curtailed.

When the input and rectified output voltages are large, the NMOS and PMOS transistors may remain turned on at all times, leading to the discharge and wastage of stored output energy [81].

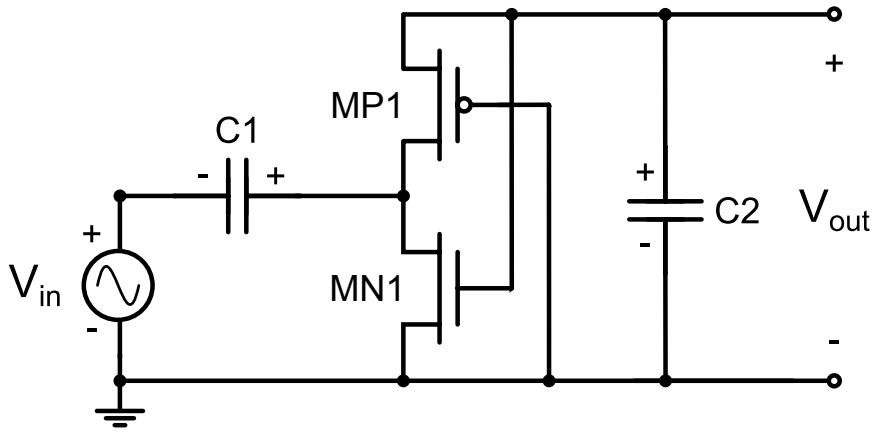


**Figure 3.9:** Self-$V_{th}$ Cancellation (SVC) rectifier [116].

### Dynamic Threshold Cancellation

The threshold cancellation techniques examined thus far rely on either generating an internal or external bias voltage, or selecting strategic nodes within the rectifier itself, in order to reduce the effective threshold voltage of the transistors. In other words, these schemes employ 'static' biasing techniques to change $V_{th}$ by a fixed amount. This inevitably leads to a compromise between achieving a low on-resistance and low reverse leakage current. Static $V_{th}$ cancellation techniques are only able to optimize the rectifier for a single operating condition. Naturally then, the next step in rectifier design would involve a dynamic cancellation scheme [81].

The first passive Dynamic $V_{th}$ Cancellation (DVC) scheme was demonstrated in [81] using 0.18 $\mu$m CMOS technology. This design achieved a PCE of nearly 67% at 953 MHz, or roughly double what the preceding IVC and SVC techniques are capable

of achieving. Furthermore, the DVC rectifier was shown to be capable of operating at up to 2 GHz while maintaining a PCE of approximately 50%. In addition, this circuit is relatively simple to design and requires no additional circuitry. Similar to the SVC rectifier, the DVC technique uses internal nodes within the rectifier to bias the transistor gates [81].

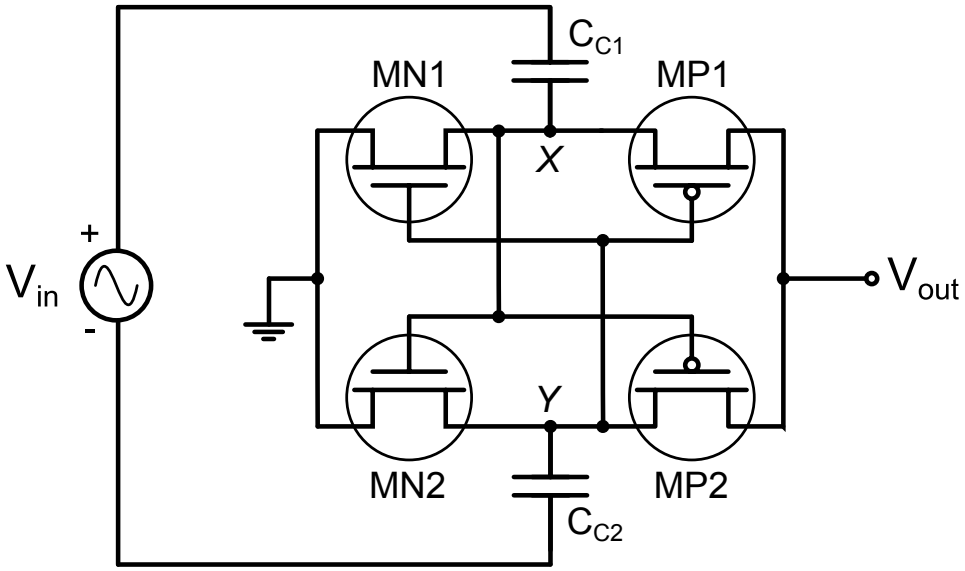


**Figure 3.10:** Dynamic $V_{th}$ Cancellation (DVC) rectifier [81].

An example of the DVC rectifier is shown in Figure 3.10. Its operation may be explained as follows. During positive half-cycles of the input waveform:

- Node X experiences a positive voltage amplitude. Since the gate terminals of MN2 and MP2 are tied to Node X, MN2 is turned on and MP2 is turned off.
- Node Y experiences a negative voltage amplitude. Since the gate terminals of MN1 and MP1 are tied to Node Y, MP1 is turned on and MN1 is turned off.
- A conduction path forms between the positive input terminal and the output node through $C_{C1}$ and MP1. The output storage capacitor (not shown) is

charged to approximately $V_{in,\,pk} + V_{C1} - V_{on}$, where $V_{in,\,pk}$ is the peak input voltage amplitude, $V_{C1}$ is the voltage stored across $C_{C1}$, and $V_{on}$ represents the voltage drop due to the on-resistance of MP1. It is assumed that $C_{C1}$ was charged to approximately $V_{in,\,pk} - V_{on}$ during the preceding negative half-cycle of the input waveform.

- A conduction path forms between the negative input terminal and the ground node through $C_{C2}$ and MN2. The coupling capacitor $C_{C2}$ is charged to approximately $V_{in,\,pk} - V_{on}$ [81].

For negative half-cycles of the input waveform, a complementary process occurs. Hence, the output voltage may be expressed as [81]:

$$\mathrm{V_{out}} \;=\; 2 \cdot (\mathrm{V_{in,\,pk}} - \mathrm{V_{on}}) \tag{3.8}$$

In this equation, $V_{on}$ represents the forward voltage drop across the transistors, which is a function of their on-resistance when operating as a MOS switch. DVC is achieved by employing a differential input voltage to dynamically vary the gate-source voltages of the transistors in such a way to provide optimal PCE. Consequently, the DVC rectifier performs full-wave rectification of the input voltage. This rectifier may alternatively be thought of as two cross-coupled SVC rectifiers. Although not shown in the figure, the body terminals of the PMOS and NMOS transistors should be connected to $V_{out}$ and ground, respectively [81]. The DVC rectifier is described in further detail in Chapter 4.

**Contemporary Trends: 2013 – Present**

Since design and development of the wireless X-ray dosimeter's energy harvesting front-end first began, several pervasive trends in RF rectification have emerged. For instance, the DVC rectifier has become commonplace among RF energy harvesters today. Due to their high achievable PCE and customizable multi-stage architecture, DVC rectifiers are still used today, even in the original configuration first presented in [81]. For example, researchers in [117] elected to implement the original DVC rectifier in their design of a 2.4 GHz wireless transceiver with embedded energy harvester.

Despite the widespread use of the original DVC rectifier topology, researchers have also attempted to improve this design through evolutionary modifications. These improvements generally involve a hybrid design approach, where the Dynamic $V_{th}$ Cancellation scheme is combined with other techniques. Most notably, researchers in [118] demonstrated a novel improvement to the DVC rectifier's PCE curve. The DVC rectifier's PCE, when plotted against input power, exhibits peak-like behaviour. Hence, optimal PCE is only achieved over a narrow range of input power. In [118], researchers were able to significantly extend the range of input powers for which maximum PCE is obtained, with only a minor reduction in peak PCE. This was achieved by the addition of quasi-floating gate transistors, which act as voltage sources that adjust the threshold cancellation effect over a wider range of input power compared to the original DVC rectifier [118].

Over the past several decades, much progress has been made toward highly efficient voltage rectification. It is likely that further advances will continue to be made, especially from the use of hybrid threshold cancellation approaches.

## 3.3 Voltage Regulator Topologies

In this section, a preliminary examination of voltage regulators is presented. The main approaches to regulator design will be discussed in terms of their applicability to energy harvesting systems.

### 3.3.1 Linear Regulators

Linear regulators represent one of the simplest forms of voltage regulation. A typical linear regulator is shown in Figure 3.11. The input voltage, $V_{in}$, is also referred to as the unregulated voltage, while the output voltage, $V_{out}$, is also known as the regulated voltage. An amplifier is used to force $V_{out}$ to track a reference voltage, $V_{ref}$. This reference voltage may be supplied by an off-chip source or implemented directly on-chip via a bandgap voltage reference circuit. The output of the amplifier is fed to the gate of MN1, which is also known as the pass transistor. This enables the amplifier to modulate the pass transistor's gate voltage, and hence, its drain-to-source voltage drop, in order to ensure that $V_{out} \cong V_{ref}$ [101].

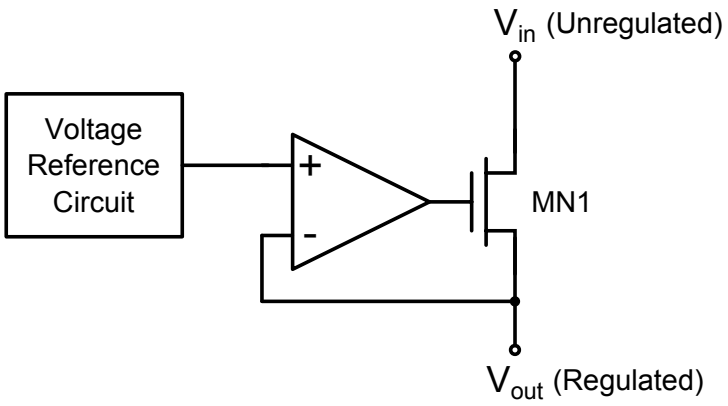


**Figure 3.11:** An example of a linear voltage regulator [101].

The minimum voltage drop across the pass transistor, or alternatively the minimum difference between the input and output nodes, is known as the dropout voltage. This attribute greatly influences the overall power efficiency of the regulator. To increase this efficiency, the NMOS transistor may be replaced by a PMOS transistor, and the polarity of the amplifier's input terminals may be reversed, to create what is known as a low-dropout (LDO) regulator. LDO regulators are able to achieve dropout voltages as small as 300–400 mV. However, compared to conventional linear regulators, they also exhibit a lower PSRR [101].

Linear and LDO regulators are comparatively simple to design and provide a relatively 'quiet' supply voltage. However, since the pass transistor must operate somewhere between the fully on and off states, the maximum achievable power efficiency is much lower than other regulators. A simplified expression for the power efficiency of a linear regulator is provided in Equation 3.9. Note that this equation does not account for the power dissipation of the amplifier [119].

$$\eta = \frac{\mathrm{P_{out}}}{\mathrm{P_{in}}} = \frac{\mathrm{I_{out}} \cdot \mathrm{V_{out}}}{\mathrm{I_{in}} \cdot \mathrm{V_{in}}} \tag{3.9}$$

The linear regulator's simple design and excellent noise performance are ideal qualities for energy harvesting systems. However, these regulators suffer from poor power efficiency, which is exacerbated by large input voltages (due to the fact that excess energy is dissipated by way of ohmic loss via the pass transistor). Moreover, the need for a bandgap voltage reference further limits the linear regulator's suitability to EH systems, especially in passive RFID tags [101, 110, 119].

### 3.3.2 Switching Regulators

Switching regulators, or converters, may be subdivided into three classes: (a) buck, (b) boost, and (c) buck-boost. Buck converters produce a regulated output voltage that is lower than the input voltage, whereas boost converters perform the opposite function. Buck-boost converters, meanwhile, are capable of producing an output voltage that is either higher or lower than the input voltage. Examples of buck and boost converters are shown in Figures 3.12(a) and (b), respectively [120].

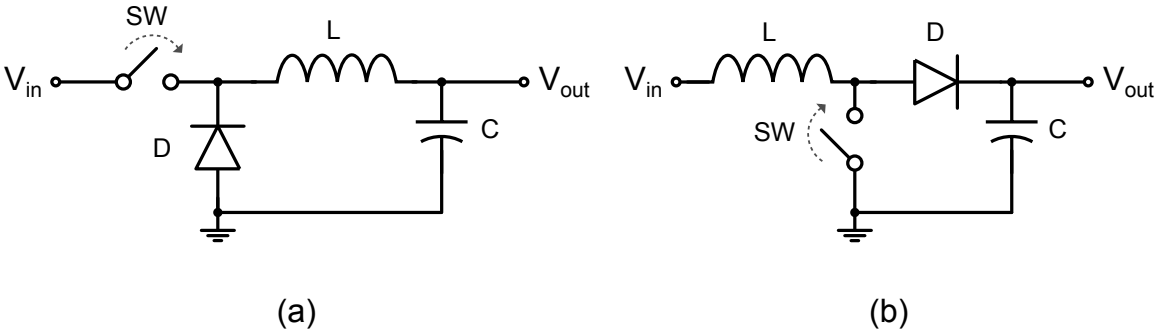


**Figure 3.12:** Switching regulators: (a) Buck converter; (b) Boost converter [120].

Recall that linear regulators utilize a pass transistor operating in the triode region to dissipate excess power through an ohmic loss. Switching regulators, on the other hand, employ reactive energy storage elements to regulate the output voltage. Furthermore, the switch, which may be implemented using a transistor, operates in either cutoff or saturation mode, thus exhibiting ideally zero power dissipation. Hence, switching regulators are theoretically 100% power efficient. However, in reality, parasitic losses in the various circuit elements contribute to a reduced power efficiency. Nonetheless, switching regulators offer superior efficiency when compared to linear regulators, and can often achieve over 90% power efficiency [119].

The operation of the buck converter shown in Figure 3.12(a) may be explained as follows. When the switch, SW, is closed, current flows through the inductor, capacitor, and output load, while the diode is reverse-biased. During this time, energy is stored in both the inductor and capacitor. When the switch is opened, the inductor opposes any abrupt changes in the current flowing through it. Consequently, along with the capacitor, the inductor continues to supply energy to the output load (the capacitor similarly ensures that voltage does not change abruptly at the output node). Together, the inductor and capacitor form an LC low-pass filter, resulting in an average DC voltage level at the output node. The duty cycle of the switch may be controlled via pulse-width modulation (PWM) to adjust the output voltage to the desired level. The boost converter in Figure 3.12(b) functions in a similar manner, with the exception that the output voltage is greater than the input voltage (note that this boosting effect is similar to the charge pumping mechanism of some rectifiers) [119, 120].

An alternative method to implementing switching regulators involves the use of switched capacitors. Switched capacitor-based voltage regulators employ a network of capacitors and switches which store and release energy at specific intervals [119].

In summary, the highly efficient nature of switching regulators makes them well-suited to use in EH systems. However, several limitations must be overcome, including considerable switching noise and the need for a switching source and controller. Furthermore, the requirement for an inductor of sufficient size may prove prohibitive to IC implementation. Even if implemented on-chip, however, the inductor introduces a significant area penalty, and thus an increased per-unit cost [110, 119, 120].

### 3.3.3 Smart Voltage Regulator

A third method of voltage regulation was introduced in [121]. This topology, depicted in Figure 3.13, is known as the Smart Voltage Regulator (SVR), and was designed specifically for semi-passive and active RFID systems which employ energy harvesting. The SVR is placed in parallel to the output of a charge pump-based rectifier, such that the output node (denoted by $V_{out}$) represents both the output of the rectifier and the regulator. A reference voltage, $V_{ref}$, meanwhile, is required for the SVR to function properly, and may be supplied by a bandgap voltage reference [121].

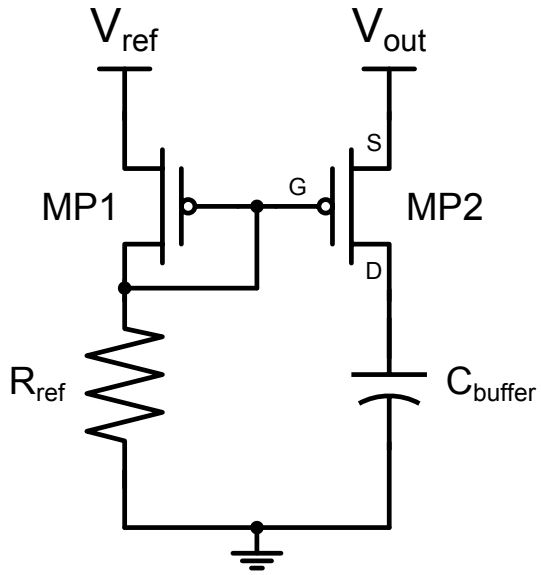


**Figure 3.13:** The Smart Voltage Regulator (SVR) topology [121].

The operation of the SVR is similar to a current mirror active load. As such, both transistors MP1 and MP2 must operate in saturation mode. The gate voltage of both transistors is fixed by the left-hand circuit branch consisting of $V_{ref}$, MP1, and $R_{ref}$. The SVR's voltage regulation mechanism stems from transistor MP2. For instance, when the input source of the rectifier (*e.g.* an antenna) experiences an increase in power, the output voltage of the charge pump rectifier necessarily increases. As a

result, the source voltage of MP2 increases, while the gate voltage remains fixed. Hence, the transistor's controlling source-gate voltage increases, as does its effective (or overdrive) voltage. Since MP2 is operating in the saturation region, an increase in the effective voltage causes an increase in current flowing through the transistor ($I_{sd2}$). Consequently, the output impedance of the right-hand circuit branch of the SVR (as seen by the rectifier) decreases, while the excess input power is stored in the buffer capacitor, $C_{buffer}$ [121].

The SVR has been shown to provide up to 85% power efficiency when the minimum and maximum voltages across $C_{buffer}$ are close in value. Unlike linear regulators, the SVR's power efficiency remains constant irrespective of the input power. This is due to the relatively constant power dissipation of MP2 [121].

The SVR topology attempts to blend the advantages of both linear and switching regulators together, making it well-suited to EH systems. It is ideal for use with charge pump rectifiers and does not require an inductor. The SVR is even simpler to design than a linear regulator, while offering better power efficiency. However, like linear regulators, it also requires a bandgap voltage reference. Furthermore, its ability to regulate the output voltage is fairly limited [121].

## 3.4 Summary

This chapter provided a thorough examination of energy harvesting systems, with an emphasis on RF EH systems. First, a system-level overview of EH systems was presented. It was explained that typical RF EH systems are comprised of an antenna, matching network, rectifier, voltage regulator, and, optionally, an energy storage device. Second, a literature review of voltage rectifiers was presented. This review

consisted of a mostly chronological presentation of rectifiers for EH systems. Several key techniques for achieving high efficiency were also examined. Finally, this chapter was concluded with a preliminary examination of voltage regulators and their suitability to EH systems. Three regulator topologies were examined: linear regulators, switching regulators, and the Smart Voltage Regulator.

# Chapter 4

# RF Energy Harvesting System and Rectifier Design

The purpose of this chapter is to fulfill two of the four research objectives outlined in Chapter 1 that pertain to engineering design. As part of these objectives, two systems related to the wireless X-ray dosimeter project are presented. First, a preliminary design of the RF energy harvesting (EH) module is described; this includes a discussion of the suggested implementation for each sub-block, as well as a summary of key performance specifications. Second, the design and simulation of a high-efficiency Dynamic $V_{th}$ Cancellation (DVC) rectifier is presented.

## 4.1 RF Energy Harvesting Module Design

This section outlines the preliminary design of an RF EH module that is intended for use within the wireless X-ray dosimeter tag. It includes a broad discussion and initial analysis of the RF EH module's various sub-blocks, including performance targets for several key design specifications. To avoid repetitive discussion, this section contains several references to design aspects that have already been described in Chapters 2 and 3.

### System Overview

The proposed RF EH module is presented in Figure 4.1. This architecture features a design similar to the generic EH system shown previously in Figure 3.1. In Chapter 2, it was noted that the X-ray dosimeter tag decodes an ASK-modulated signal, sent by the reader, containing the ID value of the tag that is to be interrogated. If the transmitted ID value matches the tag's ID and the energy storage device is sufficiently charged, then the tag's RF EH module will supply energy to the dosimeter tag's circuitry via both the rectified RF input and energy storage device. In this situation, the tag is considered to be in the active mode of operation. If the energy storage device is not sufficiently charged, then a pre-charging interval, as discussed in Section 2.4.3, is required prior to the demodulation of the tag ID. Alternatively, if the transmitted ID does not match the tag's ID, then the RF EH module will simply charge the off-chip energy storage device. Further discussion of the X-ray dosimeter tag is provided in Sections 2.3 and 2.4. A summary of the RF EH module's system-level specifications is provided in Table 4.1.

**Table 4.1:** Summary of system-level specifications for the proposed RF EH module.

| **Specification** | **Target** |
|---|---|
| Technology | IBM 0.13 $\mu$m CMOS |
| Energy source | 2.45 GHz intentional RF power source |
| Maximum operating range | 1 metre |

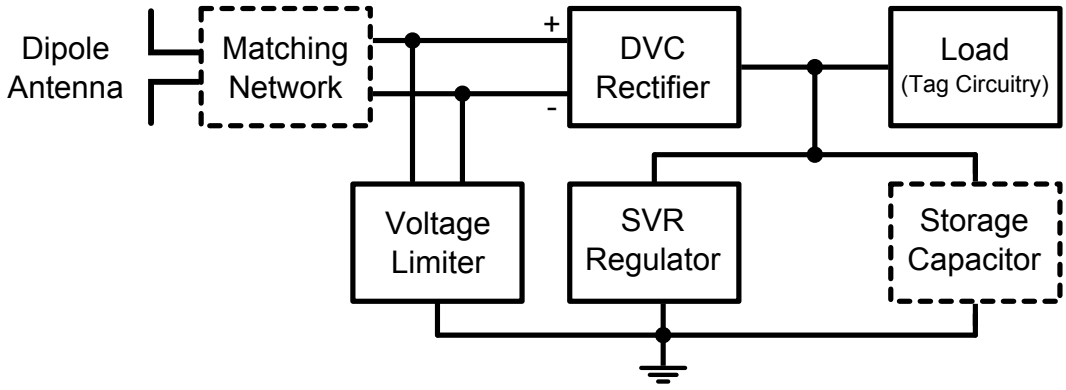


**Figure 4.1:** System-level overview of the proposed RF EH module. The antenna, in addition to sub-blocks which are inscribed by dashed lines, are to be implemented off-chip.

### Antenna

The X-ray dosimeter tag's antenna is employed by multiple subsystems, as illustrated in Figure 2.10, including the RF EH module. The proposed design consists of a half-wavelength dipole antenna implemented using a flexible inlay. Due to its differential operation, the dipole antenna is ideally suited for integration with high-efficiency full-wave rectifiers, such as the DVC rectifier. A summary of the antenna's specifications is provided in Table 4.2, while a detailed description is given in Section 2.3.2.

**Table 4.2:** Summary of specifications for the proposed RF EH module's antenna.

| **Specification** | **Target** |
|---|---|
| Configuration | Half-wavelength dipole |
| Construction | Compact flexible inlay |
| Length | 6.2 cm |
| Frequency | 2.45 GHz |
| Maximum gain | 2.2 dBi |
| Effective area | 19.6 $cm^2$ |

### Matching Network

The proposed RF EH module employs a reactive L-section matching network to conjugately match the dipole antenna's output impedance to the DVC rectifier's input impedance. The impedance of the rectifier is matched directly to that of the antenna, which maximizes the integration of the dosimeter tag IC and antenna. This approach is preferred over one which involves the use of an intermediate matching network to match each impedance to a 50 $\Omega$ system. The matching network will be designed based on experimental results obtained from the rectifier, and implemented off-chip using discrete components, which offer larger component values and higher Q (quality) factors compared to on-chip devices [122]. The self-inductance of the dosimeter tag IC's bond wires will also be incorporated into the matching network design.

### Voltage Limiter

Excessive input power to the RF EH module may occur in situations where the X-ray dosimeter reader and tag are placed in close proximity to one another. To avoid catastrophic damage to the tag's circuitry, a voltage limiter is required at each of the rectifier's inputs. Voltage limiters may be implemented as a series of diode-connected transistors, which shunt excessive energy to circuit ground during high-voltage situations. However, IC designers generally rely on electrostatic discharge (ESD) structures to provide such protection. ESD protection structures are often included in the IC process's design kit. For example, in the IBM 0.13 $\mu$m CMOS process, transistors are rated for a maximum voltage of 1.6 V; therefore the RF EH module's voltage limiter circuitry should be designed to limit input voltages to this maximum [73].

### Rectifier

Rectifiers for EH systems were discussed in detail in Section 3.2. From this discussion, it may be concluded that a high-efficiency topology, such as the DVC rectifier, represents the ideal solution for the proposed RF EH module. The DVC rectifier features a highly customizable architecture, provides full-wave rectification, and has been demonstrated to achieve a satisfactory PCE at frequencies of up to 2 GHz [81]. To determine whether it is possible to achieve high PCE when operating at 2.45 GHz, a DVC rectifier was designed based on the specific requirements of the X-ray dosimeter tag. The design and simulation of this rectifier is described in the next section, while experimental results are provided in Chapter 5.

A summary of target specifications for the proposed RF EH module's rectifier is provided in Table 4.3. The maximum input power was determined during the system link budget analysis in Section 2.4.2 to be 0.6 mW; this corresponds to the maximum power that the tag is capable of receiving under ideal conditions at a distance of one metre from the reader. An output voltage of 1.2 V was chosen based on the nominal operating voltage (*i.e.* $V_{DD}$) of the transistors in the IBM 0.13 $\mu$m CMOS process [73]. However, as explained in Section 2.3.2, additional circuitry may be required to convert this voltage to the $\pm$ 0.9 V supply required by the radiation sensor subsystem.

**Table 4.3:** Summary of specifications for the proposed RF EH module's rectifier.

| **Specification** | **Target** |
|---|---|
| RF input frequency | 2.45 GHz |
| Input power (max. at 1 m) | 0.6 mW (-2.2 dBm) |
| DC output voltage | 1.2 V |
| Peak PCE | $\geq$ 50% |

**Voltage Regulator**

From the discussion of voltage regulators in Section 3.3, it may be concluded that the ideal choice for the RF EH module is the Smart Voltage Regulator (SVR) depicted in Figure 3.13. This topology provides an ideal blend of characteristics between linear and switching regulators, offering both a relatively compact design and acceptable power efficiency. In addition, the SVR's most significant limitation – the need for a voltage reference, such as a bandgap voltage reference circuit – does not pose an issue for the wireless X-ray dosimeter, which features an energy storage capacitor that may be used to provide power to the SVR's voltage reference circuitry.

The efficiency of the SVR, $\eta_{svr}$, is related to the output voltage, $V_{out}$, and the minimum and maximum voltage across the buffer capacitor, $V_{cap,\,L}$ and $V_{cap,\,H}$, respectively, as given by [121]:

$$\eta_{\mathrm{svr}} \;=\; \frac{\mathrm{V_{cap,\,L}} + \mathrm{V_{cap,\,H}}}{2 \cdot \mathrm{V_{out}}} \tag{4.1}$$

Previously, in Section 2.4.2, the voltage regulator was assumed to have an efficiency of 75%. To achieve this level of efficiency for a nominal output voltage of 1.2 V, the SVR must satisfy the following equation:

$$\mathrm{V_{cap,\,L}} + \mathrm{V_{cap,\,H}} \;=\; 2 \cdot \eta_{\mathrm{svr}}\, \mathrm{V_{out}} \;=\; 1.8 \;\; \mathrm{V} \tag{4.2}$$

To satisfy this relation, the minimum and maximum voltage across the SVR's buffer capacitor may be set to 0.8 V and 1.0 V, respectively. However, it is crucial that the buffer capacitor's voltage does not exceed this range, or efficiency will significantly decrease. It is also important to note that the SVR's buffer capacitor and the RF EH module's energy storage capacitor are two distinct circuit elements which are

employed for different purposes. Nonetheless, the buffer capacitor may also require an off-chip implementation, depending on the SVR's final design requirements.

During the initial design of the SVR, large transistors must be used to minimize loss and ensure that the buffer capacitor can achieve its maximum voltage limit. The reference resistor (see Figure 3.13) should be sized to provide the appropriate transistor gate bias. Ultimately, the SVR's final design depends on the RF EH module's output load and the impedance presented by the rectifier; final design optimization should be performed via simulation. Preliminary specifications for the SVR are provided in Table 4.4.

**Table 4.4:** Summary of specifications for the proposed RF EH module's voltage regulator.

| **Specification** | **Target** |
|---|---|
| Nominal output voltage | 1.2 V |
| Reference voltage | 1.2 V |
| Buffer capacitor voltage swing | 0.8 – 1.0 V |
| Efficiency | 75% |

### Energy Storage

The proposed RF EH module employs a 2.2 $\mu$F Kemet C0805C225K8RACTU ceramic capacitor in a discrete SMT package for energy storage [93]. A discussion of energy storage options is provided in Section 2.4.3. Recall that energy storage is required by the X-ray dosimeter tag due to the insufficient quantity of power that may be transmitted by the reader. Earlier, it was determined that the storage capacitor must supplement the RF input by providing an additional 1.1 mW to the tag's circuitry. This quantity represents the amount of extra power required if the energy

storage device is located at the *input* of the RF EH module. However, as illustrated in Figure 4.1, the storage capacitor is placed at the output of this module. Hence, when energy is supplied (or discharged) by the capacitor, power loss due to the matching network and rectifier stages is not incurred. While the capacitor is being charged, however, these losses are present, resulting in a longer charging interval. Table 4.5 provides a summary of specifications for the energy storage device.

**Table 4.5:** Summary of specifications for the proposed RF EH module's energy storage.

| **Specification** | **Target** |
|---|---|
| Type | Ceramic capacitor (SMT package) |
| Part number | Kemet C0805C225K8RACTU |
| Capacitance | 2.2 $\mu$F |

### Output Load

The output load of the proposed RF EH module is comprised of the combined input impedance of the dosimeter tag's various subsystems, such as the radiation sensor, signal processing electronics, etc. (these subsystems are illustrated in Figure 2.10). Since many of these subsystems are being developed concurrently, the exact output impedance presented to the RF EH module cannot be determined prior to the design of this module. However, in EH literature, the load impedance generally ranges between 1 k$\Omega$ and 100 k$\Omega$ [81, 96, 100, 102, 104, 106, 114, 116, 118]. In lieu of an exact value, it will be assumed that the output impedance will fall into this range.

During the power budget analysis in Section 2.4.2, it was determined that the RF EH module must supply 263.1 $\mu$W of power to the tag. Some of this power will be supplied by the RF input, while the remaining portion will emanate from the energy

storage capacitor. To convert the maximum received RF input power of 0.6 mW to an output power of 263.1 $\mu$W, the RF module requires a PCE of 43.9% (Equation 3.1); based on the presumed efficiency of the backscatter modulator, rectifier, and voltage regulator, this is not achievable. Hence, an energy storage capacitor is required. To deliver the required power to the tag (*i.e.* 263.1 $\mu$W) at a nominal DC voltage of 1.2 V, the RF EH module requires an output impedance of:

$$R_{load} = \frac{V^2}{P_{out}} \doteq 5.5 \text{ k}\Omega \tag{4.3}$$

Consequently, this impedance would result in an output current of:

$$I_{out} = \frac{P_{out}}{V_{out}} \doteq 219.3 \ \mu\text{A} \tag{4.4}$$

However, it may not be possible to achieve this exact output impedance. If the total impedance is 1 k$\Omega$, for instance, the output power will be 1.44 mW and the load current will be 1.2 mA for an output voltage of 1.2 V. Alternatively, if the total output impedance is 100 k$\Omega$, then the output power and current will be 14.4 $\mu$W and 12 $\mu$A, respectively. Thus, the final output impedance value will ultimately determine the amount of power that is supplied to the load. A summary of specifications for optimal output loading is presented in Table 4.6.

**Table 4.6:** Summary of specifications for the proposed RF EH module's output load.

| **Specification** | **Target** |
|---|---|
| Impedance | 5.5 k$\Omega$ |
| Nominal voltage | 1.2 V |
| Current | 219.3 $\mu$A |
| Power delivered | 263.1 $\mu$W |

#### Additional Circuitry

Additional circuitry which is not shown in the proposed RF EH module's system diagram (Figure 4.1) may be required. For example, switching circuitry may be necessary to control the flow of current from the rectifier to the energy storage device and/or output load (to prevent the storage capacitor from discharging towards the input). This may be accomplished by inserting MOS switches between the rectifier and regulator stages. However, this modification would also result in increased overhead in the system power budget and additional loss within the RF EH module.

## 4.2 RF Rectifier Design and Simulation

This section presents the design and simulation results of the proposed RF EH module's voltage rectifier. While this design is based on the original DVC rectifier presented in [81], it has been specifically optimized for the wireless X-ray dosimeter's unique requirements. This involves the use of a higher RF input frequency and an IC CMOS process featuring a smaller gate length (0.13 $\mu$m versus 0.18 $\mu$m). Furthermore, this design incorporates several elements from the analysis of DVC rectifiers presented in [122], thus yielding a more rigorous design procedure than [81].

### 4.2.1 Design Overview

The design of the rectifier must naturally begin with a set of target specifications, an understanding of its operation, and an overview of the design procedure.

#### Target Specifications

To enable integration with the wireless X-ray dosimeter, the DVC rectifier must conform to the specifications outlined in Section 4.1 and summarized in Table 4.3.

Thus, the rectifier must operate at an RF input frequency of 2.45 GHz and provide a DC output voltage of 1.2 V, while ensuring a PCE of at least 50%. The maximum available RF input power is limited to 0.6 mW (-2.2 dBm). The ideal load impedance, as noted in Table 4.6, is 5.5 kΩ. However, as discussed earlier, an exact value of the load impedance is not known prior to the start of the design procedure. Therefore, a value between 1 kΩ and 100 kΩ which maximizes PCE is assumed to be acceptable.

### Rectifier Operation

Although the operation of the DVC rectifier was discussed briefly in Chapter 3, further investigation is required to find an optimal solution. Like charge pumps, DVC rectifiers may be analyzed by examining a single-stage design, as illustrated in Figure 4.2.

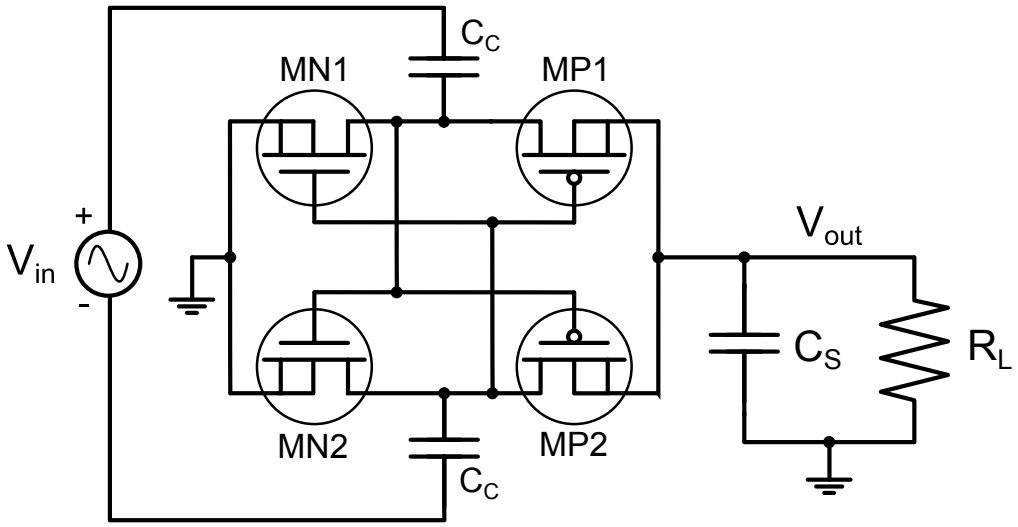


**Figure 4.2:** A single-stage DVC rectifier [81].

The DVC rectifier functions symmetrically as two distinct charge pumps which employ dynamic gate biasing. For instance, consider when the input terminal denoted by "+" in Figure 4.2 experiences a positive voltage such that $V_{in} \geq |V_{thp}|$, where $V_{thp}$

denotes the threshold voltage of the PMOS transistors (it is assumed that $|V_{thp}| \geq V_{thn}$, where $V_{thn}$ represents the threshold voltage of the NMOS transistors). In this situation, the gate voltages of transistors MP1 and MN1 are negative, while those of MN2 and MP2 are positive. Hence, MP1 and MN2 are turned on, while MN1 and MP2 remain off. Consequently, two current conduction paths are formed. In one case, charge from the positive input terminal is transferred through the upper coupling capacitor, $C_C$, and MP1, to the output load, represented by the resistor $R_L$. In the other, charge is transferred from the negative input terminal through the lower coupling capacitor and MN2, thereby effectively charging $C_C$ in preparation for the next half-cycle. When the polarity of the input source is reversed, the rectifier operates in a similar manner, with the exception that the transistors now function in the opposite manner as before, thus providing symmetrical operation. Note that a smoothing capacitor, $C_S$, is placed at the output terminal of the rectifier to store energy and minimize any ripple voltage which may arise from the inherent nature of full-wave rectification [81].

Next, consider the transfer of charge through the DVC rectifier during steady-state operation. At start-up, charges are pumped through the rectifier and the output voltage rises until the steady-state condition is reached. This charge transfer consists of several components, including: charge transferred by each transistor in the forward direction (towards the load), denoted by $Q_{Fwd,\,MP1}$, $Q_{Fwd,\,MP2}$, $Q_{Fwd,\,MN1}$, and $Q_{Fwd,\,MN2}$; and charge transferred by each transistor in the reverse direction (towards the circuit ground), denoted by $Q_{Rev,\,MP1}$, $Q_{Rev,\,MP2}$, $Q_{Rev,\,MN1}$, and $Q_{Rev,\,MN2}$ [81].

At steady-state, the net charge transferred by MN1 over one period of the input waveform, $T$, must equal the net charge transferred by MP1. Similarly, the net charge transferred by MN2 and MP2 over one operational cycle must also be equal.

If $Q_1$ and $Q_2$ denote these respective net charge transfers, then charge transfer in the DVC rectifier during steady-state operation may be expressed mathematically as follows [81]:

$$\mathrm{Q_{Fwd,\,MN1} - Q_{Rev,\,MN1} \;=\; Q_{Fwd,\,MP1} - Q_{Rev,\,MP1} \;=\; Q_1} \tag{4.5}$$

$$\mathrm{Q_{Fwd,\,MN2} - Q_{Rev,\,MN2} \;=\; Q_{Fwd,\,MP2} - Q_{Rev,\,MP2} \;=\; Q_2} \tag{4.6}$$

$$\mathrm{Q_1 + \; Q_2 \;=\; Q_L \;=\; \frac{V_{out}}{R_L} \cdot T} \tag{4.7}$$

As expressed by Equation 4.7, the amount of charge transferred to the load, $Q_L$, is equal to the sum of the net charge transferred in the upper and lower branches of the circuit. For symmetrical operation, $Q_1 = Q_2$. During start-up, the charge transferred by the transistors in the forward direction is greater than the charge which is transferred in the reverse direction. From these equations, it is also evident that, for a given input power level, optimum power efficiency occurs when $Q_L$ is maximized. This, in turn, involves maximizing $Q_1$ and $Q_2$. To accomplish this, both the reverse leakage current and the on-resistance of the transistors should be minimized, which may be achieved by increasing and decreasing the size of the transistors, respectively. This apparent contradiction results in a design trade-off, and consequently, an optimum transistor size [81].

The factors affecting the DVC rectifier's PCE and overall circuit operation may be better understood through an equivalent model. Due to the rectifier's symmetry between the upper and lower circuit branches, the design may be accurately characterized by considering only one-half of the design. This approach was employed

by [122] to obtain a simplified DC model of the DVC rectifier. From this model, the PCE may be expressed as follows [122]:

$$\mathrm{PCE} = \frac{\mathrm{P_{out}}}{\mathrm{P_{in}}} = \frac{\mathrm{V_{out}} \int_0^{2\pi} \mathrm{I}\, \mathrm{d}\theta}{\mathrm{V_{in,pk}} \int_0^{2\pi} \mathrm{I} \sin\theta\, \mathrm{d}\theta} \tag{4.8}$$

In this equation, $V_{out}$ denotes the output voltage, while $V_{in,pk}$ represents the amplitude of the input waveform, which is given by $V_{in} = V_{in,pk}\, sin\, \theta$, where $\theta$ is an arbitrary frequency term (in radians) [122]. Lastly, $I$ represents the current flowing through the equivalent model. A plot of the current waveform over a half-cycle of the input was demonstrated by [122] and is depicted in Figure 4.3.

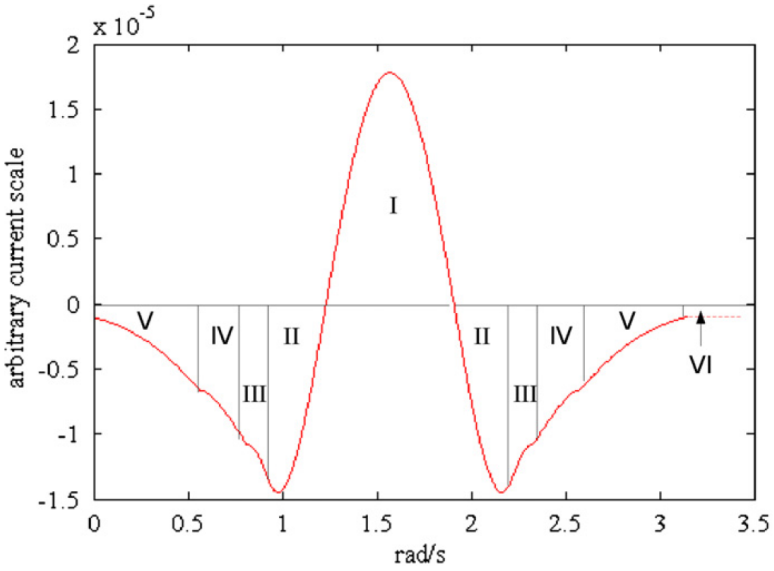


**Figure 4.3:** Current flow in the DVC rectifier's equivalent half-wave bridge rectifier DC model over a half-cycle of the input waveform. The current is divided into six regions of operation [122].

Due to the rectifier's highly non-linear operation, an expression for $I$ (from Equation 4.8) will also be non-linear. However, as shown in Figure 4.3, the waveform may be divided into six distinct regions of operation, and the current may be analyzed as a piece-wise model. These regions are summarized in Table 4.7. Further analysis,

including equations for each region, may be found in [122].

**Table 4.7:** A summary of regions of operation for the DVC rectifier's equivalent DC half-wave bridge model, which was demonstrated in [122]. It is assumed that $|V_{thp}| > V_{thn}$ and that the transistors are sized such that $V_{dsn} \cong |V_{dsp}|$. In addition, the following definition is employed: $v = V_{thp} + V_{thn} - V_{out}$. In region six, "reverse leakage mode" refers to a transistor that is turned off (*i.e.* zero gate-source voltage) and reverse-biased (*i.e.* the polarity of the drain-source voltage is reversed); hence, a small reverse leakage current flows [122].

| Region | Name | Condition | Operation |
|---|---|---|---|
| 1 | Forward Conduction | $V_{in} \geq V_{out}$<br>$V_{out} \geq \|V_{thp}\|$ | PMOS, NMOS in triode mode |
| 2 | Reversed Triode Conduction | $V_{in} < V_{out}$<br>$V_{in} \geq \|V_{thp}\|$ | PMOS, NMOS in triode mode<br>Reverse current flow |
| 3 | Partial Saturation | $V_{thn} \leq V_{in} < \|V_{thp}\|$ | PMOS in saturation mode<br>NMOS in triode mode |
| 4 | Full Saturation | $v \leq V_{in} < V_{thn}$ | PMOS, NMOS in saturation mode |
| 5 | Subthreshold Conduction | $V_{in} < v$ | PMOS, NMOS in subthreshold mode |
| 6 | Full Reverse Conduction | $-V_{out} \leq V_{in} \leq 0$ | PMOS, NMOS in reverse leakage mode |

An expression for PCE may be obtained by substituting the piece-wise expression for $I$ (obtained from the equivalent DC model) into Equation 4.8. The DC model, however, does not account for additional AC currents which are present when real transistors are considered. To capture this behaviour, an AC equivalent model is required. One such model was presented in [122], and includes a linear RC network in parallel with non-linear resistors, which are used to model the transistors' non-linear behaviour. Despite these equivalent models, however, it is not practical to obtain a

fully analytical solution (this conclusion is also affirmed by [122]). Therefore, it is necessary to appeal to simulation software for additional insight.

**Optimization Procedure**

Using a combination of equivalent models and simulation tools, it may be shown that the DVC rectifier exhibits a maximum PCE which depends primarily on three parameters: $g^2$, $V_{out}$, and $\delta$ [122]. These parameters will now be discussed.

The term $g^2$ represents the ratio of transistor properties, and is defined by Equation 4.9 [122]. In this equation, $\mu_n$ ($\mu_p$) refers to the electron (hole) mobility near the surface of the NMOS (PMOS) transistors, $C_{ox}$ represents the gate capacitance per unit area, and $(\frac{W}{L})_n$ ($(\frac{W}{L})_p$) corresponds to the width/length ratio of the NMOS (PMOS) transistors [101].

$$\mathrm{g}^2 \;=\; \frac{\beta_\mathrm{n}}{\beta_\mathrm{p}} \;=\; \frac{\mu_\mathrm{n}\,\mathrm{C_{ox}}\,(\frac{\mathrm{W}}{\mathrm{L}})_\mathrm{n}}{\mu_\mathrm{n}\,\mathrm{C_{ox}}\,(\frac{\mathrm{W}}{\mathrm{L}})_\mathrm{p}} \tag{4.9}$$

By solving the earlier expression for PCE (Equation 4.8), it is determined that the PCE does not depend solely on either $\beta_n$ or $\beta_p$, but on the ratio of the two. The optimum value for $g^2$ minimizes the amount of time that the rectifier remains in the subthreshold conduction region (region five of Table 4.7), by influencing the drain-source voltages ($V_{dsn}$ and $V_{dsp}$) of the transistors. Therefore, irrespective of process parameters, the transistor size ratio may be adjusted for maximum PCE [122].

The second influential parameter, $V_{out}$, refers to the DC output voltage of a single-stage DVC rectifier. For optimum PCE, $V_{out}$ must satisfy [122]:

$$|\mathrm{V_{thp}}| \;\leq \mathrm{V_{out}} \;\leq \mathrm{V_{in}} \tag{4.10}$$

This relationship ensures that the transistors operate as much as possible in the forward conduction region, and as little as possible in the reverse conduction region (refer to Figure 4.3 and Table 4.7). Thus, the transistors will operate in the triode mode and dissipate minimal energy. It is therefore concluded that the optimum value of $V_{out}$ will be a value slightly larger than $|V_{thp}|$ [122]. Note that this assumes that $|V_{thp}| \geq V_{thn}$, which for the target IBM 0.13 $\mu$m CMOS process, is valid [73].

The third parameter affecting PCE is denoted by $\delta$, and is defined by [122]:

$$\delta \;=\; \frac{\mathrm{V_{out}}}{\mathrm{V_{in,\,pk}}} \tag{4.11}$$

The value of $\delta$ must lie between zero and one. By re-examining Equation 4.8, it is evident that PCE is maximized when $V_{out} = V_{in,\,pk}$ and $\theta = \pi/2$, thus resulting in [122]:

$$\mathrm{PCE_{(max)}} \;=\; \frac{\mathrm{V_{out}}}{\mathrm{V_{in,\,pk}}} \;=\; \delta \tag{4.12}$$

Therefore, the ratio of output voltage to peak input voltage greatly influences the PCE (this is true for any value of $\theta$). Hence, PCE will be maximized when $\delta$ is also maximized [122].

In conclusion, an optimum solution for achieving maximum PCE from the DVC rectifier is obtained by solving [122]:

$$\frac{\partial\,\mathrm{PCE}}{\partial\,\mathrm{g^2}} \;=\; \frac{\partial\,\mathrm{PCE}}{\partial\,\mathrm{V_{out}}} \;=\; \frac{\partial\,\mathrm{PCE}}{\partial\,\delta} \;=\; 0 \tag{4.13}$$

A solution to Equation 4.13 is typically obtained via simulation. In [122], it was shown that, once an optimal solution is found, including values for $g^2$, $V_{out}$, and $\delta$,

the design may be adapted for any load current (or alternatively, load impedance) by scaling the transistor widths in such a way that $g^2$ remains constant. This approach offers additional design insight compared to other techniques in literature, which typically focus on optimizing the design for a specific load current [122].

Thus, from the analysis and insight on DVC rectifiers provided by [81] and [122], the following design procedure will be undertaken to obtain a design suitable for integration within the wireless X-ray dosimeter:

1. Beginning with a single-stage DVC rectifier architecture, a solution for optimum PCE will be obtained for an arbitrary load impedance. Next, the values of $g^2$, $V_{out}$, and $\delta$ will be extracted from the design.

2. Using the previously discussed scaling procedure, the transistor widths will be scaled to achieve maximum PCE at the desired load impedance, while maintaining the original value of $g^2$.

3. The design will be extended to a multi-stage architecture featuring the same component values as the single-stage version. An optimum number of stages will be determined, and final optimization will be performed to ensure maximum PCE.

4. A physical layout of the design will be developed, including an extraction of parasitic elements. Simulations will be repeated, and modifications to the design will be made if necessary.

### 4.2.2 Single-Stage Rectifier Design

This section presents the design and simulation results of a single-stage DVC rectifier. Since multi-stage rectifiers operate in a similar manner, it is crucial to first

characterize the performance of a single stage.

### Architecture Overview

The single-stage DVC rectifier is depicted in Figure 4.2. This rectifier consists of standard NMOS and PMOS transistors which are available from the IBM 0.13 $\mu$m CMOS design kit. RF transistor models are employed to ensure simulation accuracy at high frequency [97]. Low-$V_t$ devices are available, though, as discussed earlier, these transistors exhibit large reverse leakage currents, making them poorly suited to rectifiers [104]. As illustrated in the schematic, the bulk terminals of the NMOS and PMOS transistors are connected to circuit ground and $V_{out}$, respectively, in order to eliminate the body effect during steady-state forward operation [81].

An important transistor property which exhibits a noticeable impact on overall PCE is gate resistance. To minimize this effect, all transistors feature multiple gate fingers, whose parallel combination results in a low overall gate resistance. In this design, gate finger width will be maintained between 500–550 nm per finger [122].

The coupling and smoothing capacitors, meanwhile, are implemented as MIM capacitors. This capacitor implementation was chosen for its comparatively low substrate leakage, parasitics, and temperature dependence [86]. Furthermore, the capacitance per unit area is sufficient for the intended application.

### Parameter Extraction

To determine the condition for maximum PCE, the PCE optimization parameters (*i.e.* $g^2$, $V_{out}$, and $\delta$) are first determined for an arbitrary load impedance. The load impedance will be taken to be 5.5 k$\Omega$, which corresponds to the proposed RF EH

module's ideal output impedance. Capacitors $C_C$ and $C_S$, meanwhile, are initially set to 1.0 pF, which is similar to the capacitor values employed in [81, 122].

Next, simulations are performed using Cadence SpectreRF software to determine the optimum transistor size ratio for maximum PCE. Due to the highly non-linear nature of rectifiers, a large-signal periodic steady-state (PSS) analysis is required to accurately characterize the rectifier. While transient analysis is a viable alternative, PSS simulation provides a wider array of tools to effectively measure the rectifier's performance.

The transistor sizes which result in maximum PCE of the single-stage DVC rectifier are presented in Table 4.8. It should be noted that, to preserve symmetry, $W_{MN1} = W_{MN2}$ and $W_{MP1} = W_{MP2}$. In addition, all transistors are set to the minimum length, which, incidentally for the IBM 0.13 $\mu$m CMOS process, is 120 nm. Employing minimum-length transistors ensures high operating frequencies (*i.e.* fast switching) and minimal on-resistance.

**Table 4.8:** Summary of transistor sizes used to achieve maximum PCE from a single-stage DVC rectifier featuring a 5.5 k$\Omega$ load impedance.

| **Transistor** | **Length (nm)** | **Width ($\mu$m)** | **Finger Width (nm/finger)** |
|---|---|---|---|
| NMOS | 120 | 14 | 500 |
| PMOS | 120 | 46 | 500 |

The performance of the single-stage DVC rectifier at the point of operation where peak PCE is achieved is presented in Table 4.9.

**Table 4.9:** Summary of rectifier performance at the point of peak PCE operation for a single-stage DVC rectifier featuring a 5.5 kΩ load impedance.

| **Input Power** | **Peak Input Voltage** | **DC Output Voltage** | **PCE** |
|---|---|---|---|
| -12.72 dBm | 723.6 mV | 466.0 mV | 73.77 % |

The three PCE optimization parameters may now be extracted from these results. From Table 4.9, $V_{out} = 466.0$ mV, while $\delta$ may be found from the following expression:

$$\delta \;=\; \frac{\mathrm{V_{out}}}{\mathrm{V_{in,\,pk}}} \;\doteq\; 0.64 \tag{4.14}$$

To calculate $g^2$, the charge carrier mobility of the NMOS and PMOS transistors are required. These may be found from the IBM model library within Cadence. The electron mobility of the standard NMOS transistor, $\mu_n$, is 440 $cm^2/(V \cdot s)$, while the hole mobility of the standard PMOS transistor, $\mu_p$, is 94 $cm^2/(V \cdot s)$. The gate capacitance per unit area, $C_{ox}$, of the NMOS and PMOS transistors are equivalent and therefore cancel. Thus, the value of $g^2$ may be calculated from Table 4.8 as follows:

$$\mathrm{g^2} \;=\; \frac{\mu_\mathrm{n}\,\mathrm{C_{ox}}\,(\frac{\mathrm{W}}{\mathrm{L}})_\mathrm{n}}{\mu_\mathrm{p}\,\mathrm{C_{ox}}\,(\frac{\mathrm{W}}{\mathrm{L}})_\mathrm{p}} \;=\; \frac{\mu_\mathrm{n}\,\mathrm{W_n}}{\mu_\mathrm{p}\,\mathrm{W_p}} \;\doteq\; 1.42 \tag{4.15}$$

A summary of values for the PCE optimization parameters is provided in Table 4.10.

**Table 4.10:** Summary of PCE optimization parameters for a single-stage DVC rectifier featuring a 5.5 kΩ load impedance.

| $\boldsymbol{g^2}$ | $\boldsymbol{V_{out}}$ | $\boldsymbol{\delta}$ |
|---|---|---|
| 1.42 | 466.0 mV | 0.64 |

**Load Optimization**

Next, the extracted PCE optimization parameters will be used to scale the rectifier design to the desired output impedance (or load current). The load impedance will be scaled from 5.5 kΩ to 25 kΩ. Although the optimal load impedance of the proposed RF EH module was found to be 5.5 kΩ in Section 4.1, estimates for the dosimeter tag's power dissipation were not available prior to the design of the rectifier. Thus, a load impedance of 25 kΩ was assumed. With this load impedance and a nominal DC output voltage of 1.2 V, an output power of 57.6 $\mu$W and a load current of 48 $\mu$A is obtained (refer to Equations 4.3 and 4.4); these values are considered typical for RFID tags [48].

Using this new value for the load impedance (25 kΩ), simulations were again performed using different sizes of transistors while maintaining the same approximate value for $g^2$. The sizes of the coupling and smoothing capacitors were not modified. An optimal PCE was observed when the NMOS and PMOS transistor widths were set to 2.0 $\mu$m and 6.6 $\mu$m, respectively. This ratio results in a value for $g^2$ of approximately 1.42, which is identical to the value of $g^2$ obtained earlier for a load impedance of 5.5 kΩ.

To illustrate the influence of transistor sizing on the performance of the rectifier, Figure 4.4 presents the achieved PCE versus input power for three different PMOS widths (all other parameters, as indicated in the figure, are held constant). The results confirm the existence of an optimum transistor size ratio. Furthermore, it is observed that a larger PMOS width shifts the PCE curve left, while a smaller width produces the opposite effect. This is likely due to the proportional relationship between transistor width and drain-source current, which enables the rectifier to

operate at a lower input power when wider transistors are employed.

Furthermore, it should be noted that the PCE in Figure 4.4 is plotted with respect to the available input power, and does not indicate the true input power applied to the rectifier. Rather, this variable represents the specified power of a 100 Ω input source. This approach was taken due to the difficulty in obtaining parametric simulation results which are plotted against the actual input power, and does not affect the validity of the y-axis values. However, unless explicitly noted, all references to input power in this thesis refer to the *actual* input power applied (such as in Table 4.9).

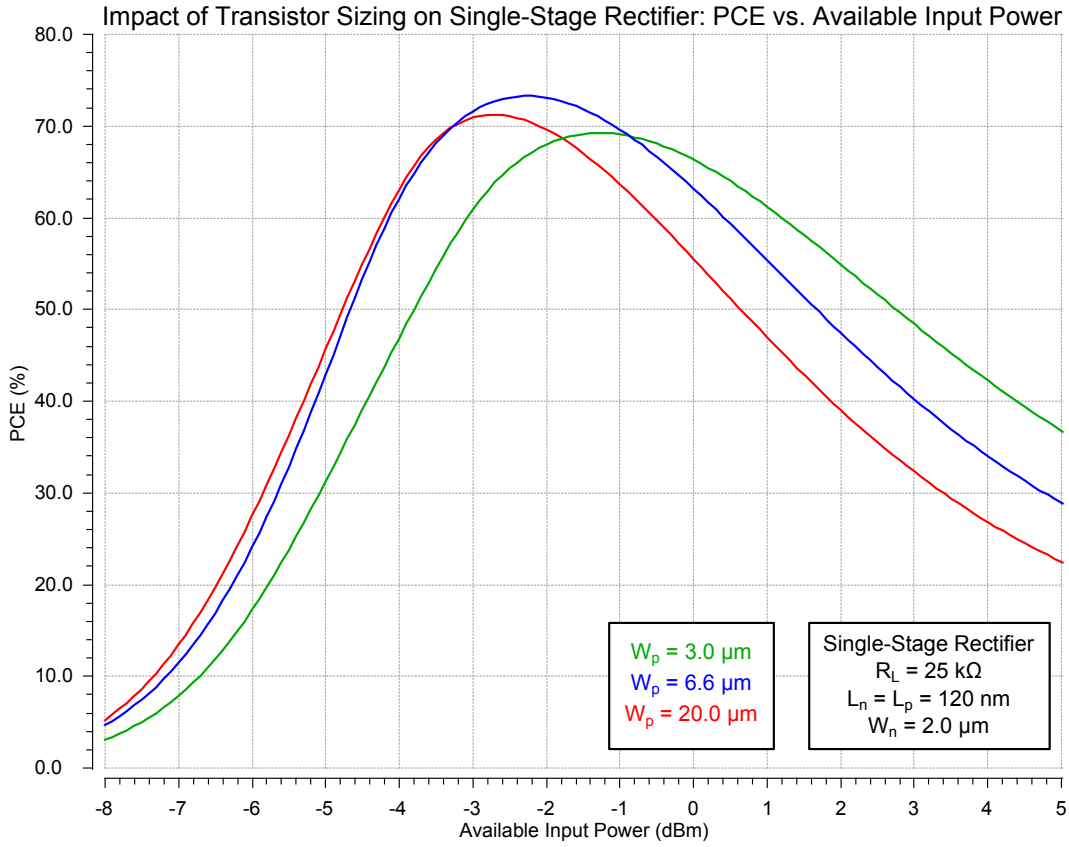


**Figure 4.4:** Effect of transistor sizing on the PCE of a single-stage DVC rectifier featuring a 25 kΩ load impedance. Three PMOS widths are shown: 3.0 $\mu$m, 6.6 $\mu$m, and 20.0 $\mu$m. The PCE is plotted with respect to the available input power of a 100 Ω source.

Similarly, the influence of transistor sizing on the rectifier's DC output voltage is demonstrated in Figure 4.5. From this graph, it is observed that the output voltage does not vary significantly according to transistor sizing.

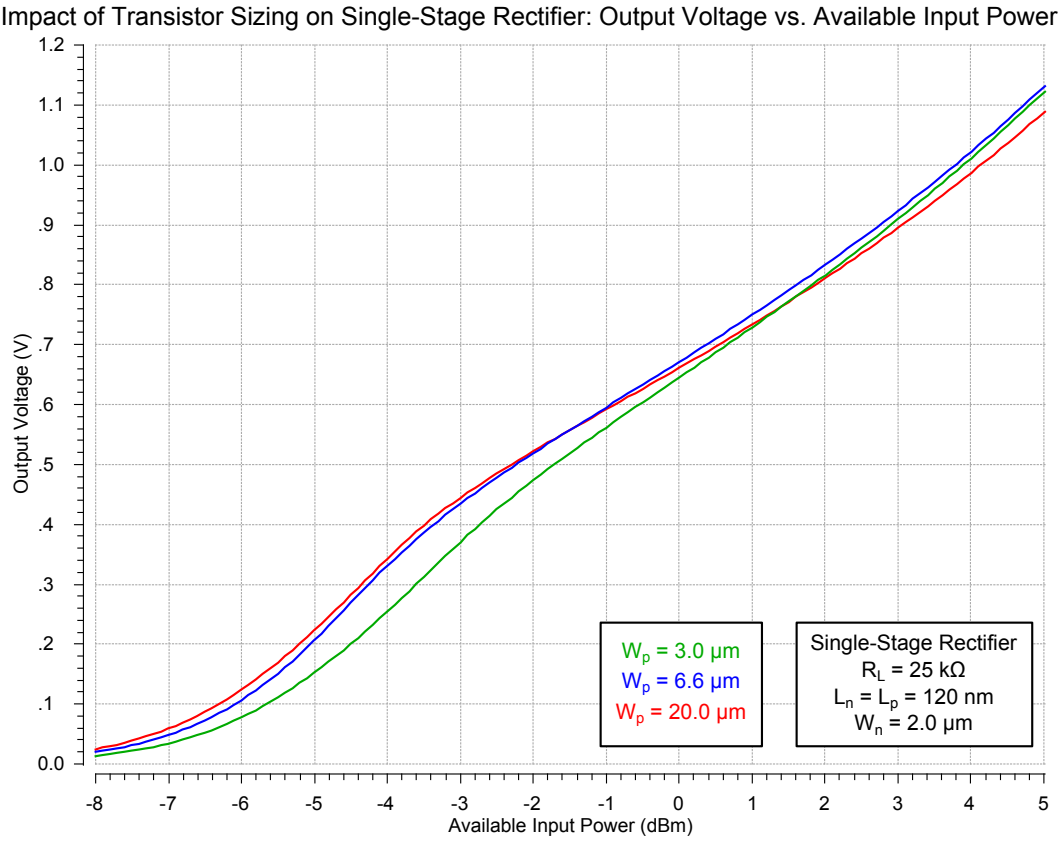


**Figure 4.5:** Effect of transistor sizing on the DC output voltage of a single-stage DVC rectifier featuring a 25 kΩ load impedance. Three PMOS widths are shown: 3.0 $\mu$m, 6.6 $\mu$m, and 20.0 $\mu$m. The output voltage is plotted with respect to the available input power of a 100 Ω source.

The transistor sizes, simulation results, and PCE optimization parameters for the single-stage DVC rectifier with 25 kΩ load impedance are summarized in Tables 4.11, 4.12, and 4.13, respectively.

**Table 4.11:** Summary of transistor sizes used to achieve maximum PCE from a single-stage DVC rectifier featuring a 25 kΩ load impedance.

| **Transistor** | **Length (nm)** | **Width ($\mu$m)** | **Finger Width (nm/finger)** |
|---|---|---|---|
| NMOS | 120 | 2.0 | 500 |
| PMOS | 120 | 6.6 | 550 |

**Table 4.12:** Summary of rectifier performance at the point of peak PCE operation for a single-stage DVC rectifier featuring a 25 kΩ load impedance.

| **Input Power** | **Peak Input Voltage** | **DC Output Voltage** | **PCE** |
|---|---|---|---|
| -18.74 dBm | 682.1 mV | 494.5 mV | 73.23 % |

**Table 4.13:** Summary of PCE optimization parameters for a single-stage DVC rectifier featuring a 25 kΩ load impedance.

| $g^2$ | $V_{out}$ | $\delta$ |
|---|---|---|
| 1.42 | 494.5 mV | 0.73 |

When comparing Table 4.10 to 4.13, it is observed that the PCE optimization parameters do not, in fact, remain constant, but vary slightly. Nonetheless, peak PCE remains nearly identical, demonstrating that it is possible to maintain the optimal PCE regardless of load impedance, provided that $g^2$ remains constant.

### 4.2.3 Multi-Stage Rectifier Design

Based on the requirements of the wireless X-ray dosimeter, it is not possible to achieve a nominal output voltage of 1.2 V from a single-stage DVC rectifier. Thus, multiple stages must be used to obtain a larger output voltage. If sized identically,

each unit stage within a multi-stage rectifier operates in the same manner. This section examines a multi-stage rectifier design suitable for the proposed RF EH module.

### Optimum Number of Stages

As noted earlier, the condition for optimum PCE occurs when the output voltage is slightly larger than $|V_{thp}|$ (where $|V_{thp}| \geq V_{thn}$). For a standard PMOS transistor from the IBM 0.13 $\mu$m CMOS design kit, a typical value for the threshold voltage is -430 mV. Hence, maximum PCE should be obtained for a value slightly above this absolute voltage. This was demonstrated during the single-stage rectifier design, where the values for $V_{out}$ were found to be 466.0 mV and 494.5 mV. Therefore, the optimum number of stages, $N_{opt}$, may be determined by [122]:

$$\mathrm{N_{opt}} = \frac{\mathrm{V_{out}}}{|\mathrm{V_{thp}}| + \Delta} \tag{4.16}$$

In this equation, $\Delta$ represents a positive offset from the PMOS threshold voltage. If $V_{thp}$ is taken to be -430 mV and $\Delta = 50$ mV, then $N_{opt} = 2.5$ for an output voltage of 1.2 V. Thus, a two- or three-stage rectifier would be equally as effective. However, a two-stage design is comparatively simpler and requires less chip area. Furthermore, in [81], it was observed that maximum PCE for a single-stage rectifier occurs between 0.5 V and 0.8 V. Therefore, a two-stage architecture will be implemented.

### Architecture Overview

A schematic of the two-stage DVC rectifier is depicted in Figure 4.6. Although not shown, transistors MN3 and MN4 are implemented as triple-well RF NFET transistors. This allows for the elimination of the body effect in the second stage NMOS transistors, since the transistors' bulk terminals do not need to be connected to the

substrate (which itself is connected to circuit ground). In addition, the coupling and smoothing capacitors remain set to 1.0 pF. However, an additional intermediate capacitor, $C_{int}$, is added between the first and second rectifier stages. This capacitor is used to minimize the minor voltage ripple which may be present due to imperfect symmetry between circuit branches, and is implemented as a 100 fF MIM capacitor. Ideally, however, inter-stage capacitors are not needed [81].

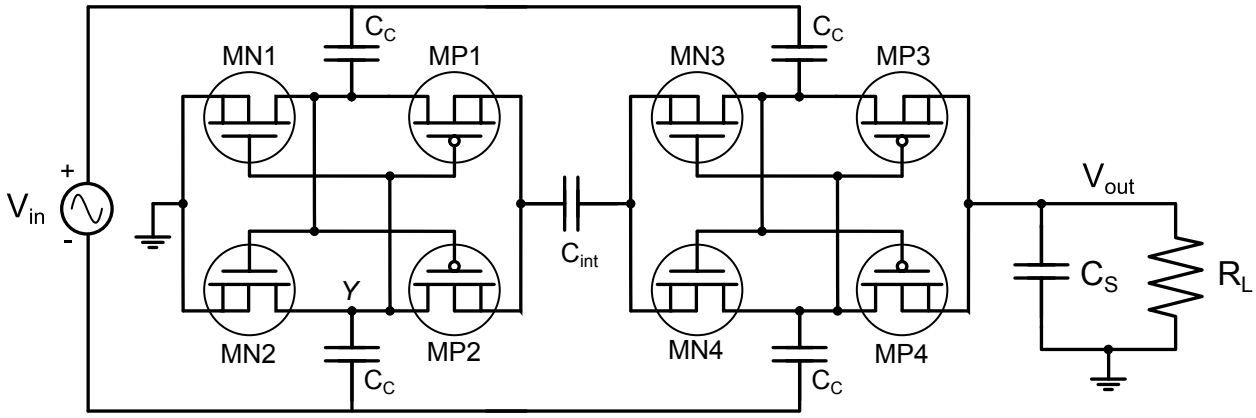


**Figure 4.6:** A two-stage DVC rectifier [81].

### Two-Stage Rectifier: Initial Performance

In the initial design of the two-stage DVC rectifier, the same transistor sizes that were used to obtain maximum PCE in the single-stage DVC rectifier with 25 kΩ load impedance were employed (refer to Table 4.11). Since the transistor size ratio is not changed, the value of $g^2$ remains approximately 1.42. A summary of the simulated rectifier performance is provided in Table 4.14. Compared to the single-stage design, peak PCE is reduced by approximately 2.5%. This may be due to additional parasitic capacitance which is inevitably introduced when adopting a multi-stage design, and further optimization would likely improve performance. However, to avoid redundant effort, further tuning of transistor sizes is deferred until the design is finalized.

**Table 4.14:** Summary of rectifier performance at: (A) the point of peak PCE operation, and (B) when $V_{out} = 1.2\ V$, for the initial two-stage DVC rectifier design featuring 25 kΩ load impedance.

| | **Input Power** | **Peak Input Voltage** | **DC Output Voltage** | **PCE** |
|---|---|---|---|---|
| (A) | -11.66 dBm | 806.6 mV | 1.10 V | 70.74 % |
| (B) | -10.86 dBm | 864.2 mV | 1.20 V | 70.17 % |

### Capacitor Sizing

If sized incorrectly, the DVC rectifier's coupling capacitors may reduce maximum PCE and lower the output voltage. Similar to charge pumps, the role of these capacitors is to store charge in one half-cycle of the input waveform, and release this charge during the subsequent half-cycle into the load impedance. As seen in Figure 4.6, the coupling capacitors form a capacitive divider with the parasitic capacitance of the transistors. An expression for the effective capacitance as seen at the input of a two-stage DVC rectifier is shown in Equation 4.17 [122]. The terms $C_p$ and $C_n$ refer to the total parasitic capacitance ($C_{Total}$) of the PMOS and NMOS transistors, respectively. In this design, there are a total of four coupling capacitors ($C_C$), four NMOS transistors, and four PMOS transistors.

$$\mathrm{C_{eff}} \;=\; \frac{4 \cdot \mathrm{C_C} \cdot \mathrm{C_{Total}}}{\mathrm{C_C} + \mathrm{C_{Total}}} \;=\; \frac{4 \cdot \mathrm{C_C}\,(\mathrm{C_n} + \mathrm{C_p})}{\mathrm{C_C} + \mathrm{C_n} + \mathrm{C_p}} \tag{4.17}$$

Thus, the coupling capacitors should be sized large enough to minimize the effect of the capacitive divider, but small enough that they are fully charged during one half-cycle of the input waveform. Simulation data illustrating the effect of coupling capacitor size on the two-stage rectifier's PCE and output voltage are shown in Figures 4.7 and 4.8, respectively (note that the PCE and output voltage are plotted with

respect to the available input power). From these results, it is observed that values larger than 1.0 pF noticeably reduce the peak PCE (by more than 6%), while smaller values exhibit little effect on PCE. However, as shown in Figure 4.8, smaller coupling capacitor values result in a slightly lower output voltage. Thus, based on these results, the coupling capacitors were chosen to be 1.0 pF.

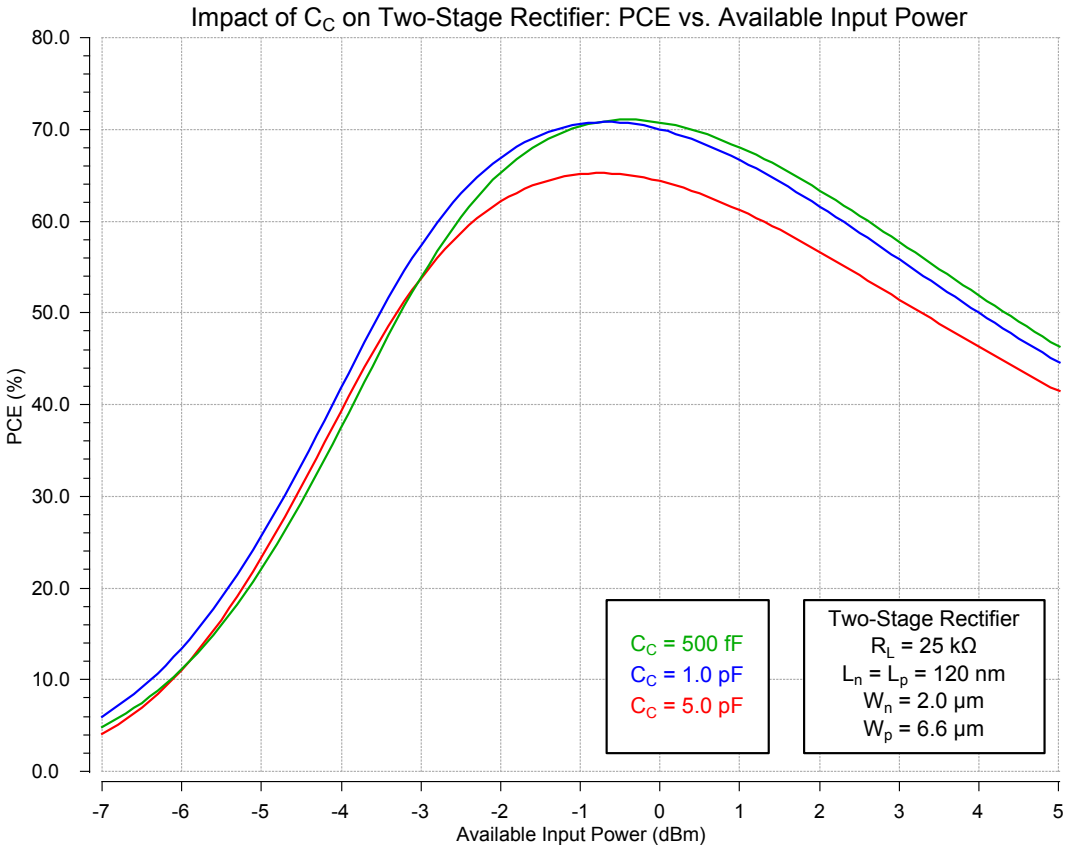


**Figure 4.7:** Effect of coupling capacitor ($C_C$) size on the PCE of a two-stage DVC rectifier featuring a 25 kΩ load impedance. Three capacitor values are shown: 500 fF, 1.0 pF, and 5.0 pF. The PCE is plotted with respect to the available input power of a 100 Ω source.

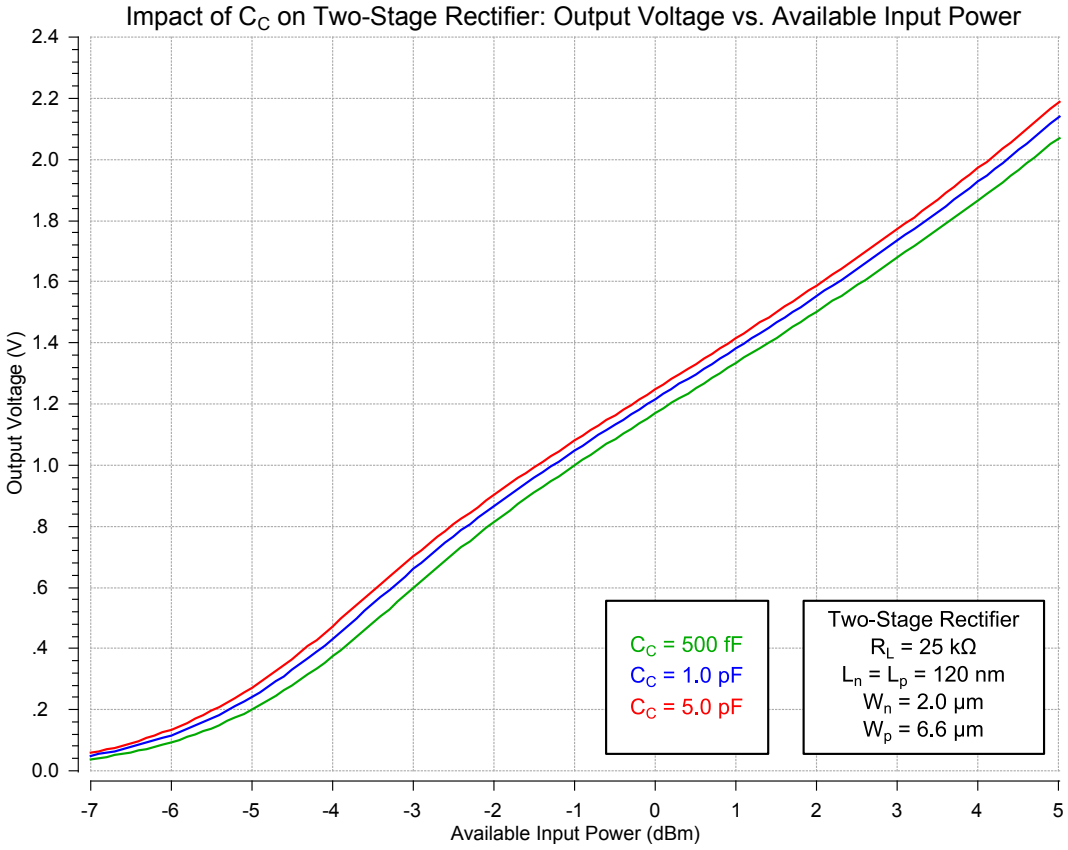


**Figure 4.8:** Effect of coupling capacitor ($C_C$) size on the DC output voltage of a two-stage DVC rectifier featuring a 25 kΩ load impedance. Three capacitor values are shown: 500 fF, 1.0 pF, and 5.0 pF. The output voltage is plotted with respect to the available input power of a 100 Ω source.

The output smoothing capacitor, $C_S$, was selected to be 1.0 pF. It was determined that this value provides an acceptable reduction in the output voltage ripple without diminishing the PCE. Similarly, the inter-stage capacitor, $C_{int}$, was optimally chosen to be 100 fF.

### Bond Pad Implementation

Bond pads provide the necessary interface between an IC and its surrounding environment (*e.g.* a PCB, test fixture, or probing station). They consist of large,

square-shaped metallic structures which are situated on the uppermost metal layer of an IC in order to provide an exposed area which may be contacted by a test probe or bond wire. Due to their physical size, which typically ranges between 100 $\mu$m and 150 $\mu$m in length, bond pads introduce significant parasitic capacitance into an IC design. This effect is due both to the fact that bond pads function undesirably as parasitic capacitors with respect to the substrate, and to the proportional relationship between plate area and capacitance. Fortunately, however, since the output of the rectifier is a DC voltage, this capacitance does not represent a concern for the output terminal. Therefore, the default size of 108 $\mu$m may be employed for the DC output pad [73].

The differential RF input terminals, however, are highly sensitive to parasitic capacitance. For example, when conventionally sized bond pads are incorporated into the two-stage rectifier design, the maximum PCE is significantly reduced. This effect may be minimized by decreasing the size of the bond pads. Thankfully, this is possible due to the availability of precision RF probes, which offer a very small pitch (*i.e.* centre-to-centre pad spacing). Consequently, the input bond pads were reduced to 75 $\mu$m in length, which is close to the minimum size permitted by the IBM 0.13 $\mu$m CMOS process [73]. In addition, the bond pads were changed from rectangular to octagonal shapes to further minimize the total pad area, and hence, parasitic capacitance. After employing these modifications, the impact of bond pads on the rectifier's performance was limited to a 2.0% reduction in maximum PCE.

### Electrostatic Discharge Concerns

IC designs typically require that ESD protection structures be connected to bond pads in order to shield against damage caused by electrostatic discharge during either IC manufacturing or laboratory testing. Common structures include a "double-diode"

configuration, which limits the bond pad voltage to within one forward diode voltage drop above and below the maximum and minimum IC supply voltages, respectively. These structures are especially important for bond pads which are connected to transistor gate terminals, since an accumulation of charge on the gate may destroy the transistor [73].

Due to the nature of rectifiers, however, the double-diode ESD structure is not a viable solution. This is due to the fact that a rectifier does not possess power supply rails (excluding the DC output terminal). However, since all transistor gate terminals in the DVC rectifier are also connected to source/drain regions of other transistors, any accumulation of charge at these nodes will be dissipated to the substrate through one of the drain-body or source-body parasitic diodes of the transistors. Therefore, it is concluded that ESD structures are not required for this design (a similar design decision was taken in [81]).

**Final Design Optimization**

The final stage in the design process involves fine-tuning the DVC rectifier by adjusting the transistor size ratios. This is necessary to account for second-order effects which may lead to a slightly different condition for optimum PCE than what is predicted by the transistor scaling technique. In addition, further optimization is necessary to account for the effect of bond pads on the performance of the rectifier. The final design results are presented in the following section.

### 4.2.4 Final Design Summary

This section presents the final design specifications and performance results of the two-stage DVC rectifier, which is designed to achieve optimum PCE while generating

a nominal output voltage of 1.2 V for a load impedance of 25 kΩ. This rectifier is suitable for integration within the wireless X-ray dosimeter project and conforms to the requirements of the proposed RF EH module (refer to Section 4.1).

### Physical Specifications

A summary of the transistor sizes that were obtained after final optimization tuning is provided in Table 4.15. Both NMOS and PMOS transistor sizes were increased slightly to account for second-order effects and the addition of bond pads to the design. Final capacitor values are listed in Table 4.16, while bond pad geometries are summarized in Table 4.17.

**Table 4.15:** Summary of transistor sizes used to achieve maximum PCE in the final two-stage DVC rectifier with 25 kΩ load impedance.

| **Transistor** | **Length (nm)** | **Width ($\mu$m)** | **Finger Width (nm/finger)** |
|---|---|---|---|
| NMOS | 120 | 3.0 | 500 |
| PMOS | 120 | 9.0 | 500 |

**Table 4.16:** Summary of capacitor sizes in the final two-stage DVC rectifier with 25 kΩ load impedance.

| **Capacitor** | **Capacitance** |
|---|---|
| $C_C$ | 1.00 pF |
| $C_{int}$ | 100.0 fF |
| $C_S$ | 1.00 pF |

**Table 4.17:** Summary of bond pad sizes in the final two-stage DVC rectifier with 25 kΩ load impedance.

| Bond Pad | Shape | Side Length ($\mu$m) |
|---|---|---|
| Positive RF Input | Octagonal | 75 |
| Negative RF Input | Octagonal | 75 |
| DC Output | Rectangular | 108 |

### Simulation Results

The simulation results of the final two-stage DVC rectifier are summarized in Table 4.18 and presented graphically in Figure 4.9. At the desired output voltage of 1.2 V, the rectifier achieves a PCE of over 68%. This result, in contrast to the target PCE of 50% which was established by the requirements of the proposed RF EH module, represents a considerable design margin. In fact, a PCE of 50% is maintained over a relatively wide input power ranging from -16.21 dBm to -6.24 dBm. Furthermore, when compared to earlier rectifier designs, including the single-stage DVC rectifier, these results do not differ significantly. Therefore, it may be concluded that the design procedure involving the characterization of a unit-stage rectifier, in conjunction with the transistor scaling technique, results in a favorable outcome in which the original design objectives are handily achieved.

**Table 4.18:** Summary of rectifier performance at: (A) the point of peak PCE operation, and (B) when $V_{out} = 1.2\ V$, for the final two-stage DVC rectifier with 25 kΩ load impedance.

| | Input Power | Peak Input Voltage | DC Output Voltage | PCE |
|---|---|---|---|---|
| (A) | -12.07 dBm | 750.5 mV | 1.04 V | 70.16 % |
| (B) | -10.75 dBm | 839.2 mV | 1.20 V | 68.47 % |

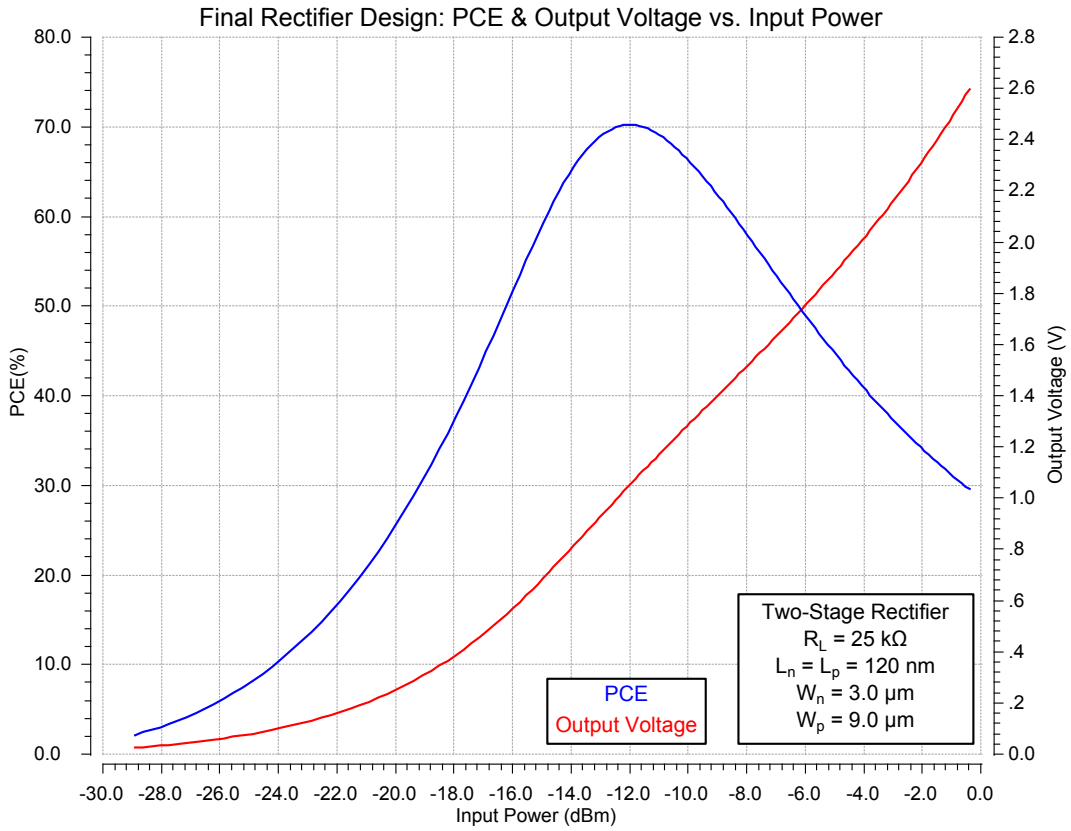


**Figure 4.9:** Simulated PCE and output voltage ($V_{out}$) of the final two-stage rectifier with 25 kΩ load impedance versus input power .

The transient behaviour of the DVC rectifier is illustrated in Figure 4.10. When an input power of -10.73 dBm is applied, the rectifier achieves steady-state operation in approximately 34.2 ns. After 16.0 ns, the output voltage of the rectifier has already reached 92% of its steady-state value. Hence, the rise time or start-up time of the rectifier is very short when compared to the typical data rate of RFID tags [48].

During steady-state operation, the rectifier generates a nominal voltage of approximately 1.2 V, while exhibiting a minor voltage ripple of 7.04 m$V_{pp}$ (peak-to-peak). However, if the input power level fluctuates, then the rectifier's output voltage will vary accordingly. Hence, as explained in Section 4.1, a voltage regulator is required

at the output of the rectifier in order to maintain a constant supply voltage.

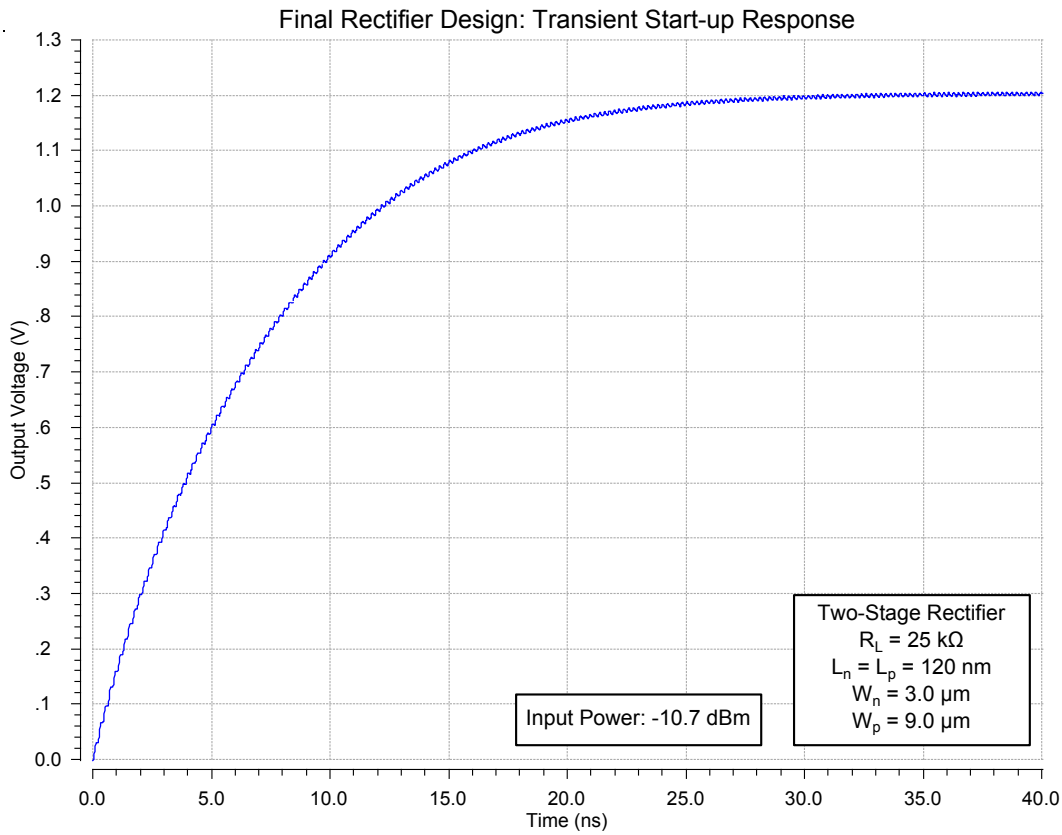


**Figure 4.10:** Transient simulation results of the final two-stage rectifier with 25 kΩ load impedance. The output voltage of the rectifier is plotted with respect to time.

### Performance Results Over Process Corners

To evaluate the performance of the design under the influence of process, voltage, and temperature (PVT) variations, the DVC rectifier was simulated over several process corners. A summary of these results is presented in Table 4.19. These process corners represent the worst-case PVT variations that may occur due to IC manufacturing, and are denoted by two letters, which refer to the relative 'speed' of the NFET and PFET transistors, respectively. The letters *t*, *s*, and *f* denote typical, slow, and

fast speeds, respectively [73]. To establish worst-case corners, the operating temperature was also varied in order to maximize performance variation; the rectifier design was evaluated over a temperature range of $-40°$ C to $100°$ C.

In addition to conventional corners, the rectifier's performance was also evaluated over absolute worst-case "functional corners," denoted by *ssf* and *fff*, which provide an estimate of PVT variations over $\pm 3\,\sigma$ (standard deviations) [73]. As demonstrated in Table 4.19, the rectifier's performance over these corners exhibits only a minor performance degradation in relation to the extreme PVT variations that the design is subjected to. Although not shown in the table, process corners *sf* and *fs* were also tested in order to evaluate the effect of NMOS and PMOS device mismatch; these corners produced similar results to those shown in Table 4.19.

Finally, it should be noted that the process corners in Table 4.19 are intended primarily for digital circuits; therefore, their applicability to analog systems is limited [73]. Exhaustive testing should include a Monte Carlo analysis. However, from these findings, it may still be concluded that PVT variations do not significantly alter the operation of the DVC rectifier.

**Table 4.19:** Summary of the final two-stage rectifier's performance at the point of peak PCE operation over various process corners.

| **Temperature** | **Process Corner** | **Input Power** | **DC Output Voltage** | **PCE** |
|---|---|---|---|---|
| 27° C | TT | -12.07 dBm | 1.04 V | 70.16 % |
| −40° C | FF | -12.09 dBm | 1.07 V | 74.28 % |
| 100° C | SS | -11.69 dBm | 1.05 V | 65.01 % |
| −40° C | FFF | -12.37 dBm | 1.04 V | 74.04 % |
| 100° C | SSF | -11.12 dBm | 1.12 V | 64.37 % |

### 4.2.5 Circuit Layout & Extraction

In this section, the physical layout of the rectifier IC is presented, including a discussion of post-extraction simulation results.

#### Physical Layout

After the performance of the rectifier was confirmed via simulation, a physical layout of the two-stage DVC rectifier IC was developed. The final layout of the entire IC is shown in Figure 4.11 (with metal fill removed for clarity). The IC is implemented in the IBM 0.13 $\mu$m CMOS process and measures 1 $\times$ 1 mm in size.

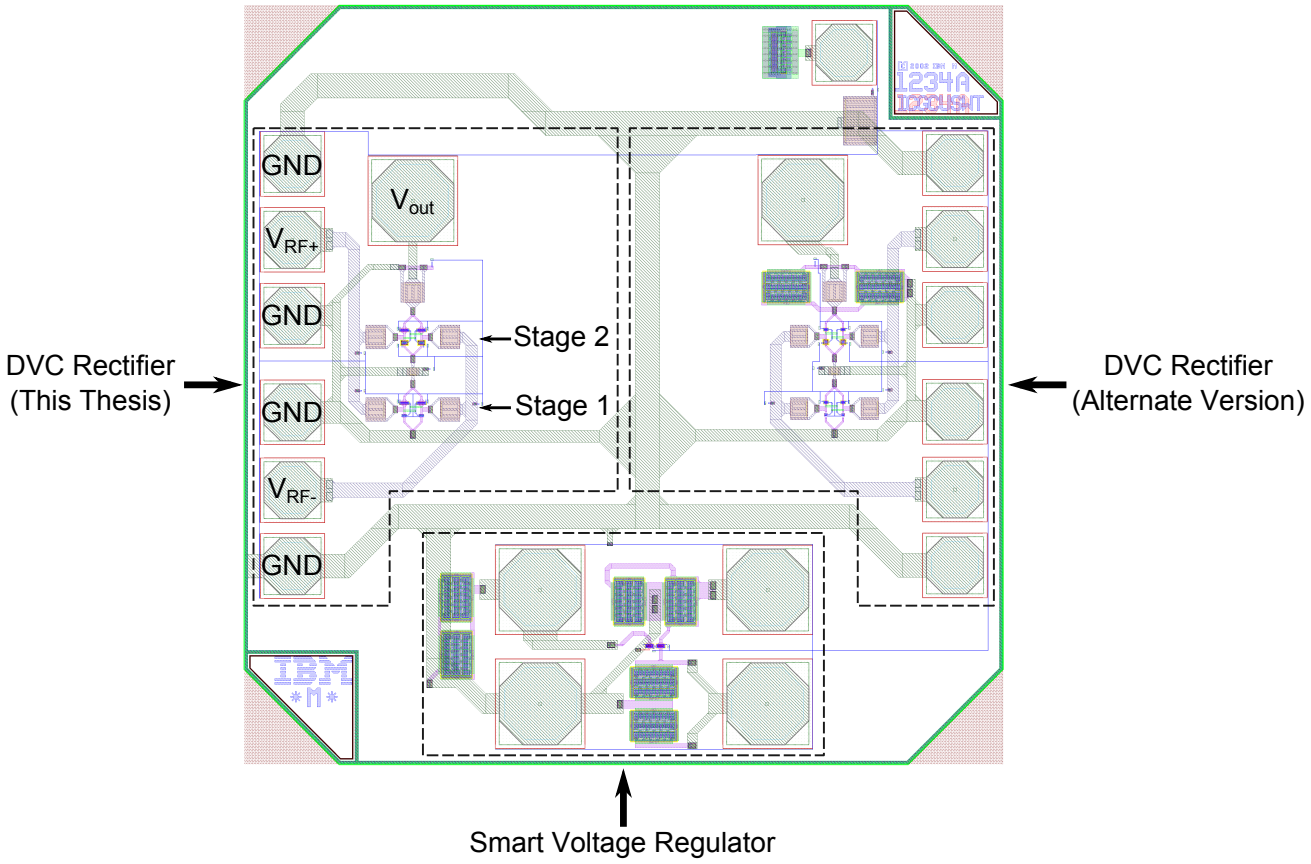


**Figure 4.11:** Physical IC layout of the final rectifier design (with metal fill removed).

The DVC rectifier presented in this thesis comprises the left-half of the IC layout and is shown in the figure with annotations. The right-half and bottom portions of the IC layout correspond to an alternate version of the DVC rectifier and an SVR voltage regulator, respectively. These additional circuits are not part of the design under consideration and therefore are not discussed in this work.

As shown in Figure 4.11, the rectifier's input bond pads consist of a GSG-GSG (dual ground-signal-ground) configuration; this arrangement was specifically chosen so that the rectifier could be directly tested using differential RF probes. The output node, meanwhile, consists of a single DC bond pad. A summary of bond pad sizes is provided in Table 4.17. It should also be noted that the load resistor, $R_L$, is to be implemented off-chip (*e.g.* using a potentiometer), so that the rectifier may be evaluated over a range of load impedance values.

**Rectifier Layout**

An enlarged view of the physical layout of the DVC rectifier is presented in Figure 4.12 with annotations. In the design of the layout, geometrical symmetry is of paramount importance, in order to reduce current mismatch between the rectifier's lower and upper circuit branches. Both stages of the rectifier are identical, with the exception that the second stage employs triple-well NMOS transistors. An intermediate capacitor, $C_{int}$, connects these stages together. The total approximate size of the DVC rectifier layout, including bond pads, is $295 \times 616$ $\mu$m; excluding bond pads, the total size is $177 \times 240$ $\mu$m.

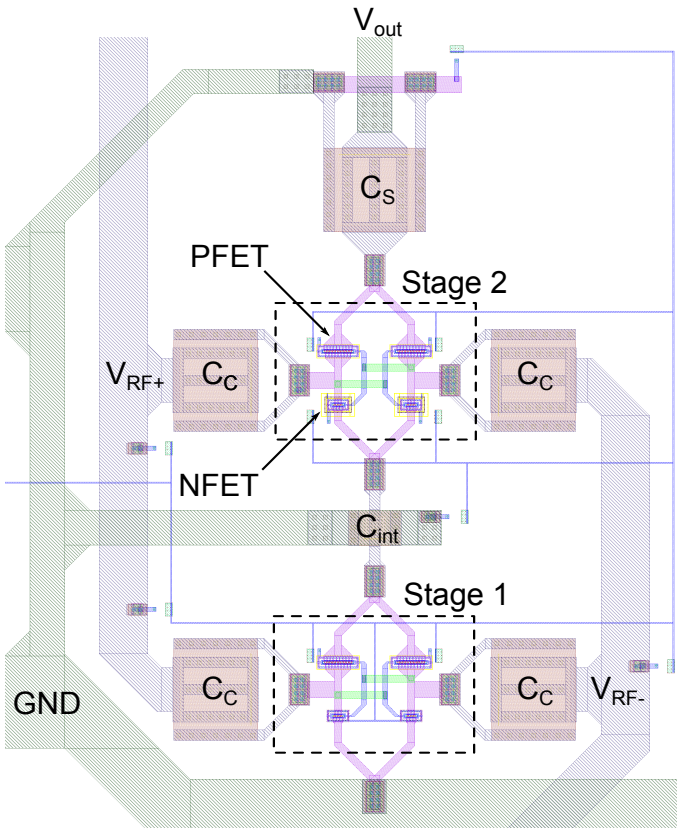


**Figure 4.12:** Physical IC layout of the final rectifier design (with metal fill removed).

### Post-Extraction Simulation Results

To conclude the design procedure, the physical layout of the rectifier must be validated. This may be accomplished by performing a parasitic RC extraction on the layout. Post-extraction simulation results of the DVC rectifier are shown in Figure 4.13. Compared to pre-extraction simulation data, it is observed that peak PCE is reduced from 70.16% to 69.63%. Similarly, at an output voltage of 1.2 V, peak PCE is diminished by 0.36%, to 68.12%. From these results, it may be concluded that the operation of the DVC rectifier does not vary significantly when parasitic RC elements are accounted for.

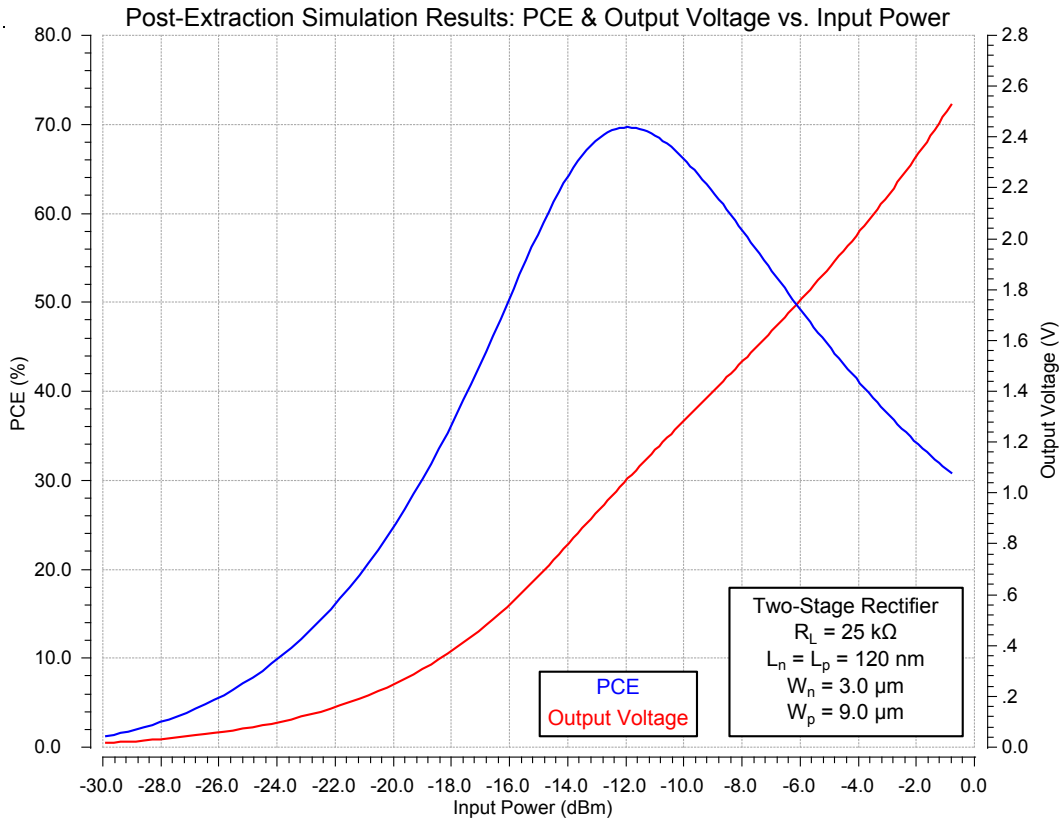


**Figure 4.13:** Post-extraction performance results of the final two-stage rectifier with 25 kΩ load impedance. The PCE and output voltage ($V_{out}$) are plotted with respect to input power.

### 4.2.6 Discussion of Design and Simulation Results

This section offers a brief discussion of several aspects related to the design and simulation of the DVC rectifier.

#### Impedance Matching

As noted earlier, in RF EH systems the rectifier stage is typically preceded by an impedance matching network, which ensures that the maximum available power is transferred from the antenna to the rectifier. During the design of the DVC rectifier, an ideal (*i.e.* lossless) matching network was assumed, so that the rectifier could be

studied independently of other sub-blocks in the RF EH module. This approach is consistent with EH literature that focuses on the design of rectifiers [81].

During the simulation of the rectifier, the balanced impedance of the RF input source was set to 100 Ω, or 50 Ω per input terminal. To account for impedance mismatch, the simulation results were presented with respect to the *actual* power delivered to the rectifier (unless explicitly stated otherwise). However, a practical matching network contains inherent resistive loss and will not be perfectly matched to the antenna and rectifier. Furthermore, in [122] it was demonstrated that, even when a large-signal impedance match is performed, the maximum power transfer from the antenna to the rectifier is theoretically limited to a maximum of 92% for a sinusoidal source. In conclusion, additional power loss due to the matching network must be considered during the design of the proposed RF EH module, though it was neglected for the independent study of the DVC rectifier in this section.

**Influence of IC Process on Rectifier Operation**

The choice of IC process will affect the operation and performance of the DVC rectifier in several notable ways. For instance, newer CMOS processes generally feature transistors with smaller gate lengths and thinner oxide thicknesses. Consequently, these transistors exhibit lower on-resistance and possess a smaller threshold voltage compared to transistors which are fabricated in older CMOS processes. Recall that the DVC rectifier does not begin to function until the input voltage is larger than the transistor threshold voltage. Thus, the sensitivity of the rectifier – that is, the minimum input voltage required for the rectifier to operate – will be improved if a newer CMOS process with a smaller minimum gate length is employed [122].

The effect of IC process on PCE, however, is not as apparent. Although transistors fabricated in IC processes which feature smaller gate lengths exhibit lower on-resistance, which improves PCE, they also possess a larger reverse leakage current, which degrades PCE. Therefore, the choice of IC technology involves a trade-off similar to the one discussed earlier regarding low-$V_t$ transistors in the IBM 0.13 $\mu$m CMOS process [81].

In addition, the ratio of electron to hole mobility for a given IC process will affect the transistor scaling parameter, $g^2$. This term represents one of the three PCE optimization parameters, and is the parameter employed during transistor scaling to maintain a constant PCE [122].

**Literature Comparison**

The performance of the DVC rectifier is summarized in Table 4.20, and is compared to the results of the literature which has been cited in this chapter. It should be noted that the PCE corresponding to [122] refers to the overall power efficiency obtained from the antenna to the output of the rectifier. From this summary, it may be concluded that the results of the DVC rectifier compare favorably to the noted works presented in literature. In addition, it is important to observe that the rectifier presented in this thesis operates at an input frequency which is more than 2.5 times higher than [81, 122], while achieving comparable efficiency.

**Table 4.20:** Comparison of the simulation results obtained for the rectifier presented in this thesis to those from designs which have been cited in this chapter. In [122], the value for PCE refers to the end-to-end power efficiency from the antenna to the output of the rectifier, while the value for input power refers to the available power from the antenna.

| | **This Work** | **[81]** | **[122]** |
|---|---|---|---|
| **Characterization** | Simulation | Experimental | Simulation |
| **CMOS Technology** | 0.13 $\mu$m | 0.18 $\mu$m | 90 nm |
| **Number of Rectifier Stages** | 2 | 1 | 3 |
| **Frequency (MHz)** | 2,450 | 953 | 915 |
| **Input Power (dBm)** | -12.1 | -12.5 | -13.5 |
| **Load Impedance (k$\Omega$)** | 25 | 10 | 29.6 |
| **PCE (%)** | 70.2 | 67.5 | 74.3 |
| **Output Voltage** | 1.04 | 0.62 | 0.99 |

## 4.3 Summary

In this chapter, two designs related to the wireless X-ray dosimeter were presented. First, a preliminary system-level design of the RF energy harvesting (EH) module was demonstrated. The proposed RF EH module is comprised of the following sub-blocks: a half-wavelength dipole antenna, impedance matching network, voltage limiter, high-efficiency Dynamic $V_{th}$ Cancellation (DVC) rectifier, Smart Voltage Regulator (SVR), and energy storage capacitor. A discussion of each sub-block was provided, including a summary of system-level specifications. In addition, it was explained that the antenna, matching network, and energy storage capacitor would be implemented off-chip, while the remaining sub-blocks were to be integrated into a single IC and fabricated in the IBM 0.13 $\mu$m CMOS process.

Second, the design and simulation of a two-stage DVC rectifier which operates at 2.45 GHz was presented. In this section, a discussion of the rectifier's target specifications, theory of operation, and optimization procedure was provided. It was noted that the transistor scaling technique from [122] would be employed to obtain maximum power conversion efficiency (PCE) for the desired load impedance of 25 k$\Omega$. After several iterations, a multi-stage rectifier architecture was developed which met all of the target performance specifications. The final two-stage DVC rectifier was demonstrated to achieve a PCE of 70.2% and a nominal output voltage of 1.04 V at an input power level of -12.1 dBm. These results compare favorably to those found in EH literature [81, 122]. The design was also validated across various process and temperature corners. Finally, a physical layout of the rectifier IC was developed and implemented in the aforementioned IBM 0.13 $\mu$m CMOS process. The entire IC measures $1 \times 1$ mm in size. Post-extraction simulation results indicate that the rectifier's performance does not vary significantly when parasitic elements are considered. In conclusion, a two-stage DVC rectifier which meets all of the target specifications of the proposed RF EH module was successfully designed and simulated.

# Chapter 5

# RF Rectifier Experimental Results

In this chapter, the experimental results of the RF rectifier which was designed and simulated in Chapter 4 are presented. First, an overview of the experimental testing procedure is provided, including a description of the laboratory test bench. Second, the experimental results of the RF rectifier are presented. These results are based on conservative assumptions for estimating the power loss due to each component in the test bench. Next, an alternative approach for modeling the power loss of the testing equipment is demonstrated. Finally, the results of the RF rectifier are presented again, based on the second technique for characterizing the power loss.

## 5.1 Testing Methodology

This section describes the laboratory test bench and experimental procedure for measuring the RF rectifier. In addition, a photomicrograph of the IC is provided.

### Device Fabrication

A photomicrograph of the rectifier IC is shown in Figure 5.1. The RF rectifier under consideration is located in the left-half portion of the die (refer to Figure 4.11).

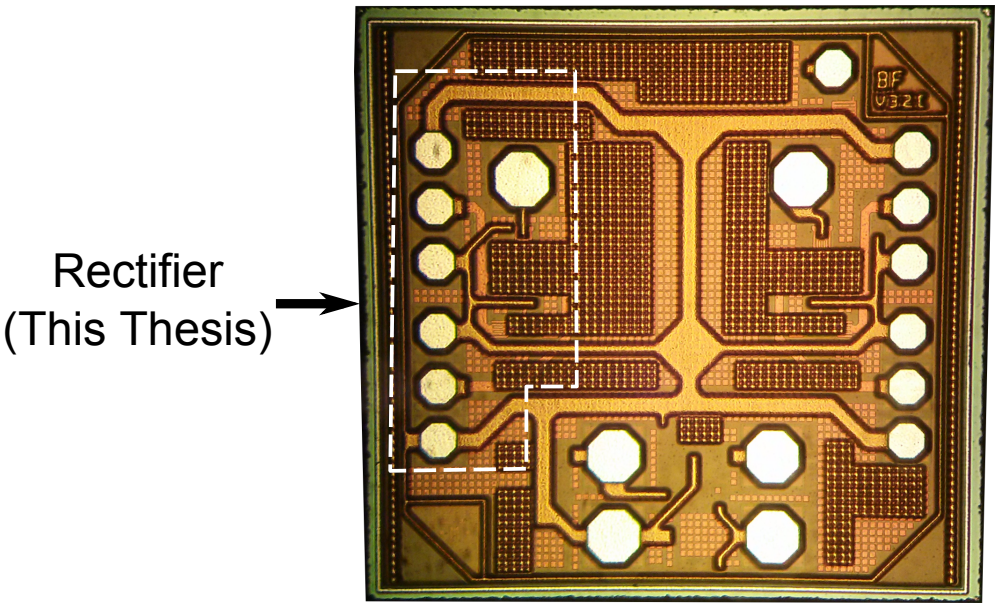


**Figure 5.1:** Photomicrograph of the rectifier IC, which was fabricated using the IBM 0.13 $\mu$m CMOS process. The rectifier under consideration is depicted in the left-half portion of the IC and is outlined in white.

### Laboratory Test Bench

To characterize the performance of the rectifier, also referred to as the "device under test" (DUT), the configuration shown in Figure 5.2 was employed.

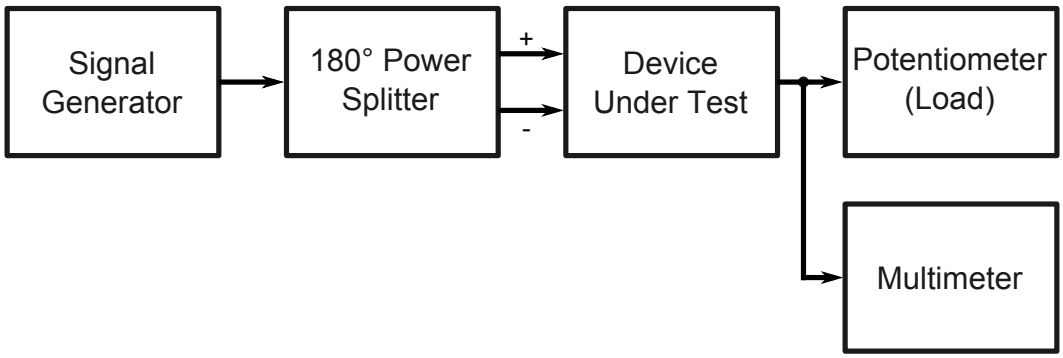


**Figure 5.2:** A diagram of the laboratory test bench which was employed to measure the performance of the RF rectifier. The SMA (SubMiniature version A) cables and differential RF probes, which connect the power splitter to the DUT, are not shown.

As illustrated in the diagram, a 180° two-way power splitter is used to convert the single-ended output of the signal generator to a differential stimulus, which may then be fed to the DUT. The power splitter is rated for operation over 1.0–2.0 GHz, provides excellent amplitude and phase unbalance characteristics, and exhibits a maximum insertion loss of 1.8 dB at either output terminal (excluding the 3 dB of loss incurred due to splitting the input signal) [123]. Although not shown in the figure, the power splitter is connected to a pair of differential RF GSG-GSG probes, which serve as an interface to the DUT [124]. The DC output voltage of the DUT is measured using a multimeter, while the output load is implemented using a potentiometer mounted in a discrete through-hole package, which enables the load impedance to be adjusted over a range of values.

A photograph of the test bench is shown in Figure 5.3(a). This picture illustrates the IC probing station and laboratory instruments that were employed to measure the performance of the rectifier. A close-up image depicting the aforementioned differential RF and DC probes landed on to the rectifier IC's bond pads is shown in Figure 5.3(b). The ICs were mounted on to a glass slide for testing purposes. This was accomplished using a hot plate and black wax. A glass slide was placed on the hot plate, which was heated to a temperature above the melting point of the wax (approximately 100° C). A small dab of wax was applied to the glass slide and an IC die was carefully lowered on to the wax. This approach is favoured over those which use epoxy or glue for adhesion primarily for two reasons. First, ICs may be easily removed or re-seated simply by applying heat and acetone. Secondly, this approach ensures that the IC will be level with respect to the glass slide which it is mounted to, as the IC will 'sink' into place within the heated wax.

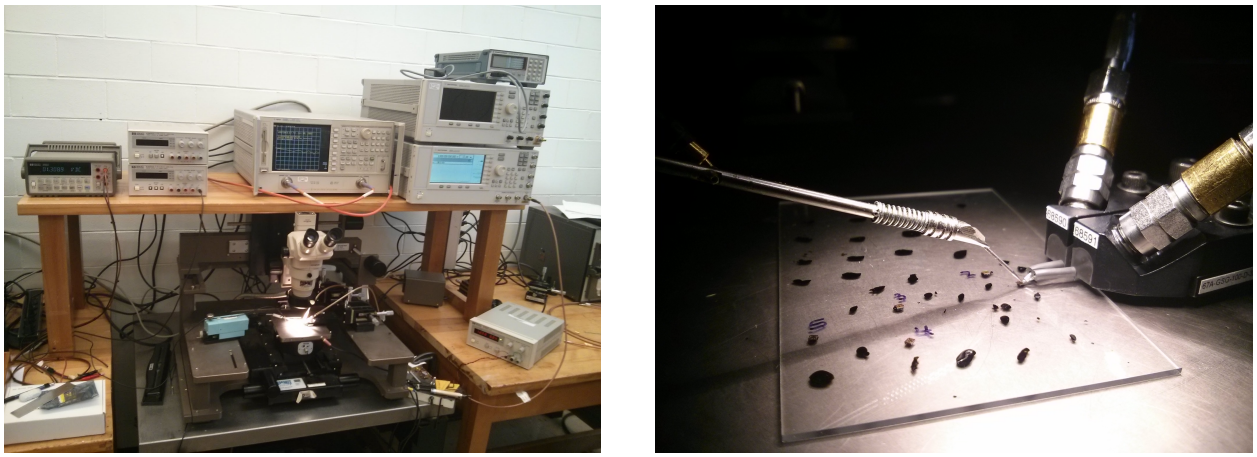


**Figure 5.3:** (a) Photograph of the laboratory test bench used to characterize the rectifier. (b) Close-up photograph of the differential RF probes and DC probe landed on top of the input and output bond pads, respectively.

### Testing Procedure Outline

From the test bench shown in Figure 5.2, the performance of the rectifier was measured using the following procedure:

1. The potentiometer is adjusted to the desired impedance using a multimeter.

2. The signal generator is calibrated to provide the desired power level to the input of the splitter (*i.e.* to the end of the SMA cable). Automatic Levelling Control (ALC) is disabled to prevent the signal generator from maintaining the power level when the DUT (which is not matched) is connected. The frequency is set to the desired value.

3. The test bench illustrated in Figure 5.2 is configured.

4. For each input power level, the output voltage which is measured by the multimeter is recorded. The DC output power is calculated as follows: $P_{out} = {V_{out}}^2/R_{Load}$.

This procedure was repeated for all input frequencies, power levels, and output impedance values of interest. In addition, the insertion loss of the power splitter and the attenuation of the SMA cables connecting the splitter to the DUT were measured. The results are summarized in Table 5.1. As expected, it was observed that the insertion loss of the splitter is much larger when the device is operating outside of its specified frequency range.

**Table 5.1:** Summary of power loss due to laboratory equipment employed by the test bench shown in Figure 5.2. All losses were measured using a power meter, with the exception of the RF probes, where the loss was estimated from the supplied datasheet. Side 1 and 2 refer to the paths which are connected to the positive and negative input terminals of the rectifier, respectively. The reported insertion loss of the splitter includes the 3 dB drop due to the splitting of the signal.

| **Power Loss (dB)** | **1.0 GHz** | **2.0 GHz** | **2.45 GHz** |
|---|---|---|---|
| SMA cable | 0.3 | 0.4 | 0.4 |
| RF probe | 0.2 | 0.2 | 0.2 |
| Splitter port 1 | 3.6 | 4.1 | 6.1 |
| Splitter port 2 | 4.0 | 4.2 | 6.2 |
| **Total, side 1** | **4.1** | **4.7** | **6.7** |
| **Total, side 2** | **4.5** | **4.8** | **6.8** |

Additional testing was also performed to measure the impedance mismatch due to the rectifier. S-parameter measurements were taken at both the input of the DUT and the input of the power splitter using a vector network analyzer (VNA). However, in the former case, since conventional S-parameter measurements apply a stimulus to only one port at a time, the rectifier is not excited differentially, and thus will not operate as expected. For this reason, in conjunction with the highly non-linear nature of the rectifier, these S-parameter measurements will not be accurate. Therefore, the

one-port S-parameter measurements taken at the input of the power splitter must be relied upon. Unfortunately, doing so results in the plane of reference being shifted further away from the DUT. Additional discussion of this topic is provided throughout the following sections.

## 5.2 Experimental Measurements

This section presents the measured results of the rectifier IC using the testing procedure outlined in the previous section. The results are presented using two separate approaches for determining the input power delivered to the DUT.

### 5.2.1 Rectifier Performance

The performance of the rectifier is characterized by its DC output voltage and PCE for a given input power level. While the output voltage is straightforward to measure, the input power, and hence the PCE, is considerably more difficult. To compute PCE, the input power delivered to the rectifier must be determined. One technique involves calculating the input power of the splitter, $P_{in,\,splitter}$, from the indicated power of the signal generator (into a matched load), $P_{SG}$, and the reflection coefficient, $S_{11}$, as follows [81]:

$$\mathrm{P_{in,\,splitter}} \;=\; \mathrm{P_{SG}} \cdot \left(1 - |\mathrm{S_{11}}|\right)^2 \tag{5.1}$$

The reflection coefficient was measured experimentally at the input of the splitter using a VNA. The S-parameter data were measured over a frequency range of 1.5–2.5 GHz and an applied input power of 0 dBm (as reported by the VNA). However, at the plane of reference, the actual power level was measured to be -0.5 dBm. The DUT,

meanwhile, was connected to a load impedance of 25 kΩ. In addition to experimental data, the reflection coefficient at the input of the splitter was also simulated using SpectreRF (for further details of the simulation setup, refer to Section 5.2.2). The experimental and simulated results are shown in Figure 5.4.

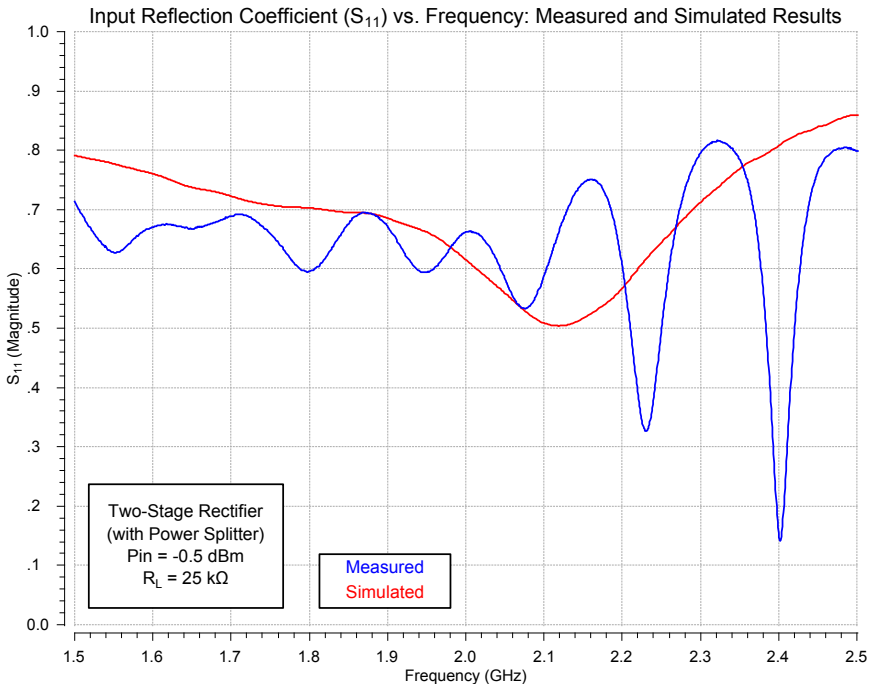


**Figure 5.4:** Experimental and simulated results of the reflection coefficient, $S_{11}$, at the input of the splitter over a frequency range of 1.5–2.5 GHz.

From Figure 5.4, a resonance phenomenon, having a periodicity of approximately 160 MHz, is observed in the experimental results. This pattern does not constitute expected behaviour of the system, and therefore should be regarded as noise. The source of this phenomenon may be due to a VNA calibration error (due to power sweeping), or perhaps from the differential RF probes, which could not be calibrated directly due to the lack of a suitable calibration substrate. However, with the exception of the resonance behaviour, the experimental results are similar to the simulation data. Therefore, simulated values of $S_{11}$ may be used to determine the incident power at

the input of the splitter; this ensures that the demonstrated results are not influenced by the undesired resonance phenomenon.

Next, from the actual input power of the splitter, the power at the input of the DUT may be estimated by subtracting the power losses due to the splitter, SMA cables, and probes, which are provided in Table 5.1. The performance of the rectifier when this approach is employed is presented in Figure 5.5.

By examining these performance results, several observations may be noted. First, in each result, the output voltage increases linearly with input power (in dBm); this behaviour is consistent with the simulation results presented in Chapter 4 and serves as confirmation that the rectifier IC is functioning properly. Second, the measured performance over different ICs is quite similar. This result is to be expected, due to the rectifier's high tolerance to PVT variations observed during simulation.

In addition, the graphs from Figure 5.5 demonstrate that maximum PCE is achieved for a load impedance of 10 kΩ and a frequency of 1 GHz, despite the fact that the rectifier was specifically designed for a load impedance of 25 kΩ and a frequency of 2.45 GHz. The observed influence of operating frequency on PCE is similar to the results presented in [81], which demonstrates an inverse relationship between PCE and frequency of operation. However, the shift in maximum PCE to a different load impedance than the one for which the design was optimized for may be attributed to the inherent limitations of the approach that was used to determine the input power of the rectifier. This assertion is argued in greater detail in the following section.

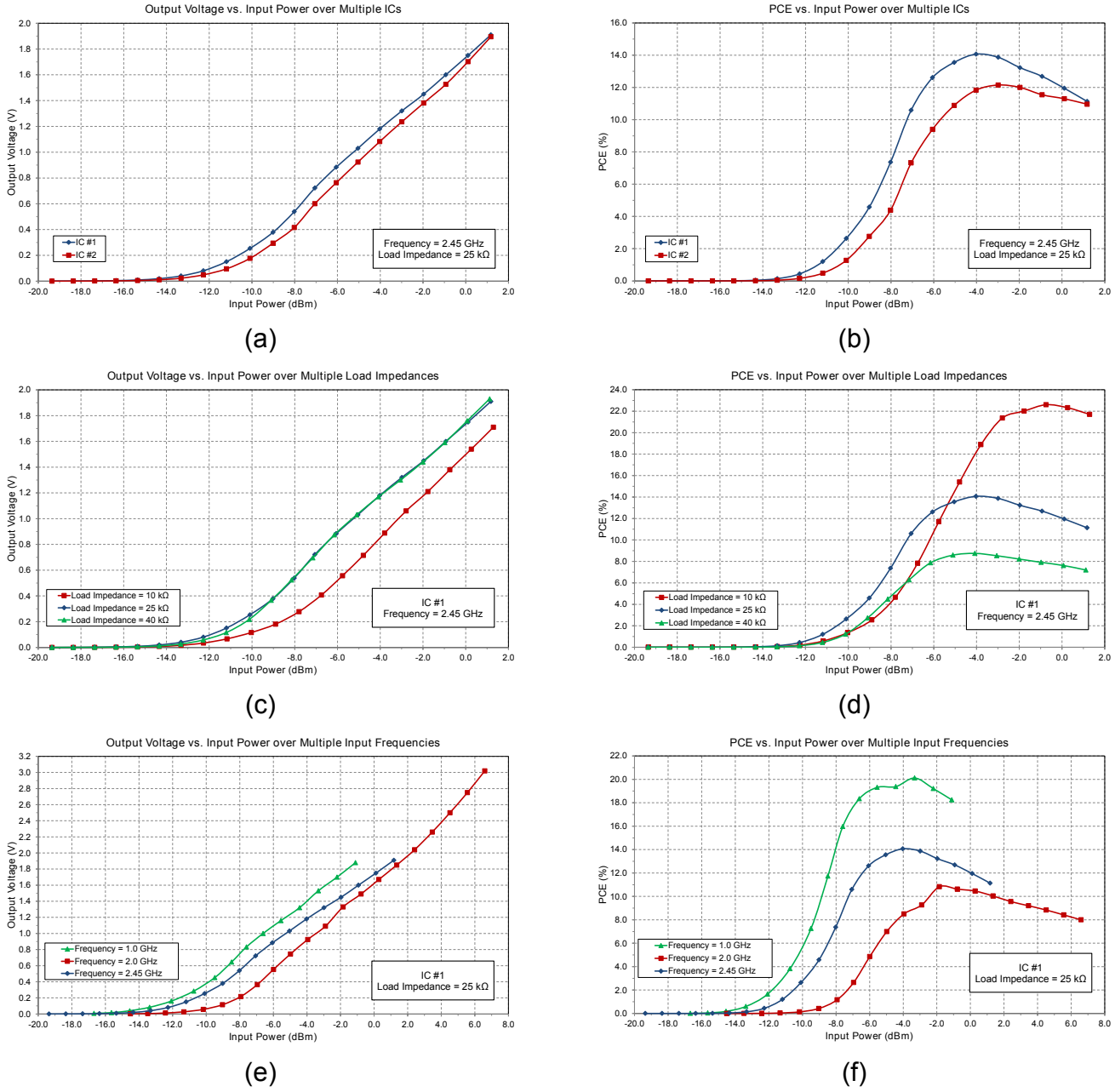


**Figure 5.5:** Experimental results of the rectifier IC. The output voltage and PCE were measured over several parameters, including: ICs ((a) & (b)), load impedance ((c) & (d)), and input frequency ((e) & (f)).

Finally, it is also observed that the achievable PCE over all operating conditions is considerably lower than expected. During simulation, the rectifier was found to achieve a peak PCE of approximately 70.2% at an input power of -12.1 dBm and a frequency of 2.45 GHz. However, the experimental results indicate that a maximum PCE of only 22.6% is achieved at an input power of -0.7 dBm for a load impedance of 10 kΩ and an input frequency of 2.45 GHz. Again, this is likely due to the approach which was used to determine the input power of the rectifier. Therefore, an alternate approach should be evaluated in order to verify whether more accurate performance results may be obtained.

### 5.2.2 Power Splitter Characterization

The 180° two-way power splitter that was employed during experimental testing of the rectifier exhibits complex behaviour which cannot be characterized solely by its input reflection coefficient (*i.e.* $S_{11}$). To better understand its behaviour, the power splitter was simulated using a simple three-port test bench in Cadence and SpectreRF. The splitter was modeled using the three-port S-parameter (Touchstone) file provided by the manufacturer.

First, a large-signal PSS simulation was conducted to assess the insertion loss of the splitter when all ports are matched to 50 Ω. Under this condition, the insertion loss was roughly consistent with the measured results provided in Table 5.1. However, when the splitter's output ports were terminated with an impedance of 950 Ω and 2 kΩ, respectively, the insertion loss increased significantly. The results of this simulation are presented in Table 5.2.

**Table 5.2:** Summary of the power splitter's simulated performance at 2.45 GHz when the output terminals are terminated with an impedance of 950 Ω and 2 kΩ, respectively.

| **Attribute** | **Value** |
|---|---|
| Input power (specified) | 0 dBm (1 mW) |
| $S_{11}$ | -1.61 dB (0.831) |
| Input power (actual) | -5.09 dBm (309.7 $\mu$W) |
| Output power, port 1 | -16.00 dBm (25.1 $\mu$W) |
| Output power, port 2 | -19.74 dBm (10.6 $\mu$W) |
| Total output power | -14.48 dBm (35.7 $\mu$W) |

From Table 5.2, the actual input power of the splitter may be determined from the value of $S_{11}$ and Equation 5.1. However, this result indicates the power loss due to mismatch between the input port and the splitter only. As seen in the table, the power at either output port is significantly lower than the input power. This is to be expected, due to the impedance mismatch which exists between each splitter output terminal and its respective load. Furthermore, asymmetrical impedance loading between the output ports may contribute to additional loss.

Similar results were obtained when the splitter was simulated within the rectifier test bench. When an input power of 0 dBm is specified, the power incident to the splitter's input terminal is -4.3 dBm, while the power at the output terminals is $-19.5$ dBm and $-21.6$ dBm, respectively. These results are similar to those obtained using the splitter test bench (*i.e.* Table 5.2). It may therefore be concluded that the approach employed in Section 5.2.1 to determine the input power of the rectifier overestimates the actual power delivered to the DUT, and therefore represents a conservative estimation of the rectifier's performance.

### 5.2.3 Rectifier Performance: Splitter Model Approach

In this section, the experimental results of the rectifier IC will now be presented using the alternate approach outlined in Section 5.2.2 to determine the input power of the rectifier IC. The power splitter is embedded in the rectifier simulation test bench and modeled using the manufacturer's S-parameter file. Simulation data is used to determine the total output power of the splitter, which is assumed to be a valid estimation of the total input power of the rectifier. The experimental performance results when this alternate approach is employed are presented in Figure 5.6.

In contrast to the results presented in Section 5.2.1, the performance results illustrated in Figure 5.6 demonstrate a significant improvement in PCE. At 2.45 GHz and using a load impedance of 25 kΩ, the maximum PCE is 49.7% and occurs at -12.01 dBm. This outcome represents a twofold improvement in maximum PCE at 2.45 GHz. However, it remains notably less than what was achieved in simulation. This discrepancy may be due to differences which exist between the manufacturer's provided model file of the splitter and the actual device which was used. For example, if the power splitter employed during experimental testing exhibits larger amplitude and phase imbalances between its output terminals than what is predicted by the model file, then the efficiency of the rectifier would be adversely affected. In general, any imbalance in the amplitude or phase between the rectifier's input terminals will result in asymmetrical operation, and will therefore exert a negative impact on PCE. In addition, the difference between the experimental and simulated PCE may be due to the aggregate sum of the various sources of measurement uncertainty. A discussion of these sources is provided in Section 5.3.

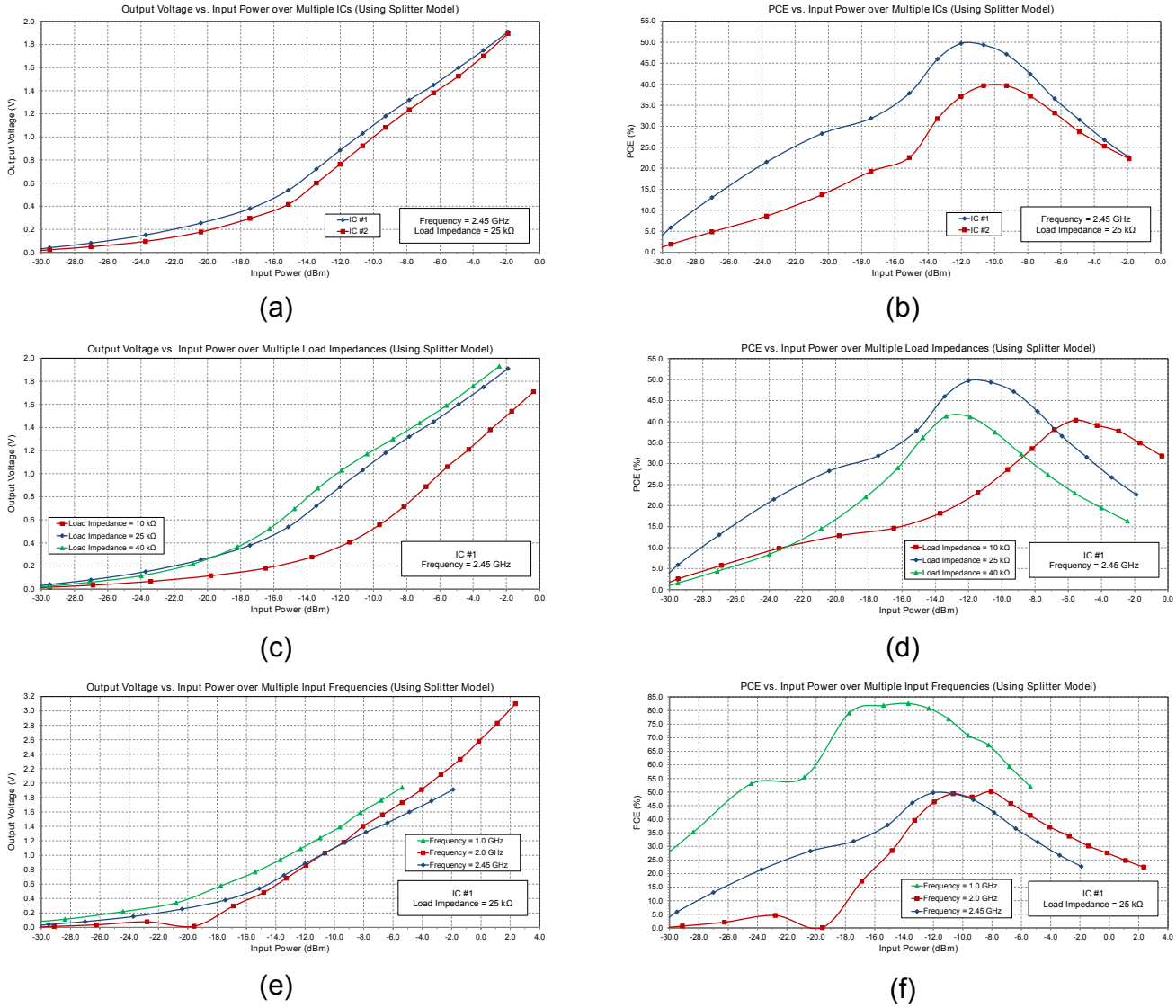


**Figure 5.6:** Alternate experimental results of the rectifier IC. The input power of the rectifier is determined via simulation. The output voltage and PCE were measured over several parameters, including: ICs ((a) & (b)), load impedance ((c) & (d)), and input frequency ((e) & (f)).

When examining the results shown in Figure 5.6(f), it is observed that the peak PCE is approximately 10% larger than what is predicted by simulation. This implies that the alternate approach for determining the input power to the DUT may over-estimate the performance of the rectifier in certain situations. Ultimately, however,

the two approaches demonstrated in this chapter provide the best possible accuracy which may be achieved from the test bench outlined in Section 5.1 and the available laboratory equipment. A test bench which may be used to obtain better measurement accuracy is suggested in Section 5.3.

Lastly, it should be noted that the rectifier could not be simulated over the same range of input power levels at 1 GHz as for other frequencies of interest, due to convergence issues which were encountered in SpectreRF.

## 5.3 Discussion of Experimental Results

This section provides a discussion of several aspects related to the laboratory test bench and experimental results provided in Sections 5.1 and 5.2, respectively.

**Measurement Uncertainty**

As with most experimental test configurations, measurement uncertainty may be introduced into the experimental results from a variety of sources. For the rectifier test bench and procedure described in Section 5.1, measurement uncertainty may arise from the:

- Potentiometer. Setting the potentiometer's impedance requires manual adjustment via a tuning stick, and therefore may not be set exactly to the desired value.

- Output voltage. Small voltage fluctuations occur due to a minor ripple voltage at the output of the rectifier. When the output voltage was measured with a multimeter, attempts were made to record the nominal DC voltage. However, for smaller output voltages, the ripple is more pronounced.

- Quality of contact made between the IC probes and bond pads. Whenever the probes are landed on to the bond pads, a different degree of physical contact is made. In some cases, this contact may be poor and lead to power loss. This was particularly evident when landing the DC probe on the output bond pad.

- Signal Generator. Prior to measuring the DUT, the output power of the signal generator was calibrated to provide the desired power levels at the end of the connected SMA cable, which represents the input to the splitter. However, the output power of the signal generator varies slightly over time as the device temperature changes. These variations are exacerbated by disabling ALC, which was done for reasons explained in Section 5.1.

Any one or a combination of these sources of uncertainty may result in reduced accuracy of the rectifier's measured performance.

**An Improved Laboratory Test Bench**

As explained earlier, RF rectifiers are typically characterized by examining the actual power delivered to the input of the rectifier, irrespective of any impedance mismatch which might exist [81]. In Section 5.2, two approaches for determining the rectifier's input power were described. Both of these methods rely on the test bench described in Section 5.1. To eliminate the dependence of experimental results on simulation data, an improved test bench may be employed. This test bench would consist of a microwave circulator and power meter attached to each output terminal of the power splitter. The quantity of power which is reflected due to the rectifier's unmatched input terminals may be measured by the power meters, and subtracted from the input power of the splitter. This approach is similar to the test configuration which was employed in [125].

### Literature Comparison

A summary of the RF rectifier's measured performance using the alternate approach for determining input power is presented in Table 5.3, in addition to similar RF rectifiers which are reported in EH literature.

**Table 5.3:** Comparison of the measured results obtained from the rectifier IC presented in this thesis to those from designs which have been reported in EH literature. Note that some results are based on simulation (denoted by "Sim."), while others were obtained experimentally (denoted by "Exp."). The results from this work are classified as experimental results with corrections ("Corr."), due to the manner in which the RF input power of the rectifier was determined (refer to Section 5.2.2 and 5.2.3).

| | **This Work** | **[81]** | **[126]** | **[127]** | **[128]** |
|---|---|---|---|---|---|
| **Year** | 2014 | 2009 | 2010 | 2012 | 2014 |
| **Results** | Exp. (Corr.) | Exp. | Sim. | Sim. | Exp. |
| **CMOS Technology** | 0.13 $\mu$m | 0.18 $\mu$m | 90 nm | 0.13 $\mu$m | 0.18 $\mu$m |
| **Frequency (MHz)** | 2,450 | 953 | 2,450 | 2,400 | 2,400 |
| **Input Power (dBm)** | -12.0 | -12.5 | -19.7 | -22.3 | 8.9 |
| **Load Impedance (k$\Omega$)** | 25 | 10 | 1,000 | 400 | 2 |
| **PCE (%)** | 49.7 | 67.5 | 14.7 | 61.0 | 47.0 |
| **Output Voltage** | 0.88 | 0.62 | 1.25 | 1.20 | 2.70 |

Each of the designs in Table 5.3 consist of a DVC rectifier or similar variant. The original DVC rectifier, presented in [81], achieves the highest PCE among the cited works, although at a much lower frequency. Simulation results of a modified DVC rectifier are presented in [126]; in this design, the original DVC rectifier is augmented with so-called "pseudo floating-gate" transistors, which are used to provide enhanced gate biasing for the transistors of the DVC rectifier cell. Although this design operates at a very low input power, the reported PCE is also comparatively low.

In [127], a comparison of Dickson Charge Pump (DCP) and DVC rectifiers was performed in simulation using a 0.13 $\mu$m CMOS process. The results of the DVC rectifier demonstrate that large PCE at a high input frequency is possible. However, the results were not verified experimentally. Lastly, in [128], a modified architecture was presented, which is comprised of two DVC rectifiers and a control circuit which maximizes the combined operation of both rectifiers. This design features a high measured PCE and output voltage. By contrast, the rectifier presented in this work offers a slightly higher PCE, and achieves efficient operation at a much lower input power (-12.0 dBm vs. 8.9 dBm). In conclusion, the results presented in this thesis compare favourably to similar contemporary works which are found in EH literature.

## 5.4 Summary

This chapter presented the experimental results of the RF rectifier that was designed and simulated in Chapter 4. First, the laboratory test bench and methodology which was used to characterize the rectifier IC was detailed. Second, the experimental results of the rectifier were presented. The results were initially determined using a conservative estimate for the power loss due to the test bench. These results confirmed that the rectifier was functioning, although the PCE was much lower than expected. It was then demonstrated that the power splitter generates more loss than what was originally predicted. Consequently, an alternate approach was presented, which employs simulations to determine the rectifier's input power. From this approach, the rectifier is reported to achieve a maximum PCE of 49.7% and an output voltage of 0.88 V for an input frequency of 2.45 GHz, an input power of -12.0 dBm, and an output loading of 25 k$\Omega$. Lastly, in the final section it was shown that the results from this work compare favourably to similar RF rectifiers cited in EH literature.

# Chapter 6

# Conclusions and Recommendations

## 6.1 Summary

In this thesis, an investigation of high-efficiency RF rectifiers for energy harvesting (EH) systems was conducted. As part of this study, an RF rectifier and an EH module were designed. These designs are specifically intended for integration within the wireless X-ray dosimeter project which is under development at Carleton University. An overview of this project was provided in Chapter 1.

In Chapter 2, a broad overview of concepts related to wireless dosimetry was presented, which included biomedical concerns related to blood storage and sterilization, in addition to fundamental RFID principles. This chapter also provided further examination of the wireless X-ray dosimeter project. The implementation of the dosimeter system, which is comprised of an RFID-based reader and tag, was outlined. Furthermore, the dosimeter tag's various subsystems were described, and a power and link budget analysis was performed to determine the tag's power requirements, which are required for the design of the EH module.

In Chapter 3, a study of RF EH systems was presented. This involved a comprehensive literature review of RF rectifiers and a preliminary study of voltage regulators. Together, Chapters 2 and 3 constitute an extensive overview of the necessary background theory and analysis for the design of the dosimeter tag's RF rectifier and EH module.

The designs of the aforementioned rectifier and EH module were detailed in Chapter 4. First, a preliminary design of the dosimeter tag's EH module was demonstrated. This included a system-level design and a discussion of the performance specifications and suggested implementation for each sub-block. Second, the design of a high-efficiency Dynamic $V_{th}$ Cancellation (DVC) RF rectifier was presented. This rectifier was designed according to the proposed EH module's specifications and was implemented in the IBM 0.13 $\mu$m CMOS process. The final simulation results indicate that the design achieves a maximum PCE of 70.2% and an output voltage of 1.04 V for an input power of -12.1 dBm, an input frequency of 2.45 GHz, and a load impedance of 25 k$\Omega$. In Chapter 5, the experimental results of the rectifier IC were presented. The design was reported to achieve a maximum PCE of 49.7% and an output voltage of 0.88 V for an input power of -12.0 dBm, an input frequency of 2.45 GHz, and an output loading of 25 k$\Omega$. When compared to similar rectifier designs reported in EH literature, the RF rectifier demonstrated in this thesis provides competitive performance.

## 6.2 Thesis Contributions

This thesis offers several notable contributions to the fields of wireless dosimetry and energy harvesting. In addition, these contributions serve as further development of the wireless X-ray dosimeter project at Carleton University. They include:

1. An investigation regarding the application of CMOS wireless dosimeters to the monitoring and tracking of blood bags, in addition to the measuring of X-ray irradiation during sterilization. From this study, a system-level design of the X-ray dosimeter tag was proposed, including a discussion of key system specifications. A power and link budget analysis was also performed.

2. A system-level design of an RF energy harvesting module for the X-ray dosimeter project. This design includes a dipole antenna, impedance matching network, high-efficiency Dynamic $V_{th}$ Cancellation (DVC) rectifier, Smart Voltage Regulator (SVR), and off-chip energy storage capacitor.

3. The design and optimization of a high-efficiency DVC rectifier. This circuit was implemented in the IBM 0.13 $\mu$m CMOS process and was designed to operate at 2.45 GHz. Experimental results demonstrate that the rectifier achieves a maximum PCE of 49.7% for an input power of -12.0 dBm. These results are among the highest reported in EH literature for microwave UHF rectifiers.

## 6.3 Future work

There exist several opportunities to extend the work presented in this thesis to additional areas of development, including:

**1. Improved Rectifier Characterization:** An improved laboratory test bench such as the one outlined in Section 5.3, which involves microwave circulators and power meters to measure the quantity of reflected power, may be used to evaluate the performance of the rectifier. This test bench would eliminate the need for simulation data to determine the input power of the rectifier, and would result in improved measurement accuracy. In addition, the extra circuitry which was incorporated on to

the rectifier IC (*i.e.* an alternate DVC rectifier design and SVR voltage regulator – refer to Figure 4.11) should be tested.

**2. Rectifier Architecture Enhancements:** Improvements to the DVC rectifier architecture may be investigated. As noted in Chapter 3, contemporary research trends in RF rectifier design have evolved towards the use of multiple efficiency techniques. For example, a hybrid rectifier topology may combine Dynamic $V_{th}$ Cancellation with boot-strapped capacitors or dynamic bulk biasing. Improvements to the performance of the DVC rectifier should focus on: larger maximum PCE, a broader efficiency curve (with respect to input power), and the ability to achieve high PCE over a range of load impedances. Furthermore, applications of the DVC rectifier for ultra-wide band (UWB) operation could be studied.

**3. Energy Harvesting Module Implementation:** A complete design of the proposed RF EH module may be developed from the preliminary system-level specifications which were outlined in Chapter 4. This would involve the design of a PCB consisting of the dipole antenna, matching network, and energy storage capacitor.

**4. SoC Antenna:** A System-on-Chip antenna for the RF EH module described in (3) may be evaluated as a potential approach for the miniaturization of the RF EH module, and consequently, the X-ray dosimeter tag.

**5. Dosimeter Tag Integration:** Upon completion of (3), efforts may be taken to integrate the RF EH module into the wireless X-ray dosimeter tag, which is under development. Once an entire system has been designed and fabricated, the finished RFID tag should be thoroughly tested and characterized.

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# Appendix A

# Analysis of Backscatter Modulation Techniques

In chapter 2, a number of RFID backscattering techniques were discussed. A summary of these techniques was provided in Table 2.2. However, the results were given without proof or analysis. This section elaborates upon these techniques, including a mathematical analysis of each method. The entirety of this appendix is based on [48].

## Equivalent Backscattering Circuit

A simplified equivalent model of an RFID tag employing backscatter modulation is illustrated in Figure A.1. The signal received by the tag antenna is represented by a voltage source, $V_{ant}$, while the equivalent impedance of the tag's IC is represented by $R_{Load}$. The resistor $R_{Rad}$, meanwhile, represents the radiation resistance of the tag antenna. The power dissipated by this resistor models the amount of power that is reflected by the antenna. In backscatter systems, this reflected power is modulated with information by the tag, and transmitted back to the reader during uplink communication. The circuit shown in Figure A.1 is referred to as the reference case, since no modulation is employed.

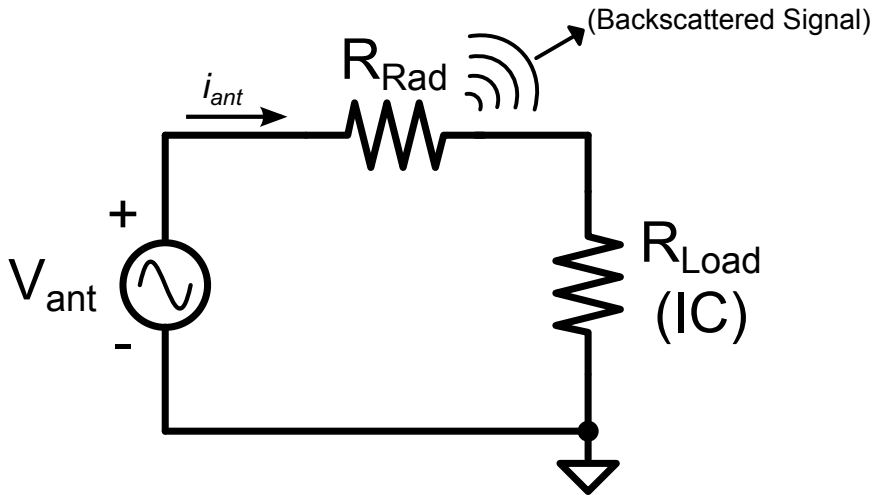


**Figure A.1:** Simplified equivalent circuit of an RFID tag employing backscatter modulation. In this case, no modulation is used. Therefore, this circuit represents the reference case.

The current, $i_{ant}$, flowing through the reference circuit is given by:

$$\mathsf{i_{ant}} = \frac{\mathsf{V_{ant}}}{\mathsf{R_{Rad} + R_{Load}}} \tag{A.1}$$

All power quantities in this appendix will be assumed to be *average powers*. In addition, all voltages and currents are assumed to be sinusoidal waveforms, while all circuits are purely resistive (unless otherwise noted). The relationship between average power, $P_{avg}$, peak voltage, $v_{pk}$, and peak current, $i_{pk}$, is given by:

$$\mathsf{P_{avg}} = \frac{\mathsf{v_{pk} \cdot i_{pk}}}{2} = \frac{\mathsf{v_{pk}}^2}{2\mathsf{R}} = \frac{\mathsf{i_{pk}}^2 \cdot \mathsf{R}}{2} \tag{A.2}$$

In Figure A.1, the power received by the antenna is apportioned between the radiated power (*i.e.* the backscatter link) and the power delivered to the load (*i.e.* the tag's IC). The quantity of power delivered to each element depends upon the relative values of the equivalent resistances. In this simplified model, it is assumed that

both impedances are conjugately matched, such that $R_{Rad} = R_{Load}$. It can be shown that this condition, referred to as the matched condition, results in optimum power transfer. The available power received by the tag antenna when both impedances are conjugately matched, $P_{Rx}$, may be calculated as follows:

$$\mathsf{P_{Rx}} = \frac{1}{2}\frac{\mathsf{V_{ant}}^2}{\mathsf{R_{Total}}} = \frac{1}{2}\frac{\mathsf{V_{ant}}^2}{2\,\mathsf{R_{Rad}}} = \frac{1}{4}\frac{\mathsf{V_{ant}}^2}{\mathsf{R_{Rad}}} \tag{A.3}$$

Consequently, the matched condition implies that the available power will be equally distributed between the backscatter link and IC. The power delivered to each element may be expressed mathematically as follows:

$$\mathsf{P_{Rad}} = \mathsf{P_{Load}} = \frac{1}{2}\,\mathsf{P_{Rx}} = \frac{1}{8}\frac{\mathsf{V_{ant}}^2}{\mathsf{R_{Rad}}} \tag{A.4}$$

## Method 1: Open-Matched Load ASK

Consider the diagram shown in Figure A.2. A switch, *SW*, is placed in series with the load. When the switch is open, no current flows in the circuit, resulting in a negligible amount of reflected power. This is shown mathematically as follows:

$$\mathsf{P_{Rad}} = \frac{1}{2}\,\mathsf{i_{ant}}^2 \cdot \mathsf{R_{Rad}} = \frac{1}{2}\,(0)^2 \cdot \mathsf{R_{Rad}} = 0 \tag{A.5}$$

In reality, practical antennas scatter energy even when connected to an open-circuit load. This is a consequence of the antenna's structural scattering mode. This term does not convey information, and thus does not contribute to the backscattered power. It is assumed that a so-called "minimum-scattering" antenna will be employed, and therefore the effect of structural mode scattering may be assumed to be negligible [51].

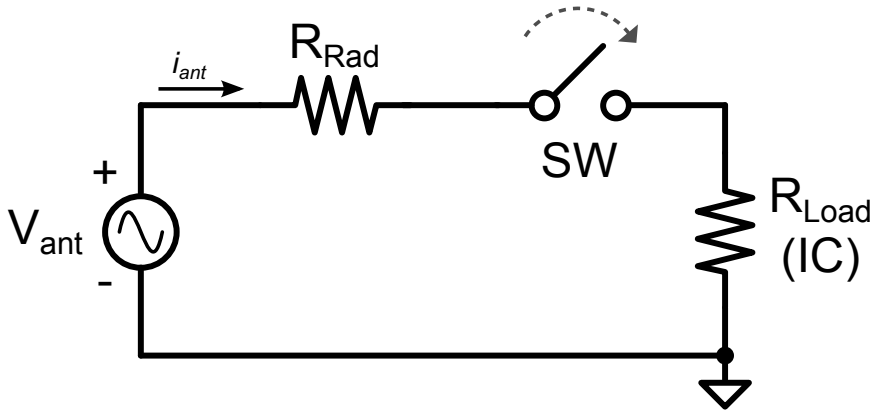


**Figure A.2:** Equivalent circuit for Method 1. A switch, *SW*, varies the impedance seen by the antenna between an open circuit and a conjugately matched load.

Therefore, when the switch is open,

$$\mathsf{P_{Rad}} = \mathsf{P_{Load}} = 0 \tag{A.6}$$

When the switch is closed, a current, $i_{ant}$, flows through the circuit. Since $R_{Rad}$ and $R_{Load}$ are conjugately matched, each element receives half of the available power at the antenna. Hence,

$$\mathsf{P_{Rad}} = \mathsf{P_{Load}} = \frac{1}{2}\,\mathsf{P_{Rx}} \tag{A.7}$$

These results are summarized in Table A.1.

**Table A.1:** Summary of delivered power in Figure A.2 (open-matched load ASK).

| **Switch State** | **Backscattered Power ($\mathbf{P}_{Rad}$)** | **IC Power ($\mathbf{P}_{Load}$)** |
|---|---|---|
| Open | 0 | 0 |
| Closed | 0.5 $\mathrm{P}_{Rx}$ | 0.5 $\mathrm{P}_{Rx}$ |

It is now possible to calculate the average power delivered to each element. It will be assumed that only ASK modulation is used, with no additional encoding of the data. In addition, it will also be assumed that the data to be transmitted contains an equal number of 0's and 1's; hence, the circuit will function in each state for an equal amount of time. Thus, the average power delivered to the IC, $P_{IC}$, is

$$\mathsf{P_{IC}} \;=\; \frac{1}{2}\left(\mathsf{P_{Load,\,SW\,Open}} + \mathsf{P_{Load,\,SW\,Closed}}\right) \;=\; \frac{1}{4}\,\mathsf{P_{Rx}} \tag{A.8}$$

Note that the power delivered to the IC is not constant and depends on which symbol is being transmitted. This is a significant limitation of this modulation technique.

In addition, the average backscattered power, $P_{BSC}$, may be computed from the difference in electrical current between states, as follows:

$$\mathsf{P_{BSC}} \;=\frac{1}{2}\,\Delta\mathsf{i_{ant}}^{2}\,\mathsf{R_{Rad}} \;=\; \frac{1}{2}\,\mathsf{P_{Rx}} \tag{A.9}$$

## Method 2: Short-Matched Load ASK

Next, consider the diagram shown in Figure A.3. A switch, $SW$, is placed in parallel with the load. When the switch is closed, no current flows through the IC. Therefore, a significant amount of power will be backscattered. This may also be illustrated mathematically as follows:

$$\mathsf{P_{Rad}} = \;\mathsf{P_{Rx}} \tag{A.10}$$

$$\mathsf{P_{Load}} = \;\mathsf{0} \tag{A.11}$$

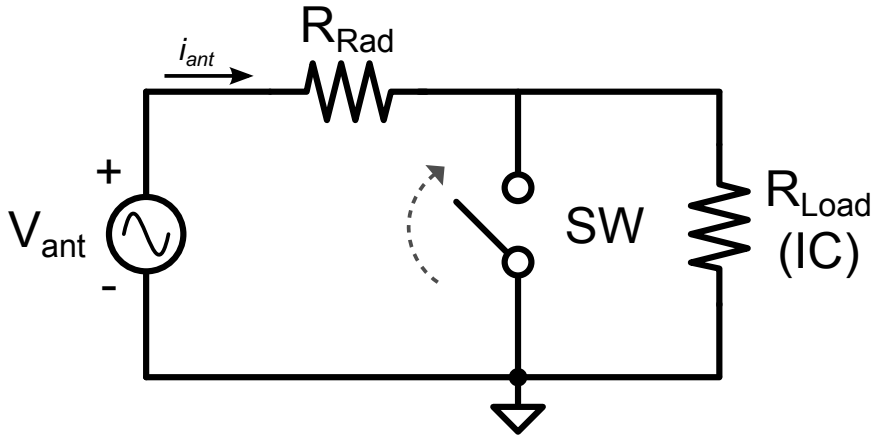


**Figure A.3:** Equivalent circuit for Method 2. A switch, *SW*, varies the impedance seen by the antenna between a short circuit and a conjugately matched load.

When the switch is open, a current, $i_{ant}$, flows through the circuit. Since $R_{Rad}$ and $R_{Load}$ are conjugately matched, each element receives half of the available power at the antenna. Hence,

$$\mathsf{P_{Rad}} \;=\; \mathsf{P_{Load}} \;=\; \frac{1}{2}\,\mathsf{P_{Rx}} \tag{A.12}$$

These results are summarized in Table A.2.

**Table A.2:** Summary of delivered power in Figure A.3 (short-matched load ASK).

| **Switch State** | **Backscattered Power ($\mathbf{P}_{Rad}$)** | **IC Power ($\mathbf{P}_{Load}$)** |
|---|---|---|
| Open | 0.5 $P_{Rx}$ | 0.5 $P_{Rx}$ |
| Closed | $P_{Rx}$ | 0 |

It is now possible to calculate the average power delivered to each element. Again, it will be assumed that only ASK modulation with no additional data encoding is used, with each state equally represented. Therefore the average power delivered to the IC is:

$$P_{IC} = \frac{1}{2}\left(P_{Load,\,SW\,Open} + P_{Load,\,SW\,Closed}\right) = \frac{1}{4}P_{Rx} \tag{A.13}$$

Similar to the first technique, this backscattering method does not result in constant IC power. The power delivered depends on which symbol is being transmitted.

The average backscattered power may be computed similarly as before, by taking the difference in electrical current between states, as follows:

$$P_{BSC} = \frac{1}{2}\Delta {i_{ant}}^2 R_{Rad} = \frac{1}{2}P_{Rx} \tag{A.14}$$

## Method 3: Resistive ASK

Now consider the diagram shown in Figure A.4. A switch, *SW*, is placed in parallel with a "modulation" resistor. This parallel combination appears in series with the load.

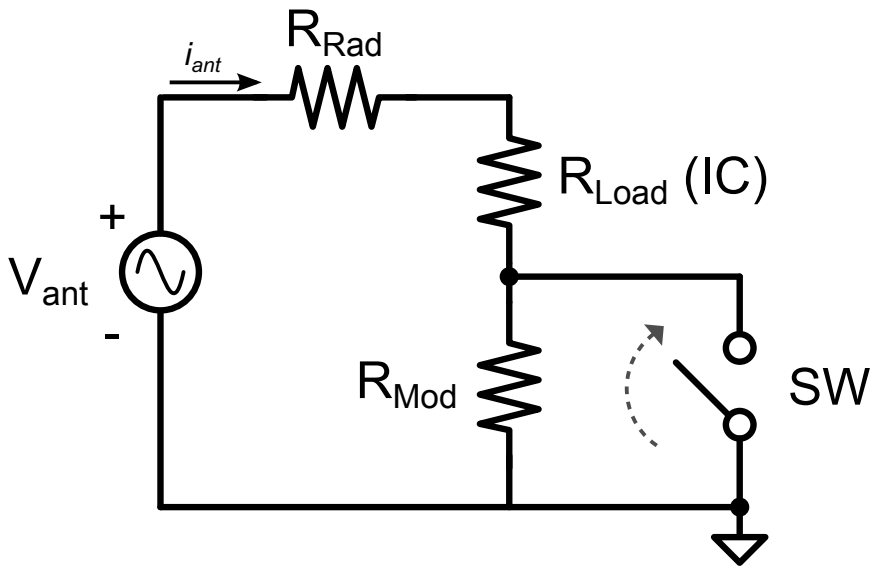


**Figure A.4:** Equivalent circuit for Method 3. A switch, *SW*, varies the impedance seen by the antenna between two resistive values.

While analyzing the preceding backscattering techniques, it was noted that the power delivered to the IC depended upon which symbol was being transmitted. In other words, the IC power was not constant. Using resistive ASK, it is possible to design the resistive loads such that the combined load, $R_{Mod} + R_{Load}$, receives constant power regardless of which symbol is being modulated. To achieve this, the loads are chosen such that:

$$\mathsf{R_{Load}} = \frac{1}{2}\,\mathsf{R_{Rad}} \tag{A.15}$$

$$\mathsf{R_{Mod}} = \frac{3}{2}\,\mathsf{R_{Rad}} \tag{A.16}$$

Let $R_{Mod+Load}$ denote the combined resistance of $R_{Mod}$ and $R_{Load}$. Next, consider the value of $R_{Mod+Load}$ when the switch is open (case 1) and when it is closed (case 2). The resistance in each case is:

$$\mathsf{R_{Mod+Load,1}} = 2\,\mathsf{R_{Rad}} \tag{A.17}$$

$$\mathsf{R_{Mod+Load,2}} = 0.5\,\mathsf{R_{Rad}} \tag{A.18}$$

Thus, the average power delivered to $R_{Mod+Load}$ in each case is:

$$\mathsf{P_{Mod+Load,\,1}} = \frac{1}{2}\,\mathsf{i_{ant}}^2\,\mathsf{R_{Mod+Load,1}} = \frac{1}{2}\left(\frac{\mathsf{V_{ant}}}{3\,\mathsf{R_{Rad}}}\right)^2 2\,\mathsf{R_{Rad}} = \frac{1}{9}\,\frac{\mathsf{V_{ant}}^2}{\mathsf{R_{Rad}}} \tag{A.19}$$

$$P_{\text{Mod+Load},\,2} \;=\; \frac{1}{2}\, {i_{\text{ant}}}^{2}\, R_{\text{Mod+Load},2} \;=\; \frac{1}{2}\left(\frac{V_{\text{ant}}}{1.5\, R_{\text{Rad}}}\right)^{2} \frac{R_{\text{Rad}}}{2} \;=\; \frac{1}{9}\,\frac{{V_{\text{ant}}}^{2}}{R_{\text{Rad}}} \qquad \text{(A.20)}$$

As seen in Equations A.19 & A.20, the average power delivered to the combined load is the same regardless of which symbol is being modulated. However, the power delivered solely to the IC in either state is given by:

$$P_{\text{Load},\,1} \;=\; \frac{1}{2}\, {i_{\text{ant}}}^{2}\, R_{\text{Load},1} \;=\; \frac{1}{2}\left(\frac{V_{\text{ant}}}{3\, R_{\text{Rad}}}\right)^{2} \frac{R_{\text{Rad}}}{2} \;=\; \frac{1}{36}\,\frac{{V_{\text{ant}}}^{2}}{R_{\text{Rad}}} \qquad \text{(A.21)}$$

$$P_{\text{Load},\,2} \;=\; \frac{1}{2}\, {i_{\text{ant}}}^{2}\, R_{\text{Load},2} \;=\; \frac{1}{2}\left(\frac{V_{\text{ant}}}{1.5\, R_{\text{Rad}}}\right)^{2} \frac{R_{\text{Rad}}}{2} \;=\; \frac{1}{9}\,\frac{{V_{\text{ant}}}^{2}}{R_{\text{Rad}}} \qquad \text{(A.22)}$$

Assuming both states are equally likely to occur, the average power delivered to the IC is:

$$P_{\text{IC}} \;=\; \frac{1}{2}\left(P_{\text{Load},\,1} + P_{\text{Load},\,2}\right) \;=\frac{5}{72}\,\frac{{V_{\text{ant}}}^{2}}{R_{\text{Rad}}} \qquad \text{(A.23)}$$

To find the average IC power in terms of the total received power in the reference (matched) case, Equation A.3 may be substituted into A.23 to yield:

$$P_{\text{IC}} \;=\; \frac{5}{18}\, P_{\text{Rx}} \;\doteq\; 0.278\, P_{\text{Rx}} \qquad \text{(A.24)}$$

The backscatter signal power may be found by taking the difference in electrical current between states as follows:

$$\mathsf{P_{BSC}} = \frac{1}{2}\left|\mathsf{i_{ant,2}} - \mathsf{i_{ant,1}}\right|^2 \mathsf{R_{Rad}} \tag{A.25}$$

$$= \frac{1}{2}\left(\frac{\mathsf{V_{ant}}}{1.5\,\mathsf{R_{Rad}}} - \frac{\mathsf{V_{ant}}}{3\,\mathsf{R_{Rad}}}\right)^2 \mathsf{R_{Rad}} = \frac{1}{18}\frac{\mathsf{V_{ant}}^2}{\mathsf{R_{Rad}}} \tag{A.26}$$

Again, using Equation A.3, the backscattered power may be referred to the available power at the antenna in the reference case:

$$\mathsf{P_{BSC}} = \frac{2}{9}\,\mathsf{P_{Rx}} \doteq 0.222\,\mathsf{P_{Rx}} \tag{A.27}$$

In view of this analysis, it is evident that constant IC power was not achieved. Furthermore, the minor advantage in available IC power is dwarfed by the disadvantage of greatly reduced backscatter power, compared to Methods 1 and 2.

## Method 4: PSK

Finally, consider the diagram shown in Figure A.5. A variable reactive impedance, $X_{Mod}$, is placed in parallel with the load. It is assumed that $X_{Mod}$ is purely reactive and varies between states 1 and 2, or +j$X_{Rad}$ and -j$X_{Rad}$, respectively. In addition, it is assumed that $R_{Load} = R_{Rad}$. Taking $|X_{Rad}| = R_{Rad}$, the parallel resistance of $X_{Mod}$ and $R_{Load}$ in each state is:

$$\mathsf{X_{Mod,1}}||\mathsf{R_{Load}} = \frac{\mathsf{jR_{Rad}}^2}{\mathsf{R_{Rad}} + \mathsf{jR_{Rad}}} = (0.5 + \mathsf{j}0.5)\,\mathsf{R_{Rad}} \tag{A.28}$$

$$\mathsf{X_{Mod,2}}||\mathsf{R_{Load}} = \frac{-\mathsf{jR_{Rad}}^2}{\mathsf{R_{Rad}} - \mathsf{jR_{Rad}}} = (0.5 - \mathsf{j}0.5)\,\mathsf{R_{Rad}} \tag{A.29}$$

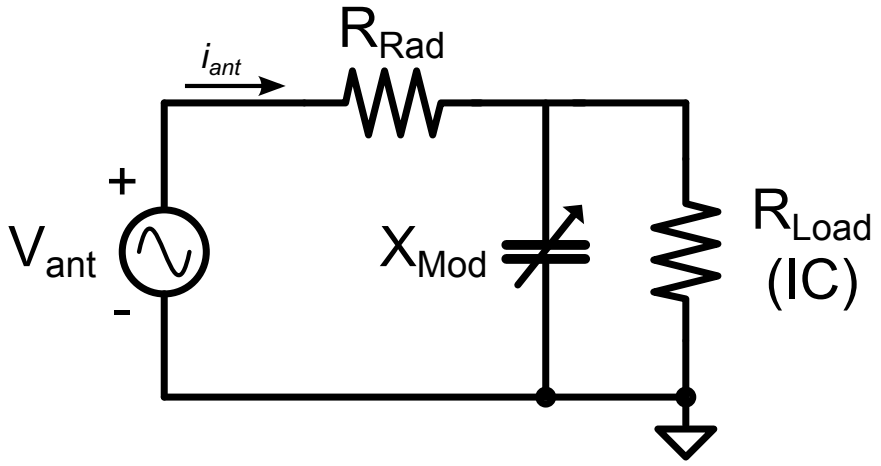


**Figure A.5:** Equivalent circuit for Method 4. An impedance placed in parallel to the load varies between two reactances with equal magnitude and opposite phase.

The total current flowing through the circuit, $i_{ant}$, in each state is:

$$\mathsf{I}_{\mathsf{ant},1} = \frac{\mathsf{V}_{\mathsf{ant}}}{\mathsf{R}_{\mathsf{Rad}} + \mathsf{X}_{\mathsf{Mod},1} \,||\, \mathsf{R}_{\mathsf{Load}}} = \frac{\mathsf{V}_{\mathsf{ant}}}{(1.5 + \mathsf{j}0.5)\ \mathsf{R}_{\mathsf{Rad}}} = (0.6 - \mathsf{j}0.2)\ \frac{\mathsf{V}_{\mathsf{ant}}}{\mathsf{R}_{\mathsf{Rad}}} \tag{A.30}$$

$$\mathsf{I}_{\mathsf{ant},2} = \frac{\mathsf{V}_{\mathsf{ant}}}{\mathsf{R}_{\mathsf{Rad}} + \mathsf{X}_{\mathsf{Mod},2} \,||\, \mathsf{R}_{\mathsf{Load}}} = \frac{\mathsf{V}_{\mathsf{ant}}}{(1.5 - \mathsf{j}0.5)\ \mathsf{R}_{\mathsf{Rad}}} = (0.6 + \mathsf{j}0.2)\ \frac{\mathsf{V}_{\mathsf{ant}}}{\mathsf{R}_{\mathsf{Rad}}} \tag{A.31}$$

Once again, the backscatter signal power may be found by taking the difference in electrical current between states as follows:

$$\mathsf{P}_{\mathsf{BSC}} = \frac{1}{2} \left| \mathsf{i}_{\mathsf{ant},1} - \mathsf{i}_{\mathsf{ant},2} \right|^2 \mathsf{R}_{\mathsf{Rad}} \tag{A.32}$$

$$= \frac{1}{2} \left| (0.6 - \mathsf{j}0.2) - (0.6 + \mathsf{j}0.2) \right|^2 \frac{{\mathsf{V}_{\mathsf{ant}}}^2}{\mathsf{R}_{\mathsf{Rad}}} \tag{A.33}$$

$$= \frac{2}{25}\ \frac{{\mathsf{V}_{\mathsf{ant}}}^2}{\mathsf{R}_{\mathsf{Rad}}} \tag{A.34}$$

Using Equation A.3 again, the backscattered power may be referred to the available power at the antenna in the reference case:

$$\mathsf{P_{BSC}} \;=\; \frac{8}{25}\,\mathsf{P_{Rx}} \;=\; 0.32\,\mathsf{P_{Rx}} \tag{A.35}$$

To find the power delivered to the IC, the voltage across the load must first be determined:

$$\mathsf{V_{Load1,2}} = \mathsf{I_{ant\,1,2}} \cdot \mathsf{R_{Load}} || \mathsf{X_{Mod1,2}} \tag{A.36}$$

$$= \left[\left(0.6 \mp \mathsf{j}0.2\right) \cdot \frac{\mathsf{V_{ant}}}{\mathsf{R_{Rad}}}\right] \times \left[\left(0.5 \pm \mathsf{j}0.5\right) \cdot \mathsf{R_{Rad}}\right] \tag{A.37}$$

$$= \left(0.4 \pm \mathsf{j}0.2\right)\mathsf{V_{ant}} \tag{A.38}$$

Note that the magnitude, $|V_{Load}|$, is the same for both states; this provides PSK modulation with a significant advantage over the other methods discussed. The constant power delivered to the load is calculated as follows:

$$\mathsf{P_{IC}} \;=\; \frac{1}{2}\frac{|\mathsf{V_{Load}}|^2}{\mathsf{R_{Load}}} \;=\; \frac{1}{10}\frac{\mathsf{V_{ant}^2}}{\mathsf{R_{Load}}} \tag{A.39}$$

Finally, using Equation A.3, the IC power referred to the total received power in the reference case is:

$$\mathsf{P_{IC}} \;=\; \frac{4}{10}\,\mathsf{P_{Rx}} \;=\; 0.4\,\mathsf{P_{Rx}} \tag{A.40}$$