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ADAPTABLE MOS CURRENT MODE LOGIC
FOR MULTI-BAND FREQUENCY SYNTHESIZERS

By
Mark Houlgate

A thesis
presented to Carleton University
in fulfilment of the
thesis requirement for the degree of
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in
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Abstract

A new form of MOS Current Mode Logic (MCML) is introduced which allows the drive current and voltage swing of the logic gates to be adaptively controlled, enabling real-time adaptation to achieve an optimum balance between power and speed. The design of a logic library in a $0.18\mu\text{m}$ CMOS process is described, and an adaptable bias controller is developed to ensure independent control of the bias current and voltage swing. Expressions predicting the stability and transient performance of the controller are derived and used to determine design guidelines for the bias controller. The Adaptable MOS Current Mode Logic (AMCML) logic developed in this thesis is used to construct a multi-band frequency divider capable of adjusting its power dissipation based on the required band of operation. The AMCML bias controller and frequency divider were successfully built and tested and confirm the ability of the AMCML-based frequency divider to trade speed for power when switching from one frequency band to another.

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to Sarah

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Chapter 1

Introduction

1.1 Motivation

To promote economic growth in the semiconductor, telephony, and wireless network sectors, governments are exploring new ways of utilizing the radio spectrum. This has led to the growth of the wireless networking infrastructure and the introduction of new applications, communication standards, and frequency band allocations [1]. With this multitude of standards and frequencies, standard, single-band radio transceivers have become ill-equipped to deal with the changing environment in which they are used. To utilize the full range of services, customers have been required to own multiple handsets for use in different geographic regions and for different applications. As a result, continued growth in the wireless sector depends on the integration of all bands and services into a single radio transceiver. To achieve this inter-operability, software-defined radio (SDR) has been introduced [2, 3]. In a SDR, software controls the characteristics of the radio transceiver to adapt to the required frequency band and communications protocol. In addition, SDR enables “cognitive radio”, in which the transceiver can adapt not only to changes in the band of operation, but also to changes in the operating environment itself. While ideal

SDR uses digital signal processing (DSP) to implement all the functions of a traditional radio, multi-band transceivers are still required for the RF front-end [4].

Recently, a great deal of research has been performed on the development of fully-integrated multi-band transceivers [4–8]. Most of the published work has focused on the design of circuits which are traditionally narrow-band, such as low noise amplifiers and voltage-controlled oscillators. These circuits have either been replaced with wide-band implementations, or have used controllable passive devices using MEMs technology or high speed switches to select between different values of fixed passive components. However, there is an absence of work related to optimizing the power of the transceiver over various frequency bands.

One of the largest contributors to power dissipation in any RF transceiver is the frequency divider, which provides channel selection within the frequency synthesizer. Since these circuits are inherently wide-band, traditional multi-band transceivers either operate the divider at the power dissipation required for the highest frequency band, or have employed separate dividers for each band of operation [5, 8]. While simple, these techniques result either in wasted power dissipation when operating at lower frequencies, or wasted silicon area.

1.2 Focus of Thesis

This thesis discusses the implementation of an adaptable frequency divider suitable for use in a multi-band frequency synthesizer. A new form of MOS Current Mode Logic (MCML) is developed which allows the drive current and voltage swing to be adaptively controlled, enabling real-time adaptation to achieve an optimum balance between power and speed.

The new logic family is used to construct a multi-band frequency divider in a $0.18\mu\text{m}$ CMOS technology. The fabricated chip also includes other components of a PLL-based frequency synthesizer.

1.3 Thesis Organization

Chapter 2 provides an overview of conventional MOS Current Mode Logic and discusses recent research in the area. In addition, a background of the operation of frequency synthesizers is presented.

Chapter 3 discusses the principles behind the Adaptable MOS Current Mode Logic (AMCML) introduced in this thesis and provides a summary of the design of a logic library. The design and implementation of an adaptable bias controller used to tune the logic gates for operation at different frequency bands is presented. Stability and transient performance of the controller is explored with the aid of simulation results.

Chapter 4 presents the design of the complete frequency synthesizer using AMCML. Simulation results for the complete divider, phase/frequency detector, and voltage controlled oscillators are provided.

Chapter 5 outlines the implementation of the frequency synthesizer in a $0.18\mu\text{m}$ CMOS process. The design of various buffers and interface circuits are discussed as is the general topology of the chip.

Chapter 6 provides test and measurement results for the chip. In addition, the design of a custom printed circuit board is presented.

Chapter 7 concludes the thesis, summarizes the contributions to research, and provides some suggestions for future work and improvements.

Chapter 2

Background

2.1 Chapter Overview

Advancements in high-frequency mixed signal CMOS technology have resulted in improved digital logic families with reduced power dissipation at high frequencies, improved noise immunity, increased speed, and reduced switching noise. One such logic family is MOS Current Mode Logic (MCML), which was first introduced in [9]^{*} and has since been applied to high frequency microprocessors [10,11], data pipelines [12], asynchronous circuits [13], ring oscillators [14] and frequency dividers used in RF synthesizers [15–23]. In an attempt to simplify the design of MCML, significant research has been performed into design methodologies which can be incorporated into automated computer algorithms [24–26]. This section introduces the basic operation of MCML and Section 2.2.2 reviews some recent work in the area of MCML gate design. In Chapter 3, a new form of MCML is proposed which allows a single library of gates to be used for a wide range of currents and frequencies, by allowing adaptive control of the DC bias condition. This control allows real-time adaptation to achieve an optimum balance between speed and power for a wide range of frequency bands.

^{*}To the author's knowledge

Finally, this chapter presents an overview of PLL-based frequency synthesizers.

2.2 MOS Current Mode Logic

2.2.1 MCML Overview

While standard CMOS logic utilizes the switching nature of CMOS transistors to pull its outputs towards V_{DD} or V_{SS} , MCML (MOS Current Mode Logic) employs the current-steering properties of the differential pair to steer current from one part of the logic gate to another. The general topology of an MCML gate is presented in Figure 2.1. An MCML logic gate can be sub-divided into three elements: a current sink, a logic network, and a load. In the most basic case, the load impedance Z_L is implemented as a resistor with a value of R . Digital logic is realized by designing the pull-down network to steer the current from one branch of the load to the other, based on the polarity of the differential input signals. In the branch where current is flowing, a resistive voltage drop equal to $I \cdot R$ is developed at the output while at the complementary output, ideally no current flows through the resistor and the output is pulled to V_{DD} . As a result, the output signal swing of an MCML logic gate is not rail-to-rail, but is determined by the tail current and the value of the resistive load. Therefore, the digital logic levels of MCML are given by:

$$V_{oH} = V_{DD} \quad (2.2.1)$$

and

$$V_{oL} = V_{DD} - \Delta V \quad (2.2.2)$$

where

$$\Delta V = IR \quad (2.2.3)$$

Logic '1' is represented by V_{oH} , while logic '0' is represented by V_{oL} . The difference between the two is termed the MCML voltage swing, denoted by ΔV .

Figure 2.1: Topology of an MCML gate. The bias current, I , is steered from one load to the other based on the polarity of the differential input signals.

Typical voltage waveforms at the two outputs of an MCML gate are plotted in Figure 2.2. In this exemplary case, the voltage swing is set to 350mV. Since MCML gates respond to the difference between the two signals, Figure 2.3 plots the differential output voltage of a typical MCML gate. Logic levels are not represented by absolute voltage levels, but by the polarity of the differential signal. Binary '1' is represented by a voltage of $+\Delta V$, while binary '0' is represented by $-\Delta V$.

The high speed of MCML logic gates compared to standard CMOS logic results from the fact that the load capacitance only needs to be charged or discharged by an amount equal to the signal swing, instead of from V_{SS} to V_{DD} . Typically, MCML output swings are about 20% of V_{DD} [9]. In addition, the constant current draw inherent to MCML gates reduces switching noise caused by $L(dI/dt)$ effects, and the differential nature of

Figure 2.2: Single-ended output waveforms of an MCML logic gate. V_{oH} and V_{oL} are equivalent to logic '1' and logic '0'. ΔV is the voltage swing, set in this case to 350mV.

Figure 2.3: Differential output waveforms of an MCML logic gate. Logic '1' is represented by $+\Delta V$, while logic '0' is represented by $-\Delta V$. In this case, the voltage swing is 350mV.

MCML increases its immunity to common-mode noise. Although MCML gates are only truly differential at the switching point, the effects of common-mode noise are significantly smaller than single-ended logic implementations. These properties make MCML attractive for mixed signal environments in which highly-sensitive analog circuits are integrated with digital circuitry on the same die.

The differential logic network of an MCML gate is implemented using an NMOS differential pair for each input signal to steer the tail current through the gate to the appropriate load. Figure 2.4 shows a differential pair comprised of two matched NMOS transistors, loaded with ideal, matched resistors and fed with an ideal current sink. The total current, I , is split between the two loads as I_1 and I_2 . The amount of current distributed to each load is dependent on both the magnitude and polarity of the input signal defined as $v_{in} = v^+ - v^-$. In [27, p.529], the currents are described as:

$$I_1 = \frac{I}{2} + \left(\frac{I}{V_{GS} - V_t} \right) \left(\frac{v_{in}}{2} \right) \sqrt{1 - \left(\frac{v_{in}/2}{V_{GS} - V_t} \right)^2} \quad (2.2.4)$$

and

$$I_2 = \frac{I}{2} - \left(\frac{I}{V_{GS} - V_t} \right) \left(\frac{v_{in}}{2} \right) \sqrt{1 - \left(\frac{v_{in}/2}{V_{GS} - V_t} \right)^2} \quad (2.2.5)$$

,where V_{GS} is the gate-source voltage of the NMOS transistors when $v_{in} = 0$ and the current is equally split between the two branches.

Figure 2.5 plots the normalized branch currents as a function of the differential input voltage, v_{in} . When the differential input voltage is zero, the current is equally split between the two branches. However, as the magnitude of v_{in} is increased, the current in one branch gradually decreases while the current in the other increases. For large enough positive

Figure 2.4: CMOS Differential Pair.

input voltages, $I_1 = I$ and $I_2 = 0$, while for large negative input voltages $I_1 = 0$ and $I_2 = I$. According to [27, p.530], complete current switching occurs when:

$$|v_{in}| \geq \sqrt{2} (V_{GS} - V_t) \quad (2.2.6)$$

Using the standard square-law description of an NMOS transistor in saturation, the current through each of the differential pair transistors when $v_{in} = 0$ is given by:

$$\frac{I}{2} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_t)^2 \quad (2.2.7)$$

Solving for $(V_{GS} - V_t)$ in (2.2.7) and substituting the result in (2.2.6) yields a more informative expression for the current switching requirement:

$$|v_{in}| \geq \sqrt{\frac{2I}{\mu_n C_{ox} (W/L)}} \quad (2.2.8)$$

Figure 2.5: Normalized Currents in a CMOS Differential Pair.

Equation (2.2.8) describes the minimum logic level swing required to ensure logic propagation through cascaded MCML gates. When this condition is not satisfied, undesired current in the “off” branch causes V_{oH} to fall below V_{DD} , while the reduced current in the “on” branch causes V_{oL} to rise, reducing the output swing. The reduced output swing results in poorer switching in the next stage, which causes a further reduction in signal swing. As the signal passes through a chain of logic gates, the signal deteriorates rapidly resulting in the inability of logic to function with the degraded signal levels.

Ignoring switching non-idealities *, the total current draw of an MCML gate is constant before, during, and after switching resulting in a total power dissipation per gate of:

$$P_{MCML} = V_{DD} \cdot I \quad (2.2.9)$$

The resulting static power dissipation of MCML gates results in high power dissipation compared to standard static CMOS logic for low frequency operation. While the power

*Charging and discharging of parasitic capacitors in the logic gate result in brief current spikes during switching transients. However, these spikes are brief in duration and do not significantly affect the average current draw of an MCML gate. As a result, the total MCML power dissipation is approximately equal to the DC power dissipation.

dissipation of MCML is ideally independent of frequency, the power dissipation of standard CMOS logic rises proportionally with frequency as given by:

$$P_{CMOS} = C \cdot V_{DD}^2 \cdot f \quad (2.2.10)$$

where C is the load capacitance and f is the switching frequency.

Figure 2.6 illustrates the relationship between power dissipation and frequency for MCML and standard CMOS logic gates. For low frequencies, static power dissipation causes MCML gates to dissipate more power than standard CMOS. However, for frequencies higher than a few hundred megahertz, the frequency-dependent power dissipation of standard CMOS exceeds the static power dissipation of MCML and MCML dissipates less power [9]. As a result, MCML is better suited to high-speed applications than standard CMOS logic gates.

Figure 2.6: MCML and standard CMOS power dissipation as a function of switching frequency.

The approximate propagation delay of an MCML gate is given by:

$$\tau = \frac{C \Delta V}{I} \quad (2.2.11)$$

in which C is the total load capacitance on each of the differential outputs, ΔV is the output voltage swing, and I is the tail current [10]. This relationship indicates that the propagation delay can be reduced by a combination of lowering the signal swing and increasing the tail current used to charge and discharge the capacitance. The current and the signal swing are closely related by (2.2.3): if the current is increased, the load resistance should be decreased in order to keep the swing constant. It is important to note that while small voltage swings can reduce the propagation delay of the logic gate, the swing must be kept large enough to ensure complete current switching in cascaded logic gates. Alternatively, the current can be increased to reduce the delay, but this increases the required signal swing as a result of (2.2.8). In MCML gates using fixed resistive loads, the current and voltage swing cannot be independently controlled to account for process variations or to optimize power dissipation when the circuit is used to operate over multiple frequency bands. This shortcoming of standard MCML is addressed using AMCML (Adaptable MOS Current Mode Logic), introduced in Section 3.2.

2.2.2 Recent Work

Despite the many advantages of MCML, static power dissipation is problematic. As a result, a great deal of research has been conducted to improve the performance of MCML by reducing the power required to operate at a given frequency, either by lowering the power supply voltage, or by reducing the constant current draw of MCML gates.

Although a common method used to increase the maximum operating frequency of logic gates is process scaling, there has been some work which investigates possible changes to circuit topology. In [28], shunt-peaking in MCML gates is proposed to increase the

bandwidth of MCML circuits. Using this technique, series inductors are added to the load of each gate, partially offsetting the effect of the load capacitance. This reduces the propagation delay of the logic gate, effectively increasing the bandwidth of the circuit. Using planar inductors, the bandwidth can be increased by up to 85%, however, the large size of planar inductors makes this technique unsuitable for circuits with even a moderate number of MCML gates. Alternatively, it is shown in [28] that active inductors can be used which alleviates the problem with chip area, but significantly reduces the effectiveness of the peaking.

Since the power dissipation of MCML gates is given by $V_{DD} \cdot I$, reducing the power supply is an alternative technique used to decrease power consumption. Usually, the minimum power supply voltage that can be used is dictated by the requirement to keep all transistors in saturation. In [29,30], a multi-threshold CMOS technology is used to lower the minimum allowable supply voltage. However, since a specialized process is required, this technique is not appropriate for integrated circuits with low cost and high integrability.

In [30,31], the authors demonstrate that the static power dissipation inherent to MCML can be reduced by disabling the current to the logic gate when there is no requirement to change the digital output. This solution is accomplished using a pulse generator which enables the current sink transistor only when there are changes present at the input to the gate. Unfortunately, this technique requires sense amplifiers at the output of each MCML gate. The overhead of the sense amplifiers and pulse generators significantly reduce the effectiveness of this technique. In addition, since one of the primary advantages of MCML is the reduction in switching noise resulting from the constant-current nature of the logic gates, the “self-timed” MCML introduced in [31] is not attractive for use in mixed-signal

environments.

The Adaptable MOS Current Mode Logic proposed in Chapter 3 maintains the basic topology of the MCML logic gates, uses standard CMOS processes, and retains the constant current inherent to standard MCML. In contrast, power is reduced in multi-band circuits by allowing the logic gates in a single circuit to utilize only the power required for operation at a given frequency.

2.3 Frequency Synthesizer Overview

In many radio transceivers, frequency synthesizers are used to tune the circuit to a desired carrier frequency on which information is modulated. Figure 2.7 shows the simplified topology of the front-end of a generic RF transceiver. In the receive path, a low-noise amplifier (LNA) amplifies weak signals while minimizing added noise. A bandpass filter is then responsible for attenuating all signals which are outside of the desired frequency band, and a mixer converts the signal to the intermediate frequency, f_{IF} . The frequency of the down-converted signal is given by:

$$f_{IF} = f_{RF} - f_{LO} \quad (2.3.1)$$

Since the IF filter is usually fixed with a narrow bandwidth around f_{IF} , (2.3.1) demonstrates that the local oscillator signal, f_{LO} , selects which RF frequencies are shifted into the bandwidth of the IF filter. The process is mirrored in the transmit path, in which the IF signal is shifted to the RF carrier, given by $f_{RF} = f_{IF} + f_{LO}$. A power amplifier (PA) amplifies the RF signal to overcome channel losses, and the antenna radiates the signal into the environment.

Figure 2.7: Simplified topology of an RF transceiver front-end.

Many wireless standards use closely spaced channels within a given bandwidth to transmit and receive data. In the case of a cellular phone system, dedicated transmit and receive channels are assigned when a call is made or received, and the appropriate local oscillator signal is generated by the frequency synthesizer. Since the channels are closely spaced, it is critical for the local oscillator signal to be stable and accurate in order to ensure that information from adjacent channels is not mixed into the IF bandwidth. An ideal frequency synthesizer generates purely sinusoidal signals, but practical implementations result in a local oscillator signal with spectral components at frequencies around the desired carrier. These components must be as small as possible to reduce interference from unwanted RF signals.

One possible implementation of a frequency synthesizer capable of generating accurate oscillator signals at a controlled frequency is the charge-pump phase-locked loop (PLL) shown in Figure 2.8. The output frequency is generated by a voltage-controlled oscillator (VCO) placed into a control loop. The instantaneous output frequency of the VCO (and

Figure 2.8: A charge pump PLL implementation of a frequency synthesizer.

the synthesizer) is given by:

$$f_{out} = f_0 + K_{VCO} \cdot v_{control} \quad (2.3.2)$$

in which f_0 is the free-running frequency of the VCO, K_{VCO} is the VCO gain expressed in Hz/V, and $v_{control}$ is the oscillator's control voltage. The correct control voltage is set by feedback in the PLL. The frequency of the VCO output signal is divided by M in the frequency divider and sent to a phase/frequency detector (PFD). The PFD simultaneously compares the phase and frequency of the feedback signal to that of a reference, f_{ref} , and generates error signals indicating whether or not the control voltage should be increased or decreased in order to reduce the difference. These *UP* and *DOWN* signals control switches in a charge pump which either charge or discharge the capacitors in the loop

filter, thereby increasing or decreasing $v_{control}$. The synthesizer reaches steady state when both the phase and frequency of the reference and feedback signals are equal and the PFD stops outputting error pulses. At this point, the capacitors in the loop filter maintain their charge, and $v_{control}$ is held constant. The resulting output frequency of the VCO is given by:

$$f_{out} = M f_{ref} \quad (2.3.3)$$

where M is an integer value.

Equation (2.3.3) indicates that the frequency synthesizer in Figure 2.8 can tune to channels located at integer multiples of the reference frequency, f_{ref} . As a result, f_{ref} determines the minimum channel spacing which can be used with the synthesizer. The reference signal is usually generated using a highly stable (and fixed) quartz crystal oscillator. Frequently, an additional divider is used to generate f_{ref} from the crystal and to lower the channel spacing.

It is shown in [32, p.264] that the closed loop phase transfer function of the charge-pump PLL (assuming $C_1 \gg C_2$) is given by:

$$H(s) = \frac{\frac{I_{CP}}{2\pi C_1} (RC_1 s + 1) K_{VCO}}{s^2 + \frac{I_{CP}}{2\pi} K_{VCO} R s + \frac{I_{CP}}{2\pi C_1} K_{VCO}} \quad (2.3.4)$$

Equation (2.3.4) demonstrates that the charge-pump PLL can be approximated by a second-order system with a zero at $\omega_z = -1/(RC_1)$ and a natural frequency and damping constant given, respectively, by:

$$\omega_n = \sqrt{\frac{I_{CP}}{2\pi C_1} K_{VCO}} \quad (2.3.5)$$

$$\zeta = \frac{R}{2} \sqrt{\frac{I_{CP}}{2\pi} K_{VCO}} \quad (2.3.6)$$

Since ω_n and ζ affect the transient, noise, acquisition, and tracking performance of the PLL, the design of the loop filter involves a great deal of performance tradeoffs [32]. Usually, I_{CP} and C_1 are selected first to give the required natural frequency, and R is then chosen by (2.3.6) to give the desired damping constant. While C_2 has very little effect on the performance of the loop, it is included to reduce ripple on the VCO control line. The resulting component sizes can be quite large, and are implemented off-chip on a printed circuit board (PCB). While the detailed tradeoffs in the design of the loop filter are outside the scope of this thesis, the integrated circuit implementation of the other synthesizer components is discussed in Chapter 4.

2.4 Chapter Summary

This chapter provided the background information for this thesis. The basic topology of MCML was introduced, and the fundamental properties of MCML were discussed. These properties were shown to give MCML the following advantages [9]:

- High speed compared to standard CMOS logic
- Improved immunity to common-mode noise
- Reduced switching noise resulting from its constant current draw

- Lower power dissipation at high frequencies compared to standard CMOS logic

Recent research in the area of MCML gate design was presented and the idea behind AMCML was introduced. Finally, a basic overview of PLL-based frequency synthesizers was presented.

Chapter 3

Adaptable MOS Current Mode Logic

3.1 Chapter Overview

This chapter provides an overview of the theory and design of Adaptable MOS Current Mode Logic (AMCML). Section 3.2 provides a system-level overview of AMCML and discusses the benefits of using AMCML instead of conventional MCML. A detailed description of the logic gate design is presented in Section 3.3. Simulated gate performance is also presented for the AMCML library used in this thesis. The design of the AMCML adaptable bias controller is outlined in Section 3.4. A transfer function for the bias control loop is derived and used to predict the stability performance of the loop. Finally, the transient performance of the AMCML bias controller is presented.

3.2 AMCML System Overview

Despite the advantages of MCML, standard MCML gates suffer from the inability to independently control the drive current and output voltage swing due to their fixed resistive loads. This deficiency results in the requirement for multiple sets of logic gates for use with varying drive strengths and frequency bands. Alternatively, a single set of MCML gates utilizing the current necessary for operation at the highest required frequency can be

used. While this remedies the problem of maintaining a large cell library, excess power is dissipated for low-speed parts of the circuit that would function with lower current drives. Finally, the fixed load inherent to standard MCML makes the voltage swing susceptible to process variations, and limits the ability of the user to adjust performance of the gates after fabrication.

Adaptable MOS Current-Mode Logic (AMCML) seeks to address these problems while incorporating all of the benefits of traditional MCML gates. Figure 3.1 shows a system-level representation of AMCML. In AMCML, the fixed load of standard MCML gates is replaced with a variable load, controlled by an external bias. All logic gates are controlled by a common current control block and an adaptable bias controller. The bias controller senses the current from the current control block and sets the bias of all variable loads to achieve the desired output swing. Since the signal swing and drive current of AMCML affect the speed and power consumption of the overall circuit, the system proposed in Figure 3.1 allows the performance of the AMCML circuit to be adjusted in real-time to find an optimum operating point for the circuit. AMCML also reduces the sensitivity of the circuit to variations in the fabrication process, as the appropriate operating point does not need to be determined in the initial design phase. Figure 3.2 presents an expanded block diagram for an AMCML demonstrating the use of feedback in the adaptable bias controller to generate the bias voltage for all active loads in the biased AMCML circuit. Section 3.3 presents the design of the AMCML gates, while Section 3.4 describes the implementation of the adaptable bias controller.

A similar technique was proposed in [24, p.9], however, the required circuitry was not implemented and published results were based on performance estimations. Most

Figure 3.1: Block diagram of an Adaptable MOS Current Mode Logic (AMCML) system. The feedback loop for the bias controller is shown in Figure 3.2.

Figure 3.2: Expanded block diagram of an Adaptable MOS Current Mode Logic (AMCML) system. Feedback in the adaptable bias controller sets the bias voltage for all active loads in the biased AMCML circuit.

importantly, the MCML implementation used in [24] restricted the drive current to within 10% of its nominal value. For large current variations, such as those supported in this thesis, multiple gate sizes were required.

3.3 AMCML Logic Gate Design

3.3.1 Logic Gate Implementation

The circuit implementation of an AMCML inverter/buffer is presented in Figure 3.3. The pull-down network of the inverter is implemented as a standard NMOS differential pair supplied with a tail current through an NMOS current sink. The gate of the current sink transistor is connected to the control signal RFN , which is generated by the current control block. A current mirror can be used to implement the current control block, which generates RFN from its common gate. Two PMOS transistors, biased in the triode region using RFP , are used to create the variable load of the AMCML gate. RFP is generated by the adaptable bias controller and sets the effective resistance of the PMOS loads, and hence, the signal swing. It is interesting to note that since AMCML circuits are differential, a signal is always accompanied by its complement. Therefore, the AMCML inverter is not required to implement logical inversions, but is used primarily as a buffer to restore signals which may become distorted in more complicated gate implementations.

Other AMCML gates are created by changing the differential pull-down network to implement the desired logic function, leaving the current sink and the load unchanged. The circuit implementation of an AMCML AND gate is presented in Figure 3.4. Since DeMorgan's Theorem states that $\overline{AB} = \bar{A} + \bar{B}$ [27, p.1063], the same circuit can be used to implement the OR function by exploiting the differential nature of AMCML to invert

Figure 3.3: Circuit implementation of an AMCML buffer. The DC load resistance is set using the adaptable bias controller while the current bias is set using the current controller.

all inputs and outputs. In Figure 3.4, the signal names without parentheses are for the AND/NAND gate, while the signal names within the parentheses are for the OR/NOR gate.

Figure 3.4: Circuit implementation of an AMCML AND/NAND (OR/NOR)gate.

Similarly, the circuit implementation of an XOR/XNOR gate is given in Figure 3.5, while the implementation of a D-Latch is shown in Figure 3.6. Various types of flip-flops

are implemented by placing the latches in a master-slave configuration as shown in Figure 3.7.

Figure 3.5: Circuit implementation of an AMCML XOR gate.

While the topology of the circuit determines the logic function, the performance of the gate is governed by the following factors:

- Voltage swing
- Drive current
- PMOS load size
- Current sink transistor size
- Size of the transistors in the differential logic network
- CMOS technology parameters

Figure 3.6: Circuit implementation of an AMCML D-Latch. Flip-flops are created by placing two latches in a master-slave configuration.

Figure 3.7: Master-slave implementation of a rising-edge D-type flip-flop. A separate inverter is not required when AMCML latches are used.

Because of the numerous degrees of freedom available in the design of AMCML gates, the design process is iterative and relies heavily on simulation tools. Some of the considerations and design trends that were used to design the cell library in this thesis are outlined in the next paragraphs. Due to its relative simplicity, the AMCML inverter/buffer was designed first, and the resulting transistor sizes were duplicated in all of the other gates in the cell library, changing only the topology of the pull-down network to implement the various logic functions.

A good starting point for the design of AMCML gates is the choice of voltage swing. From (2.2.11), it is evident that reducing the signal swing decreases the delay of the gate and increases the frequency of operation, but (2.2.8) indicates that the swing must still be large enough to ensure complete current switching in the differential pairs. In addition, reducing the swing lowers cross-talk and substrate coupling, but renders the gate more susceptible to noise. Also, the input differential pairs would need to be made larger to ensure current switching. This would result in a larger input capacitance and would increase the delay of the gate. In an attempt to balance these competing requirements, the signal swing was set to a nominal value of 350mV. However, this value is adjustable using the adaptable bias controller discussed in Section 3.4.

The transient performance of the gate is determined to a large degree by the magnitude of the drive current. Higher currents allow the gate loading capacitance to be charged or discharged at a faster rate, reducing the delay. However, as indicated in equation (2.2.9), increasing the current also results in greater power dissipation. Optimizing the design of the gate for power consumption requires using the smallest current necessary to operate at the desired frequency. In addition, since increasing the current requires a larger voltage swing

to ensure complete current switching as indicated in (2.2.8), the current is limited by the choice of signal swing. If larger currents are needed to improve the transient performance of the gate, the voltage swing may need to be increased to compensate. In this thesis, the drive currents ranged from $7.5\mu\text{A}$ to $80\mu\text{A}$ depending on the frequency of operation. Although simulations in Section 4.2 indicate that the maximum desired frequency of 2.4GHz can be reached with a drive current of approximately $50\mu\text{A}$, the gates were designed to function with up to $80\mu\text{A}$ of current to provide a margin for possible performance reductions caused by process variations in the fabricated chip.

Once an estimate of the required current is obtained using (2.2.11), the current-sink transistor is sized. To increase the output impedance of the current sink, the length of the transistor should be non-minimum. From simulations, it was determined that a length of $1\mu\text{m}$ was sufficient to obtain a high output impedance while keeping the size of the device small. Achieving a high output impedance is necessary to ensure that the transistor accurately mirrors the bias current in the current controller, independent of the voltage across it. The width of the current sink was chosen to ensure that the gate voltage was at least a few hundred millivolts above threshold for the entire range of current while ensuring that the device remains in saturation. These considerations resulted in a width of $1.5\mu\text{m}$.

Sizing of the differential input stage is crucial as these transistors implement the logic function by switching the current from one load to the other. Using equation (2.2.8), the transistors must be large enough to fully switch the current with the given voltage swing and drive current. However, since logic gates are typically connected to the inputs of other logic gates, the differential pair transistors should be kept as small as possible to reduce the input capacitance. This input capacitance contributes to the output capacitance of

previous gates, which lowers the speed of the circuit as indicated in equation (2.2.11). To satisfy these requirements, all differential pair transistors were assigned the minimum length of $0.18\mu\text{m}$. From simulations, a width of $1\mu\text{m}$ was sufficient to ensure current steering while minimizing the area and capacitance of the input transistors.

Since AMCML uses PMOS loads in conjunction with an adaptable bias controller, the size of the PMOS loads is critical in determining the allowable range of bias voltages and output swings. The range of output swings should be maximized, while keeping the area of the loads as small as possible to conserve die area and reduce capacitive loading on the output of the gate. However, it is very difficult in practice to achieve all of these goals. To optimize reliability and performance, a high current and low current version of each gate was developed, differing only in the width of the PMOS load. Because of the complexity involved in sizing the load, the sizing of the PMOS transistors is discussed further in Section 3.3.2.

Table 3.1 summarizes the final design parameters used in the AMCML logic gates. Although the voltage swing is listed as a fixed value, it is independently variable using the adaptable bias controller.

3.3.2 Variable Load Considerations

The ability of AMCML to independently control the drive current and voltage swing results from the use of active PMOS loads in place of the fixed load resistors inherent to standard MCML. Since the circuit was designed to operate over a wide range of currents and voltage swings, the loads were sized with tunability and sensitivity of the voltage swing to changes in the control voltage, RFP , in mind. This was accomplished by ensuring that the PMOS

Table 3.1: Summary of AMCML Gate Design Parameters

Design Parameter	Value
Supply Voltage (V_{DD})	1.8V
Voltage Swing (ΔV)	350mV
Drive Current	$7.5\mu\text{A}$ - $80\mu\text{A}$
(W/L) of Current Sink	$1.5\mu\text{m}/1.0\mu\text{m}$
(W/L) of Input Differential Pair Transistors	$1.0\mu\text{m}/0.18\mu\text{m}$
(W/L) of PMOS Load (low current)	$0.5\mu\text{m}/0.18\mu\text{m}$
(W/L) of PMOS Load (high current)	$0.9\mu\text{m}/0.18\mu\text{m}$

transistors operated in their linear (triode) region of operation over all desired combinations of current and voltage swing.

In the triode region of operation, the current through a PMOS transistor can be modeled by [33, p.57]:

$$I_D = \mu_p C_{ox} \left(\frac{W}{L} \right) \left[(V_{SG} - |V_{tp}|) V_{SD} - \frac{V_{SD}^2}{2} \right] \quad (3.3.1)$$

The transistor operates in the triode region provided that:

$$\begin{aligned} V_{SG} &> |V_{tp}|, \\ V_{SD} &\leq V_{SG} - |V_{tp}| \end{aligned} \quad (3.3.2)$$

Although the above equations do not account for short-channel effects observed in deep sub-micron CMOS technologies, they are suitable for the prediction of design trends and are used throughout this thesis in the interest of obtaining clear and insightful results. Using (3.3.1) it is possible to determine the relationship between the voltage swing and the control voltage RFP , while (3.3.2) is used to determine which design parameters can be used to increase the range over which the loads operate in the triode region. In the case

of a fully-switched AMCML logic gate:

$$\begin{aligned} I_D &= I, \\ V_{SG} &= V_{DD} - V_{RFP}, \\ V_{SD} &= \Delta V = V_{DD} - V_{oL} \end{aligned} \quad (3.3.3)$$

Substituting (3.3.3) in (3.3.1) and solving for V_{oL} (discarding the invalid solution to the quadratic) gives:

$$V_{oL} = (V_{RFP} + |V_{tp}|) + \sqrt{(V_{DD} - V_{RFP} - |V_{tp}|)^2 - \frac{2I}{\mu_p C_{ox} (\frac{W}{L})}} \quad (3.3.4)$$

Figure 3.8 shows a plot of (3.3.4) along with the results of a swept DC simulation with an AMCML bias current of $25\mu A$. The theoretical results are plotted only for the triode region of operation while the simulated plot demonstrates the steep curve which occurs when the PMOS load enters the saturation region. Sensitivity of the logic low level to changes in the control voltage is clearly reduced as the difference between the operating point and the “knee” of the curve is increased.

The minimum allowable value of V_{oL} is found by manipulating (3.3.2) using the values of V_{SG} and V_{SD} from (3.3.3):

$$V_{oL,min} = V_{RFP,max} + |V_{tp}| \quad (3.3.5)$$

Substituting (3.3.5) in (3.3.4) and solving for V_{RFP} :

$$V_{RFP,max} = V_{DD} - |V_{tp}| - \sqrt{\frac{2I}{\mu_p C_{ox} (\frac{W}{L})}} \quad (3.3.6)$$

Figures 3.9 and 3.10 plot (3.3.6) as a function of current and device gate width along with the values from a series of DC simulations on a fully-switched AMCML buffer. These simulations swept V_{RFP} for a series of gate widths and determined the voltage at which the

Figure 3.8: Theoretical and simulated plots of V_{OL} vs. V_{RFP} for the AMCML buffer with an AMCML bias current of $25\mu A$.

PMOS loads entered the triode region, using DC operating point values to determine the region of operation. In both cases, the theoretical equations match the trends predicted by the simulations.

Examining (3.3.5) and (3.3.6) together with Figures 3.9 and 3.10 yields the following conclusions:

- For higher currents, the allowable voltage swing is larger.
- PMOS devices with smaller (W/L) allow for a larger voltage swing.

Complicating matters, the PMOS load must be compatible with the adaptable bias controller discussed in Section 3.4. Due to the implementation of the bias controller, the available voltage range of RFP is slightly less than rail-to-rail since very high and

Figure 3.9: Theoretical and simulated plots of $V_{RFP,max}$ vs. AMCML bias current for the AMCML inverter/buffer.

Figure 3.10: Theoretical and simulated plots of $V_{RFP,max}$ vs. PMOS gate width for the AMCML inverter/buffer ($L=0.18\mu\text{m}$.)

low values of RFP cause the transistors in the output stage of the op-amp to leave the saturation region. Figure 3.11 plots the values of V_{RFP} required to achieve a V_{oL} of 1.45V as a function of current for PMOS widths of 500nm and 900nm, which are used in the AMCML library used in this thesis. For a width of 500nm, the required control voltage drops to extremely low levels and the bias controller is unable to maintain a logic low level of 1.45V. Increasing the width to 900nm remedies this problem and allows the bias controller to function with currents well above the desired maximum current of $80\mu A$.

Figure 3.11: V_{RFP} and V_{oL} (using the adaptable bias controller) as a function of current for two PMOS load sizes.

Optimizing the PMOS load requires a balance between:

- Maximizing the range of voltage swings for which the PMOS loads are linear, reducing sensitivity of the logic gate to noise or errors in RFP .
- Minimizing the area and capacitance of the PMOS loads, reducing silicon area increasing operating frequency

- Ensuring compatibility with the adaptable bias controller by ensuring that the required values of *RFP* are within its acceptable operating range.

These design goals were accomplished using both a high current and low current version of the logic gates. For low-speed, low current applications, the width and length of the PMOS loads were set to their minimum sizes * of $0.5\mu\text{m}$ and $0.18\mu\text{m}$, respectively. Increasing the length would reduce (W/L) further and improve the linearity, but would also result in a larger loading capacitance at the output of the AMCML gate and could degrade the high frequency performance. For high current versions of the gates, the width was increased to $0.9\mu\text{m}$ to ensure compatibility with the adaptable bias controller, as demonstrated earlier in this section.

3.3.3 Transient Response

The requirement for logic gates to charge and discharge loading capacitances limits high frequency operation by creating propagation delays and finite voltage level rise and fall times. Equation (2.2.11) describes the relationship between propagation delay, voltage swing, load capacitance, and drive current. The differential output voltage of an AMCML inverter/buffer with a signal swing of 350mV and drive current of $7.5\mu\text{A}$ is illustrated in Figure 3.12. Rise and fall times are defined as the duration of time between the 10% and 90% points of the logic transition [27, pp.1046-1047]. Similarly, the propagation delay of the logic gate is illustrated in Figure 3.13 as the duration between the switching points of the input and output signals (equivalent to the zero-crossings of the voltage signal).

Transient simulations of the logic gates were performed in Spectre using the adaptable

*As allowed by the process

Figure 3.12: Rise and fall times for AMCML Inverter/Buffer with an AMCML bias current of $7.5\mu\text{A}$.

Figure 3.13: Propagation delay (low-to-high) for AMCML Buffer with an AMCML bias current of $7.5\mu\text{A}$.

bias controller to set the voltage swing to 350mV. To simulate a realistic loading capacitance, the logic gate being tested was loaded with N AMCML buffers, where N is the fan-out of the device. Tables 3.2 and 3.4 summarize the simulated rise/fall times and propagation delays of the logic gates for a swing of 350mV when loaded with a single AMCML buffer. Similarly, Tables 3.3 and 3.5 summarize the rise/fall times and propagation delays for three different values of the fan-out, with an AMCML bias current of 25 μ A. The low current versions of the logic gates were used for the 7.5 μ A and 25 μ A currents, while the high current versions were used for a current of 50 μ A. Symmetry in the inverter/buffer and the D-latch resulted in the rise and fall times being equal. Similarly, the low-high propagation delay was equivalent to the high-low propagation delay. For all other logic gates, separate values are listed in the table for rise and fall times, and for the high-low/low-high propagation delays.

Table 3.2: Summary of AMCML gate rise/fall times for various bias currents, I ($\Delta V = 350mV$, fan-out=1)

Logic Gate	$I=7.5\mu A$	$I=25\mu A$	$I=50\mu A$
Inverter/Buffer	714ps	148ps	94ps
AND/NAND (OR/NOR)	737ps/925ps	161ps/187ps	97ps/115ps
XOR/XNOR	1043ps/936ps	225ps/187ps	129ps/111ps
D-Latch (transparent)	1232ps	249ps	145ps

As predicted by (2.2.11), transition times and propagation delays decrease with higher currents and increase with gate complexity, where higher gate complexity results in a greater number of transistors connected to the output node of the circuit and a higher loading capacitance. In addition, larger values of the fan-out result in larger delays and transition times due to the increased load capacitance on the logic gate.

Table 3.3: Summary of AMCML gate rise/fall times for various fan-outs, N ($\Delta V = 350mV, I = 25\mu A$)

Logic Gate	$N=1$	$N=3$	$N=7$
Inverter/Buffer	148ps	262ps	483ps
AND/NAND (OR/NOR)	161ps/187ps	275ps/302ps	494ps/527ps
XOR/XNOR	225ps/187ps	332ps/300ps	547ps/520ps
D-Latch (transparent)	249ps	362ps	586ps

Table 3.4: Summary of AMCML gate propagation delays for various bias currents, I ($\Delta V = 350mV$, fan-out=1)

Logic Gate	$I=7.5\mu A$	$I=25\mu A$	$I=50\mu A$
Inverter/Buffer	130ps	40ps	30ps
AND/NAND (OR/NOR)	153ps/170ps	49ps/55ps	33ps/33ps
XOR/XNOR	258ps/149ps	90ps/49ps	53ps/30ps
D-Latch (transparent)	222ps	72ps	43ps

Table 3.5: Summary of AMCML gate propagation delays for various fan-outs, N ($\Delta V = 350mV, I = 25\mu A$)

Logic Gate	$N=1$	$N=3$	$N=7$
Inverter/Buffer	40ps	72ps	135ps
AND/NAND (OR/NOR)	49ps/55ps	79ps/86ps	143ps/151ps
XOR/XNOR	90ps/49ps	121ps/78ps	185ps/141ps
D-Latch (transparent)	72ps	101ps	165ps

3.4 Adaptable Bias Controller

3.4.1 Implementation

The adaptable bias controller, similar to that introduced in [24, p.9], is shown in Figure 3.14. The control loop uses a representative version of the AMCML buffer to model the AMCML gates in the rest of the circuit. The inputs to the reference buffer are biased as shown in Figure 3.14 so as to provide a logic low voltage at the output. This voltage is fed back to an operational amplifier, which minimizes the difference between the feedback signal and the desired low-level output voltage, V_{oL} . Negative feedback forces the output of the op-amp to converge to the required bias for the desired signal swing, given by $\Delta V = V_{DD} - V_{oL}$. This bias then serves as the *RFP* control voltage for the rest of the logic gates in the circuit. In practice, there are small variations between the bias required for gates with a single level of inputs such as the buffer, and for multi-level gates such as AND gates, OR gates, XOR gates, and latches. Greater accuracy is achieved by using a separate control loop for multi-level gates in which the reference buffer is replaced with a reference AND or OR gate. In this thesis, an AND gate is used for the multi-level control loop, although other multi-level gates could be used instead. In total, four bias control loops are used to individually control single and multi-level gates for both high and low current implementations.

One of the key challenges in designing the adaptable bias control loop is ensuring that the loop is stable. Since the PMOS load of the representative AMCML gate appears to AC signals as a common-source amplifier, the gain of the loop is high, making it difficult to maintain stability. Dependence of the AC gain on the current makes it possible for the

Figure 3.14: Implementation of the adaptable bias controller. A reference buffer is used in a negative feedback configuration to generate the adaptable load bias voltage corresponding to the desired low level, V_{oL} , and bias current, I_{AMCML} .

loop to be stable for some currents and unstable for others. Whereas the design of the logic gate is dictated by the requirements in Section 3.3, the op-amp can be designed to ensure that the loop is stable. Figure 3.15 shows the circuit implementation of the two-stage op-amp used in the adaptable bias controller. In this implementation, source degeneration resistors are used to lower the gain of the op-amp, while a compensation capacitor (C_C) and series PMOS transistor (M_8) increase the phase margin and improve stability of the loop. Table 3.6 summarizes the op-amp design parameters. With the exception of the source-degeneration resistors, these parameters were chosen as part of a previous design and were not optimized in this thesis. V_{Bias} is generated using a current mirror with a size equivalent to M_5 and a current of $11\mu A$. The power dissipation of the bias controller is equal to the sum of the power dissipation of the op-amp and the AMCML gate in the

feedback path. While the power dissipation of the AMCML gate is variable and equal to $V_{DD} \cdot I_{AMCML}$, the power dissipation of the op-amp is fixed at $94\mu\text{W}$ from a 1.8V supply. This is approximately equal to the power dissipation of a single high-speed flip-flop.

Figure 3.15: Implementation of the operational amplifier used in the adaptable bias controller.

3.4.2 Stability Considerations

Since the adaptable bias controller relies on negative feedback to operate, it can be represented by the block diagram in Figure 3.16. The op-amp is modeled by the frequency dependent forward gain, $A(j\omega)$, while the effect of the representative AMCML buffer is modeled using the frequency independent feedback gain, β . Strictly speaking, β is also frequency dependent, but the op-amp is designed to ensure that any poles introduced by the buffer are insignificant to the overall behavior of the loop. However, it will be shown that the small-signal gain of the buffer is a function of the AMCML bias current. As a result, the performance of the feedback system varies as the bias current is changed from operation in one frequency band to another.

Table 3.6: Summary of Op-amp Design Parameters

Design Parameter	Value
Supply Voltage (V_{DD})	1.8V
V_{Bias}	598mV
Input Stage Current Sink (M_5)	$2.77\mu\text{m}/1.0\mu\text{m}$
Output Stage Current Sink (M_6)	$9.7\mu\text{m}/1.0\mu\text{m}$
Input Differential Pair Transistors (M_1, M_2)	$1.5\mu\text{m}/1.0\mu\text{m}$
PMOS Current-Mirror Load (M_3, M_4)	$1.5\mu\text{m}/0.18\mu\text{m}$
Degeneration Resistors (R)	$20\text{K}\Omega$
Compensation Capacitor (C_C)	1.1pF
Lead Compensation Transistor (M_8)	$40\mu\text{m}/1.0\mu\text{m}$
Output Stage Gain Transistor (M_7)	$49.5\mu\text{m}/1.0\mu\text{m}$

Figure 3.16: Feedback model of the AMCML adaptable bias controller. The op-amp is represented by the transfer function $A(j\omega)$, while the representative AMCML buffer is represented by β .

The closed-loop gain of the feedback system is given by:

$$\frac{v_{out}}{v_{in}} = \frac{A(j\omega)}{1 + \beta A(j\omega)} \quad (3.4.1)$$

In (3.4.1), $\beta A(j\omega)$ is termed the “loop gain” and is critical in the determination of loop stability. In particular, it can be seen that the system is unstable if the magnitude of the loop gain is greater than unity for phase shifts greater than 180° . When these conditions are met, the negative feedback changes to positive feedback and noise in the loop at frequencies satisfying these conditions grows in amplitude, resulting in oscillations and instability. The frequency at which the loop gain crosses unity is termed the “gain crossover” (ω_t) while the frequency at which the phase in the loop reaches -180° is referred to as the “phase crossover” point [34, p.346]. Stability is ensured by designing the op-amp such that the gain crossover occurs at a lower frequency than the phase crossover. A typical measure of the degree of stability in the loop is the “phase margin” which is given by:

$$PM = \angle \beta A(j\omega_t) - (-180^\circ) \quad (3.4.2)$$

Since each pole in the transfer function contributes -90° to the overall phase response, two poles are required before the phase reaches -180° . The phase margin can be increased either by lowering the loop gain and moving the gain crossover to a lower frequency, or by pushing the second pole (and the phase crossover) to a higher frequency. It is shown in this section that the adaptable bias controller can be modeled as a two-pole system with a single zero and the stability of the loop depends only on their relative positions and on the low-frequency loop gain. While phase margin is a measure of stability, it also

plays a role in the transient response of the feedback loop to changes in I_{AMCML} and V_{oL} . Even when the loop is stable, a low phase margin results in ringing in the output of the feedback system. Typically, a phase margin of at least 60° is used, although 45° is usually sufficient [34, pp.353-354].

Appendix A presents the complete derivation of the op-amp transfer function, $A(s)$. The op-amp can be modeled using two poles and one zero and has a simplified transfer function given by:

$$A(s) = -A_v \frac{\left(1 + s/\omega_z\right)}{\left(1 + s/\omega_{p1}\right) \left(1 + s/\omega_{p2}\right)} \quad (3.4.3)$$

where A_v is the low-frequency gain of the op-amp, ω_z is the frequency of the zero, and ω_{pn} denotes the pole frequencies.

The location of the zero is determined primarily by the phase-lead compensation transistor, M_8 , and is given by:

$$\omega_z = \frac{-1}{C_c \left(R_Z - \frac{1}{g_{m7}}\right)} \quad (3.4.4)$$

where

$$R_Z = r_{ds8} = \frac{1}{\mu_p C_{ox} \left(\frac{W_8}{L_8}\right) (V_{SG8} - |V_{tp}|)} \quad (3.4.5)$$

The pole locations are approximately equal to:

$$\omega_{p1} \approx \frac{1}{g_{m7} C_c (r_{ds4} || [r_{ds2} (1 + 2g_{m1} R)]) (r_{ds6} || r_{ds7})} \quad (3.4.6)$$

and

$$\omega_{p2} \approx \frac{g_{m7}}{C_L} \quad (3.4.7)$$

Finally, the low frequency gain of the op-amp is given by:

$$A_v = \frac{g_{m1} g_{m7}}{(1 + g_{m1} R)} [r_{ds4} || r_{ds2} (1 + 2g_{m1} R)] (r_{ds6} || r_{ds7}) \quad (3.4.8)$$

The load capacitance of the output stage, C_L , is comprised of the combined parasitic capacitance of all PMOS loads being controlled by the bias controllers in addition to the interconnect capacitance of the bias distribution network. As a result, C_L varies based on the number of logic gates being driven by the bias controller and is significantly larger than the parasitic capacitances in the output stage of the op-amp and in the feedback AMCML buffer.

It is evident from (3.4.8) that the source degeneration resistors, R , lower the gain of the op-amp, improving the stability of the overall loop by moving the gain crossover to a lower frequency. As an alternative, the gain could be reduced by increasing the current and lowering the output impedance, or by using smaller transistors and lowering g_m . Increasing the current results in higher power dissipation, while using smaller transistors reduces the immunity of the op-amp to the effects of mismatch and process variations. However, since on-chip resistors have a high tolerance, the induced mismatch in the transistors may be smaller than the mismatch of the resistors themselves, and the resulting silicon area would be reduced. More research is required into the optimization of the op-amp to provide only the gain required for accurate tracking in the adaptable bias controller.

Equation (3.4.6) shows that the dominant pole is set primarily by the size of the compensation capacitor, C_c , while the second pole is set by the load capacitance of the bias controller, C_L . Since the phase margin of the system improves as the pole separation increases, it is evident that the stability of the loop can be improved by using a larger compensation capacitor. However, a larger compensation capacitor consumes more silicon area and reduces the slew rate of the op-amp and the speed at which the bias controller can switch from one frequency band to another when used in a multi-band circuit. Conversely,

(3.4.7) demonstrates that a larger value of C_L (resulting from an increased number of AM-CML gates in the biased circuit) moves the second pole to a lower frequency, reducing the phase margin of the bias controller.

Figure 3.17: Feedback AMCML buffer. For the purpose of deriving the small-signal gain of the buffer in the bias controller, v_{in} is placed at the gates of the PMOS loads.

With the transfer function of the op-amp, $A(s)$, defined by (3.4.3), the primary remaining contributor to the phase margin of the adaptable bias controller is the AMCML buffer in the feedback path, β . Figure 3.17 shows the schematic of the buffer. For the purpose of this analysis, the small signal input, v_{in} , is connected to the bias voltage of the PMOS load transistors while the output is taken at the drains of M_9 and M_{10} . Since the logical inputs to the buffer are set such that all of the bias current flows through M_9 , the effects of M_{11} and M_{12} can be neglected. In actuality, M_{11} increases the capacitance at the input, however the resulting pole is at a much higher frequency than those of the operational amplifier and can be ignored in our analysis. The remaining circuit formed by M_9 and M_{10}

appears to small signals as a common-source amplifier, and has a gain given by:

$$\beta = \frac{v_{out}}{v_{in}} = -g_{m9} (r_{ds9} || r_{ds10}) \quad (3.4.9)$$

It is important to note that since M_9 is biased in the triode region of operation, g_{m9} and r_{ds9} are approximately * given by:

$$g_{m9} = \frac{\partial I_D}{\partial V_{SG}} = \mu_p C_{ox} \left(\frac{W}{L} \right)_9 \Delta V \quad (3.4.10)$$

$$r_{ds9} = \frac{\partial V_{SD}}{\partial I_D} = \frac{1}{\mu_p C_{ox} \left(\frac{W}{L} \right)_9 (V_{SG} - |V_{tp}| - \Delta V)} \quad (3.4.11)$$

Since M_{10} is in saturation, its output impedance is approximately equal to:

$$r_{ds10} = \frac{1}{\lambda I_{AMCML}} \quad (3.4.12)$$

where λ is the channel length modulation factor and is process dependent.

The complete loop gain of the adaptable bias controller, $\beta A(s)$ is given by the product of (3.4.3) and (3.4.9). This product can be used to predict the changes in phase margin which result from changes in the AMCML bias current, I_{AMCML} . As the current is increased, it is evident from (3.4.12) that r_{ds10} is reduced. In addition, the bias control loop acts to lower the gate voltage of M_9 , keeping the DC voltage drop constant, as set by V_{oL} . This has the effect of simultaneously lowering the small signal resistance of M_9 , given by (3.4.11). Because of the simultaneous reduction of r_{ds9} and r_{ds10} , the feedback gain given by (3.4.9) is reduced. The gain crossover point is moved to a lower frequency while the phase crossover point remains fixed. As a result, increasing the AMCML bias current improves the phase margin of the loop. In this analysis, the effect of I_{AMCML} on the op-amp zero is temporarily neglected to simplify the discussion. Its effect is discussed later in this section.

*Although simple square-law transistor models are not accurate for short-channel devices, they are suitable for the prediction of design trends.

Simulations were performed in Spectre to verify the stability performance of the adaptable bias controller and to validate the trends predicted in this section. Using Spectre, a stability simulation is available which directly simulates open-loop gain and phase margin. Bode plots of the loop gain and phase margin results are given as the simulation outputs. A zero-volt DC source was inserted between the output of the AMCML buffer and the input to the op-amp to identify the location at which the loop should be “broken” by the simulator. All stability simulations shown in this section were performed with the nominal AMCML voltage swing of 350mV. A bode plot of the loop gain, $\beta A(j\omega)$, is shown in Figure 3.18. As predicted by (3.4.3), the open loop transfer function exhibits two poles and one zero. In addition, it can be seen that $\omega_Z \gg \omega_{p2} \gg \omega_{p1}$ and the zero has no significant effect since $\omega_Z \gg \omega_t$. This plot shows that the third pole can be safely neglected, and validates the approximation made in (A.0.15), which assumed widely separated poles.

Figure 3.18: Bode plot of the loop gain $\beta A(j\omega)$ for $I_{AMCML} = 25\mu A$ and $C_L = 500fF$.

Figure 3.19 plots the phase margin and low frequency loop gain as a function of AMCML bias current for low current values. As expected, increasing the AMCML current lowers the loop gain and improves the phase margin by moving the gain crossover to a lower frequency. For most values of current, the adaptable bias controller has a phase margin which is greater than the typical target of 45° . However, as this simulation was conducted with $C_L=500\text{fF}$, the phase margin would decrease for higher values of the load capacitance.

Figure 3.19: Phase margin and low frequency loop gain as a function of AMCML bias current with $C_L=500\text{fF}$ (low current version).

The effect of load capacitance on the phase margin is seen in Figure 3.20, for an exemplary AMCML bias current of $15\mu\text{A}$. As expected, increasing the load capacitance results in a deteriorating phase margin since the second pole moves to a lower frequency as predicted by (3.4.7), while the dominant pole remains fixed. As the loop gain is unchanged, the phase crossover moves closer to the gain crossover and the phase margin is reduced.

The situation is slightly different for high values of the AMCML bias current. The

Figure 3.20: Phase margin as a function of loading capacitance, C_L with $I_{AMCML} = 15\mu A$.

phase margin and low-frequency loop gain for high current values are plotted in Figure 3.21. As before, the loop gain steadily decreases as the current is increased. However, the phase margin drops dramatically for $I_{AMCML} > 45\mu A$.

The cause of this problem is seen in Figure 3.22 which plots $\beta A(j\omega)$ for an AMCML bias current of $60\mu A$. It is evident from the bode plot that the zero predicted by (3.4.4) has moved between the two poles of the transfer function, pushing the gain crossover to a higher frequency. This effect results from the use of an active PMOS transistor, M_8 , as the phase lead compensation resistor, R_Z . As shown in (A.0.8), R_Z is not constant, but is equal to r_{ds8} , which is a function of V_{SG} . While the gate of M_8 is connected to ground, the source is connected to the output of the op-amp, which is used to bias the PMOS load of the AMCML gate. As the AMCML bias current is increased, the output voltage of the op-amp is reduced in order to keep V_{OL} of the AMCML buffer constant. This in turn increases R_Z , and moves the zero to a lower frequency, as predicted by (3.4.4). In the

Figure 3.21: Phase margin and low frequency loop gain as a function of AMCML bias current with $C_L=500\text{fF}$ (high current version).

worst case, the output voltage drops below the PMOS threshold voltage and M_8 turns off, no longer compensating for the zero in the op-amp.

Figure 3.23 demonstrates the large change in τ_{ds8} as the bias current is increased. While this problem is the result of a design oversight, it is easily solved by interchanging the positions of C_c and M_8 in the operational amplifier. The revised topology exhibits a V_{SG} of M_8 that is much more constant, resulting in the plot of τ_{ds8} vs. I_{AMCML} in Figure 3.24.

Figure 3.25 plots the low-frequency loop gain and phase margin of the improved bias controller. While the loop gain is unchanged by the new topology, the zero is removed and the phase margin increases steadily with the AMCML bias current.

The stability performance of the adaptable bias controller can be summarized as follows:

- The adaptable bias controller can be accurately modeled using two poles and one

Figure 3.22: Bode plot of the loop gain $\beta A(j\omega)$ for $I_{AMCML} = 60\mu A$ and $C_L = 500fF$.

Figure 3.23: r_{ds8} as a function of AMCML bias current for the fabricated bias controller.

Figure 3.24: r_{ds8} as a function of AMCML bias current for the proposed bias controller.

Figure 3.25: Phase margin and low frequency loop gain as a function of AMCML bias current with $C_L=500\text{fF}$ (improved high current version).

zero.

- Increasing the AMCML current improves the stability of the bias controller by lowering the low-frequency loop gain.
- Increasing the number of gates in the AMCML circuit being biased decreases the phase margin by increasing C_L and reducing the pole separation.
- For high bias currents, the op-amp zero is not canceled and the phase margin deteriorates.
- The stability of the adaptable bias controller can be improved for high currents by interchanging the positions of C_c and M_8 in the op-amp of Figure 3.15.

3.4.3 Transient Performance

In addition to determining the stability of the adaptable bias control loop, the design of the operational amplifier also determines the transient response of the loop to changes in the AMCML bias current, I_{AMCML} . Figures 3.26 and 3.27 show the simulated transient response of V_{RFP} and V_{oL} for the high current version of the bias controller, when I_{AMCML} is changed periodically from $25\mu\text{A}$ to $60\mu\text{A}$. This simulation models the situation in which a multi-band circuit built using AMCML is switched between high and low frequency bands. The response is shown for exemplary load capacitances of 0.5pF and 2pF.

When the bias current is changed, the control loop acts to restore V_{oL} to the desired value by changing V_{RFP} . Figure 3.26 shows that when I_{AMCML} is increased, V_{RFP} decreases such that the DC resistance of the AMCML loads remains constant. However, the speed at which the bias voltage reaches its new value is limited by the requirement to charge

Figure 3.26: Step response of V_{RFP} for two values of C_L .

or discharge the large capacitances associated with the op-amp compensation network. The maximum rate of change occurs when the differential input voltage to the op-amp is large and all of the bias current in M_5 flows into (or out of) the compensation capacitor, C_c . This rate of change is equal to the “slew rate” of the op-amp and is approximated by [33, pp.227-228]:

$$SR_{\max} = \frac{I_5}{C_c} \quad (3.4.13)$$

The maximum speed of the adaptable bias controller can be quantified using the time required for V_{RFP} to settle within 1% of its final value. This settling time is determined by a combination of the slew rate, which determines the time required to acquire the new voltage value, and the amount of ringing in the bias voltage around the final value. For small phase margins, this ringing can account for a substantial proportion of the settling time [33, p.235]. From Figure 3.20, the phase margin of the bias controller is reduced

Figure 3.27: Step response of V_{OL} for two values of C_L .

for large values of C_L . Therefore, large values of the loading capacitance result in more ringing in the bias controller, as shown in Figures 3.26 and 3.27. The amount of ringing is quantified as the percentage of the overshoot of the final value to the bias voltage step size as given by:

$$\%Overshoot = \frac{V_{max} - V_{final}}{V_{final} - V_{initial}} \quad (3.4.14)$$

where V_{max} , V_{final} , and $V_{initial}$ are the maximum, final, and initial voltage values of the waveform, respectively. Figure 3.28 plots the settling time and overshoot percentage as a function of the load capacitance. Since the settling time increases with the overshoot percentage despite the constant slew rate, it is evident that a small phase margin detrimentally affects the speed of the bias controller. The transient response in Figure 3.26 also exhibits a “glitch” in the transition from high current to low current. This results from the low phase margin present at the start of the transition in conjunction with the sudden disturbance in the loop. The disturbance causes ringing in the loop which is quickly

suppressed as the phase margin increases as a result of the reduced AMCML bias current.

Figure 3.28: Settling time and % overshoot for transition from $I_{AMCML} = 25\mu A$ to $I_{AMCML} = 60\mu A$ as a function of C_L .

Figure 3.26 also indicates the lack of ringing when I_{AMCML} is decreased from $60\mu A$ to $25\mu A$ and the significant ringing when the current is increased. This discrepancy results from the phase margin performance plotted in Figure 3.21. For an AMCML bias current of $25\mu A$, the phase margin is 67° , while the phase margin is only 10° for a bias current of $60\mu A$. By using the improved version of the bias controller proposed in Section 3.4.2, the phase margin can be improved for high bias currents and the ringing in the step response is reduced.

3.5 Chapter Summary

In this chapter, Adaptable MOS Current Mode Logic (AMCML) was introduced and the design of a complete library of logic gates was detailed. The discussion demonstrated the advantages of using both a high current and low current version of the logic gates, although

only the high current version is absolutely necessary since AMCML allows a single gate size to be used for a wide range of currents. Transient simulation results for the logic gates indicating expected propagation delays and rise/fall times were presented for a range of bias currents. These results demonstrate the ability to increase the speed of an AMCML gate by using a larger bias current.

Section 3.4 outlined the design of the AMCML adaptable bias controller. The topology of the controller was presented, and the discussion indicated that accuracy is improved using separate bias controllers for single-level and multi-level logic gates. In addition, the implementation of the operational amplifier was described. Using this implementation, the transfer function for the bias control loop was developed and used to predict trends in the stability of the bias controller. It was shown in this section that a design oversight in the op-amp causes potential instability in the control loop when high AMCML bias currents are used. A simple fix for this problem was presented. The effect of the number of biased AMCML gates was also shown. Finally, the transient response of the control loop to steps in the bias current was presented, and ringing and overshoot were related to the phase margin of the control loop.

Chapter 4

Implementation of Frequency Synthesizer Components

4.1 Chapter Overview

In this chapter, the implementation of the frequency synthesizer components discussed in Section 2.3 is presented. Figure 4.1 shows the charge pump PLL implementation of the frequency synthesizer used in this thesis. Although all of the components of the synthesizer are included on the test chip, the synthesizer was not optimized for performance and is included only as an application for the AMCML gates developed in this thesis.

Section 4.2 outlines the design and implementation of the frequency divider using the AMCML library developed in Chapter 3. Simulation results are presented for the divider, and the advantages of using AMCML in the design are demonstrated.

Section 4.3 details the design and simulation of the phase/frequency detector using AMCML. Finally, Sections 4.4 and 4.5 summarize the charge pump and VCOs used in the test chip. Unlike the frequency divider and phase/frequency detector, these components were not built using AMCML and are included in the test chip to enable the possibility of testing the AMCML-based components within the context of a complete synthesizer. The

loop filter is implemented off-chip, and is not discussed in this chapter.

Figure 4.1: A charge pump PLL implementation of a frequency synthesizer.

4.2 Frequency Divider

4.2.1 Topology

The programmable frequency divider is used in the frequency synthesizer to control the output frequency by means of the relation $f_{out} = M f_{ref}$, where M is the modulus of the divider and f_{ref} is the reference frequency of the synthesizer, usually provided by a crystal oscillator. Since the first stage of the divider must operate at frequencies up to that of the voltage-controlled oscillator (VCO), implementing programmable counters with operating frequencies in the GHz range is impractical with existing CMOS technologies. This problem is alleviated by using a pulse-swallow frequency divider as shown in Figure 4.2 and introduced in [32, pp.270-271].

Figure 4.2: Block diagram of a pulse-swallow frequency divider.

In the pulse-swallow frequency divider, a dual-modulus prescaler is used to divide the input frequency by either N or $N + 1$, depending on the logical value of *ModulusControl*. The divided output of the prescaler, *SlowCLK*, is then used to clock a 7-bit program counter and a 6-bit swallow counter. The program counter is designed to count P pulses before outputting a pulse and resetting its count. Similarly, the swallow counter is designed to count S pulses before asserting *ModulusControl* and halting its count. Unlike the program counter and swallow counter, which must change their division ratios based on user-provided control signals, the prescaler always divides the input frequency by N or $N + 1$. As a result, the required logic is much simpler, allowing the prescaler to operate at higher frequencies than the programmable counters.

To determine the modulus of the divider, it is useful to describe the operations which occur in one output cycle of the divider. Initially, the prescaler divides the input signal by $N + 1$. After S pulses of *SlowCLK*, the swallow counter asserts *ModulusControl*, changing the modulus of the prescaler to N . At this point in the cycle, the program counter has also counted S pulses of *SlowCLK*. The program counter then counts the remaining $(P - S)$

Figure 4.3: Simulated waveforms for the pulse-swallow frequency divider. N is the modulus of the prescaler when *ModulusControl* is high, P and S are the program and swallow counts, and T_{IN} is the period of the input signal.

pulses of *SlowCLK* and outputs a pulse. This pulse is also used to reset both counters, returning *ModulusControl* to its initial state and restarting the cycle. Provided S is less than P , the overall division ratio, M , can be expressed as:

$$M = S(N + 1) + N(P - S) = NP + S \quad (4.2.1)$$

where P and S are specified by user-provided control signals [32, p.270]. In this work, $N = 15$, P is a 7-bit number and S is a 6-bit number. Using equation (4.2.1), the highest achievable modulus is 1984. Similarly, the minimum achievable modulus is found by setting $S = 1$ and $P = 2$, resulting in a division ratio of 31. Figure 4.3 presents simulated results for the divider output and for *ModulusControl*, indicating the duration of each interval relative to the input period, T_{IN} . Since the duty cycle of the divided signal is significantly less than 50%, circuits which rely on this signal should be duty-cycle independent.

4.2.2 Dual-Modulus (15/16) Prescaler

Adaptable MOS Current Mode Logic (AMCML) was used to construct the high-frequency 15/16 dual-modulus prescaler presented in Figure 4.4 [32, p.295]. The prescaler divides the frequency of the input signal by 16 when *ModulusControl* is low, and by 15 when *ModulusControl* is high.

Figure 4.4: Implementation of the 15/16 dual modulus prescaler.

Four flip-flops were used to create a finite state machine with 16 possible states, and next-state generation logic was used to cycle through the states on each cycle of the input signal. When *ModulusControl* is low, all 16 states are possible, however, setting *ModulusControl* high causes the circuit to skip the zero state. Since only 15 states are used, the prescaler divides by 15 when *ModulusControl* is high. As the prescaler is required to operate at the full input frequency of the pulse-swallow divider, it was implemented using the high current version of the AMCML gates, presented in Chapter 3. Figure 4.5 shows the layout of the prescaler with AMCML gates arrayed in a “standard cell” configuration. This layout of the prescaler consumes a chip area of $120\mu\text{m}$ by $45\mu\text{m}$.

Figure 4.5: Layout of the 15/16 dual modulus prescaler.

Transient simulations of the extracted circuit were conducted to determine the relationship between AMCML drive current and voltage swing, and the maximum operating frequency of the circuit. In the simulation, the prescaler was loaded with an AMCML buffer, which is also used at the output of the prescaler in the complete divider. Simulated waveforms for an input frequency of 2GHz and a modulus of 15 are presented in Figure 4.6. The signal swing, ΔV , was set to 350mV. The maximum operating frequencies for various drive currents are presented in Figure 4.7. As expected, increasing the drive current results in a higher prescaler operating frequency. For frequencies below 2GHz, the required current is still small enough to ensure complete current switching in the differential pairs, so the swing was kept constant at 350mV. For high frequencies, it was necessary to increase the swing to ensure complete current switching in the AMCML gates, as indicated by (2.2.8).

Figure 4.6: Post-layout simulation waveforms of the 15/16 dual modulus prescaler with a modulus of 15.

Figure 4.7: Prescaler operating frequency as a function of AMCML bias current [16].

Figure 4.8: Prescaler power dissipation as a function of operating frequency [16]. Using standard MCML, the power dissipation required for the highest frequency is used for operation in all bands.

The DC power dissipation of the prescaler for various frequencies of operation (from a 1.8V supply) is presented in Figure 4.8. Ignoring AMCML switching non-idealities *, the DC power dissipation of the prescaler is equivalent to the total power dissipation. Table 4.1 summarizes the performance of other recently published dual-modulus prescalers. Operating at a frequency of 2.45GHz, the power dissipation of the prescaler in this work is competitive. The ability to lower the power dissipation of the AMCML-based prescaler for operation at other frequencies increases its attractiveness for use in multi-band transceivers. It should be noted that although Figure 4.8 indicates that the prescaler can operate at frequencies up to 3GHz, 2.45GHz was listed as the maximum frequency as it represents the ISM band at 2.45GHz, while leaving a margin to account for process, voltage, and temperature variations.

Table 4.1: Summary of other published dual-modulus prescalers.

Reference	Division Ratio	Maximum Frequency	Power Dissipation	CMOS Process
[35]	4/5	2.5 GHz	1mW @ 1.5V	0.25 μ m
[20]	32/33	5.5 GHz	52mW @ 1.8V	0.18 μ m
[18]	8/9	2.4 GHz	4.5mW @ 1.8V	0.18 μ m
[22]	4/5	2.4 GHz	11.5mW @ 1V	0.2 μ m
[23]	4/5	15 GHz	54mW @ 1.5V	0.12 μ m
[36]	16/17	1.5 GHz	1.7mW @ 2.7V	0.5 μ m
This work	15/16	2.45 GHz	1.3mW @ 1.8V	0.18 μ m

Table 4.2 lists the power savings available (relative to the power required for operation at 2.45GHz) when AMCML is used to construct a multi-band dual-modulus prescaler. For

*Charging and discharging of parasitic capacitors in the logic gate result in brief current spikes during switching transients. However, these spikes are brief in duration and do not significantly affect the average current draw of an MCML gate. As a result, the total MCML power dissipation is approximately equal to the DC power dissipation.

operation in the GSM400 band (400MHz), 82% of the power can be conserved. Based on these results, a single AMCML circuit can be used for all bands in a multi-band transceiver, dissipating only the power required for the selected frequency of operation. Using traditional MCML, multi-band transceivers would either use a single prescaler dissipating the power required for operation at the maximum frequency of operation, or would implement multiple prescalers optimized to the different frequency bands.

Table 4.2: Prescaler power savings using AMCML (relative to the power required for 2.45GHz operation) [16]

Frequency Band	Power Savings
GSM400 (400MHz)	82%
ISM (900MHz)	71%
GSM1800 (1.8GHz)	35%
GSM1900 (1.9GHz)	31%
ISM (2.45GHz)	0% (baseline)

4.2.3 Program Counter

As described in Section 4.2.1, the program counter is responsible for counting P pulses of *SlowCLK* before outputting a pulse and resetting itself and the swallow counter. Figure 4.9 shows the implementation of the program counter used in this work, which incorporates a 7-bit binary counter, a 7-bit comparator, and a “one” detector.

The binary counter is clocked by *SlowCLK*, and increments its count each clock cycle. For each count value, the 7-bit comparator checks each bit for equality with the corresponding bit in the control signal and outputs a logical one for each equal bit. When the one detector detects equivalence in all of the 7-bits, indicating that the desired count has

Figure 4.9: Implementation of the 7-bit program counter.

been reached, F_{out} is driven high. The output signal is also connected to the synchronous reset input on all flip-flops in the binary counter. On the cycle after F_{out} is driven high, the binary counter is reset to zero and the count is restarted. In addition, the output pulse is used to reset the swallow counter, indicating the end of one complete cycle of the frequency divider. Since the program counter contains 7-bits, any count between 0 and 127 can be set by the control signal. However, it is important to realize that in order to achieve a division ratio as specified in equation (4.2.1), the control signal must be set to $P - 1$ since the zero-state is included in the count. Also, P must be greater than S to ensure correct operation.

Figure 4.10 shows the implementation of the binary counter. While only 4 bits are shown in the diagram, additional bits are easily added by repeating the pattern for each bit. The counter is constructed using AMCML-based toggle flip-flops. These flip-flops are designed to change their output state on the clock edge, provided the toggle input is high.

Figure 4.10: Implementation of the binary counter.

If the toggle input is low, the output of the flip-flop is unchanged. AMCML versions of the toggle flip-flop were created by adding an input multiplexer to the master-slave D flip-flop. The multiplexer implements the function $D = T \cdot \bar{Q} + \bar{T} \cdot Q$, and was implemented using two AND gates feeding an OR gate. Each bit in the binary count is taken directly from the output of the corresponding flip-flop. Since the first flip-flop maintains the least-significant bit in the count (*CNT0*), its output must toggle unconditionally on each clock cycle. As a result, its *T* input is always connected to logic “1”. The next bit in the chain, *CNT1*, is set to toggle on the clock edge after *CNT0* becomes high. Similarly, the third flip-flop, representing *CNT2*, is set to toggle on the clock edge after all of the previous bits become high. This pattern is repeated for all additional bits by ensuring that the *T*-input of the corresponding flip-flop is connected to the logical AND of all previous count bits. It is useful to note that the logical AND of all previous values is readily obtained by ANDing *T* and *Q* for the previous flip-flop in the chain.

Since the program counter and swallow counter are clocked at a much lower frequency than the prescaler, the low current version of AMCML gates was used to reduce power dissipation. Using a reference current of $7.5\mu\text{A}$ for all AMCML gates, the program counter

dissipates $908\mu\text{W}$ from a 1.8V supply.

4.2.4 Swallow Counter

The swallow counter, as discussed in Section 4.2.1, is used to count S pulses of *SlowCLK* before asserting *ModulusControl* and changing the modulus of the prescaler from $N + 1$ to N . The implementation of the swallow counter, shown in Figure 4.11, is almost identical to that of the program counter due to the similarity in their functions. Since S is always less than P , only 6-bits were used in the binary counter and comparator. The only other difference between the program counter and swallow counter is a result of the different action taken when the desired count is reached. While the program counter outputs a pulse and resets itself, the swallow counter asserts *ModulusControl* and holds its count until reset. As a result, *ModulusControl* is connected to an active low enable input on the counter. When *ModulusControl* is high, combinational logic forces the T input of all flip-flops to be low, effectively holding the current state until the circuit is reset by the output of the program counter. Using a reference current of $7.5\mu\text{A}$ for all AMCML gates, the swallow counter dissipates $809\mu\text{W}$ from a 1.8V supply.

4.3 Phase/Frequency Detector

Phase error detection in the synthesizer is accomplished using a phase/frequency detector (PFD), which simultaneously compares the phase and frequency of the PLL reference to that of the signal at the output of the frequency divider. In general, the PFD generates an output signal that is proportional to the phase or frequency difference between the two signals and the phase-locked loop acts to minimize this difference. Although many PLLs

Figure 4.11: Implementation of the 6-bit swallow counter.

can accomplish this task using a simple phase detector, a device capable of simultaneously measuring both phase and frequency decreases the acquisition time of the synthesizer [32, p.262].

In the case of a charge-pump based PLL, the phase/frequency detector actually outputs two signals: *UP* and *DOWN*. The *UP* signal indicates that the VCO frequency should be increased to obtain lock, while the *DOWN* signal indicates that the frequency should be decreased. These signals are used by switches in the charge pump to charge or discharge a capacitor in the loop filter, thereby increasing, or decreasing the VCO control voltage. As a result, the duration of the *UP* and *DOWN* signals determines how much charge is transferred into the loop filter and the corresponding change in the loop control voltage. For large differences in the phase or frequency of the input signals, the duration of the corresponding PFD output signal is large.

Figure 4.12: State diagram for the tri-state phase/frequency divider.

Figure 4.12 shows the state diagram of a tri-state phase/frequency detector with separate *UP* and *DOWN* output signals. As indicated in the state diagram, the PFD maintains three states: a reset state in which neither of the two signals are asserted, an *UP* state, and a *DOWN* state. State transitions occur on the rising edges of the reference and feedback signals. As a result, the PFD determines phase and frequency differences by the relative occurrences of edges in the signals and is duty-cycle independent. This duty-cycle independence is crucial for the proper operation of the frequency synthesizer since the output of the programmable frequency divider discussed in Section 4.2 does not have a 50% duty cycle.

To understand how phase-detection occurs, it is useful to investigate the state transitions in Figure 4.12 when the frequencies of the two signals are equal. Initially, the PFD is in its reset state and *UP* and *DOWN* are both low. On the rising edge of one of the input signals (say the reference signal), the PFD moves to the *UP* state and asserts the signal. Since both signals have the same frequency, the next edge to occur is that of the feedback signal. When this edge is detected, the PFD returns to the reset state until the next reference edge causes the *UP* signal to be asserted once again. If the first edge to occur were on the feedback signal instead of the reference, the equivalent loop would occur

Figure 4.13: Phase/Frequency detector waveforms with equal, fixed frequency inputs.

into and out of the *DOWN* state. As a result, the *UP* or *DOWN* signal is high for a duration equal to the phase difference between the two signals with the particular output indicating which signal is leading the other (determined based on when the circuit is reset). It is important to note that when the PFD is placed in the PLL, the non-zero width of the output pulses causes a change in the VCO control voltage. Therefore, it is impossible for the synthesizer to maintain frequency lock until the phase difference between the signals goes to zero [32, p.262]. Simulation results for the PFD with equal frequency inputs are shown in Figure 4.13. In this situation, pulses with a width equal to the phase difference appear on the *UP* signal. The brief reset pulses present in the *DOWN* signal result from the implementation of the phase/frequency detector, which is discussed shortly.

Frequency detection is achieved in the PFD by counting the relative number of edges in the two signals. If the frequency of the reference signal is higher than that of the feedback

Figure 4.14: Phase/Frequency detector waveforms with a large, fixed input frequency difference. The wide *DOWN* pulses indicate that the frequency of the VCO should be lowered to compensate.

signal, the *UP* signal remains high for numerous cycles of the reference, indicating that the VCO should increase its frequency. When an edge is finally detected on the feedback signal, the PFD briefly returns to the reset state until the next edge of the reference signal returns the PFD to the *UP* state. The larger the frequency difference, the greater the proportion of time that the *UP* signal is high. Similar logic can be applied to the case where the frequency of the feedback signal is higher and the *DOWN* signal is asserted. Although it is possible for the first edge to the PFD to drive the output in the wrong direction (depending on the timing of the initial reset), the PFD quickly recovers on subsequent edges. Transient simulation waveforms for the case of large and small frequency differences are presented in Figures 4.14 and 4.15. In both cases, the frequencies of the input signals are fixed for illustrative purposes. However, when used within a frequency synthesizer, the

VCO will change its frequency to compensate for the phase or frequency difference and the exemplary waveforms shown in this section will never be observed. In the first case, the feedback frequency is four times higher than the reference signal. As a result, large *DOWN* pulses are present indicating to the charge pump that the control voltage should be decreased. In actuality, frequency differences in the loop are much smaller and the waveforms appear more like those in Figure 4.15, in which the frequency of the feedback signal is only 1.1 times that of the reference. This figure also demonstrates the situation in which the PFD initially outputs an *UP* pulse before recovering.

Figure 4.15: Phase/Frequency detector waveforms with a small, fixed input frequency difference.

The state diagram of Figure 4.12 can be closely approximated using the circuit shown in Figure 4.16. The circuit is comprised of two D-type flip flops whose inputs are tied high, and whose outputs correspond to the *UP* and *DOWN* signals. Their clock signals are tied to the input signals, and their asynchronous reset terminals are tied to the logical

AND of the two output signals. When an edge is detected on either of the two signals, the corresponding flip-flop drives its output high, where it remains until it is reset. This reset occurs when an edge on the complementary signal is detected, driving its flip-flop high. After a brief delay, the output of the AND gate becomes high resetting the two flip-flops. Since this implementation allows both inputs to be high simultaneously for the brief duration of the reset, it is not exactly equal to the state diagram presented in Figure 4.12. However, the remainder of the operation remains the same as discussed in the ideal case.

Figure 4.16: Implementation of the tri-state phase/frequency detector.

Another critical difference occurs in the case where the phase of the two signals is zero. In this case, the PFD would still produce brief pulses on *UP* and *DOWN* with a duration equal to the delay of the reset path. Ideally, the charge pump would then attempt to charge and discharge the loop filter by the same amount resulting in no net charge flow from the capacitor. However, inevitable mismatches in the charge and discharge current or in the duration of the *UP* and *DOWN* pulses result in a non-zero change in the loop control voltage. This creates a small disturbance in the PLL which must be corrected. Since these pulses occur at the reference frequency, sidebands known as “reference spurs”

are created in the output spectrum of the VCO.

For small phase differences, the phase/frequency detector suffers from a condition known as the “dead zone”. In this case, the required output signal does not reach the threshold required to enable the current in the charge pump before being reset. As a result, the PFD does not function for small phase differences, resulting in jitter around the desired frequency of the synthesizer. This problem can be remedied by ensuring that there is sufficient delay in the reset path to allow a pulse to be fully developed.

Figure 4.17: NOR-gate implementation of the flip-flop used in the PFD.

The schematic in Figure 4.16 is implemented using the low current version of the AMCML gates and the flip-flop schematic shown in Figure 4.17. This topology, taken from [32, pp.260-261], implicitly results in the D input being tied high. Using tail currents of $7.5\mu\text{A}$ for all AMCML gates, the PFD dissipates $122\mu\text{W}$ from a 1.8V supply.

4.4 Charge Pump

In a frequency synthesizer incorporating a charge pump, the phase/frequency detector and charge pump work together to adjust the VCO control voltage based on the phase or

frequency error in the loop. *UP* and *DOWN* signals from the PFD enable switches in the charge pump which steer current into, or out of a capacitor in the loop filter. The design of the charge pump shown in Figure 4.18 and summarized in Table 4.3 was taken directly from [37], with permission, and dissipates $97\mu\text{W}$ from a 1.8V supply.

Figure 4.18: Current Steering Charge Pump Topology [37]

Table 4.3: Summary of the charge pump design parameters.

Design Parameter	Value
Supply voltage (V_{DD})	1.8V
(W/L) of NMOS transistors ($M_6, M_7, M_8, M_9, M_{10}, M_{15}$)	$1\mu\text{m}/0.18\mu\text{m}$
(W/L) of PMOS transistors ($M_{11}, M_{12}, M_{13}, M_{14}$)	$1\mu\text{m}/0.18\mu\text{m}$
(W/L) of current mirror transistors (M_1, M_2, M_3, M_4, M_5)	$1.5\mu\text{m}/0.5\mu\text{m}$
Bias current (I_{bias})	$15\mu\text{A}$

Table 4.4: Summary of the LC-VCO design parameters.

Design Parameter	Value
Supply voltage (V_{DD})	1.8V
(W/L) of PMOS cross-coupled pair (M_1, M_2)	100 μm /0.18 μm
(W/L) of NMOS cross-coupled pair (M_3, M_4)	50 μm /0.18 μm
Bias current (I_{bias})	4mA
(W/L) of current mirror (M_5, M_6)	100 μm /0.54 μm
Inductor (L)	6.1nH
Fixed capacitor (C_{fixed})	0.66pF
(W/L) of MOSCAPs (C_{var})	(5 μm /10 μm) X 8

Table 4.5: Simulation results for the cross-coupled LC-VCO

Center Frequency (@1.5V control voltage)	1.41 GHz
VCO Gain	400 MHz/V
Peak Differential Output Swing	1.43 V
Phase Noise (at 1MHz offset from carrier)	-110 dBc/Hz
DC Power Dissipation (from 1.8V supply)	8.3 mW

4.5.3 Ring Oscillator

Figure 4.20: Ring Oscillator Topology

To provide greater flexibility in testing components in the synthesizer, a ring oscillator with a wide tuning range was constructed using five AMCML inverter stages, as shown in Figure 4.20. The oscillation frequency of a ring oscillator is given by [33, p.675]:

$$f_{osc} = \frac{1}{2N\tau_{inv}} \quad (4.5.1)$$

where N is the number of stages and τ_{inv} is the propagation delay of a single inverter stage.

The delay of an AMCML inverter is:

$$\tau_{inv} = \frac{C\Delta V}{I} \quad (4.5.2)$$

where C is the parasitic load capacitance of each stage and ΔV is the signal amplitude.

Substituting equation (4.5.2) into equation (4.5.1), the VCO oscillation frequency can be expressed as:

$$f_{osc} = \frac{I}{2NC\Delta V} \quad (4.5.3)$$

Equation (4.5.3) suggests that the frequency can be controlled by varying the bias current used to drive each stage in the ring oscillator. As a result, the control voltage is connected to the gate of a PMOS transistor feeding into the current mirror which supplies RFN to the AMCML inverters. Since increasing the control voltage reduces the current drive, the frequency of the VCO decreases as the control voltage is increased. This implementation was used so that the polarity of the ring oscillator matched that of the LC VCO.

Figure 4.21: Simulated frequency vs. control voltage for the ring oscillator VCO.

Figure 4.21 plots the simulated frequency of the VCO as a function of the control voltage, while Figure 4.22 plots the peak differential output voltage. Since the drive current in the VCO changes rapidly with the control voltage, the ring oscillator has a wide tuning range, from approximately 400MHz to 3GHz. While the gain of the VCO is fairly non-linear due to the simplicity of the design, the average VCO gain is -3GHz/V. This wide tuning range provides flexibility in testing the synthesizer.

The simulated phase noise of the ring oscillator at a 1MHz offset from a fundamental

Figure 4.22: Simulated differential output amplitude vs. control voltage for the ring oscillator VCO.

frequency of 1.4GHz was found to be -70dBc/Hz. This is inferior to the narrow-band LC-VCO. DC power dissipation ranges from $136\mu\text{W}$ for low frequencies to 1.32mW for high frequencies, from a 1.8V supply.

4.6 Chapter Summary

In this chapter, an overview of the implementation of the frequency synthesizer components was provided. An AMCML-based implementation of a pulse-swallow frequency divider incorporating a dual-modulus prescaler, a program counter, and a swallow counter was described. Simulation results for the divider were presented along with a discussion of the advantages of using AMCML to construct a multi-band divider.

Finally, the design of the phase/frequency detector, charge pump, and two voltage controlled oscillators were outlined. The components designed in this chapter allow AMCML to be tested within the context of a complete synthesizer, and demonstrate its usefulness

when applied to multi-band circuits.

Chapter 5

Integrated Circuit Implementation (ICFCUMDK)

5.1 Chapter Overview

Implementation of the AMCML-based frequency synthesizer is discussed in this chapter. The prototype was implemented in a $0.18\mu\text{m}$ CMOS process available from the Taiwanese Semiconductor Manufacturing Corporation (TSMC) through a grant from the Canadian Microelectronics Corporation (CMC). The process has a single salicided polysilicon layer with six metal layers available for routing. Substrate doping is p-type, requiring all PMOS devices to be formed within n-wells. As a result, all NMOS devices share a common substrate, while PMOS devices can be isolated in their own wells to eliminate the body effect. Although TSMC allows the use of “deep n-wells” in this process to isolate NMOS devices from the substrate, this option was not used because of the significant area requirements. The nominal supply voltage for the process is 1.8V and the nominal threshold voltage (with zero bulk-source voltage) is 0.45V.

Figure 5.1 shows the topology of the prototype. The complete frequency synthesizer is fabricated on-chip, with the exception of the loop filter, which is implemented on a

printed circuit board (PCB). A series of high-speed digital multiplexors allow one of three possible VCOs to be used with the chip. Using the control signal *VCOab*, the user can determine whether to use a low phase-noise LC-VCO or a wide tuning range ring oscillator. Alternatively, an external oscillator can be used by setting *VCOInExt* low.

To facilitate testing and diagnosis of the chip, monitoring points are added to the outputs of most critical devices. The prototype provides access to the output of the charge pump, VCO, dual modulus prescaler, and both program and swallow counters. To reduce pin count, the internal counts of the PC and SC can also be monitored through a 7-bit count multiplexer, controlled with *CNTMuxCtl*. AMCML bias monitors allow for DC measurements to ensure operation of the four adaptable bias controllers on the chip.

The pin count is reduced by using single-ended signals for all outputs and converting between single-ended and differential signals on chip. For all digital control signals, CMOS-MCML logic converters allow single-ended rail-to-rail signals to be used on the PCB without specific knowledge of the on-chip logic levels (variable using the adaptable bias controller). Output buffers convert differential signals to single-ended, while allowing the chip to drive long bond-wires and capacitive loads. Separate output buffers exist for low frequencies ($< 2\text{MHz}$), medium frequencies ($2\text{MHz}-100\text{MHz}$), high frequencies ($100\text{MHz}-500\text{MHz}$) and RF frequencies ($>500\text{MHz}$). The implementation of these buffers is discussed in Section 5.5.

A photograph of the fabricated chip is shown in Figure 5.2. Sixty-four bonding pads are used and are arrayed in a $2\text{mm}\times 2\text{mm}$ square, with sixteen pads on each edge. The bond-pads are rectangular with a size of $75\mu\text{m}$ by $65\mu\text{m}$ with $35\mu\text{m}$ spacing ($100\mu\text{m}$ pitch). All metal layers are used in the pad, with the exception of metal1 which is used only for

V_{DD} and GND pads. Wide power and ground traces ($27\mu\text{m}$) run along the perimeter of the chip to lower the impedance of the power distribution network and to improve its current-handling capability. High frequency pads are placed between DC pads to reduce crosstalk and coupling through the bond-wires and PCB traces. Supply and ground is also available at each edge of the chip. Internally, an additional copy of the LC-VCO was implemented for wafer probing. Remaining space was used by another researcher.

Figure 5.1: Chip Topology.

5.2 Power Supply and Bias Network

The power supply and bias network of the integrated circuit was designed to reduce power supply and substrate coupling, while ensuring that replica bias currents and voltages are

Figure 5.2: Photograph of the completed chip (ICFCUMDK). Faded regions identify the area shared with another researcher.

With the exception of the PMOS loads inherent to AMCML gates, currents are used to bias all circuit elements. Five replica bias currents are provided to the chip for the

charge pump, LC-VCO, adaptable bias controllers, low-current AMCML gates, and high-current AMCML gates. With the exception of the LC-VCO and charge pump bias circuitry, designed in [37], all replica currents are connected to a current distribution network, shown in Figure 5.3. In each of the distribution networks, an NMOS current mirror replicates the bias current. The replicated current is then fed into a PMOS current mirror which re-generates the current and routes it to other parts of the chip. For circuits close to a current mirror, $V_{REF,local}$ is connected directly to the current sink transistors in the destination circuit. To improve current matching over large distances, current is routed instead of voltage and localized current mirrors are used. This scheme eliminates current mismatches caused by IR drops in the ground line between the diode-connected transistor at the input to the chip and the current sink transistor at the destination circuit.

Metal-insulator-metal (MIM) capacitors with a value of 1pF are connected to the each of the current mirrors to help shunt high frequency noise to ground and provide a stable reference voltage. Similar capacitors are also used between V_{DD} and ground to reduce noise in the supply lines. Additional supply filtering is provided by the PCB.

5.3 VCO Multiplexer

As introduced in Section 5.1, the user can select between one of two internal VCOs, or an external signal generator. On-chip, the output of the VCO is selected using the VCO multiplexer shown in Figure 5.4 in conjunction with two digital control signals. The mux is comprised of two stages. The first stage implements the logic function $VCO_{LC} \cdot VCO_{select} + VCO_{Ring} \cdot \overline{VCO_{select}}$ and selects between the two internal VCOs. The second stage uses an identical logic structure to toggle between the output of the first stage and the external

signal generator based on the logical value of VCO_{InExt} . Finally, an output buffer is used to restore the signal and drive the input to the frequency divider.

Figure 5.4: Implementation of the VCO multiplexer. All logic gates are implemented using AMCML.

The multiplexer was implemented using the high current version of AMCML gates and uses the same tail current used by all other high current AMCML gates. As a result, the power dissipation varies for each frequency of operation, as in the dual modulus prescaler.

5.4 Divider Count Multiplexer

To reduce the number of pins, the internal count values of the program counter and swallow counter are multiplexed to seven bond pads. An array of six multiplexer cells is used to toggle between the least significant six bits in the two counters. Figure 5.5 shows the implementation of each of the multiplexer cells. The mux implements the logic function $CNT[n] = PC[n] \cdot Sel + SC[n] \cdot \overline{Sel}$ where $CNT[n]$, $PC[n]$, and $SC[n]$ are the n -th bit of the output, program counter, and swallow counter, respectively. Sel determines whether the program count or swallow count is connected to the output; when Sel is high, the program counter is selected, otherwise the swallow counter passes through the mux. The most-significant bit in the program counter is passed directly through an AMCML buffer. Using the low-current version of AMCML gates with a tail current of $7.5\mu A$, the mux dissipates $344\mu W$ from a $1.8V$ supply.

Figure 5.5: Multiplexer cell for internal divider count. An array of 6 cells is used to multiplex $PC[0..5]$ and $SC[0..5]$. $PC[6]$ is passed simply through an AMCML buffer.

5.5 Output Buffers

Output buffers are required to convert on-chip differential signals to single-ended, while driving the load of the chip caused by bond-pad capacitance, bond-wire inductance, and capacitive traces on the printed circuit board (PCB). Figure 5.6 presents a model for the load in which the bond-pads are modeled with a simple capacitor C_{pad} , the bond-wire is represented by inductor L_W and resistor R_W , and the loading of the PCB is represented by a lumped capacitor, C_{PCB} . In general, the bond-pad capacitance is a few hundred femto-Farads, and the bond-wire inductance is approximately 1nH/mm of length [38, p.136]. Bond-wire resistance was neglected as it is typically less than a couple of ohms. The buffers in this design were simulated with 3mm bond-wires, and a PCB load capacitance of 1pF. Alternate high frequency models of the package involve using lossless transmission lines, terminated by a load impedance [39].

Separate output buffers exist for signals at different frequencies. Figure 5.7 shows the schematic of the low frequency buffer, used for signals less than 2MHz, such as the output of the divider and phase/frequency detector. The output buffer is divided into two stages. The input stage is a differential amplifier with a current-mirror load, which amplifies the input signal and has a single-ended output. The output of the first stage is passed to a

Figure 5.6: Package model for a chip-on-board implementation.

standard CMOS inverter, which drives the signal rail-to-rail. Transistors in the first stage are sized to ensure that the peak voltages straddle the switching point of the inverter.

Figure 5.7: Schematic of the low-frequency output buffer.

For signals with a frequency between 2MHz and 100MHz, such as the internal count values of the divider, the buffer shown in Figure 5.8 is used. This buffer reduces the delay of the output stage by tripling the widths of the transistors, providing a higher transient current during switching. However, since the input differential stage cannot drive the increased input capacitance of the output inverter, an intermediate inverter stage is used, equal to the output stage of the low-frequency buffer. Tapered buffer sizes optimize

the overall delay of the circuit by reducing the input-to-output capacitance ratio at each stage [40, 41].

Figure 5.8: Schematic of the medium-frequency output buffer.

At high frequencies, the performance of the CMOS inverter as an output buffer deteriorates because of the large rail-to-rail swings. Also, large transient current spikes increase switching noise which is coupled to other circuitry through the power supply and substrate. Differential current-mode-logic (CML) buffers have been shown to increase the bandwidth of the buffer while reducing switching noise [39]. Figure 5.9 shows the implementation of the high frequency buffer used for *SlowClkOut*, which has a frequency of around 100-200MHz. Fixed resistive loads were used instead of PMOS load transistors since the parasitic capacitance of PMOS transistors would load the output and reduce the bandwidth. Since the current sink transistor is biased by RFN_{Fast} , the buffer uses 3.5mA of current when the fast bias current for AMCML gates is set to $50\mu A$. To reduce pin-count, only one end of the differential signal was taken. As this creates an unbalanced load on the buffer, future versions of the chip would either output the differential voltage

or provide a dummy load on the unused branch. In addition, since the use of fixed resistive loads results in an amplitude-current dependence, future chips would utilize a dedicated current reference for the buffers, instead of using RFN_{Fast} , which is designed to vary with the use of AMCML.

Figure 5.9: Schematic of the high-frequency output buffer.

For RF frequencies, such as those obtained from the VCO, the buffer of Figure 5.9 is insufficient to drive the package model in Figure 5.6 without substantial attenuation of the signal. Since the AMCML gates in the core of the circuit are optimized for power to drive similar logic gates, they are incapable of driving the high input capacitance of a suitably-sized output buffer. Therefore, tapered CML buffers are used as shown in Figure 5.10 [39]. The output of the last CML buffer is passed through a high-current source-follower amplifier which provides a low output impedance, suitable for driving 50-ohm loads [33]. With an AMCML reference current of $50\mu\text{A}$, the output buffer dissipates 21mW. It is interesting to

note that the power dissipation of the output buffers can be significantly greater than that of the core circuit. As in the case of the buffer in Figure 5.9, an improved design would balance the load on the last CML buffer using a dummy source-follower and would use a dedicated current reference.

Figure 5.10: Schematic of the GHz-frequency output buffer.

5.6 CMOS-AMCML Logic Converter

Although on-chip AMCML logic is differential and uses voltage swings of about 350mV, discrete logic devices (and standard equipment outputs) are single-ended and rail-to-rail. To ensure compatibility with off-chip logic and to reduce the number of pins required on the chip, all digital control signals are passed through a CMOS-AMCML logic converter, shown in Figure 5.11. The logic converter is equivalent to an AMCML buffer with a standard CMOS inverter connected to one of its inputs. This topology ensures that the inputs of the AMCML buffer are always connected to the input signal and its logical complement. Since the rail-to-rail differential input of the buffer is significantly higher than the minimum voltage swing required for complete current-steering, the AMCML buffer outputs a differential signal with the appropriate voltage swing, set by RFN_{Slow}

and $RFP1_{slow}$ with the adaptable bias controller.

Figure 5.11: Schematic of the CMOS-AMCML logic converter.

This circuit is also used for low-frequency AC signals, such as the PLL reference frequency. However, this topology is not well-suited to high speed applications as a result of the increased delay of the signal to the negative input of the AMCML buffer, caused by the CMOS inverter.

5.7 AMCML Voltage Swing Monitors

AMCML voltage swing monitors are added to the chip to verify the correct operation of the adaptable bias controllers. Although it is difficult to directly measure RFP without loading the controller and affecting its stability, the inputs to several AMCML gates are fixed to provide a low-level at their outputs. This low-level is then connected to bonding pads on the chip. One monitor gate is used for each of the four adaptable bias controllers used in the circuit. Since there is a direct mapping between the RFP control voltage and the logic low level, the monitors provide an indirect way to observe the behavior of the

bias control loop over different voltage swings and currents.

Chapter 6

Integrated Circuit Test

6.1 Chapter Overview

This chapter discusses the measurement results for the fabricated circuit.

Section 6.2 summarizes the design of a printed circuit board (PCB) used to facilitate testing, and the results of RF board simulations are provided.

Section 6.3 provides measurement results for the chip. This section begins with a discussion of electrostatic discharge (ESD) problems encountered during the early stages of testing. Next, test-setups and measurement results are provided for the AMCML adaptable bias controller, frequency divider, and phase/frequency detector. Discrepancies between measured and simulated results are explained, and suggestions are given for an improved implementation of the chip.

6.2 Printed Circuit Board Design

Testing of the completed chip was facilitated using a custom-designed printed circuit board (PCB) and the chip-on-board packaging technique. The die was mounted to a gold-plated landing pad with conductive silver epoxy and bond-wires with a length of up to 3mm were used to connect all 64 aluminum pads on the chip to designated gold-plated traces on the

PCB. In addition to providing a rigid substrate for the chip, the PCB is responsible for:

- Providing connectivity to test equipment
- Reducing power supply noise from DC power supplies
- Providing 5 adjustable current references to the chip
- Allowing discrete components to be used for the PLL loop filter
- Providing a means to connect the PCB to a PC through an FPGA control board
- Protecting the chip against damage caused by electrostatic discharge

Figure 6.1: Topology of the printed circuit board.

Figure 6.1 shows the topology of the PCB and some of the key connections to the chip (ICFCUMDK). The board has a thickness of 62-mils and uses an FR4 substrate. Both sides of the board are used for signal routing, with the bottom of the PCB providing a solid ground-plane underneath all RF signals. Gold-plated copper conductors are used to facilitate wire-bonding. With the exception of power-supply decoupling capacitors, all components are mounted on the top surface of the PCB. Gold SMA connectors are used for all signals with a frequency higher than 100MHz, and for the PLL reference signal. Momentum was used to simulate the RF performance of the PCB to ensure that cross-talk between RF signals and their adjacent traces was acceptably low. Table 6.1 summarizes the FR4 substrate parameters used in the simulation. Figure 6.2 plots the simulated crosstalk between the external VCO input and its adjacent signals, V_{DD} and $SlowCLK$. Similarly, 6.3 plots the crosstalk between the VCO output and its adjacent signals, V_{DD} and I_{Fast} , which serves as the bias current for the high frequency AMCML gates. With the exception of the coupling between the external VCO input and V_{DD} , which can be as high as -8dB, the worst-case crosstalk over the desired range of operating frequencies is less than -13dB. However, the high crosstalk value with V_{DD} is not a concern since unwanted signals coupled into the power supply are filtered by the decoupling network on the PCB.

Table 6.1: FR4 substrate parameters used by Momentum.

Substrate Parameter	Value
Dielectric constant (ϵ_r)	4.5
Dielectric loss tangent	0.015
Substrate thickness	0.062"
Conductor thickness	0.002"
Conductor conductance	∞

Figure 6.2: Simulated cross-talk between external VCO input (*VCOExtIn*) and adjacent signals.

In conjunction with a PC-based graphical user interface (created by research students), the Altera Stratix 1S40 FPGA board is used to generate the digital control signals for the chip. Since the FPGA board uses 3.3V signalling while the test-chip requires 1.8V, the MC74LVX50 hex buffer is used to convert the logic levels on the PCB. These buffers accept input voltages of up to 7V, while providing a buffered output with a high-level voltage equal to its supply voltage [42], set to 1.8V on the PCB. Figure 6.4 shows a screen capture of the graphical user interface, which is described in detail in [43–45].

Providing a stable, low-noise supply voltage to the chip is one of the fundamental duties of the PCB. The power supply decoupling network shown in Figure 6.5 filters high frequency noise at the input of the PCB, and provides a low impedance path to ground

Figure 6.3: Simulated cross-talk between VCO output (F_{out}) and adjacent signals.

Figure 6.4: Screen capture of the PC-based graphical user interface.

for undesired AC signals. A ferrite chip presents a large series impedance at high frequencies*, while providing a low impedance (less than an ohm) at DC. As a result, noise from the bench-top power supply is attenuated before reaching the PCB power distribution network. An array of capacitors ranging in size from $0.01\mu\text{F}$ to $10\mu\text{F}$ presents a low-impedance path to ground for remaining AC signals. Since the impedance of a capacitor is $1/(j\omega C)$, large capacitors reduce the impedance to ground and improve noise filtering. However, large capacitor values are typically provided in large packages which contribute parasitic inductance. As the frequency increases, the inductor impedance becomes larger. At the self-resonant frequency of the capacitors, the parasitic inductance cancels the capacitance and the network has a low impedance to ground; above this frequency the parasitic inductance dominates, and the capacitor no longer acts to suppress noise. Smaller capacitor values typically require smaller packages with less parasitic inductance and have higher self-resonant frequencies. As a result, using an array of capacitor values ensures a low impedance to ground over a much greater bandwidth than would be possible using a single, large decoupling capacitor [46, pp.263-293]. In addition, it is possible to select the capacitors such that their self-resonant frequencies (with corresponding impedance nulls) are distributed across the range of operating frequencies. Localized $0.1\mu\text{F}$ capacitors are placed underneath all integrated circuits on the PCB to further stabilize the power supply.

The RF output of the chip is designed to be measured using a spectrum analyzer. Since the spectrum analyzer used to test the chip can be damaged by DC power, the PCB includes

*The impedance of the BLM21A102S from Murata is 1000Ω at 100MHz , and greater than 300Ω in the band from 10MHz to 1GHz .

Figure 6.5: Power supply decoupling. All components are manufactured by Murata.

DC blocking capacitors, as shown in Figure 6.6. To prevent attenuation of the output signal, the impedance of the DC blocking network must be small across the desired bandwidth of the signal (400MHz-2.45GHz), requiring a large capacitance value. Large capacitors suffer from low self-resonant frequencies making their use impractical at high frequencies. This problem is alleviated by choosing a small capacitor with a self-resonant frequency at the frequency of interest. However, the resulting solution is narrow-band and is unsuitable for broadband or multi-band applications. The bandwidth of the DC blocking circuit is improved by placing two capacitors with different self-resonant frequencies in parallel. Using measured data from MuRata* in an ADS S-parameter simulation, a 51pF capacitor (GRM1885C1H510JA01) in parallel with a 0.5pF capacitor (GRM1885C1HR50CZ01) was found to yield a low impedance over the frequencies of interest, as shown in Figure 6.7.

Figure 6.6: RF Output Circuit.

*Measured data is obtained by downloading the "Murata Chip S-Parameter & Impedance Library" available at www.murata.com.

Figure 6.7: Impedance of the DC blocking network over the desired operating range.

Figure 6.8 shows the circuitry used on the PCB to generate the adjustable current references used to bias the chip. The LM334Z acts as a three-terminal adjustable current source, with a reference current equal to [47]:

$$I_{REF} = \frac{227 \mu V / ^\circ K}{R_{Set}} \quad (6.2.1)$$

Twelve-turn trimming potentiometers (Bourns 3269W series) implement the variable resistor, R_{Set} , used to adjust the bias current. Table 6.2 summarizes the potentiometers used to generate the various bias currents. A 2-pin header is connected in series with the bias current to allow measurement of the the current with a multimeter. Once the current is set, a jumper is used to provide a path for current to flow into the chip.

The thin gate oxides associated with transistors in a $0.18 \mu m$ CMOS process renders input circuitry susceptible to damage from electrostatic discharge (ESD), which can result in irreversible breakdown of the gate dielectric. A second version of the PCB was created

Figure 6.8: Variable current supply circuitry. The LM334Z is used with a Bourns 3269 potentiometer to form an adjustable current supply.

Table 6.2: Potentiometer sizes used in the bias current circuitry

Bias Current Name	Nominal current	Potentiometer Value	Potentiometer Part Number
I_{Slow}	$7.5\mu A$ - $25\mu A$	$10K\Omega$	3269-W-1-103
I_{Fast}	$25\mu A$ - $70\mu A$	$10K\Omega$	3269-W-1-103
I_{RFPgen}	$11\mu A$	$10K\Omega$	3269-W-1-103
I_{CP}	$15\mu A$	$10K\Omega$	3269-W-1-103
I_{VCO}	$1mA$	100Ω	3269-W-1-101

that incorporates ESD protection on all DC and low-frequency inputs. Figure 6.9 shows a schematic of the ESD protection circuitry. Reverse-biased diodes are used to shunt charge from an ESD strike to the supply-rails and away from the chip [41, p.69]. During normal operation, the diodes are reverse biased and present a low capacitance (less than 3pF) to the protected signal. However, the high voltages associated with an ESD strike forward-bias the diodes and rapidly re-direct the damaging charge to the PCB power supply network. An additional zener diode is added between the supply and ground to facilitate the dissipation of charge to the ground plane. The clamp diodes are implemented using the NUP4301MR6T1 diode array from ON Semiconductor, which simultaneously protects four data lines [48]. The zener diode is implemented using the DS9502 from Dallas Semiconductor [49].

Figure 6.9: ESD Protection Circuitry.

Once the die is affixed to the PCB and wire-bonded to the designated traces, solder paste is used to affix all surface-mount components to the top of the board. A hot-plate is used to heat the board to 200°C for approximately one minute, reflowing the solder. The remaining surface mount components on the bottom of the board, and all through-hole

components, are soldered by hand. Figure 6.10 shows a photograph of the completed PCB with all of the signals labeled. The pin-out of the FPGA connection header is shown in Figure 6.11, and a description of all input/output signals is provided in Table 6.3. Appendix B provides the bill of materials for the PCB. Pin headers are not listed as they are readily available from many suppliers.

Figure 6.10: Photograph of the completed PCB.

Table 6.3: PCB connection summary

Signal Name	Description
F_{out}	Frequency synthesizer output
F_{Ref}	Synthesizer reference frequency
VCO_{ExtIn}	External VCO input
$SlowCLK$	Dual-modulus prescaler output
V_{DD}	Power supply voltage (1.8V nominal)
I_{RFPgen}	Adaptable bias controller bias current
I_{Slow}	Low-current AMCML bias current
I_{Fast}	High-current AMCML bias current
I_{CP}	Charge pump bias current
I_{VCO}	LC-VCO AMCML bias current
CP_{Out}	Charge pump output
VCO_{Ctl}	VCO control voltage
$ModulusControl$	Sets modulus of prescaler
$UP, DOWN$	Phase/frequency detector outputs
$V_{low,mon}[1..4]$	AMCML low level monitors
$CNT[0..6]$	PC/SC count value (selected by $CNTMuxCtl$)
$CNTMuxCtl$	Selects PC/SC count for monitoring by $CNT[0..6]$
$P[0..6]$	Program count value, P
$S[0..5]$	Swallow count value, S
$VCOInExt$	Selects internal/external VCO
VCO_{ab}	Selects whether LC-VCO or ring oscillator is active
$Reset$	Resets all AMCML flip-flops
$V_{oLAdjust}$	AMCML logic low level

Figure 6.11: Pin-out of the FPGA connection header. NC indicates that the pin is not connected.

6.3 Measurement Results

6.3.1 Electrostatic Discharge Problems

During initial testing, four chips were either completely non-functional, or became non-functional within a period ranging from minutes to hours. Investigation into the failures indicated that in all of the three input current mirrors which used metal-insulator-metal (MIM) capacitors to filter noise (I_{Slow} , I_{Fast} , and I_{RFPgen}), the input voltage was approximately equal to zero volts when the on-board current sources were used to set the input current. However, input current mirrors associated with the circuitry designed in [37], such as I_{CP} and I_{VCO} , did not use MIM capacitors and remained functional. To further characterize this problem, the test setup shown in Figure 6.12 was used to characterize all of the damaged current mirrors. The on-board current sources were disconnected from the chip by removing their associated jumpers, and a DC power supply was used to sweep the input voltage, V_{Test} . For each value of V_{Test} , the input current, I_{Test} , was recorded by

placing a Keithley 2010 multimeter in series with the input. The resulting measurements are plotted with the simulated results in Figure 6.13

Figure 6.12: Measurement setup to confirm ESD damage to current mirrors.

Figure 6.13 indicates that for a functional current mirror, the input current should be negligible for input voltages less than the NMOS threshold voltage of 0.45V since the diode-connected transistor is turned-off. For higher input voltages, the current closely resembles the square-law characteristic of a transistor in saturation. However, measured results of the damaged current mirror indicate there is current for all positive input voltages resulting in measured currents that are drastically higher than expected. It is interesting to note that for voltages less than a threshold voltage, the current-voltage relationship is linear. In conjunction with the observations indicating that damage only seemed to occur to current mirrors containing a MIM capacitor, it was theorized that electrostatic discharge (ESD) damaged the thin dielectric of the capacitor, essentially creating a resistor to ground. Provided that the NMOS transistors were undamaged, this would result in the

total measured current being equal to the desired current through the diode-connected transistor in addition to the current through the “resistor”, equal to V_{Test}/R . The value of R could be determined using a linear approximation of the measured current in Figure 6.13 for small input voltages.

Figure 6.13: Current vs. voltage for an ESD damaged current mirror. The simulated current for a functional current mirror is also shown.

Figure 6.14 plots the measured current with the theoretical resistor current removed. As in the simulated curve, the adjusted input current is negligible for input voltages less than the threshold voltage of the transistor. However, the adjusted currents are still dramatically higher than expected. Simulations using the TSMC provided process corners of the transistors (SS and FF models) did not account for this large difference. These results suggest that the transistors in the current mirror were also damaged.

Based on the preceding measurements and discussion, it was concluded that while the

Figure 6.14: Measured current with linear portion removed. The simulated current for a functional current mirror is also shown.

MIM capacitor seemed to render the current mirrors more susceptible to damage caused by ESD, the resulting damage was not confined to the capacitor itself but included the input transistors. Although the exact reason for this increased susceptibility is unknown, it is possibly related to the ability of the capacitor to store the excess charge associated with an ESD event. This charge storage would prolong the period of time for which the gates of the transistors are subjected to damaging oxide breakdown voltages. As a result of these conclusions, a second version of the PCB was designed and manufactured which included ESD protection circuitry as described in Section 6.2. No ESD problems were observed using the modified boards. The manufactured chip did not include ESD protection diodes due to size constraints and incomplete models for the CMC-provided ESD protection circuitry.

However, the problems encountered with ESD highlight the importance of including on-chip protection from the outset.

6.3.2 Adaptable Bias Controller

Figure 6.15 depicts the setup used to test the AMCML adaptable bias controllers. The AMCML swing was set on the PCB using a potentiometer, while the AMCML bias currents, I_{Slow} and I_{Fast} , were set using the adjustable current sources described in Section 6.2. An Agilent Infiniium 54832D oscilloscope was used to measure the outputs of the AMCML voltage swing monitors. $V_{Low,mon1}$ and $V_{Low,mon2}$ correspond to the low current single-level and multi-level bias controllers, while $V_{Low,mon3}$ and $V_{Low,mon4}$ correspond to the high-current versions.

Figure 6.15: Adaptable bias controller measurement setup.

To determine the tracking behavior of the bias controllers, I_{Slow} and I_{Fast} were swept over their typical operating ranges (listed in Table 6.2) for a desired low level of 1.45V and the measured low levels in the monitors were recorded. Figure 6.16 plots the results for

the low current version of the controllers, while Figure 6.17 plots the results for the high current version. For the low current version, the worst case variation was 50mV as I_{Slow} was varied from $8\mu\text{A}$ to $30\mu\text{A}$. In the case of the high current version, the tracking results are even better, with a variation of less than 35mV for a current variation from $25\mu\text{A}$ to $70\mu\text{A}$ (ignoring the anomaly at $60\mu\text{A}$). This anomaly is likely the result of the low phase margin around this point, as described in Section 3.4.2.

Figure 6.16: Measured voltages at the output of the AMCML swing monitors with a desired low level of 1.45V (low current version).

The measurement results indicate a slight difference between the desired low level set on the PCB and the measured low levels in the voltage swing monitors. This error may be created by a combination of the mismatch between the PMOS load transistors in the bias controller with those in the biased AMCML gates, in addition to the input offset voltage inherent to the operational amplifiers. Simulations indicated that a 20% variation in the

op-amp source degeneration resistors can account for 50mV of offset error, while a 10% mismatch* in the width of the PMOS loads can account for close to 30mV.

Figure 6.17: Measured voltages at the output of the AMCML swing monitors with a desired low level of 1.45V (high current version).

Although process variations are likely, it may be possible to reduce the offset error by designing an operational amplifier that is more immune to mismatch. One possible design change would be to eliminate the use of source degeneration resistors and to improve stability using transistor sizing to lower the gain instead. Replacing the active load in the output stage of the op-amp with a resistor could also lower the gain. Using larger transistors would reduce the gain by lowering amplifier output impedance, while decreasing susceptibility of the circuit to process variations. In addition, the sizing of the active PMOS loads in the AMCML gates could be re-visited to minimize sensitivity of the voltage swing

*For minimum size, low-current transistors, it is shown in [50] that MOSFET mismatch can exceed 10%.

to errors in voltage or transistor sizing, as discussed in Section 3.3.2.

6.3.3 Frequency Divider Test

The frequency divider was tested using the setup shown in Figure 6.18. The AMCML bias currents and voltage swing were set on the PCB using their corresponding potentiometers. An Altera Stratix 1S40 FPGA board was used in conjunction with the PC-based graphical user interface (GUI) discussed in Section 6.2 to generate all digital control signals for the chip, including the desired values for the program counter and swallow counter. Using the GUI, the VCO multiplexer was set to allow the use of an external signal generator. A high-speed, mixed-signal oscilloscope was used to simultaneously measure the output of the dual-modulus prescaler (*SlowClk*), the program counter (F_{Div}), and the swallow counter (*ModulusControl*).

Figure 6.18: Frequency divider measurement setup.

It was discovered during testing that the AMCML voltage swing needed to be increased in order to obtain a useable signal at the output of the prescaler. Although the circuit was initially designed to operate with a logic low level of 1.45V, this was reduced to 1.0V during testing. This problem was reproduced in simulation by artificially adding a 10% mismatch in the active PMOS loads. Since this mismatch can result in an effective voltage swing reduction in one of the two logic gate outputs, decreasing the low-level compensates for this reduction and ensures complete current switching in the prescaler. In [50], it is shown that mismatch between minimum size transistors with low currents can exceed 10%. Smaller mismatches both in the current-mirrors and in the loads can also create this problem.

Figure 6.19: Measured output of the prescaler with an input frequency of 400MHz and *ModulusControl* = 1.8V.

Using the increased voltage swing, the prescaler successfully divides by 16 when the *ModulusControl* signal is low, and by 15 when *ModulusControl* is high. Figure 6.19 shows the measured output of the prescaler for an input frequency of 400MHz and a modulus of 15, while Figure 6.20 shows the results with an input frequency of 650MHz. Figure 6.21

plots the maximum operating frequency of the prescaler as a function of AMCML bias current, while Figure 6.22 plots the power savings relative to the power required for operation at 600MHz. As predicted by (2.2.11), higher operating frequencies required higher bias currents. Unfortunately, the prescaler did not function with input frequencies above 700MHz. This reduction in operating frequency can be explained by the larger required AMCML voltage swing. The larger swing increases the delay of the logic gates by means of equation (2.2.11) and lowers the maximum frequency of operation. Transient simulations in Cadence using the increased swing and the slow transistor models confirm the substantial reduction in operating frequency from the design target of 2.4GHz. Despite the lower than expected operating frequencies, these results confirm the usefulness of AMCML in adjusting the power dissipation based on the required frequency of operation. In addition, the measurements in Section 6.3.2 demonstrate the successful operation of the bias controllers over the measured range of AMCML bias current.

Figure 6.20: Measured output of the prescaler with an input frequency of 650MHz and *ModulusControl* = 1.8V.

Figure 6.21: Prescaler operating frequency vs. AMCML bias current.

Figure 6.22: Prescaler power savings relative to the power required for operation at 600MHz.

The measured results also demonstrate significant feedthrough of the input signal, which becomes worse at higher frequencies and nearly dominates at 650MHz. Transient simulations of each of the prescaler sub-circuits traced the source of this feedthrough to capacitive coupling (through C_{GD} of the transistors) in the AMCML latches. Since the parasitic gate-to-drain capacitance is proportional to transistor size, feedthrough could be reduced using smaller sizes in the differential pairs. Unfortunately, since this would also require a larger swing to ensure current switching in the logic gates, more work needs to be done to determine effective methods of reducing the feedthrough.

Figure 6.23: Measured output of the frequency divider (200KHz) with an input frequency of 200MHz and a division ratio of 1000.

Since the remainder of the frequency divider is clocked by the output of the prescaler, the maximum operating frequency of the prescaler defines that of the complete divider. The measured output of the frequency divider with an input frequency of 200MHz and a division ratio of 1000 is shown in Figure 6.23. Figure 6.24 shows the measured *ModulusControl*

signal under the same operating conditions. As expected, the frequency of both signals is equal to 200KHz. In addition, it is evident by comparing Figures 6.23 and 6.24 that *ModulusControl* is reset to zero by the divider output pulses. The divider was successfully tested with large and small division ratios and input frequencies up to 650MHz.

Figure 6.24: Measured *ModulusControl* signal with an input frequency of 200MHz and a division ratio of 1000.

6.3.4 Phase/Frequency Detector

The phase/frequency detector (PFD) was tested using the configuration in Figure 6.25. The configuration is identical to that of the divider, with the addition of the Agilent 80MHz signal generator, which is used to provide F_{Ref} to the chip. In addition, different signals are monitored by the oscilloscope, as shown in Figure 6.25.

To test the operation of the PFD, the frequency divider was set to operate with an

Figure 6.25: Phase/frequency detector measurement setup.

input frequency of 200MHz and a division ratio of 1000. This resulted in a divider output frequency of 200KHz. F_{Ref} was varied from 195KHz to 205KHz and the *UP* and *DOWN* signals were monitored using an oscilloscope. As expected, when F_{Ref} was less than 200KHz, pulses appeared on the *DOWN* signal, while pulses appeared on the *UP* signal when F_{Ref} was greater than 200KHz. When pulses occurred on the *UP* signal, *DOWN* remained low. The reverse was true when pulses occurred on the *DOWN* signal. The brief reset pulses described in Section 4.3 could not be observed on the oscilloscope due to their inability to drive the bond-pad capacitance, however, their existence was confirmed based on the successful operation of the circuit. Figure 6.26 plots the measured *DOWN* signal with F_{Ref} set to 195KHz. As described in Section 4.3 and simulated in Figure 4.15, the pulses gradually become larger until the duty cycle of the signal approaches 100%. At this point, the pulses become narrow once again and the cycle is repeated.

Figure 6.26: Measured *DOWN* signal with $F_{Ref}=195\text{KHz}$ and $F_{Div}=200\text{KHz}$.

Successful operation of the circuit according to state diagram in Figure 4.12 can be inferred using the measured results in Figure 6.27 and Figure 6.28. As shown in Figure 6.27, when F_{Ref} is less than F_{Div} , the *DOWN* signal is asserted on the rising edges of the divider output signal and is reset on the rising edges of the reference. When F_{Ref} is greater than F_{Div} , as shown in Figure 6.28, the *UP* signal is asserted on the rising edges of the reference and reset on the rising edges of the divider output signal. This behavior confirms the existence of the brief reset pulses on the alternate signals, despite the inability to see them on the oscilloscope.

6.4 Chapter Summary

This chapter began with a description of the design of a custom printed circuit board (PCB) used to test the fabricated chip. Measurement results for the first tested chips were presented, indicating ESD damage to current-mirror inputs which contain a MIM capacitor

Figure 6.27: Measured PFD waveforms with $F_{Ref}=195\text{KHz}$ and $F_{Div}=200\text{KHz}$. The arrows indicate the effect of edges on F_{Ref} and F_{Div} on the $DOWN$ signal.

Figure 6.28: Measured PFD waveforms with $F_{Ref}=205\text{KHz}$ and $F_{Div}=200\text{KHz}$. The arrows indicate the effect of edges on F_{Ref} and F_{Div} on the UP signal.

for noise filtering. These results were used as justification for a second version of the PCB which included on-board ESD protection diodes.

The AMCML adaptable bias controller was successfully tested and the tracking behavior over a wide range of currents was demonstrated. Error offsets were explained in terms of process variations and mismatches in the the fabricated chip. The dual-modulus prescaler and complete frequency divider were successfully tested at frequencies up to 650MHz. The lower than expected operating frequency was related to an increased AMCML voltage swing required as a result of on-chip process variations. A discussion of clock feed-through in the prescaler was also presented. A plot of power savings as a function of operating frequency was presented which demonstrated the applicability of AMCML for use in a multi-band divider.

Finally, the phase/frequency detector was tested. The PFD was shown to successfully implement its state diagram presented in Chapter 4.

In spite of the lower operating frequency of the divider, the measurements presented in this chapter confirm the successful operation of the AMCML bias controllers and the use of a complete AMCML library in a fully-functional frequency divider.

Chapter 7

Conclusions

7.1 Contributions to Research

In this thesis, Adaptable MOS Current Mode Logic (AMCML) was explored as an alternative to traditional MCML. AMCML alleviates the problem of increased static power dissipation and the requirement to maintain large libraries of gates for various ranges of operating frequencies. A single circuit built using AMCML can be adjusted in real-time to dissipate only the power required to operate at the needed frequency.

A library of AMCML gates was designed in this thesis and major design considerations were discussed. An adaptable bias controller was also designed that allows the drive current and voltage swing of AMCML gates to be independently controlled. Stability of the bias controller was discussed in depth. The fabricated bias controller was tested and the AMCML voltage swing was found to exhibit an error of less than 50mV over a wide range of AMCML bias currents. These voltage errors resulted from process variations and mismatch on the fabricated chip.

The AMCML library was used to construct a pulse-swallow frequency divider and a phase/frequency detector which was designed to operate at frequencies up to 2.45GHz.

Simulation results indicated an 82% power savings at 400MHz relative to the power required for operation at the maximum frequency. The divider and phase/frequency detector were tested and found to be functional up to 650MHz. The discrepancy between the simulated and measured frequencies of operation was related to process variations and mismatch on the fabricated chip, which necessitated the use of a larger AMCML voltage swing. In spite of the reduced frequency, the measured chip demonstrates the ability of AMCML to trade power for speed in a multi-band frequency divider. In addition, the use of AMCML allowed the current to be varied based on the frequency of operation, confirming the usefulness of AMCML in multi-band transceivers.

7.2 Future Work

More work is needed to improve on the design of the chip based on the lessons learned during measurements.

The primary shortcoming of this implementation is the lower than expected operating frequency of the divider. Since a preliminary investigation of this problem has suggested process variations are the root cause of this problem, more work needs to be done to confirm this theory and to explore new design changes that could be taken to improve the immunity of the circuit to these variations. Using larger transistor sizes in the AMCML gates would reduce the sensitivity of the design to changes and would also make it easier to employ common-centroid matching techniques in the layout to ensure that the active PMOS loads are well matched. However, this would invariably affect the performance of the logic gate itself. To facilitate this investigation, it would be useful to build a test chip that contained simple chains of different versions of AMCML gates. In addition, since the prescaler was

found to be the bottleneck for the design, the test chip could ignore the remaining low frequency circuitry in the interests of reducing silicon area and ensuring that system-level interface issues do not interfere with the testing of the core circuitry.

Since test results also indicated high levels of clock feed-through in the latches, more work needs to be done to investigate ways of improving the latch design. Preliminary work has indicated that this feed-through is the result of capacitive coupling from the gate to drain of the transistors and can be reduced by using smaller device sizes. However, since this conflicts with the need to use larger transistors to improve immunity to process variations, this may prove to be a difficult task.

Next, the operational amplifier in the adaptable bias controllers should be redesigned to minimize the voltage swing error caused by process variations and mismatch. Once again, the possibility of using larger transistor sizes and improved layout techniques should be explored.

In interfacing all of the core components to each other and to the output of the chip, various buffers were used which utilized fixed resistive loads in the interest of improving bandwidth. Unfortunately, a design oversight resulted in these buffers sharing a current reference with the AMCML gates in the circuit. This design choice made it difficult to distinguish between changes to the operation of the core circuit with the buffers as the AMCML bias current was varied. As a result, future chips should utilize independently controlled current references for the buffers.

Finally, since this chip implementation used digital multiplexors to select the VCO, to pass the desired count value to the output pins, and in the counters themselves, work can be done to improve the design of the multiplexors. To reduce the number of logic

Figure 7.1: Circuit implementation the proposed AMCML multiplexor.

gates in the AMCML library, two AND gates and one OR gate were used to implement each multiplexor. However, it is possible with AMCML to create a single logic gate which realizes the function of a multiplexor directly, as shown in Figure 7.1. This topology has the same level of complexity as an XOR gate and uses only one tail current. As a result, future implementations of the circuit should be modified to use the new multiplexor in the interests of reducing power dissipation and silicon area.

Appendix A

Derivation of Operational Amplifier Transfer Function

In this chapter, the transfer function of the op-amp used in the AMCML adaptable bias controllers is derived. Figure A.1 shows the op-amp implementation used in this thesis.

Figure A.1: Implementation of the operational amplifier used in the adaptable bias controller.

To simplify the derivation of the op-amp transfer function, $A(j\omega)$, it is divided into two stages. The first stage, shown in Figure A.2 is a differential input, single-ended output gain stage, while the second stage, shown in Figure A.3 is a common source gain stage. The

compensation capacitor, C_c , and lead compensation transistor, M_8 , connect the outputs of the two stages and are addressed later in this section.

Figure A.2: Differential input stage of the operational amplifier.

Figure A.3: Output gain stage of the operational amplifier.

The low frequency gain of the first stage is derived using the small-signal model in Figure A.4. In this model, M_1 and M_2 are represented with the T-model of the transistor, the diode connected transistor M_3 is replaced with its equivalent resistance ($r_{ds3} || (1/g_{m3})$), and the hybrid- π model is used for M_4 . To simplify the analysis, the current source in

Figure A.2 is assumed to have an infinite output impedance and the body effect of M_1 and M_2 is neglected. The effect of finite output impedance of the current source is to create a non-zero common-mode gain which reduces common-mode noise immunity in the op-amp. Neglecting the body effect can be justified in this application since its primary effect is to lower the gain of the op-amp, further improving the stability of the loop. As a result, if the expressions derived ignoring the body effect imply stability, greater stability is ensured in reality. In addition, the purpose of the expressions in this section are not to accurately predict the precise phase margin of the loop, but to identify the effects of load capacitance, the source degeneration resistors, and AMCML bias current on stability. Temporarily neglecting r_{ds1} and r_{ds2} and defining $v_{in} = v^+ - v^-$:

$$i_1 = -i_2 = \frac{-v_{in}}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}} + 2R} \quad (\text{A.0.1})$$

Figure A.4: Small signal model of the differential input stage used for calculation of the low-frequency gain.

Since M_1 and M_2 are matched, $g_{m1} = g_{m2}$ and (A.0.1) reduces to:

$$i_1 = -i_2 = \frac{-v_{in}}{\frac{2}{g_{m1}} + 2R} \quad (\text{A.0.2})$$

Due to the current mirror load formed by M_3 and M_4 , the total output current is given by:

$$i_{out} = i_i + (-i_2) = 2i_1 = \frac{-g_{m1}v_{in}}{1 + g_{m1}R} \quad (\text{A.0.3})$$

The output voltage can now be calculated using the product of the output current, i_{out} , and the output impedance, r_{out} . Calculation of the output impedance is facilitated using the small signal model in Figure A.5. This model is based on Figure A.4, with the exception being the use of the hybrid- π model for M_2 . In addition, r_{ds1} is neglected as it is much larger than $1/g_{m1}$, and $1/g_{m1}$ is neglected since it appears in series with $2R$, which is assumed to be significantly larger using the sizes in the op-amp.

Figure A.5: Small signal model of the differential input stage used for calculation of the output impedance.

Using nodal analysis at the output and at v_x , the output impedance is found to be:

$$r_{out} = r_{ds4} || [r_{ds2} (1 + 2g_{m1}R)] \quad (\text{A.0.4})$$

Multiplying (A.0.3) with (A.0.4) and dividing by v_{in} , the low frequency gain of the first

stage is found to be:

$$A_{v1} = \frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{(1 + g_{m1}R)} [r_{ds4} || r_{ds2} (1 + 2g_{m1}R)] \quad (A.0.5)$$

Equation (A.0.5) makes it apparent that the source degeneration resistors, R , lower the gain of the op-amp, improving the stability of the overall loop by moving the gain crossover to a lower frequency. The second stage of the op-amp, shown in Figure A.3, is simply a common-source amplifier and has a gain given by [33, p.129]:

$$A_{v2} = -g_{m7} (r_{ds6} || r_{ds7}) \quad (A.0.6)$$

The low frequency gain of the complete op-amp can now be written as *:

$$A_v = A_{v1}A_{v2} = \frac{g_{m1}g_{m7}}{(1 + g_{m1}R)} [r_{ds4} || r_{ds2} (1 + 2g_{m1}R)] (r_{ds6} || r_{ds7}) \quad (A.0.7)$$

Calculation of the frequency response of the op-amp is aided using the small signal model in Figure A.6. In this model, R_1 and R_2 represent the output resistance of the first and second stage while C_1 and C_2 represent the total capacitance seen at the output of each stage. The outputs of the two stages are connected with the compensation network formed by C_c in series with R_Z . R_Z models the drain-source resistance of M_8 , which is biased in the triode region.

The components in the model can be summarized as:

$$\begin{aligned} R_1 &= r_{ds4} || [r_{ds2} (1 + 2g_{m1}R)] \\ C_1 &= C_{db2} + C_{db4} + C_{gs7} \\ R_2 &= r_{ds6} || r_{ds7} \\ C_2 &= C_{db7} + C_{db6} + C_L \approx C_L \\ R_Z &= r_{ds8} = \frac{1}{\mu_p C_{ox} (\frac{W}{L}) (V_{SG} - |V_{tp}|)} \end{aligned} \quad (A.0.8)$$

*Multiplying the gains of the two stages is only valid if the input of the second stage does not load the output of the first stage. Since the input to the second stage is capacitive, this expression is valid at low frequencies.

Figure A.6: Equivalent small signal model of the two stage operational amplifier.

The load capacitance of the output stage, C_L , is comprised of the combined parasitic capacitance of all PMOS loads being controlled by the bias controllers in addition to the interconnect capacitance of the bias distribution network. As a result, C_L varies based on the size of the circuit being driven by the bias controller and, is significantly larger than the parasitic capacitances in the output stage of the op-amp. Therefore, it is safe to neglect these capacitances in the determination of the pole locations since C_c and C_L are responsible for the dominant poles in the frequency response. By design, C_c is always much larger than the parasitic capacitors (otherwise it is not effective at creating a dominant pole), and C_L is always significantly larger than the parasitic capacitors if the bias controller is used to drive more than a couple of logic gates.

Equations (A.0.9) and (A.0.10) give the nodal equations at v_1 and v_{out} which are used to compute the transfer function of the op-amp.

$$\frac{-g_{m1}v_{in}}{1 + g_{m1}R} + v_1 \left(\frac{1}{R_1} + sC_1 \right) + \frac{v_1 - v_{out}}{\frac{1}{sC_c} + R_Z} = 0 \quad (\text{A.0.9})$$

$$\frac{v_1 - v_{out}}{\frac{1}{sC_c} + R_Z} - g_{m7}v_1 - v_{out} \left(\frac{1}{R_2} + sC_2 \right) = 0 \quad (\text{A.0.10})$$

Eliminating v_1 in (A.0.9) and (A.0.10) and solving for v_{out}/v_{in} , the transfer function of the op-amp is obtained:

$$A(s) = \frac{v_{out}}{v_{in}} = \frac{-A_v \left(1 + s \left(R_Z C_c - \frac{C_c}{g_{m7}} \right) \right)}{a + bs + cs^2 + ds^3} \quad (\text{A.0.11})$$

where

$$\begin{aligned}
 A_v &= \frac{g_{m1}g_{m7}R_1R_2}{1+g_{m1}R} \\
 a &= 1 \\
 b &= C_c(R_Z + g_{m7}R_1R_2 + R_1 + R_2) + R_1C_1 + R_2C_2 \\
 c &= C_c(R_1R_ZC_1 + R_2R_ZC_2 + R_1R_2C_1 + R_1R_2C_2) + R_1R_2C_1C_2 \\
 d &= R_1R_2R_ZC_1C_2C_c
 \end{aligned} \tag{A.0.12}$$

As seen in (A.0.11), the transfer function has one zero and three poles. However, the third pole exists at a frequency that is much higher than the first two and can be ignored [33, p.243]. This assumption should always hold in a practical bias controller since C_c is sized so that it determines the dominant pole, and since C_L is always much larger than the parasitic capacitances when the biased circuit contains more than a couple of logic gates. As a result, the transfer function can be written as:

$$A(s) = -A_v \frac{(1 + s/\omega_z)}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})} \tag{A.0.13}$$

Comparing (A.0.11) and (A.0.13) the location of the zero is given by (A.0.14) and can be eliminated by sizing M_8 such that $R_Z = 1/g_{m7}$.

$$\omega_z = \frac{-1}{C_c \left(R_Z - \frac{1}{g_{m7}} \right)} \tag{A.0.14}$$

Assuming that the poles are widely separated, the denominator can be written as [33, p.242]:

$$\left(1 + \frac{s}{\omega_{p1}} \right) \left(1 + \frac{s}{\omega_{p2}} \right) \approx 1 + \frac{s}{\omega_{p1}} + \frac{s^2}{\omega_{p1}\omega_{p2}} \tag{A.0.15}$$

The poles can now be found by equating (A.0.15) to the denominator in (A.0.11) and solving for the pole locations. Therefore,

$$\begin{aligned}
 \omega_{p1} &= \frac{1}{b} = \frac{1}{C_c(R_Z + g_{m7}R_1R_2 + R_1 + R_2) + R_1C_1 + R_2C_2} \\
 \omega_{p1} &\approx \frac{1}{g_{m7}R_1R_2C_c}
 \end{aligned} \tag{A.0.16}$$

and

$$\begin{aligned}
 \omega_{p2} &= \frac{1}{\omega_{p1}} = \frac{C_c(R_Z + g_{m7}R_1R_2 + R_1 + R_2) + R_1C_1 + R_2C_2}{C_c(R_1R_ZC_1 + R_2R_ZC_2 + R_1R_2C_1 + R_1R_2C_2) + R_1R_2C_1C_2} \\
 \omega_{p2} &\approx \frac{g_{m7}R_1R_2C_c}{R_1R_2C_2C_c + R_1R_2C_1C_2 + R_1R_2C_1C_c} \approx \frac{g_{m7}C_c}{C_c(C_1 + C_2) + C_1C_2} \\
 \omega_{p2} &\approx \frac{g_{m7}C_c}{C_2(C_1 + C_c)} \approx \frac{g_{m7}C_c}{C_2C_c} \\
 \omega_{p2} &\approx \frac{g_{m7}}{C_L}
 \end{aligned} \tag{A.0.17}$$

Appendix B

Printed Circuit Board Bill of Materials

Table B.1: Bill of materials for the printed circuit board.

Quantity	Description	Manufacturer	Part Number
2	10 μ F Tantalum Capacitor (3528)	Kemet	T491B106K010AS
21	0.1 μ F SMT Capacitor (0603)	MuRata	GRM188R71C104KA01D
2	0.01 μ F SMT Capacitor (0603)	MuRata	GRM188R71H103KA01D
1	0.5pF SMT Capacitor (0603)	MuRata	GRM1885C1HR50CZ01
1	51pF SMT Capacitor (0603)	MuRata	GRM1885C1H510JA01
4	SMA Straight Jack Receptacle	Johnson	142-0701-201
1	1000 Ω Ferrite Chip	MuRata	BLM21AG102SN1D
1	100 Ω SMT Resistor (0603)	Panasonic-ECG	ERJ-3EKF1000V
7	0.1 Ω SMT Resistor (0603)	Panasonic-ECG	ERJ-3RSFR10V
5	10K Ω Potentiometer	Bourns	3269-W-1-103
1	100 Ω Potentiometer	Bourns	3269-W-1-101
3	Hex Buffer	ON Semi	MC74LVX50D
5	Current Source	National Semi	LM334Z
1	ESD Protection Diode	Maxim-Dallas	DS9502P
6	ESD Protection Diode Array	ON Semi	NUP4301MR6T1

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