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Design and Optimization of
MOS Current-Mode Logic Circuits
Using Mathematical Programming

By

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A thesis submitted to the Faculty of Graduate Studies and Research

in partial fulfillment of the requirements for the degree of

Master of Applied Science

Department of Electronics

Carleton University

Ottawa, Ontario, Canada

June 2004

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Abstract

MOS Current-Mode Logic (MCML) is an appealing design style for high-speed applications. This thesis addresses the practical issues in the design of high-performance MCML circuits. In gate-level analysis, the emphasis is on MCML universal gate, which has higher design complexity compared to other gates implemented in this logic style. We present a design and optimization methodology for high-speed MCML universal gate topologies, and applied it to the standard and two modified topologies of universal logic gates that are proposed in this thesis. Implementation of those universal gates in a standard $0.13\ \mu m$ CMOS process shows that the modified topologies improve the speed by 25% to 30% over that of the standard one, while dissipating the same amount of power. The target frequency for this implementation is 10 GHz range.

We also introduce an All-MUX MCML circuit design technique. The only primitive logic gate in this circuit design technique is the standard MCML MUX with fully differential and symmetrical structure.

The major contribution of this work, however, is a mathematical programming technique for design and optimization of MCML circuits. The technique is used to satisfy a variety of design goals such as minimum delay and minimum power-delay product. It also provides an acceptable estimation for various design figures. A comparison with schematic-level simulation shows that our predictions are valid with maximum error of 15%. We use this technique to design different versions of MCML universal gates for minimum delay and minimum power-delay product (PDP). A standard MCML four-bit ripple-carry adder (RCA) is also implemented with targeting minimum delay. All these designs are implemented in a standard $0.18\ \mu m$ CMOS technology. Delay and PDP of the MCML RCA is one third and a quarter of those in the conventional CMOS RCA at 1.5 GHz, respectively. The power dissipation of the MCML RCA is also 22.5% less than that of the CMOS RCA at 1.5 GHz. The total layout area of MCML RCA is $3733.3\ \mu m^2$.

Acknowledgements

At the end of my M.A.Sc. program, I would like to thank all those people, who have made this work possible. Specially, I would like to extend my sincere gratitude to my supervisor, Prof. Maitham Shams, for his meticulous guidance, support and great patience. I appreciate his valuable comments on my papers and his great influence to my work. I wish him all the best in life.

My thanks are also due to my dear friend, Mr. Saied Hemati, for his outstanding advice during this work.

Finally, I would like to express my deepest gratitude for the constant support, understanding and love that I received from my parents during the past years.

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List of Symbols and Abbreviations

Nomenclature

V_{dd}	Power supply
C_L	Load capacitance
ΔV	Voltage swing
V_{th}	Threshold voltage for NMOS
V_{thp}	Threshold voltage for PMOS
η	A criterion for DC-level difference
ΔV_{p-p}	Peak-peak voltage swing
V_{dsat}	Saturation voltage
W_s	Transistor width for the tail NMOS
L_s	Transistor length for the tail NMOS
g_m	Transconductance of MOSFET
W_l	Transistor width for the PMOS pair
L_l	Transistor length for the PMOS pair
V_M	Switching threshold voltage
V_{ss}	Ground voltage
t_r	Rise time
t_f	Fall time
L_{min}	Minimum channel length
t_p	Propagation delay
t_{pp}	Theoretical propagation delay
t'_p	post-layout propagation delay
C_{gd}	Gate to drain capacitance
C_{db}	Drain to bulk capacitance

C_{gs}	Gate to source capacitance
C_{sb}	Source to bulk capacitance
C_{dg}	Drain to gate capacitance
C_g	Overall gate-oxide capacitance
C_{os}	Gate-source overlap capacitance
C_{od}	Gate-drain overlap capacitance
C_{ox}	Thin-oxide capacitance per unit area
C_{gso}	Gate to source overlap capacitance per unit of gate width
C_{gdo}	Gate to drain overlap capacitance per unit of gate width
C_j	Zero-bias depletion-layer capaci- tance per unit area
C_{jsw}	Zero-bias depletion-layer capaci- tance per unit length of diffusion perimeter
i_{DS}	Drain-source current
V_{BEON}	Base-emitter voltage
v_{GS}	Gate-source voltage
v_{DS}	Drain-source voltage
v_{SB}	Source-bulk voltage
V_{odc}	Output DC voltage
h_s	Half the voltage swing
PDP_p	Theoretical PDP
D	Delay
f	Switching frequency
I	DC bias current
L	transistor length
P	Power dissipation

Q	Electric charge on capacitance
R	Pull-up resistor
VRP	Voltage reference for the PMOS pair
VRS	Reference voltage for the tail NMOS
W	Transistor width
z	Length of drain (source)

Abbreviations

AC	Alternating Current
BDD	Binary Decision Diagram
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
CSL	Current Steering Logic
DC	Direct Current
diff-pair	differential pair
DyCML	Dynamic Current-Mode Logic
ECL	Emitter Coupled Logic
MCML	MOS Current-Mode Logic
min.	minimum
NMOS	N-channel MOSFET
PDP	Power-Delay Product
PMOS	P-channel MOSFET
RCA	Ripple-Carry Adder
SR	Slew Rate
univ.	universal
VCO	Voltage Controlled Oscillator

CHAPTER 1

Introduction

Advancements in process technology, such as the introduction of tens of nano-meter channel-length devices has significantly contributed to achieving VLSI goals such as increasing the speed and decreasing the power consumption. However, innovative circuit design techniques are still needed to take further advantage of shrunken devices.

MOS Current-Mode Logic (MCML) is an appealing design style for high-speed applications. This thesis addresses the practical issues in the design of high-performance MCML circuits and introduces a mathematical programming approach for designing these circuits.

1.1 Motivation

In conventional CMOS circuits, power dissipation increases linearly with its switching frequency. This makes other design styles such as MOS Current-Mode Logic (MCML) attractive, when it comes to very high performance applications [1].

MCML gates are current-mode circuits, working with voltage swings in the order of hundreds of mV. Due to the tail current source, an MCML gate dissipates a constant amount of static power, $P = V_{dd} \cdot I$, where V_{dd} is the power supply and I is the DC tail current [1-2]. For a conventional CMOS gate, power dissipation is well known as, $P = C'_L \cdot f \cdot V_{dd}^2$, where f is the switching frequency and C'_L is the load capacitance at

the output node [3-4]. Hence at multi GHz frequencies, an MCML gate consumes less power compared to its conventional CMOS counterpart. Moreover, reduced voltage swing in MCML gates, reduces the delay of these gates.

Regardless of the mentioned advantages, one of the major drawbacks in utilizing MCML circuits in large scales, is their design complexity [2], [6]. In conventional CMOS the only design parameter is the size of transistors, while in MCML, transistor sizes, resistor values, current source topology, DC biasing points, and output voltage swing have to be taken into consideration. Furthermore, due to the smaller voltage swing and, and therefore, lower noise margin compared to conventional CMOS circuits, MCML gates are more susceptible to problems arising from process, voltage and temperature variations, which may lead to malfunction.

In this work among MCML gates, the design of the universal gate receives special attention. The MCML universal gate integrates all AND/NAND/OR/NOR functions in a single gate with similar timing characteristics. This property allows the designer to focus on one logic gate instead of different gates. Nevertheless, because of its non-symmetrical structure, MCML universal gate has a very challenging design, compared to other MCML logic gates.

1.2 Objective

The objectives of this thesis are as follows

1. Developing a methodology for design and optimization of MCML circuits
2. Modifying standard MCML gate topologies to improve their performances

1.3 Thesis organization

This thesis is organized in six chapters. Chapter 2 introduces the basic operation of MCML gates. Then, in Chapter 3, an optimization methodology for the design of MCML gates in high-speed applications is presented.

In Chapter 4, some alternative topologies for standard MCML universal gate are proposed and their performances are compared with the standard one. In the same chapter, an All-MUX MCML circuit design technique, which only uses multiplexers as the basic building block of MCML digital circuits, is introduced. This characteristic offers a great advantage in system-level implementations.

In Chapter 5, to obtain a comprehensive design methodology that is capable of being automated for CAD tools, a mathematical programming approach for designing MCML circuits, is presented. This methodology may be used for full-custom design of any blocks of MCML circuits with multi-goal design specification. In this chapter, with this methodology, three different versions of MCML universal gate in a standard $0.18\ \mu\text{m}$ CMOS technology are designed and their performances are compared. The chapter also reports on full custom design of a four-bit ripple-carry adder and compares its performance with that of a conventional CMOS counterpart. All simulations are performed at the schematic and post-layout levels.

The final chapter presents some concluding remarks.

CHAPTER 2

Background and Theory of MCML Circuits

This chapter begins with reviewing the basic operation of an MCML gate. Then, it elaborates on practical challenges in design of MCML circuits, and provides an understanding of numerous trade-offs between design parameters.

2.1 Basic operation of MCML gates

In order to understand the issues in designing practical MCML gates, it is beneficial to start with reviewing the basic operation of an ideal gate. For convenience, a simple buffer/inverter MCML gate is selected for analysis. Figure 2.1 shows such a gate.

Figure 2.1: An MCML buffer/inverter

As depicted in Figure 2.1, an MCML gate comprises of three sections; the pull-up resistors, pull-down logic network, and a current source. Inputs are applied in a differential fashion in order to eliminate common-mode noise.

In ideal operation, depending on the input values, one of the branches is off, with its output node voltage clipped to V_{dd} , while the other branch takes all the current and, so, its output node voltage is at $V_{dd} - R \cdot I$. Thus, the voltage swing is $\Delta V = R \cdot I$, which is much smaller than V_{dd} that is the case for a conventional CMOS logic. Therefore, for the same amount of current, the delay of an MCML gate is given by

$$D = \frac{C_L \cdot \Delta V}{I},$$

compared to that of a conventional CMOS gate, which is

$$D = \frac{C_L \cdot V_{dd}}{2 \times I'}, \text{ where } I' \text{ is the average current to charge and discharge the load capacitance.}$$

2.2 Design challenges in practical MCML circuits

In order to speed up the operation of digital MCML gates for high-speed applications, the NMOS diff-pair transistors do not perform complete switching. In a case of a complete switching of the NMOS transistors, a relatively long period of time is wasted to charge and discharge the parasitic capacitances. Hence, we prefer to have some transistors on, while the others are partially on [6].

Figure 2.2 shows an MCML universal gate, which may perform a NAND/AND or NOR/OR function. In this figure VRP and VRS are the reference bias voltages for the PMOS-pair and the tail-current NOMS devices, respectively. In Figure 2.2, the pull-up resistors are replaced by a pair of PMOS transistors, which are biased in the triode region.

A review of some limitations and challenges in the design and optimization of practical MCML circuits follows next.

Figure 2.2: Standard Diff-pair Universal gate in MCML

2.2.1 Nonlinear behavior of PMOS devices

If the PMOS devices are not well biased in the triode region, with current and voltage variations, their equivalent resistance would also change. By increasing the voltage swing, the source-drain voltage of the PMOS devices, v_{SD} , increases, which makes the task of keeping the PMOS devices in the linear mode, more difficult. Therefore, we might need to apply a negative voltage potential to VRP, to satisfy $v_{SG} - V_{th} > v_{SD}$.

To reduce the delay, it is desirable to have small resistances at the pull-up network. This means W/L of the PMOS devices should increase. But reducing L, results in the PMOS devices going into saturation. It also reduces the gain, which in turn, deteriorates the robustness and regenerativity of the circuit. Also, increasing the width of the devices, degrades its linear behavior, and introduces more parasitic capacitances to the circuit, which may be quite considerable in high frequencies. Therefore, to avoid these non-ideal effects, it is recommended to use resistors instead of the PMOS transistors for high-speed applications. However, the advantages of using PMOS transistors are reduced area and lower cost.

2.2.2 Matching rise time and fall time

The rise time is associated with RC of the pull-up network and the fall time is determined by the pull-down network. The asymmetrical structure of the circuit in Figure 2.2 makes the task of matching the rise time and the fall time very difficult.

2.2.3 Output DC voltage

For non-symmetrical MCML gates such as the one illustrated in Figure 2.2, it is important to select the transistor sizes such that both complementary outputs have the same DC voltage levels. Otherwise, from one stage to another, there will be DC-level shift depending on which output is connected to which input. As a result of this DC-level shift, we will have instability and unpredictability in the circuit.

To obtain a good criterion for measuring this effect, first we define the differential output signal as $v_{out} - \bar{v}_{out}$, where v_{out} and $\bar{v}_{out}$ are complementary output voltages for an MCML gate. In general, for non-symmetrical gates, positive and negative peaks of the differential output signal, are not equal. If the value of the smaller peak is $|\Delta V_p|_{min}$ and that of the larger one is $|\Delta V_p|_{Max}$, then, peak-peak voltage swing can be expressed as $\Delta V_{p-p} = |\Delta V_p|_{Max} + |\Delta V_p|_{min}$. One good criterion to control the DC-level shift is

$$\eta = \frac{|\Delta V_p|_{min}}{\Delta V_{p-p}} \quad (2.1)$$

In Equation (2.1), $\eta \leq 0.5$. Figure 2.3 shows three different cases of complementary signals with different DC-levels and amplitudes, as it is the case for non-symmetrical MCML gates. As this figure shows, when complementary outputs have the same DC voltage levels, $\eta = 0.5$, otherwise $\eta < 0.5$. For convenience, from here on, ΔV represents the minimum differential voltage swing, $|\Delta V_p|_{min}$, and is simply referred to as voltage swing.

$$\eta = \frac{b-a}{2(b-a)} = 0.5$$

$$\eta = \frac{b-a}{2(b-a)} = 0.5$$

$$\eta = \frac{b-a}{b-a+d-c} < 0.5$$

Assuming:

$$b-a < d-c$$

Figure 2.3: Criterion for controlling DC-level shift

2.2.4 Threshold voltage fluctuation

In deep submicron (DSM) technologies, where the size of MOSFET transistors shrink, due to process related variations in the gate-oxide thickness, gate length and random placement of the channel dopant, the threshold voltage (V_{th}) of MOSFET devices fluctuates. This variation degrades transistor matching, and reduces voltage swing, which could end up in circuit malfunction.

2.2.5 Dependency of design parameters

Unlike conventional CMOS, in design of MCML gates, there are many design parameters that have to be taken into consideration. Nonlinear inter-dependency of these design parameters, adds to the difficulty of design and optimization of MCML circuits.

The following examines some of these trade offs for a simple MCML buffer/inverter gate illustrated in Figure 2.1.

- Pull-up resistors

Increasing the amount of pull-up resistors, raises the differential DC gain of the gate. This provides more robustness for the gate by boosting the signal integrity. On the other side, RC delay at the output node also increases, which in turn raises the overall delay of the gate.

- Bias current

Increasing the bias current, raises the gain and slew rate

$$SR = \frac{I}{C_L} \quad (2.2)$$

where, I is the bias current, and C_L is the output load capacitance. Increasing the bias current, would also reduces the delay, $D = Q/I$. However, increasing the bias current, elevates the power consumption of the gate. It also degrades switching quality of the gate [2].

- Tail NMOS

In Figure 2.1, by increasing L_s , the output impedance of the current source increases as well. This would provide more stable current, independent of voltage variations across the tail NMOS. It also improves the matching between two branches of the current mirror structure. But increasing L_s , also increases the saturation voltage, V_{dsat} , of the tail NMOS, which at typical low voltage drops across the current source, can push the NMOS transistor out of saturation. At the expense of larger area, one may keep L_s high and at the same time increases W_s , to lower V_{dsat} , and lead the tail NMOS back to saturation.

- Voltage swing

reducing the voltage swing reduces the delay, which is desirable. But at the same time, it degrades signal integrity of the gate, which lowers the switching quality of the next stage.

- Power supply

Increasing the value of the power supply, V_{dd} , helps to bias the tail NMOS in saturation. The price is, higher power dissipation.

- diff-pair NMOS transistors

In Figure 2.1, there is almost no benefit in increasing L . Therefore, to take advantage of higher speed for NMOS transistors, we keep the value of the channel length to the minimum value allowed for each technology. By increasing W , g_m of the device increases, which leads to higher gain for the gate. The drawback is having more parasitic capacitances, which cuts down the maximum speed of the gate.

- Reference voltage for tail NMOS (VRS)

Increasing VRS, allows us to use smaller tail NMOS transistor for high bias currents, which saves on area. On the other hand, increasing V_{GS} of the tail NMOS requires

higher v_{DS} across its drain-source, to keep the tail NMOS in saturation. Therefore, it becomes more difficult to keep the tail NMOS in saturation. This is particularly true, when it comes to multi level MCML gates.

2.3 Literature review

In this section current-mode logic styles from the literature are presented and their basic functionalities are discussed.

2.3.1 Emitter Coupled Logic (ECL)

Emitter coupled logic (ECL) is the fastest logic style known for silicon integrated circuits. However, because of utilizing Bipolar transistors and resistors, integration density in ECL technology is not high. Therefore, ECL is often used in conjunction with other logic families and its application is only limited to those sections which require high-speed operation. Input and output buffers are some of the examples where ECL interfaces on-chip CMOS and BiCMOS logic with off-chip systems operating at ECL voltage levels [19].

In ECL style, in order to minimize the output voltage perturbations induced from the power supply noise, it is a common practice to ground the positive end of the power supply. In this logic family to achieve fast operations, switching transistors are biased with relatively high currents (i.e. a few mA). Also, the supply voltage in ECL is about several base-emitter voltage drop (V_{BEON}). As a result, static power consumption in ECL circuits is high. An ECL NOR/OR gate is depicted in Figure 2.4.

This circuit is comprised of a conventional differential amplifier, a reference voltage circuit, a current source, and Emitter-follower output buffers.

2.3.2 Current Steering Logic (CSL)

Figure 2.5 illustrates a 4-input NOR gate implemented in CSL family.

Figure 2.4: An ECL NOR/OR logic gate

Figure 2.5: A 4-bit CSL NOR gate

In first-order analysis, in this logic family, a constant current is drawn from the voltage source. Therefore, the width of the biasing path can be set regardless of the gate switching activity, which is not possible in the case of a conventional CMOS logic circuit. Also, sub-threshold currents do not deteriorate the performance of a CSL gate, which makes this logic style attractive for deep sub-micron technologies [20].

CSL circuits are suitable for mixed-signal applications, where high-precision sensitive analog circuits are working with noisy digital switching circuits.

As Figure 2.5 shows, CSL gate does not have a high level of robustness. The voltage swing changes with threshold voltage variations in the diode-connected NMOS transistor. The circuit performance is also vulnerable to loading effects and input combination.

2.3.3 Dynamic Current-Mode Logic (DyCML)

In this logic style, to save on the static power consumption in a conventional CML circuit, the pull-up network and current source section are modified according to Figure 2.6 [6].

In DyCML circuits, when clock is low, outputs are pre-charged to V_{dd} , and when it is high, due to different impedances in the output branches, they are discharged with different rates, and the final values will be kept in the latch circuitry.

This circuit is similar to DCVSL logic family. It also incorporates a dynamic current source which is controlled by the clock signal. Unlike the conventional MCML, in this logic family transistors are rarely completely on. Therefore, this style is not suitable for high-speed operations.

2.3.4 Feedback MCML

As explained earlier, threshold voltage fluctuations in MOS transistors degrade the matching quality of output branches in MCML circuits, which has a negative impact on overall performance of the circuits.

An MCML circuit with negative feedback has been introduced in [5], which reduces the sensitivity of the circuit to parameter variations, and it also increases the bandwidth of the circuit. The drawback is a reduction in the DC gain. However, this is not a sensitive issue in digital gates, as long as the voltage gain is greater than unity. A gain of

Figure 2.6: DyCML gate

more than unity is required to preserve regenerativity of the gates and proper signal propagation. Figure 2.7 illustrates a Buffer/Inverter in feedback MCML style.

Figure 2.7: A Buffer/Inverter in feedback MCML style

CHAPTER 3

*Simulation Environment and
Optimization Methodology*

In order to compare different topologies in MCML logic family, it is necessary to have a solid design and optimization methodology. Unless a proper transistor level adjustment is made, it is not possible to judge the true performance of different circuits. This chapter will present different design and optimization techniques for high performance MCML circuits. In particular, the asymmetrical structure of the standard MCML universal gate, adds to the existing challenge of the design and optimization for high-speed applications. Moreover, as the standard MCML universal gate, integrates four fundamental logic functions into a single gate, it has a high degree of importance among MCML logic gates. Therefore, in order to address the real challenges of incorporating MCML circuits in high performance systems, our examples will be focused on design and optimization of MCML universal gate for high-speed applications.

3.1 Design and optimization of MCML universal gate using simulation iterations

Figure 3.1 Shows a standard MCML universal gate, with two separate reference voltages to control the tail NMOS and the pair of PMOS devices in the pull-up network.

For parameter optimization, it is necessary that a simulation environment be provided, so that we can measure different performance metrics, such as the propagation

By definition [4], according to Figure 3.3, V_M is a mid-swing point, where $v_{out} = v_{in}$.

Figure 3.3: mid-swing point in an inverter

This definition applies for an inverter in digital gates. But it is also a good point for inputs of the MCML universal gate. Hence to provide proper input biasing for the gate under test (i.e. I0 in Figure 3.2), I1 is configured as an inverter, and its inputs are connected to its outputs. To create the worst-case scenario, by applying the input signal to A and $\sim A$, and setting B = High and $\sim B$ = Low, the longest path in the gate is selected. We prefer to minimize simulation artifacts, in the whole process of design and optimization. Hence, for generating High and Low logic levels, V_{dd} and V_{ss} go through similar cascaded gates (i.e. I3 and I4), before being applied to the gate under test, i.e. I0. In Figure 3.2, I2 is a dummy load for the gate under test. One good criterion for having a reasonable DC-level difference between the outputs, as discussed in Section 2.2.3, is $\eta \geq 0.4$. When DC-level of both outputs are the same, η has the maximum value of 0.5.

The two mentioned constraints have to be met in any design. However, depending on the application and design goals, different approaches exist to select proper sizing for the tail NMOS, the pair of PMOS devices and NMOS diff-pairs. In the following we discuss these approaches.

3.1.1 *Variable gate current*

In this method, the tail current source device is in linear mode of operation. Therefore, the amount of current changes according to the switching requirements of the gate.

3.1.1.1 *Tail NMOS*

In this approach, the tail NMOS is not kept in saturation. In fact the tail NMOS similar to [6], sinks the current, whenever it is required. For this means, the tail NMOS is in triode region. In order to be able to select small values for W_s to save on area, its gate is connected to a high reference voltage. Since we are not looking for a high output impedance current source, therefore, the channel length of the tail NMOS is also selected small.

3.1.1.2 *PMOS pair*

In this approach, the PMOS pair is not bound to stay all the times in triode region. When it is in saturation, a tiny amount of current change in one branch, generates a large amount of voltage swing at the corresponding output node, which increases the gain and the voltage swing.

3.1.1.3 *NMOS diff-pair*

For high-speed design with simulation iterations, W of each NMOS transistor is selected such that the greatest of $\{t_r, t_f, \tilde{t}_r, \tilde{t}_f\}$ is minimized. t_r and t_f are rise and fall times of one output signal. $\tilde{t}_r$ and $\tilde{t}_f$ are those of the complement output signal.

As this method does not emphasize the bias current, the reliability and the controllability of the circuit is low. However, due to the flexibility of the gate current, the switching activity takes place in a more efficient manner. Therefore, this approach is suitable for high-speed applications. Moreover, because of the self controlled current consumption of the gate, we have relatively low power consumption compared to other approaches.

3.1.2 Constant bias current and variable swing

In this approach, in order to gain more control on the circuit, PMOS pair is biased in triode region, and the tail NMOS operates in saturation. However, we do not impose a complete switching regime on the circuit.

3.1.2.1 Tail NMOS

The tail NMOS is biased in saturation to have a constant bias current flowing through the gate. Therefore, VRS has to be taken small, to facilitate the task of keeping the tail NMOS in saturation. To have enough voltage swing at high frequencies, we need higher currents. But increasing the bias current, raises the voltage drops throughout the gate. At some point, further increase in bias current, prevents having enough voltage drop across the tail NMOS to keep that in saturation. This would set a limit on maximum bias current. Increasing the channel length of the tail NMOS, L_s , effectively increases the output impedance of the current source, up to $L_s = 5 \times L_{min}$. On the other hand, for large bias currents, having small V_{GS} and large L_s for the tail NMOS, requires a huge W_s . This sets a limit on increasing L_s .

3.1.2.2 PMOS pair

Increasing W_l in Figure 3.1, increases the parasitic capacitances, and also lowers the voltage swing. Therefore, we try to use the minimum required size for the PMOS pair. PMOS devices should be large enough to allow the bias current flows through them, while they are working in triode region. On the other hand large W_l , lowers the voltage swing. Thus for a fixed V_{SG} , this helps to keep the PMOS in triode region. At the same time, large W_l , lowers V_{dsat} . Therefore, here we have a trade off for W_l .

3.1.2.3 NMOS diff-pair

An NMOS transistor, located on the shortest path to the output is assigned with minimum size, and the rest are sized up, accordingly. To achieve the maximum speed, the goal is to minimize the greatest of $\{t_r, t_f, \tilde{t}_r, \tilde{t}_f\}$, and to minimize the propagation delay as well.

In this method, we do not have complete switching. If the switching ratio between the two branches is $k/(1 - k)$, then, the differential voltage swing at the output is

$$\Delta V = R \cdot I \cdot (2k - 1) \quad (3.1)$$

Where R is equivalent resistance of each PMOS transistor. As the frequency of operation goes up the switching time reduces. Therefore, the switching ratio between the two branches gets closer to one. According to Equation (3.1), this changes the voltage swing too.

This approach provides more controllability and reliability than the previous approach, due to constant bias current and linear PMOS behavior. But due to lack of control on voltage swing, it remains susceptible to loading effects.

3.1.3 Complete switching

This approach is similar to the ideal operation of standard MCML gates. In other word, switching transistors perform complete switching, and the gate bias current is constant.

3.1.3.1 Tail NMOS

Similar to previous method, in order to gain a good control on electrical parameters of the circuit, the tail NMOS is biased in saturation. Since the switching event is performed completely, then, the fall time and the rise time are controlled by slew rate, Equation (2.2). This equation indicates, for high-speed optimization, the bias current has

to be selected large to gain high slew rate. However, as it was mentioned before, due to various voltage drops along the gate, there is a trade off between having high bias current and keeping the tail NMOS in saturation.

3.1.3.2 PMOS pair

From Equation (3.1), the voltage swing for complete switching is derived as

$$\Delta V = R \cdot I \quad (3.2)$$

To optimize the gate for maximum speed, we select the minimum voltage swing that still preserves the signal integrity of the circuit. The voltage swing of down to 200mV is acceptable. But to leave some marginal space for approximations and inaccuracy of the design and optimization and also to consider process variation factor, we decided to take 300mV as the minimum voltage swing in our design. By knowing the bias current and voltage swing, PMOS-pair will be sized appropriately.

3.1.3.3 NMOS diff-pair

According to [16], the minimum input signal for a diff-pair to have complete switching is determined by

$$|v_i| \geq \sqrt{2} \cdot (V_{GS} - V_{th}) \quad (3.3)$$

According to Figure 3.4, V_{GS} in Equation (3.3), is the minimum common mode voltage that is required to deliver a bias current of $I/2$ to each branch.

In Equation (3.3), $|v_i|$ is replaced by the voltage swing, which is selected 300mV. Now in Figure 3.4, by increasing the size of the NMOS diff-pair, V_{GS} is adjusted such that Equation (3.3) becomes true.

This approach is very reliable and gives great amount of control over design parameters. It gives us control, over bias current of the gate and the amount of voltage

Figure 3.4: Differential pair in common mode

swing. However, because of the complete switching of NMOS diff-pair transistors, this approach is not suitable for high-speed design and optimization.

Once the initial set of parameter values are found, the loading capability of the gate under test is evaluated by the secondary test bench illustrated in Figure 3.5.

Figure 3.5: Secondary test bench for MCML universal gate

This figure shows four stages, comprising a chain of eight MCML gates. Each stage has a fan-out of three. To have the worst-case, all measurements are done on the last stage (i.e. I7 and I8). The input combination is selected so that it resembles the worst-case scenario. In Figure 3.1, by applying the differential signal to the lowest level in the gate and connecting input B to the High logic level and input $\sim B$ to the Low logic level, the longest path in the gate will be selected. A loop circuitry, consisting of I13 and I14 is incorporated to generate the actual High and Low logic levels for the test bench. In the secondary test bench, the optimization goal is while maintaining the gain of greater than unity and minimum voltage swing of 300 mV, tune the circuit at its highest frequency of operation. By changing the size of PMOS and NMOS devices according to the guidelines explained previously, the maximum operating frequency at which these constraints are met, will be found.

By using Cadence calculator, most of metric design parameters, such as the rise time, fall time, propagation delay, gain and voltage swings can be written as closed-form expressions. This gives the advantage of plotting each metric design parameter, and observe its behavior, when performing multi-parameter sweeps.

Simulations show that due to nonlinear large signal effects, there will be a slight DC output level shift by changing the frequency of operation that affects the voltage swing at high frequencies. Gain reduction due to limited bandwidth, is another factor, which contributes in speed limitation.

CHAPTER 4

*Alternative Circuits in
MCML Logic Family*

This chapter starts with reviewing a technique to derive standard MCML implementations for any boolean function. This is followed by presenting new topologies for MCML universal gate. Next a new circuit design technique in MCML family is introduced. This design technique only incorporates multiplexers as the building block of all its logic implementations. With respect to speed, two of the most promising alternative topologies for MCML universal gate are designed and their performances are compared with that of the standard MCML universal gate. All simulation results are performed in schematic-level in a standard 0.13 μm CMOS technology.

4.1 Binary Decision Diagram (BDD)

BDD is a method that allows to implement any Boolean expression in standard MCML logic family. Let us review this method in an example.

The function that we want to implement is

$$F = AB\bar{C} + \bar{A}B + BD + \bar{B}C \quad (4.1)$$

By manipulating Equation (4.1), we have

$$F = A(B\bar{C} + BD + \bar{B}C) + \bar{A}(B + BD + \bar{B}C)$$

$$\begin{aligned}
&= A[B(\bar{C} + D) + \bar{B}C] + \bar{A}(B + \bar{B}C) \\
&= A[B(\bar{C}(1 + D)) + CD] + \bar{B}C + \bar{A}(B + \bar{B}C) \\
&= A[B(\bar{C} + CD) + \bar{B}C] + \bar{A}(B + \bar{B}C)
\end{aligned}$$

A flow chart for Equation (4.1) is illustrated in Figure 4.1, and its circuit imple-

Figure 4.1: A flow chart for Equation (4.1)

mentation is shown in Figure 4.2.

In a similar approach, any other logic function can be implemented in standard MCML logic family. Figure 4.3 shows a D-Latch and a MUX 2:1 in MCML logic family.

4.2 Alternative topologies for MCML universal gate

In this section we present three topologies as alternatives for standard MCML universal gates. Simulation results show that the proposed topologies have superior or comparable performances, compared to the standard universal gate, illustrated in Figure 3.1.

Figure 4.2: MCML implementation for Equation (4.1)

4.2.1 MCML universal gate with active load

Figure 4.4 shows an MCML universal gate with active load in the pull-up network.

In this circuit, resistors are replaced by active loads. Usually, the voltage gain in standard MCML universal gate is low. To overcome this problem, PMOS transistors in the pull-up network of Figure 4.4, are biased in saturation. Therefore, we have larger equivalent resistances in compare with situation, where PMOS devices are biased in triode region. This raises the voltage gain. Another problem that exists in the standard universal gate, is the non-symmetrical structure of its output branches. This non-symmetry, makes the task of balancing the output signals more difficult. In Figure 4.4, in DC analysis, the PMOS current mirror structure at the pull-up network, equalizes the DC currents in the output branches. Moreover by selecting the proper sizing for the NMOS current mirror

Figure 4.3: Examples of standard MCML logic gates

structure, as designated in Figure 4.4, we ensure that the DC bias current flowing through each branch is half the amount of that, flowing through the tail NMOS.

As it was mentioned above, the advantage of this topology is more electrical balance characteristic, despite the non-symmetrical structure of the output branches, as well

Figure 4.4: MCML universal gate with active load

as more reliability and robustness, due to higher voltage gain. The drawback is an extra branch and more transistor count, which leads to more power consumption. Also because of having high output impedance, this topology is not suitable for high-speed circuits.

4.2.2 Non-diff MCML universal gate

Figure 4.5, presents a Non-diff MCML universal gate [7].

The logic network, like the standard universal gate, contains all NAND/AND/NOR/OR functions. In this topology, the logic network is less complicated, in comparison with the standard one. The cross connection, which is between the output branches in the standard Diff-pair universal gate, in this topology has been eliminated. This will facilitate the task of sizing and balancing the NMOS transistors in the logic network.

Main disadvantage of this topology, compared to the standard Diff-pair universal gate, is lower common mode noise immunity.

Figure 4.5: Non-diff MCML universal gate

4.2.3 MUX-based MCML universal gate

Figure 4.6 shows a MUX-based MCML universal gate [7].

MUX-based universal gate is in fact, a MUX 2:1 with one of its inputs connected to its control signal. Figure 4.7 demonstrates four different implementations of MUX-based universal gate with a MUX 2:1.

By inverting input signals and having complementary outputs, each implementation of Figure 4.7, has all NAND/AND/NOR/OR functionality. MUX-based universal gate transfers the non-symmetry of Diff-pair universal gate, from outputs to the inputs. At the same time, unlike Non-diff topology, it has a fully differential structure. Later we will see that despite having two extra NMOS transistors in MUX-based topology in comparison with the standard Diff-pair, the total transistor widths in optimized MUX-based gate is less than that of the Diff-pair, which will make their gate areas comparable.

Figure 4.6: MUX-based MCML universal gate

Figure 4.7: Four different implementations of AND/OR with MUX 2:1

4.3 All-MUX MCML design technique

Using the same idea, which was explained in Section 4.2.3, one can develop a library of digital gates, only with multiplexers. Figure 4.8 illustrates some examples with All-MUX MCML circuit design technique.

Figure 4.8(a) is a negative-level D-Latch. When the CLK is Low, the output, Q, holds its value. When the CLK becomes High, the output gets updated by input data, D. Figure 4.8(b) has the same functionality, except latching the data at positive level of CLK.

Figure 4.8: Examples of All-MUX logic blocks

Figure 4.8(c) illustrates a MUX-based implementation of an XOR2. If $B = \text{High}$, $\sim A$ is passed to the output. If $B = \text{Low}$, A is passed to the output. Since in MCML, both complementary signals are generated at the output, therefore, both A and $\sim A$ are accessible for use. Figure 4.8(d) is a digital High/Low level generator. If output port o , is Low, then, input port 0, will be selected by control port S . Input port 0, is already connected to the output port $\sim o$, with logic level High. Therefore, a transition takes place, which changes the value of output port o , from Low to High. Now the circuit reaches a stable situation, where logic level High is latched at output port o , and logic level Low is latched at output port $\sim o$.

We can implement more complicated blocks by using multiplexers. Figure 4.9 shows a digital Voltage Controlled Oscillator (VCO), which is implemented by using a MUX 2:1.

Figure 4.9: A digital VCO implementation with MUX 2:1

In this figure the feedback is taken from complementary output signal, $\sim Out$. Therefore, the output signal, Out , toggles any time that $\sim Out$ gets updated. The toggling frequency is controlled by a voltage-controlled delay circuitry. In Figure 4.9, we can remove one of the feedback paths, and simply connect the control port, S to the logic level corresponding with the other input, which has a feedback.

4.4 A comparative analysis of MCML universal gates

Having concentrated on speed improvement, in this section, we compare the performance of two more promising versions of MCML universal gate introduced in Section 4.2, i.e. Non-diff and MUX-based, with that of the standard Diff-pair universal gate.

Figure 3.1 shows the standard Diff-pair universal gate, and the two modified versions of this gate, the Non-diff and the MUX-based, are depicted in Figure 4.5 and Figure 4.6, respectively.

As we see in those figures, comparing to the standard Diff-pair, the Non-diff has more balanced output branches. This characteristic in turn, produces more balanced complementary output waveforms, and equal DC-levels for the output voltages.

The MUX-based universal gate is a MUX 2:1 with one of its inputs connected to its control signal. In Figure 4.7, due to availability of complementary signals, by swapping the position of the complementary inputs, all NAND/AND/NOR/OR functions can be obtained. Therefore, we can implement a MUX-based universal gate in many different ways. This gives a great amount of flexibility when it comes to system-level design. By evenly incorporating complementary signals, we can equalize the loading effect on complementary signals and avoid overloading of one branch against the other. The MUX-based universal gate has both advantages of being fully differential and possessing a symmetrical topology, at the same time. This gives the benefit of having both high Common Mode Rejection Ratio (CMRR), and maximum differential swing, as discussed earlier. The other two topologies, only have one of these properties each. That is, the standard Diff-pair only provides a differential structure, leading to a high CMRR, and the Non-diff just provides a balanced output, but not the both at the same time.

4.4.1 Simulation results and discussion

All three MCML universal gates described earlier, according to the optimization method described in Section 3.1, were simulated and optimized for maximum speed in a standard TSMC 0.13 μm , using Spectre simulator in Cadence. The simulated results are shown in Figure 4.10, Figure 4.11, Figure 4.12 and Table 4.1. For convenience, the area, gain and voltage swing are normalized to those of the standard Diff-pair gate.

According to results, Non-diff and MUX-based operate at frequencies up to 13 and 12.5 GHz, respectively. This amounts to a speed improvement of up to 30% over that of the standard Diff-pair.

Since there is no layout to compare the area of different topologies, the total sum of transistor widths in each optimized gate is considered as a criterion to compare the area of different MCML universal topologies. This shows that although, the MUX-based universal gate uses more transistors, its total sum of the transistor widths is less than those of

Figure 4.10: Output waveforms of Figure 3.5, for Diff-pair universal gate, in 0.13 μm

Figure 4.11: Output waveforms of Figure 3.5, for Non-diff universal gate, in 0.13 μm

the others. For optimization of the MUX-based universal gate in secondary test bench of Figure 3.5, to create the worst-case situation, one output signal of all the four stages was unilaterally overloaded by connecting it to the input of the next stage with more fan-in. Therefore, we see a DC-level shift and reduced voltage swing for MUX-based gate at 12.5 GHz. The lowest power dissipation belongs to the MUX-based universal gate. However, since the MUX-based, due to extra fan-in of each gate has to drive a larger load than the

Figure 4.12: Output waveforms of Figure 3.5, for the MUX-based universal gate, in $0.13 \mu m$

other two, thus the total power dissipation of each gate including its driver, at maximum frequency of operation, is minimum for the Non-diff topology.

TABLE 4.1: Simulation results for different universal gate topologies

Universal Gate Topology	Diff-pair	Non-diff	MUX-based
Frequency of Operation (GHz)	10	13	12.5
Max{tp,~tp} (ps)	18.4	14.3	21.5
Vdd (V)	1.5	1.5	1.5
I (Univ.)+I (Inv.) (μA)	$270 + 427 = 697$	$297 + 382 = 679$	$221 + 481 = 702$
Normalized Area	1	0.92	0.90
Normalized Gain	1	1	1
Normalized swing	1	0.6	0.55

To estimate the propagation delay, let us consider the standard Diff-pair of Figure 3.1, with the PMOS devices working in triode region and the NMOS transistors in saturation. The small signal model for such a gate is shown in Figure 4.13.

The worst-case propagation delay happens, when the switching input, v_i , is applied to M1 and M2, B is connected to High and $\sim B$ is connected to Low. M5 and M6 in Figure 4.13, are replaced with their equivalent linear resistors, R_D . By applying the time

Figure 4.13: Small signal model for standard Diff-pair universal gate
constant method for linear networks with dominant pole [17], the worst-case propagation delay for the step input is derived as follows. For detail, see Appendix A.

$$t_p = 0.69[R_D(2C_{gd3} + C_{db3} + C_{db5} + C_{gd5} + C_{gs1}) + \frac{1}{g_{m3}}(C_{gd1} + C_{db1} + C_{sb3} + C_{sb4} + C_{gs4} + C_{gs3})] \quad (4.2)$$

$$\sim t_p = 0.69[R_D(C_{gd2} + C_{db4} + C_{dg4} + C_{db6} + C_{dg6} + C_{gs2})] \quad (4.3)$$

Where

$$R_D = \left[\mu_p C_{ox} \left(\frac{W_l}{L_l} \right) (V_{GS}|_{5,6} - V_{thp}) \right]^{-1} \quad (4.4)$$

t_p and $\sim t_p$ are the propagation delays of the complementary signals. In Figure 4.13

$$\begin{aligned}
C1 &= C_{gd1}, C2 = C_{db1} + C_{sb3} + C_{sb4} + C_{gs4}, C3 = C_{gs3}, C4 = C_{gd3}, \\
C5 &= C_{db3} + C_{db5} + C_{gd5} + C_{gs1}, C6 = C_{gd2}, \\
C7 &= C_{db4} + C_{dg4} + C_{db6} + C_{dg6} + C_{gs2}
\end{aligned} \tag{4.5}$$

By comparing Equation (4.2) and Equation (4.3), one can conclude that $\sim t_p < t_p$. Therefore, t_p is taken as the longer propagation delay for the standard Diff-pair gate.

Applying the same method to Non-diff universal gate results in an expression for propagation delay, similar to Equation (4.2), except $C_{sb4} = C_{gs4} = 0$. This predicts a lower propagation delay for the Non-diff gate than that of the standard Diff-pair gate. The worst case propagation delay for an MCML MUX 2:1 gate is given in [18].

$$\begin{aligned}
t_p &= 0.69[R_D(2C_{gd3} + C_{db3} + C_{db1} + C_{gd1} + C_{db5} + C_{gd5} + C_{gs8} + C_{gs3}) + \\
&\quad \frac{1}{g_{m3}}(C_{db8} + C_{gd8} + C_{sb3} + C_{gs3} + C_{gs4} + C_{sb4})]
\end{aligned} \tag{4.6}$$

Equation (4.6) has three extra terms of C_{db1} , C_{gd1} and C_{gs3} , compared to Equation (4.2). Therefore, Equation (4.6) predicts the longest propagation delay for the MUX-based universal gate among all the three topologies. Simulation results reported in Table 4.1, confirm these predictions.

Although, the propagation delay of the MUX-based is more than that of the standard Diff-pair, due to its topological advantages, this gate is capable of meeting our design constraints, which were outlined in Section 3.1, up to the maximum frequency of 12.5 GHz, while the standard Diff-pair can only meet those constraints up to 10GHz. As a matter of fact, in all these three cases, the propagation delay is much less than what is required to operate at this range of frequency, and the bottleneck for maximum speed is determined by the maximum output swing, worst-case voltage gain and fall/rise time of the gate, rather than the propagation delay of the gate.

4.5 Summary

In this chapter, three alternative topologies for MCML universal logic gate were proposed, and their advantages and disadvantages were discussed. In particular, a new version of MCML gates, comprised of only multiplexers was introduced. These All-MUX MCML circuits are topologically symmetrical while maintaining the traditional high common-mode noise immunity of standard MCML gates due to their fully differential structure. Later three versions of MCML universal gate, according to the methodology discussed in Section 3.1, were designed and optimized for maximum speed, in a standard TSMC 0.13 μm CMOS technology. Compared to the standard Diff-pair topology, the Non-diff and the MUX-based topologies, improve the maximum frequency of operation from 10 GHz to 13 and 12.5 GHz, respectively. The MUX-based consumes less power, compared to the other ones and occupies less area as well.

CHAPTER 5

*Mathematical Programming
for Design and Optimization
of MCML Digital Circuits*

This chapter introduces a methodology for designing MCML circuits, using a mathematical programming approach. The technique can be used to achieve a variety of design goals, such as minimum delay, minimum power consumption, and minimum power-delay product (PDP).

We demonstrate how to obtain practical circuits by deriving appropriate objective functions and imposing relevant constraints and design variable ranges. A by-product of this technique is that it provides an acceptable estimation of various design figures, such as delay, power dissipation, voltage swing and DC bias values.

In this work for complex mathematical operations, Maple, and for optimization purposes, MATLAB are used.

5.1 Design procedure

The following steps outline our design procedure.

5.1.1 Identifying the worst-case scenario

In order to replicate the worst-case scenario, input combinations are chosen such that the signals pass through the longest path in the circuit, and are connected to those input ports that have the maximum fan-in.

5.1.2 Determine design variables

Independent design unknowns such as size of transistors, are assigned based on the topology of each gate. In general, those devices that are in relatively similar positions, are assigned the same sizes to maintain the symmetry of the gate. Some variables such as the internal DC node voltages, voltage swing and DC-level of the output voltage, can be either specified as design parameters or be taken as design unknowns. Parameters such as technology-related data, the differential DC gain, and the power supply value are specified as design parameters.

In order to take advantage of the maximum speed, except for the current source, the rest of NMOS devices have minimum length.

5.1.3 Set constraints

We obtain an expression for the differential DC voltage gain of the circuit. The DC biasing equations are also written so that the output DC voltages are level. This would maximize differential output swing of the circuit. Also to avoid DC-level shift between cascaded stages, DC-level of the input and output signals are designed equal. Furthermore all the upper bounds and lower bounds of the design unknowns will be added as supplemental design constraints. Also any further condition that might apply to each circuit, will be imposed accordingly, by means of an additional equality or inequality.

5.1.4 Express design goals

According to design goals, objective functions are derived based on design parameters and design unknowns.

Now, by having a set of linear and nonlinear equalities and inequalities, and one or more objective functions, the design becomes an optimization problem that can be solved by a mathematical optimization tool such as MATLAB Optimization Toolbox. The result

is an optimum set of values for design unknowns that meet all the defined constraints and design goals. Figure 5.1 illustrates inputs and outputs of the optimization tool.

Figure 5.1: Inputs and outputs of the optimization tool

Since the number of gates and interconnections do not impose any restriction on the methodology, therefore, we can apply this technique to a block of MCML gates simultaneously, to determine the value of design unknowns, as well as individual gates.

5.2 MOSFET models

A MOSFET device has different parasitic capacitances [4],[10]. Considering the maximum value of each capacitance in all region of operation, implies

$$C_g = C_{ox} \cdot W \cdot L \quad (5.1)$$

$$C_{os} = C_{gso} \cdot W, C_{od} = C_{gdo} \cdot W \quad (5.2)$$

$$C_{sb} = C_{db} = C_j \cdot W \cdot z + C_{jsw}(2z + W) \quad (5.3)$$

According to Figure 5.2, z is the length of the drain (source), W is the device width, and L is the channel length in MOSFET device. C_g is an approximation for the

Figure 5.2: Layout of a MOSFET

maximum value of MOSFET oxide capacitance, in all regions of operation. Similarly, $C_{os}(C_{od})$ and $C_{sb}(C_{db})$ are the overlap and diffusion junction capacitances for source (drain). C_{ox} is the thin-oxide (gate to channel) capacitance per unit area, and $C_{gso}(C_{gdo})$ is the gate-to-source (drain) overlap capacitance per unit of gate width. C_j is the zero-bias depletion-layer capacitance per unit area, and C_{jsw} is the zero-bias depletion-layer capacitance per unit length of diffusion perimeter.

The Shockley-Sah model of an NMOS transistor [8-9], for short-channel devices in CMOS deep submicron DSM technologies is not accurate enough. Instead a set of customized MOSFET models for MCML NMOS transistors in different region of operation are adopted to be used in this work.

In this chapter, we will use standard TSMC 0.18 μm CMOS technology to implement our designs. Therefore, all the adopted expressions are related to this technology.

For an NMOS transistor in saturation region, alpha-power formula [11] is

$$i_{DS} = K \cdot \frac{W}{L} (v_{GS} - V_{th})^\alpha \quad (5.4)$$

For typical biasing of NMOS transistors in MCML gates, from Spectre simulations in TSMC 0.18 μm , Equation (5.4) becomes

$$i_{DS} = 82 \times 10^{-6} \times \frac{W}{L} (v_{GS} - V_{th})^{1.2} \quad (5.5)$$

For a more accurate model of a short-channel NMOS transistor in saturation region, channel length modulation effect will be taken into account too [11],[13].

$$i_{DS} = K \cdot \frac{W}{L} (v_{GS} - V_{th})^\alpha (1 + \lambda \cdot v_{DS})$$

Spectre simulations for TSMC 0.18 μm yields

$$i_{DS} = 66.7 \times 10^{-6} \times \frac{W}{L} \cdot (v_{GS} - V_{th})^{1.3} (1 + 0.36 \times v_{DS}) \quad (5.6)$$

For the short-channel NMOS transistor in triode region, a modified version of Shichman-Hodges model suggests that [12,13]

$$i_{DS} = K \cdot \frac{W}{L} (v_{GS} - V_{th} + \alpha \cdot v_{DS}) v_{DS} (1 + \lambda \cdot v_{DS})$$

Which is in fact, a polynomial in the form of

$$i_{DS} = K \cdot \frac{W}{L} (A_1 \cdot v_{GS} \cdot v_{DS} + A_2 \cdot v_{GS} \cdot v_{DS}^2 + A_3 \cdot v_{DS} + A_4 \cdot v_{DS}^2 + A_5 \cdot v_{DS}^3)$$

For typical biasing of the NMOS devices in MCML gates, extracting the model parameters by Spectre simulator, implies

$$i_{DS} = 327 \times 10^{-6} \times \frac{W}{L} (v_{GS} - V_{th} + 1.03 \cdot v_{DS}) v_{DS} (1 - 2.3 v_{DS}) \quad (5.7)$$

The above models have been adopted by noting that NMOS transistors in MCML gates, for an N-well process have non-zero, source-bulk voltages. In other words, the body effect has been considered in the model extractions.

For the tail NMOS, which is a long-channel device, with $V_{SB} = 0$, the parameter extraction of Equation (5.4), yields

$$i_{DS} = 82.5 \times 10^{-6} \times \frac{W_s}{L_s} (v_{GS} - V_{th})^{1.4} \quad (5.8)$$

These expressions are used to model NMOS transistor behavior for typical biasing values of MCML gates in TSMC 0.18 μm CMOS technology, in different regions of operation.

For NMOS devices in saturation region, whenever it is possible, we will use Equation (5.6), instead of Equation (5.5). However, because of limitations of the optimization tool in solving constrained nonlinear minimization problems, and also to avoid having complex expressions for the voltage gain, sometimes Equation (5.5) is preferred, as indicated in the text.

In the following, we will apply the mathematical programming technique, which was described in Section 5.1, to the design of three different versions of MCML universal gates, discussed in Section 4.4, i.e. standard Diff-pair, Non-diff, and MUX-based universal gates. The mentioned gates will be optimized for minimum delay and minimum power-delay product (PDP). The results will be verified by schematic-level simulations, in a standard TSMC 0.18 μm CMOS technology. Those will also be compared with post-layout simulation results to find out the accuracy of our methodology.

Using this technique, we also detail the full-custom design of a four-bit ripple-carry adder (RCA). The circuit is implemented, using a standard 0.18 μm CMOS technology. Post-layout simulations verifies the functionality of our design, and the accuracy of our performance predictions. A four-bit RCA implemented in conventional CMOS is also designed and compared with the MCML RCA to demonstrate the superiority of the optimized MCML RCA to the conventional CMOS counterpart in high frequencies.

5.3 Design of MCML universal gates

5.3.1 Standard Diff-pair universal gate

Figure 5.3 illustrates a standard Diff-pair universal gate.

Figure 5.3: Diff-pair universal gate

Applying the input signals to M1 and M2 and having $B = V_L$, and $\sim B = V_H$, where V_L and V_H are low and high logic levels, respectively, resembles the worst case input combination. Due to non-symmetrical topology of the gate, in order to balance the output signals, M1 and M2 are assigned with different size, w_1 and w_2 . M3 and M4, which have similar positions in the gate, are considered to be of equal size. However, in general case, they can be assigned different sizes. In DC analysis as it was discussed in Section 2.2.3, in order to obtain the maximum differential output swing, DC-levels of the output voltages have to be equal. Thus the DC current flowing through the left and right resistors in Figure 5.3 are taken the same, $I/2$. Also we ignore the DC current going through M4 as its input is connected to V_L .

The large signal differential DC voltage gain of the Diff-pair universal gate can be expressed as a function of design parameters and design unknowns (See Appendix B).

$$Gain = 351.2 \times \frac{I \cdot w_1^5 \cdot w_2^5 \cdot R}{(I \cdot w_1^5)^{5/6} w_2^5 + (I \cdot w_2^5)^{5/6} w_1^5} \quad (5.9)$$

To have a predictable design, there should be no DC-level shift from input to output. If the DC-level of the output is V_{odc} and the differential output swing is $\Delta V = 2 \times h_s$, then, $V_L = V_{odc} - h_s$ and $V_H = V_{odc} + h_s$, where $V_{odc} = V_{dd} - R \frac{I}{2}$.

For simplicity, in Equation (5.9), channel length modulation effect is ignored. However, for DC bias equations, to consider this effect, we will use Equation (5.6), instead of Equation (5.5). If DC voltages at nodes x and d in Figure 5.3, are named V_x and V_d , then, in DC analysis for M1, M2 and M3 the following equations are valid.

$$\frac{I}{2} - 66.7 \times 10^{-6} \times \frac{w_1}{l} (V_{dd} - R \frac{I}{2} - V_x - V_{th})^{1.3} (1 + 0.36(V_d - V_x)) = 0 \quad (5.10)$$

$$\frac{I}{2} - 66.7 \times 10^{-6} \times \frac{w_2}{l} (V_{dd} - R \frac{I}{2} - V_x - V_{th})^{1.3} (1 + 0.36(V_{dd} - R \frac{I}{2} - V_x)) = 0 \quad (5.11)$$

$$\frac{I}{2} - 66.7 \times 10^{-6} \times \frac{w_{34}}{l} (V_{dd} - R \frac{I}{2} + h_s - V_d - V_{th})^{1.3} (1 + 0.36(V_{dd} - R \frac{I}{2} - V_d)) = 0 \quad (5.12)$$

If the design goal were to minimize the delay of the gate for a fan-out of two, assuming a dominant-pole behavior, the objective function would be

$$R \cdot C_L = R[2(C_{g1} + C_{os1}) + C_{db2} + C_{db4} + C_{od4}]$$

By replacing Equation (5.1), Equation (5.2) and Equation (5.3) in the above equation, we can express the objective function as a function of the design parameters and design unknowns.

$$R \cdot C_L = R[2(C_{ox} \cdot l \cdot w_1 + C_{gso} \cdot w_1) + C_j \cdot z \cdot w_2 + C_{jsw}(2z + w_2) + C_j \cdot z \cdot w_{34} + C_{jsw}(2z + w_{34}) + C_{gdo} \cdot w_{34}] \quad (5.13)$$

To avoid non-practical results, it is a good practice to set some additional constraints, which define the lower and upper bounds of the design unknowns. By considering the technology limitations and design specifications, those limits are defined.

$$R_{min} \leq R \leq R_{Max}, w_{min} \leq \{w_1, w_2, w_{34}\} \leq w_{Max}, I_{min} \leq I \leq I_{Max} \quad (5.14)$$

Equation (5.9) to Equation (5.12) and Equation (5.14) are regarded as design constraints, and Equation (5.13) is the objective function that should be minimized. A mathematical optimization package such as MATLAB is capable of solving this sort of optimization problem. One interesting property of this method is, as the voltage swing reduces, the voltage nodes and currents get closer to their DC values. Therefore, the non-linear effects that are generated by large amount of signal swings, decrease. This would allow the gain equation to predict a more accurate behavior of the circuit. Thus at lower swings, signal integrity becomes more robust, which prevents further signal degradations at lower swings. Later in simulation results this effect will be verified.

5.3.1.1 Current source

Figure 5.4 shows the tail current source, which is in fact a current mirror structure.

Figure 5.4: Current mirror

At minimum voltage drop across the current source, to keep the device in saturation, $v_{GS} - V_{th}$ in Equation (5.8) is replaced by V_{dsat} , which is the saturation voltage in the MOSFET device. By this replacement the ratio of $\frac{w_s}{l_s}$ in Figure 5.4 is known. Smaller

I_s , requires smaller w_s , which saves on area and at the same time lowers V_{dsat} , which in turn helps to keep the tail NMOS in saturation. However, the drawback is more current mismatch in the current mirror, due to lower output impedance of the current source, and more AC current leakage through the current source. Since the voltage swing at node x is low, therefore, low output impedance does not create a serious problem in the performance of the gate. However, for predictability reasons, I_s is selected such that a mismatch of less than 10% exists between I and I_{dc} in Figure 5.4.

5.3.2 Non-diff universal gate

Figure 5.5 illustrates a Non-diff universal gate, designated with its DC biasing and large signal symbols.

Figure 5.5: Non-diff universal gate

The worst-case input combination happens, when the input signal is applied to M1 and goes through M2. In a similar approach initially the large signal differential DC gain of the circuit is derived (See Appendix B).

$$Gain = \left(\frac{164 \times 10^{-6}}{l} \right)^{5/6} \times \frac{R \cdot I^{1/6} \cdot w_{34} \cdot w_1^{2/3}}{(w_1 + w_{34})^{5/6}} \quad (5.15)$$

Writing the DC equations for M3, M2, M1 and M4 yields

$$I_3 = 82 \times 10^{-6} \times \frac{w_{34}}{l} \left(V_{dd} - R \frac{I}{2} - h_s - V_x - V_{th} \right)^{1.2} \quad (5.16)$$

$$\frac{I}{2} = 82 \times 10^{-6} \times \frac{w_2}{l} \left(V_{dd} - R \frac{I}{2} + h_s - V_d - V_{th} \right)^{1.2} \quad (5.17)$$

$$\frac{I}{2} = 82 \times 10^{-6} \times \frac{w_1}{l} \left(V_{dd} - R \frac{I}{2} - V_x - V_{th} \right)^{1.2} \quad (5.18)$$

$$\frac{I}{2} - I_3 = 82 \times 10^{-6} \times \frac{w_{34}}{l} \left(V_{dd} - R \frac{I}{2} - V_x - V_{th} \right)^{1.2} \quad (5.19)$$

Assuming a dominant-pole behavior, the propagation delay of the gate for real inputs (See Appendix C) is approximated by

$$R \cdot C_L = R[2(C_{g1} + C_{os1}) + C_{db3} + C_{db4} + C_{od3}]$$

By replacing the equivalent values of parasitic capacitors, from Equation (5.1), Equation (5.2) and Equation (5.3), we have

$$R \cdot C_L = R[2(C_{ox} \cdot l \cdot w_1 + C_{gso} \cdot w_1) + C_j \cdot z \cdot w_{34} + C_{jsw}(2z + w_{34}) + C_j \cdot z \cdot w_{34} + C_{jsw}(2z + w_{34}) + C_{gdo} \cdot w_{34}] \quad (5.20)$$

The lower and upper limits of the design unknowns are also defined with inequalities similar to those indicated in Equation (5.14). All these equalities and inequalities form a set of nonlinear constraints with objective function of Equation (5.20) that can be minimized by an optimization tool. The value of differential DC gain is one of the design parameters. For high-speed applications, in order to achieve a wider bandwidth, and at the same time to ensure signal propagation from input to output, the DC gain will be selected just greater than unity [5].

5.3.3 MUX-based universal gate

A MUX-based universal gate with the worst-case input combination is depicted in Figure 5.6.

Figure 5.6: A MUX-based universal gate with worst-case input combination

Input combination is selected such that the signal path is the longest path, and the input signals are connected to the most loaded input port. Like the previous designs, the DC differential voltage gain for Figure 5.6 is (See Appendix B)

$$Gain = 952.2 \times \frac{R \cdot V_{th}^{1/5} \cdot w_6 (w_5 \cdot w_2 + w_5 \cdot w_1 + w_2 \cdot w_1)}{w_6 \cdot w_2 + w_6 \cdot w_1 + w_5 \cdot w_2 + w_5 \cdot w_1} \quad (5.21)$$

In DC analysis

$$I = \frac{82 \times 10^{-6}}{I} \left(V_{dd} - R \frac{I}{2} - V_x - V_{th} \right)^{1.2} (w_1 + w_2) \quad (5.22)$$

$$\frac{I}{2} - \frac{82 \times 10^{-6}}{l} \left(V_{dd} - R \frac{I}{2} + h_s - V_d - V_{th} \right)^{1.2} w_{34} = \frac{82 \times 10^{-6}}{l} \left(V_{dd} - R \frac{I}{2} - V_d - V_{th} \right)^{1.2} w_5 \quad (5.23)$$

$$\left(V_{dd} - R \frac{I}{2} + h_s - V_d - V_{th} \right)^{1.2} w_{34} = \left(V_{dd} - R \frac{I}{2} - V_x - V_{th} \right)^{1.2} w_1 \quad (5.24)$$

$$\frac{I}{2} = \frac{82 \times 10^{-6}}{l} \left(V_{dd} - R \frac{I}{2} - V_d - V_{th} \right)^{1.2} w_6 \quad (5.25)$$

In addition, similar to the previous cases, the lower and upper limits of design unknowns are imposed to the design as additional constraints.

The objective function to achieve the maximum frequency of operation for fan-out of two, with a dominant-pole assumption is

$$R \cdot C_L = R[2(C_{g2} + C_{os2} + C_{g6}) + C_{db3} + C_{db5}]$$

By replacing the equivalent values of parasitic capacitors, we have

$$R \cdot C_L = R[2(C_{ox} \cdot l \cdot w_2 + C_{gso} \cdot w_2 + C_{ox} \cdot l \cdot w_6) + C_j \cdot z \cdot w_{34} + C_{jsw}(2z + w_{34}) + C_j \cdot z \cdot w_5 + C_{jsw}(2z + w_5)] \quad (5.26)$$

By feeding all the constraints and objective function into the optimization tool, the optimum value of design unknowns is obtained.

5.4 Four-bit ripple-carry adder (RCA) design

In this final example, the goal is to design a block of complex MCML gates, to demonstrate the complete capability of this methodology. For this means a four-bit RCA in standard MCML logic family is selected to be designed for maximum speed. Figure 5.7 shows the block diagram of such an adder [4]. Each full adder is comprised of two gates, the sum and carry.

Figure 5.7: Block diagram of a four-bit RCA

5.4.1 Sum circuit

The sum circuit is in fact, a three input XOR [4], which consists of three stages and two symmetrical sections. Figure 5.8 illustrates an MCML implementation of such a circuit [2].

Figure 5.8: An implementation of sum function in MCML

For a three-input XOR function, $A \oplus B \oplus C_i$, position of A , B and C_i in the Boolean expression is indifferent. This provides an opportunity to decide on how to connect the inputs to the circuit. By considering the fact that the output of the sum circuit is not along the critical path of the four-bit RCA, there won't be any advantage in connecting the input carry signal, C_i , to the input port, which is the closest one to the output node. Besides, the first diff-pair level, located at the bottom, comprises of only two NMOS transistors, while the third level at the top includes eight NMOS transistors. Therefore, The first level inserts less capacitance load for the connected input signal than the other two levels in the gate. For all these reasons, according to Figure 5.8, we decide to connect the input carry signal, to the first level of the sum circuit. The next thing to decide is choosing an input combination that creates the worst-case situation. For this means the input signal is input carry, which goes through all levels in the gate. A and B are also given different values to set the RCA in a propagation mode.

The next thing, is to determine the design unknowns. In general, to maintain the symmetry of a gate, those devices, which topologically and electrically have the same relative positions and situations in the gate, are given the same size. As Figure 5.8 indicates, we assign different size to the NMOS transistors in each three levels of the gate.

In this circuit, due to body effect, we allocate different threshold voltages, V_{th1} , V_{th2} , V_{th3} for different levels in the gate. Now, to write the equations, we need a realistic estimate of each device's operating region. Usually, it is desirable to have all diff-pair devices in saturation to get the maximum g_m , so the maximum gain. However, due to number of levels in a gate and V_{dd} limitation, it is not always possible to meet this condition. As a solution, to have a realistic estimate of each device's operating region, and to obtain a proper value for design parameters such as the value of V_{th} , a prototype of the circuit in minimum size is designed and simulated.

As the sum circuit consists of four similar sections, only a quarter of the circuit will be considered for further analysis. In Figure 5.8, the NMOS devices in the third diff-pair level at the top, remain in saturation. To know why, for instance consider M8 in Figure 5.8. In DC mode, we have

$$V_{DS8} = V_{odc} - V_{d2} \quad (5.27)$$

$$V_{GS8} - V_{th3} = V_{odc} + h_s - V_{d2} - V_{th3} \quad (5.28)$$

In Equation (5.28), h_s is half of the differential voltage swing. According to the general expression for delay, $D = Q/I = C_L \cdot \Delta V/I$, the lower voltage swing, provides lower delay. However, to preserve the signal integrity, robustness and switching quality of the gate [2], the voltage swing cannot be chosen too small. In high-speed MCML circuits, the typical value for the voltage swing in $0.18 \mu m$ CMOS technology, is 300 mV. Thus h_s is taken 150 mV. On the other hand, from the prototype simulation, by considering the body effect, the typical value of V_{th3} in Equation (5.28) is 0.6 V. Using these estimates, and combining Equation (5.27) and Equation (5.28), implies $V_{GS8} - V_{th3} < V_{DS8}$. It means M8 in Figure 5.8, is in saturation. Considering the symmetry of the circuit in Figure 5.8, by using a similar approach, one can show that all NMOS devices in the third diff-pair level are in saturation. The simulation results of the prototype circuit, confirms this fact, and also indicates that the approximate operating region of NMOS devices in the first and the second levels is triode region. However, in general, one can ideally assume all the devices in saturation, and examine its feasibility, by looking for a mathematical solution. In this case, MATLAB is not able to find a mathematical solution, while all NMOS devices are assumed in saturation. So we write the equations for the first and the second level NMOS devices in triode region. Another approach for this matter, is utilizing unified models such as those expressed in [14], which are valid for all regions of operation. In that case the whole design can be fulfilled independent of operational mode estimation for each device.

By taking a similar approach to those in designing universal gates, the large signal differential DC gain of the sum circuit for minimum length devices is derived as

$$Gain = -181.67 \times R_s \cdot w_c (-10V_{d1} + 23V_{d1}^2 - 46V_{d1} \cdot V_x + 10V_x + 23V_x^2) \quad (5.29)$$

Since the voltage swing at internal nodes, $d1$ and x , are small, v_{d1} and v_x are approximated with V_{d1} and V_x . Simulation results show that Equation (5.29) predicts the DC gain of the prototype circuit with less than 15% error.

At DC biasing point we have

$$\frac{I_s}{2} = 66.7 \times 10^{-6} \times \frac{w_a}{l} (V_{odc} + h_s - V_{d2} - V_{th3})^{1.3} (1 + 0.36(V_{odc} - V_{d2})) \quad (5.30)$$

$$\begin{aligned} \frac{I_s}{2} = & 327 \times 10^{-6} \times \frac{w_b}{l} (V_{odc} + h_s - V_{d1} - V_{th2} + 1.03(V_{d2} - V_{d1})) \times \dots \\ & \dots \times (V_{d2} - V_{d1})(1 - 2.3(V_{d2} - V_{d1})) \end{aligned} \quad (5.31)$$

$$\begin{aligned} \frac{I_s}{2} = & 327 \times 10^{-6} \times \frac{w_c}{l} (V_{odc} - V_x - V_{th1} + 1.03(V_{d1} - V_x)) \times \dots \\ & \dots \times (V_{d1} - V_x)(1 - 2.3(V_{d1} - V_x)) \end{aligned} \quad (5.32)$$

Where,

$$V_{odc} = V_{dd} - R_s \cdot \frac{I_s}{2}.$$

We take advantage of the flexibility of the methodology, and impose more constraints to the design, to increase the predictability of the design. According to Equation (5.33), to avoid unrealistic results, a lower limit on DC voltages across the NMOS diff-pairs is set.

$$V_{odc} - V_{d2} \geq V_{min1}, V_{d2} - V_{d1} \geq V_{min2}, V_{d1} - V_x \geq V_{min3} \quad (5.33)$$

In a further attempt, according to Equation (5.34), upper and lower boundaries for each design unknown is set. This would put the optimized set of values in the desired range.

$$w_{min} \leq w_a, w_b, w_c \leq w_{Max},$$

$$R_{min} < R_s < R_{Max},$$

$$I_{min} < I_s < I_{Max},$$

$$V_{min4} < V_x < V_{Max4},$$

$$V_{min5} < V_{d1} < V_{Max5},$$

$$V_{min6} < V_{d2} < V_{Max6} \quad (5.34)$$

Assuming that the output of the sum gate is connected to a fixed load of C'_L , which is resembling the parasitic capacitance of the output buffer, implies

$$R_s \cdot C_s = R_s(4C_{db}^{w_a} + C'_L) = R_s(4(C_j \cdot w_a \cdot z + C_{jsw}(2z + w_a)) + C'_L) \quad (5.35)$$

Another constraint that is imposed on the circuit, is to limit $R_s \cdot C_s$ to a maximum value.

$$R_s \cdot C_s \leq rc_{Max} \quad (5.36)$$

Equation (5.36), helps to search for the optimum point in a larger neighborhood.

5.4.2 Carry circuit

Figure 5.9, represents an MCML implementation of the carry circuit [2].

Carry logic is a majority vote between three inputs, with Boolean expression $C_o = AB + BC_i + AC_i$. A , B and C_i in this Boolean expression, have interchangeable positions, such that replacing one with another, does not change the value of the function. This property allows us to decide on how to connect the inputs of the circuit.

In the carry circuit, although, the output participates in forming the critical path of the four-bit RCA in propagation mode, it is still not beneficiary to connect C_i input to the closest point from the output node. The reason is, at higher levels in the carry circuit, the number of NMOS transistors connected to the inputs and also their sizes grows significantly. Consequently, larger amount of load is imposed on the outputs of the driving gates,

Figure 5.9: A carry circuit implementation in MCML logic family

comparing to the situation, where the carry signal is connected to the lowest level in the carry circuit. Unlike conventional CMOS gates, in optimized current-mode circuits, in higher levels in the gate, we have larger diff-pair NMOS devices. This is to accommodate for the same amount of current, as it is for the lower levels, but with smaller gate-source voltages.

For the mentioned reasons, we decided to connect C_i input signal, to NMOS diff-pairs located at the lowest level in the gate. To create the worst-case scenario, the longest path in the gate is selected by applying the input combinations according to Figure 5.9. For simplicity and symmetry purposes, the DC node voltages at drains of M1 and M2 are taken identical. In a general case, they could be assigned with different design unknown. To estimate operating region of each device, a similar approach to the one explained for the sum circuit is taken. the NMOS devices on the third level and M4, M5 in Figure 5.9, operate in saturation mode, while the rest are in triode region.

Similar to the previous designs, the DC voltage gain of the carry circuit is obtained as

$$Gain = -181.7 \times R_c \cdot w_{cc}(-10V_{d1c} + 23V_{d1c}^2 - 46V_{d1c} \cdot V_{xc} + 10V_{xc} + 23V_{xc}^2) \quad (5.37)$$

In Equation (5.37), there are some approximations. The DC drain voltages of M1 and M2 in Figure 5.9, are taken the same. large signals of v_{d1c} and v_{xc} are approximated to their DC values V_{d1c} and V_{xc} , respectively. The currents flowing through M8 and M9 are taken the same.

For Figure 5.9, in DC analysis, we have

$$\frac{I_c}{2} = 66.7 \times 10^{-6} \times \frac{w_{bc}}{l} (V_{odc} + h_s - V_{d2c} - V_{th3})^{1.3} (1 + 0.36(V_{odc} - V_{d2c})) \quad (5.38)$$

$$\begin{aligned} \frac{I_c}{2} = & 327 \times 10^{-6} \times \frac{w_{a1}}{l} (V_{odc} + h_s - V_{d1c} - V_{th2} + 1.03(V_{d2c} - V_{d1c})) \times \dots \\ & \dots \times (V_{d2c} - V_{d1c})(1 - 2.3(V_{d2c} - V_{d1c})) \end{aligned} \quad (5.39)$$

$$\begin{aligned} \frac{I_c}{2} = & 327 \times 10^{-6} \times \frac{w_{cc}}{l} (V_{odc} - V_{xc} - V_{th1} + 1.03(V_{d1c} - V_{xc})) \times \dots \\ & \dots \times (V_{d1c} - V_{xc})(1 - 2.3(V_{d1c} - V_{xc})) \end{aligned} \quad (5.40)$$

$$\frac{I_c}{2} = 66.7 \times 10^{-6} \times \frac{w_{a2}}{l} (V_{odc} + h_s - V_{d1c} - V_{th2})^{1.3} (1 + 0.36(V_{odc} - V_{d1c})) \quad (5.41)$$

$$V_{odc} = V_{dd} - R_c \cdot \frac{I_c}{2} \quad (5.42)$$

In the above equations, due to non-zero source-bulk voltages in an N-well process, three different threshold voltages have been assigned to diff-pair levels in the circuit.

To obtain the objective function for minimum delay, according to Figure 5.7, Figure 5.8 and Figure 5.9, carry output signal of previous bit, feeds both carry and sum circuits of the next bit.

Therefore

$$R_c \cdot C_c = R_c [C_g^{wcc} + C_{os}^{wcc} + 2C_{db}^{wbc} + C_{db}^{wa2} + C_g^{wc} + C_{os}^{wc}]$$

By replacing the equivalent values of parasitic capacitors, we will have

$$R_c \cdot C_c = R_c [C_{ox} \cdot w_{cc} \cdot l + C_{gso} \cdot w_{cc} + 2(C_j \cdot z \cdot w_{bc} + C_{jsw}(2z + w_{bc})) + \dots \\ \dots + C_j \cdot w_{a2} \cdot z + C_{jsw}(2z + w_{a2}) + C_{ox} \cdot w_c \cdot l + C_{gso} \cdot w_c] \quad (5.43)$$

By being more specific and imposing additional constraints, similar to Equation (5.33) and Equation (5.34) to the design, we achieve more control and increase the predictability of the final results.

5.4.3 Four-bit RCA

The intended design goal in this example is delay minimization for the four-bit RCA. The worst-case delay for such an adder in propagation mode is

$$rc_{adder} = 3R_c \cdot C_c + R_s \cdot C_s \quad (5.44)$$

By feeding all the equalities and inequalities from Equation (5.29) to Equation (5.42) and any other additional constraints, accompanied with Equation (5.44) as the objective function, into an optimization tool, all the design unknowns are obtained.

In this methodology, based on the capability of the mathematical optimization tool, a multi-goal design can also be carried out. In this design example, it was assumed that all the carry circuits in the four-bit RCA are the same size. Therefore, in Equation (5.44), $R_c \cdot C_c$ for all the carry circuits was taken the same. Simply by duplicating the equations and design unknowns, and modifying the objective function, an optimized design of the four-bit RCA with progressive sizing concept can be obtained [4].

In the following section, simulation results of the circuits, designed in Section 5.3 and Section 5.4 are reported.

5.5 Simulation results

5.5.1 Universal gates

All three universal gates, described in Section 5.3, were designed for minimum delay and minimum power-delay product (PDP), for a fan-out of two.

The results were also evaluated by BSIM3v3 model [15], using Spectre simulator in Cadence.

In simulation environment, as Figure 5.10 indicates, the gate under test (GUT) was driven by a similar gate, to generate real input signals.

Figure 5.11, Figure 5.12 and Figure 5.13 show the input-output waveforms of each universal gate for the minimum delay and minimum PDP designs.

The results are also summarized in Table 5.1 and Table 5.2. In those tables, t_{pp} is the theoretical propagation delay of each gate from MATLAB analysis, and t_p is the average propagation delay from schematic simulation, $t_p = (t_{PHL} + t_{PLH})/2$. PDP is the power-delay product of each gate from schematic simulation, and PDP_p is the theoretical PDP from MATLAB analysis.

Comparing Table 5.1 and Table 5.2, implies that the delay and PDP for each universal gate have improved as much as 20% and 51%, respectively, from one design to another. It also refers that the maximum error in theoretical results is 16%, while its average is 8.3%.

This is partially due to some approximations that were made during the design, and partially due to fine-tuning adjustments of transistor sizes after the design. In fact, before the simulation, the transistor sizes were slightly altered to balance the DC voltages at the outputs. In all cases the adjustments were made with less than 15% deviation from the theoretical values. The propagation delay of MUX-based universal gate is less than that of the Diff-pair universal gate. This doesn't match with delay predictions, explained in

Figure 5.10: Simulation environment for universal gates

Figure 5.11: Schematic simulation results for Diff-pair universal gate in $0.18\mu m$ technology

Figure 5.12: Schematic simulation results for Non-diff universal gate in $0.18\mu m$ technology

Figure 5.13: Schematic simulation results for MUX-based universal gate in $0.18\mu\text{m}$ technology

Section 4.4.1. Because, the optimized design of MUX-based and Diff-pair universal gates in this methodology have different sizing, and the extra terms in propagation delay expression for MUX-based are compensated by its smaller transistor size.

TABLE 5.1: Universal gates designed for minimum delay

Universal gate	$t_{pp}(ps)$	$t_p(ps)$	$PDP(fj)$
Diff-pair	24.7	24.9	14.8
Non-diff	19.5	21.7	13.6
MUX-based	22.7	19.6	16.0

TABLE 5.2: Universal gates, designed for minimum PDP

Universal gate	$t_p(ps)$	$PDP(fj)$	$PDP_p(fj)$
Diff-pair	27.1	9.8	9.66
Non-diff	22.9	12.8	11.0
MUX-based	22.8	11.8	12.6

For further investigation, the layouts of all universal gate designs, described in this section, were made. The post-layout simulations, with considering RC parasitic elements, confirm the schematic results within 10% error. Figure 5.14, Figure 5.15 and Figure 5.16

show the layout designs of Diff-pair, Non-diff and MUX-based MCML universal gates in TSMC 0.18 μm CMOS technology.

Figure 5.14: Layout of Diff-pair univ. gate

Figure 5.17 shows the effect of lowering voltage swing on gain. As it was already predicted, when the voltage swing drops, up to a certain point, where the switching activity is not affected yet, the gain improves. Lower voltage swing, brings the signals closer to their biasing points, where the design methodology is based on. Therefore, the gain expression predicts its pre-defined value more accurately. Besides, lack of large signals, reduces non-linear effects, which prevents degradation of the circuit performance.

5.5.1.1 Scaling

Designed values of minimum delay Diff-pair universal gate, according to the following, were scaled with factor of s .

$$w \Rightarrow s \times w,$$

Figure 5.15: Layout of Non-diff univ. gate

$$I \Rightarrow s \times I,$$

$$R \Rightarrow \frac{1}{s} \times R$$

In Figure 5.18(a) the propagation delay and the differential voltage gains are plotted versus the scaling factor of s . $\text{gain}(+)$ and $\text{gain}(-)$ are differential voltage gains, corresponding to positive and negative input swings, respectively. As Figure 5.18(a) refers, when the scaling factor deviates from one, either $\text{gain}(+)$ or $\text{gain}(-)$ drops below one, which is not desired. In fact, for minimum delay optimization as explained before, t_p is not the only factor that has to be considered. For proper signal propagation, both differential voltage gains should also stay above unity.

As it was mentioned previously, in RF circuits, while operating in non-flat region of the gain curve, reducing the gain, increases the bandwidth. In this case with an analogy to Gain-Bandwidth product, Gain/t_p is considered as a criterion to roughly evaluate

Figure 5.16: Layout of MUX-based univ. gate

optimality of this design. Figure 5.18(b) illustrates $\text{gain}(+)/t_p$ and $\text{gain}(-)/t_p$ versus the scaling factor of s . This figure indicates that the point, which offers the maximum Gain/t_p for both positive and negative swings, resides somewhere close to $s=1$. This point also maximizes the equivalency of the circuit in respect to input polarity. Investigation on other universal gate designs, yields similar results.

5.5.2 Four-bit RCA

The four-bit RCA was designed in TSMC 0.18 μm CMOS technology, to achieve minimum delay. Therefore, Equation (5.44) is used as the design goal. The results are examined by doing schematic-level simulation by Spectre. Besides, the layout of the four-bit RCA is made and its post-layout simulation results is compared with those of the schematic-level simulation.

Figure 5.17: Effect of voltage swing on voltage gain

Figure 5.18: Scaling the min. delay design for Diff-pair univ. gate. (a) gain and t_p versus s (b) Gain/t_p versus s

Figure 5.19 shows the layout of the four-bit RCA in MCML. The four-bit RCA is

Figure 5.19: Layout of the four-bit RCA in MCML

setup in propagation mode, so that the carry signal propagates from one bit to another. This creates the worst-case propagation delay for the adder. In Figure 5.20, the results of schematic simulation of the four-bit RCA is shown. This figure contains the first bit input carry signals, the forth bit output carry signals and the forth bit sum signals. In

Figure 5.20: MCML four-bit RCA signals from schematic simulation

Figure 5.21: MCML four-bit RCA signals from post-layout simulation

Figure 5.21, from post-layout simulations, the same signals are plotted. The schematic and post-layout simulations are performed in 1.5 and 1GHz, respectively. For comparison, a four-bit RCA implemented in conventional pull-up, pull-down CMOS [4] is also designed and simulated in schematic-level. The schematic of such an adder is depicted in Figure 5.22 and Figure 5.23. The four-bit RCA in conventional CMOS is simply designed, based on balancing the pull-up and the pull-down networks [4].

For convenience, the results of schematic and post-layout simulations for MCML four-bit RCA and also those of the conventional CMOS four-bit RCA are summarized in Table 5.3.

In Table 5.3, t_{pp} is the theoretical propagation delay of the RCA. t_p is its propagation delay, from schematic simulation. t'_p is its propagation delay, from post-layout simulation. P is dissipated power of the RCA from schematic simulation, and PDP is its

Figure 5.22: Sum circuit in conventional pull-up, pull-down CMOS

power-delay product from schematic simulation. Table 5.3 shows that from schematic to layout, the propagation delay has increased by 8%. This is mostly due to parasitic effects in layout design. Table 5.3 also refers that the theoretical propagation delay is off by only 15%, compared to post-layout results.

Comparing the conventional CMOS and the MCML designs, implies the delay and PDP of the MCML design are more than three times less than that of the CMOS design.

Figure 5.23: Carry circuit in conventional pull-up, pull-down CMOS

Also, the power dissipation of the MCML design compared to that of the CMOS design at 1.5 GHz has reduced by 22.5%.

TABLE 5.3: Four-bit RCA implemented in conventional CMOS and MCML

Four-bit RCA	$t_{pp}(ps)$	$t_p(ps)$	$t'_p(ps)$	$P(mW)$	$PDP(pj)$
CMOS	-	763.5	-	6.71	5.12
MCML	240	260.9	282.4	5.2	1.36

The MCML four-bit RCA is in fact, a practical example of multi-goal design. In addition to delay minimization, a maximum limit was also set on the area. During the

design, a set of constraints were set to avoid large sizes of NMOS devices. This led to a small design with total layout area of only $116.52\mu m \times 32.04\mu m$.

5.6 Layout techniques

In the layout design of MCML gates for high-speed applications, the following techniques are useful to be considered:

1- To achieve balanced output DC voltages, it is important to have matched poly resistors in the pull-up network. One useful technique for this means, is to interdigitate the poly resistors.

2- In order to reduce the parasitic capacitances, except for the tail NMOS, we avoid multi-fingering as long as it is possible. Typically in digital circuits, where switching devices are relatively small, multi-finger technique increases the area of the device.

3- In RF frequencies, to avoid antenna effects, the angles of interconnections are preferably 45° , instead of 90° .

4- To reduce substrate parasitic capacitances, high frequency signals are routed on higher levels of metal.

5- To reduce parasitic effects, interconnections are as short as possible.

6- More contacts and via, provides redundancy for bad connections due to fabrication problems, and also reduces the equivalent resistors of those contacts and via. But they also increase parasitic capacitances. Thus, it is a trade-off.

7- In selecting appropriate metal widths and number of contacts and via, current density rules have to be considered for each technology.

8- Using substrate contacts, reduce the effect of substrate noise on the circuit.

9- To avoid cross-talk effect, high frequency signals are routed, with having enough distance from each other.

5.7 Summary

In this chapter we introduced a design methodology for MCML circuits, using a mathematical programming approach. The technique may be used to achieve a variety of design goals, such as minimum delay, minimum power consumption or minimum PDP. We have demonstrated how to obtain practical circuits by deriving appropriate objective functions, and imposing relevant constraints.

A by-product of this technique is that it provides an acceptable estimation of various design figures, such as delay, power dissipation, voltage swing and even DC bias values. We applied the technique to the design of three versions of MCML universal gates, tuned for minimum delay and minimum PDP.

Comparing the two designs for each gate in a standard $0.18\ \mu\text{m}$ CMOS technology shows that the PDP improvement is significantly more than that of the delay. This indicates that, one may save considerable amount of power by a marginal compromise on speed.

Using our technique, we also designed and implemented a standard MCML four-bit RCA, in this standard $0.18\ \mu\text{m}$ CMOS technology. The reported results for post-layout simulations, verified the functionality of our design and showed that our performance prediction was accurate within 15%.

A four-bit RCA implemented in conventional CMOS was also designed to compare its results with those of the MCML RCA. At 1.5 GHz the MCML RCA compared to the CMOS RCA shows more than three times improvement in delay and PDP. Its power dissipation is also down by 22.5%. The total layout area of the four-bit MCML RCA is only $3733.3\ \mu\text{m}^2$.

In this work, MATLAB Optimization Toolbox version 6.5.1 was used.

CHAPTER 6

Conclusions and Future Work

In this work, first an optimization method for designing MCML universal gates operating in the range of 10 GHz has been developed. Three modified topologies for MCML universal gates were proposed that demonstrate comparable or superior performance compared to the standard Diff-pair universal gate.

In a standard 0.13 μm CMOS technology, the introduced Non-diff and MUX-based universal gates can operate at 13 GHz and 12.5 GHz, respectively, compared to 10 GHz for the standard Diff-pair universal gate. The power dissipation remains almost the same for all three topologies at 1 mW. This work has also presented an All-MUX MCML circuit design technique. Incorporating only symmetrical MCML multiplexers, as building blocks of various digital gates, significantly simplifies the process of design and optimization. Its single-cell library, makes this circuit design technique a good candidate for system-level implementation and automatic synthesis.

Most importantly, using a heuristic approach, a mathematical programming technique was employed to design and optimize the performance of a block of MCML circuits, simultaneously. This methodology is applicable for a variety of design goals. It can also be incorporated in multi-goal designs. A by-product of this technique is an acceptable estimation of various design figures, such as delay, power dissipation, voltage swing and DC biasing values.

With this methodology, we designed three versions of MCML universal gates, for minimum delay and minimum PDP. We also used this technique, to implement an MCML four-bit RCA in TSMC 0.18 μm CMOS technology. The post-layout simulation results indicate a total propagation delay of 282.4 ps, power dissipation of 5.2 mW and PDP of 1.357 pj, for MCML RCA at 1 GHz. A comparison of the MCML RCA with conventional CMOS RCA has shown one third of the delay and a quarter of the PDP for the MCML RCA design. The power dissipation of the MCML RCA has also reduced by 22.5%.

The contributions of this research are outlined as follows

1. Have developed a design and optimization methodology for MCML circuits based on mathematical programming technique.
2. Have developed two modified topologies for MCML universal gate, (called Non-diff and MUX-based) with higher performance than the standard MCML universal gate.
3. Have proposed an All-MUX MCML circuit design technique.
4. Have designed and implemented an MCML four-bit ripple-carry adder in TSMC 0.18 μm CMOS technology for high-speed applications.

Continuation of this work includes incorporating more rigorous MOSFET models, developing a mathematical methodology to identify the critical path, developing a complete CAD tool with a user friendly interface and an optimization engine for designing MCML circuits. There is also a need to evaluate the tolerance of MCML circuits against the process and temperature variations. For further investigation, it is helpful to incorporate this methodology for design and optimization of more complicated circuits. Future work also includes development of an automated methodology for system-level implementation of All-MUX MCML circuits.

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Appendix A: Propagation Delay in Diff-pair MCML Universal Gate

To find the propagation delay, we apply the time-constant method for linear networks with a dominant pole[17]. In this method, we find the equivalent resistor of each capacitor in the circuit, while the rest of capacitors are open circuit, and all independent sources are zeroed.

Applying this method to small signal equivalent circuit of Diff-pair MCML universal gate, depicted in Figure 4.13, yields

$$R_{C_1} = \frac{V_T}{I_T} = \frac{V_T}{g_{m3} \cdot V_T} = \frac{1}{g_{m3}}$$

$$R_{C_2} = \frac{1}{g_{m3}}$$

$$R_{C_3} = \frac{1}{g_{m3}}$$

$$R_{C_4} = 2R$$

$$R_{C_5} = R$$

Dominant pole is determined by

$$\tau_1 = \frac{-1}{P_1} = \sum_{i=1}^5 (R_{C_i} \times C_i) = \frac{1}{g_{m3}} (C_1 + C_2 + C_3) + R(2C_4 + C_5)$$

In the above equation, by replacing C_i $i=1..5$, with their equivalents from Equation (4.5), and having $t_p = 0.69\tau$ for an ideal step input, Equation (4.6) is derived.

Appendix B: DC Voltage Gain in MCML Universal Gates

1. Diff-pair universal gate

In Figure 5.3, differential large signal output voltage is expressed as

$$v_{OD} = v_{O1} - v_{O2} = -R \cdot i_{OD} \quad (\text{B.1})$$

We also have

$$i_{OD} = i_L - i_R \quad (\text{B.2})$$

$$I = i_L + i_R \quad (\text{B.3})$$

In Equation (B.2) and Equation (B.3), i_L and i_R are large signal currents going through the left and right resistors. Differential large signal input voltage in Figure 5.3, is

$$v_{ID} = v_{I1} - v_{I2} = v_{GS1} - v_{GS2} \quad (\text{B.4})$$

By considering M1 and M2 in saturation, to maximize the gain, $i_4 \approx 0$ and Equation (5.5), we have

$$i_L = 82 \times 10^{-6} \times \frac{w_1}{l} (v_{GS1} - V_{th})^{1.2} \quad (\text{B.5})$$

$$i_R = 82 \times 10^{-6} \times \frac{w_2}{l} (v_{GS2} - V_{th})^{1.2} \quad (\text{B.6})$$

Equation (B.2) and Equation (B.3) can be rephrased as

$$i_L = (I + i_{OD})/2, i_R = (I - i_{OD})/2 \quad (\text{B.7})$$

From Equation (B.4), Equation (B.5), Equation (B.6), Equation (B.7) and using minimum length device, i.e. $l = 180^{nm}$, v_{ID} is derived as a function of I and i_{OD} .

$$v_{ID} = 6.09 \times 10^{-3} \left[\frac{((0.5I + 0.5i_{OD}) \cdot w_1^5)^{5/6}}{w_1^5} - \frac{((0.5I - 0.5i_{OD}) \cdot w_2^5)^{5/6}}{w_2^5} \right] \quad (B.8)$$

The differential DC voltage gain is defined as

$$Gain = \frac{-v_{OD}}{v_{ID}} \quad (B.9)$$

In order to derive an equation for the gain, which is independent of i_{OD} , Equation (B.8) is approximated to a first order equation in respect to i_{OD} , by expanding its Taylor's series over the DC biasing point of $i_{OD} = 0$.

Applying the results to Equation (B.9), leads to an expression for the differential DC gain of Figure 5.3, around its DC biasing point, for minimum length devices in $0.18\mu m$ CMOS technology.

$$Gain = 351.2 \times \frac{I \cdot w_1^5 \cdot w_2^5 \cdot R}{(I \cdot w_1^5)^{5/6} \cdot w_2^5 + (I \cdot w_2^5)^{5/6} \cdot w_1^5} \quad (B.10)$$

2. Non-diff universal gate

In Figure 5.5, differential input signal is

$$v_{ID} = v_{I1} - v_{I2} = v_{GS1} - v_{GS4} \quad (B.11)$$

Since the gate of M3 is connected to V_L and v_x is not changing a lot, i_3 is approximated with I_3 . Therefore

$$i_L = 82 \times 10^{-6} \times \frac{w_1}{l} (v_{GS1} - V_{th})^{1.2} \quad (B.12)$$

$$i_R - I_3 = 82 \times 10^{-6} \times \frac{w_{34}}{l} (v_{GS4} - V_{th})^{1.2} \quad (B.13)$$

By solving Equation (B.7), Equation (B.12) and Equation (B.13) for v_{GS1} and v_{GS4} , we will have

$$v_{GS1} = \left[\frac{I + i_{OD}}{2} \cdot \frac{1}{w_1 \times 82 \times 10^{-6}} \right]^{5/6} + V_{th} \quad (B.14)$$

$$v_{GS4} = \left[\left(\frac{I - i_{OD}}{2} - I_3 \right) \cdot \frac{1}{w_{34} \times 82 \times 10^{-6}} \right]^{5/6} + V_{th} \quad (B.15)$$

Replacing Equation (B.14) and Equation (B.15) in Equation (B.11) yields

$$v_{ID} = \left[\frac{I + i_{OD}}{w_1 \times 2 \times 82 \times 10^{-6}} \right]^{5/6} - \left[\left(\frac{I - i_{OD}}{2} - I_3 \right) \cdot \frac{1}{w_{34} \times 82 \times 10^{-6}} \right]^{5/6} \quad (B.16)$$

Figure B.1 illustrates i_{OD} versus v_{ID} in Equation (B.16).

Appendix B.1: i_{OD} versus v_{ID} for Non-diff MCML universal gate

Where,

$$y_1 = I - 2I_3, y_2 = -I, x_1 = \left(\frac{I \cdot (I - I_3)}{82 \times 10^{-6} \times w_1} \right)^{5/6} \text{ and}$$

$$x_2 = \frac{-1}{(82 \times 10^{-6})^{5/6}} \times \frac{(I - I_3)^{5/6}}{w_{34}^{5/6}}.$$

To obtain the DC gain, a part of the curve in Figure B.1 is approximated with two lines, connecting the point O to the points A and B. Slope of the curve, on the right pane is

proportional to the differential DC gain for positive input swings, gain(+), and the slope on the left pane is related to the differential DC gain for negative input swings, gain(-). The smaller slope of two mentioned lines, determines the smaller gain of the two positive and negative swings.

$$\frac{\tan \theta}{\tan \theta'} = \frac{I - 2I_3}{I} \left(\frac{w_{34}}{w_1} \right)^{5/6} \quad (\text{B.17})$$

Writing DC equations for M1 and M4 implies

$$\frac{I}{2} = 82 \times 10^{-6} \times \frac{w_1}{l} \left(V_{dd} - R \cdot \frac{I}{2} - V_x - V_{th} \right)^{1.2} \quad (\text{B.18})$$

$$\frac{I}{2} - I_3 = 82 \times 10^{-6} \times \frac{w_{34}}{l} \left(V_{dd} - R \cdot \frac{I}{2} - V_x - V_{th} \right)^{1.2} \quad (\text{B.19})$$

Combining Equation (B.18) and Equation (B.19) yields

$$(I - 2I_3) \times w_1 = I \times w_{34} \quad (\text{B.20})$$

By applying Equation (B.20) to Equation (B.17),

$$\frac{\tan \theta}{\tan \theta'} = \left(\frac{w_{34}}{w_1} \right)^{11/6} \quad (\text{B.21})$$

The DC current in M1 is equal to total of the DC currents in both M3 and M4. Also $V_{DS1} < V_{DS34}$. Thus it is appropriate to say that $w_{34} < w_1$. Applying this to Equation (B.21) implies

$$\frac{\tan \theta}{\tan \theta'} < 1 \quad (\text{B.22})$$

Equation (B.22), indicates that the positive input swing is magnified with a lower gain, compared to the negative input swing. Therefore, from Figure B.1, the lowest DC gain, considering Equation (B.1), Equation (B.9) and Equation (B.20) is derived as

$$Gain = \left(\frac{164 \times 10^{-6}}{l} \right)^{5/6} \times \frac{R \cdot I^{1/6} \cdot w_{34} \cdot w_1^{2/3}}{(w_1 + w_{34})^{5/6}} \quad (B.23)$$

3. MUX-based universal gate

In large signal analysis, for Figure 5.6, we have

$$v_{ID} = v_{GS1} - v_{GS2} \quad (B.24)$$

$$i_1 = 82 \times 10^{-6} \times \frac{w_1}{l} (v_{GS1} - V_{th})^{1.2} \quad (B.25)$$

$$I - i_1 = 82 \times 10^{-6} \times \frac{w_2}{l} (v_{GS2} - V_{th})^{1.2} \quad (B.26)$$

Where, i_1 is large signal current flowing through M1. Also,

$$v_{ID} = v_{GS5} - v_{GS6} \quad (B.27)$$

By ignoring the small amount of current flowing through M4, for M5 and M6 we have

$$i_L - i_1 = 82 \times 10^{-6} \times \frac{w_5}{l} (v_{GS5} - V_{th})^{1.2} \quad (B.28)$$

$$i_R = 82 \times 10^{-6} \times \frac{w_6}{l} (v_{GS6} - V_{th})^{1.2} \quad (B.29)$$

By solving Equation (B.24) to Equation (B.26) for i_1 , and applying the results to Equation (B.27) to Equation (B.29) and Equation (B.7), and replacing l with minimum length, we will have

$$\begin{aligned} v_{ID} = & 0.001 \times (w_6 \cdot i_{OD} \cdot w_1 + w_6 \cdot i_{OD} \cdot w_2 - w_6 \cdot I \cdot w_1 + w_6 \cdot I \cdot w_2 - \dots \\ & \dots - w_5 \cdot I \cdot w_2 + w_5 \cdot i_{OD} \cdot w_1 + w_5 \cdot i_{OD} \cdot w_2 - w_5 \cdot I \cdot w_1) / \dots \\ & \dots / [V_{th}^{1/5} \cdot w_6 \cdot (w_5 \cdot w_2 + w_5 \cdot w_1 + w_2 \cdot w_1)] \end{aligned} \quad (B.30)$$

But we already know

$$(v_{ID} = 0) \Leftrightarrow (i_{OD} = 0) \quad (B.31)$$

Applying Equation (B.31) to Equation (B.30), and using Equation (B.1) and Equation (B.9), the DC gain of minimum length devices in Figure 5.6 is derived as

$$Gain = 952.2 \times \frac{R \cdot V_{th}^{1/5} \cdot w_6 \cdot (w_5 \cdot w_2 + w_5 \cdot w_1 + w_2 \cdot w_1)}{w_6 \cdot w_2 + w_6 \cdot w_1 + w_5 \cdot w_2 + w_5 \cdot w_1} \quad (B.32)$$

Appendix C: Propagation Delay of Cascaded Gates with Real Input

Figure C.1 shows a situation, where the input signal of a gate, has a time constant, equal to that of the output signal, $\tau = R \cdot C$.

$$v_i(t) = (1 - e^{-t/\tau}) \cdot u(t)$$

Appendix C.1: RC model for the output of a gate, with real input signal

Transfer function of Figure C.1, implies

$$\frac{V_o(S)}{V_i(S)} = \frac{1/(C \cdot S)}{R + 1/(C \cdot S)} = \frac{1/\tau}{S + 1/\tau}$$

$$\therefore V_o(S) = \frac{1/\tau}{S + 1/\tau} \times \left(\frac{1}{S} - \frac{1}{S + 1/\tau} \right) = \frac{1}{S} - \frac{1}{S + 1/\tau} - \frac{1/\tau}{(S + 1/\tau)^2} \quad (C.1)$$

Converting Equation (C.1) to time domain

$$v_o(t) = \left(1 - e^{-t/\tau} - \frac{t}{\tau} \cdot e^{-t/\tau} \right) \cdot u(t) \quad (C.2)$$

According to definition of propagation delay, which is the time interval from 50% of input to 50% of the output, we have

$$v_i(t_1) = 0.5 \Rightarrow t_1 = 0.69\tau \quad (\text{C.3})$$

$$v_o(t_2) = 0.5 \Rightarrow t_2 = 1.678\tau \quad (\text{C.4})$$

Therefore

$$t_p = t_2 - t_1 = 0.988\tau \approx \tau \quad (\text{C.5})$$