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**BIPOLAR TRANSISTOR MODELLING FROM A
POWER AMPLIFIER DESIGNER'S PERSPECTIVE**

by

Marquis C. Julien, B. Sc. (Elec.)

A thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfilment of
the requirements for the degree of
Master of Engineering

Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada
April, 1997

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April 1997

The information used in this thesis comes in part from the research program of Dr. Barry Syrett and Dr. Miles Copeland. The research results appearing in this thesis represent an integral part of the ongoing research program. All research results in this thesis including tables, graphs and figures but excluding the narrative portions of the thesis are effectively incorporated into the research program and can be used by Dr. Syrett and his associates for education and research purposes, including publication in the open literature with appropriate credits given to Marquis Julien. Matters of intellectual property may be pursued with Carleton University and Dr. Syrett where and as appropriate.

Abstract

The limitations of the SPICE Gummel-Poon Model (SGPM), first introduced in the 70s, have accumulated to the point where the model is no longer valid for Power Amplifier (PA) designs. As an alternative, the bipolar model HICUM with its better overall accuracy, wider application range, and greater flexibility is proposed. A brief history of bipolar modelling is presented followed by a description of HICUM. The application of HICUM to PA designs is discussed.

In order to fully take advantage of HICUM with respect to PA circuits, the model needs to be implemented in a commercially available Harmonic Balance simulator. The Libra simulator (copyright of HP/EEsof software inc.) is chosen for the implementation. The basic steps required to implement HICUM using the Libra interface are presented.

Using both models, a narrowband, medium power PA, with center frequency $f_c=1.9\text{GHz}$, a 3V rail voltage and meeting commercial application specifications is designed. The technology used is a high speed bipolar process provided by Nortel. Nortel offers a double poly technology with transit frequencies (f_T) in the order of 25 GHz.

Finally, layout and packaging considerations are discussed. Techniques are given to help minimize the effects of parasitics.

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Dedication

I dedicate this thesis to my father, André Julien, the best *engineer-without-a-paper* I know.
I thank him for all his inspirations and encouragements.

Je dédie cette these à mon père, André Julien, le meilleur *ingénieur-sans-papier* que je
connaît. Je le remercie pour ses nombreuses inspirations et son encouragement.

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List of Symbols and Abbreviations

AC	alternate current
A_E	effective emitter area
A_f, A_r	forward and reverse current gains (Ebers- Molls model)
B	factor for measure of stability
BC	base-collector
BE	base-emitter
BJT	bipolar junction transistor
CAD	computer aided design
C_{BCx}	external base-collector capacitance
C_{Cox}	emitter oxide capacitance
C_{dE}, C_{dEp}	emitter diffusion capacitance
C_{Eox}	emitter-oxide capacitance
C_i	total capacitance connected to the internal base node B'
C_j	depletion capacitance

C_{jBE}	base-emitter junction capacitance
C_{jBE0}	zero-bias base-emitter junction capacitance
C_{jCi}	internal collector junction capacitance
C_{jE}	emitter junction capacitance
$C_{jE,max}$	maximum emitter junction capacitance
C_{jS}	substrate capacitance
C_{j0}	zero bias depletion capacitance
C_M	Miller capacitance
C_{rBi}	internal base shunt capacitance
C_{th}	thermal capacitance
c_1	variable for calculation of i_T
c_{10}	variable for calculation of i_T
CS	collector-substrate
DC	direct current
f_{AVL}	coefficient for Avalanche process
f_{BC}	partitioning factor of C_{Cox}
F_C	parameter for junction capacitance (SGPM)
f_{DQr0}	correction factor for modulation
f_{geo}	geometry factor
f_{max}	maximum oscillation frequency

f_{Qi}	ratio of high frequency shunt to total internal capacitance
f_T	transit frequency
G_A	available gain
GaAs	gallium Arsenite
G_p	power gain
GPM	Gummel Poon model
G_T	transducer gain
HBT	heterojunction bipolar transistor
h_c	weighting factor for calculation of Q'_f
h_{fe}	current gain of a transistor
HICUM	high current model
I_{AVL}	avalanche generation current
I_{BEiS}, I_{BEpS}	internal and peripheral BE saturation currents
i_{B^0Ei}, i_{B^0Ep}	internal and peripheral BE quasi-static currents
i_{B^0Ci}, i_{B^0Cx}	internal and external BC currents
IC	integrated circuit
I_{CL}	variable indicating increase of τ_f
I_{Ch}	high-current correction factor
I_{CK}	critical current
I_{KB}	operating point dependent current, characterizes the onset of

	high-injection effects in the neutral base
i_f, i_r	forward and reverse diode currents (Ebers-Molls model)
I_{RB}	base current when base resistance is half its zero bias value (SGPM)
I_{SE}, I_{SC}	saturation currents for the BE and BC diodes (Ebers-Molls model)
I_S	saturation current for the transfer current
i_{TC}, i_{Tf}	ideal forward transfer current
i_{Tf}, i_{Tr}	charge controlled transfer currents
i_T	(total) transfer current
I_{10}	HICUM model parameter for calculation of τ_1
K	factor measuring the stability of a two port network
LC	inductor-capacitor
m_{BCi}, m_{BCx}	internal and external collector non-ideality coefficients
m_{BEi}, m_{BEp}	internal and peripheral emitter non-ideality coefficients
MMIC	multi-module integrated circuit
MOS	metal-oxide-silicon
M_x	exponent for junction capacitance (SGPM)
N_C	collector doping
n_i	intrinsic carrier concentration of silicon
NQS	Non-Quasi-Static
n^+	n-type doped material

PA, PAs	Power Amplifier (s)
PAE	power added efficiency
P_{out}	output power
P_{1dB}	P_{out} at the 1dB compression point
p^+	p-type doped material
q	electron charge
q_{AVL}	exponent factor for Avalanche process
Q'_f	weighted minority charge stored in the transistor
Q_{fB}	base minority charge
Q_{fC}	collector minority charge
Q_{fE}	emitter minority charge
Q_{jEi}	depletion charge stored within the BE junction
Q_{jCi}	depletion charge stored within the BC junction
Q_f	minority charge
Q_{f0}	low current charge component of Q_f
Q_{f1}	medium current charge component of Q_f
Q_{f2}	high current charge component of Q_f
Q_j	depletion charge
Q_p	hole charge
Q_{p0}	hole charge within the internal transistor at thermal equilibrium

Q_{pC}	minority charge stored in the collector
Q_r	BC diffusion charge
r_{Bx}	external operating point independent base resistance
RC	resistor - capacitor
r_B	a.c. internal base resistance (SGPM)
r_{Bi}	d.c. internal base resistance
r_{Bi0}	zero-bias internal base resistance
r_{Bi}^*	a.c. internal base resistance (HICUM)
r_{Bx}	external base resistance
r_{ci0}	epitaxial collector low-field resistance
r_{Cx}	external collector resistance
r_E	emitter resistance
RF	radio frequencies
r_{Su}	substrate resistance
S_f, S_r	forward and reverse transconductance
SGPM	SPICE Gummel Poon Model
SiGe	Silicon Germanium
s_{20}	slope caused by emitter charge
T_j	junction temperature
T_0	reference temperature

$V_{B'E'}$	internal base - internal emitter voltage
$V_{B^*E'}$	peripheral base - internal emitter voltage
v_c	auxiliary voltage for calculation of τ_{f0}
V_D	built-in voltage
$V_{C'E'}$	internal collector - internal emitter voltage
$V_{C'E's}$	internal CE saturation voltage
V_{DE}, V_{DC}	built-in voltage
V_G	bandgap voltage
V_{Gb}	base region averaged bandgap voltage
V_{jE}, V_{jS}	built-in voltage for junction capacitance
V_{jPCi}	internal punch-through voltage
V_{PT}	punch-through voltage
V_{lim}	limitation voltage
V_0	Early voltage
$V_{PT}, V_{PTCi}, V_{PTS}$	punch-through voltage
V_{sat}	saturation voltage
V_{swing}	voltage swing at the output of a transistor
V_T	thermal voltage
V_1	carrier jam voltage

w_c	collector width
z_E, z_S	exponent coefficients
α_B	relative temperature coefficient for low current gain
α_{CEs}	relative temperature coefficient of $V_{CE's}$
α_{jE}	$C_{jE,max}$ divided by C_{jE}
α_{iT}	factor for additional delay time of i_T
α_n	coefficient describing the Avalanche process
α_K	model parameter, factor for I_{CL}
α_{vs}	relative temperature coefficient of saturation drift velocity
α_{Qf}	factor for additional delay time of Q_f
α_0	model parameter for calculation of τ_{f1}
α_1	constant for calculation of τ_{f1}
β, β_F	forward low-frequency current gain
β_n	coefficient describing the Avalanche process
β_0	low-frequency current gain
β_R	reverse low-frequency current gain
Γ_{in}	input reflection coefficient
Γ_L	load reflection coefficient
Γ_{ML}	load reflection coefficient for simultaneous conjugate match

Γ_{MS}	source reflection coefficient for simultaneous conjugate match
Γ_{out}	output reflection coefficient
Γ_S	source reflection coefficient
ΔQ_i	hole charge in the internal transistor during a switching process
ΔQ_{r0}	correction charge
μ_{nB}	mobility of base minority charge
μ_n	mobility between base and collector region
μ_{nC0}	mobility of collector charge
η	current crowding factor
$\psi(h)$	emitter current crowding function
τ_f	(total) transit time
τ_{f0}	low-current component of total transit time
τ_{f1}	medium-current component of total transit time
τ_{f2}	high-current component of total transit time
τ_1	time constant for calculation of τ_{f1}
τ_{10}	time constant for calculation of τ_1
τ_{20}	time constant modelling the high current region
τ_{pE0}	minority charge storage time in the neutral emitter
ξ	temperature coefficient (mobility) for epitaxial-collector
ξ_{rBi}	temperature coefficient (mobility) for internal base resistance

ξ_{rBx}	temperature coefficient (mobility) for external base resistance
ξ_{rCx}	temperature coefficient (mobility) for external collector resistance
ξ_{rEx}	temperature coefficient (mobility) for external emitter resistance

Chapter 1

Introduction

1.1 Motivation

Power Amplifier design is sometimes referred as the “black art” of analog design, mainly because typical CAD tools and commercial bipolar transistor (BJT) models do not meet designers’ needs. For instance, most CAD tools - HSPICE for example - are intended for small signal applications thus large signal analyses are difficult to conduct. This makes it tedious to simulate certain figures of merit such as the 1dB compression point or the 3rd order intercept. Some CAD tools offer large signal analysis - Libra for example - but the transistor models available within them are inadequate for accurately analyzing the large signal behavior of power amplifiers. Designers must perform *load-pull measurements*, to determine design data.

In brief, load-pull measurements on bipolar transistors are done by applying a large signal at the base of a common-emitter transistor and varying a complex load at the output until maximum power transfer between the transistor and the load is achieved. Power contours are plotted on a Smith Chart and results are used for the design of the Power Amplifier (PA).

Load-pull measurements are extremely time consuming and expensive. Moreover, when a new technology is introduced, load-pull data are not available at the outset. Fabricating silicon integrated circuits, requires approximately three to six months depending on the

maturity of the process. Consequently, there is a long delay before the designer can start applying a transistor within a certain circuit configuration. The end result is a long delay between the first design iteration and the final product.

Circuit designers have been urged to produce low cost and ultra efficient PAs to accommodate the new trends of wireless communications. Bipolar transistor technologies are thought to be good candidates for these types of circuit applications. While bipolar technologies have indeed matured enough to compete against other technologies, the industry is in need for a more accurate bipolar model than the presently commercially implemented bipolar model, the Spice Gummel Poon model.

The availability of an accurate bipolar transistor model within a simulator with large-signal simulation capabilities may eliminate the need to perform load-pull measurements. The need for prefabricated transistors would be avoided and design time would be largely reduced. HICUM is a newly developed bipolar model which offers options that should in theory give a better prediction of the behavior of a BJT. In practice, are these options as important as they are believed to be? This thesis will give an insight on this issue.

1.2 Objectives

The objectives of this thesis are to implement the High CURRENT Model (HICUM) into the Libra simulator and to compare its performance to the SPICE Gummel-Poon Model (SGPM) for simulation of PA circuits.

Accomplishing these objectives is achieved in two steps. The first consists of implementing the HICUM model into a commercial simulator that is suitable for PA simulation. For this, the Harmonic Balance simulator, Libra (copyright of HP/EEsof

Software Inc.), is chosen. The second step requires the design of a PA using both models. A PA is designed to conform to commercial specifications.

A secondary objective of this thesis is to provide a better understanding of BJT modelling for circuit designers. It is a known fact that too many designers are ignoring critical aspects of modelling. This ignorance is often reflected through the end result of their circuit performance. By learning these critical aspects of modelling, designers may avoid false simulation results before the circuit is fabricated, thus increasing production yield.

1.3 Contributions

This thesis will contribute the following to research:

1. An implementation of the HICUM model into the Libra simulator (trademark of HP/EEsof Software Inc.).
2. An integrated PA is designed and laid out. According to simulations done with the HICUM model, the PA meets commercial specifications. This circuit will be kept in a Nortel module library for future needs. Optimization of the circuit will be done using both the SGPM and HICUM.
3. Literature for a better understanding of bipolar transistor modelling for circuit designers to reduce the existing gap between circuit design and the device modelling.

1.4 Thesis Outline

Chapter 2 contains a brief history of bipolar modelling and will explain why the SGPM is no longer suited to simulate high-speed circuits.

Chapter 3 presents a condensed description of HICUM. The concepts and philosophies behind HICUM along with the major equations governing HICUM are presented. Special

options and modelling issues in HICUM relevant to PA simulations are discussed. An overview of the HICUM implementation into Libra is also given.

Chapter 4 explains the design approach of a PA. The class of operation, the operating conditions and the design specifications are presented. The bipolar technology is described and the strategies, or tactics, chosen for the design are discussed.

Chapter 5 gives a discussion of various layout and packaging considerations. It will be shown that layout and packaging introduces important parasitics which significantly alter the behavior of a PA if not carefully taken into account.

Chapter 6 presents a summary of the accomplishments, some concluding thoughts and recommendations for further work in this area.

Chapter 2

Overview of Traditional Bipolar Transistor Models

Proper transistor modelling forms the basis of any efficient circuit design. Circuit designers need to be familiar with transistor models because the accuracy of their circuit simulations depends greatly on the accuracy of the transistor models. Without proper modelling, a fabricated circuit will not function as predicted by simulations, calling for additional design iterations. The IC market is an extremely fast paced market thus any unnecessary design iteration must be avoided.

There are several types of transistor models, namely, physical models, numerical models and compact models. The type of transistor model of most importance to circuit designers is the compact model because it requires least computational complexity and therefore least simulation time. A compact model is formed by a relatively small set of equations describing the characteristics of lumped elements and voltage or current controlled current sources forming the model's equivalent circuit. The model's equivalent circuit and equations attempt to predict the transistor's behavior under different conditions determined by terminal voltages and currents, frequency of operation and ambient temperature.

Circuit designers are given a set of parameters describing a specific transistor. These parameters are used by the simulator to solve the model's equations. Model parameters are usually provided by the IC process group. They are a function of physical and electrical

effects and technology specific data and are extracted using complicated methods. The method of extraction plays an important part in modelling since a false extraction results in a bad representation of the device. Extraction methods are not discussed in this thesis but good references are [1] and [2].

Like any other aspect of science, modelling began using very basic concepts and has evolved through the years. In this chapter we will discuss the history of bipolar transistor modelling. The simple Ebers-Moll model will be used as a starting point. Then an overview of the Gummel-Poon Model (GPM) and its modified version, the SPICE-GPM (SGPM), is given along with the problems associated with it when utilized for simulation of modern IC applications. Since HICUM is the model of interest for this thesis, its discussion will not be undertaken in this chapter. Instead, Chapter 3 will be entirely dedicated to HICUM.

2.1 Ebers - Moll Model

Ebers and Moll were the first to propose a large-signal bipolar transistor compact model in 1954 [3]. The model was based on the assumption that a bipolar transistor consists of two junction diodes in opposite configuration sharing the same terminal, called the base. The large-signal equivalent circuit of the original Ebers-Moll model is presented in Figure 2.1. The model is based on the injection current relation, meaning the transistor is treated as a current controlled element. The model can be divided in three parts: modelling of the DC operation; effects caused by AC operation; and losses due to series resistances.

Figure 2.1 Large-signal equivalent circuit of the original Ebers-Moll model.

The DC operation is first characterized by the currents produced by the diodes, described by

$$i_f = I_{SE} \left[\exp\left(\frac{V_{BE}}{V_T}\right) - 1 \right] \quad (2.1)$$

and

$$i_r = I_{SC} \left[\exp\left(\frac{V_{BC}}{V_T}\right) - 1 \right] \quad (2.2)$$

The currents transferred to the output of the transistor are given by

$$i_{Tf} = A_f i_f \quad \text{and} \quad i_{Tr} = A_r i_r \quad (2.3)$$

where A_f and A_r are the DC forward and reverse mode current gains respectively. The most common forms for representing the forward and the reverse transfer currents are

$$i_{Tf} = I_S \left[\exp\left(\frac{V_{BE}}{V_T}\right) - 1 \right] \quad (2.4)$$

and

$$i_{Tr} = I_S \left[\exp\left(\frac{V_{BC}}{V_T}\right) - 1 \right] \quad (2.5)$$

where

$$I_S = A_f I_{SE} = A_r I_{SC} \quad (2.6)$$

Junction capacitances, also referred to as depletion capacitances, model the fixed charges in the depletion regions (see Figure 2.2). The junction capacitances are current independent but are a non-linear function of voltage, given by

$$C_{jBE} = C_{jBE0} \left[1 - \frac{V_{BE}}{V_{jE}} \right]^{-M_{jE}} \quad (2.7)$$

where the zero bias depletion capacitance, C_{jBE0} , the junction built-in voltage, V_{jE} . Base-collector and collector-substrate capacitances are calculated similarly by applying their respective model parameters and voltages to the above equation.

Figure 2.2 Cross-section of a simple NPN transistor with parasitic elements.

Diffusion capacitances model the charge due to the mobile carriers in the transistor and are given by:

$$C_{dE} = \tau_F \frac{i_f}{V_{BE}} \quad \text{and} \quad C_{dC} = \tau_R \frac{i_r}{V_{BC}} \quad (2.8)$$

where τ_F and τ_R are model parameters characterizing the forward and reverse transit times.

R_{Bx} , R_{Cx} and R_{Ex} are operating point independent series resistances. They are included in the equivalent circuit to model ohmic potential drops between the external contacts (nodes C, B, E in Figure 2.1) and the internal nodes (nodes C', B' and E' in Figure 2.1). As shown in Figure 2.2 , R_{Cx} is composed of the collector contact resistance and the sum of series resistance leading to the collector base region. R_{Bx} is mostly composed of the base contact resistance and the high resistivity p-type semiconductor forming the base of the NPN transistor finally. R_{Ex} is largely associated to the emitter contact resistance.

The Ebers-Moll model formed the basis of bipolar models. Its main problem is that it was not developed for easy implementation for CAD tools, since there were none in 1954. With an increasing complexity in applications of the BJT the Ebers-Moll model is no longer sufficient to accurately model the BJT. The Gummel-Poon model was developed as an improvement to the Ebers - Moll model.

2.2 Gummel - Poon Model

An extended Ebers-Moll model was provided in 1970 by Gummel and Poon [4]. The Gummel-Poon Model (GPM) presents a more physics-based model with ease of implementation into circuit simulators. Its equivalent circuit follows the same topology as the Ebers-Moll model, but the equations governing the lumped elements were altered to take into account numerous physical effects. These physical effects add non-linearities to

the operation of the BJT. Essentially, three physical effects were introduced: high-level injection, basewidth modulation, and transit time (τ_f) variation with I_C [5].

The model is based on the Integral Charge-Control Relation (ICCR) which treats the bipolar transistor as a charge controlled element. This is in contrast to the Ebers-Moll model where the BJT is treated as a current controlled element. The forward and reverse transfer currents are now defined as:

$$\begin{aligned} i_{Tf} &= \frac{I_S}{Q_p/Q_{p0}} \left[\exp\left(\frac{V_{BE}}{V_T}\right) - 1 \right] \\ &= \frac{i_{Te}}{Q_p/Q_{p0}} \end{aligned} \quad (2.9)$$

and

$$\begin{aligned} i_{Tr} &= \frac{I_S}{Q_p/Q_{p0}} \left[\exp\left(\frac{V_{BC}}{V_T}\right) - 1 \right] \\ &= \frac{i_{Tc}}{Q_p/Q_{p0}} \end{aligned} \quad (2.10)$$

where i_{Te} and i_{Tc} represent the ideal transfer currents.

Comparing (2.9) and (2.10) to (2.4) and (2.5) reveals that the difference between the transfer currents of the Ebers-Moll model and the GPM is the Q_p/Q_{p0} term. By definition, Q_{p0} is the zero-bias majority carrier base charge and Q_p is the total bias dependent majority carrier base charge. Gummel and Poon have partitioned Q_p into physical components:

$$Q_p = Q_{p0} + Q_{JE} + Q_{JC} + Q_f + Q_r \quad (2.11)$$

where Q_{jE} and Q_{jC} are the charges in the BE and BC depletion regions respectively,

$$Q_{jE} = \int_0^{V_{BE}} C_{jBE} dv \quad (2.12)$$

$$Q_{jC} = \int_0^{V_{BC}} C_{jBC} dv \quad (2.13)$$

and Q_f and Q_r are the charges associated to the mobile carriers for forward and reverse operation respectively,

$$Q_f = \int_0^{V_{BE}} C_{dE} dv = \tau_f i_{Tf} \quad (2.14)$$

$$Q_r = \int_0^{V_{BE}} C_{dC} dv = \tau_r i_{Tr} \quad (2.15)$$

The first modelling error [2] in the GPM and all of its variants consists in the definition of the transit times, τ_f and τ_r . According to (2.14) and (2.15), the model's authors have set

$$\tau = \frac{Q}{I} \quad (2.16)$$

which corresponds to a DC or static definition of the transit time. A more proper definition of τ is

$$\tau = \frac{dQ}{dI} \quad (2.17)$$

since it is determined from small-signal measurements. Figure 2.3 shows the forward transit time versus collector current density where $\tau_{f(dc)}$ is calculated on the basis of the GPM's static definition and $\tau_{f(ac)}$ is calculated on the basis of the small-signal definition

[2]. The result is a very optimistic value of $\tau_{f(dc)}$ in the high current operating region, if $\tau_{f(dc)}$ is interpreted as $\tau_{f(ac)}$ which is usually the case in parameter extraction.

Figure 2.3 Comparison of Small-Signal and DC definition of τ_f [2]

Substituting (2.14) and (2.15) into (2.11) and the result into (2.9) gives:

$$i_{Tf} = \frac{i_{if}}{Q_{p0} + Q_{jE} + Q_{jC} + \tau_f i_{Tf} + \tau_r i_{Tr}} \cdot Q_{p0} \quad (2.18)$$

Equation (2.18) is an implicit function on i_{Tf} and can only be solved numerically if τ_f is a function of i_{Tf} . When the GPM was first introduced, solving equations with numerical methods was not convenient since today's high performance computers were not available. Consequently, i_{Tf} and i_{Tr} in (2.14) and (2.15) were replaced by the ideal transfer current i_{Te} and i_{Tc} and as further simplification, τ_f and τ_r were assumed to be current independent:

$$Q_f = \tau_f i_{Te} \quad (2.19)$$

$$Q_r = \tau_r i_{Tc} \quad (2.20)$$

Grouping the current independent and the current dependent charges of (2.11) together:

$$Q_1 = Q_{p0} + Q_{jE} + Q_{jC} \quad (2.21)$$

and

$$Q_2 = Q_f + Q_r \quad (2.22)$$

Equation (2.11) becomes:

$$Q_p = Q_1 + Q_2 \cdot \frac{Q_{p0}}{Q_p} \quad (2.23)$$

Multiplying both sides of (2.23) by Q_p and solving the quadratic equation gives:

$$Q_p = \frac{Q_1}{2} \pm \sqrt{\left[\frac{Q_1}{2}\right]^2 + Q_{p0}Q_2} \quad (2.24)$$

The positive root gives a plausible solution because Q_p is always larger than Q_{p0} , thus:

$$Q_p = \frac{Q_1}{2} + \sqrt{\left[\frac{Q_1}{2}\right]^2 + Q_{p0}Q_2} \quad (2.25)$$

Circuit simulator vendors each have their own methods for calculating the charges needed for solving (2.25). The most popular method is seen in the next section when the Spice-GPM, a variant of the GPM is discussed.

2.3 Spice Gummel - Poon Model

The SGPM is the most widely used bipolar model. It is implemented in a wide range of circuit simulators such as HSPICE, PSPICE, Libra, Eldo and Spectre. The basis of the SGPM is indeed the GPM but with several simplifications for easy implementation and reduction of computation time. Components were added to the equivalent circuit in order to model additional effects, as shown in Figure 2.4. In this section, the basic equations of

the SGPM are discussed. For an extensive description of the SGPM, please refer to [6] and [7].

Figure 2.4 SGPM equivalent circuit

2.3.1 Transfer Current Derivation

The normalized form of (2.25) is referred as q_b and is given by:

$$q_b = \frac{q_p}{q_{p0}} = \frac{Q_1/Q_{p0}}{2} \left[1 + \sqrt{1 + \frac{4(Q_2/Q_{p0})}{(Q_1/Q_{p0})^2}} \right] \quad (2.26)$$

Three simplifications were made to this equation. The first consists of the normalized depletion charge (Q_1/Q_{p0}).

$$q_1 = \frac{Q_1}{Q_{p0}} = \frac{1}{1 - \frac{v_{BE}}{V_{Ar}} - \frac{v_{BC}}{V_{Af}}} \quad (2.27)$$

The presence of V_{Af} and V_{Ar} are consequences of Early-effects. The forward Early-effect is responsible for the slope of I_C in the active region. Extrapolating the DC characteristics of I_C in the active region of the transistor (see Figure 2.5) shows that all lines intersect the origin at the same voltage (V_{Af}). The reverse Early voltage, V_{Ar} has the same effect when

the base-emitter diode is reverse biased but this is seldom the case in analog design. Note that the physical explanation of the Early effect is the voltage dependence of the base width [8].

Figure 2.5 Illustration of the Forward Early effect

The second simplification is the normalized minority charge which is approximated by:

$$q_2 = \frac{Q_2}{Q_{p0}} = \frac{i_{if}}{I_{kf}} + \frac{i_{ir}}{I_{kr}} \quad (2.28)$$

The forward knee current (I_{kf}) defines the onset of high-level injection for forward operation. As seen in the gummel plot shown in Figure 2.6, the slope of I_C changes when V_{BE} reaches a certain threshold. This change in slope is caused by high-level injection effects. The physical explanations for high-level injection are derived in [4]. Similarly, the reverse knee current (I_{kr}) defines the onset of high-level injection for reverse operation.

Figure 2.6 Illustration of the Forward Knee Current

Substituting the left hand side of (2.27) and (2.28) into (2.26) gives (2.29).

$$q_b = \frac{q_1}{2} \left[1 + \sqrt{1 + \frac{4(q_2)^2}{(q_1)^2}} \right] \quad (2.29)$$

Equation (2.29) is further simplified, depending on the level of current injection. A first level is referred as *low level injection* and occurs when

$$4q_2 \ll (q_1)^2 \quad (2.30)$$

In this operating region, (2.29) simplifies to

$$q_b = \frac{q_1}{2} \quad (2.31)$$

The second level is referred as the *high-level injection* and occurs for

$$4q_2 \gg (q_1)^2 \quad (2.32)$$

and (2.29) reduces to

$$q_b = \sqrt{q_2} \quad (2.33)$$

The medium level injection case is given by the solution of the quadratic equation, (2.26).

In addition to the normalized base charge q_b , non-ideality coefficients were introduced in (2.9) and (2.10) to give the final form of forward and reverse transfer currents, (2.34) and (2.35). The non-ideality coefficients, n_f and n_r are technology specific parameters. Their values are typically between 1.002 and 1.01. Their usage models small changes in the neutral emitter widths and current reduction due to recombination [7].

$$i_{Tf} = \frac{I_S}{q_b} \left[\exp\left(\frac{V_{BE}}{n_f V_T}\right) - 1 \right] \quad (2.34)$$

$$i_{Tr} = \frac{I_S}{q_b} \left[\exp\left(\frac{V_{BC}}{n_r V_T}\right) - 1 \right] \quad (2.35)$$

The typical application of the BJT is characterized with $V_{BE} > 0$ and $V_{CE} > 0$, in which case $i_{Tr} = 0$. Assuming $V_{Ar} \rightarrow \infty$ and $I_{Kr} = 0$, the collector current is given by:

$$I_C = i_{Tf} = \begin{cases} I_S \cdot 2 \left(1 - \frac{v_{BC}}{V_{Ar}} \right) \exp\left(\frac{V_{BE}}{n_f V_T}\right) & 4q_2 \ll (q_1)^2 \\ \sqrt{I_S} \cdot I_{Kf} \exp\left(-\frac{V_{BE}}{2V_T}\right) & 4q_2 \gg (q_1)^2 \end{cases} \quad (2.36)$$

2.3.2 Base Current

According to the equivalent circuit shown in Figure 2.4 , the base current is composed of four components.

$$i_B = i_f + i_r + \frac{i_{Te}}{\beta_f} + \frac{i_{Tr}}{\beta_r} \quad (2.37)$$

The first two components are the currents flowing through the BE and BC diodes respectively:

$$i_f = I_{SE} \left[\exp\left(\frac{V_{BE}}{n_{SE} V_T}\right) - 1 \right] \quad (2.38)$$

and

$$i_r = I_{SC} \left[\exp\left(\frac{V_{BC}}{n_{SC} V_T}\right) - 1 \right] \quad (2.39)$$

where I_{SE} , n_{SE} , I_{SC} and n_{SC} are model parameters describing the nature of the diodes. The last two terms consist of the ideal forward and reverse transfer currents, from (2.14) and (2.15), divided by their respective current gains. For forward operation, which is usually the case, the conditions are $V_{BE} > 0$ and $V_{BC} < 0$ thus $i_r \approx 0$ and $i_{Tr} \approx 0$. Consequently the base current can be reduced to two components, i.e.:

$$i_B = i_f + \frac{i_{Te}}{\beta_f} \quad (2.40)$$

2.3.3 Base Resistance

In the Ebers-Moll model the base resistance was made to be bias independent. In the SGPM, the base resistance is separated in two parts, as shown in Figure 2.7 . The bias independent resistance (r_{B0}) models the extrinsic component of the base resistance which

is composed of the external contact resistance and the sheet resistance of the external base region. The intrinsic base resistance (r_{Bi}) is formed by the region directly under the emitter and is bias dependent because of base conductivity modulation and DC current crowding. Current crowding for the AC behavior is not modelled in the SGPM.

Figure 2.7 Separation of Base Resistance into two parts

Two methods are employed [6] for calculating the total base resistance depending on the value of a model parameter labelled “IRB”. This parameter indicates the base current at which the base resistance is halfway between its zero-bias and minimum values.

If $IRB=0$, then

$$r_B = r_{Bo} + \frac{r_{Bi} - r_{Bo}}{q_b} \quad (2.41)$$

with q_b as discussed earlier in this chapter and $r_{Bi} > r_{Bo}$.

If $IRB > 0$, then

$$r_B = r_{Bo} + (r_{Bi} - r_{Bo}) \left(\frac{1}{1 + 3 \left(\frac{i_B}{IRB} \right)^{0.852}} \right)^{\frac{1}{2}} \quad (2.42)$$

For *low level injection*, $q_b \approx 1$ and $I_B \ll IRB$ and both (2.41) and (2.42) give

$$r_B \rightarrow r_{Bi} \quad (2.43)$$

For *high level injection*, $q_b > 1$ and $I_B \gg IRB$, thus

$$r_B \rightarrow r_{B0} \quad (2.44)$$

Since often $r_{B0} < r_{Bi}$, the effect of DC current crowding is a reduction of the total base resistance.

2.3.4 Capacitances

Depletion capacitances follow the same relation as the Ebers-Moll model, rewritten here in (2.45) where the 'x' can be replaced by either B'E', B'C' or C'S'.

$$C_{jx} = \frac{C_{jx0}}{\left[1 - \frac{V_x}{V_{jx}}\right]^{M_1}} \quad (2.45)$$

Depletion capacitances increase rapidly for forward biasing ($V_x > 0$) and (2.45) reveals that if $V_x \rightarrow V_{jx}$ then $C_{jx} \rightarrow \infty$. In reality this is not the case. For automated calculation, the purpose of CAD tools, it is important to avoid this problem thus the SGPM uses (2.46) to calculate a depletion capacitance when V_x approaches V_{jx} .

$$C_{jx} = \frac{C_{jx}}{(1 - F_C)^{M_1}} \left[1 + \frac{M_1(V_x - F_C V_{jx})}{V_{jx}(1 - F_C)} \right] \quad (2.46)$$

The condition for using (2.46) instead of (2.45) is $V_x > F_C V_{jx}$ where F_C is a parameter which takes a value between 0 and 1. Note that for normal operation of the BJT, only the BE junction is forward biased thus equation (2.46) mostly applies to C_{jBE} .

Diffusion capacitances are more complicated to model because they depend on a transit time that is current dependent. The emitter diffusion capacitance C_{dE} is modelled by

$$C_{dE} = \frac{\partial}{\partial V_{B'E'}} (\tau_{FF} i_{TF}) \quad (2.47)$$

where the current dependent transit time, τ_{FF} is modelled by [6]:

$$\tau_{FF} = \tau_F \left[1 + X_{TF} \left(\frac{i_{if}}{i_{if} + I_{TF}} \right)^2 \exp \frac{V_{B'C'}}{1.44 V_{TF}} \right] \quad (2.48)$$

where X_{TF} , I_{TF} , V_{TF} and τ_F are model parameters. At *low level injection*, $i_{if} \ll I_{TF}$ and according to (2.48), $\tau_{FF} \rightarrow \tau_F$ hence τ_F is referred as the low current forward transit time.

Equation (2.48) is purely empirical without any physical concepts except for the inclusion of τ_F . Instead, it makes use of fitting numbers such as the 1.44 constant to “fit” simulation results to measurements. This type of equation is often used in the SGPM and introduces problems when conducting yield analysis. This subject will be discussed in more details in Chapter 3.

The collector-base diffusion capacitor is modelled by

$$C_{dC} = \tau_R \left[\frac{I_S}{n_r V_T} \exp \frac{V_{B'C'}}{V_T} \right] \quad (2.49)$$

where τ_R is a model parameter describing the low current reverse transit time.

Figure 2.4 shows two capacitors, C_{B1} and C_{B2} , between the internal base node and the internal collector. These are a combination of C_{jBC} and C_{dC} . If C_{BC} is the total collector-base capacitance, then

$$C_{BC} = C_{jBC} + C_{dC} \quad (2.50)$$

The physical distance between the external base node and the internal base node can not always be considered infinitesimally small (see Figure 2.2). It is therefore important to distribute C_{BC} across R_B . The distribution is dependent on the nature of the process technology and the layout format of the BJT. Consequently, the SPGM employs a partitioning factor to distribute C_{BC} across R_B such that

$$C_{B1} = C_{BC}(1 - X_{CJC}) \quad (2.51)$$

and

$$C_{B2} = C_{BC}X_{CJC} \quad (2.52)$$

where X_{CJC} is the partitioning factor. Further explanations on this concept of capacitance distribution will be undertaken in Chapter 3 when HICUM is discussed.

2.3.5 Problems Associated with the SGP Model

For many years the SGP model was never modified to properly model the changes brought to bipolar fabrication techniques and the operating conditions imposed by modern applications. Modern bipolar applications have extended from the megahertz frequencies to the gigahertz frequencies. Transistor dimensions have been reduced by factors in the one hundred to one thousand range. It is understood in [9] that the SGP model must be enhanced to remain the bipolar model of choice by the design community. Some of these problems were discussed in this chapter. The problems associated to the SGP model that are relevant to PA simulations are [10]:

- improper modelling of the high current region
- inconsistencies in treatment of excess phase (non quasi-static (NQS) effects)
- parameter extraction and yield analysis
- lack of modelling of the avalanche generation and breakdown region
- no modelling of self-heating

These will be discussed in the next chapter when advantages associated to HICUM are presented.

Chapter 3

HICUM

HICUM is the result of bipolar modelling research conducted by Schröter, Rein *et al.* [12] - [16] at Ruhr University, Bochum, Germany. The first version was published in 1986 and its validity was verified with high speed digital circuits using ECL logic. The name HICUM was derived from the fact that special attention was paid to the operation of the BJT at high current densities (High CUrrent Model). Since its first appearance, the model has always been updated to accommodate the changes brought to bipolar fabrication techniques. For various reasons the model took a long time before being implemented into a commercial circuit simulator. In fact, to this date HICUM is not offered to the industry by any commercial circuit simulator vendor. For the last few years, HICUM was Nortel's proprietary model where it was implemented in Eldo and Spectre for use by the organization only.

The equations governing the HICUM model are much more complicated and numerous than the ones for the SGPM. Understanding them requires a more in-depth look at the physical properties of the BJT. For this reason, this chapter will simply look at a subset of equations and principles that are more relevant to power amplifier simulations. For a more detailed description of HICUM please refer to [12] - [16].

As part of this thesis HICUM was implemented into the Libra simulator. This was done to aid RF circuit designers at Nortel. Section 3.3 will summarize the implementation, discuss

problems encountered during the implementation and state those that remained unresolved.

3.1 Equivalent Circuit

The equivalent circuit for the HICUM model is shown in Figure 3.1 . At first glance, the equivalent circuit looks quite similar to the SGPM's equivalent circuit shown in Figure 2.4 but with additional lumped elements. This is somewhat true except that the components do not necessarily model the same effects as in the SGPM. For instance, both models contain four diodes but two of them model completely different effects. In HICUM, the i_{Tc}/β_R and i_{Tc}/β_F diodes are not used because the authors did not consider the current gain as a physically independent parameter. Instead these diodes were replaced by independent components I_{BEi} and I_{BCi} and additional elements such as the I_{BCx} and the I_{BEp} diodes were added to model effects that have become more important with the introduction of modern BJT fabrication techniques.

Figure 3.1 HICUM equivalent circuit

Indeed, modern fabrication techniques, which have greatly reduced the dimensions of the transistor have introduced many phenomena that were not present when the SGPM was first published. Figure 3.2 shows cross sections of two types of bipolar technologies: a $2\mu\text{m}$ standard technology and an advanced self-aligning polysilicon technology [17]. Although $0.5\mu\text{m}$ self-aligning polysilicon technologies are presently available, Figure 3.2 clearly demonstrates that physical dimensions have been reduced quite significantly.

Figure 3.2 Comparison of standard and self-aligning polysilicon bipolar technologies [17]

A first example of a lumped element resulting from the reduction of dimensions is the presence of the base-emitter oxide capacitance (C_{Eox}). The basic equation of a plate capacitance ($C = \epsilon A/d$) indicates that a capacitance is inversely proportional to the

distance between the two plates. Comparing both modern and old transistors reveals that the oxide spacer thickness between the emitter contact and the base contacting polysilicon has reduced significantly giving rise to C_{Eox} .

A second example is the presence of the emitter periphery capacitor, C_{jEp} , which models the junction formed by the BE periphery as opposed to the bottom junction modelled by C_{jEi} (see Figure 3.3). With the reduction of emitter area, A_E , the ratio of peripheral junction to bottom junction has increased greatly and both should not be combined together as in the SGPM.

Figure 3.3 Peripheral and bottom emitter-base diodes (not to scale)

HICUM also has two diodes for modelling the base-collector junction. The first, I_{BCi} models the current flowing through what is often called the internal transistor which consists of the section directly under the emitter. The second models the junction which surrounds the internal transistor (see Figure 3.4).

Figure 3.4 Internal and external base-collector diodes

The base resistance in HICUM is separated into two parts, a bias independent resistor (R_{Bx}) and a bias dependent one (R_{Bi}). This is similar to the SGPM except that an extra node (B^*) was inserted between both resistors. The reason for inserting an extra node is to separate the internal transistor from the peripheral and external transistor. The p-type material forming the base of the transistor has a certain sheet resistance. This causes voltage drops along the base region as demonstrated in Figure 3.5. Although the voltage drop may not be very large, its consequence is important because a diode current is an exponential function of voltage, i.e. (2.1). In fact, the voltage difference is sometimes significant enough to cause I_{BCi} , C_{jCi} and C_{jEi} to be a few orders of magnitude lower than their respective external and peripheral counterparts. The internal BC diode can often be neglected to reduce computational time without affecting the overall accuracy.

Figure 3.5 Potential drops across the base region

Two capacitors (C'_{BCx} , C''_{BCx}) were inserted on either side of R_{Bx} . The sum of both capacitors is given by:

$$C'_{BCx} + C''_{BCx} = C_{Cox} + C_{jBCx} \quad (3.1)$$

where C_{Cox} is a linear capacitor given as a model parameter and C_{jBCx} is a non-linear capacitor calculated using (3.2).

$$C_{jBCx} = C_{jBCx0} \left[1 - \frac{V_{BCx}}{V_{jBCx}} \right]^{-M_{BCx}} \quad (3.2)$$

The right hand side of (3.1) is partitioned across R_{Bx} with the help of a model parameter referred as a partitioning factor and labelled f_{BC} . The value of f_{BC} ranges between 0 and 1 depending on fabrication techniques and transistor layout. Good partitioning of these capacitors is needed to produce the proper input time constant and input impedance of the transistor. The SGPM also has partitioned capacitors across R_{Bx} (see Figure 2.4). However a method for calculating the partitioning factor was never published. Often the capacitors are estimated using an area ratio or by s-parameter measurements.

A current source (I_{AVL}) is used to model avalanche multiplication effects. Avalanche multiplication, or avalanche generation, takes place when the base-collector voltage exceeds a threshold voltage. This voltage depends on the technology and is in the order of 3V for modern technologies. The overall effect is a dramatic increase in the collector current and a transistor breakdown if overly exceeded. In a power amplifier circuit, the base-collector voltage may be increased above the threshold voltage in order to maximize the output power. Consequently, the avalanche process will be discussed in more details later in this chapter.

The thermal network in Figure 3.1 is used to model self-heating. Self-heating is a process causing an increase in temperature due to thermal dissipation of current flowing through a

resistive element. A transistor's electrical response is deeply coupled to its internal (and surrounding) temperatures. A change in temperature will affect currents which in turn affects the temperature. It is important to model this relation between temperature and electrical behavior of a transistor, especially when dealing with high currents such as in power amplifier circuits. As for the avalanche generation, self-heating will be discussed in more detail.

The internal resistance shunt capacitance (C_{rbi}) is included in the equivalent circuit to take into account high-frequency emitter current crowding.

The series substrate resistance (R_{SU}) may be used for a first order modelling of low-frequency inter-device substrate coupling. However, in most cases this resistance is omitted, since it is very difficult to measure accurately.

3.2 Interesting HICUM Options for Power Amplifiers

Power amplifiers present operating conditions not normally addressed in conventional integrated circuits such as LNAs and digital circuits. The most evident are high current operation and large signal swings. These operating characteristics can produce excessive heat affecting the electrical behavior of the BJT. They add extra non-linearities to the BJT known as high current effects and non-quasi static (NQS) effects. They also give rise to a new source of current called the avalanche generation current. Finally, they test the limits of a given process in terms of power handling. To minimize design iterations and avoid post-fabrication problems, it is important to access a bipolar model capable of predicting the mentioned effects.

HICUM was formulated by paying special attention to the physics of the BJT when operated in such operating conditions. This section will discuss these features thought to be important for proper modelling of the BJT when utilized in power amplifier circuits.

3.2.1 High Current Effects

Many bipolar characteristics are a function of collector current density. Collector current density of a BJT is the ratio of collector current over emitter area:

$$J_C = \frac{I_C}{A_E} \quad \left[\frac{mA}{\mu m^2} \right] \quad (3.3)$$

According to the authors of HICUM [12], the trend to further raise the switching speed and to further reduce the dimensions of high-speed bipolar transistors requires an increase of collector current density. As a result, proper modelling of this operating region is an important issue and will only become more important as bipolar applications and fabrication techniques mature.

HICUM is based on the integral charge-control relation (i.e. (2.9) and (2.10)) introduced by Gummel and Poon although the method is applied more consistently. A comparison of the output DC characteristics and transit time for the SGPM, HICUM, 1D device simulation and measurements is shown in Figure 3.6 and Figure 3.7 to demonstrate the capability of the intrinsic model formulation in Figure 3.2.

High current effects are characterized by a steep increase in the transit time as a result of the extension of the effective base into the epitaxial collector. The dotted line in Figure 3.6 defines the onset of high-current effects. In HICUM, this limit is referred as the *critical current* and was developed in [12] as:

$$I_{CK} = \frac{V_c}{r_{ci0}} \cdot \frac{1}{\sqrt{1 + \left(\frac{V_c}{V_{lim}}\right)^2}} \cdot \begin{cases} 1 & V_c \leq V_{lim} \\ 1 + \frac{V_c - V_{lim}}{V_{PT}} & V_c > V_{lim} \end{cases} \quad (3.4)$$

where $V_c = V_{CE} - V_{CES}$ with V_{CES} as the *internal saturation voltage* roughly approximated by 0.1V, r_{ci0} is the series resistance of the metallurgical epitaxial collector region below the emitter at zero electric field, V_{lim} is the voltage drop across this region when the field dependence of the electron mobility becomes dominant, and V_{PT} is the *punchthrough voltage* of the epitaxial collector.

Figure 3.6 DC output characteristics comparing SGPM and HICUM[2]

According to Figure 3.6, the saturation region of the transistor which is characterized with $V_{CE} < 0.2V$ is part of the high-current region, independently of the drive level (I_B). It will

be shown in Chapter 4 that proper modelling of the saturation region is particularly important for PA applications.

For low injection the SGPM shows reasonable accuracy in the prediction of I_C . In the saturation region, we see a discrepancy in the output transconductance (slope of I_C). As the simulation enters the high current region, the SGPM quickly deviates from the measurements.

The HICUM model gives a sound prediction of measurements in the entire operation region.

Figure 3.7 Transit time (τ_f) comparison of SGPM and HICUM[2]

Two discrepancies are noticed in the prediction of τ_f by the SGPM in Figure 3.7. The first is at low current densities where τ_f measurements show a dependency on V_{CE} . This dependency is a result of the Early effect discussed previously in Chapter 2. In the SGPM the Early effect is used to model the DC characteristics, i.e. (2.27), but is omitted when τ_f is concerned. The second discrepancy is at high current density where the SGPM's τ_f is

optimistic compared to measurements. Only a small V_{CE} range can be approximated properly.

Improved modelling of the high current region is achieved in HICUM by proper modelling of τ_f , which is achieved by dividing τ_f into three parts defined in Figure 3.8 and in (3.5).

$$\tau_f = \tau_{f0} + \tau_{f1} + \tau_{f2} \quad (3.5)$$

Each of the components are estimated using simple formulas combining first-order physical mechanisms in the transistor and results of numerous simulations and experiments with modern high-speed transistor technologies. Most importantly, the equations are easily modified to adopt to changes brought to transistors by new fabrication techniques. In 1987, the equations for τ_{f0} , τ_{f1} , and τ_{f2} were given in [12] as:

$$\tau_{f0} = \tau_0 \left[1 - \sqrt{\frac{V_c}{V_A}} + \frac{V_1}{V_c} \right] \quad (3.6)$$

$$\tau_{f1} = \begin{cases} 0 & I_C \leq I_1 \\ \frac{\tau_1}{2} \left[\left(\frac{I_C - I_1}{I_{CK} - I_1} \right)^2 + \left(\frac{I_C - I_1}{I_{CK} - I_1} \right)^\alpha \right] & I_1 < I_C < I_{CK} \\ \tau_1 & I_C \geq I_{CK} \end{cases} \quad (3.7)$$

$$\tau_{f2} = \begin{cases} 0 & I_C \leq I_{CK} \\ \tau_{20} \left[1 - \left(\frac{I_{CK}}{I_C} \right)^2 \right] + s_{20}(I_C - I_{CK}) & I_C > I_{CK} \end{cases} \quad (3.8)$$

In (3.6), V_A is the Early Voltage modelling the V_{CE} dependency and the V_1/V_c term models the low electric field reduction in the drift velocity of the minority carriers at the

base-collector junction where V_1 is in the order of 0.05V. In (3.7), α is required to assure a continuous slope at $I_C = I_{CK}$ and I_1 is a semi-empirical expression indicating the start of the slight increase in τ_f . In (3.8), s_{20} defines the slope of τ_f at very high collector density. The model parameters needed for the analysis of the transit time are thus $\tau_0, \tau_{10}, \tau_{20}, V_A, V_1, V_{lim}, V_{PT}, r_{ci0}, s_{20}$ and α_1 .

Figure 3.8 Definition of the parameters used in the analytical τ_f approximation [12]

3.2.2 Modelling of Avalanche Generation

HICUM contains an avalanche generation model for the base-collector junction. Avalanche generation causes an exponential increase in collector current when the BC junction is reverse biased beyond a certain voltage (see Figure 3.9). If the BC junction is reversed biased too far into the avalanche regime, the transistor will reach breakdown. The model is characterized as being a “weak” avalanche model meaning its intentions are only to give an indication of the start of avalanche and is not meant for simulation of BJTs operating deeply into the avalanche regime or at breakdown.

Avalanche generation is caused by a physical mechanism referred to as impact ionization. At high reverse voltage, the carriers gain sufficient kinetic energy to shatter the bonds

between silicon atoms. This action leads to an increase in electron-hole pairs. These newly generated carriers are quickly accelerated by the large electric field, which in turn generates more carriers. This process continues and rapidly leads to the generation of a large number of carriers and hence a large reverse current.

Figure 3.9 Effect of avalanche generation on collector current in HICUM

The model equation for the I_{AVL} element in Figure 3.1 is based on the physical relationship [2]

$$I_{AVL} = I_T \int_0^{w_{BC}} \alpha_n \exp\left(-\frac{b_n}{|E|}\right) dx \quad (3.9)$$

where E is the electrical field across the junction, w_{BC} is the width of the BC depletion region, x is the ordinate in the vertical direction, α_n and b_n are coefficients describing the

avalanche process. From this, an equation was derived [2] which is more suitable for compact models,

$$I_{AVL} = \begin{cases} 0 & , V_{BC} \geq 0 \\ I_T f_{AVL} (V_{DCi} - V_{BC}) \exp\left(\frac{q_{AVL}}{C_{jCi} (V_{DCi} - V_{BC})}\right) & , V_{BC} < 0 \end{cases} \quad (3.10)$$

where f_{AVL} and q_{AVL} are new model parameters which depend on physical data and emitter area, C_{jCi} is the internal BC capacitance and V_{DCi} is the built-in voltage for the BC junction.

From a numerical point of view, the implementation of I_{AVL} is difficult to achieve in a compact model. Efficient simulation and design of circuits in the avalanche regime depends on the numerical robustness of the particular circuit simulator. Consequently, the avalanche generation model can significantly increase simulation time or may even cause severe convergence problems if not carefully implemented. The avalanche generation model may be turned off by setting f_{AVL} to zero.

3.2.3 Temperature Scaling and Modelling of Self-Heating

Electrical characteristics of BJTs are strongly coupled to temperature. For example, a temperature dependent factor is the thermal voltage ($V_T = kT/q$) in the diode equation, i.e. (2.38). Often it is the model's parameters that are temperature dependent. At the start of a simulation, model parameters are scaled according to the device temperature. There are two mechanisms affecting a device's temperature. The first is characterized by the ambient temperature and the second by the transistor's self-heating effects.

The ambient temperature is indicated to the simulator via a simulation control variable. It is estimated by the designer according to the real life conditions under which the circuit will operate. For instance, if the application of the circuit is in a communication tower near

the earth's equator, the ambient temperature may be set to 90°C. The ambient temperature is involved in a unidirectional process, meaning the ambient temperature affects a transistor's behavior but transistor's behavior produces no change in the ambient temperature.

When self heating is included in the modelling, the thermal information is involved in a bidirectional process. The operation of the transistor produces heat, affecting the device's temperature. This new temperature is then coupled to the model's equations. Device temperature and model equations are constantly updated.

Modelling of self heating effects requires a method for properly evaluating the change in temperature according the physical nature of the transistor and its ability to dissipate heat. In HICUM, self-heating is modelled the same way as demonstrated in [21] for modelling of the HBT. The model uses a thermal circuit as shown on the left of Figure 3.10 . The thermal resistor, R_{th} , models the proportional increase in junction temperature due to power while the thermal capacitor, C_{th} , models the time delay associated with the change in temperature. The units for R_{th} and C_{th} are not the typical units of resistors and capacitors. They were properly chosen to calculate the junction temperature, T_j .

Figure 3.10 Thermal network versus electrical network

The advantage of calculating a junction temperature using the topology of an electrical circuit is the ease of implementation into a circuit simulator. The thermal network is implemented as an electrical circuit and the simulator is responsible for solving the equations. The node voltage T_j is interpreted as a junction temperature. The final device temperature is thus:

$$T_{device} = T_{ambient} + T_j \quad (3.11)$$

According to Figure 3.10 the steady state junction temperature is given as:

$$T_j = P_{dis} \cdot R_{th} \quad (3.12)$$

The current source, P_{dis} , corresponds to the thermal power dissipated in the device. Since most of the electrical power in a resistive element is dissipated as thermal energy,

$$P_{dis} \approx V_{CE} \cdot I_C + V_{BE} I_B \quad (3.13)$$

Inserting (3.12) and (3.13) into (3.11) gives,

$$T_{device} = T_{ambient} + R_{th} \cdot (V_{CE} \cdot I_C + V_{BE} I_B) \quad (3.14)$$

Equation (3.14) indicates that T_{device} is proportional to current flowing in the transistor. In circuit applications such as power amplifiers, the collector current is relatively high and self-heating is expected to play an important role in the electrical behavior of the transistor.

The authors of HICUM have carefully studied the temperature dependency of the HICUM parameters. They have included equations to scale parameters to ambient temperatures ranging between 250K and 400K [15].

3.2.4 Non Quasi-Static Effects

The equations discussed in Chapter 2 assumed that the carriers within the transistor followed the electric field without any delay. In reality, carriers travel through the various transistor regions with a finite velocity thus in a finite time. This *Non Quasi-Static (NQS) effect* occurs in high-frequency circuit applications, where “high-frequency” is dependent on the technology employed. There are two forms of NQS effects, one in the lateral direction and the other in the vertical direction.

The NQS effect in the lateral direction is caused by AC emitter crowding at high frequencies. At high operating frequencies, the impedance seen into the internal base is reduced and an imaginary part appears [18]. To model the imaginary part, C_{rbi} was introduced in HICUM. An analytical treatment of the input impedance of transistors with long emitters stripes showed that for frequencies below f_T ,

$$C_{rbi} = f_{C_{rbi}} \cdot C_i \quad (3.15)$$

where $f_{C_{rbi}}$ is a model parameter ranging between 0 and 1 and C_i is the total capacitance connected to the node B'. From theory, $f_{C_{rbi}} = 0.2$.

Compact modelling of NQS effects in the vertical direction was first published in [19] where it was shown that at high frequencies the minority charge (Q_f) and the transfer current (i_T) react delayed with respect to the voltages across the BC and the BE junctions. In HICUM, it is modelled with the introduction of two additional delay times τ_2 and τ_m for both i_T and Q_f respectively. These additional delay times were made operating point dependent by relating them to the small signal transit time (τ_f) by:

$$\tau_2 = \alpha_{Q_f} \tau_f \quad (3.16)$$

and

$$\tau_m = \alpha_{iT} \tau_f \quad (3.17)$$

where α_{Qf} and α_{iT} are two model parameters. The fact that α_{Qf} and α_{iT} are simply model parameters indicates that they are not dependent on current. It was shown in [20] that α_{Qf} and α_{iT} are in fact slightly dependent on current density. Nevertheless (3.16) and (3.17) suffice for a first-order approximation. In the SGP model, only τ_m is available and is specified for a single operating point.

3.2.5 Parameter Extraction and Yield Analysis

Electrical characteristics of a device are represented to a simulator through a list of parameters. These parameters are extracted following a specific procedure. Each model has its own set of parameters. The method of extraction differs from one model to another.

Process variations (PVs) occur during fabrication of integrated circuits. A PV is usually caused by mechanical variations, temperature fluctuations, calibration errors and human error. Process variations alter physical state of layers forming a device. Physical changes translate to modifications in the electrical behavior of the device. Depending on the nature of a PV, it may be possible to point out which layer on an IC was altered by a PV. Also, the percentage variation of a layer for a given process is sometimes known by the process group. Ideally, this information should be used to predict the effect of PV on the overall performance of an IC. This can only be done if it is possible to quickly link the changes caused by PV to one or more parameters representing the device. An example is given for clarification.

Suppose it is known that PVs cause the doping of the internal base to vary by 5%. If the extraction method for the bipolar model is extremely efficient, the process support group should be able to link this 5% variation to the parameters representing the internal base of a transistor. A best case/worst case parameter list would then be produced and this

information would then be passed on to the IC design group. Designers would then simulate their circuits using the new parameters and determine whether or not the fluctuation in base resistance has an important consequence on the performance of their circuits. Not every type of circuit is affected by a parameter variation but should the performance of a circuit be affected the design should be modified to reduce or eliminate the effect of the process variation.

The parameters extracted for the SGPM are not properly thought-out for easy prediction of tolerances of circuits on process variations. Many parameters are either uncorrelated with each other, unrelated to the physical properties of the BJT and finally, too many act as *fitting* parameters such as in the case of (2.48). When a transistor model includes many fitting parameters it is very difficult to adjust parameters to account for process variations.

HICUM parameters relate closely to the physical aspects of a bipolar transistor. The parameter extraction method combines device measurements and equations modelling the physical properties of transistor [1]. The study of PVs on fabrication steps and their affect on HICUM's parameters will greatly improve the quality control of final products. Also, designers will have a better chance to investigate the relation between variations in HICUM parameters on the behavior of bipolar circuits.

3.3 HICUM Implementation into Libra

For this exercise, the HICUM model equations were already available from the reference simulator DEVICE [23] [24]. The implementation consisted of writing the code needed for linking these equations in a manner that is recognized by the Libra interface. Certain functions had to be completed and specific data structures had to be followed, all of which are explained in [25] and [26]. This section will give an insight on the work that was done to complete the model implementation.

The Libra simulator offers an interface allowing users to create their own circuit element models. User-defined element models are implemented by writing ANSI-C code. When properly coded, these elements can be used in linear, nonlinear, transient and convolution simulations. The interface requires two files describing the element, a *senior.ael* file and a *model.c* file.

[illegible]

Figure 3.11 Graphical Representation of the HICUM BJT in the Libra Interface

The parameter values shown are the default values. They can be modified by invoking an “Edit Item Parameter” menu. When this menu is requested, the list of parameters appears along with their respective definitions. The designer then manually changes the default values for values representing a particular transistor. The goal of the simulator is to determine the element’s external pin voltages and currents. In order to achieve this goal the topology of the equivalent circuit and the model equations must be communicated to the simulator. This information is contained in the *model.c* file.

To achieve its goal, the simulator requires all node charges (Q) and branch currents (I) and their respective derivatives, capacitances (C) and conductances (Y). These values are presented to the simulator by means of matrices.

From basic circuit theory:

$$Q_i = \sum_{j=0}^{N-1} [C_{ij} \cdot (V_i - V_j)] \quad (3.18)$$

where Q_i is the total charge on the i th node, V_i and V_j are node voltages, C_{ij} is the branch capacitance between node i and node j and N is the number of nodes in the equivalent circuit.

Similarly, a branch current is given by:

$$I_i = \sum_{j=0}^{N-1} [Y_{ij} \cdot (V_i - V_j)] \quad (3.19)$$

where I_j is the total nodal current, Y_{ij} is the conductance between nodes i and j and I_{ij} is a current source between nodes i and j .

In matrix form, (3.18) and (3.19) take on the following form:

$$\begin{bmatrix} Q_0 \\ \vdots \\ Q_{N-1} \end{bmatrix} = \begin{bmatrix} C_{00} & \cdot & \cdot & \cdot & C_{0j} \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ C_{i0} & \cdot & \cdot & \cdot & C_{N-1,N-1} \end{bmatrix} \cdot \begin{bmatrix} V_0 \\ \vdots \\ V_{N-1} \end{bmatrix} \quad (3.20)$$

and

$$\begin{bmatrix} I_0 \\ \vdots \\ I_{N-1} \end{bmatrix} = \begin{bmatrix} Y_{00} & \cdot & \cdot & \cdot & Y_{0j} \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ Y_{i0} & \cdot & \cdot & \cdot & Y_{N-1,N-1} \end{bmatrix} \cdot \begin{bmatrix} V_0 \\ \vdots \\ V_{N-1} \end{bmatrix} \quad (3.21)$$

For convergence, two conditions must apply. The first states that the sum of nodal charges must equal to zero:

$$\sum_{i=0}^{N-1} Q_i = 0 \quad (3.22)$$

The second is Kirchoff's current law stating that nodal currents must be equal to zero:

$$I_i = 0 \quad (3.23)$$

Note that (3.23) is actually true for the internal nodes only because it is applied to the transistor's equivalent circuit only and not the entire circuit in which the transistor is used. The simulator is attempting to solve for the external currents. Therefore, (3.23) must be modified as follows:

$$I_i = \begin{cases} \epsilon C & i \leq M-1 \\ 0 & i > M-1 \end{cases} \quad (3.24)$$

where M is the number of external nodes (the external nodes are listed as the first nodes) and C indicates the Complex ensemble.

Using (3.20) and (3.21) the simulator varies node voltages until (3.22) and (3.24) are satisfied. Due to lack of precision in the numeric representation in a computer, (3.22) and (3.24) are never quite satisfied. Consequently, the simulator presents a set of simulation controls that indicates when convergence is sufficiently accurate. For instance, the user may indicate the simulator to stop when the internal node currents are less than 10^{-8} Amperes. Increasing the precision will require more iterations thus increasing computation time. Trade-off between precision and computation time is always a concern.

3.3.2 Solving Convergence Problems

The implementation using the given model equations and the topology of the equivalent circuit shown in Figure 3.1 demonstrated convergence problems. Symptoms of improper convergence are either characterized by final results that are completely out of range or simply by a halt from the simulator engine. Convergence problems are caused by either discontinuities in the equations for the various currents, charges, transconductances and capacitances, by improper implementation of the equivalent circuit, or by the simulator itself. The equations are identical to those used for successful implementations of HICUM into other simulators such as Eldo and Spectre, meaning they are correct. The code was revised several times until no discrepancies were found. After numerous discussions with Farag Fattouh at Nortel and the people at HP/EEsof, it was concluded with great probability that the problems encountered were caused by the Libra interface and not by the implementation. A method for improving the convergence was proposed as a result of these discussions.

The method applied for improving convergence consisted of strategically placing small value resistors to isolate the diodes and the output current source from one another. The

Figure 3.12 HICUM equivalent circuit after modifications for improved convergence

3.3.3 Interface Restrictions

There are several restrictions with the Libra interface that either reduce the model's accuracy or increase the computation time.

The first restriction affects the minimal resistance value allowed between two connecting nodes. The interface requests a resistance of more than $10^{-8}\Omega$. Aside from the fact that this restricts the value of R_{MIN} , this affects the accuracy of the model when the user wishes to set the values of series resistances (R_{Bi} , R_{Bx} , R_{Cx} and R_E) to zero. In reality these resistances are always greater than 10^{-8} but in some instances it is desirable to set them to zero in order to evaluate their effect on a circuit's behavior or to verify the model's implementation. For instance, the internal resistance, R_{Bi} , is operating point dependent and setting it to zero will thus remove the operating point dependency.

Other commercial simulators with user-defined device interfaces such as Eldo do not pose this restriction. If a series resistance is set to zero, the simulator engine reduces the two nodes to one node. Simulation time is greatly dependent on the number of nodes in the equivalent circuit thus reducing the number of nodes is important.

The second restriction effects the implementation of the thermal network. In a proper implementation, the thermal network should be completely isolated from the equivalent circuit and the bottom node should be directly connected to a ground terminal. It is impossible to know which external pin, if any, will be connected to circuit ground. If efficient, the simulator should be able to interpret a pin label as being a ground pin. In fact, Libra offers this option but only in the harmonic balance and transient analyses but not in the small-signal analysis. To remedy this situation for the small-signal analysis, the thermal network was implemented as shown in Figure 3.13 .

Figure 3.13 Implementation of thermal network

The junction temperature which was previously defined in “Temperature Scaling and Modelling of Self-Heating” on page 36 as being the voltage at node N15 (in Figure 3.13). It must now be redefined as the voltage difference between nodes N15 and N3.

To validate the implementation, basic simulation results of the HICUM-Libra implementation were compared to the HICUM implementation in the DEVICE [23] simulator. Some results are presented in Appendix C. The reference transistor is a one emitter stripe bipolar transistor with an emitter width of $0.5\mu\text{m}$ and emitter length of $5\mu\text{m}$. Depending on the operating conditions, the HICUM-Libra implementation shows some deviations from the reference. The cause of those deviations are unknown but could be a result of the modifications brought to the equivalent circuit discussed in the previous sections.

In the next chapter, a Power Amplifier is designed using the newly implemented HICUM model and the SGPM. Results will show that both models give different design values.

Chapter 4

Power Amplifier Design

The PA design intended for this thesis is to be implemented using a Silicon IC technology as opposed to the more common approach using MMIC technology. The main goal of this design exercise is to prove that HICUM may be utilized for designing PAs. Through every step of the design, simulations are done using the Libra simulator and using both the HICUM model and the SGP model. Thus, values of certain components incorporated in the design will be chosen according to the simulation results arising from using both bipolar models.

The second most important goal is to maximize the on-chip integration of the various components of a PA circuit. According to the future trends of wireless communications, the ideal PA would have all of its components integrated on one die. These components, as shown in Figure 4.1 , consist of:

- i) Blocking capacitors for isolation of DC currents at the RF input and output ports.
- ii) RF isolation for isolation of the RF signal from the DC power supply and DC base biasing circuitry.
- iii) Input and output matching elements to provide the necessary reflection coefficients at the RF ports.

iv) Biasing circuitry to provide self-biasing at the base of the amplifying transistor.

Figure 4.1 Basic block diagram of the Power Amplifier

4.1 Class of Operation

The PA is configured to operate in Class A. Classes of Operation for PAs are discussed in [27] and [28]. In brief, a Class of Operation is defined according to the length of the conduction angle of the amplifying transistor. During Class A operation the amplifying transistor is conducting for the total cycle of the input signal, thus the conduction angle is of 360° . In a Class B configuration, the amplifying transistor would be conducting for half of the input signal's cycle (180°) whereas in Class C, D, E and F configurations, the amplifying transistor would be conducting for less than half of the cycle.

The differences resulting from the various classes of operation are seen by the maximum power available at the output of the PA and the efficiency of the PA. Theoretical efficiency

versus conductance angle of the amplifying transistor are plotted in Figure 4.2 . Efficiency is defined as:

$$eff = \frac{P_{out}}{P_{DC}} \cdot 100 \quad (4.1)$$

where P_{out} is the power delivered to the load and P_{DC} is the power drawn from the power supply.

Figure 4.2 Efficiency versus conductance angle (y) for various class of operation [28]

In modern portable communication systems, it is estimated that the PA is responsible for approximately 90% of the total power consumption [29]. Consequently, maximum power efficiency is desirable to maximize battery lifetime. According to Figure 4.2 , the Class A configuration has the lowest efficiency of all Classes, with a maximum theoretical efficiency of 50%. Recent publications, [30] for example, have shown that it is possible to reach efficiencies as high as 65% using the higher Classes of operation. Class A operation was chosen for this research. since it is simple to design and utilizes the BJT in all of its

operating regions. The PA design for this exercise has no intention of competing against high efficiency PAs.

4.2 Bipolar Technology

A 0.5 μ m self-aligning double-poly bipolar technology was used for the PA design. Bipolar devices were chosen for the transmitter because of their superior power handling and speed when compared to MOS devices. The generic features of double-poly bipolar technology are:

- polysilicon base contact to minimize collector-base capacitance
- an emitter self-aligned to the extrinsic base to minimize base resistance

There are two figures of merit that are commonly used to describe the performance of a BJT. These are gain-bandwidth frequency (f_T), which is the frequency where the short-circuit gain $|h_{fe}(\omega)|$ approximates unity, and maximum frequency of oscillation (f_{max}), which is the frequency where the maximum available power gain of the transistor is equal to 1. The npn bipolar devices used in this thesis have an expected maximum f_T of 25 GHz and f_{max} of 30 GHz.

The process is intended for low power applications such as digital circuitry. This contradicts the requirement for relatively powerful PA applications, where a high power handling process is a definite asset. Since present and future wireless system applications require relatively low transmit power - in the order of hundreds of milliwatts [29] - it has been postulated, that a low power process may suffice for the design of the output stage of a radio. The usage of a low power process would be beneficiary since the PA could be integrated on the same IC along with the low power counterpart of the radio.

The IC technology also offers resistors, capacitors and inductors. Whereas integrated resistors and capacitors are well known, the use of on-chip inductors is a relatively new concepts in IC design and have proven to be prominent components in RF analog circuits [31], [32]. As discussed later in this chapter, inductors are used in PA circuit applications as matching elements and in resonant tanks.

4.3 Design Steps

The schematic of the PA to be designed for this thesis is presented in Figure 4.3 . The design procedures followed to produce the component values in Figure 4.3 are discussed in this section. It is important to note that at the beginning of the design we assume ideal inductors and capacitors and an ideal voltage or current source for the biasing of the base of the amplifying transistor. This assumption is acceptable because parasitics associated to a component are proportional to the frequency of operation and the nominal value of the component. Thus, until the nominal value of the component is known, the parasitics associated to the component are unknown.

Figure 4.3 Schematic of the Power Amplifier

4.3.1 DC Biasing for Class A operation

Biasing for Class A operation implies that the transistor always conducts current for any reasonable input signal amplitude. Figure 4.4 defines the different operating regions of a transistor. A load-line was traced to show the movement of the bias point during an ideal AC operation. The term ideal is important because, as it will be seen in section 4.3.5.2, the AC load-line is not likely to be a straight line due to the non-linearities introduced by the BJT during an actual AC operation.

Figure 4.4 Operating regions of a transistor

When V_{CE} reaches a certain “low” threshold the transistor enters the saturation region and when V_{BE} reaches a “low” threshold, the transistor enters the cut-off region. If either of these regions are reached, the transistor behaves as an extremely non-linear device and the output waveform is no longer a duplicate of the input signal with some gain. In view of this, it is apparent that for maximum output power with low distortion the Class A amplifier must be biased in the center of the active region, or at mid-rail.

The DC output characteristics of the Q_{PA} device, collector current (I_C) versus collector-emitter voltage (V_{CE}) for various base currents (I_B), are plotted in Figure 4.5 to help choose the DC bias point of the device.

A load-line was superimposed on the DC output characteristics. The coordinates of the load-line were chosen to best describe the operation of the PA, knowing the power supply

voltage, the basic circuit configuration and the maximum output power required by the specifications.

Figure 4.5 DC output characteristics for Q_{PA} ($V_{BE}/V = 0.88 - 0.98$)

The first coordinate of the load-line (label X in Figure 4.5) is given by the maximum collector-emitter voltage (V_{CE}) during AC operation. As shown in Figure 4.3, the design makes use of an inductor (L_{ro}) between the collector and a 3V power supply. Assuming an ideal inductor, the impedance of the inductor is $Z_{Lro} = j\omega L_{ro}$. During DC operation ($\omega = 0$), the voltage drop across the inductor is zero and the voltage at the collector is thus 3V. Therefore, during DC operation, the inductor has no effect on the behavior of the amplifier. The advantage of inserting an inductor between the collector and the power supply becomes apparent during the AC operation. During AC operation, the self-inductance of the inductor causes the collector voltage to double its DC value, resulting in a maximum collector voltage of 6V (label X in Figure 4.5). This design method thus results in a doubling of the maximum output voltage swing.

The second coordinate of the load-line is established by the DC bias point of the amplifier. As explained in the previous paragraph, the collector-emitter voltage for DC operation is of 3V. The collector current is a function of the emitter area of Q_{PA} . The transistor chosen for this exercise has an emitter size of $120\mu m$. For the technology employed, maximum f_T is achieved at current densities between $0.6mA/\mu m^2$ to $0.7mA/\mu m^2$. Consequently, the biasing current is limited by:

$$0.6mA/\mu m^2 \cdot 120\mu m^2 = 72mA \leq I_C \leq 84mA = 0.7mA/\mu m^2 \cdot 120\mu m^2 \quad (4.2)$$

A collector current of 80mA is thus chosen. The coordinates of label Y are thus $V_{CE} = 3.0V$ and $I_C = 80mA$.

4.3.2 Estimation of Maximum Output Power

Maximum output power is given by:

$$P_{out,max} = \frac{1}{2} \cdot V_{swing} \cdot I_C \quad (4.3)$$

and V_{swing} is given by:

$$V_{swing} = \min[(V_{CC} - V_{sat}), (V_{AC,max} - V_{CC})] \quad (4.4)$$

where $V_{sat} = 200mV$, is the saturation voltage of a BJT, $V_{CC} = 3V$, is the DC collector-emitter voltage and $V_{AC,max} = 6V$ is the maximum AC collector-emitter voltage. Thus V_{swing} is approximately 2.8V.

Solving for $P_{out,max}$ gives:,

$$P_{out,max} = \frac{1}{2} \cdot 2.8V \cdot 0.080A = 112mW = 20.5dBm$$

4.3.3 Automatic Base Biasing Circuit.

To strengthen the philosophy of single chip integration, the PA includes an automatic base biasing circuitry. The circuitry is composed of two subcircuits: the current mirror and the RF isolation circuit.

4.3.3.1 Current mirror derivation

If we neglect the effect of the RF isolation circuitry between Q_B and Q_{PA} for the DC analysis of the biasing circuitry, the circuit reduces to Figure 4.6 where R_{EB} and R_{EPA} are the parasitic emitter resistors (R_{Ex} in Figure 3.1) of transistors Q_B and Q_{PA} , respectively.

Figure 4.6 Current mirror analysis

The voltage at the base of both transistors is given by:

$$V_B = \left(I_{REF} - \frac{I_{CPA}}{\beta_{PA}} \right) \cdot R_{EB} + V_{BEB} \quad (4.5)$$

The voltage at V_{EPA} is given by:

$$V_{EPA} = V_B - V_{BEPA} = \left(I_{REF} - \frac{I_{CPA}}{\beta_{PA}} \right) \cdot R_{EB} + V_{BEB} - V_{BEPA} \quad (4.6)$$

The collector current of Q_{PA} is given by:

$$I_{CPA} = \frac{\beta_{PA}}{\beta_{PA} + 1} \cdot I_{EPA} = \frac{\beta_{PA}}{\beta_{PA} + 1} \cdot \frac{V_{EPA}}{R_{EPA}} \quad (4.7)$$

where β_{PA} is the DC current gain of the transistor. Substituting (4.6) into (4.7) gives:

$$I_{CPA} = \frac{1}{R_{EPA}} \cdot \frac{\beta_{PA}}{\beta_{PA} + 1} \cdot \left[\left(I_{REF} - \frac{I_{CPA}}{\beta_{PA}} \right) \cdot R_{EB} + V_{BEB} - V_{BEPA} \right] \quad (4.8)$$

For the technology employed, β is approximately equal to 120. Consequently,

$$\frac{\beta_{PA}}{\beta_{PA} + 1} \rightarrow 1 \quad (4.9)$$

and

$$\frac{I_{CPA}}{\beta_{PA}} \rightarrow 0 \quad (4.10)$$

Equation (4.8) can thus be simplified to:

$$I_{CPA} = \frac{1}{R_{EPA}} [R_{EB} \cdot I_{REF} + V_{BEB} - V_{BEPA}] \quad (4.11)$$

Assuming $V_{BEB} \approx V_{BEPA}$,

$$I_{CPA} = \frac{R_{EB}}{R_{EPA}} \cdot I_{REF} \quad (4.12)$$

It is advantageous to minimize I_{REF} as much as possible in order to minimize the current drawn from the power supply. Any current drawn from the power supply increases P_{DC} in (4.1), thus reducing the total efficiency of the PA. The emitter area of Q_B is chosen to be one sixth the size of Q_{PA} because this transistor is actually made of six identical transistors in parallel.

The next step consists of calculating R_{REF} which will produce the proper I_{CPA} . Applying Kirchhoff's voltage and current laws to Q_B gives:

$$V_{CC2} = R_{REF} \cdot I_{REF} + R_{EB} \cdot \left(I_{REF} - \frac{I_{CPA}}{\beta_{PA}} \right) + V_{BEB} \quad (4.13)$$

Solving for R_{REF} gives,

$$R_{REF} = \frac{1}{I_{REF}} \cdot \left[V_{CC2} - V_{BEB} - R_{EB} \cdot \left(I_{REF} - \frac{I_{CPA}}{\beta_{PA}} \right) \right] \quad (4.14)$$

Table 4.1 summarizes the design variables needed to solve (4.14). Since both emitters are connected directly to ground, R_{E1} and R_{E2} are simply the parasitic resistors of each transistor. Substituting in (4.12) and (4.14) gives:

$$I_{REF} = 13.33 \text{ mA} \quad (4.15)$$

and

$$R_{REF} = 150 \Omega \quad (4.16)$$

VARIABLE	VALUE
V_{CC2}	3.0 V
A_{PA}	$120 \mu\text{m}^2$
A_B	$20 \mu\text{m}^2$
I_{CPA}	80 mA
V_{BEB}	0.94 V
β_{PA}	120
R_{EB}	1.828Ω
R_{EPA}	0.3046Ω

Table 4.1 Design variable for the current mirror

4.3.3.2 RF Isolation

The purpose of RF isolation circuitry is to isolate a DC source from an RF signal, while allowing a DC current to flow. Two methods for providing RF isolation were investigated. The first being an LC resonant tank, resonating at the PA's centre frequency and the second being a single inductor to form an RF Choke. In theory, both methods are capable of producing infinite impedances although in practice, process limitations add design restrictions, resulting in finite impedances for both methods. The method producing the highest impedance will therefore be chosen. The PA in this design requires two RF isolation circuit, one between the current mirror and the base of Q_{PA} and one between the V_{CC1} and Q_{PA} . In this section, the circuitry between the current mirror and the base of Q_{PA} is discussed and the other is identical.

The first method to be investigated is the resonant tank as shown in Figure 4.7. The impedance (Z_{π}) as by the RF signal is (without the presence of R_p):

$$Z_{rt} = L_{rb} \parallel C_{rb} + R_c \parallel C_{di}$$

$$Z_{rt} = \frac{j\omega L_{rb}}{1 - \omega^2 L_{rb} C_{rb}} + \frac{1}{1/R_c + j\omega C_{di}} \quad (4.17)$$

Figure 4.7 Resonant tank and decoupling capacitor configuration

The denominator of the first term in Z_{rt} indicates that for given values of L_{rb} and C_{rb} , there is a frequency for which Z_{rt} will produce an infinite impedance. Setting the denominator to zero and solving for ω gives:

$$\omega = 2\pi f = \sqrt{\frac{1}{L_{rb} C_{rb}}} \quad (4.18)$$

We can thus find the necessary values for L_{rb} and C_{rb} which will produce an infinite impedance at the RF frequency ($f = 1.9$ GHz). Solving for L_{rb} and C_{rb} yields:

$$L_{rb} C_{rb} = \frac{1}{(2\pi f)^2} \quad (4.19)$$

Setting $L_{rb} = 2$ nH and solving for C_{rb} gives:

$$C_{rb} = \frac{1}{L_{rb}} \cdot \frac{1}{(2\pi f)^2} = \frac{1}{2E-9} \cdot \frac{1}{(2\pi \cdot 1.9E9)^2} = 3.51 \text{ pF} \quad (4.20)$$

So far, no attention was paid to the parasitics associated to the resonant tank. Indeed, the inductor and the capacitor have resistive losses attributed to them. These inherent losses are modelled using R_p in Figure 4.7 . Rewriting (4.17) to include R_p in the resonant tank gives:

$$Z_{rt} = \frac{j\omega L_{rb}}{1 - \omega^2 L_{rb} C_{rb} + \frac{j\omega L_{rb}}{R_p}} + \frac{1}{1/R_C + j\omega C_{di}} \quad (4.21)$$

The Quality factor (or Q factor) of an inductor or capacitor is a figure of merit indicating the amount of resistive loss. The equivalent R_p associated to an inductor and a capacitor knowing the Q each element is given by,

$$R_{pL} = (\omega L) \cdot \frac{(Q_L^2 + 1)}{Q_L} \quad (4.22)$$

and

$$R_{pC} = \frac{1}{\omega C} \cdot \frac{(Q_C^2 + 1)}{Q_C} \quad (4.23)$$

respectively. It was said at the beginning of this chapter that the parasitics associated to a component are somewhat unknown until the value of the component is known. At this point it is possible to calculate the resistive parasitics associated to L_{rb} and C_{rb} because their nominal values and the frequency of operation are known. Using the technology specifications data sheets, the Q factors for L_{rb} and C_{rb} for an operating frequency of 1.9GHz were found to be 7 and 20 respectively. Substituting these values in the above two equations yields:

$$R_{pL} = 171\Omega \quad \text{and} \quad R_{pC} = 479\Omega \quad (4.24)$$

The total parasitic resistance (R_p) is the parallel combination of R_{pL} and R_{pC} , thus

$$R_p = 126\Omega \quad (4.25)$$

Since we have set $L_{rb}C_{rb} = 1/\omega^2$ in (4.19), we can simplify (4.21) to give the impedance at the center frequency:

$$Z_{rt} = 126 + \frac{1}{1/R_C + j\omega C_{di}} \quad (4.26)$$

The presence of R_p changes dramatically the impedance seen by the RF signal at the input of the resonant tank. The impedance is no longer infinite at 1.9GHz and a small portion of the RF signal will flow through the resonant tank.

The function of C_{di} is to form a low impedance to ground for any RF signal leaking through the resonant tank. Without C_{di} , leakage current will flow through R_C and will corrupt the power supply with RF noise. Thus, C_{di} is added to form a low impedance path directly to ground. The impedance of a capacitor is given by:

$$Z_C = \frac{1}{j\omega C} \quad (4.27)$$

According to (4.27), the higher the value of C_{di} , the lower the impedance. Information about the process used for this design indicates that capacitor values should not exceed 10pF to assure good yield. Thus, setting C_{di} to 10pF gives:

$$Z_{C_{di}} = \frac{1}{j\omega C_{di}} = -j8.37\Omega \quad (4.28)$$

$Z_{C_{di}}$ is indeed much less than R_C in (4.14) thus most of the RF leakage current will flow through the ground terminal as opposed to the power supply terminal.

The method for RF isolation using an inductor as an RF Choke is shown in Figure 4.8 .

Figure 4.8 RF Choke configuration

The impedance (Z_{rfc}) as seen by the RF signal is:

$$Z_{rfc} = R_S + j\omega L_{rfc} + \frac{1}{1/R_C + j\omega C_{di}} \quad (4.29)$$

Equation (4.29) indicates that as $L_{rfc} \rightarrow \infty$, then $Z_{rfc} \rightarrow \infty$. Unfortunately, process specifications limit the maximum size of inductors to approximately 10nH with $Q_L \approx 2$.

The series parasitic resistance due to the Q-factor of an inductor is given by:

$$R_S = \frac{\omega L}{Q_L} \quad (4.30)$$

Setting $L_{rfc} = 10\text{nH}$ and $\omega = 2\pi \cdot 1.9\text{E}9 \text{ rad/sec}$,

$$Z_{rfc} = 60 + j119 + \frac{1}{1/R_C + j\omega C_{di}} \quad (4.31)$$

and the decoupling capacitor, C_{di} , is set to 10pF as in (4.27).

Comparing (4.26) and (4.31), shows that the impedance seen by the RF signal is larger when the RF Choke method is used. The forward transconductances (Y_{21}) of both isolation circuitries were simulated and results are presented in Figure 4.9. The resonant tank has the highest Y_{21} at the centre frequency and has a narrowband response meaning it is prone to frequency shifts if the LC elements deviate from their nominal values. The RF Choke has a relatively flat frequency response and the lowest Y_{21} . It was therefore chosen for the final design.

Figure 4.9 Y_{21} for the resonant tank (RT) and RF choke (RFC)

4.3.4 Small Signal Analysis

With the operating point determined, the circuit is ready for the small signal analysis. Two types of analysis are performed, stability and small signal matching. Since both analyses depend greatly on the behavior of the Q_{PA} , thus the bipolar model, simulations are done

using both models. For this exercise it is assumed that the PA is driven by a 50Ω source and the output of the PA is driving a 50Ω load. The analysis starts with the stability of the circuit.

4.3.4.1 Stability Considerations

The stability of a two port device is characterized with the K-factor and the B-factor [33]: Two conditions suffice for unconditional stability. They are:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \quad (4.32)$$

and

$$B = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \quad (4.33)$$

where S_{11} , S_{12} , S_{21} and S_{22} are the S-parameters of the two-port network and $|\Delta|$ is the determinant of the S-matrix,

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}|. \quad (4.34)$$

Stability is verified for frequencies between 100MHz and 10GHz. The PA, as it was designed in the previous sections is presented in Figure 4.10 . Libra requires that the input and output ports be DC isolated. Consequently, DC blocking capacitors, C_{dci} and C_{dco} , were inserted in series with the input and output ports. Since their values are relatively high, they have no impact on the circuit's behavior at high frequencies. Using both bipolar models, the circuit in Figure 4.10 was simulated. Results, presented in Figure 4.11 , show that the circuit is unstable for frequencies above 300MHz, with K less than 1.

Figure 4.10 PA Configuration for small signal analysis

Figure 4.11 Stability and small-signal s-parameters for Figure 4.10

By inspection of (4.32) and the S-parameters of the circuit (Figure 4.11 (a)), two methods were found to significantly improve the stability.

According to (4.32), increasing the K-factor is achieved by decreasing S_{21} . The gain of an amplifier can be reduced by adding negative feedback. Many methods of producing negative feedback exist and the method chosen for this design is collector feedback. A series RC network is added between the base and the collector of Q_{PA} as shown in Figure 4.12 . By properly choosing values for R_f and C_f the gain roll-off of Q_{PA} is decreased. The impedance of the series RC network is given by:

$$Z_{fb} = R_f - j\frac{1}{\omega C_f} \quad (4.35)$$

The RC network's transfer function is a high-pass filter. For low frequencies, the branch has a high impedance due to the capacitor, thus $I_f \approx 0$. For higher frequencies, the capacitor has a low impedance and the impedance of the branch is basically R_f . The overall effect is an impedance in parallel with the transistor's Miller Capacitance. The Miller Capacitance (C_M) is the total capacitance between the base and the collector of the transistor as shown in Figure 2.4 for the SGPM and in Figure 3.1 for HICUM. If R_f is large enough, then the effect of the series RC network at high frequencies is negligible compared to C_M .

Figure 4.12 Collector feedback network

The series RC network adds a zero to the total transfer function of Q_{PA} . According to (4.35), the frequency of the zero is given by

$$f = \frac{1}{2\pi} \cdot \frac{1}{R_f C_f} \quad (4.36)$$

This corner frequency must be less than the frequency at which S_{21} peaks, therefore less than $f=0.4\text{GHz}$ according to Figure 4.12 (a).

Simulation results presented in Figure 4.13 were done with $R_f = 500\Omega$ and $C_f = 10\text{pF}$, thus,

$$f = \frac{1}{2\pi} \cdot \frac{1}{R_f C_f} = 0.031\text{GHz} \quad (4.37)$$

Figure 4.13 Stability and small signal s-parameters after collector feedback

The RC network improved the stability of the circuit for frequencies between 0.3GHz and 0.6GHz. The stability for frequencies above 0.8 GHz is unchanged since S_{21} remained the

same. At high frequencies the impedance of the RC network is larger than the transistor's base to collector capacitance.

The stability for high frequencies is achieved by improving S_{11} and S_{22} . According to Figure 4.13 (b), S_{11} degrades rapidly towards unity (0dB). This has an important impact on the K-factor. S_{11} is improved by adding 2Ω resistors (R_{par1} and R_{par2} in Figure 4.14) in series with the input and output. When the PA design is finalized, the 2Ω resistors will be absorbed by the parasitic resistors attributed to the metal lines and the Q-factors of the elements in the matching networks.

Figure 4.14 PA Configuration after stability compensation

Simulations of the stability factors and the S-parameters for the circuit in Figure 4.14 were done and results are presented in Figure 4.15. The circuit is stable for frequencies between 100MHz and 10 GHz.

Figure 4.15 Stability and small signal s-parameters after collector feedback and R_{par}

4.3.4.2 Simultaneous Conjugate Match

The matching networks at the input and the output will be optimized for maximum output power. Maximum output power is achieved when the matching networks are designed for maximum power transfer between the input source and the input of the PA and the output of the PA and its load. This form of matching is commonly referred as *simultaneous conjugate match*.

Consider the diagram of Figure 4.16. The input and output reflection coefficient of a transistor amplifier are given by [33]:

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (4.38)$$

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \quad (4.39)$$

Figure 4.16 Definitions of Reflection Coefficients

Simultaneous conjugate match, or maximum power transfer is achieved when

$$\Gamma_S = \Gamma_{IN}^* \quad (4.40)$$

and

$$\Gamma_L = \Gamma_{OUT}^* \quad (4.41)$$

Consequently, for simultaneous conjugate match, (4.38) and (4.39) become:

$$\Gamma_S = \left[S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right]^* \quad (4.42)$$

$$\Gamma_L = \left[S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right]^* \quad (4.43)$$

According to the above equations, Γ_S is dependent on Γ_L and vice-versa. A special case occurs, referred as unilaterality, when S_{12} is set to zero, in which case (4.42) and (4.43) reduce to S_{11} and S_{22} respectively. When S_{12} is set to zero the design procedure is much simpler. The error involved in assuming $S_{12} = 0$ is derived in [33] and is given by:

$$\frac{1}{(1+U)^2} < \mathcal{E} < \frac{1}{(1-U)^2} \quad (4.44)$$

where

$$U = \frac{|S_{12}||S_{21}||S_{11}||S_{22}|}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \quad (4.45)$$

is referred as the *unilateral figure of merit*.

Table 4.2 presents the simulated s-parameters for the circuit in Figure 4.14 . Inserting these numbers in (4.44) gives

$$-1.9dB < \mathcal{E}_{HICUM} < 2.4dB \quad (4.46)$$

with the HICUM model, and

$$-1.8dB < \mathcal{E}_{SGPM} < 2.2dB \quad (4.47)$$

for the SGP model. Since the error is larger than 0.5 dB, unilaterality should not be assumed.

S-parameter	HICUM	SGPM
S_{11}	0.8833 $\angle$ -176	0.8604 $\angle$ -172°
S_{12}	0.0194 $\angle$ 7°	0.0205 $\angle$ 3°
S_{21}	4.3583 $\angle$ 109°	6.1129 $\angle$ 119°
S_{22}	0.5720 $\angle$ 181°	0.4542 $\angle$ 174°

Table 4.2 Small-Signal S-parameters for f=1.9 GHz

Designing a simultaneous conjugate matched amplifier for the bilateral case requires solutions for Γ_S and Γ_L which satisfy (4.42) and (4.43). If Γ_{MS} and Γ_{ML} represent Γ_S and Γ_L for simultaneous match, then solutions for (4.42) and (4.43) are:

$$\Gamma_{MS} = \frac{B_1 - \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \quad (4.48)$$

$$\Gamma_{ML} = \frac{B_2 - \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \quad (4.49)$$

where

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \quad (4.50)$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \quad (4.51)$$

$$C_1 = S_{11} - \Delta S_{22}^* \quad (4.52)$$

$$C_2 = S_{22} - \Delta S_{11}^* \quad (4.53)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (4.54)$$

Inserting the numbers from Table 4.2 into (4.48) - (4.53) gives:

$$\Gamma_{MS_{HICUM}} = 0.9387 \angle 171^\circ \quad \Gamma_{MS_{SGPM}} = 0.9237 \angle 168^\circ \quad (4.55)$$

$$\Gamma_{ML_{HICUM}} = 0.7441 \angle 144^\circ \quad \Gamma_{ML_{SGPM}} = 0.6389 \angle 130^\circ \quad (4.56)$$

Figure 4.17 presents Γ_{MS} and Γ_{ML} on a Smith Chart. The location of the points on the Smith Chart are as expected. The input and output impedances of a BJT are always capacitive thus the conjugate match requires an inductive impedance. Two configurations exist for matching to 50Ω , a series L - shunt C matching network or a series C - shunt L matching network. The latter is the most convenient because the series C serves two purposes.

When external components are an option, the DC blocking capacitors (C_{dci} and C_{dco} in Figure 4.14) are not part of the matching networks but part of external circuitry. One of the goals of this exercise is to maximize the integration of the various design elements for a possible integration of the PA with other modules on a common IC. Consequently, it would be an asset to have the DC blocking capacitors as part of the PA. In the series C - shunt L matching network configuration, the series C element will act as a DC blocking capacitor thus external DC blocking capacitors will not be required.

The trajectories traced by Γ_{MS} and Γ_{ML} for a series C - shunt L matching network are shown by the arcs in Figure 4.17 . When a series C is added, the trajectories follow the constant impedance circle until the admittance unit circle is crossed. The shunt L then follows a trajectory along the admittance unit circle until the normalized 50Ω point is reached.

The resulting component values are given in Table 4.3 and the frequency response is presented in Figure 4.18 .

PORT	COMPONENT	HICUM	SGPM
INPUT	C_{mi}	12.5 pF	10.1 nF
	L_{mi}	0.86 nH	1.08 nH
OUTPUT	C_{mo}	12.5 pF	7.14 pF
	L_{mo}	2.18 nH	3.47 nH

Table 4.3 Component values for the matching networks

Figure 4.19 presents the complete PA design. In the following section, the operation of the PA under large signal operation is discussed.

Figure 4.17 Input and output reflection coefficients on a Smith Chart

Figure 4.18 Small signal s-parameters versus frequency after matching

Figure 4.19 Complete Design with matching networks

4.3.5 Large Signal Analysis

A BJT's large signal behavior is somewhat different from its small signal behavior. Many of the lumped elements in the equivalent circuits of Figure 2.4 and Figure 3.1 are voltage or current dependent. Small signal analysis solves the model equations for the given DC operating point, then AC operation is assumed under the same conditions as the DC. In many circuit applications, the signal swing is relatively small, thus small signal analysis is considered sufficiently accurate. However, during the operation of a PA, the signal swings are large and small signal operation can no longer be assumed. Two types of large signal analysis are viewed in this section: gain, compression point and power added efficiency and the dynamic load-line (DLL) of the Q_{PA} BJT. Definitions and simulation results for the two types of analyses are given and a discussion about the variations in the simulation results will follow.

It is important for the reader to note that the HICUM implementation into the Libra simulator demonstrates convergence problems under large signal operation. When the signal swings become too large, usually soon after the 1 dB compression point, the simulator loses convergence. Consequently, the extent of the large signal analyses with the HICUM model is limited and simulations of the large-signal s-parameters were impossible to achieve. The HICUM results presented are for the maximum signal swings permitted by the implementation.

4.3.5.1 Gain, 1dB Compression Point and Power Added Efficiency

There are three commonly known gain definitions [33]:

$$\text{Transducer Gain, } G_T = \frac{P_L}{P_{AVS}} \quad (4.57)$$

$$\text{Power Gain, } G_P = \frac{P_L}{P_{IN}} \quad (4.58)$$

$$\text{Available Gain, } G_A = \frac{P_{AVN}}{P_{AVS}} \quad (4.59)$$

In this chapter, the power gain, G_P , is verified because it takes into account the matching networks.

The gain of an amplifier compresses as the input power is increased beyond a certain threshold [27]. An important figure of merit for a PA is its 1dB compression point. As the name indicates it, the 1dB compression point is a measure of the output power when the gain decreases by 1dB below its small signal gain.

Power added efficiency is defined as:

$$PAE = \frac{P_{OUT}}{P_{DC}} \times 100 \quad (4.60)$$

where P_{OUT} is the RF power at the output of the PA and P_{DC} is the power drawn by the DC power supply, including the power needed for the biasing circuitry.

These figures of merit were simulated using the SGP model and the HICUM model. Simulations using the HICUM model were done with both avalanche and self-heating effects because the small signal matching was done with these options. Simulation results are presented in Figure 4.20 and Figure 4.22 .

Figure 4.20 P_{out} , G_p and PAE versus P_{in} with the SGPM

Figure 4.21 P_{out} , G_p and PAE versus P_{in} with HICUM (without avalanche and self heating)

Figure 4.22 P_{out} , G_p and PAE versus P_{in} with HICUM (with avalanche and self heating)

4.3.5.2 Dynamic Load Line

The dynamic load line (DLL) analysis investigates the large signal behavior of the quiescent point (or bias point) formed by the collector current (I_C) and collector-emitter voltage (V_{CE}) of the Q_{PA} BJT. In Figure 4.5, the AC load line was drawn as a straight line but in actual AC operation, the I_C - V_{CE} characteristics form elliptical contours around the quiescent point. Simulation results using the SGP model are presented in Figure 4.23 while Figure 4.24 to Figure 4.27 present HICUM results with and without avalanche and self heating effects to verify the importance each option.

Elliptical contours are formed as a result of the currents generated by the various capacitances ($i = C \cdot \frac{dV}{dt}$) inside the BJT. Therefore, the widths of the elliptical contours define the amount of imaginary output impedance for a given BJT.

The Libra dynamic load line test bench and PA circuit used for the dynamic load line analysis are presented in Appendix A. Libra executes two types of simulations. The first is an harmonic balance simulation for given DC bias conditions and input drive. The I_C - V_{CE} characteristics at each sampled time point for a complete signal cycle are plotted. The second is a DC analysis, where the biasing at the base of Q_{PA} is varied, by varying the voltage source controlling the current mirror (V_{CC2} in Figure 4.14).

Figure 4.23 Dynamic Load Line with the SGPM

Figure 4.24 Dynamic Load Line with HICUM (without avalanche and self heating)

Figure 4.25 Dynamic Load Line with HICUM (avalanche only)

Figure 4.26 Dynamic Load Line with HICUM (self-heating only)

Figure 4.27 Dynamic Load Line with HICUM (no self heating in current mirror)

4.3.5.3 Discussion

It is difficult to deduce any conclusive results from the gain and efficiency versus input power analysis (Figure 4.20 - Figure 4.22) due to the absence of HICUM simulations beyond compression. Some results can be compared and are presented in Table 4.4. As discussed in Chapter 3, self-heating causes an increase in the bias current. This results in a 6% disagreement in the PAE of the power amplifier at the 1dB compression point. This difference is expected to be larger if the amplifier was simulated far beyond the compression point which unfortunately can not be proven due to the convergence problems with the HICUM implementation.

MODEL	OPTIONS (no NQS in all case)	G _P (dB)	P _{1dB} (dBm)	PAE (%) (at P _{1dB})
SGPM	-	22.5	19.5	23
HICUM	no avl. and S.H.	22.0	17.5	15
	complete	22.0	18.5	16.3

Table 4.4 Large signal simulation data for SGPM and HICUM

Important comparison data for the DLL analyses are presented in Table 4.5 . The relative widths of the ellipses are given using the following formula:

$$W_{relative} = \frac{W_{HICUM}}{W_{SGPM}} \quad (4.61)$$

The SGPM predicts a bias collector current of 98mA whereas HICUM predicts a collector current between 80mA and 100mA. The fact that the SGPM predicts a higher bias current than the basic HICUM model is due to improper modelling of the high current region discussed in Chapter 3 (i.e.: Figure 3.6).

The DLL of Figure 4.25 shows that avalanche generation has no important impact on the large signal behavior of the PA. This is easily explained by comparing the nature of the DLL and the nature of the avalanche generation. The DLL shows that when V_{CE} is high, I_C is low (label A in Figure 4.25) and when I_C is high, V_{CE} is low (label B in Figure 4.25). The avalanche generation occurs when both V_{CE} and I_C are high. Since this is never the case in the present application, the avalanche process has no impact.

When self-heating is modelled, the bias current increases by approximately by 35%. This increase in bias current pulls the DLL away from the cutoff region. If this increase in bias current was the only parameter affected by self-heating, the P_{1dB} would also increase. Results in Table 4.4 show that with self heating the P_{1dB} increases by no more than 0.5

dBm. The justification for such behavior is given by the 40% increase in the width of the ellipse. Because the ellipse is wider, the DLL enters the cut-off region at a lower V_{CE} . In fact, the best case DLL would consist of a linear DLL, with the DLL entering the cutoff region at nearly 6V. The worst case would consist of a circular DLL, with the DLL entering the cutoff region at 3.0V.

MODEL	HICUM OPTIONS (no NQS in all case)	I_C (mA)	WIDTH RATIO OF ELLIPSES for $P_{IN} = -5\text{dBm}$
SGPM	-	98	1
HICUM	no avl., no S.H.	80	1.71
	avalanche	80	1.71
	self heating	100	2.38
	self heating in Q_{PA} only	110	2.38

Table 4.5 DLL data for SGPM and HICUM

It is interesting to observe the increase in bias current when the self-heating for current mirror is removed (see Figure 4.27). This change in current is easily explained with the use of (4.13). When self-heating is applied to the current mirror, the collector current increases. A larger voltage drop occurs across R_C , which in turn reduces the voltage drop across the base-emitter diode of both transistors. This indicates that the self-heating in the current mirror gives some degree of compensation to reduce the negative effect of self-heating in Q_{PA} .

In the next chapter, we will see how parasitics affect the performance of the PA and we will discuss methods used either to take advantage of the parasitics or to minimize their effects.

Chapter 5

Layout and Packaging Issues

The layout of PA circuits necessitates special attention and does not follow the same layout techniques and practices as for conventional low power circuits. Minimum design rules are rarely followed but rules concerning maximum power and current handling must always be verified. The latter are not automatically verified by the layout software package. Instead, the layout designer must manually verify each critical area in the layout to assure that all dimensions conform to technology specific maximum current handling rules.

The layout was done using the simulation results of the HICUM model and is presented in Figure 5.1 . The layer legend along with an enlarged view of the basic bipolar transistor used for the layout are given in Appendix B.

The IC architecture and its packaging introduces parasitics which can not be neglected at RF frequencies. These parasitics affect major design issues of PAs such as biasing, gain and input and output matching. In order to achieve the simulated results previously shown in this chapter, these parasitics must either be eliminated or incorporated as part of the design, such as in the matching networks.

Important layout and packaging issues are overviewed without discussing any proprietary information about the IC technology and without discussing a specific packaging format. Instead, these issues are discussed in general terms to help the novice PA designer.

Figure 5.1 Layout (dimensions: 1.9mm x 1.3mm)

5.1 Transmission Line Effects

If the wavelength of the RF signal is comparable to the length of a signal path in the layout, then transmission line effects need to be taken into consideration. The wavelength of a signal is given by:

$$\lambda = \frac{c}{\sqrt{\epsilon_r} \cdot f} \quad (5.1)$$

where $c=3.0E8$ m/s is the speed of light in free space, $\epsilon_r = 11.9$ is the relative dielectric constant for silicon [37] and $f=1.9E9$ GHz is the frequency of the RF signal. Inserting these number in (5.1) yields:

$$\lambda = 46mm$$

The die size for the PA is less than 2mm on a side. Assuming no signal path must contour any large element, which is a reasonable assumption since three layers of metal are available, all signal paths are less than 2mm in length. Compared to the wavelength of the RF signal, the signal paths are much shorter thus transmission line effects can be neglected.

5.2 Parasitics

Resistive and capacitive parasitics due to metal lines are relatively low in IC design and can easily be incorporated within the design without too many difficulties. For instance, the resistive parasitic of the METAL1 layer was strategically used to form R_{par1} and R_{par2} in Figure 4.19. The capacitive parasitic of these metal lines was subtracted from C_{MI} and C_{MO} respectively.

Bonding inductances are parasitics introduced by the short *bonding* wire which connects the pads to the packaging. The value of inductance is dependent on the length of the wire, thus dependent on the type of packaging employed. Typical values are in range of 0.8nH to 1nH or approximately 0.8 nH/mm.

Bonding inductance must be carefully taken into account in the design of the matching networks. According to Table 4.3 , the matching inductors have specific values and are of relatively low values. These inductors will be connected to ground through a bond pad and consequently to a bond wire. The equivalent circuit is shown in Figure 5.2 . The shunt capacitor, C_{pad} , is relatively small and can be neglected at RF.

Figure 5.2 Matching inductance, bond pad and bond wire equivalent circuit

Since both the matching inductor and the bonding inductance are in series, the total inductance is the sum of both inductances. According the Table 4.3 , matching inductors (L_{mi} and L_{mo}) may be less then the bond inductance The result is an inductive impedance which is higher than what is required. To reduce the total inductance, a capacitor is added in series with the matching inductance as shown in Figure 5.3 .

Figure 5.3 Addition of a series capacitor

The total impedance is given by:

$$Z = j\left(\omega(L_m + L_{bond}) - \frac{1}{\omega C_{series}}\right) \quad (5.2)$$

and Z is the impedance required by the design, $Z = j\omega L'$, where L' is taken from Table 4.3 . Inserting this into (5.2) and solving for C_{series} gives:

$$C_{series} = \frac{1}{\omega^2 \cdot (L_m + L_{bond} - L')} \quad (5.3)$$

The on-chip inductor, L_m , is taken from an inductor library and C_{series} is calculated accordingly. Since the value of L_{bond} is not precisely known, a good tactic is to calculate C_{series} for worst case and best case L_{bond} . In the layout, multiple capacitors are laid out in parallel as shown in Figure 5.1 . With the use of micro-surgery, connections between capacitors are cut to enable some degree of manual tuning.

The most crucial parasitics are those located between the emitter of Q_{PA} and the ideal ground. They have great impact on the voltage gain of a common emitter amplifier given by:

$$G = \frac{Z_C}{Z_E + R_e} \quad (5.4)$$

where Z_C is the total impedance connected to the collector, Z_E is the total impedance connected to the emitter and R_e is the emitter resistance of the BJT. Before taking the parasitics into account Z_E was null since the emitter was connected to an ideal ground. When layout and packaging parasitics are taken into consideration, Z_E is given by:

$$Z_E = R_{line} + j\omega L_E \quad (5.5)$$

where R_{line} is the resistance due to the sheet resistance of the metal lines connecting the BJT to the bond pads and L_E is the bonding inductance due to the bond wires between the bond pads and ground.

Figure 5.4 presents simulation results when inductance is added between the emitter of Q_{PA} and ground. It appears as though the design can not tolerate more than 0.1nH of emitter inductance to maintain an appreciable gain. Although the effect of bonding inductance is unavoidable, it can be reduced by connecting the emitter of Q_{PA} to multiple output pads and by keeping the bond wires as short as possible. Multiple pad connections result in multiple inductors in parallel, thus decreasing the total inductance seen from the emitter of Q_{PA} . The reduction in inductance is not directly dependent on the number of pads due to coupling between each bond wire. Although coupling is dependent on the spacing between each bond wire, a good rule of thumb for estimating the total bonding inductance is

$$L_E = \frac{L_{bond}}{\sqrt{n}} \quad (5.6)$$

where n is the number of bond wires.

Figure 5.4 Emitter inductor (L_E) effect on S_{21}

The impact of R_{line} is not quite as important for the frequency behavior as it is for the DC biasing. When the current mirror was analyzed, the derivations of (4.12) and (4.14) did not assume any R_{line} . Of the two equations, (4.12) is the most sensitive to R_{line} . Rewriting (4.12) to include R_{line} gives:

$$I_{CPA} = \frac{(R_{EB} + R_{lineB})}{(R_{EPA} + R_{linePA})} \cdot I_{REF} \quad (5.7)$$

To keep the I_{CPA} at the designed value, the layout of both metal paths to ground must be done in order to assure the ratio of six. Therefore,

$$R_{lineB} = 6 \cdot R_{linePA} \quad (5.8)$$

The resistance of a metal line is given in terms of sheet resistance ($\rho \Omega/\text{square}$), where square indicated a square piece of the metal line of any dimension. Therefore to calculate

R_{line} , the physical line is divided into a series of square pieces and the sum of these squares are multiplied by ρ :

$$R_{line} = \rho \cdot \sum squares \quad (5.9)$$

It is important to note that in order for (5.8) to be true, the physical dimensions of both lines need not to be identical but the sum of squares must. To minimize the effect of R_{linePA} for the AC behavior, in (5.4) for example, METAL3 which has the least sheet resistance is used to connect Q_{PA} to the bond pads.

5.3 RF Choke

On-chip inductors are formed with the METAL3 layer and rely on the coupling of the magnetic field between the metal tracks to produce inductance. The coupling is dependent on track spacing and track width. Wider tracks have less coupling, thus present lower value inductors.

The Q_{PA} transistor is biased at approximately 100mA. This implies that a current of 100mA will flow through the RF choke between the collector of Q_{PA} and the power supply. According to the maximum current handling specifications of METAL3, the required metal line widths for this RF choke is in the order of 50 μ m. A metal line of this width will not produce a sufficiently high impedance inductor. Therefore, the RF choke between the collector of Q_{PA} and V_{CC1} will be added as an off chip component.

5.4 Other Considerations

Due to the temperature sensitivity of a BJT, (5.7) is true only if both transistors operate at identical ambient temperatures. In a practical application, it is intuitive to say that the

temperature on a die varies from one location to another. For instance, the maximum temperature gradient will be near the Q_{PA} transistor. From Figure 4.26 and Figure 4.27, it was seen that the bias point of Q_{PA} is less sensitive to a rise in temperature if Q_B is also influenced by the rise in temperature. Consequently, it is important to position Q_B as close as possible to Q_{PA} , as shown in Figure 5.1. In addition to a better temperature behavior, placing Q_B near Q_{PA} assures better matching characteristics between the transistors.

Since the transistors in this design are significantly large, important quantities of currents will be injected through the substrate. These currents could easily cause unwanted feedback mechanisms and affect the performance of the PA. It is therefore important to collect substrate currents by forming low impedance paths in the substrate. This is achieved by routing PDEV paths strategically with connections to pads (i.e.: pads labelled SUB_G3 and SUB_G5 in Figure 5.1). The impedance of the paths is further reduced by connecting the PDEV layer to the METAL1 layer.

Chapter 6

Conclusion

6.1 Summary

This thesis gave a description of two bipolar transistor models. The first was a conventional model known as the Spice Gummel Poon Model. This model is used extensively in most commercial circuit simulators. It is a known fact that the SGPM lacks in accuracy when modelling modern bipolar technologies. A new model, HICUM, was developed to overcome the problems of the SGPM. The HICUM model was overviewed with special attention paid to the model options pertaining to the simulation of Power Amplifier circuits.

In the scope of this thesis, the HICUM model was implemented in Libra (copyright of HP/EEsof Software Inc.). Libra is an Harmonic Balance simulator which is more suitable for RF design than Time Domain simulators such as HSPICE. Unfortunately, the implementation is not fully operational and shows convergence problems in certain operating regions. Nevertheless, the implementation can be used for not-so-large signal drives in simulations of Power Amplifier circuits.

In Chapter 4, a Class A medium power PA was designed using the SGPM and the newly implemented HICUM model. Simulation results were presented and differences between both models were discussed. Results showed differences between both models. More

significant differences are expected in large signal simulations (i.e. large-signal s -parameters) but the present HICUM-Libra integration did not allow to do so.

6.2 Future Work

The first recommendation for future work is solving the convergence problems in the HICUM-Libra implementation for large signal operation. This will require much cooperation with the people supporting the HP/EEsof interface. A good starting point is an extensive discussion with the people who have implemented the HICUM model in other commercial simulators and who have encountered similar problems.

Finally in order to realize the full potential of the HICUM model, simulation results using both the SGPM and the HICUM model must be compared to measured results. This exercise was to be done in the course of this thesis but due to unforeseen problems in the fabrication of the test circuit it was not possible. When the test circuit was laid out, poly capacitors were used. Since the process was not fully matured, it required a few changes during the last few months. One of these changes consisted of replacing poly capacitor by metal capacitors. Due to a lack of communication between the process group and the designer, the original layout was not modified to reflect this change in the fabrication of capacitors. The end result is an open circuit between the two stages of a two stage Class A power amplifier.

If a simulation-measurement comparison study was to be successfully accomplished, two important procedures must be followed. The first consists of fabricating the actual test circuit next to parameter extraction test structures. This will assure a good correlation between the extracted parameters modelling the BJTs in the test circuit and the actual behavior of the circuit, therefore eliminating batch to batch variations, of even wafer to wafer variations.

The second procedure to follow consists of fully characterizing the IC packaging. It was seen in Chapter 5 that packaging introduces parasitics that alter the behavior of a PA. These parasitics must be carefully taken into account in the simulations.

By following both of these steps, any discrepancies between simulation and measurement could be attributed with great certainty to the modelling of the BJT.

Appendix A

Libra Test Benches

Figure A.1 Test bench for dynamic load-line

Figure A.2 PA circuit of Dynamic load-line

Figure A.3 Large signal s-parameter test bench

Appendix B

Layout Layer Legend and Close-up

Figure B.4 Layer legend for all layouts

Figure B.5 Close-up on 2 of BJTs forming Q_{PA}

Appendix C

HICUM-Libra Versus HICUM-Device

Figure C.6 Internal base-emitter junction charge (Q_{jei}) and capacitance (C_{jei}), $T=300$ K

Figure C.7 Internal base-collector junction charge (Q_{jci}) and capacitance (C_{jci}), $T=300$ K

Figure C.8 Transfer current (I_t) and its forward transconductance (S_f), $T=300\text{K}$

Figure C.9 Forward transit time (T_f) and minority charge (Q_f), $T=300$ K

Figure C.10 Internal diffusion capacitance (C_{dei}) and internal base resistance (R_{bi}), $T=300$ K

Figure C.11 Gummel plot for the complete transistor at $V_{CE} = 3.0V$. Note: (1) The high current deviation for $T=400K$ is thought to be caused by the linearization of the C_{10} parameter for high temperatures in DEVICE. (2) The low current deviation for $T=300K$ and $T=400K$ is thought to be caused by numerical errors in Libra (recombination in HICUM-Libra is not implemented).

Figure C.12 Avalanche generation at $V_{BE} = (0.75, 0.77, 0.78)$ V.

Figure C.13 Self-heating at $V_{BE} = (0.80, 0.825)$ V. For this figure, $C_{th} = 3 \times 10^{-8} \text{Ws/K}$, $R_{th} = 3000 \text{K/W}$ and $T = 300 \text{K}$.

Figure C.14 Y_{11} versus frequency. For this figure, $al_{it}=0.45$ and $al_{qf}=0.225$.

Figure C.15 Y_{21} versus frequency For this figure, $al_{it}=0.45$ and $al_{qf}=0.225$.

References

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- [1] M. Schröter, "TRADICA - A program for dimensioning and calculation of integrated bipolar transistors", Manual Version 4.1, Ruhr University Bochum, June 1994.
 - [2] M. Schröter, "Bipolar transistor modelling for integrated circuit design", Graduate Course, Carleton University, Ottawa, 1995.
 - [3] J.J. Ebers and J.L. Moll, "Large-Signal Behavior of Junction Transistors", Proc. IRE, Vol. 42, pp. 1761-1772, 1954.
 - [4] H. K. Gummel and H.C. Poon, "An integral charge control model of bipolar transistors", Bell Systems Technical Journal, Vol. 49, pp. 827-852, May 1970.
 - [5] P. Ashburn, *Design and Realization of Bipolar Transistors*, John Wiley & Sons Ltd, 1988.
 - [6] Antognetti and G. Massobrio, *Semiconductor Device Modelling with SPICE*, McGraw-Hill, 1988.
 - [7] I. E. Getreu, *Modelling the Bipolar Transistor*, Elsevier, Amsterdam, 1978.
 - [8] J. M. Early, "Effects of Space-Charge Layer Widening in Junction Transistors", Proc. IRE, Vol. 40 , pp. 1401-1406, November 1952.
-

-
- [9] Farid Najm, "VBIC95: An improved Bipolar Transistor Model", *Circuits & Devices*, March 1996.
- [10] McAndrew et al., "VBIC95, The Vertical Bipolar Inter-Company Model", *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 10, pp. 11-15, October 1996.
- [11] M. Schröter and H.-M. Rein, "A compact physical large-signal model for high-speed bipolar transistors including the high-current region" (in German), NTG meeting, Würzburg, Mai 1986.
- [12] H. Stübing and H.-M. Rein, "A compact physical large-signal model for high-speed bipolar transistors at high current densities - Part I: One-dimensional model", *IEEE Trans. Electron Dev.*, Vol. 34, pp. 1741-1751, 1987.
- [13] H.-M. Rein and M. Schröter, "A compact physical large-signal model for high-speed bipolar transistors at high current densities - Part II: Two-dimensional model and experimental results", *IEEE Trans. Electron Dev.*, Vol. 34, pp. 1752-1761, 1987.
- [14] M. Schröter and H.-M. Rein, "A compact physical large-signal model for high-speed bipolar transistors with special regard to high current densities and two-dimensional effects", (in German), Dissertation, Ruhr-University Bochum, Bochum, Germany, Jan. 1988.
- [15] M. Schröter and H.-M. Rein, "Transit time of high-speed bipolar transistors in dependence on operating point, technological parameters, and temperature", *Proc. IEEE Bipolar Circuits and Technology Meeting, Minneapolis*, pp. 85-88, 1991.
- [16] M. Schröter and H.-M. Rein, "Simulation and modelling of the low-frequency base resistance of bipolar transistors in dependence on current and geometry", *IEEE Trans. on Electron Devices*, Vol. 38, pp. 538-544, 1991.
-

-
- [17] H.-M. Rein, "Multi-Gigabit-Per-Second Silicon Bipolar IC's for Future Optical-Fiber Transmission Systems", *IEEE Journal of Solid-State Circuits*, Vol 23, No 3, pp. 664-675, 1988.
 - [18] A. Koldehoff, M. Schröter, and H.-M. Rein, "A compact bipolar transistor model for very-high-frequency applications with special regards to narrow emitter stripes and high current densities," *Solid-State Electronics*, vol. 36 pp. 1035-1048, 1993.
 - [19] J. TeWinkel, "Extended Charge-Control model for bipolar transistors", *IEEE Trans. on Electron Devices*, Vol. 20, pp. 389-394, 1993.
 - [20] M. Schröter and H.-M. Rein, "Investigation of very fast and high-current transients in digital bipolar IC's using both a new compact model and a device simulator", *IEEE Journal of Solid-State Circuits*, Vol. 30, No 5, pp. 551-562, May 1995.
 - [21] C.C. McAndrew, "A complete and consistent electrical/thermal HBT model", *IEEE Bipolar and BiCMOS Circuits and Technology Meeting*, Minneapolis, pp. 217-220, 1992.
 - [22] R. L. Pritchard, *Electrical Characteristics of Transistors*, McGraw-Hill Book Company, Totonto, 1967.
 - [23] M. Schröter, *DEVICE - A Program for Numerical Simulation of Three-Dimensional Heterostructure Semiconductor Devices with Inclusion of External Circuit Elements*, Ruhr-University Bochum AG Halbleiterbauelemente, May 1993.
 - [24] M. Schröter, *HICUM - An accurate physical bipolar compact transistor model*, Documentation of BNR/NT - Version 1.00, August 1995.

-
- [25] *HP EEsof High-Frequency Design Solutions - User-Defined Elements*, Hewlett Packard Series IV User Manual, Release 6.0, July, 1995.
 - [26] *HP EEsof High-Frequency Design Solutions - Circuit Network Items*, Hewlett Packard Series IV User Manual, Release 6.0, July, 1995.
 - [27] T. Varelas, "A Monolithic BiCMOS Power Amplifier for Low Power Digital Radio Transmitter", Thesis, Carleton University, 1992.
 - [28] H.L. Krauss, C.W. Bostian and F.H. Raab, "Solid State Radio Engineering", John While & Sons, 1980.
 - [29] A. Abidi, "Low-power radio-frequency IC's for portable communications", Proceedings of the IEEE, 1995.
 - [30] Tirdad Sowlati et al., "Low Voltage, High Efficiency GaAs Class E Power Amplifiers for Wireless Transmitters", IEEE Journal of Solid-State Circuits, Vol. 30, No. 10, pp. 1074-1080, October 1995.
 - [31] J.R. Long, M. Copeland, "Modelling, Characterization and Design of Monolithic Inductors for Silicon RFICs", Digest of Technical Papers, ISSC, February 1996, San Francisco, CA
 - [32] M. Frchette, "LNA and Mixer Design Study for 900 MHz Receiver Applications", Thesis, Carleton University, 1996.
 - [33] G. Gonzalez, *Microwave Transistor Amplifiers Analysis and Design*, Pretice-Hall Inc., 1984.

-
- [34] Kenneth S. Kendert et al., "Simulation of Nonlinear Circuits in the Frequency Domain", IEEE Transactions on Computer-Aided Design, Vol. CAD-5, No. 4, pp. 522-535, October 1986.
- [35] Chris Bowick, *RF Circuit Design*, Sams Publishing, 1993.
- [36] M. Schröter and D. Walkey, "Physical Modeling of Lateral Scaling in Bipolar Transistors", IEEE Journal of Solid-State Circuits, Vol 31, No. 10, pp. 1484-1492, October 1996.
- [37] D. M. Pozar, *Microwave Engineering*, Addison Wesley, 1990.